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Final Project Work

Evaluation of a high-temperature technology for aerospace applications

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In the following I prefer to switch in Italian because I wish everyone could read it.
Un ringraziamento particolare va ai miei genitori, alla mia fidanzata e a mia zia Katia, i quali mi sono stati vicino e mi hanno supportato durante questa esperienza che mi ha portato a stare lontano da casa. Il ringraziamento a questi ultimi si estende, aggiungendo il resto della mia famiglia, a tutto il periodo di conseguimento di laurea, percorso non privo di difficoltà, nel quale mi hanno supportato e aiutato a raggiungere l'obiettivo.

Summary

Figure's summary

Introduction

In the scope of circuits facing severe environments, it is complex to find CMOS technologies able to reach performances and power consumption needs. High temperature dramatically increases leakage and limits circuit performances. Certain applications have to operate beyond the melting point of many materials used in commercial electronics.

Traditionally, engineers had to rely on active or passive cooling when designing electronics that must function outside of normal temperature ranges, but in some applications, cooling may not be possible or it may be more appealing for the electronics to operate hot to improve system reliability or reduce cost. Robust electronics for harsh environments are essential for the exploration and exploitation of new energy supplies, production processes to conserve natural resources or to improve energy efficiency in automotive and aerospace. These environments have extreme temperatures, vibration, pressures and moisture levels, among other stressful factors.

Conventional electronics built for consumer products have amazing functionality but cannot withstand these harsh industrial environments [1]. Manufacturing semiconductors for these environments presents a number of challenges. As temperature goes above 175°C, many aspect of silicon processes, material properties, and design constraints change, and the availability of companion components is severely limited. A broad range of integrated circuits (ICs) have been developed using Silicon on Insulator (SOI) CMOS technology, for aircraft engines, turbine power-generation engines, and down-hole drilling tools that measure pressures, vibrations, chemical parameters, stress and similar parameters. The ICs perform the same basic functions as today's commercial electronics, including digital, analog and mixed signals devices. The products allow electronic systems to be developed and implemented in environments that cannot be supported by commercial electronics. ICs are packaged in ceramic through-hole packages to survive the rugged environment.

At high temperatures, the overriding limitation for semiconductors is leakage current of the individual transistors. The largest part of the solution comes from use of a SOI CMOS in place of bulk CMOS. SOI greatly reduces the amount of leakage current in the IC, which impacts all types of designs. In digital designs, the large number of devices on an IC can create excessive power consumption and reduce performance. Analog designs will tend to lose resolution for measuring and controlling very small signals. There are two main leakage paths to address: the larger one is leakage from drain to the silicon substrate, and there is a smaller component of leakage from the drain to the source. With bulk CMOS, there is a large area directly from the drain to the source. This leakage path is eliminated when using SOI CMOS. The silicon dioxide (SiO_2) insulates the drain from the bulk substrate. The difference is illustrated in **Figure 1**.

To further reduce the leakage current, modifications are made to the transistors to shift the threshold voltage (V_T). By increasing the V_T, the transistor stays in its off state and

reduces leakage at high temperatures until a higher voltage is applied. With the combination of SOI CMOS and shifting V_T, designers can achieve a reduction in leakage current of three order of magnitude compared to standard bulk CMOS at 250°C. For the analog circuits, it improves the stability of linearity over temperature.
Another technique used to improve performance and reduce leakage current is to balance the P-channel and N-channel devices, relative to leakage current. The objective is to match the values and minimize the new current.

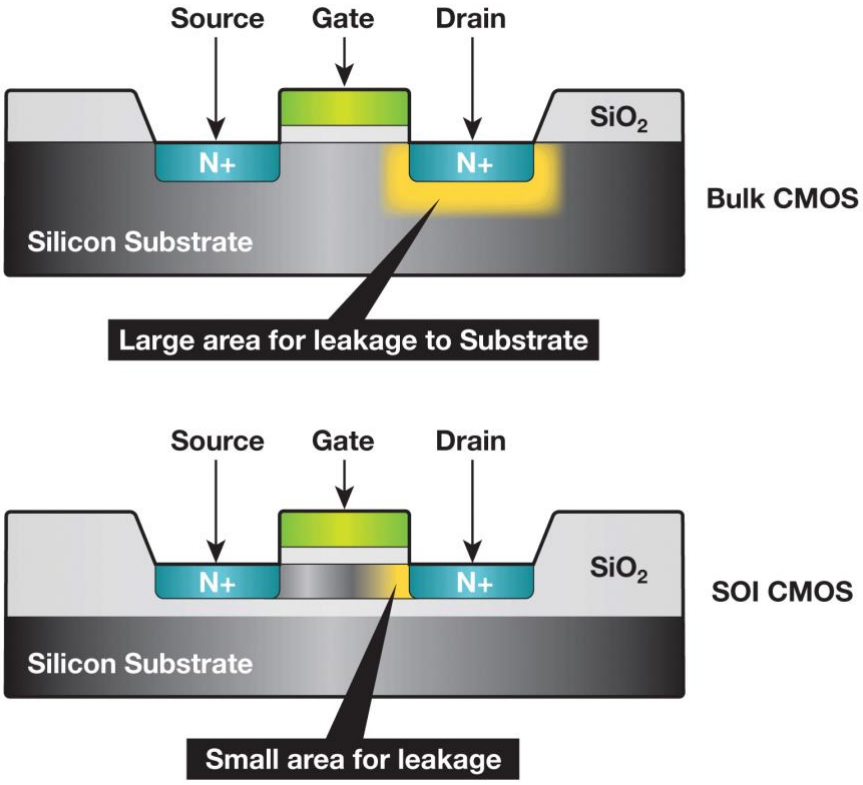


Figure 1: Leakage-current paths bulk CMOS and SOI CMOS

Continuous operation at temperature above 150°C places a number of unique constraints on the materials commonly used for assembling and packaging a high temperature IC. Some of the specific items are that must be managed are:

- Consideration of interconnect conductors: Different materials are used, within the IC, based on their resistivity and their electromigration. Aluminum is used on IC interconnect traces and tungsten on vias.
- Decreased electrical resistance of insulation materials causing additional leakage: The leakage current between pins of ceramic packages at temperatures below 150°C are usually negligible. At higher temperatures, the levels can become significant. They can become high enough to become issues with sensitive analog inputs.

- Increased chemical and metallurgical activity within and between materials: One of the main areas of focus here is the gold and aluminum interface. Over time and high temperature, the inter-metallic bond changes characteristics. Most of the ICs have aluminum pads and the packages have gold pads. The selection of wire joining the two is crucial to operation at high temperatures.
- Stability of adhesives: Traditional die attach adhesives such as epoxies are not stable at temperatures above approximatively 150°C. Alternative high-temperature adhesives, such as Cyanate Esters, must be qualified and used in high temperature applications.

There are a number of reliability characteristics which need to be addressed to achieve a long-life operation before the device breakdown. The high temperature impacts the lifetime of materials and changes their characteristics. These are associated the current in the conductors (electromigration) and voltage applied to insulators (gate oxide).
These include:

- Electromigration: This phenomenon is the actual moving of atoms to the point where open circuits can occur due to the current in traces. Adequate conduction material in the interconnect is used to compensate for the inevitable atomic migration during the lifetime of the circuit. Barrier metals are also used between metal and silicon to slow the migration.
- Time-Dependent Dielectric Breakdown (TDDB): This is a long-term failure mechanism in the gate oxide of MOSFETs. It is a result of long-time application of relatively low electric field (as opposite to immediate breakdown, which is caused by electrostatic discharge, ESD). It is accelerated by high temperature. Although this does not require a specific modification to the process, special screening processes are implemented to be sure processing impurities do not impact long-term reliability.

As you build the high-temperature IC into a full design, external factors bring new constraints. The designer must address three main factors:

- What are the temperature zones of the system?
- What functions are required in each zone?
- Do components exist to support the design?

At this point my contribution starts, we aim to evaluate a high temperature technology for our performance needs and check, by simulation, if we can reach our specifications. The considered technology is the X-FAB XT018 that is a platform specifically designed for a next generation automotive, industrial and medical applications operating in the temperature range of -40°C to 175°C; however, our target is 250°C and more. In a first phase of this internship, the objective was to estimate the behavior of the technology depending on frequency, voltage and temperature. This step consists in estimating the technology performances, by electrical simulations of classical structures: firstly, we simulated a ring oscillator, a very simple and fast circuit, but not accurate, to which we correlated the silicon results in order to highlight simulations and test discrepancies;

then, after the ring oscillator, we used fan-out of 4 and critical path replica circuits, even them simple circuits but much more accurate.
Then, in a second time, power reduction techniques were evaluated and proposed to optimize performances.
Finally, as mentioned before, after developing some simple devices on silicon, we tested them to compare the results obtained from the tests and the ones obtained during the simulation phase.

1 High-temperature applications

The hostile environment we are considering is high temperature; high temperature, for electronic, commonly means above 125°C.
Sensing and control are the main reasons for placing electronics in hostile environments. Placing sensors and electronics in, or in close proximity to, the environments or processes that they are monitoring allows more accurate measurements to be made, as well as lighter, faster, and more accurate control systems. The functions to be performed are sensing, signal amplification, signal conditioning and processing, and energizing electrical actuators. In many applications, these functions will need to be performed with high accuracy and reliability over a wide temperature range in order to add value. Some applications may be satisfied by a sensor and amplifier in the hostile environment with higher order functions performed in low-temperature ambient. The more challenging applications will require a sensor, precision amplifiers and analog-to-digital converters, power amplifiers, and power supply to operate in the hostile environment.

1.1 Downhole drilling application

Figure 2: Downhole drilling

The oldest, and currently largest, user of high-temperature electronics is the downhole oil and gas industry [2]. In this application, the operating temperature is a function of the

underground depth of the well. Worldwide, the typical geothermal gradient is 25°C/km depth, but in some areas, is greater. Originally, drilling operations have been done in a temperature range of 150°C up to 175°C, but running out reserves of natural resources, that are of easy access in addition to the advances obtained thanks to the new technologies, have motivated the industry to drill deeper, as well as in regions of the world with a higher geothermal gradient. Temperatures in these hostile environments can exceed 200°C, with pressures greater than 25kpsi. Active cooling techniques are not effective when the heating is not confined to the electronics. The importance of system reliability is crucial, as the cost of downtime due to equipment failure can be quite severe. A failed electronics assembly on a drill equipment, operating miles underground, can take more than a day to find and replace, for instance the average cost for operating a complex deep-water offshore rig is of the order of $1M per day. Today, conventional electronics are used in these applications by enclosing them in a dewar. Dewars and associated data loggers are a well-developed work-around for the high-temperature environment. However, if a properly working set of components were available in a broad range of temperature with respect to the previous one, there would be interest by these industries.

1.2 Avionic application

Figure 3: Aircraft engine with electronic controls

Besides the oil and gas industries, other applications, such avionics, are emerging for high-temperature electronics [3]. Electronic sensors and controls are used in jet engines and might be embedded in the skins of supersonic aircraft. For high performance military applications, the sensors, signal conditioning, and computers used in jet engines are cooled to below 125°C using the aircraft's fuel or putting them in remote location. In commercial aircraft, the electronics are positioned in manner to be air cooled. Due to the high temperatures in jet engines, many sensors are located remotely from the real points to be checked, for example hydraulic fluid pressure sensors at the ends of isolation tubes. High temperature sensors and signal processing electronics could increase aircraft

reliability and performance by providing better response in turbine controls, and by eliminating the weight of cooling systems and high-performance cabling. Even an important company like NASA is interested in replacing hydraulic aircraft controls with electrical controls, the so-called *fly by wire*. Supersonic flight also heats sensors in some areas of the aircraft skins. This is the case of the hypersonic cruise missiles investigated in the 1970's, which were expected to reach skin temperatures of >350°C. A next generation of turbine controls is being developed using electronics that will operate at up to 300°C. There are presumably additional applications that could be addressed with 600-800°C devices. The Air Force, Office of Naval Research, NASA, GE, and United Technologies have funded research for this application for many years. The HSCT, acronym of High Speed Civil Transport, for supersonic flight is being considered by NASA, Boeing, McDonnell-Douglas, Pratt & Whitney, and others. Controls are being contemplated for engine inlets that must operate in the 180-250°C range. Failures in electronics and cabling are one of the largest maintenance items in the supersonic Concorde. High-temperature electronics might be an enabling technology for HSCT. Aerospace is a real and fairly substantial market for the 21st century; due to the fact that aerospace is a high-value market, the improvements in fuel efficiency, reliability, or safety can justify substantial investment in controls.
Nowadays, the aviation industry has a growing movement toward the "more electric aircraft", so called MEA. Part of this initiative seeks to replace traditional centralized engine controllers with distributed control systems. The encountered problem using centralized control is that it requires large, heavy wire harnesses with hundreds of conductors and multiple connector interfaces, while, moving to a distributed control scheme it is possible to place the engine controls closer to the engine, reducing the interconnections complexity, saving hundreds of pounds of aircraft weight, and increasing the system reliability. The tradeoff, however, is that the ambient temperature, in close proximity to the engine, ranges from -55°C to +200°C. Although electronics can be cooled in this application, it is undesirable for two reasons:

- cooling adds costs and weight to the aircraft;
- failure of the cooling system could lead to failure of the electronics that controls critical systems.

Another aspect introduced by the MEA initiative is utilizing power electronics and electronic controls instead of hydraulic systems, in order to improve reliability and reduce maintenance costs. The control electronics ideally need to be very close to the actuators, which produce a high ambient temperature environment.

1.3 Automotive application

The automotive industry provides another emerging application for use of high-temperature electronics. As with avionics, the auto industry is migrating from purely mechanical and hydraulic systems to electromechanical or mechatronic systems. This requires locating sensors, signal conditioning, and control electronics closer to the heat

sources. Sensors and associated signal-conditioning electronics are very important in automotive applications. Apparently, the largest number of automotive applications under consideration are for temperatures of less than 250°C. Some experts of this application claim that 180-200°C is the highest temperature of real interest, with the exception of antilock brake sensors in the 250°C range. However, combustion sensors or sensors at the inlet of a catalytic converter could be very hot, up to 1000°C. For this specific and other sensors are required devices which the lifetime is of about 3000 hours with very high reliability and which can support wide and frequent temperature cycles.

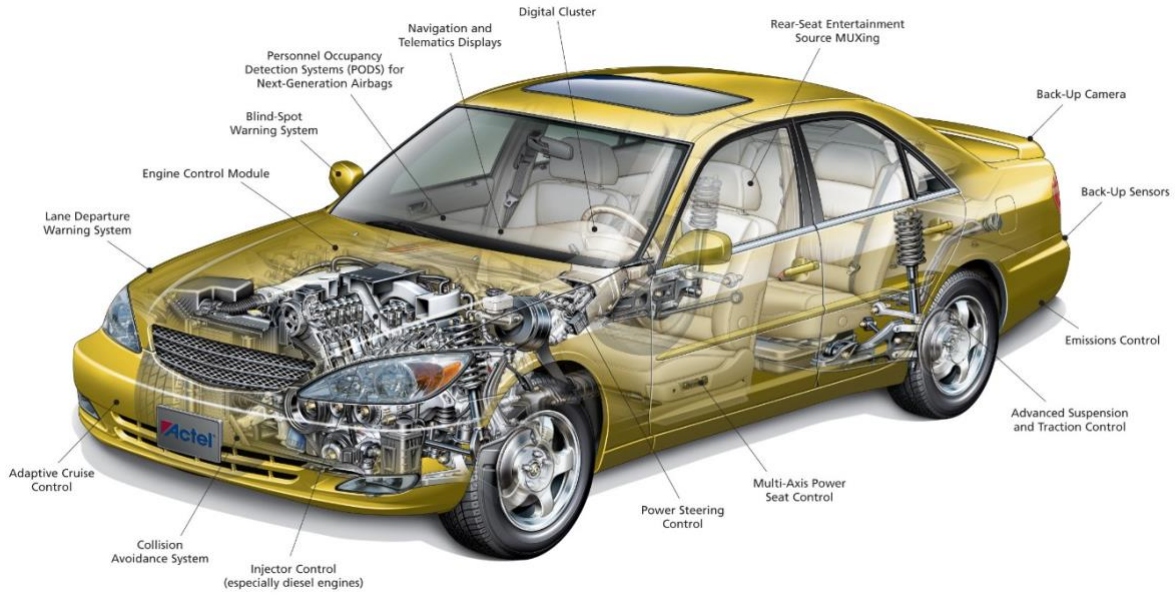


Figure 4: Electronics in automotive

The market size of the sensors to be applied in conventional or internal combustion engines for the automotive market, is very difficult to quantify and, probably, is very price sensitive. However, with around 15 million automobiles and light trucks produced each year in the US alone, this could be a very large market. The potential of reducing pollution and improving fuel economy by the usage of more precise sensors and controls might justify the relatively moderate price components.

The maximum temperature and exposure time varies by vehicle type and location of the electronics of the vehicle, then the higher integration of electrical and mechanical systems, such as collocation of the transmission and transmission controller, could simplify the manufacture, test, and maintenance of automotive subsystems. Another example is the one of electric vehicles and hybrid-electrics that require power electronics with high energy density for converters, motor controls, and charging circuits, all devices associated to high temperatures.

1.4 High-temperature electronic device technologies

In the past, high temperature electronics designers were compelled to use standard temperature components well above their rated specification due to the unavailability of high-temperature integrated circuits. Some standard-temperature ICs will indeed work at elevated temperatures, but it is an arduous and risky effort to use them. During the design phase, engineers must identify potential critical candidates, completely test them and characterize performance over temperature, and qualify the reliability over a long period of time. Performance and lifetime of the part are often substantially degraded.
This a challenging, expensive, and time-consuming process, below the main steps explanation:

- Qualifying components needs testing in a lab oven with a high-temperature printed-circuit board (PCB) and fixtures, for at least as long as the mission profile requires. It is difficult to accelerate testing because new failure mechanism may be encountered. Failures during testing require another iteration of component selection and long-term test, delaying project timelines.
- Operation outside of data sheet specifications is not guaranteed, and performance may vary between component lots. In particular, IC process changes can result in unexpected failures at temperature extremes.
- Plastic packages are only robust up to 175°C with reduced operating life. Near this temperature limit, it can be difficult to distinguish between a packaging-related failure and silicon-related failure without costly and time-consuming laboratory failure analysis. Availability of standard components in ceramic packages is not so common.
- Often, components used in harsh environments must survive not only high temperature but also severe shock and vibration. Many engineers prefer to use packages with leads because they provide a more robust attachment to the PCB. This further limit device selection, as other industries trend toward smaller, leadless packages.
- It could be desirable to obtain parts in die form, especially if a component is otherwise only available in a plastic package. The die can then be repackaged in a high-temperature compliant hermetic package or multichip module. However, of the few components that will work at elevated temperature, yet a smaller subset is readily available as tested dice.
- Due to time constraints and test-equipment limitations, engineers in the industry may tend to restrict qualification of a device to a specific application circuit, without covering all key device parameters, thus limiting component reuse for other projects without further testing.
- Key non-data-sheet IC properties, such as electromigration in metal interconnections, could lead to failures at high temperatures.

In the last years, the newer IC technology has produced some specific devices capable to operate reliably at elevated temperature guarantying data sheet specifications compliance. All of this has been possible thanks to the reached advantages in process technology, circuit design, and layout techniques.
Managing many key device characteristics is crucial for successful, high-performance operation at elevated temperatures. One of the most important and well-known challenges is posed by increased substrate leakage current. Although standard silicon can operate well beyond the military requirement of 125°C, leakage in standard silicon processes doubles for every 10°C increase, making it unacceptable for many precision applications.
High-temperature electronics development is a system problem, not just a problem for discrete and integrated circuit semiconductor devices. As temperature increase, materials degrade: this is the case of polymers and solders that melt or break down. While development of semiconducting devices that operate at high temperature may be the most challenging aspect of the problem, the market for high-temperature semiconductors will also be limited by the availability of system solutions. Semiconductor die must be attached to packages and wirebonded to leads. These packages must then be attached to high-temperature-capable printed wiring boards. And, finally, systems require reliable and inexpensive passive devices like resistors, capacitors and inductors.
Wide band gap materials have demonstrated that are able to work in high-temperature environment; but are still emerging processes technology, and, currently, only simple devices are available on the market. The two most used wide band gap materials are shown in the follows:

- ***SiC (Silicon Carbide)***
    - Silicon Carbide is a wide bandgap semiconductor that has a big potential for high-temperature electronic applications, exceeding the physical limits of Silicon (Si).
    - Property:
        - It can operate above 500°C
        - Wide bandgap (3,23eV @25°C)
- ***GaN (Gallium Nitride)***
    - Gallium Nitride has a large bandgap and a large conduction band discontinuity, leading to high channel densities and high breakdown fields.
    - Property:
        - Wide bandgap (3,4eV @25°C)

Both of them, thanks to their good reliability, are the most promising materials used for high frequency (Radio Frequency), Switching Power devices, microelectromechanical systems actuators and smart sensors with integrated electronics.
The recent availability of power devices based on GaN and SiC offers the potential for making significant progress since they can be operated at temperature beyond 200°C,

increasing the overall system performance. However, in order to exploit the high-temperature capability of these new power devices, CMOS control electronics must also be able to operate at these high temperatures.
The SOI technology enables the possibility to develop highly integrated embedded systems for application temperature up to 250°C. Another positive aspect is the relatively cheap development cost; this is due to the fact that to develop SOI devices are used many procedures used to develop Si devices, then migrating to this technology doesn't require huge costs.
The classical interconnections are not able to guarantee high reliability at high temperature then new materials for the interconnections have to be used. A high reliability can be provided by employing Tungsten for the metal lines, it is not prone to electromigration because of high activation energies for material transport along the electron current.
The majority of the requirements of previously presented applications (oil and gas drilling, avionics, automotive) and others that are not reported in this document, can be easily satisfied by SOI devices. Chapter **2** will explain, more in detail, the Silicon On Insulator technology and its behaviors.
Once high-temperature functional silicon has been developed, the battle is only half won. Packaging the die, and then attaching the package to the PCB, is not trivial at high temperatures. Many factors affect package integrity at temperature as shown in **Figure 5**.

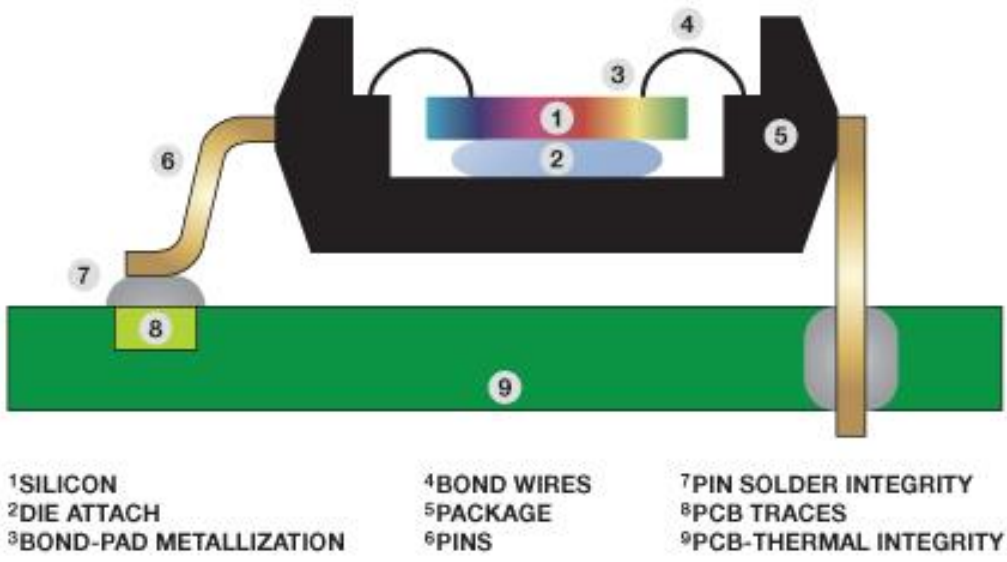


Figure 5: Elements of IC packaging and mounting

The die-attach material secures the silicon to the package or substrate. Many materials proven for use in standard temperature ranges are not suitable for high-temperature operation. Particular attention should go to matching the Coefficient of Thermal Expansion (CTE) between the die, die-attach, and substrate so that the die is not stressed or fractured over cycles of wide temperature variations. Even slight mechanical stress on the die can cause electrical parameters to shift to unacceptable levels for precision

applications. Metallic die-attach materials prove to be necessary when power devices require thermal and electrical connection to the package substrate.
Wire bonding is a method for interconnecting the die to the pins by attaching metallic wires from the lead frame to bond pads on the die surface. The compatibility of the metals used for the wire and bond-pad metallization is of major concern when considering wire bond reliability at elevated temperatures. Failures related to poor compatibility of bonding metals are dual: InterMetallic Compound (IMC) growth at the boundary interface, which creates a brittle bond; and diffusion, well-known as Kirkendall effect, which creates voids at the interface as shown in **Figure 6**, weakening the bond's strength and increasing its resistance.

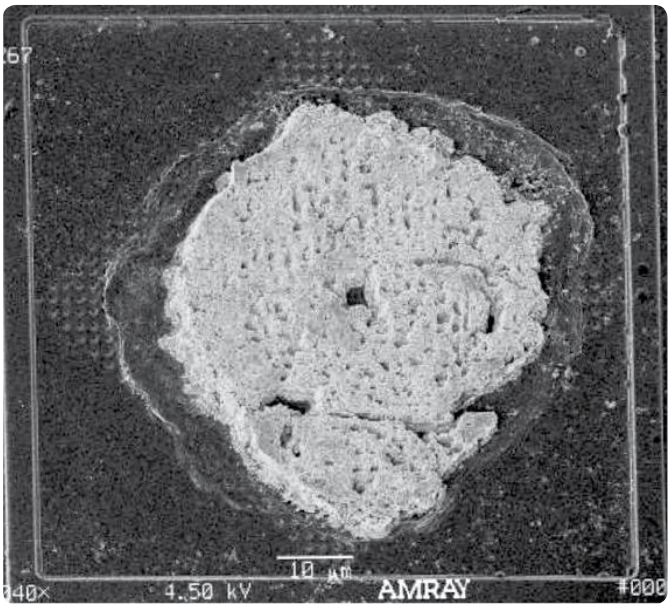


Figure 6: Kirkendall voids after bond failure

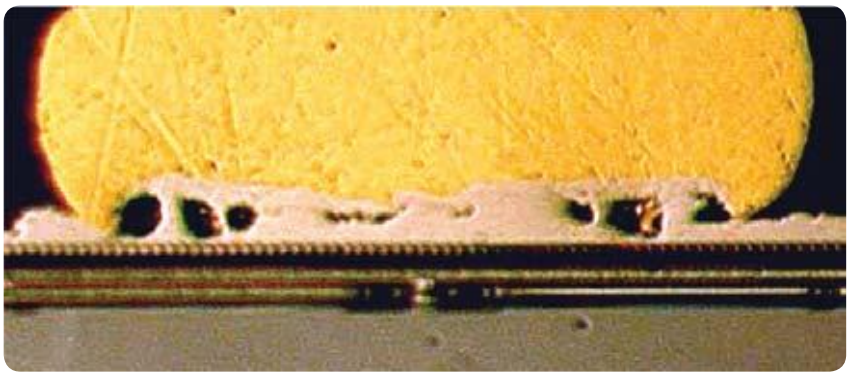


Figure 7: Au/Al InterMetallic Compound growth after 500 hours at high temperature

Unfortunately, one of the most popular metal combination in industry (gold wire and aluminum bond-pad metallization) is prone to these phenomena at elevated temperatures as shown in **Figure 7**.

Thus, there is a strong incentive to use the same metal for the bond wire and bond pad (a monometallic bond) to avoid these negative effects. If this is not possible, engineers should select metals that have slow enough IMC growth and diffusion rates to be reliable over the required lifetime. **Figure 8** shows the robustness of the monometallic bond when it is stressed for long time at high temperatures.

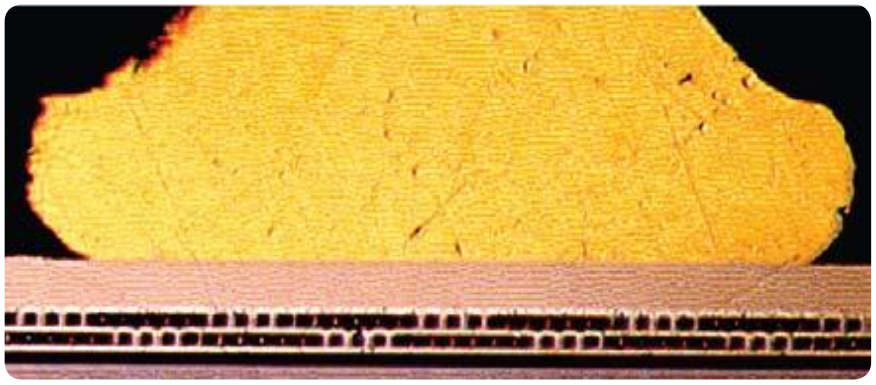


Figure 8: Monometallic bond after 3000 hours at high temperature

The IC package must also withstand stresses imposed by harsh environments. Although plastic packages are the standard in the market, they have been positively rated only up to 150°C for sustained uses; due to the recent interest in high-temperature applications, some investigations have shown that this rating can be stretched to 175°C but only for relatively short durations. For this reason, hermetic ceramic packages are preferred for high-temperature applications. The hermetic seal provides a barrier to the humidity and contamination ingress that cause the silicon corrosion. Unfortunately, as easily predictable, hermetic packages are normally more expensive, larger and heavier than their plastic counterparts. In some applications, that need less extreme temperature requirements (175°C), plastic packages may be preferred to conserve PCB area, reduce cost, or provide better vibration compliance. For systems requiring hermetic packaging and high component density, encapsulate more than one chip in a high-temperature multichip modules may be an appropriate solution. However, this solution requires that very good dice be available.
Package lead configuration and metallization must also be evaluated. Components mounted directly onto the surface of PCBs depend only on the bond pad area and quality of the adhesive between the copper layer and the pre-impregnated material. In extreme cases, the attachment strength can be further improved by bending the pins on the bottom side of the board to fix it to the PCB, but the through-hole pinout does not allow component population of the bottom side of the board.

The most popular standard solder alloys have melting points below 200°C, however there is a category of "High Melting Point" (HMP) alloys that have melting points well above 250°C. Even in such cases, the maximum recommended operating temperature for any solder subject to stress is about 40°C below its melting point. For example, the standard HMP solder alloy composition of 5% pond, 93.5% lead, and 1.5% silver has a melting point of 294°C but is recommended for use only up to about 255°C.

Last but not least, the PCB itself is a potential source of failure. The most common material used to develop PCB is FR4, it is a composite material composed of woven fiberglass cloth with an epoxy resin binder that is flame resistant (self-extinguishing). If a PCB, made of FR4, is used above the recommended temperature, even for short time durations, it can expand and delaminate. A good proven alternative is polyamide. However, polyamide suffers of very high moisture absorption, which can quickly lead to failure of the PCB, so it is important to control moisture exposure. In recent years, industry has introduced "exotic" laminates that absorb less moisture and maintain integrity at high temperatures.

Another important aspect is the verification of high-temperature components, testing them in the laboratory is not a trivial task, as it requires engineers to incorporate all the previously mentioned techniques to test performance at temperature extremes. In addition to using special materials in the construction of the mask, test engineers must manage the environmental chambers carefully, allowing the system to adjust to the required temperature changes. Due to the mismatch in expansion coefficients, fast temperature changes can result in damage to the solder joints on the PCB, warping and premature system failure. A guideline employed in the industry is to maintain the temperature variation below 3°C per minute.

To accelerate testing of life and reliability, a well-known practice for electronic components is the burn-in test, which consists in performing the tests at an elevated temperature. Although accelerated aging works well for standard products, increasing the stress temperature well above the nominal temperature may introduce new failure mechanism and yield inaccurate results.

2 SOI CMOS

In the last years, have been widely demonstrated and recognized that Silicon in Insulator (SOI) technology, thanks to the mature technological processes achieved, plays an important role in the market, thus giving a viable alternative to mainstream Bulk silicon, for the realization of high-speed, low-power digital and analog CMOS circuits, as well as applications under extreme high-temperature or radiation operating conditions [4].
SOI technology refers to the use of a layered silicon–insulator–silicon substrate in place of conventional silicon substrates in semiconductor manufacturing.
In a SOI fabrication technology, transistors are built on a silicon layer resting on an insulating layer of silicon dioxide (SiO_2), so creating devices and circuits with an active device area restricted to a silicon film of small thickness, perfectly isolated by the buried and field oxide. The insulating layer is created by flowing oxygen onto a plain silicon wafer and then heating the wafer to oxidize the silicon, thereby creating a uniform buried layer of silicon dioxide. Thanks to the insulating layer the device performances are increased because of the reduced junction capacitance unlike Bulk silicon's junction that is not isolated. The decrease in junction capacitance also reduces overall power consumption.
In a standard Bulk CMOS process technology, the P-type body of the NMOS transistor is held at the ground voltage, while in a PMOS transistor in the Bulk CMOS process technology is fabricated in an N-well, with the transistor body held at the V_{dd} supply voltage by means of a metal contact to the N-well.
In SOI process technology, the source, and drain regions of transistors are isolated from the substrate. The body of each transistor is typically left unconnected and that results in floating body that can get freely charged/discharged due to the transient (switching). The charging/discharging condition affects threshold voltage (V_t) and many other device characteristics.
In addition, another important aspect of the SOI technology compared to the Bulk one, is that the transistor area in SOI process is smaller because is not necessary the metal contacts to the wells which is used in making MOS transistors.
According to the combination of film and oxide thickness and channel doping, different types of SOI MOSFET can be realized:

- Partially Depleted (PD) devices
    - Thicker films (over 100 nm)
- Fully Depleted (FD) devices
    - Thinner films (less than 50 nm)
- Ultrathin film devices surrounded by a top and bottom common gate (GAA that means Gate-All-Around)
    - In ultrathin film device the active device area is restricted to a silicon film of small thickness, perfectly isolated by the buried field oxides. In contrast to other SOI devices, ultrathin film devices fabrication requires non-standard processing.

Figure 9 shows the comparison between the standard Bulk CMOS (top of the figure), Partially Depleted SOI transistor (bottom left) and Fully Depleted SOI transistor (bottom right) in which is highlighted the difference of the depletion layer in all the cases [5].

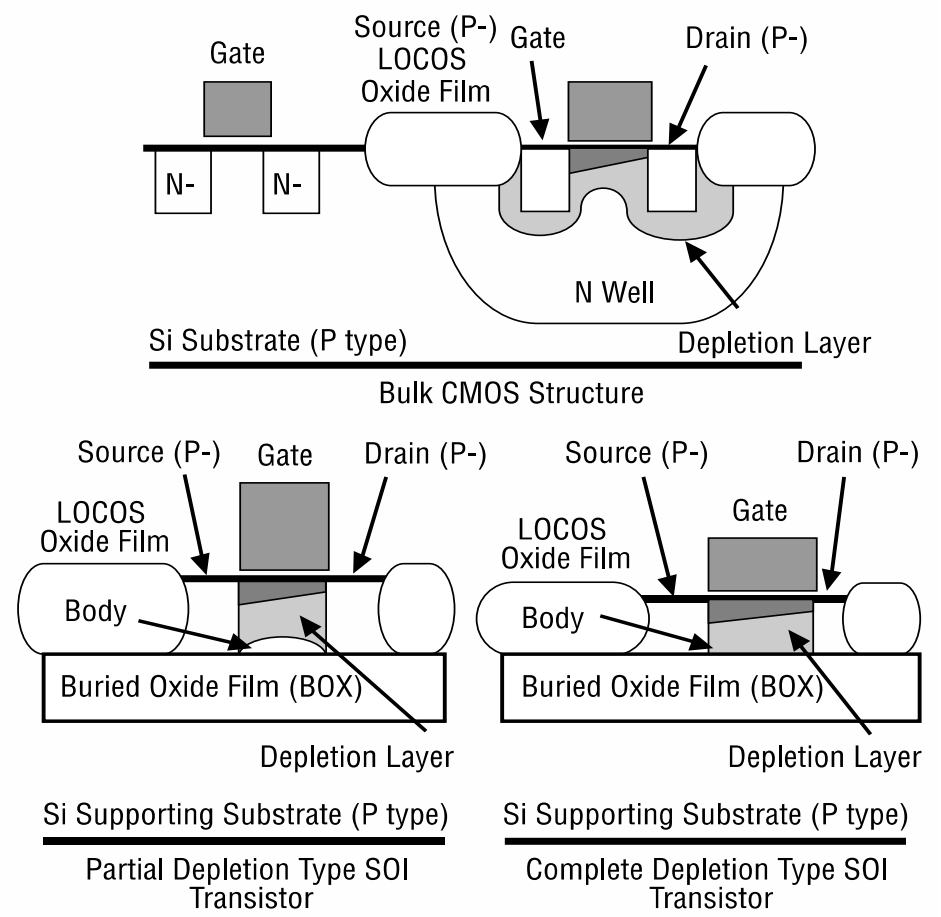


Figure 9: Bulk CMOS (top), PD SOI (bottom left) and FD SOI (bottom right)

Figure 10, instead, shows the source/drain and perpendicular cross-section of the Gate-All-Around SOI transistor. GAA transistors have the advantage of being totally free of body effect, as the active region is completely shielded by the gate. The threshold voltage is does fixed by the doping level for all operating conditions.

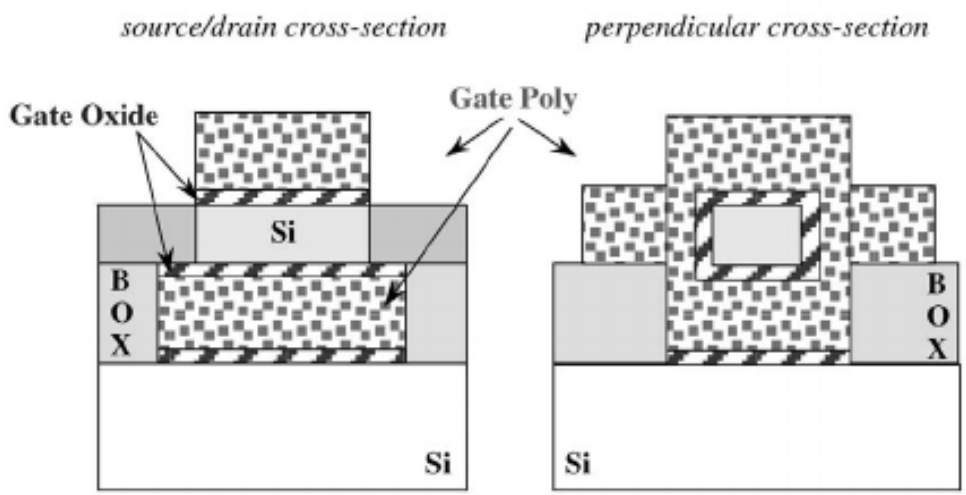


Figure 10: Gate-All-Around SOI transistor

In an NMOS transistor, applying a positive voltage to the gate depletes the body of P-type carriers and induce an N-type inversion channel on the surface of the body. If the insulated layer of silicon is made very thin, the layer fills the full depth of the body. A technology design to operate this way is called a Fully Depleted (FD) SOI technology. The thin body avoids a floating voltage. In 45nm and below CMOS, the V_t can be tuned by a midgap metal gate leaving the fully-depleted body undoped. By this configuration you will achieve a higher channel mobility, hence a higher performance, as well as lower variability from one device to another. Fully depleted SOI enables a CMOS low-power technology with undoped body. FD SOI is a perfect choice for low power applications, thanks to the best performance/low leakage couple.

On the contrary when the insulated layer of a silicon is made thicker, we obtain a depletion layer which is not extended for the full depth of the body. A technology having these characteristics is named a Partially Depleted (PD) SOI technology, as previously mentioned and illustrated in **Figure 9**. The undepleted portion of the body is not connected to anything. The exact voltage depends on the history of source, gate, and drain voltages leading up to the current time (the "history effect"). However, the voltage can be expected to fall within a known range.

A list of advantages, of SOI technology with respect to Bulk technology, and their explanation are reported below:

- Lower parasitic capacitance due to isolation from the Bulk silicon
- Resistance to latch-up due to complete isolation of the n-well and p-well structures
- Reduced temperature dependency due to no doping
- Good yield due to high density, better wafer utilization
- Lower leakage currents due to isolation thus higher power efficiency

2.1 History effect

The body of the NMOS or PMOS transistors in the SOI is floating instead of bound to ground (NMOS) or V_{dd} (PMOS) as in bulk CMOS [6]. This floating body can change the MOS

transistor threshold voltage due to differences in the body voltages. This could cause variation in the circuit delay and mismatch between two identical devices.

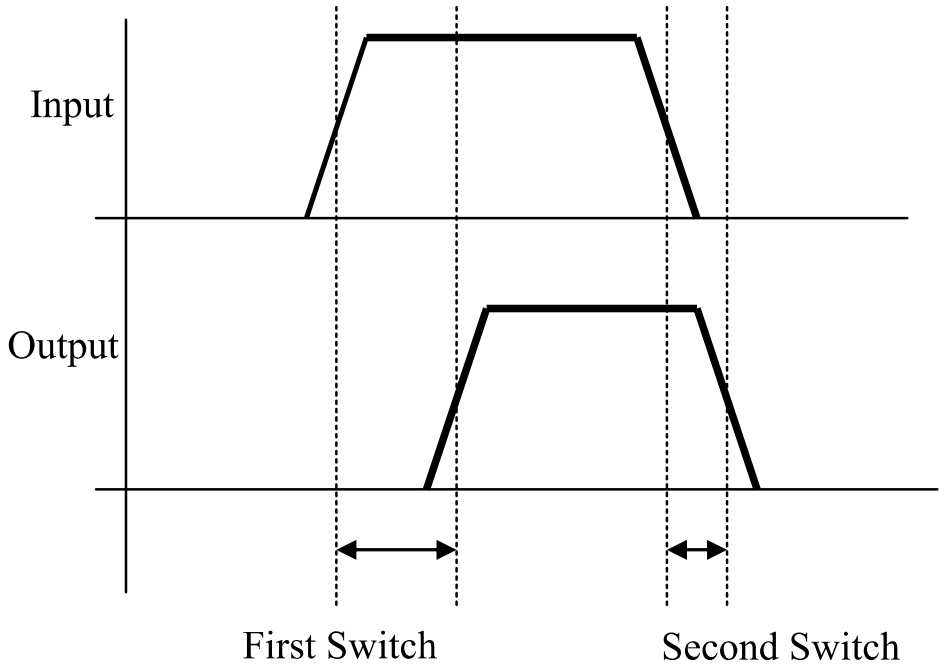


Figure 11: History effect

As the SOI circuit switches, the body voltages of the switching transistor will change from their previous steady state condition. This is called the history effect. The delay of a SOI logic circuit can be different (in most of the case shorter) if switching regularly versus a circuit that has been inactive for a long time and then switches. If a circuit is not active for long enough time to be in a steady state and then switches, this switching activity is called first switch, while if the circuit is switching more regularly, this is called second switch; both the switches are reported in **Figure 11**. Typically, second switch has shorter delay than first switch due to the fact that the body-source voltage of the second switch is higher than first switch, which reduces the V_t of the second switch transistor.
This is one of the most interesting circuit design issues in SOI, but, at the same time, it is also a benefit which contributes to achieve better performances over Bulk CMOS. Modeling timing parameters of transistor and circuit, considering the history effect, is crucial for silicon success.

2.2 Stack height effect

Due to floating body in PD SOI and low substrate effect in FD SOI, in a stack of transistors, the V_t of the upper device results smaller than in Bulk silicon, improving performances. Then the first switch is typically 20-30% faster than in Bulk, while the second switch is even faster.

2.3 Substrate noise

With the increased integration of Digital and Analog circuits on the same die, substrate noise issue is dominant in the Bulk process. Especially the digital noise can affect the sensitive analog circuits. In SOI technology the buried oxide layer acts a die-electric barrier and it helps reducing the substrate noise.

2.4 Latch up elimination

Bulk CMOS relies on junction isolation between devices, while SOI uses dielectric isolation to surround the entire device sides and bottom. SOI has no wells into the substrate and therefore has no latch-up or leakage paths. It eliminates the need of guard rings, thus smaller area for the same function.

2.5 Self-heating

The insulation layer of the SOI wafer creates a potential temperature delta between devices called self-heating. Self-heating is evident at the high power regions. May not have huge impact on digital circuits, however this effect must be considered for analog circuit.

2.6 Temperature sensitivity

SOI CMOS is much less sensitive to temperature than Bulk. In all SOI processes, the leakage to the substrate is obviously suppressed.

2.7 Body contacts

In the digital circuits, the transistor operates as a switch and remains in a steady state most of the time. Modeling switching characteristics with floating body effects are slightly complicated, but it can be modeled. Modeling the behavior of linear characteristics circuit with varying potential of the floating body is very difficult in the case of Analog/Mixed/IO design as it changes the output impedance of the device and its V_t-matching to the next device. A body contact transistor can be used as the current source or as any matching transistors designs to eliminate the floating body effect in the SOI technology.
However, body contact has RC delay associated with it, and shows poor transient response due to high capacitance and resistance. Also body contacts do not scale with the gate length, and requires bigger transistor size and low density. Body contacts are used only where needed because they increase the layout area and decrease performance.

A summary of pros and cons of SOI technology compared to the Bulk technology is reported below:

Pros:

- Higher performance at equivalent V_{dd}
- Reduced temperature sensitivity
- Latch-up eliminated

- Reduced antenna issues
- No body or well taps needed
- Small transistors save a lot of area
- Power savings

Cons:

- V_t dependent switching (history effect)
- Bipolar currents
- Self-heating
- Modeling issues

2.8 SOI threshold voltage

In Bulk MOSFETs the threshold voltage variation mainly depends on the variation of the maximum depletion width, and typical shifts of 3-5 mV/°C are observed, depending on the doping, temperature, etc [7]. The shift in SOI MOSFETs presents limited variation because, using a FD silicon film, the temperature dependence can be almost suppressed. All FD SOI devices are characterized by a variation as low as 1 mV/°C up to a certain temperature.

It can be inferred that the temperature dependence is characterized as follows:

- As the maximum depletion width is reduced when increasing the temperature, there is a critical point (200°C) above which SOI transistors feature a Bulk-like dependence, because the device becomes PD.
- GAA transistors do not feature such a degradation thanks to double-gate operation and thinner films (up to more than 300°C).

2.9 SOI drain leakage current

As depicted in **Figure 12**, in Bulk MOSFETs, the drain leakage current increases with temperature as the square of the intrinsic concentration (n_i), because the dominant mechanism is the diffusion of the carriers in the quasi-neutral region surrounding the drain junction.
In FD SOI MOSFETs, this quasi-neutral region is totally suppressed, and the generation-recombination mechanism in the depleted region becomes dominant, so that the leakage current only increases with temperature as n_i.

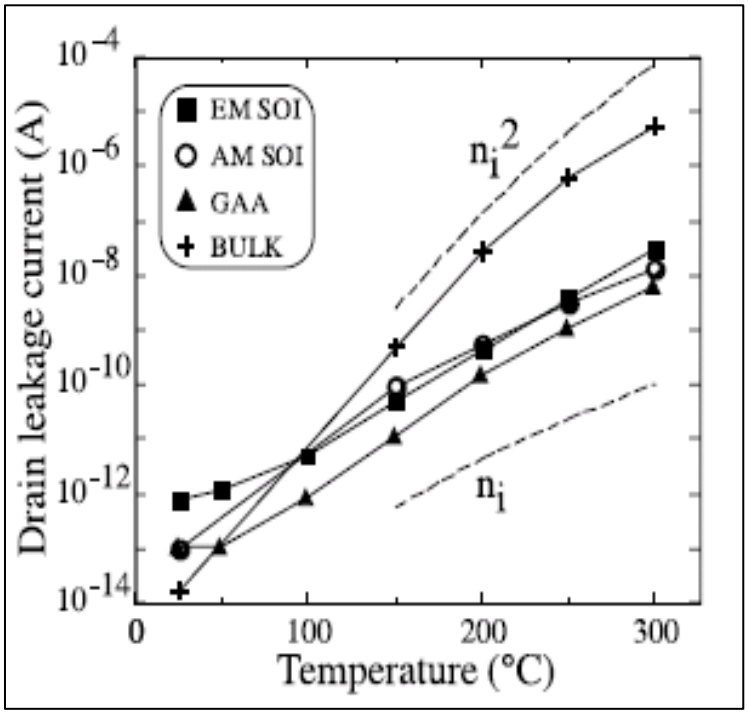


Figure 12: Drain leakage current vs temperature

Again, as previously seen for FD SOI devices, above the critical temperature at which the film becomes PD, a squared behavior is observed. SOI devices have the potential to offer a reduction in static power dissipation by at least one order of magnitude at 150°C and by 3-4 decades at 300°C when compared with Bulk devices.
At high temperature, device leakage current directly contributes to standby power dissipation.
Thanks to its lowest leakage, FD SOI CMOS therefore enables the realization of complex electronic circuits able to be operated above 250°C.

2.10 SOI output conductance

The output conductance, shown in **Figure 13**, is defined as the derivative of the drain current by the drain voltage at constant gate voltage.
In Bulk transistors, two conductance components add up:

- MOS channel current component;
- Drain junction current component.

As evidenced by **Figure 14** the Bulk output conductance value first improves with temperature then very rapidly decreases above 150 °C.

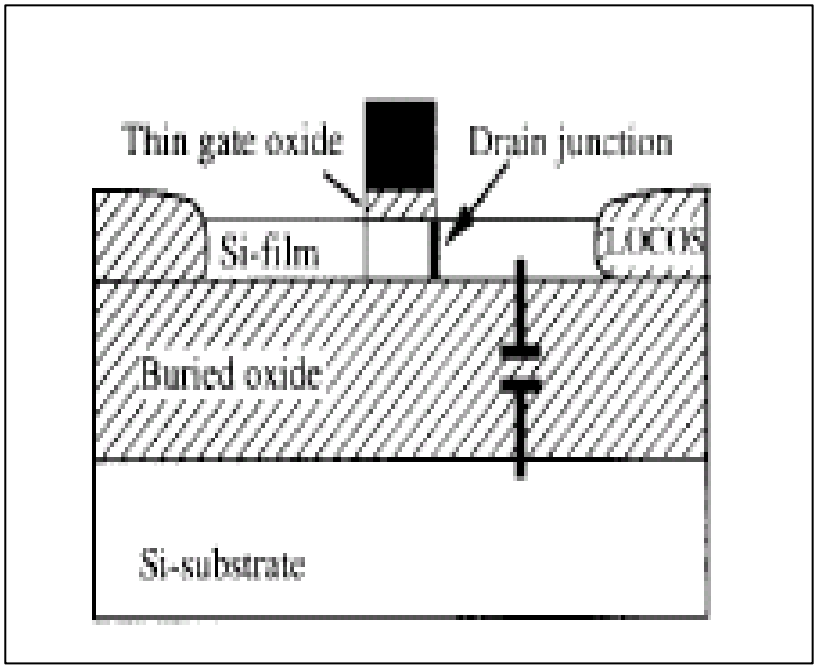


Figure 13: Junction component of the output conductance

In SOI devices, the junction component is almost completely suppressed, so that the output conductance value becomes much better than that in Bulk devices at high temperatures. The intrinsic gate-to-source capacitance is related to dynamic variations of the charges stored within the device. Measurement results on FD SOI MOSFETs show that the capacitance characteristics mostly follow the threshold voltage variation up to 320°C.

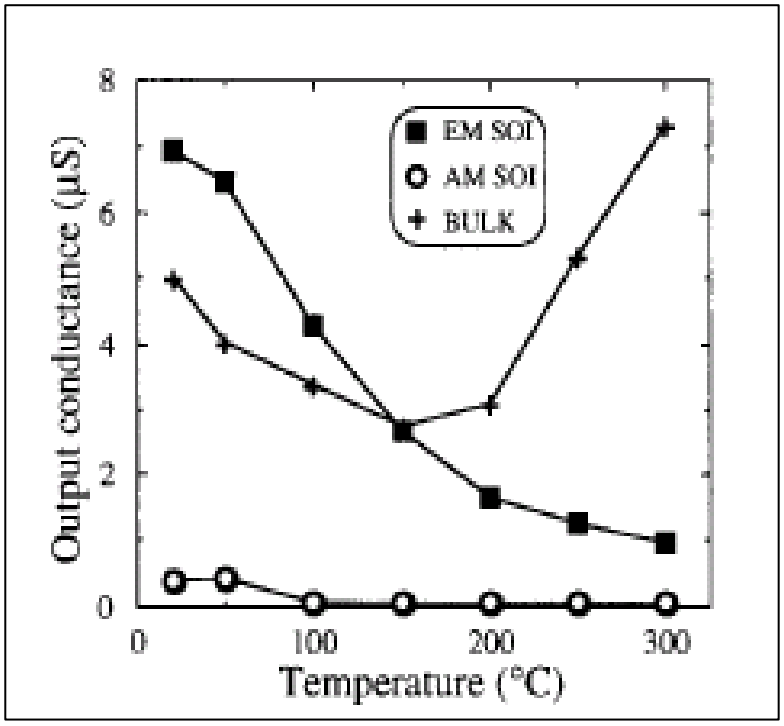


Figure 14: Output conductance vs temperature

2.11 SOI range temperature

This chapter highlights the previously explained technologies and their maximum operative temperature:

- Bulk MOSFETs can only be used up to 200°C;
- PD SOI transistors only extend the range up to 250°C
    - Adds radiation hardness to the high-temperature capability;
    - Advantageous for nuclear applications;
- FD devices can go up to 300°C
    - Also up to 400-500°C but with very degraded device characteristics;
- AAG devices can be used up to 350°C.

3 X-FAB XT018 Technology

This chapter gives a short description of the studied technology and the reason why this technology was introduced in the market.

3.1 About X-FAB?

X-FAB is the world's largest analog/mixed-signal foundry group manufacturing silicon wafers for mixed-signal integrated circuits (mixed-signal ICs). Its marketing network and client base span the Americas, Europe and Asia, offering manufacturing capacity of approximately 864000 200mm-equivalent wafers per year. The largest specialty fab group, X-FAB is unlike typical foundry services because of its specialized expertise in advanced analog and mixed-signal process technologies.
These technologies are not intended for digital applications with smallest possible structure size, but rather are targeted for analog applications that can be integrated with additional functions such as high voltage, non-volatile memory or sensors. By combining solid, specialized expertise in advanced analog and mixed-signal process technologies with excellent service, a high level of responsiveness and first-class technical support, X-FAB optimally manages the product development flow and supply chain for its customers' semiconductor products.
At its five manufacturing sites in Germany, the U.S., and Malaysia, X-FAB manufactures wafers on modular CMOS and BiCMOS (Bipolar junction transistor and CMOS transistor integration) processes with technologies ranging from 1.0 to 0.18 µm, and special BCD (Bipolar-CMOS-DMOS), SOI and MEMS (Microelectromechanical Systems) long-lifetime processes. The sites can handle approximatively 72000 8-inch equivalent wafer starts per month in total. Always endeavoring to create long-term customer relationships based on stability, reliability and confidence in X-FAB's expertise, X-FAB adds value to the wafer manufacturing process by offering customers outstanding technical support.
X-FAB customers benefit from high-performance technologies, excellent technical design and prototyping services; and fast, easy and flexible foundry access worldwide. Privately held and headquartered in Erfurt, Germany, X-FAB has sustained steady growth year over year, often exceeding that of the industry at large. It currently employs approximatively 2500 people worldwide.

3.2 XT018 technology

X-FAB Silicon Foundries in 2015 announced the industry's first cost-efficient 180nm SOI technology for automotive and industrial applications that need to operate in harsh environments. X-FAB's new suite of 40V and 60V high-voltage devices for its XT018 180-nanometer SOI platform outperforms bulk CMOS technologies and provides cost savings of up to 30-percent. The XT018 technology includes comprehensive design support, resulting in fewer design cycles and the possibility of first-time-right success; it offers cost-competitive implementation of next-generation automotive solutions and leads to

faster time to market. The new devices make the XT018 process ideal for advanced automotive applications such as monolithic motor controllers and physical layer transceivers including integrated or stand-alone LIN/CAN transceivers.
The XT018 platform is specifically designed for next-generation automotive, industrial and medical applications with up to 200V operating voltage and an operating temperature range of -40° up to 175°C.
The XT018 series is X-FAB's 0.18-micron Modular High-Voltage SOI CMOS Technology. It combines the benefit of SOI wafers with Deep Trench Isolation (DTI) and those of a state-of-the-art six metal layers 0.18-micron process.
Using SOI wafers as the starting material, in combination with trench isolation instead of the more commonly used junction isolation techniques in CMOS, simplifies the design concept. The SOI wafers eliminates the parasitic bipolar effects to substrate, reducing latch-up risk. They also enable the development of devices such as truly isolated diodes, allowing reverse supply voltage protection that is difficult to achieve with the bulk CMOS technology.
In the following are reported the XT018 device schematic cross section [8], **Figure 15**, and the XT018 basic design rules, **Figure 16**.

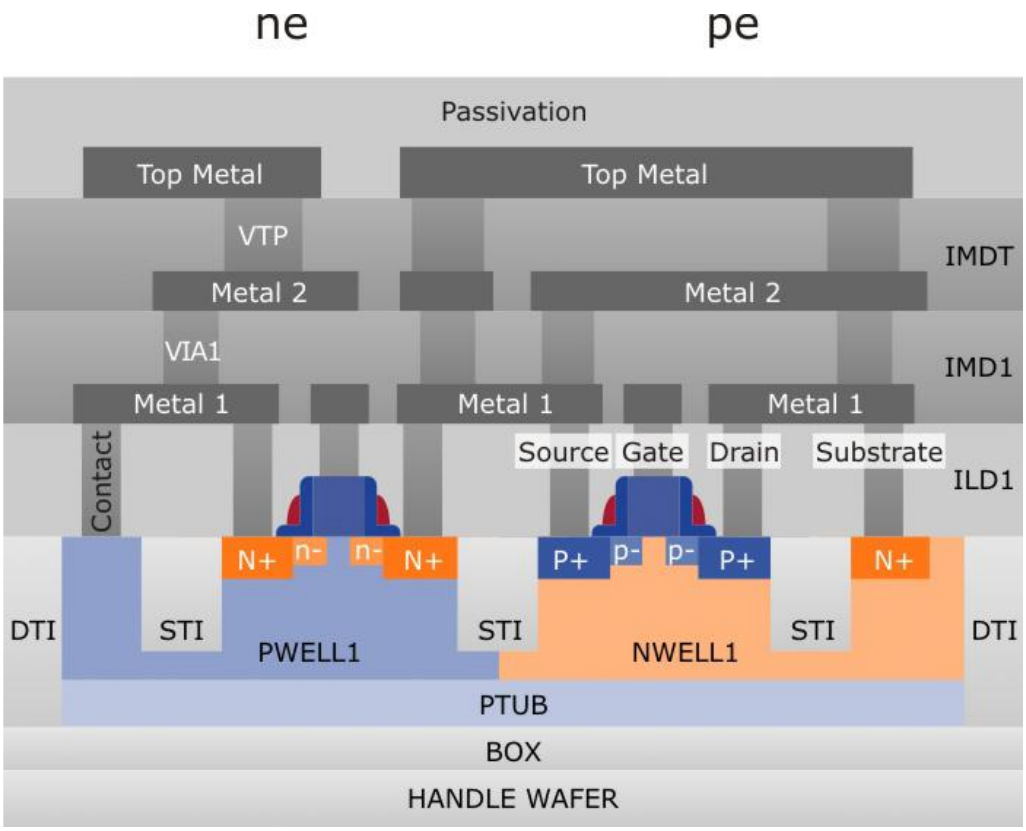


Figure 15: Device schematic cross section

As can be seen in the design rules' table, **Figure 16,** the key value is the width of the active area, that is 0.22µm. A thickness film of 0.22µm can be considered quite thick, and, as seen

in chapter **2**, it means that the XT018 technology is partially depleted, or well-known as PD SOI CMOS.

XT018 BASIC DESIGN RULES		
Mask	**width [µm]**	**Spacing [µm]**
N-well	0.86	1.40
Active area	0.22	0.28
Polysilicon gate	0.18	0.25
Polysilicon resistor	0.44	0.44
Contact	0.22	0.25
Metal1	0.23	0.23
Via 1/2/3/4	0.26	0.26
Metal 2/3/4/5	0.28	0.28
Top Via / Metal	0.36 / 0.44	0.35 / 0.46
Thick Metal	3.0	2.5

Figure 16: Basic design rules

As said in the description of XT018 technology, the maximum working temperature, given by the foundry, is 175°C. During the internship at CEA, the purpose of my work is to establish and evaluate the technology's behavior at temperatures above this limit. To do this, some simple circuits have been considered and will be presented in the next chapters.

XT018 MOS TRANSISTORS							
Device	**Name**	**Available with module**	**|VT| [V]**	**IDS [µA/µm]**	**BVDS [V]**	**Max. VDS [V]**	**Max VGS [V]**
1.8V NMOS	ne	LP5MOS	0.60	515	> 3.6	1.98	1.98
1.8V PMOS	pe, pe_5	LP5MOS	0.67	195	> 3.6	1.98	1.98

Figure 17: MOS transistor characteristics

In **Figure 17** are shown the characteristics of the MOS transistor, in particular the NMOS transistor (ne) and the PMOS transistor (pe), they will be used in the next chapters to design a 99-stages ring oscillator. The ne and pe transistors are designed to be used at 1.8V and are available in the X-FAB library named LP5MOS. In the table is also represented the threshold voltage, which is the major cause for which the technology changes its performances depending on the environment temperature. Another important value is the maximum V_{GS} value that is equal to 1.98V or rather +10% than the typical voltage reference (1.8V).

4 Simulations

In this chapter is reported a short explanation of the simple circuits taken into account and the relative simulations' results done on them under different conditions.
The simulation part has been realized using Cadence Virtuoso and, in particular, the simulator called Cadence Spectre Circuit Simulator.

4.1 Cadence Virtuoso Analog Design Environment

The Cadence Virtuoso Analog Design Environment family of products provides a comprehensive array of capabilities for the electrical analysis and verification of analog/mixed-signal designs, including the flexibility to integrate into a variety of custom flows [9].
The Virtuoso Analog Design Environment product suite provides all the capabilities required to fully explore, analyze, and verify a design against the user's desired goals. As the industry's leading solution for analog simulation control and management, it allows users to flexibly select the tier that best supports their design goals as they move through the design flow.
Analog Design Environment L provides a quick entry into the analysis process with easy entry and execution of simulations. Analog Design Environment XL extends the L tier capabilities, providing multiple test support, analysis over sweeps, and corners and easy reviewing of all results directly or as a datasheet. Analog Design Environment GXL builds one the ADE L and XL capabilities by providing targeted tools that aid with key design challenges with early parasitic analysis, design centering, and designing in multi-technologies. Additional options allow the user to detect and fix problem caused by layout-dependent effects early in the design cycle, and to access the electrically aware design package that provides insight into the parasitic on a route as it is created.
The Virtuoso family provides multiple benefits that are reported in the following list:

- Provides built-in support for all Virtuoso simulators, with integration support for third-party simulators;
- Supports multiple test methodologies to fully explore and validate designs;
- Accelerates design debug using a variety of built-in analysis tools;
- Facilitates early correction via easy evaluation of pre- and post-layout parasitic effects;
- Quickly detects and explores circuit problems via a clear visualization cockpit;
- Offers integrated documentation and fast waveform visualization across all tests;
- Supports manual or automated design evaluation and sizing to target specifications;
- Provides a tiered set of capabilities to support a variety of design flows and design challenges.

For the purpose of my simulations Virtuoso ADE L provides all the needed characteristics, for this reason in the following is explained more in detail.

4.1.1 Virtuoso Analog Design Environment L overview

Virtuoso ADE L is the entry-level analog design and simulation environment for the Virtuoso custom design platform. ADE L is the industry's leading task-based environment for simulating and analyzing full custom, analog, and RF-IC designs. It features a graphical user interface, an integrated waveform display, distributed processing, and interfaces to popular third-party simulators.
ADE L provides the foundation to facilitate extended design analysis and validation into the ADE XL and ADE GXL products.

4.1.1.1 ADE L Benefits

The list of benefit is reported below:

- Reduced learning curve with a simulator-independent environment;
- Maximum efficiency in the script-driven mode;
- Close integration with Virtuoso Schematic Editor for interactive analysis;
- Easy design and test parameterization for fast circuit exploration;
- Configurable window for optimum display of relevant data;
- Integrated visualization cockpit for exploration of simulation results;
- Built-in calculator and extensive list of functions to extract quantifiable results.

4.1.1.2 ADE L Features

4.1.1.2.1 Easy-to-use interactive simulation environment

The interactive environment has everything users need to set-up, run, and analyze results with any integrated simulator. It offers a variety of tools for displaying and analyzing results, giving designers the flexibility to visualize and understand the many interdependencies of an analog, RF, or mixed-signal design. These tools allow users to quickly and easily pinpoint critical design parameters and their effect on circuit performance. The environment is flexible enough to take advantage of the Virtuoso Multi-Mode Simulation technology, by making it easy to switch between different simulators without having to re-enter all measurements.
Virtuoso ADE L has an extensive scripting language (OCEAN) built in. OCEAN is based on the Cadence SKILL programming language for development of more complex analysis. It can be used to set-up, run, and post process results in a batch-oriented methodology. Lastly, ADE L includes the capability to interface with other commercially available and in-house simulators through the OASIS Integrator's Kit.

4.1.1.2.2 Built-in waveform display and signal analysis capabilities

The waveform display tool, coupled with an extensive waveform calculator, provides a comprehensive post-simulation analysis environment. The waveform window can handle all types of analog and mixed-signal data, including advanced displays such as noise, corner, statistical, and RF plots. Additionally, it contains a variety of changeable display attributes for the axes, waveform colors, and labels, so you can make professional plots

for your reports. Waveforms markers and a built-in waveform calculator allow accurate measurement of signals in a variety of different modes, including transient, AC, and RF. The calculator's algebraic expressions can be composed of any combination of input or output voltages or currents.

4.1.1.2.3 Integral part of the Virtuoso custom design platform

Virtuoso ADE L is an integral part of the Virtuoso custom design platform. It bridges the gap between schematic design and physical layout by providing a simulation environment where the designer can compare designs in both pre- and post-extracted forms, thereby completing the Cadence IC design flow. It supports analog system to IC design methods with complete access to behavioral modeling languages for both simulation and cross-probing for waveform display. Post-simulation operating condition can be easily annotated back to the schematic with net voltages, currents, and device operating information.

4.2 Spectre Circuit Simulator

The Spectre Circuit Simulator is an industry-proven, fast, SPICE-accurate and RF simulator for tough analog RF, mixed-signal circuit simulation, and library and IP characterization [10]. It is tightly integrated with the Virtuoso custom design platform and provides a comprehensive set of detailed transistor-level analyses in multiple domains for faster convergence on design goals. Its superior advanced architecture allows for low memory consumption and high-capacity analysis.

4.2.1 Spectre Benefits

A list of pros of which the designer can benefit with the use of Spectre is reported below:

- Provides high-performance, high-capacity SPICE-level analog and RF simulation with out-of-the-box tuning for accuracy and faster convergence;
- Facilitates the tradeoff between accuracy and performance through user-friendly simulation setup applicable to the most complex analog and custom-digital ICs;
- Enables accurate and efficient post-layout simulation;
- Supports out-of-the-box S-Parameter models, enabling simulation of complex n-port devices;
- Delivers signal integrity analysis capability with an advanced transmission line library and graphical editor;
- Provides a platform to measure and analyze system-level performance metric;
- Performs application-specific analysis of RF performance parameters (spectral response, gain compression, intermodulation distortion, impedance matching, stability, and isolation);
- Offers advanced statistical analysis to help design companies improve the manufacturability and yield of ICs at advanced process nodes without sacrificing time to market;

- Delivers fast interactive simulation setup, cross-probing, visualization, and post-processing of simulation results through integration with the Virtuoso Analog Design Environment;
- Ensures higher design quality using silicon-accurate, industry-standard, foundry-certified device models shared across the simulation engines.

4.2.2 Spectre Features

4.2.2.1 Production-proven circuit simulation techniques

The Spectre Circuit Simulator uses proprietary techniques (including adaptive time step control, sparse matrix solving, and multi-processing of MOS models) to provide high performance while maintaining signoff accuracy. It includes native support for both Spectre and SPICE syntax, giving users the flexibility to use Spectre technology for any design flow without worrying about the design format. Additionally, it converges to results that are "silicon-accurate" by modeling extensive physical effects in devices for deep sub-micron processes.

4.2.2.2 Comprehensive statistical analysis

Spectre bridges the gap between manufacturability and time to market at advanced process nodes by providing a comprehensive set of statistical analysis tools tailored to IC design. The DC Match capability efficiently analyzes local process mismatch effects and identifies the yield-limiting devices and parameters. Tight integration between the Spectre Circuit Simulator and the Virtuoso Analog Design Environment offers user-friendly interactive setup and advanced visualization of statistical results.

4.2.2.3 Transient noise analysis

It provides transient noise analysis for accurate calculation of the large signal noise in nonlinear non-periodic circuits. All noise types are supported, including thermal, shot, and flicker.

4.2.2.4 Built-in Verilog-A and MDL

The Spectre simulator offers design abstraction for faster convergence on results, including behavioral modeling capabilities in full compliance with Verilog-A 2.0. The compiled Verilog-A implementation is optimized for compact device models offering comparable performance to built-in device models.
In addition to supporting standard SPICE measurement functions, it offers a measurement description language (MDL) to automate cell and library characterization. Spectre MDL enables the designer to post-process the results and tune the simulator to provide the best performance/accuracy tradeoff for a specific measurement.

4.2.2.5 Advanced device modeling and support

Furthermore, it supports MOS, BJT, specialty transistor models, resistors, capacitors, inductors, transformers and magnetic cores, lossy and lossless transmission lines, independent and controlled voltage and current sources, and Z and S domain sources.
Provides a user-defined compiled model interface (CMI). It allows for the rapid inclusion of user-defined models for a "model once, use everywhere" capability. It offers a curve tracer analysis capability for rapid model development and debugging.

4.2.2.6 Co-simulation with Simulink

The MathWorks Simulink interface to Spectre offers system and circuit designers a unique integrated environment for design and verification. Designers can insert their analog and RF schematics and post-layout netlist directly in the system-level block diagram and run co-simulation between Simulink and Spectre technologies. Designers can reuse the same Simulink testbench from system-level design to post-layout verification, minimizing the unnecessary format conversion while maintaining accuracy throughout the design flow.

4.2.2.7 Post-layout simulation

Last but not least Spectre enables analog and RF block and subsystem post-layout verification at near the speed of pre-layout simulation. An accurate parasitic reduction technique enhances the simulation performance of parasitic-dominant circuits by a significant amount over traditional SPICE-level simulation. The technology enables designers to trade-off accuracy and performance using a simple user-friendly setup.

4.3 Ring Oscillator

A ring oscillator is a device composed of an odd number of NOT gates whose output oscillates between two voltage levels, representing true and false value. The NOT gates, or inverters, are attached in a chain and the output of the last inverter is fed back into the first.
The ring oscillator is one of the most common circuit that, thanks to its simplicity, is used to test new technologies and show how that technology works under different conditions. A ring oscillator only requires power supply to operate. Above a certain threshold voltage, oscillations begin spontaneously. To increase oscillation frequency, two methods are commonly used:

- The applied voltage may be increased
    - This increases both the frequency of the oscillation and the current consumed. The maximum permissible voltage applied to the circuits limits the speed of a given oscillator;
- Reducing the inverters number of the ring, results in a higher frequency of oscillation given a certain power consumption.

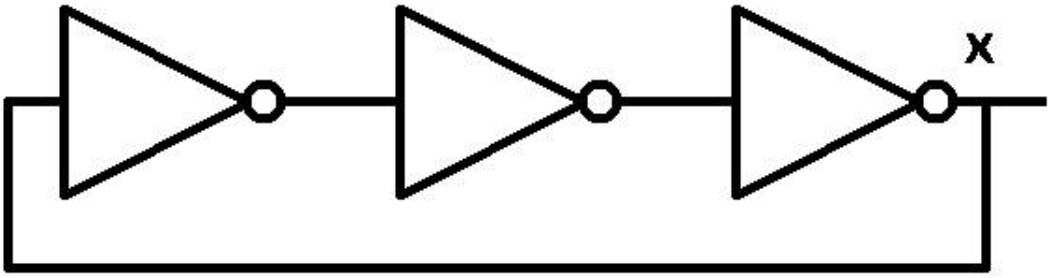
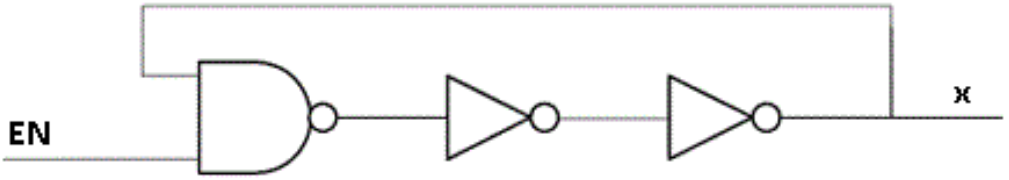


Figure 18: 3-stages Ring Oscillator

In **Figure 18** is reported a typical 3-stages RO. To evaluate the leakage current is necessary stop oscillating the ring, to do this, starting from the standard configuration, the first stage has to be modified. The modification can be done putting a NAND or a NOR gate instead of a NOT, **Figure 19**. In this way, thus using an enable signal, we can start and stop oscillating the ring as it is shown in the truth table in **Figure 19**.
As said before, RO is one of the most common circuit used to evaluate the quality of a new technology, because, thanks to the output frequency, we are able to understand how the technology reacts under different condition. In this particular case, we know that CMOS transistors are sensible to temperature variations because switching time changes under different temperatures. For the reasons mentioned above, we take the RO as a reference test for estimating the technology behavior.



EN	x	Next x
0	*	1
1	0	1
1	1	0

Figure 19: 3-stages Ring Oscillator with Enable signal

4.3.1 Simulation results

For the RO's simulations I considered a 99-stages RO, made of 98 NOT gates and 1 NAND gate. I simulated the RO at different temperatures, starting from -40°C up to 500°C, and using different supply voltages: 1.98V, 1.8V and 1.62V. 1.8V is the reference voltage given by the datasheet while 1.98V and 1.62V are the maximum compliance limits or rather 1.8V ± 10%.
During my internship, new models have been released by X-FAB, for this reason, in the following graphs, a comparison between old models and new models is represented.

In **Figure 20**, **Figure 21** and **Figure 22** are shown the resulting frequency of each RO driven by the voltages: 1.98V, 1.8V and 1.62V respectively. In each figure are depicted the performances, for each voltage, using three different simulation modes: worst power mode (wp mode, NMOS=FAST, PMOS=FAST), typical mode (tp mode, NMOS=TYPICAL, PMOS=TYPICAL) and worst speed mode (ws mode, NMOS=SLOW, PMOS=SLOW).

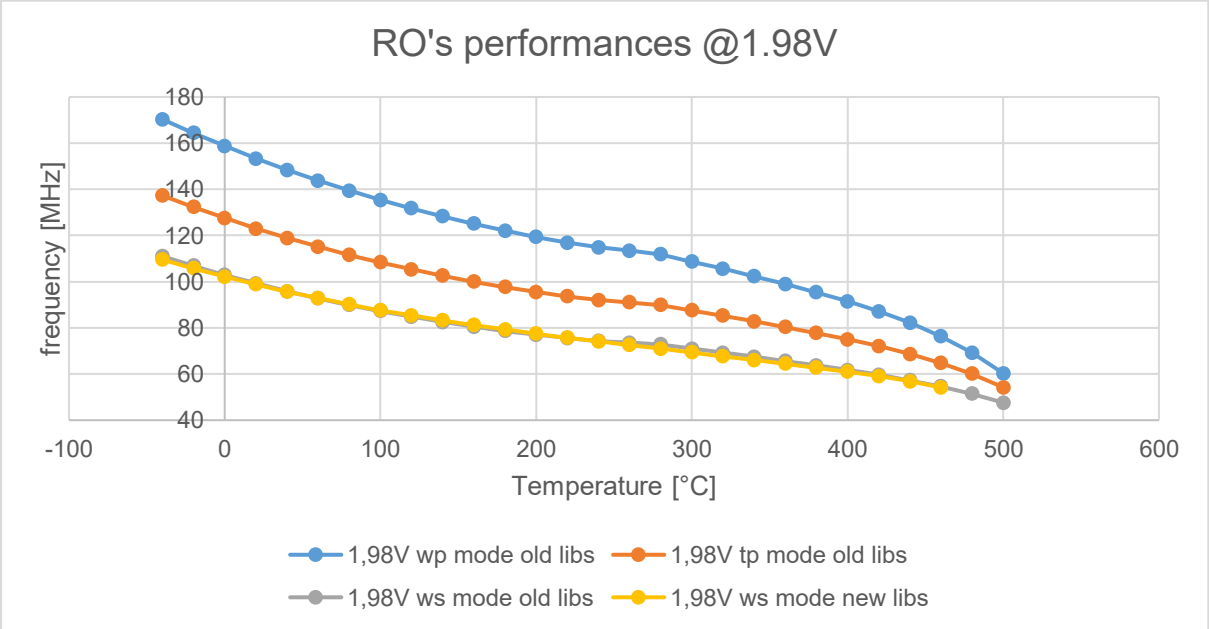


Figure 20: RO's frequency driven at 1.98V

The three different modes have been simulated in order to evaluate the most appropriate working condition, in which classify the silicon wafer used to develop the tested devices, which results will be explained in chapter **5**.

As we can see in **Figure 20**, **Figure 21** and **Figure 22**, the RO's output frequency decreases increasing temperature.
Looking the resulting graphs, it's easy notice that between the older model and the newer one performances are almost the same. The only difference is that using the newer model, for temperatures above 460°C, the breakdown effect occurs, then the RO stops working.
Another important aspect, which has to be mentioned, is that, starting from 269°C, some voltages are clamped by the simulator because they became too small. Using different warnings, the simulator signals that some voltages are less than 10mV due to temperature effect, so, during the simulation, those values are clamped at 10mV. This means that, starting from 270°C, simulation results are an extrapolation of the trend expected by the simulator, thus would be better check during the test phase if those values are conforming to the results given by the device under test.

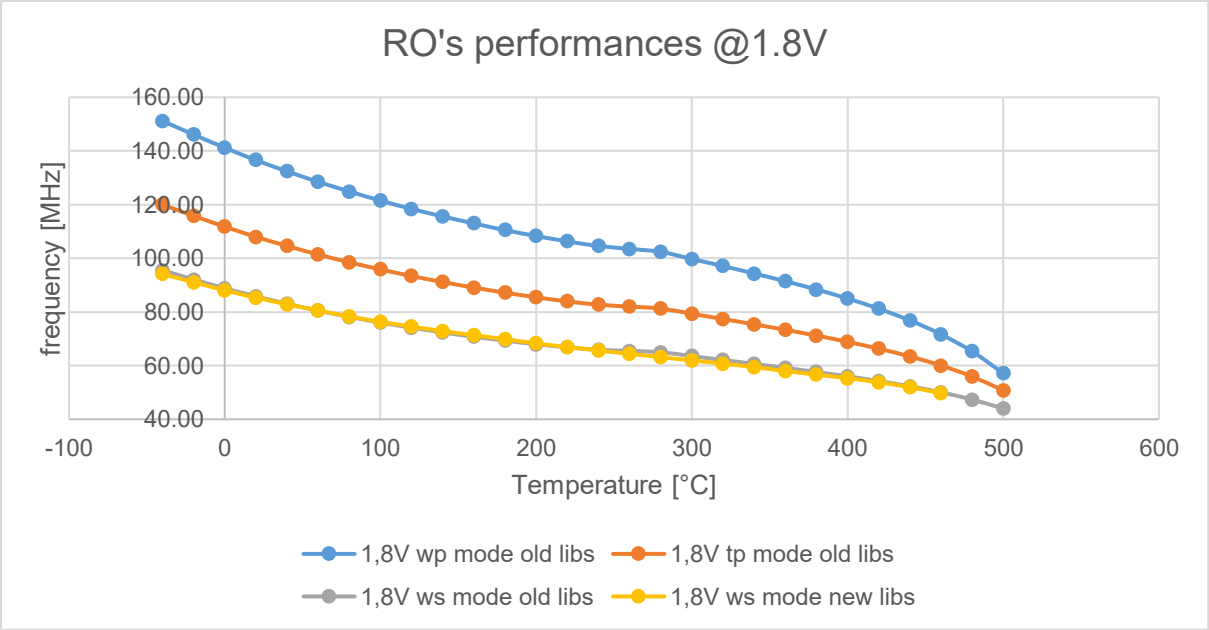


Figure 21: RO's frequency driven at 1.8V

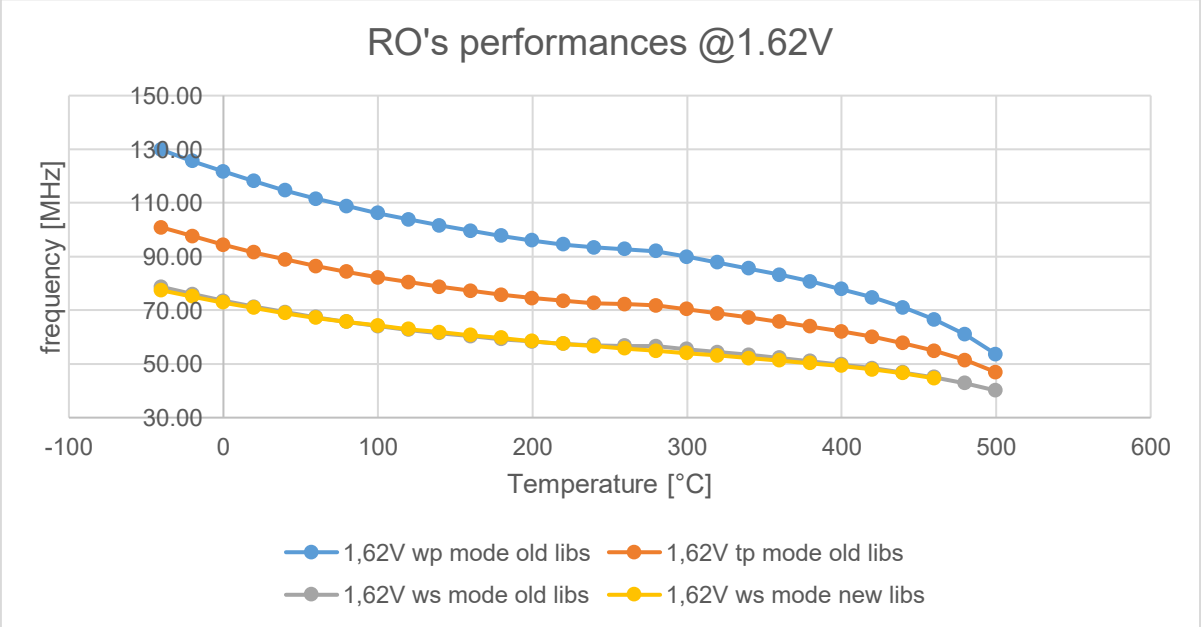


Figure 22: RO's frequency driven at 1.62V

All the RO's simulations were done twice, the first one without the digital PAD to have a comparison with the simple circuits, explained in the next sections, and the second one using PAD to compare the results with the ones given by the tests. The resulting output frequency, as expected, is the same in both the simulations, but the power consumption undergoes a substantial change due to the bigger PAD consumption compared to the RO. In **Figure 23**, **Figure 24** and **Figure 25** are depicted the power consumptions without the digital PAD in FAST, TYPICAL and SLOW mode for Vdd equal to 1.98V, 1.8V and 1.62V respectively.

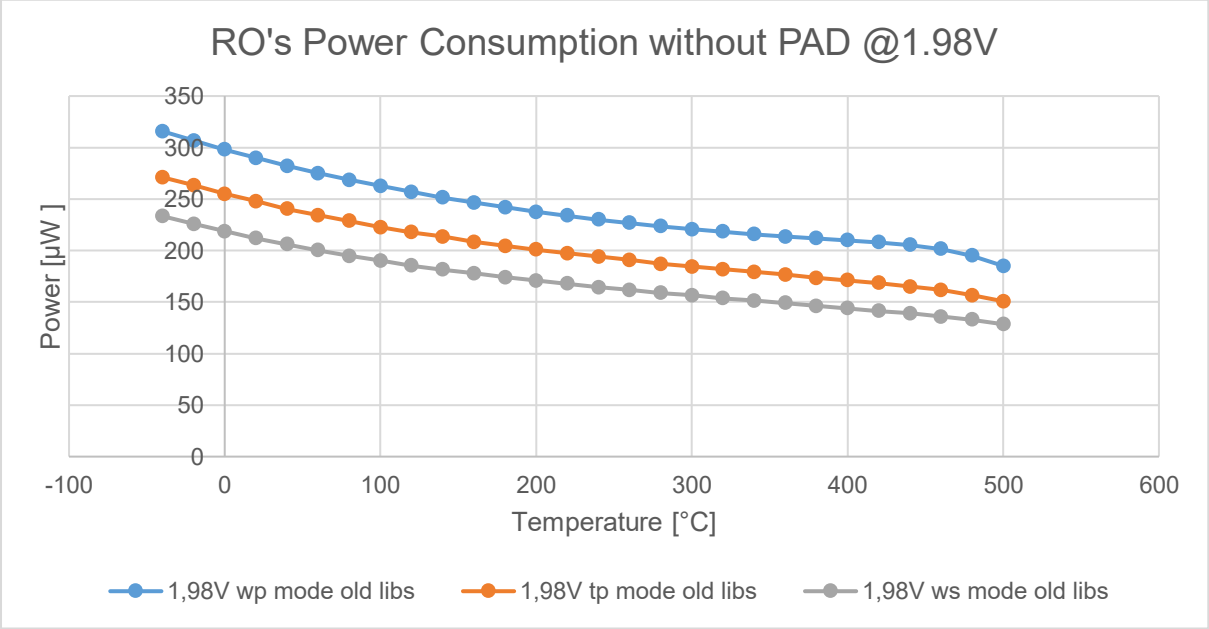


Figure 23: RO without PAD power consumption driven at 1.98V

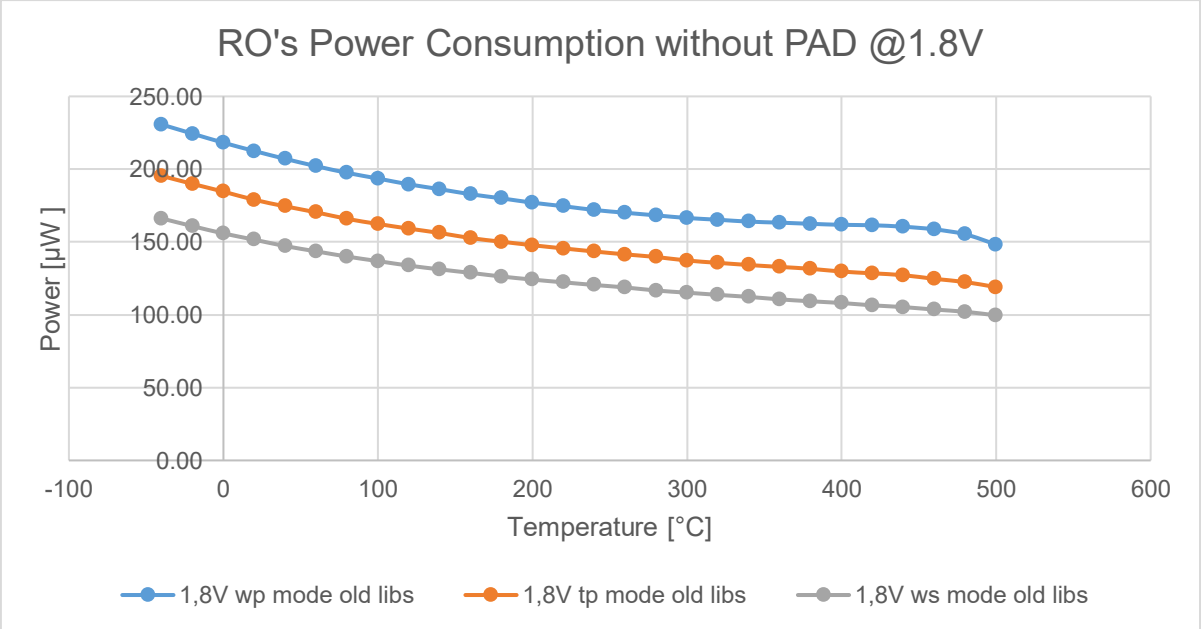


Figure 24: RO without PAD power consumption driven at 1.8V

As can be seen in **Figure 23**, **Figure 24** and **Figure 25**, the power consumption is directly proportional to the RO output frequency and therefore we can notice that consumed power decreases increasing temperature.
In **Figure 26** are represented the RO's power consumptions driven by the different voltages in SLOW mode because, in the following, it will be used to make a comparison in terms of performance and power consumption with another circuit.

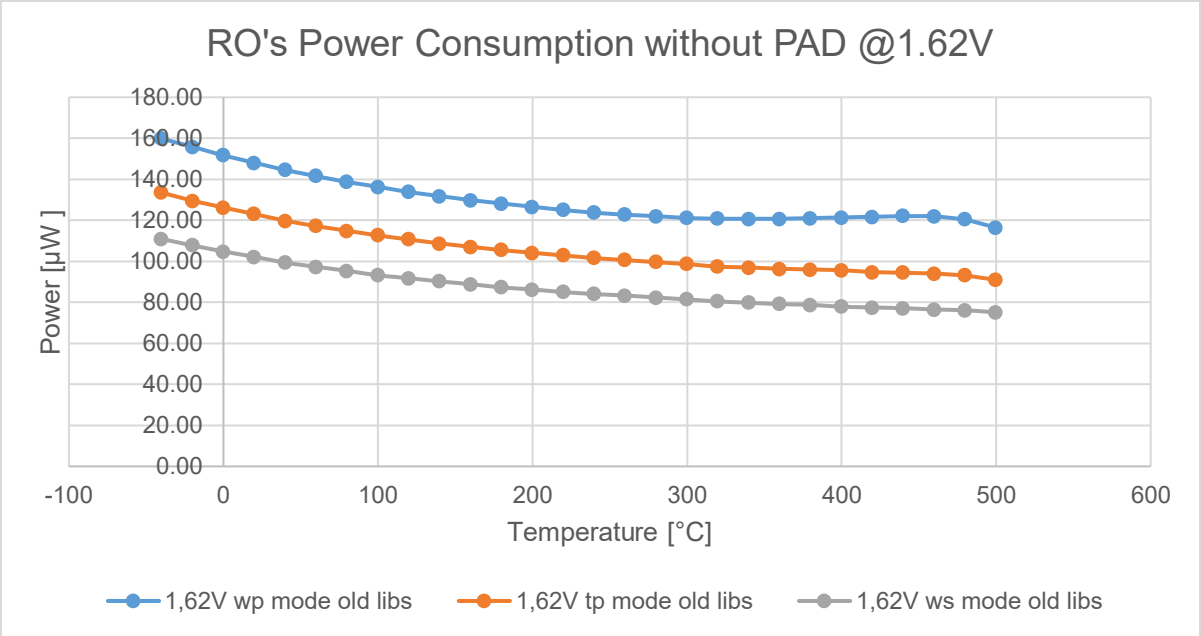


Figure 25: RO without PAD power consumption driven at 1.62V

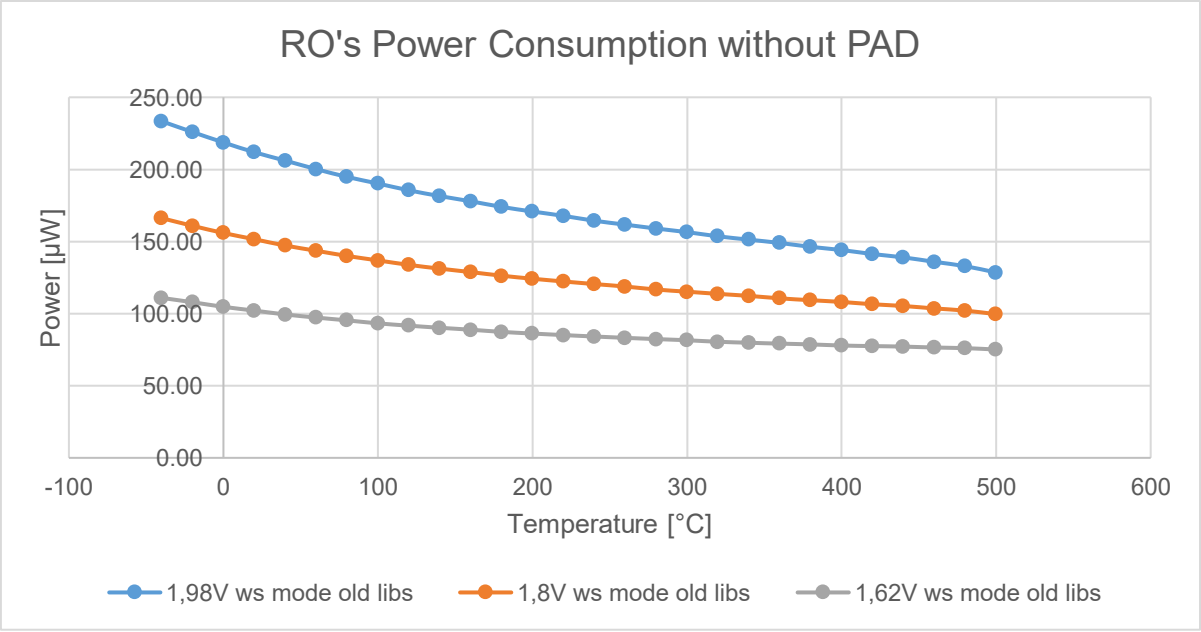


Figure 26: RO's consumed power vs temperature

After seeing the consumption trend without the digital PAD, in the follows, in **Figure 27**, the RO's power consumption of the older model and, in **Figure 28**, the power consumption of the newer one using the digital PAD. Differently from what seen for the RO's frequencies, the power consumption is quite different comparing the two models. In the older model the power consumption increases increasing temperature while in the newer model it decreases till about 100°C, stays almost constant up to 300°C and then resumes growing in an exponential way.

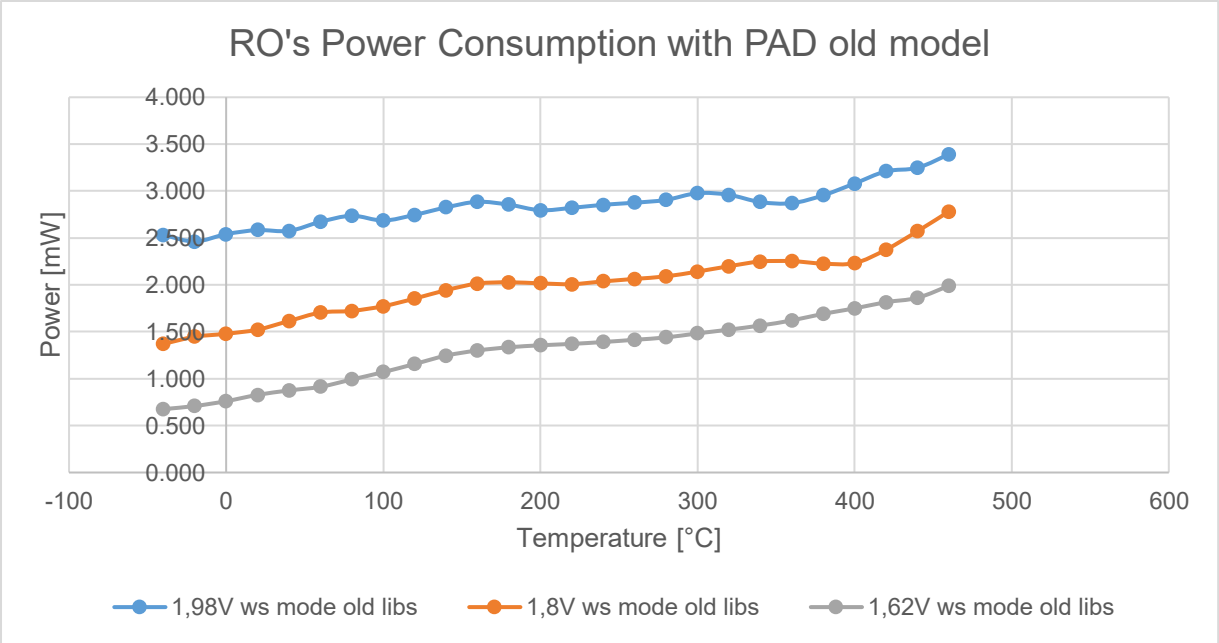


Figure 27: RO's consumed power vs temperature

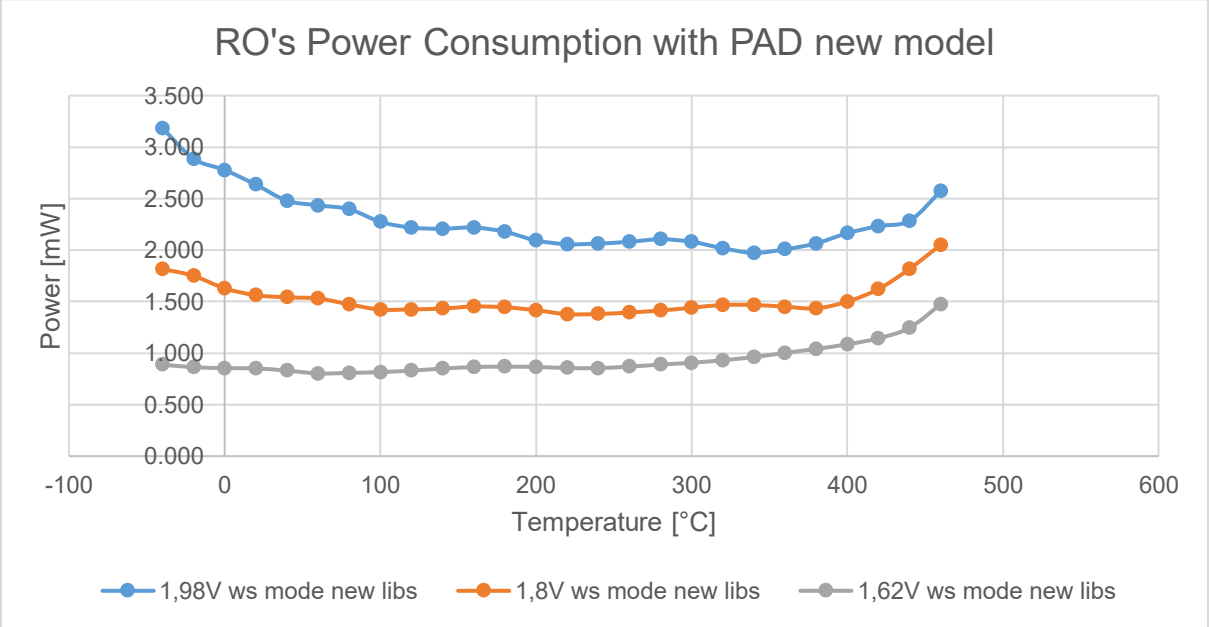


Figure 28: RO's consumed power vs temperature

The differences that catch immediately the eyes are: the order of magnitude that changes from few hundreds of µW without the digital PAD up to few mW including it, and the different trend. Regarding the RO without the PAD, we saw that the power consumption decreases following the frequency's trend, while, inserting the digital PAD, it increases with the old models, instead with the newer one it decreases at low temperatures and increases again at high temperatures.

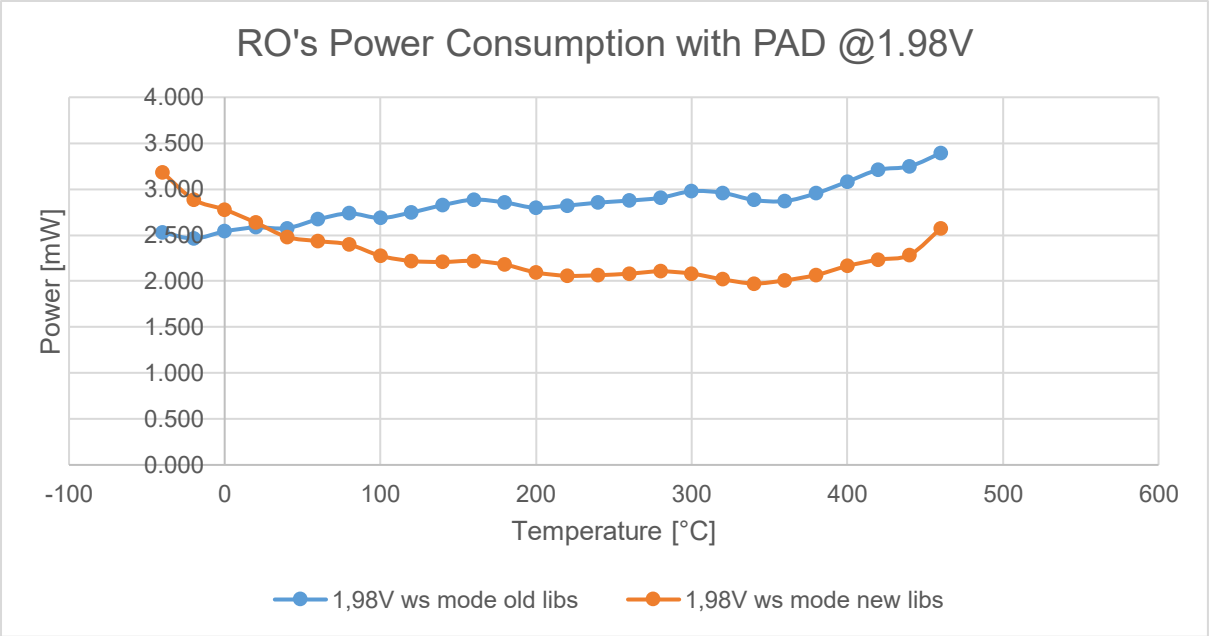


Figure 29: RO's consumed power vs temperature driven at 1.98V

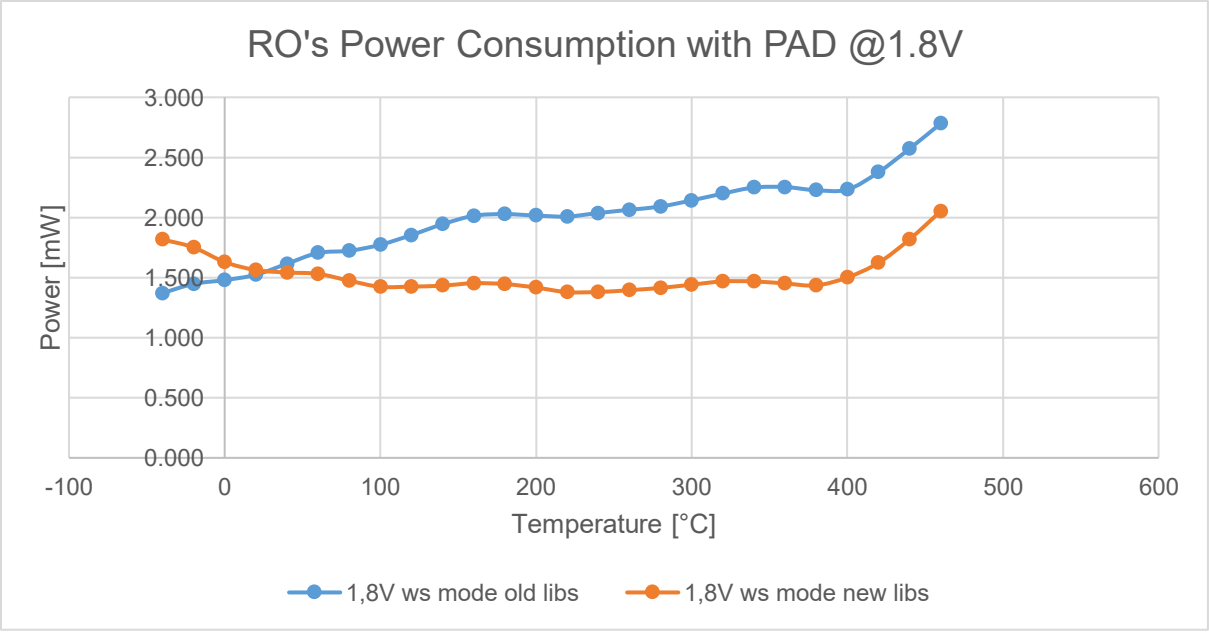


Figure 30: RO's consumed power vs temperature driven at 1.8V

In **Figure 29**, **Figure 30** and **Figure 31** are shown the detailed comparisons between the different models for 1.98V, 1.8V and 1.62V respectively. Have been used three different graphs, one per each supply voltage, in order to highlight the differences that instead of using one single graph would be more difficult to be appreciated.

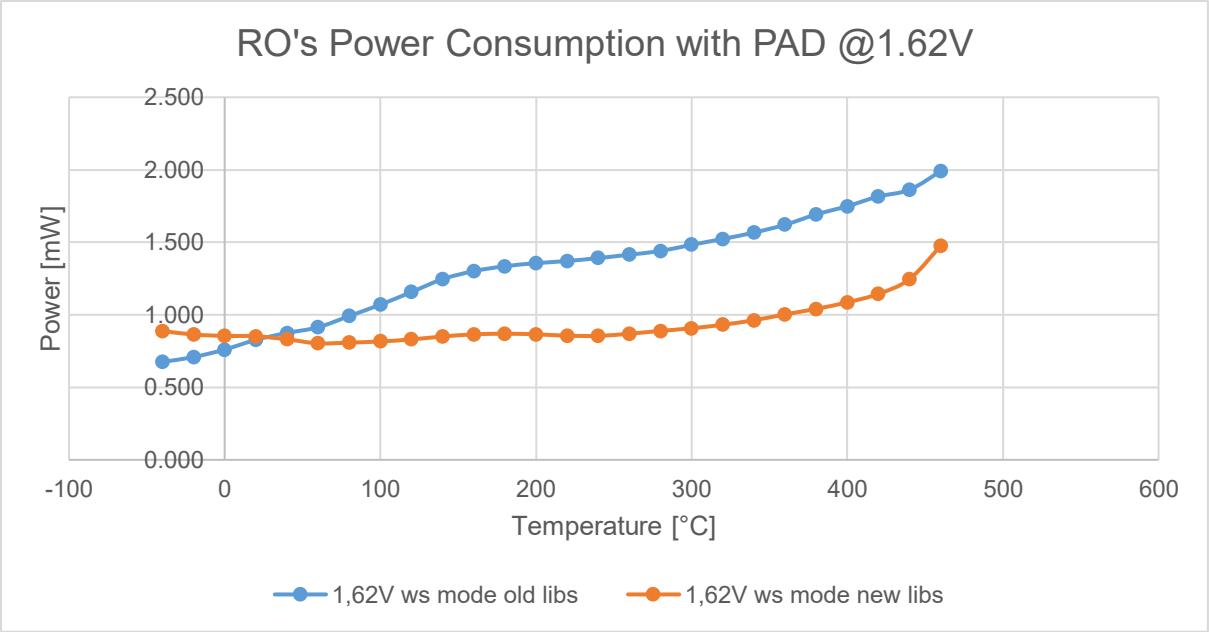


Figure 31: RO's consumed power vs temperature driven at 1.62V

In **Figure 32** is depicted the leakage current trend as a function of temperature. As we can notice in the graph, leakage current is a bottleneck when working in high-temperature environment because it increases in an exponential manner with temperature. This characteristic could lead the full system, in terms of energy consumption. In the worst case could cause failure in components that have to work at high temperatures for long period. As shown in the graph, leakage current starts from few pA at -40°C up to few µA at 500°C.

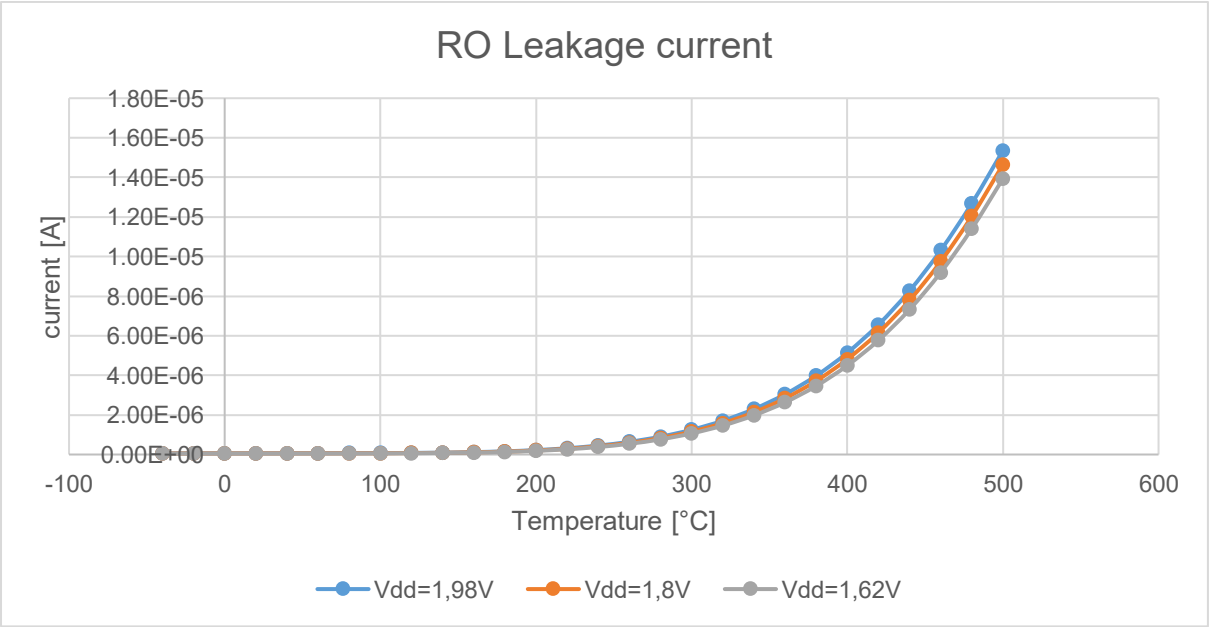


Figure 32: RO's leakage current vs temperature

4.4 Fan-out of 4

FO4 is a process-independent delay metric used in digital CMOS technology to understand which design has the better fabrication process. Because scaled technologies are all inherently faster, circuit performance can be more fairly compared using the FO4 as a metric.

As represented in **Figure 33**, FO4 is the delay of an inverter driven by an inverter 4x smaller than itself and driving an inverter 4x larger than itself. Both conditions are necessary since input signal rise/fall time affects the delay as well as the output loading.

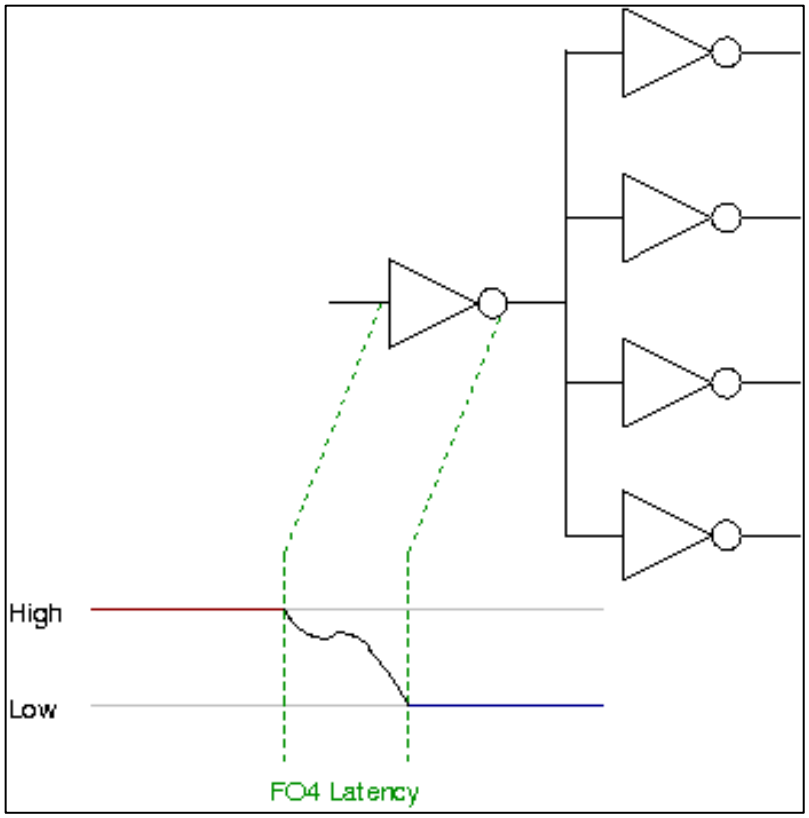


Figure 33: Fan-out of 4 latency

4.4.1 Simulation results

Unlike what done for the RO, in this case, there aren't simulations with the newer models, done just for the RO in order to have a better comparison with the device tests. Newer models apart, the same simulations done for the RO have been done for the FO4.

All the results are reported in the following: in **Figure 34** is represented how the FO4 delay varies increasing temperature. As already seen in the case of the RO, increasing temperature we have a loss in performance that increase the FO4 delay in a linear manner with temperature.

The trend shown in the graphs is the opposite compared to the RO one, **Figure 20**, because, now, are shown the delays and not the frequencies. The delay reported in the

graph (t_p) is the average between the LOW-TO-HIGH and HIGH-TO-LOW delays, which are evaluated from 50% to 50% of input and output transition respectively.
Also in this case, during simulations, the simulator had shown a series of warnings starting from 269°C. The reasons of the warnings, as previously discussed, were some voltages clamped due to the overcome of the minimum value because of the temperature effect.

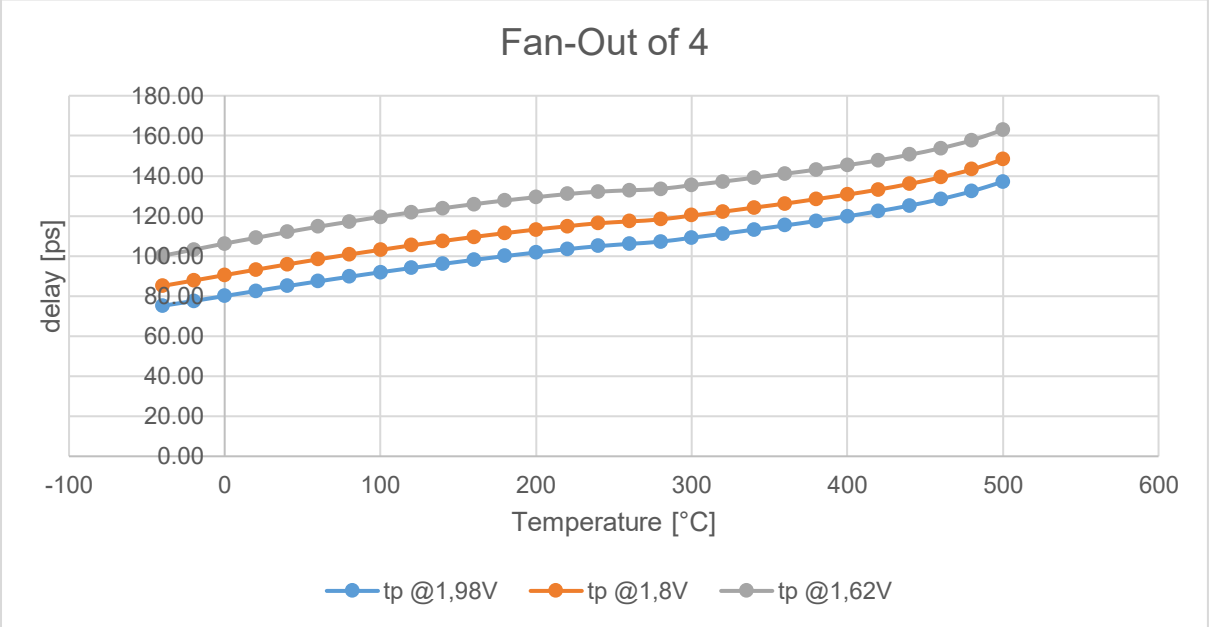


Figure 34: FO4 vs temperature

In **Figure 35** is depicted the FO4 power consumption which slightly increases, but remaining comparable, up to 280°C and after that increases a little bit more taking the form of an exponential curve.
Finally, in **Figure 36**, the FO4 leakage current is depicted and we can notice that, as for the RO, the leakage increases in an exponential manner increasing temperature. It goes from few pA at -40°C up to few µA at 500°C.

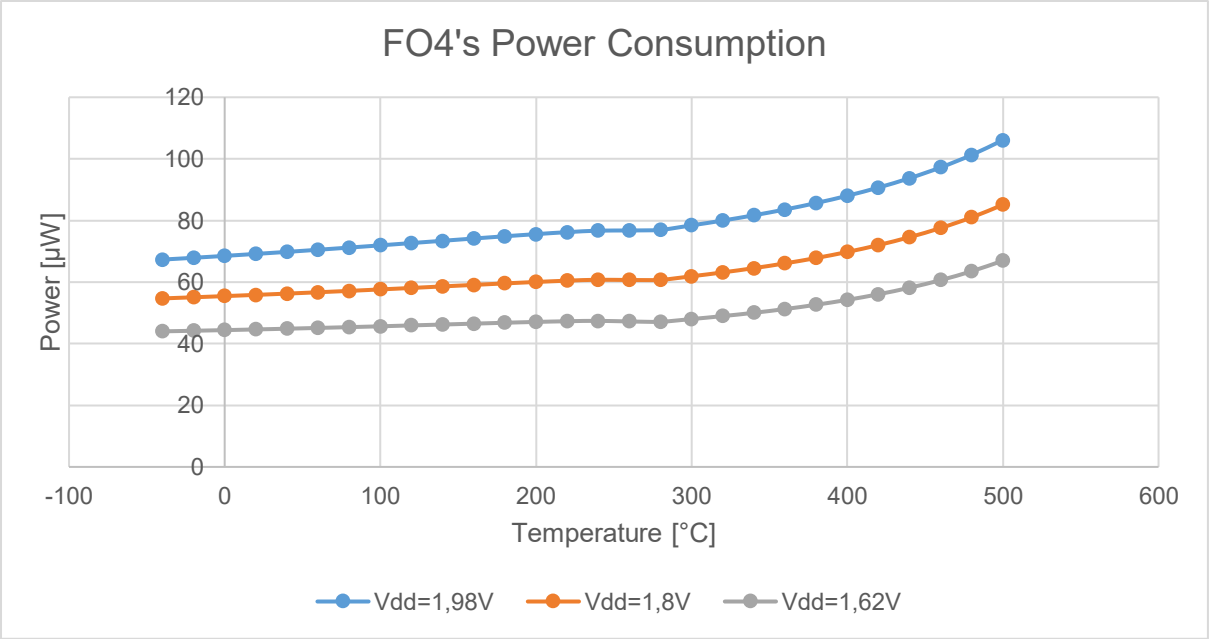


Figure 35: FO4's consumed power vs temperature

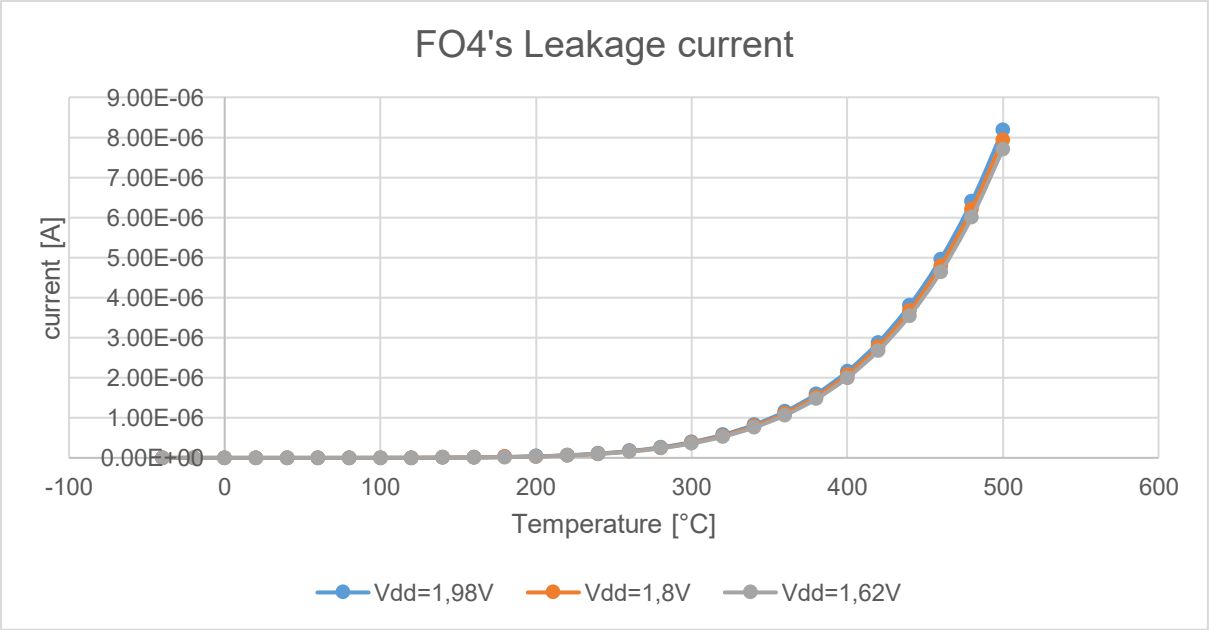


Figure 36: FO4's leakage current vs temperature

4.5 Critical Path Replica

Before starting to talk of Critical Path Replica, also known as CPR, would be better make a short comparison between Dynamic Voltage Scaling (DVS) and Adaptive Voltage Scaling (AVS).

4.5.1 Dynamic Voltage Scaling

DVS is a power management technique in computer architecture, where the voltage used in a component is increased or decreased, according to the throughput requirements [11]. DVS to increase voltage is known as overvolting, DVS to decrease voltage is known as undervolting. Undervolting is done in order to conserve power, particularly in mobile device, where energy comes from a battery and thus is limited. Overvolting is done in order to increase computer performance or, in other case, to increase reliability. The architecture of a generic DVS system has a performance manager, a phase-locked loop and a voltage regulator. The performance manager block uses a software interface in order to predict the performance requirements of the next task. Once the determination of the power requirement is done, the voltage and the frequency are set by the performance manager in order to finish the task. The phase-locked loop accomplishes the frequency scaling depending on the target frequency set by the performance manager. Similarly, the voltage regulator is programmed to scale the supply voltage so as to achieve the target voltage for the task. The open-loop DVS systems employ the one-to-one mapping of the voltage to frequency to perform the voltage scaling. The frequency-voltage pairs are stored in lookup table and are obtained as per the determined task needs. In case of the open-loop DVS systems the frequency-voltage relationship is determined by considering the chip characterization at worst case conditions so as to guarantee the robust operation under the temperature and process variations. Thus in order to accommodate for the worst case variations there is a lot of power margin left by the open-loop DVS systems for power scaling. This margin is not lost in closed-loop systems, Chapter **4.5.2**, because they employ a feedback mechanism that keeps under control the actual on chip conditions.

4.5.2 Adaptive Voltage Scaling

AVS is a closed-loop dynamic power minimization technique that reduces power based on the actual operating conditions on the chip (the power consumption is continuously adjusted during the run time of the chip) [12]. Typically, the design of any chip is done such a way it meets most demanding application throughput requirements under worst case operating conditions. AVS is beneficial compared to the conventional DVS approach because AVS eliminates the excess power margins that are present in the open loop DVS systems due to the fixed voltage-frequency relations employed in those systems. In AVS technique the chip's exact process corner is determined either during the manufacturing test or during runtime and the appropriate voltage-frequency relationship is determined, which will be used during the dynamic voltage and frequency scaling operations. This eliminates the extra margin that will be present if the worst case operating conditions are taken into account while the chip is actually operating under typical conditions. The closed-loop voltage scaling system utilizes on chip circuit structures to provide feedback required to adaptively track the actual silicon behavior. One of the most commonly used approach is to use a ring oscillator that operates at the same voltage as that of the rest of the chip. The voltage-frequency relationship for the chip at that particular frequency is determined by the frequency of the ring oscillator.

To check the operating frequency of the ring oscillator and to decide the operation to do, a Critical Path Manager (CPM) is needed.

4.5.2.1 Critical Path Manager

A Critical Path Manager (CPM), **Figure 37**, is composed by a Toggle Flip-Flop (TFF), one or more Critical Path Replica, and a Timing Checker [13].
As can be seen in the picture, the Toggle Flip-Flop is done using a simple FF, a feedback and an Inverter. In this configuration, it produces an alternate input signal at every clock cycle.
Whenever the input signal enters, it goes through all of the CPRs in parallel and the worst delay appears at the output.
Finally, the output of the CPRs reaches the Timing Checker, which is composed of FFs, XORs and Tunable Delays, and it generates the three bit codes P[2:0]. Because the CPM samples the delay of the CPRs at every clock cycle, it can continuously check the speed of a chip.

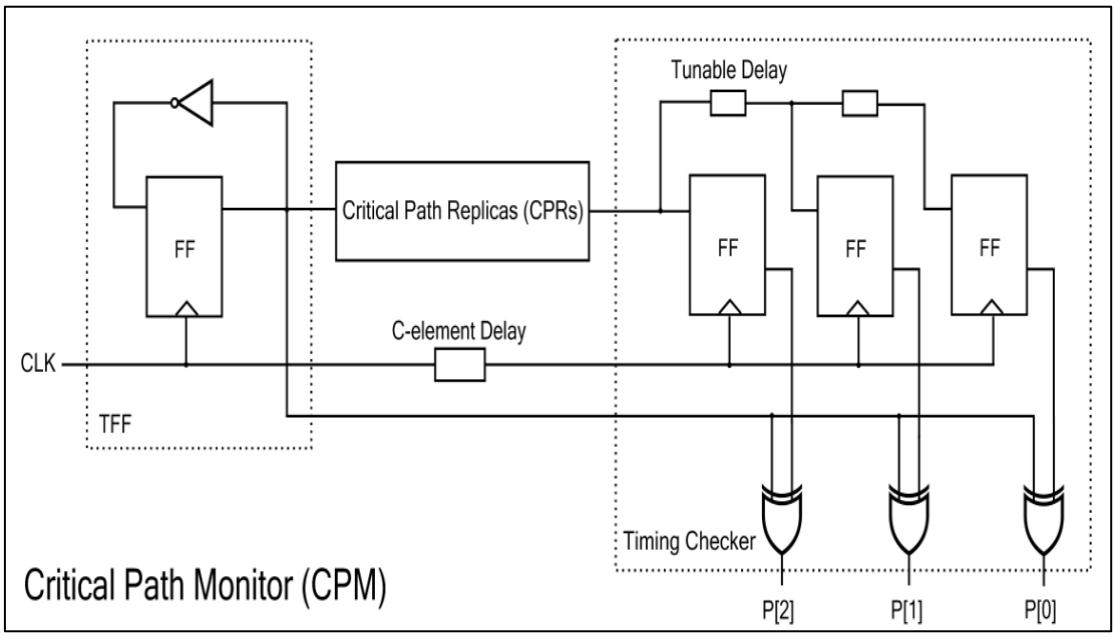
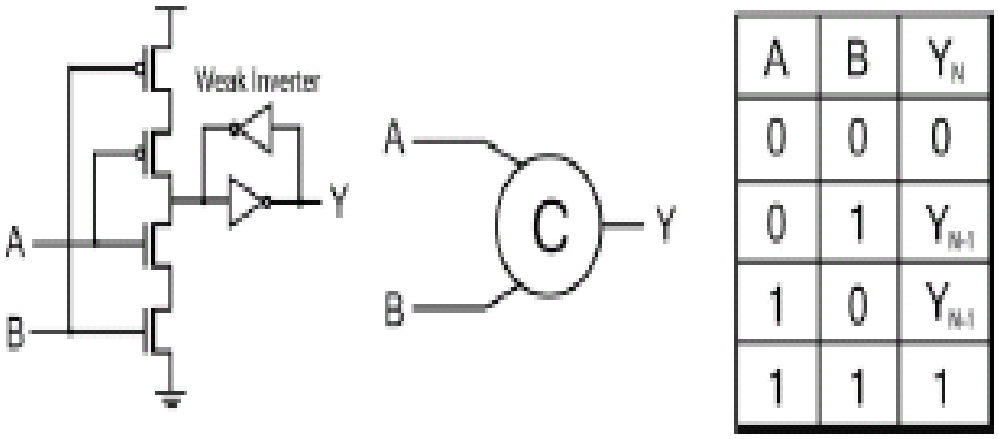


Figure 37: Critical Path Monitor

The latest delay path only affects the final delay, because the C-elements, **Figure 38**, automatically select the longest delay among CPRs' delay.
In order to compensate for the C-element stack delays in the configuration, the same number of C-elements is inserted into the clock network as shown in **Figure 37**.
The output code, generated by the Timing Checker, is used to inform the Frequency Controller on how to manage the working frequency.



A	B	Y_N
0	0	0
0	1	Y_{N-1}
1	0	Y_{N-1}
1	1	1

Figure 38: C-element, symbol and logic function

P[2:0]	Delay of CPRs	Frequency Control
{0,0,0}	Fast	↑
{0,0,1}	Appropriate	–
{0,1,1}	Slow (Safety Margin)	↓
{1,1,1}		

Figure 39: Results of the CPM and frequency control

In **Figure 39** is depicted the table that shows how the Frequency Controller controls frequency depending on the code coming from the CPM.
A description of all the possible actions is reported below:

- If the CPR delay is faster than that of the clock time, when P[2:0] is {0,0,0}, the system will increase its clock frequency in order to exploit the timing margins;
- If slower than the clock cycle, when P[2:0] is {0,1,1}, the system will decrease its clock frequency to prevent real critical paths to fail;
- The three-bit output of the monitor leads to an intermediate state where the values of the P[2:0] is {0,0,1}, indicating that this is an optimal point for the system to remain stable;
- The state where the P[2:0] is {1,1,1} exists for safety margin
    - The safety margin can be controlled by Tunable Delay, which is composed of various delay segments.

To better control the chip's working condition, CPMs can be located in the areas where variation is likely to occur.
For the multiple CPM approach, all of the CPMs' outputs are ORed and transferred to the frequency controller.

As said before, a critical path (CP) of a system can be duplicated using four simple circuit:

- A Ring Oscillator;
- A Fan-Out of 4 delay;
- A delay line;
- A real copy of the Critical Path.

4.5.3 Configurable Critical Path Replica

In **Figure 40** is shown a configurable CPR, DELs (path on the left side) are delay cells with a relative large delay time compared to BUFFs (path on the right side) [14].
The first part is used to a coarse-grained regulation of the path length while the second part is used to a fine-grained adjustment. The length of the CPR can be fine-grained re-configured depending on the operation environment.
The first part is composed of: six delay cells (DELs) and the first multiplexer MUX1, while the second part is composed of: six buffers (BUFFs) and the second multiplexer MUX2.

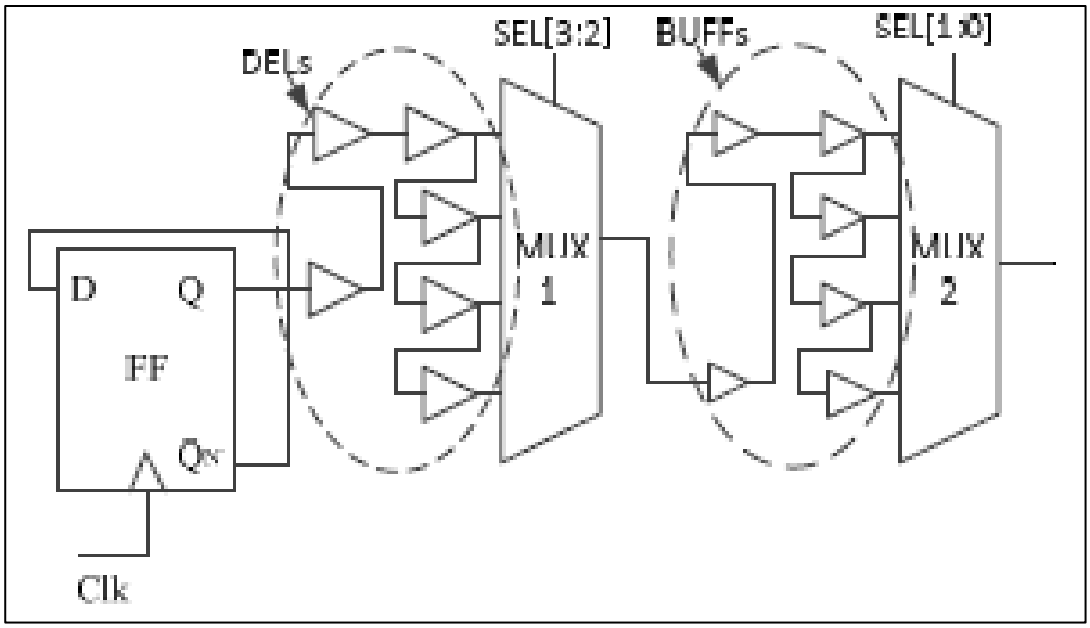


Figure 40: Configurable Critical Path Replica

The big advantage of the configurable CPR is that even after circuit fabrication, using SEL[3:0], the path length can still be adapted depending on the different operation conditions.
The selection of CPR numbers is critical because the CPRs should be able to cover the whole chip, and at the same time, without causing large area and power overhead.

4.5.4 Simulation results

This chapter shows the results obtained during CPR simulation, like previously done in the case of the FO4, Chapter **4.4.1**. In the follows two different results are presented, each

of them was obtained configuring properly the tunable CPR in order to reach frequencies and delays comparable with the ones obtained from the RO and from the FO4.

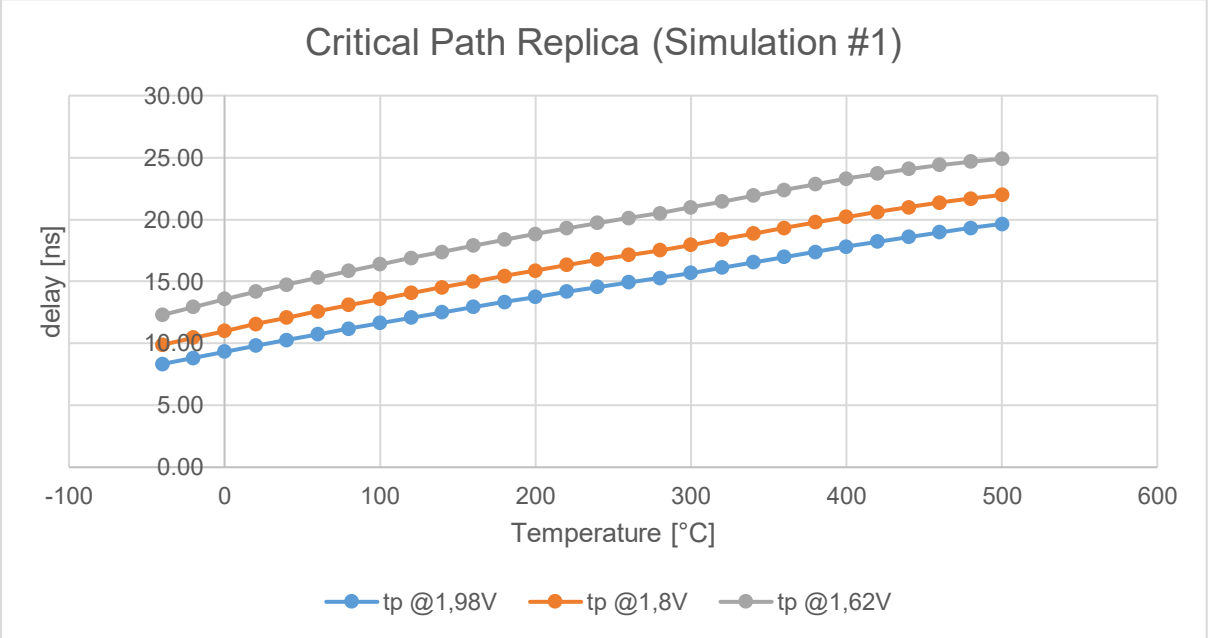


Figure 41: CPR's delay vs temperature (Simulation #1)

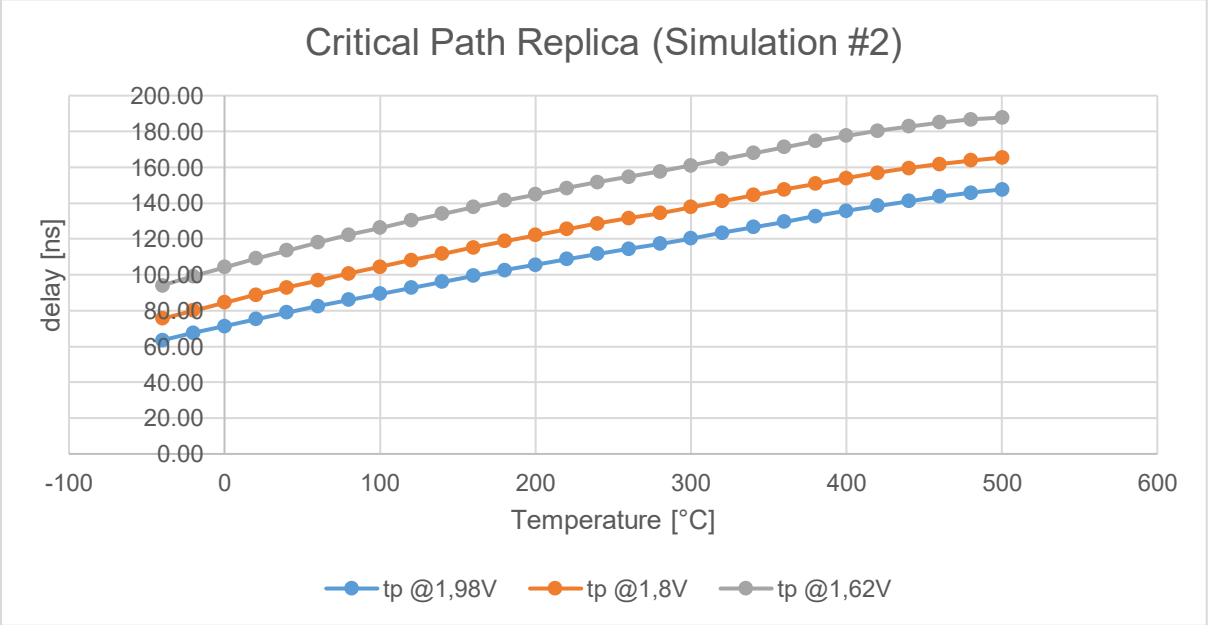


Figure 42: CPR's delay vs temperature (Simulation #2)

As mentioned in the FO4 case, the delay (t_p) is the average between the LOW-TO-HIGH and HIGH-TO-LOW delays, which are evaluated from 50% to 50% of input and output transition respectively.

In **Figure 41** and **Figure 42** is depicted how the delay varies increasing temperature. From the graph it is clear to note that the CPR delay increases in a linear manner with respect to temperature.

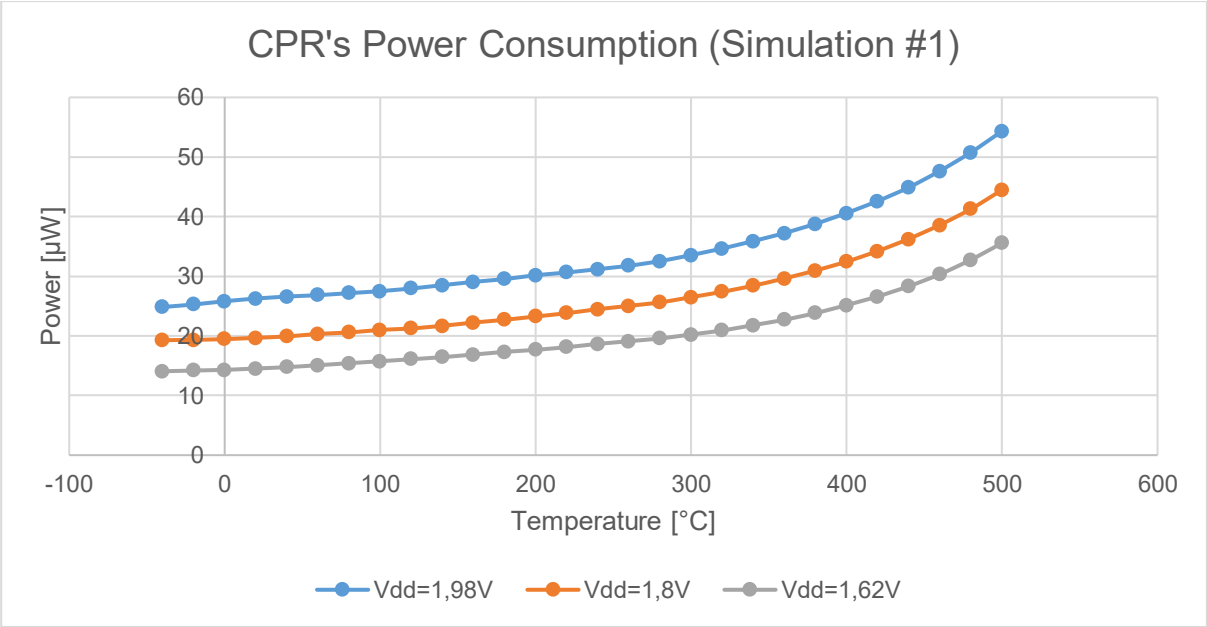


Figure 43: CPR's consumed power vs temperature (Simulation #1)

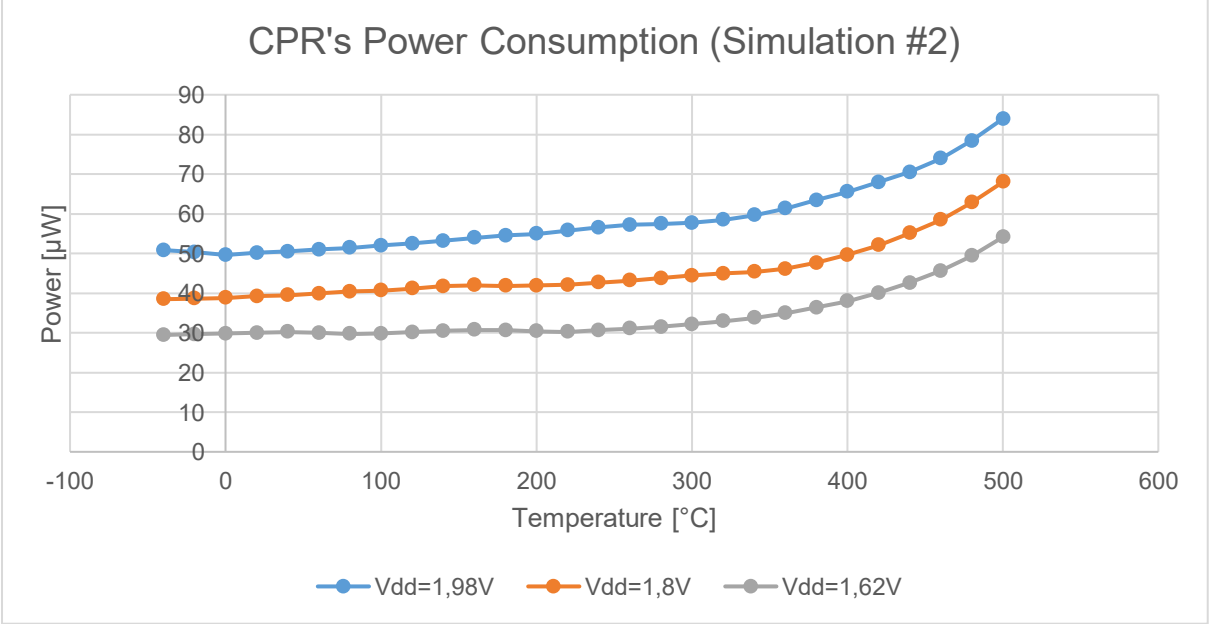


Figure 44: CPR's consumed power vs temperature (Simulation #2)

In the case of the power consumption, **Figure 43** and **Figure 44,** the trend is like the one obtained for the FO4, it remains almost constant up to 300°C and then starts to increase at higher temperatures.

Like in the previous simulations, also in the CPR case (simulation #1), **Figure 45**, leakage current increases in an exponential manner increasing temperature. The current leak starts from few pA at low temperatures up to few µA, reaching considerable values at temperatures higher than 300°C.
From what was seen until now, we can say that, as regards the power consumption, it increases at high temperatures because of the critical leakage current shown by the Partially Depleted SOI technology. This would be a real problem in the case of more complicated circuits, which must operate for long period at high temperatures, used for applications in which the power consumption is one of the bottlenecks.

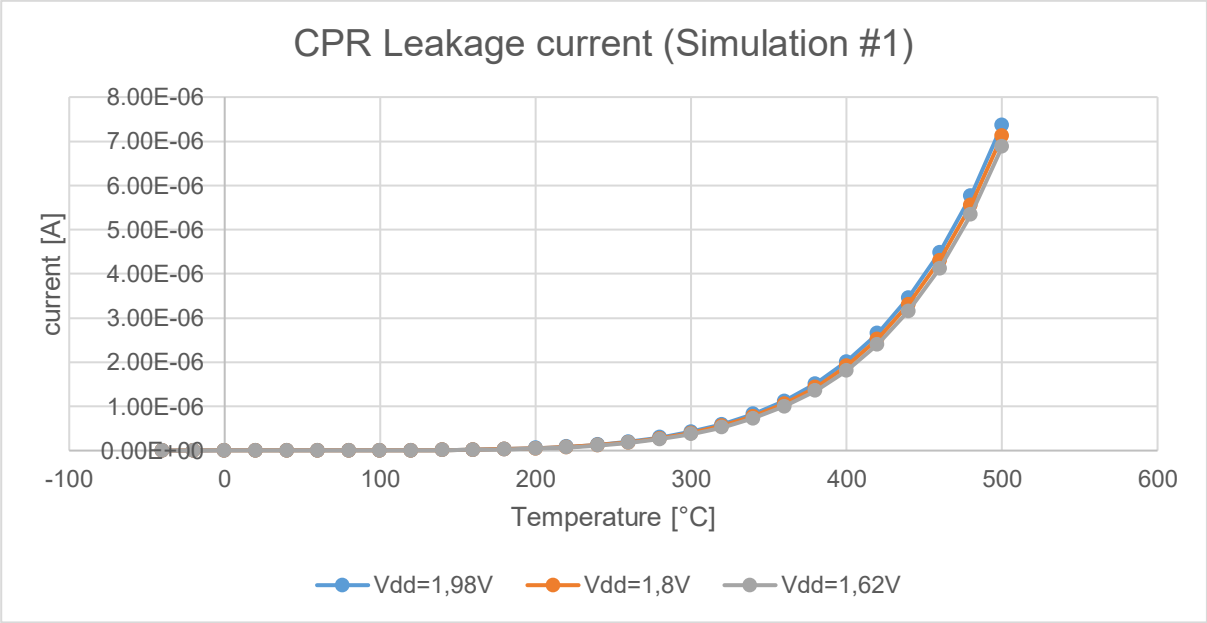


Figure 45: CPR's leakage current vs temperature

4.6 Comparison between RO and tunable CPR

Since a critical path can be duplicated using a RO or a tunable delay, this chapter shows a comparison of performances and power consumptions of the RO and CPR. To make it possible, since the CPR gives us a delay metric, is taken into account the t_p of the CPR, and using the following formula:

$$f = \frac{1}{t_p}$$

the tunable CPR is tuned so as to obtain a frequency, as much as possible, similar to the one of the RO.
As already mentioned in the chapter dedicated to the RO's simulations, Chapter **4.3**, to make possible the power consumption comparison, is taken into account the RO without the digital PAD, which has the same order of magnitude in terms of power consumption.

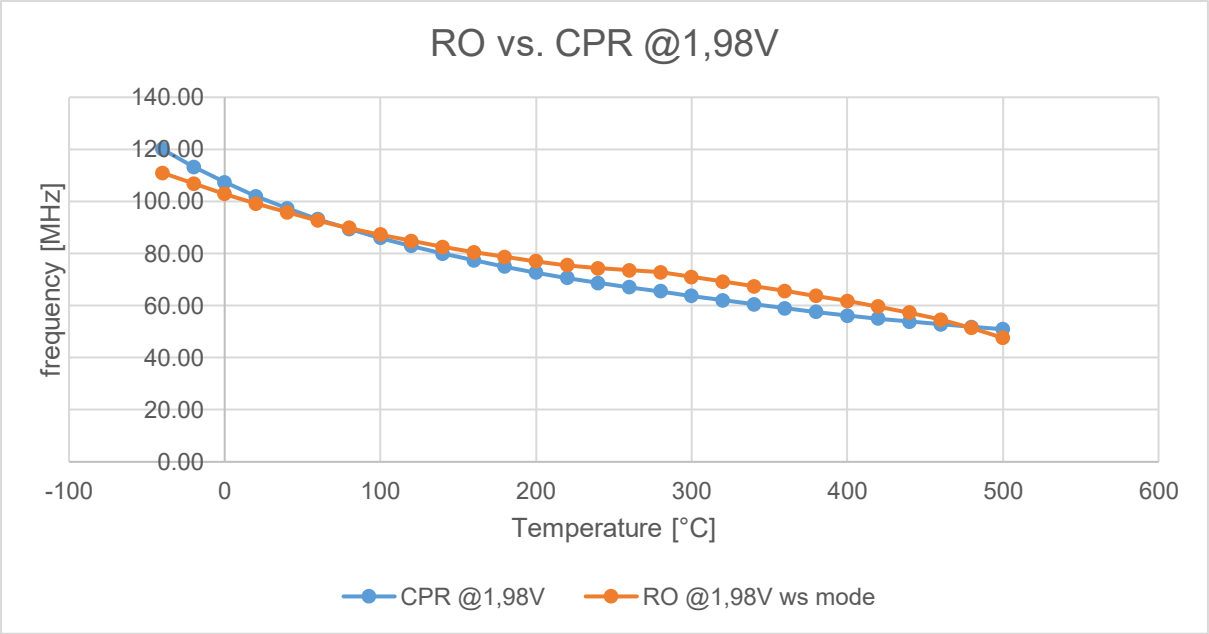


Figure 46: RO vs. CPR frequency as a function of temperature driven at 1.98V

In **Figure 46** and **Figure 47** are represented frequency and power consumption of the RO and of the tunable CPR driven at 1.98V. From a performance point of view, in a CPM the CPR could be designed interchangeably using a RO or a tunable delay, because the working frequencies are almost the same and both follow the same trend. This is not true in terms of power consumption; the tunable CPR definitely consumes less. The CPR's power consumption is almost constant up to 300°C, and slightly increases at higher temperatures. In the case of the RO, it consumes a lot at very low temperatures and decreases, in a way almost linear, increasing temperature, but still remaining more power consuming than tunable CPR.
In this particular case, the tunable CPR, can be defined better and preferable compared to the RO.

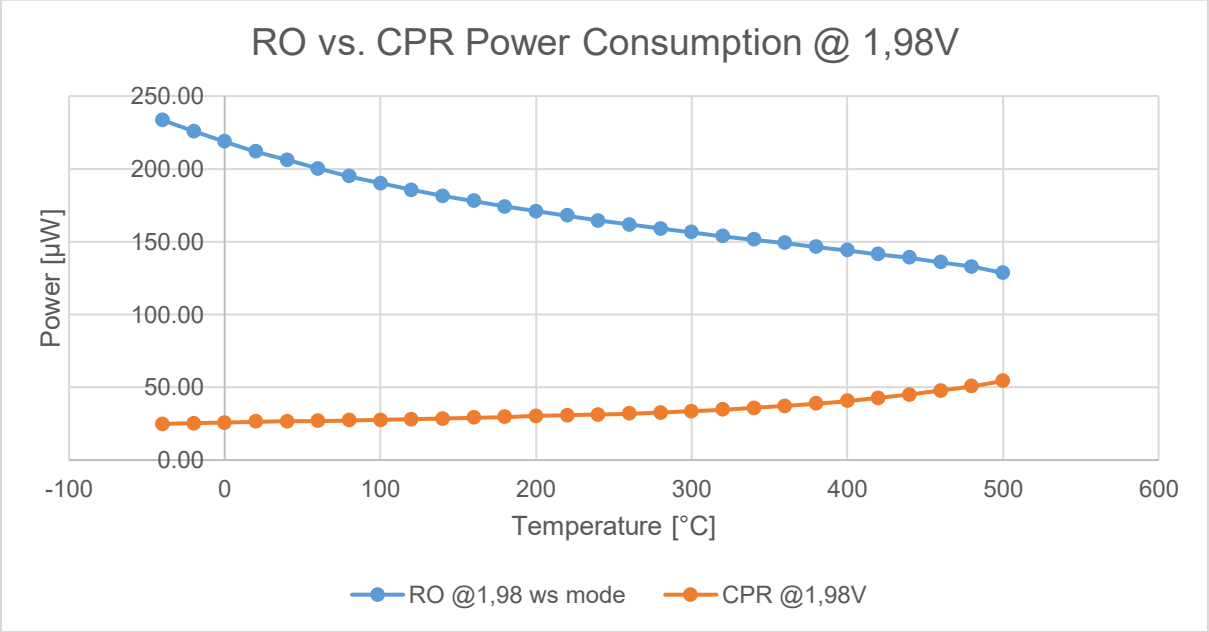


Figure 47: RO vs. CPR power consumption as a function of temperature driven at 1.98V

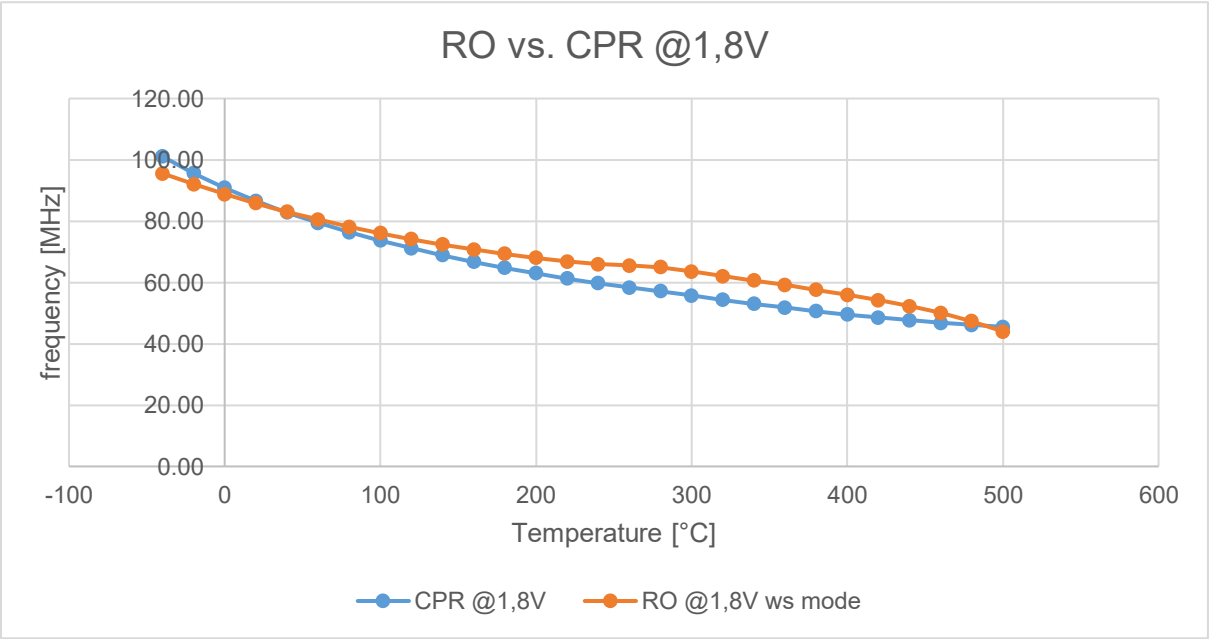


Figure 48: RO vs. CPR frequency as a function of temperature driven at 1.8V

Figure 48, **Figure 49**, **Figure 50** and **Figure 51** show the comparisons of frequencies and power consumptions between RO and tunable CPR when they are driven using a power supply equal 1.8V and 1.62V respectively.

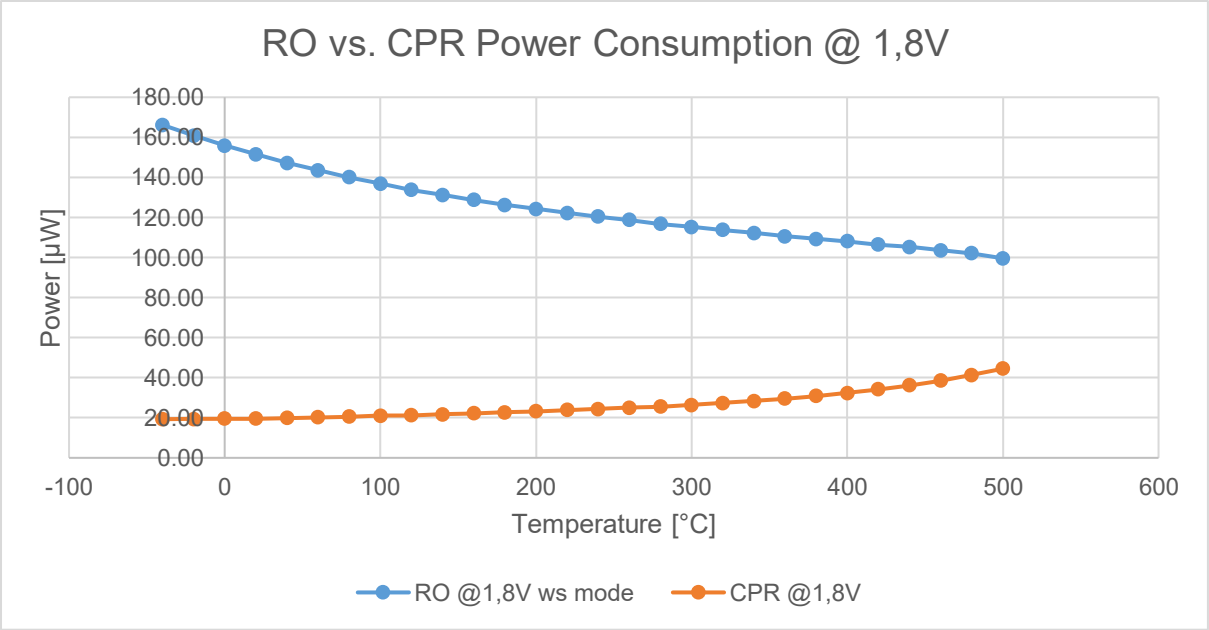


Figure 49: RO vs. CPR power consumption as a function of temperature driven at 1.8V

Like in the previously discussed circuits' simulations, when the circuits were powered with 1.98V, the RO's and CPR's frequencies are comparable. Only in the range 200°C÷400°C, when the circuits are driven at 1.62V, the difference becomes slightly larger. In both the case the power consumption is favorable to the CPR, because, for each simulated temperature, it is smaller compared to the one of the RO.

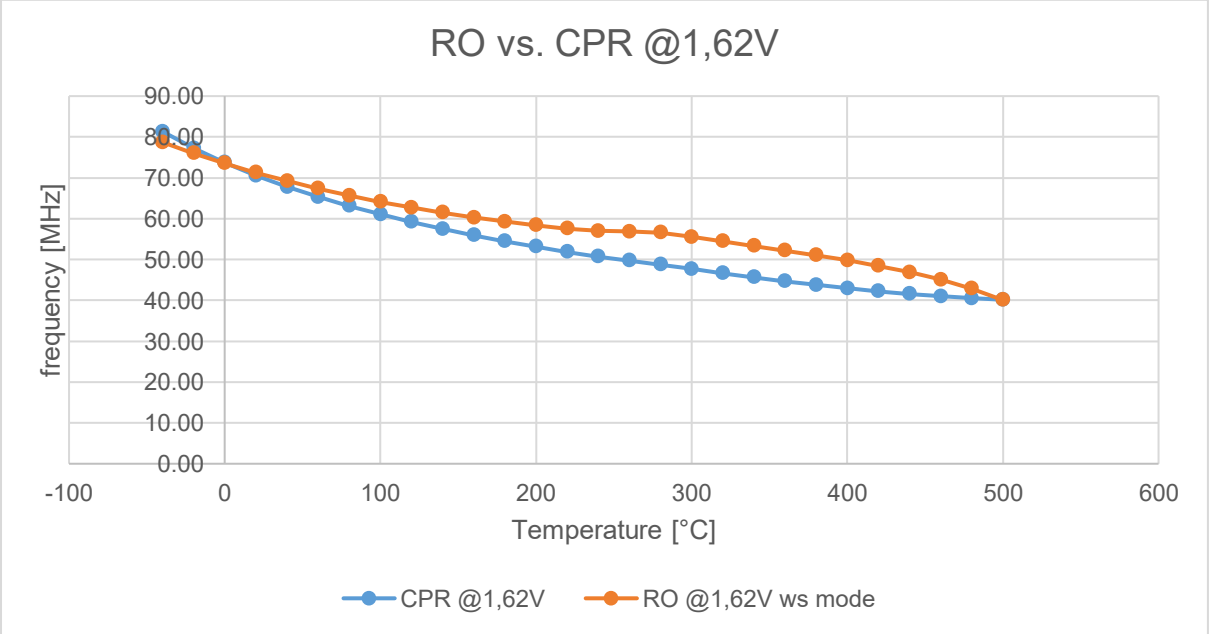


Figure 50: RO vs. CPR frequency as a function of temperature driven at 1.62V

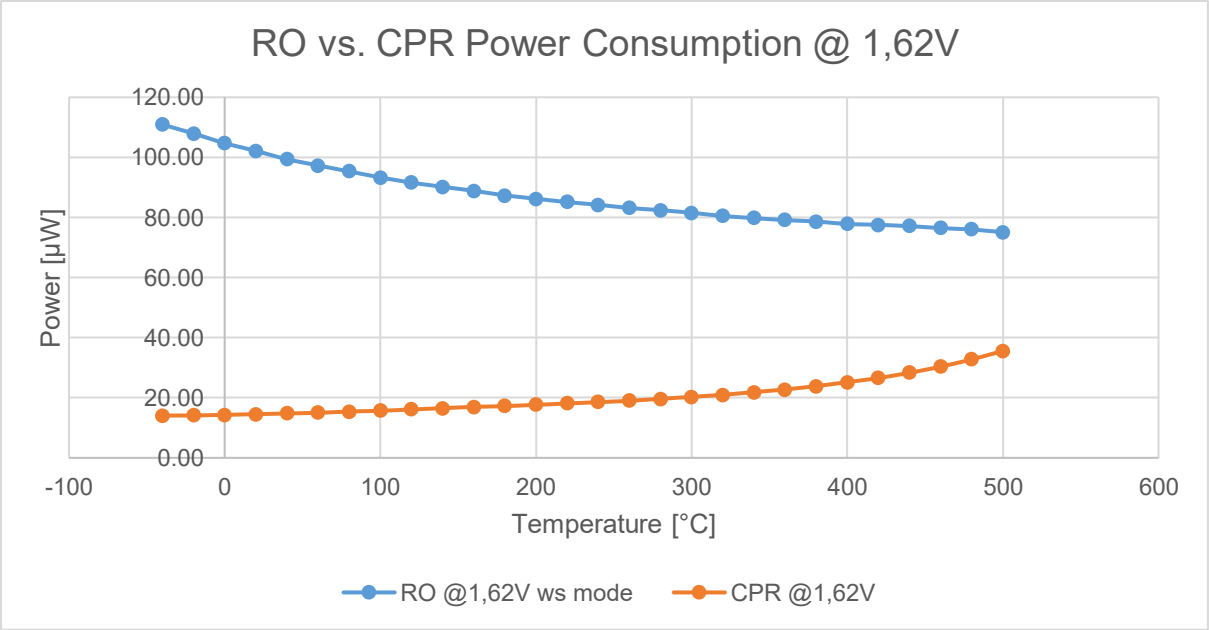


Figure 51: RO vs. CPR power consumption as a function of temperature driven at 1.62V

4.7 Comparison between FO4 and CPR

In addition to what was shown in Chapter **4.6**, also the FO4 can be used to duplicate a critical path. For this reason, in this chapter, the tunable delay is configured in a way to have a comparable delay to the one of the FO4.

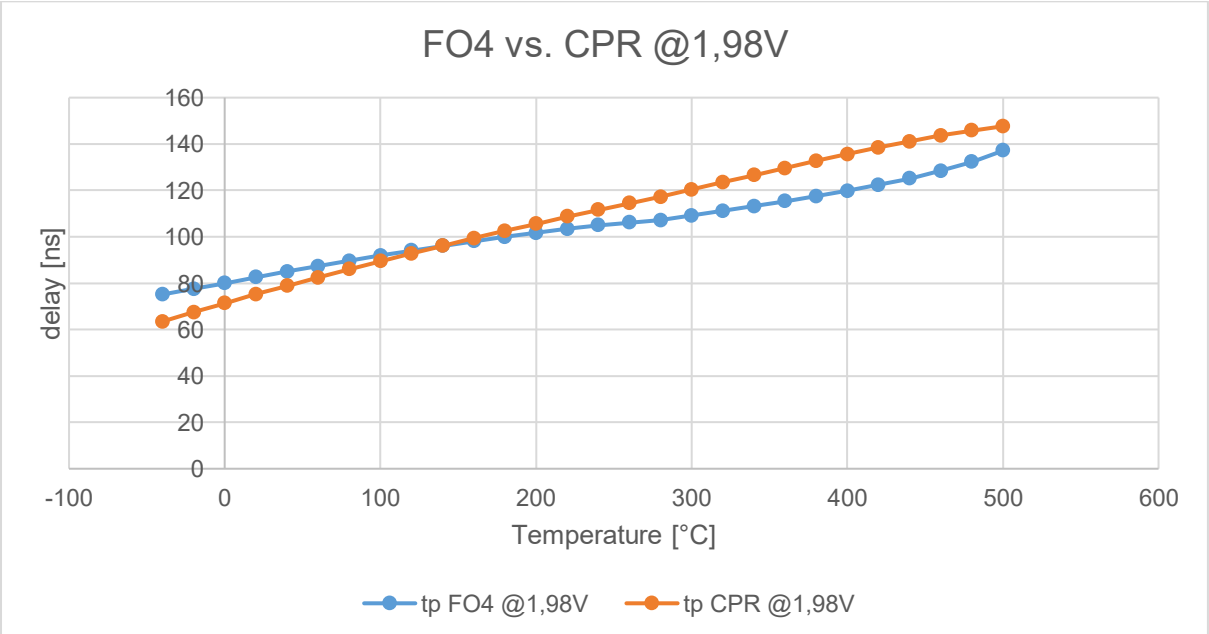


Figure 52: FO4 vs. CPR propagation time as a function of temperature driven at 1.98V

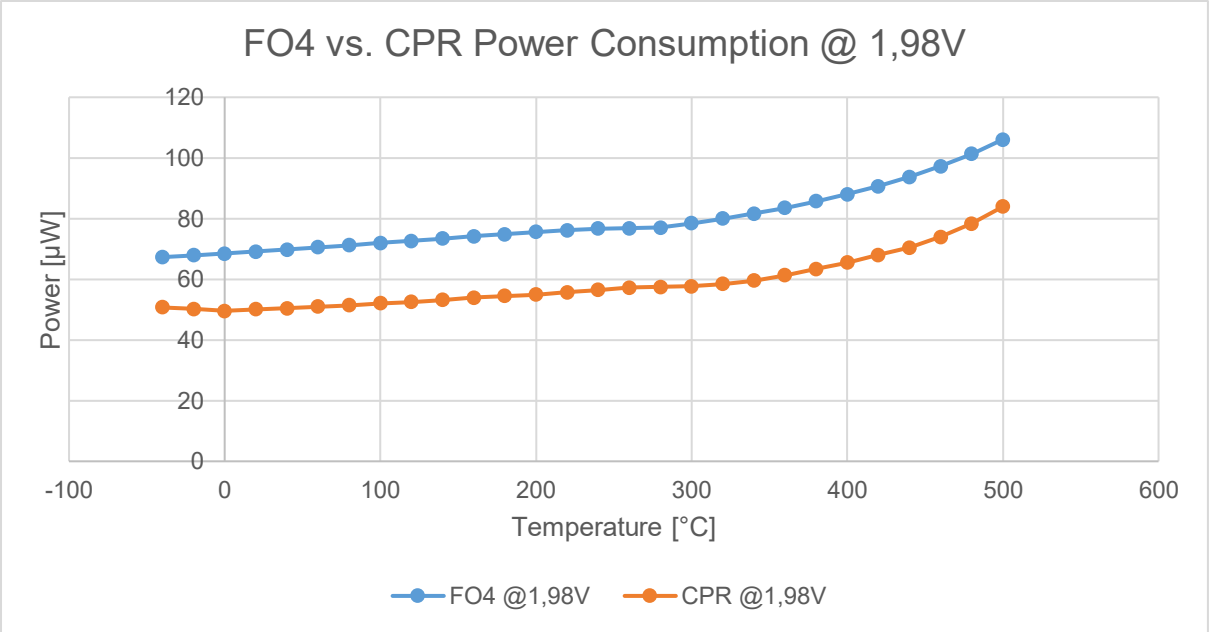


Figure 53: FO4 vs. CPR power consumption as a function of temperature driven at 1.98V

Like in the previous chapter, doing this modification it is possible to make a comparison it in terms of delay and power consumption.

In **Figure 52** is depicted the growth of the FO4's delays and tunable CPR's delays increasing the ambient temperature. The delay of the CPR increases in a linear manner with temperature, while, in the case of the FO4, the trend is not monotonic, then less predictable and less accurate than CPR. **Figure 53** shows the power consumptions of the two circuits, they have almost the same trend. Even speaking in terms of energy efficiency, the CPR is better than FO4 because it consumes less power. In the graph, it can be easily noticed that, there is a difference of about 20µW for each simulated temperature.

In **Figure 54**, **Figure 55**, **Figure 56** and **Figure 57** are represented delays and power consumptions of the FO4 and of the tunable CPR, powered at 1.8V and 1.62V respectively. Even in these two last cases, in which the circuits are driven at lower voltage than 1.98V, are valid the same considerations made previously, that is, the way in which the CPR's delay changes with temperature is more predictable and, at the same time, less power consuming.

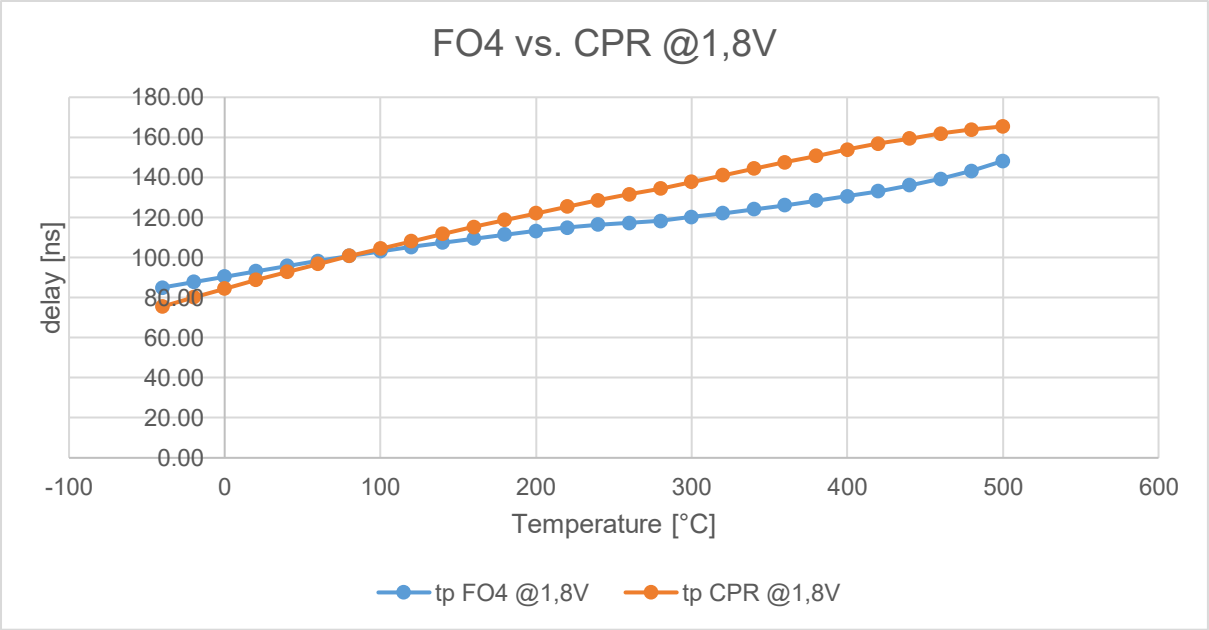


Figure 54: FO4 vs. CPR propagation time as a function of temperature driven at 1.8V

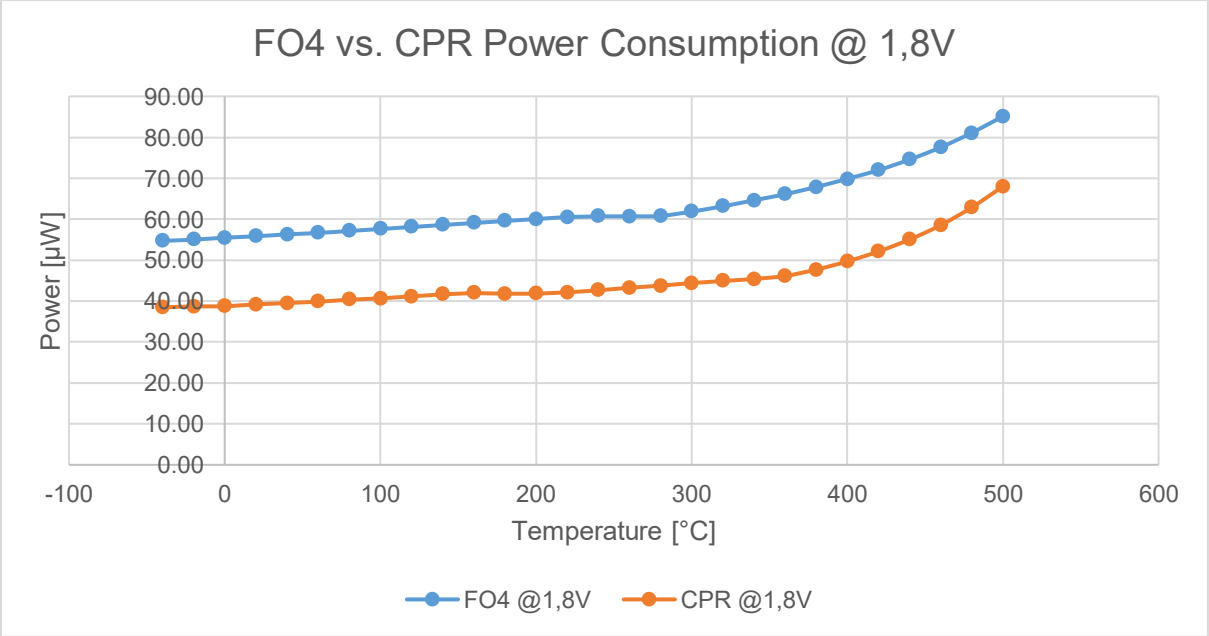


Figure 55: FO4 vs. CPR power consumption as a function of temperature driven at 1.8V

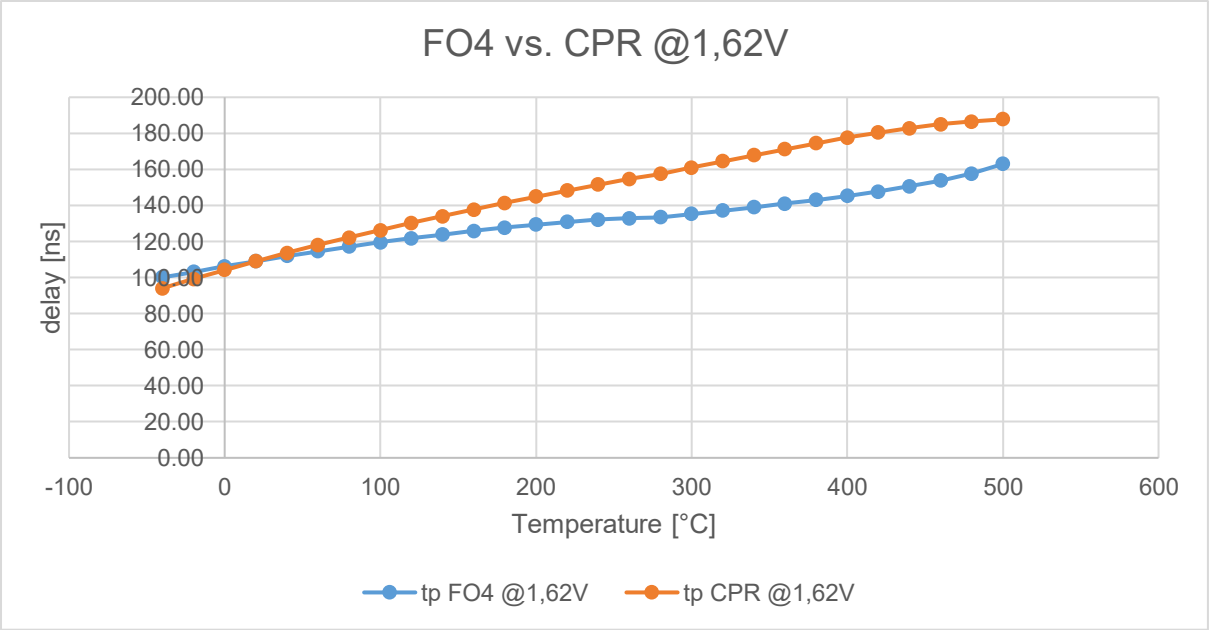


Figure 56: FO4 vs. CPR propagation time as a function of temperature driven at 1.62V

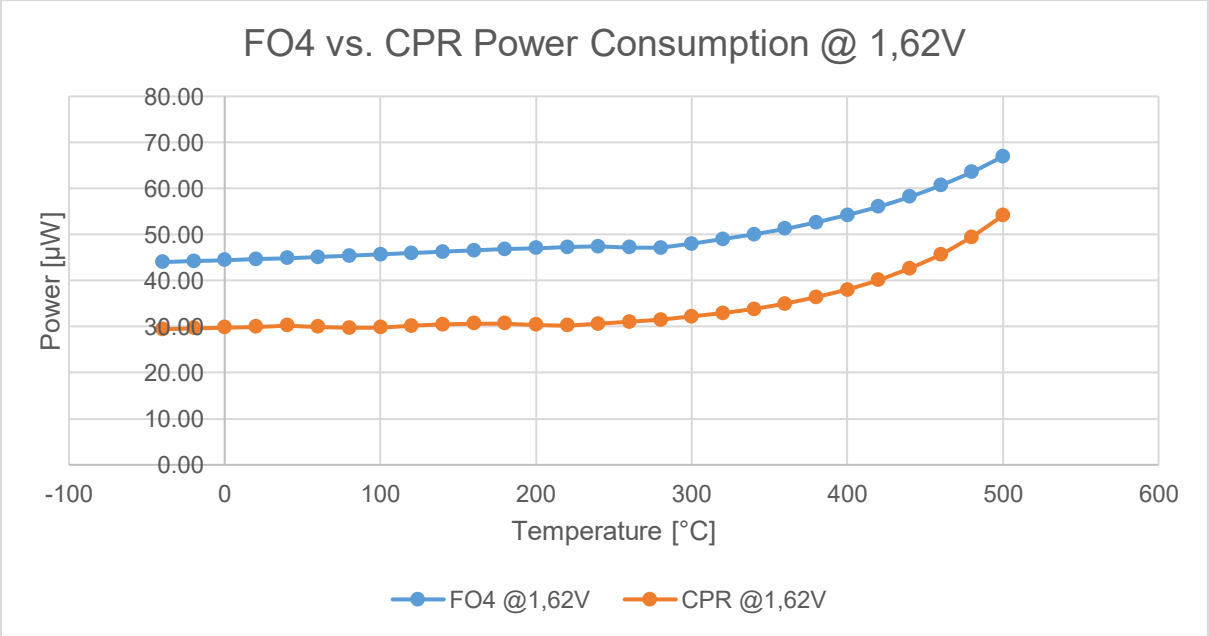


Figure 57: FO4 vs. CPR power consumption as a function of temperature driven at 1.62V

From what seen in Chapters **4.6** and **4.7**, this section can be concluded by saying that the best solution to replicate a critical path is a tunable delay. The tunable delay, in addition to being more accurate and less power consuming, is more flexible. Thanks to selection's signals, it can be configured to duplicate multiple critical paths, using always the same circuit.

5 Tests

This chapter is dedicated to the test made on the physical chip, containing a 99-stages RO. All the test results will be compared with the ones obtained from simulations, for extrapolate, in an accurate manner, the technology behavior under temperatures that do not belong to the datasheet range (above 175°C).

Figure 58: Ceramic package

5.1 Chip presentation

The chip has been developed using the X-FAB technology explained before, and to encapsulate it was used a 28 pins ceramic package, **Figure 58**.
The tests were made, not only, to evaluate if the technology is able to work above the maximum temperature, but, also, to check if the ceramic package, the bonding of the chip inside the package, the connection of the chip's pads to the package's pins and the encapsulation using a cover without windows are adequate to work in harsh conditions, in particular, they have to withstand in environments in which the temperature is 200°C÷250°C and, if it is possible, even higher (300°C÷350°C). **Figure 59** shows a picture of the chip while in **Figure 60** are depicted the connections between pads and pins.
In the following, some chip's characteristics are reported:

- Dimension of the pad: 53µm*65µm;
- Smallest space from center to center: 60µm;
- Metal of the pad: AlCu;
- Passivation using nitride with the exception of the pads;

- Number of metal layers: 6;
- Thickness of the chip: 725µm.

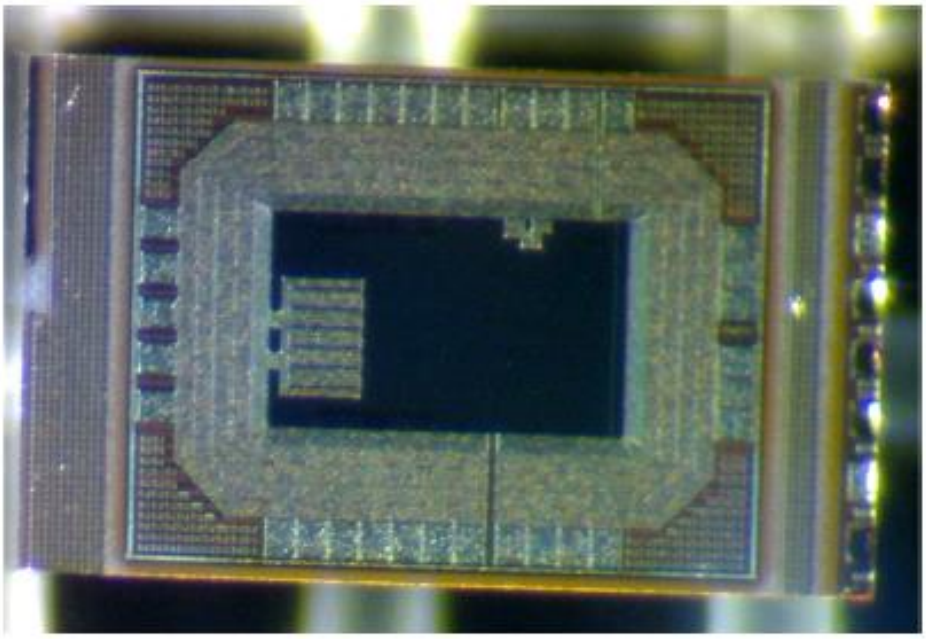


Figure 59: Silicon chip

An inert gas has been injected, inside the package, in order to limit the pads' oxidation induced by the thermal conditions, so during the test was checked if high temperatures can cause the leakage of gas and the consequent detachment of the cover.

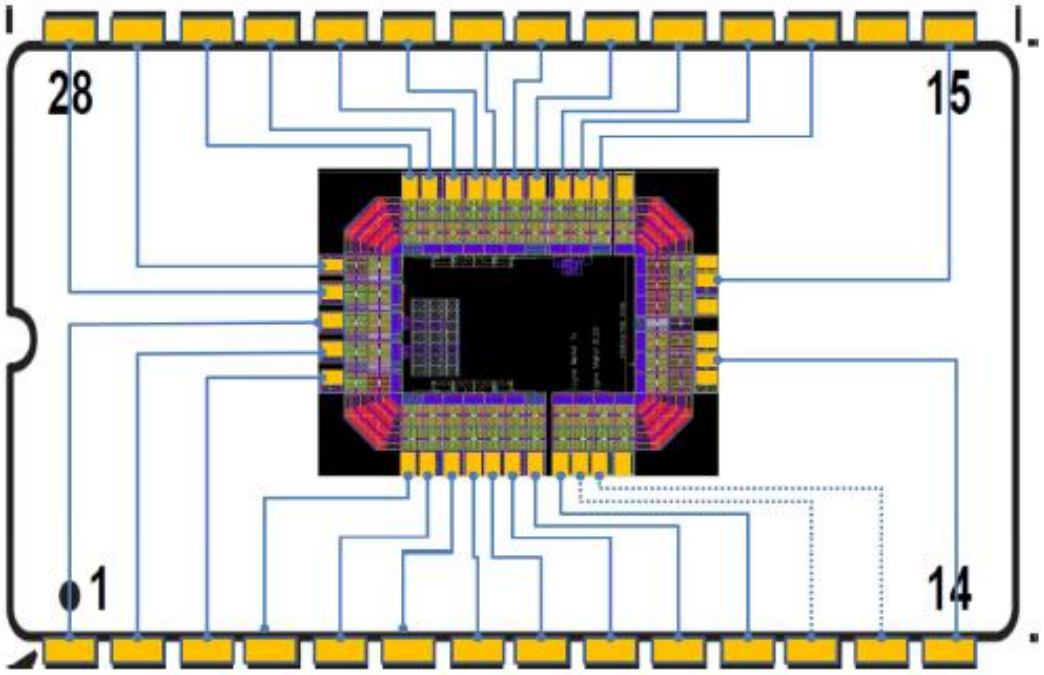


Figure 60: Wires' connection inside the package

In a first time, I had not a board on which positioning the chip during the test, because of that I soldered some wires on the pins needed for the RO test. As explained before, normal wires cannot be used due to the high temperatures, which could melt them and, in the worst case, burn them provoking fire. For this reason, I used high-temperature wires (made with Silicon isolation) and soldering material that can resist at temperatures up to 200°C. Finally, after plugging the chip to the instruments, and inserted it inside the heater, the test can take place.

5.2 Automated-Test Program

Firstly, I tried to do the tests manually but, due to the big temperature range taken into account, and the long time required by the heater to reach the temperature and keep it stable, I decided to spend some time to create program that could control, automatically, the entire test sequences. In this way was possible save time, launching the test program and leaving it working, even during the night, till the end of the test.
In order to do this, I created, with a colleague collaboration, a LabVIEW program that tests all the temperatures considered during simulations, and saves in an excel file the results. In the following I explain how the automated program works, in particular, specifying the steps taken by the program to test the device.

5.2.1 LabVIEW

LabVIEW, acronym of Laboratory Virtual Instrument Engineering Workbench, is a system-design platform and development environment for a visual programming language from National Instruments [15].
The graphical language is named "G" (not to be confused with G-code). Originally released for the Apple Macintosh in 1986, LabVIEW is commonly used for data acquisition, instrument control, and industrial automation on a variety of platforms including Microsoft Windows, various version of UNIX, Linux, and OS X.

5.2.1.1 Dataflow Programming

The programming language used in LabVIEW, also referred to as G, is a dataflow programming language. Execution is determined by the structure of a graphical block diagram (the LabVIEW-source code) on which the programmer connects different function-nodes by drawing wires. These wires propagate variables and any node can execute as soon as all its input data become available. Since this might be the case for multiple nodes simultaneously, G is inherently capable of parallel execution. Multi-processing and multi-threading hardware is automatically exploited by the built-in scheduler, which multiplexes multiple OS threads over the nodes ready for execution.

5.2.1.2 Graphical programming

LabVIEW ties the creation of user interfaces (called front panel) into the development cycle. LabVIEW programs/subroutines are called virtual instruments (VIs). Each VI has

three components: a block diagram, a front panel and a connector panel. The last is used to represent the VI in the block diagram of other, calling VIs. The front panel is built using controls and indicators. Controls are inputs, they allow a user to supply information to the VI. Indicators are outputs, they indicate, or display, the results based on the input given to the VI. The back panel, which is a block diagram, contains the graphical source code. All of the objects placed on the front panel will appear on the back panel as terminals. The back panel also contain structures and functions which perform operations on controls and supply data to indicators. The structures and functions are found on the Functions palette and can be placed on the back panel. Collectively controls, indicators, structures and functions will be referred to as nodes. Nodes are connected to one another using wires (e.g. two controls and an indicator can be wired to the addition function so that the indicator displays the sum of the two controls). Thus a virtual instrument can either be run as a program, with the front panel serving as a user interface, or, when dropped as a node onto the block diagram, the front panel defines the inputs and outputs for the node through the connector panel. This implies each VI can be easily tested before being embedded as a subroutine into a larger program.
The graphical approach also allows non-programmers to build programs by dragging and dropping virtual representations of lab equipment with which they are already familiar. The LabVIEW programing environment, with the included examples and documentation, makes it simple to create small applications. This a benefit on one side, but there is also a certain danger of underestimating the expertise needed for high-quality G programming. For complex algorithms or large-scale code, it is important that the programmer possess an extensive knowledge of the special LabVIEW syntax and the topology of its memory management. The most advanced LabVIEW development systems offer the possibility of building stand-alone applications. Furthermore, it is possible to create distributed applications, which communicate by a client/server scheme, and are therefore easier to implement due to the inherently parallel nature of G.

5.2.1.3 Benefits

Using LabVIEW, the user can take advantage from all its functionalities. The following part, of this chapter, is aimed to show the full list of advantage.

5.2.1.3.1 Interfacing to Devices

LabVIEW includes extensive support for interfacing to devices, instruments, cameras, and other devices. Users interface to hardware by either writing direct bus command (USB, GPIB, and Serial) or using high-level, device-specific, drivers that provide native LabVIEW function nodes for controlling the device.

5.2.1.3.2 Code compilation

In terms of performance, LabVIEW includes a compiler that produces native code for the CPU platform. The graphical code is translated into executable machine code by interpreting the syntax and by compilation. The LabVIEW syntax is strictly enforced

during the editing process and compiled into the executable machine code when requested to run or upon saving. In the latter case, the executable and the source code are merged into a single file. The executable runs with the help of the LabVIEW run-time engine, which contains some precompiled code to perform common tasks that are defined by the G language. The run-time engine reduces compilation time and also provides a consistent interface to various operating systems, graphic systems, hardware components, etc. The run-time environment makes the code portable across platforms. Generally, LabVIEW code can be slower than equivalent compiled C code, although the differences often lie more with program optimization than inherent execution speed.

5.2.1.3.3 Large libraries

Many libraries with a large number of functions for data acquisition, signal generation, mathematics, statistics, signal conditioning, analysis, etc., along with numerous graphical interface elements are provided in several LabVIEW package options. The number of advanced mathematic blocks for functions such as integration, filters, and other specialized capabilities usually associated with data capture from hardware sensors is enormous. In addition, LabVIEW includes a text-based programming component called MathScript with additional functionality for signal processing, analysis and mathematics. MathScript can be integrated with graphical programming using “script nodes” and uses a syntax that is generally compatible with MATLAB.

5.2.1.3.4 Parallel programming

LabVIEW is an inherently concurrent language, so it is very easy to program multiple tasks that are performed in parallel by means of multithreading. This is, for instance, easily done by drawing two or more parallel while loops. This is a great benefit for test system automation, where it is common practice to run processes like test sequencing, data recording, and hardware interfacing in parallel.

5.2.1.3.5 Ecosystem

Due to the longevity and popularity of the LabVIEW language, and the ability for users to extend the functionality, a large ecosystem of third party add-ons has developed through contributions from the community. This ecosystem is available on the LabVIEW Tools Network, which is a marketplace for both free and paid LabVIEW add-ons.

5.2.1.4 Criticism

LabVIEW is a proprietary product of National Instruments. Unlike common programming languages such as C or FORTRAN, LabVIEW is not managed or specified by a third party standards committee such as ANSI, IEEE, ISO, etc., then for this reason a certain number of disadvantage can be encountered.

5.2.1.4.1 Dataflow programming model

Due to its thorough adoption of a data-flow programming model as opposed to the sequential ordering or arbitrary commands like most other (usually text-based) languages, there is a very real barrier to many people who attempt to apply already-learned principles from other programming approaches to LabVIEW. The inherent parallel nature of the execution of LabVIEW code is a perennial source of confusion among those who are accustomed to other approaches. Due to this, most opinions tend to be highly polarized with people either being extremely fond of it or being extremely hostile to it.

5.2.1.4.2 Licensing

Building a stand-alone application with LabVIEW requires the Application Builder component which is included with the Professional Development System but, requires a separate purchase if using the Base Package or Full Development System.

5.2.1.4.3 Run-time environment

Compiled executables produced by version 6.0 and later of the Application Builder are not truly standalone in that, they also require the LabVIEW run-time engine be installed on any target computer which runs the application. The use of standard controls requires a run-time library for any language. All major operating systems supply the required libraries for common languages such as C. However, the run-time required for LabVIEW is not supplied with any operating systems and has to be specifically installed by the administrator or user. This can cause problems if an application is distributed to a user who may be prepared to run the application but does not have the inclination or permission to install additional files one the host system prior to running the executable.

5.2.1.4.4 Parallel execution and race conditions

The G language includes constructs for creating multiple execution threads. Like with any language that targets non-deterministic operating systems such as Windows, Mac OS, and Linux, parallel execution of multiple threads can lead to the possibility of race conditions. Although the G language greatly simplifies both the programming and thread management on multi-core and multi-processor system, the G developer must still guard race conditions; for which there are several functions and techniques available for doing so. Programming with the LabVIEW FPGA module results in true parallel implementation on FPGA target.

5.2.1.4.5 Performance

LabVIEW tends to produce applications that are slower than hand coded native languages such as C, although high performance can be achieved when using multi-core machines or dedicated toolkits for specific operations. LabVIEW makes multi-core programming much simpler than text based languages, due to its implicit parallelism and automatic thread management.

5.2.1.4.6 Light weight applications

Very small applications still have to start the runtime environment which is a large and slow tasks. This tends to restrict LabVIEW to monolithic applications. Examples of this might be tiny programs to grab a single value from some hardware that can be used in a scripting language, the overheads of the runtime environment render this approach impractical with LabVIEW.

5.2.1.4.7 Non-textual

G language being non-textual, software tools such as versioning, side-by-side (or diff) comparison, and version code change tracking cannot be applied in the same manner as for textual programming languages.

5.2.1.4.8 Not backwards compatible

A VI generated in a newer version of LabVIEW cannot be opened in an older version (not even for viewing). The "Save for Previous Version" feature can be a partial solution (if developer knows up-front that this would be needed).

5.2.1.4.9 No zoom-in function

There is no capability to zoom in to (or enlarge) a VI which will be hard to see on a large, high-DPI monitor.

5.2.2 Program description

Once explained main functions, pros and cons of the LabVIEW platform, we are able to see more in detail the functionality of the generated program.
The program has a user interface for the acquisition of the input values. The inputs are: the range of temperatures that we want to test, the step between one test and another, a list containing the different voltages with which the test will be executed, and the addresses of the used instruments. In my case the temperature range is from -40°C up to 180°C, with steps of 20°C (the upper limit is only 180°C because is the maximum temperature for the heater used in this part of the test). At the beginning, the test realizes the initialization of the variables used during the execution, and creates the table for the selected temperatures. When the initialization has been completed, the test enters a main loop, which loops for each temperature contained in the temperatures table. For each temperature, the program manages the heater, in order to set the selected temperature and wait that the temperature inside the heater becomes stable. When a stable temperature is reached, the program enters in another loop which cycles for each value contained in the voltages' table; inside this last loop, the power supply generator (Keithley Series 2400 SourceMeter) is initialized with the required voltage level, and activated just after. In addition, the current is read from the generator in order to compute the power consumption and save the result in a table. Immediately after, the scope (LeCroy waveRunner 625Zi) is programmed in order to read frequency and peak-to-peak value of the RO's output, and save them into another table.

Once all the voltages have been tested, the program can continue with the next temperature and repeat all the steps explained.
In the end, when all the previous loops have been completed, the results saved in two tables are written in two Excel files:

- one file for the peak-to-peak values and the frequencies;
- one file for the power consumptions.

5.3 Test Description

The test phase was composed of two tests using two different test equipment and two different devices. The first test uses a small freezing and heating chamber, which covers a temperature range from -60°C up to 180°C. During this phase I encountered different troubles, because I tried to connect directly the pins of the device, which was positioned inside the chamber, to the power supply, and to the scope using long high-temperature wires. The length of the wires has introduced a lot of noise, which occurred problematic for the proper circuit functioning. Most of the times, due to the inserted noise, the RO was not able to leave the steady state, viewing on the scope only the noise without the ring oscillation. To solve this problem, I tried to add a decoupling capacitance, close as much as possible to the device pins, but it did not solve completely the problem of the starting condition. Even using this solution, the automated test could spend a lot of time doing the test without obtaining good results at the end. I also tried to change the device to check if there was a fault inside it, but, even changing the device, the problem continued to persist. The only possible solution was to check if decreasing the length of the wires, the RO began to oscillate, showing a clear wave on the output. To do this, I took a simple board, not for high temperatures, just to check if the taken solution was the correct one. I soldered the device on the board with very short wires to connect it to the equipment. Using this solution, the problem of the starting condition was almost completely suppressed; at this point, the output signal was clear without any noise which distorts it. Another way to completely solve the problem of the starting condition, is to modify the design substituting the first NOT gate with a NAND or a NOR gate, as previously shown in Chapter **4.3**. Inserting a NAND/NOR gate adds the advantage of being able to drive the RO using an enable signal. In this specific case, the design had been done by another person, and the devices already developed; for these two reasons, for the continuing of my work the latter solution was not feasible, so I adopted the previous one. The only problem to solve, was to find a board resistant to high temperatures; we solved it using a board used for an older project. Even though the pin configuration were different, we were able to adapt the board to the device and use it.
This configuration was used for the automated test, which uses the heating chamber previously explained, and also for the other test in which was used a different test equipment. The latter test, instead of using a chamber like the first one, uses a tube under which is positioned the device, the temperature is controlled from the air which flows inside the tube. The temperature range of this equipment is from -60°C up to 300°C, which allowed us to test the technology in very critical environment conditions.

5.4 Test Results

In the graphs, contained in this chapter, are shown the results obtained during the test phase described in Chapter **5.3**.

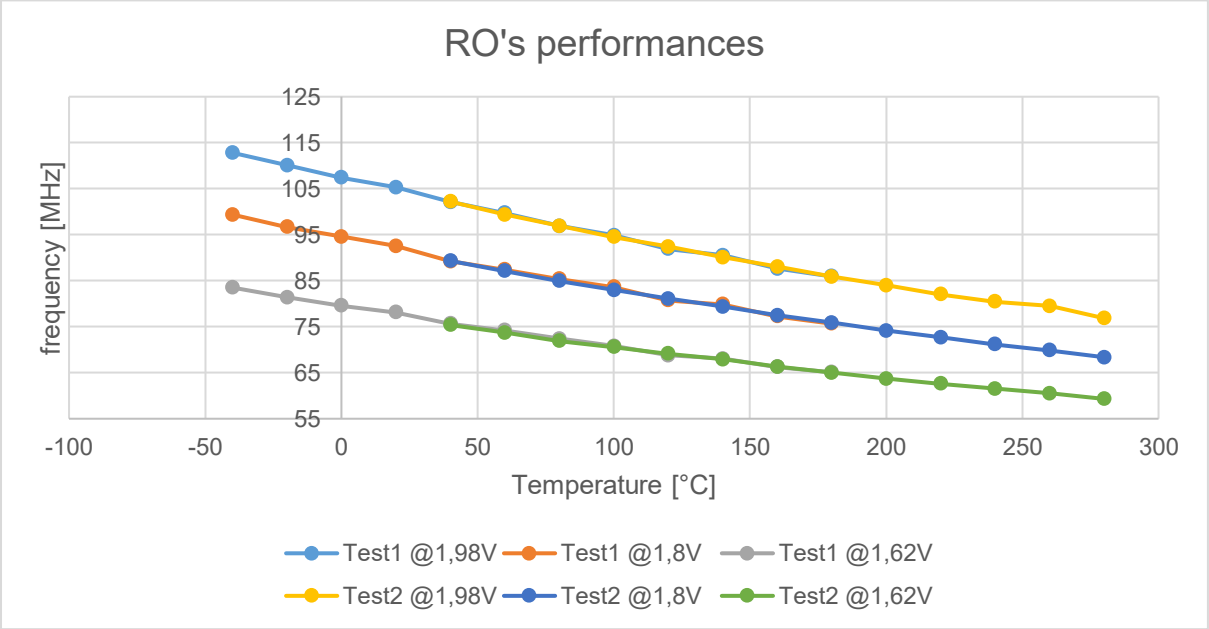


Figure 61: RO's frequency vs temperature

In **Figure 61** is shown the output frequency trend as a function of temperature. In both the test we got practically the same results. The curves of the first test are visible only thanks to the temperature range not covered by the second test; in the remaining part of the graph seems to see only three curves, but, up to 180°C, there are the curves obtained from the first test, which are not visible because are almost completely overlapped with the results of the second device.

In **Figure 62** are represented the power consumptions of the two tested devices. Even if in terms of performances we obtained practically the same results, as we saw in **Figure 61**, in terms of consumption there are some differences between the two tests. When the device is driven with a voltage equal to 1.98V (light blue and yellow in the graph), we have a comparable power consumption till 140°C, then for higher temperature the first device still shows a decreasing curve, while the second device shows a slight increase, keeping the power consumption almost constant and then resume to grow from 240°C. In the second case, supplying the circuit at 1.8V (orange and blue in the graph), unless a small difference at 40°C, the power consumptions' trends are similar, but with a gap of about 300µW. Like in the 1.8V case, even in the last case, when the devices are driven using 1.62V (grey and green lines), the trends are almost the same, but with a gap of about 200µW.

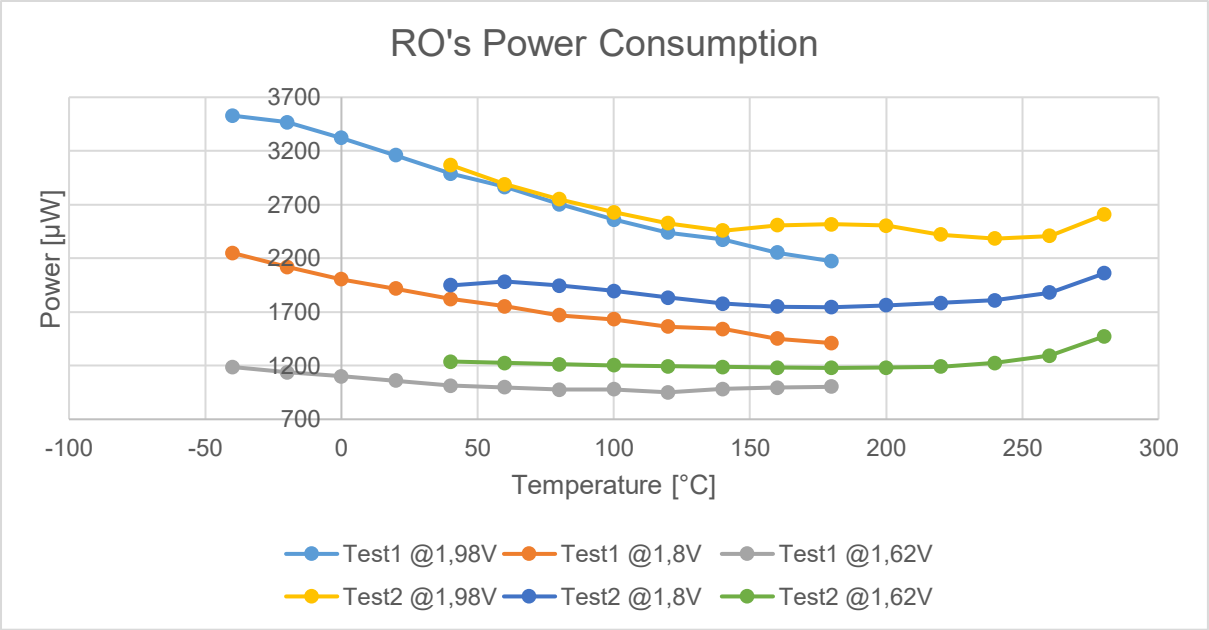


Figure 62: RO's power consumption vs temperature

Considering that, during the devices' tests, is used only the RO, differences of 300µW and 200µW are not negligible; for this reason, it would be advisable to conduct further tests using different devices, in order to have more comparisons with respect to the two presented in this work. I could not make further tests for timing reasons, due to the duration of my internship.

In contrast to what previously said, in the graphs explained in **Figure 61** and **Figure 62**, there are not the results obtained during the tests at 300°C; this is due to the fact that, during those tests, after few seconds of correct working at that temperature, the device stopped working. I also tested at 300°C the first device (the one tested up to 180°C), but the result was the same; the circuit works properly for few seconds, after that the output goes to zero and does not work anymore.

A curious thing is that, after the tests at 300°C, decreasing the temperature and restarting the power supply, the first device was still functioning while the second not. To better understand the reason of the malfunction, would be advisable to carry out further checks on the second device, an example could be: the opening of the package and check bonding and interconnections with the microscope, in order to find the problem that caused the device's death.

5.5 Test and Simulation comparison

Finally, this last chapter summarizes the work done till now, including a comparison between simulation results and test results. This is done to evaluate the simulator accuracy for the future works, which will be designed using the X-FAB XT018 technology for high-temperature applications.

Like previously said in Chapter **4.3.1**, I compared the test results with the results obtained during the simulations in ws mode (SLOW); the reason is that, the test results are between

the results obtained during the simulations in ws mode and tp mode (TYPICAL), but closer to the first one, hence easier and more accurate to compare with.
Remembering that ws mode is the one with (NMOS=SLOW, PMOS=SLOW), while tp mode the one with (NMOS=TYPICAL, PMOS= TYPICAL), has to be said that, probably, the mode which fits exactly our real case, could be one of the two modes: (NMOS=SLOW, PMOS=FAST) or (NMOS= FAST, PMOS= SLOW), which I didn't tested for time issues.
In **Figure 63** are depicted the RO's performances when the power supply is equal to 1.98V. As we already saw during simulations comparison, and tests comparison, the output frequencies are almost the same, but there is a small gap between SLOW mode simulation results and test results. The difference between test and simulation is of about 10 MHz, it remains practically constant for all the tested temperatures.

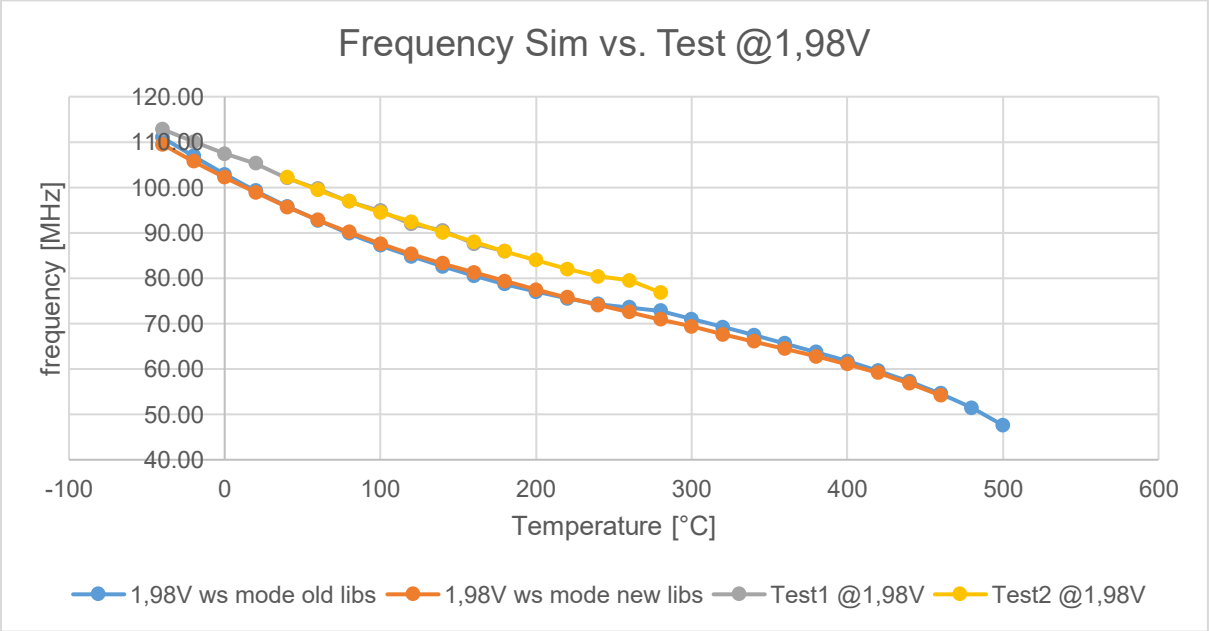


Figure 63: Simulation and Test frequencies driven at 1.98V

In **Figure 64** are reported the different power consumptions. Comparing the results obtained during the test with the simulated ones, we can assert that the new models are much more accurate compared to the older ones, which have a tendency completely different. Even in this case, as for the frequencies, there is a gap between simulations and tests; this is normal since in the simulation phase we obtained higher frequencies, which means more switching activity then bigger power consumptions.

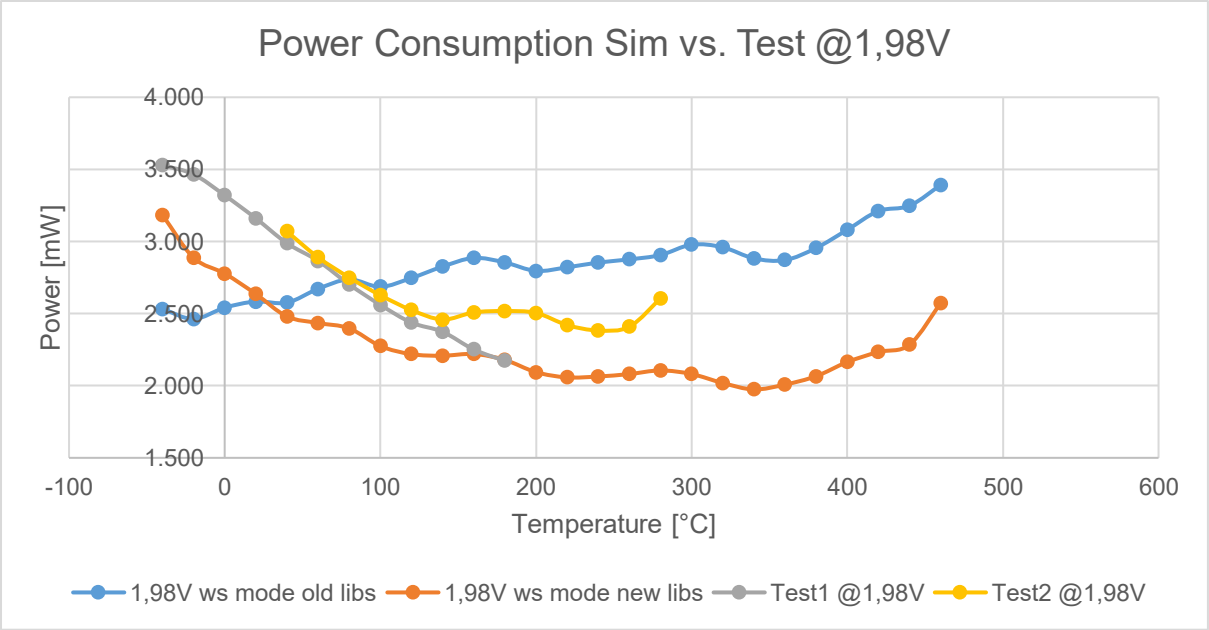


Figure 64: Simulation and Test power consumptions driven at 1.98V

Another important aspect is evinced comparing simulations and tests in **Figure 64** is that, during simulations with new models, the results are much more similar to the ones obtained in the test phase. With this assumption, we can say that, the older models have been improved regarding power consumptions, in fact with the new models we reached more accurate and acceptable results, which follow almost the same trend of the tests, just shifted down because of the different working frequencies. A difference is that the curve obtained from the simulation results starts an exponential increase from 380°C instead of 260°C like in Test2 (orange and yellow line respectively in **Figure 64**).

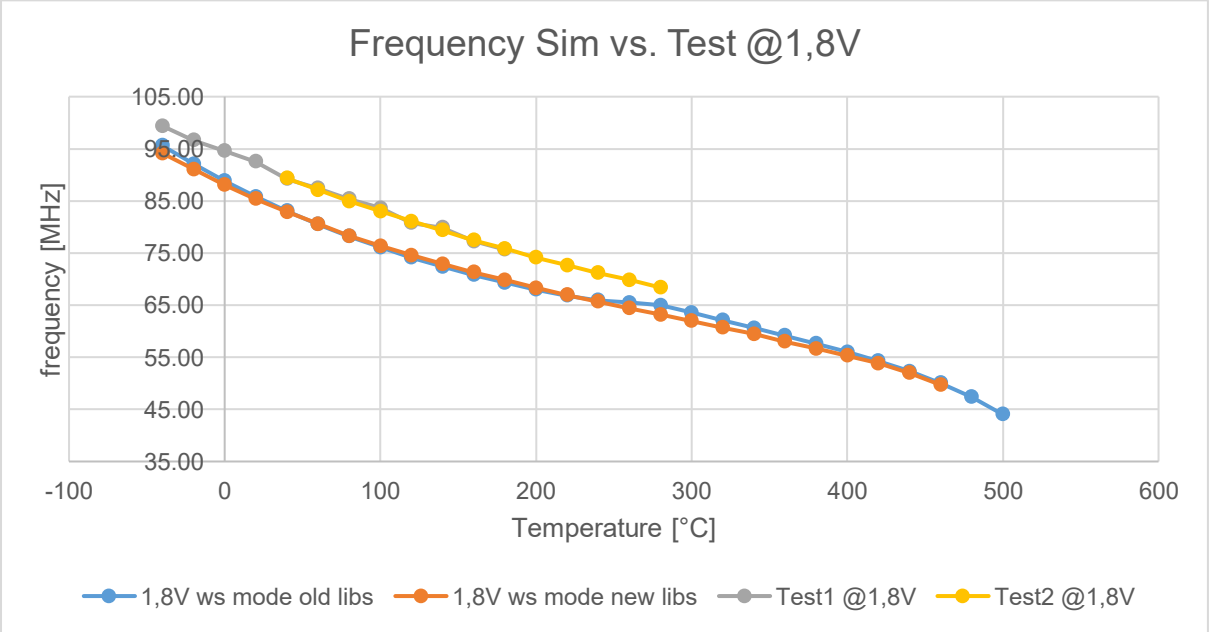


Figure 65: Simulation and Test frequencies driven at 1.8V

In **Figure 65** and **Figure 66** are represented tests and simulations comparisons when the RO is driven using a power supply equal to 1.8V. Also in this case, are valid the considerations done for Vdd=1.98V, they confirm that the new model has almost the same trend of Test2 results.

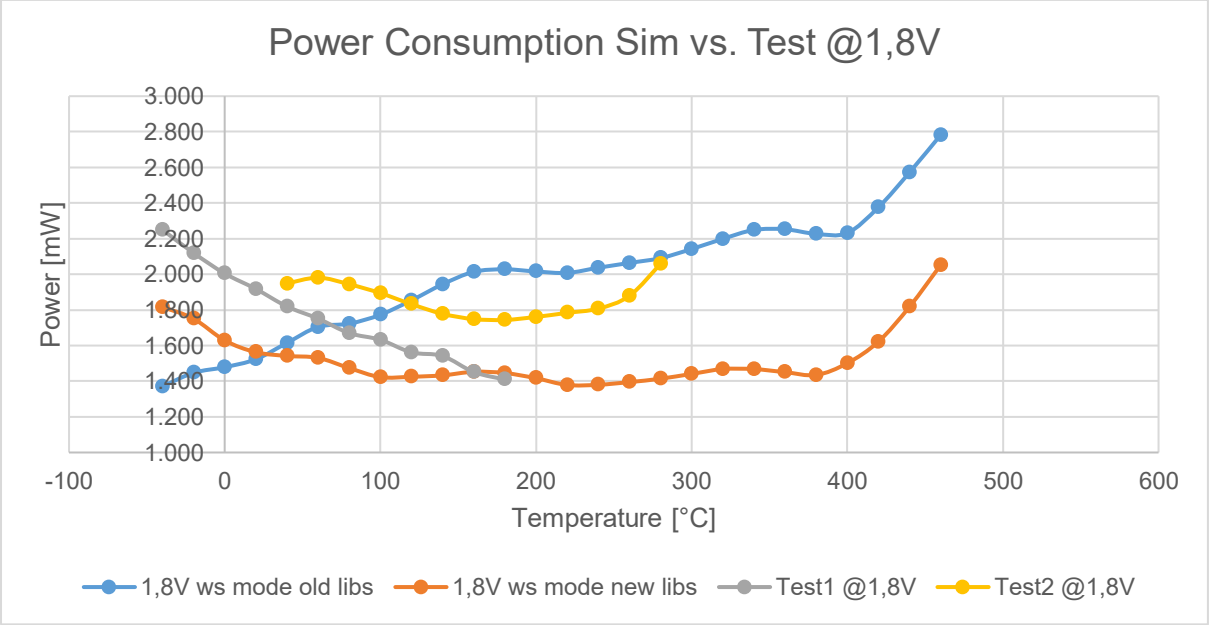


Figure 66: Simulation and Test power consumptions driven at 1.8V

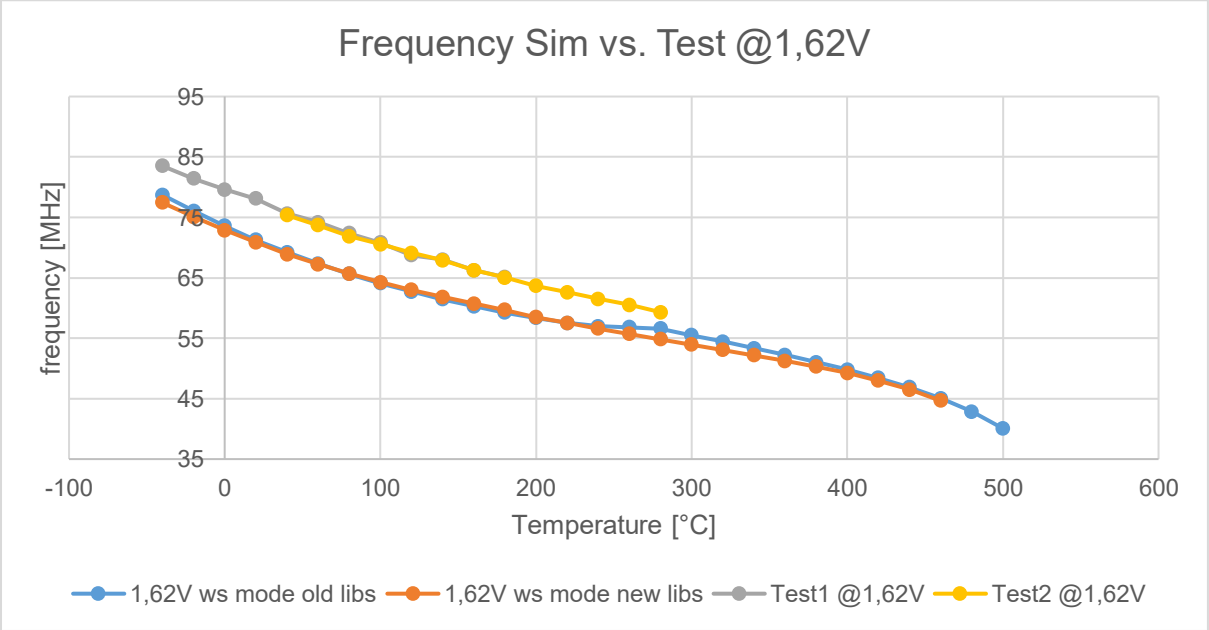


Figure 67: Simulation and Test frequencies driven at 1.62V

Finally, **Figure 67** and **Figure 68** conclude my contribute during the internship at CEA Grenoble. These two last pictures represent the comparisons of frequencies and power consumptions between simulations and tests when the power supply is set to 1.62V.

In my opinion, the only remark that have to be done, in addition to the previously explained examples (1.98V and 1.8V), is that using a smaller voltage reference, then closer to the threshold voltage, the power consumption starts to increase, even in the simulation, in an exponential manner from smaller temperatures (from about 300°C).

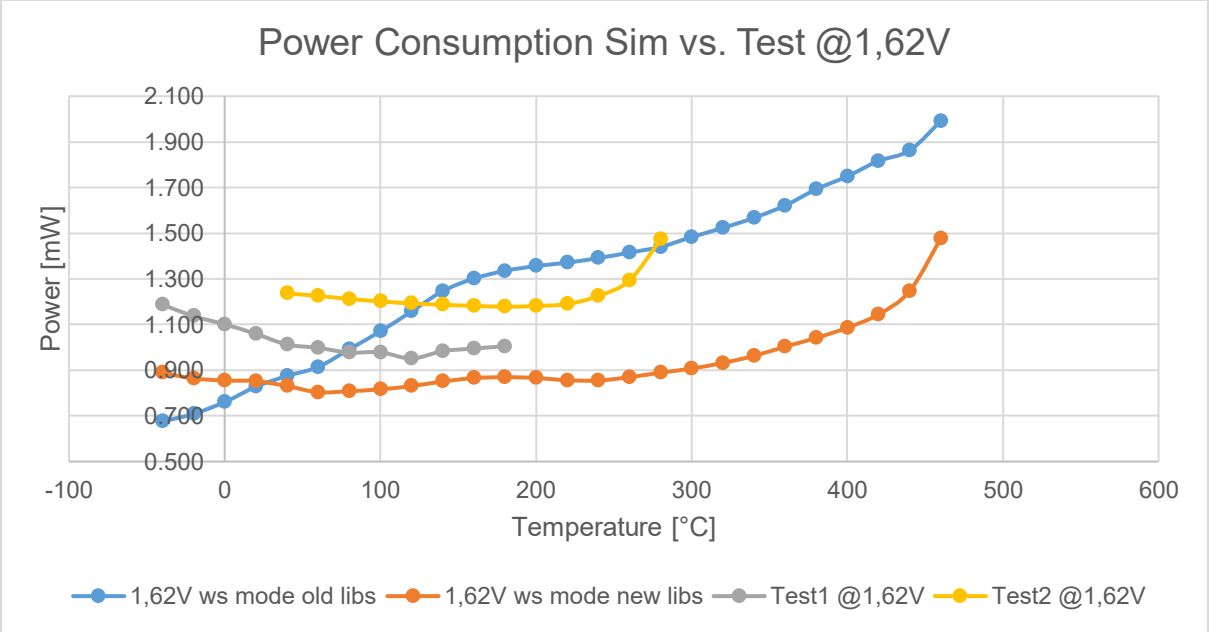


Figure 68: Simulation and Test power consumptions driven at 1.62V

All the comparisons, explained in this chapter, do not consider results obtained using the old models, because they turned out to be very inaccurate. Although they are not mentioned, I included the results in the graph in order to give an helpful vision of the difference between the two models (old and new) and the tests of the physical device.

Conclusions

The results presented in this document demonstrate that X-FAB XT018 (175°C is the maximum working temperature given by the producer) technology is suitable to offer a real opportunity for integrating, at reasonable cost, digital circuits which can withstand temperatures up to 280°C. SOI CMOS devices and circuits clearly outperform comparable bulk silicon implementations above 150-200°C in terms of stand-by power and stability of circuits operation.
Compared with promising materials as SiC and GaN, CMOS on SOI is a simple, mature and cheap technology, because it is fully compatible with the techniques and equipment used for standard silicon CMOS processing.
In addition, the technology properties may open up the industrial feasibility of accelerated burn-in lifetime testing at higher temperatures than in bulk, thereby reducing significantly test's duration and costs.
Regarding the test done using the automated program (up to 180°C), the test duration was programmed to 30 minutes, leaving the devices, for that time, at the desired temperatures before reading the output results. Instead, for higher temperatures (using another tester machine) tests were evaluated for short period (mean time: 5 minutes) because the tests were done manually. For this reason, an improvement for the future work could be to execute the test for longer period; doing this, will be possible to replicate more accurately the aerospace conditions, that may remain at very high temperatures for very long time due to the temperature generated by the engines.
In order to have more realistic and reliable results, other tests have to be done on further devices that contain more complicated circuits, for example designing a kind of circuit test-case performed till the place&route phase with back-annotated simulations.
A further improvement could be to include into the devices one of the proposed solutions for implementing the Adaptive Voltage Scaling technique, which can control and manage the voltage/frequency level in order to optimize power consumption and device's performance based on the temperature environment.

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[16] **Electromigration -** *[Wikipedia]*
[17] **Latch-up -** *[Wikipedia]*

Appendix

Electromigration

Electromigration is the transport of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing atoms [16]. The effect is important in applications where high direct current densities are used, such as in microelectronics and related structures. As the structure size in electronics such as integrated circuits decreases, the practical significance of this effect increases.

Electromigration decreases the reliability of chips (ICs). It can cause the eventual loss of connection or failure of a circuit. Since reliability is critically important for space travel, military purposes, anti-lock braking systems, medical equipment like Automated External Defibrillators and is even more important for personal computers or home entertainment systems, the reliability of chips (ICs) is major focus of research efforts. Although electromigration damage ultimately results in failure of the affected IC, the first symptoms are intermittent glitches, and are quite challenging to diagnose. As some interconnects fail before others, the circuit exhibits seemingly random errors, which may be indistinguishable from other failure mechanism (such as electrostatic discharge damage). In a laboratory setting, electromigration failure is readily imaged with an electron microscope, as interconnected erosion leaves telltale visual markers on the metal layer of the IC.

In modern consumer electronic devices, ICs rarely fail due to electromigration effects. This is because proper semiconductor design practices incorporate the effects of electromigration into the IC's layout. Nearly all IC design houses use automated EDA tools to check and correct electromigration problems at the transistor layout-level. When operated within the manufacturer's specified temperature and voltage range, a properly designed IC device is more likely to fail for other (environmental) causes, such as cumulative damage from gamma-ray bombardment.

Electromigration can be a cause of degradation in some power semiconductor devices such as low voltage power MOSFETs, in which the lateral current through the source contact metallization (often aluminum) can reach the critical current densities during overload conditions. The degradation of the aluminum layer causes an increase in on-state resistance, and can eventually lead to complete failure.

Latch-up

In CMOS technology, there are a number of intrinsic bipolar junction transistors [17]. In CMOS processes, these transistors can create problems when the combination of n-well/p-well and substrate results in the formation of parasitic n-p-n-p structures. Triggering these thyristor-like devices leads to a shorting of the Vdd and gnd lines, usually resulting in destruction of the chip, or a system failure that can only be resolved by power-down.

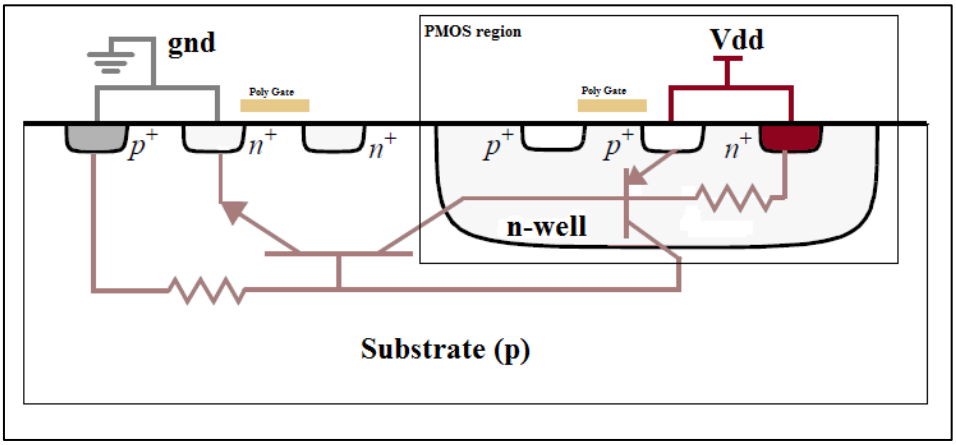

Figure 69: Thyristor created by the n-p-n-p structures

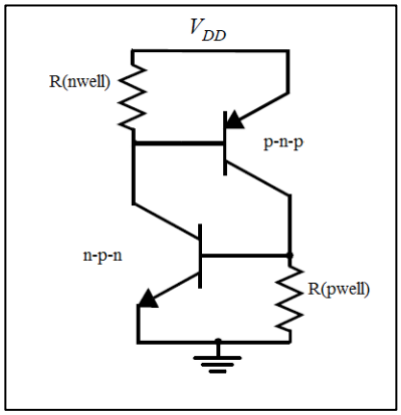

Figure 70: Equivalent circuit of the thyristor