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Analysis and Simulation of Emerging FET Devices: FinFET, TFET

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Summary

In this thesis the electrostatic analysis of three-dimensional FinFETs was done in detail. Taking all main issues of such devices in mind, new emerging devices like Tunnel FET and sandwich tunnel barrier FET (STBFET) were investigated.

Firstly, different analytical models for long channel and short channel double-gate (DG) FinFETs were simulated with MATLAB, focusing on their reliability. In particular, TCAD Synopsys Sentaurus simulations were used to validate the correctness among the analytical models that were implemented. Then, the most reliable MATLAB model for DG FinFET was succesfully extended to triple-gate (TG) and trapezoidal TG FinFETs. Finally, a capacitance analysis for TG FinFET was carried out.

Secondly, several analytical models for Tunnel FET were implemented in MATLAB. One among them was found as the most reliable and valid for different transistor sizes, so analytical simulations in MATLAB have been implemented for different structures of Tunnel FET, such as single-gate (SG), double-gate(DG) and gate-all-around (GAA) TFETs. To verify the accuracy of such models, physical simulations in TCAD Synopsys Sentaurus of Tunnel FET devices have been done, focusing on cylindrical gate all around (GAA) structures. An electrostatic analysis, a capacitance analysis and a temperature analysis was carried out in order to compare the behaviour of both GAA FET and GAA TFET.

To enhance the behaviour of TFET in the ON-state, a study of material dependence was done. A Si/Ge nanowire hetero-structure Tunnel FET was studied and simulated in TCAD Synopsis Sentaurus. In fact, a Germanium source enables the reduction of the barrier width and henance tunneling of electrons from source to drain.
Another solution to let Tunnel FET be an applicable device is to modify the structure, such as in sandwich tunnel barrier FET (STBFET). In such device, the source is sandwiched in the substrate and that allows to switch the tunneling from lateral to vertical direction in the ON-state. STBFET presents a higher current and a steeper slope, still mantaining a low leakage current.

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Chapter 1

Introduction

Historically, device scaling in semiconductor industry has been driven by Moore's Law, 'for a constant increase in performance and scaling of transistor ′ [41]. Gordon Moore, one of Intel founders, in 1965 made an observation, which became a prophecy for semiconductor companies:

'The number of transistor on integrated circuits doubles approximately every two years′ [42].

However, this trend seems to have an end around the 20nm technology node, because of several transistor scaling limits known as short channel effects (SCEs). Physical limits in CMOS technology are goig to became the most relevant issue in Silicon process.

A first improvement in the last 20 years is the performance henances due to the SOI instead of Bulk substrate.The key feature of the SOI structure (compare with the bulk-Si) is the layer of silicon dioxide just below the surface [24].
Transistors are now made in a thin silicon layer sitting on top of a Si02 layer, that allows to improve circuit speed and power consumption. Furthermore, SOI technology brings improvements in temperature dependence and flexibility in the device design, since substrate and device are physically separated by an insulator.
Finally, the main feature of SOI technology is the evident reduction of short channel effets. A comparison in behaviour between Bulk and SOI devices could be useful to better understand the trouble.

In a bulk device, the propagation of electric field is evident in depletion region associated with the junctions.

The electric field contribution on channel performance can be reduced by increasing doping concentration. Obviously, there is a limit in increase doping concentration for proper device operation.

On the other hand, a FDSOI MOSFET is characterized by an electric field that propagates through the buried oxide before going in the channel region. If a thin burid oxide is realized over a ground plane, short channel effects are reduced.
The drawbacks behind that is the body effect and the increasing in junction capacitance, that can however be overcame by doubling the gate structure. In fact, by the use of this approach, the electric field propagates to the bottom gate electrode and cannot reach the channel region.

Furthermore, as MOSFET scales in dimensions, there is a need to preserve long-channel behaviour as it possible. In fact, due to the reduction of channel length dimension, the depletion width of the source and drain become comparable to the channel length and punch-through between the drain and source will eventually occur [24].
This effect can be solved increasing channel doping, but as consequence there will be an increase of the threshold voltage. To solve again that, the thickness of the oxide can be reduced, but there is a limit related to that.
With this in mind, different scaling rules were used to optimize the device performance, but even with that rules, the long-channel behaviour is difficult to reach with the channel length scaling.
This is mainly due to the exponential increase of leakage current with reducing the supply voltage. This behaviour is mainly related to a thermionic behaviour of MOSFET.

Another short-channel effect is the CLM, which is defined as the reduction of the inverted channel region length with increase in drain voltages, that results in an increase in current with drain bias and a reduction of output resistance.
More in detail, as the drain voltage increases, the un-inverted region expands toward the source due to the extension of the control over the current toward the source. This results in an shortening of the channel region length. But, shortening the channel decreases its resistance [24], causing an increase in current with increase in drain bias. The effect is more evident as channel length reduces, the drain junction becomes deeper and the thickness of the oxide increases.
In particular, if the sum of these depletion widths approaches the channel length, a condition called punch-through is verified.
It results in an increase in leakage current between source and drain that is function

of the drain bias.
The origin of punch-through is the lowering of the barrier near the source, commonly referred to as DIBL (drain-induced barrier lowering) [24]. When the drain is close to the source, the drain bias can influence the barrier at the source end, such that the channel carrier concentration at that location is no longer fixed [24]. For a long-channel device, a drain bias can change the effective channel length, but the barrier at the source end remains constant [24]. For a short-channel device, this same barrier is no longer fixed [24]. The lowering of the source barrier causes an injection of extra carriers, thereby increasing the current substantially [24]. This increase of current shows up in both, above-threshold and subthreshold regimes [24]. Furthermore, the fabrication of such short channel FETs increases in complexity. Short-channel effects make the device operation more complicated and the performance of the devices degrades. Several solutions are needed to minimize these effects.
Recent solutions for future transistor scaling include a three-dimensional structure such as FinFETs, in order to improve isolation, reduce the subthreshold swing and parasitic capacitances, and increase on-current.
Multiple gate devices allow a reduction in parasitic transverse electric field in the channel, since there is an increase of the mobility.
Obviously, there is a better channel control that results in higher on current, better subthreshold slope and smaller DIBL.
However, FinFETs present a poor subthreshold slope and high leakage current when the device gate length is scaled below 14nm, so the main issues related to short channel effects still remain. Several solutions have been studied to overcome such limits and to become a future alternative to conventional MOSFETs.

One emerging device is the Tunnel FET. As for technological fabrication it is a MOS-like structure, except for having opposite doping between source and drain. The device can be seen as a gated p-i-n junction, whose operating principle is based on
Band-to-Band Tunneling. If a bias is applied to the drain terminal, the conduction band in the channel region is pushed below the valence band in the source region, so that tunneling occurs at the source/channel junction.

Tunneling is a quantum mechanical effect where particles have a non zero probability to tunnel through an energy barrier due to their wave nature [30], and this effect becomes domaninant as device scaled.
Tunnel FETs are based on this effect, since carriers are injected through a barrier instead of over a thermal barrier, a in conventional MOSFET. [30].

The subthreshold slope of Tunnel FETs can go below the classic thermal limit of 60mV/dec. Indeed, it is characterized by a very low off-current and a weak temperature dependence. The main characteristics of Tunnel FET are an increase in Ion to Ioff ratio and in a reduction of short channel effects.
Even if the drain potential can affect the tunneling barrier at very short channel lengths, a reduction in VDD enabled by the steep subthreshold swing of a TFET can likely lessen the effect [30]. Therefore, the TFET device structure potentially allows for scaling to shorter channel lengths prolonging Moore's Law, and these properties make TFETs a candidate for ultra-low power logic applications [30]. However, an important issue of Tunnel FETs is the very low current in the on-state. Indeed, researchers are studying several solutions, such as different gate materials, metal gate engineering, heterostructure or vertical structures.

1.1 Thesis Outline

This work is divided in two main parts. After a brief introduction on CMOS scenario, the firs part is dedicated to the modelling of Double Gate and Triple Gate FinFETs. Physical simulations in TCAD Synopsis Sentaurus will check the accuracy and the computational effciency of the implemented model.
The second part of the thesis is devoted to investigate on new emerging devices such as Tunnel FET, as alternative to conventional FETs.
Modelling of different Tunnel FET structures and relative physical simulations were done in order to validate the reliability of such analytical models.
Analysis and simulation of emerging devices include IV behaviour, a capacitance analysis, a temperature analysis of DG,TG,GAA FinFET, and SG,DG,GAA TFETs.
Finally, physical simulations of heterostructure tunnel fet and STBFET occupy the last part of this thesis, as possible solutions to TFET main issues.

Chapter 2

FinFET

Multi-Gate (MG) MOSFETs are nowadays the most promising devices for the short channel effects reduction, since the device scaling brought them in evidence.
MG transistors allows to a better control of the channel, a better subthreshold slope and smaller DIBL parameter, an higher on current since more inversion volumes are created.
Among all multi-gate FETs, the simple structure an fabrication process of FinFET lead to some advantages with respect to the planar-MOSFET. The FinFET is a non-planar multi-gate transistor realized on a SOI substrate. Despite of MOSFET, which have an horizontal channel, the FinFET presents a vertical channel, named fin. It can be seen as an ultra thin MOSFET, where the conducting channel is wrapped by a thin silicon fin. The channel length is the extension of the fin under the gate.

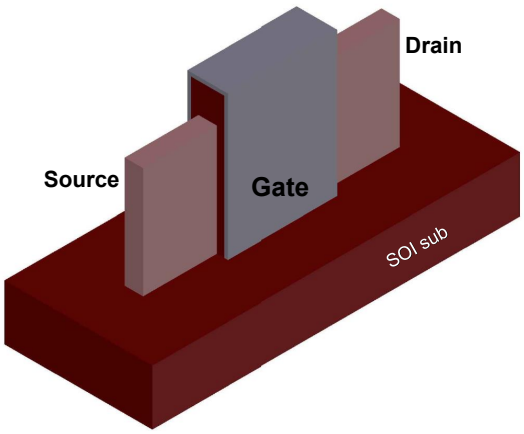

Figure 2.1: Device Structure of SOI FinFET

It is a three-dimensional device which allows to a further scaling above the 20nm.

In fact, as the channel length scales down, short channel effects are reduced by reducing the width of the fin. Furthermore, the use of three gate surrounding the fin ensures excellent electrostatic control. Furthermore, DIBL effect is less than planar MOSFET, since fins are wrapped into the gate.

Finally, since it is a three-dimensional structure, it allows to provide a greater device width per wafer area. In this way, the density of packaging increases quicker than for planar MOSFETs.

However, reducing fin widths it could be a problem for the device performance, since a narrower fin means a high access resistane, reducing the current in the on-state. A solution to increase such current is to use multiple fins in parallel.

2.1 DG FinFET Analytic Models

Several analytical models already present in leterature were implemented in MATLAB. The aim was to realize an electrostatical analysis a DG FinFET and to investigate on advantages and limits of such three-dimensional FET.
The implemented models were used to analyze both long channel and short channel FinFET, so that a scaling behaviour of FinFET could be studied. Next sections will be dedicated to the theorical explanation of analytical models, than results on simulations of such models will be done.

2.2 Taur Model

A Double Gate FinFET can be modeled as first approximation as a very thin body DG MOSFET. With this in mind, a continuous analytic IV model is derived using Pao-Sah integral with no charge sheet approximation.

In this way, all linear, saturation and subthrehold region of MOSFET can be analyzed. The model is based on the Pao Sah's gradual channel approach. If a cut along the vertical direction of the Si film is done, Poisson's equation can be derived as follows:

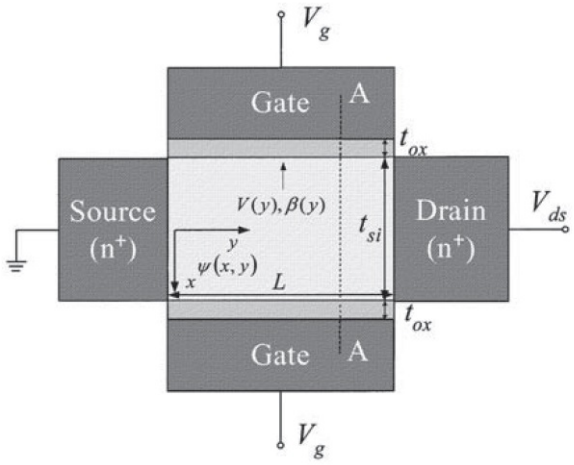

Figure 2.2: Schematic diagram of a DG MOSFET (taken from [1])

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_{si}} n_i e^{\frac{q(\psi - V)}{kT}} \tag{2.1}$$

where ψ is the electrostatic potential, q is the electronic charge, n_i is the intrinsic carrier density, ε is the silicon permittivity, kT/q is the thermal voltage, and V is the electron quasi-Fermi potential.

In this model the n-MOSFET is evaluated with $q\psi/kT \gg 1$, so that the hole density is negligible [1].
The major contribute of the current flow is from the source to the drain along the y-direction, so also the gradient of the electron quasi-Fermi potential V is in the y-direction. Hence, the electron quasi-Ferm potential V can be approximated to be constant in the x-direction [1]. By integrating twice the above expression, surface potential can be evaluated:

$$\psi(x) = V - \frac{2kT}{q} ln[\frac{t_{si}}{2\beta}\sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}} cos(\frac{2\beta x}{t_{si}})] \tag{2.2}$$

where β can be derived by solving the following equation as a function of V:

$$\frac{q(V_g - \Delta\phi - V)}{2kT} - ln[\frac{2}{t_{si}}\sqrt{\frac{2\varepsilon_{si}kT}{q^2 n_i}}] = ln\beta - ln[cos\beta] + \frac{2\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\beta tan\beta \tag{2.3}$$

Where V_g is the voltage applied to front gate and back gate, $\Delta\phi$ is the metal work function, t_si and t_ox are respectively the silicon and oxide thickness, and ε_{ox} is the oxide permittivity.

The current can be derived integrating $I_{ds}dy$ and expressing dV/dy as $(V/d\beta)(d\beta/dy)$. So, Pao-Sah's integral can be written as:

$$I_{ds} = \mu\frac{W}{L}\int_0^{V_{ds}} Q_i(V)dV = \mu\frac{W}{L}\int_{\beta_s}^{\beta_d} Q_i(\beta)\frac{dV}{d\beta}d\beta \tag{2.4}$$

Where β_s and β_d the solutions of β equation, respectively for V=0 and V=V_{ds}, while Q_i derived from Gauss's law as $Q_i = 2\varepsilon_{si}(d\psi/dx)_{x=t_{si}/2}$. The charge equation can be expressed as function of β using (2.15) : $Q_i = 2\varepsilon_{si}(2kT/q)(2\beta/t_{si})tan\beta$. The derivative $dV/d\beta$ can be also expressed as function of β by differentiating (2.16).

The analytical integral can be now carried out:

$$\begin{aligned} I_{ds} = \mu\frac{W}{L}\frac{4\varepsilon_{si}t_{ox}}{t_{si}}(\frac{2kT}{q})^2\int_{\beta_d}^{\beta_s}[tan\beta + \beta tan^2\beta + \frac{2\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\beta tan\beta\frac{d}{d\beta}(\beta tan\beta)]d\beta \\ = \mu\frac{W}{L}\frac{4\varepsilon_{si}}{t_{si}}(\frac{2kT}{q})^2[\beta tan\beta - \frac{\beta^2}{2} + \frac{\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\beta^2 tan^2\beta] \end{aligned} \tag{2.5}$$

The range of β is $0 < \beta < \pi/2$, while β_s and β_d are found for given V_{gs} and V_{ds} from the conditions:

$$\begin{aligned} f_r(\beta_s) = (q/2kT)(V_g - V_0) \\ f_r(\beta_d) = (q/2kT)(V_g - V_0 - V_{ds}) \end{aligned} \tag{2.6}$$

Where $f_r(\beta)$ is the right hand side of (2.16) si equals to $f_r(\beta) = ln\beta - ln[cos\beta] + \frac{2\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\beta tan\beta$, while V_0 is found to be:

$$V_0 \equiv \Delta\phi + \frac{2kT}{q} ln[\frac{2}{t_{si}}\sqrt{\frac{2\varepsilon_{si}kT}{q^2 n_i}}] \tag{2.7}$$

The current I_{ds} can be computed as $I_{ds} \propto [g_r(\beta_s) - g_r(\beta_d)]$, where the function $g_r(\beta)$ derives from (2.18) so that: $g_r(\beta) = \beta tan\beta - \frac{\beta^2}{2} + \frac{\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\beta^2 tan^2\beta$.

Solving β function as function of the gate voltage, this analytical model can extract the FET characteristic for all operating regions.

In the linear region above the threshold it is found to be $f_r(\beta_s)$, $f_r(\beta_d) \gg 1$, so β_s,$\beta_d \sim \pi/2$. The current in the linear region can be expressed as follows:

$$\begin{aligned} I_{ds} &= \mu C_{ox}\frac{W}{L}[(V_g - V_t)^2 - (V_g - V_t - V_{ds})^2] \\ &= 2\mu C_{ox}\frac{W}{L}(V_g - V_t - \frac{V_{ds}}{2})V_{ds} \end{aligned} \tag{2.8}$$

In the saturation region, $\beta_s \sim \pi/2$, and $f_r(\beta_d) \ll 1$, so $(\beta_d) \ll 1$. The current can be derived as:

$$I_{ds} = \mu C_{ox}\frac{W}{L}[(V_g - V_t)^2 - \frac{8\varepsilon_{si}t_{ox}k^2T^2}{q^2\varepsilon_{ox}t_{si}} \exp\frac{q(V_g - V_0 - V_{ds})}{kT}] \tag{2.9}$$

Finally, in the subthreshold region, it is found to be both β_s,$\beta_d \ll \pi/2$, so that both f_r,$f_r \sim \beta^2/2$. The current can be expressed as:

$$I_{ds} = \mu\frac{W}{L}kTn_i t_{si} \exp\frac{q(V_g - \Delta\phi)}{kT}(1 - \exp -\frac{qV_{ds}}{kT}) \tag{2.10}$$

"This continuous IV model is derived from analytic solutions of Poisson's and current continuity equation for long channel DG MOSFET" [1].

2.2.1 Matlab Implementation

Taur Model [1] was implemented in Matlab in order to simulate the double-gate (DG) FinFET electrostatic characteristic. In fact, such model can be used to describe the behaviour of a FinFET if the latter is seen as a MOSFET with a very thin layer.
The device parameters extracted from Fasarakis model [4] are described in the table below:

Quantity Name	**Value**	**u.m. (S.I.)**
Gate Length	200 - 20	nm
Oxide Thickness (t_{ox})	1	nm
Fin Width (W_{fin})	10	nm
Temperature (T)	300	K
Source/Drain doping concentration (N_{sd})	10^{20}	cm^{-3}
Channel doping concentration (N_{ch})	10^{15}	cm^{-3}
Metal workfunction ϕ_m	4.1	eV

Table 2.1: Input data used for implementation of Taur model [1]

A simulation of DG FinFET were carried out in MATLAB varying the channel length, hence the scaling behaviour of such FET could be put in evidence.
The following figure represents the trend in channel length scaling described from the Taur model, with $V_{ds} = 1$V.

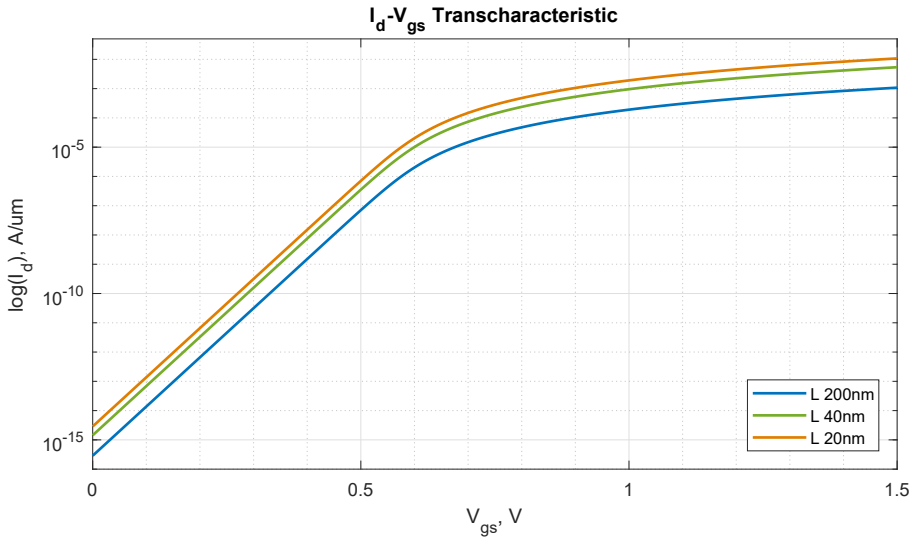

Figure 2.3: $I_d - V_{gs}$ characteristic of analytical model simulated in Matlab for different gate length

The table below includes the current values for on and off state. In this way, the trend of the model implemented varying the gate length can be analyzed.

Parameters	L = 200nm	L = 40nm	L = 20nm
Ioff, A/um	2.87e-16	1.44e-15	2.87e-15
Ion, A/um	1.08e-3	5.37e-3	1.07e-2

Table 2.2: Current values varying gate length

The leakage curent varies of one order of magnitude varying the gate length from 200nm to 20nm, while the drive current remains quite stable.
The model seems to be a quasi ideal model, since going from 200nm to 20nm of channel length the characteristic doesn't change. This is quite strange, since one of main issues of FinFETs is the increasing of leakage current and subthreshold slope when a short channel device is considered.
Here, the curves remains stable and increases in a quasi linear way, so that a real difference between long channel and short channel behaviour can't be appreciated. Furthermore, the threshold voltage seems to be not influenced by channel length variation.

In conclusion, a continuous analytical model for DG MOSFET were extended to DG FinFET. The model has been derived from "analytic solutions of Poisson's and current continuity equation fro long-channel DG MOSFETs" [1]. The results were in agreement with those present in [4], hence include all operating regions of FET.

2.3 Fasarakis Analytical Model

This compact model has been developed for lightly-doped short-channel triple-gate fin-shaped FET [6]. However, if the top gate oxide is much thicker than the gate oxide on the two sides, the TG FinFET can be treated as a DG FinFET.
In this thesis, a DG FinFET is modeled first and compared with Taur model previous explained. Then , it is extended to the case of TG FinFET. Fasarakis model, based on prevoius analytical modeling of drain current in DG MOSFETs, derives a "fully analytical and compact drain current model valid in all regions of operation for FinFETs" [6]. Several effect has been taken into account, so quantum-mechanical (QMEs) and short-channel effects such as threshold-voltage shifts, DIBL and subthreshold slope degradation. Also the effects of series resistance, surface roughness scattering, channel length modulation and saturation velocity in the sauration region were considered [6].

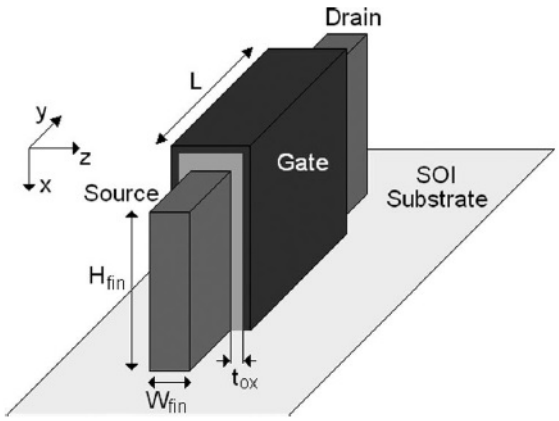

Figure 2.4: 3D Representation of FinFET (taken from [6])

This model is based on analytical expressions for the threshold voltage and SS of lightly doped DG and TG MOSFETs [4]. Taking this as a starting point, it has been derived a fully analytical and compact drain-current model valid in all regions of operation for TG FinFETS.

In particular, it has been derived an unified expression for the inversion charge

and drain current that is valid in all operation regions.

The model can be extended to a DG FinFET by changing the effective channel width definition.

$$W_{TG} = H_{fin} + \frac{W_{fin}}{2} \quad W_{DG} = 2 * H_{fin} \tag{2.11}$$

Where W is the effective channel width of a Triple Gate and of a Double Gate FinFET, respectively. It has been considered here that each half of the top gate width W_{fin} contributes to the side gate of width H_{fin} [6].

The drain-current equation of the modeled FinFET is similar to the one of DG MOSFET expressed with the unified charge-based equation [6], but with modified threshold voltage V_{th} and subthreshold swing coefficient η_{TG} and with increased channel width W.

The TG FinFET drain current is derived as follows:

$$I_d = \mu_o \frac{2W}{L} \frac{\epsilon_{ox}}{t_{ox}} (2V_T)^2 [(q_{is} - q_{id}) + \frac{(q_{is}^2 - q_{id}^2)}{2}] \tag{2.12}$$

Where μ_0 is the low-field electron mobility, W is the channel width, L is the channel length, ε_{ox} is the gate oxide permittivity, t_{ox} is the gate oxide thickness, and V_{th} is the thermal voltage.

It has been noticed that the first term in the above equation brings a dominant contribution in the subthreshold region, while the second charge term is more dominant in the above-threshold region. In the above expression, q_{is} and q_{id} are the normalized inversion sheet-charge densities calculated at the source and drain, respectively, and that are calculated from the unified normalized inversion sheet-charge density of DG MOSFET [4].

The characteristic of the device can be studied by evaluating the threshold voltage in an accurate way. In particular, starting from the strong inversion region, the normalized sheet-charge density can be written as:

$$q_{ix1} = LambertW[\exp\frac{1}{2V_{th}}[(V_g + \Delta V_t - V_{fb} - V_x) + 2V_{th}ln(\frac{qt_{ox}}{\varepsilon_{ox}}\sqrt{\frac{n_i^2\varepsilon_{si}}{2kTN_A}})]] \tag{2.13}$$

The threshold voltage can be derived by equating the above equation with: $q_{ix2} = LambertW[\exp\frac{1}{V_{th}}(V_g - V_t' - V_x)]$.

The threshold voltage for a DG FinFET can be expressed as follows:

$$V_th = V_{fb} - \frac{A_{1,DG}(V_{bi} + V_d) + A_{2,DG}V_{bi}}{1 - (A_{1,DG} + A_{2,DG})} + \frac{V_t}{1 - (A_{1,DG} + A_{2,DG})}ln(\frac{Q_{th}N_A}{n_i^2 W_{fin}}) \tag{2.14}$$

Where V_bi is the built-in potential at the source/drain interface, and $A_{1,DG}$,$A_{2,DG}$ are parameters which are function of the device natural length and channel length. If such parameters are oppurtunal changed, the model can be succesfully extended to the TG FinFET.

The minimum carrier sheet density obtained from the above analysis of the sheet-charge density in the strong inversion, is given by:

$$Q_{th} = (\frac{2V_{th}}{q})(\frac{C_{ox}^2}{C_{Si}}) \tag{2.15}$$

Where $C_{Si} = \varepsilon_{si}/W_{fin}$. This analytical expression leads to a calculation of the characteristic of the device.

Several effects have been included in this model. The first one is the channel length modulation. The CLM effect can be described as the pinchoff in the channel that moves from drain toward the source when the V_{ds} is increased beyond the saturation voltage $V_{dsat} = V_g - V_{th}$. This effect can be seen as the reduction of the physical gate length, such that the effective electrical gate length is given by

$$L' = L - \Delta L \tag{2.16}$$

where ΔL is the gap between L and the channel pinchoff. So, considering the CLM effect, the drain-current equation becomes [6]:

$$I_d = 2W\mu_o \frac{\epsilon_{ox}}{t_{ox}}(2V_T)^2[\frac{q_{is} - q_{id}}{L} + \frac{1}{2}\frac{(q_{is}^2 - q_{id}^2)}{L - \Delta L}] \tag{2.17}$$

The effects of series resisance and saturation velocity due to the horizontal drain field and surfac roughness scattering due to the vertical gate filed were considered, in order to compare the model with simulation and experimental results [6]. These effects are included in the electron mobiliy expression like:

$$\mu = \frac{\mu_o}{1 + \Theta_1 V_{th} q_{is}} \tag{2.18}$$

So, in this sense the final compact equation for drain current becomes:

$$I_d = 2W\mu \frac{\epsilon_{ox}}{t_{ox}}(2V_T)^2[\frac{q_{is} - q_{id}}{L} + \frac{1}{2}\frac{(q_{is}^2 - q_{id}^2)}{L - \Delta L}] \tag{2.19}$$

The last effects that have been included are the QMEs, since for short channel FETs a quantum well is formed in the fin width between the two-side oxide layers. The model of QMEs used in this model inserts the carrier-energy quantization caused by the structural confinement, as a widening of the bandgap in thin films [6].
In the particular case of DG FinFETs, the minimum energy of the first subband above the conduction band is [6]:

$$E_{G1} = \frac{\hbar^2 \pi^2}{2m_e f f W_{fin}^2} \tag{2.20}$$

This correction results in an increase in the threshold voltage, such as:

$$\Delta V_{th}^{QM} = \alpha \frac{(\pi\hbar)^2}{2q m_{eff} W_{fin}^2} \tag{2.21}$$

Where α is equal to 1 for DG and 2 for TG.
So, as first QME effect, this is the shift of V_{th} due to structural confinement, including the second effect of bias-independent quantum degradation gate capacitance [22], [23].
The second effect arises from the quantum-mechanical distribution of the inversion charge, showing a peak inside the substrate at some distance away from the $SiO_2 - Si$ interface. [6] This effect can be accounted for by considering two capacitance values

connected in series: the oxide capacitance formed by the physical oxide layer and the capacitance developed within the average distance of Δz inside the silicon from the interface [22], [23].
The QME results in an henanced value of the gate oxide thickness given by:

$$t_{ox}^{QM} = t_{ox} + \Delta z \frac{\epsilon_{ox}}{\epsilon_{Si}} \tag{2.22}$$

It is obvious to understand that this modified value of t_{ox} results in a shift of the threshold voltage by $\Delta V_{th,tox}^{QM}$. This effect is calculated by replacing t_{ox} with t_{ox}^{QM}. Thus, including the QMEs in the drain-current equation, the classical threshold V_{th} is replaced by $V_{th}^{QM} = V_{th} + \Delta V_{th}^{QM} + \Delta V_{th,tox}^{QM}$ and t_{ox} with t_{ox}^{QM}.

2.3.1 Matlab Implementation

The trancharacteristic of DG FinFET varying the channel length has been simulated. The device parameters extracted from Fasarakis model [4] are described in the table below:

Quantity Name	**Value**	**u.m. (S.I.)**
Gate Length	200 - 20	nm
Oxide Thickness (t_{ox})	1	nm
Fin Width (W_{fin})	10	nm
Temperature (T)	300	K
Source/Drain doping concentration (N_{sd})	10^{20}	cm^{-3}
Channel doping concentration (N_{ch})	10^{15}	cm^{-3}
Metal workfunction ϕ_m	4.1	eV

Table 2.3: Input data used for implementation of Fasarakis model [6]

The channel length variation was useful to study the behaviour of the analytical model and verify the reliability of the model with scaling devices.

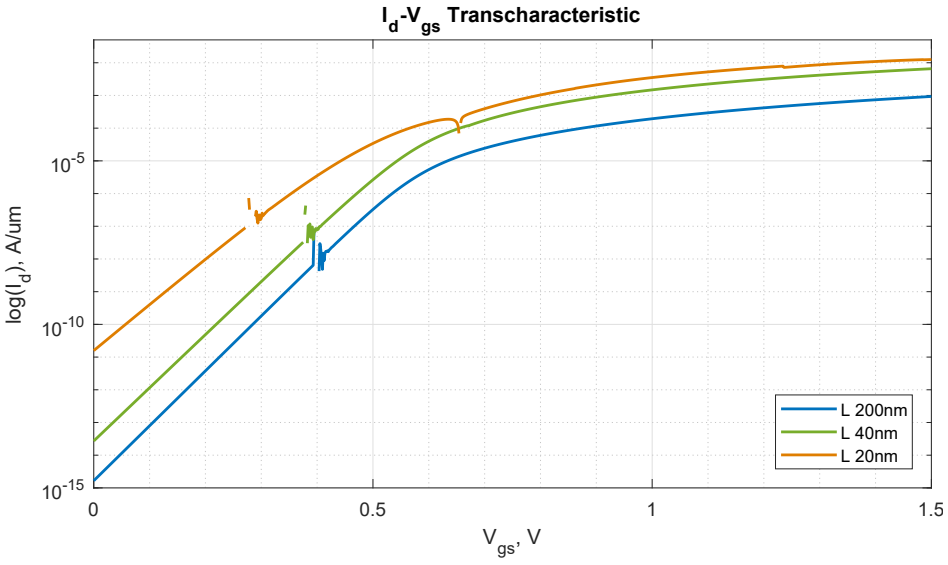

Figure 2.5: Transcharacteristic in logarithmic representation varying gate length ($V_{DS} = 1V$)

Figure (2.5) shows the results of the implemented model where gate length parameter was varied. The trend of the simulated model is in agreement with the physical model described in [4]. In particular, the most important extracted values are riassumed in the table below:

Parameters	L = 200nm	L = 40nm	L = 20nm
Ioff, A/um	1.66e-15	2.71e-14	1.57e-11
Ion, A/um	9.31e-4	6.60e-3	1.25e-2
Vth, V	0.57	0.58	0.72
SS, mV/dec	59.53	61.6	70.63

Table 2.4: Parameters values varying gate length

In this model, an appreciable variation can be observed by varing the channel length. In fact, the aim of this model validation was to check the accuracy of physical models, even if such models didn't agree with results present in leterature. In this case, there is a variation of 4 order of magnitude in leakage current if a long and short channel DG FinFET is taken into account. It can be observed an increase of 25% of subthreshold slope with reducing the gate length from 200nm to 20nm, and as consequence an increase of Vth of 30% is shown.

In conclusion, this analytical model for FinFET, which accounts short channel effects such as QMEs, CLM, were implemented in MATLAB in order to check its accuracy.

2.4 TG FinFET Analytic Models

Fasarakis compact model for a DG FinFET can be extended to a rectangular TG FinFET and hence to a trapezoidal one [5], engineered by Intel. Equivalent non planar device parameters and corner effects have been included.
For compact modeling, the non vertical sidewalls are assumed to be symmetric with equal slopes of the lateral sides, such the real fabricated device by Intel [20].
The triangular shape of the fin can improve the electical characteristic of a trigate FinFETs.

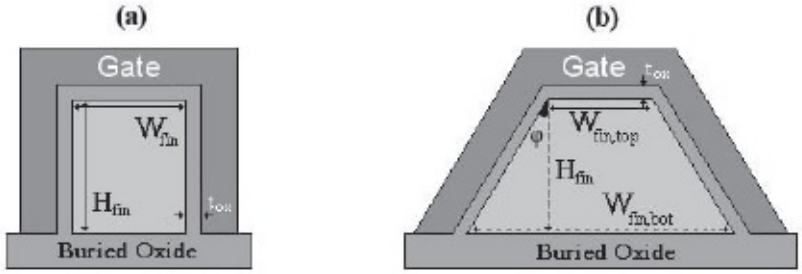

Figure 2.6: Schematic representation of (a) Rectangulal Re-TG FinFET, (b) Trapezoidal Tz-TG FinFET (taken from [5])

In the rectangular TG FinFET compact model, physical effects such as SCEs, filed-dependent mobility, series resistance, CLM and QM effects were included [5]. Several considerations have to be done with a Re-TG FinFETs, such as the fact that in non planar devices, significant error is introduced in Cox when $tox/Wfin > 0.1$ [21]. The model implemented is the same as for DG FinFET, except for the effective channel width. For the trapezoidal structure, the effective channel width is found to be:

$$W_{fin} = W_{fin,top} + \frac{\lambda}{\lambda + 1}(W_{fin,bot} - W_{fin,top}) \tag{2.23}$$

2.4.1 Matlab Implementation

The compact model for DG FinFET was extendend to Rectangula TG-FinFET. Furthermore, a comparison of electrostatic behaviour between a rectangular and a trapezoidal TG FinFET was carried out.
Device parameters are extracted from [5], and in the table below are riassumed the most relevant parameters used for the simulation.

Quantity Name	**Value**	**u.m. (S.I.)**
Gate Length	50	nm
Oxide Thickness (t_{ox})	1	nm
($W_{fin,bot}$)	15	nm
($W_{fin,bot}$)	13	nm
H_{fin}	30	nm
Source/Drain doping concentration (N_{sd})	$5 * 10^{19}$	cm^{-3}
Channel doping concentration (N_{ch})	10^{15}	cm^{-3}
Metal workfunction ϕ_m	4.1	eV

Table 2.5: Input data used for implementation of Fasarakis model of Tz-TG and Re-TG FiNFET (taken from [5])

In the figure below is shown the $I_d - V_g$ characteristic of the descripted device, simulated with $V_{ds} = 1V$.

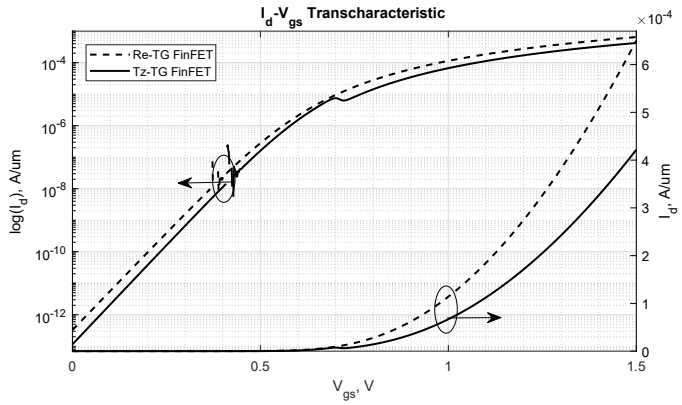

Figure 2.7: Comparison of $I_d - V_{gs}$ characteristic of Tz-TG FinFET and Re-TG FinFET

The characteristic in figure (2.7) shows the variation of electrical parameters if a rectangular or a trapezoidal structure is considered for FinFET. As it can be observed from the table below, the most evident variation between the two named structure is in drive current. In fact, it can be noticed that the current in on state increase by a factor of 1.5X, while all the other electrical parameters remain quite stable.

Parameter	Tz-TG	Re-TG
I_{OFF}, A/um	1.15e-13	3.27e-13
I_{ON}, A/um	4.21e-4	6.5e-4
Vth, V	0.57	0.54
SS, mV/dec	65.53	64.74

Table 2.6: Electrical parameters extracted from simulation

Furthermore, the compact model for TG FinFET was extended to Trapezoidal TG FinFET. Since the model is the same of previous analysis of DG FiNFET, also in this case all short channel effcts are taken into account. Furthermore, it were considered the corner effect and the effect of the top gate on the natural length [5]. Device parameters used for MATLAB simulation are shown in the table below:

Quantity Name	**Value**	**u.m. (S.I.)**
Gate Length	25	nm
Oxide Thickness (t_{ox})	1	nm
($W_{fin,bot}$)	15	nm
($W_{fin,bot}$)	5	nm
H_{fin}	30	nm
Source/Drain doping concentration (N_{sd})	$5 * 10^{19}$	cm^{-3}
Channel doping concentration (N_{ch})	10^{15}	cm^{-3}
Metal workfunction ϕ_m	4.1	eV

Table 2.7: Input data used for implementation of Fasarakis model of Tz-TG FiNFET (taken from [5])

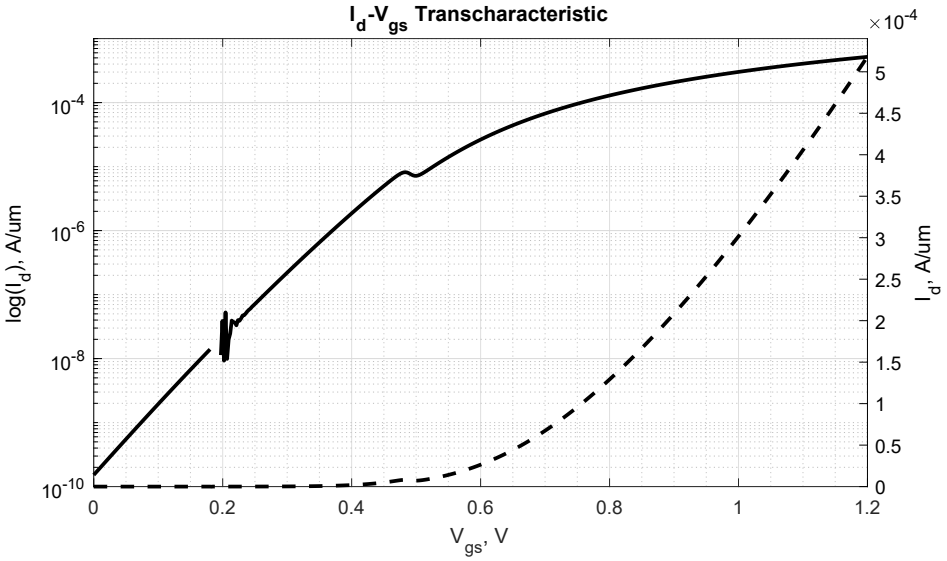

Figure 2.8: Simulated transfer-characteristic of a Tz-TG FinFET

In the figure above is shown the $I_d - V_g$ characteristic of the descripted device, simulated with $V_{ds} = 1V$. It can be observed that there is not so evident variation in electrostatic behaviour with respect to the short channel DG FinFET simualted in section (2.3.1).
Such result is in agreement with leterature, since a trapezoidal structure is done because of a ease fabrication but it doesn't lead to any real improvement in electrostatic behaviour. However, reducing the gate length of the Tz-TG FinFET, the current in off state increases of 3 order of magnitude for reducing the gate length of an half.

Parameters	Extracted Values
Ioff, A/um	1.52e-10
Ion, A/um	5.18e-4
Vth, V	0.492
SS, mV/dec	85.15

Table 2.8: Parameters values of a Tz-TG FinFET simulated in Matlab

Chapter 3

Physical Simulations of FinFET

3.1 Double-Gate FinFET Simulations

TCAD Synopsis Sentaurus simulations were carried out with the aim to validate the previous implemented models. The structure which this work referred to is the same for all the models. The device parameters are shown in tha table below:

Quantity Name	**Value**	**u.m. (S.I.)**
Gate Length	200 - 20	nm
Oxide Thickness (t_{ox})	1	nm
Fin Width (W_{fin})	10	nm
Temperature (T)	300	K
Source/Drain doping concentration (N_{sd})	10^{20}	cm^{-3}
Channel doping concentration (N_{ch})	10^{15}	cm^{-3}
Metal workfunction ϕ_m	4.1	eV

Table 3.1: Input data used for implementation of Fasarakis model [6]

The structure extracted from the physical simulation is shown below and is quite similare for both DG and TG FinFET, since the difference is in the thickness of top gate oxide. The colours refer to the materials used for the simulations, so a Silicon fin and a Silcon channel, Aluminum as gate metal and SiO2 for gate oxide.

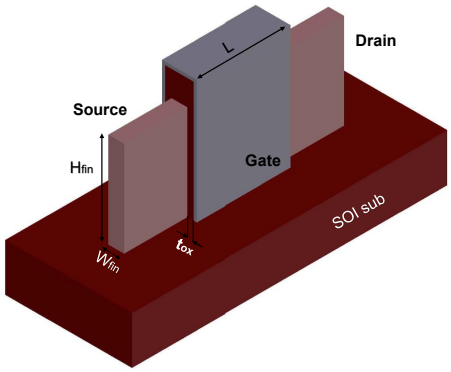

Figure 3.1: FinFET structure

The IV characteristic of a DG FinFET with channel length of 200nm was simulated in TCAD Synopsis Sentaurus, with Vds=1V.

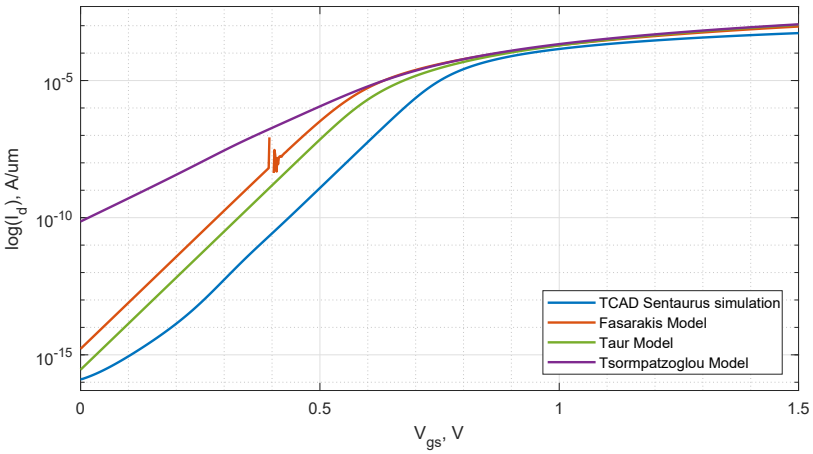

Figure 3.2: L 200nm

The models based on DG MOSFET could be potentially good to describe a long channel FinFET. However, the Tsormaptzoglou one seems to be far from the physical simulation in the off state also for a long channel device. Instead, Taur model, which is also based on DG MOSFET modelling, results in a quite good approximation of the FinFET.

Other simulations had been done with the same approach, varying the gate length in order to going in deep with scaling and investigate on FinFET limits.

The following figures represent the same simulation with gate length respectively of 40nm and 20nm.

The same structure was simulated for all the models implemented. In particular a comparison was done for long channel FinFET, and one for a short channel.

In fact, a difference in the behaviour was noticed if a long channel or a short channel device was considered. This is due to the physics approximation of the models.

In particular, since Taur and Tzompazoglou considered the FinFET as a MOSFET with a very thin box oxide, they are not so accurate as can be Fasarakis. In the figure above, a DG FinFET with gate length of 200nm was compared among different compact models and Sentaurus.

Taur and Fasarakis seems to be more accurate than Tzompazoglou, even if a long channel is considered.

In the figure below, the same comparison was done for the case of a short channel DG FinFET.

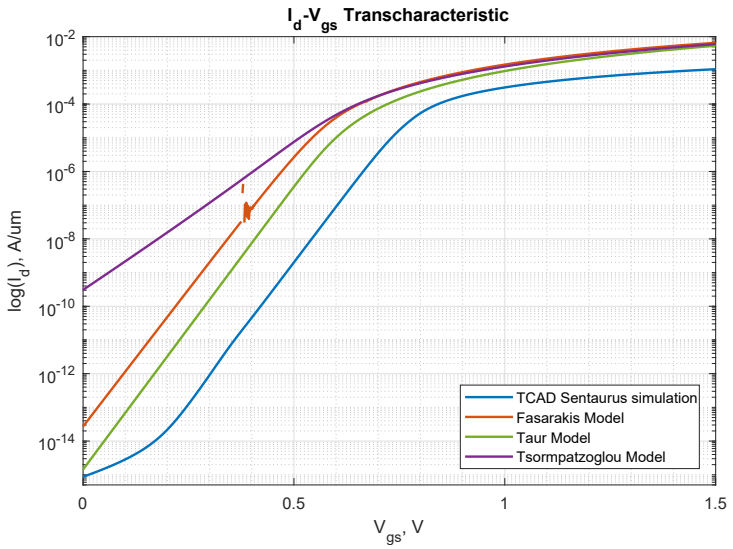

Figure 3.3: L 40nm

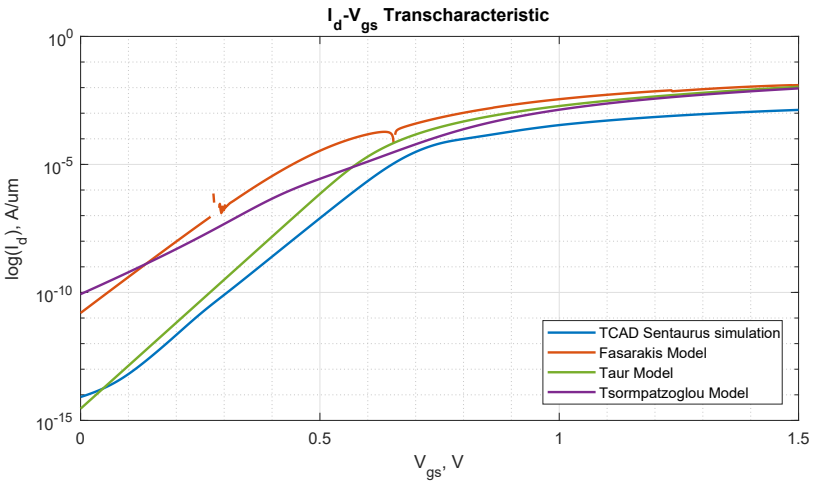

Figure 3.4: L 40nm

The last plots put in evidence the behaviour of the analytical models implemented and the physical simulations, in the case of short channel FinFETs. Even if Taur model seems to be the most accurate model, it is not considered as the best one. In fact, it can be noticed that it doesn't vary with gate length reduction, so it is not so reliable. Also Tsormaptzoglou is not an accurate model, since it doesn't respect the trend of such physical simulations.

The table below shows the most important parameter extracted from the physical simulation varying the channel length in a DG FinFET.

Parameters	L=200nm	L=40nm	L=20nm
Ioff, nA/um	2e-5	1.57e-4	3.27e-6
Ion, uA/um	1.34e3	1.08e3	5.38e2
Vth, V	0.87	0.82	0.86
SS, mV/dec	67.74	61.4	60.5
Gm, S/um	2.15e-3	1.59e-3	8.41e-4

Table 3.2: Important parameters extrcted from TCAD Synopsis Sentaurus

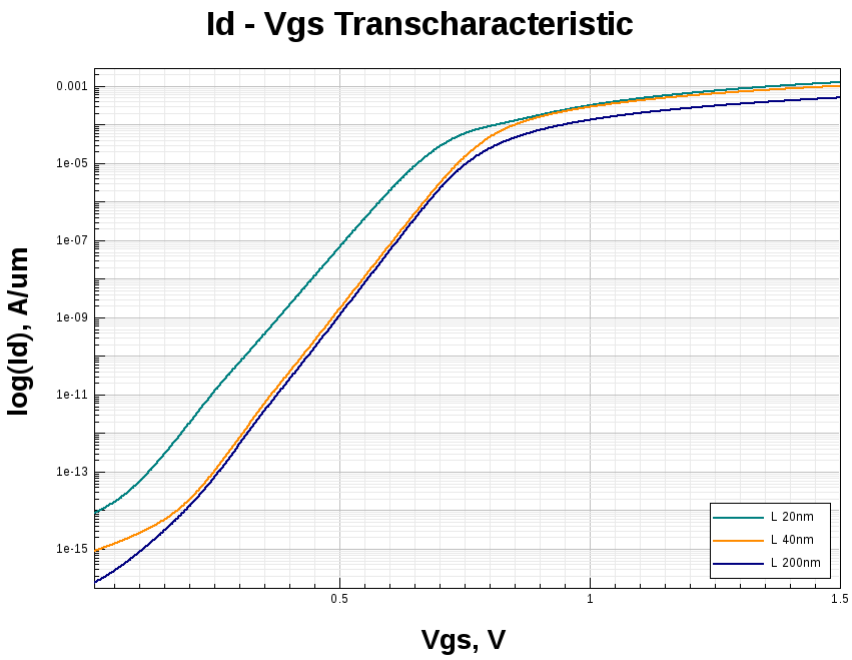

Figure 3.5: TCAD Synopsis Sentaurus results of DG FinFET simulation varying channel length L = 200nm - 40nm - 20nm

From the above results, it can be observed that the device simulated it is a quasi ideal device, since the sbthreshold slope is near the thermal limit of 60mV/dec and the current in the off state is lower than usual. In fact, in the paper which this part of the work is referred to, the current in the on state is quite higher.

However, these simulation ar useful to understand and better validate the anlytical model implemented.

Finally, from these analysis, it can be observed that the Fasarakis model is the most reliable model to describe the electrostatic characteristic, if an accurate and reliable trend among the variation of channel length is considered. Since the aim of these simulations was to check the most reliable and accurate analytical model, what it did matter was not the extact value among all simulations compared, but the respect in the trend of scaling transistor. The model that is the most reliable from this point of view is the Fasarakis one, since an appreciable variation between logn channel and short channel can be seen from the presented electrostatic analysis.

3.2 Gate-All-Around FET Simulations

The analysis of FinFET exploit in simulation of GAA FET, in order to investigate on further scaling of device and improvement of electrostatic characteristic.
Device parameters are presented in the table below:

Quantity Name	**Value**	**u.m. (S.I.)**
Gate Length	40	nm
Oxide Thickness (t_{ox})	1	nm
(t_{si})	10	nm
Source/Drain doping concentration (N_{sd})	10^{20}	cm^{-3}
Channel doping concentration (N_{ch})	10^{15}	cm^{-3}
Metal workfunction ϕ_m	4.1	eV

Table 3.3: Input data used for implementation of GAA FinFET

The metal gate is Aluminum, while the channel is made of Silicon. A TCAD Synopsis Sentaurus simulation was carried out to study the electrostac behaviour and the temperature variation of a Silicon gate all around FET, whose structure is shown below:

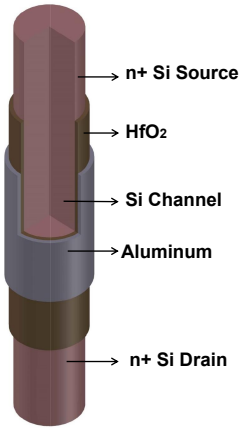

Figure 3.6: Schematic representation of GAA FET for physical simulation

In particular, a variation of gate dielectric material was done in order to study the improvement of the current with dielectric permittivity, as shown in the following figure:

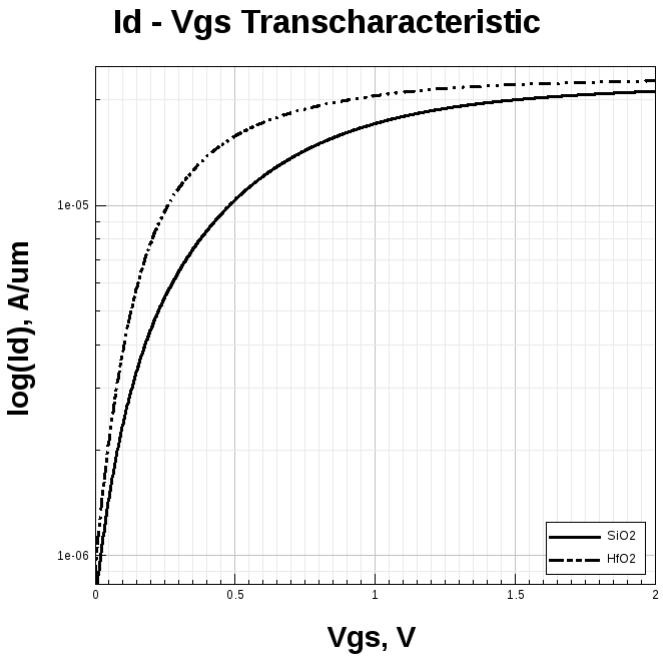

Figure 3.7: IV characteristic of GAA FET varying gate dielectric material, with Vds=1V

It can be demonstrated that varying the gate dielectric from SiO2 to HfO2 it varies the permittivity by a factor of 6. This leads a decrease of the subhreshold slope, paying with an increase of leakage current.

Parameters	SiO2	HfO2
Ion, A/um	2.13e-5	2.28e-5
Ioff, A/um	9.23e-7	1.2e-6
Vth, V	0.164	0.25
SS, mV/dec	94.95	71.72

Table 3.4: GAA FET results with gate dielectric variation

Furthermore, a temperature analysis was carried out for the same structure. In the following tables are described the most important electrical parameters influenced by a variation of temperature.

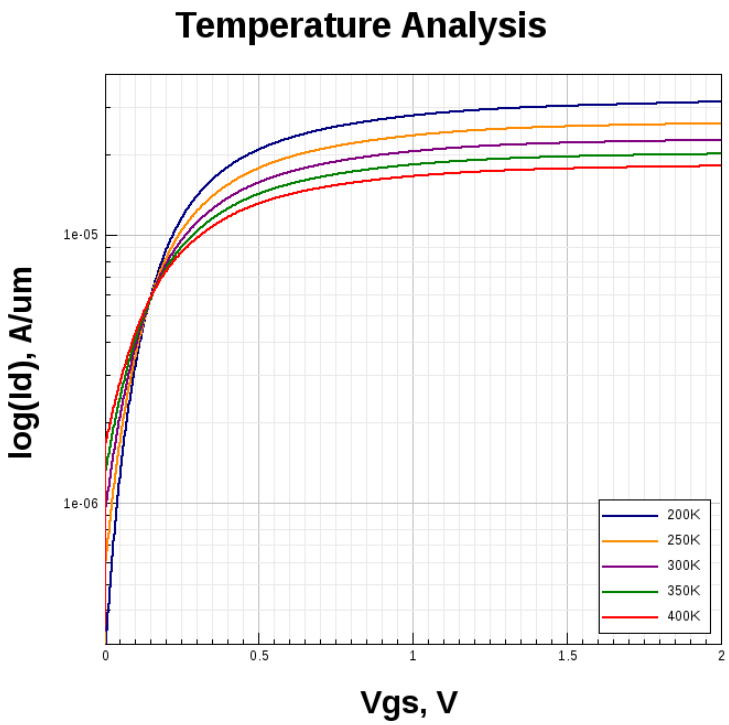

Figure 3.8: Comparative Temperature Analysis of GAA FinFET

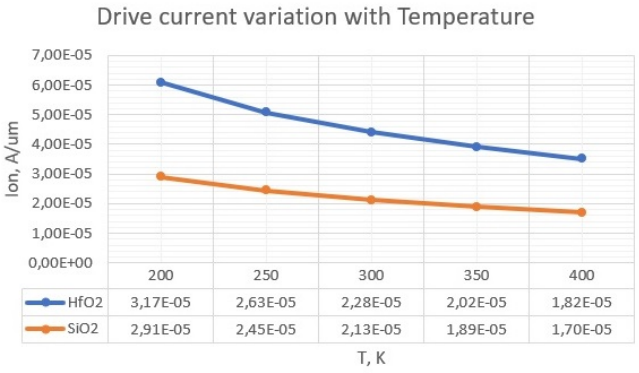

Figure 3.9: Comparative Temperature Analysis of drive current in GAA FinFET

In particular, as can be shown from figure (3.7), the current in the on state

does'nt vary in an evident way with temperature variations from 200K to 400K. On the other hand, as can be seen in the figure below, the off current increases of about two order of magnitude, while thesubthreshold slope increases in a dramatic way by a factor 4.

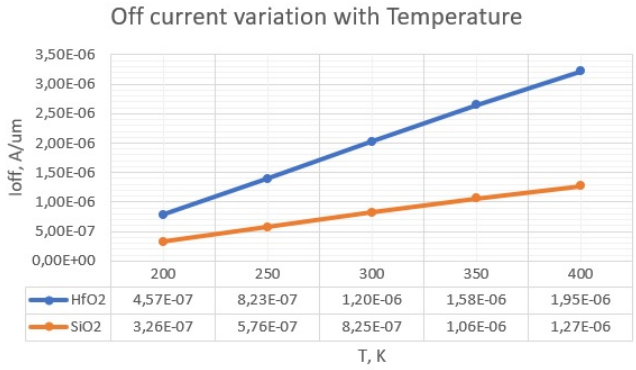

Figure 3.10: Comparative Temperature Analysis of subthreshold current in GAA FinFET

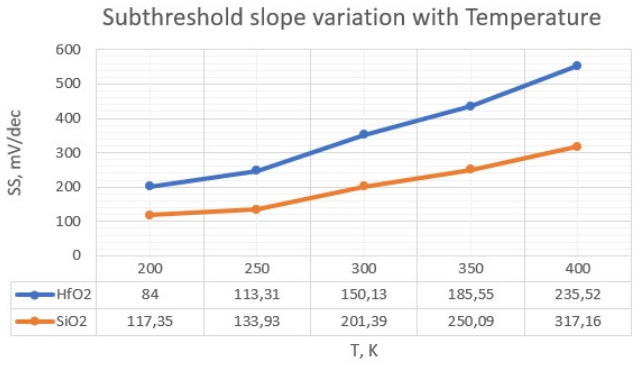

Figure 3.11: Comparative Temperature Analysis of SS in GAA FinFET

3.2.1 Nanowires FET Simulations

Finally, a further scaling of gate length was done. So, a nanowire fet was realized and simulated in TCAD. Tungsten as gate metal and Hfo2 for gate dielectric.

Quantity Name	**Value**	**u.m. (S.I.)**
Gate Length	15	nm
Oxide Thickness (t_{ox})	1	nm
(t_{si})	8	nm
Source/Drain doping concentration (N_{sd})	10^{20}	cm^{-3}
Channel doping concentration (N_{ch})	10^{15}	cm^{-3}
Metal workfunction ϕ_m	4.1	eV

Table 3.5: Input data used for implementation of GAA FinFET

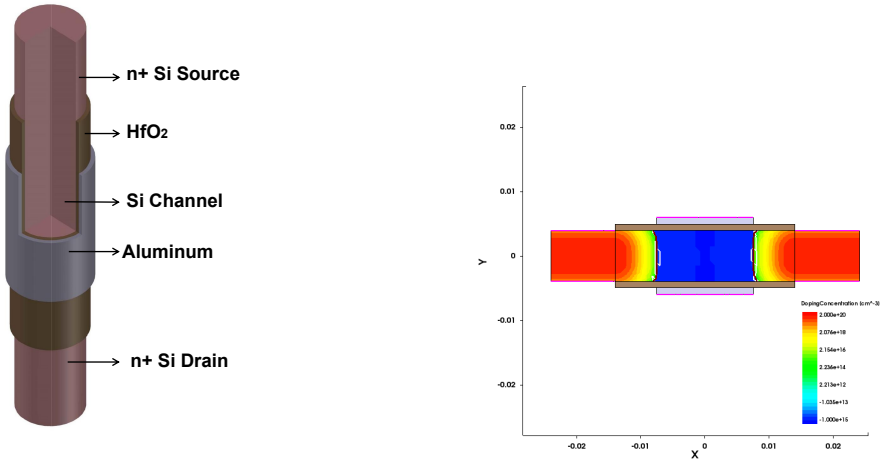

Figure 3.12: NW FinFET Structure - Cross section of NW FET

The characteristic shows a better behaviour of the nanowire FET, in particular in the off state. In fact, the Ion over Ioff ratio increases reducing the channel length and modifying the other materials. Also the subthreshold slope leads to the physical thermal limit of such devices.

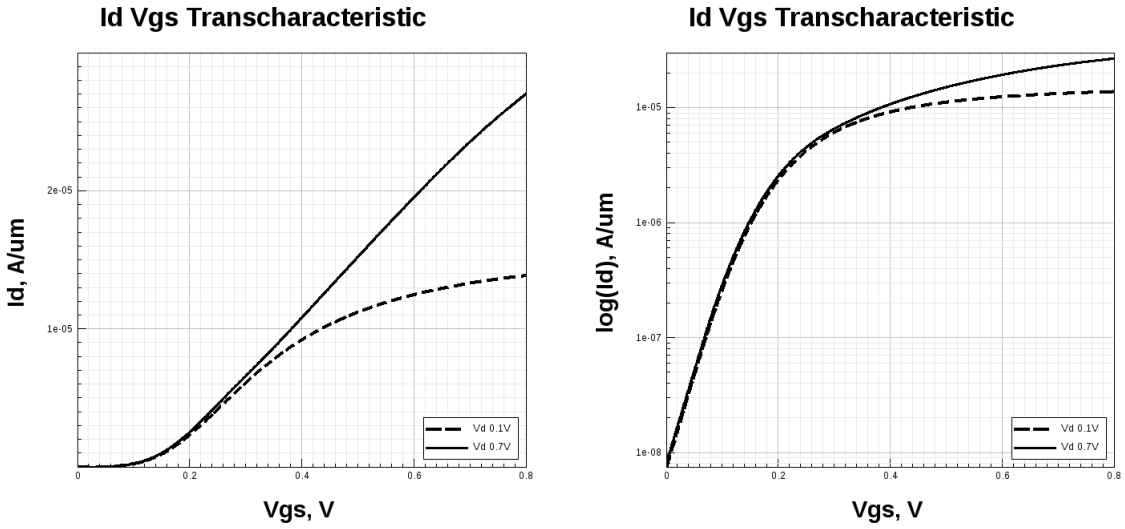

Figure 3.13: Linear and logarithmic IV characteristic of nanowire FET with Vds=0.7V

Parameters	Results
Ioff, A/um	9.55e-9
Ion, A/um	2.65e-5
SS, mV/dec	66.93
DIBL, mV/V	11e-3

Table 3.6: Parameters extracted from TCAD Synopsis Sentaurus for NW FET

The table above shows the most important parameters of an electrostatic analysis. The result seems to be a very good one with respect to the theorical expectations. Since the structure dimensions between the gaa and nw are completely different, no comparison can be done, but a quantitative evaluation of behaviour in electrostatic analysis can be done.

3.3 FinFET Main Issues

3.3.1 Advantages and Drawbacks

Altough FinFET is being a promising alternative to conventional MOSFET, since several benefits are exploited from its fabrication.
In particular, a Double Gate FinFET present a reduced electric field from the gate to the top of the fin, and this is due to the channel fabricated with an ultra-thin layer of Silicon on an Insulator.
In the case of a Tri-Gate FinFET, the gate wraps around the channel on the three sides which allows a better electrostatic control of the channel itself. Furthermore, the main benefit derives from the higher packing density due to the vertical structure.
One important feature of FinFET is the fin thickness, which needs to be smaller than or equal to the gate length [3]. The behaviour of FET is mainly due to the lithography process, since the scaling of the fin thickness doesn't depend on the oxide thickness.
Another advantage is the low threshold voltage variability with drain voltage variations. As a consequence, the channel is well controlled and litghly doped.

Fabrication of FinFETs is the same as the one of the conventional MOSFET, however several drawbacks have to be taken into account with device scaling in semiconductor industry. In fact, challenges and complexity in fabrication play an important role in the recent few years.

Limitations of MOSFET are mainly related to the channel length reduction and to the thermal limits of the device.
Thermal limits refer to the poor SS that characterize conventional MOSFETs. Short channel effects include velocity saturation effect, DIBL, impact ionization, hot carrier effect.
In fact, due to scaling of MOSFETs what can be noticed is the increase of the electric field, hence velocity of charge carriers increases. The problem is that when the electric field goes to a high value, velocity saturates.

Since electrons velocity is high, they can impact on silicon atoms and pair of electron and holes are created and this is the impact ionization [10]. As a consequence, this pair of electrons and holes enter into dielectric because of gaining high kinetic energy [10], hence changing the capacitance of the system and making it less reliable [10].
Secondly, as if for long channel devices the threshold voltage doesn't vary with the drain voltage, with the device scaling the threshold voltage decreases with the increasing of Vds.

Going in deep with drawbacks related to the FinFET design, several effects have to be taken into account in reducing the transistor dimensions.
Firstly, fin-width reduction let decrease of short channel effects, but there is an increase of parasitic drain/source capacitance and as a consequence there is a current reduction and transconductance reduction. Secondly, with the reduction of the fin width device temperature increases since heat cannot easily flow through the device. The effect is more pronounced in case of SOI technology, where buried insulating layer causes severe self-heating effects due to low thermal conductivity of oxide layer [3].

The well-known corner effect is defined as the increase in leakage current at the corner of the fin with the Vgs increasing. In fact, because of the device sclaing, the charge sharing occurs in the cornerregion of the two adjacent gates [3], hence there is a premature inversion at the corners and a trnasversal electric field is verified in being concentrated at the fin corners. As primary effect of the premature inversion at the corners, subthreshold characteristics degrade so higher off state current can be shown.
A solution to this problem is to fabricate a rounded profile of the fin. This allow a leakage current reduction , but the extraction of prasatics increases in complexity.

In particular, with dimension reduction becames difficult to extend FinFET RC parasitic models to be close to those extracted in simulations. A reduction of oxide thickness or channel doping concentration could solve corner effects.

Finally, as FinFET thickness reduces, the quantum effect reduces the density of available states at the band edge, hence carriers need more energy to occupy available states higher than the band edge, and be free to conduct device current.

Other challenges due to gate length reduction below 20nm are related to the needed of double patterning to print correctly with current lithography equipment. Secondly, electormigration becomes more of a concern as geometries shrink [3].While double patterning will make immersion lithography practical at 20nm, a new approach will be needed at 10nm [3], known as SIT.
In conclusion, FinFETs have several benefits, such as a quite good control of SCEs. However, fabrication is now complex with technological node below 20nm.
A new alternative is needed to overcome all the FinFET and MOSFET drawbacks.

Chapter 4

Tunnel Field Effect Transistors

"As the evice dimension further scales, the semiconductor devices are entering into a tunneling epoch" [44]. Recently, the "green-transistor" Tunnel Field Effect Transistor (TFET) has been proposed to overcome conventional MOSFET limits. It is a MOS' like tunneling transistor, and it can be seen as a gated Esaki tunneling diode based on Band to band tunneling working principle. It is simple to realize since its structure is the same of that of the conventional MOSFET, so the fabrication can be realized in CMOS technology, but source and drain regions are doped of opposite doping types.

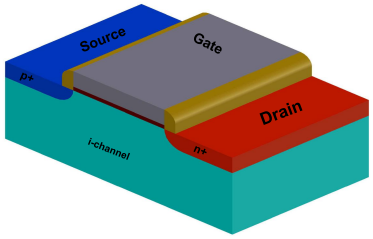

Figure 4.1: Schematic representation of n-MOS like Tunnel FET

In the last few years TFET is under research, since could bring several advantages with respect to the conventional MOSFET.

Since it can be seen as a gated p-i-n diode which works on the basis of reverse bias [10], such reverse pin junction present an high barrier. The higher barrier lead to a lower leakage current, so that such transistor could be the ideal device for low power applications.

The most evident difference in structure between MOSFET and TFET is the different doping between source and drain regions. Indeed, source and drain regions are heavily doped with opposite types, depletion region forms at the junction of

intrinsic region and the n+ doped drain region [10].
While thermal injection is the mechanism for the source of carrier injection used in MOSFET [25], BTBT is the mechanism used in Tunnel FET. A TFET is a three terminal pin diode, where source terminal is the source of majority carrier, drain terminal carries out the majority carrier, and finally gate terminal is used to control the majority carriers that move from source to drain. In particular, the channel needs of gate oxide since it prevents the current leakage from channel to gate [26]. The channel is an intristic region, and as consequence the threshold voltage fluctuations are removed since there is no dopant atom distribution. As it will be demonstrated in the next sections, the TFET present several issues. Since the tunneling region is smaller with respect to the silicon body [44], the current in on state is relativel low. An high doping concentration in both source and drain regions is needed in order to enhance the tunneling at the interface between source and channel junctions.

Following sections will be dedicated to the theorical study of Band to Band Tunneling, then physical simulations of TFETs different structures will be carried out. In particular, before the investigation on electrostatic behaviour of Tunnel FETs, a study of Esaki Diode will be useful to better understand the behaviour of current when a tunneling principle is considered. Finally, a comparison in electrostaci behaviour between MOFET and TFET will be done, to put in evidence the differences between the two devices.

4.1 Band-to-Band Tunneling in p-i-n Diodes

The p-i-n diode working principle is discussed in this section to better understand TFET. In fact, the latter can be seen as a gated p-i-n diode. A p-i-n diode is realized as the union of two junctions heavily doped, where an intrinsic region is sandiwched insde them. The intrinsic region lightly doped is useful to let the potential drop mostly in this region [44].

"The Esaki tunnel diode was first presented by Dr. Esaki in Physical Review, 1958. By forming the heavily doped p-n junction, the negative resistance was found in the forward I-V characteristics. This is the discovery of a new quantum mechanical tunneling phenomenon. This tunneling effect is called Esaki-Tunneling" [44].

The energy band diagram a thermal equilibrium is sohwn in the figure below:

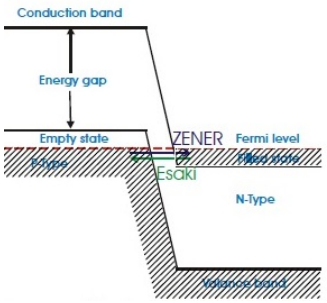

Figure 4.2: Energy band diagram of tunnel diode (taken from [44])

In off state, the barrier width is quite large, so that tunneling is suppressed. In such p-i-n diode there are two main tunneling current contributions: the Zener tunneling and the Esaki tunneling current. The first one is the current that flows from the valence band to the conduction band, while the latter one results from electrons flow from the conduction band to valence band. Furthermore, tunnel diode current comprises three main components: the tunneling current, the excess current and the thermal current.

The tunneling current from the conduction band to the valence band is given by the "number of electrons times the unoccupied states in the valance band times the probability for tunneling from the conduction band to the valance band without any energy change" [44].

$$I_{tunnel}(E) = (f_c(E)\rho_c(E))((1 - f_v(E)\rho_v(E))T(E) \tag{4.1}$$

Where f_c and f_v can be calculated with the Fermi- Dirac distribution functions and are defined as the probabilities of a quantum state to occupy the cunduction and valence band respectively [44]. Then, ρ_c and ρ_v are defined as the energy level densities in the conduction and valence band respectively. E is the energy level, and finally T(E) is the probability for tunneling from the conduction band to valence band.

Furthermore, the Esaki and Zener tunneling current can be derived by the integral of the tunneling current over the range of overlapping energy states.

The transmission probability T(E) can be derived by applying the WKB approximation on the Schrodinger time-dependent wave equation:

$$T(E) \sim exp^{-2\int p(x)\frac{dx}{\hbar}} \tag{4.2}$$

Where p(x) is the absolute value of the momentum of the particle in the barrier [44], $\hbar$ is the normalized Planck's constant.

So, if the WKB approximation is applied, the energy barrieri for tunneling can be approximate to a triangle, as shown in the figure below:

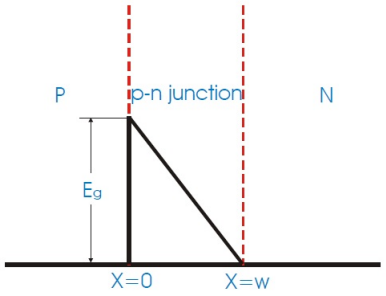

Figure 4.3: Triangular energy barrier approximation (taken from [44])

The probability of tunneling can be calculated as:

$$T(E) = exp(-\frac{4}{3}\frac{\sqrt{2m^*}}{\hbar}\frac{E_B^{3/2}}{e\varepsilon}) \tag{4.3}$$

Naming the Esaki and Zener tunneling current respectively I_E and I_Z, the total tunneling current can be derived as:

$$I_t = I_E - I_Z \tag{4.4}$$

It can be demonstrated that if no bias is applied, the Zener tunneling current equals to Esaki tunneling current [44]. If the bias is applied, he current increases as:

$$I_t = I_P(V/V_P)exp(1 - V/V_P) \tag{4.5}$$

where I_P and V_P are respectively the peak current and peak voltage. Finally, the complete current expression includes three main contirbutes: the esaki tunneling curent, the excess current and the thermal current.

$$J = J_t + J_x + J_{th} \\ = J_P(V/V_P)exp(1 - V/V_P) + J_V exp[A_2(V - V_V)] + J_0(exp^{qv/kT} - 1) \tag{4.6}$$

4.1.1 Physical Simulations of Esaki Diode

In order to understand the behaviour of the Esaki Diode explained in the prevous section, a p-i-n diode was simulated in TCAD Sentaurus.

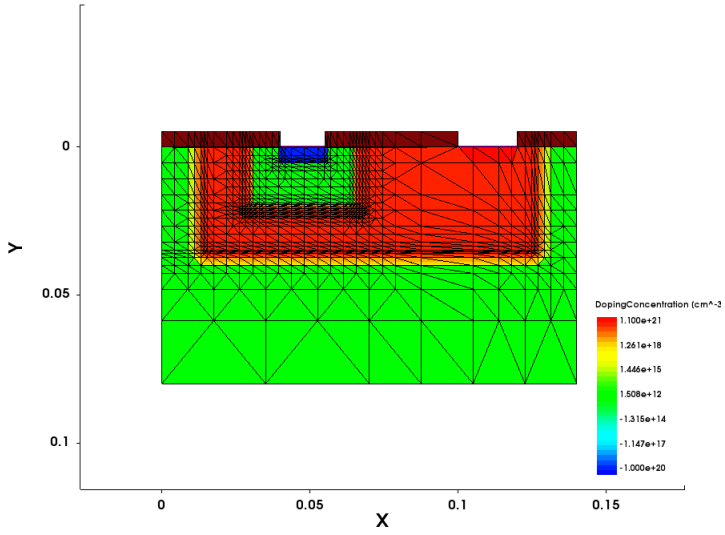

Figure 4.4: Esaki Diode structure

An Esaki diode is a highly doped pn junction which is based on band to band tunneling phenomenon.
The tunneling effect is defined as the non null probability of a quantum particle to tunnel across the barrier of a junction even if it has energy less than the energy barrier [29].
The probability increases with barrier energy decreasing , as shown in the above expression :

$$P \propto exp(-AE_bW) \tag{4.7}$$

Where P is the probability of a particle to tunnel across the barrier, Eb is the barrier energy of the junction, and W is the width of the barrier.

The IV characteristic that result from simulation is shown below:

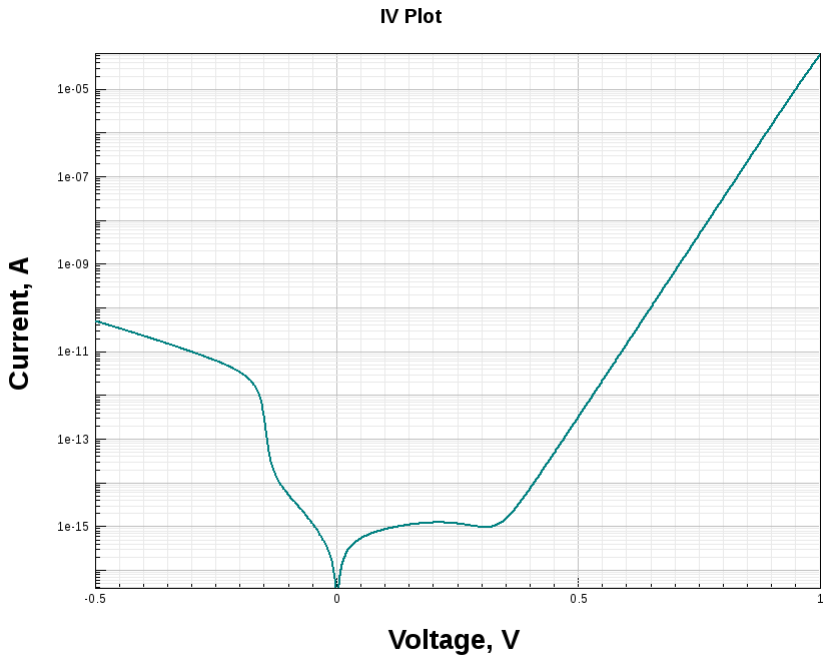

Figure 4.5: Esaki Diode IV characteristic

The main feature of the IV characteristic of a tunnel diode is the NDR (Negative diode region), while behind this region the Esaki diode acts as a normal diode. As voltage increases the current also increases until it reaches the so called peak current around 1e-15 A.
If voltage increases, the current starts to decrease, hence it is in the negative resistance region.
Beyond valley point the tunnel diode acts as normal diode.

4.2 Comparison between MOSFET and TFET

It could be useful to first compare MOSFET and Tunnel FET behaviour, to better understand the most evident differences among the two devices.

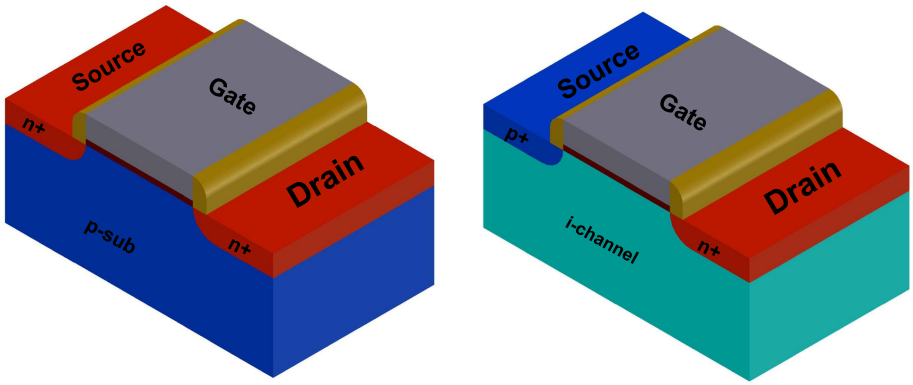

Figure 4.6: TFET and MOSFET structures

In the above figure it can be noticed that in the conventional MOSFET both source and drain regions are doped in the same way, while in the Tunnel FET the type of doping of source and drain is different.

From the band diagrams in off and on state that are shown below, it is easy to see that the first main difference between the two FETs is the working principle which are based on.

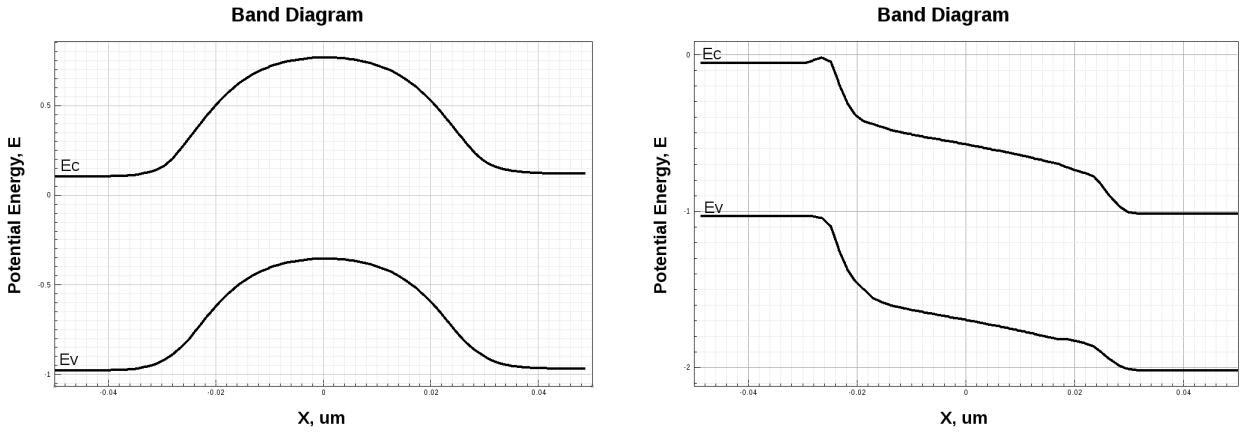

Figure 4.7: Conventional MOSFET Band Diagram in OFF-state and ON-state

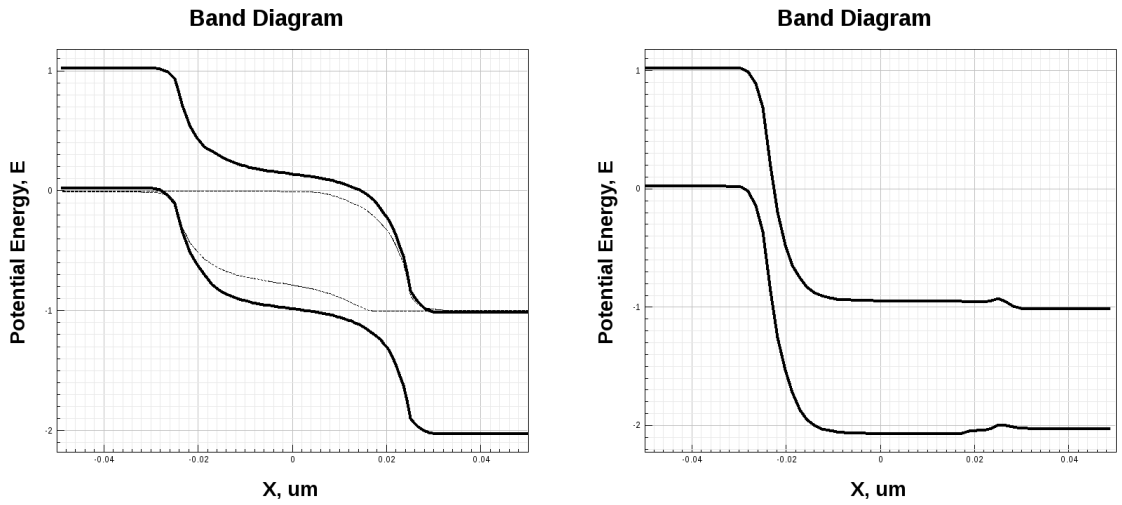

Figure 4.8: TFET Band Diagram in OFF-state and ON-state

In fact, electrons in MOSFET flow from source to drain through a thermionic emission physic, while Tunnel FET is based on band to band tunneling. So that, when the conduction band of the intrinsic channel goes below the valence band of the p-doped source, the electrons flow through the barrier toward the drain.
The main difference between a conventional MOSFET and the emerging TFET is in the working principle, since the latter is based on the principle of band to band tunneling phenomenon.
Before explaining the band to band tunneling principle, it could be useful to recall the conventional MOSFET principle.

In the OFF state, the conduction in MOSFET is limited by the source side p-n junction barrier which prevents the thermionic emission of carriers. In the ON state, the source barrier is negligible enabling thermionic emission of carrieris [31].

On the other hand, for TFETs in OFF state the transmission probability is low due to the wide source to channel tunnel junction barrier (low electric field) [31], and as consequence a very low leakage current can be shown.
In the ON state the tunnel barrier get narrower, hence it henables carriers to tunnel through it and go into the channel.

The TFET works by modulating the width of a tunneling barrier trhough the

gate, that is a different operation. In fact, in MOSFET the gate is used to modulat the height of the barrier and carrier must surmount that height via thermionic emission. The device is normally off, hence a wide barrier potential is present between the channel and the source, so that no BTBT occur and the leakage current is present but in a very small contribution.
The main effect in the working principle difference can be seen with physical simulation.

When a voltage is applied on the gate such that it is higher than the threshold voltage, the barrier potential between the source and the channel gets narrower. In this case, a tunneling current occurs and the device is the on state.
The transmission probability in a Tunnel FET is derived by the use of Wentzel Kramers Brillouin (WKB) approximation:

$$T_{wkb} \approx [\frac{4\lambda\sqrt{2mE_g^3}}{3qh[E_q + \Delta\phi]}] \tag{4.8}$$

where m is the effective mass, Eg is the band gap energy of the channel material, λ is the screening tunnel length. The screening tunnel length is defined as the extention of the transistion region at the source-channel interface [26], [28] .
While in MOSFET, the subthreshold swing is limited by the tail of the Fermi-Dirac distribution of electrons in the n+ source region, in the TFET the Fermi tail is cut-off by the band gap in the source-region.

Similar to a tunnel diode equation, the drain current is expressed as follows:

$$I = A \int_{E_C}^{E_V} [F_S(E) - F_D(E)]T(E)N_S N_D dE \tag{4.9}$$

Where T(E) is the tunneling probability, Fs(E) and Fd(E) are the source and drain side Fermi-Dirac distributin and Ns and Nd are the corresponding density of States [31]. In particular, the WKB approximation is used for tunneling probability.

A MOSFET and TFET devices were realized in TCAD Synopsis Sentaurus. The device parameters are shown in the table below:

Quantity Name	**Value**	**u.m. (S.I.)**
Gate Length	40	nm
Oxide Thickness (t_{ox})	3	nm
Silicon Thickness (t_{si})	10	nm
Temperature (T)	300	K
Source/Drain doping concentration (N_{sd})	10^{20}	cm^{-3}
Channel doping concentration (N_{ch})	10^{15}	cm^{-3}
Metal workfunction ϕ_m	4.1	eV

Table 4.1: Input data used for physical simulations of MOSFET and Tunnel FET [1]

The IV characteristic has been simulated by the use of TCAD Sentaurus, in order to check the theorical advantages of Tunnel FET over the conventional MOSFET.

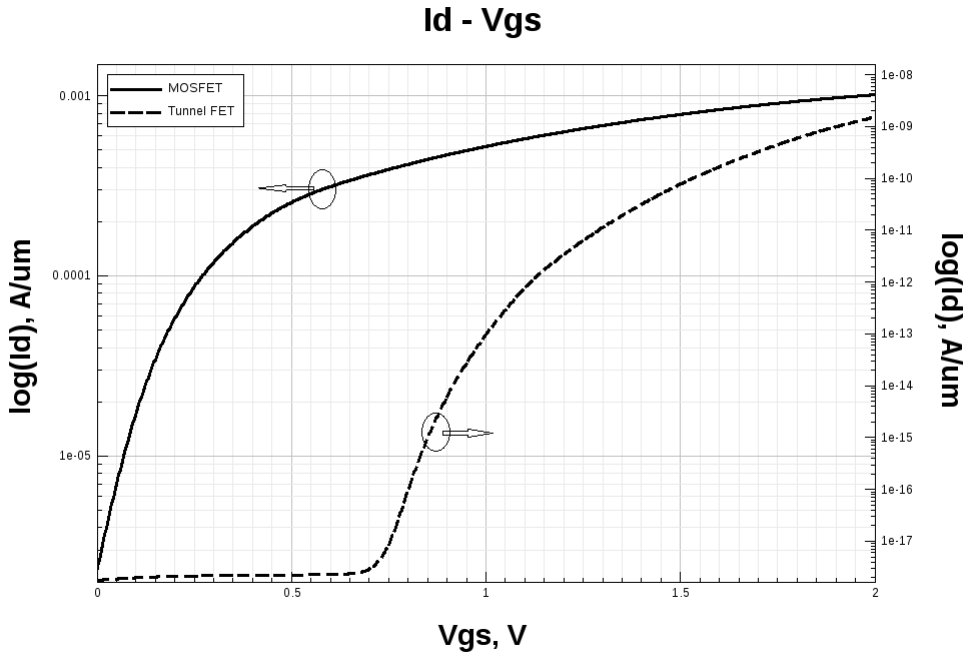

Figure 4.9: Id - Vgs Transcharacteristic for comparison of MOSFET and TFET behaviour

As can be seen from the plot and the table above, Tunnel FET shows a steeper characteristic with respect to the SOI MOSFET, but also a very low Ioff current. The main issue of this emerging FET is the low Ion and high threshold voltage,

Parameter	MOSFET	TFET
I_{OFF}, A/um	1.81e-9	1.82e-18
I_{ON}, A/um	1.02e-3	1.55e-9
G_m, S/um	7.11e-4	6.35e-9
SS, mV/dec	111.85	86.51
V_{th}, V	0.45	1.34

Table 4.2: MOSFET vs TFET most important extracted parameters

which pin it not to be used for low power applications.

4.2.1 Temperature Analysis

Also a temperature analysis has been carried out. In fact, since TFET is based on tunneling effect, it does not depend on temperature in on state. But, in the subthreshold region the dominant effect is the recombination, so the current in off state varies and it is strongly influenced by the temperature.
On the other hand, MOSFET characteristic degrades both in on and off state with temperature.

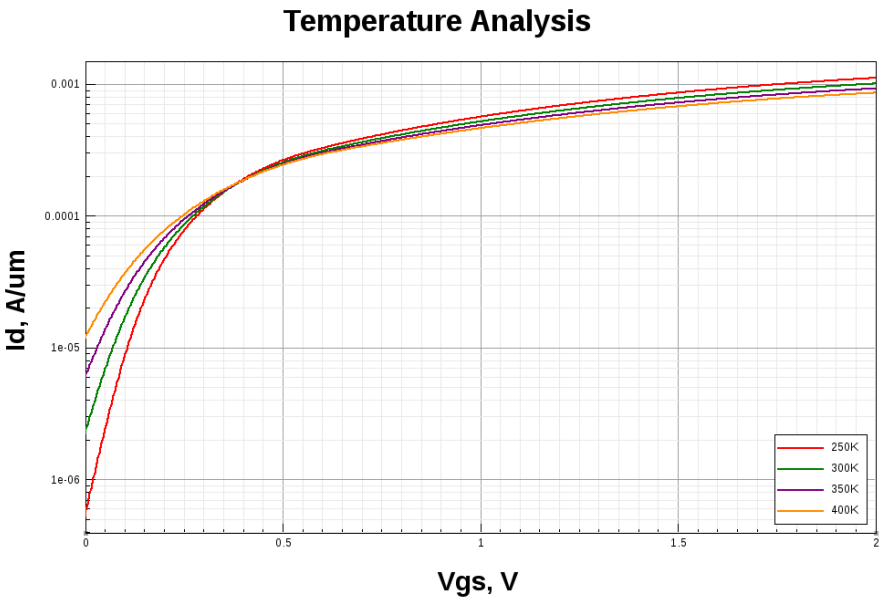

Figure 4.10: MOSFET - Temperature analysis

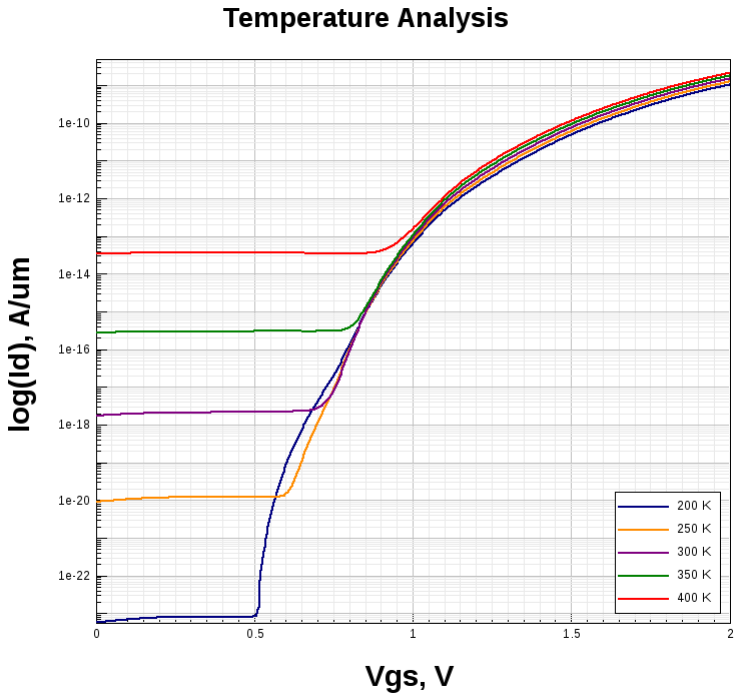

Figure 4.11: SG TFET - Temperature analysis

In particular, varying the temperature from 200K to 400K, what can be demonstrated is that in MOSFET case the off current increases of about 3 order of magnitude, SS increases by a factor of 3 (from 76,67 to 207,97), threshold voltge decreases and Ion decreases more than one order of magnitude.
On the other hand, TFET shows a stable on current due to tunnel effect, an increase of off current of about 8 order of magnitude but it still remains very low, and an increase of SS of a factor 5, but until the room temperature the subthreshold slope can overcome the thermal limit of 60mV/dec.

In Tunnel FET, the temperature dependence comes from the energy bandgap term in the expression of tunneling current [17]:

$$I_{ds} = A\frac{|E|^2}{\sqrt{E_g}}exp(-\frac{BE_g^{3/2}}{|E|}) \tag{4.10}$$

Where E is the electric field along the channel, Eg is the bandgap, A and B are Kane's parameters.
In particular, the bandgap expression depends on temperature as follows:

$$E_g(T) = E_g(300) - \frac{\alpha T^2}{T+\beta} \tag{4.11}$$

Where $\alpha = 4.73\text{e-}4$ eV/K and $\beta = 636$ K, while Eg (300) = 1.08 eV in the Silicon case.

From the above expression, it can be noticed that with temperature raising, bandgap reduces and as direct consequence drive current increases.
What can be noticed from a physical analysis of Tunnel FET is that, as in Esaki

Temperature	Ioff, A/um	Ion, A/um	SS, mV/dec	Vth, V
250	6.5e-7	1.12e-3	76.67	0.15
300	2.61e-6	1.02e-3	110.05	0.129
350	6.74e-6	9.39e-4	161.78	0.1
400	1.3e-5	8.71e-4	207.97	0.075

Table 4.3: MOSFET Temperature analysis

Diode case, both recombination and tunnel effect are combined in subthreshold region.
In particular, for low voltages applied to the gate,what can be shown is that recombination and tunneling are combined in a sum. While, over the threshold voltage tunneling is the dominant effect in the device.
For that reason, it is evident that at high gate voltages the temperature influences weakly the device, since BTBT is weakly depedent temperature. It is more dominant in the off state, since the SRH contribution dominates at low electric field and has a strong temperature dependence [17].

On the other hand, for a MOSFET there are several parameters that are temperature-dependent, such as threshold voltage, carrier mobility, saturation velocity and parasitic series resistance [17].
What can be noticed is that MOSFET drain current is more dependent on temperature fluctuations in comparison to Tunnel FET. This difference can be noticed in a particular way in th subthreshold region, since in the case of a MOSFET, the subthreshold current strongly depends on temperature through the square of intrinsic carrier concentration term [18].

In fact, the intrinsic carrier concentration $n_i$has a temperature dependence as:

$$n_i = N_a exp(-\frac{E_g}{2kT}) \tag{4.12}$$

Furthermore, the drain current in a MOSFET is directly proportional to mobility and threshold voltage which has temperature-dependent terms [17].

Temperature	Ioff, A/um	SS, mV/dec
200	6.15e-24	20.71
250	9.7e-21	48.10
300	1.85e-18	60.94
350	2.96e-16	70.38
400	3.71e-14	115.04

Table 4.4: TFET Temperature

In fact, if an increase in temperature is present, the threshold voltage shows a decreasing, so it can be seen is that the drain current increase with temperature. On the other hand, the temperature-dependent mobility term results in reduction of drain current with increase in temperature due to lattice scattering which degrades channel mobility [17].

4.3 Compact Models

To build TFET circuits and hence to make quite reliable performance predictions, closed form models for the drain current that contain the basic physics expression of the tunneling have been developed.
Next sections are dedicated to the description of quite a few compact models for the TFET that have been implemented in Matlab.

4.4 Hao Lu Model

This is an analytical model, based on the Kane-Sze formula, that describes the behaviour in IV characteristic of TFETs.
The generalized formulation widely configurable since is not specific to a particular TFET geometry [2].
The model is applied to the representation of a homojunction InAs double-gate n-TFET and a broken gap AlGaSb/InAs SG TFET. The model is extended into other operating regions by incorporating the ambipolar current and negative differential resistance [2].

4.4.1 Modeling

The device is normally in off-state, so that the minimum conduction band of the channel is over the maximum valence band of the source. In this case the device is in off state, suppressing band-to-band tunneling. If a bias is applied to the gate, the conduction band of the channel is shifted below the valence band of the source [2] . Electrons in the valence band tunnel into empty states in the channel and the transistor is ON [2].
Tunnel FET can be seen as a gated p-i-n junction. With this is mind, the main expression for tunneling current in such model derives from a generalization for three-terminals Zener tunneling in p-n junctions.

"The drain current is evaluated by integrating the product of charge flux and

the tunneling probability in the tunneling window, where the tunneling probability is calculated by applying the WKB approximation" [2]:

$$I_{dt} = afEV_{tw}e^{-b/E} \tag{4.13}$$

Where V_{tw} is the tunneling window, which relates to the energy band crossed by charges, E is the maximum electric field in the reverse biased junction, and a and b are geometric coefficients:

$$a = \frac{WT_{ch}q^3}{8\pi^2\hbar^2}\sqrt{\frac{2m_r^*}{E_g}} \qquad b = \frac{4\sqrt{2m_r^*E_g^3}}{3q\hbar} \tag{4.14}$$

Where m_r^* is the reduced effective mass, W is the channel width, tch is the channel thickness, Eg is the semiconductor bandgap.

"The tunneling process is evaluated as a particle tunneling through a triangular barrier, with a slope given by the electron charge times the electric field" [2]. "The detailed dependence of maximum electric field is taken to be linearly dependent on Vgs and Vds" [2] by dropping the second and higher order terms:

$$E = E_0(1 + \gamma_1 V_{DS} + \gamma_2 V_{GS}) \tag{4.15}$$

Where E_0 is the electric field at the source/channel junction if no bias is applied to both gate and drain terminals, while γ_1 and γ_2 are model coefficients. From the above formula it can be observed the electric field dependence from gate and drain voltages. In fact, as gate bias voltage increases, the electric field rises at the source-channel junction "by both enlarging the voltage drop and narrowing the tunneling barrier region" [2]. On the other hand, increasing the drain bias has a lesser effect due to the screening of the drain field by the gate electrode.

The tunneling window expression can control in a continuous way both sub-threshold and above threshold regions, as follows:

$$V_{tw} = Uln[1 + e^{(V_{gs}-V_{th})/U}] \tag{4.16}$$

In subthreshold region, the tunneling window has an exponenetial dependence from gate voltage, while in the above-threshold region, "it tends to a linear dependence with the gate bias".

The model is extended to the other regions, with several fitting parameters, hence it accounts for bias dependent subthreshold swing, saturation, the superlinear current onset, ambipolar conduction, and negative differential resistance. In this work, only the current for both positive Vgs and Vds is considered.

4.4.2 Matlab Implementation

Double Gate homojunction Tunnel FET were implemented in this model. Both devices shares the same channel material that is InAs, so both energy gap Eg and effective mass are the same. All fitting parameters are taken from Hao Lu model [2] and are shown in the table below:

Quantity Name	**Value**	**u.m. (S.I.)**
Gate Length	20	nm
Oxide Thickness (t_{ox})	1	nm
Silicon Thickness (t_{si})	5	nm
Temperature (T)	300	K
Source/Drain doping concentration (N_{sd})	10^{20}	cm^{-3}
Channel doping concentration (N_{ch})	10^{15}	cm^{-3}
Metal workfunction ϕ_m	4.1	eV
V_{th}	0.15	V
γ_0	0.64	-
γ_1	0.01	m^{-1}
γ_2	1.89	m^{-1}
Electric field E	0.507	MV/cm
λ	0.19	V

Table 4.5: Input data used for implementation of DG Tunnel FET [1]

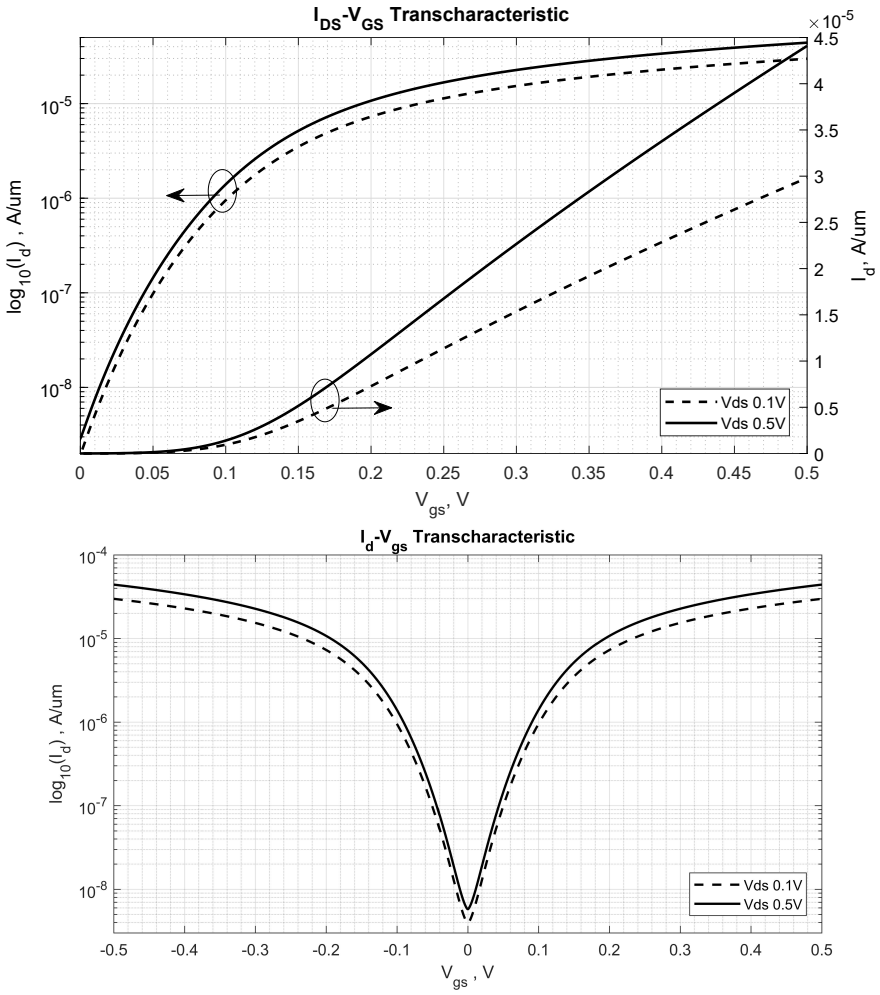

Figure 4.12: InAs DG TFET implementation of analytical model [2]

The results above are in according to the refering paper. However, several issues have been noticed in implementing such model. In fact, there is no possiblity to exploit structures different from that described in the paper.
In particular, the model seems to be not dependent on doping concentrations, geometries or gate dielectric variations.

4.5 Praveen Model

Another model on the same WKB approximation was implemented in MATLAB, with some differences. In fact this model allows to a gate engineering of the structure. Gate engineering refers to changing the architecture of the gate terminal of the TFET [15] by means of variation in screening length. The screening length or natural length, is defined as the spatial extent of the electric field, or the length over which an electric charge has an influence before being screened out by the opposite charges around it [19].
It depends upon gate geometry:

$$\lambda_{SG} = \sqrt{(\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{si} t_{ox})} \tag{4.17}$$

$$\lambda_{DG} = \sqrt{(\frac{\varepsilon_{si}}{2\varepsilon_{ox}} t_{si} t_{ox})} \tag{4.18}$$

$$\lambda_{GAA} = \sqrt{\frac{2\varepsilon_{si} t_{si}^2 (1 + \frac{2t_{ox}}{t_{si}}) + \varepsilon_{ox} t_{si}^2}{16\varepsilon_{ox}}} \tag{4.19}$$

Based on Kane's model, tunneling current general expression can be evaluated as

$$I = \frac{4q}{h} \int T(E)[f_S(E) - f_D(E)]dE \tag{4.20}$$

Hence:

$$I = \frac{W t_{ch} \sqrt{2m^* q^3} EV}{4pi^2 \hbar^2 \sqrt{E_g}} exp^{-\frac{4\sqrt{2m^* E_g^3}}{3q\hbar E}} \tag{4.21}$$

where the tunneling probability can be approximated as a triangle using the WKB approximation:

$$T_{tunnel} \approx \exp(-\frac{4\sqrt{2m_r^* E_g^{3/2}}}{3q\hbar\xi}) \tag{4.22}$$

where ξ is the uniform electrical field if triangle potential barrier is assumed.
It should be noted the BTBT occurs only if T_{tunnel} is high enough and there

are enough electrons at the starting side under Ev and enough empty states at the ending side above Ec [15].

With this in mind, "the current expression in the TFET model is an experimentally well-estabilished equation for band-to-band, Zener tunneling in planar p-n junctions" [2]. "The two-teminal Zener tunneling behavior is then generalized to three terminals by introducing physics-based expressions for the bias dependent tunneling window Vtw and a dimenionless factor f, which accounts for the superlinear current onset in the output characteristic" [15].

$$I_{dt} = afEV_{tw}e^{-b/E} \tag{4.23}$$

$$a = \frac{WT_{ch}q^3}{8\pi^2\hbar^2}\sqrt{\frac{2m_r^*}{E_g}} \qquad b = \frac{4\sqrt{2m_r^*E_g^3}}{3q\hbar} \tag{4.24}$$

The factor f is given by

$$f = \frac{1 - e^{-V_{dse}/\Gamma}}{1 + e^{\frac{V_{thds} - V_{dse}}{\Gamma}}} \tag{4.25}$$

Where Γ is the saturation shape parameter.

$$V_{dse} = V_{dsmin}[\frac{V_{ds}}{2V_{dsmin}} + \sqrt{\Delta^2 + (\frac{V_{ds}}{2V_{dsmin}})^2} - \sqrt{\Delta^2 + 1}] \tag{4.26}$$

$$V_{thds} = \Lambda tanh(V_{gs}) \tag{4.27}$$

The tunneling window is given by

$$V_{tw} = ln(1 + e^{(V_{gs} - V_{th})/U}) \tag{4.28}$$

Tunnel FETs garnered interest by its virtues of reduced SCEs, SS and low power consumption [15]. A drawback is the very low Ion current.
One of the possible solutions to enhance Ion includes structural engineering: a DG or GAA structure could be a solution of Ion with no impact on Ioff current. GAA TFETs have shown a great deal in performance improvement , compared to SG and

DG.

Tunnel FET is an emerging device in afield of continuing research. Obviously, MATLAB analysis allow to limited explorations. Thus, detailed simulations using advanced TCAD tools have to been carried out.

4.5.1 Matlab Implemantation

Same structure as before was used to validate this model, since the approximation used is the same. The same conclusions have been done for the Praveen model, since both analytical models used WKB approximation to derive the current expression of the tunnel fet. So, the model seems to lead an accurate result, but it doesn't take care of several parameter. The model can't be considered as a universal model for different structures, materials and sizes.

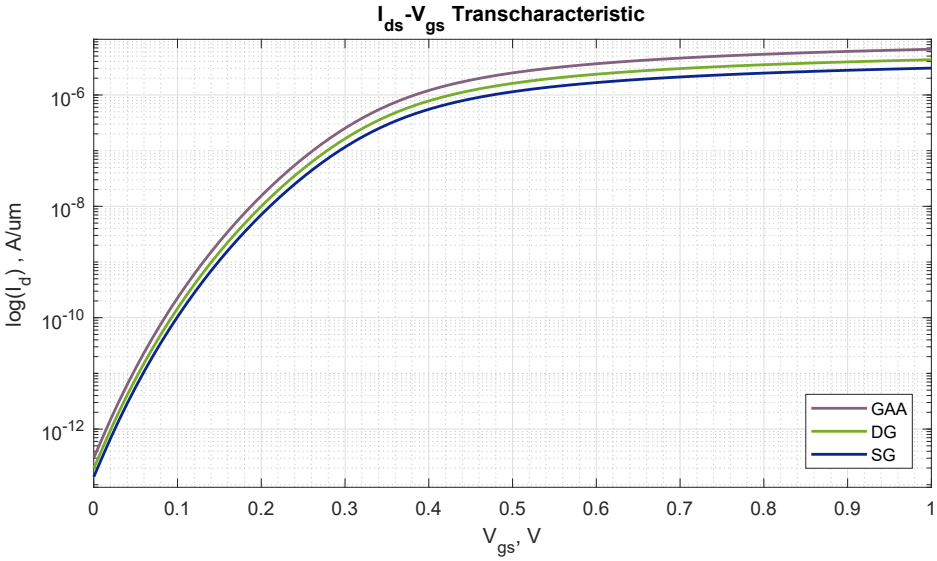

Figure 4.13: $I_D - V_{gs}$ characteristic of TFET for the model implemented

Parameter	SG	DG	GAA
I_{OFF}, A/um	1.38e-13	1.95e-13	3.01e-13
I_{ON}, A/um	3.03e-6	4.29e-6	6.62e-6

Table 4.6: Most important extracted parameters from Praveen model

4.6 Dash Model

The current is evaluated using initial and final tunneling length of band-to-band process. The tunneling process of charge carriers has been realized analytically using initial and final tunneling point. Both the tunneling points play important roles for the estimation of the DC parameters such as SS, ON current and transconductance [7].

4.6.1 Modeling

First, the potential profile in the channel is studied, in order to derive the surface potential. Here the effect of electron space charge has been neglected due to the light doping nature of intrinsic channel [7].
With this in mind, the surface potential is seen as the potential profile along the x-axis with specified boundary conditions at the gate-channel interface, and it plays a crucial role in the analysis of the tunneling path and drain current [7].

$$V_s(x) = C_O e^{\alpha x} + C_1 e^{-\alpha x} - (V_{FB} - V_{gs}) \tag{4.29}$$

where:

$$\alpha = \sqrt{\frac{\varepsilon_{ox}}{\varepsilon_{si} t_{si} t_{ox}}} \tag{4.30}$$

$$C_0 = \frac{1}{2sinh(\alpha L)}[-V_{bi}(1 + e^{-\alpha \ell}) + (V_{FB} - V_{gs})(1 - e^{-\alpha \ell}) + V_{ds}] \tag{4.31}$$

$$C_0 = -\frac{1}{2sinh(\alpha L)}[-V_{bi}(1 + e^{\alpha \ell}) + (V_{FB} - V_{gs})(1 - e^{\alpha \ell}) + V_{ds}] \tag{4.32}$$

At the same time, the eletric field along the x-axis plays an important role for the evaluation of the tunneling volume. It is derived by differentiating the surface potential, as follows:

$$E_x = -\frac{\partial \varnothing(x,y)}{\partial x} = -C_0 \alpha e_{\alpha x} + C_1 \alpha e_{-\alpha x} \tag{4.33}$$

If the applied gate voltage is zero, there is a wide potential barrier between the source and channel region there is no BTBT of charge carriers, hence the device is OFF.
When positive gate voltage is applied, the potential barrier between source and channel region gets narrower gradually until the gate voltage exceeds the threshold voltage so that the potential barrier becomes narrow enough to allow tunneling of charge carriers.
In the ON state the conduction band of channel goes below with respect to the valence band of source, so that it enables the charge carriers to tunnel from source to drain. However the charge carriers move to the drain end by the process of drift diffusion mechanism [7].

Tunneling path is defined as the distance between L1 and L2 along the channel length. It is responsible for BTBT among carriers.
In particular, L1 is defined as the initial tunneling length from the source which indicates the start of BTBT tunneling process and can be evaluated as [7]:

$$L1 = \frac{1}{\alpha} ln(\frac{Z + \sqrt{Z^2 - 4C_0C_1}}{2C_0}) \tag{4.34}$$

Where

$$Z = V_{bi} + \frac{E_g}{q} + (V_{FB} - V_{gs}) \tag{4.35}$$

While, the final tunneling length L2 indicates the end of the tunneling process and can be evaluated as the value in the channel region at which surface potential is maximum [7], so:

$$L2 = \frac{1}{\alpha} ln(\sqrt{\frac{C_1}{C_0}}) \tag{4.36}$$

The drain current in the BTBT process can be evaluated by the evaluation of band to band generation rate, which is defined as follows:

$$G_R(x,y) = A_K E_{avg} E_x e^{-B_K/E_{avg}} \tag{4.37}$$

where A_K and B_K are the Kane's tunneling-dependent parameters, while the average electric field is expressed as

$$E_{avg} = \frac{E_g}{q\ell_{path}} \tag{4.38}$$

Where ℓ_{path} is the length of tunneling path varying from L1 to L2.

So, the tunneling current can be determined by integrating the band to band generation rate over the TFET volume:

$$I_D = q \int \int G_R(x,y) dxdy \tag{4.39}$$

By sobsituiting the Generation rate expression in the integral above, it can been obtained:

$$I_D = q \int_0^{t_{si}} \int_{L1}^{L2} A_K E_{avg} E_x e^{-B_K/E_{avg}} dxdy \tag{4.40}$$

Again, sobstituting the electrical field expression, the drain current final expression can be get:

$$I_D = q \int_0^{t_{si}} \int_{L1}^{L2} A_K \frac{E_g}{qx} (-C_0 \alpha e_{\alpha x} + C_1 \alpha e_{-\alpha x}) e^{-B_K qx/E_{avg}} dxdy \tag{4.41}$$

4.6.2 Matlab Implementation

Since the explained model seems to be the most reliable analytical model to describe the Tunnel FET behaviour, also TCAD Sentaurus simulations were done to compare the results.

In particular, the same structure was used, by varying the gate engineering.

The analytical model results in agreement with physical simulations, except for the subthreshold region.

The reason is that the Tunnel FET in subthreshold region is dominated by SRH more than tunneling, but the analytical model takes into account the tunneling effect only. It results in a quite difference of off region.

It could be useful to consider an analytical model that consider separately subthreshold and above-threshold region, in order to integrated such model in the Dash Matlab model that has been implemented in this work.

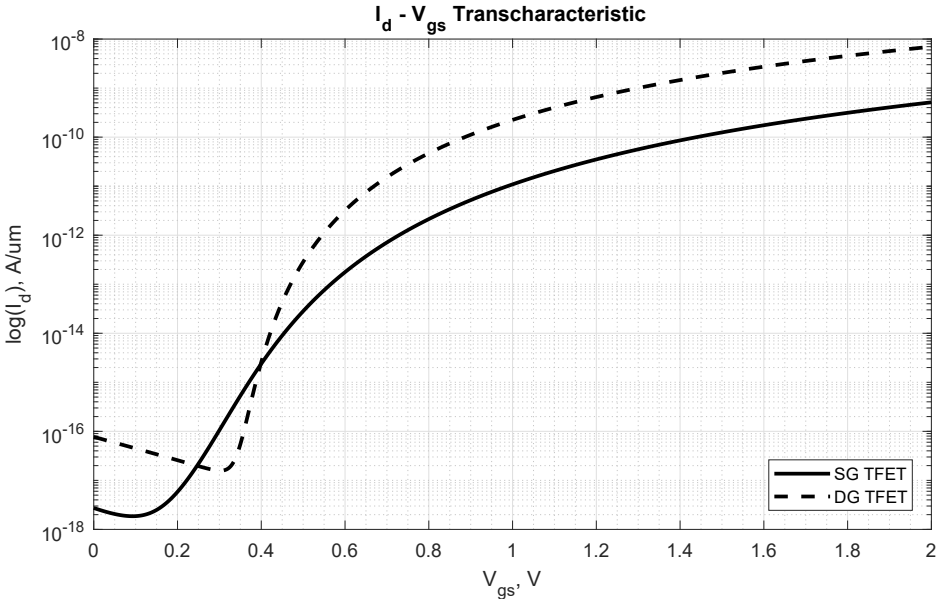

Figure 4.14: DG TFET SiO2 vs SGTFET Transcharacteristic Comparison

Parameters	SG TFET	DG TFET	GAA TFET
Ioff, nA/um	2.73e-18	7.7e-17	8.94e-18
Ion, uA/um	5.12e-10	6.98e-9	4.66e-9

Table 4.7: Important parameters extrcted from Model varying the geometric structure

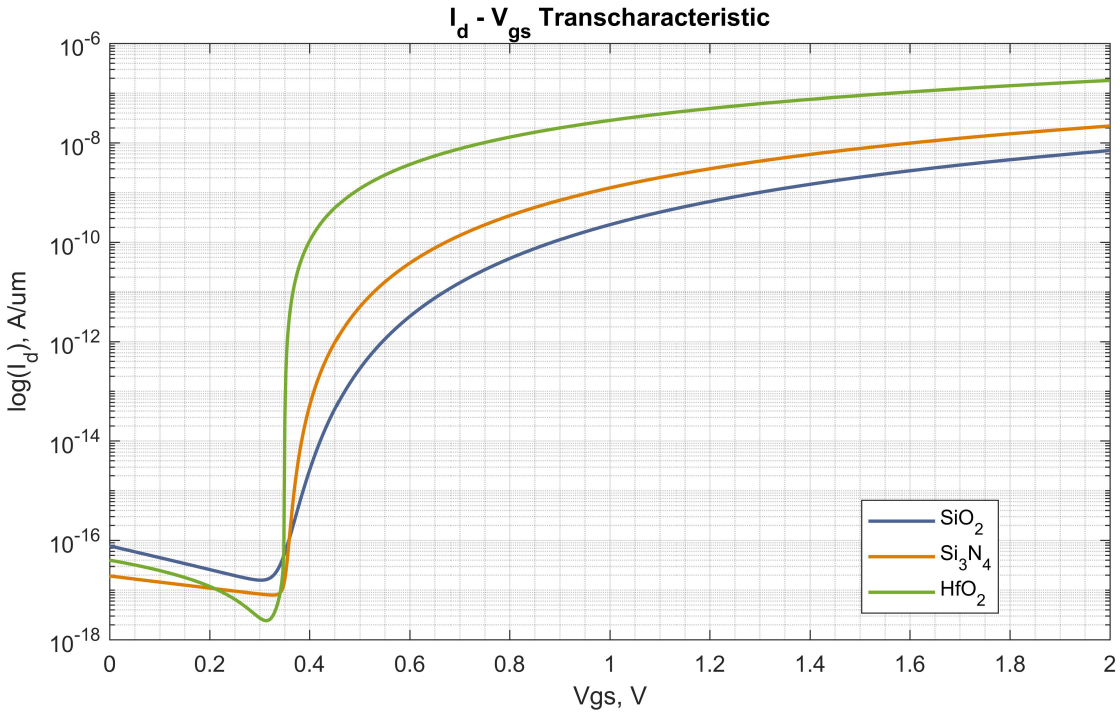

Figure 4.15: Transcharacteristic comparison among different structures

Parameters	SiO2	Si3N4	HfO2
Ioff, nA/um	7.e-17	1.91e-17	4.08e-17
Ion, uA/um	6.98e-9	2.17e-8	1.79e-7

Table 4.8: Important parameters extrcted from Model varing gate dielectric

Chapter 5

Sentaurus Simulations

Several simulations of Tunnel FETs structures had been carried out in TCAD Synopsis Sentaurus in order to check and validate the analytical models implemented in MATLAB.
A further aim of such simulations was to verify the possibility of new emerging devices like Tunnel FET to overcome the main issues of FinFET. In fact, from previous simulations of different FinFET structures, it had been emerged several problems and limits in scaling such devices below 20nm.
With this in mind, different structures of Tunel FET were investigated going in deep with scaling and analyzing new problems emerged from this kind of analysis.

This chapter is divided into several parts as follows:

- Simulation of single-gate (SG) Tunnel FET investigating on electrostatic analysis, temperature analysis and capacitance analysis

- Simulation of double-gate (DG) Tunnel FET varying the gate dielectric material

- Simulation of gate-all-around (GAA) nanowire Tunnel FETs with high-k dielectric

- Comparison of such physical simulations with analytical model implemented in the previous part in MATLAB

5.1 Single Gate Tunnel FET

Firstly, a Single Gate TFET was simulated in TCAD Synopsis Sentaurus. As can be shown in the following picture, a SG TFET is realized in CMOS'like structure. The main feature of such device is the different doping type between the source and drain terminal.

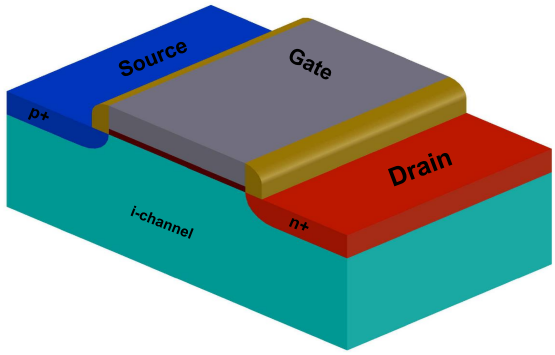

Figure 5.1: SG Tunnel FET Structure

The device parameters are: channel length Lg = 40nm, source and drain length Lsd = 20nm, oxide thickness tox = 2nm using SiO2 material, source doping concentration Ns = 1e20 cm-3, drain doping concentration Nd = 5e19 cm-3, channel doping concentration Nchannel = 1e15 cm-3, silicon layer thickness of tsi = 10nm.

Quantity Name	**Value**	**u.m. (S.I.)**
Gate Length	40	nm
Oxide Thickness (t_{ox})	2	nm
Silicon Thickness (t_{si})	10	nm
Temperature (T)	300	K
Source doping concentration (N_s)	10^{20}	cm^{-3}
Drain doping concentration (N_d)	$5 * 10^{19}$	cm^{-3}
Channel doping concentration (N_{ch})	10^{15}	cm^{-3}
Metal workfunction ϕ_m	4.1	eV

Table 5.1: Input data used for physical simulation of SG Tunnel FET [1]

A cross section of the device is shown in the figure below:

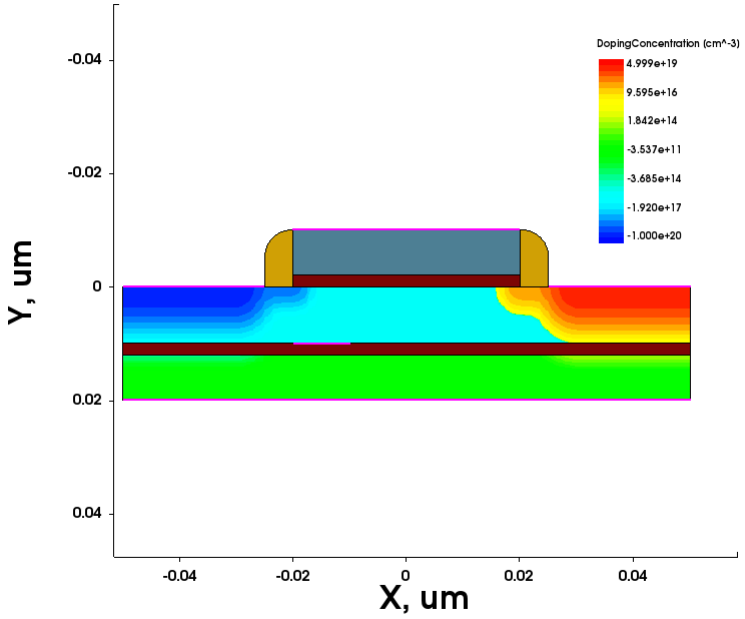

Figure 5.2: Cross section of SG Tunnel FET used for TCAD simulation

The above cross section is useful to better understand the difference in doping concentration of such devices. In fact, the source terminal is p-doped, while the drain terminal is n-doped, with an intrinsic channel. As it was explained in the previous sections, the device is normally off. Then, it is in on state when a drain bias is applied so that the concuction band of the intrinsic channel goes below the valence band of the source p region.
Band diagrams of OFF and ON state respectively from Sentaurus inspection are shown below.

The figure below shoes the variation of electric field alog the channel varying the gate voltage.

It can be observed that both in OFF and ON state, the electric field takes its maximum value along the x-axis at the source/channel interface.
In fact, thanks to the high electric field, the electron charges tunnel from source to

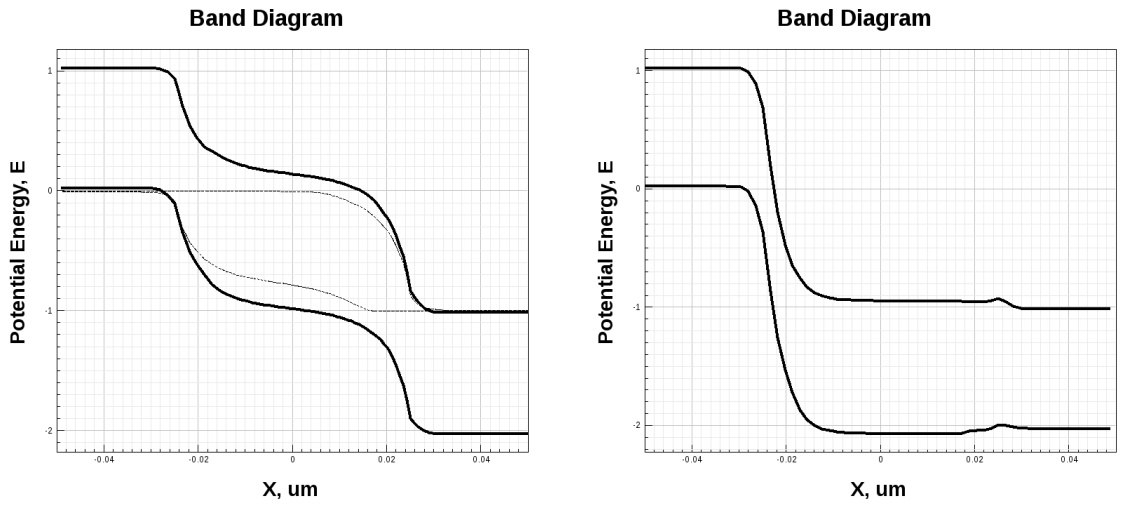

Figure 5.3: Energy band diagram of n-channel TFET in OFF-state ($V_{gs} < V_{th}$) and ON-state ($V_{gs} > V_{th}$)

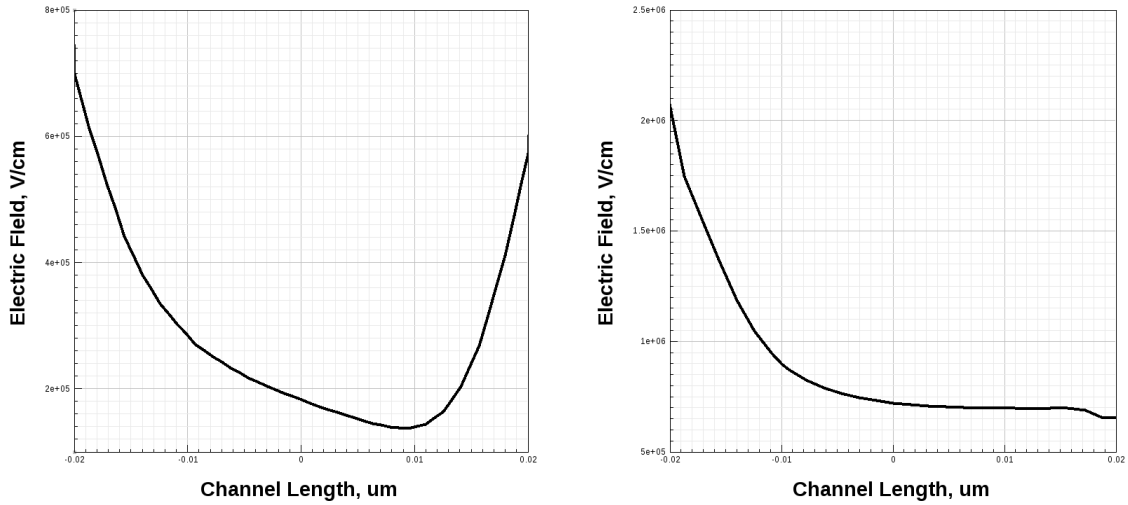

Figure 5.4: Electric Field distribution in OFF-state and ON-state

drain with an higher probability.

The transfer characteristic of a SG TFET is simulated in TCAD Synopsis Sentaurus, with Vds = 1V, and varying the gate voltage from 0V to 2 V.

For small Vgs, the current at the drain terminal lightly decreases until the named "peak valley". Then, increasing the gate voltage beyond the threshold voltage, the current increases in an exponential way with a fixed drain bias.

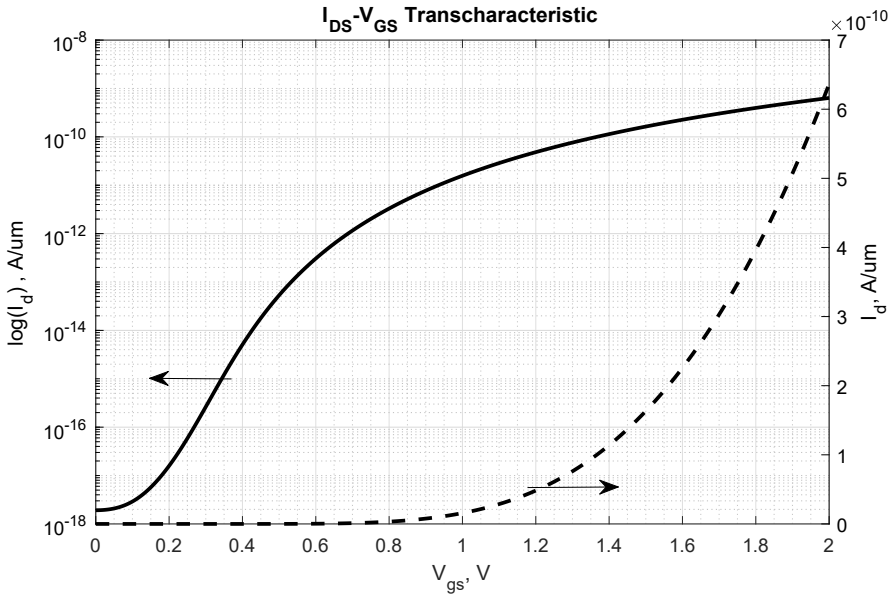

Figure 5.5: Drain current as a function of gate voltage in linear and logaritmic scale

More detailed results are shown in the following table:

Parameters	Results
I_{off},$nA/\mu m$	1.85e-9
I_{on},$\mu A/\mu m$	1.55e-3
SS,mV/dec	49.55
V_{th},V	1.46

Table 5.2: Important electrical parameters for Vds = 1V

From this first simulation, it can be observed how the leakage current in Tunnel FET is effectively lower than in MOSFET. However, the threshold voltage is quite high and as a consequence the tunneling current it doesn't go further the nA order of magnitude. This represents the main issue of such emerging device, since it can't be seen as an applicable switch.

A capacitance analysis was then exploited in TCAD Sentaurus, in order to investigate on possible differences in capacitance behaviour among FETs.

The figure below represent the gate capacitance variation varying the drain voltage.

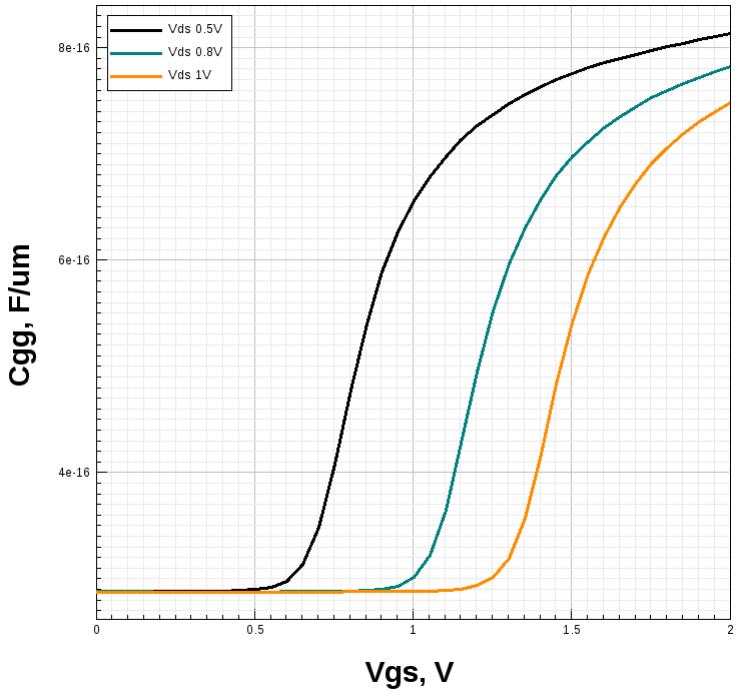

Figure 5.6: SG Tunnel FET Gate Capacitance varying drain voltage Vds

The intrinsic capacitance Cgg increases with the increase of the gate voltage in on state. The increased capacitive effect is due to the combined enhancement of both drain capacitance (Cgd) and source capacitance (Cgs) [7]. From the graph above, it can be observed that the main contribution to the intrinsic gate capacitance is given by the drain capacitance. In fact, as the drain voltage $V - ds$ increases, the gate capacitance drecreases. But, low capacitances limit the cut-off frequency of the device.

A temperature analysis of a DG TFET has been done, in order to evaluate the temperature dependence in the device.

Since TFETs are based on tunneling phenomenon, they are weakly dependent on temperature.
In particular, in the case of indirect tunneling there is a dependence on phonon-electron interactions for the change in momentum from the Γ-valley to the X-valley

minimum. The phonon occupation obeys to Bose-Einstein statistics, and the number of phonons is sensitive to temperature [30]. But, indirect tunneling can occur even with a zero phonon occupancy due to phonon emission by the tunneling particle, hence tunneling does not depend on temperature in an exponential way.

TCAD Synopsis Sentaurus was used to carry out simulations of FET devices varying the temperature.

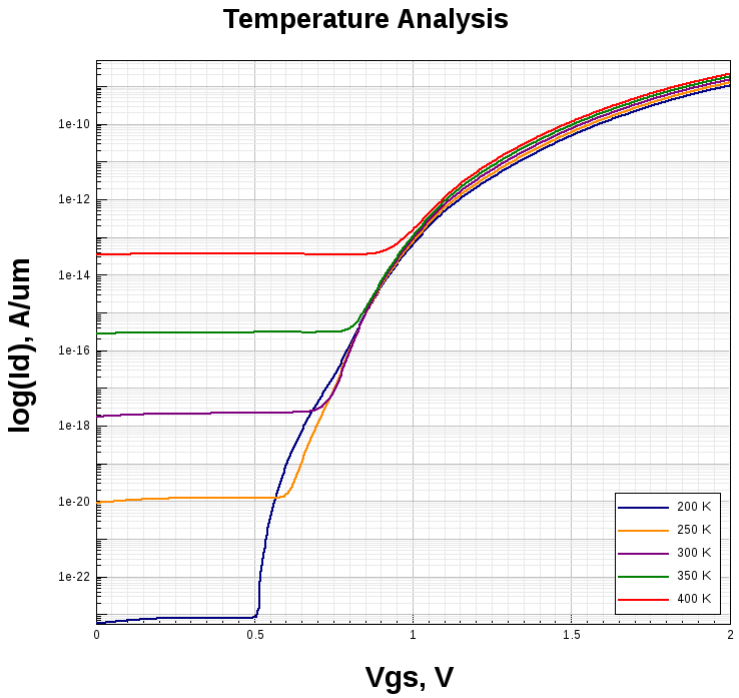

Figure 5.7: SG TFET Temperature analysis

Temperature, K	SS, mV/dec	Ioff, nA/um
200	20,71	6,15e-15
250	44,10	9,70e-12
300	49,55	1,85e-9
350	70,35	2,96e-7
400	115,04	3,71e-6

Table 5.3: Temperature variation of electrical parameters for Vds = 1V

In order to check the reliability of Matlab models, a transcharacteristic of such device was simulated in TCAD Sentaurus, with Vd = 1V and Vg = 2V. The same behaviour of a Tunnel Diode was exploited.

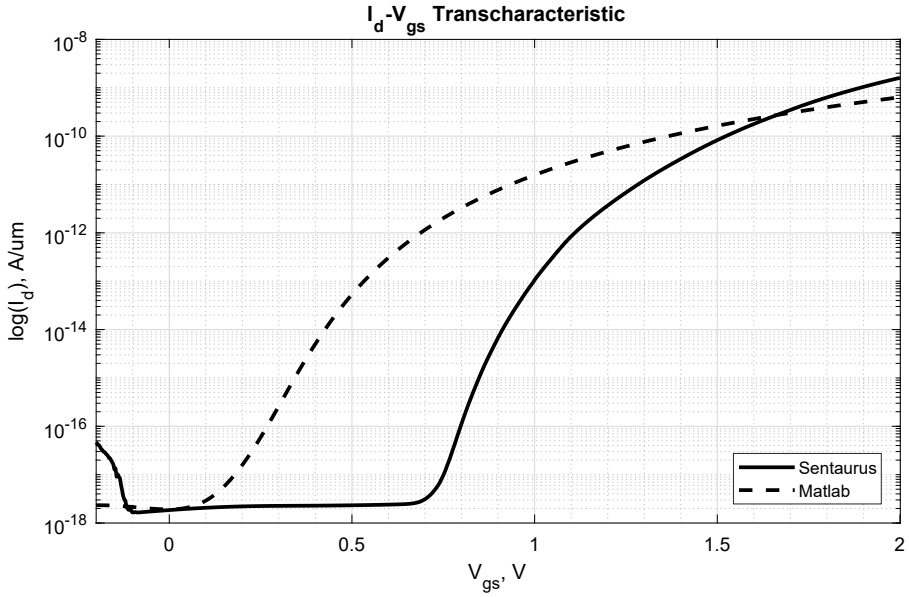

Figure 5.8: SG Tunnel FET Transcharacteristic

The model agrees with the physical simulation.It presents a difference in the subthreshold slope, even if the value of leakage current is the same. This is probably due to the accuracy of the model: such model presents an accurate analysis of the device, describing the tunneling current. The current is calculated by integrating the generation rate in the device volume. Such generation rate is evaluated as the electron probability to tunnel from the minimum tunneling distance to the maximum tunneling distance. The current is derived from this tunneling path, so the

subthreshold region where the recombination is the major contribute to the current is omitted. This can be explain this disagreement in the curve slope.

The Ion/Ioff ratio has been raised of about 4 order of magnitude with respect to the MOSFET case. The subthreshold swing goes below the conventional 60mV/dec due to the working principle which TFET is based on.

However, the main issue of a Tunnel FET realized in Silicon material is the low ON current.

5.2 Double Gate Tunnel FET

The study of Tunnel FET was exploited by simulating a double gate structure. The device parameters are the same of the Single Gate structure, with the only difference of doubling the gate.

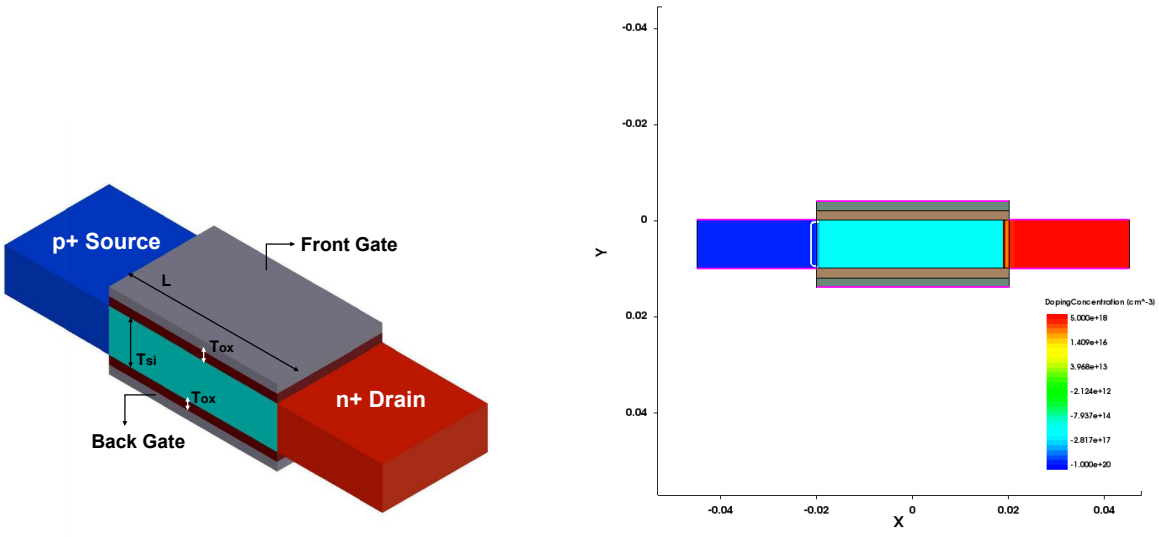

Figure 5.9: DG Tunnel FET structure and cross section in Sentaurus

The device parameters are:

Quantity Name	**Value**	**u.m. (S.I.)**
Gate Length	40	nm
Oxide Thickness (t_{ox})	2	nm
Silicon Thickness (t_{si})	10	nm
Temperature (T)	300	K
Source doping concentration (N_s)	10^{20}	cm^{-3}
Drain doping concentration (N_d)	$5 * 10^{19}$	cm^{-3}
Channel doping concentration (N_{ch})	10^{15}	cm^{-3}
Metal workfunction ϕ_m	4.1	eV

Table 5.4: Input data used for physical simulation of DG Tunnel FET [1]

The same analysis as before has been carried out for a double gate structure. So,

several comparison were done in order to investigate the behaviour of the Tunnel FET varying the gate engineering and the gate dielectric materials.

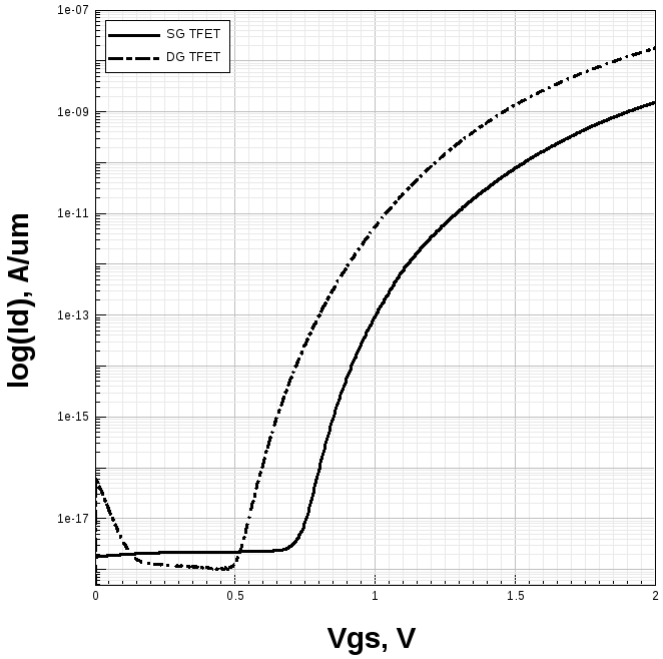

Figure 5.10: Comparison of electrostatic analysis between a SG and a DG TFET

From figure(5.10) the difference in the I-V characteristic can be noticed between a single-gate and double-gate structure. The table below recaps the improvement in current and subthreshold slope by varying the gate engineering.

Parameters	SG TFET	DG TFET
Ioff, A/um	1.82e-18	5.58e-17
Ion, A/um	1.55e-9	1.84e-8
SS, mV/dec	76.11	69.6
Vth, V	1.34	1.33
Gm, S/um	6.35e-9	6.88e-8

Table 5.5: SG vs DG TFET Extracted parameters from TCAD

For such comparison, a SiO2 gate dielectric material is used, but also the same gate metal material and structure parameters. From the results above, it can be observed that gate coupling leads to an increase of drain current of one order of

magnitude. Also the off current increases with respect to the case of a SG TFET, but it still remains a very low leakage current.

The results in TCAD were compared with MALTAB simulations, using the same model as for SG TFET. Since the model is the same, the same accuracy can be noticed, bu also the same problem of accuracy in the subthreshold region.

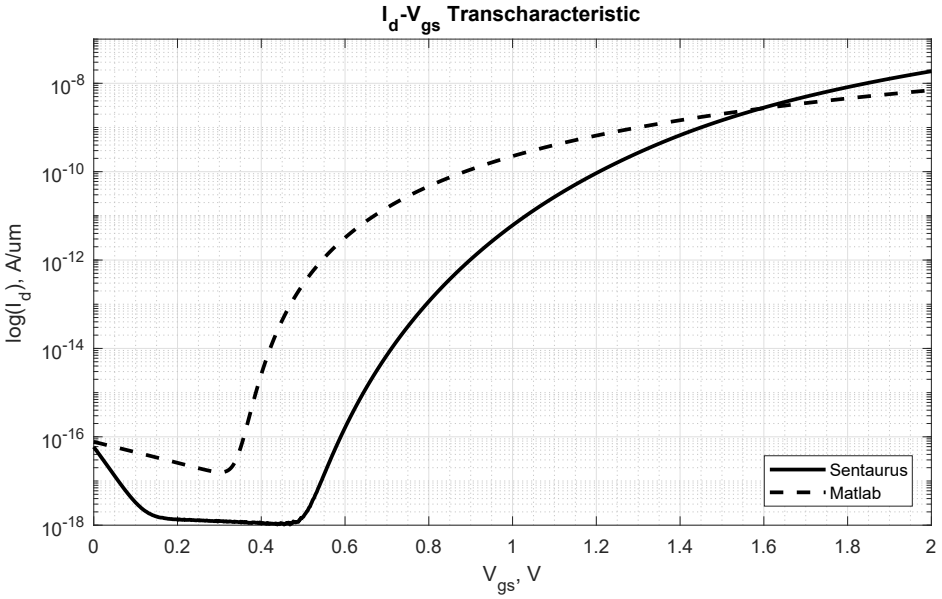

Figure 5.11: Validation of MATLAB model with physical simulation

A Double-gate structure presents several advantages with respect to a single-gate structure. However, the tunneling current still remains too low for every possible applications. Several solutions can be studied in order to overcome such limit. One among them could be change the gate dielectric material, since the tunneling probability depends from this factor in an exponential way.

With this in mind, an anlysis in both MATLAB and TCAD were carried out, where the gate dielectric were varied. In the figures below, the characteristic of a DG TFET with respectively Si3N4 and Hfo2 is represented.

It can be observed that the difference in the behaviour between the model and the physiscal simulation get less evident with increasing the permittivity of the dielectric. Furthermore, the evident dependency of current on gate dielectricis shown below.

From figure (5.13) it can be seen the increase of on current with increasing of permittivity, but also a steeper slope of the characteristic.

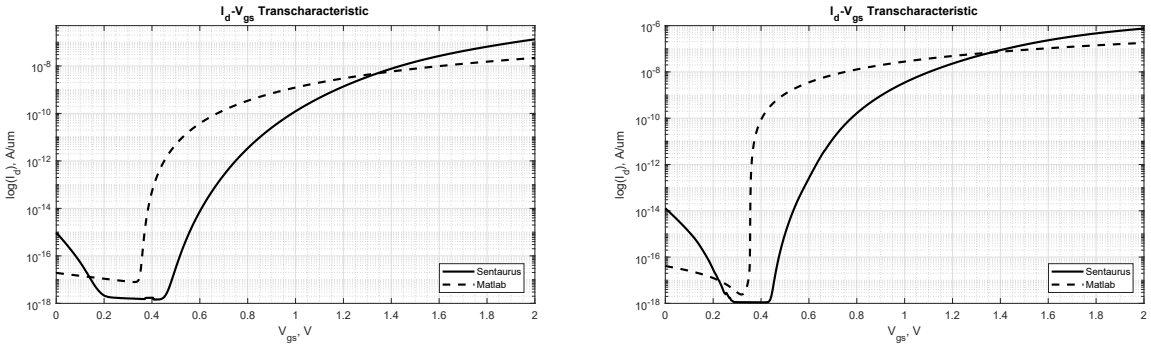

Figure 5.12: DG Tunnel FET varying gate dielectric, (a) Si3n4 and (b) HfO2

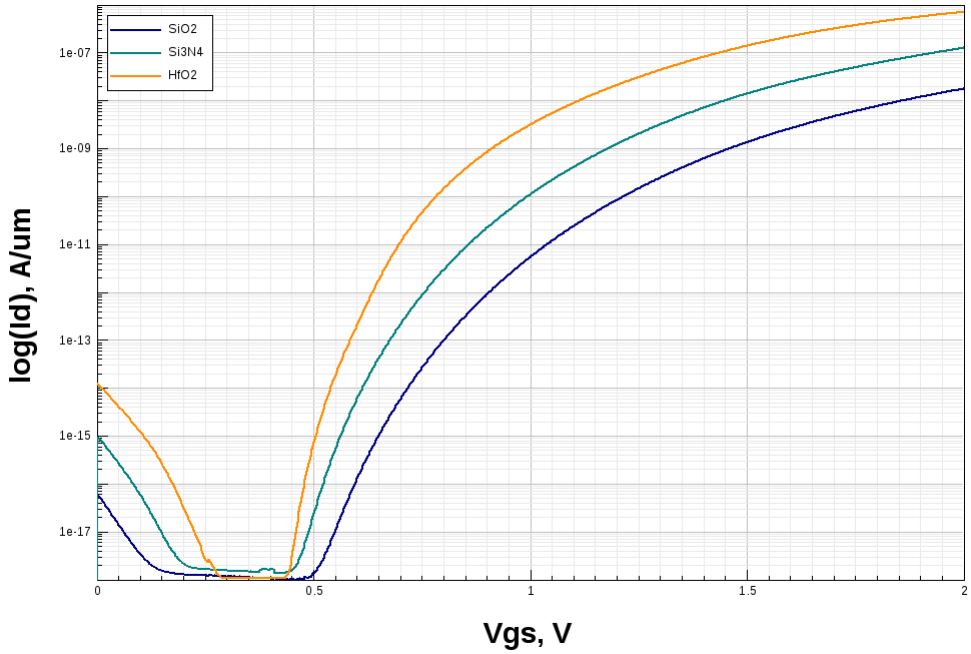

Figure 5.13: DG Tunnel FET Gate Dielectric Comparison with physical simulation

The most evident results stays in 38% in SS reduction, a 3 order of magnitude in increase of Ion current and in a not so evident Vth threshold voltage variation.

The above table shows the results of the comparative study of the current dependency on gate dielectric variation. It can be seen that the most relevant variation in device parameters is the growing of on current of about 3 order off magnitude, and the reduction of the SS of about 38%.

Parameters	SiO2	Si3N4	HfO2
Ioff, A/um	5.48e-17	9.03e-16	1.16e-14
Ion, A/um	1.84e-8	1.3e-7	7.36e-7
SS, mV/dec	69.6	52.2	36.72
Vth, V	1.33	1.37	1.36
Gm, S/um	6.88e-8	4.26e-7	1.5e-6

Table 5.6: Gate dielectric variation

A temperature analysis of a DG TFET has been done, with an high k dielectric, in order to evaluate the temperature dependence in the device.

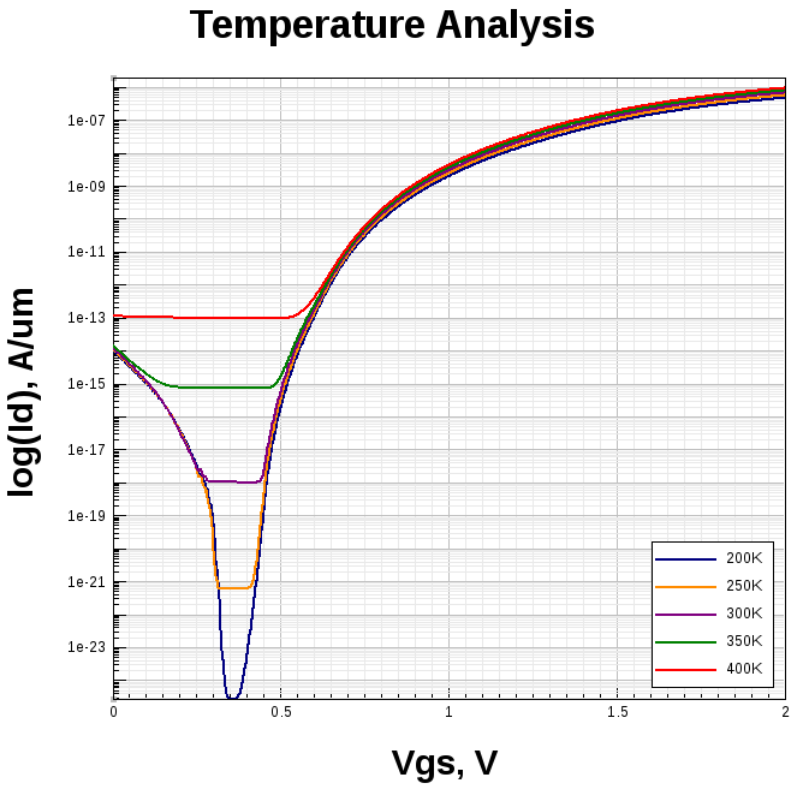

Figure 5.14: DG TFET Temperature analysis

Temperature, K	SS,mV/dec	Ioff, nA/um
200	36.15	8,9e-15
250	33.61	9,89e-15
300	34,72	1,09e-14
350	51,01	1,29e-14
400	47,75	1,25e-13

Table 5.7: Temperature variation of electrical parameters for Vds = 1V

From the results above, it can be noticed that the variation in off current is less evident than in sg tfet case, even if the recombination remains the major contribution in that region. As before, the on current doesn't vary with the temperature as in the case of a conventional MOSFET. Except for the valley of negative conductance, the current characteristic seems to be not influenced from the temperature variation.

5.3 Gate All Around Tunnel FET

A cylindrical structure for Tunnel FET was realized in TCAD Sentaurus, based on the same parameters as for the case of single gate and double gate structure.

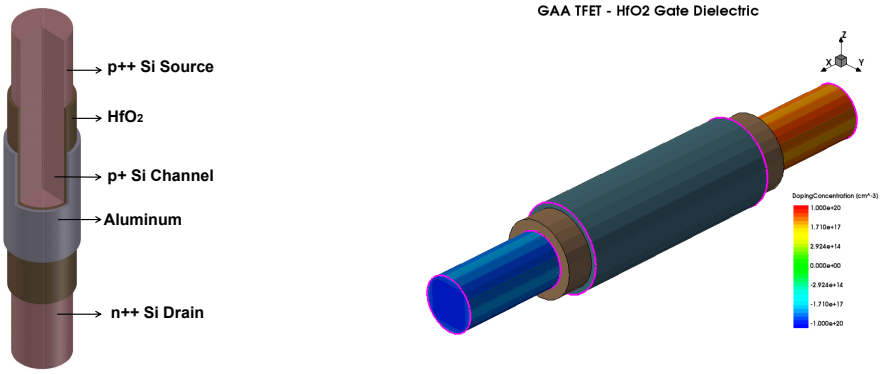

Figure 5.15: GAA Tunnel FET Sentaurus Structure with HfO2 gate dielectric and doping concentration

Quantity Name	**Value**	**u.m. (S.I.)**
Gate Length	40	nm
Oxide Thickness (t_{ox})	2	nm
Silicon Thickness (t_{si})	10	nm
Temperature (T)	300	K
Source doping concentration (N_s)	10^{20}	cm^{-3}
Drain doping concentration (N_d)	$5 * 10^{19}$	cm^{-3}
Channel doping concentration (N_{ch})	10^{15}	cm^{-3}
Metal workfunction ϕ_m	4.1	eV

Table 5.8: Input data used for physical simulation of DG Tunnel FET [1]

The same analysis as before was carried out. In particular, the structure of a gate-all-around was simulated, varying the dielectric from SiO2 to HfO2. In this way, it was further demonstrate the improvement in tunneling current and subthreshold slope if a high k dielectric is used.

In fact, as can be noticed, the current again increase by an order of magnitude, and a steeper slope characteristic can be appreciated. However, an issue of such

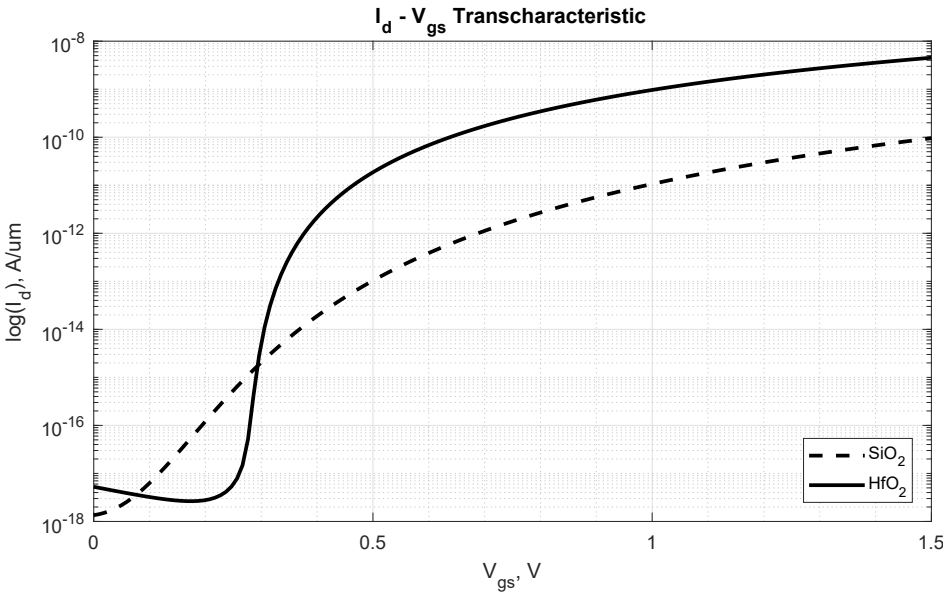

Figure 5.16: GAA Tunnel FET characteristic varying gate dielectric

Parameters	SiO2	HfO2
Ion, A/um	3.19e-10	1.77e-9
Ioff, A/um	4.48e-21	1.26e-18
Vth, V	1.11	1
SS, mV/dec	51.9	30,61

Table 5.9: Extracted parameters from physical simulation of GAA TFET

device is the on current that is even lower with respect t the double gate structure.

Even if a gate wrapping the channel could better control it, for a tunnel FET it seems to have no effect on the tunneling current.

5.3.1 NW TFET

The analysis can be further carried out, by further scaling the device. SO, a nanowire tunnel fet was simulated in TCAD Sentaurus, to investigate on deep scaling of such emerging devices.

The device parameters are:

Quantity Name	**Value**	**u.m. (S.I.)**
Gate Length	40	nm
Oxide Thickness (t_{ox})	2	nm
Silicon Thickness (t_{si})	10	nm
Temperature (T)	300	K
Source doping concentration (N_s)	10^{20}	cm^{-3}
Drain doping concentration (N_d)	$5 * 10^{19}$	cm^{-3}
Channel doping concentration (N_{ch})	10^{15}	cm^{-3}
Metal workfunction ϕ_m	4.1	eV

Table 5.10: Input data used for physical simulation of DG Tunnel FET [1]

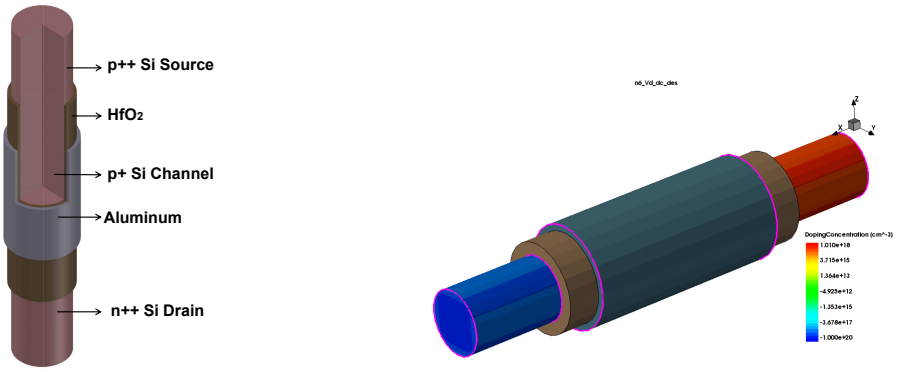

Figure 5.17: GAA Tunnel FET Sentaurus Structure with HfO2 gate dielectric and doping concentration

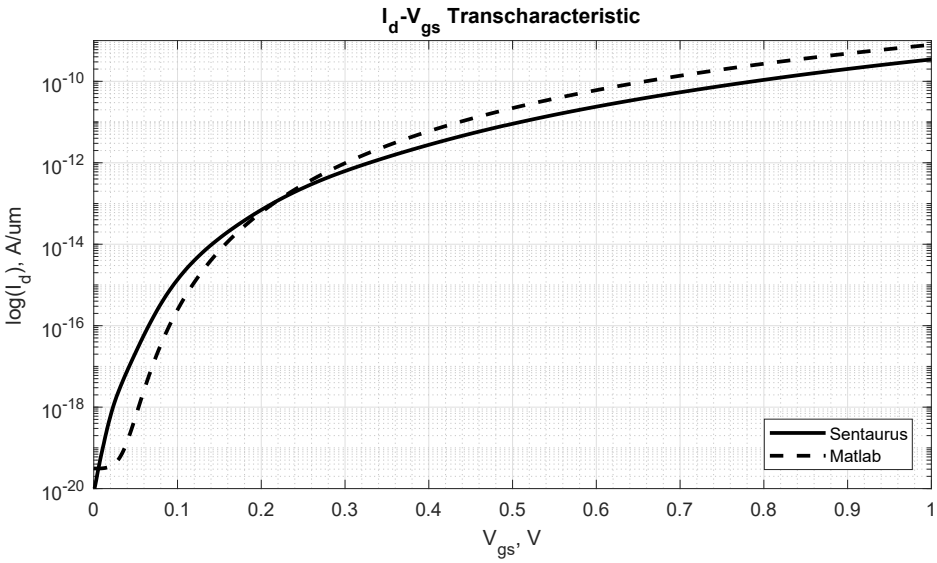

Figure 5.18: NW TFET IV characteristic for validation of Matlab model

Parameters	Results with HfO2, Vds = 1V
Ion, A/um	3.39e-10
Ioff, A/um	1.26e-20
Vth, V	0.8
SS, mV/dec	35.54

Table 5.11: NW TFET extracted parameters from physical simulation

The case of a nanowire tfet represents the best result for the validity of the analytical model. As shown in the figure above, the model is in agreement with the TCAD simulation.

However, even if a deep scaling has been carried out, the poor tunneling current remains the main issue in this device. Probably, it can be improved by study the trend of variation of the diameter in a proportional way to the channel length. The Ion over Ioff ratio is optimum since it reaches about 10^10, but the low current didn't allow the device to be applicable in a circuit.

What is strange is the fact that a double gate structure presents a better behaviour rather than a gate all around structure. Probably the nanowire tfet is not the way to further improve the current.

5.4 GAA FET vs GAA TFET

The cylindrical structure allows to compare FET and TFET electrostatic behaviour.

A simulation study was carried out in order to evaluate the advantages of a device with respect to the other one. The structure is the same as before, the only difference stays in the doping types between the tunnel fet and the fet. So, a high k dielectric is used for the gate, the channel length is of 40nm and the diameter of 10nm, with a temperature of 300K.

Figure 5.19: GAA Tunnel TFET and GAA FET

Quantity Name	**Value**	**u.m. (S.I.)**
Gate Length	40	nm
Oxide Thickness (t_{ox})	2	nm
Silicon Thickness (t_{si})	10	nm
Temperature (T)	300	K
Source doping concentration (N_s)	10^{20}	cm^{-3}
Drain doping concentration (N_d)	$5 * 10^{19}$	cm^{-3}
Channel doping concentration (N_{ch})	10^{15}	cm^{-3}
Metal workfunction ϕ_m	4.1	eV

Table 5.12: Input data used for physical simulation of DG Tunnel FET [1]

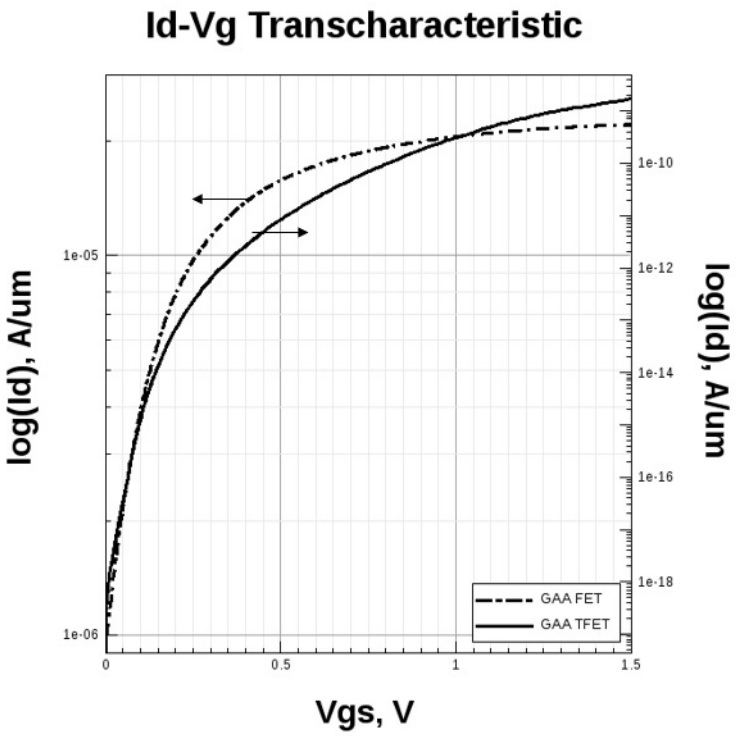

Figure 5.20: Comparison of electrostatic analysis between cylindrical structures of FET and TFET

Parameters	GAA FET	GAA TFET
Ion, A/um	2.22e-5	1.72e-9
Ioff, A/um	1.32e-6	2.92e-18
Gm, S/um	4.11e-5	3.58e-9
SS, mV/dec	98.38	56.91

Table 5.13: Comparison between GAA TFET and GAA FET

The table above shows in evidence the main issues of both devices. In particular, TFET has a far better Ion over Ioff ratio, since it is of the order of 10^9 compared to 10 of the conventional FET. This results in a steeper slope, in fact the TFET leads to go below the FET thermal limit of 60mV/dec. However, the TFET shows a low current in tunneling compared to a FET, and this is an important limit which has to be overcame.

Chapter 6

Tunnel FET issues and solutions

Tunnel Field Effect Transistors show several advantages with respect to FinFETs and could be presented as promising device which is able to overcome main conventional MOSFET issues.
In fact, from previous studies it was noticed a better Ion over Ioff and a steeper slope in the Id Vg characteristic.
Also a different behaviour on temperature variations was investigated. With this in mind, TFETs could be the best candidate for low power applications.
On the other hand, what is evident from the simulations in the prevoius chapters is that TFET on current is too low (order of nA) to be considered for any technological applications, even if the low Ioff is good for low power dissipation.
Low Ion current is due to carrier tunneling between energy states of different simmetry, which causes a large tunneling resistance [37].

Several issues have been emerged from the analysis of Tunnel FET in chapter 5. The most evident and relevant is the low value of currnt in tunneling region. In fact, such limit doesn't let the device to be applicable as a switch and exploit the advantage of low leakage current and steeper slope.

Several solutions have to be studied in order to overcome such limit. It could be useful to investigate on the expression of tunneling current. In this way, indeed, the main contributions to tunnel could emerge and could be improved. According to the triangular Wentzel-Kramer-Brillouin (WKB) approximation:

$$T_{WKB} \approx exp(-\frac{4\lambda\sqrt{2m^* sqrt E_g^3}}{3q\hbar(E_g + \Delta\phi)}) \tag{6.1}$$

where m^* is the effective mass, E_g i the band gap, λ is the screening tunneling length, and $\Delta\phi$ is the potential difference between the source valence band and the

channel conduction bands.
In particular the screening tunneling length varies with the device geometry.

From the formula above, it can be easily noticed that in order to increase tunneling probability, the effective mass, the band gap and the screening lenght should be reduced.

With this in mind, reserarches have been investigated on several solution to improve current in the on state. In this section, simulation in TCAD Sentaurus have been carried out in particular for heterostructure TFET and STBFET.

6.1 Si/Ge Hetero-structure Tunnel Field Effect Transistor

A heterostructure is a junction between two different semiconductor material [38]. The most evident feature of semiconductor materials are band gap, effective mass and electron affinity, so that the interface properties of such junction could change if two different material are used. In particular, the study of energy band diagrams related to the change in physical properties is of great interest. In heterostructure such as Si/Ge, the electron affinity model is used to relate the electron affinities and band gap for the energy band diagram study, such that:

$$\Delta E_C = \chi_1 - \chi_2 \qquad \Delta E_V = (E_{g,1} + \chi_1) - (E_{g,2} + \chi_2) \tag{6.2}$$

where χ is the electron affinity and E_g is the band gap energy of the materia, and 1 and 2 reder to different semiconductor material.

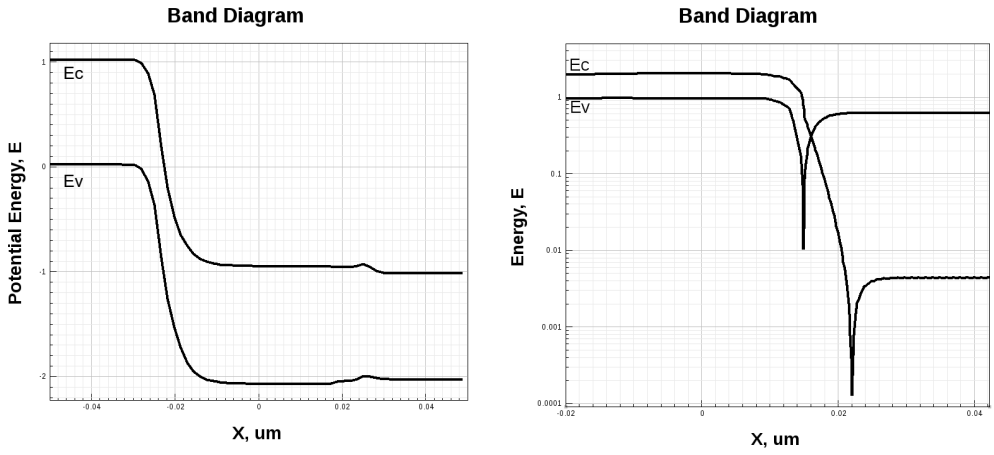

Figure 6.1: Band Diagram of a conventional TFET (left) and a Si/Ge heterostructure (right) in ON-state

Hetero-structure TFETs are realized by the use of lower band gap materials for source region, which enhance drive current behaviour.
In fact, if a material with a lower band gap and effective mass with respect to Silicon

is used in the source region, the tunneling probability will increase, according to (6.1). So materials like Germanium should replace Silicon in the source region so that the tunneling barrier widht can be reduced.
Indeed Germanium has band gap of 0.66 eV compared to 1.12eV of Silicon, and effective mass of 0.06 compared to 0.02 of silicon. On the other hand, a reducing the screening length means increase the modulation of the channel bands by the gate, and thus smaller barrier for tunneling [35]. Since the screening length depend on device geometry, it is found to be the smallest in the case of a gate-all-around structure.

6.1.1 Physical simulation of Si/Ge heterostructure TFET

A hetero-structure Si/Ge nanowire TFET have been realized and simulated in TCAD Synopsis Sentaurus. 3D Physical simulations have been carried out to validate the theorical study, so that an imporvement in on current should be observed.

Quantity Name	**Value**	**u.m. (S.I.)**
Gate Length	30	nm
Oxide Thickness (t_{ox})	1.5	nm
Silicon Thickness (t_{si})	8	nm
Temperature (T)	300	K
Source doping concentration (N_s)	10^{19}	cm^{-3}
Drain doping concentration (N_d)	10^{18}	cm^{-3}
Channel doping concentration (N_{ch})	10^{15}	cm^{-3}
Metal workfunction ϕ_m	4.1	eV

Table 6.1: Input data used for physical simulation of heterostructure Tunnel FET [1]

The heterostructure NW TFET is realized with a gate-to-source overlap of 5nm, an HfO2 gate dielectric of 1.5nm, the diameter of 8nm. A p++ Germanium material was used for source region, with acceptor active concentration of Na = 1e19. Silicon was used for both channel and drain region. The channel was p+ doped with Na 1e18, while drain was n-doped region with donor concentration of 1e19. As for [35], "A dynamic nonlocal band-to-band (BTB) tunneling model is utilized in

conjunction with Shockley-Reed-Hall (SRH) recombination, drift-diffusion physics, and Fermi statistics" [35].

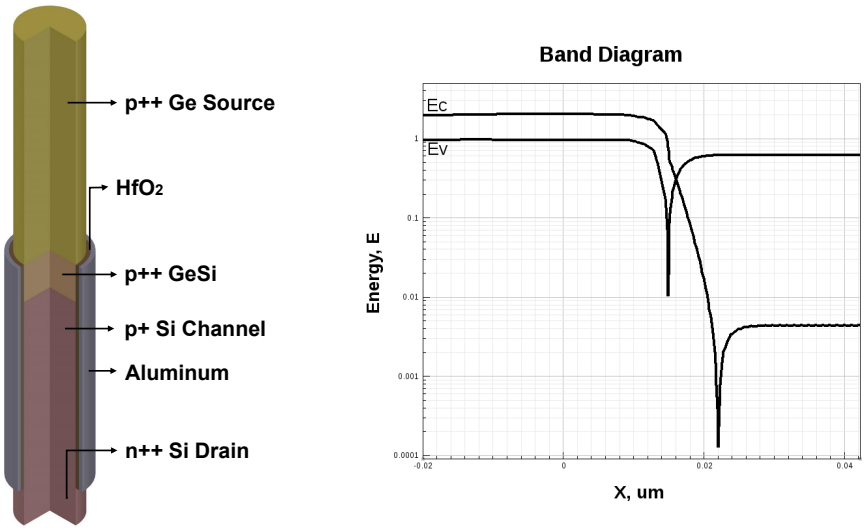

Figure 6.2: Hetero-structure

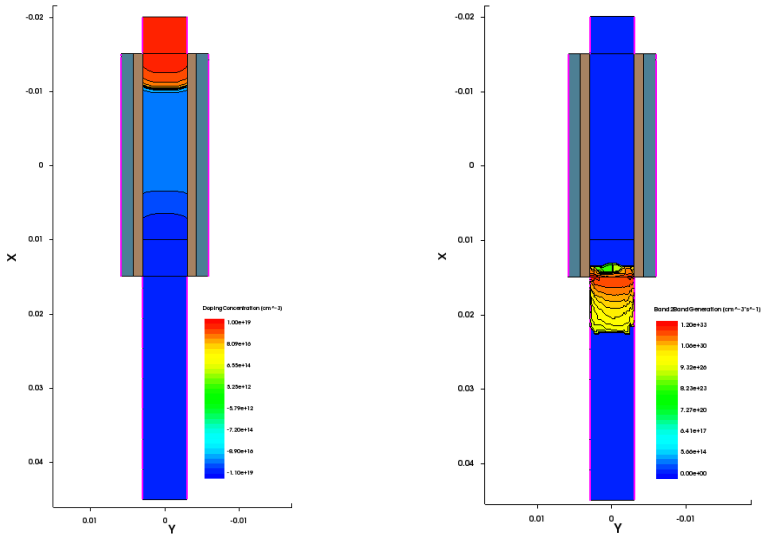

Figure 6.3: Hetero-structure

The figure below represents the simulated heterostructure at Vd = 1V, while the table recaps the electrical parameters extracted from the simulation.

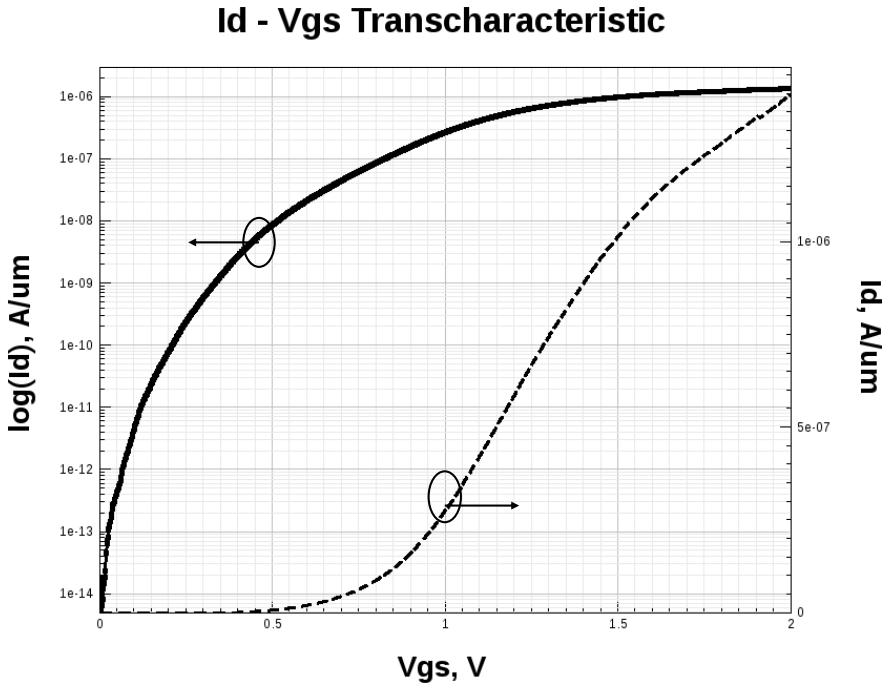

Figure 6.4: Transcharacteristic of a Si/Ge heterostruture with Vds = 1V

It can be observed that the current in on state improves of 3 order o magnitude with respect to homojunction nanowire tfet, while mantaining a steep slope and a low leakage current. This is a great result for the consideration of TFET as applicable device, and could be a starting point for an enanched tfet.

Parameters	Values
Ioff, A/um	1.27e-14
Ion, A/um	1.39e-6
Vth, V	0.86
SS, mV/dec	46.05

Table 6.2: Extracted parameters from physical simulation of Si/Ge heterostructure

6.2 Sandwich Tunnel Barrier FET

Many other considerations must be done and other solutions have to be taken into account.
Different materials which present lower bandgap, such as SiGe or InAs, or the use of high-k dielectric and vertical TFET were studied in the prevous section, in order to enhance on current performances.
In fact, both tunneling area and tunneling probability influence the current in on state. So, the conventional planar TFET even if it is an heterostructure device, can not provide an high drain current because of a small tunneling area [37].

A Sandwich tunnel barrier FET structure is realized by creating a source region p-doped which is sandwiched in between two drain regions, and which is under the gate and channel region [37].
This allows to enhance Ion current performances mantaining a low Ioff current, that result in an highr Ion over Ioff ration with respect to MOSFET or planar TFETs.
This is mainly due to the difference in gate dependency: in particular, tunneling current reduces with gate area instead of reducing with gate width.
While, the off current is dependent on the spacers thickness.

6.2.1 Physical simulation of STBFET

The STBFET structure is simulated by the use of TCAD Synopsis Sentaurus, in order to investigate this modified TFET behaviour.
The channel region is an epitaxially grown Si layer which is 2nm thick. The source region is under the gate and channel region [36] and is p-doped with Boron doping of 2e20 cm-3. The drain regions are on both sides of the high-k spacers and they are n-doped with Phosphorus doping of 5e19 cm-3. The gate is realized with Aluminum, with workfunction of 4.1eV, while HfO2 material is used for the gate dielectric. The spacers are realized using high-k HfO2 material, in order to reduce the channel resistance.
The channel length is of 30nm, while the gate dielectric is 0.4nm thick.
A simulation was carried out, with Vds at 1V.

Device parameters are riassumed in the table below:

Quantity Name	**Value**	**u.m. (S.I.)**
Gate Length	30	nm
Oxide Thickness (t_{ox})	0.04	nm
Silicon Thickness (t_{si})	2	nm
Temperature (T)	300	K
Source doping concentration (N_s)	$2 * 10^{20}$	cm^{-3}
Drain doping concentration (N_d)	$5 * 10^{19}$	cm^{-3}
Channel doping concentration (N_{ch})	10^{15}	cm^{-3}
Metal workfunction ϕ_m	4.1	eV

Table 6.3: Input data used for physical simulation of DG Tunnel FET [1]

When the device is off, there is no channel inversion under the gate and spacer region [36]. With the increas of gate bias, an inversion layer forms in the channel region, so that the device can be seen as a p+ n+ reverse biased diode with a tunnel distance equivalent to the epilayer thickness [36]. An higher tunneling current is obtained as a consequence of the eduction in tunnel distance and the use of high-k spacers.

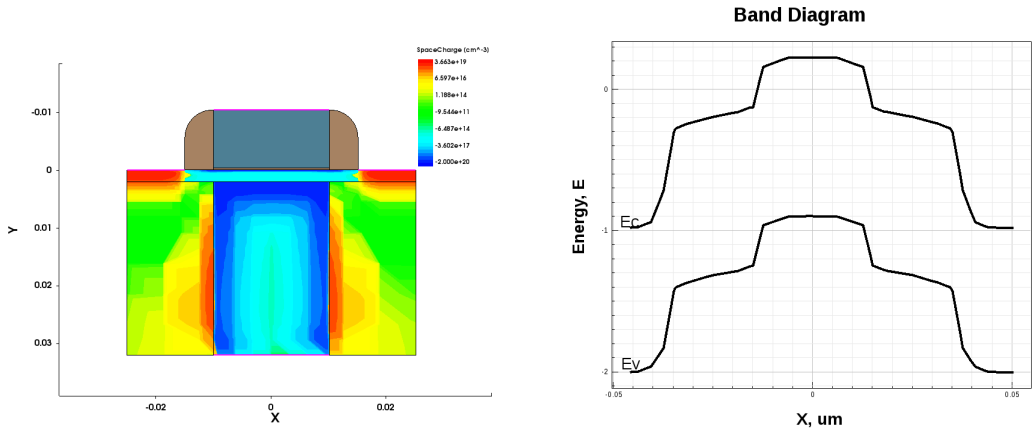

Figure 6.5: STBFET Structure

In STBFET, the band diagram behaviour looks different with respect to TFET. In fact, the band bending at the tunnel junction is negligibly small [36]. With the

increase of Vds, a large band bending in the soacer-chanel region can be seen, with negligible drop across source-channel region [36].
The voltage dropp across the tunnel junction does not vary with the drain bias, there is negligible modulation of the tunnel distance [36].

The transcharacteristic of a n-channel STBFET is shown in the figure below.

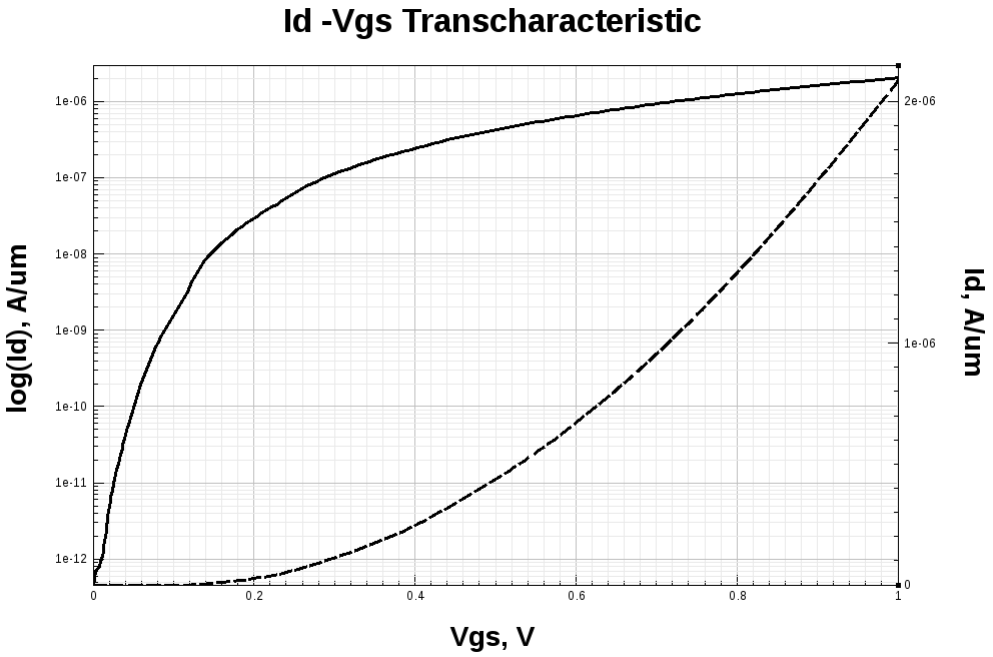

Figure 6.6: Transcharacteristic of a STBFET

The simulated Ion is of the order of uA / um when compared with nA/um in a conventional silicon TFET. The off current is quite higher with respect to conventional TFET, which allows an higher SS.

Parameters	Values
Ioff, A/um	7.22e-13
Ion, A/um	2.48e-6
Vth, V	0.3
SS, mV/dec	28.43

Table 6.4: Extracted parameters from the physical simulation of STBFET

Chapter 7

Conclusions

The work of thesis was divided in two main parts. After a brief introduction on FinFET working principle, the main structures and their issues, the firs part was dedicated to the modelling of Double Gate and Triple Gate FinFETs.
It had been implemented several models in order to study the scaling behaviour of such Multiple-Gate Transistors. Validation of the model through simulation proves the accuracy and the computational effciency of the resulting model [31].

The second part of the thesis is devoted to investigate on new emerging devices as alternative to conventional FETs and that can overcome their main issues, as TFETs.
Again, after a study of the working principle of TFET, a modelling of different Tunnel FET structures and relative simulations were done to validate the reliability of the analytical models.
The characterization of such devices includes IV behaviour, a capacitance analysis, a temperature analysis of DG,TG,GAA FinFET, and SG,DG,GAA TFETs. In particulare a comparative study of GAA FinFET and TFET behaviour was done in order to underline the promising benefits of Tunnel FET.

The description of the obtained results occupies the last part of the work together with the discussion of the main theoretical insight gained with the conducted study [31].

7.1 Future Work

Future work behind the presented thesis could focus on analytical modelling of TFET in subthreshold region, going in deep with scaling of nanowire structures, for example by the use of NEGF .
Then, a stability analysis can be performed to compare the two emerging devices analyzed, so that a simulation at circuit level can be done.
In fact, it can be interesting to investigate on the TFET behaviour in a NAND gate or in an analog differential amplifier circuit.
Finally, other emerging structures such as heterostructures, strained-Ge can be studied and analyzed, in order to overcome Tunnel FET main issues.

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