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Design of a 240-GHz Low Noise Amplifier in 130-nm SiGe BiCMOS technology

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Chapter 1

Introduction

Radar sensing has become an essential technology in numerous applications, including automotive safety, industrial automation, robotics, and high-resolution imaging [1], [2]. Compared with optical sensors such as cameras and LiDAR, radar systems are inherently robust to adverse weather and lighting conditions, enabling reliable operation in rain, fog, dust, and darkness [3]. Recent advances in integrated-circuit technology have further accelerated the adoption of radar by enabling compact, low-cost, and highly integrated transceivers suitable for mass-market applications.

Frequency-Modulated Continuous-Wave (FMCW) radar has become one of the most widely adopted radar architectures because it can simultaneously estimate target range and radial velocity while operating continuously at relatively low transmit power. Figure 1.1 shows a block diagram of the main components of an FMCW radar system. The transmitted waveform is a continuous signal whose frequency varies linearly with time, commonly referred to as a *chirp*. The generated signal is amplified by a Power Amplifier (PA), and transmitted by the transmitter (TX) antenna. The signal reflected by the target is received by the receiver (RX) antenna, amplified by the Low Noise Amplifier (LNA), and mixed with a replica of the transmitted signal. This process produces a beat signal whose frequency contains information about the target's range and radial velocity. The beat signal then passes through a Low Pass filter (LPF) and an Analog to Digital Converter (ADC) before being processed [4]. The achievable range resolution depends primarily on the modulation bandwidth, making wideband operation particularly attractive for high-resolution sensing [3].

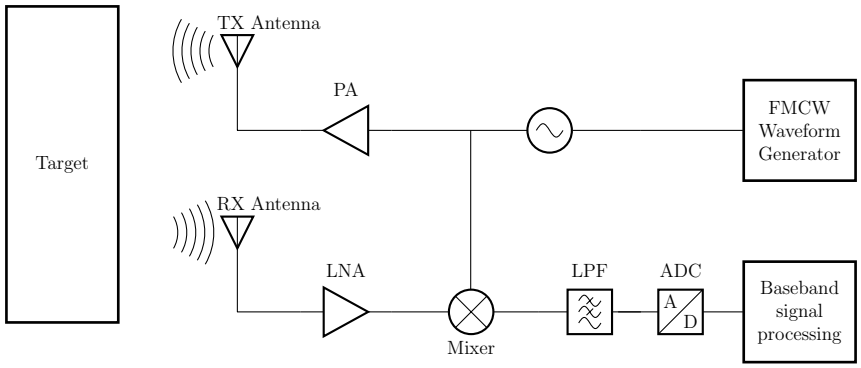


Figure 1.1: Block diagram of an FMCW radar system, adapted from [4]

The sub-terahertz (sub-THz) frequency window, spanning from approximately 100

GHz to 300 GHz, enables various advantages for modern radar systems. The large amount of available spectrum enables modulation bandwidths of several tens of gigahertz, allowing range resolutions on the order of a few millimeters. Additionally, a free-space wavelength as small as a few millimeters allows the realization of compact antennas and dense antenna arrays, improving angular resolution while reducing the overall size of the radar module. FMCW radars operating at these frequencies could be used for high-resolution imaging, package inspection, and non-destructive inspection of composite materials [5]. At sub-terahertz (sub-THz) and terahertz (THz) frequencies, the non-ionizing nature of electromagnetic radiation also makes radar attractive for biomedical imaging [6], [7]. The realization of integrated circuits operating at sub-THz frequencies presents considerable design challenges. As the operating frequency approaches the transit frequency (f_{T}) and maximum oscillation frequency (f_{max}) of the active devices, transistor gain decreases while parasitic capacitances, interconnect losses, substrate coupling, and radiation effects become increasingly significant [8].

Historically, the realization of integrated circuits operating above 200 GHz relied predominantly on III–V compound semiconductor technologies, such as gallium arsenide (GaAs) and indium phosphide (InP), owing to their superior carrier mobility and saturation velocities. These technologies have enabled state-of-the-art sub-THz and THz circuits with exceptional gain and noise characteristics. However, they generally suffer from high fabrication costs, lower manufacturing yield, limited integration density, and reduced compatibility with large-scale digital circuitry, making them less suitable for high-volume, cost-sensitive applications. Continuous advances in Silicon-Germanium (SiGe) Heterojunction Bipolar Transistor (HBT) technologies have significantly narrowed the performance gap with III–V processes while retaining the advantages of mature silicon manufacturing [9]. Modern SiGe HBTs exhibit transit and maximum oscillation frequencies well above 400 GHz, enabling the implementation of integrated circuits operating beyond 200 GHz. Furthermore, the BiCMOS platform combines high-performance RF devices with CMOS digital circuitry on the same die, offering high integration density, excellent manufacturing yield, and substantially lower production costs.

Within the receiver front-end, the LNA plays a fundamental role in determining the overall system sensitivity because it is typically the first active stage after the antenna. The noise introduced at this point cannot be removed by subsequent stages, so that a low-noise first stage is critical for a good overall receiver sensitivity. A high gain is also highly desirable, in that it suppresses the noise contributions of subsequent stages, such as the mixer and baseband circuitry. The LNA also affects other aspects of receiver performance. Its bandwidth must accommodate the complete radar signal bandwidth without excessive gain variation, while its input reflection coefficient determines how much of the signal collected by the antenna is delivered to the amplifier. Its linearity establishes the maximum input level that can be processed without significant compression or intermodulation distortion and therefore contributes to the receiver dynamic range in the presence of strong reflections or interfering signals. Finally, unconditional stability is required to prevent oscillations for the range of source and load impedances encountered during operation. The design of the LNA therefore requires a careful trade-off among noise figure, gain, bandwidth, matching, linearity, stability, and power consumption [8], [10].

This thesis presents the design of a 240-GHz LNA implemented in IHP's 130-nm SiGe

BiCMOS technology. The work focuses on selecting the circuit architecture, designing and optimizing the input and output matching networks, and analyzing transistor biasing and stability. Particular attention is devoted to the impact of layout parasitics at sub-THz frequencies and to the comparison of schematic and electromagnetic (EM) simulation results. Based on the results of this analysis, a prototype was designed and submitted for fabrication. Since the hardware was not yet available at the time of publication of this work, the measured data will be presented in a separate publication, enabling an assessment of the accuracy of the high-frequency transistor models and the EM simulations of the passive structures.

Chapter 2

Theoretical Background

2.1 Introduction

This chapter introduces the theoretical concepts required for the design and characterization of the LNA presented in this work. First, scattering parameters and the main gain definitions for two-port networks are introduced, providing the framework used to characterize the amplifier. The noise behavior of two-port networks and the noise mechanisms of SiGe HBTs are then discussed, with particular emphasis on the parameters relevant to LNA design. The chapter subsequently addresses amplifier linearity and the characterization of gain compression and intermodulation distortion. Finally, the Friis formula is introduced to highlight the importance of noise figure and gain in the first stage of a receiver.

2.2 Scattering parameters

At low frequencies, electrical networks are commonly characterized using impedance (Z) or admittance (Y) parameters. At microwave and sub-THz frequencies, however, these representations become less convenient due to the distributed nature of transmission lines and the difficulty of realizing open- and short-circuit conditions required for their measurement. Instead, linear RF networks are typically described by means of scattering parameters, or S-parameters, which relate the incident and reflected power waves at each port of the network [10].

For an N-port network, the incident power wave at port i is denoted by a_i, while the reflected power wave is denoted by b_i. Assuming all ports are referenced to the same characteristic impedance Z_0, the scattering matrix relates the incident and reflected waves according to

$$\mathbf{b} = \mathbf{S}\mathbf{a}, \tag{2.1}$$

where

$$\mathbf{a} = \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}, \qquad \mathbf{b} = \begin{bmatrix} b_1 \\ b_2 \end{bmatrix}, \qquad \mathbf{S} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}, \tag{2.2}$$

for the particular case of a two-port network.

Each scattering parameter is defined as the ratio between the reflected wave at one port and the incident wave at another port while all remaining ports are terminated by matched loads. For a two-port network,

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0}, \qquad S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0}, \tag{2.3}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0}, \qquad S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0}, \tag{2.4}$$

where the condition $a_i = 0$ indicates that the corresponding port is terminated with a matched load, so that no wave is reflected back into the network.

The physical meanings of the four scattering parameters can be summarized as follows. The input reflection coefficient S_{11} is the ratio of the wave reflected at the input port to the incident wave and therefore quantifies the input matching. Similarly, S_{22} is the output reflection coefficient and quantifies the output matching. The forward transmission coefficient S_{21} describes transmission from the input to the output and is directly related to the forward gain of the linear network. Finally, the reverse transmission coefficient S_{12} describes coupling from the output back to the input. Ideally, an amplifier exhibits a large magnitude of S_{21} and a low magnitude of S_{12}, indicating high gain and good reverse isolation, respectively.

Since scattering parameters are complex quantities, they include both amplitude and phase information. They are functions of frequency and completely characterize the small-signal behavior of a linear two-port network. Throughout this work, the S-parameters obtained from small-signal simulations are used to evaluate the amplifier gain, matching performance and stability.

2.3 Gains of a two-port network

When a generator is directly connected to a load, as in Figure 2.1, the maximum power delivered to the load is obtained when the load impedance Z_L is equal to the complex conjugate of the generator's impedance Z_G, namely $Z_\mathrm{L} = Z_\mathrm{G}^*$. This condition is referred to as *power matching*, and the corresponding power transferred to the load is the available power $P_\mathrm{A,G}$ of the generator. The available power is thus the maximum power that the generator can deliver to a load, and its value is independent of the load itself [11]:

$$P_\mathrm{A,G} = \frac{|V_\mathrm{G}|^2}{8R_\mathrm{G}}, \tag{2.5}$$

where V_G is the peak amplitude of the generator open-circuit voltage and $R_\mathrm{G} = \Re\{Z_\mathrm{G}\}$ is the real part of the generator impedance.

Inserting a two-port network between the generator and the load affects the power transfer and may introduce gain or attenuation. An amplifier can be represented as a linear two-port network characterized by its scattering parameters. In practical amplifier design, matching networks are commonly placed between the source and the amplifier input and between the amplifier output and the load. These networks can be implemented

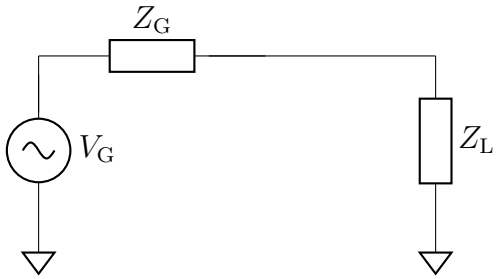


Figure 2.1: Voltage generator directly connected to a load

using distributed elements, such as transmission lines, or lumped elements, such as capacitors and inductors, to transform the source and load impedances into the values required to achieve the desired amplifier performance. Several gain definitions can be introduced depending on the considered power quantities at input and output.

The **operating power gain** G_P, also referred to simply as power gain, is defined as the ratio between the power delivered to the load and the power entering the amplifier input:

$$G_P = \frac{P_L}{P_{in}}. \tag{2.6}$$

When the amplifier output is conjugately matched, the operating power gain reaches its maximum value. Because G_P is normalized to the power entering the amplifier, it is independent of the input mismatch. In the linear operating region, a change in the power entering the amplifier produces a proportional change in the power delivered to the load, leaving their ratio unchanged. The operating power gain is therefore a suitable optimization objective when designing the Output Matching Network (OMN) standalone.

The **available power gain** G_A, also referred to simply as available gain, is instead defined as

$$G_A = \frac{P_{av,out}}{P_{av,s}}, \tag{2.7}$$

where $P_{av,out}$ is the available power at the amplifier output and $P_{av,s}$ is the available power from the source. The available power gain depends on the input matching but not on the output matching. Improving the input match increases the power entering the amplifier and, consequently, the available output power $P_{av,out}$. By contrast, $P_{av,s}$ remains constant because it is determined solely by the source generator. Changing the output match affects the power actually delivered to the load but does not alter either available-power quantity. Thus, G_A is independent of the load impedance, and is used as an optimization goal when designing the Input Matching Network (IMN) standalone.

The most commonly used definition in the design of an amplifier is the **transducer gain**,

$$G_T = \frac{P_L}{P_{av,s}}, \tag{2.8}$$

which accounts for both input and output mismatch. As discussed above, $P_{\mathrm{av,s}}$ remains constant because it is a property of the source. Improving the input match increases the power entering the amplifier and, consequently, its available output power. Improving the output match increases the fraction of this available power delivered to the load. Because G_{T} describes the overall power transfer from the source to the load, it is generally the most meaningful gain definition for complete amplifier design. It is therefore used as an optimization objective when jointly designing the IMN and OMN.

For a two-port described by its scattering parameters and terminated by arbitrary source and load reflection coefficients Γ_{S} and Γ_{L}, the transducer gain is

$$G_{\mathrm{T}} = \frac{(1-|\Gamma_{\mathrm{S}}|^2)|S_{21}|^2(1-|\Gamma_{\mathrm{L}}|^2)}{|(1-S_{11}\Gamma_{\mathrm{S}})(1-S_{22}\Gamma_{\mathrm{L}})-S_{12}S_{21}\Gamma_{\mathrm{S}}\Gamma_{\mathrm{L}}|^2}. \tag{2.9}$$

For an unconditionally stable two-port, simultaneous conjugate matching of the source and load can be achieved, and the transducer gain reaches the maximum available gain (MAG), defined as

$$\mathrm{MAG} = \frac{|S_{21}|}{|S_{12}|}\left(K-\sqrt{K^2-1}\right), \tag{2.10}$$

where K is the Rollet stability factor, defined as

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|}. \tag{2.11}$$

K quantifies the stability of a two-port based on its scattering parameters, together with the determinant

$$\Delta = S_{11}S_{22}-S_{12}S_{21}. \tag{2.12}$$

Unconditional stability is ensured when $K > 1$ and $|\Delta| < 1$. An alternative criterion for unconditional stability based on a single parameter, μ, is given by

$$\mu = \frac{1-|S_{11}|^2}{|S_{22}-\Delta S_{11}^*|+|S_{12}S_{21}|} > 1. \tag{2.13}$$

If $K < 1$, simultaneous conjugate matching of the source and load cannot be achieved while maintaining stability. In this case, the maximum stable gain (MSG) is used as a figure of merit and is given by

$$\mathrm{MSG} = \frac{|S_{21}|}{|S_{12}|}. \tag{2.14}$$

The power quantities used for the gain definitions are shown in Figure 2.2.

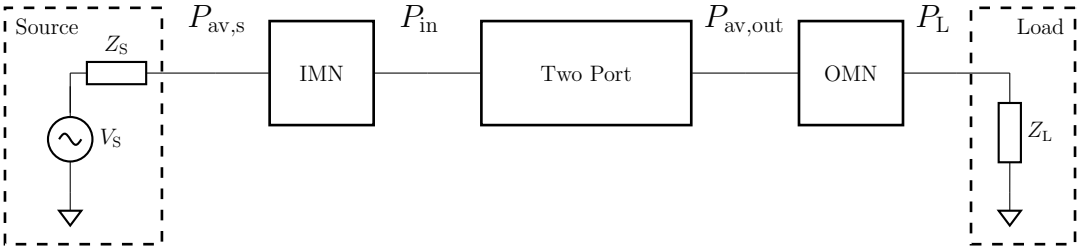


Figure 2.2: Block diagram illustrating the power quantities used for the two port gain definitions, adapted from [11]

2.4 Noise of a two-port network

The noise generated by a two-port network degrades the signal-to-noise ratio (SNR) of the processed signal and therefore limits the receiver sensitivity. The noise performance is quantified by the noise factor [12]:

$$F = \frac{\mathrm{SNR_{in}}}{\mathrm{SNR_{out}}}, \tag{2.15}$$

which is always greater than or equal to unity for a physical network. It is commonly expressed in decibels as the noise figure

$$\mathrm{NF} = 10 \log_{10}(F). \tag{2.16}$$

The noise factor depends not only on the intrinsic noise sources of the two-port, but also on the source termination. For a source admittance $Y_\mathrm{s} = \frac{1}{Z_\mathrm{s}} = G_\mathrm{s} + jB_\mathrm{s}$, it can be expressed as

$$F = F_\mathrm{min} + \frac{R_\mathrm{n}}{G_\mathrm{s}} \left| Y_\mathrm{s} - Y_\mathrm{s,n} \right|^2, \tag{2.17}$$

where F_min is the minimum achievable noise factor, $Y_\mathrm{s,n}$ is the optimum source admittance for noise matching, and R_n is the equivalent noise resistance of the two-port. These three quantities are referred to as the *noise parameters* and, like the S-parameters, are intrinsic properties of the two-port network. Equation (2.17) shows that the minimum noise factor is obtained when the source admittance equals the optimum admittance,

$$Y_\mathrm{s} = Y_\mathrm{s,n}. \tag{2.18}$$

The parameter R_n determines the sensitivity of the noise figure to deviations from the optimum source termination. A smaller R_n results in a weaker degradation of the noise factor when perfect noise matching cannot be achieved. Consequently, both a low F_min and a small R_n are desirable for low-noise amplifier design. The noise parameters of a SiGe HBT are discussed in Section 2.5.

2.5 Structure and noise modelling of SiGe HBTs

SiGe HBTs offer an excellent compromise between high-frequency performance, noise characteristics, manufacturing cost, and integration density. Unlike conventional silicon bipolar junction transistors (BJTs), SiGe HBTs employ a heterojunction formed by a

silicon emitter and a thin SiGe base. The difference in bandgap between silicon and SiGe creates a heterojunction at the emitter-base interface, enabling *bandgap engineering* to improve transistor performance without changing the basic operation of a conventional BJT [9].

The introduction of germanium reduces the bandgap between the base and the emitter relative to silicon. As a consequence, the potential barrier for electron injection from the emitter into the base is lowered, increasing the collector current for a given base-emitter voltage while leaving the base current nearly unchanged. This results in a higher current gain compared to an equivalent silicon BJT.

In modern SiGe HBTs, the germanium concentration is typically graded across the base, increasing from the emitter side toward the collector side. This grading creates a built-in electric field within the neutral base that accelerates electrons from the emitter to the collector. The reduced carrier transit time improves the transistor cutoff frequency f_{T} while simultaneously increasing the Early voltage, leading to higher gain and better high-frequency performance.

The use of a very thin SiGe base allows high base doping without significantly reducing current gain, as the reduced bandgap of the SiGe base enhances emitter injection efficiency and compensates for the increased recombination losses associated with higher base doping. The lower base resistance obtained in this way contributes to a higher maximum oscillation frequency f_{max} and improved noise performance. The schematic cross section of a SiGe HBT is shown in Figure 2.3.

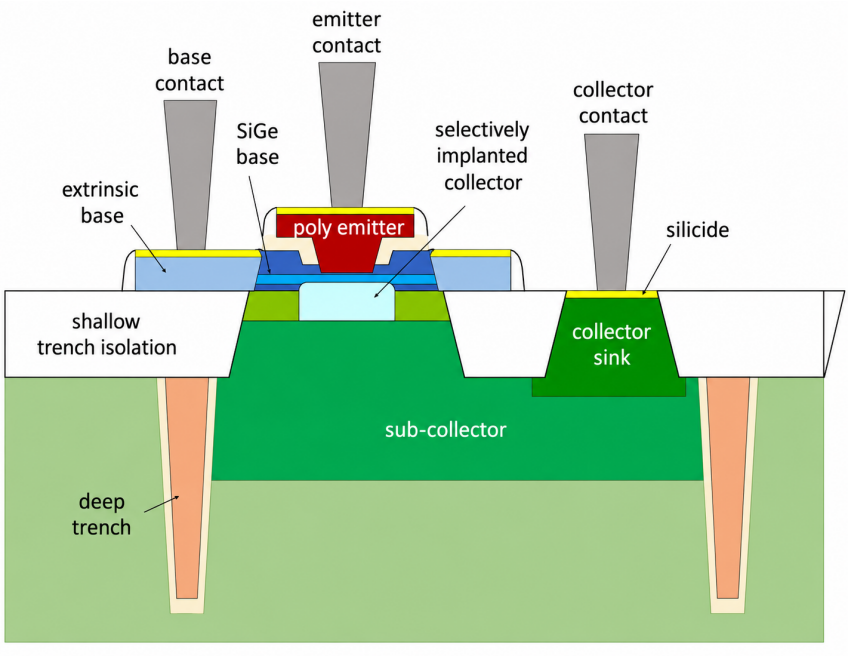


Figure 2.3: Cross section of a SiGe HBT, adapted from [13]

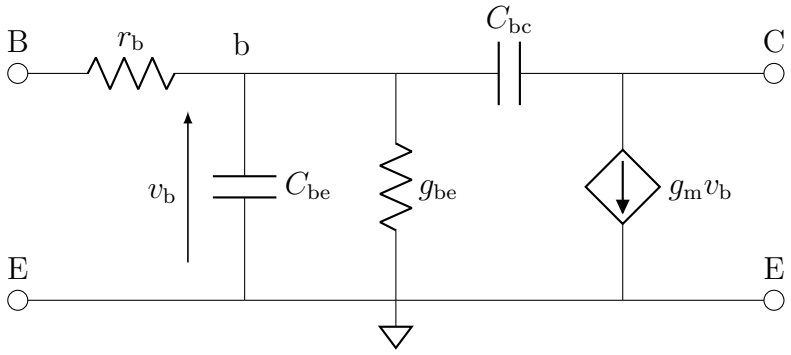


Figure 2.4: Small-signal model of a SiGe HBT used for noise parameters computation, adapted from [12]

Using the small-signal equivalent circuit of Figure 2.4, the noise parameters of a SiGe HBT can be expressed as

$$R_\mathrm{n} = r_\mathrm{b} + \frac{1}{2g_\mathrm{m}}, \tag{2.19}$$

$$G_\mathrm{s,n} = \sqrt{\frac{g_\mathrm{m}}{2R_\mathrm{n}}\frac{1}{\beta} + \frac{(\omega C_\mathrm{i})^2}{2g_\mathrm{m}R_\mathrm{n}}\left(1 - \frac{1}{2g_\mathrm{m}R_\mathrm{n}}\right)}, \tag{2.20}$$

$$B_\mathrm{s,n} = -\frac{\omega C_\mathrm{i}}{2g_\mathrm{m}R_\mathrm{n}}, \tag{2.21}$$

$$Y_\mathrm{s,n} = G_\mathrm{s,n} + jB_\mathrm{s,n}, \tag{2.22}$$

$$F_\mathrm{min} = 1 + \frac{1}{\beta} + \sqrt{\frac{2g_\mathrm{m}R_\mathrm{n}}{\beta} + \frac{2R_\mathrm{n}(\omega C_\mathrm{i})^2}{g_\mathrm{m}}\left(1 - \frac{1}{2g_\mathrm{m}R_\mathrm{n}}\right)}, \tag{2.23}$$

where r_b is the base resistance, $C_\mathrm{i} = C_\mathrm{be} + C_\mathrm{bc}$ is the sum of the base-emitter and base-collector capacitances, g_m is the small-signal transconductance, β is the current gain, and $\omega = 2\pi f$ is the angular frequency at which the noise parameters are evaluated [12].

f_T is the transition frequency, i.e. the frequency at which the short-circuit current gain of the transistor goes to unity, and it is related to C_i by

$$f_\mathrm{T} = \frac{g_\mathrm{m}}{2\pi C_\mathrm{i}}. \tag{2.24}$$

If $g_\mathrm{m}r_\mathrm{b} \gg 1/2$, Equation 2.23 can be simplified as follows:

$$F_\mathrm{min} = 1 + \frac{1}{\beta} + \sqrt{2g_\mathrm{m}r_\mathrm{b}}\sqrt{\frac{1}{\beta} + \left(\frac{f}{f_\mathrm{T}}\right)^2}. \tag{2.25}$$

Equation (2.23) shows that the minimum noise factor F_min decreases as the ratio of the transit frequency f_T to the operating frequency increases. Consequently, the minimum noise figure NF_min also decreases. At a given operating frequency, a transistor with a higher f_T can therefore provide both greater high-frequency current gain and a lower minimum noise figure. Increasing β further reduces NF_min, while lowering r_b reduces both NF_min and R_n, thereby limiting noise-figure degradation under imperfect noise-matching conditions. SiGe HBTs exhibit excellent noise performance because, as discussed at the beginning of this section, they can simultaneously achieve a high f_T, a low r_b, and a high β.

2.6 Linearity of an amplifier

An ideal amplifier exhibits a linear relationship between its input and output signals. Under these conditions, the gain remains constant regardless of the input power. In practice, an amplifier exhibits a nonlinear input-output relationship that can be represented by a power series. Under small-signal conditions, the higher-order terms are negligible, and the series can be truncated to obtain a linear approximation. As the input power increases, however, the higher-order terms become significant, introducing distortion and causing the gain to decrease. Consequently, the output power falls below the value predicted by extrapolating the small-signal gain [8].

The onset of gain compression is commonly characterized by the 1-dB compression point. This parameter is defined as the input or output power at which the amplifier gain drops by 1 dB with respect to its small-signal value. The input-referred 1-dB compression point (IP_{1dB}) is the input power at which this condition occurs, while the output-referred 1-dB compression point (OP_{1dB}) is the corresponding output power. Figure 2.5 illustrates the typical transfer characteristic of an amplifier compared to the ideal linear response.

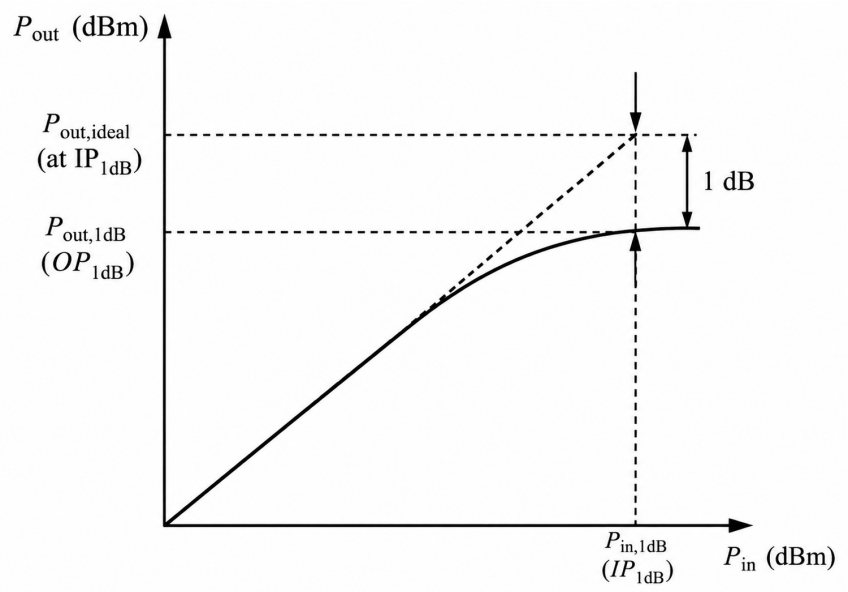


Figure 2.5: Definition of input- and output-referred 1-dB compression points, adapted from [8]

Assuming a small-signal gain G, the relationship between the IP_{1dB} and the OP_{1dB} is

$$\mathrm{OP_{1dB}} = \mathrm{IP_{1dB}} + G - 1\ \mathrm{dB}, \tag{2.26}$$

where all quantities are expressed in dBm or dB. Although the 1 dB compression point does not represent a sharp transition into the non-linear operation, it provides a convenient and widely adopted figure of merit for comparing amplifier linearity.

Nonlinearities also generate undesired frequency components when the amplifier operates below the compression region. These components, known as *intermodulation products*, arise when multiple input signals are simultaneously amplified by a nonlinear device. To characterize this behavior, the amplifier is commonly excited with two closely spaced

tones at frequencies f_1 and f_2. Due to the nonlinear transfer characteristic of the amplifier, the sum of the two components is raised to a power greater than unity. As a result, the output spectrum contains not only the amplified fundamental tones, but also additional frequency components located at combinations of the input frequencies,

$$f_{\mathrm{IM}} = mf_1 \pm nf_2, \tag{2.27}$$

where m and n are positive integers defining the order $(m + n)$ of the intermodulation product. Among these distortion products, the third-order intermodulation products (IM3s) are of particular importance. As shown in Figure 2.6, they appear at $2f_1 - f_2$ and $2f_2 - f_1$.

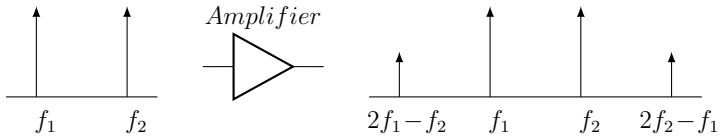


Figure 2.6: Third order intermodulation products

Unlike second-order products, which are generally located far from the desired signal and can often be removed by filtering, the third-order products lie very close to the fundamental frequencies when the input tones are closely spaced. For example, if the input frequencies are separated by Δf, the third-order products appear only Δf away from the desired signals. Consequently, they fall within the amplifier operating band and cannot be effectively suppressed by conventional filtering.

The input third-order intercept point (IIP3) is the theoretical input power level at which the linear extrapolations of the fundamental output power and of the IM3 power intersect, and the output third-order intercept point (OIP3) is the corresponding output power. Because this intersection typically occurs beyond the onset of gain compression, it cannot be actually observed. As shown in Figure 2.7 the IIP3 is determined by extrapolating results obtained in the approximately linear operating region, where the fundamental and IM3 output powers increase with input-power slopes of 1 dB/dB and 3 dB/dB, respectively. It can be demonstrated that the IIP3 is approximately 9.6 dB above the IP_{1dB} [8].

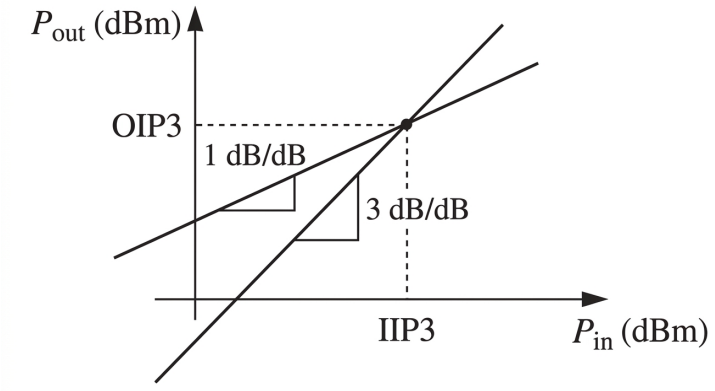


Figure 2.7: Definition of input and output third order intermodulation product, adapted from [8]

2.7 Noise figure of cascaded stages

Practical receivers consist of multiple cascaded stages, and the overall noise performance depends not only on the noise figure of each individual block but also on their gains.

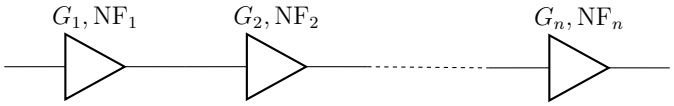


Figure 2.8: Cascaded stages

For a chain of N cascaded stages like the one shown in Figure 2.8, the overall noise factor F_{tot} is given by the Friis formula:

$$F_{\text{tot}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}}, \tag{2.28}$$

where F_i is the linear noise factor of the i-th stage and G_i is its power gain expressed as a linear ratio. Since the noise figure is commonly specified in decibels, the corresponding noise factor is obtained as

$$F = 10^{\mathrm{NF}/10}. \tag{2.29}$$

Equation (2.28) shows that the excess noise contribution of each stage is divided by the cumulative gain of the preceding stages. Consequently, the first stage has the greatest influence on the overall noise performance, while the contributions of subsequent stages are progressively suppressed by the gain preceding them. For this reason, the input stage must achieve the lowest possible noise figure because its noise contribution is added directly to the overall receiver noise and cannot be mitigated by subsequent stages. It must also provide sufficient gain to reduce the impact of noise generated by later receiver components, such as mixers, filters, and intermediate-frequency amplifiers. The Friis formula shows why minimizing the noise figure and providing sufficient gain are the principal design objectives of a LNA, which is typically the first stage of a receiver [8].

Chapter 3

Technology and passive components

3.1 Introduction

This chapter describes the technology and passive components used to implement the LNA. The main characteristics of IHP's 130-nm SiGe BiCMOS technology are first presented, including the high-frequency SiGe HBTs and the metal stack. The electromagnetic simulation methodology used throughout the design is then introduced, followed by the characterization of the transmission-line configurations provided by the technology. Finally, the behavior and modeling of the Metal-Insulator-Metal (MIM) capacitors are investigated, with particular attention to their parasitic effects and self-resonant frequency. These analyses provide the models and design considerations required for the implementation of the matching and bias networks presented in Chapter 4.

3.2 IHP's SG13G3 technology

The amplifier presented in this work is implemented using the IHP SG13G3 130-nm SiGe BiCMOS technology, which integrates high-performance SiGe HBTs and CMOS devices on a single substrate. The SG13G3 is a particular version of the 130-nm SiGe BiCMOS technology, and owing to its excellent high-frequency performance, this version is well suited for millimeter-wave and sub-THz integrated circuits, enabling the realization of low-noise, high-gain amplifiers operating at frequencies approaching 300 GHz.

The Process Design Kit (PDK) includes several HBT variants intended for high-speed, medium-voltage, and high-voltage applications. These variants differ in their peak cutoff frequency f_{T}, maximum oscillation frequency f_{max}, open-base collector-emitter breakdown voltage $\mathrm{BV_{CEO}}$, and emitter length. The maximum oscillation frequency is defined as the frequency at which the transistor's maximum unilateral power gain becomes unity. The highest-speed SiGe HBTs available in the process exhibit a state-of-the-art cutoff frequency of $f_{\mathrm{T}} = 470$ GHz, making them well suited for sub-THz LNAs. These devices achieve a maximum oscillation frequency of $f_{\mathrm{max}} = 650$ GHz, which also makes the technology suitable for the implementation of power amplifiers in the same frequency range. Finally, they feature an open-base collector-emitter breakdown voltage of $\mathrm{BV_{CEO}} = 1.5$ V [14].

All bipolar devices included in the SG13G3 PDK are modeled using the so-called HICUM/L2, a geometry-scalable, physics-based model for silicon BJTs and SiGe HBTs

designed to accurately predict DC, RF, noise, and large-signal behavior [15]. Accurate compact models are particularly important at sub-THz frequencies, where circuit performance is highly sensitive to parasitic effects and transistor nonidealities.

The process provides a seven-metal-layer back end of line, enabling the implementation of multiple transmission-line configurations as discussed in Section 3.4 and MIM capacitors with a capacitance density of 1.5 fF/μm^2. A cross-sectional image of the 130 nm BiCMOS wafer, including an enlarged view of a high-speed SiGe HBT, is shown in Figure 3.1.

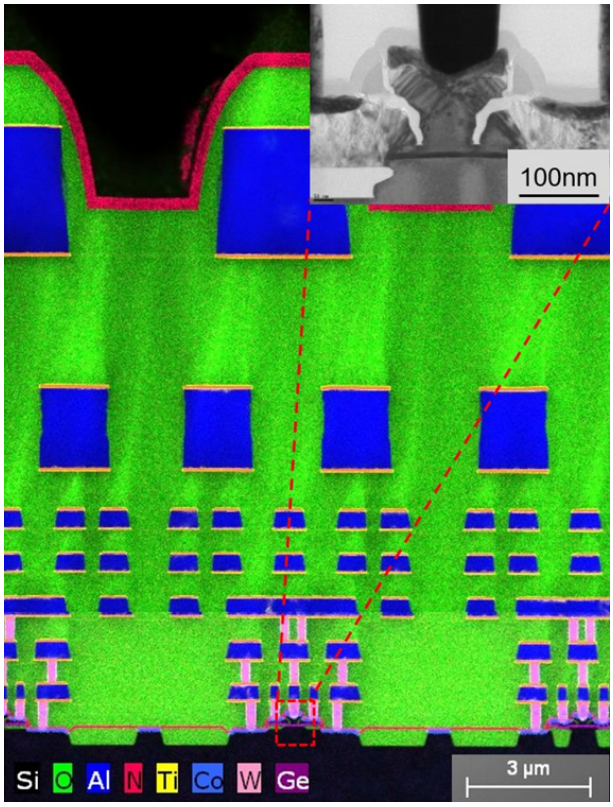


Figure 3.1: Scanning Transmission Electron Microscopy (STEM) image of a 130-nm BiCMOS wafer with enlarged cross section of a high-speed SiGe HBT (Courtesy of IHP [16])

3.3 Electromagnetic simulations

In any integrated circuit (IC), the layout introduces parasitics which are not accounted for in the schematic model and contribute significantly to the performance of the circuit. While in low-frequency analog applications these effects can be mostly captured by an RC extraction, at mm-wave and sub-THz range operating frequencies this is no longer sufficient. Since the signal is effectively a propagating EM field, effects such as parasitic inductances, skin effect, electromagnetic coupling and radiation effects become relevant, which can be captured using an EM simulator. The simulator used in this work is EMX, which is fully integrated in the Cadence Virtuoso [17] flow.

The simulator takes as input a layout file and a *process file* containing information about the metal stack, including the conductivity, height, dielectric constant, and magnetic permeability of each layer. To extract the electrical behavior of the layout, the

simulator uses the Method of Moments to solve Maxwell's equations in the frequency domain by means of an equivalent integral formulation. The structure is first discretized into mesh elements, within which the current and charge densities are assumed to have simple spatial distributions. The vector and scalar potentials generated by each element are then computed. The total vector and scalar potentials in space are obtained by summing the contributions of all elements and are used to determine the electric and magnetic field. The electric field produces current flow according to Ohm's law, while charge and current are related through the charge conservation. These relations are combined to generate a linear system of equations relating the currents to the values of the voltage sources applied at the corresponding ports. Solving this system yields the electrical parameters of the structure.

By default, conductors are assumed to have a small thickness relative to their width. Although the current flow is distributed throughout their volume, charge can accumulate only on the top and bottom surfaces, with equal charge densities on both. In this work, the conductors are instead treated as fully three-dimensional, allowing charge to accumulate on any surface with independently determined densities. For greater accuracy, the inductance and capacitance of the vias are included. Furthermore, to account for radiation effects, all simulations use the full-wave model rather than the quasi-static model, at the cost of significantly greater computational complexity and simulation time.

The *edge width* option sets the width of the mesh elements near conductor edges. Its value should be on the order of the skin depth [18], which is given by

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}}, \tag{3.1}$$

where ω is the angular frequency ($\omega = 2\pi f$), σ is the electrical conductivity, and μ is the magnetic permeability. The process file reports a relative magnetic permeability of unity for all layers; therefore, their magnetic permeability is equal to the vacuum permeability, $\mu = \mu_0$. The minimum skin depth is obtained at the maximum frequency of interest, 260 GHz, in the layer with the highest conductivity. Based on the metal thicknesses and sheet resistances reported in the process file, the highest conductivity is obtained for the uppermost layer, Top Metal 2. At 260 GHz, its corresponding skin depth is approximately 186 nm. The edge width is therefore set to 200 nm. The same value is used for the *thickness* setting, which controls the mesh size in the vertical direction.

The simulator supports two types of ports: edge ports and internal ports. Edge ports are fed by voltage sources that supply current flowing across the edge of a conductor. They are therefore used, for example, to model the excitation of the upper conductor of a microstrip transmission line. Internal ports are placed within a conductor and are fed from above by voltage sources that supply current flowing through a small region surrounding the port. They are used, for example, to model the excitation of the RF pads. In this case, the size of the ports is taken smaller than the pad surface to represent the actual dimensions of the probe tip more accurately.

By default, the reference terminals of the voltage sources are connected to an ideal, perfectly conducting metal plate placed below the metal stack. This approach should generally be avoided because it does not capture correctly the actual return path of the

current. Alternatively, they can be connected to one or more ports designated as reference ports. Ground-Signal-Ground (GSG) pads consist of a central signal pad positioned between two ground pads and are commonly used with GSG probes in RF measurements to provide signal isolation and a well-defined ground connection. When simulating this structure, the port on the signal pad is referenced to the ports on the two ground pads. Similarly, for a microstrip transmission line, the port on the top conductor is referenced to the port on the ground conductor.

The simulations are performed over the frequency range specified in the settings, which in this work typically extends from DC to 300 GHz. After meshing, the simulator provides a 3D view of the structure, which is used throughout this work to illustrate the simulated components and interconnections. The simulation results are then used to generate an S-parameter black-box model whose pins correspond to the non-reference ports. This model can subsequently be used in schematic-level testbenches.

3.4 Transmission lines

As shown in Figure 3.2, the technology features seven metal layers: Metal 1, with a thickness of 0.42 μm; Metal 2 through Metal 5, each with a thickness of 0.49 μm; and the two upper layers, TopMetal 1 and TopMetal 2, with thicknesses of 2 μm and 3 μm, respectively [19]. These layers enable various transmission-line configurations. The foundry provides scalable layouts and corresponding mathematical models for one coplanar-line configuration using TopMetal 2 and Metal 3, as well as for six microstrip configurations based on different choices of layers for the top conductor and ground plane.

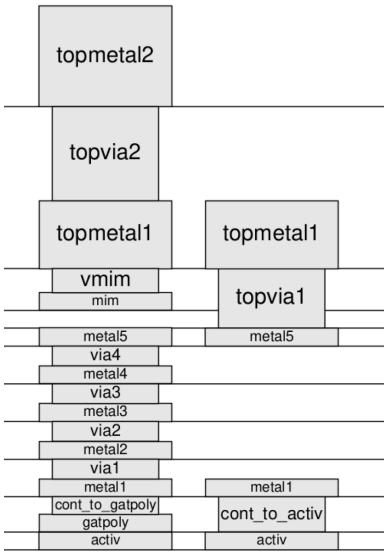


Figure 3.2: Technology's metal stack

Based on the equations derived in [20], an S-parameter-based testbench was used to extract the propagation constant γ and characteristic impedance Z_c of each transmission line. The real part of γ, denoted by α, is the attenuation constant and quantifies signal loss during propagation, whereas its imaginary part, denoted by β, is the phase constant and determines the phase shift per unit length. The propagation constant and characteristic impedance are computed as follows:

$$e^{-\gamma l} = \left\{ \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right\}^{-1}, \tag{3.2}$$

$$K = \left\{ \frac{\left(S_{11}^2 - S_{21}^2 + 1\right)^2 - \left(2S_{11}\right)^2}{\left(2S_{21}\right)^2} \right\}^{\frac{1}{2}}, \tag{3.3}$$

$$Z_{\mathrm{c}}^2 = Z_0^2 \frac{(1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2}, \tag{3.4}$$

$$\alpha = \mathrm{Re}\{\gamma\}, \tag{3.5}$$

$$\beta = \mathrm{Im}\{\gamma\}, \tag{3.6}$$

where Z_0 is the reference impedance used for the S-parameter calculations, set to 50 Ω, and l is the length of the transmission line under test. These quantities were then used to calculate the effective permittivity $\varepsilon_{\mathrm{eff}}$, which is used in the design of the distributed matching networks, as well as the quality factor Q, which provides a useful metric for comparing the different transmission-line configurations:

$$\varepsilon_{\mathrm{eff}} = \left(\frac{c\,\beta}{\omega} \right)^2, \tag{3.7}$$

$$Q = \frac{\beta}{2\alpha}, \tag{3.8}$$

where c is the speed of light in vacuum. For a meaningful comparison, the width of each transmission-line configuration was selected to obtain a characteristic impedance as close as possible to 50 Ω. Each configuration is identified by the metal layers used for the top conductor and ground plane, respectively. As shown in Tables 3.1 and 3.2, the transmission-line configuration with the highest quality factor is the microstrip which uses the uppermost metal layer, TM2, as the top conductor and the lowest metal layer, M1, as the ground plane. This configuration was therefore selected, with M1 also serving as the ground plane throughout the rest of the circuit.

Configuration	Z_{c} [Ω]	γ	Q
TM2-M1	49.54 − j482.9m	93.46 + j9.356k	**50.05**
TM2-M3	50.34 − j601.5m	114.9 + j9.443k	41.09
TM2-M5	49.14 − j756.3m	149.2 + j9.568k	32.06
TM1-M1	49.18 − j899.8m	187.5 + j10.13k	27.02
TM1-M3	47.58 − j1.413	311 + j10.4k	16.73
TM1-M5	37.12 − j2.756	837 + j11.25k	6.72

Table 3.1: Transmission-line parameters at 240 GHz for different microstrip configurations

Configuration	Z_{c} [Ω]	γ	Q
TM2-M3	47.98 − j2.138	463.2 + j10.31k	11.13

Table 3.2: Coplanar waveguide transmission-line parameters at 240 GHz

For the TM2-M1 configuration, the effective dielectric constant at 240 GHz, required for the design of the matching networks, is calculated as $\varepsilon_{\text{eff}} = \left(\frac{c\,\beta}{\omega}\right)^2 = \left(\frac{c \cdot 9.356\text{k}}{2\pi \cdot 240\ \text{GHz}}\right)^2 = 3.46$.

3.5 Capacitors

The PDK provides a scalable layout and a corresponding mathematical model for a MIM capacitor formed between Metal 5 and a closely spaced dedicated layer called *MIM*, as shown in Figure 3.3. The small separation between these layers provides a high capacitance per unit area [21].

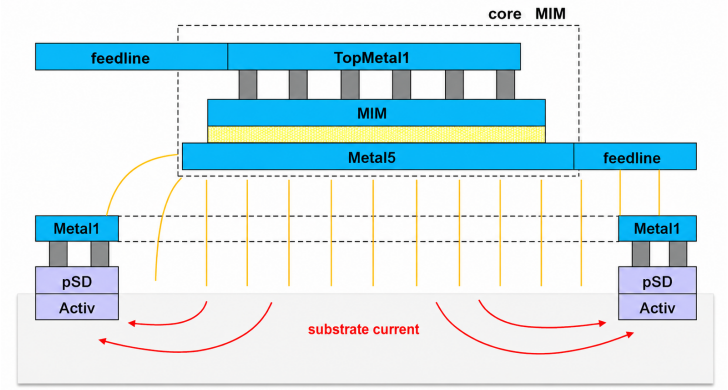


Figure 3.3: MIM capacitor from the PDK, adapted from IHP's rfcmim documentation [21]

To improve accuracy at high frequencies, the model includes the feed lines and a Metal 1 ground ring tied to the substrate, providing well-defined substrate coupling and ground-return path.

An equivalent circuit for a MIM capacitor that includes the main parasitic components is shown in Figure 3.4. Here, R_{s} and L_{s} represent the parasitic series resistance and inductance, respectively. The resistance R_{p}, placed in parallel with L_{s}, models the frequency-dependent series resistance caused by the skin effect in the metal conductors and vias. The core capacitance is represented by C_{s}, while C_{ox} represents the parasitic oxide capacitance between the bottom plate and the substrate. Finally, R_{sub} models the resistance of the lossy silicon substrate [22].

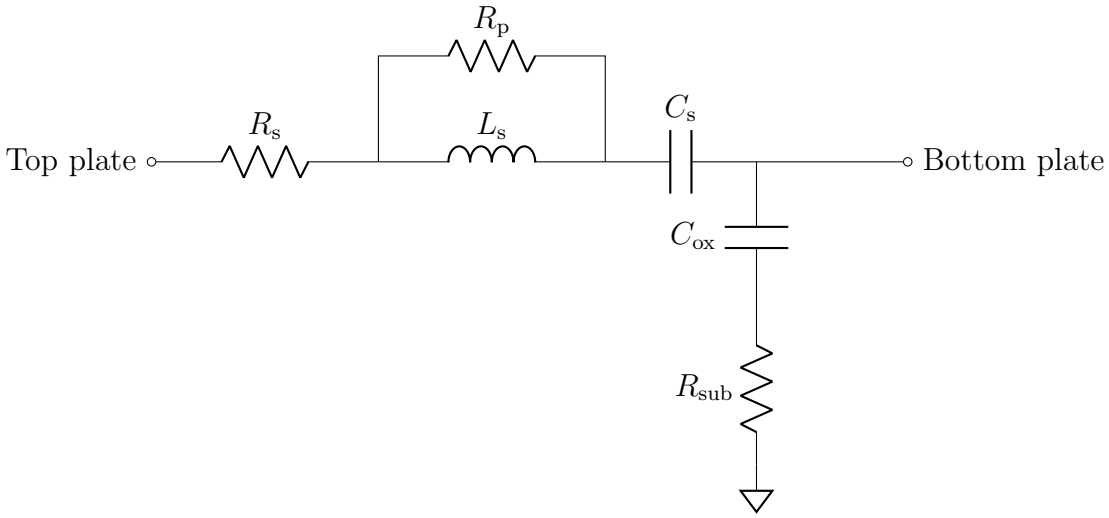


Figure 3.4: Equivalent circuit of a MIM capacitor, adapted from [22].

Due to parasitic effects, a capacitor can cease to behave capacitively at high frequencies; that is, the imaginary part of its impedance may no longer be negative. The frequency at which the imaginary part goes to zero, which sets the boundary between capacitive and inductive behavior, is referred to as Self Resonant Frequency (SRF), and decreases as the capacitance gets larger.

The maximum SRF achievable with the PDK capacitors is approximately 200 GHz, even when the plate area is reduced to the minimum allowed value. To obtain a higher SRF, custom capacitors are formed between Metal 5 and Metal 4. The greater separation between these layers results in a lower capacitance for a given plate area. The plate dimensions are then tuned using an EM-extracted model of the custom capacitor until the required SRF is achieved. Figure 3.5 shows the effective capacitance of a custom capacitor with a SRF of approximately 500 GHz. The effective capacitance is computed as

$$C_\mathrm{eff} = -\frac{1}{\omega \,\mathrm{Im}(Z)}, \tag{3.9}$$

where Z is the input impedance obtained with the second terminal of the capacitor tied to ground. After the resonance the effective capacitance becomes negative, meaning that the impedance is inductive.

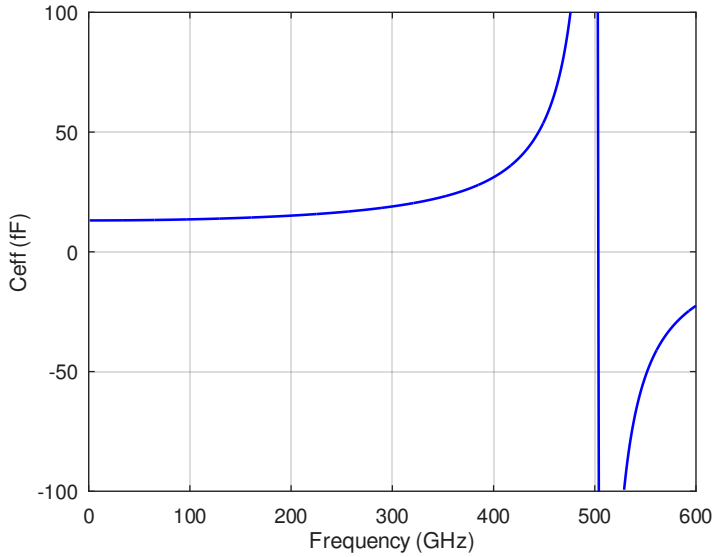


Figure 3.5: Effective capacitance with SRF=503.8 GHz as a function of frequency

In RF circuits, capacitors are often used to provide a low-impedance AC path to ground. In this case, the SRF is tuned close to 240 GHz. At the SRF, the imaginary part of the impedance becomes zero, resulting in the minimum impedance magnitude, as shown in Figure 3.6. Near the resonance, the impedance magnitude is below 2 Ω. As shown in Figure 3.7 the EM simulation includes the vias connecting one terminal to the Metal 1 ground plane and the other to the TopMetal 2 conductor of a transmission line. Therefore, the result represents the complete impedance to ground rather than only the impedance between the capacitor terminals.

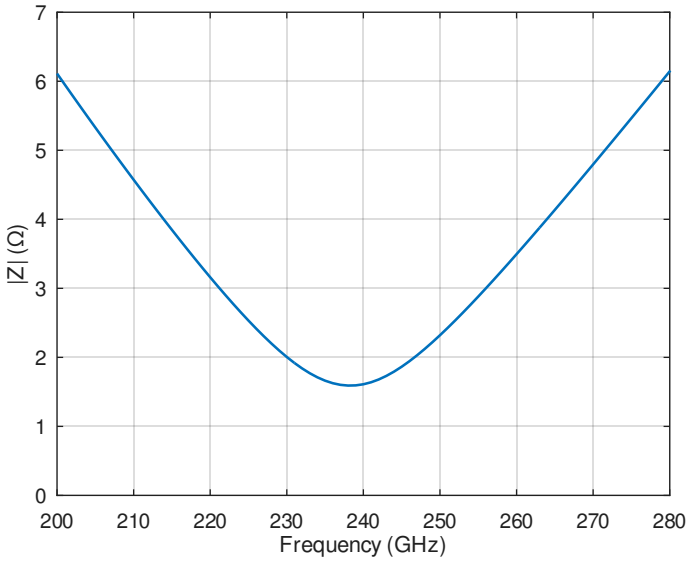


Figure 3.6: Impedance magnitude of the capacitor with SRF=238.8 GHz

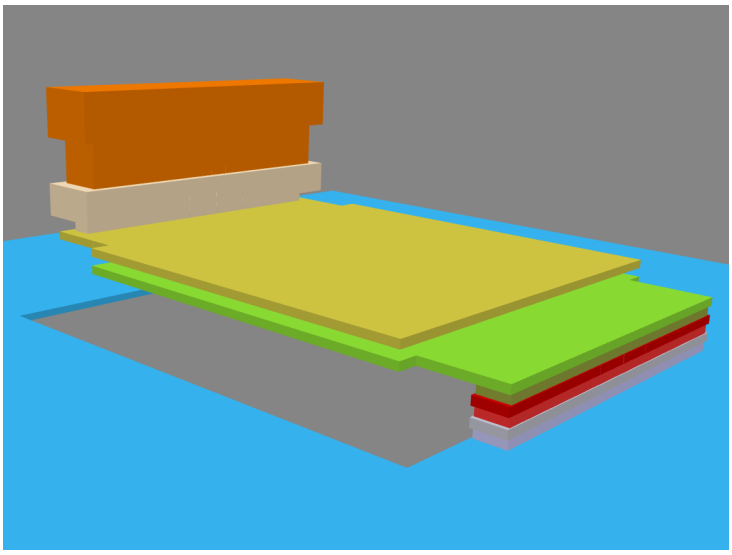


Figure 3.7: 3D view of the capacitor with SRF=238.8 GHz including vias to TM2 and M1

Centering the SRF at 240 GHz intentionally places the operating frequency in a region where the parasitics compensate the core capacitance value. As shown by the equivalent model in Figure 3.4, those parasitics include shunts to the grounded substrate. This introduces significant losses when the capacitor is not itself shunted to ground. Therefore, this design is not used for series capacitors.

For series capacitors, the SRF must be significantly higher than 240 GHz because, as shown in Figure 3.5, the effective capacitance varies rapidly with frequency near the resonance. With an SRF of 503.8 GHz, the effective capacitance values at 220 and 260 GHz, shown in Figure 3.8, deviate by less than ±5 % from the value at 240 GHz:

$$\Delta C_{\text{eff}}(220\ \text{GHz}) = \frac{15.63\ \text{fF} - 16.24\ \text{fF}}{16.24\ \text{fF}} \times 100\ \% = -3.76\ \%, \tag{3.10}$$

$$\Delta C_{\text{eff}}(260\ \text{GHz}) = \frac{16.98\ \text{fF} - 16.24\ \text{fF}}{16.24\ \text{fF}} \times 100\ \% = +4.56\ \%. \tag{3.11}$$

The capacitance value which allows to attain this SRF is 16.2 fF, resulting in an impedance magnitude greater than 40 Ω at 240 GHz. Increasing the SRF would further reduce the relative variation in effective capacitance across the frequency band, but would also increase the impedance magnitude. Therefore, the series capacitors cannot be approximated as RF short circuits, and their impedance must be included in the circuit design.

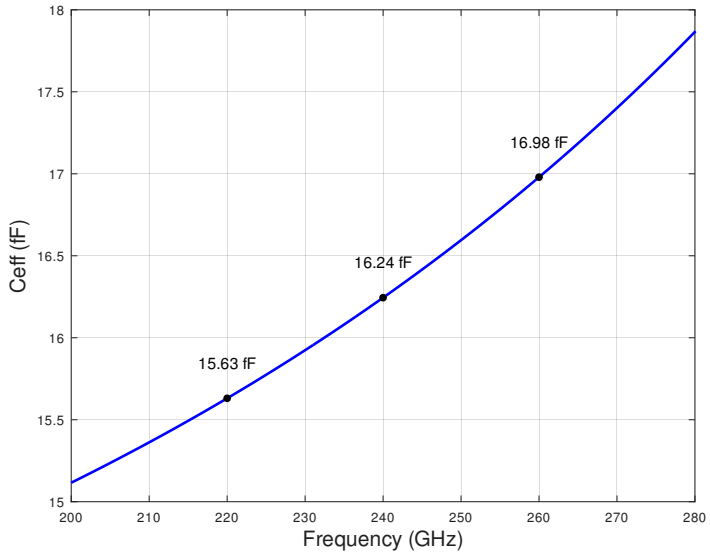


Figure 3.8: Effective capacitance with SRF=503.8 GHz as a function of frequency

Chapter 4

LNA Design

4.1 Introduction

This chapter presents the detailed design of the 240-GHz LNA implemented in IHP's 130-nm SiGe BiCMOS technology. The design process began with the selection of the circuit topology and transistor dimensions. These initial comparisons used ideal bias-Ts and preliminary implementations of the bias and matching networks that did not yet account for layout parasitics, routing constraints, or specific performance optimization. Realistic bias-Ts were then designed using the custom capacitors and transmission lines described in Chapter 3. The final matching networks were designed after extracting models for the component interconnections, pads, and transmission-line bends and junctions. This approach accounted for the parasitic impedances between the RF input and output probes and the transistor terminals. The final matching networks were also designed to embed the bias-Ts. After the layouts of the transistors' access structures, matching networks, and RF pads had been designed and simulated, a realistic bias network was implemented that accounted for routing constraints and stability.

4.2 Literature review

Despite the very competitive f_{T} and f_{max} values achieved by the latest SiGe-based technologies, the design of LNAs in the $200 - 300$ GHz frequency range remains particularly challenging. As the operating frequency approaches the transistor's maximum oscillation frequency, the available gain decreases considerably, making it difficult to achieve sufficient amplification while simultaneously maintaining a low noise figure, adequate bandwidth, unconditional stability, and reasonable power consumption.

While sub-THz SiGe LNAs using Common Emitter (CE) and Common Base (CB) topologies are reported in the literature [23],[24], recent publications show a widespread adoption of the cascode topology [25],[26],[27],[28]. CE stages generally provide the lowest intrinsic noise figure, but their available gain becomes increasingly limited at frequencies approaching 240 GHz. Najmussadat *et al.* [26] report that the cascode configuration offers a more favorable trade-off between gain, reverse isolation, and bandwidth, making it particularly suitable for operation near the technological limits of the transistors. The authors conclude that the increase in noise figure is reasonable when compared to two CE stages, and that it is compensated by the significantly higher gain and improved isolation

achieved by the cascode architecture.

Singh [27] presented two sub-THz LNAs implemented in an earlier generation of the IHP technology considered in this work: a four-stage differential cascode LNA operating at 290 GHz and a single-stage, single-ended cascode LNA centered at 235 GHz. Both amplifiers operate above $f_{\max}/2$ because of the lower f_{T} and $f_{\max}$ of the technology employed. Nevertheless, the single-stage implementation demonstrates that sufficient gain and a competitive noise figure can be achieved at 235 GHz without resorting to a multistage architecture. More recently, Gadallah *et al.* [28] demonstrated a three-stage differential cascode LNA operating at 291 GHz in IHP's SG13G3 130-nm SiGe BiCMOS technology. This design exploits the improved f_{T} and $f_{\max}$ of the newer technology generation to operate farther into the sub-THz range. The reported results show that sufficient overall gain can be achieved at frequencies approaching 300 GHz, although the available gain per stage is reduced and a multistage architecture is employed.

The results reported in [27], [28] highlight the importance of the f_{T} and $f_{\max}$ provided by the transistor technology. In particular, operation above $f_{\max}/2$ imposes increasingly stringent constraints on the achievable gain and noise performance. The higher f_{T} and $f_{\max}$ of SG13G3 compared with the preceding SG13G2 generation therefore provide additional design margin at 240 GHz. This motivates investigating whether the improved transistor performance can be exploited to achieve sufficient gain using a single-stage cascode architecture while simultaneously improving the noise figure and bandwidth relative to previous implementations.

4.3 Topology selection

In the literature, both single-ended [27],[24],[26] and differential [28],[27],[25] architectures are reported for sub-THz LNAs. The differential architecture offers advantages such as higher output power, greater immunity to substrate and supply noise, and cancellation of even-order distortion. However, it also increases the circuit area, power consumption and layout complexity, and requires baluns for measurement [8]. In this work, the LNA is designed as a standalone device without system-level constraints that would directly favor either architecture. One objective is to assess the accuracy of the high-frequency transistor and passive-component models. A differential architecture would require measurement baluns whose effects would need to be de-embedded, introducing additional uncertainty into this assessment. Therefore, a single-ended architecture is selected.

The main circuit topologies reported in the literature, namely the CE, CB, and cascode configurations, were implemented using the high-speed HBTs included in the PDK and compared in terms of their minimum noise figure $\mathrm{NF}_{\min}$ and maximum gain $G_{\max}$ at 240 GHz, as well as the frequency f_{stab} above which unconditional stability is achieved. $G_{\max}$ represents the MAG for an unconditionally stable device and the MSG for a potentially unstable device, as described in Section 2.3. Stability was assessed using the μ factor, and the topologies were evaluated without external stabilization networks.

Because the collector current affects $\mathrm{NF}_{\min}$ [12], each topology was evaluated at the current that minimized it. Ideal current sources connected to the transistor bases were used to set the bias currents precisely. In the cascode configuration, the bias current is

established by the CE transistor, therefore, the current source was connected to its base. For the CE and CB configurations, a voltage source was used to set the collector-emitter voltage V_{CE} to 1.2 V, which is below the $\mathrm{BV_{CEO}}$ reported in Section 3.2. In the cascode configuration, the base and collector voltages of the CB transistor were set to 2.1 V and 2.4 V, respectively. Because the base-emitter voltage V_{BE} of the high-speed HBTs is approximately 0.9 V, both cascode transistors operate with $V_{\mathrm{CE}} \approx 1.2$ V. The bias currents and voltages were supplied through the ideal bias-T shown in Figure 4.1. The bias-T is a block whose function is to separate the RF and DC current paths, and its ideal implementation consists of a capacitor that acts as a DC block and an RF short, together with an inductor that acts as a DC short and an RF block. The results of the comparison are presented in Table 4.1.

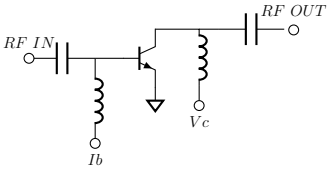
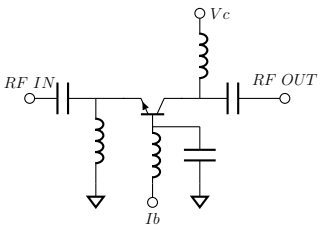
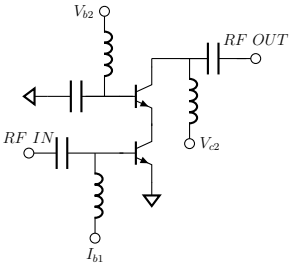
	CE	**CB**	**Cascode**
$\mathrm{NF_{min}}$ @ f_0	2.5 dB	3.0 dB	3.4 dB
$\mathrm{G_{max}}$ @ f_0	6.8 dB	11.8 dB	22.6 dB
$\mathrm{f_{stab}}$	170 GHz	295 GHz	246 GHz
Topology			

Table 4.1: Comparison of various LNA topologies at 240 GHz

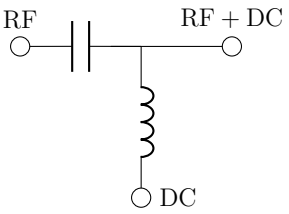


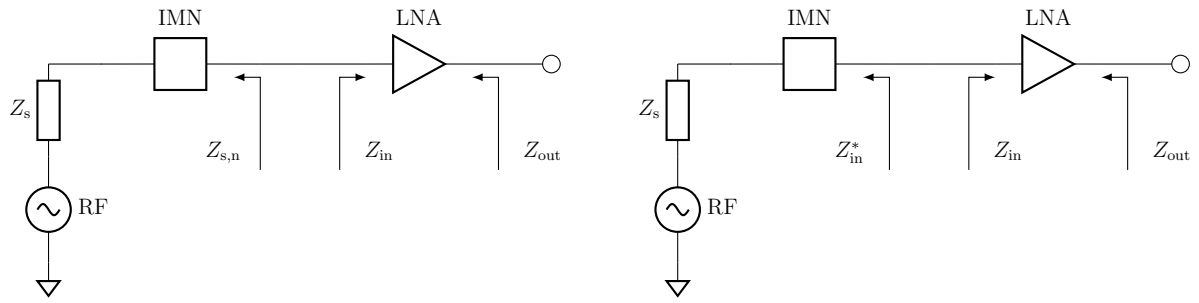
Figure 4.1: Ideal bias-T

The cascode provides significantly higher maximum gain than the other two topologies, while its minimum noise figure is less than 1 dB higher than that of the best-performing configuration, the CE stage. These two metrics correspond to different matching conditions: the minimum noise figure is achieved by presenting the optimum noise impedance to the input, whereas the maximum gain requires simultaneous input and output power matching. Consequently, they cannot generally be achieved simultaneously, and optimizing the noise figure results in a gain below G_{max} as will be discussed in Section 4.4. Furthermore, the maximum-gain values do not account for losses that will be introduced by the layout parasitics. The gain of the CE and CB configurations is therefore most likely insufficient for a single-stage design, and the cascode topology was selected. As discussed in Section 4.2, Singh proved the feasibility of a cascode single-stage sub-THz

LNA even with an older version of the technology available for this work, in accordance with the results obtained here.

4.4 Transistors sizing

As discussed in Chapter 2 the noise figure is minimized when the source impedance presented to the amplifier input is equal to the optimum noise impedance, denoted by $Z_{\mathrm{s,n}}$ (see Figure 4.2a). Maximum power transfer into the amplifier instead requires the source impedance to equal the complex conjugate of the input impedance, Z_{in}^* (see Figure 4.2b). In general, $Z_{\mathrm{in}}^* \neq Z_{\mathrm{s,n}}$, therefore, $\mathrm{NF}_{\mathrm{min}}$ and G_{max} cannot be achieved simultaneously, and a compromise between noise matching and input power matching is required. If the transistor dimensions can be selected such that $Z_{\mathrm{in}}^* = Z_{\mathrm{s,n}}$, simultaneous noise and input power matching can be achieved. In this work, the simultaneous-matching parameter $\mathrm{SM} = 10\log_{10}(|Z_{\mathrm{in}}^* - Z_{\mathrm{s,n}}|\,/1\ \Omega)$ is defined to quantify the difference between these two impedances during transistor sizing. In other contexts, the term *simultaneous matching* may instead denote simultaneous power matching at the input and output.



(a) IMN for noise Matching (b) IMN for input power matching

Figure 4.2: IMN for noise matching and for input power matching

As described in Section 3.2, the PDK provides several HBT variants. The transistors with the highest transition frequency f_{T} were selected to maximize the current gain and minimize $\mathrm{NF}_{\mathrm{min}}$, as discussed in Section 2.5. Because the emitter length of this transistor variant is fixed, only the number of emitters, N, can be adjusted, with discrete values ranging from 1 to 8. To determine the optimum value of N, the cascode topology was evaluated without matching networks, using ideal bias-Ts and the preliminary bias network shown in Figure 4.3. As N was varied, the total bias current was scaled proportionally to maintain the bias current per emitter finger that minimized $\mathrm{NF}_{\mathrm{min}}$. The base and collector bias voltages of the CE transistor were selected to maintain both cascode transistors in the forward-active region, with a collector-base voltage of approximately $V_{\mathrm{CB}} = 0.3$ V.

As shown in Figure 4.3, to set the bias current accurately, the base voltage of the CE transistor V_{b1} is generated by a diode-connected transistor forming a current mirror, driven by a reference current source. The base voltage of the CB transistor V_{b2} is generated by adding a resistor and a second diode-connected transistor above the mirror transistor. The collector voltage of the CB transistor V_{c2} is generated directly by the 2.4 V supply.

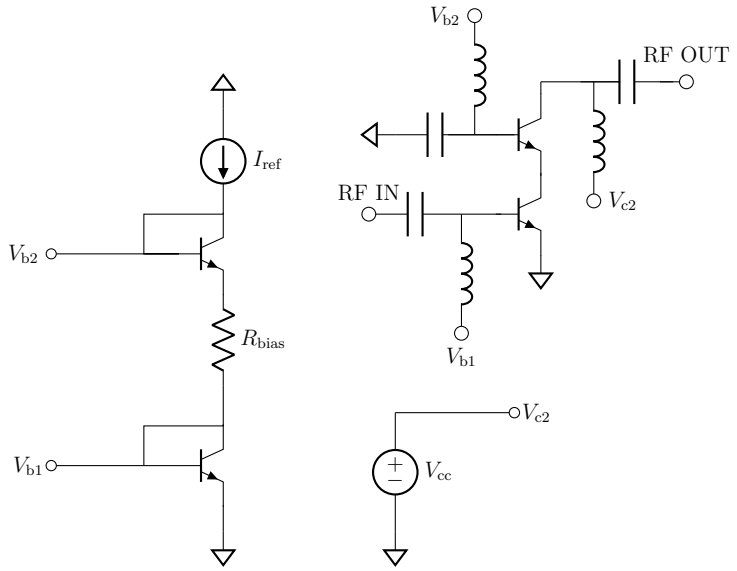


Figure 4.3: Cascode with initial bias network implementation

As shown in Table 4.2, when the bias current per emitter, I_c/N, is held constant to maintain the lowest NF_{min}, increasing the number of emitters in both transistors causes Z_{in} and $Z_{s,n}$ to decrease approximately in inverse proportion with N.

N	I_c **[mA]**	$Z_{s,n}$ [Ω] @ f_0	Z_{in} [Ω] @ f_0	Z_{out} [Ω] @ f_0
1	2.84	$115.4 + j71.41$	$39.71 - j37.74$	$17.51 - j316.10$
2	5.69	$57.71 + j35.71$	$19.72 - j18.53$	$11.85 - j157.80$
3	8.53	$38.48 + j23.81$	$13.12 - j12.14$	$8.94 - j105.30$
4	11.38	$28.86 + j17.86$	$9.861 - j8.964$	$7.16 - j79.08$
5	14.22	$23.09 + j14.29$	$7.921 - j7.078$	$5.96 - j63.32$

Table 4.2: Effect of the number of emitters on optimal noise impedance, input impedance and output impedance at f_0=240 GHz

In addition to Z_{in} and $Z_{s,n}$, the number of emitters affects the amplifier output impedance, Z_{out}. According to the Bode–Fano theorem, the achievable bandwidth (BW) of a passive impedance matching network is fundamentally limited by the required Impedance Transformation Ratio (ITR). In general, larger ITRs require higher-quality-factor matching networks, resulting in a narrower BW [10]. Furthermore, because the matching networks are lossy, the required transformations also affect their insertion losses. For these reasons, both the input and output matching networks must be designed to determine the optimum number of emitters. The sizing of the networks depends in turn on the number of emitters, so that a co-optimization of the actives and passives is required [29].

At sub-THz frequencies, distributed matching networks are generally preferred to lumped-element implementations because the physical dimensions of lumped components become non-negligible relative to the signal wavelength. Under these conditions, parasitic inductance, capacitance, and self-resonance strongly influence the behavior of the component, reducing the validity of the lumped-element approximation. For this comparison,

both matching networks were implemented using a series transmission-line segment and a single stub based on the PDK models. The type of stub termination, either open- or short-circuited, and the initial line lengths were determined using an online Smith chart tool configured with the previously extracted transmission-line parameters. The lengths were then refined using the optimizer embedded in the simulation environment, in conjunction with the PDK model of the transmission lines.

Compared with ideal lumped LC networks or ideal transmission lines, the PDK transmission-line models provide more realistic results and account for losses that improve amplifier stability. As shown in Section 4.3, the cascode configuration without matching networks was unconditionally stable only above 246 GHz. Incorporating the lossy matching networks rendered it unconditionally stable throughout the simulated frequency range of 1–300 GHz. Each configuration could therefore be evaluated without an additional stabilization network, which would otherwise have to be optimized to minimize the gain and noise figure degradation in-band.

The input and output matching networks could not be designed independently. Indeed, due to the finite reverse transmission coefficient S_{12} of the amplifier, Z_{in} shows substantial dependence on the load impedance. At 240 GHz, the magnitude of S_{12} is approximately -38 dB. For a two-port network terminated by a load with reflection coefficient Γ_{L}, the input impedance can be expressed as

$$Z_{\text{in}} = Z_0 \frac{1 + \Gamma_{\text{in}}}{1 - \Gamma_{\text{in}}}, \tag{4.1}$$

where

$$\Gamma_{\text{in}} = S_{11} + \frac{S_{12} S_{21} \Gamma_{\text{L}}}{1 - S_{22} \Gamma_{\text{L}}}. \tag{4.2}$$

These relations show that the implementation of the OMN modifies the load reflection coefficient Γ_{L} and therefore affects the input impedance. If the reverse transmission coefficient were sufficiently small, the second term in the expression for Γ_{in} would be negligible, such that

$$\Gamma_{\text{in}} \approx S_{11}, \tag{4.3}$$

and the input impedance would be effectively independent of the OMN.
The OMN was therefore implemented first and optimized using the operating power gain G_{P} of the amplifier as the optimization goal rather than the transducer gain G_{T}. The reason is that otherwise the optimizer may compromise the output match in an attempt to improve the match between the source and the amplifier input, which is instead the task of the IMN.

Table 4.3 presents the input and optimum noise impedances for several values of N, both before and after implementation of the OMN. The optimum noise impedances remain virtually unchanged, whereas the OMN reduces both the real part and the imaginary part (in absolute value) of the input impedances.

	Before OMN	**After OMN**	**Before OMN**	**After OMN**
N	Z_{in} [Ω] @ f_0	Z_{in} [Ω] @ f_0	$Z_{\text{s,n}}$ [Ω] @ f_0	$Z_{\text{s,n}}$ [Ω] @ f_0
1	$39.71 - \text{j}37.74$	$27.97 - \text{j}30.42$	$115.4 + \text{j}71.41$	$114.2 + \text{j}70.56$
2	$19.72 - \text{j}18.53$	$11.73 - \text{j}13.99$	$57.71 + \text{j}35.71$	$57.39 + \text{j}35.48$
3	$13.12 - \text{j}12.14$	$7.22 - \text{j}8.45$	$38.48 + \text{j}23.81$	$38.32 + \text{j}23.7$
4	$9.861 - \text{j}8.964$	$5.15 - \text{j}6.26$	$28.86 + \text{j}17.86$	$28.76 + \text{j}17.79$
5	$7.921 - \text{j}7.078$	$3.56 - \text{j}5.091$	$23.09 + \text{j}14.29$	$23.02 + \text{j}14.24$

Table 4.3: Input impedance Z_{in} and optimal noise impedance $Z_{\text{s,n}}$ before and after implementing the OMN optimized for power gain

Table 4.4 shows that increasing N improves both G_{P} and SM, but also increases the required bias current and, consequently, the DC power consumption. Because the improvements in G_{P} and SM become progressively smaller as N increases, values above 5 were not considered.

N	I_{c} [mA]	G_{P} [dB] @ f_0	SM @ f_0
1	2.84	15.74	19.78
2	5.69	17.44	17.03
3	8.53	18.15	15.40
4	11.38	18.53	14.19
5	14.22	18.76	13.32

Table 4.4: Operating power gain and simultaneous matching parameter of the LNA with OMN for different values of N, under constant bias current density

After implementing the IMN, the input and output matching networks were jointly optimized using NF, G_{T}, and S_{11} as optimization objectives. As shown in Table 4.5, both NF and S_{11} exhibit limited sensitivity to the number of emitters, whereas G_{T} reaches its maximum for $N = 3$ and the BW increases with increasing N. The $N = 4$ configuration provides a G_{T} and BW close to their respective maximum values, while avoiding the additional power consumption associated with larger transistor sizes, making it the best overall compromise. Here, the BW is defined as the frequency interval over which G_{T} remains within 3 dB of its value at 240 GHz.

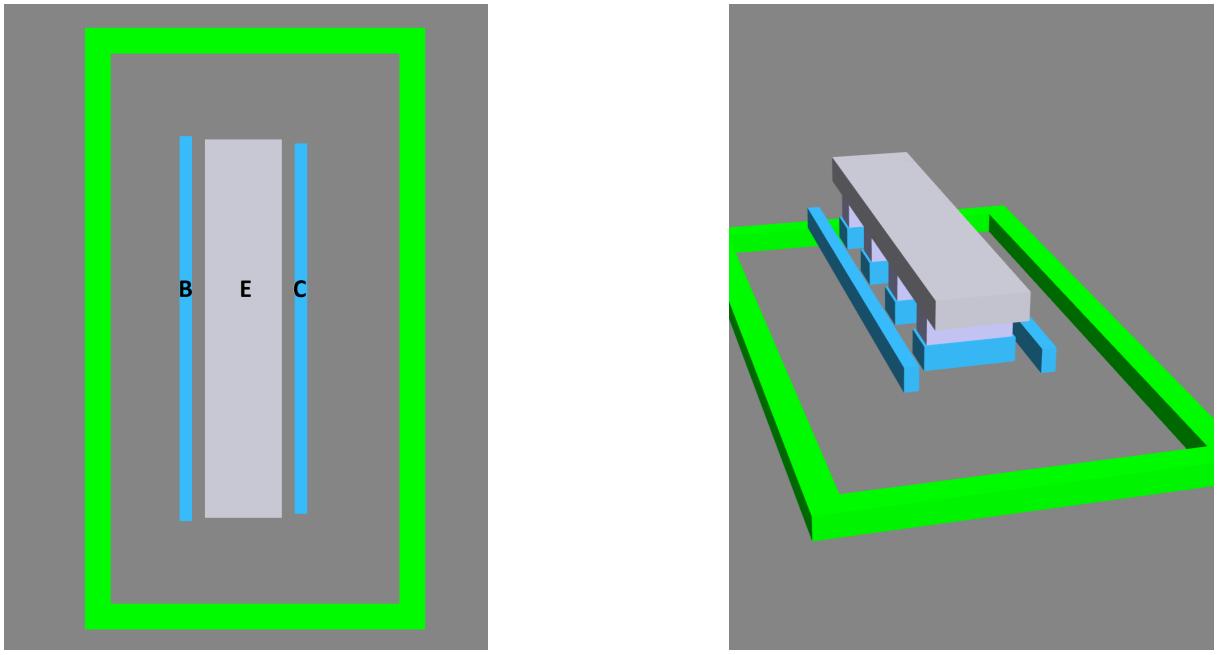
N	**NF [dB] @ f_0**	**G_{T} [dB] @ f_0**	**BW [GHz]**	**S_{11} [dB] @ f_0**	I_{c} [mA]
1	5.02	14.86	23	-30.75	2.84
2	4.97	15.67	40	-31.81	5.69
3	4.96	16.06	45	-28.24	8.53
4	4.93	15.99	56	-28.06	11.38
5	4.89	15.81	58	-28.8	14.22

Table 4.5: Noise figure, transducer gain, BW, input reflection coefficient and collector current of the LNA with IMN and OMN

In all cases, the substantial difference between G_{P} and G_{T} indicates that the implementation of the IMN introduces considerable losses relative to an ideally matched input. Since the input reflection coefficients indicate good input power matching, this difference is attributed primarily to transmission-line losses. Similarly, the implementation of the OMN reduces the gain significantly compared to G_{max}. As discussed in Section 4.3, these losses explain why the CE and CB configurations were ruled out for a single-stage design.

4.5 Transistor access structures and core layout

The base and collector pins of the transistor model are located on Metal 1, whereas the emitter pin is located on Metal 2. The metals used for the pins set the boundary of the transistor's model, meaning that the parasitics are included up to Metal 1 for the base and collector and up to Metal 2 for the emitter. As shown in Figure 4.4 the pins are narrow and closely spaced, and only a limited number of vias can be used to connect to the transistors, resulting in significant parasitic impedances.



(a) Simplified layout view

(b) 3D view

Figure 4.4: Simplified layout and 3D view of NPN transistor with N=4

The contribution of the parasitic impedances associated with the connection to the non-grounded terminals, namely the base of the CE transistor and the collector of the CB transistor can be accounted for by tuning the IMN and OMN, respectively. By contrast, the connections to ground cannot be compensated through the matching networks and are therefore optimized to minimize the parasitic impedance overhead. As shown in Figure 4.5, the emitter of the CE transistor is grounded on both sides through very short lines connecting its Metal 2 pin to the ground plane on Metal 1.

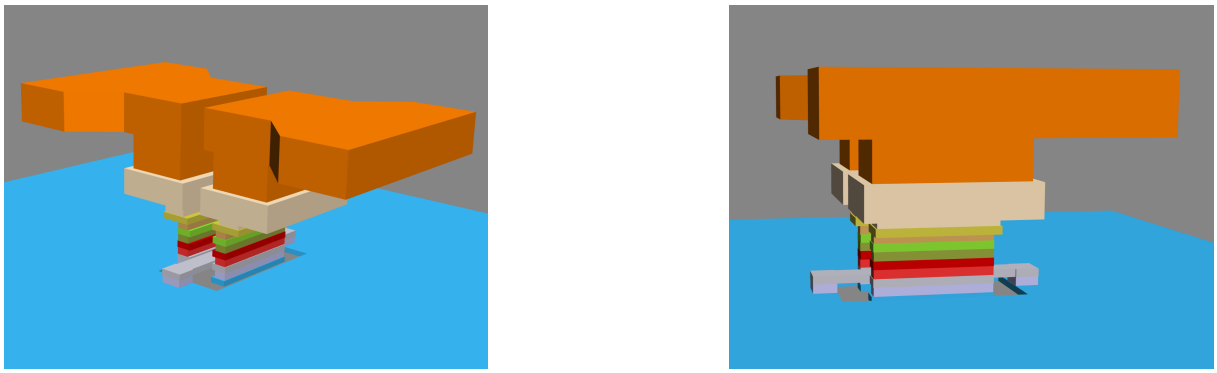


Figure 4.5: 3D views of the CE transistor's access structure

The base of the CB transistor must be grounded only for the AC by means of a capacitor, so that the bias voltage can be supplied. As discussed in Section 3.5, centering the capacitor's SRF at 240 GHz minimizes the magnitude of its impedance. However, the relevant impedance is that between the transistor base pin and ground, which includes also additional interconnections and vias. The capacitor is therefore placed close to the base, and its plate area is adjusted so that the SRF of the complete base-to-ground structure is centered at 240 GHz.

The bias line for V_{b2} is implemented on Metal 4 and connected directly to the capacitor feed line on the transistor side. Because it has a non-negligible effect on the SRF, it is included in the simulated structure. Using a narrow Metal 4 line instead of a TopMetal 2 line provides two advantages: it creates a high-impedance transmission line that improves the separation between the DC and RF paths, and it avoids the need to reposition the other TopMetal 2 lines to comply with the minimum-spacing design rule. Farther from the transistor, the bias line is routed to TopMetal 2 to connect to the remainder of the bias network.

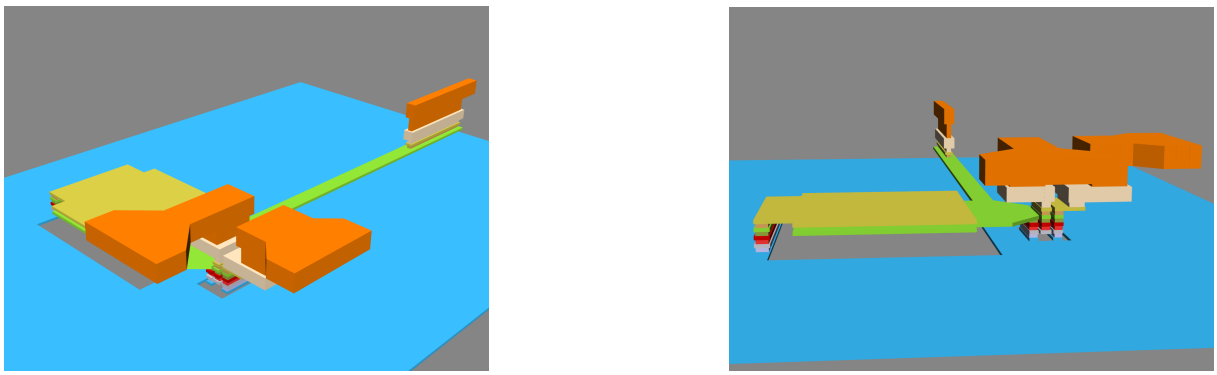


Figure 4.6: 3D views of the CB transistor's access structure

The CE and CB transistors of the cascode are connected by a transmission line with a 90° bend, which also serves as an interstage matching network for reducing the noise figure [30]. Optimizing the line length reduced the noise figure by 0.36 dB compared with directly connecting the two transistor access structures. The resulting layout of the amplifier core is shown in Figure 4.7.

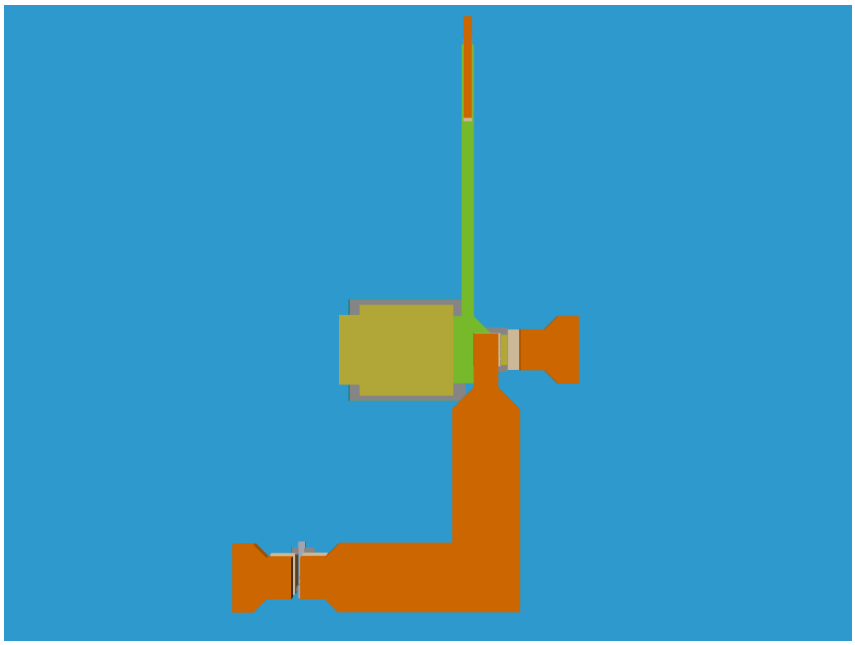


Figure 4.7: Top view of the amplifier core's layout

4.6 Impedance Matching Networks

4.6.1 Topologies with embedded bias-T

The ideal bias-T shown in Figure 4.1 uses a lumped inductor to create a DC short and an RF open. At sub-THz frequencies, implementing conventional spiral inductors with high inductance and a high quality factor is challenging because of the skin effect, substrate losses, parasitic capacitance, and reduced self-resonant frequency [31]. The inductor can therefore be replaced by a quarter-wavelength transmission line terminated with a grounded capacitor as shown in Figure 4.8. The capacitor provides an RF ground, which the $\lambda/4$ transmission line transforms into an RF open circuit. Because the transmission line also acts as a short for DC, the required separation between the RF and DC currents at the design frequency is achieved.

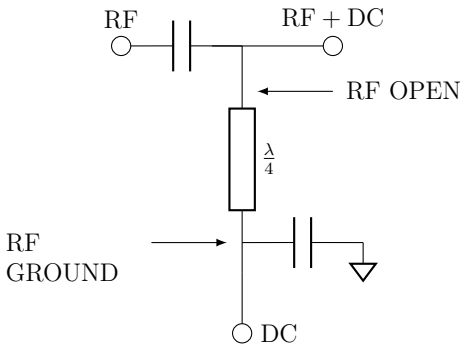


Figure 4.8: Bias-T without lumped inductor

The DC-blocking capacitors exhibit non-negligible impedance at the frequencies of interest, and they therefore affect the impedance matching. The transmission lines and

RF-grounding capacitors of the bias-Ts can also contribute to the impedance transformation. A $\lambda/4$ transmission line ideally makes the bias-T branch appear as an open circuit to the RF path; however, a quarter-wavelength line is not essential for preventing the RF signal from entering the DC path. The capacitor provides a low-impedance path to ground, while a narrow metal line is used for the DC feed, forming a high-characteristic-impedance transmission line that further isolates the RF path. Consequently, the bias-Ts are not implemented as separate networks placed next to the transistors, but are instead embedded within the matching networks.

Using a transmission-line length different from $\lambda/4$ causes the line and grounded capacitor to behave as a short-circuited stub that contributes to the impedance matching. This approach transforms the original single line-stub topology into a double line-stub topology without adding components, which can be exploited to obtain greater BW and improve consistency between schematic and EM simulations. Indeed, while a single line-stub matching network produces one resonance, the double line-stub network produces two resonances that can be distributed across the operating band to increase its BW [10]. Moreover, because the resonance frequencies generally shift when transitioning from schematic to EM simulations, using multiple resonances makes the overall performance less sensitive to the frequency shift of any individual resonance.

To highlight the effect of the matching-network topology, a single-line, single-open-stub IMN and a double-line, double-open-stub IMN were compared using ideal bias-Ts. The IMNs were designed to power match the input impedance shown by the amplifier core, and the target impedance is $Z_{\text{in}}^{*} = (14.76 - \text{j}1.16)\ \Omega$. The schematic and impedance transformations of the single line-stub IMN and of the double line-stub IMN are shown respectively in Figures 4.9 and 4.10. In both cases an additional transmission line is placed before the first stub, to accurately model the T-junction, as will be discussed in Subsection 4.6.2. This line has a negligible effect on the impedance matching because its characteristic impedance is close to 50 Ω and it is connected directly to a node which shows a 50 Ω impedance.

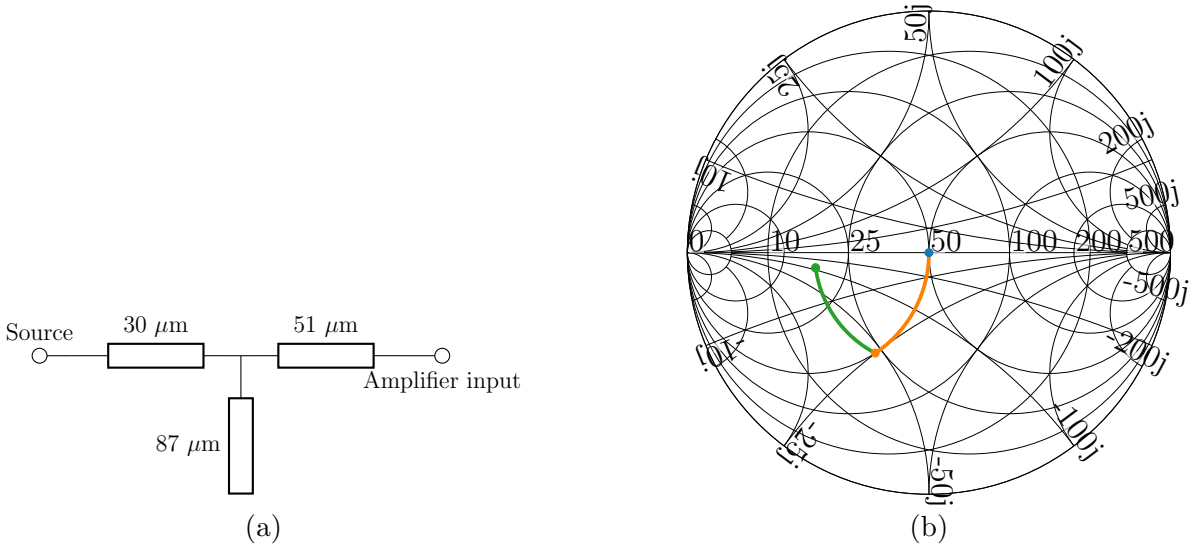


Figure 4.9: Single-line stub IMN: (a) circuit diagram, (b) Smith-Chart plot of the impedance transformation at 240 GHz

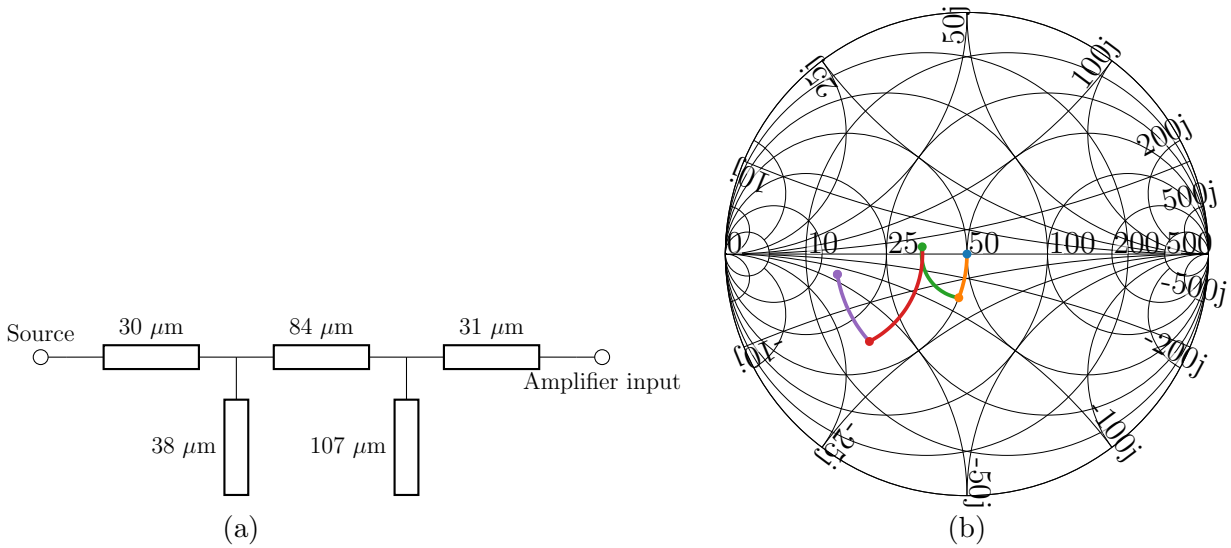
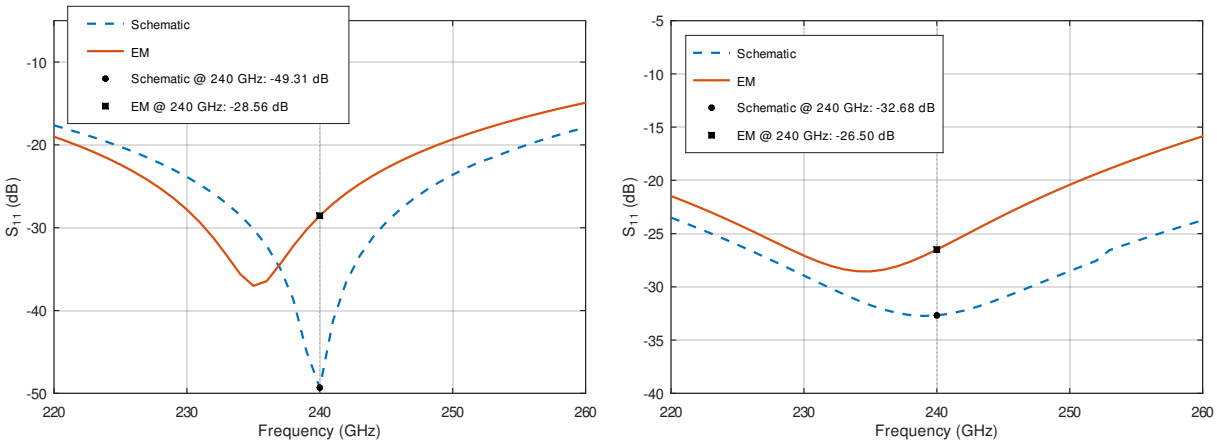


Figure 4.10: Double line-stub IMN: (a) circuit diagram, (b) Smith-Chart plot of the impedance transformation at 240 GHz

As shown in Figure 4.11a, the shift of the single resonance between the schematic and EM simulations produces substantially different responses in the case of a single-line, single-stub matching network. By contrast, the double-line, double-stub topology produces a flatter response, as shown in Figure 4.11b, making its performance less sensitive to shifts in the resonance frequencies. Although the discrepancy between the schematic and EM results is reduced compared to the single line-stub case, it remains significant for the double line-stub IMN. This behavior can be attributed to the high sensitivity of the input reflection coefficient to variations in the IMN, which is also why it was selected as the performance metric for this comparison.



(a) Single line-stub IMN

(b) Double line-stub IMN

Figure 4.11: S_{11} versus frequency for the single line-stub and double line-stub IMNs

The main drawback of embedding the bias-T within the matching network is that it restricts the space of the usable topologies. One of the stubs must be grounded, while the bias current must be prevented from flowing either into the RF port or to ground, as would be the case with the topology of Figure 4.12. Consequently, the DC-blocking

capacitor, which forms the other component of the bias-T, cannot be placed after the DC-carrying stub in the IMN or before it in the OMN. Additionally, if two short-circuited stubs are used, the capacitor must be placed between them.

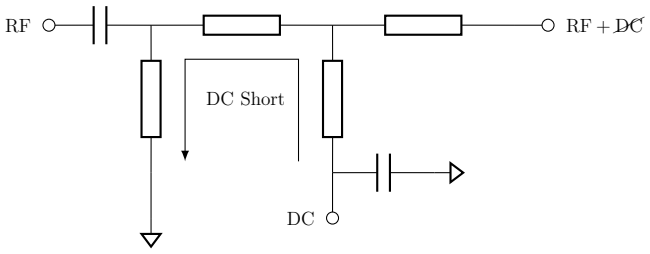
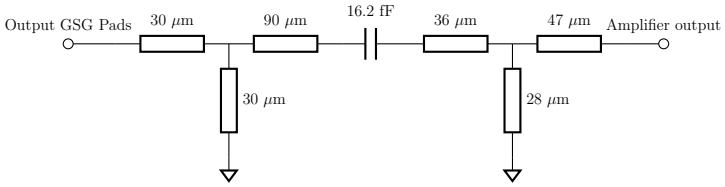


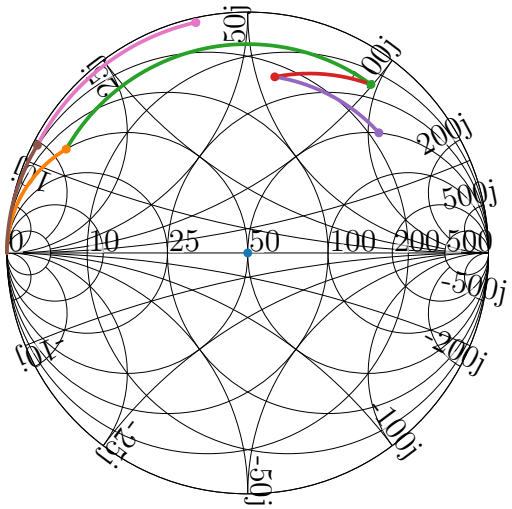
Figure 4.12: Matching network with embedded bias-T and DC bias short

4.6.2 Design and optimization

The matching networks were initially designed using the Smith-chart tool to transform the external 50 Ω port impedances into the complex conjugates of the input and output impedances of the complete amplifier core, including the transistors, their access structures, and the bent interstage transmission line (see Section 4.5). The target impedances are $Z_{\text{in}}^{*} = (14.76 - \text{j}1.16)\ \Omega$ for the IMN and $Z_{\text{out}}^{*} = (1.03 + \text{j}40)\ \Omega$ for the OMN.

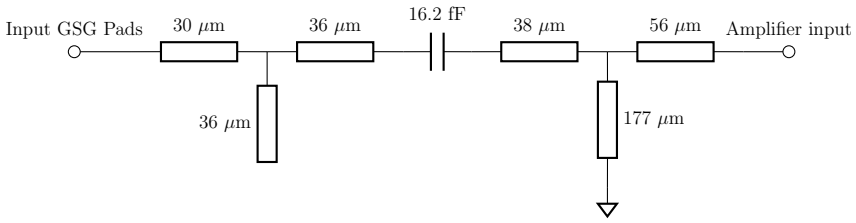


(a) Schematic of the OMN

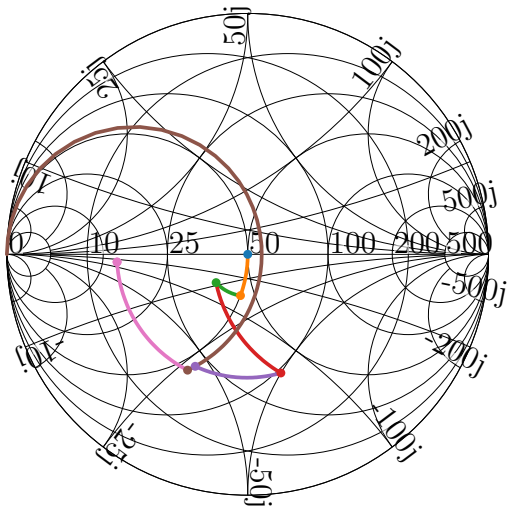


(b) Impedance transformation of the OMN

Figure 4.13: Smith-chart tool design of the OMN



(a) Schematic of the IMN



(b) Impedance transformation of the IMN

Figure 4.14: Smith-chart tool design of the IMN

As shown in Figure 4.13a, the selected OMN consists of two short-circuited stub and series line sections, separated by the DC-blocking capacitor. As shown in Figure 4.14a, the IMN consists of one open-circuited stub and series line section and one short-circuited stub and series line section, also separated by the DC-blocking capacitor. The corresponding impedance transformations are shown respectively in Figure 4.13b and Figure 4.14b. Some intermediate points on the chart are not connected because the Smith-chart tool plots each short-circuited-stub arc starting from 0 Ω.

After the initial transmission-line and stub lengths had been determined, the matching networks were tuned using the optimization tool, with transducer gain, noise figure, S_{11}, and BW specified as optimization goals. Although, for the reasons discussed in Section 3.3, EM simulations are essential for accurately evaluating the performance of the matching networks, the optimization itself was performed at the schematic level, because of the much lower computational cost. As described in the following, models extracted from EM simulations of individual components were incorporated into the schematic-level testbench to improve the agreement with the EM simulation of the complete layout.

Some passive structures cannot be represented accurately using the schematic models provided by the PDK. As an example, the available transmission-line T-junction and 90° bend models do not sufficiently agree with their EM-extracted counterparts. These components, along with the components that are not included in the PDK such as the custom capacitors described in Section 3.5 and the transistor access structures described in Section 4.5, are therefore represented at the schematic level using models extracted from

their individual EM simulations. As described in Section 3.3, these are S-parameter-based black-box models; consequently, the physical structure cannot be modified without repeating the EM simulation and model extraction. However, this limitation does not cause significant problems because the capacitors do not require further modification once the desired SRF is achieved, and components such as transmission-line junctions and bends have fixed dimensions.

Once the matching-network topology has been selected, the optimization reduces to adjusting the transmission-line lengths. Unlike the schematic models of other components, the scalable transmission-line model provided by the PDK accurately reproduces the corresponding EM results. Therefore, this model is used in conjunction with the EM-extracted component models during the optimization process. Since the PDK does not provide schematic models for transmission-line tapers or vias between metal layers, each individually simulated component includes the required vias to connect it to the rest of the circuit. Where necessary, a short tapered access line is also incorporated into the model. As an example, the DC-blocking capacitors are connected to transmission lines at both terminals. Their EM model therefore includes the vias connecting the capacitor to TopMetal 2 as well as the tapers required to match the transmission-line width, as shown in Figure 4.15. This approach allows the transmission-line lengths to be optimized at the schematic level while accounting for the parasitic effects introduced by the vias and tapers.

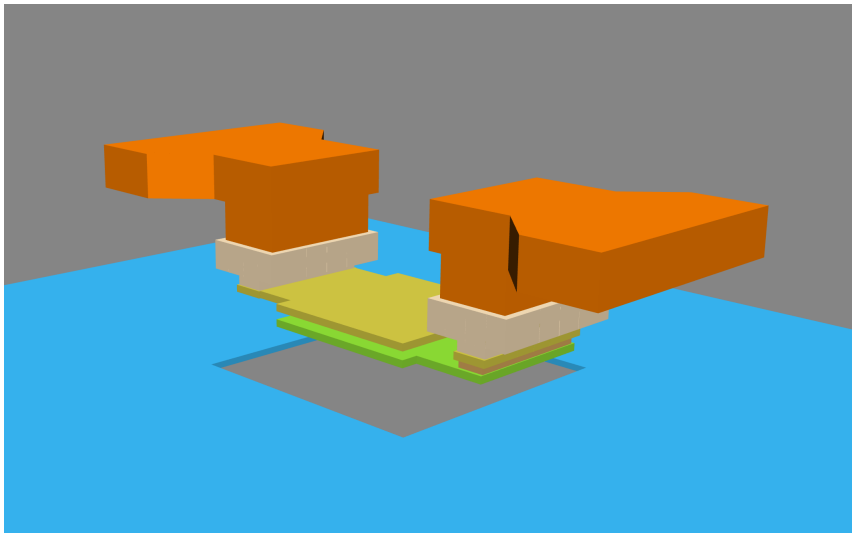


Figure 4.15: 3D view of the simulated DC-blocking capacitor, including vias, tapering and access line

T-junctions are required to connect a stub to series transmission lines, and since they introduce both capacitive and inductive parasitics [11], a schematic model is needed to account for these effects. The PDK provides both a width-scalable layout and a corresponding schematic model for the T-junction. However, as mentioned previously, the latter does not provide sufficiently accurate results. Its accuracy was assessed by comparing simulations of the T-junction model connected to transmission-line models with EM simulations of the corresponding complete structure. The T-junction was subsequently EM-simulated as a standalone structure using the layout provided in the PDK, consisting of three 24 μm-long microstrip legs. Applying the same validation procedure, the EM-

extracted model provided accurate results. That is, simulating the EM-extracted model of the T-junction connected to transmission-line models yielded compatible results with the EM-simulation of the corresponding complete structure.

The RF GSG pads at the input and output ports also introduce parasitic inductance and capacitance which must be modeled. The size and pitch of the pads were selected according to the probing equipment available at the facility where the fabricated chip will be tested. Each pad measures 30 μm $\times$ 30 μm, and the center-to-center pitch between the signal and ground pads is 50 μm. Because the probe tip is smaller than the pad, the EM simulation ports on the signal pad and on the two ground pads are defined each as a 12 μm $\times$ 12 μm square. The extracted model for the pads includes the vias connecting the two ground pads to Metal 1 and a tapered access line connected to the signal pad, as shown in Figure 4.16.

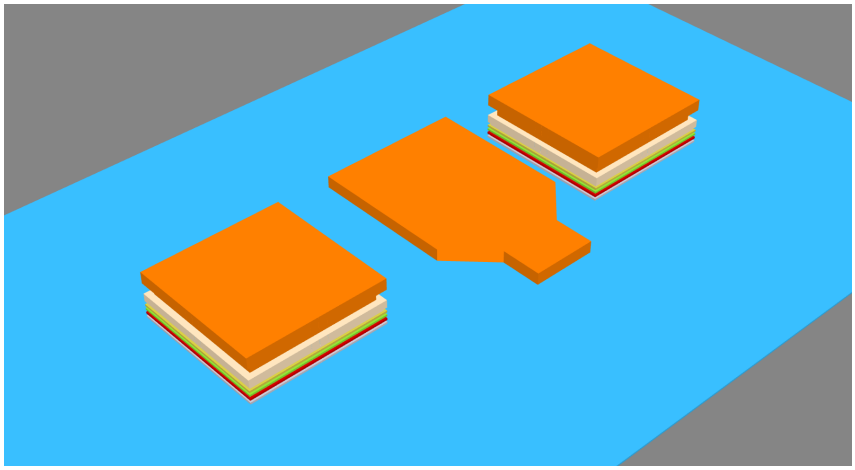


Figure 4.16: 3D view of the simulated GSG Pads, including vias, tapering and access line

The schematic used to optimize the matching networks is shown in Figure 4.17. With the exception of the transistors, all components enclosed by dashed outlines represent models extracted from EM simulations. All ground connections denote vias to Metal 1.

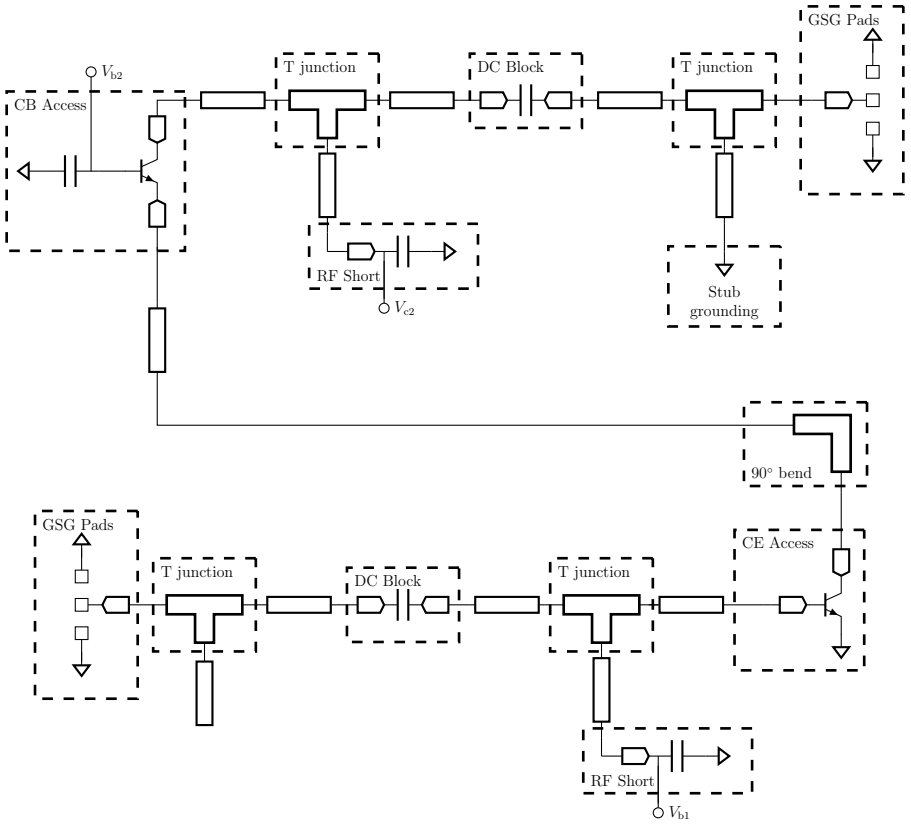


Figure 4.17: Schematic used for matching-networks optimization

The optimization procedure was performed starting from an initial set of transmission-line lengths, which are not the values obtained using the Smith-chart tool due to the presence of the component modelling the T-junctions and of the access lines included in each EM-extracted model. The access lines included in the models of the capacitors, stub grounding, and GSG pads are all 5 μm long. T-junctions, on the other hand, can be modeled using two series transmission lines with a stub in between, with equivalent lengths derived in the following.

The equivalent model for the T-junction was derived from the simulated impedances between the ports. Using the port numbering shown in Figure 4.18, the impedance between Ports 1 and 2 was found to be equivalent to a 60 μm transmission line, while the impedance between Ports 1 and 3, equal to that between Ports 2 and 3 by symmetry, corresponded to a 49 μm transmission line. The resulting equivalent circuit therefore consists of two 30 μm series transmission lines and a 19 μm shunt stub, obtained as 49 μm $-$ 30 μm.

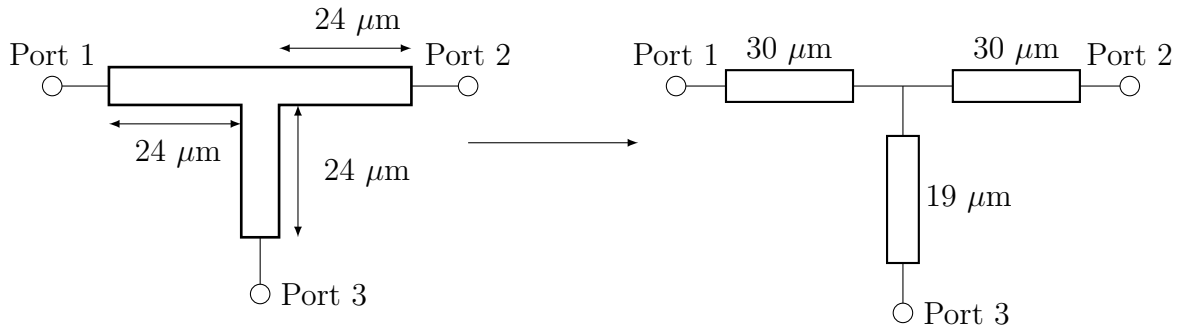


Figure 4.18: Equivalent model for the transmission line T junction

Starting from the lengths determined using the Smith-chart tool, the lengths assigned to the scalable transmission-line sections in the schematic are obtained by subtracting the equivalent lengths included in the junction models. Similarly, if the opposite end of a transmission line is connected to a component model that includes an access line, the length of that access line must also be subtracted. It follows that the initial length found on the Smith-chart tool for a series line or stub could be shorter than the lengths included already in the component models.

The shortest series line or stub that can be modeled using this methodology is obtained by connecting two EM-extracted component models directly, without an intermediate scalable transmission-line section. In this case, the effective length is determined solely by the access lines included in the component models. Consequently, the sum of the equivalent T-junction length and the access-line length of the adjoining component defines the minimum realizable series-line or stub length within the described schematic-level optimization method. As an example, a short-circuited stub cannot be shorter than 24 μm, as this length is already included in the models of the T-junction and of the connection to the Metal 1 ground plane. Matching network topologies requiring shorter transmission lines can still be implemented, but their evaluation requires an EM simulation of the complete structure, resulting in a considerably higher computational cost.

The transmission-line lengths obtained from the Smith-chart design are all above the minimum values described above. Therefore, the selected matching-network topologies could be directly optimized using the combination of EM-extracted component models and scalable transmission-line sections. The resulting layouts of the OMN and IMN, including the RF pads, are shown in Figures 4.19 and 4.20, respectively.

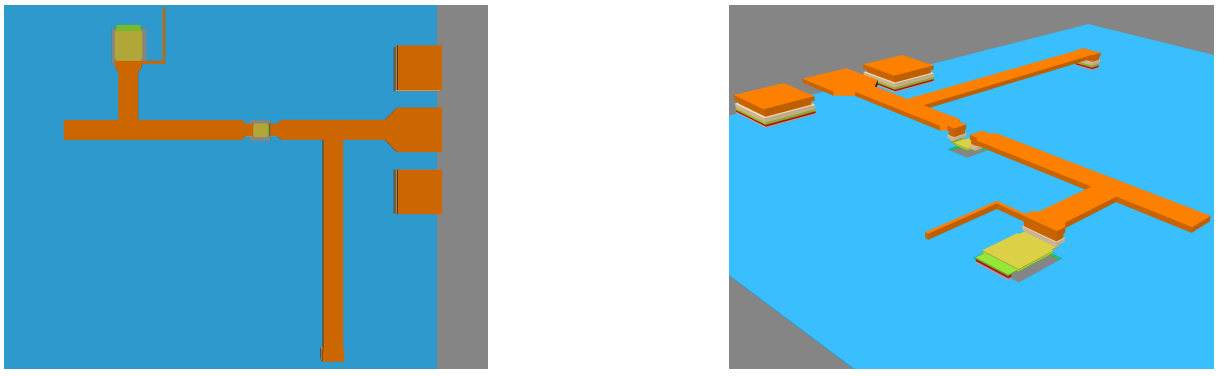


Figure 4.19: 3D views of the OMN layout

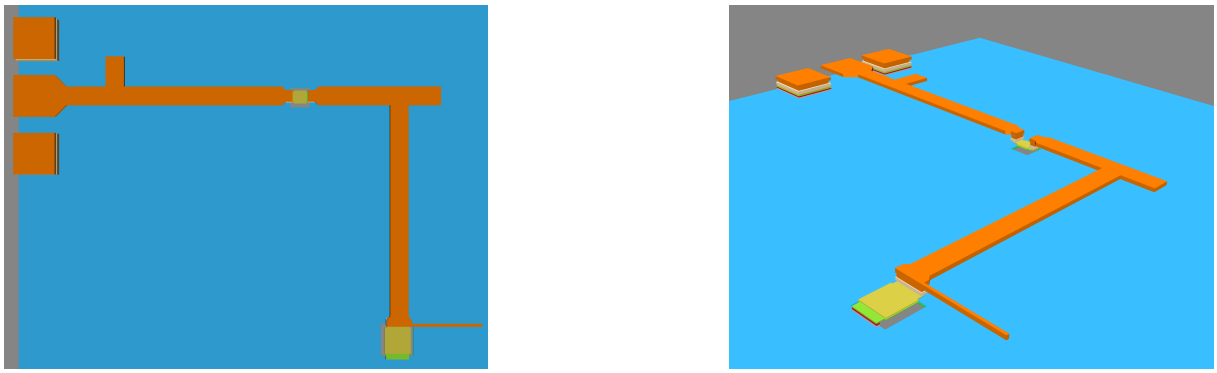


Figure 4.20: 3D views of the IMN layout

The layout of the amplifier core connected to the two matching networks, which is used for preliminary simulations, is shown in Figure 4.21

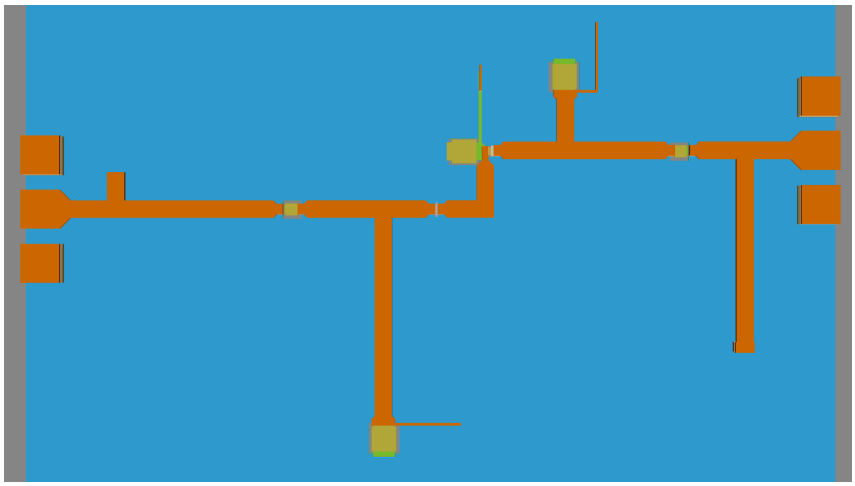


Figure 4.21: Top view of the amplifier's core and matching networks layout

4.7 Bias network

Because of the positions of the transistor bases, the initial bias network described in Section 4.4 would require long bias lines routed beneath the transmission lines of either the input or OMN, which might result in undesired electromagnetic coupling. Moreover, generating both base bias voltages from a single branch would prevent them from being adjusted independently through external bias sources if necessary. To avoid these issues, the branch that generates the two base voltages is divided into two separate branches. The first contains only the current-mirror transistor, whereas the second contains two stacked diode-connected transistors and a resistor, R_{bias} (see Figure 4.23). Because the collector current of the amplifier transistors affects every aspect of the performance of the amplifier, it must be set precisely. A reference current source is therefore used to establish the base voltage of the CE transistor through the current mirror. Since the bias current of the cascode is set through the CE transistor, the base voltage of the CB transistor does not require the same precision. Therefore, rather than using a dedicated current source, the current in the second branch can be derived from the supply voltage through an additional resistor, R_{ref} (see Figure 4.23). By selecting R_{ref} to produce the

same nominal current as the first branch, the second branch can be fed either from the supply voltage or by the same reference current source used for the first branch.

In its nominal configuration, the amplifier requires only one supply voltage and one reference current. However, additional voltage or current sources can be used if independent control of the two base voltages and the collector voltage of the CB transistor is required. With a reference current of 2.5 mA and a supply voltage of 2.4 V, the collector current of the CE transistor is 11.01 mA, while the base and collector voltages of the CB transistor are 2.15 V and 2.38 V, respectively. The total DC power consumption is 34.98 mW.

The DC pads have the same dimensions as the RF pads, 30 μm × 30 μm, but use a larger pitch of 100 μm. To suppress potential fluctuations on the bias lines, which might lead to the build-up of unwanted oscillations, a large decoupling capacitor is connected in shunt to each bias pad. Each capacitor has a small resistor connected in series to improve the attenuation of such oscillations [32]. Schematic simulations without these series RC networks show an out-of-band peak in the transducer gain at 63 GHz. The decoupling networks reduce this peak by 3 dB and shift it to 65 GHz, as shown in Figure 4.22.

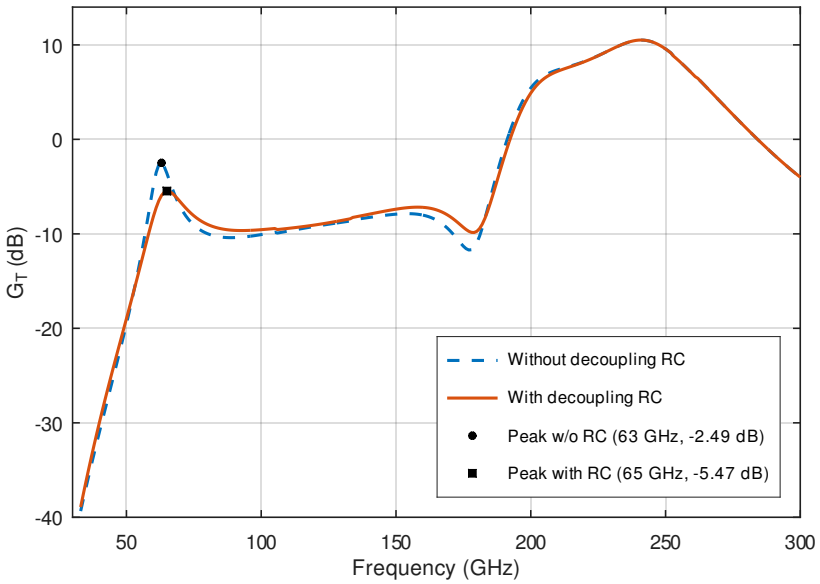


Figure 4.22: Effect of the RC decoupling on G_T

Because all the bias and decoupling resistors have relatively low values, with a maximum of 136 Ω, they are implemented using silicided n+ polysilicon, which provides the lowest available sheet resistance among the resistors included in the PDK. This choice requires the highest resistor length for a given resistance, thereby reducing the relative impact of length variations introduced during fabrication. The resistor widths are selected to withstand the worst-case current obtained at an input power of 3 dBm, which is 10 dB above the input-referred 1-dB compression point. Similarly, the widths of the bias network conductors are selected to satisfy the current-density limits and prevent electromigration.

Because the decoupling capacitors operate at low frequencies, their self-resonant frequency is not a limiting factor. Therefore, the high cap-density MIM capacitors from

the PDK are selected. The final bias network schematic is shown in Figure 4.23. The final schematic simulations, used for comparison with the EM simulations of the complete layout, incorporate this bias network into the circuit shown in Figure 4.17.

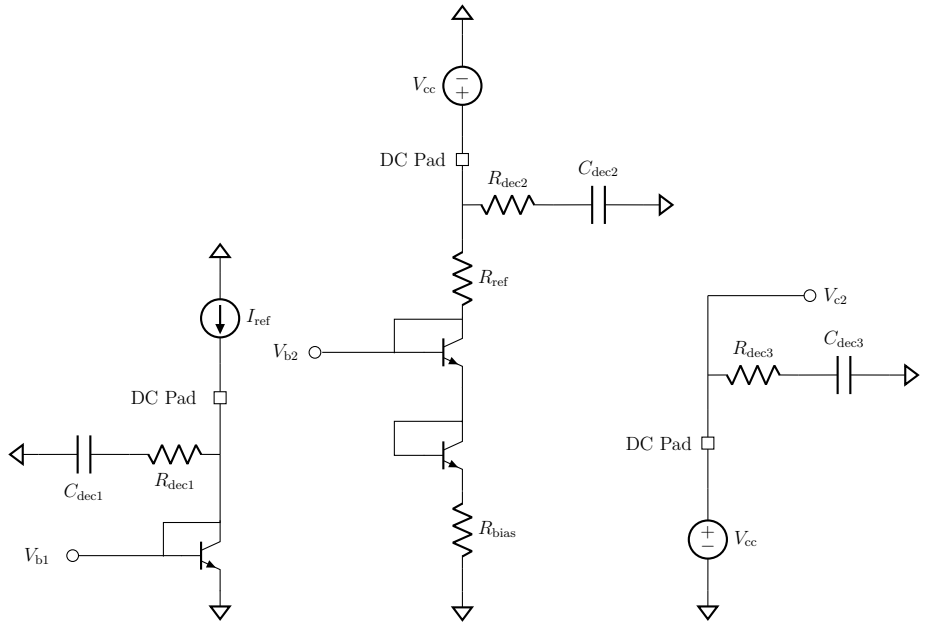


Figure 4.23: Final bias network schematic

4.8 Schematic model validation

The density design rules require large, uninterrupted metal areas to contain openings referred to as *slits*. Slits are already included in the scalable transmission-line layouts, and similar openings are manually placed near junctions, bends, capacitors, and transistors where required. These manually placed slits are included in the EM simulation of the complete layout. A denser array of slits is generated automatically throughout the remainder of the ground plane. Each automatically generated slit measures 2.8 μm $\times$ 2.8 μm, with an edge-to-edge spacing of 6 μm. At $f_0 = 240$ GHz, using the effective dielectric constant ε_{eff} of the TM2-M1 transmission line calculated in Chapter 3, the guided wavelength is

$$\lambda_{\text{g}} = \frac{\lambda_0}{\sqrt{\varepsilon_{\text{eff}}}} = \frac{c}{f_0\sqrt{\varepsilon_{\text{eff}}}} = 671.52\ \mu\text{m}. \tag{4.4}$$

Because the automatically generated slits are electrically small relative to the guided wavelength and are distant from the RF structures, they are not expected to significantly affect circuit performance. However, including them would substantially increase simulation complexity and computation time. They are therefore omitted from the EM model and included only in the final prototype layout.

The minimum-density design rules are satisfied by adding *fill*, consisting of floating metal, polysilicon and diffusion structures. Fill is excluded from the regions surrounding the RF structures and is therefore omitted from the EM simulation. The final layout used for the EM simulation, including the bias network, is shown in Figure 4.24. As discussed in Section 3.3, the EM simulations include only structures implemented using the metal

layers. The transistors and polysilicon resistors are therefore excluded from the simulation and are not present in Figure 4.24.

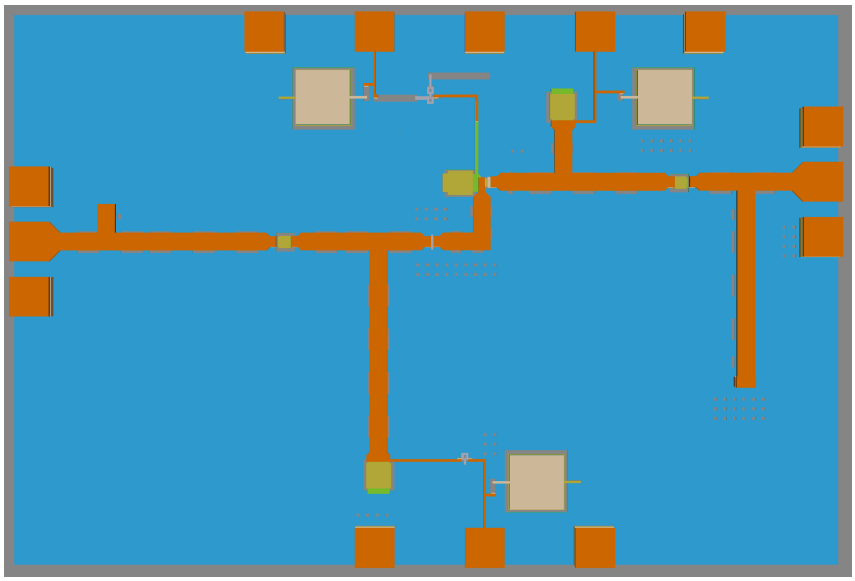


Figure 4.24: Top view of the layout used for the EM simulation

The final schematic and EM simulations are performed with a reference current of 2.5 mA, which establishes the base voltage of the CE transistor, and a supply voltage of 2.4 V, which establishes the base and collector voltages of the CB transistor. As shown in Table 4.6, the schematic and EM simulation results are in close agreement in terms of noise figure and transducer gain. This result supports the effectiveness of combining individually-extracted EM models and the scalable PDK transmission-line model to perform parametric optimization at a schematic level, while still accounting for layout parasitics.

At the center frequency, the EM simulation predicts a significantly lower S_{11}; however, the discrepancy decreases across the remainder of the frequency band of interest, as shown in Figure 4.26. The EM simulation also predicts a wider BW and a flatter transducer-gain response, as shown in Figure 4.25. The difference in BW is partly attributable to the lower peak transducer gain predicted by the EM simulation, which reduces the gain level defining the 3-dB bandwidth and therefore shifts the corresponding band edges farther apart.

Parameter	**Schematic simulation**	**EM simulation**
NF [dB] @ f_0	5.83	5.88
G_T [dB] @ f_0	10.50	10.01
S_{11} [dB] @ f_0	-24.08	-47.14
S_{22} [dB] @ f_0	-19.06	-17.13
BW [GHz]	45 (213–258)	56 (205–261)

Table 4.6: Comparison between schematic and EM simulation results

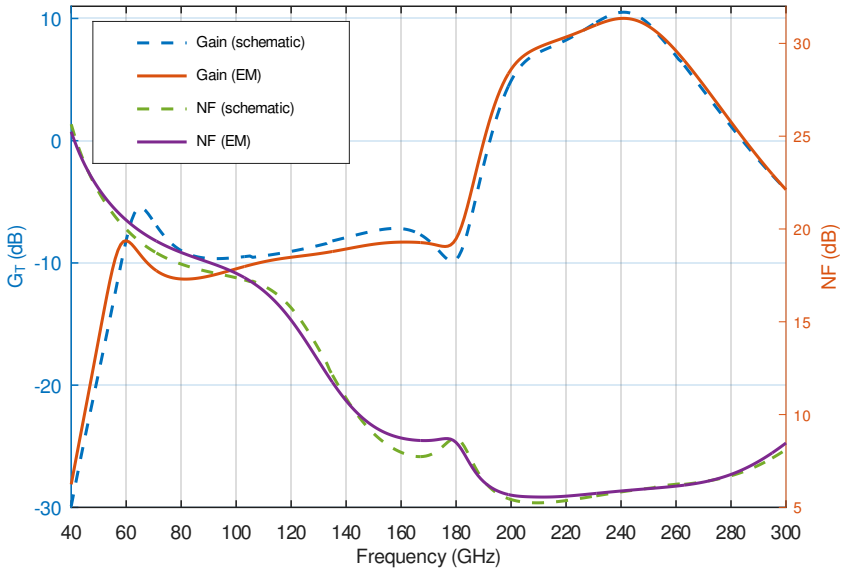


Figure 4.25: Comparison of G_{T} and NF obtained from schematic and EM simulations

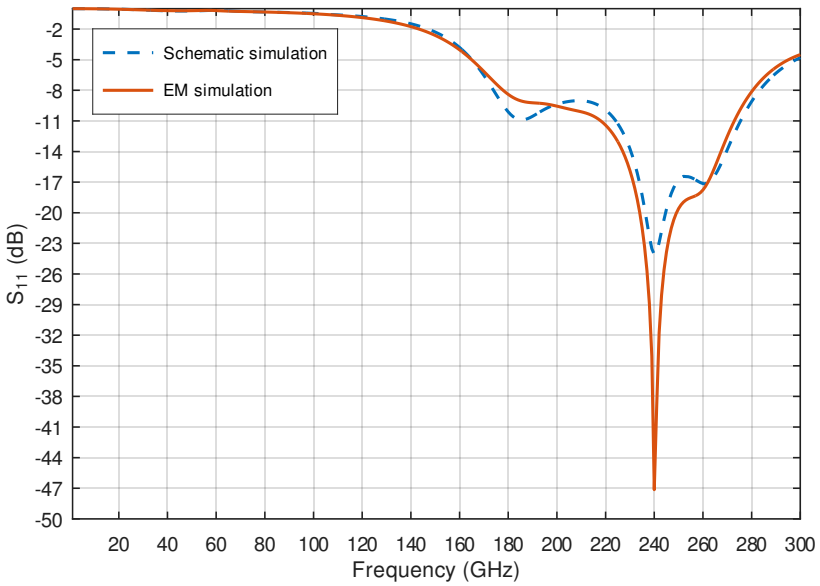


Figure 4.26: Comparison of S_{11} obtained from schematic and EM simulations

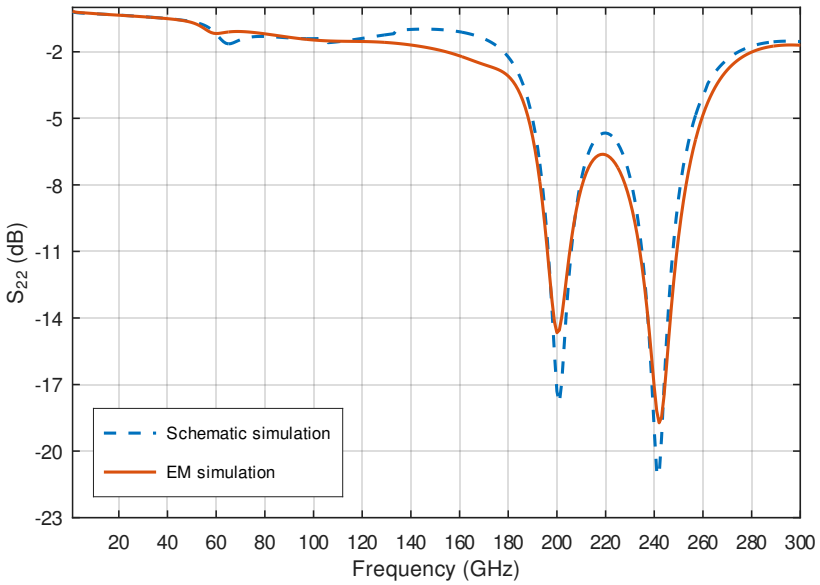


Figure 4.27: Comparison of S_{22} obtained from schematic and EM simulations

Chapter 5

LNA prototype implementation and verification

5.1 Introduction

This chapter presents the performance of the post-layout LNA resulting from the design process described in Chapter 4. The small-signal performance, including transducer gain, bandwidth, noise figure, and input and output matching, was previously presented in Section 4.8 to assess the agreement between the final schematic simulation and the full-layout EM simulation. Here, the small-signal performance of the final post-layout design is examined in greater detail. The large-signal behavior is then investigated through gain compression and third-order intermodulation analysis. The stability of the complete amplifier is subsequently assessed under small- and large-signal operating conditions, including the effect of possible impedances connected to the DC pads. The final prototype submitted for production is also described, and the performance of the proposed amplifier is compared with that of previously reported sub-THz HBT-based LNAs using the relevant performance metrics and a figure of merit.

5.2 Post-layout verification

The final performance of the amplifier is evaluated using the full layout EM simulation described in Section 4.8. While the design and optimization process relied on EM-extracted models of individual passive components and interconnections, the complete-layout simulation includes all the metal structures present in the final prototype and their electromagnetic interactions. This allows the impact of the physical implementation on the amplifier performance to be assessed prior to fabrication. The following sections investigate the small-signal, large-signal, and stability performance of the resulting post-layout design.

5.2.1 Small-signal analysis

The transducer gain is shown in Figure 5.1. It reaches a maximum of 10.01 dB at 241 GHz. The 3-dB BW extends from 205 GHz to 261.3 GHz, corresponding to a total BW of 56.3 GHz.

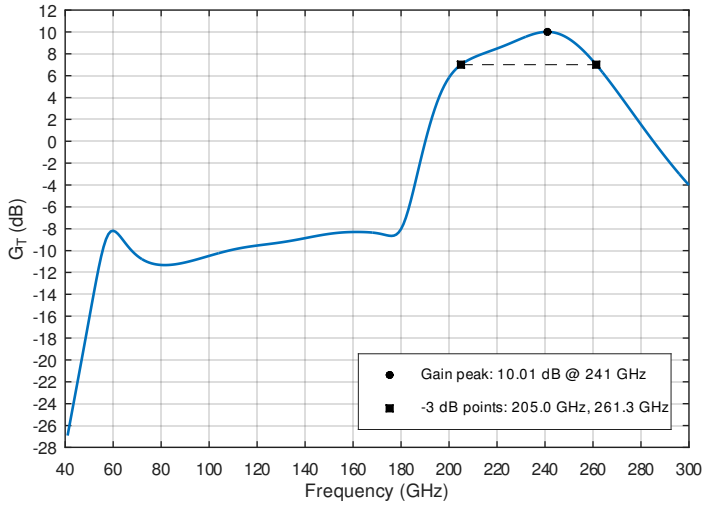


Figure 5.1: G_{T} as a function of frequency

As mentioned in Chapter 1, the range resolution ΔR of an FMCW radar is inversely proportional to the transmitted chirp bandwidth. In particular:

$$\Delta R = \frac{c}{2B_{\mathrm{chirp}}}, \tag{5.1}$$

where c is the speed of light and B_{chirp} is the frequency-sweep bandwidth. Although the range resolution is fundamentally determined by the transmitted waveform, the receiver front-end must provide sufficient bandwidth to amplify the entire received chirp. Assuming a modulation BW equal to the simulated 3-dB gain BW of 56.3 GHz and sufficient bandwidth in the remaining receiver stages, the corresponding range resolution would be approximately 2.7 mm.

The noise figure is shown in Figure 5.2. It is 5.88 dB at 240 GHz, while its maximum value within the 3-dB gain BW is 6.2 dB at 261.3 GHz.

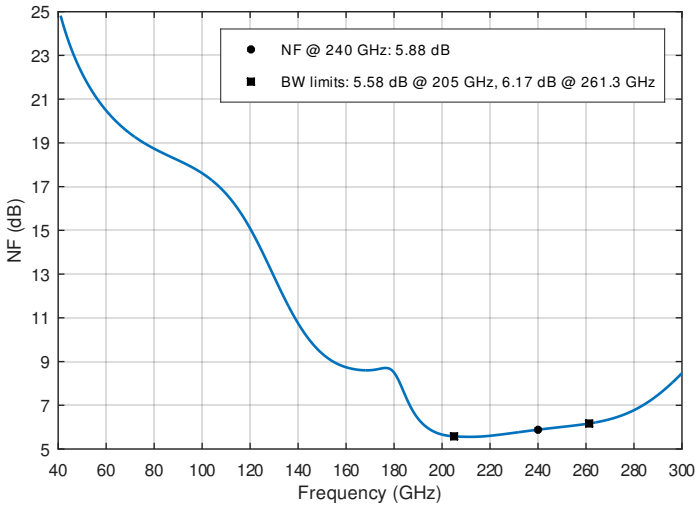


Figure 5.2: Noise figure as a function of frequency

The input and output reflection coefficients, S_{11} and S_{22}, are shown in Figure 5.3. At 240 GHz, they are -47.14 dB and -17.13 dB, respectively. Throughout the BW of interest, S_{11} remains below approximately -10 dB, while S_{22} remains below -5 dB.

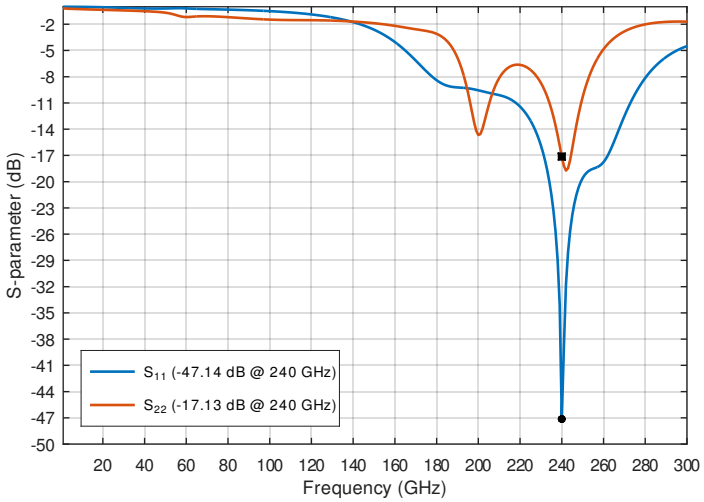


Figure 5.3: Input and output reflection coefficients as a function of frequency

5.2.2 Large-signal analysis

Since an LNA is primarily intended to amplify low-power signals, gain and noise figure are generally prioritized over large-signal linearity during the design process. Therefore, linearity was not considered a primary design criterion in the optimization and is evaluated here as part of the post-layout verification of the final amplifier. Linearity was evaluated using harmonic-balance analysis, with single-tone simulations used to characterize gain compression and two-tone simulations used to evaluate third-order intermodulation products. The output power as a function of input power is shown in Figure 5.4. The IP_{1dB} and OP_{1dB} are -6.8 dBm and 1.8 dBm, respectively.

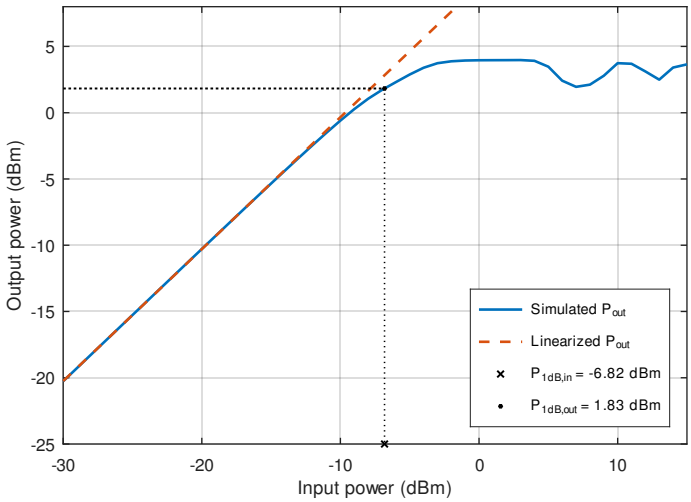


Figure 5.4: Output power as a function of input power

To determine the IIP3, two closely spaced, equal-power tones at $f_1 = 239.5$ GHz and $f_2 = 240.5$ GHz were applied to the input of the LNA. Each tone had a power of -33 dBm, corresponding to a combined input power of -30 dBm. This level is significantly below the input-referred 1 dB compression point, ensuring operation in the approximately linear region. The third-order intermodulation product was evaluated at $f_{\mathrm{IM3}} = 2f_2 - f_1 = 2(240.5\ \mathrm{GHz}) - 239.5\ \mathrm{GHz} = 241.5\ \mathrm{GHz}$. The tone spacing was selected to minimize variations in amplifier gain among f_1, f_2, $2f_2 - f_1$, and $2f_1 - f_2$. The four tones are confined to the frequency range from 238.5 GHz to 241.5 GHz, corresponding to a total span of only 3 GHz, which is significantly narrower than the amplifier's 56 GHz gain bandwidth. Therefore, the gain can be considered approximately constant across the four frequencies.

As shown in Figure 5.5, the simulated IIP3 is 2.45 dBm. The analytical approximation described in Section 2.6 predicts that the IIP3 is about 9.6 dB above the input-referred 1-dB compression point. The simulated difference is 9.3 dB, in good agreement with this prediction.

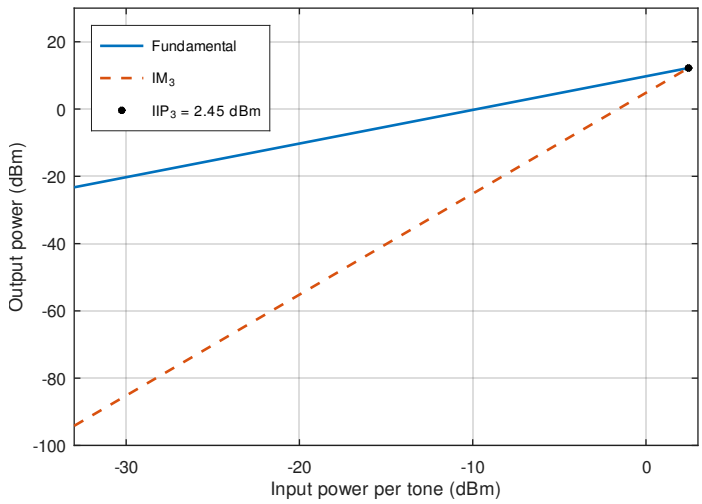


Figure 5.5: Output power at the fundamental and at the IM3 as a function of the input power per tone, with the extrapolated IIP3

5.2.3 Stability analysis

The amplifier's stability was evaluated under both small-signal and large-signal operating conditions. Small-signal stability was assessed using the μ factor, whereas stability under large-signal excitation was evaluated through pulse-response and harmonic-balance analyses. Finally, stability robustness was assessed by sweeping the values of series and parallel impedances connected to the DC pads.

As described in Section 2.3, the μ factor provides a single-parameter sufficient condition for unconditional small-signal stability. This criterion assumes, however, that the network can be represented as a two-port and that its scattering parameters are free of right-half-plane poles [10]. Accordingly, the μ factor was used primarily during the design phase, while additional analyses and supply-impedance sweeps were performed to assess

the stability of the complete amplifier.

As shown in Figure 5.6, μ remains greater than unity throughout the simulated frequency range from 1 GHz to 300 GHz. Under the aforementioned assumptions, this result indicates unconditional stability across the entire frequency range.

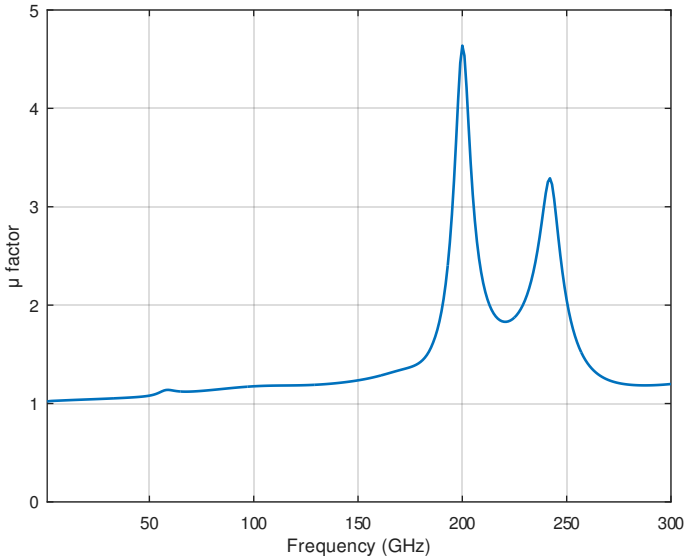


Figure 5.6: Stability factor μ as a function of frequency

The harmonic-balance stability analysis provided by the SpectreRF simulator evaluates circuit stability using loop gain. Although the designed amplifier does not contain intentional feedback loops, parasitic feedback paths may be present, and their loop gain can reveal potential sources of instability. In this analysis the circuit is linearized about a periodically varying operating point rather than a static DC operating point. It therefore accounts for the time-varying operating conditions produced by a large-signal input [33].

The loop gain was evaluated using a current probe inserted at each terminal of the cascode transistors to identify potential unintended feedback paths. Each loop-gain response was simulated over frequencies from 1 GHz to 300 GHz and input power levels from -30 dBm to 3 dBm, with the upper limit corresponding to 10 dB above the input-referred 1-dB compression point. The highest loop gain, shown in Figure 5.7, was obtained with the probe at the emitter of the common-base transistor. However, its magnitude remained below 0 dB for all the simulated frequencies and input power levels; therefore, none of the unintended feedback paths can satisfy the Barkhausen criterion, regardless of phase.

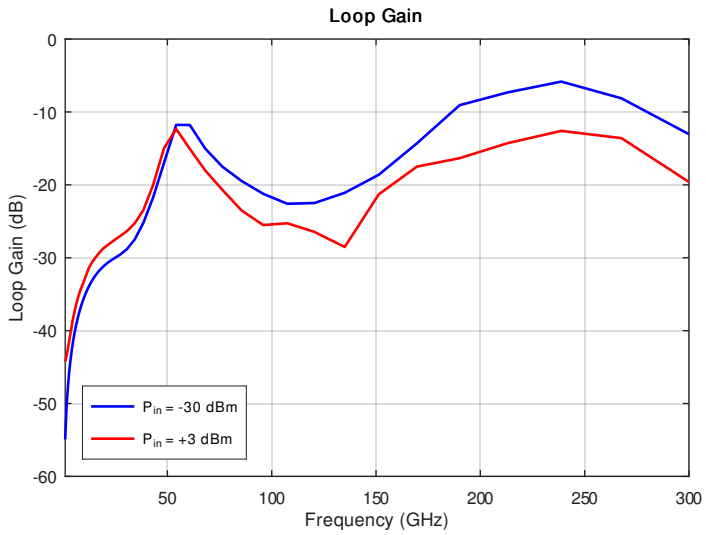
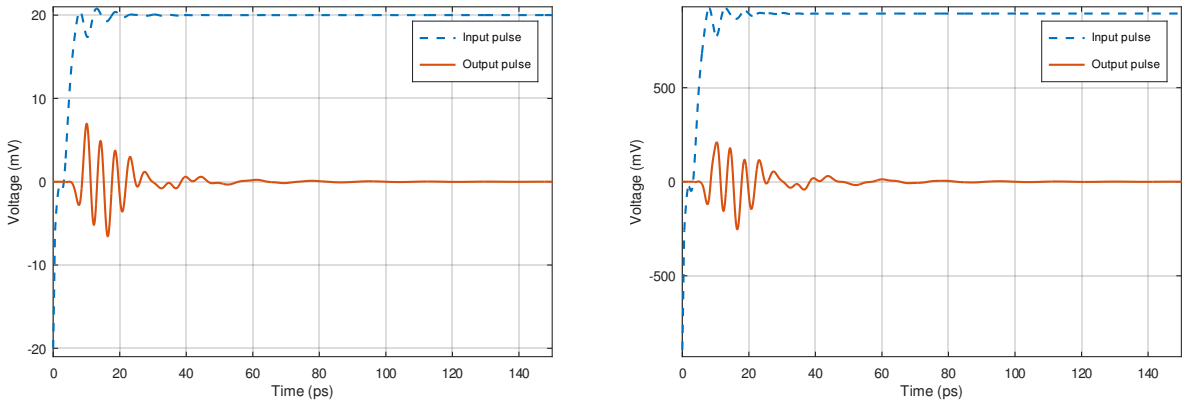


Figure 5.7: Loop gain with the current probe connected to the emitter terminal of the CB stage

The pulse response was tested using two input transitions, one below and one above the input-referred 1-dB compression point: from −10 mV to 10 mV, corresponding to −30 dBm for a 50 Ω source, and from −447 mV to 447 mV, corresponding to 3 dBm. In both cases, the rise time was 500 fs, introducing spectral content at frequencies up to approximately 2 THz. As shown in Figures 5.8a and 5.8b, the resulting input and output waveforms exhibit no self-sustained oscillations in either case. The voltage pulse at the amplifier input differs from the waveform generated by the source because the broadband pulse contains substantial frequency content outside the input-matching BW, resulting in significant reflections.



(a) Input power of −30 dBm

(b) Input power of 3 dBm

Figure 5.8: Pulse response below and above the input-referred 1 dB compression point

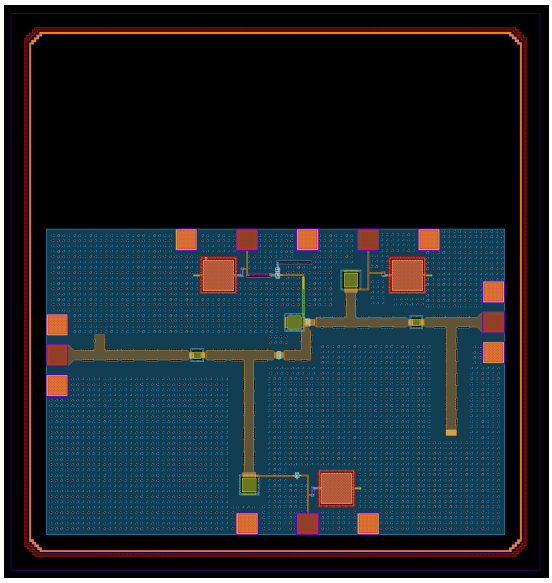
To evaluate stability robustness, series and parallel impedances were connected to the DC pads, and their component values were swept to identify potential instabilities. First, a series RL network was inserted at each pad, with R varied from 0.1 Ω to 50 Ω and L

from 1 pH to 500 pH. A series RC branch was then connected in parallel at each pad, with R varied over the same range and C from 1 fF to 1 pF. The amplifier remained unconditionally stable for all simulated values.

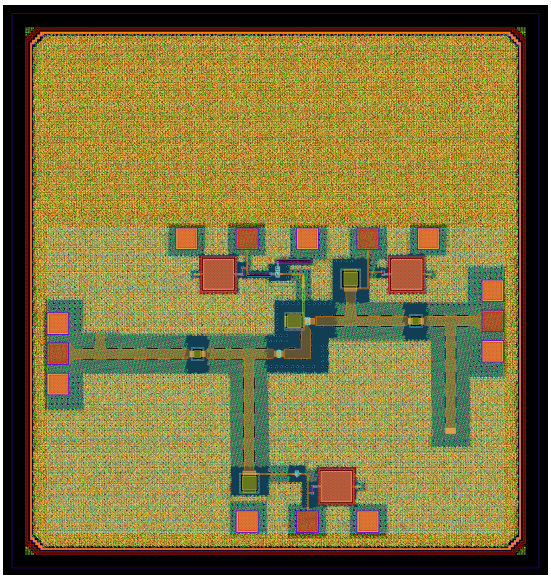
5.3 Final prototype implementation

As mentioned in Section 4.8, the density design rules require *slits* in large, uninterrupted metal areas and the addition of *fill*. All types of fill are excluded from the areas close to transistors, resistors and capacitors, while all the metal fills are excluded from the areas close to transmission lines and pads. The chip must also be enclosed by a *seal ring*, a continuous metal structure placed around its perimeter. The seal ring consists of multiple metal layers connected by arrays of vias. Its primary function is to improve the mechanical robustness of the die by protecting the active circuitry from damage caused during wafer dicing, packaging, and handling. It also acts as a barrier to crack propagation and contamination from the die edges into the active area [34].

Excluding the seal ring, the chip occupies an area of 756 μm $\times$ 504 μm = 0.38 mm^2. The chip is fabricated as part of a multi-project wafer (MPW) run, for which the minimum reservable area is 0.8 mm^2. The seal ring is therefore positioned such that the remaining allocated area can accommodate an unrelated circuit, which is omitted from Figure 5.9. The final prototype layouts without fill and including fill are shown in Figures 5.9a and 5.9b, respectively; the version without fill is included for clarity.



(a) Final prototype without fill



(b) Final prototype including fill

Figure 5.9: Layout of the final prototype

5.4 Comparison with recent literature

Table 5.1 shows a comparison of the amplifier implemented in this work with designs based on HBTs with similar operating frequencies. The LNAs can be compared using the

Figure of Merit (FoM) [28] defined as:

$$\mathrm{FoM}\,[\mathrm{GHz/mW}] = \frac{\mathrm{Gain}\,[\mathrm{dB}] \cdot \mathrm{BW}\,[\mathrm{GHz}]}{(\mathrm{NF}\,[\mathrm{dB}] - 1) \cdot P_{\mathrm{DC}}\,[\mathrm{mW}]}, \tag{5.2}$$

where *Gain* indicates the peak transducer gain.

	This work	[27]	[26]	[35]
Technology	IHP 130-nm SiGe	IHP 130-nm SiGe	IHP 130-nm SiGe	Teledyne 130-nm InP
$f_{\mathrm{T}}/f_{\mathrm{max}}$ [GHz]	470/650	300/450	300/500	500/1000
Circuit topology	Single-ended cascode	Single-ended cascode	Single-ended cascode	Single-ended common emitter
Stages	1	1	7	5
f_0 [GHz]	240	235	240	212
NF [dB] @ f_0	5.9 (sim.)	11 (meas.)	13.7 (sim.)	5.3 (meas.)
Gain per stage [dB] @ f_0	10.0 (sim.)	7.8 (meas.)	4.1 (meas.)	3.1 (meas.)
BW [GHz]	56 (sim.)	50 (meas.)	14 (meas.)	50 (meas.)
IP_{1dB} [dBm]	-6.82	-14	-	-
P_{DC} per stage [mW]	35	18	13.9	1.5
Area [mm^2]	0.38	0.07	0.45	0.25
FoM [GHz/mW]	3.3	2.2	0.33	24

Table 5.1: Comparison of HBT-based sub-THz LNAs reported in the literature

The amplifier reported in [27] provides the most meaningful comparison in terms of process advancements because, like the amplifier presented in this work, it employs a single-stage cascode architecture and has a similar center frequency, but it was implemented in IHP's SG13G2 technology. This is an earlier generation of the process described in Section 3.2, with lower f_{T} and f_{max}, such that the amplifier is operating beyond $f_{\mathrm{max}}/2$. For the sake of the comparison it should be noted that the noise-figure, gain, and bandwidth results reported in [27] are measured, whereas those presented in this work are simulated. The post-layout simulations of the proposed amplifier predict higher gain, a significantly lower noise figure, wider bandwidth, and improved linearity. Conversely, the amplifier reported in [27] occupies a significantly smaller area and consumes less power. As discussed in Section 4.4, a higher power consumption of the proposed amplifier was accepted to improve both gain and bandwidth; therefore, the improvements in those regards cannot be attributed solely to advances in the fabrication process. Regarding the noise figure, the author states that to maintain sufficient gain while operating beyond $f_{\mathrm{max}}/2$, the transistors are biased at the collector current corresponding to the peak f_{max}, as opposed to biasing them for the minimum $\mathrm{NF}_{\mathrm{min}}$ [27]. With the higher f_{max} provided by the latest generation, this compromise is not needed, and the transistors can be biased for the minimum $\mathrm{NF}_{\mathrm{min}}$. The increase in f_{T} provides a further reduction of $\mathrm{NF}_{\mathrm{min}}$, resulting in a significantly lower noise figure for the proposed amplifier.

The amplifier reported in [35] illustrates the performance advantage offered by an InP HBT technology, which provides a similar f_{T} but a significantly higher f_{max} than the SiGe technology used for the proposed amplifier. Operating farther from the transistor's limits, sufficient gain can be achieved with a CE topology, which provides the lowest intrinsic noise figure, as discussed in Section 4.3. While it must be noted that its operating frequency is lower than those of the other amplifiers, it achieves the lowest reported noise figure and per-stage power consumption, resulting in a particularly high figure of merit.

Although the per-stage power consumption of the proposed amplifier is significantly higher than those reported in [27] and [26], the post-layout simulations indicate that the proposed amplifier provides the highest FoM among the SiGe-based designs, primarily due to its low noise figure and wide bandwidth. The multistage amplifier reported in [26] achieves higher overall gain, whereas the proposed single-stage amplifier provides a higher gain per stage.

Chapter 6

Conclusions

This work presented the design of a 240-GHz LNA with potential applications including the receiver front-ends of FMCW radars for high-resolution remote sensing. The amplifier is implemented in IHP's SG13G3 technology, which features state-of-the-art SiGe HBTs with $f_T/f_{max} = 470/650$ GHz, enabling sub-THz operation with favorable gain and noise performance. The circuit topology, transistor dimensions, and bias current were selected to provide a suitable trade-off between gain and noise figure. The transmission-line configurations provided by the foundry were compared to identify the one with the highest quality factor, and custom capacitors were designed to overcome the SRF limitations of those included in the PDK. The selected transmission lines and capacitors were then used to implement the distributed matching networks, which embed the bias-Ts and account for the parasitic impedances of the interconnections and RF GSG pads.

All passive components and interconnections implemented using the metal layers were characterized through EM simulations to account for conductor losses, electromagnetic coupling, parasitic effects, and radiation. During the optimization of the matching networks, individually extracted EM models were used in conjunction with the scalable transmission-line model provided by the PDK. This approach enabled efficient schematic-level optimization while accounting for most layout parasitics, as demonstrated by the close agreement between the final schematic-level and complete-layout EM simulation results.

The stability of the amplifier was verified in both small-signal and large-signal conditions, testing also its robustness to the presence of parasitic impedances at the DC pads. The post-layout simulations include small-signal and large-signal analyses, to verify the amplifier's transducer gain, bandwidth, noise figure, linearity and DC power consumption. The results were compared to similar designs reported in the literature. In particular, comparison with an amplifier implemented in an earlier generation of the same technology provided useful insight into the impact of process improvements on amplifier performance. Comparison with an InP-based amplifier, on the other hand, highlighted the performance advantage offered by a III-V compound technology at sub-THz frequencies.

The post-layout simulation results obtained in this work suggest that IHP's SG13G3 technology enables the realization of sub-THz LNAs with competitive noise and gain performance even with a single-stage architecture. The final prototype was submitted to IHP for fabrication, enabling future experimental validation of the simulated results.

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