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Layout Design and Characterization of a Scan-Enabled Latch

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Chapter 1

Introduction

In the field of electronic circuits, sequential logic is a critical part of any complex system design. As opposed to combinational logic, whose output is a function of only its inputs, sequential logic relies on both its current inputs and its internal state to determine the output. This kind of logic is the basis of Finite State Machines (FSMs), which are a fundamental block in digital circuitry.

Because they need to retain the current state of the system for it to work, sequential circuits require memory elements to store data. These components are, in their most basic form, bistable circuits that represent a single *bit* of data. Depending on the particular state the circuit is in, the element can represent either a logical `1` or `0`.

The most basic memory elements present in a sequential circuit are latches and flip-flops (FFs). At their core, these simple elements are designed to store and read information given to them in the form of a feedback loop that maintains a stable voltage state.

A Set-Reset latch, also known as an SR latch, can be made by connecting two NOR gates in a cross-feedback loop. One input, known as the set control, raises the output of the latch to `1` when high while the second input, called reset control, lowers the output to zero when high.

Components of this kind are highly responsive, but they may encounter issues regarding data stability and timing conditions: variance in delay across different data paths may cause the input of the latch to vary under the same initial circumstances. This is a huge issue in sequential logic, as the variance may cause the circuit to behave unexpectedly or fail without explanation, due to the latch's lack of synchronization.

A simple solution to this problem is to make the component transparent while storing data, and opaque when the output must be stable regardless of input changes. Two extra logic gates can be added to the initial circuit prevent the data from being stored unless an additional ENABLE input is held high.

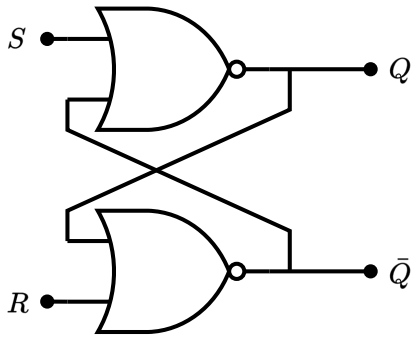


Figure 1.1: SR latch constructed from cross-coupled NOR gates.

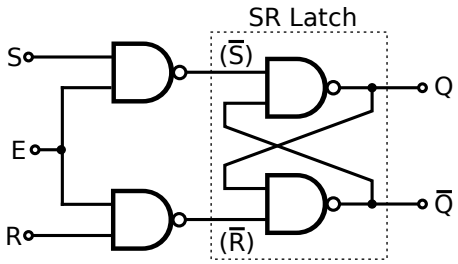


Figure 1.2: NAND gated SR latch.

One final modification can be made to this circuit: by realizing that the active input combinations of the SR latch are `01` and `10`, one can merge the set and reset controls into a single signal. This input, typically known as the DATA input, simplifies the control scheme of the component by reducing the number of input signals required to drive the circuit. It also helps to avoid the invalid `11` set-reset configuration. This type of component is known as a gated data latch, or simply D-latch, and is a crucial component in sequential logic, being a fast, reliable way to store information in a circuit.

One major drawback of this component is that, while the ENABLE signal allows for more precise control of the memory, the component is still transparent during the entire high-level interval. This kind of control is called level-sensitive or level-triggered logic, and it still shares some of the problems of the previous SR latches, namely race-condition and timing issues.

This limitation can be overcome by adopting edge-triggered architecture. Components of this kind store the input data only during a specific transition on the ENABLE input, typically the rising edge of a clock signal. By restricting the data-capture interval, the component becomes more stable and less prone to timing-related issues.

A simple design that accomplishes this goal consists of two D-latch blocks

connected in series driven by complementary ENABLE signals. In this type of design the first latch is responsible for controlling the second latch's input, which in turn changes its state when the clock signal changes. Due to this nature, these latches are usually called master and slave latch, respectively.

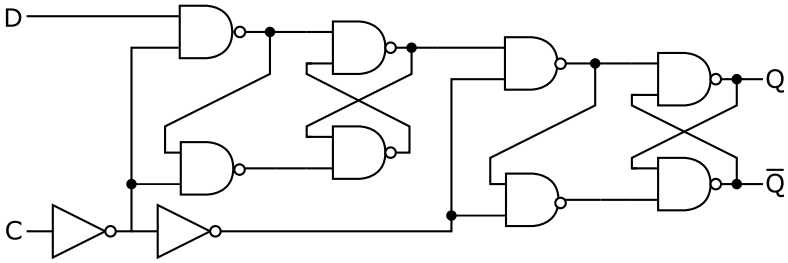


Figure 1.3: Master-slave D flip-flop implementation.

The previously described circuit is called a D-flip flop (D-FF), and it is one of the most common elements in a sequential system. Their simple yet robust response to a clock signal makes them extremely reliable circuits. Being edge-triggered components, they do not need complex clock signals and can efficiently operate with a square-wave clock input.

D-FFs are currently considered the default element when it comes to designing a sequential circuit. However, recent developments in circuit optimization have shed new light on the utility of latches.

Latches possess key advantages when used as sequential elements in a circuit: their timing flexibility makes them ideal candidates for timing optimization, and their simpler design can yield significant area savings.

One notable example of such optimizations at play is known as *time borrowing*. In FF-based designs, paths are strictly limited by the FF timing, meaning any signal has to be setup before the clock edge arrives. This can be a problem for unbalanced designs where some paths are longer than others. In such cases, the clock frequency is forced to match the slowest path unless path balancing is applied.

Latch-based designs on the other hand do not have such *hard edges*, as the latch is transparent during the entire clock half-cycle. This means that a large path can borrow time from a following stage, up to a clock half-cycle, as long as this process does not cause any setup violations [1].

Latch adoption in circuits has also been shown to lower power consumption: studies such as [2], [3] and [4] have successfully reduced the power consumption of several circuits by adopting either a latch-based or mixed design in their workflow.

Research has also been made in latch adoption in error-resilient applications [5] and to increase frequency.

All-in-all, latch-based solutions offer several advantages which make them worthy of consideration in digital design. For this reason, research has been made to offer

optimization flows that convert FF-based circuits into latch-based equivalent designs. The following section is dedicated to highlight a few key advancements in the area.

1.1 Latch-Based Literature

The seminal work of Sakallah et al. [6] offers key solutions for the implementation of latch-based sequential logic. The study first lays out a complete set of timing constraints for latch-controlled digital circuits. These constraints include a series of phase and delay equations and inequalities that govern the latch behavior and exhibit mild nonlinearity. The authors then present a simplified linear programming problem and prove its equivalence to the minimum clock cycle computation for latch-based logic. This enables an LP-based algorithm which successfully optimizes timing requirements of the circuit.

Pulsed-latch solutions such as the one presented by Shin and Paik [7] aim to modify the clock pulse width to achieve a higher degree of timing precision while offering the typical advantages of latch-based designs. The authors evidence that FFs are responsible for a large portion of resources from a conventional Application Specific Integrated Circuit (ASIC), such as clock period, power consumption and total area [8]. To address this, they propose replacing FFs with level-sensitive latches, which offer lower overhead and a smaller footprint compared to FFs, and implementing a dedicated clocking scheme to overcome the timing constraints. The pulse signal is generated from the digital system clock by using specialized circuitry. The main drawback of this solution, however, is that pulse generation circuitry can be highly complex as well as being prone to signal degradation.

Another solution is based on the idea of generating multiple phases starting from an initial clock signal: studies such as the one by Zhang and Calhoun [9] propose a two-phase clocked latch-based method for ultra low power applications, while Fojtik et al. [5] present similar ideas for error detection purposes in an ARM Cortex-M3 processor. These multi-phase timing schemes are possible but their complexity limits their potential application.

1.2 Mix&Latch

Among the proposed latch integration options in the literature, the *Mix&Latch* technique stands out as particularly promising. First introduced by Minella and colleagues, the workflow promises to convert any initial FF-based design into a latch-based circuit.

Compared to other methods, *Mix&Latch* offers several advantages:

- The algorithm does not require a specialized clock scheme. Instead it relies on

a 50% duty cycle single-phase clock, which greatly simplifies the clock signal generation, as well as post-layout evaluations.

- Sequential elements are not moved between the original and the optimized designs. In other words, the algorithm has a 1-to-1 correspondence in sequential elements between the initial design and the final result.

- The implementation is fully based on commercially available tools.

In brief terms, the method works by replacing all sequential elements of the initial design with Positive Triggered Latches (PTLs). This effort ensures that the position and timing of the elements is preserved, and allows for time borrowing application in critical paths. However, the introduction of PTLs may cause hold violations in some paths if their minimum arrival time is lower than the positive pulse width of the clock signal. In these cases, the algorithm places Negative Triggered Latches (NTLs) in the suspected paths to block the signal from creating a race condition. This process is implemented using an Integer Linear Programming (ILP) model which aims to select the optimal positions for the NTL insertion.

With this process, the added NTLs should solve the detected hold violations without a performance penalty. Finally, any found NTL-PTL pairs are merged into Positive-Edge-Triggered flops (PETF) and PTL-NTL pairs are merged into Negative-Edge-Triggered flops (NETF). This is done in order to reduce the total area of the circuit.

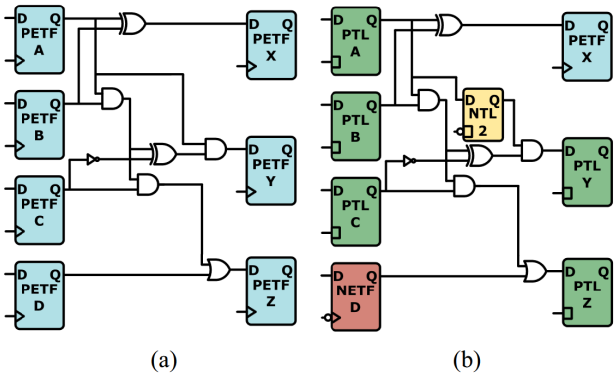


Figure 1.4: Example of *Mix&Latch* optimization on a PETF-based circuit [10].

Initial experiments with benchmark circuits ranging from cryptographic IPs to processor cores showed an average performance increase of 1.33×, with an area increase of only 1.2×. In some edge cases, the total area of the circuit actually decreased compared to the initial design [11].

Subsequent studies on the *Mix&Latch* method yielded successful performance improvements and reduced runtime. This updated and improved flow was then tested in a benchmark RISC-V core as it imposed a stricter set of conditions compared to the previous set of benchmark circuits.

The results obtained were compared with modern retiming schemes, showing a sizable improvement in frequency with the added benefit of comparable power and area, and preserving the original position of the sequential elements [10].

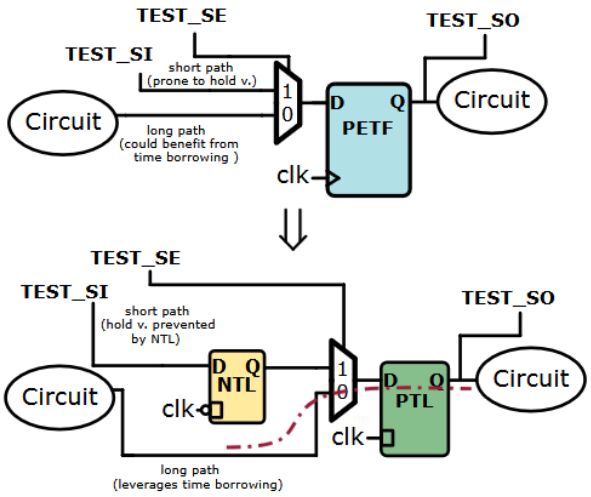


Figure 1.5: Scan Latch structure for Mix&Latch methodology [12].

The next step in the project is aimed at expanding the current Design-For-Testability (DFT) techniques to allow *Mix&Latch* integration during testing and design verification [12].

1.3 Design-For-Testability

DFT has become a fundamental strategy in the digital design space. As modern circuits grow increasingly complex, so do the manufacturing processes. While functional verification consumes a massive portion of the pre-silicon design workflow [13], ensuring the physical integrity of the manufactured chip is equally critical. Any physical defects not caught during post-fabrication testing become exponentially more expensive as the product moves down the supply chain.

Moreover, a significant amount of designs end up behind schedule as a result of incomplete or late send-offs, resulting in increasing costs for the design team.

Looking at these trends, it becomes apparent that verification and testing is

an essential step in the design process. As such, the benefits of implementing testing-friendly workflows and environments are ever so larger.

In this context, DFT emerges as a series of techniques that integrate testing capabilities directly to a design, aiding in the testing of the final product. These techniques span all levels of hardware design, from adding physical probe points on specific nets to including dedicated logical elements to facilitate the system's observability and controllability.

One of the simplest yet most effective methods used for verification is known as a **scan chain**. This technique takes advantage of sequential elements of a circuit by implementing scanning capabilities in the registers of a circuit. This way, one is able to observe and monitor the different stages of the system during testing at any given state. Coupled with an adequate set of test vectors, this technique drastically simplifies testing, speeding up the process and making it more resilient to errors. In this system, memory elements operate in two distinct modes: normal mode and scan mode. The first one corresponds to the regular operating condition of the component while the second one reconfigures the memory elements into a shift register, also called scan chain. Scan capabilities can be added to any sequential element by simply placing a 2-to-1 multiplexer (MUX) at its input. The two MUX inputs, typically called D and Scan Input (SI), handle the regular memory input and the scan chain input respectively, while the selector signal, also known as Scan Enable (SE), controls the operating mode of the element.

Being a powerful, cost-effective technique, scan chain implementation has become an essential part of ASIC and SoC design workflows, and most modern Electronic Design Automation (EDA) tools fully support it.

1.4 Theoretical Framework

1.4.1 MOSFETs

One of the most common components in modern digital circuits is the MOS transistor or MOSFET. Their wide range of uses and ease of integration in silicon-based projects make them one of the most versatile components in all of electronics, ranging from logic gates and memory devices to high-power applications.

There are two main types of MOSFET: n-type transistors (nMOSs) are built on an n-type semiconductor and have heavily p-doped terminals, while p-type transistors (pMOSs) have a p-type semiconductor substrate and n-doped terminals. A typical MOSFET has four terminals: the gate, source, drain and body or bulk nodes. Usually, the bulk node is connected to the source, so the study of the MOS can be simplified to the three former terminals. The gate terminal acts as a control input, depending on its voltage level, it will either allow or block the flow

of electrons from source to drain. The latter connection between the two terminals is usually called channel for this very reason.

In a typical nMOS transistor, current will flow if the gate-source voltage (V_{GS}) reaches a given threshold aptly called threshold voltage (V_{th}). If V_{GS} is higher than the threshold, the nMOS is considered ON, otherwise, it is considered OFF. The case for pMOS transistors is reversed: if V_{GS} sits above the given threshold, the transistor is OFF. If V_{GS} drops below V_{th}, the transistor is ON.

The specific static response of a MOSFET however, is defined by its I-V characteristic, which describes the drain current of the device (I_D) as a function of its terminal voltages V_{GS} and V_{DS}. The first condition, called cutoff mode, happens when V_{GS} is lower than V_{th} and shows no conduction between suorce and drain. After the threshold is exceeded, a channel forms and the device can conduct electrons. At low drain voltages, the MOSFET enters its linear region, where it operates like a resistor controlled by the gate voltage. If V_{DS} surpasses a value known as the saturation voltage of the MOS, defined by the expression $V_{\mathrm{dsat}} = V_{GS} - V_{th}$, the device is pushed into its saturation region, where the current remains constant regardless of the drain voltage.

A simplified model describing a MOSFET's characteristic is shown below:

$$I_D = \begin{cases} 0, & V_{\mathrm{GS}} < V_{\mathrm{th}} \\ \beta \left(V_{\mathrm{dsat}} V_{\mathrm{DS}} - \frac{V_{\mathrm{DS}}^2}{2} \right), & V_{\mathrm{GS}} \geq V_{\mathrm{th}},\ V_{\mathrm{DS}} < V_{\mathrm{dsat}} \\ \frac{1}{2} \beta V_{\mathrm{dsat}}^2, & V_{\mathrm{GS}} \geq V_{\mathrm{th}},\ V_{\mathrm{DS}} \geq V_{\mathrm{dsat}} \end{cases} \tag{1.1}$$

Where $\beta = \mu C_{\mathrm{ox}} W/L$ encapsulates the process and geometric parameters that influence the electrical characteristics of the MOSFET. While the electron mobility μ and the oxide capacity C_{ox} are determined by the manufacturing process and materials, the channel width-to-length ratio $\frac{W}{L}$ is a key parameter set during the design process. This distinction will play a crucial role in later sections of this work.

1.4.2 Logic gates

By placing a single pMOS and an nMOS transistor in a complementary structure, we can create a CMOS inverter, the simplest type of logic gate.

If the input voltage is sufficiently low ($V_{\mathrm{in}} < V_{\mathrm{th,n}}$), the nMOS remains OFF while the pMOS turns ON. Consequently, the pMOS connects the supply voltage (V_{DD}) to the output node, pulling the output HIGH. Conversely, if the input voltage exceeds $V_{\mathrm{DD}} - |V_{\mathrm{th,p}}|$, the pMOS turns OFF while the nMOS turns ON, connecting the output to ground and driving the output LOW.

The described gate thus implements a logical negation, taking a single input value and inverting it as its output.

By plotting V_{out} as a function of V_{in} one obtains the static voltage transfer characteristic of the logic gate. Notably, digital inverters do not behave as ideal, discrete step functions that switch instantaneously at a single threshold; rather, they exhibit a continuous DC transfer characteristic across the full input voltage range.

The crossover point where $V_{\text{out}} = V_{\text{in}}$ is defined as the switching threshold, representing the operating point at which the inverter transitions between logic states. In a balanced gate, this threshold sits exactly at $V_{\text{DD}}/2$, indicating that both the nMOS and pMOS possess equal drive strength ($\beta_n = \beta_p$). If one transistor is sized to have a greater drive strength than the other, the inverter is referred to as a skewed gate. This imbalance shifts the switching threshold away from the midpoint, moving higher toward V_{DD} for a stronger pMOS network, or lower toward ground for a stronger nMOS network.

Thresholds not only define the transition voltage of a given gate, they also control the delays caused by the gate: a balanced gate will, ideally, have the same rising and falling propagation delay ($t_{pLH} = t_{pHL}$). Skewed gates on the other hand will react faster or slower to a transition due to their skew. This results in different propagation delays for rising and falling transitions. This means, for example, that a delay imbalance can be solved by adjusting the beta ratio of one or more logic gates in the path.

1.4.3 Drive Strength

In standard-cell methodology, logic cells and storage elements are usually designed as an array of functionally equivalent yet different layouts. The main distinction between these cells comes in the transistor sizing and the presence of output buffers. Larger transistors are capable of delivering more current to the load at the cost of a larger footprint, while the opposite is true for smaller MOSs.

Standard-cell designers often provide layouts with different sizing for easier path optimization and minimal area usage. This property is called **drive strength** and it is usually represented as a letter 'X' or 'D' followed by the drive strength number. For example, a D2 cell will be larger in size than an equivalent D1 cell.

1.5 Goal

The primary goal of this thesis project is the design, physical layout and post-layout verification of a dedicated standard cell for a Scan Latch circuit. The cell will replace the macro-based implementation currently in use in [10] with the aim of

significantly reducing the silicon area and power consumption while maintaining or improving timing performance.

To achieve this main objective, the project encompasses the following sections:

- **Standard Cell Layout** Design a DRC/LVS-clean layout that adheres to the constraints of the target technology node to ensure compatibility with the existing methodology.
- **Cell Sizing** Design and characterize a set of drive strength variants ($1\times$, $2\times$ and $4\times$) by scaling W/L ratios and adding buffers systematically.
- **Parasitic Extraction & Simulation** Perform RC parasitic extraction (PEX) and run post-layout SPICE simulations to verify functionality and performance.
- **Comparative Analysis** Quantify and compare the obtained results with similar cells in terms of area, power consumption and timing parameters
- **EDA Implementation** Generate the necessary library abstraction files, such as .lib and LEF files, to allow the cell to be incorporated into standard synthesis and physical implementation flows.

Chapter 2

Methodology

2.1 Standard Cell Reference

A large portion of the work conducted in this project is based on the `TCBN28 HPCPLUS BWP12T40P140` Standard Cell Library by *TSMC*. The library itself is a 28nm process, High-Performance Compact Plus (HPC+) kit, released in 2017 and featuring a large array of cells, such as logic gates, storage elements and multiplexers [14]. This is a widely-used library which offers a solid starting point as well as providing a good reference baseline to compare any results obtained. The specific cell used as reference is `SDFQDx`, a Scan D-flip flop with single output (Q). The scan capability is a crucial aspect for the DFT purposes of this work, while the `'x'` denotes the drive strength of the cell, which scales the cell sizing accordingly for optimized load driving. The `TCBN28` library offers four different drive strength variants of the cell (`"D0"`, `"D1"`, `"D2"`, `"D4"`), which will be discussed In later sections of this project.

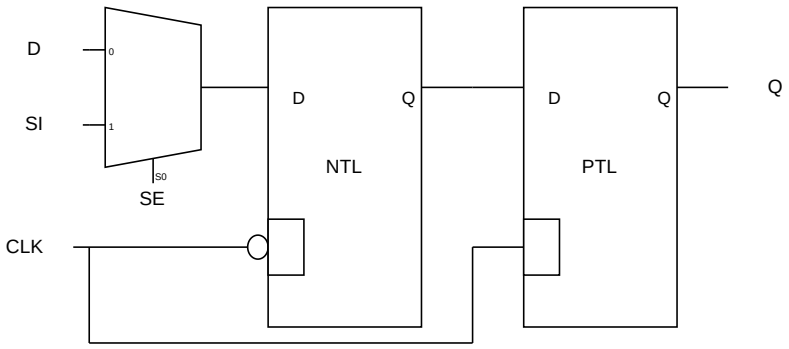


Figure 2.1: D-FF Logic Diagram.

The study focuses on the nominal conditions for characterization and comparison. The conditions are set as follows:

- 0.9V nominal supply voltage
- 25°C temperature
- Typical-Typical process corner

The library also features several models for the specific `SDFQDx` cell, which offer optimized solutions under different conditions. These options include examples such as synchronizer units `"SYN"`, meant for faster state resolution to overcome metastability issues, and `"OPTMAD"` cells for minimal average delay at the cost of area. For simplicity, the study will mainly focus on the standard model.

2.2 Schematic Integration and Verification

The first step in designing the required cell is establishing a baseline object to serve as a reference point for future testing. A crucial component of this cell is its schematic, which is currently missing from the object. A functional schematic is essential for testing purposes, as well as being a prerequisite for Layout Versus Schematic (LVS) verification.

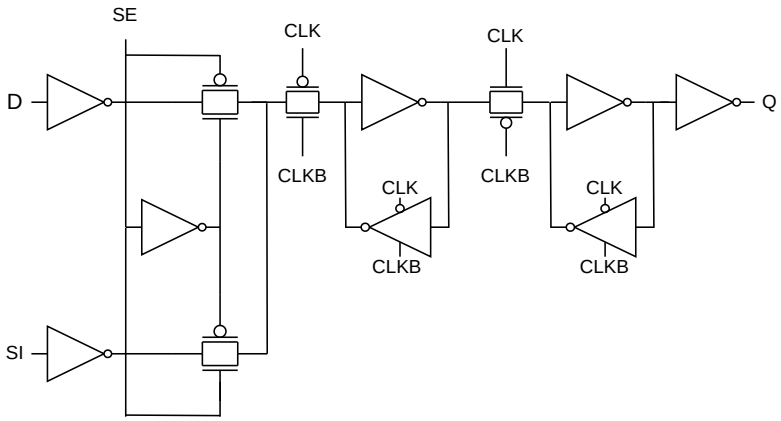


Figure 2.2: D-FF Gate Schematic.

A valid schematic can be derived from the netlist present in the library, from which the complete circuit can be drawn. The transistor models `nch_mac` and `pch_mac` used in the schematic are taken from the TSMC 28nm Process Design Kit

(PDK). All of the transistor dimensions (length/width) and their specific threshold voltages were accurately set up to perfectly match the cell's specifications.

It is also crucial to verify that the schematic functions as intended. For this reason a testbench is also set up with the designed cell instantiated as Unit Under Test (UUT). The testbench connects its inputs with several stimuli to simulate different operating conditions and validate its behavior.

Transient simulations are then performed, setting up the stimuli to verify that the circuit functions as intended.

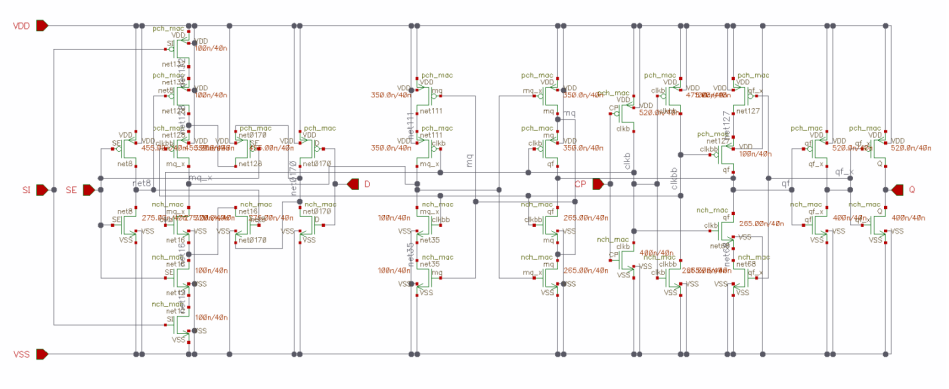


Figure 2.3: D-FF schematic view in Cadence Virtuoso.

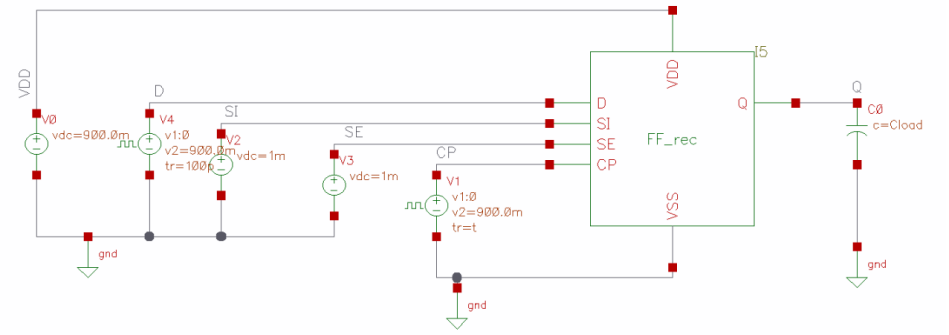


Figure 2.4: Testbench schematic view in Cadence Virtuoso.

2.3 Scan Latch Schematic

The functional block scheme of the target cell is shown in 2.5. As it can be noted, the circuit is designed to act as a regular PTL during functional mode (SE = 0),

while preserving the scan chain implemented with Scan FFs in scan mode (SE = 1). In other words, the cell bypasses the NTL block of the Scan FF.

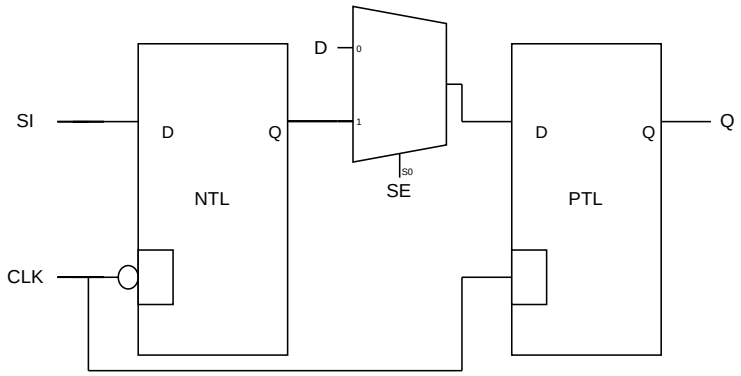


Figure 2.5: Scan Latch Logic Diagram.

Ideally, the Scan Latch cell can be derived from the original Scan FF by placing the input multiplexer of the Scan FF in between the latches, then re-wiring the circuit so the NTL input is connected directly to the SI signal and its output is connected to the second input of the multiplexer.

Looking at the gate schematic, it is possible to obtain this configuration by placing the NTL block before the multiplexer. The resulting schematic is shown in figure 2.6.

An important thing to note is that, by shifting the placement of the NTL, the logic structure of the cell is altered. Namely, the D-to-Q path now has 3 inverters instead of 4. To preserve this logic chain, an additional inverter is placed after the input gate. This structure also maintains the input capacitance of the original cell, as the initial gate is unaffected.

Initial parameters of the added inverter, namely the gate width of the transistors, are initially copied from the input inverter and their effects will be studied more closely in a later section.

The new schematic is subsequently tested to ensure its behavioral correctness.

2.4 Scan Latch Optimization

Although the system is working as intended, one thing stands out as a potential problem: measuring the D-to-Q propagation delay reveals that the circuit is highly imbalanced. In other words, the rising time delay is significantly shorter than the falling time delay.

Table 2.1: Propagation Delay Comparison

Parameter	**D-FF**	**HE Latch, Single Output**	**Scan Latch**
$t_{pLH,\mathrm{CLK}\rightarrow\mathrm{Q}}$	47.67 ps	49.86 ps	48.31 ps
$t_{pHL,\mathrm{CLK}\rightarrow\mathrm{Q}}$	48.19 ps	46.93 ps	50.08 ps
$t_{pLH,\mathrm{D}\rightarrow\mathrm{Q}}$	N/A	49.10 ps	50.64 ps
$t_{pHL,\mathrm{D}\rightarrow\mathrm{Q}}$	N/A	51.81 ps	57.22 ps

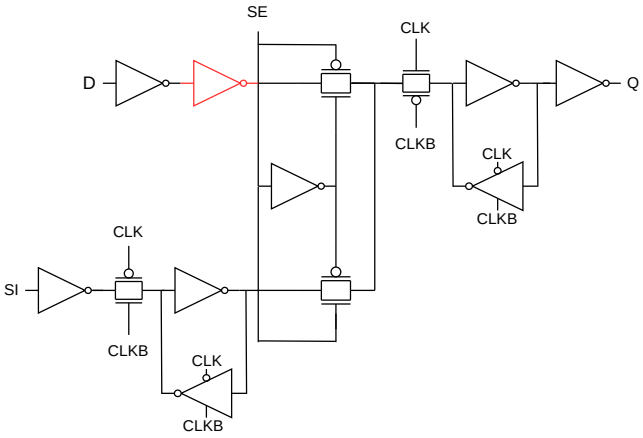


Figure 2.6: Scan Latch Gate Schematic.

This imbalance is due to the sizing of the individual transistors on the D-to-Q path.

As discussed in Chapter 1.4.2, logic gates can be skewed to favor either rising or falling transitions. This skew is given by the ratio between the beta parameters (β_n and β_p) of the nMOS and the pMOS networks and it can also be tuned to correct any delay imbalances in the path.

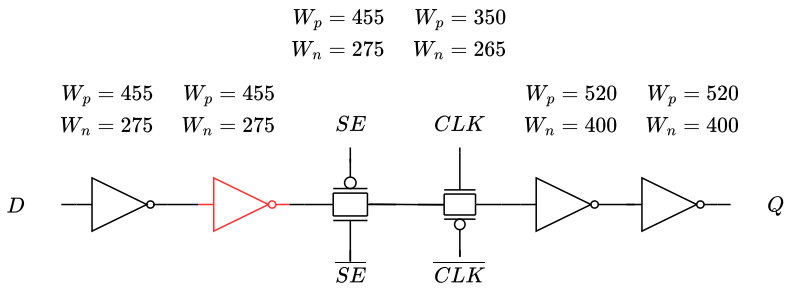


Figure 2.7: D-to-Q Path. W_n and W_p values reported in nm.

A closer look at the Scan Latch's D-to-Q path reveals that the input inverter is configured as a high-skew gate ($\beta_n/\beta_p < 1$). This means that, by copying its sizing parameters for the added inverter in the path, rising transitions will be inherently favored at the expense of low or falling transitions.

The answer to solve the delay imbalance is to adjust the beta ratio of the added inverter so the delays are balanced.

Recalling the expression for the beta parameter in MOSFETs:

$$\beta = \mu C_{\text{ox}} \frac{W}{L} \tag{2.1}$$

where the electron mobility μ and the oxide capacitance per unit area C_{ox} are defined by the manufacturing process, while L is usually fixed to the minimum feature size of the technology node. This leaves the channel width (W) as the sole design variable available for tuning the beta parameter of the transistors.

In the analyzed inverter, both the nMOS and pMOS channel widths (W_n and W_p) influence its performance. Instead of studying each width independently, we define W_n and the ratio $\beta = W_n/W_p$ as the chosen design variables. These variables were then established as parameters, with W_n being swept from 255 nm to 455 nm with 25 nm intervals, and β spanning values from 0.5 to 1.5 with 0.1 step. Afterwards, a transient analysis of 2 ns duration was set up. The simulation was made sure to have both a rising and a falling output transition.

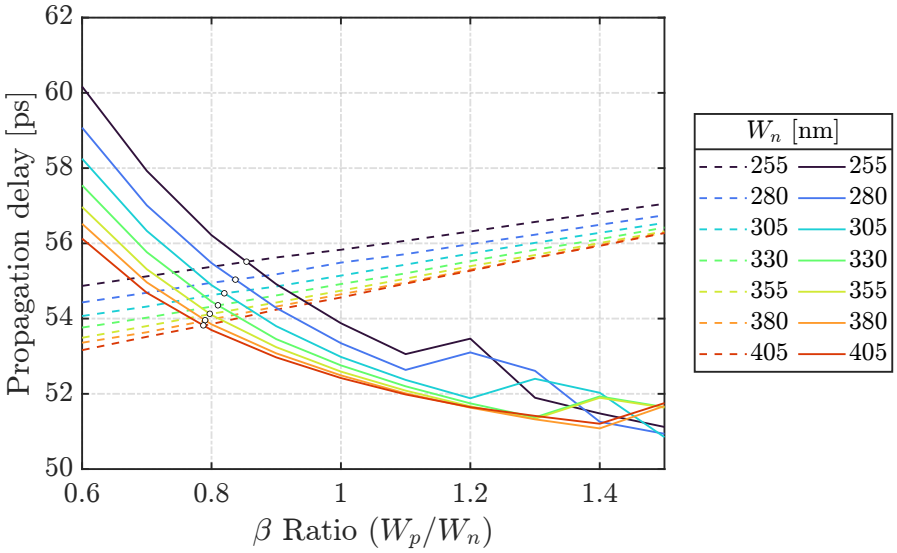


Figure 2.8: Inverter propagation delay versus β ratio. LH transitions are solid lines, HL transitions are dashed lines

Studying the obtained results, we can observe that as the β ratio increases, propagation delay decreases for LH transitions while it rises for HL transitions. This is consistent with what was previously discussed, as a larger ratio corresponds with a high-skew inverter which favors high transitions.

Another thing to note is that, as W_n is increased, both types of transitions become faster. This is due to the wider MOSs being able to conduct more current which accelerates the transition regardless of its directional state.

The figure also highlights the crossing point between the two transitions at any given W_n value with white dots. This indicates the β values where the circuit is balanced, meaning that HL and LH transition delays are equal.

As seen in the chart, these points sit around the $\beta = 0.8$ mark. If the ratio is fixed at this value, we can plot the cell delay as a function of W_n.

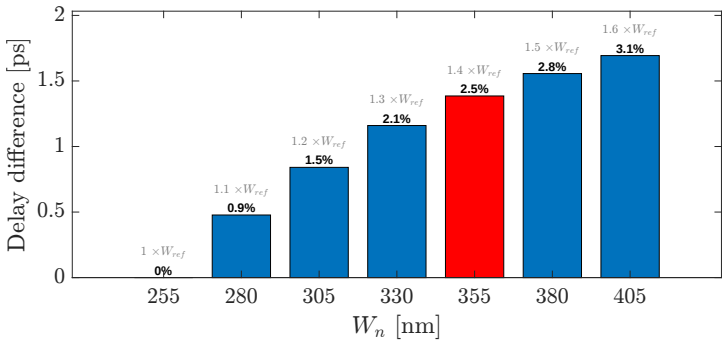


Figure 2.9: Delay difference between nMOS channel width values.

The figure illustrates the delay percentage decrease in delay relative to the baseline W_n value of 255 nm. The main takeaway is that beyond the $W_n = 355$ nm point, we obtain diminishing returns in delay reduction.

Another factor to take into account when choosing an appropriate set of design parameters is the power consumption of the observed inverter: a larger logic gate will let more current through during a transition, resulting in a higher energy consumption per switching event.

A simple way to quantify this is to measure the current flowing through the cell during a transition. This current can then be used to compute the switching power of the circuit via the following expression:

$$P_{\text{switching}} = \frac{1}{T} \int_0^T i_{DD}(t) V_{DD} \, dt \tag{2.2}$$

where T is the switching period, i_{DD} is the supply current and V_{DD} is the supply voltage. For this specific test, V_{DD} was kept at 0.9 V while the measuring period was set at $T = 10$ ns.

From Figure 2.10, we observe a gradual current increase as W_n increases: The peak current rises from 110 μA to approximately 150 μA.

By applying the same procedure to this data, we obtain the relative power consumption increase for each corresponding W_n value. As shown on Figure 2.11, the P_{avg} follows a linear increase in function of the channel width.

From all the collected information, we can establish the following design parameters: $W_n = 355$ nm, $\beta = 0.8$. These values offer a balanced circuit and reduced propagation delays without an excessive consumption.

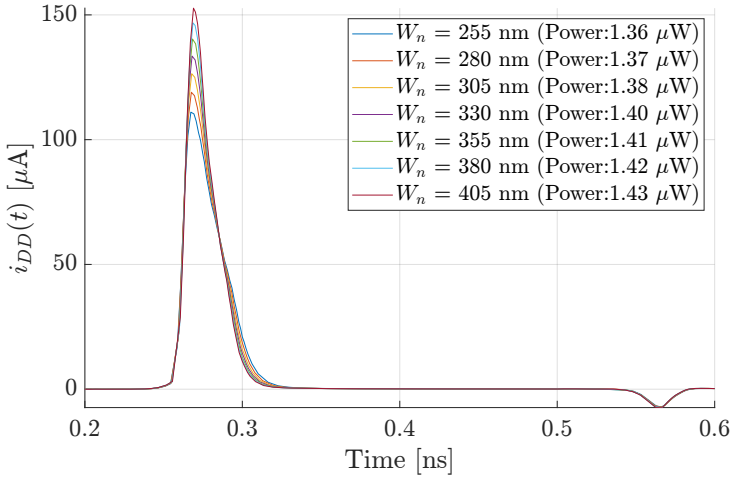


Figure 2.10: Inverter supply current versus time.

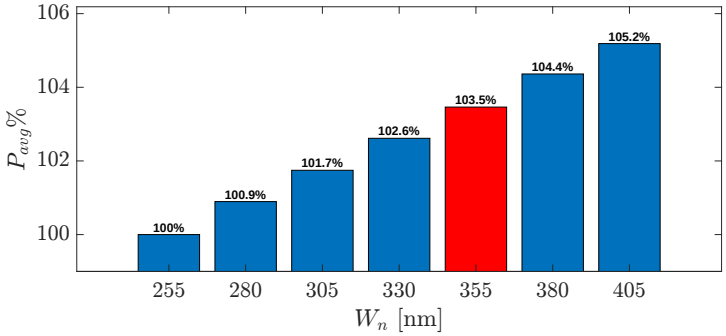


Figure 2.11: Switching power difference between nMOS channel width values.

Table 2.2 shows the delay values of the updated Scan Latch design, confirming the improvements made.

Table 2.2: Propagation Delay Comparison with the Revised Scan Latch Design

Parameter	**D-FF**	**HE Latch, Single Output**	**Scan Latch**	**Scan Latch Revised**
$t_{pLH,\mathrm{CLK}\rightarrow\mathrm{Q}}$	47.67 ps	49.86 ps	48.31 ps	49.10 ps
$t_{pHL,\mathrm{CLK}\rightarrow\mathrm{Q}}$	48.19 ps	46.93 ps	50.08 ps	50.11 ps
$t_{pLH,\mathrm{D}\rightarrow\mathrm{Q}}$	N/A	49.10 ps	50.64 ps	54.07 ps
$t_{pHL,\mathrm{D}\rightarrow\mathrm{Q}}$	N/A	51.81 ps	57.22 ps	54.17 ps

2.5 Scan Latch Layout

Once the Scan Latch schematic has been designed and verified, we can proceed with the layout design.

To design the Scan Latch layout, we modified the baseline FF layout rather than building from scratch. Using the original FF provided an established foundation with optimized transistor channel widths and low-parasitic metal routing. Retaining this baseline also established a consistent reference frame for evaluating area expansion, timing degradation, and power overhead introduced by the resulting modifications.

To maintain standard cell compatibility with the library, cell height, track pitch, power rails and boundary locations were kept strictly identical to the initial layout.

After observing both schematics, the main distinction between them, aside from the previously discussed inverter, is that the first D-FF latch has been placed before the MUX section in the SL layout. Identifying and re-routing the key nodes between these blocks yields the final cell layout.

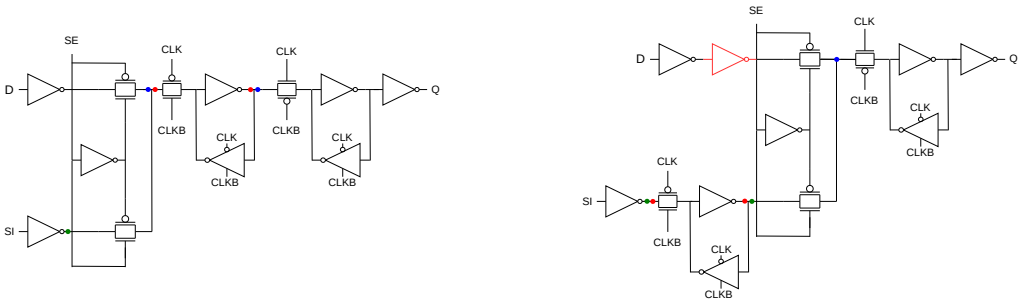


Figure 2.12: D-FF and SL schematics. Key nodes highlighted.

After determining the nodes in the schematic, the next step is to identify them in the FF layout.

Notably, adjacent connected transistors in a layout typically share a diffusion region, meaning the drain of one MOSFET and the source of the next form a single contiguous section. While this source-drain sharing minimizes silicon area and reduces unnecessary metal routing and vias, it complicates re-routing, as these shared nodes must be split. Otherwise, the transistors will remain connected and cause unwanted behavior.

Analysis of the FF layout confirms that two of the three key nodes share a diffusion region. These nodes are separated and a dummy polysilicon gate is placed between them, which increases the overall silicon area. Furthermore, one of these regions has a narrow active area as the constituent transistors feature

a small channel width. This impedes the placement of contacts according to the Design Rules. Properly connecting these MOSFETs requires enlarging the diffusion region, thereby increasing the parasitic capacitance of the node. While significant degradation of the cell is unexpected, the effects of this modification will be evaluated in a later section.

The second layout modification involves placing the second inverter along the D-to-Q path after the input inverter. This step complicated by the fact that the inverter's need for supply rail connections (V_{DD} and GND). Since no adjacent MOSFET requires V_{DD}/GND share nodes with this gate, these have to be exclusively tied to the inverter. A minor optimization can be applied in this case: The supply rails can be shared between the input inverters, which means that only the left-most edge of the layout must be isolated.

Considering all of the aforementioned modifications, the Scan Latch layout is shown on Figure 2.13.

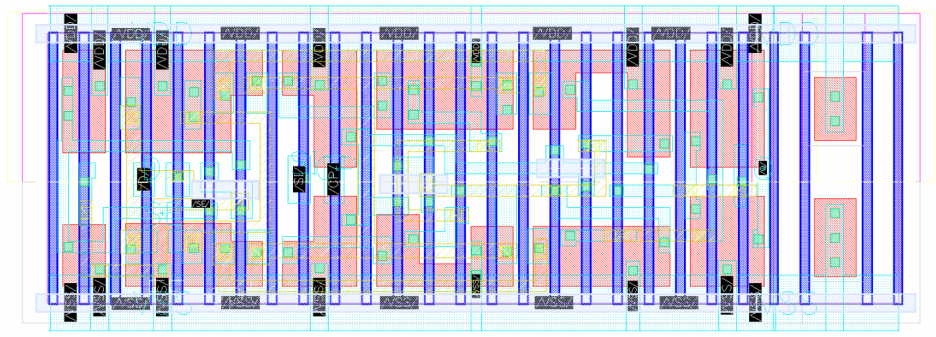


Figure 2.13: Scan Latch layout view in Cadence Virtuoso

2.6 DRC and LVS Verification

After designing the Scan Latch layout, Design Rule Check (DRC) and Layout Versus Schematic (LVS) verifications must be performed. DRC ensures that the layout is consistent with the technology node manufacturing rules while LVS checks both the schematic and the extracted netlist of the layout to verify that the physical implementation matches the intended connectivity and the device sizes.

At this stage, minor adjustments to the layout were required to comply with the DRC. For instance, the diffusion geometry is restricted to simple rectangular or L/U-shaped polygons. This meant that some device sizes had to be adjusted.

After such changes were made in the schematic, the cell passed the LVS verification, becoming LVS-clean.

2.7 Parasitics extraction

Performing Parasitic Extraction (PEX) is an essential part layout development, as it provides accurate information on parasitic parameters that are present in the physical design. These parameters directly affect everything from timing performance to power consumption, thus running a PEX is mandatory to ensure the layout still meets both its required function and expected performance.

After the PEX was successfully executed, the simulations were re-done. Timing, area and power consumption measurements will be examined in Chapter 3 .

2.8 Drive Strength Development

Once the main cell for the Scan Latch is fully realized, we can extend the library to include different drive strengths.

As different applications require different current requirements, having an array of functionally identical cells with appropriate drive capacities is a crucial part of Standard Cell design.

The primary cell sizes are D0, D1, D2 and D4. They are the sizes featured in the library for the original FF cell, which serves as a natural baseline for the Scan Latch. Each variant will be studied individually, using the FF layout as reference, and adapted from the D1 layout to maintain consistency and simplify the design process.

Comparing the FF D0 layout, it is apparent that the main structure is near identical to the D1 layout, the sole exception being the output inverter being halved in size. Applying this modification to the Scan Latch yields a valid D0 Scan Latch cell.

The D2 and D4 cases diverge slightly: in addition to scaling the output inverters for added drive capacity, these layouts have split gates for $CLK/\overline{CLK}$ whereas the D1 layout drives both signals from single-gate structures. This design choice mainly provides more stability to the clock signal. Since the larger transistors and the added output buffers introduce a higher capacitance, splitting the gates ensures the heavier load is driven in a stable and efficient manner.

Adopting this feature in the Scan Latch cells proved too complex due to the limited space left in the M2 layer after the initial re-routing, therefore the single-gate design was kept from the initial cell.

All of the variants were tested, verified and made DRC- and LVS-clean following the same procedure as the D1 cell.

2.9 LEF file extraction

The last step in designing a standard cell is the generation of the required abstraction files that allow physical design tools to interpret and use the cell. These files are the means by which cells are distributed and integrated into workflows.

The Library Exchange Format (LEF) is a standard used to represent the standard cell in ASCII format. It is distributed by the *Si2* organization and is supported by *Cadence Design Systems*. The LEF file includes, among other things, information regarding the cell layout such as layers, vias and core area [15].

Cadence offers a built-in method to extract the LEF file of any cell in the present. All four drive strength variants were exported.

Chapter 3

Results

Following design and verification, the Scan Latch cells are tested for functional verification and performance evaluation via Cadence Virtuoso simulations. These tests allow us to characterize the designs for `.lib` file generation and give us confirmation that our modifications have not degraded the layout's functional integrity.

The main metrics for this analysis are timing, power consumption and area. Because these parameters are the basis of standard cell Liberty files, they serve as a solid framework for evaluation. To contextualize the results, the Liberty file data of the technology library containing the reference flip-flop used during the design phase `tcbn28hpcplusbwp40p140tt0p9v25c.lib` will be taken as a baseline for these performance comparison.

3.1 Timing

Liberty `(.lib)` files report several key cell delay measurements such as transition delays and rise/fall times. These reports provide accurate information about the cell's behavior and performance under varying conditions and specifying parameters such as power signals and direction.

The library defines the following key timing measurements:

- **cell_rise**: Time interval between the input signal delay threshold (defined in this instance as the 50% mark) and the output signal delay threshold, measured during the output rising transition.

- **cell_fall**: Time interval between the input signal delay threshold (defined as its 50% mark) and the output signal delay threshold, measured during the output falling transition.

- **rise_transition**: Time interval between the output signal 10% mark and its 90% mark, observed during the rising transition of the output.
- **fall_transition**: Time interval between the output signal 90% mark and its 10% mark, observed during the falling transition of the output.

These reports are parameterized by both output capacitance and input net transition time, which correspond to the `index_1` and `index_2` arrays of the `.lib` file, resulting in a 7×7 matrix for each report. The indices for the flip-flop vary depending on the drive strength layout. To be precise, the output capacitance index of each cell roughly doubles for each increasing drive strength value above a fixed 0.22 fF intrinsic baseline.

The library also defines time measurements for each input-output pin pairs, such as D-to-Q, CP-to-Q and SE-to-Q delays. This work will primarily focus on the CP-to-Q path, as it's delay is the most relevant metric for our analysis.

For clarity, all timing measurements are presented as a heatmap against the reference flip-flop measurements, where red indicates a degradation (increased delay), while blue signifies an improvement (decreased delay).

3.1.1 D0 layout

The input indices are as follows:

1. $t_{\text{transition}} = [0.002, 0.0119, 0.0318, 0.0715, 0.151, 0.31, 0.628]$ ns
2. $C_{\text{load}} = [0.00022, 0.00116, 0.00304, 0.0068, 0.01432, 0.02937, 0.05947]$ pF

The D0 cell exhibits overall poor timing performance. Rise and fall times show a 100-150% overhead when compared to the original cell, while rise and fall transitions provide noticeably better results. From the transition delay graphs, one can also observe that the difference between the Scan Latch and the reference FF is primarily dictated by the output capacitance value. The designed cell performing worse at higher capacitances while showing marginal improvements at lower values. On the other hand, input transition values are not shown to drastically affect the cell's performance.

These results can likely be explained by the relative lack of design optimization during the layout process. Because the D0 cell is the smallest drive strength variant, it could prove to be more sensitive to any modifications made to the original FF layout. The added metal paths and layer adjustments could have added parasitic parameters that negatively impacted on the cell. Furthermore, the consistent bias shown in Fig.3.1 and 3.2 could also suggest that the Cadence simulation methodology to obtain the results has introduced unexpected variables to the measurements.

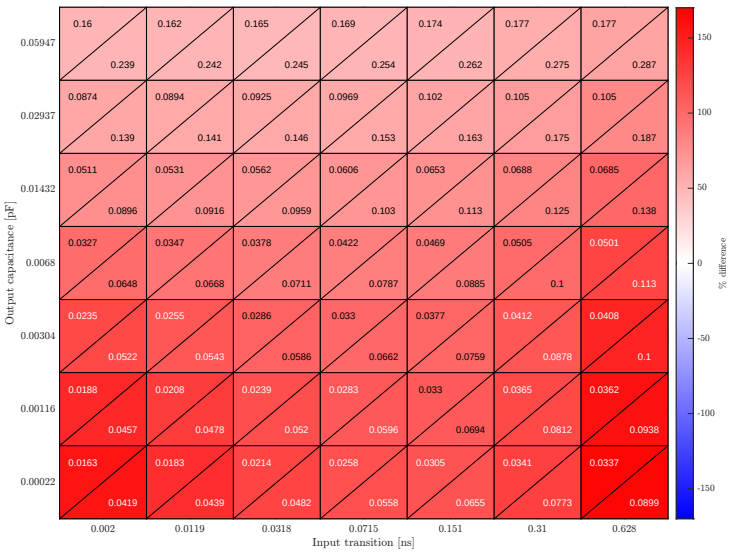


Figure 3.1: SL/FF D0: Cell rise comparison (ns).

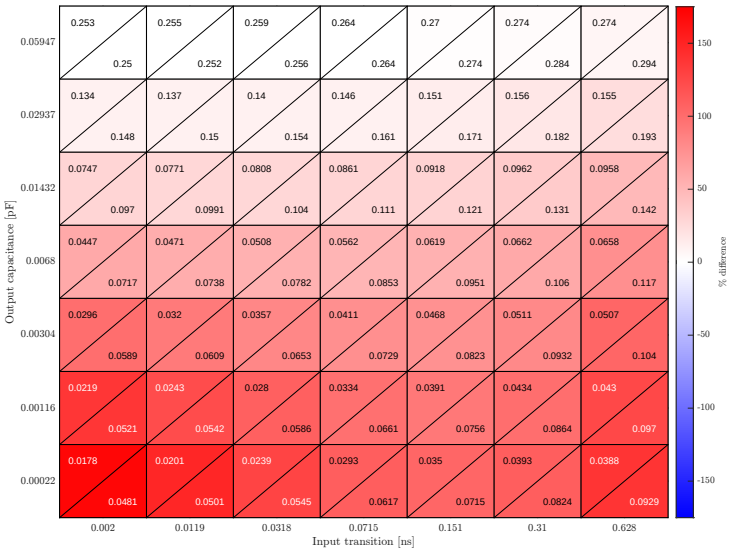


Figure 3.2: SL/FF D0: Cell fall comparison (ns).

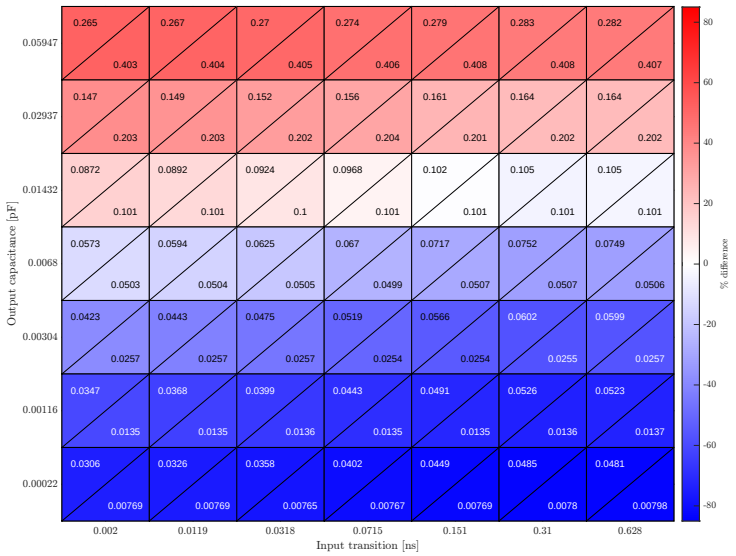


Figure 3.3: SL/FF D0: Rise transition comparison (ns).

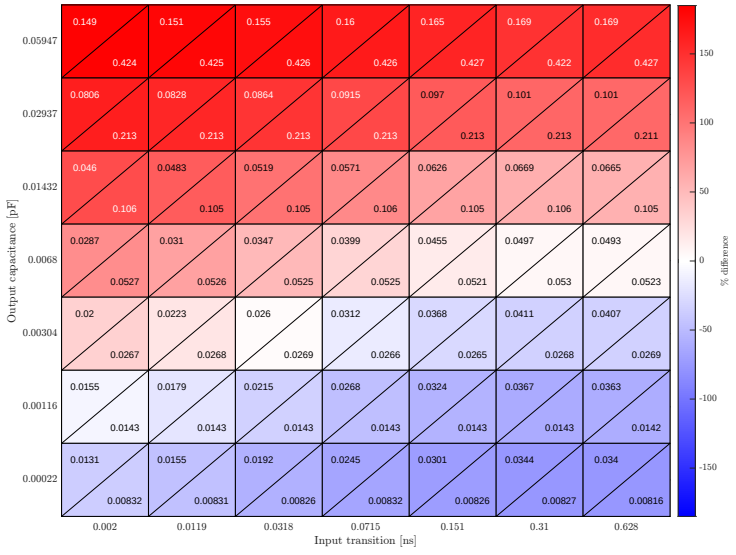


Figure 3.4: SL/FF D0: Fall transition comparison (ns).

3.1.2 D1 layout

The input indices are as follows:

1. $t_{\text{transition}} = [0.002, 0.0119, 0.0318, 0.0715, 0.151, 0.31, 0.628]$ ns
2. $C_{\text{load}} = [0.00022, 0.0021, 0.00587, 0.01341, 0.02848, 0.05863, 0.11893]$ pF

The D1 cell's performance closely follows the original FF. Post-layout simulations show consistent improvements over the reference cell, providing decreased rise and fall delays as well as transition delays. Interestingly, while the D0 cell showed worsening performance for increasing output capacitance, the D1 cell performs better at higher capacitances. Rise and fall times show 20-25% improvements at higher capacitance values while transition delays show more modest gains. Once again, output capacitance is the leading parameter in terms of variance, while input transition shows little variance. Lastly, transition delays for the lowest output capacitance show significantly worse results compared to the rest of the graph. This may be caused by the lower accuracy in the Cadence simulations at these boundaries.

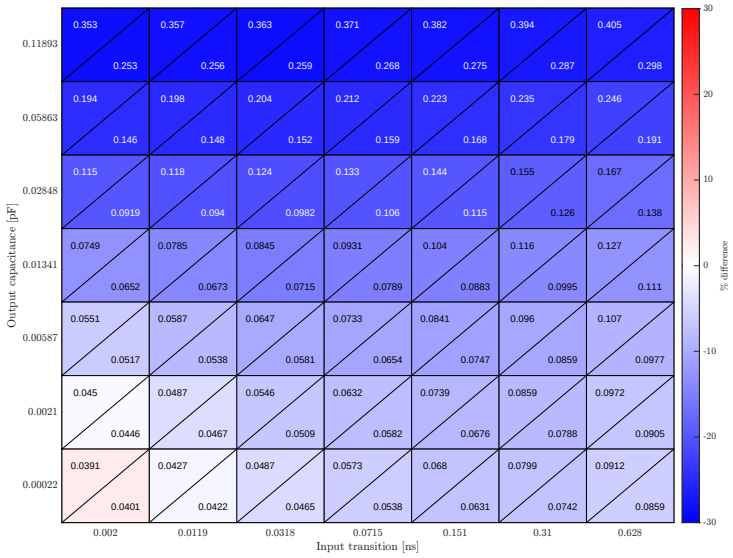


Figure 3.5: SL/FF D1: Cell rise comparison (ns).



Figure 3.6: SL/FF D1: Cell fall comparison (ns).

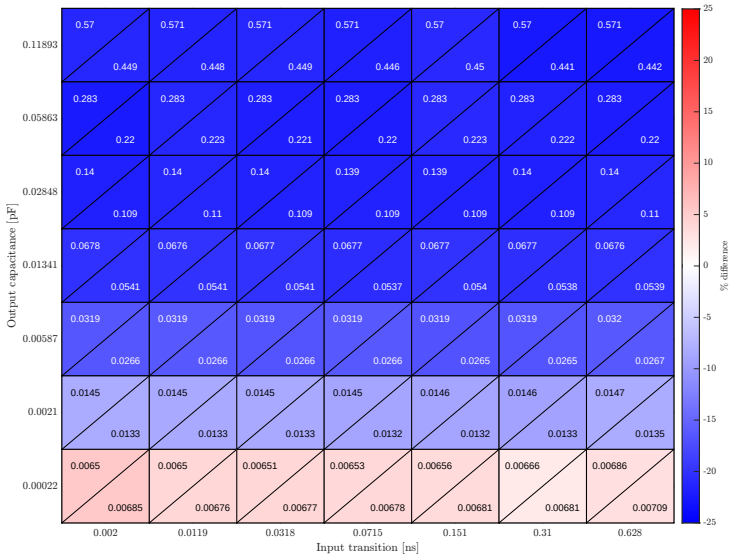


Figure 3.7: SL/FF D1: Rise transition comparison (ns).

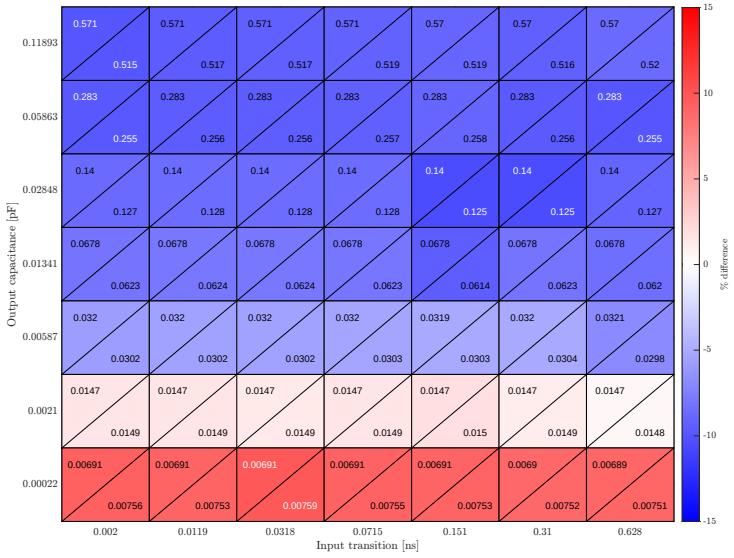


Figure 3.8: SL/FF D1: Fall transition comparison (ns).

3.1.3 D2 layout

The input indices are as follows:

1. $t_{\text{transition}} = [0.002, 0.0119, 0.0318, 0.0715, 0.151, 0.31, 0.628]$ ns
2. $C_{\text{load}} = [0.00022, 0.00399, 0.01153, 0.02662, 0.0568, 0.11716, 0.23787]$ pF

The higher drive strength layouts deviate more from their respective reference cell compared to the D1 variant. As explained previously, the original FF cells feature split gates for the clock input for improved signal stability. Since the Scan Latch layouts forgo this design, the overall load of the clock signal should be lighter which should aid in the cells' timing performance. However, this comes at the cost of reduced cell stability.

In the case of the D2 layout, this change yields significant timing improvements for both rise/fall and transition delays. Gains reach 25-30% over the reference cell in the case of rise/fall times, and 20% for transition times. Once again, delays are further reduced for higher capacitance values, while the lowest output capacitance exhibits slightly worse results compared to the reference.



Figure 3.9: SL/FF D2: Cell rise comparison (ns).



Figure 3.10: SL/FF D2: Cell fall comparison (ns).

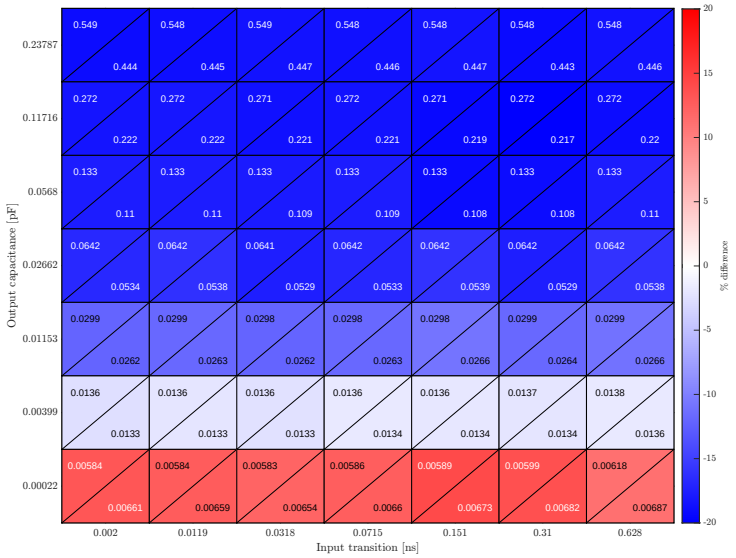


Figure 3.11: SL/FF D2: Rise transition comparison (ns).

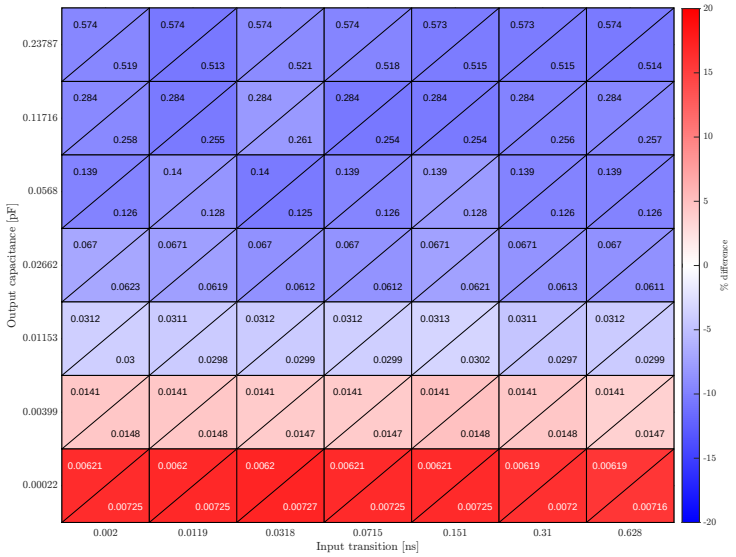


Figure 3.12: SL/FF D2: Fall transition comparison (ns).

3.1.4 D4 layout

The input indices are as follows:

1. $t_{\text{transition}} = [0.002, 0.0119, 0.0318, 0.0715, 0.151, 0.31, 0.628]$ ns
2. $C_{\text{load}} = [0.00022, 0.00776, 0.02286, 0.05305, 0.11343, 0.2342, 0.47573]$ pF

The D4 layout shows similar improvements to the D2 variant. The graph shows up to 25% gains across all delays, having the biggest difference at higher load capacitances, consistent with the previous layouts.

Sensitivity to input transition is also minimal, showing that despite the changes made to the original FF layout, the Scan Latch remains a highly stable cell.

As an additional note, while the performance improvements at larger output loads grow across the different cells, the performance at the smallest load progressively worsens for each successive layout. This can be explained by the fact that larger cells fare worse at driving smaller loads due to their higher internal parasitic capacitance. This makes it so the charge and discharge time is longer, making these cells less efficient in these scenarios.

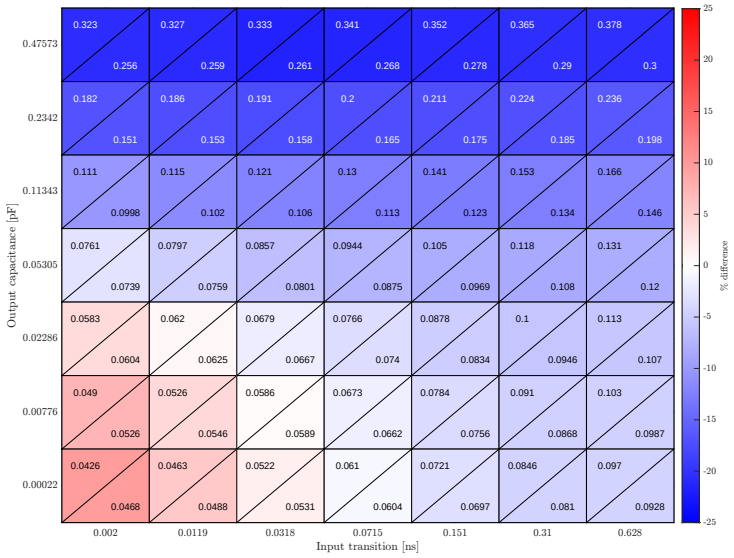


Figure 3.13: SL/FF D4: Cell rise comparison (ns).

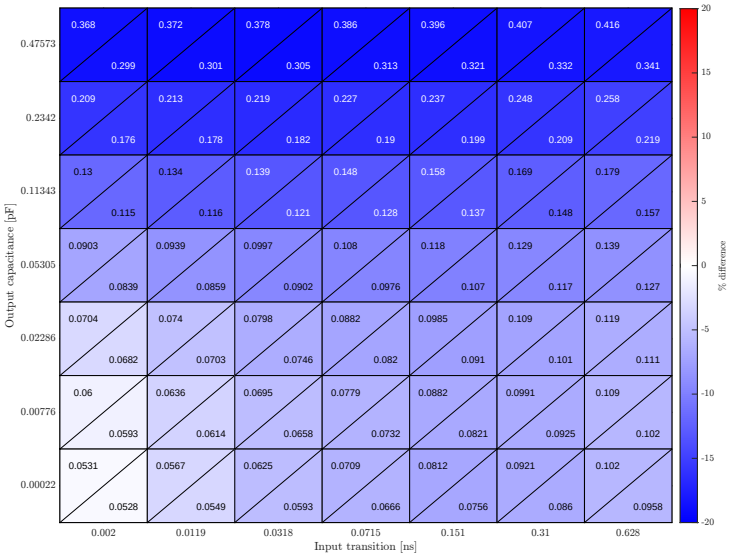


Figure 3.14: SL/FF D4: Cell fall comparison (ns).

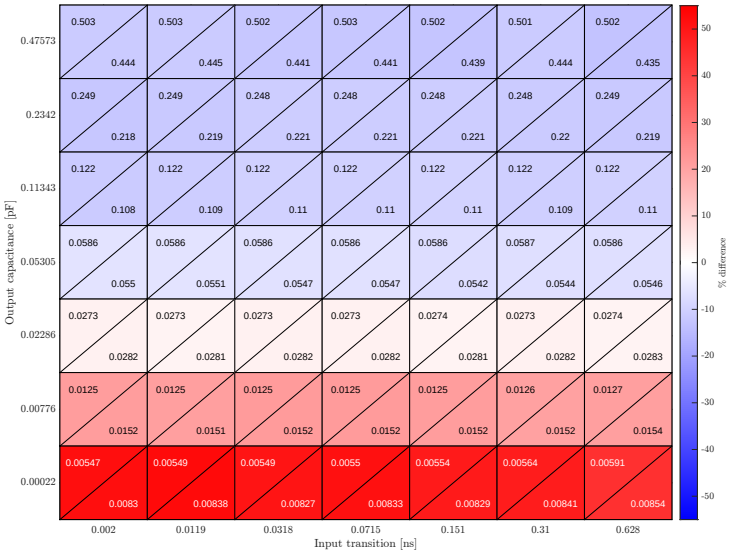


Figure 3.15: SL/FF D4: Rise transition comparison (ns).

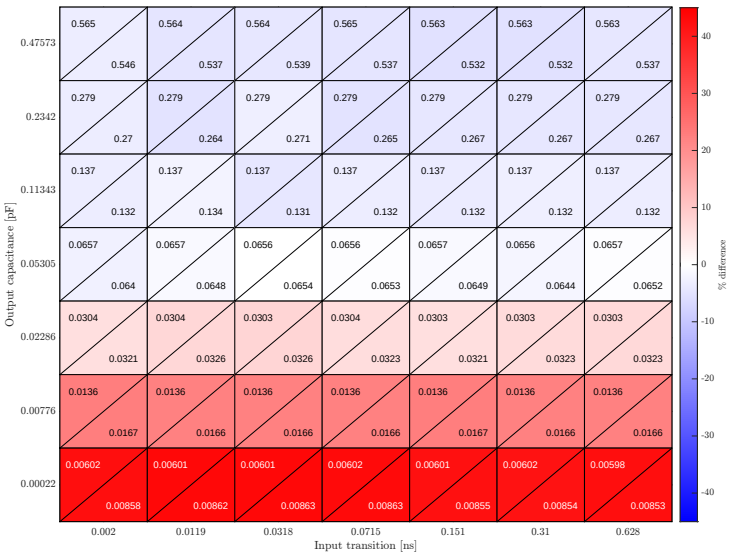


Figure 3.16: SL/FF D4: Fall transition comparison (ns).

3.1.5 Summary

By averaging all delay measurements for each drive strength variant, we can compare the general trends of both the FF reference and the SL design (Fig. 3.17). We observe that, apart from the D0 cell anomaly, all FF layouts stay consistently within the 0.15÷0.16 ns range. By contrast, while the delay of SL layouts slightly increases as they get larger, they mostly remain in the 0.12÷0.13 ns range, meaning the SL layouts are, on average, marginally faster than their FF counterparts.

Notably, the D0 layout is the only variant that performs noticeably worse than the FF cell. This may be because the added parasitic capacitances have a proportionally larger impact on cell performance. Conversely, the D1 cell shows the largest comparative improvement.

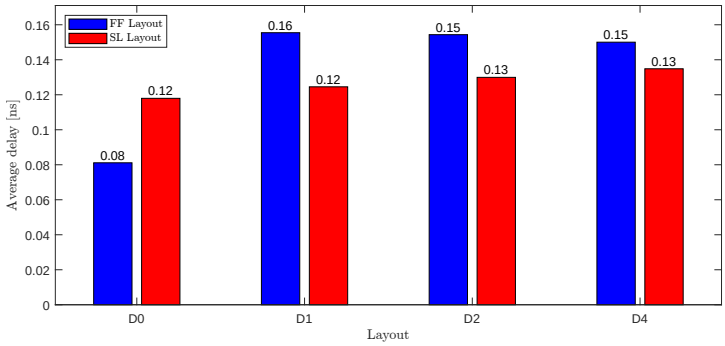


Figure 3.17: Flip Flop versus Scan Latch Average Timing.

3.2 Power consumption

Power consumption is also reported in the Liberty files of a library, measuring parameters such as the internal power of a cell or the transition energy during a rising/falling signal. This work will mostly focus on this last report as measuring the internal power of a cell requires more precise tools. To be specific, the reports in the `.lib` file are defined as follows:

- **rise_power**: Internal energy of the cell during an output rising transition.
- **fall_power**: Internal energy of the cell during an output falling transition.

Notably, the reports show internal energy of the cell, which means that the output capacitance should not be strongly linked to the results.

Analogous to the previous section, power consumption reports for cell transitions are detailed in a 7×7 matrix using the same input arrays for each layout as in

Chapter 3.1. Similarly, the results obtained are displayed as a heatmap graph with the FF `.lib` file reports as a reference. Energy decrease is noted as green while energy increase is noted as red.

Power measurements were obtained by performing Cadence Virtuoso simulations, obtaining the supply current I_{VDD} and computing the transition energy using the formula 2.2, subtracting the energy stored by the output capacitance in the case of the rising transition following the expression:

$$E_{load} = C_{load} V_{DD}^2 \tag{3.1}$$

3.2.1 D0 layout

The input indices are as follows:

1. $t_{\text{transition}} = [0.002, 0.0119, 0.0318, 0.0715, 0.151, 0.31, 0.628]$ ns
2. $C_{\text{load}} = [0.00022, 0.00116, 0.00304, 0.0068, 0.01432, 0.02937, 0.05947]$ pF

Rise and fall power of the D0 cell show consistent results. Rise power increases by 35% on average while fall power shows a 20% difference compared to the reference cell. These differences are consistent regardless of output capacitance or input skew, meaning that the internal power of the cell is not correlated to said parameters.

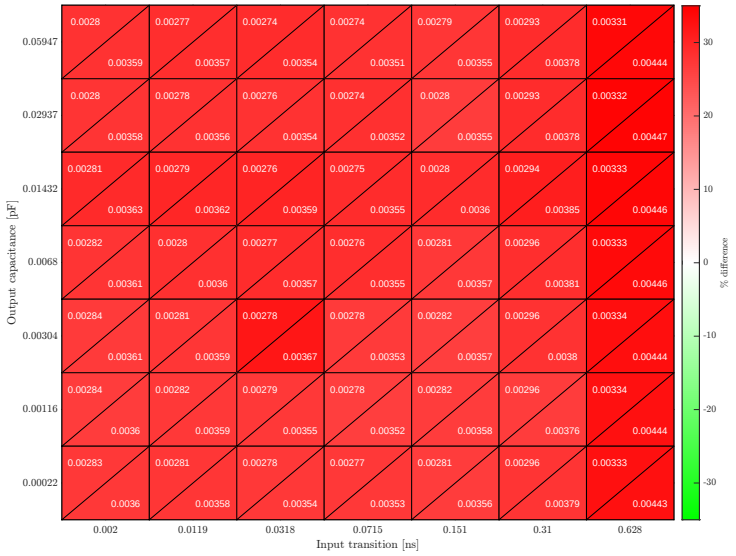


Figure 3.18: SL/FF D0: Rise power comparison (pJ).

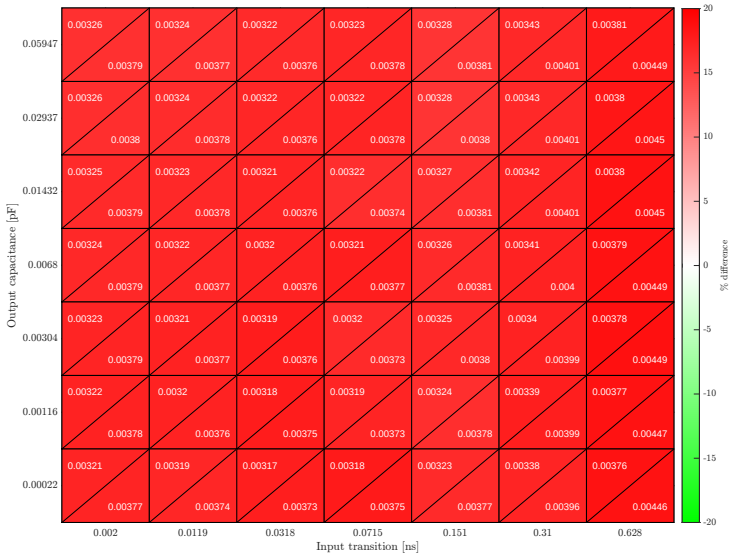


Figure 3.19: SL/FF D0: Fall power comparison (pJ).

3.2.2 D1 layout

The input indices are as follows:

1. $t_{\text{transition}} = [0.002, 0.0119, 0.0318, 0.0715, 0.151, 0.31, 0.628]$ ns
2. $C_{\text{load}} = [0.00022, 0.0021, 0.00587, 0.01341, 0.02848, 0.05863, 0.11893]$ pF

Rise and fall power of the D1 cell show nearly identical results as the previous layout, having noticeably higher power consumption values across the board. Values are also strongly consistent which still indicates no correlation between the input parameters and the results.

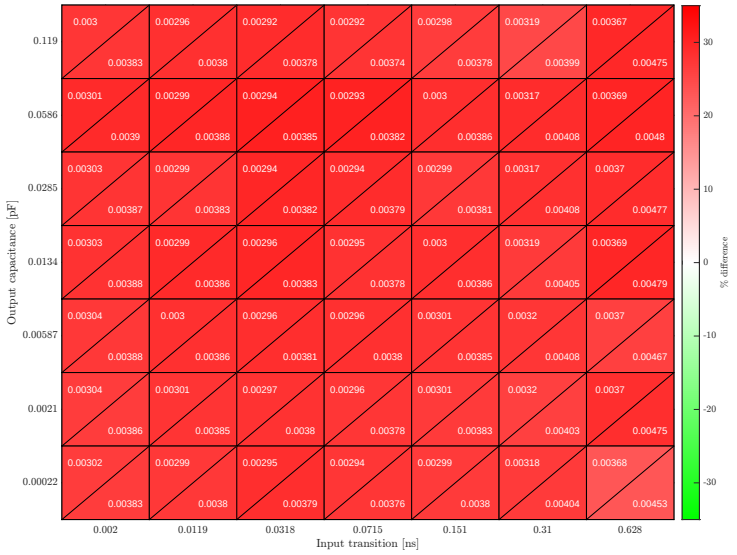


Figure 3.20: SL/FF D1: Rise power comparison (pJ).

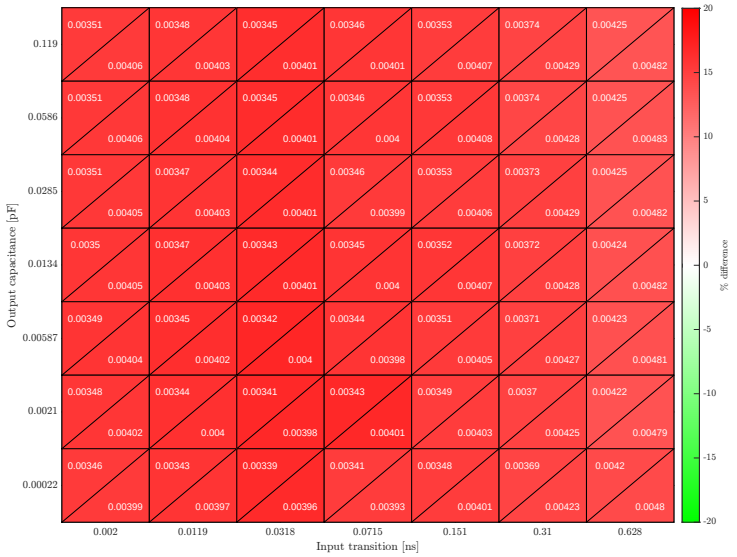


Figure 3.21: SL/FF D1: Fall power comparison (pJ).

3.2.3 D2 layout

The input indices are as follows:

1. $t_{\text{transition}} = [0.002, 0.0119, 0.0318, 0.0715, 0.151, 0.31, 0.628]$ ns
2. $C_{\text{load}} = [0.00022, 0.00399, 0.01153, 0.02662, 0.0568, 0.11716, 0.23787]$ pF

Rise and fall power of the D2 cell overall are slightly better compared to the smaller variants, having 20 to 25% power consumption increase. An interesting thing to note is that this time, results are not as consistent as in previous cases, suggesting that the Scan Latch cell is not as robust as the FF reference.

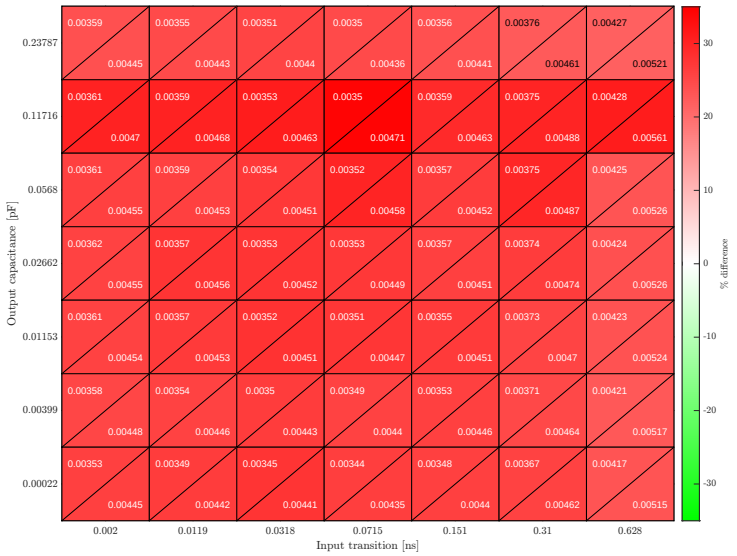


Figure 3.22: SL/FF D2: Rise power comparison (pJ).

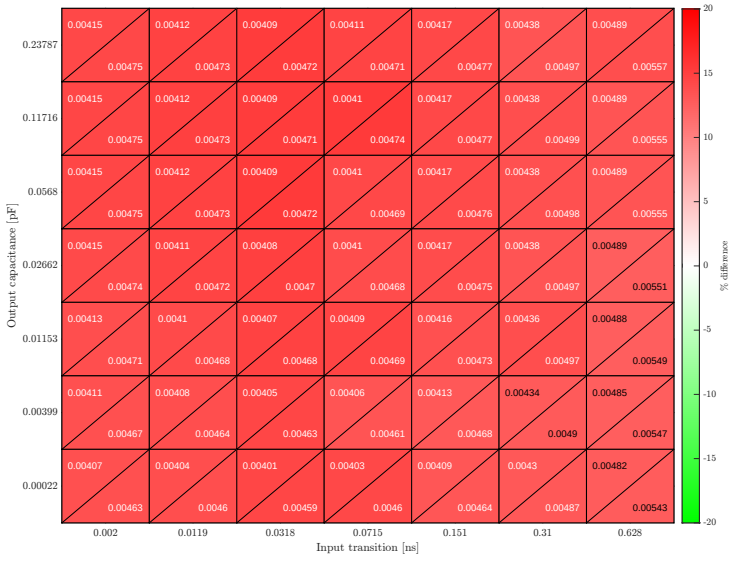


Figure 3.23: SL/FF D2: Fall power comparison (pJ).

3.2.4 D4 layout

The input indices are as follows:

1. $t_{\text{transition}} = [0.002, 0.0119, 0.0318, 0.0715, 0.151, 0.31, 0.628]$ ns
2. $C_{\text{load}} = [0.00022, 0.00776, 0.02286, 0.05305, 0.11343, 0.2342, 0.47573]$ pF

The D4 layout exhibits the best comparative results of the drive strength variants, having a 15 to 20% difference when compared to the reference cell. The layout also shows the same inconsistencies as the D2 cell, although the variance is less noticeable.

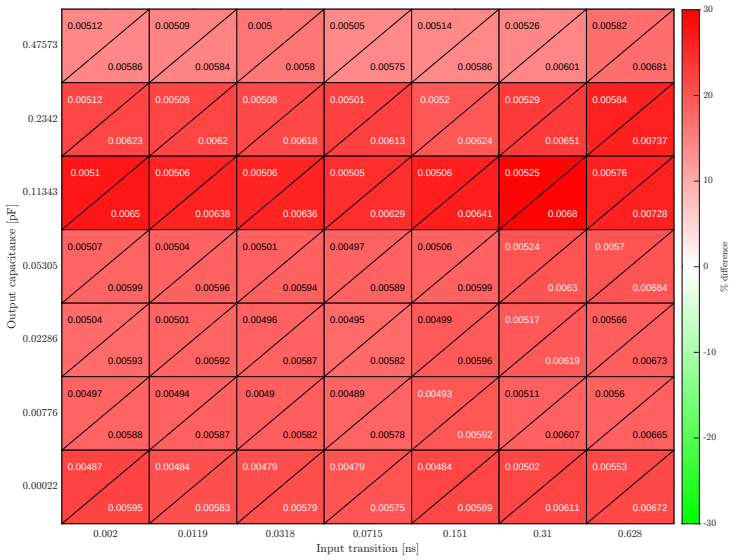


Figure 3.24: SL/FF D4: Rise power comparison (pJ).

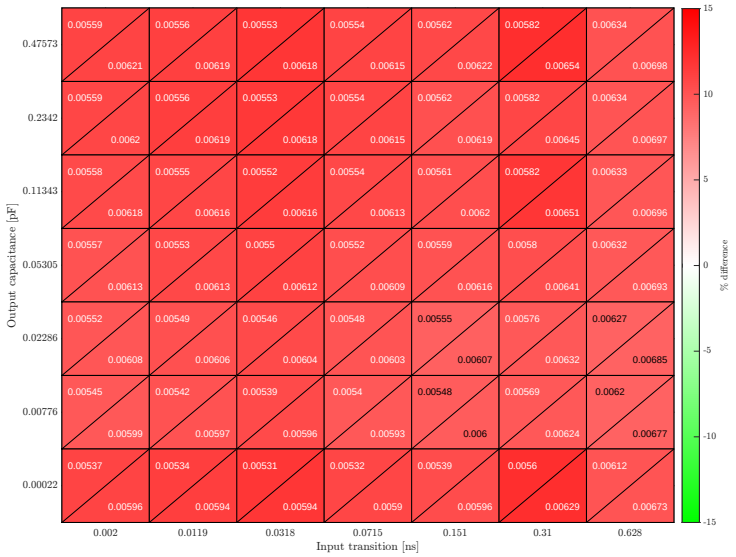


Figure 3.25: SL/FF D4: Fall power comparison (pJ).

3.2.5 Summary

Analogous to the previous section, we can average the power consumption of the rise and fall transitions to analyze the general trends of both FF and SL cells. The resulting figure is shown in 3.26.

Power consumption-wise, the Scan Latch cells perform slightly worse than their FF counterparts. Averages show a 24% energy increase for the D0 layout while larger layouts such as D4 exhibit a 14% rise. These results are expected however, given the inclusion of an extra inverter as well as the increased parasitic resistance/capacitance from the longer Metal paths. Overall, the results are acceptable and within reasonable margins.

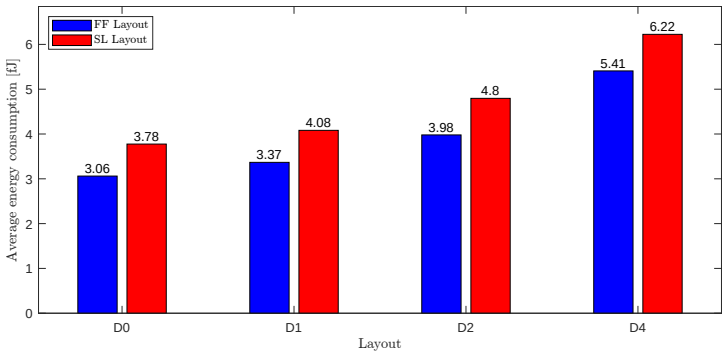


Figure 3.26: Flip Flop versus Scan Latch Average Energy.

3.3 Area

Total area is one of the main concerns of this work, as the custom Scan Latch layout aims to replace the larger macro structure present in the *Mix&Latch* algorithm. Silicon area is the primary cost of an integrated circuit production, and reducing it is a critical part of IC design.

Results of the Scan Latch layouts are shown in Fig.3.27. A larger footprint compared to the FF layout is to be expected, since three additional gates had to be added to each of the cells to obtain the target circuit. Area increase totals 18% for the D0 and D1 cells, while D2 and D4 show more modest increases (13% and 8% respectively), due to the split gate design not being used in the latter layouts.

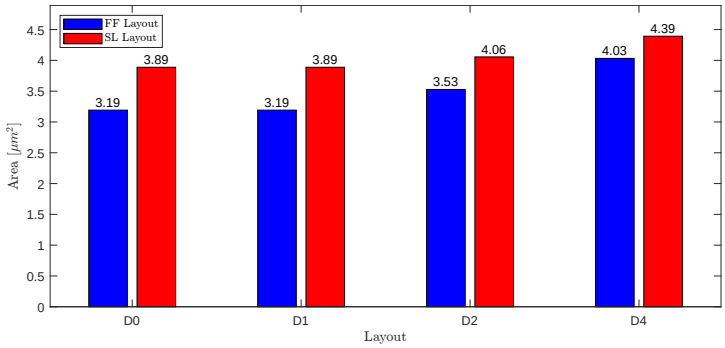


Figure 3.27: Flip flop versus Scan Latch layout area.

Although the cells are larger, it is important to note that these components will replace a macro structure containing three standard cells (a PTL, an NTL and a MUX cell), resulting in an overall area decrease.

Chapter 4

Conclusion

The presented thesis work lays out a complete route for designing and characterizing a standard cell, following all the required steps for future integration into EDA tools.

The designed Scan Latch cell exhibits the desired functionality and has no significant disadvantages compared to the macro-structure currently in use in the Mix&Latch methodology. Timing results are very promising while power measurements are slightly worse when compared to a reference cell. Nevertheless, the cell looks to be a successful design and is bound to be an improvement in the project.

The next step is the complete integration of the standard cell in the aforementioned workflow to verify its correct functionality and compatibility with the rest of the environment.

Chapter 5

Appendix

5.1 Timing Results

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.041880	0.043924	0.048190	0.055769	0.065518	0.077309	0.089858
0.001160	0.045712	0.047766	0.052030	0.059612	0.069374	0.081204	0.093754
0.003040	0.052245	0.054305	0.058574	0.066162	0.075925	0.087764	0.100325
0.006800	0.064757	0.066809	0.071066	0.078676	0.088463	0.100260	0.112827
0.014320	0.089596	0.091649	0.095906	0.103498	0.113213	0.125017	0.137608
0.029370	0.139297	0.141381	0.145728	0.153074	0.163198	0.174644	0.187500
0.059470	0.239487	0.241532	0.245450	0.253776	0.262355	0.274670	0.286958

Table 5.1: Scan Latch D0 cell rise results (ns)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.048089	0.050137	0.054538	0.061688	0.071532	0.082406	0.092914
0.001160	0.052134	0.054181	0.058580	0.066147	0.075588	0.086415	0.096953
0.003040	0.058857	0.060904	0.065303	0.072879	0.082310	0.093154	0.103670
0.006800	0.071711	0.073757	0.078151	0.085303	0.095119	0.105983	0.116519
0.014320	0.097045	0.099111	0.103524	0.111037	0.120589	0.131389	0.141913
0.029370	0.147714	0.149825	0.154290	0.161446	0.171216	0.182018	0.192716
0.059470	0.249656	0.251916	0.256474	0.263633	0.273676	0.284109	0.294300

Table 5.2: Scan Latch D0 cell fall results (ns)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.007686	0.007686	0.007647	0.007673	0.007686	0.007797	0.007983
0.001160	0.013508	0.013468	0.013555	0.013509	0.013547	0.013648	0.013705
0.003040	0.025709	0.025703	0.025691	0.025397	0.025353	0.025545	0.025717
0.006800	0.050325	0.050378	0.050477	0.049912	0.050695	0.050674	0.050649
0.014320	0.100645	0.100601	0.100413	0.101176	0.100797	0.100750	0.101210
0.029370	0.202841	0.202759	0.202216	0.204054	0.200861	0.202321	0.201739
0.059470	0.403340	0.403862	0.405470	0.406017	0.408408	0.407664	0.406508

Table 5.3: Scan Latch D0 rise transition results (ns)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.008318	0.008314	0.008261	0.008315	0.008263	0.008270	0.008162
0.001160	0.014282	0.014288	0.014300	0.014286	0.014305	0.014268	0.014242
0.003040	0.026735	0.026810	0.026856	0.026637	0.026477	0.026825	0.026868
0.006800	0.052694	0.052591	0.052495	0.052495	0.052147	0.052988	0.052296
0.014320	0.105573	0.105355	0.105132	0.106037	0.105008	0.106057	0.104892
0.029370	0.212572	0.212918	0.213154	0.213221	0.212637	0.213291	0.210667
0.059470	0.423888	0.425139	0.426069	0.426223	0.427179	0.421954	0.427381

Table 5.4: Scan Latch D0 fall transition results (ns)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.040100	0.042200	0.046500	0.053800	0.063100	0.074200	0.085900
0.002100	0.044600	0.046700	0.050900	0.058200	0.067600	0.078800	0.090500
0.005870	0.051700	0.053800	0.058100	0.065400	0.074700	0.085900	0.097700
0.013400	0.065200	0.067300	0.071500	0.078900	0.088300	0.099500	0.111000
0.028500	0.091900	0.094000	0.098200	0.106000	0.115000	0.126000	0.138000
0.058600	0.146000	0.148000	0.152000	0.159000	0.168000	0.179000	0.191000
0.119000	0.253000	0.256000	0.259000	0.268000	0.275000	0.287000	0.298000

Table 5.5: Scan Latch D1 cell rise results (ns)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.046731	0.048784	0.053158	0.060533	0.069598	0.079857	0.089647
0.002100	0.051755	0.053806	0.058183	0.065138	0.074616	0.084883	0.094757
0.005870	0.059743	0.061797	0.066176	0.073556	0.082632	0.092887	0.102750
0.013410	0.075033	0.077063	0.081444	0.088835	0.097940	0.108125	0.118063
0.028480	0.105300	0.107381	0.111768	0.119158	0.128265	0.138518	0.148297
0.058630	0.166113	0.168245	0.172639	0.180046	0.189031	0.199072	0.209027
0.118930	0.287723	0.289974	0.294395	0.301914	0.310762	0.321163	0.329833

Table 5.6: Scan Latch D1 cell fall results (ns)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.006846	0.006758	0.006768	0.006781	0.006807	0.006806	0.007087
0.002100	0.013312	0.013289	0.013296	0.013229	0.013246	0.013279	0.013456
0.005870	0.026615	0.026637	0.026583	0.026646	0.026504	0.026549	0.026717
0.013410	0.054100	0.054095	0.054108	0.053724	0.054021	0.053821	0.053867
0.028480	0.109020	0.110023	0.109355	0.109089	0.109294	0.109116	0.109870
0.058630	0.219551	0.222750	0.220590	0.220369	0.223144	0.222073	0.220239
0.118930	0.448648	0.448460	0.448941	0.446043	0.449684	0.441391	0.441726

Table 5.7: Scan Latch D1 rise transition results (ns)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.007561	0.007535	0.007588	0.007550	0.007534	0.007519	0.007513
0.002100	0.014907	0.014914	0.014909	0.014913	0.014988	0.014867	0.014773
0.005870	0.030151	0.030240	0.030227	0.030331	0.030319	0.030351	0.029842
0.013410	0.062294	0.062411	0.062411	0.062321	0.061425	0.062252	0.062031
0.028480	0.127381	0.127624	0.127631	0.127607	0.124969	0.124755	0.126996
0.058630	0.255464	0.256183	0.256323	0.256791	0.257785	0.255540	0.254903
0.118930	0.514500	0.516512	0.517283	0.518651	0.518696	0.516455	0.520245

Table 5.8: Scan Latch D1 fall transition results (ns)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.042023	0.044076	0.048326	0.055653	0.065007	0.076220	0.087943
0.003990	0.047145	0.049190	0.053443	0.060764	0.070128	0.081345	0.093117
0.011530	0.054513	0.056548	0.060816	0.068133	0.077495	0.088724	0.100492
0.026620	0.067839	0.069852	0.074143	0.081459	0.090831	0.102085	0.113813
0.056800	0.093942	0.095992	0.100339	0.107656	0.117047	0.128245	0.139970
0.117160	0.146696	0.148764	0.152796	0.160168	0.169341	0.180355	0.192578
0.237870	0.251102	0.253085	0.258243	0.265176	0.275562	0.284857	0.296851

Table 5.9: Scan Latch D2 cell rise results (ns)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.048563	0.050606	0.054993	0.061954	0.071372	0.081731	0.091704
0.003990	0.054292	0.056338	0.060728	0.068081	0.077100	0.087418	0.097282
0.011530	0.062433	0.064475	0.068884	0.075824	0.085302	0.095565	0.105396
0.026620	0.077486	0.079571	0.083950	0.091316	0.100367	0.110642	0.120603
0.056800	0.107282	0.109237	0.113729	0.121080	0.130001	0.140301	0.150280
0.117160	0.166624	0.168752	0.173270	0.180161	0.189634	0.199695	0.209516
0.237870	0.285591	0.287884	0.292546	0.299042	0.308450	0.319219	0.328390

Table 5.10: Scan Latch D2 cell fall results (ns)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.006606	0.006586	0.006540	0.006595	0.006728	0.006816	0.006874
0.003990	0.013267	0.013327	0.013276	0.013378	0.013374	0.013408	0.013566
0.011530	0.026238	0.026325	0.026153	0.026284	0.026552	0.026360	0.026620
0.026620	0.053367	0.053790	0.052863	0.053265	0.053868	0.052932	0.053838
0.056800	0.109625	0.109577	0.109276	0.109438	0.107648	0.107990	0.109645
0.117160	0.221710	0.221788	0.220746	0.221425	0.218768	0.217344	0.219650
0.237870	0.444483	0.444615	0.447010	0.445530	0.447416	0.442664	0.446487

Table 5.11: Scan Latch D2 rise transition results (ns)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.007245	0.007247	0.007272	0.007249	0.007250	0.007195	0.007164
0.003990	0.014766	0.014776	0.014732	0.014693	0.014823	0.014763	0.014656
0.011530	0.029990	0.029841	0.029871	0.029941	0.030236	0.029690	0.029874
0.026620	0.062288	0.061944	0.061194	0.061204	0.062107	0.061287	0.061141
0.056800	0.125760	0.127782	0.124986	0.125916	0.128312	0.125720	0.125829
0.117160	0.257611	0.254636	0.261098	0.254349	0.254440	0.256378	0.257030
0.237870	0.518994	0.512974	0.520740	0.518141	0.514543	0.514546	0.514339

Table 5.12: Scan Latch D2 fall transition results (ns)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.046766	0.048815	0.053069	0.060398	0.069743	0.080977	0.092789
0.007760	0.052556	0.054602	0.058850	0.066167	0.075584	0.086783	0.098681
0.022860	0.060412	0.062476	0.066713	0.074028	0.083447	0.094646	0.106574
0.053050	0.073872	0.075936	0.080144	0.087471	0.096897	0.108096	0.119940
0.113430	0.099835	0.101904	0.106032	0.113358	0.122780	0.133965	0.145893
0.234200	0.151176	0.153340	0.158006	0.165342	0.174748	0.185414	0.197786
0.475730	0.256032	0.258517	0.260832	0.268077	0.277720	0.290103	0.300340

Table 5.13: Scan Latch D4 cell rise results (ns)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.052828	0.054881	0.059263	0.066627	0.075593	0.085956	0.095838
0.007760	0.059349	0.061406	0.065786	0.073152	0.082125	0.092474	0.102337
0.022860	0.068202	0.070252	0.074632	0.081975	0.091017	0.101324	0.111162
0.053050	0.083874	0.085918	0.090246	0.097611	0.106648	0.116949	0.126811
0.113430	0.114596	0.116492	0.121039	0.128303	0.137386	0.147678	0.157486
0.234200	0.176122	0.178021	0.182469	0.189796	0.198618	0.208706	0.219118
0.475730	0.299033	0.301151	0.305095	0.312928	0.321167	0.331570	0.340657

Table 5.14: Scan Latch D4 cell fall results (ns)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.008305	0.008377	0.008265	0.008326	0.008285	0.008409	0.008539
0.007760	0.015151	0.015111	0.015226	0.015222	0.015198	0.015200	0.015406
0.022860	0.028208	0.028090	0.028172	0.028249	0.028105	0.028185	0.028251
0.053050	0.054997	0.055069	0.054741	0.054737	0.054226	0.054401	0.054564
0.113430	0.107870	0.108549	0.109773	0.109800	0.109957	0.109306	0.109704
0.234200	0.217547	0.218852	0.221069	0.221070	0.220656	0.219934	0.218676
0.475730	0.444409	0.444606	0.441184	0.440563	0.438797	0.444142	0.435280

Table 5.15: Scan Latch D4 rise transition results (ns)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.008578	0.008616	0.008627	0.008627	0.008545	0.008541	0.008529
0.007760	0.016681	0.016635	0.016610	0.016601	0.016657	0.016646	0.016603
0.022860	0.032106	0.032551	0.032602	0.032265	0.032085	0.032280	0.032347
0.053050	0.064005	0.064808	0.065405	0.065314	0.064907	0.064371	0.065208
0.113430	0.132119	0.133758	0.130615	0.131962	0.131501	0.132270	0.131947
0.234200	0.270097	0.264473	0.270954	0.264869	0.267088	0.266635	0.266747
0.475730	0.546179	0.536914	0.538942	0.537074	0.531600	0.532118	0.537457

Table 5.16: Scan Latch D4 fall transition results (ns)

5.2 Power results

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.003603	0.003583	0.003542	0.003527	0.003563	0.003786	0.004425
0.001160	0.003601	0.003587	0.003555	0.003521	0.003575	0.003758	0.004440
0.003040	0.003606	0.003588	0.003671	0.003532	0.003566	0.003798	0.004443
0.006800	0.003609	0.003601	0.003575	0.003554	0.003574	0.003812	0.004457
0.014320	0.003635	0.003617	0.003590	0.003553	0.003605	0.003850	0.004464
0.029370	0.003581	0.003565	0.003537	0.003520	0.003546	0.003782	0.004471
0.059470	0.003586	0.003570	0.003538	0.003508	0.003554	0.003781	0.004437

Table 5.17: Scan Latch D0 rise power results (pJ)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.003767	0.003737	0.003729	0.003751	0.003774	0.003964	0.004458
0.001160	0.003780	0.003760	0.003746	0.003733	0.003776	0.003994	0.004470
0.003040	0.003789	0.003770	0.003757	0.003732	0.003800	0.003992	0.004486
0.006800	0.003788	0.003769	0.003757	0.003773	0.003808	0.004002	0.004493
0.014320	0.003795	0.003776	0.003763	0.003745	0.003806	0.004009	0.004499
0.029370	0.003795	0.003776	0.003763	0.003780	0.003799	0.004007	0.004499
0.059470	0.003792	0.003773	0.003760	0.003777	0.003808	0.004014	0.004492

Table 5.18: Scan Latch D0 fall power results (pJ)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.003835	0.003804	0.003793	0.003755	0.003802	0.004036	0.004535
0.002100	0.003857	0.003849	0.003805	0.003778	0.003827	0.004033	0.004754
0.005870	0.003877	0.003857	0.003815	0.003797	0.003846	0.004079	0.004669
0.013400	0.003882	0.003863	0.003832	0.003781	0.003862	0.004051	0.004790
0.028500	0.003869	0.003832	0.003820	0.003788	0.003810	0.004075	0.004768
0.058600	0.003897	0.003881	0.003847	0.003820	0.003856	0.004084	0.004801
0.119000	0.003825	0.003804	0.003775	0.003736	0.003775	0.003986	0.004748

Table 5.19: Scan Latch D1 rise power results (pJ)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.003992	0.003972	0.003962	0.003933	0.004009	0.004230	0.004797
0.002100	0.004024	0.004001	0.003984	0.004005	0.004032	0.004250	0.004788
0.005870	0.004044	0.004020	0.004004	0.003983	0.004048	0.004270	0.004807
0.013400	0.004052	0.004027	0.004011	0.003998	0.004069	0.004280	0.004819
0.028500	0.004054	0.004028	0.004012	0.003991	0.004064	0.004293	0.004823
0.058600	0.004062	0.004037	0.004015	0.004004	0.004079	0.004280	0.004830
0.119000	0.004057	0.004027	0.004012	0.004009	0.004071	0.004291	0.004821

Table 5.20: Scan Latch D1 fall power results (pJ)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.004451	0.004424	0.004406	0.004350	0.004400	0.004619	0.005149
0.003990	0.004485	0.004460	0.004431	0.004397	0.004459	0.004643	0.005174
0.011530	0.004544	0.004534	0.004514	0.004473	0.004510	0.004698	0.005238
0.026620	0.004554	0.004557	0.004518	0.004488	0.004510	0.004740	0.005261
0.056800	0.004550	0.004530	0.004507	0.004576	0.004520	0.004867	0.005256
0.117160	0.004699	0.004680	0.004625	0.004713	0.004634	0.004879	0.005608
0.237870	0.004450	0.004432	0.004404	0.004363	0.004411	0.004609	0.005205

Table 5.21: Scan Latch D2 rise power results (pJ)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.004634	0.004598	0.004592	0.004604	0.004636	0.004867	0.005435
0.003990	0.004670	0.004643	0.004634	0.004608	0.004675	0.004899	0.005466
0.011530	0.004706	0.004682	0.004677	0.004688	0.004728	0.004968	0.005492
0.026620	0.004738	0.004716	0.004695	0.004676	0.004754	0.004967	0.005506
0.056800	0.004753	0.004726	0.004719	0.004692	0.004762	0.004984	0.005553
0.117160	0.004754	0.004735	0.004714	0.004737	0.004773	0.004992	0.005554
0.237870	0.004751	0.004730	0.004716	0.004708	0.004771	0.004973	0.005574

Table 5.22: Scan Latch D2 fall power results (pJ)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.005952	0.005833	0.005794	0.005747	0.005890	0.006112	0.006722
0.007760	0.005881	0.005868	0.005822	0.005780	0.005919	0.006072	0.006646
0.022900	0.005927	0.005920	0.005873	0.005822	0.005959	0.006185	0.006732
0.053100	0.005991	0.005961	0.005940	0.005892	0.005989	0.006301	0.006841
0.113000	0.006496	0.006383	0.006358	0.006286	0.006408	0.006795	0.007276
0.234000	0.006227	0.006197	0.006180	0.006132	0.006239	0.006514	0.007372
0.476000	0.005855	0.005836	0.005804	0.005754	0.005861	0.006010	0.006808

Table 5.23: Scan Latch D4 rise power results (pJ)

Cload	t=2e-12	t=1.19e-11	t=3.18e-11	t=7.15e-11	t=1.51e-10	t=3.1e-10	t=6.28e-10
0.000220	0.005963	0.005940	0.005935	0.005901	0.005964	0.006290	0.006733
0.007760	0.005986	0.005971	0.005962	0.005933	0.005997	0.006242	0.006773
0.022900	0.006075	0.006057	0.006045	0.006028	0.006068	0.006323	0.006854
0.053100	0.006134	0.006128	0.006115	0.006093	0.006161	0.006408	0.006933
0.113000	0.006182	0.006158	0.006157	0.006130	0.006197	0.006508	0.006963
0.234000	0.006196	0.006185	0.006177	0.006152	0.006192	0.006455	0.006975
0.476000	0.006208	0.006186	0.006181	0.006152	0.006220	0.006539	0.006982

Table 5.24: Scan Latch D4 fall power results (pJ)

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