POLITECNICO DI TORINO

Master's Degree in Biomedical Engineering



Master's degree thesis

Hardware test system for the development of implantable nerve recording and stimulation interfaces

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September 2026

Abstract

This thesis presents the design and implementation of a custom hardware platform to validate the Intan RHS2116 and Intan RHD2132 integrated circuits for neural stimulation and acquisition.

A dedicated Printed Circuit Board (PCB) was developed as a shield for the STM Nucleo-H723ZG development board. The shield generates the voltage supplies required by the Intan headstages. It routes the Serial Peripheral Interface (SPI) communication bus from the microcontroller through two onboard Low-Voltage Differential Signalling (LVDS) transceivers.

To emulate the electrical behaviour of a peripheral nerve coupled with a multi-contact cuff electrode, a finite element model was first developed in COMSOL Multiphysics and its impedance Bode plot extracted. Based on this model, an equivalent RC network was designed in LTspice to reproduce the target impedance response. Over the 100 Hz–10 kHz frequency range, the LTspice and COMSOL models exhibited maximum impedance magnitude and phase deviations of 38.1% and 7.1°, respectively. The model was then extended by incorporating the electrode-electrolyte interface dynamics derived from NerveRepack experimental data and implemented on a dedicated PCB, referred to as the Passive Nerve Testbed (PNT).

The integration of the PCB shield and the PNT board, which interface with the Intan headstages, resulted in a comprehensive test bench for functional validation. The evaluation of the setup was tailored to the specific headstage in use. For the RHD chip, the testing involved 1000 iterations of a 1 kHz impedance check across a target range of 390 Ω to 6.8 kΩ. The results demonstrated that the relative error of the calculated mean, compared to the nominal value, remained strictly below 5%, with a maximum standard deviation of 13.61 Ω. To evaluate the RHS chip, standard clinical current stimuli were applied to the PNT board, showing a maximum deviation of 13.4% in the peak-to-peak output voltage relative to the model simulated in LTspice using an ideal current source.

In conclusion, this custom hardware provides a testing environment for evaluating impedance checks and response to current stimuli, laying a preliminary foundation for upcoming in vivo and ex vivo experiments.

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Chapter 1

Introduction

Nowadays, the global prevalence of Peripheral Nerve Injuries (PNIs) is estimated to be 2400 to seven thousand per one hundred thousand individuals, severely affecting patient mobility, autonomy, and physical deterioration [1]. The upper extremities are particularly susceptible to these types of lesions; in the US, about 2.6% of all arm injuries are caused by nerve damage [2]. Highlighting this vulnerability, comprehensive research conducted in a European Level I trauma center found that more than 88% of peripheral nerve injuries occur in arms and hands, with the median and ulnar nerves the most frequently affected [3]. In case surgical treatments fail to restore motor function or if the injury is irreversible, amputation is a possibility for the patient. About 13 million new amputations occur in a year, whereof 5% involved the upper limb above the wrist [4]. There has been limited use of prosthetic devices in clinical practice to address this major motor deficit due to the high abandonment rate of myoelectric prostheses observed over the past 25 years [5]. The major limitation of current commercial myoelectric systems is that they do not provide sensory feedback to the user and translate their motor intentions only into mechanical actions [5]. This highlights the need to develop more advanced neuroprostheses and neural interfaces to restore somatosensory input and intuitive motor control, allowing prosthetics to be natural extensions of the body.

1.1 Aim of the study

This work is developed within the framework of two main international research projects, NerveRepack and ReWiRe, in which the eLiONS research group from the Department of Electronics and Telecommunications at Politecnico di Torino participates. Both projects aim to restore motor and sensory functions following peripheral nerve injuries, employing distinct yet technologically overlapping approaches.

NerveRepack is a European research project joined by several partners focused

on the design and development of advanced implantable neural interfaces capable of establishing a bidirectional communication channel between the human nervous system and external mechatronic devices, such as exoprostheses and exoskeletons. The main proposal is to re-establish the physical connection between severed neural pathways and artificial limbs, providing users with both direct motor control and coherent sensory feedback [6]. The technological system of NerveRepack is based on a closed-loop architecture driven by bidirectional implantable electrodes. These interfaces connect the healthy nerve segments directly to external exoprostheses or exoskeletons, bypassing the physiological interruptions caused by amputation or paralysis. As shown in Figure 1.1, the hardware includes an implantable module with an Application-Specific Integrated Circuit (ASIC), a microcontroller, an antenna for radio communication, and a coil with a supercapacitor for wireless power transfer (WPT) and energy storage. In addition, a specific embedded system is integrated into the prosthesis, which is responsible for data transmission, power control, and Artificial Intelligence (AI) applications. These AI algorithms are trained to read the neural motor signals and translate them into mechanical commands, while also sending the environmental information from the robotic sensors back to the peripheral nerves [7].

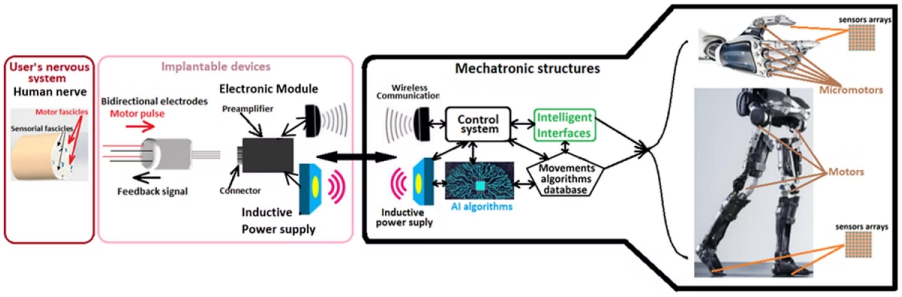


Figure 1.1: NerveRepack closed-loop architecture. The left side shows the human nerve and the implantable system that is formed by bidirectional electrodes and an electronic module for signal preamplification. Through inductive power transfer and wireless communication links, this internal part connects to the right side of the mechatronic structure. The external mechatronic architecture has a central control system, with artificial intelligence algorithms, that controls robotic exoprostheses equipped with micromotors and sensor arrays [7].

ReWiRe is in partnership with Politecnico di Milano and Ulsan National Institute of Science and Technology. It addresses the clinical context, where natural nerve regeneration or standard surgical reconstructions are often unable to provide a functional recovery due to severe peripheral nerve injuries. ReWiRe aims to create a permanent internal bioelectronic functional bypass to overcome nerve discontinuity and restore limb mobility by acquiring neural signals from the proximal nerve segment, processing them to extract specific motor intentions, and stimulating the

distal portion to obtain motor outputs. This objective is pursued through a novel implantable 'Neural Decode and Forward' (ND&F) system (Figure 1.2) that electronically bridges the anatomical lesion. The system is based on a multi-contact cuff electrode placed close to the injury site that records residual electromyographic (ENG) activity. The recorded data consists of aggregated signals from different nerve fibers, and the MIMO decoding and spiking machine learning algorithm is used to separate the fascicle signals and classify them. Once separated, the motor intentions are transmitted to the target nerve, restoring the interrupted neural pathway. To ensure reliable long-term operation without the physical constraints and safety risks of implanted batteries, the device is based on a custom WPT architecture [8].

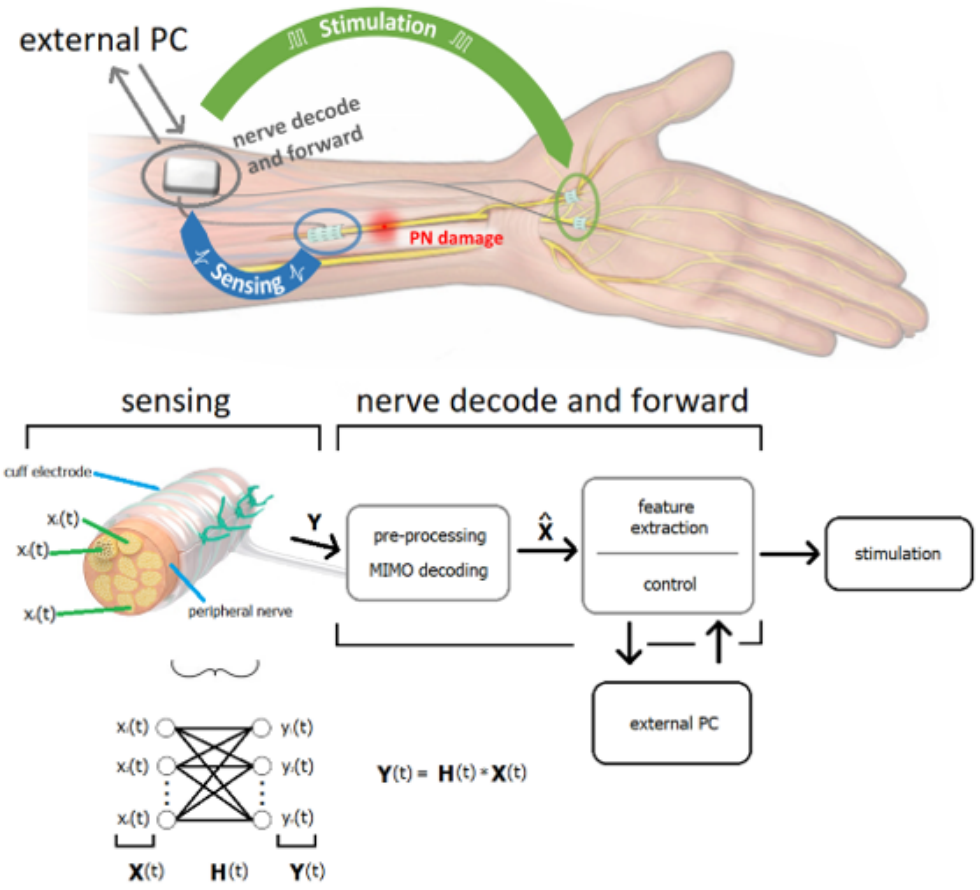


Figure 1.2: Architecture of the ReWiRe bioelectronic bypass bridging a peripheral nerve injury. A proximal multi-contact cuff electrode acquires neural signals from the healthy nerve segment. The central Neural Decode and Forward system processes the aggregated data via MIMO decoding and feature extraction blocks. The unit translates the classified motor intentions into specific commands for distal nerve stimulation, restoring the interrupted neural pathway.

In the NerveRepack and ReWiRe projects, the research group is responsible for developing and testing the implementable device. One of the key requirements of both systems is the recording of low-amplitude neural signals and the correct stimulation. Intan Technologies integrated circuits have been chosen: the RHD2132 headstage for neural recording and the RHS2126 headstage for simultaneous recording and stimulation. The initial laboratory setup was based on generic Low-Voltage Differential Signalling (LVDS) Transceiver adapter boards connected to the main microcontroller STM32 Nucleo H7 through male-to-male jumpers for a single-ended SPI connection. This setup introduces a lot of noise to the system, mechanical instability, and signal degradation, thus not allowing for a low-noise environment for biological data processing.

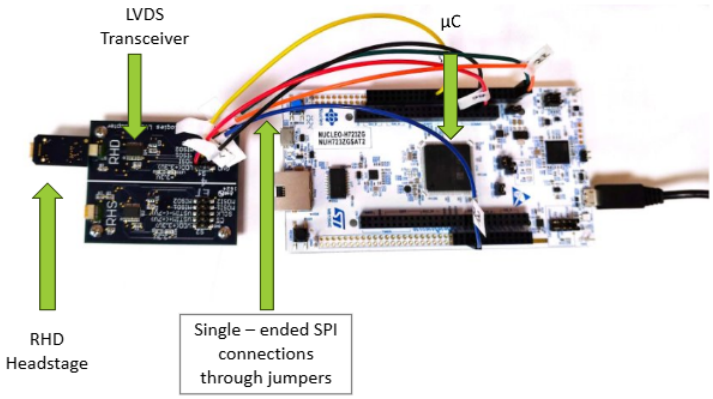


Figure 1.3: Starting setup

The intended goal of this work is to design low-noise hardware to power and connect the Intan neural chips. This is achieved by a dedicated Printed Circuit Board (PCB) consisting of a shield able to provide a direct and low-noise SPI connection between the headstages and the microcontroller development kit. The shield will be responsible for generating and routing the correct logic and bipolar stimulation power supplies for the different architectures of the NerveRepack and ReWiRe projects. Furthermore, to verify the integrated circuits, a PCB will be built to mimic the electrical impedance of a peripheral nerve coupled with an implanted electrode. By providing an equivalent biological electrical model, this circuit provides a reliable testbench to evaluate the performance of the whole system.

Chapter 2

State of art

2.1 Bidirectional nerve interfaces

Bidirectional peripheral nerve interfaces are a revolution in modern neuroengineering and bioelectronics. These systems are designed not only to record neural signals from the peripheral nervous system but also to provide specific electrical stimulation. By recording motor signals and stimulating sensory nodes, these systems seek to restore artificial sensation such as proprioceptive and tactile feedback in individuals with limb differences [9].

Conceived as a chronic research platform for freely behaving small animals, the SenseBack project [10] aims to develop enabling technologies to restore sensory feedback, such as touch and proprioception, in assistive devices like prosthetic hands. The authors have designed a system with compliance voltages up to ± 20 V to drive currents through different tissue impedances and to achieve high performance with a small footprint. The hardware is divided into specialized functional nodes (Figure 2.1). The implant is developed using a rigid-flex printed circuit board (PCB) that separates the neural interface from the power and communication modules. At the core of the design lies an ASIC to control the 32-channel bidirectional analog front end. The primary chip is supported by a field-programmable gate array (FPGA) to provide a fast-moving buffer and a low-power Bluetooth microcontroller for wireless data transmission. To accommodate the demanding power requirements, the implant incorporates integrated wireless power receivers and boost converters. This modular hardware topology allows for an optimal distribution of physical components: the bulkier wireless and power interfaces are positioned in a less constrained anatomical region, while only the miniaturized sensing node is routed directly to the target peripheral nerve.

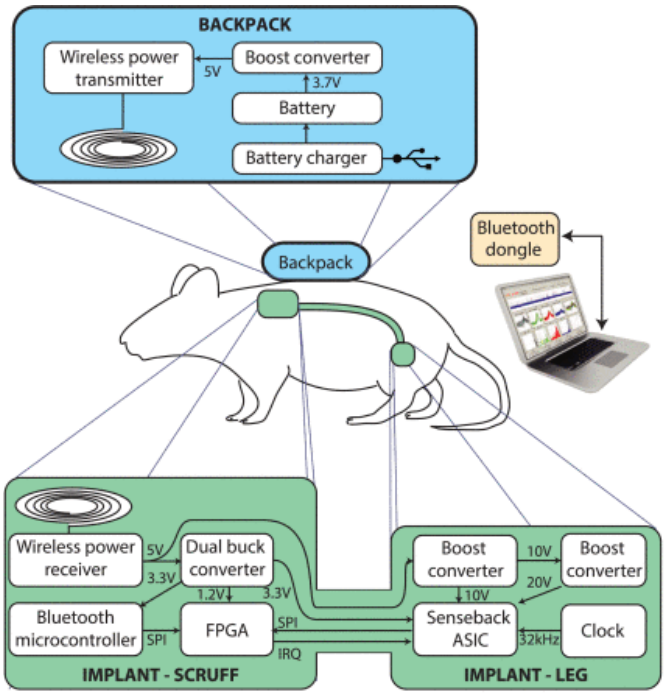


Figure 2.1: System architecture of the SenseBack research platform. The diagram shows hardware grouped into different functional nodes. An external backpack transmits power to the implantable scruff module, which contains the FPGA and Bluetooth microcontroller for wireless data transfer. The power and digital signals are sent to the leg implant, which is the center of the ASIC and boost converters to produce high compliance voltages for the neural interface.

2.2 RHD/RHS Intan Technologies chips

The validation of peripheral nerve interface depends on the availability of robust, low-noise, and reliable data acquisition and stimulation hardware. In current bioelectronic research, the application of Intan Technologies integrated circuits is the standard for electrophysiology studies. These devices are widely adopted due to their compact footprint and integrated digital conversion capabilities. Yan et al. [11] used the Intan RHD2216 16-channel amplifier board to validate a new ultra-flexible Microneedle Nerve Array (MINA). In acute in vivo experiments, the RHD system successfully acquired intrafascicular neural signals from the rat peroneal nerve. The recording platform was able to resolve action potentials with peak-to-peak amplitudes between 23 and 40 µV with a signal-to-noise ratio of 9.74 dB after applying a digital band-pass filter. Hiendlmeier et al. [12] used the RHS2116 headstage to characterize a 4D-printed self-folding cuff electrode for small peripheral

nerves. The RHS2116 chip was used in the laboratory to apply in vivo stimulation and recording on the Locust metathoracic nerve. The RHS2116 chip delivered precise biphasic current pulses (Figure 2.2) to produce motor responses, while simultaneously recording both efferent and afferent neural activity at a sampling rate of 30 ksps.

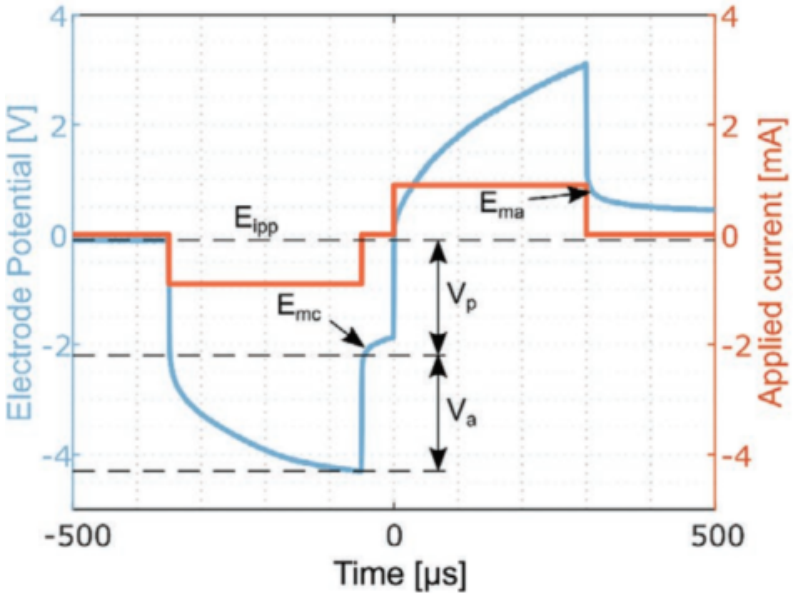


Figure 2.2: The transient electrical response of the electrode-tissue interface to a biphasic constant current stimulation pulse is shown [12]. The orange trace shows the applied current waveform produced by the RHS2216. The blue trace shows the resulting electrode potential. In the voltage profile, the initial resistive voltage drop (V a), capacitive polarization (V p), maximum cathodic potential (E_{mc}), and maximum anodic potential (E_{ma}).

Although commercial Intan development boards are suitable for basic validations, the integration of these chips into highly specific experimental setups requires a significant custom hardware design. Jacobs et al [13] have recently developed the Iris 128x, an open-source architecture that incorporates RHD2164 and RHS2116 integrated circuits. Their work clearly illustrates the physical engineering requirements for routing and powering such advanced ASICs at the hardware level. The chips require a standard 3.3V supply for digital logic and analog operation, and the RHS stimulator circuitry needs to use a bipolar power supply ranging from $\pm$3.3 V to $\pm$7 V. Since the stimulation across 128 electrodes can easily overwhelm a standard controller's power rails, Jacobs et al also require an external DC power supply to carry the current. In addition, as illustrated in Figure 2.3, their hardware design includes dedicated adapter boards equipped with a Power Management Unit (PMU) to supply the higher voltages needed for the auxiliary components directly

from the main 3.3V supply. To protect the signal integrity at the PCB level, power lines are routed on special internal layers and covered by copper ground planes to protect the sensitive analog biological signals from the power supply noise. Besides power, to ensure reliable and fast data transfer from the headstage to the main controller, Low Voltage Differential Signaling (LVDS) is implemented on the SPI communication lines to reduce EMI and prevent digital noise.

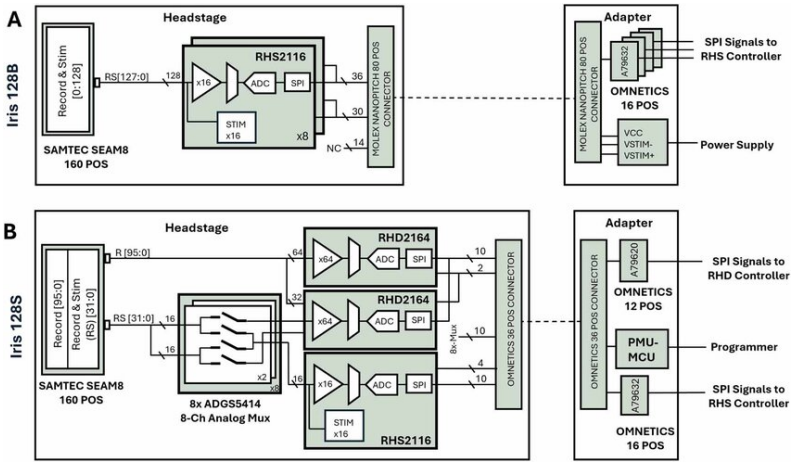


Figure 2.3: System-level block diagrams of Iris open-source neural interfaces [13]. (a) Architecture of the Iris 128B headstage and adapter board. 8 RHS2116 chips form a headstage with 128 bidirectional channels for recording and stimulation. SPI lines are routed to the RHS controller from the adapter, which contains VCC, VSTIM+ and VSTIM- power connections. (B) Architecture of the Iris 128S headstage and adapter board. This hybrid design uses two 64-channel RHD2164 chips for neural recording and one 16-channel RHS2116 chip for recording and stimulation. An array of eight ADGS5414 analog multiplexers distributes the 16 stimulation channels over 32 target electrodes. An Omnetics 36-position connector bridges the headstage and the adapter. The adapter splits the SPI signals into distinct RHD and RHS controller interfaces and integrates a Power Management Unit and a microcontroller.

2.3 Electrode-nerve coupling

One of the most important aspects of developing bidirectional neural interfaces is modeling the electrode-nerve coupling. Once the custom hardware architecture with the stimulation and acquisition chips is realized, it is crucial to verify it before performing in vivo trials. While preliminary benchtop tests often rely on simple resistive loads, these simple components can't account for the complex, frequency-dependent, and electrochemical nature of biological tissues.

2.3.1 Electrode-electrolyte coupling

Placed in a physiological medium, a metal electrode creates a direct physical boundary between the two phases. The charge in the metal electrode and its associated circuits is carried only by electrons, while in the physiological electrolyte it is carried by ions such as sodium, potassium, and chloride. Consequently, the main physiological mechanism in the electrode-electrolyte interface during stimulation is the transfer of charge carriers from electrons in the metal to ions in the biological medium [14]. According to the physical laws of electrochemistry, there are two main mechanisms for charge transfer at this interface (Figure 2.4a). The first one is capacitive or non-Faradaic, and the electrons are not transferred from the electrode to the electrolyte. Instead, the charge injection is due to redistributing charged chemical species in the solution in a reversible way so that opposite charges are aligned at the metal surface to form a double layer. Since the process is reversible and does not change the chemical composition of the medium, it is electrically described by a capacitor, C_{dl}. The second mechanism is Faradaic charge transfer, which involves the direct transfer of electrons across the interface, reducing or oxidizing the chemical species in the electrolyte. Electrically, this is represented by a Faradaic impedance, which acts as a charge dissipation pathway. Faradaic reactions can be reversible, e.g., localized oxidation of the oxide in water, or irreversible, for example, oxidation or reduction of the water that leads to gas evolution [14].

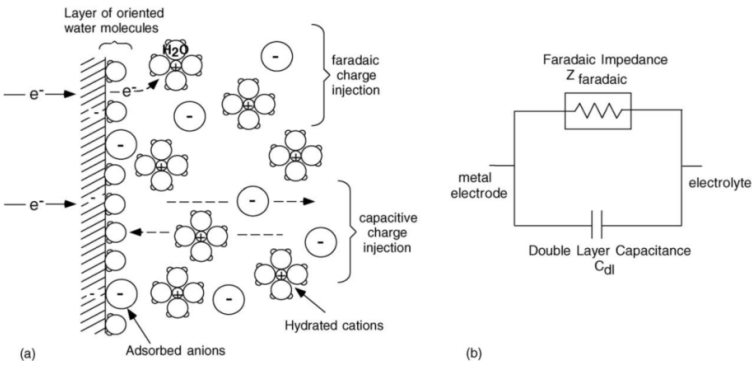


Figure 2.4: The electrode/electrolyte interface, illustrating Faradaic charge transfer (top) and capacitive redistribution of charge (bottom). (a) physical representation; (b) two-element electrical circuit model for mechanisms of charge transfer at the interface.

These irreversible Faradaic reactions result in a net change in the local chemical environment, which can lead to toxic species harmful to both the surrounding excitable tissue and the electrode itself. Electrical equivalent circuits are therefore needed to translate these physiological and electrochemical phenomena into functional engineering tools. The physical double layer formed by opposite charges is

described by the capacitance C_{dl} (Figure 2.4b). However, the interface is not a perfect insulator: the charge that manages to leak across this boundary to participate in the Faradaic electrochemical reactions encounters a natural opposition. In the electrical model, this specific opposition to electron transfer is defined as the charge transfer resistance (R_{ct}) (Figure 2.4b). In addition, these Faradaic reactions are based on ions diffusing from the bulk of the electrolyte to the interface at a finite rate, which gives rise to the Warburg impedance, mathematically expressed as $Z_w = (1 - j)\sigma\omega^{-0.5}$ where σ is the diffusion coefficient and ω is the angular frequency of the applied signal [15]. The diffusion and the charge transfer resistance form the Faradaic branch of the circuit in parallel to the double layer capacitance.

Current literature approaches the characterization of the electrode-electrolyte interface through standard empirical methods rather than purely theoretical models. The established procedure involves immersing the fabricated electrode in a saline solution and performing Electrochemical Impedance Spectroscopy (EIS). In their study on electrical impedance tomography, J. Hope et al. demonstrate this procedure by immersing nerve cuff electrodes in a phosphate-buffered saline solution and recording impedance measurements across a 5 Hz to 50 kHz frequency sweep. By analyzing the resulting spectral data, they establish that the physical fluid-metal interaction can be accurately abstracted into a simplified electrical equivalent. Specifically, they fit their bench-top measurements directly to a parallel network comprising an electrode capacitance (C_e) and an electrode resistance (R_e), proving that experimental saline bath data provide the exact lumped parameters [16].

2.3.2 Pheripheral nerve modelling

In addition to the electrode-electrolyte interface, it is important to consider the contributions of the nerve itself and its tissue layers. Most neuroprosthetic research relies on computational modeling, specifically the Finite Element Method (FEM) in environments such as COMSOL Multiphysics, to study peripheral nerves and their unique morphology and physiology. One of the most robust and important contributions to this field is ASCENT (Automated Simulations to Characterize Electrical Nerve Thresholds) [17]. ASCENT is a unified, modular, high-performance software pipeline to automate the complex multi-step process of the electrical activation and block of peripheral nerves. The pipeline integrates Python, Java, COMSOL Multiphysics, and the NEURON simulation environment to simulate how a real nerve reacts to a stimulus. The modeling workflow (Figure 2.5) begins by defining the physical anatomy of the nerve, allowing users to input segmented histological images for a highly accurate, sample-specific model or use a built-in generator to mathematically define an elliptical nerve populated with explicitly placed or probabilistically distributed fascicles [18]. Following the morphological definition,

Python outputs 2D CAD files to define the tissue boundaries, and the pipeline provides a 3D modeling toolset for the electrode interface. This enables researchers to choose from a library of commercially available cuff electrodes or create their own designs by using very basic parts for the metal contacts, the insulating cuff, and the surrounding fill material. Once the geometry is established, ASCENT uses a Java interface to enable COMSOL to generate an unstructured 3D mesh and assign different electrical conductivities to tissue layers and electrode materials. Once the geometry is established, ASCENT utilizes a Java interface to command COMSOL to generate an unstructured 3D mesh and assign specific electrical conductivities to the different tissue layers and electrode materials.COMSOL then solves Laplace's equation to map out the exact extracellular electrical potentials generated when a current is applied to the contacts [18]. After transferring these data, Python maps the coordinates of the target nerve fibers and mathematically provides the stimulation waveforms over time. Electrical potentials along the length of the nerve are fed into NEURON, a sophisticated biophysical cable model of individual myelinated or unmyelinated fibers, to determine when and how the simulated neurons are activated or blocked in response to the current injected [18].

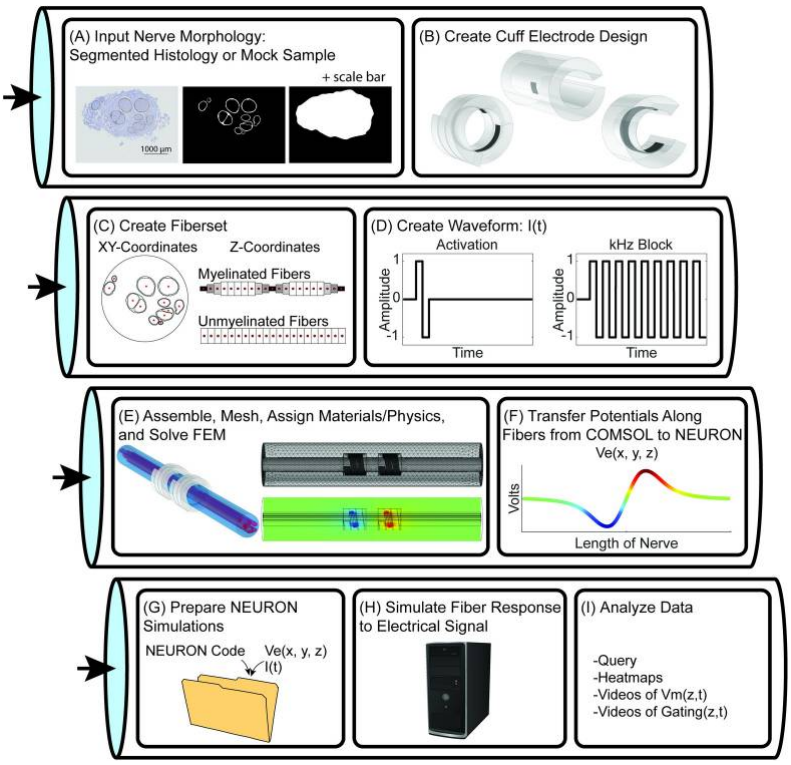


Figure 2.5: Overview of the ASCENT pipeline for simulating the response of sample-specific nerves to electrical stimulation with custom cuff electrodes and stimulation waveforms.

One of the most significant studies utilizing the ASCENT pipeline is the work by Musselman et al.[19], which investigated vagus nerve stimulation. This work aimed to provide a valid model for designing electrode geometry and stimulation waveforms to achieve the best therapeutic outcomes while minimizing common clinical side effects (e.g., laryngeal muscle activation or bradycardia). For this purpose, the nerve was anatomized and reconstructed in the FEM, outlining its different biological layers: epineurium, endoneurium, perineurium, and surrounding environments (muscle tissue, saline, chronic encapsulation tissue). Each of these specific anatomical domains was assigned a distinct, biophysically realistic electrical conductivity. For example, the perineurium, which acts as a highly resistive physiological barrier to electrical current, was modeled either as a volumetric conductive domain for complex fascicles or as a specialized surface impedance layer based on the fascicle's effective diameter. This meticulous assignment of material properties ensured that the simulated current's path through the nerve mirrored reality as closely as possible [19] . By driving specific currents through the appropriate tissue conductivities, the study demonstrated that the individual differences in nerve morphology and tissue layer dimensions are the primary reasons why the same electrical dose can lead to different threshold responses in different subjects, further highlighting the potential of the ASCENT pipeline, which can automatically reconstruct the exact nerve geometry starting directly from histological images. While such advanced computational pipelines like ASCENT focus on the morphological and topographical modelling of peripheral nerves, they present a biophysical limitation: the oversimplification of the tissues' capacitive effects. These models have treated nerve layers as predominantly resistive, largely ignoring how their electrical behaviour fluctuates across different frequencies. Actually, the electrical properties of biological tissues are highly frequency-dependent; failing to conduct a proper frequency-domain analysis obscures how the overall impedance of the electrode-nerve system dynamically changes in response to the specific spectral content of the applied stimulus. This is an absolute engineering necessity for the accurate design, impedance matching, and tuning of the actual stimulation and acquisition chips. To overcome the problem of a realistic model, it is important to assign accurate mammalian values for the resistivity and dielectric constant to several nerve layers. A foundational breakthrough in this field was made by Horn et al. The intrinsic electrical properties of the mammalian peripheral nerve laminae were characterized using complex electrochemical impedance spectroscopy. Before this work, most of the computational modeling community had been working with a resistive parameter set dating back to 1984 based on amphibian models (e.g., frog sciatic nerve). Horn et al. used a custom characterization chamber and a four-point impedance setup throughout the range of frequencies from 10 mHz to 50 kHz and fit the impedance spectra with the equivalent circuit model. This allowed them to represent the complex impedance of the nerve and to distinguish the contributions of epineurium, perineurium, and endoneurium. They were able to obtain geometrically independent bulk material

properties which can be applied to any nerve model. The longitudinal resistivity of the endoneurium was determined to be primarily resistive in the order of 0.97 Ω·m. They estimated the relative permittivity of the perineurium to be around 2018 and the resistivity to be 3751.3 Ω·m. Even more startlingly, the epineurium had a large relative permittivity of about 9.4×10^6 and a resistivity of 55.0 Ω·m. [20] Most importantly, high permittivity values bring the "corner frequencies": the exact frequency at which the tissue's capacitive reactance peaks and begins to short its electrical resistance, right into the standard bioelectric operating bandwidth. The authors identified these critical corner frequencies at approximately 2.6 kHz for the perineurium and 368 Hz for the epineurium. Because these thresholds fall squarely within the operational frequencies of typical neural interfaces, assuming a purely resistive model or utilizing the relative permittivity of standard saline (around 80) leads to massive simulation errors and fails to capture the true transient behaviour of the nerve [20]. Adopting the stable bulk values for resistivity and relative permittivity established by Horn et al., and coupling them with the powerful geometric generation capabilities of the ASCENT pipeline in COMSOL, constituted the initial steps for the FEM simulations developed in this work. How these foundational biophysical parameters and precise anatomical models were practically combined to build a complete frequency-domain analysis of the electrode-nerve interface will be thoroughly explored and expanded upon in the subsequent chapters.

2.4 Pheripheral nerve stimulation

The efficacy of peripheral nerve stimulation is highly dependent on the particular electrical stimulus. The frequency and the pulse width of the stimulation is not universal; it is strongly influenced by the anatomical target,different species model, and the electrode type. In a wide range of bioelectronic applications, the charge-balanced biphasic rectangular current pulse is commonly used as the gold standard waveform. The main reason for this choice is electrochemical safety: charge balancing prevents toxic byproducts and irreversible tissue damage and protects delicate electrode materials such as gold and platinum from damage over time [21], [22], [23], [24], [25], [26]. To further optimize the waveform, a short inter-phase delay (e.g., 100 µs) is sometimes introduced to prevent the secondary recovery phase from immediately extinguishing the action potential generated by the active phase [22]. The frequency of stimulation is the key component of the macroscopic physiological response, and its selection is highly dependent on whether the goal is diagnostic mapping, functional movement, or autonomic modulation. The low frequencies, typically between 1 Hz and 4 Hz, are diagnostic. These frequencies are used to isolate single muscle twitches without creating tetanic fusion, which allows researchers to map electrode selectivity and record precise compound muscle action potential (CMAP) recruitment curves, avoiding muscle fatigue during calibration [23], [24]. Medium frequencies, between 24 Hz and 30 Hz, are better for long-term functional

and autonomic modulation. In vagus nerve stimulation (VNS), 30 Hz is an established physiological standard to reliably saturate nerve responses and induce acute, measurable autonomic effects, such as bradycardia [21]. In motor neuroprosthetics for human patients, 24 Hz is the ideal balance: it is high enough to induce a smooth, tetanic contraction for functional grasping but low enough to postpone muscle fatigue and to facilitate complex muscle synergies [22]. In animal models, higher frequencies are required for specific kinematic outcomes. For instance, in rodents, 100 Hz is needed for the muscle twitches to completely fuse into a smooth and sustained kinematic movement of the limb [26]. At the extreme end of the spectrum, ultra-high frequencies of 1 kHz are employed to induce massive, fast depolarizations, thus mimicking explosive physiological commands like the jumping reflex in locusts [25]. The pulse width also needs to be tuned to the desired spatial selectivity and target nerve fibers. Low pulse widths (10 to 20 µs) are used for researchers who want the highest spatial selectivity to build high amplitude-modulated recruitment curves [24]. Standard pulse widths of 100 µs to 200 µs are the ideal range for most in vivo and clinical applications and can be used to achieve functional motor grasping and autonomic neuromodulation [23]. However, if strong and immediate tetanic response is needed, longer pulse widths of 500 µs or 1000 µs can be used to ensure that the charge is delivered strongly and concentrated [21].

Ultimately, establishing universal stimulation parameters remains a highly complex challenge, as the current literature demonstrates significant variability in activation thresholds across different animal species, distinct anatomical nerves, and even among different individuals targeting the exact same nerve. Narrowing the focus to the human median nerve which represents the primary anatomical target of this thesis the clinical trial conducted by Azevedo Coste et al. provides crucial insights and practical operational boundaries. In their study, the authors electrically stimulated the nerve using multi-contact epineural electrodes and recorded the resulting surface electromyography (EMG) to objectively evaluate muscle recruitment and synergistic responses. Through this rigorous empirical process, they were able to establish highly reliable parameter ranges necessary to successfully elicit functional grasping movements. Specifically, while utilizing a fixed pulse width of 150 µs, they identified that the optimal current amplitudes for inducing powerful, sustained functional grips typically fall within a well-defined operational window ranging from 360 µA to 500 µA, with the absolute minimum activation thresholds starting as low as 184 µA to 260 µA depending on the subject [22].

Table 2.1: Comparison of stimulation parameters and electrode types across different studies.

Article	**Electrode Type**	**Subject (Model)**	**Waveform**	**Frequency**	**Pulse Width**
Wright et al. [21]	Commercial (Micro-Leads / CorTec) or custom cuffs.	Vagus nerve, mice	Biphasic, charge-balanced (passive charge balancing)	30 Hz	100 μs (range: 100–1000 μs)
Azevedo Coste et al. [22]	Multicontact epineurial cuff (CorTec).	Median nerves, humans	Biphasic, symmetric, charge-balanced	24 Hz	150 μs
Lienemann et al. [23]	Soft & Stretchable multicuff electrodes	Sciatic nerve, pig	Biphasic pulse trains, cathodic-first	1 Hz	200 μs
Brill et al. [24]	FINE (Flat Interface Nerve Electrode).	Arm nerves, macaques	Single pulses, biphasic, rectangular, balanced	4 Hz	10 μs or 20 μs
Zurita et al. [25]	3D-printed cuff (Inkjet + 2-photon).	Leg nerve, locust	Bipolar pulse trains, balanced	1 kHz	500 μs
Carnicer-Lombarte et al. [26]	Ultra-conformable Parylene C cuff.	Arm and sciatic nerves, rats	Trains of 100 biphasic pulses	100 Hz (10 ms period)	100 μs

Chapter 3

Shield Development

3.1 Setup and specification

The first objective of this work is the design and implementation of a custom Printed Circuit Board (PCB) shield to interface directly with an STM32H7 Nucleo-144 development board. The STM32H7 Nucleo-144 is a development board to prototype and test the STM32H7 series microcontrollers, which involve an Arm Cortex core architecture in an LQFP144 package. The board is engineered to be hardware-expandable with the presence of the ST Zio connectors and the ST morpho headers. The latest pins provide complete access to all microcontroller input/output signals and power pins, thereby facilitating the seamless integration and stacking of customized or highly specialized hardware shields [27]. The custom PCB shield serves as a physical and electrical link between the microcontroller unit, the Intan RHD2132 module for neural recording, and the RHS2116 module for bidirectional recording and stimulation. The Intan RHD2132 microchip (Figure 3.1) is a complete low-power electrophysiology signal acquisition system. It has an array of 32 unipolar low-noise amplifiers with programmable upper and lower bandwidths. A multiplexed 16-bit analog-to-digital converter (ADC) samples biological signals, serializes data over a standard Serial Peripheral Interface bus (SPI), and converts weak electrode potentials into a digital stream without external analog instrumentation [28].

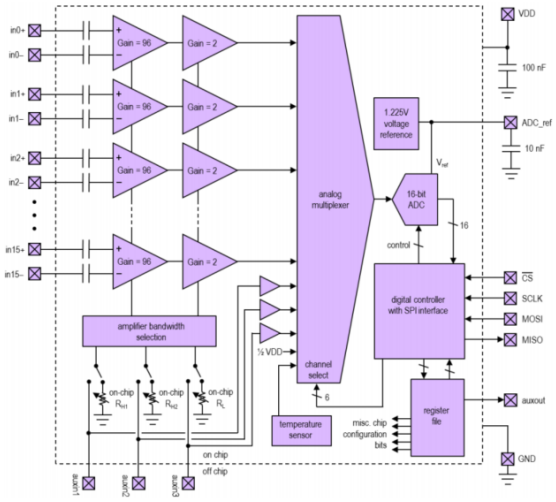


Figure 3.1: Functional block diagram of the Intan RHD2216 microchip (RHD2000 series). The internal architecture is made up of 16 differential analog inputs, a programmable bandwidth selection module, an analog multiplexer, and a 16-bit ADC. A digital controller drives the data transmission through a standard SPI bus[28].

The Intan RHS2116 microchip (Figure 4.4a) is a complete bidirectional electrophysiology interface system. It consists of 16 independent stimulation and amplifier blocks. Each channel has a low-noise amplifier with programmable bandwidth and a constant current stimulator. The stimulation module generates biphasic current pulses with programmable amplitudes from 10 nA to 2.55 mA. An ADC digitizes the biological signals acquired by the device. The digital controller checks data flow through a standard 32 bit SPI bus [29].

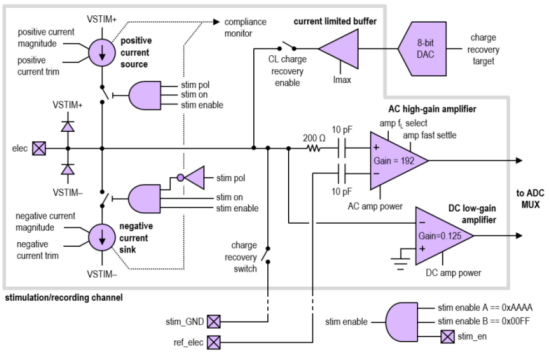
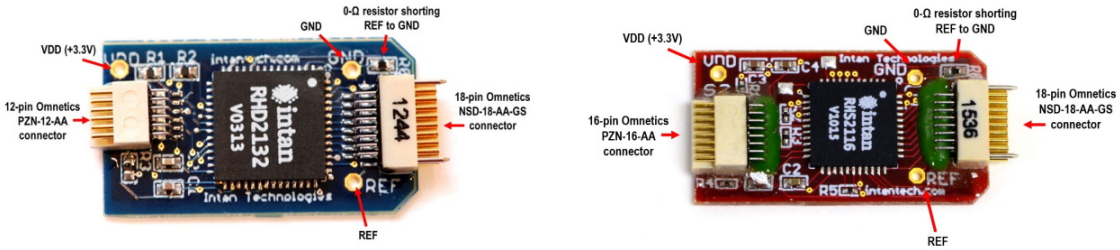


Figure 3.2: Simplified functional block diagram of a single stimulation and recording channel within the Intan RHS2116 microchip. The internal architecture integrates an AC high-gain amplifier, a DC low-gain amplifier, a constant-current stimulator with compliance monitoring, and charge-recovery circuits [29].

Both RHD2132 and RHS2116 microchips are directly integrated onto small printed circuit boards referred to as headstages. These hardware devices support commercial electrodes, ensuring the immediate amplification and digitization of electrophysiological signals at the recording site. Figure 3.3 shows the component distribution on both headstage variations, highlighting the power supply inputs, the ground pins, the electrode connectors, and the digital interface ports [30].



(a) (b)

Figure 3.3: **(a)** Pinout and component layout of an Intan RHD-series digital headstage with central RHD2132 chip, power supply pads (VDD and GND), references, and Omnetics connectors for digital interface and electrode integration [30]. **(b)** Pinout and component layout of an Intan RHS-series digital headstage with the central RHS2116 stimulator/amplifier chip, power supply pads (VDD and GND), reference connections, and Omnetics connectors for digital interface and electrode integration [31].

The communication between the STM32H7 microcontroller and the specialized Intan RHD and RHS headstages is based on an SPI protocol. The microcontroller generates and receives single-ended logic signals at standard 3.3V levels: Master

Out Slave In (MOSI), Master In Slave Out (MISO), Serial Clock (SCLK), and Chip Select (CS) lines. However, the transmission of high-speed, single-ended SPI signals over external cables to connected neural headstages presents significant signal integrity challenges, as the system is susceptible to electromagnetic interference (EMI), crosstalk, and severe signal degradation. To bypass the problem and to comply with the native communication standard of the Intan chips, these single-ended signals must be translated into LVDS, which converts a single digital logic state into a differential pair consisting of a positive (P) and a negative (N) signal. Because external noise typically couples equally onto both wires (common-mode noise), the differential receiver can easily subtract the noise, resulting in excellent signal integrity, low electromagnetic emissions, and the ability to support extremely high data rates with minimal power consumption [32].

Based on the Intan Technologies LVDS Adapter board (Figure 3.4), the PCB shield is designed with the differential conversion circuitry directly on board, without any intermediate adapter modules. In the preliminary setups, the signal conversion is carried out with external Intan Technologies LVDS adapter boards. The layout of these reference adapters reveals two different circuits specifically tailored to the requirements of the respective Intan headstages. The RHD section for neural recording only is used to route the standard SPI data lines and to supply the 3.3V logic supply to drive the headstage's internal digital components. The RHS section is used for both neural recording and active electrical stimulation with a more complex routing. Besides the standard SPI data lines and the 3.3V logic lines, the RHS circuit also has pathways to the high-voltage stimulation compliance rails. Both route the standard SPI data lines and the 3.3V logic supply to drive the headstage's internal digital components. In addition, the RHS circuit incorporates dedicated pathways for the high-voltage stimulation compliance rails labeled VSTIM+ and VSTIM-. The key objective of the data architecture design is to completely recreate external LVDS adapter boards and integrate them into the custom PCB shield. By integrating the LVDS transceivers, logic power delivery, and high-voltage stimulation routing into a single board, the design eliminates the reliance on intermediate adapter modules. This embedded architecture yields a significantly more compact hardware footprint that removes the need for additional bridging cables, which would otherwise introduce latency and inject extra noise into the data transmission.

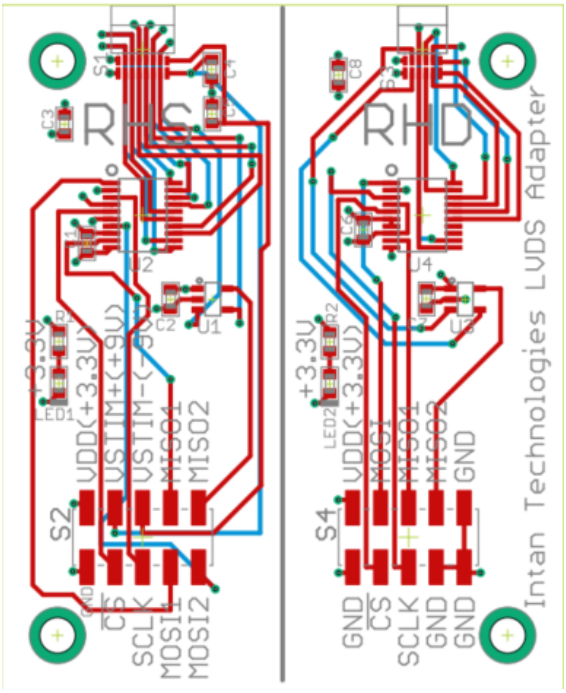


Figure 3.4: Intan LVDS adapter board

The shield design respects the distinct operational specifications of the two separate projects (figure 3.5): NerveRepack and Rewire. For neural recording, the NerveRepack project requires 5 recording channels operating at a 10 kHz sampling frequency, whereas the Rewire project demands higher bandwidth, specifying 8 recording channels operating at a 20 kHz sampling frequency. Similarly, the electrical neural stimulation requirements scale from 2 stimulation channels in the NerveRepack setup to 8 independent channels in the Rewire configuration. Regardless of the project, the internal digital logic of both the RHD and RHS headstages requires a clean, regulated 3.3V DC supply. However, the stimulation compliance rails are different: the RHS headstage needs a $\pm$3.3V DC supply for NerveRepack, while the Rewire setup needs a higher voltage compliance rail of $\pm$7V DC. A critical functional requirement of the custom shield is the strict management, conversion, and distribution of these different power domains. The Nucleo-144 board has a baseline 5V supply provided by either its USB connection or an external VIN power supply. The shield picks up this 5V source from the Nucleo headers and converts it locally to a low-noise power source to generate the standard 3.3V logic rail and the specific $\pm$3.3V or $\pm$7V stimulation rails needed by the project.



RHD Headstage	NerveRepack	Rewire
Recording channels	5	8
Recording Frequency (Hz)	10k	20k
Logic Supply Voltage (V)	3.3	3.3



RHS Headstage	NerveRepack	Rewire
Recording channels	5	8
Stimulation channels	2	8
Recording Frequency (Hz)	10k	20k
Stimulation Supply Voltage (V)	±3.3	±7
Logic Supply Voltage (V)	3.3	3.3

Figure 3.5: Summary of specifications

3.2 Power Dissipation

The power dissipation analysis is an important step for sizing the voltage regulators and DC-DC converters integrated into the PCB shield. Indeed, this board is required to offer a stable and low-noise power supply to the two Intan front-end chips: the RHD module for neural recording and the RHS module for simultaneous recording and stimulation. The power consumption of components changes depending on the application, dictated by the distinct operational requirements of either the NerveRepack or the Rewire project. The power consumption of the RHD recording module is based on the technical specifications given by the official Intan RHD2000 series datasheet. This component operates using a single 3.3V logic supply voltage. The overall current consumption of this device is not a static value; rather, it comprises a fixed quiescent baseline and dynamic components that scale strictly as a function of the recording settings. The quiescent baseline is composed of the current drawn by the amplifier array (0.2 mA), the baseline ADC current (0.51 mA), the impedance measurement module (0.12 mA), and the LVDS I/O transceiver (5.7 mA). These baseline currents are then supplemented by the dynamic current consumption of the AC amplifiers, which depends on the upper cutoff frequency f_H at a rate of 7.6 $\mu A/kHz$ for each active amplifier. Finally, the block of the ADC and MUX requires an extra current proportional to the total sampling frequency, which is 2.14 $\mu A/(kS/s)$. Defining N_{ch} as the number of active recording channels and f_{sample_ch} as the sampling frequency per channel, the general equation of the total current consumption (I_{tot}) of the RHD chip is as follows:

$$\begin{aligned} I_{tot} = {} & 0.2\ \text{mA} + 0.51\ \text{mA} + 0.12\ \text{mA} + 5.7\ \text{mA} \\ & + \left(N_{ch} \cdot 7.6 \frac{\mu\text{A}}{\text{kHz}} \cdot f_H \right) + \left(N_{ch} \cdot f_{sample_ch} \cdot 2.14 \frac{\mu\text{A}}{\text{kS/s}} \right) \end{aligned} \tag{3.1}$$

Applying this analytical model to the two project scenarios revealed differences in the energy load imposed by bandwidth specifications. In the case of the NerveRepack project, the system involves acquiring from only 5 channels ($N_{ch} = 5$) with a sampling frequency of 10 kS/s per channel. By setting the upper cut-off frequency f_H to 5 kHz, the dynamic consumption of the amplifiers stands at 0.19 mA. Simultaneously, the total sample rate of 50 kS/s results in an absorption by the ADC/MUX block of approximately 0.107 mA. By adding the previously described fixed baseline components to these values, a total current of 6.8 mA is obtained, which, when powered at 3.3V, translates into an overall dissipated power (P_{diss}) of 22.5 mW.

The quiescent current drawn from the 3.3V logic supply (V_{DD}) by the RHS chip involves a higher fixed baseline compared to the RHD. According to the technical specifications, the fixed baseline current is 3.2 mA to power various voltage references, bias current generators, and ADC circuitry. The 5.7 mA load for the LVDS I/O transceiver and 0.12 mA for the impedance measurement module must be added. The dynamic recording consumption scales proportionally to the bandwidth and channel count, but with different coefficients: 9.2 μA/kHz per active AC amplifier and 5.2 μA/(kS/s) for the ADC/MUX block. The total quiescent logic current (I_{VDD_quies}) is formulated as follows:

$$\begin{aligned} I_{VDD_quies} = {} & 3.2\ \text{mA} + 0.12\ \text{mA} + 5.7\ \text{mA} \\ & + \left(N_{rec} \cdot 9.2 \frac{\mu\text{A}}{\text{kHz}} \cdot f_H \right) + \left(N_{rec} \cdot f_{sample_ch} \cdot 5.2 \frac{\mu\text{A}}{\text{kS/s}} \right) \end{aligned} \tag{3.2}$$

Beside the standard 3.3V logic supply, the stimulator circuits demand dedicated high-voltage compliance rails (V_{STIM+} and V_{STIM-}). Even when no stimulation pulses are being actively generated, these rails draw tabulated quiescent currents that heavily depend on the selected project voltages. For the NerveRepack configuration ($\pm$3.3V), the quiescent currents are 0.57 mA (I_{quis_pos}) and 0.41 mA (I_{quis_neg}) for the positive and negative rails, respectively. Conversely, the Rewire configuration ($\pm$7.0V) draws 0.62 mA (I_{quis_pos}) from the positive rail and 0.48 mA (I_{quis_neg}) from the negative rail. Beyond the quiescent power consumption, the active generation of stimulation pulses represents the most demanding operational phase for the RHS2116 chip, imposing substantial transient loads on all power domains. According to the manufacturer's specifications, injecting a biphasic stimulation current (Figure 3.6) with a magnitude of I_{STIM} across N_{stim} active channels induces an instantaneous additional current draw on the 3.3V logic supply (V_{DD}) as well as on the high-voltage compliance rails (V_{STIM+} and V_{STIM-}).

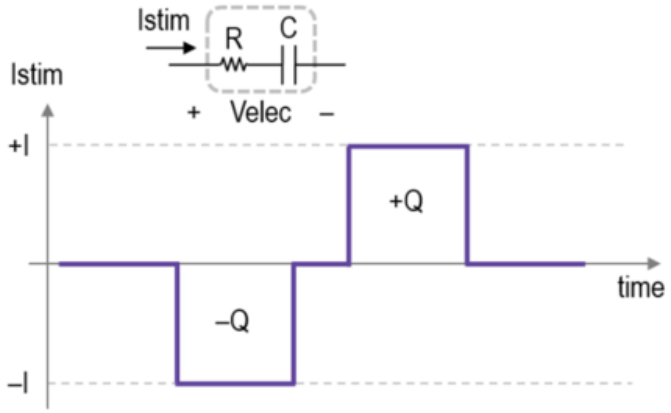


Figure 3.6: Electrical modeling and biphasic stimulation waveform used in the RHS power consumption analysis. The top insert depicts the series resistor-capacitor (RC) network representing electrode impedance under current stimulation (Istim). The waveform timeline illustrates the charge-balanced phases, defining the negative (-Q) and positive (+Q) charge transfer over time.

During the initial negative (cathodic) stimulation phase, which lasts for a duration of T_1, the instantaneous current increases are defined as:

$$\Delta I_{VDD}^{(-)} = N_{stim} \cdot 0.10 \cdot I_{STIM} \tag{3.3}$$

$$\Delta I_{VSTIM+}^{(-)} = N_{stim} \cdot 0.34 \cdot I_{STIM} \tag{3.4}$$

$$\Delta I_{VSTIM-}^{(-)} = N_{stim} \cdot 1.31 \cdot I_{STIM} \tag{3.5}$$

Conversely, during the subsequent positive (anodic) phase of duration T_2, the current draw redistributes asymmetrically across the rails:

$$\Delta I_{VDD}^{(+)} = N_{stim} \cdot 0.23 \cdot I_{STIM} \tag{3.6}$$

$$\Delta I_{VSTIM+}^{(+)} = N_{stim} \cdot 1.15 \cdot I_{STIM} \tag{3.7}$$

$$\Delta I_{VSTIM-}^{(+)} = 0 \tag{3.8}$$

Because stimulation pulses are not continuous but are delivered cyclically at a specific frequency f_{stim}, the effective energetic and thermal load imposed on the PCB shield must be evaluated as a time-averaged value. By defining the overall stimulation duty cycle as $D = f_{stim} \cdot (T_1 + T_2)$, the average dynamic current increase on each supply rail can be calculated by weighting the instantaneous draws by the relative duration of their respective phases. Consequently, the average dynamic current contributions ($\Delta \bar{I}$) are formulated as follows:

$$\Delta\bar{I}_{VDD} = D \cdot \left[\left(\frac{T_1}{T_1 + T_2} \right) \Delta I_{VDD}^{(-)} + \left(\frac{T_2}{T_1 + T_2} \right) \Delta I_{VDD}^{(+)} \right] \tag{3.9}$$

$$\Delta\bar{I}_{VSTIM+} = D \cdot \left[\left(\frac{T_1}{T_1 + T_2} \right) \Delta I_{VSTIM+}^{(-)} + \left(\frac{T_2}{T_1 + T_2} \right) \Delta I_{VSTIM+}^{(+)} \right] \tag{3.10}$$

$$\Delta\bar{I}_{VSTIM-} = D \cdot \left[\left(\frac{T_1}{T_1 + T_2} \right) \Delta I_{VSTIM-}^{(-)} \right] \tag{3.11}$$

Finally, the total average power dissipation (P_{tot}) of the RHS module—which serves as the primary constraint for the thermal management and component selection of the custom shield's DC-DC converters—is derived by superimposing these dynamic stimulation averages onto the quiescent baselines across all three voltage domains:

$$\begin{aligned} P_{tot} = & V_{DD} \cdot \left(I_{VDD_quies} + \Delta\bar{I}_{VDD} \right) \\ & + V_{STIM+} \cdot \left(I_{quis_pos} + \Delta\bar{I}_{VSTIM+} \right) \\ & + |V_{STIM-}| \cdot \left(I_{quis_neg} + \Delta\bar{I}_{VSTIM-} \right) \end{aligned} \tag{3.12}$$

To evaluate the electrical impact of stimulation, a parametric analysis is performed by sweeping the stimulation parameters across a defined operational grid. Specifically, the simulation explores a wide range of stimulation current amplitudes (I_{stim}) spanning from 2.55 μA up to the absolute hardware limit of 2.55 mA, combined with pulse widths (T_1, T_2) ranging from 20 μs to 1000 μs per phase. This matrix reflects realistic electrophysiological protocols derived from the state-of-the-art configuration, evaluated at a typical stimulation frequency (f_{stim}) of 24 Hz.

As a result of processing of these grids in the analytical power consumption model, it is possible to map the total power dissipation P_{tot} and the worst-case operating condition in the two different projects. For NerveRepack (with ±3.3V compliance rails and $N_{stim} = 2$ active stimulation channels), the system is at least as expected for constant power consumption. The highest current density is reached for the most extreme stimulation conditions with $I_{stim} = 2.55$ mA and a pulse width of 1000 μs per phase. The maximum current demand is 9.550 mA for the logic supply V_{DD}, 0.752 mA for the positive compliance rail V_{STIM+} and 0.570 mA for the negative compliance rail V_{STIM-}. As can be seen in the heatmap of the simulation results (Figure 3.7), the maximum total power dissipation is about 35.88 mW. In contrast, Rewire introduces a more demanding profile due to its higher channel count dedicated to stimulation ($N_{stim} = 8$) and the wider voltage span of the compliance rails (±7.0V). Consequently, the energetic cost increases significantly; operating at the same extreme boundary of $I_{stim} = 2.55$ mA and a pulse width of 500 μs, the peak current requirements escalate to 10.750 mA on the V_{DD} line, 1.350 mA on V_{STIM+}, and 1.121 mA on V_{STIM-}. Under these conditions, the overall

power dissipation reaches a maximum peak of 52.77 mW(Figure 3.8). In the end, the results of the consumption analysis provide the absolute upper bounds for the proper sizing of the active DC-DC converters on the PCB shield and are suitable for operation in all situations.

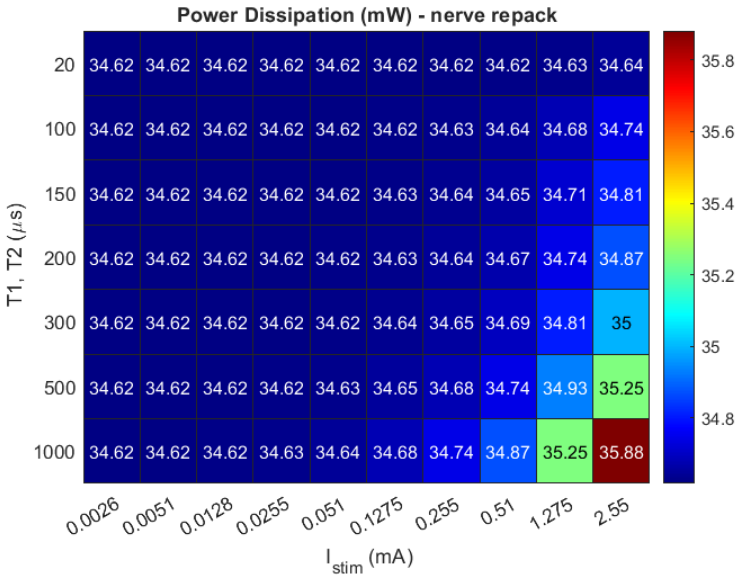


Figure 3.7: Total average power dissipation (P_{tot} in mW) of the RHS bidirectional module as a function of the stimulation current magnitude (I_{stim}) and pulse width (T_1, T_2), mapped for the NerveRepack scenario across the evaluated parametric grid.

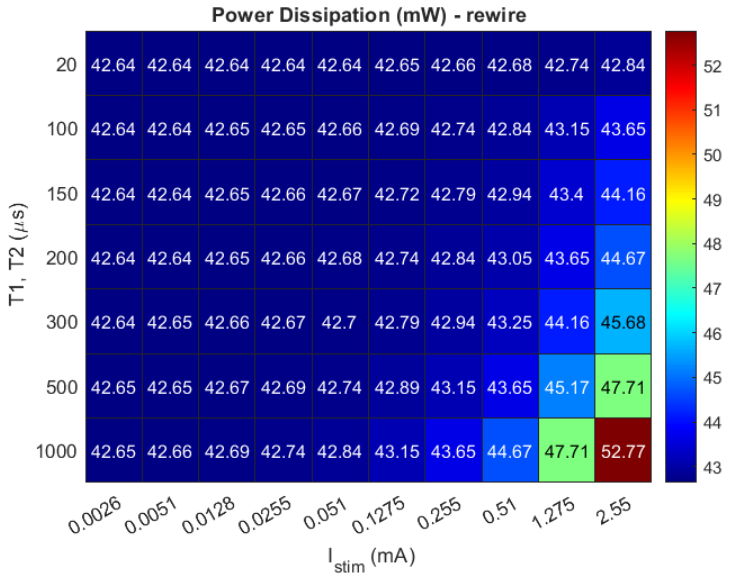


Figure 3.8: Total average power dissipation (P_{tot} in mW) of the RHS bidirectional module as a function of the stimulation current magnitude (I_{stim}) and pulse width (T_1, T_2), mapped for the Rewire scenario across the evaluated parametric grid.

3.3 Power Management

Based on the power analysis, the next phase in the shield development is the selection of the power management components. The main objective is to provide a reliable, low-noise power supply for the Intan RHD and RHS front-end chips to guarantee the requested output voltage and to respect the maximum value of the peak transient currents calculated in the worst-case analysis (e.g., 10.75 mA for the logic line and up to 1.35 mA for stimulation compliance rails). In addition to the electrical aspects, the physical size of the components was one of the key design challenges to keep the shield compact and portable. As neural system interfaces are highly sensitive to power supply noise, a variety of conversion configurations were investigated. LDO linear regulators, switched-capacitor charge pumps, and fully integrated magnetic µModule DC-DC converters were considered. Assuming a standard 5V primary input bus, the component research and selection process was based on three distinct conversion pathways to suit the operational needs of both the NerveRepack and Rewire projects: 5V to 3.3V for the main logic supply, 5V to ±7V for high-voltage stimulation, 5V to ±5V for alternative compliance ranges and the generation of ±3.3V compliance rails for lower-voltage stimulation. For this latter pathway, the design takes advantage of the positive 3.3V logic supply and inverts it using the ICL7660S charge pump to generate the corresponding negative rail. Rather than limiting the design to a single definitive component per pathway,

multiple solutions were practically implemented on the shield. This versatile layout approach allows for direct comparative testing and for the selection of the best configuration based on the specific experimental use case.

3.3.1 5V to 3.3V Logic Supply Conversion

Generating a stable and low-noise 3.3V logic from a 5V bus is essential for the operation of the Intan front-end chips. Four distinct conversion architectures were physically implemented on the custom shield based on switched-capacitor charge pumps, fully integrated magnetic step-down modules, and traditional linear regulators, allowing for direct comparative testing. The first architecture implemented is based on the LTC3246, a wide input range switched-capacitor buck-boost DC/DC converter. The LTC3246 employs a multimode fractional conversion topology without any bulky inductors, generating ultralow EMI emissions. This architecture can deliver up to 500 mA of continuous output current, offering a safety margin over the worst-case peak demand of the Intan chips, while maintaining an ultra-low quiescent current of just 20 µA. From an operational standpoint, when converting a nominal 5V input to a 3.3V output, the internal control circuits of the LTC3246 automatically select the 1:1 step-down mode, as the input voltage is between the target output and the double of the target output (3.3 V $<$ 5 V $<$ 6.6 V). The internal switch network alters its typical charge-pumping behavior, acting instead similarly to a linear regulator. The charge is delivered almost directly from the node to the pin for most of the oscillator period, and current is controlled to minimize the output ripple. Because the input current is approximately equal to the load current in 1:1 step-down mode, the conversion efficiency is simply proportional to the voltage ratio, and it is equivalent to 66% Although the flying capacitor's primary voltage-dividing or multiplying role is bypassed in this specific steady-state mode, it remains a strictly mandatory hardware component for the chip's multimode architecture to satisfy the internal state machine and enable seamless transitions to step-up operation should the input voltage experience severe drops. According to the manufacturer's technical specifications, stable operation requires a specific arrangement of passive components. A ceramic decoupling capacitor of 1 μF is placed at the input, while a 2.2 μF ceramic flying capacitor is connected between the C^+ and C^- terminals to fulfil the charge pump's architectural requirements. At the output node, a 47 μF filter capacitor is utilized to severely reduce the voltage ripple, alongside a 10 μF bypass capacitor required for the internal 5V LDO regulator at the BIAS pins. The hardware is set up for the 3.3V fixed output mode by tying both the SEL1 and SEL2 logic pins high to the V_{IN} supply, and the OUTS/ADJ sense pin is shorted directly to the V_{OUT} rail to close the internal regulation loop. Finally, an external 510 kΩ resistor acts as a pull-up for the open-drain reset output ($\overline{\text{RST}}$) (Figure 3.9).

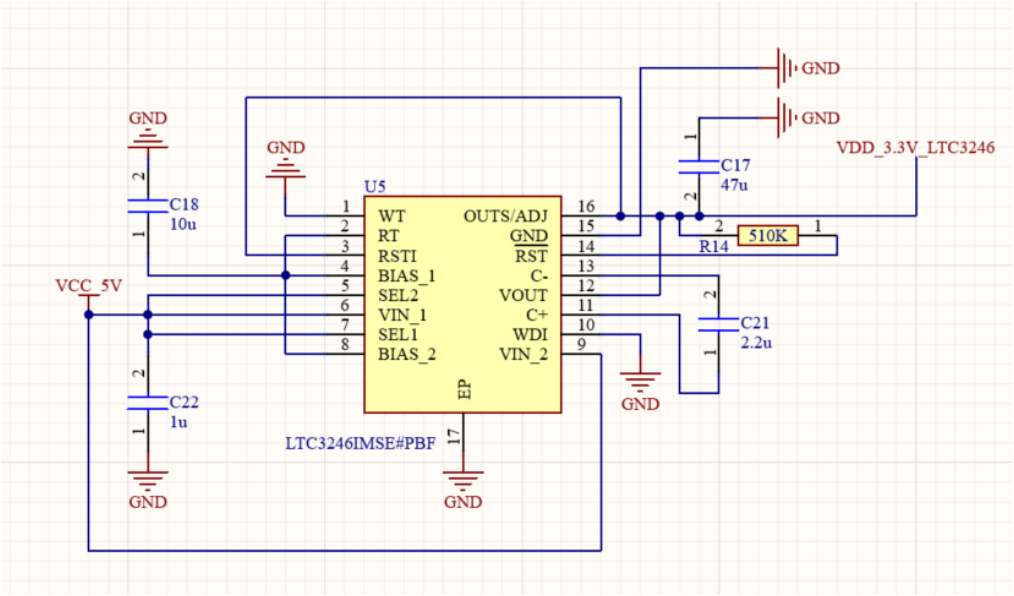


Figure 3.9: Schematic implementation of the LTC3246 switched-capacitor buck-boost converter on the custom PCB shield. The circuit is hardwired to generate a fixed 3.3V logic supply from the 5V primary bus by tying both SEL1 and SEL2 control pins high, detailing the external flying capacitor (C_{21}) and the filtering network (C_{17}, C_{18}, C_{22}) required for stable 1:1 step-down operation

As an alternative, highly compact solution for the 5V to 3.3V logic conversion, the custom shield also integrates the MCP1253, a positive-regulated, inductorless charge pump DC/DC converter. Designed specifically for space-constrained applications requiring low noise and high efficiency, this device automatically switches between buck and boost operation to maintain strict output regulation without the need for magnetic components, which intrinsically mitigates radiated EMI. Although the maximum continuous output current is conservatively rated at 120 mA, it can provide an abundant supply of the peak transient current of the Intan logic circuit. It also has a low quiescent current of 80 µA and has internal soft-start circuitry to control inrush currents during power-up (approximately 300 µs), as well as thermal shutdown and foldback short-circuit protection. The MCP1253 is always in buck mode when stepping down the 5V primary bus to the 3.3V target. The internal regulation control is hysteretic, which compares the output voltage against an internal reference and triggers discrete charge transfer phases only when the output falls below the regulation point. In this buck configuration, the power efficiency is approximately equal to the voltage ratio (V_{OUT}/V_{IN}), as in a linear regulator, where the untransferred power is simply dissipated as heat. The hardware layout closely follows the manufacturer's application guidelines for the miniature 8-lead MSOP package, which occupies a minimal board area. As depicted in the schematic implementation (Figure 3.10), stable charge transfer is sustained by a

minimal external network of three ceramic capacitors: a 10 µF input decoupling capacitor (C_{23}) to filter source transients, a 10 µF output filter capacitor (C_{27}) to suppress the residual voltage ripple inherent to the hysteretic control, and a 1 µF flying capacitor (C_{26}) to drive the internal charge-pump mechanism. To set the ideal output voltage, the SELECT logic pin (pin 8) is connected directly to the 5V input supply (V_{CC_5v}), and the internal feedback controller regulates the converter output to a fixed value of 3.3V. The active-low shutdown pin ($\overline{\text{SHDN}}$, pin 7) is also connected to the input supply to keep the converter running. The power-good output (PGOOD, pin 1) is another open-drain indicator that sinks current when the output is less than 93% of its nominal value, and it is pulled up to the 3.3V rail via a 100 kΩ resistor, completing the functional block.

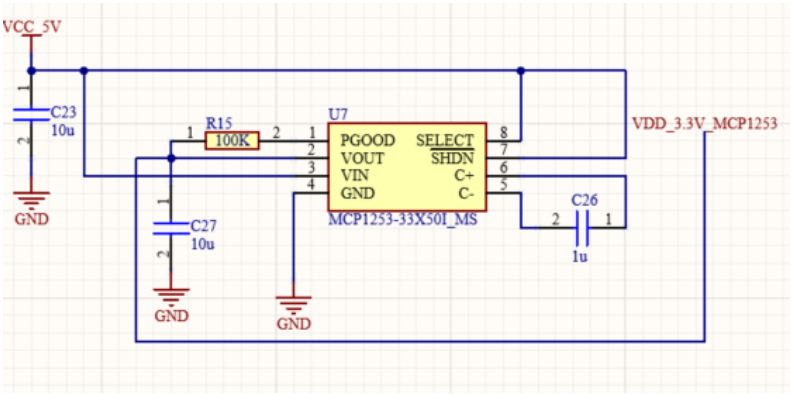


Figure 3.10: Schematic implementation of the MCP1253 inductorless charge pump on the custom PCB shield. The device is configured for a fixed 3.3V output by tying the SELECT pin to the 5V supply, highlighting the minimal external capacitor network (C_{23}, C_{26}, C_{27}) and the PGOOD pull-up configuration (R_{15}).

A third architecture evaluated for the 5V to 3.3V logic conversion relies on the MagI3C 173950336, a fully integrated fixed step-down regulator module from the FDSM series. This component radically simplifies the power supply design by embedding the controller Integrated Circuit, the switching inductor, and fundamental compensating capacitors entirely within a single package. Capable of accepting input voltages up to 36V, the module delivers up to 0.5A of continuous output current with a peak efficiency reaching 93%, providing an abundant safety margin for the targeted 10.75 mA logic peak demand without generating excessive heat. It is housed in a standard 3-pin SIP (Through-Hole Technology), which is deliberately designed to be pin-compatible with traditional 78xx linear regulators for simple drop-in replacements. The module is rigorously designed to comply with the stringent EN 55032 (CISPR 32) Class B standard for both radiated and conducted emissions, heavily mitigating the risk of injecting switching noise into the neural signal path. The internal architecture further enhances system reliability

by inherently providing an internal soft-start of approximately 1.5 ms to prevent voltage overshoot during power-up, alongside thermal shutdown and cycle-by-cycle short-circuit protection.

The component works as an asynchronous step-down regulator controlled by a current-mode regulation loop. Internally, the output voltage is divided by a built-in feedback resistor network and fed into an error amplifier, which compares this signal against a precise 0.75V internal reference. This continuous comparison dictates the on-time of a fixed-frequency pulse width generator that drives the internal MOSFET. This specific architecture supports fast transient response and intrinsically achieves very small output voltage ripple values. The manufacturer's layout guidelines recommend the addition of supplemental external filtering. As illustrated in the schematic implementation (Figure 3.11), an input capacitor is placed on the line to stabilize the 5V primary source against high-frequency switching transients, while an output capacitor is tied to the terminal to further suppress ripple and support dynamic load variations. The minimalist hardware layout—comprising only (pin 1), GND (pin 2), and a fixed 3.3V (pin 3) eliminates the need for external feedback resistor networks or complex configuration logic, offering a highly robust and straightforward solution for the logic rail generation.

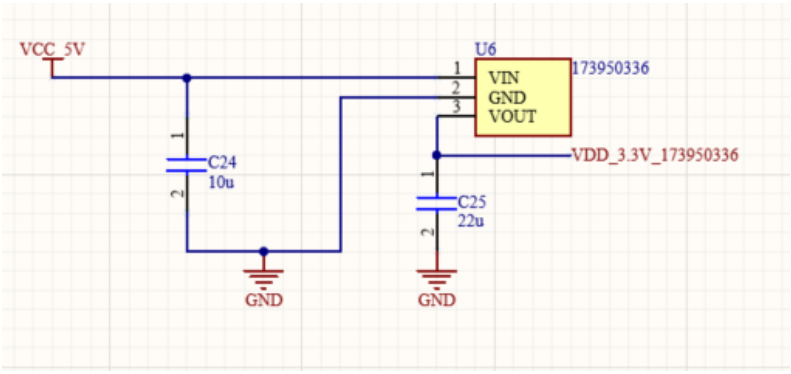


Figure 3.11: Schematic implementation of the MagI3C 173950336 integrated step-down module on the custom PCB shield. The highly integrated 3-pin configuration requires only a 10 μF input capacitor (C_{24}) and a 22 μF output capacitor (C_{25}) to achieve a fully regulated, low-noise 3.3V logic supply.

At the end, completing the suite of 5V-to-3.3V conversion architectures, the AZ1117C was integrated onto the custom shield as a purely linear regulation alternative. Specifically utilizing the fixed 3.3V variant (AZ1117CH-3.3TRG1) housed in an industry-standard SOT223 surface-mount package, this Low-Dropout (LDO) regulator offers an exceptionally clean power profile. Inherently devoid of any internal switching mechanism or high-frequency oscillator, this topology intrinsically produces zero radiated EMI and completely eliminates switching ripple. It features

an ultra-low output noise of just 0.003% of V_{OUT} and a high Power Supply Rejection Ratio (PSRR) of 70 dB, characteristics that make it theoretically ideal for supplying the highly sensitive analog front-ends of the Intan recording modules. Capable of delivering a typical current limit of 1.35 A, the AZ1117C provides a power margin over the 10.75 mA peak requirement, while additionally embedding robust on-chip thermal shutdown to protect against excessive junction temperatures. Its power efficiency is strictly dictated by the input-to-output voltage ratio ($V_{OUT}/V_{IN} \approx 66\%$), with the untransferred energy across the voltage drop being safely dissipated as heat into the board.

The fixed-voltage version internally integrates the necessary feedback adjustment resistors, significantly minimizing the external component count. As illustrated in Figure 3.12, the ADJ/GND terminal (pin 1) is tied directly to the common ground plane. To ensure proper operation and stability, the design strictly adheres to the manufacturer's filtering guidelines, which require compatibility with low-ESR ceramic capacitors and a minimum output capacitance of 10 μF. Consequently, a 10 μF ceramic capacitor (C_{20}) is placed at the input (pin 3) to filter source transients from the 5V bus, while a 22 μF ceramic capacitor (C_{19}) is connected across the output nodes (pins 2 and 4) to securely surpass the minimum stability threshold and optimize the transient response. This minimalist layout results in a highly reliable, ultra-low-noise power management block.

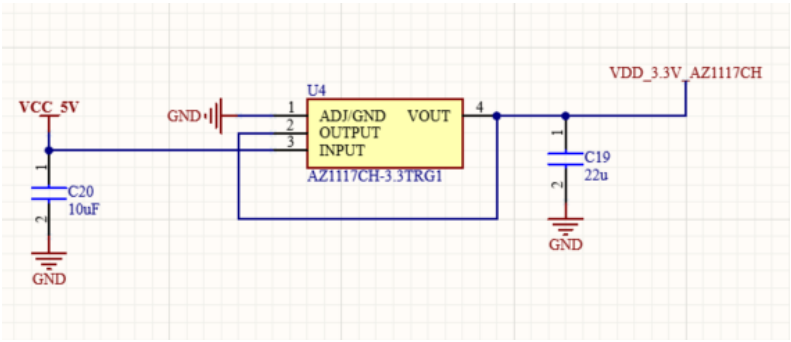


Figure 3.12: Schematic implementation of the AZ1117C low-dropout (LDO) linear regulator on the custom PCB shield. Configured for a fixed 3.3V output, the circuit leverages its internally trimmed feedback resistors, requiring only a 10 μF input capacitor (C_{20}) and a 22 μF output capacitor (C_{19}) to guarantee high-PSRR, noise-free logic supply.

As summarized in Table 3.1, each topology presents specific advantages. The linear LDO regulator (AZ1117C) represents the baseline for signal integrity, offering an inherently noise-free output with zero radiated EMI, albeit at the cost of the lowest energy efficiency, as the untransferred power is entirely dissipated as heat. In this specific 5V-to-3.3V step-down application, both the LTC3246 and MCP1253 charge pumps exhibit efficiency equivalent to that of the linear regulator

($\approx$ 66%), since they are forced to operate in 1:1 and buck modes, respectively. However, these inductorless charge pumps dramatically reduce the overall PCB footprint and offer an ultra-low quiescent current, making them exceptionally well-suited for space-constrained, low-power applications while maintaining low EMI profiles. Conversely, the fully integrated MagI3C step-down module achieves the highest theoretical energy efficiency (up to 93%) through its magnetic switching architecture, ensuring minimal thermal dissipation. To offset the typical noise disadvantages of switching regulators, this module is rigorously shielded and certified for Class B EMI compliance, though this comes at the expense of a significantly larger volumetric footprint and the highest quiescent current among the evaluated solutions. This versatile, multi-component layout guarantees complete hardware redundancy. It allows the operator to dynamically select the most appropriate power supply pathway based on the specific experimental constraints.

Table 3.1: Comparative summary of the 5V to 3.3V logic conversion components implemented on the custom shield, detailing topology, input voltage range, maximum output current, efficiency, EMI profile, and physical dimensions.

Component	Conversion Topology	Input Range	Max Current	Efficiency	EMI / Noise Profile	Dimensions ($L \times W \times H$)
LTC3246	Multimode Charge Pump	2.7V – 38V	500 mA	$\approx$ 66% (1:1)	Ultralow EMI	$4.04 \times 5.10 \times 1.10$ mm
MCP1253	Hysteretic Charge Pump	2.7V – 5.5V	120 mA	$\approx$ 66% (Buck)	Low (Inductorless)	$3.00 \times 4.90 \times 1.10$ mm
MagI3C	Magnetic Step-Down μMod.	4.75V – 36V	500 mA	Up to 93%	EN 55032 Class B	$11.60 \times 7.55 \times 10.20$ mm
AZ1117C	Linear LDO Regulator	4.7V – 15V	1.35 A	$\approx$ 66% (V_{OUT}/V_{IN})	Zero Radiated / 70dB PSRR	$6.50 \times 7.00 \times 1.75$ mm

3.3.2 $\pm$3.3V Stimulation Supply

Transitioning from the logic power management to the stimulation circuitry, the NerveRepack project explicitly requires $\pm$3.3V compliance rails to drive the neural stimulation outputs of the Intan RHS front-ends. To conserve valuable PCB real estate and drastically minimize the overall component count, the design intentionally avoids utilizing two separate, bulky DC/DC converters for this specific pathway. Instead, the architecture takes advantage of the highly stable and low-noise positive +3.3V logic supply previously generated. This positive rail is routed directly to serve as the positive stimulation terminal (VSTIM+). Consequently, the only remaining requirement is to generate the symmetrical negative rail (-3.3V). The Renesas ICL7660S monolithic CMOS super voltage converter was integrated into the shield for the voltage inversion. Housed in a compact 8-lead SOIC package, the ICL7660S operates as an inductorless charge pump specifically designed to perform supply voltage conversions from positive to negative, boasting an exceptional open-circuit voltage conversion efficiency of 99% and a power efficiency of 98%. The chip achieves voltage inversion through a two-phase switched-capacitor network with an internal RC oscillator and four internal MOS power switches. In the first half-cycle of the oscillator, the internal logic closes two of the MOS switches and connects an external flying capacitor across the input supply (V+) and ground, thus charging

it to the full positive input voltage. In the second half-cycle, the first switches open and the remaining two switches close. This process essentially re-references the flying capacitor as it is forced to ground, and its negative terminal drops to a negative potential equal to the input. This inverted charge is then dumped into the output reservoir capacitor, effectively mirroring the positive input as a steady voltage at the output pin. The hardware layout adheres to the low-voltage application guidelines. As depicted in the schematic (Figure 3.13), the input supply (V+, pin 8) is fed directly by the $+3.3V$ logic line. A 10 μF ceramic flying capacitor (C_{46}) is connected between the CAP+ (pin 2) and CAP- (pin 4) terminals to physically transport the charge during the switching cycles. The inverted output at V_{OUT} (pin 5) is smoothed by a 10 μF output reservoir capacitor (C_{47}) tied to ground, establishing the stable -3.3V stimulation rail (Vstim-). The voltage drop can severely degrade performance at lower input potentials. Since the input voltage in this application falls below the critical 3.5V threshold, the LV pin is directly connected to ground. This bypasses the internal regulator and reduces the output source resistance. Finally, the BOOST (pin 1) and OSC (pin 7) pins are left floating, allowing the internal oscillator to continue running at its nominal frequency without interference.

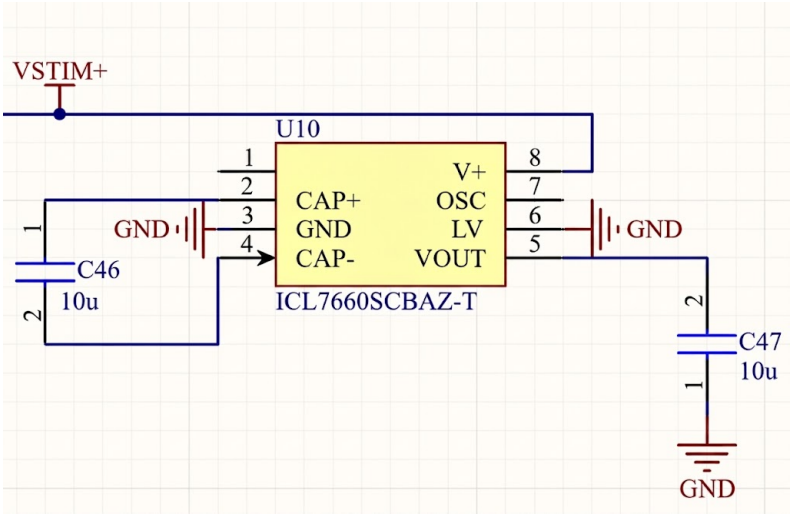


Figure 3.13: Schematic implementation of the ICL7660S voltage inverter on the custom PCB. The circuit mirrors the +3.3V logic supply to generate the −3.3V stimulation rail ($Vstim-$) using a minimal external network comprising a flying capacitor (C_{46}) and a reservoir capacitor (C_{47}).

3.3.3 ±7V Stimulation Supply

Following the generation of the low-voltage logic and stimulation rails, the subsequent power management requirement involves the creation of a robust ±7V

symmetrical supply. This higher-voltage bipolar rail is strictly dedicated to driving the Rewire stimulation stage, which demands higher compliance voltages to properly push current through the neural tissue interfaces. To perform this 5V to ±7V DC/DC conversion while maintaining high efficiency, minimizing the PCB footprint, and mitigating electromagnetic interference, two advanced magnetic μModule regulators were selected for physical implementation and comparative evaluation: the LTM8045 and the LTM8049. Both components are switching regulators that incorporate the current-mode controller, power switching system, and magnetic inductors in one overmolded package. The devices can operate in either the SEPIC (Single-Ended Primary Inductor Converter) topology to produce the positive +7V rail or in the inverting topology to generate the negative -7V rail. However, they are very different in their architectural integration: the LTM8045 is a single-output converter with a dual IC layout to produce a symmetrical supply, while the LTM8049 is a dual-output converter that can produce the positive and the negative rail in a single BGA footprint. The first highly integrated solution implemented to generate the dual 7 V ± stimulation rails is based on the LTM8049, a dual-channel SEPIC and inverting module DC/DC converter. Designed to operate over a wide input voltage range from 2.6V to 20V, this versatile device is capable of delivering substantial output currents, rated up to 1A per channel depending on the specific step-up/step-down conversion ratio, providing an optimal power margin for the demanding neural stimulation pulses. Housed in a thermally enhanced, low-profile BGA package measuring 15×9×2.42 mm, the LTM8049 allows for the simultaneous generation of both the positive and negative stimulation compliance voltages from a single IC footprint. Internally, the LTM8049 encapsulates two completely independent switch-mode power supplies. Each channel features its own current-mode controller, power switching element, tightly coupled power inductors, power diodes, and fundamental input/output capacitance. The LTM8049 is designed to have the output in a SEPIC configuration to generate a positive voltage in the circuit or inverting to generate a negative voltage. On the positive stimulation rail (+7V), Channel 1 is selected as a SEPIC converter. According to the manufacturer's design, it is connected to ground as well as to the channel negative output terminal (V_{OUT1N}), and the regulated positive potential is generated from the V_{OUT1P} terminal. On the other hand, Channel 2 is tuned to an inverting converter to generate the symmetrical negative stimulation rail (-7V). The positive output terminal (V_{OUT2P}) is connected to the ground while the other terminal (V_{OUT2N}) is tied to the negative potential. Moreover, to fully implement this dual-topology architecture on the custom PCB, the hardware schematic includes custom feedback and filtering networks for the 5V to ±7V conversion. The 5V primary bus is supplied to both V_{IN1} and V_{IN2} pins, heavily decoupled by two 10 μF ceramic capacitors (C_1, C_2). To dictate the output voltages, the device utilizes independent feedback equations for each topology. For the +7V SEPIC channel,

the feedback resistor (R_2) is set to 69.8k *Omega*, calculated via the SEPIC regulation formula $R_{FB} = (V_{OUT} - 1.204)/0.0833$. For the -7 V inverting channel, the feedback resistor (R_6) is set to 84.5 kΩ, following the inverting regulation formula $R_{FB} = (|V_{OUT}| + 0.007)/0.0833$. Both channels are synchronized to a fast 1 MHz switching frequency, explicitly programmed by connecting 80.6 kΩ resistors (R_5, R_8) from the respective RT pins to ground to optimize efficiency and minimize component size. 22 nF soft-start capacitors (C_7, C_{11}) are placed on SS pins to ensure a gradual ramp-up of the switch currents, and active-high Power Good signals (PG1, PG2) are also implemented with 200 kΩ pull-up resistors to flag when both channels are in proper regulation. In addition to the extensive output capacitor banks (22μF,10μF,1μF for the positive rail, and 47μF,10μF,1 μF for the negative rail), the design integrates surface-mount ferrite beads (FB1, FB2) in series with the final output traces (Figure 3.14). These components drastically attenuate the residual 1 MHz switching ripple inherently produced by the μModule's internal magnetics, yielding the highly stable Vstim+ and Vstim- test points.

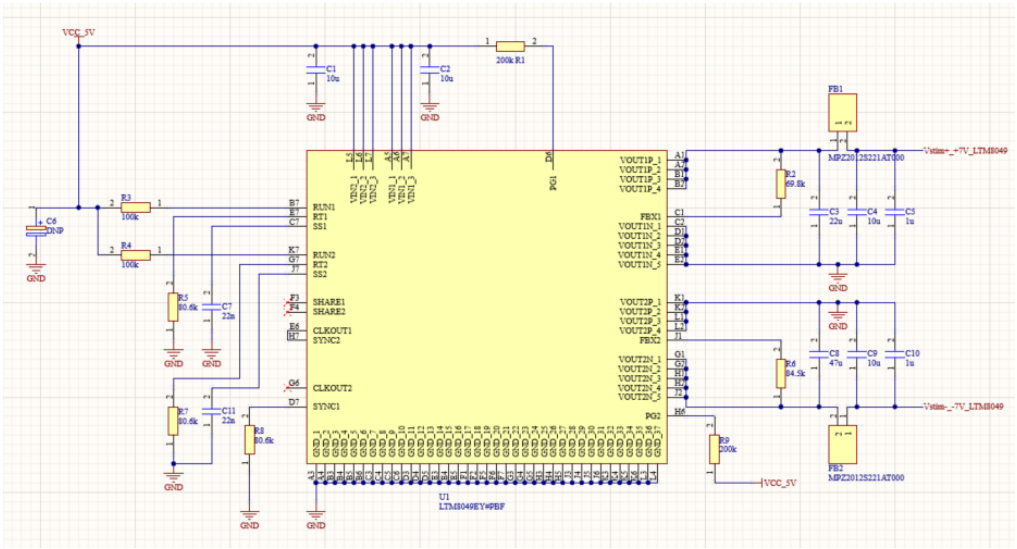


Figure 3.14: Schematic implementation of the dual-channel LTM8049 μModule on the custom shield. Channel 1 is configured as a SEPIC to generate the +7V rail (V_{OUT1N} grounded), while Channel 2 is configured as an inverter to generate the -7V rail (V_{OUT2P} grounded). Both outputs feature extensive multi-stage capacitive filtering coupled with series ferrite beads (FB1, FB2) to guarantee a low-noise stimulation supply.

The alternative solution evaluated for the ±7V stimulation supply generation relies on the LTM8045, a versatile μmodule DC/DC converter. Functionally identical in architectural concept to the LTM8049, the LTM8045 is designed to operate over a wide input voltage range of 2.8V to 18V and can independently function as

either a SEPIC or an inverting converter by grounding the appropriate output rail. However, unlike the dual-channel LTM8049, the LTM8045 is a single-output device. Consequently, to generate the symmetrical bipolar rails required by the Rewire system, the hardware design necessitates the instantiation of two discrete LTM8045 modules. While this physically increases the total PCB footprint, requiring two individual 6.25×11.25×4.92 mm BGA packages, it provides complete galvanic and thermal isolation between the positive and negative power pathways, potentially mitigating cross-channel noise coupling during heavy asymmetrical stimulation pulses. As depicted in the schematic implementation (Figure 3.15), the primary 5V source (VCC_5V) is fed in parallel to the V_{IN} terminals of both modules (U2 and U3), decoupled by a shared 4.7 μF input capacitor (C_{12}). The upper module (U2) is configured to generate the negative -7V rail (Vstim_-7V_LTM8045). This is achieved by operating it in an inverting topology, established by directly grounding its positive output terminal (V_{OUT+1} through V_{OUT+4}). The negative output voltage is strictly regulated by an 84.5 kΩ feedback resistor (R_{10}) connected between the active negative rail and the FB pin, explicitly following the manufacturer's inverting equation $R_{FB} = (|V_{OUT}| + 0.005)\,/0.0833$. The lower module (U3) is dedicated to generating the positive +7V rail (Vstim_+7V_LTM8045). This device is forced into a SEPIC topology by physically grounding its negative output terminal (V_{OUT-1} through V_{OUT-4}). The precise +7V output is dictated by a 69.8 kΩ feedback resistor (R_{12}) tied between the active positive rail and its respective FB pin, calculated using the SEPIC regulation formula $R_{FB} = (V_{OUT} - 1.215)\,/0.0833$. Both converters are synchronized to operate at 1 MHz. This switching frequency is independently programmed for each IC by connecting 90.9 kΩ resistors (R_{11}, R_{13}) from their respective RT pins to ground. To limit inrush currents from the 5V bus during activation, independent 10 nF soft-start capacitors (C_{14}, C_{16}) are integrated at the SS pins of each module. Finally, to ensure the delivery of a stable, low-ripple stimulation voltage to the neural front-ends, the negative rail is filtered by a 22 μF capacitor (C_{13}), while the positive rail utilizes a 47 μF capacitor (C_{15}).

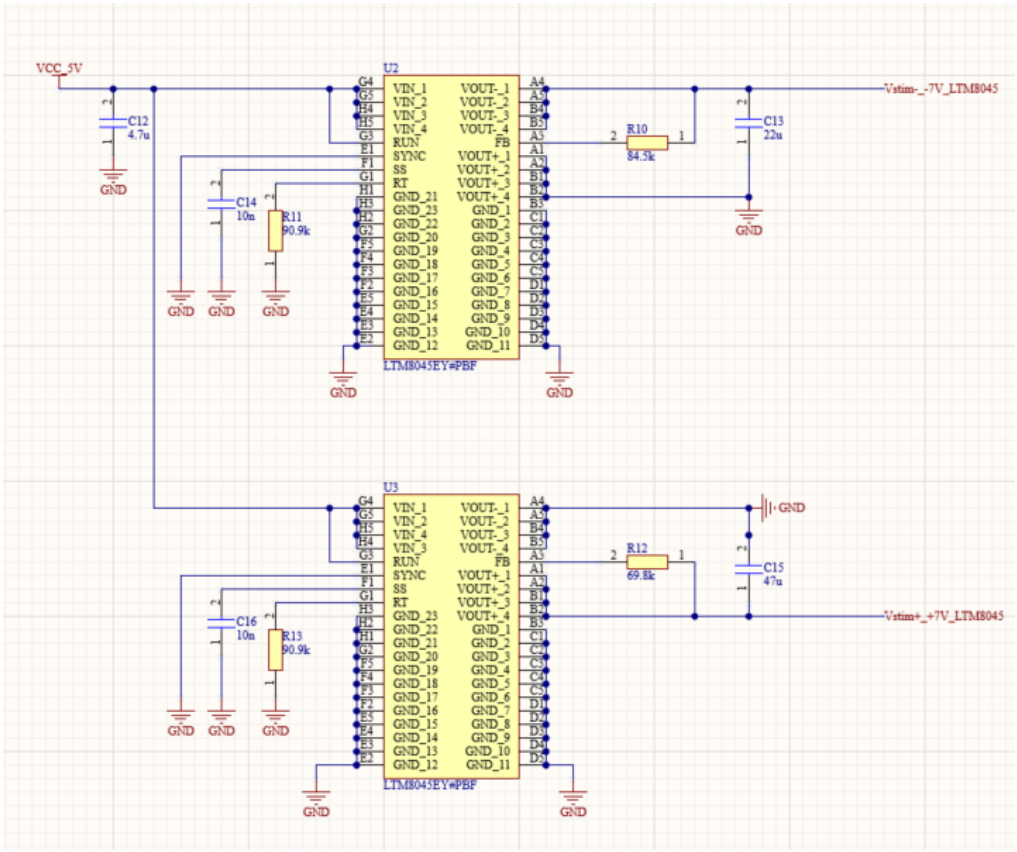


Figure 3.15: Schematic implementation of the symmetrical ±7V stimulation supply utilizing two independent LTM8045 μModules. The upper module (U2) is configured as an inverting converter to generate the negative rail, while the lower module (U3) operates in a SEPIC topology to provide the positive rail. Both devices are programmed to switch at 1 MHz via 90.9 kΩ RT resistors

An additional ±5V bipolar supply was incorporated into the power management architecture alongside the nominal ±7V and ±3.3V rails. The inclusion of this specific voltage level serves two fundamental engineering purposes. First, it offers an intermediate stimulation compliance voltage. If the neural electrode impedance during in-vivo or in-vitro testing proves to be lower than the worst-case estimates, driving the stimulation pulses at ±7V could result in unnecessary power dissipation and excessive thermal stress on the Intan front-ends. Providing a selectable ±5V fallback rail allows the operator to dynamically optimize the power efficiency of the stimulation stage without compromising the pulse integrity. Second, ±5V represents an industry-standard bipolar supply rail for a vast array of legacy operational amplifiers, multiplexers, and alternative analog front-ends. Its availability on the board guarantees that the NerveRepack shield remains backward-compatible and adaptable to future sensor architectures beyond the Intan RHS series. Finally,

generating ±5V exactly replicates the typical application benchmark provided in the manufacturer's specifications, serving as an ideal baseline circuit to validate the intrinsic noise and thermal performance of the selected μModules. To generate this intermediate rail, the design duplicates the previously validated dual-IC architecture, utilizing two additional LTM8045 μModule converters (U8 and U9). As shown in the schematic implementation (Figure 3.16), both modules draw power from the primary 5V bus (VCC_5V), sharing a 4.7 μF ceramic input decoupling capacitor (C_{28}). The upper module (U8) is specifically configured in an inverting topology to generate the -5V rail ($Vstim - _ - 5V_LTM8045$). This is accomplished by grounding its positive output terminal ($VOUT + _1$ through $VOUT + _4$). To set the precise -5V output, a 60.4 kΩ feedback resistor (R_{16}) is applied, accurately derived from the manufacturer's inverting formula $R_{FB} = (|V_{OUT}| + 0.005)/0.0833$. According to the optimal design parameters for this voltage step, the converter is programmed to operate at a switching frequency of 700 kHz by tying a 130 kΩ resistor (R_{17}) from the RT pin to ground. The output is then filtered by a 22 μF reservoir capacitor (C_{29}). The lower module (U9) is responsible for the symmetrical +5V rail ($Vstim + _ + 5V_LTM8045$). It operates in a SEPIC topology by grounding its negative output terminal ($VOUT - _1$ through $VOUT - _4$). The output voltage is strictly regulated by a 45.3 kΩ feedback resistor (R_{18}), calculated using the SEPIC regulation equation $R_{FB} = (V_{OUT} - 1.215)/0.0833$. To optimize efficiency for the positive conversion, the switching frequency is slightly increased to 800 kHz via a 115 kΩ timing resistor (R_{19}). To adequately suppress the ripple at this specific frequency and voltage, a massive 100 μF output capacitor (C_{31}) is utilized, directly adhering to the datasheet's optimal component selection table. Lastly, to ensure a safe and controlled power-up sequence that limits the inrush current drawn from the main 5V supply, both modules are equipped with independent 10 nF soft-start capacitors (C_{30}, C_{32}) connected to their respective SS pin.

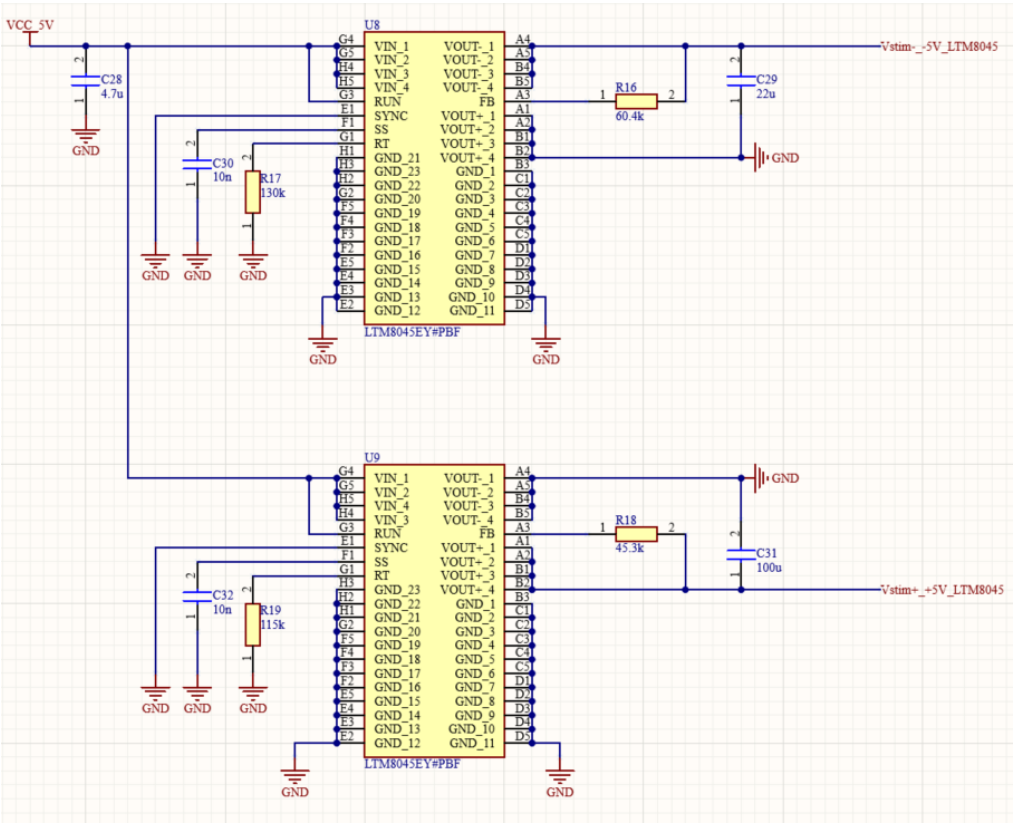


Figure 3.16: Schematic implementation of the auxiliary ±5V stimulation supply utilizing two LTM8045 μModules (U8, U9). The circuit replicates the manufacturer's optimal application baseline, providing an intermediate compliance voltage to optimize power dissipation during stimulation. U8 generates the -5V rail at 700 kHz, while U9 generates the +5V rail at 800 kHz, with dedicated output filtering networks tailored to each specific topology.

3.4 LT SPICE simulation

To validate the transient behavior, voltage ripple, and power efficiency of the designed circuits, a simulation phase was conducted using LTspice. Among the various power management components selected for the custom shield, the LTC3246, LTM8049, and LTM8045 provided an opportunity for computational analysis, as their models are available within the software's standard libraries, being original Linear Technology products. Although it was not possible to simulate every single component implemented on the board, this subset guarantees the validation of a representative component for every single voltage domain required by the system. Consequently, dedicated simulations were developed for all the main cases: the 3.3V logic supply (V_{DD}), as well as the ±3.3V, ±5V, and ±7V bipolar stimulation rails.

The LTC3246 charge pump was the first architecture to be computationally evaluated to validate the 3.3V logic supply generation. As depicted in (Figure 3.17), the LTspice schematic accurately replicates the intended hardware implementation, utilizing the exact external capacitor network ($C_{IN} = 1$ μF, $C_{FLY} = 2.2$ μF, $C_{OUT} = 47$ μF, $C_{BIAS} = 10$ μF). To accurately model the steady-state power demand of the Intan RHD recording front-end, a load resistor (R_{load}) was employed at the output node. Based on the maximum theoretical current draw of 6.8 mA calculated in Section 3.1, the load was determined via Ohm's Law as $R_{load} = 3.3\text{V} / 6.8\text{mA} = 485.29\ \Omega$. This mathematically forces the converter to operate exactly at the targeted boundary. To quantitatively assess the converter's steady-state performance, a transient analysis was executed over a 5 ms window. The initial 3 ms were intentionally discarded (`.tran 0 5m 3m startup`) to completely bypass the initial power-up transients and isolate the stable steady-state regime. The following SPICE `.MEAS` directives were embedded directly into the simulation environment to automatically compute the average power, overall efficiency, mean output voltage, and peak-to-peak ripple:

```
.MEAS TRAN P_IN AVG(abs(V(in) * I(V1)))
.MEAS TRAN P_OUT AVG(abs(V(out) * I(R1)))
.MEAS TRAN EFFICIENCY PARAM (P_OUT / P_IN)
.MEAS TRAN V_OUT_AVG AVG V(out)
.MEAS TRAN V_OUT_RIPPLE PP V(out)
```

In the output log the converter regulates an average output voltage of 3.29 V, demonstrating excellent load tracking. The peak-to-peak voltage ripple is strictly bounded to 20.6 mV_{pp} Furthermore, the extracted input power ($P_{IN} \approx 31.98$ mW) and output power ($P_{OUT} \approx 22.31$ mW) yield a simulated power efficiency of 69.7%. This computational result strongly corroborates the theoretical $\approx 66\%$ efficiency previously established for the 1:1 buck operating mode, with the slight positive variance attributed to intrinsic SPICE model parameters and internal bias current modeling. To better visualize the transient response, the raw LTspice data array was exported and plotted via MATLAB (Figure 3.18).

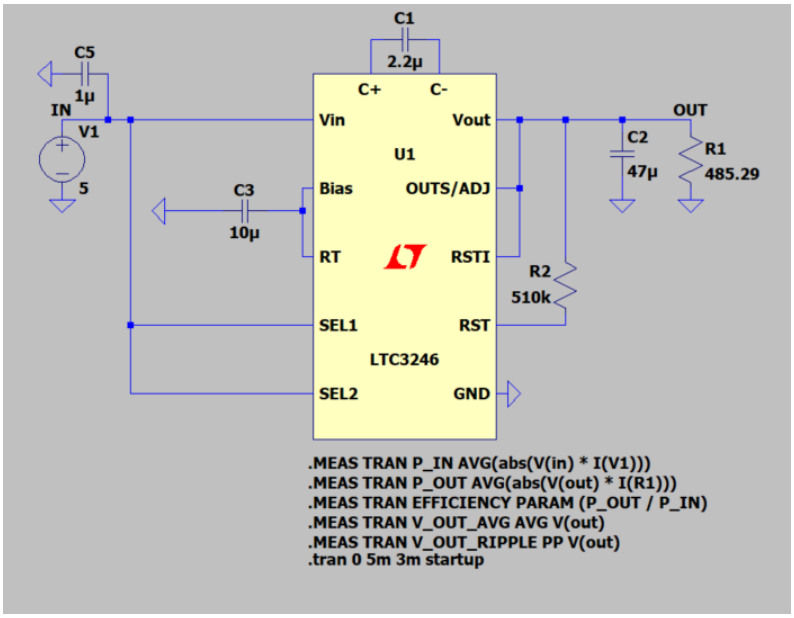


Figure 3.17: LTspice simulation schematic for the LTC3246 charge pump. The circuit utilizes the native Analog Devices component model and simulates a 6.8 mA worst-case current draw via the 485.29 Ω load resistor.

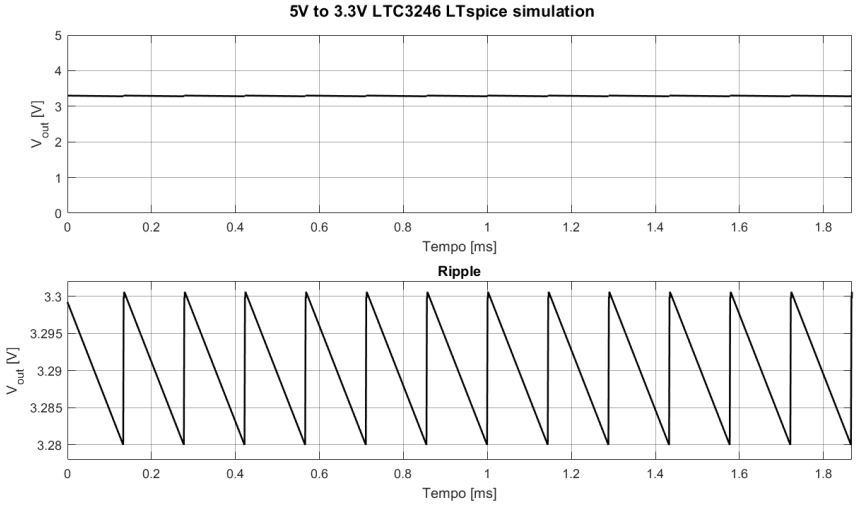


Figure 3.18: MATLAB plot of the exported LTspice transient data for the LTC3246. The top plot displays the steady-state macro-behavior, while the bottom plot isolates the 20.6 mV_{pp} hysteretic voltage ripple generated under the simulated load condition.

In addition to the baseline logic evaluation, a secondary SPICE simulation was

conducted on the LTC3246 schematic to accurately model the comprehensive load profile imposed by the *NerveRepack* project. In this specific application, the 3.3V rail generated by the charge pump does not exclusively supply the digital logic (V_{DD}). To minimize component count, this rail is directly routed to serve as the positive stimulation voltage ($Vstim+$) and simultaneously feeds the ICL7660S inverter to generate the symmetrical negative stimulation voltage ($Vstim-$). Consequently, the current demand account for the aggregate absorption of all these operational branches. Based on the system's power budget calculations, the peak current requirements are 9.55 mA for the V_{DD} logic, 0.75 mA for the positive stimulation rail, and 0.57 mA for the negative stimulation rail, resulting in a total demanded current of 10.87 mA. To physically model this simultaneous multi-rail power draw within the LTspice environment, the equivalent static load resistor was recalculated via Ohm's Law (R_{load} = 3.3V / 10.87 mA) and updated to 303.59 Ω. The converter maintains the target regulation with an average output voltage of 3.29 V, a peak-to-peak ripple of 20.6 mV_{pp}, and the simulated power efficiency settled at 65.3%.

Following the logic supply validation, a dedicated simulation was performed on the LTM8049 dual μModule to evaluate the generation of the ±7V stimulation rails required by the *Rewire* project. As shown in the LTspice schematic plot (Figure 3.19), the simulation models the dual-topology implementation: Channel 1 is configured as a SEPIC converter to output the positive rail, while Channel 2 operates in an inverting configuration for the negative rail. The model includes the complete passive network, including the specific 69.8 kΩ and 84.5 kΩ feedback resistors, as well as the output filtering stages. The component is tested under the worst-case stimulation scenarios described in Section 3.2, and independent static load resistors were calculated for each channel. Based on the maximum theoretical current consumption of the *Rewire* stimulation stage, the positive rail supply was 1.35 mA, while the negative was 1.121 mA. Using Ohm's Law, the equivalent simulation loads were set to R_{load1} = 7V / 1.35 mA ≈ 5185.18 Ω and R_{load2} = 7V / 1.121 mA ≈ 6244.42 Ω. A transient analysis was configured over a 6 ms window, and the start ramping phase was excluded; data logging was restricted to the final 2 ms of the simulation. Utilizing the same SPICE `.MEAS` of the LTC3246, the LTM8049 achieved a power efficiency of 88.35% (P_{IN} ≈ 20.77 mW versus a total P_{OUT} ≈ 18.35 mW). This high-efficiency metric proves that the magnetic step-up/inverting topology radically minimizes thermal dissipation compared to standard linear regulation, transferring almost the entirety of the power to the stimulation load. The average output voltages settled at 7.14 V and -7.28 V, as illustrated in the MATLAB transient plot (Figure 3.20), remain stable and flat across the evaluated operational window.

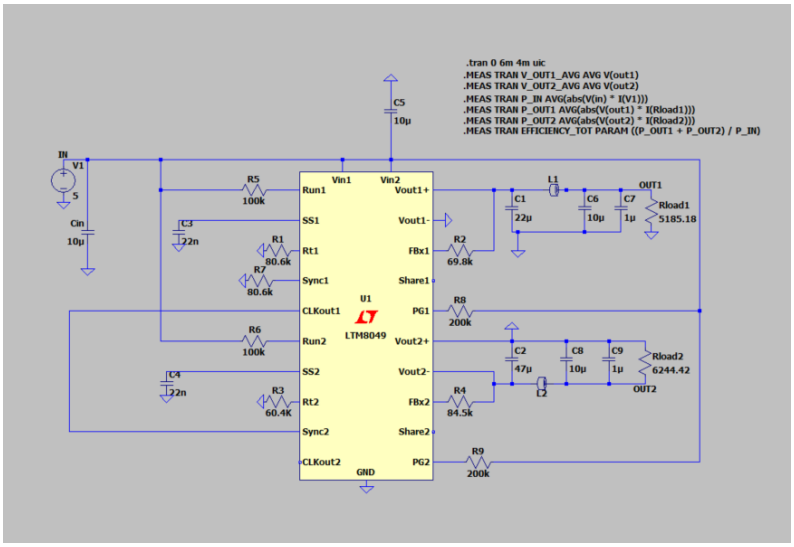


Figure 3.19: LTspice simulation schematic for the LTM8049 dual μModule. Channel 1 (top) is configured as a SEPIC converter, while Channel 2 (bottom) is configured as an inverting converter. The static loads (R_{load1} and R_{load2}) simulate the worst-case asymmetrical current draw of the Rewire stimulation stage.

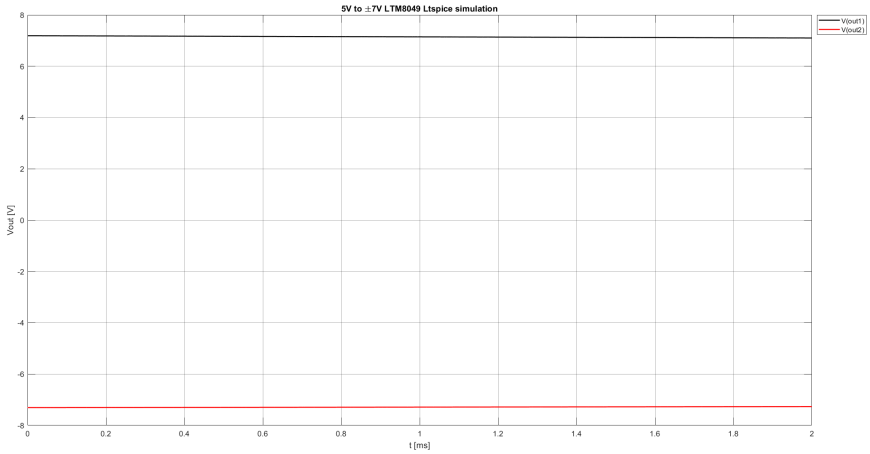


Figure 3.20: MATLAB plot of the exported LTspice transient data for the LTM8049. The graph demonstrates the simultaneous and stable generation of the positive (+7.14V) and negative (-7.28V) stimulation rails under the designated worst-case load conditions.

The auxiliary ±5V stimulation supply was evaluated using the dual LTM8045 architecture. The LTspice schematic (Figure 3.21) replicates the proposed hardware design, with module U1 configured in an inverting topology to generate the

negative rail, and module U2 configured as a SEPIC to generate the positive one. The simulation incorporates the exact passive networks defined in the schematic, including the 60.4 kΩ and 45.3 kΩ feedback resistors, and the 130 kΩ and 115 kΩ timing resistors to set the 700 kHz and 800 kHz switching frequencies, respectively. A nominal light-load condition of 1 mA per channel was established to evaluate the baseline regulations, and the loads were calculated as $R_{load+} = R_{load-} = 5\text{V} \ / \ 1\text{mA} = 5000\ \Omega$. The converters generate stable output voltages of 5.22 V and -5.13 V (Figure 3.22) with an efficiency of 49.5%.

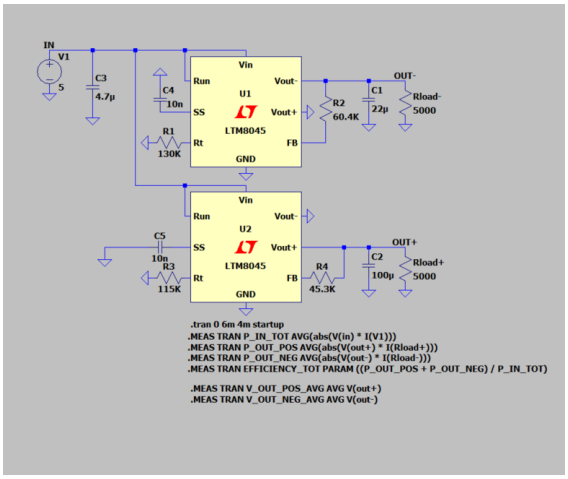


Figure 3.21: LTspice simulation schematic for the auxiliary ±5V supply utilizing two independent LTM8045 μModules.

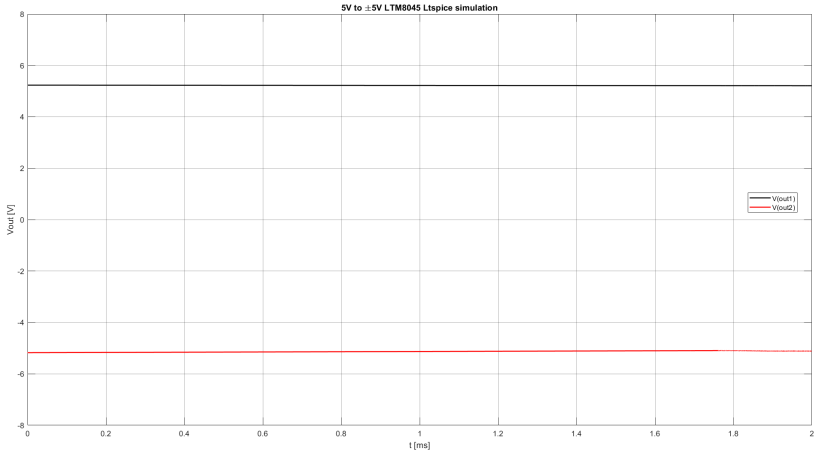


Figure 3.22: MATLAB plot of the exported LTspice transient data for the dual LTM8045 architecture. The graph confirms the stable generation of the +5.22V and -5.13V rails.

3.5 Shield schematic

The schematic of the custom shield is organized into different blocks to maximize readability and facilitate PCB routing operations.The individual functional blocks comprising the system architecture are detailed below:

- **Nucleo H7 DK connectors.** This block represents the physical interface between the custom shield and the host development board (STM32 Nucleo H7). Through these headers, referenced as CN11 and CN12, the shield extracts its primary 5V power supply and establishes the system ground. The block is critically responsible for routing the high-speed digital communication lines, dividing the data across two distinct Serial Peripheral Interface (SPI) buses of the STM32 microcontroller. The SPI1 peripheral is dedicated to the microSD, and the lines are sent to the microcontroller pins PA6, PA7, PA5, and PA4, respectively. The SPI2 peripheral manages the Intan RHS and RHD headstages. The signals are mapped to different GPIO pins on the STM32: the RHS pins are PB14, PB15, PB10, and PB4 for MISO, MOSI, SCLK, and CS; the RHD pins are PC2, PC1, PD3, and PA11. Finally, from a signal integrity perspective, the schematic illustrates that all SPI lines directed towards the RHS and RHD transceivers are equipped with 22 Ω series resistors (e.g., R20, R22-R28). These discrete components act as source termination resistors, explicitly placed to dampen high-frequency ringing, mitigate signal reflections, and ensure reliable data transmission across the external cables connecting the shield to the active neural front-ends.

- **DK Power Supply FB, capacitor and LED.** This section is dedicated to the primary filtering of the power supply from the Nucleo board. The raw supply line initially passes through a ferrite bead (FB4), which is a passive low-pass filter designed to attenuate high-frequency noise and electromagnetic interference (EMI). To stabilize the rail and provide local energy storage over a wide frequency range, a parallel decoupling capacitor bank made of a 100 nF ceramic capacitor (C36), a 1 μF capacitor (C37), and a 22 μF capacitor (C38) is tied to ground. The clean supply is distributed by a connector J2. Furthermore, this block also has a power visual indicator made of a surface-mount LED (LED1, model SML-P11MTT86) and a 1.8 kΩ current-limiting resistor (R21). This LED is located directly between the VCC_5V rail and the ground of the system, provides visual feedback to the operator immediately, and is illuminated when the system is energized to confirm that the primary power supply is active.

- **External Power Interface.** The shield incorporates a dedicated external power input with a 4-pin connector (J1) to bypass the onboard regulators and directly access independent external voltages for the logic supply (Ext_VDD_+3.3V), the positive stimulation rail (Ext_Vstim+), and the negative stimulation rail (Ext_Vstim-). Since external power provided over long laboratory cables is highly susceptible to picking up electromagnetic interference (EMI) and environmental noise, each incoming line is subjected to a rigorous localized filtering stage upon entering the board. Specifically, each rail passes through a surface-mount ferrite bead (model BLM18AG601SZ1D) acting as a high-frequency noise suppressor, immediately followed by a robust decoupling bank consisting of 100 nF, 1 μF, and 22 μF capacitors connected in parallel to the system ground.

- **Voltage selection.** It acts as the central power routing of the custom shield and allows the operator to dynamically assign the neural front-end with standard physical jumper shunts. The design comprises three main selection pin headers. The first header (J5) governs the 3.3V digital logic supply for both the headstages. The voltage is selectable to power independently the VDD_3.3V_RHS and VDD_3.3V_RHD nets by choosing from the comprehensive array of integrated step-down converters (the LTC3246 and MCP1253 charge pumps, the 173950336 magnetic module, the AZ1117C linear regulator, or an external supply). The second header is J7, and it is dedicated to the positive stimulation rail VSTIM+. It is possible to select from the project-required voltages such as +7V from the LTM8049 or LTM8045 modules, an intermediate +5V rail, the raw 5V Nucleo supply, any of the 3.3V logic sources, or an external input. The third header, J8, configures the negative stimulation rail (VSTIM-), providing direct access to the -7V and -5V outputs generated by the respective LTM μModules, as well as an external input option. To

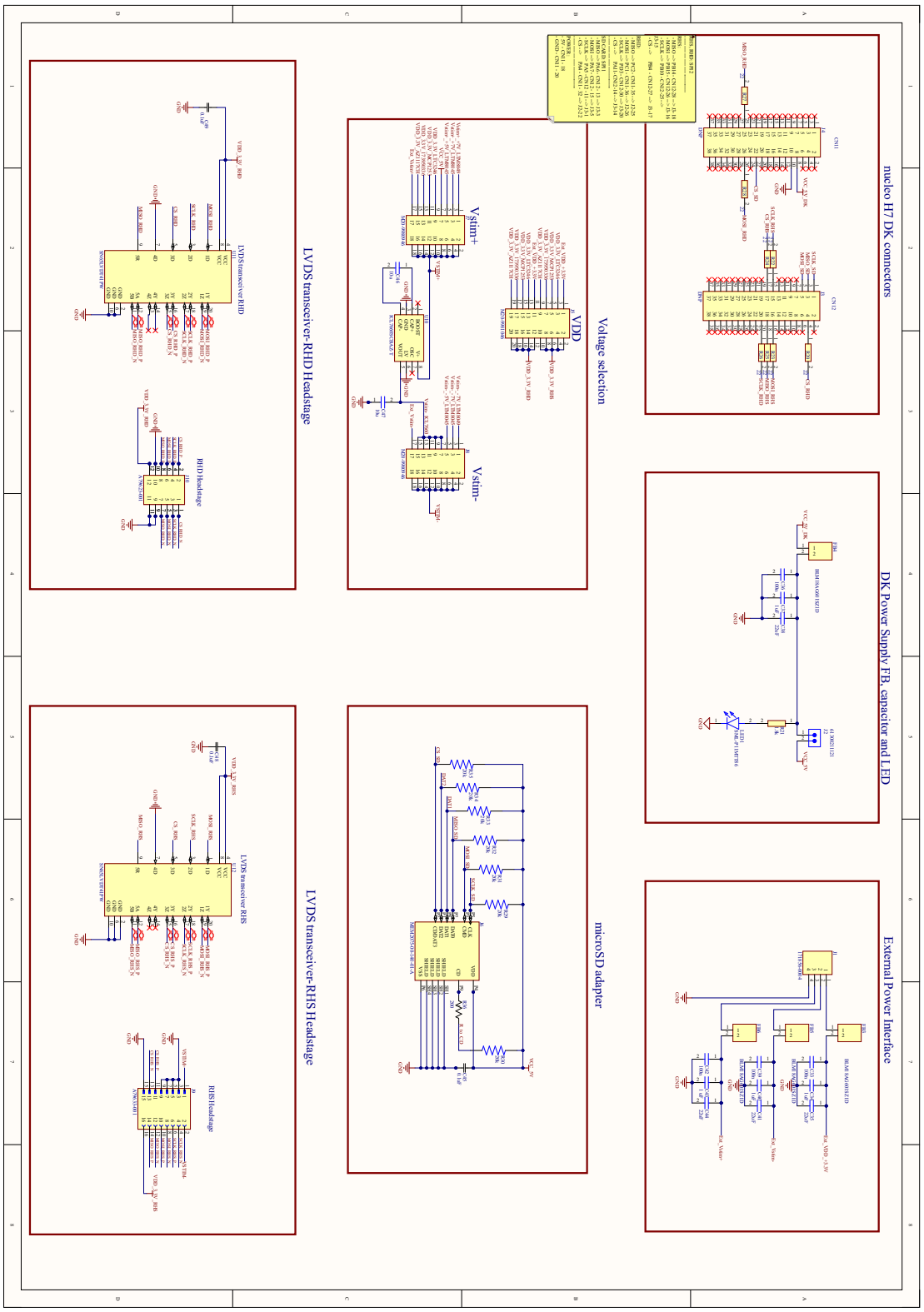
generate -3.3V stimulation voltages without the need for additional dual converters for every possible rail, this routing section integrates the ICL7660S monolithic voltage inverter (U10) into the signal path. As illustrated in the schematic, the dynamically selected +3.3V VSTIM+ nets are routed directly into the supply pin (V+) of the ICL7660S. Utilizing a 10 μF flying capacitor (C46) and a corresponding 10 μF output reservoir capacitor, the chip actively inverts the positive potential to output the negative rail (Vstim-_ICL7660). This inverted output is sent back to the J8 header, ensuring that a perfectly symmetrical bipolar stimulation supply can be easily established and transferred to the VSTIM- net utilizing a minimal component footprint.

- **microSD adapter.** This area provides the hardware required to connect the SD storage to save the acquired neural data. The block consists of the physical card slot, bypass capacitors, and a series of pull-up resistors on the SPI bus lines to guarantee the integrity of high-speed digital signals.

- **LVDS transceiver - RHD Headstage.** The module is the critical digital communication interface between the external Intan RHD chip and the shield. Because SPI signals are highly susceptible to capacitive degradation and electromagnetic interference (EMI) this section implements a differential signaling architecture. At the heart of this interface is the U11 LVDS transceiver, the SN65LVDT41PW, which translates standard single-ended CMOS logic levels into Low-Voltage Differential Signaling (LVDS). The LVDS is powered by the dedicated VDD_3.3V_RHD logic rail,with a 0.1 μF bypass capacitor (C49). On the transmission side, the single-ended SPI control signals originating from the microcontroller (MOSI_RHD, SCLK_RHD, and CS_RHD) are fed into the driver inputs of the transceiver. The device then generates the corresponding differential pairs, denoted with _P (positive) and _N (negative) suffixes, to drive the external cable. All these high-speed differential data pairs, along with the VDD_3.3V_RHD power supply and system ground, are bundled into the J10 Omnetics connector (model A79623-001).

- **LVDS transceiver - RHS Headstage:** Analogous to the preceding block, this section provides the differential signaling interface and the specific physical connection for the Intan RHS headstage, which is uniquely dedicated to combined neural recording and electrical stimulation operations. The electromechanical mating is established via an Omnetics A79633-001 connector (J9). Alongside the high-speed differential communication lines, the logic power supply, and the system ground, this high-density connector explicitly routes the dynamically selected bipolar power rails, denoted as VSTIM+ and VSTIM-.

The following schematic illustrates the complete integration of these functional blocks.


nucleo H7 DK connectors
Voltage selection
VDD
Vstim+
Vstim-
DK Power Supply FB, capacitor and LED
External Power Interface
microSD adapter
LVDS transceiver-RHD Headstage
LVDS transceiver-RHS Headstage

3.6 PCB Layout and Routing

The physical layout and mechanical design of the PCB were engineered to ensure seamless integration with the host system and maximize laboratory ergonomics. As illustrated in the 3D CAD rendering and top-layer view (Figure 3.23), the board measures exactly 70 mm by 90 mm. This specific footprint was designed to act as a dedicated expansion shield, providing perfect electromechanical alignment with the male header pins of the underlying STM32 Nucleo H7. Also, all components requiring external physical interaction were placed along the perimeter of the PCB, such as the microSD card adapter for continuous data logging and the dedicated header pins for external power injection. In the central area of the top layer are placed the pin-header matrices dedicated to dynamic voltage selection. This highly visible and accessible configuration allows the user to easily route the desired potentials for both the logic supply (VDD_3V3) and the bipolar stimulation rails (Vstim+ and Vstim-), effectively centralizing the power management routing between the onboard regulators and the neural headstage interfaces.

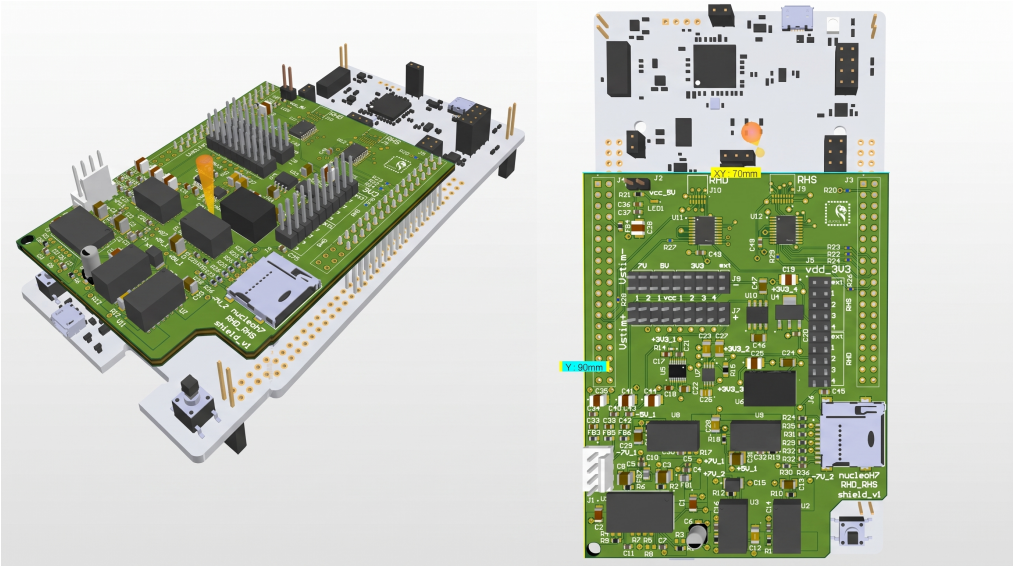


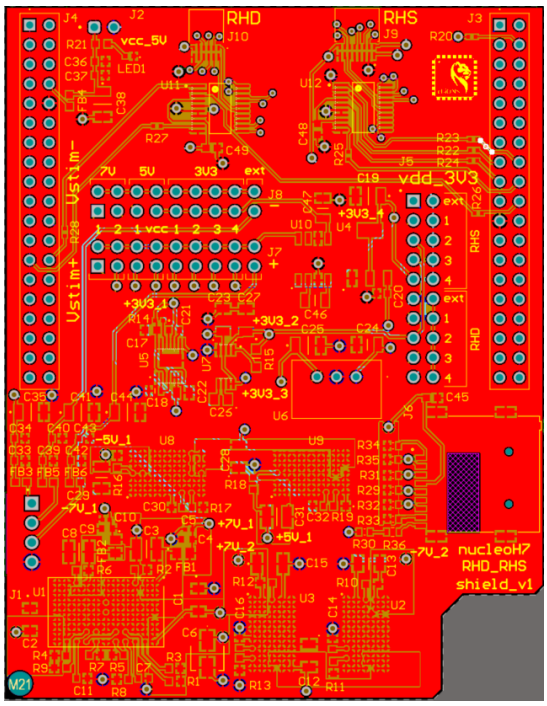
Figure 3.23: Three-dimensional Altium Designer rendering of the custom shield mounted on the STM32 Nucleo H7.

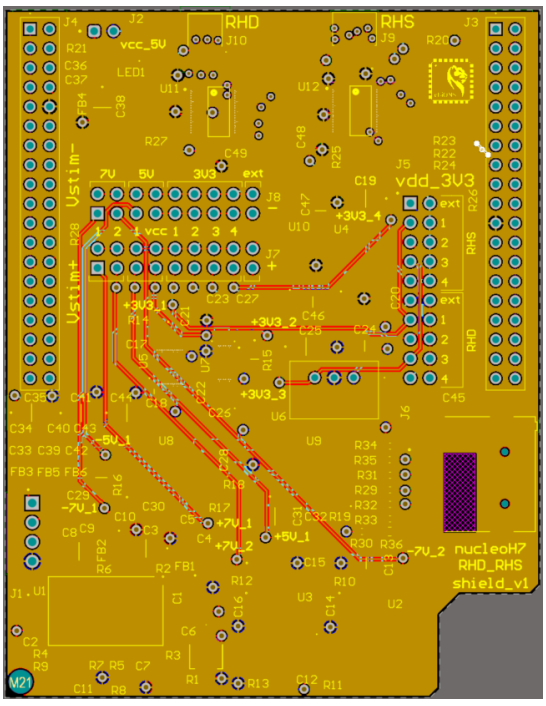
To support high-frequency digital communications, multiple switching power supplies, and a high component density within the strict geometric constraints imposed by the STM32 Nucleo footprint, a 4-layer PCB stack-up architecture was designed (Figure 3.24). Since the sheer volume of power tracks for the selectable VDD logic rails and the bipolar Vstim stimulation voltages could not be routed exclusively on the outer surfaces without causing critical spatial bottlenecks and trace crossovers, the two inner copper layers (Figure 3.24b and 3.24c) were used

as subsurface routing channels. These inter-layer transitions were performed with standard 1.27 mm diameter through-hole vias and a track width of 0.3 mm to reduce DC resistance and accommodate transient current demands. The Design Rule Check was followed to guarantee Design for Manufacturability (DFM) and prevent short circuits, with a global minimum clearance of 0.15 mm rigorously maintained between all discrete copper elements (tracks, pads, vias, and polygon pours). In addition to signal and power routing, a continuous ground plane (GND) was implemented on all four layers using the polygon pour function for three reasons: signal integrity by offering low-impedance return paths for high-speed traces and decreasing loop inductance, thermal management by using the copper mass to dissipate heat from power ICs, and power integrity by maintaining a stable 0V reference potential across the shield. As observed in the top and bottom layer layouts (Figure 3.24a and Figure 3.24d), the digital lines are routed on the outer surfaces of the PCB. The SPI tracks connecting the Nucleo headers to the transceivers were routed with a standard 0.25 mm width, ensuring reliable signal integrity over the longer physical distances across the shield, while the LVDS differential pairs connecting the transceivers to the output connectors were routed with a trace width of 0.219 mm. This dimension was calculated according to the PCB dielectric stack parameters to achieve the required controlled differential impedance of 100 Ω, which is strictly necessary to prevent signal reflections and ensure high-speed transmission to the neural headstages. Focusing on the top layer, the layout of the power management μModules closely follows the design guidelines provided by the manufacturers' evaluation boards. To minimize high-frequency switching noise and optimize the regulators' performance, critical passive components, such as decoupling capacitors and feedback resistors, were placed as close as possible to the IC pads. Furthermore, instead of using standard routing traces for power delivery, wide copper pours (polygons) were drawn directly on the top layer. As shown in the LTM8049 BGA footprint detail (Figure 3.25), these solid copper regions connect not just the ground pins, but also the main power nodes, such as the VCC_5V input and the stimulation outputs. Using these top-layer copper pours rather than standard tracks lowers the DC resistance, prevents voltage drops under load, and significantly improves the thermal dissipation directly from the BGA pads of the converters.

(a) Top layer

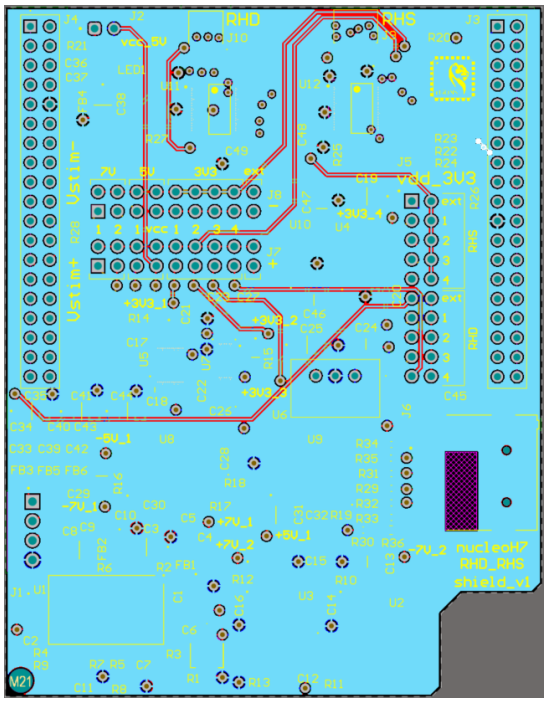
(b) Inner 1





(c) Inner 2

(d) Bottom layer



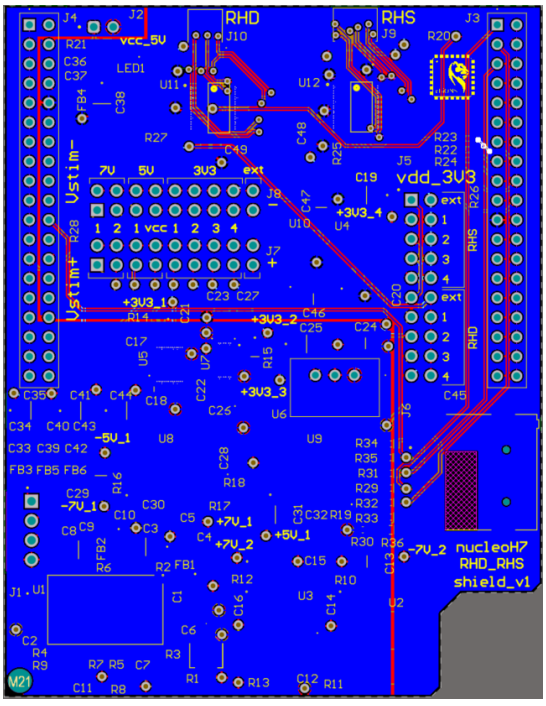


Figure 3.24: Layer-by-layer breakdown of the 4-layer PCB routing. (a) Top layer, hosting the primary components, voltage selection matrices, and major power traces. (b) Second inner layer and (c) Third inner layer, predominantly acting as inner ground planes and routing channels for internal power and signal crossing. (d) Bottom layer, containing the external connections and bottom-side data traces.

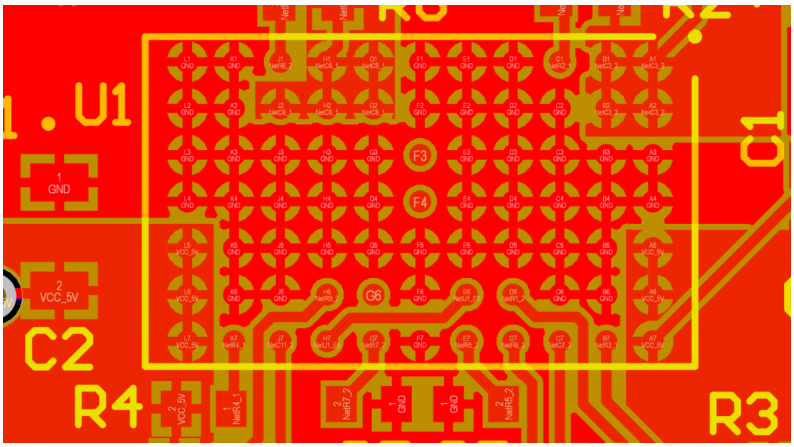


Figure 3.25: Detailed top-layer routing of the LTM8049 μModule footprint.

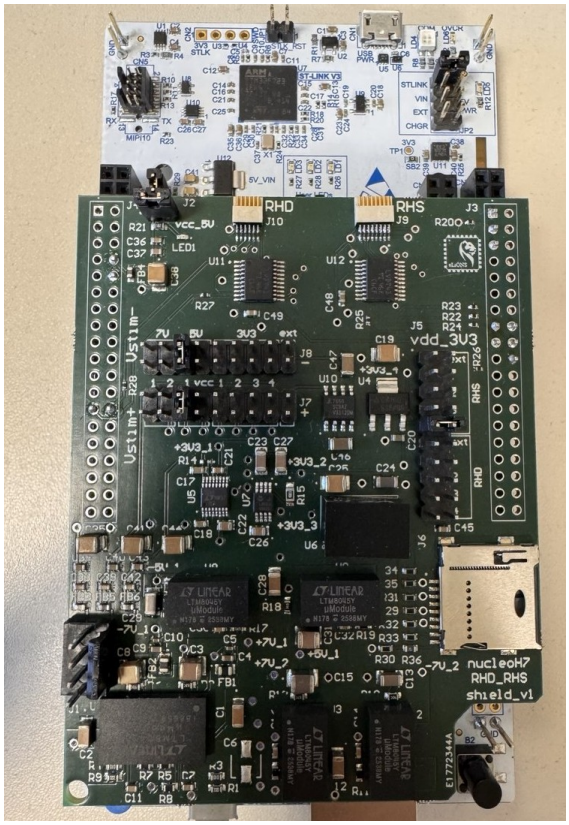


Figure 3.26: The picture shows the fully assembled custom neural shield physically mated to the host STM32 Nucleo H7 development board.

Chapter 4

PNT Development

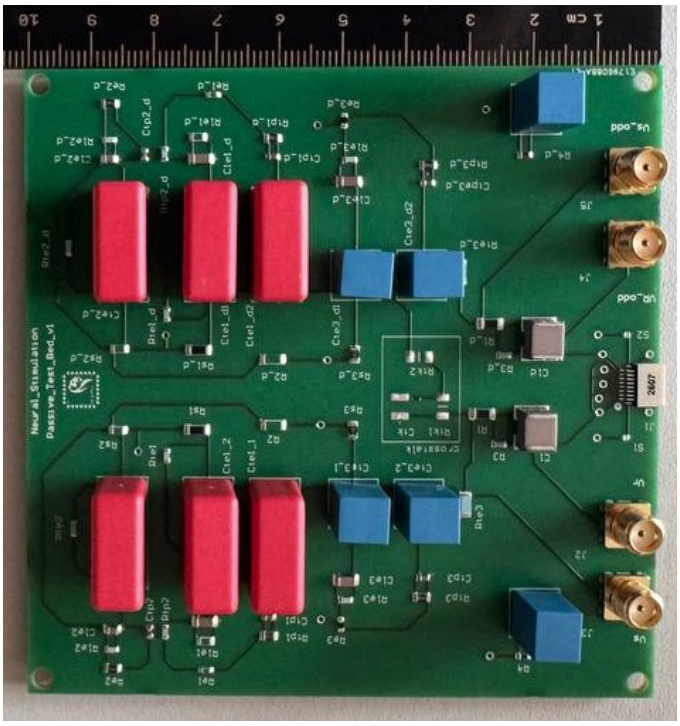


Figure 4.1: Fully assembled Passive Nerve Testbed (PNT) board.

Following the design of the shield, the next step of the hardware development phase was to develop the Passive Nerve Testbed (PNT), illustrated in Figure 4.1. The objective of PNT is to provide a stimulation and recording system, comprising STM Nucleo, the custom shield, and the Intan headstages, with a PCB that mimics the electrical impedance of a cuff electrode interfaced with a peripheral nerve. Recreating this operational environment required a detailed evaluation of two distinct

physical phenomena: the electrochemistry of the electrode-electrolyte coupling and the electrical properties of the biological tissue. As shown in the conceptual block diagram in Figure 4.2, the resulting PNT architecture translates these physical interactions into a structured lumped-parameter circuit. The electrical path is made up of the electrode-electrolyte interfaces at both the stimulation input and the return to ground, and they are modelled using a parallel $R_e - C_e$ network, with parameters directly extracted from Electrochemical Impedance Spectroscopy (EIS) tests performed on the physical Nerverepack cuff deliverables. Bridging these two contact points is the central tissue impedance block (Z_{tissue}). This section is characterized by the development of a Finite Element Method (FEM) in COMSOL Multiphysics recreating a peripheral nerve enveloped by a designed electrode. From this model, the impedance contribution of the biological tissues was extracted across the frequency spectrum and then reproduced as a lumped-parameter equivalent circuit, allowing the complex electrical behavior of the nerve to be physically reproduced on the PNT board.

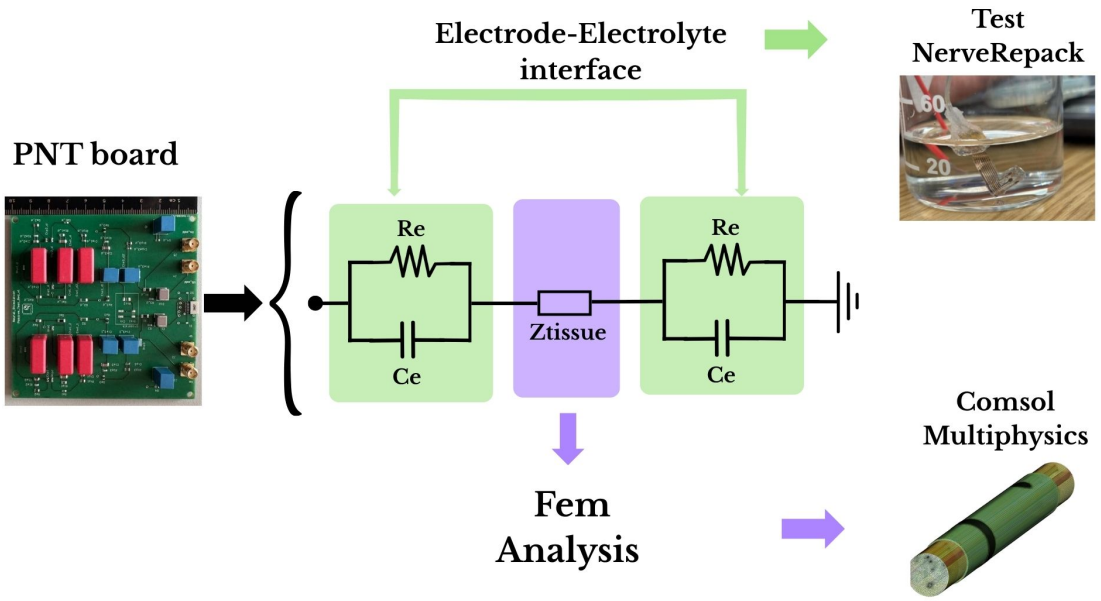


Figure 4.2: Conceptual framework of the Passive Nerve Testbed (PNT) board design. The overall target impedance is synthesized by combining the electrode-electrolyte interface, modeled as a parallel $R_e - C_e$ network derived from empirical EIS testing on the physical Nerverepack cuff, and the peripheral nerve tissue impedance (Z_{tissue}). The tissue contribution was evaluated via COMSOL Multiphysics FEM analysis of a modeled nerve-cuff arrangement.

4.1 Electrode-Electrolyte interface

The first barrier that a stimulation or recording electrode must cross is the physical coupling at the electrode-electrolyte boundary. During electrical stimulation, irreversible Faradaic reactions result in a net change in the local chemical environment, which can lead to toxic species harmful to both the surrounding excitable tissue and the electrode itself. Electrical equivalent circuits are therefore needed to translate these physiological and electrochemical phenomena into functional engineering tools. The standard theoretical equivalent circuit model used to describe this interface impedance is illustrated in Figure 4.3. The physical double layer formed by opposite charges is described by the capacitance (C_{dl}). However, the interface is not a perfect insulator: the charge that manages to leak across this boundary to participate in the Faradaic electrochemical reactions encounters a natural opposition. In the electrical model, this specific opposition to electron transfer is defined as the charge transfer resistance (R_{ct}). In addition, these Faradaic reactions are based on ions displacing from the bulk of the electrolyte to the interface at a finite rate, which gives rise to the Warburg impedance, mathematically expressed as $Z_w = (1 - j)\sigma\omega^{-0.5}$ where σ is the diffusion coefficient and ω is the angular frequency of the applied signal [15]. The diffusion and the charge transfer resistance, respectively Z_w and R_{ct}, form the Faradaic branch of the circuit in parallel to the double layer capacitance, C_{dl},. Finally, to complete the four-component model, this entire parallel interface block is placed in series with the spreading resistance R_s. This final component represents the purely ohmic resistance of the bulk electrolyte solution (the biological tissue or saline medium) that exists between the active electrode and the reference ground.

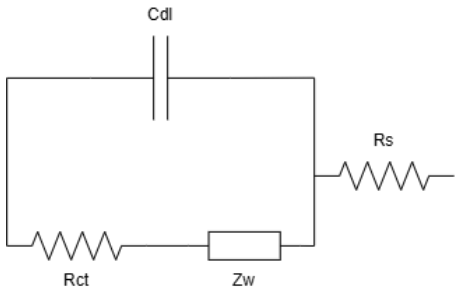


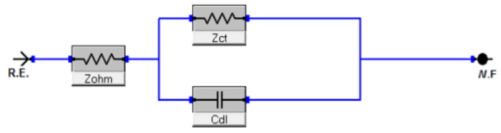
Figure 4.3: Theoretical equivalent circuit model of the electrode-electrolyte interface impedance. In the schematic (C_{dl}) is the double layer capacitance describing the physical charge separation; parallel Faradaic branch includes charge transfer resistance (R_{ct}) representing electrochemical reactions and Warburg impedance (Z_w) ion diffusion; complete parallel interface block connects in series with spreading resistance (R_s) defining ohmic properties of bulk electrolyte.

However, in real bioelectronic applications, this model is always greatly simplified due to the operating frequency and the electrochemical nature of the electrode. On the relatively high frequencies that are usually used to measure the impedance of a solid biomedical electrode, the double layer capacitance gives the interface a low impedance path that will bypass the Faradaic branch, i.e., the impedance of the interface is given by the capacitance in series with the sum of the lead and electrolyte resistances. In contrast, looking at the interface in the very wide frequency range, we can observe the parallel R_{ct}. Even in this broad frequency range, the Warburg diffusion impedance can be omitted if the electrode is very polarizable. In this case, the Faradaic resistance (R_{ct}) is very large, so there is virtually no direct current flow. Because no significant redox reactions occur to consume reactants, the mass-transport diffusion of ions to the interface is not a rate-limiting step, rendering the Warburg impedance practically negligible[15].

To quantify this interface accurately, the exact parameters of the electrical equivalent circuit should be mathematically determined. The Faradaic charge transfer resistance (R_{ct}) is governed by electrochemical kinetics and can be calculated from the Butler-Volmer equation with a low-field approximation: $R_{ct} = \frac{RT}{J_0 z F}$ where R is the gas constant, T is the temperature, J_0 is the equilibrium exchange current density, z is the number of electrons involved in the redox reaction, and F is Faraday's constant.

This equation underlines that the charge transfer resistance of a Faradaic electrode is inversely proportional to the equilibrium exchange current density (J_0) and therefore an ideally polarizable electrode has an exchange current that is close to zero, which is what makes the Faradaic transfer resistance of an electrode massive enough to halt Faradaic reactions. In series with this whole interfacial boundary is the solution resistance (R_S), which represents the resistance encountered by current spreading out into the bulk electrolyte and depends only on the geometric area of the surface. In addition to these resistive components, the model needs to account for the capacitive storage of charge. Theoretically, the metal surface is perfectly smooth, and the charge accumulation is homogeneous as in an ideal capacitor C_{dl}. However, real electrodes present microscopic surface roughness and porosity, causing an inhomogeneous distribution of the charge and the deviation of the capacitive behaviour from constant to frequency-dependent. In the case the classical capacitor is replaced by a theorical component called a Constant Phase Angle (CPA) impedance which is defined as $Z_{CPA}(\omega) = \frac{1}{(j\omega Q)^n}$, where Q is the impedance magnitude, ω is the angular frequency and n ranges from 0 to 1, is the surface inhomogeneity factor. When $n = 1$, the surface is smooth, and the CPA element is just an ordinary capacitor [33]. In this contest, Electrochemical Impedance Spectroscopy (EIS) is the most common technique used to assess the electrode properties and functions. It involves applying a sinusoidal electrical stimulus to the electrode immersed in a saline solution over a wide frequency range. By recording the amplitude reduction and the phase shift, the frequency-dependent

changes are shown, and the physical reaction is elucidated. At high frequencies, the double-layer capacitance acts as a short circuit, and the impedance represents the purely resistive electrolyte and tissue. As the frequency decreases, the impedance $|Z|$ rises, and the phase angle (θ) dynamically shifts between a purely resistive (0°) and a purely capacitive (-90°) response [34]. By capturing the full spectrum, the recorded complex data can be fit to an equivalent electrical circuit model using a least-squares fit, allowing the characterization of physical mechanisms: double-layer capacitance C_{dl}, charge transfer resistance R_{ct}, and solution resistance R_s. The practical application of this theoretical framework can be clearly demonstrated in the experimental characterization of state-of-the-art neural interfaces developed within the NerveRepack project. To convert these neural interfaces to equivalent circuits the project performed Electrochemical Impedance Spectroscopy of the flexible soft cuff electrodes, based on a Thermoplastic Polyurethane (TPU) substrate with embedded gold tracks [35]. By immersing the cuff electrodes in a 0.9% NaCl physiological solution, the researchers applied the aforementioned fitting process to successfully extract the exact physical parameters of the simplified classical circuit model directly from the experimental EIS data. The measurements yielded an average solution resistance of approximately 356 Ω, and an average double-layer capacitance of 3.01×10^{-7} F. Most importantly, the extracted charge transfer resistance was exceptionally high, averaging $1.24 \times 10^{8}\Omega$. This massive Faradaic resistance explicitly confirms a quasi-ideal polarizable behavior at the electrode interface. Because the resistance is extremely high, virtually no DC electron transfer occurs across the boundary, meaning no significant redox reactions take place. This practical finding elegantly closes the theoretical loop: since no Faradaic current flows and the process is overwhelmingly capacitive, there is no mass-transport diffusion of chemical reactants required. Consequently, these in vitro EIS results not only confirm the exceptional safety and electrochemical stability of the Nerve Repack electrodes, but they also provide the ultimate experimental justification for the theoretical exclusion of the Warburg diffusion impedance.



(a)

	Z[ohm]	Zct[ohm]	Cdl [F]
1_3	3,80E+02	1,10E+09	3,48E-07
1_5	3,64E+02	8,47E+05	3,33E-07
1_6	3,48E+02	1,00E+06	3,25E-07
1_7	3,54E+02	9,88E+05	3,02E-07
1_8	3,33E+02	1,33E+06	3,00E-07
2_1	8,33E+01	1,38E+05	2,42E-06
2_3	3,56E+02	1,29E+06	2,88E-07
2_5	3,55E+02	1,55E+06	2,58E-07
2_6	3,48E+02	1,30E+06	2,74E-07
2_7	3,67E+02	1,32E+06	2,80E-07
Avg (electrode)	3,56E+02	1,24E+08	3,01E-07
SD (electrode)	1,26E+01	3,46E+08	2,78E-08
GND electrode	8,33E+01	1,38E+05	2,42E-06

(b)

Figure 4.4: (a) Classical circuit model determined from the electrochemical measurements (b) Values determined from the classical circuit model [35].

To computationally validate the theoretical behavior of the electrode-electrolyte barrier and as a fundamental preliminary step before physically integrating this equivalent load in the PNT, the circuit was simulated in LTspice. The AC sweep analysis utilized the average physical parameters from the average experimental EIS data summarized in Figure 4.2b: solution resistance $R_s = 356\ \Omega$, average double-layer capacitance $C_{dl} = 3.01 \times 10^{-7}$ F, and charge transfer resistance $R_{ct} = 1.24 \times 10^{8}\ \Omega$. The results of this AC frequency analysis are represented in the Bode plot in Figure 4.5 and show the frequency-dependent nature of the electrode interface. At higher frequencies, the double-layer capacitance (C_{dl}) effectively acts as a short circuit, and the overall impedance clamps directly to the ohmic value of the solution spreading resistance ($|Z| \approx 356\ \Omega$), while the phase angle is equal to $0°$ to indicate a resistive behavior. In the lower and mid-frequency regions, the interface becomes dominated by the capacitive reactance of C_{dl}. This capacitive component is highlighted by the linear increase of the impedance magnitude when the frequency decreases, accompanied by a phase angle closely approaching $-90°$. Since the charge transfer resistance (R_{ct}) is high, it is completely bypassed by the AC signal, and the Faradaic branch is practically open. This simulated frequency response characterized by a high-frequency resistive plateau and a dominant low-frequency capacitive slope, is highly consistent with the electrochemical behavior of gold-contact cuff electrodes documented in the literature [36], [37].

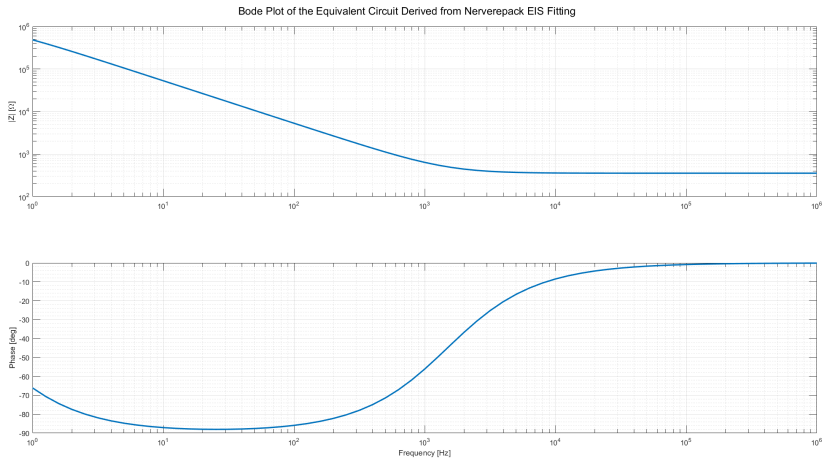


Figure 4.5: Bode plot (magnitude and phase) of the equivalent electrode-electrolyte circuit simulated via LTspice/MATLAB. The response highlights a capacitive behavior at low frequencies and a purely resistive plateau at high frequencies.

4.2 Tissues impedance modeling

To accurately evaluate the specific electrical impedance contribution introduced by the biological tissue, it was necessary to develop a realistic model of the target peripheral nerve. Existing literature exhibits significant variability regarding nerve morphological and electrical parameters, which are dependent on the species and the anatomical extraction site. To overcome this generalization and tailor the analysis to the specific requirements of the targeted application, a 3D FEM simulation was developed utilizing COMSOL Multiphysics software. This computational approach was specifically engineered to faithfully reproduce the physiological structure and the bioelectrical properties of a human median nerve located at the level of the forearm.

4.2.1 Cross-sectional geometry

Peripheral nerves are composed of bundles of nerve fibers and surrounding connective tissue sheaths, which are hierarchically organized into three primary layers. At the innermost level, each nerve fiber and its supporting Schwann cells are surrounded by a loose connective tissue called the endoneurium. Multiple nerve fibers are then held together by collagen fibrils to form a distinct bundle known as a fascicle, which is bounded by a dense connective tissue called the perineurium. Finally, all the independent fascicles within a single nerve trunk are completely surrounded by the epineurium, a dense and irregular connective tissue that serves as the outermost protective layer of the nerve.

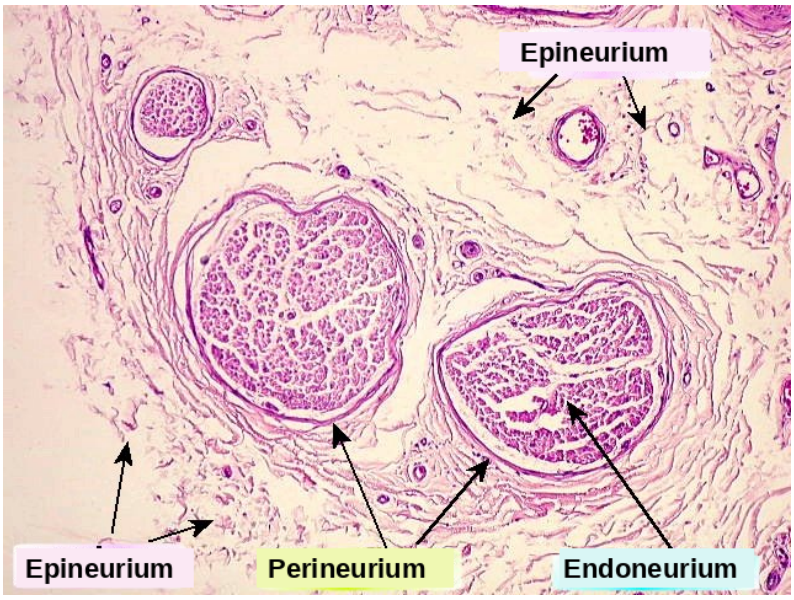
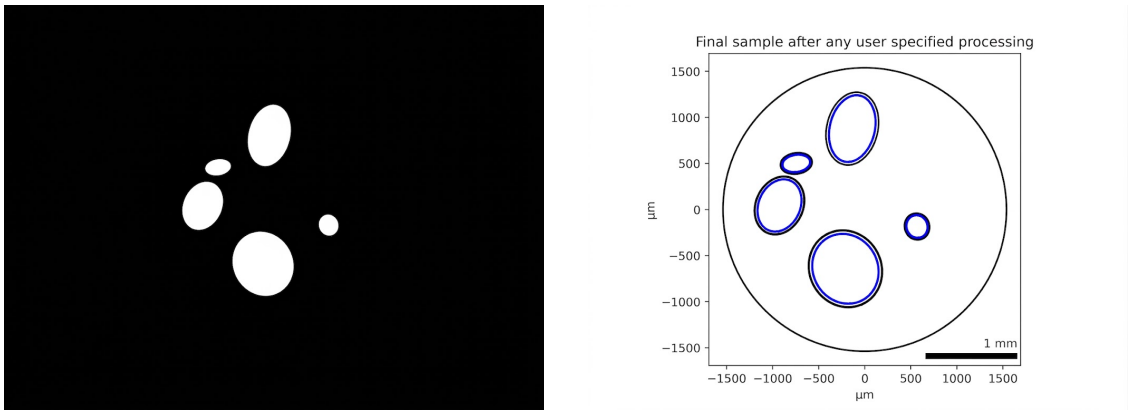


Figure 4.6: Histological transverse section of a peripheral nerve illustrating its hierarchical connective tissue architecture. The outermost epineurium encapsulates the entire nerve structure. The dense perineurium delineates the individual nerve fascicles. The internal endoneurium separates the single nerve fibers within each fascicle.

The open-source *Ascent* pipeline developed by Duke University was used to generate the median nerve's cross-sectional geometry. Because subject-specific histological images of the nerve were not available for this study, the pipeline's mock morphology generator [38] provided a representative 2D anatomical mask of the human median nerve at the forearm level. Based on the custom configuration parameters provided, the simulated median nerve achieved a total cross-sectional area of approximately 4.75 mm^2 [39]. A simplified multifascicular model reconstructed the internal topology, featuring 5 distinct fascicles randomly positioned within the epineurium (Figure 4.7). The structure was determined by a set of physical and geometric parameters. To prevent unphysical overlapping of the domains during finite element meshing, the boundary between them was set to be at least 15 µm distant from each other and from the outer epineurium. Since peripheral nerves are highly compliant structures that naturally deform in contact with a rigid implant, the algorithm simulated the mechanical deformation of the nerve into a circular profile, closely mimicking the physical compression exerted by a standard cylindrical cuff electrode. The pipeline automatically extracted the exact spatial coordinates (x, y), the major and minor elliptical axes (a, b), and the rotation angles for both the inner and outer boundaries of each generated fascicle, seamlessly importing these explicitly calculated parameters into COMSOL

to extrude the final 3D domains [40]. An important geometric parameter for the accuracy of the FEM simulation is the thickness of the perineurium (the tissue surrounding the endoneurium of each fascicle). The perineurium is an high resistive electrical barrier, and its thickness plays a dominant role in determining the neural activation threshold and the impedance value. The perineurium is able to affect the electrical field in two ways. In the transverse plane, the thicker the perineurium, the stronger the resistive barrier to the electrical current applied around the fascicle, and the less current is able to penetrate to the endoneurium. In the longitudinal plane, the thick perineurium prevents the intrafascicular current from easily leaking back out into the epineurium, and the current flows longitudinally. This confinement widens the longitudinal potential distribution, which ultimately flattens the second spatial derivative of the extracellular potential (the activating function) and thus increases the stimulation threshold [41]. Because perineurium thickness naturally increases with fascicle diameter, assigning a fixed static value to all fascicles would lead to incorrect results. Instead, a dynamic calculation determined the perineurium thickness (thk_{peri}) for each simulated fascicle based on a human nerve morphological model integrated within the pipeline. This algorithm computes the thickness as a linear function of the individual fascicle's diameter (d_{fasc}), according to the specific morphometric relationship for human peripheral nerves: $thk_{peri} = 10.50\ \mu\text{m} + 0.03702 \cdot d_{fasc}$. This dynamic scaling ensures that larger simulated fascicles correctly present a thicker, more resistive boundary.



(a) (b)

Figure 4.7: (a) The initial binary mask defining the mock cross-sectional areas and random spatial distribution of the five generated fascicles. (b) The final 2D geometric reconstruction after the application of topological constraints and physics-based circular deformation. The inner (blue) and outer (black) boundaries of each fascicle explicitly illustrate the dynamically calculated, diameter-dependent perineurium thickness before extrusion into the 3D FEM environment.

4.2.2 Nerve Modelling

After generating the 2D morphological mask, the geometry was imported into COMSOL Multiphysics for the realization of the 3D finite element model. The 2D cross-section, comprising the detailed internal anatomy of the nerve, specifically the epineurium and the individual endoneurial fascicles, was extruded linearly along the longitudinal axis (z-axis) to create the complete nerve segment with a total length of 64 mm, as illustrated in Figure 4.8. This specific longitudinal extension was strategically chosen to ensure that the electrical boundary conditions at the extremities of the model would not create artifacts and distortions of the electric field distribution in the central region of interest where the cuff electrode is placed. The external volume of the model replicates the experimental environment and physiological conditions, and it is subdivided into two concentric cylindrical media to control the subsequent meshing process and computational load. The proximal medium represents the immediate fluid layer surrounding the nerve and was set to a radius of approximately 1.73 mm. This domain was entirely enclosed within a larger distal medium, representing the bulk surrounding tissue, which featured an outer radius of 10 mm and matched the 64 mm total length of the nerve model.

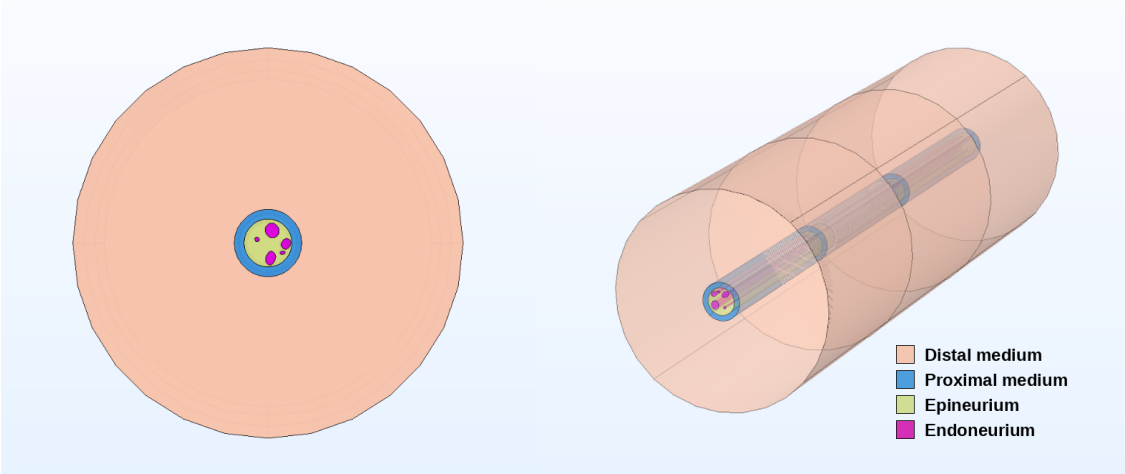


Figure 4.8: 3D Finite Element geometry constructed in COMSOL Multiphysics highlighting the extruded internal anatomy

Electrical conductivity (σ) and relative permittivity (ϵ_r) should be assigned to the different domains. Biological tissues and physiological fluids exhibit different electrical behavior depending on their structure. Domains that do not show preferential structural direction, such as physiological fluids, were modeled as electrically isotropic. On the other hand, highly organized tissues of aligned cells such as endoneurium tracts and muscles vary in resistance to current flow, thus should be modeled as anisotropic with different transverse (σ_{xy}, σ_{yy}) and longitudinal (σ_{zy})

conductivity tensors. The proximal medium is an isotropic saline solution with a conductivity of 1.76 S/m and a relative permittivity of 80, while the distal medium is considered anisotropic since skeletal muscle fibers are parallel aligned, with a transverse conductivity of 0.086 S/m, a longitudinal conductivity of 0.35 S/m and a relative permittivity of 1. Within the nerve anatomy, the endoneurium was also treated as a highly anisotropic medium. The parallel arrangement of nerve fibers within the fascicles facilitates current flow along the longitudinal axis much more readily than across the transverse plane. The endoneurial conductivity tensor was defined with a transverse conductivity of 0.167 S/m and a longitudinal conductivity of 1.0309 S/m while maintaining a relative permittivity of 1. A critical advancement in this computational model is the parameterization of the epineurium and the perineurium, according to new experimental findings of peripheral nerves of mammals. Computational models are usually based on purely resistive models of amphibian nerves. However, recent experimental observations of vagus nerves using impedance spectroscopy have revealed that the laminae of the epineurium and the perineurium govern the bioelectric impedance at the neural interface. Based on this, the epineurium was assigned a transverse conductivity of 0.0182 S/m and an extraordinary relative permittivity of 9.4×10^6. To account for longitudinal current channeling along the nerve trunk, the longitudinal conductivity of the epineurium was mathematically matched to that of the endoneurium. The perineurium was also modeled as a highly resistive and capacitive barrier with a contact impedance boundary condition at the endoneurium and epineurium junction. The perineurium was made of a conductivity (σ_{peri}) of 2.66×10^{-4} S/m and a relative permittivity of 2018 [20]. In order to adapt to the diameter dependence of the perineurial sheath thickness on different shapes of fascicles, the surface resistance (ρ_s) and surface capacitance (C_s) in the contact impedance node of COMSOL were defined as:

$$\rho_s = \frac{1}{\sigma_{peri}} \cdot \left(ci_a \cdot 2\sqrt{\frac{A_{inner}}{\pi}} + ci_b \right)$$

$$C_s = \frac{\epsilon_0 \cdot 2018}{ci_a \cdot 2\sqrt{\frac{A_{inner}}{\pi}} + ci_b}$$

In these equations, the parenthesis extracts the equivalent fascicle diameter directly from its cross-sectional area (A_{inner}), while ci_a and ci_b are the respective linear coefficients for the nerves of the human body.

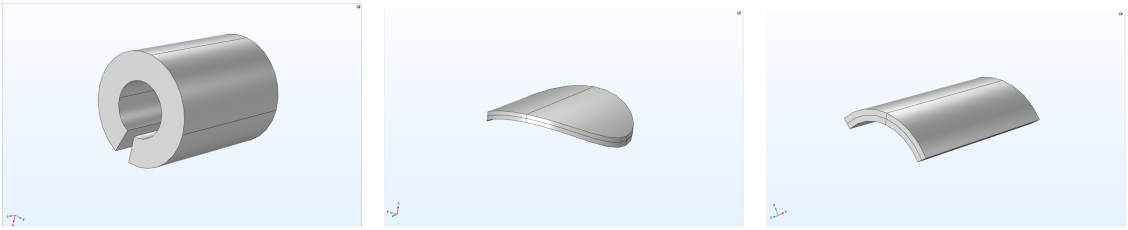
Table 4.1: Electrical properties assigned to the specific domains of the 3D finite element model.

Domain	**Material**	**Conductivity σ [S/m]**	**Relative Permittivity ϵ_r [-]**
Proximal Medium	Saline Solution	1.76	80
Distal Medium	Skeletal Muscle	$\sigma_{xx,yy} = 0.086$, $\sigma_{zz} = 0.35$	1
Endoneurium	Endoneurial Tissue	$\sigma_{xx,yy} = 0.167$, $\sigma_{zz} = 1.0309$	1
Epineurium	Epineurial Tissue	$\sigma_{xx,yy} = 0.0182$, $\sigma_{zz} = 1.0309$	9.4×10^6
Perineurium*	Perineurial Tissue	2.66×10^{-4}	2018

*Implemented dynamically as a Contact Impedance boundary condition.

4.2.3 Electrode Modelling

The custom cuff electrode was modeled using the ASCENT code by custom-assembling three distinct geometric primitives offered by the software's library. The objective was to reproduce a preliminary and simplified version of the NerveRepack electrode concept, specifically featuring only a single active disk contact, a single annular return contact, and an outer silicone cuff. As illustrated in Figure 4.9, the three specific primitives utilized for this custom assembly are the Tube Cuff Primitive, the Circle Contact Primitive, and the Ribbon Contact Primitive.

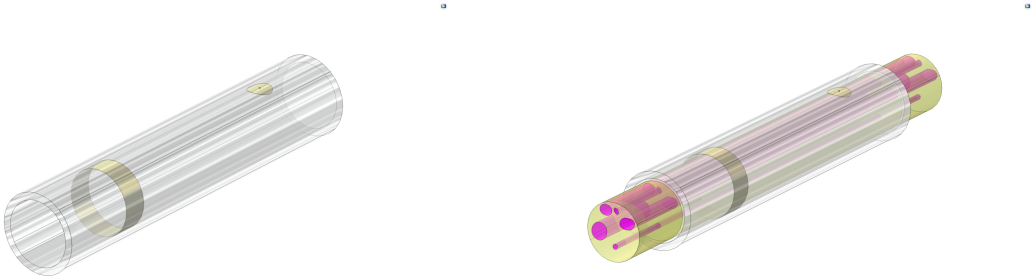


(a) Tube Cuff Primitive (b) Circle Contact Primitive (c) Ribbon Contact Primitive

Figure 4.9: Geometric primitives utilized from the ASCENT pipeline for the construction of the custom cuff electrode. **(a)** The main silicone insulating body. **(b)** The active circular disk contact. **(c)** The return annular ribbon contact.

The main insulating body of the interface was defined as a flexible cylindrical sheath with a total longitudinal length of 16 mm. To ensure a conforming fit around the nerve while deliberately accommodating a 100 μm interstitial saline gap, the inner radius was set to 1.33 mm with a wall thickness of 300 μm. A 359° radial coverage was specified to structurally mimic the surgical slit required for in vivo implantation. The active contact was developed using the Circle Contact Primitive, which modeled a flat circular disk with a 1 mm diameter and a 20 μm radial thickness. The return contact was generated via the Ribbon Contact Primitive,

forming an annular ribbon with a 1 mm longitudinal width, a 20 μm thickness, and a 355° circumferential span to provide a distributed current return path. Finally, the active disk and the return ribbon were designated as solid gold ($\sigma = 4.1 \times 10^7$ S/m) to establish highly conductive equipotential boundaries for current injection, while the surrounding Tube Cuff Primitive was parameterized as a silicone elastomer, acting as an ideal insulator with a low conductivity of 10^{-12} S/m.



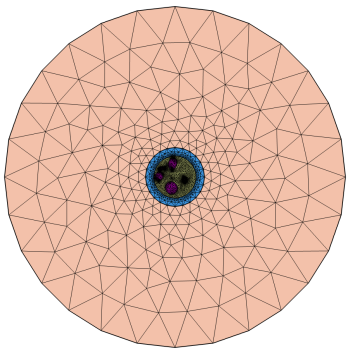
(a) Cuff Electrode (b) Complete Nerve Model

Figure 4.10: 3D finite element geometry: (a) The isolated custom neural interface, displaying the silicone insulating body, the proximal active disk contact, and the distal annular return contact. (b) The integrated assembly showing the cuff electrode positioned around the extruded median nerve, illustrating the spatial alignment between the conductive contacts and the internal fascicular anatomy.

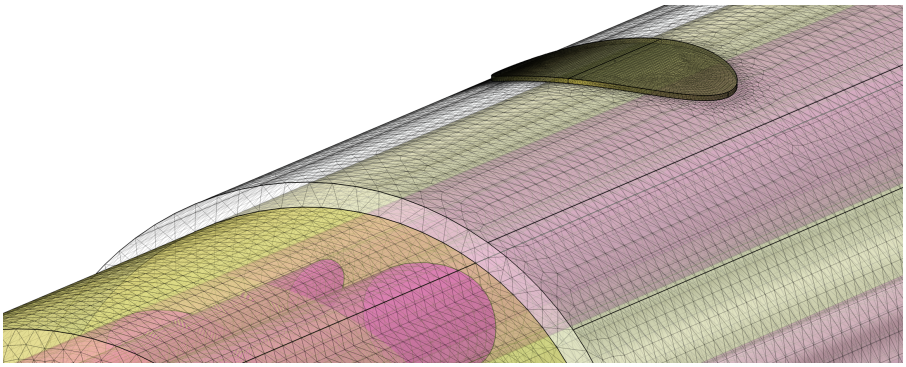
4.2.4 Meshing

Generating the mesh for the 3D finite element model presented a challenging computational task due to the high aspect ratio between the micro-scale geometric features such as the 20 μm electrode contacts and the macroscopic 64 mm total length of the nerve. The solution adopted consists of longitudinally splitting the geometry into three equal portions: a central region containing the cuff electrode and two lateral extremities. The mesh process followed a hierarchical sequence, applying high-resolution grids to central structures and progressively coarsening the elements outward to optimize computational load. First, a custom *Swept* mesh was applied to the central segment of the nerve trunk. The element size was set with a maximum of 100 μm, a minimum of 10 μm, and a curvature factor of 0.2 to maintain high geometric resolution along the curved boundaries of the fascicles. Around the nerve, the parts of the asymmetrical cuff electrode and the 100 µm interstitial saline gap were discretized using an "Extremely fine" *Free Tetrahedral* mesh with a curvature factor of 0.2 to account for the thin active contacts and the small electric field gradients near the current source. Moving radially outward within the central zone, the extracellular media were meshed with progressively decreasing density.

The proximal medium was discretized with an "Extra fine" *Free Tetrahedral* grid, acting as a spatial transition zone, while the massive distal muscle medium was assigned a "Coarse" *Free Tetrahedral* mesh, exploiting the homogeneous diffusion of the electric field far from the electrode. The two lateral extremities covering the rest of the 64 mm longitudinal extension were meshed using a second Swept design made with hexahedral-dominant elements. This final step linearly extruded the 2D cross-section mesh from the central region out along the z-axis in order to reduce the number of elements and keep the electrical boundary condition integrity at the extremities of the model.



(a) Cross-sectional mesh (XY plane)



(b) Detailed 3D mesh at the contact

Figure 4.11: Finite element mesh details: (a) Macroscopic view illustrating the radial meshing strategy, where the element size progressively coarsens from the highly resolved central nerve region outward to the "Coarse" tetrahedral grid of the distal muscle medium. (b) High-resolution close-up of the central region. The 20 μm thick active disk and the 100 μm interstitial saline gap are discretized with an "Extremely fine" free tetrahedral mesh, while the underlying epineurium and endoneurial fascicles feature a custom structured swept mesh.

The overall geometric integrity of the computational domain and the effectiveness of the hierarchical meshing strategy were visually and quantitatively validated

using the Skewness metric. The complete spatial discretization resulted in a total of 2,629,725 domain elements, strategically comprising 1,935,357 tetrahedral elements highly localized around the complex central cuff electrode and interstitial saline gap, which seamlessly transition into 657,072 prismatic elements generated by longitudinal sweeping operations along the distal nerve extremities. This configuration yielded an average element quality of 0.6911, safely above the standard 0.6 threshold indicative of a numerically stable mesh in finite element modeling. The detailed element quality histogram displays a pronounced right-skewed distribution with the highest concentration of elements peaking between 0.8 and 0.9 on the Skewness scale (Figure 4.12). The negligible count of highly distorted elements confirms that lower-quality geometries are statistically marginal and strictly confined to unavoidable sharp structural transitions, such as the interface between the 20 μm metallic contacts and the surrounding bulk media. This controlled spatial distribution prevents numerical singularities and guarantees the stable convergence of the volume conduction solver.

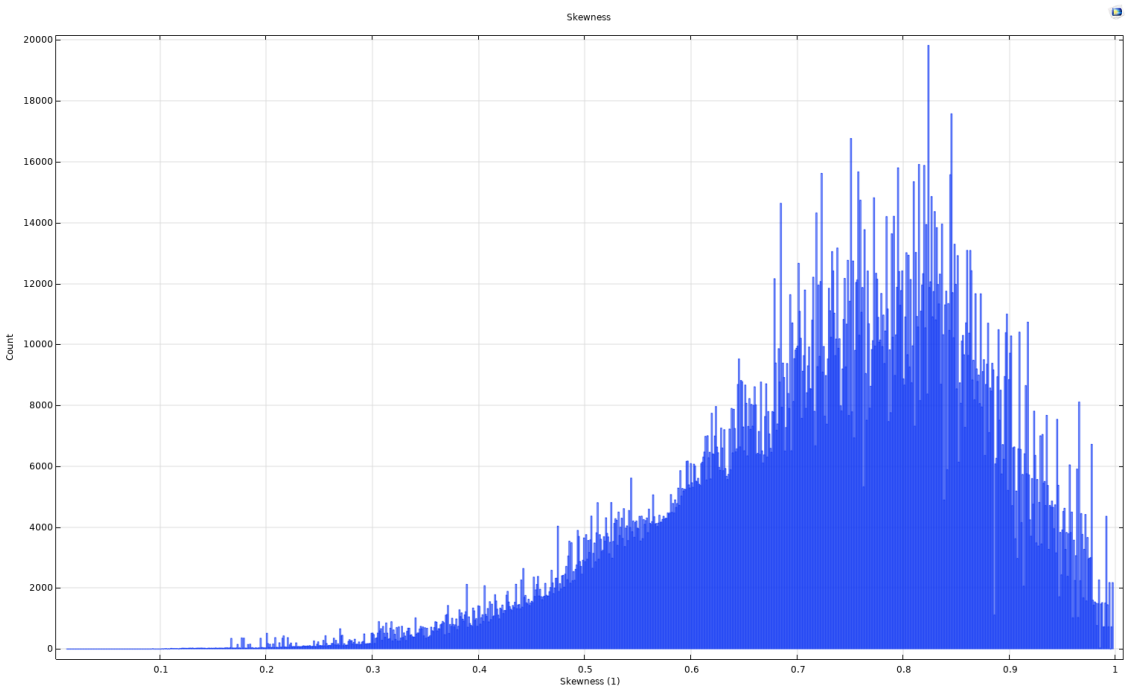


Figure 4.12: Element quality histogram based on the Skewness metric for the complete 3D finite element model.

4.2.5 Physics and Studies

The governing equations implemented within the *Electric Currents* (EC) interface of COMSOL Multiphysics were explicitly formulated in the frequency domain to account for the dielectric properties of the biological tissues and to evaluate the

macroscopic electrical impedance profile of the nerve as a function of frequency. The total current density $\mathbf{J}$ was defined as the linear combination of the conduction current, the displacement current, and an externally generated current density $\mathbf{J}_e$:

$$\mathbf{J} = \sigma\mathbf{E} + j\omega\mathbf{D} + \mathbf{J}_e$$

where σ is the electrical conductivity tensor, $\mathbf{E}$ is the electric field vector, ω is the angular frequency of the applied signal, and $\mathbf{D}$ is the electric displacement field. The fundamental relationship between the electric field and the scalar electric potential V is:

$$\mathbf{E} = -\nabla V$$

and all computational domains follow the continuity equation:

$$\nabla \cdot \mathbf{J} = Q_{j,v}$$

where $Q_{j,v}$ represents the volumetric current source. The constitutive relations for the conduction ($\mathbf{J}_c = \sigma\mathbf{E}$) and dielectric ($\mathbf{D} = \epsilon_0\epsilon_r\mathbf{E}$) models were dynamically linked to the explicitly defined material properties. This direct integration ensures that the complex, anisotropic conductivity and permittivity matrices assigned to the endoneurial fascicles and the bulk epineurium mathematically guide the spatial distribution of the electric field. The discretization order for the electric potential dependent variable was set to use linear shape functions rather than the software's default quadratic elements: with over 2.6 million elements, quadratic discretizations would have significantly increased the degrees of freedom, exceeding available memory resources. By using a linear discretization, the computational load remained manageable for the available system. The active simulation was modeled by setting the central active disk of the cuff electrode as a terminal current source of a sinusoidal wave with a peak amplitude of $I_0 = 1$ mA across all evaluated frequencies. Instead, the return ring is fixed to $V = 0$ V to simulate the system ground and close the electrical circuit. The external boundaries of the macroscopic model, including the outer surfaces of the surrounding muscle medium and the transverse sections at the longitudinal extremities of the nerve, were set to Electrical Insulation ($\mathbf{n} \cdot \mathbf{J} = 0$). These conditions ensures that no current flows outside the defined computational domain, confining the electric field entirely within the modeled tissues. The study performed was a frequency sweep over 1 Hz to 1 MHz ($10^0 - 10^6$ Hz) using a logarithmic step of 0.1 decades ($10\hat{}range(0,0.1,6)$), where a sinusoidal current with a peak amplitude of 1 mA was injected at each discrete frequency step. Solving this computational model fundamentally yields the 3D spatial distribution of the electric potential across the entire simulated volume. Then, the *Store in Output* setting was specifically restricted to the active disk to focus exclusively on the contact interface and extract the impedance seen by the electrode at each computed frequency. Focusing on the 1 kHz frequency, the electric potential distribution (Figure 4.13) clearly highlights the dispersive behavior of the

different connective tissue laminae. The perineurium still exhibits a relatively high resistive component since the signal frequency is lower than the corner frequency of the perineurium (2.6 kHz ± 1.0 kHz) and, as a consequence, the capacitive effect is not sufficient to short-circuit the membrane. The epineurium, which presents a corner frequency of 368.5 Hz, shows a lower potential. In fact, this tissue has already surpassed its purely resistive behavior, allowing the current to propagate more easily within the macroscopic volume outside the fascicles. Moreover, the color distribution suggests the effect of morphology in spatial modulation: larger fascicles have a thicker perineurium, presenting a higher resistance. Smaller fascicles, on the contrary, have a thinner perineurium in proportion to their diameter, offering lower transverse resistance and registering a higher internal endoneurial potential for the same stimulation level.

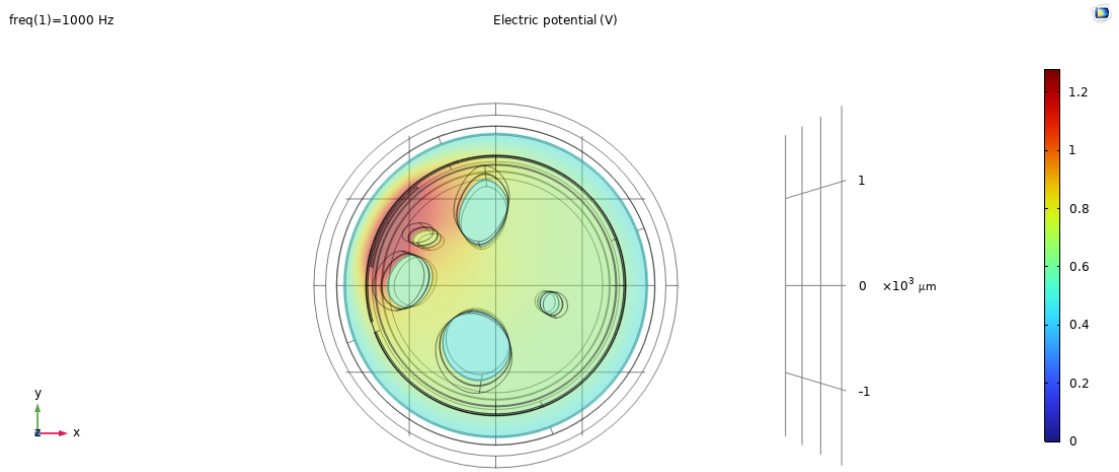


Figure 4.13: Cross-sectional (xy-plane) electric potential distribution within the multi-fascicular nerve model at a stimulation frequency of 1 kHz.

From a longitudinal point of view (Figure 4.14), the potential reaches its maximum at the active injection contact and drops to 0 V at the grounded return ring. However, other values of potential different from zero are observable at the longitudinal extremities of the modeled nerve. This distribution profile is a direct consequence of the realistic incorporation of a 100 µm conductive fluid film (saline gap) between the silicone cuff and the nerve surface. Because of this conductive interface, a fraction of the injected current is not strictly confined by the cuff, but finds alternative lower-resistance ways to flow through the surrounding macroscopic medium before re-entering the nerve at distal zones and close to the ring ground electrode.

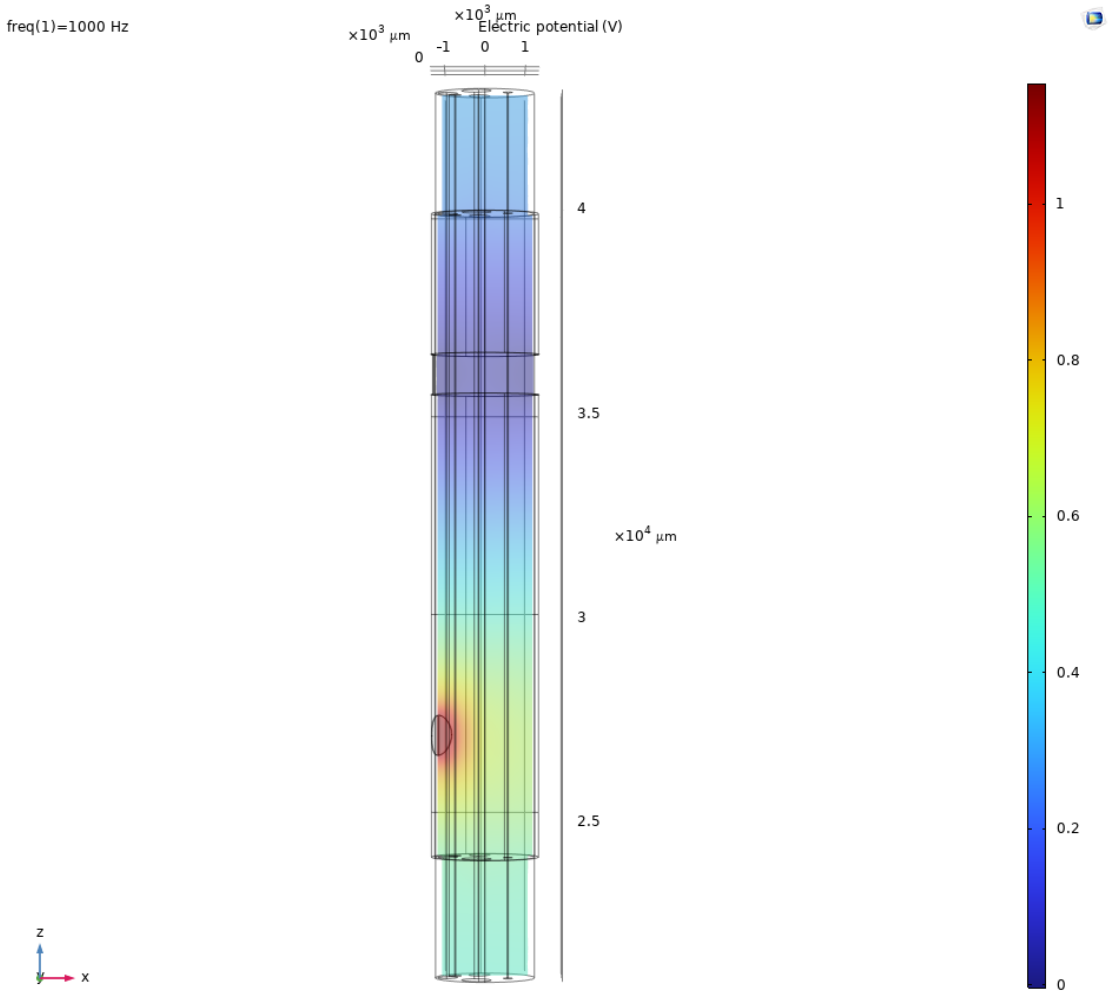


Figure 4.14: Longitudinal cross-section (zx-plane) illustrating the electric potential distribution along the nerve model at a stimulation frequency of 1 kHz.

The complex impedance data evaluated at the active electrode contact were extracted from COMSOL Multiphysics and processed in MATLAB to construct the Bode plot (Figure 4.15). This diagram characterizes the frequency-dependent macroscopic impedance of the nerve-electrode interface, linking the curve profiles directly to the dispersive properties of the tissues. At frequencies up to 100 Hz, the cellular membranes block the current, and the anatomical structures behave as purely resistive barriers. At exactly 100 Hz, the impedance magnitude remains high at 1908.59 Ω, while the phase begins a slight downward shift to −9.38°. This initial deviation reflects the capacitive effect of the epineurium beginning to short-circuit its structural resistance, allowing current to flow more easily into the outer connective matrix. The most prominent variation occurs between 1 kHz and 10 kHz,

corresponding to the capacitive unlocking of the perineurium. At 1 kHz, the magnitude drops to 1280.13 Ω with a phase of −25.96°. This value falls well within the acceptable operational range of commercial cuff-electrode devices (600 Ω – 5300 Ω) [42]. As the frequency reaches 10 kHz, the magnitude exhibits a steep roll-off down to 235.7 Ω, and the phase reaches its minimum negative peak at −56.55°. As this primary resistive shield is fully short-circuited, the injected current bypasses the barrier and floods the highly conductive endoneurial fascicles, causing the overall impedance to drop sharply. Above 100 kHz, the magnitude plateaus at a low baseline value and the phase returns toward 0°. At this stage, all biological capacitive barriers are fully short-circuited. The entire nerve-electrode system behaves once again as a pure resistor, governed solely by the bulk ohmic conductivity of the intra- and extracellular fluids.

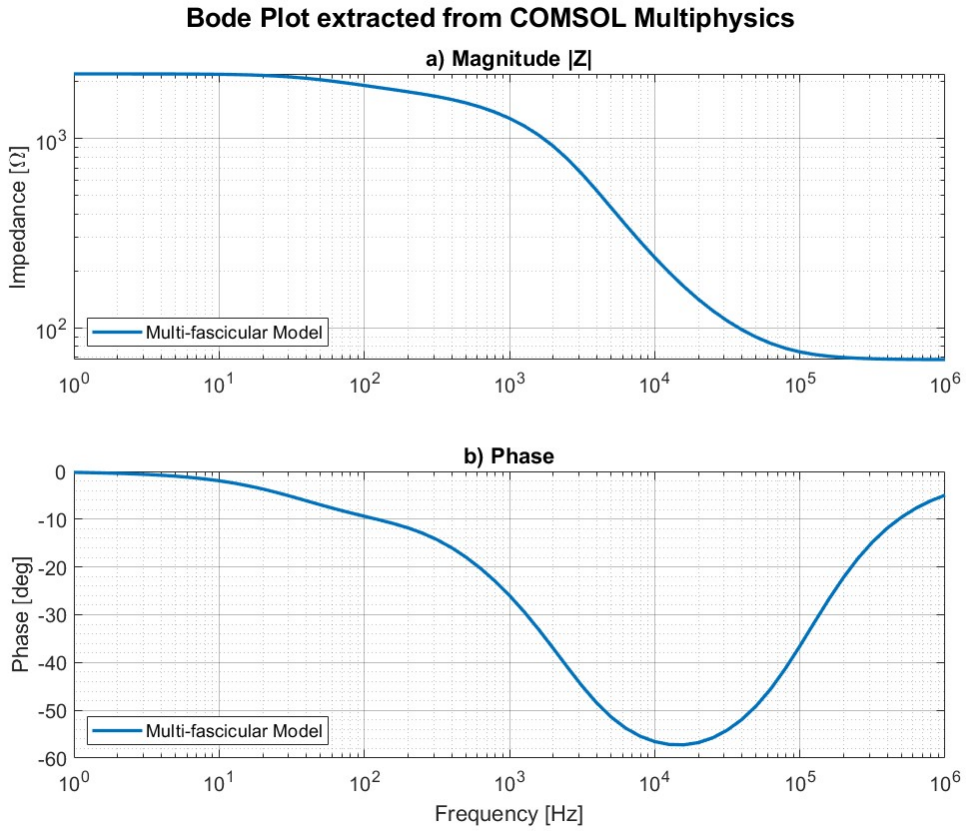


Figure 4.15: Bode plot characterizing the frequency-dependent macroscopic impedance of the nerve-electrode interface, evaluated at the active contact. (a) Impedance magnitude ($|Z|$) illustrating the transition from a highly resistive low-frequency state to a low-resistance high-frequency plateau. The steep roll-off between 1 kHz and 10 kHz reflects the short-circuiting of the tissue barriers. (b) Phase angle highlighting the capacitive behavior of the biological membranes. The initial descent indicates the capacitive effect of the epineurium, while the prominent negative peak corresponds to the capacitive unlocking of the perineurial shield.

4.2.6 Lumped Parameters Circuit

After extracting the Bode plot from the FEM analysis, the objective was to develop an equivalent RC circuit that accurately replicates the simulated frequency response. An additional FEM simulation was conducted using a simplified model. This new setup maintained the same electrical boundary conditions but featured a single endoneurial fascicle (Figure 4.16). The simplified geometry enabled the derivation of mathematical relationships, directly linking the anatomical dimensions of the model to precise resistor and capacitor values.



Figure 4.16: 3D geometry of the simplified mono-fascicular nerve model, featuring a single centered fascicle and the surrounding cuff electrode, used to derive the analytical RC circuit parameters.

The frequency response of the simplified mono-fascicular model was extracted as a Bode plot and compared with the main multi-fascicular model (Figure 4.17). The direct comparison confirms the validity of the geometric approximation. The mono-fascicular model reproduces the dispersive dynamics of the complete anatomical nerve. Both geometries exhibit the three fundamental physical regimes including the resistive plateau at low frequencies, the steep capacitive roll-off in the central band, and the pure ohmic stabilization at high frequencies. A slight overestimation of the impedance occurs in the transition band between 10^2 Hz and 10^4 Hz. This occurs because grouping the entire endoneurial volume into a single macro-fascicle alters the perineurial volume-to-surface ratio. This anatomical simplification also reduces the interstitial epineurial current pathways compared to a fragmented architecture. The magnitude maintains a maximum relative percentage error of 10.06% (Figure 4.18a). This error rate is acceptable given the drastic geometric reduction. The phase curves show a solid match between the two models and the point of maximum capacitive behavior maintains the same depth. A minor shift of this peak toward higher frequencies occurs in the simplified model. This translation generates a maximum absolute phase difference of 6.12° at high frequencies (Figure 4.18b). The shift indicates a small variation in the equivalent time constant of the system deriving from the different spatial distribution of the resistive barriers.The maximum recorded errors remain minimal across the evaluated spectrum and the overall stability of the frequency response validates the mono-fascicular geometry as a robust analytical tool.

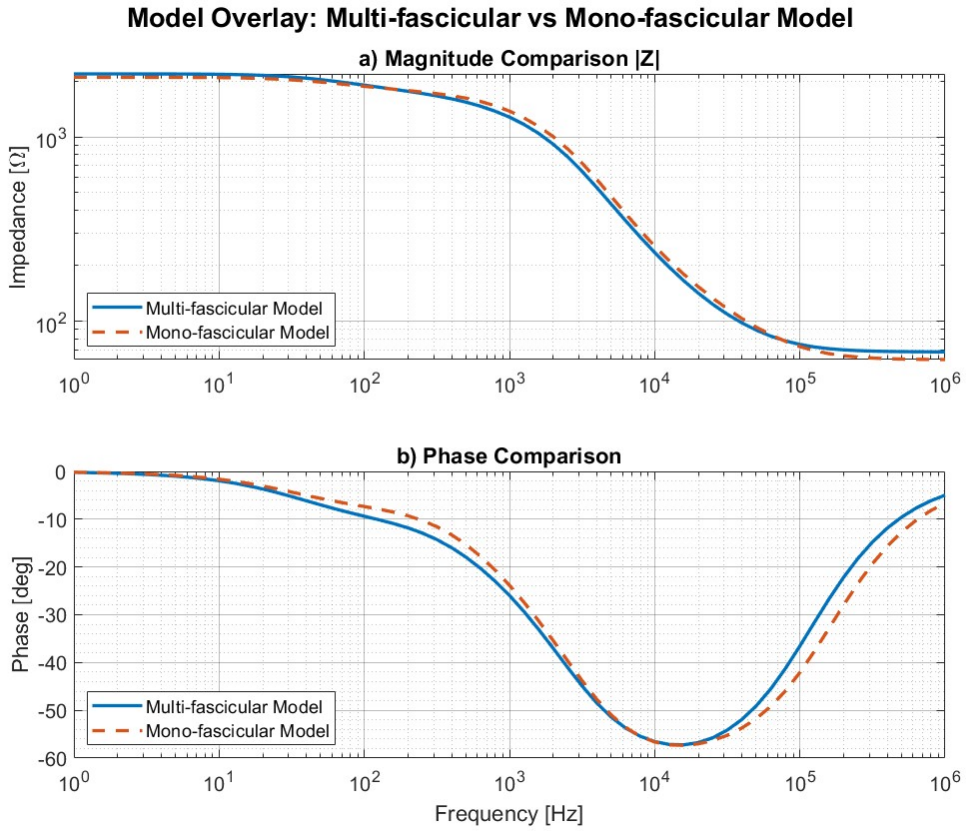


Figure 4.17: Bode plot comparison between the complete multi-fascicular nerve model and the simplified mono-fascicular model. (a) Impedance magnitude comparison and (b) phase response. The curves demonstrate a strong overall agreement between the two geometric models across the evaluated frequency spectrum.

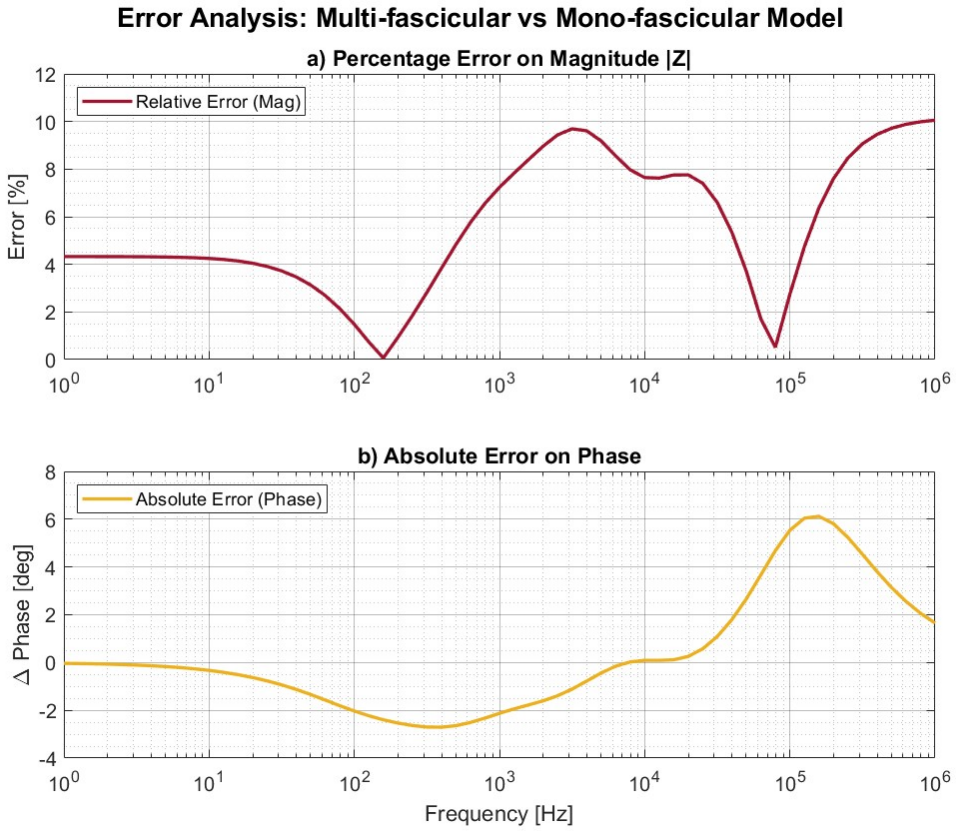


Figure 4.18: Error analysis quantifying the deviations between the mono-fascicular and multi-fascicular models. (a) Relative percentage error for the impedance magnitude and (b) absolute phase difference in degrees. The maximum recorded variations (10.06% for the magnitude and 6.12° for the phase) confirm the validity of the simplified geometric approximation.

The simplified mono-fascicular model was decomposed into independent transverse and longitudinal electrical pathways. Anatomical layers and interfaces were translated into equivalent lumped parameters based on their geometric dimensions and material properties. In the transverse direction (Figure 4.19a), the tissues and the surrounding fluid act as parallel RC circuits. The perineurium, epineurium, and saline gap are represented by parallel resistor-capacitor pairs (denoted with the subscript 't'). The transverse electrical contribution of the endoneurium is negligible and was excluded from this network. The parameter values for these cylindrical shells derive from standard coaxial cable equations:

$$R_t = \frac{\rho}{2\pi L} \ln\left(\frac{r_{out}}{r_{in}}\right)$$

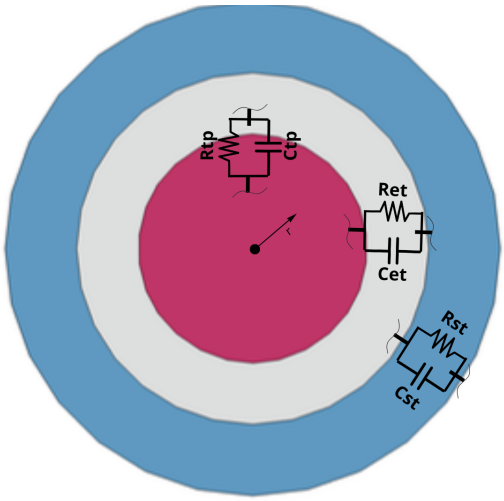
$$C_t = \frac{2\pi\varepsilon_0\varepsilon_r L}{\ln\left(r_{out}/r_{in}\right)}$$

The variables in these equations represent specific physical and geometric properties of each anatomical layer. The parameter ρ is the electrical resistivity of the tissue. The terms ε_0 and ε_r represent the vacuum permittivity and the relative permittivity of the specific material, respectively. The geometric dimensions include the length of the modeled segment L, along with the inner radius r_{in} and the outer radius r_{out} of each cylindrical shell. The longitudinal direction requires a different set of electrical approximations based on the FEM boundary conditions and physical tissue behavior (Figure 4.19b). The perineurium is omitted from the longitudinal network because the numerical model defines it strictly as a 2D boundary contact impedance. The endoneurium and the saline gap act primarily as conductive channels along the z-axis. Their longitudinal capacitive effects are negligible, reducing their representation to pure series resistors (R_e and R_{sl}). The epineurium retains a parallel RC structure (R_{el} and C_{el}) due to its specific dielectric properties. The longitudinal lumped parameters are calculated using standard uniform cylinder equations:

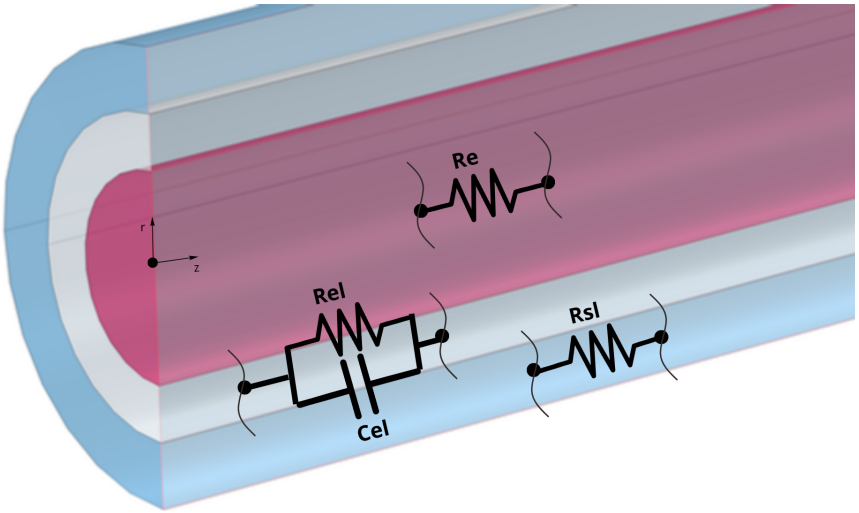
$$R_l = \rho\frac{L}{A}$$

$$C_l = \varepsilon_0\varepsilon_r\frac{A}{L}$$

In these formulas, A represents the transverse cross-sectional area of the specific anatomical layer. The length L and the material properties (ρ, ε_0, ε_r) retain the same physical meaning as in the transverse calculations. This mathematical approach directly links the 3D geometry of the nerve to the 1D electrical components of the equivalent circuit.



(a) Transverse lumped parameters



(b) Longitudinal lumped parameters

Figure 4.19: Spatial mapping of the lumped parameters over the simplified mono-fascicular model. **(a)** In the transverse direction, the perineurium (R_{tp}, C_{tp}), epineurium (R_{et}, C_{et}), and saline gap (R_{st}, C_{st}) are defined as parallel RC pairs, while the endoneurium contribution is considered negligible. **(b)** In the longitudinal direction, the endoneurium (R_e) and saline gap (R_{sl}) act as pure series resistors. The epineurium retains a parallel RC structure (R_{el}, C_{el}), and the perineurium is excluded from this axis.

The mono-fascicular model was longitudinally divided into five distinct sections. The central section spans 9 mm, representing the distance between the active disc

electrode and the return ring electrode. Two intermediate sections extend from the electrodes to the edges of the silicone cuff: a 3 mm segment on the left and a 4 mm segment on the right. Two distal extremities flank the cuffed region, each measuring 24 mm in length. Lumped resistor and capacitor values were calculated for each specific section using the previously defined analytical formulas. The resulting network topology governs the current distribution pathways (Figure 4.20). Current entering the system first encounters the transverse saline gap (R_{st}, C_{st}). At this node, the current divides. A fraction shunts longitudinally through the highly conductive fluid (R_{sl}), while the remainder penetrates transversely into the epineurium (R_{et}, C_{et}). Inside the epineurium, a second branching occurs. The current either flows longitudinally along the epineurial tissue (R_{el}, C_{el}) or crosses the highly resistive perineurial barrier (R_{pt}, C_{pt}). Current crossing the perineurium reaches the target endoneurium, propagating strictly along the longitudinal axis (R_e).

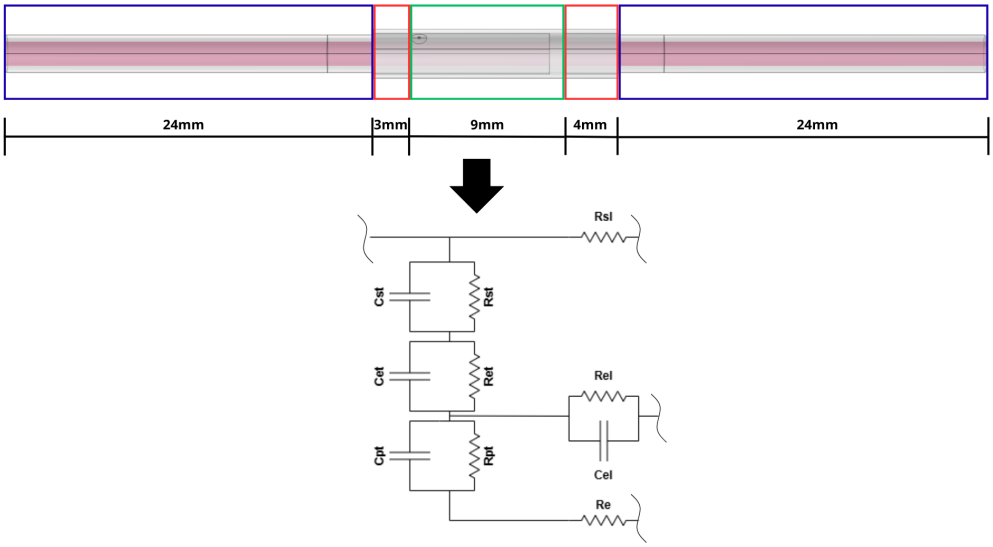


Figure 4.20: Longitudinal segmentation of the mono-fascicular model and the equivalent circuit topology for a single section. The 3D geometry is divided into a 9 mm central active region, two intermediate intra-cuff segments (3 mm and 4 mm), and two 24 mm distal extremities. The schematic illustrates the localized electrical network, highlighting the anatomical competition between transverse tissue penetration (RC parallel blocks) and longitudinal current shunting (series components).

By integrating the five distinct longitudinal sections, the complete global equivalent circuit of the experimental setup was assembled. All lumped resistance and capacitance values for each anatomical layer and fluid domain were rigorously calculated using the previously defined analytical equations, based on their specific physical properties and geometric dimensions. The resulting full network topology,

implemented for the final computational analysis, is illustrated in Figure 4.21. In addition to the anatomical nerve layers, external resistive components were integrated into the global network topology (Table 4.3) to properly mimic the complete experimental setup. The electrode access resistance (R_{acc}) was calculated as 72 Ω. This value represents the transverse resistance of a cylindrical fluid volume with a height of 100 μm and a radius of 0.5 mm, simulating the immediate electrode-tissue interface. Furthermore, the extraneural skeletal muscle surrounding the experimental setup was modeled using a resistor (R_m). This parallel resistor account for the alternative current pathway located outside the boundaries of the insulating silicone cuff.

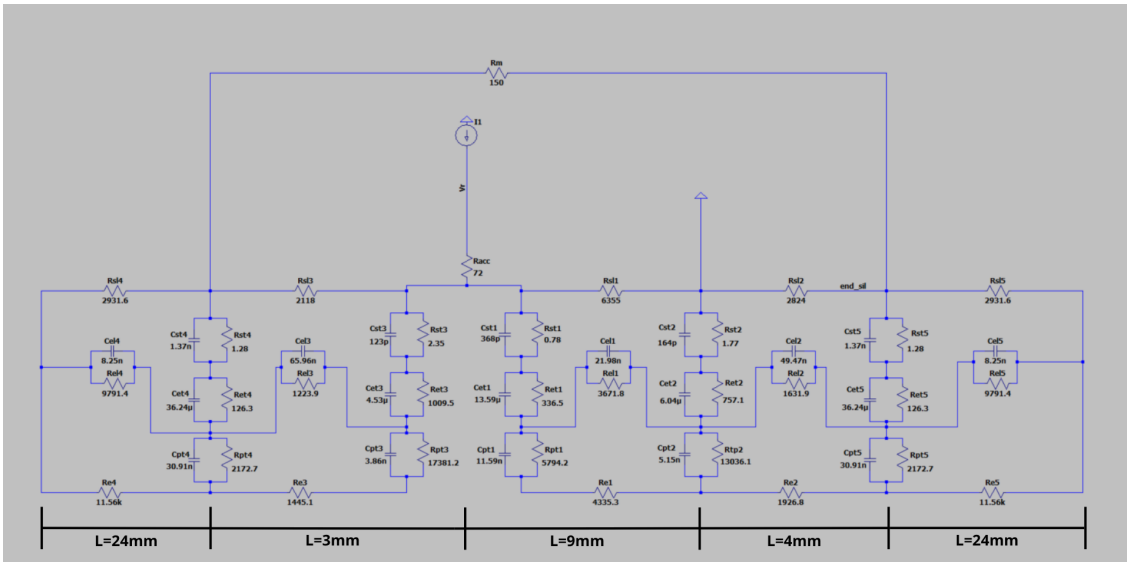


Figure 4.21: Complete global equivalent circuit of the cuffed mono-fascicular nerve model. The schematic integrates the five longitudinal sections ($L = 24, 3, 9, 4, 24$ mm) with their explicitly calculated lumped parameters.

Table 4.2: Calculated lumped parameters for each longitudinal section of the equivalent circuit.

Component	**Left Distal** ($L = 24$ **mm**)	**Left Intra-cuff** ($L = 3$ **mm**)	**Central** ($L = 9$ **mm**)	**Right Intra-cuff** ($L = 4$ **mm**)	**Right Distal** ($L = 24$ **mm**)
R_e	11.56 kΩ	1445.1 Ω	4335.3 Ω	1926.8 Ω	11.56 kΩ
R_{pt}	2172.7 Ω	17381.2 Ω	5794.2 Ω	13036.1 Ω	2172.7 Ω
C_{pt}	30.91 nF	3.86 nF	11.59 nF	5.15 nF	30.91 nF
R_{et}	126.3 Ω	1009.5 Ω	336.5 Ω	757.1 Ω	126.3 Ω
C_{et}	36.24 μF	4.53 μF	13.59 μF	6.04 μF	36.24 μF
R_{st}	1.28 Ω	2.35 Ω	0.78 Ω	1.77 Ω	1.28 Ω
C_{st}	1.37 nF	123 pF	368 pF	164 pF	1.37 nF
R_{el}	9791.4 Ω	1223.9 Ω	3671.8 Ω	1631.9 Ω	9791.4 Ω
C_{el}	8.25 nF	65.96 nF	21.98 nF	49.47 nF	8.25 nF
R_{sl}	2931.6 Ω	2118 Ω	6355 Ω	2824 Ω	2931.6 Ω

Table 4.3: External environment and electrode access resistance parameters.

Parameter	**Description**	**Value (Ω)**
R_{acc}	Electrode access resistance	72
R_m	Central extraneural skeletal muscle	150

For the internal nerve tissues, the parameter variations strictly follow the analytical cylinder equations. The longitudinal resistances (R_e, R_{el}) scale directly with L. A longer anatomical section presents a longer pathway for the charge carriers, linearly increasing the longitudinal resistance. The longitudinal capacitance (C_{el}) is inversely proportional to L. In the transverse direction, the geometric relationship inverts. Transverse resistances (R_{pt}, R_{et}) scale inversely with L. A longer nerve segment offers a larger cylindrical surface area for the current to cross, thereby lowering the overall transverse tissue resistance. Conversely, transverse capacitances (C_{pt}, C_{et}) scale directly with length, reflecting the larger biological membrane area available for charge accumulation.The saline gap parameters (R_{sl}, R_{st}, C_{st}) exhibit a unique behavior between the intra-cuff and distal sections. This deviation highlights the physical impact of the insulating silicone cuff. Inside the cuff ($L = 3$ mm, 4 mm, 9 mm), the saline volume is severely constrained between the epineurium and the internal cuff wall. This restricted cross-sectional area yields a high longitudinal resistance (R_{sl}). Outside the cuff in the distal regions ($L = 24$ mm), the extraneural domain expands significantly into the surrounding bulk fluid. This massive increase in the conductive cross-sectional area drastically lowers the distal R_{sl} value (2931.6 Ω), despite the section being geometrically much longer than the central region (6355 Ω for 9 mm).These parametric variations dictate the bioelectrical current steering during stimulation. The highly resistive, restricted saline gap inside the cuff prevents the current from easily shunting along the nerve surface. This

geometric constraint forces the electrical field to penetrate transversely through the epineurial and perineurial barriers. Once the current reaches the distal extremities beyond the cuff edges, the sudden drop in external longitudinal resistance creates a massive low-impedance shunt. The current naturally diverges outward into the bulk fluid, causing a rapid decay of the effective electric field that reaches the distal endoneurial targets. A frequency sweep simulation of the lumped parameter circuit was performed in LTspice and its global complex impedance was extracted. The Bode plot was then overlaid onto the COMSOL data to compare the magnitude and phase response (Figure 4.22). The relative percentage error of the impedance and the absolute angular deviation for the phase were calculated at each frequency point to evidence the difference between the two models (Figure 4.23). In the low-frequency resistive plateau (10 Hz to 100 Hz), the LTspice model underestimates impedance magnitude, showing a relative error from -31.06% to -38.08%. In the mid-frequency capacitive transition (1 kHz to 10 kHz), the magnitude error crosses the zero axis and moves to a positive overestimation of +37.11% at 10 kHz. The peak relative error is in the high-frequency range at +51.57% at 100 kHz. The absolute phase deviation remains minimal at low frequencies: -1.59° at 10 Hz and -1.10° at 100 Hz. During the capacitive transition, the absolute deviation increases to +7.08° at 1 kHz, drops to +3.57° at the 10 kHz phase peak, and reaches its maximum divergence of +12.48° at 100 kHz. Both models converge back to a 0° phase shift at 1 MHz. The observed deviations reflect the problem of discretizing a continuous volume into five sections. The 1D network forces current to follow separate paths, resulting in a baseline resistive offset at low frequencies and altering the exact RC attenuation slope in the high-frequency band. Despite the absolute numerical offsets, the 1D network replicates the correct dynamic trends across the frequency spectrum, captures the global electrical signature of the FEM model, and maintains the structural transitions between the resistive plateaus and the capacitive phase peak.

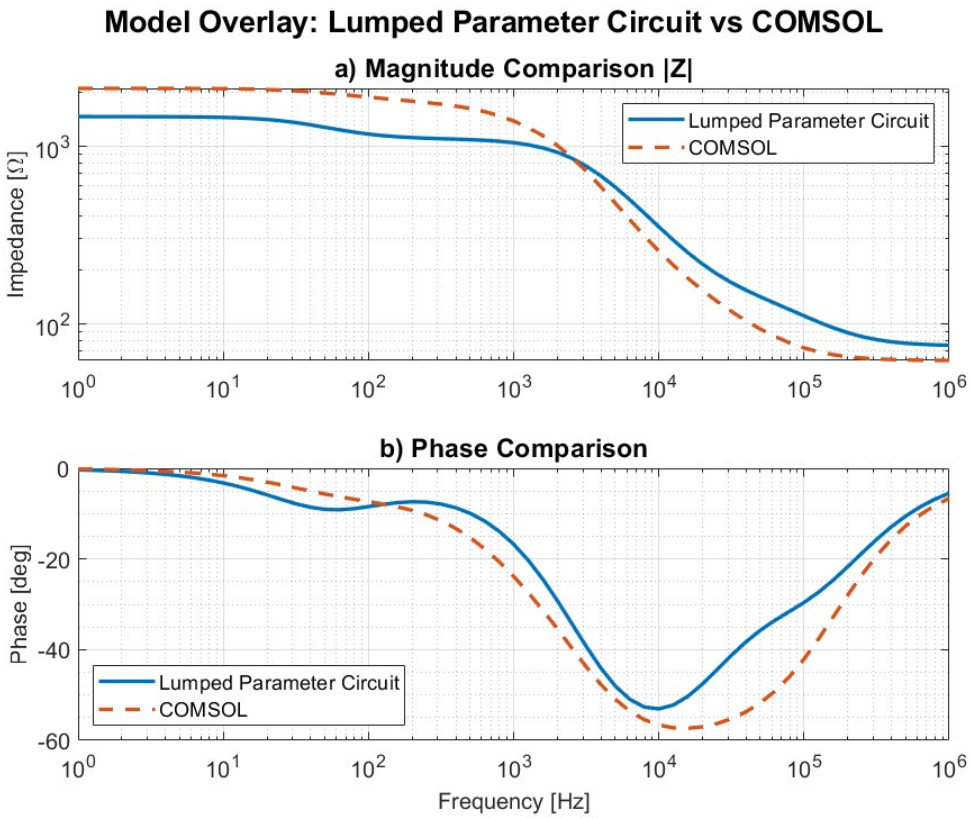


Figure 4.22: Bode plot overlay comparing the impedance of the lumped parameter circuit (blue line) with the 3D COMSOL FEM model (dashed red line). (a) The magnitude response $|Z|$ shows the alignment at high frequencies and a baseline resistive offset at low frequencies (b) The phase response shows the mid-frequency capacitive transition and the peak phase shift around 10 kHz.

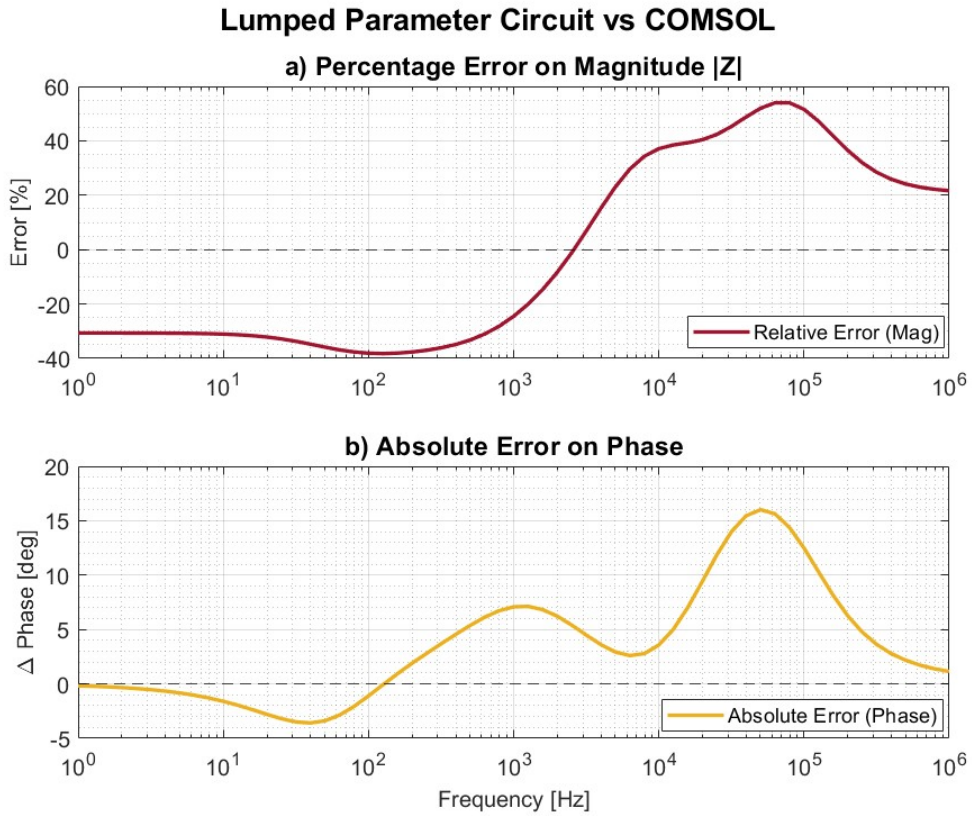


Figure 4.23: Error in frequency-dependent variation between the lumped parameter circuit and 3D FEM model. (a) Percentage relative error on the impedance magnitude $|Z|$, illustrating a low-frequency underestimation plateau and a localized overestimation peak in the high-frequency band. (b) Absolute error on the phase response in degrees, highlighting the bounded angular discrepancies across the resistive and capacitive structural transitions.

A spectral analysis evaluated the equivalent circuit under the exact operational parameters established for median nerve stimulation. As discussed in the state-of-the-art, the reference protocol employs a biphasic current waveform featuring a 100 μs active phase, a 150 μs inter-phase delay, and a 24 Hz repetition rate. To correlate the frequency-dependent modeling errors (Figure4.23) with the actual forcing term applied to the system, the spectral distribution of the stimulation signal was quantified. Power Spectral Density (PSD) was computed through MATLAB using the periodogram method,and the fractional normalized signal power across targeted frequency bands was calculated through numerical integration of the PSD. The integration reveals that frequencies below 100 Hz contain only 0.01% of the total stimulus signal power. Similarly, the high-frequency tail extending above 10 kHz

carries 9.67% of the total signal energy. Because these boundary regions lack significant harmonic content, the pronounced magnitude errors recorded at the spectrum edges, namely the 38% underestimation at 100 Hz and the 37% overestimation at 10 kHz, exert a negligible impact on the overall stimulation dynamics and charge balancing process. The vast majority of the stimulus energy, totaling 90.32%, concentrates within the main operative band spanning from 100 Hz to 10 kHz. To define the accuracy of the model during the most critical spectral phase, a targeted zoom isolates the core energetic lobe between 600 Hz and 5 kHz. This specific window contains 70.74% of the localized signal power. Within this critical band, the magnitude deviation crosses zero at 2.5 kHz. Although magnitude offsets persist at the outer boundaries of this 600 Hz to 5 kHz core band, the absolute phase error remains strictly bounded below 7.1 degrees. In linear systems, this minimal phase shift ensures that the magnitude discrepancy acts solely as a static amplitude scaling factor. Consequently, the circuit preserves the exact temporal morphology of the biphasic current pulse without inducing structural distortion, maintaining high simulation fidelity exactly where the stimulus concentrates its maximum spectral energy. For a clear graphical representation of the stimulation dynamics, Figure 4.24 displays the amplitude spectrum of the current pulse derived via FFT. This plot allows for a direct visual appreciation of how the injected harmonic current distributes across the frequency range. By overlaying the current spectrum with the tissue impedance profiles, the graphical analysis visually confirms the numerical PSD results: the bulk of the stimulus amplitude is injected precisely into the frequency band where the simplified circuit better approximates the 3D COMSOL model.

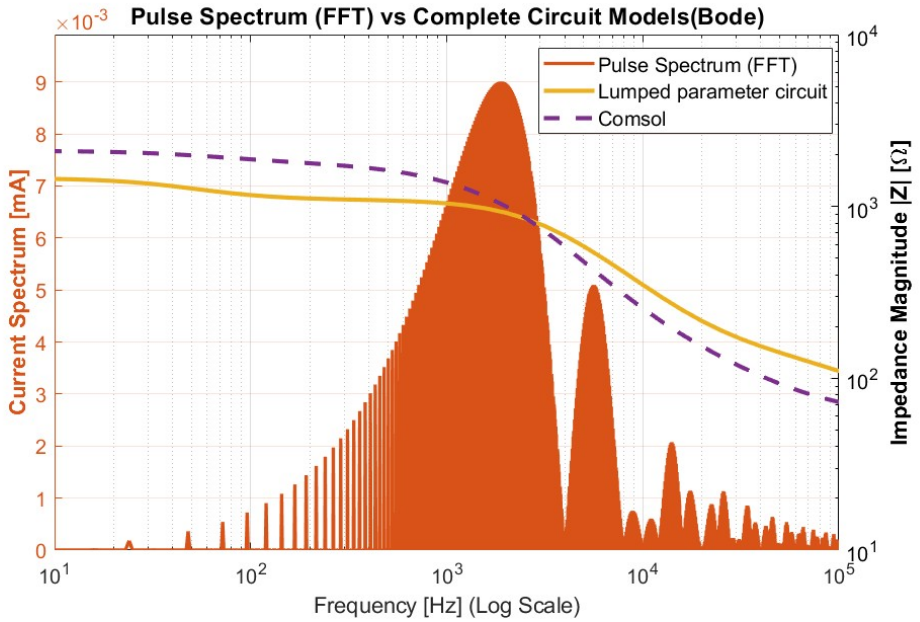


Figure 4.24: Spectral overlay of the stimulus amplitude and tissue impedance magnitude. The left axis displays the amplitude spectrum of the 100 μs biphasic current pulse (solid area, mA) extracted via Fast Fourier Transform (FFT). The right axis reports the frequency-dependent impedance magnitude (Ω) for both the 3D COMSOL model (dashed line) and the lumped-parameter equivalent circuit (solid line). This dual-axis visualization demonstrates that the primary harmonic current is injected directly into the mid-frequency band where the simplified circuit optimally tracks the 3D model, while the high-error peripheral regions remain devoid of significant stimulation current.

The first five section circuit was reduced to a three section network for practical hardware implementation without modifying the impedance load in a relevant way (Figure 4.25). The left and right 24 mm distal extremities were removed from the circuit since the main electrical load is inside the silicone cuff. Outside the cuff edges, the saline fluid expands into a large volume and creates a low-resistance path. The electrical potential in this wide area becomes uniform, and the voltage gradient decreases to near zero. Without a voltage gradient, no electrical current flows through these distant tissues. Since parallel circuit branches with zero current do not affect the total input impedance, their removal simplifies the hardware model and the electrical behavior remains unchanged. The transverse saline (R_{st}, C_{st}) components of the circuit were also excluded in all sections. The value of the resistance R_{st} ranges between 0.78 and 2.35 Ω, while the epineurial and perineurial barrier resistances are 300 and 5000 Ω. In this case, the saline gap could be considered as a short circuit with a small voltage drop. The removal of these nodes can be used to simplify the circuit without changing the voltage gradient to the

endoneurium.

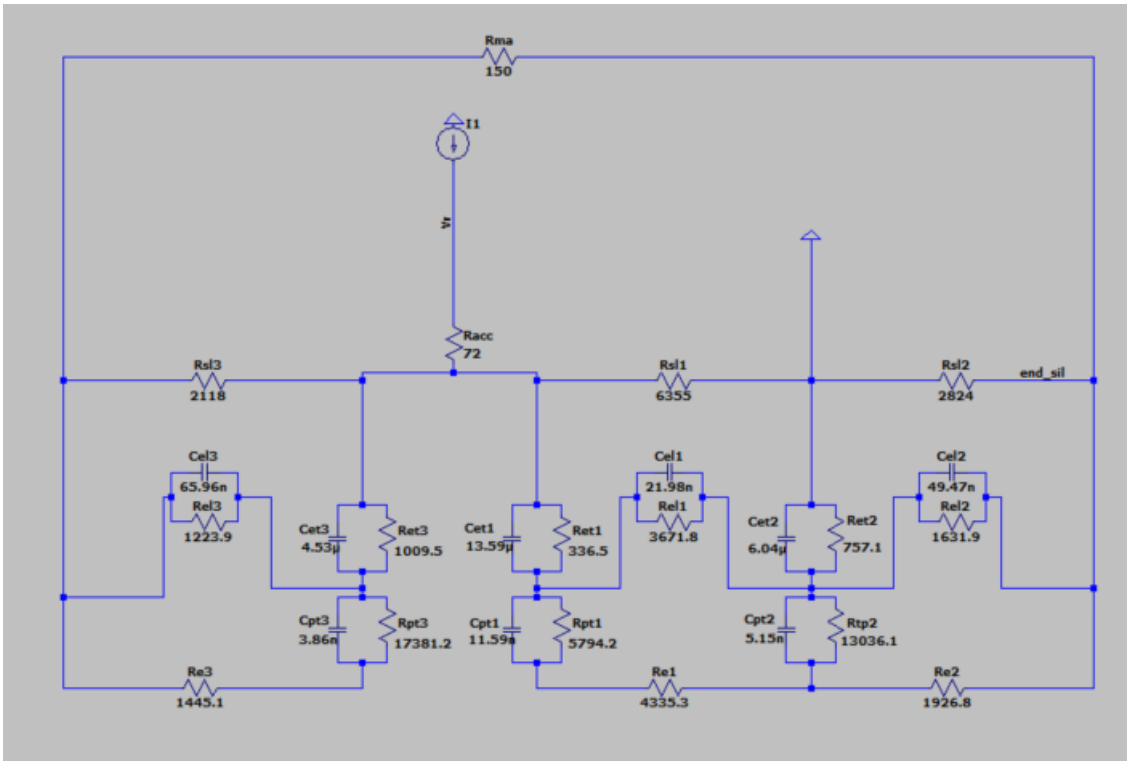


Figure 4.25: Reduced three-section equivalent circuit of the cuffed nerve. The 24 mm distal extremities and transverse saline components were removed. The central 9 mm active region and the two sections inside the cuff (3 mm and 4 mm) remain intact. The architecture isolates the central current steering zone, maintains the core electrical load and makes it easy to implement physical hardware.

Frequency sweep simulation validates the reduction of circuits. A global Bode plot shows the 3D COMSOL model, the original five-section circuit, and the simplified three-section circuit (Figure 4.26). The magnitude and phase curves of the simplified and the original circuit overlap across the whole frequency spectrum. This visual representation demonstrates that the simplification applied does not affect the main electrical response. A specific error analysis calculates the numerical difference between the simplified circuit and the original circuit (Figure 4.27). The magnitude error is close to zero. It stays below 2% for most frequencies. The absolute phase deviation is less than 0.7 degrees for the whole spectrum. These values show that the distal extremities and transverse saline components have no significant electrical weight. A final comparison evaluates the simplified circuit with the original 3D FEM model (Figure 4.28). The error profile is similar to the original five-section network. The magnitude error exhibits a -38.4% underestimation at 100 Hz. The curve transitions into a positive overestimation and reaches a peak

of +48.8% at 100 kHz. At the specific frequency of 1 kHz, the magnitude error registers at -24.7%. The absolute phase error remains bounded across the entire spectrum. At 1 kHz, the phase deviation is 7.08 degrees. The peak phase difference occurs at 100 kHz with a 12-degree divergence. These specific percentages replicate the exact error profile of the original five-section circuit across all critical frequency decades.

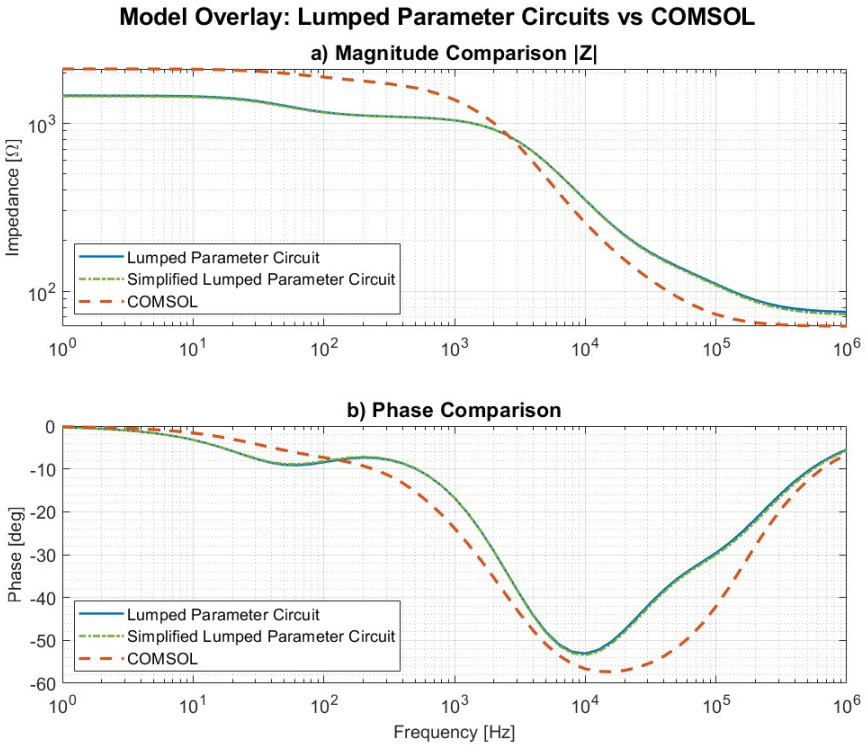


Figure 4.26: Bode plot overlay comparing the 3D COMSOL model, the original five-section circuit, and the simplified three-section circuit. (a) Magnitude comparison $|Z|$, illustrating the close alignment of the impedance magnitude across the entire frequency spectrum. (b) Phase comparison in degrees, highlighting the complete overlap of the phase responses for the simplified and original circuits.

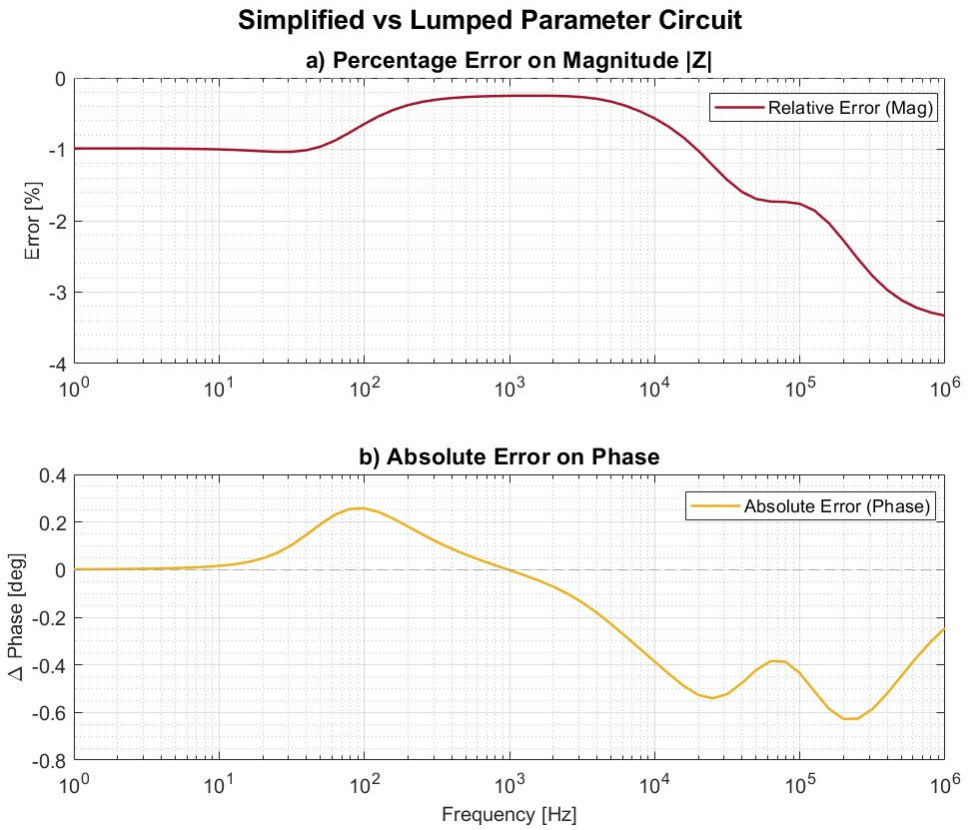


Figure 4.27: Error in frequency-dependent variation between the simplified three-section circuit and the original five-section network. (a) Percentage relative error on the impedance magnitude $|Z|$, illustrating a negligible deviation remaining near zero across the entire frequency spectrum. (b) Absolute error on the phase response in degrees, highlighting minimal angular discrepancies bounded below 0.7°.

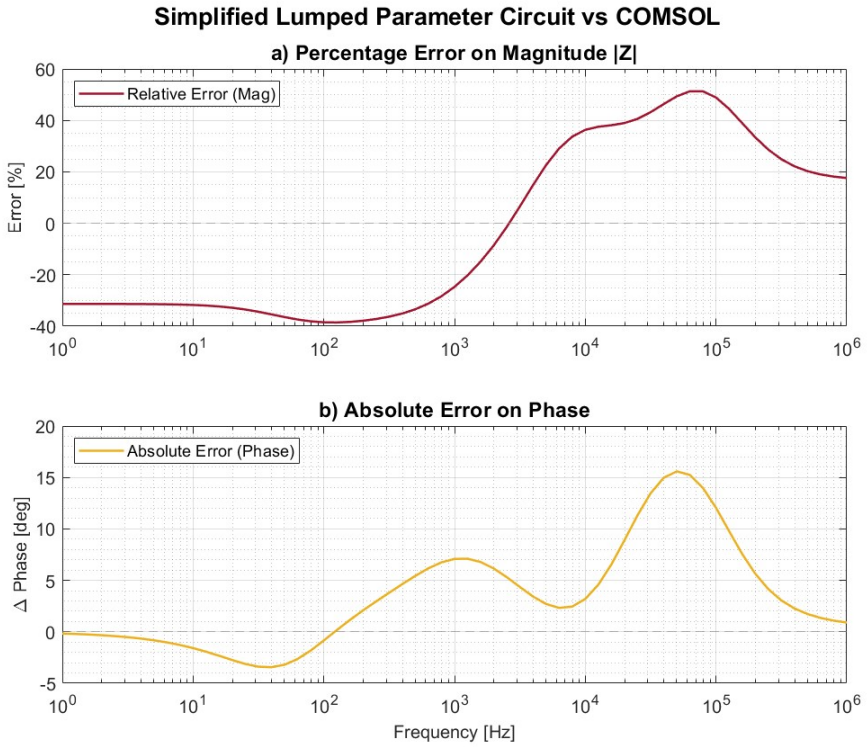
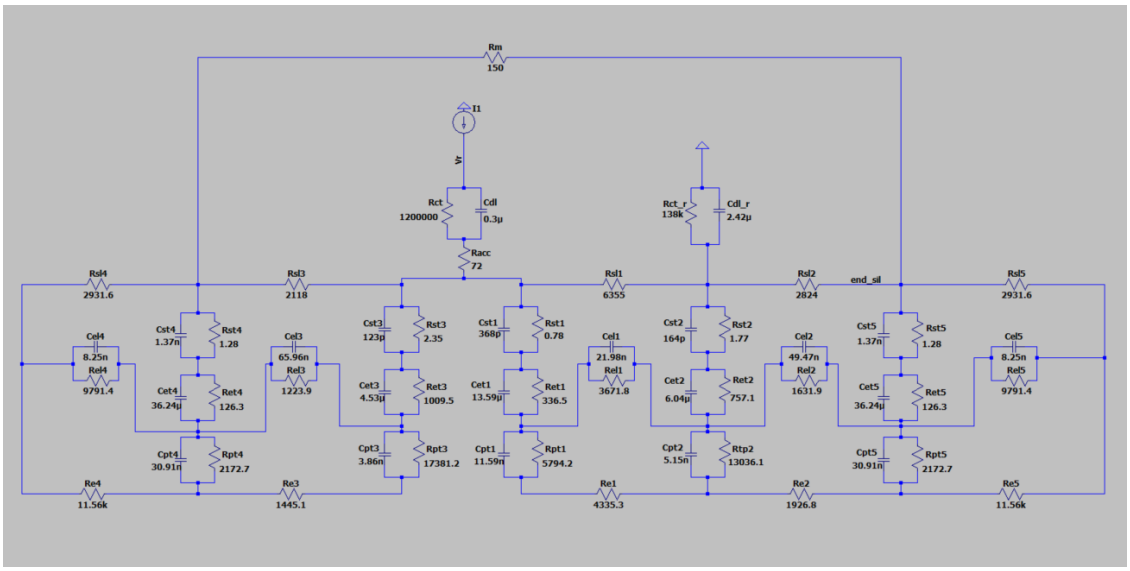


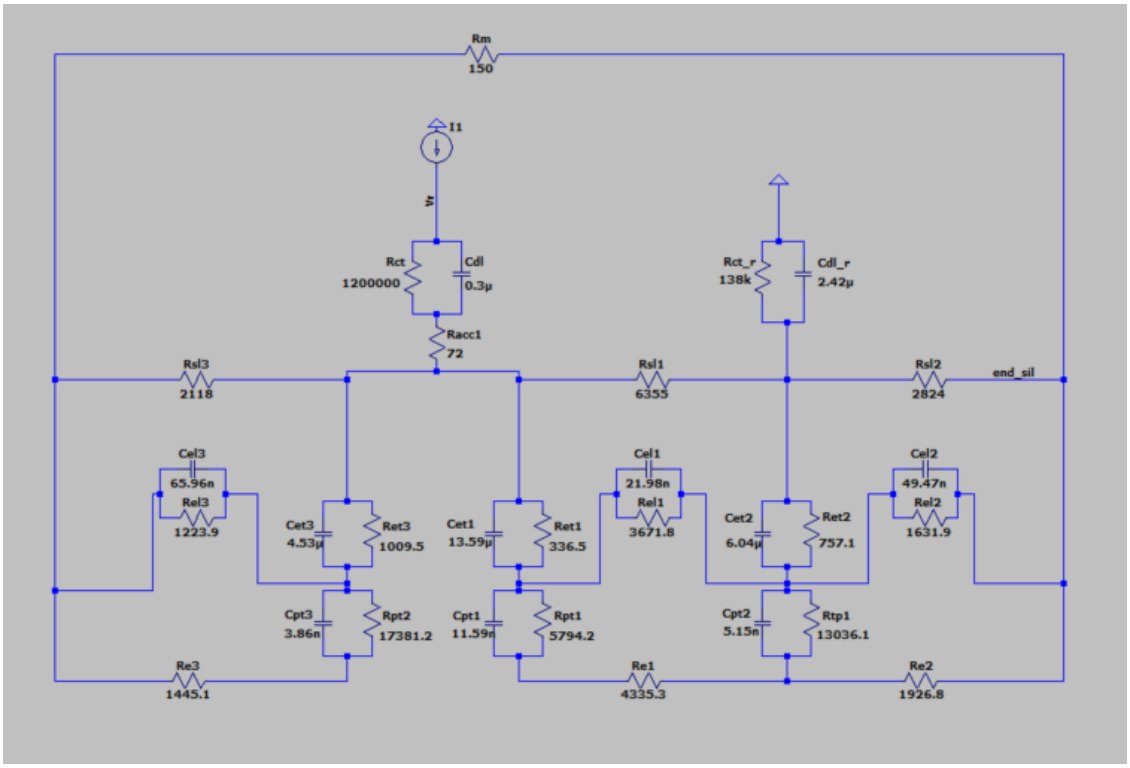
Figure 4.28: Error in frequency-dependent variation between the simplified three-section circuit and the 3D FEM model. (a) Percentage relative error on the impedance magnitude $|Z|$. (b)Absolute error on the phase response in degrees.

4.3 Complete circuit models

Once the electrical impedance of the nerve tissues is modeled through the lumped-parameter network, the contribution of the electrode-electrolyte interface must be included. Following the detailed analysis in Section 4.1, this polarization behavior is integrated at the input stage. Parallel components represent the active disk electrode with a charge transfer resistance of $R_{ct} = 1.2$ MΩ and a double-layer capacitance of $C_{dl} = 0.3$ μF. Equivalent branches represent the return electrode with $R_{ct_r} = 138$ kΩ and $C_{dl_r} = 2.42$ μF, utilizing values derived from the NerveRepack project database. This complete interface integration is applied to both the original five-section network and the simplified three-section architecture, as illustrated in Figure 4.29. Once the electrical impedance of the nerve tissues is modeled through the lumped-parameter network, the electrode-electrolyte interface must be added to complete the global system architecture. Following the analysis in Section 4.1, this electrochemical coupling is integrated at the active stimulation input and the return path. Parallel components represent the active disk electrode with a charge transfer resistance of $R_{ct} = 1.2$ MΩ and a double-layer capacitance of $C_{dl} = 0.3$ μF. Equivalent branches represent the return ring electrode with $R_{ct_r} = 138$ kΩ and $C_{dl_r} = 2.42$ μF, utilizing values derived from the NerveRepac project database. This interface integration applies to both the original five-section network and the simplified three-section architecture, as illustrated in Figure 4.29.



(a) Five-section circuit



(b) Three-section circuit

Figure 4.29: Complete and simplified lumped-parameter circuits incorporating the electrode-electrolyte interface dynamics, including the active (R_{ct}, C_{dl}) and return (R_{ct_r}, C_{dl_r}) branches derived from the NerveRepac database.

An AC sweep simulation in LTspice evaluated the frequency response of both the complete Five-section Circuit and the simplified Three-section Circuit. As illustrated in Figure 4.30, the resulting Bode plots of the two circuits are overlapped and compared to the 3D COMSOL impedance trends. The latest represents the biological tissue load without the electrode-electrolyte interfaces' contribution. The plots demonstrate a strict overlap between the two circuit models, yielding identical magnitude and phase curves across the entire frequency spectrum. This demonstrates that the simplification of the lumped-parameter circuits in Section 4.3 does not lead to relevant impedance changes in the ultimate design. At frequencies below 1 kHz, the electrode-electrolyte interface determines the circuit behavior. The double-layer capacitance (C_{dl}) introduces a dominant high-impedance barrier, generating a steep magnitude drop and forcing the phase shift toward -90 degrees. At the same time, the COMSOL model does not present this specific interface stage, and it maintains a flat resistive baseline and a zero-degree phase in this low-frequency region. When frequency increases, the global impedance of the LTspice models converges toward the electrical footprint of the nerve tissue, bending the circuit magnitude and phase to replicate the COMSOL tissue dynamics. Indeed, beyond 1 kHz, the impedance of the interface capacitors approaches zero, causing the C_{dl} components to transition into short circuits. Consequently, the electrode-electrolyte interface does not provide a significant contribution. A quantitative error analysis of the deviations between the Five and Three section circuits is performed. The percentage error of the impedance magnitude $|Z|$ is close to zero at low and mid frequencies (-0.11% at 100 Hz and -0.17% at 1 kHz). The deviation increases in the high-frequency bands, reaching -1.68% at 100 kHz and -3.5% at 1 MHz (Figure 4.31a). The absolute error of the phase response is minimal at low frequencies; it is shifted by -0.04° at 1 kHz and increases at higher frequencies without exceeding 0.7° (Figure 4.31b).

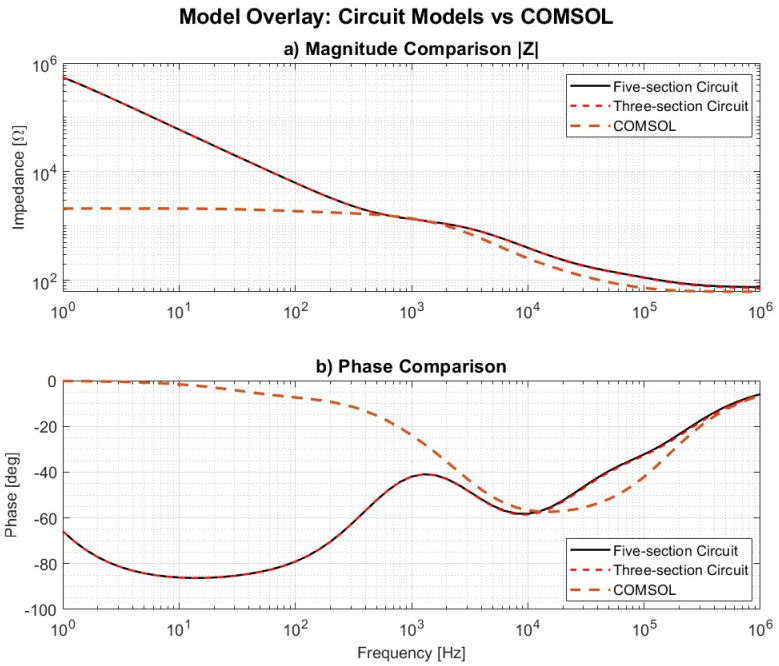


Figure 4.30: Bode plot overlay comparing the full Five-section Circuit, the simplified Three-section Circuit, and the 3D COMSOL tissue model. (a) Magnitude comparison $|Z|$. The LTspice circuits exhibit a steep capacitive drop at low frequencies driven by the electrode interface. The curves transition at 1 kHz to track the COMSOL tissue footprint. (b) Phase comparison in degrees. The circuits demonstrate a near -90 degree phase shift at low frequencies due to the double-layer capacitance (C_{dl}).

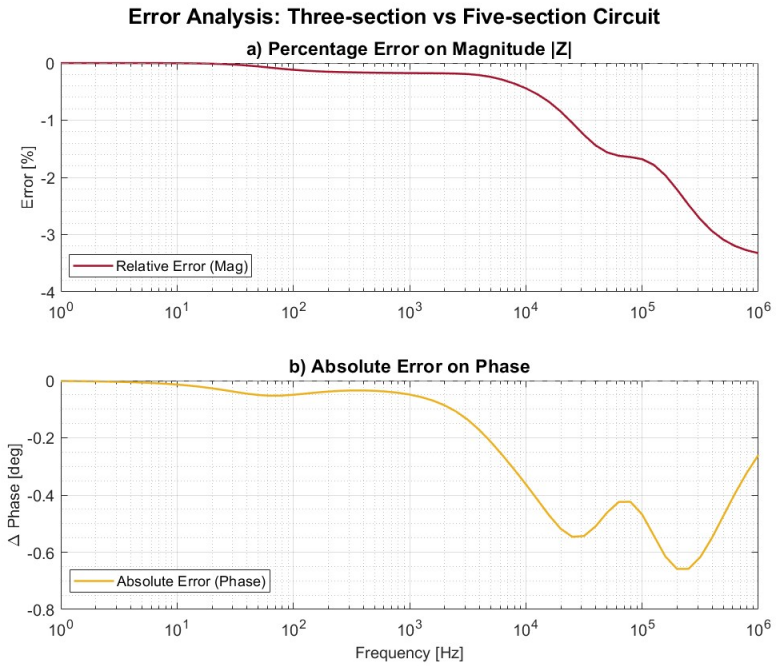


Figure 4.31: Error analysis quantifying the frequency-dependent deviations between the simplified Three-section Circuit and the original Five-section Circuit. (a) Percentage relative error on the impedance magnitude $|Z|$, illustrating deviations below 0.2% in the low and mid-frequency bands and a bounded maximum error below 3.5% at high frequencies. (b) Absolute error on the phase response in degrees, highlighting a maximum angular discrepancy that remains below 0.7° across the entire investigated spectrum.

Following the spectral methodology established in Section 4.3, Figure 4.32 overlays the amplitude spectrum of the 100 μs pulse with the Bode magnitude plots of the complete Five-section and Three-section Circuits. This visualization serves to physically contextualize the stimulus energy transfer within the final models. The primary energetic lobe of the injected current reaches its absolute peak strictly in the mid-frequency band, effectively bypassing the initial low-frequency capacitive barrier of the electrode-tissue interface (C_{dl}). The graphical analysis directly confirms that the maximum stimulus amplitude is delivered exactly into the region where the impedance has a plateau, ensuring optimal and stable current transfer for the complete circuit models.

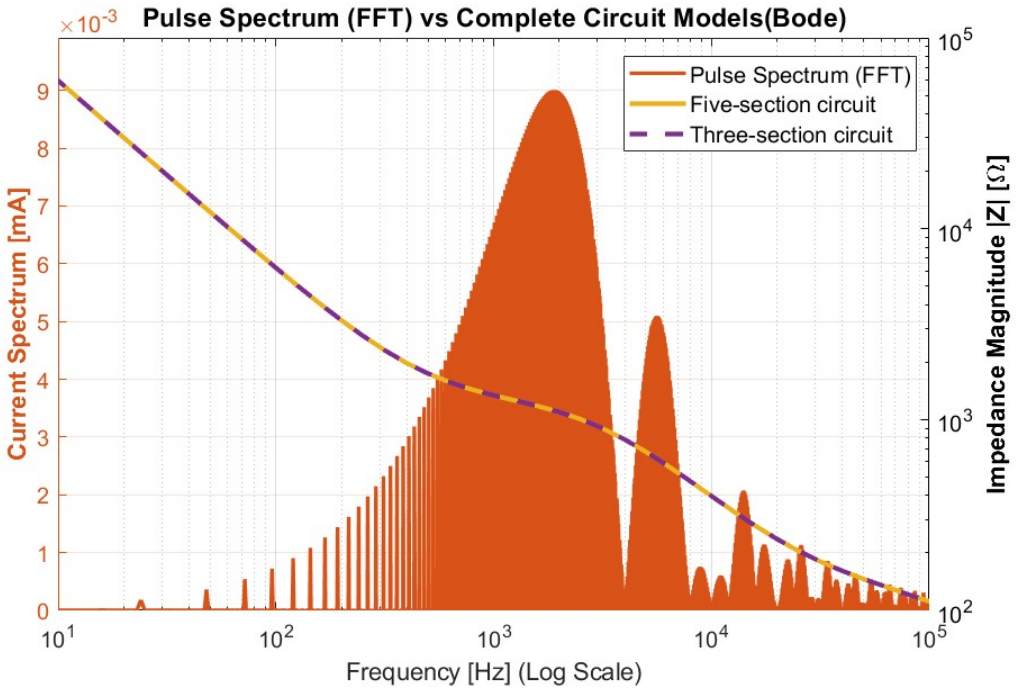


Figure 4.32: Spectral overlay of the 100 μs biphasic pulse amplitude (FFT, mA) and the impedance magnitude (Ω) for the complete circuit models. The Five-section (solid yellow line) and Three-section (dashed purple line) lumped-parameter architectures exhibit perfect magnitude overlap across the entire evaluated spectrum. The visualization confirms that the primary energetic lobe of the stimulus effectively bypasses the high-impedance low-frequency barrier (C_{dl}), injecting maximum harmonic current directly into the attenuated-impedance mid-frequency band where the complex tissue dynamics are accurately captured.

4.4 Altium PNT Development

4.4.1 Schematic

Following the validation of the final simplified circuit model (Three-section Circuit), the physical realization of the hardware was designed and developed using Altium Designer. As shown in the schematic, the architecture interfaces with the RHS/RHD headstage output with an 18-channel Omnetics connector. At the connector level, the even and odd channels are short-circuited to each other and routed with their own circuit: the layout includes two identical and separate circuits, and the components associated with the odd channels' circuit are designated with the _d suffix. To evaluate potential inter-channel interference, a crosstalk network comprising a series resistor (R_{tk}) and a parallel RC network (C_{tk}) was integrated

immediately following the access resistance stage and linking the two potential nodes $V_{s,\mathrm{d}}$ and V; these designated pads are left unpopulated for future developmental optimization. Each circuit incorporates two SMA connectors strategically placed at the initial input and downstream of the electrode interface block (encompassing the access resistance and double-layer capacitance, C_{dl}). This dual-SMA configuration enables independent experimental evaluation of both the overall circuit impedance and the specific potential drop induced by the electrode-electrolyte coupling. The implemented components closely adhere to the theoretical framework, with minor adjustments introduced to comply with commercial component availability. Additionally, to optimize board real estate and save physical space, high-value capacitances, specifically $C_{te3,1}$, $C_{te3,2}$, $C_{te3,\mathrm{d1}}$, $C_{te3,\mathrm{d2}}$ and $C_{te1,1}$, $C_{te1,2}$, $C_{te1,\mathrm{d1}}$, $C_{te1,\mathrm{d2}}$, were realized by placing two parallel components, each sized at half of the nominal theoretical value. All resistors are implemented in SMD technology with a maximum tolerance of 1%, reaching up to 0.1% for high-precision components. As for the capacitors, the majority utilize SMD packages with a 1% tolerance, whereas the higher-capacitance components are realized using through-hole film capacitors with a 5% tolerance. The resulting Bill of Materials (BOM) detailing these components is summarized in Table 4.4.

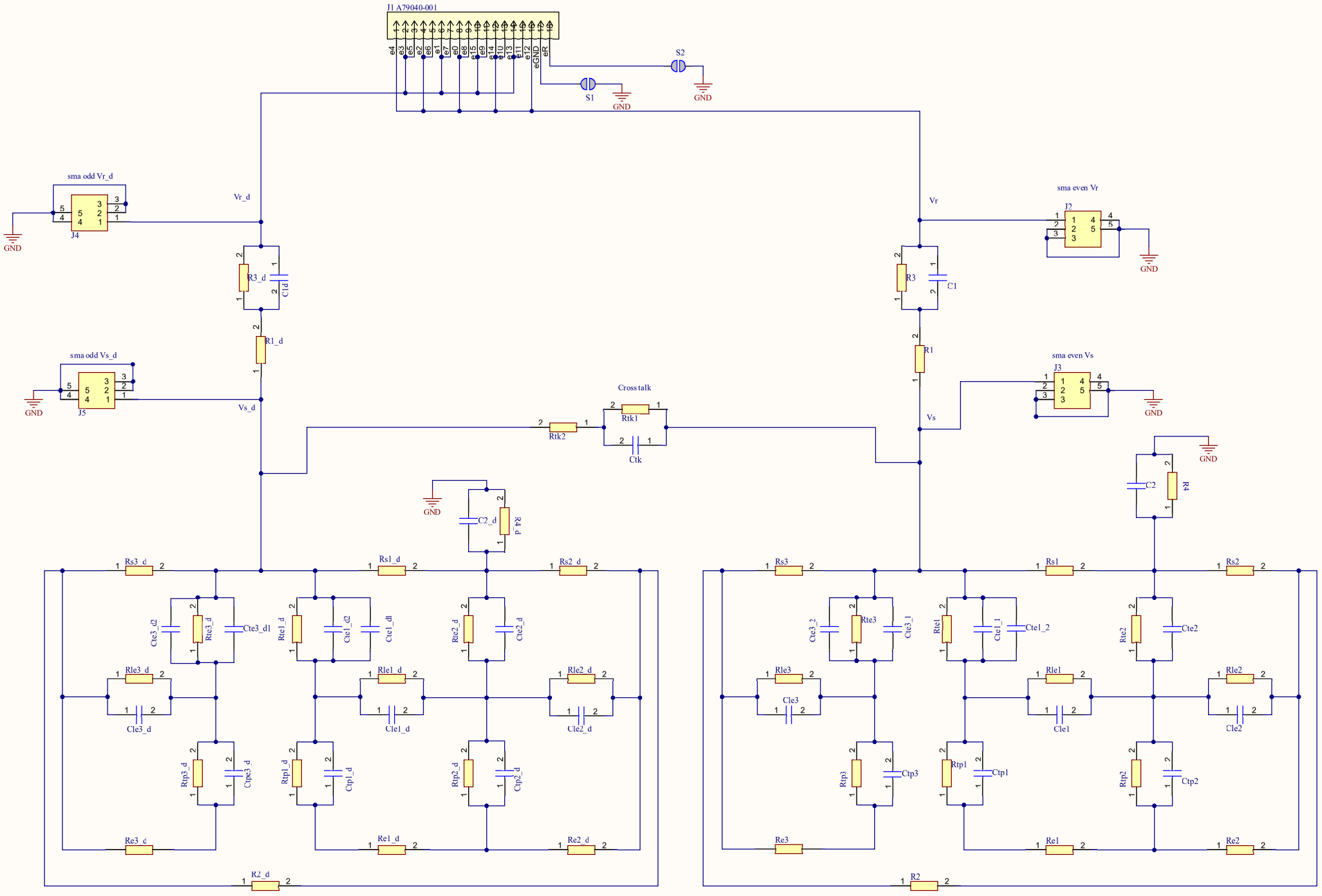

J1 A79040-001
S1
S2
GND
sma odd Vr_d
J4
Vr_d
R3_d
C1d
R1_d
sma odd Vs_d
J5
Vs_d
Cross talk
Rtk1
Rtk2
Ctk
C2_d
R4_d
Rs3_d
Rs1_d
Rs2_d
Cte3_d2
Rte3_d
Cte3_d1
Rte1_d
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Rle3_d
Cle3_d
Rle1_d
Cle1_d
Rle2_d
Cle2_d
Rtp3_d
Ctpe3_d
Rtp1_d
Ctp1_d
Rtp2_d
Ctp2_d
Re3_d
Re1_d
Re2_d
R2_d
Vr
sma even Vr
J2
R3
C1
R1
Vs
sma even Vs
J3
C2
R4
Rs3
Rs1
Rs2
Cte3_2
Rte3
Cte3_1
Rte1
Cte1_1
Cte1_2
Rte2
Cte2
Rle3
Cle3
Rle1
Cle1
Rle2
Cle2
Rtp3
Ctp3
Rtp1
Ctp1
Rtp2
Ctp2
Re3
Re1
Re2
R2

Table 4.4: Complete list of resistors and capacitors implemented on the PCB design, detailing component designators, electrical values, mounting styles, package dimensions, and tolerances.

Component/s	Value	Mounting Style	Dimension	Tolerance
Resistors				
R1, R1_d	70.6 Ω	SMD	1206	1%
R2, R2_d	150 Ω	SMD	1206	0.1%
Rte1, Rte1_d	332 Ω	SMD	0603	1%
Rte2, Rte2_d	750 Ω	SMD	0603	1%
Rte3, Rte3_d,	1 kΩ	SMD	1206	1%
Rle3, Rle3_d	1.21 kΩ	SMD	0603	1%
Re3, Re3_d	1.43 kΩ	SMD	0603	0.1%
Rle2, Rle2_d	1.62 kΩ	SMD	0603	1%
Re2, Re2_d	1.91 kΩ	SMD	0805	0.1%
Rs3, Rs3_d	2.1 kΩ	SMD	0805	0.1%
Rs2, Rs2_d	2.84 kΩ	SMD	0805	0.1%
Rle1, Rle1_d	3.65 kΩ	SMD	0805	0.1%
Re1, Re1_d	4.32 kΩ	SMD	0603	0.1%
Rtp1, Rtp1_d	5.76 kΩ	SMD	0805	0.1%
Rs1, Rs1_d	6.34 kΩ	SMD	1206	0.1%
Rtp2, Rtp2_d	13 kΩ	SMD	0603	1%
Rtp3, Rtp3_d	17.4 kΩ	SMD	0805	1%
R4, R4_d	138 kΩ	SMD	0603	1%
R3, R3_d	1.2 MΩ	SMD	0603	1%
Capacitors				
Ctp3, Ctpe3_d	3900 pF	SMD	0603	1%
Ctp2, Ctp2_d	5100 pF	SMD	0603	1%
Ctp1, Ctp1_d	0.012 μF	SMD	0603	1%
Cle1, Cle1_d	0.022 μF	SMD	1206	1%
Cle2, Cle2_d	0.047 μF	SMD	0805	1%
Cle3, Cle3_d	68 nF	SMD	1206	1%
C1, C1d	0.3 μF	SMD	6050 (Metric)	5%
C2, C2_d, Cte3_1, Cte3_2, Cte3_d1, Cte3_d2	2.2 μF	Through-Hole (Film)	7.8 × 7.8 mm	5%
Cte1_1, Cte1_2, Cte1_d1, Cte1_d2, Cte2, Cte2_d	6.8 μF	Through-Hole (Film)	18 × 8 mm	5%

An AC sweep frequency analysis in LTspice verified the physical implementation of the Three-section circuit. The simulation substituted theoretical parameters with the commercial component values detailed in Table 4.4. The macroscopic Bode plot overlay (Figure 4.33) shows a clear visual overlap of the magnitude and phase profiles among the theoretical Five-section model, the theoretical Three-section model, and the Three-section hardware realization. In the low-frequency capacitive region (below 100 Hz), the hardware circuit shows a peak error of +1.1%. As the frequency increases and the tissue's bulk resistive properties dominate the impedance profile, the magnitude error between the commercial and theoretical Three-section models converges to zero (Figure 4.34a). The comparison between the Three-section hardware model and the complete Five-section reference (Figure 4.34b) provides the most stringent evaluation. This specific overlay stacks the structural simplification error with the physical component values. Despite this combined effect, the hardware performance remains stable in the operational band of interest. Between 100 Hz and 10 kHz, the region where the stimulus energy is concentrated, the magnitude error stays below 0.8%. The maximum structural deviation reaches -3.3% at 1 MHz, a frequency located far outside the primary energetic band of the injected pulse. The absolute phase error analysis (Figure 4.35) reinforces this dynamic fidelity. In both comparisons, the phase discrepancy oscillates close to zero across the entire 1 Hz to 1 MHz spectrum. Even in the most stringent scenario against the complete model, the maximum deviation peaks at just -0.78° near 30 kHz. This minimal difference demonstrates that the physical test bed successfully preserves the essential RC time constants of the theoretical network, accurately replicating the reactive timing and dispersion dynamics of the biological tissue.

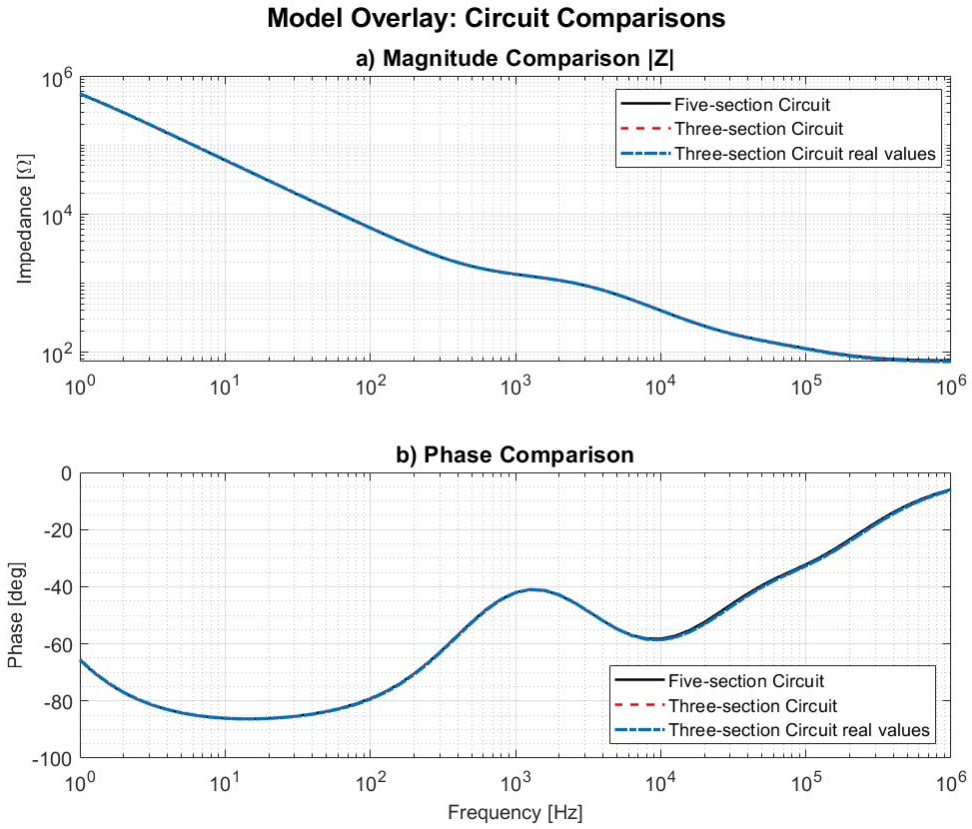


Figure 4.33: Macroscopic Bode plot overlay evaluating the frequency response of the modeled architectures across the 1 Hz to 1 MHz spectrum. Panel (a) illustrates the impedance magnitude ($|Z|$, Ω) and panel (b) details the phase angle (deg). The graphical analysis demonstrates a near-perfect visual superimposition among the complete theoretical Five-section reference (solid black line), the simplified theoretical Three-section circuit (dashed red line), and the LTspice hardware simulation of the Three-section Circuit real values.

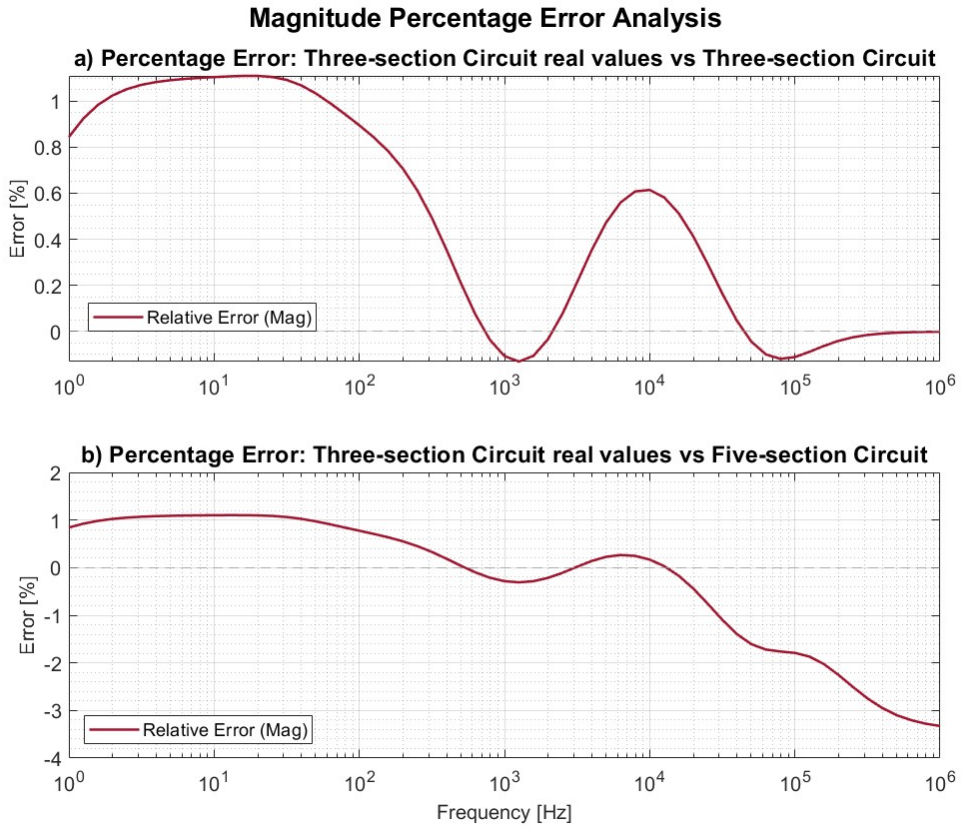


Figure 4.34: Magnitude percentage error analysis evaluating the hardware realization across the 1 Hz to 1 MHz spectrum. Panel (a) compares the hardware model (utilizing commercial component values) directly against the theoretical Three-section circuit. Panel (b) evaluates the hardware model against the complete theoretical Five-section reference.

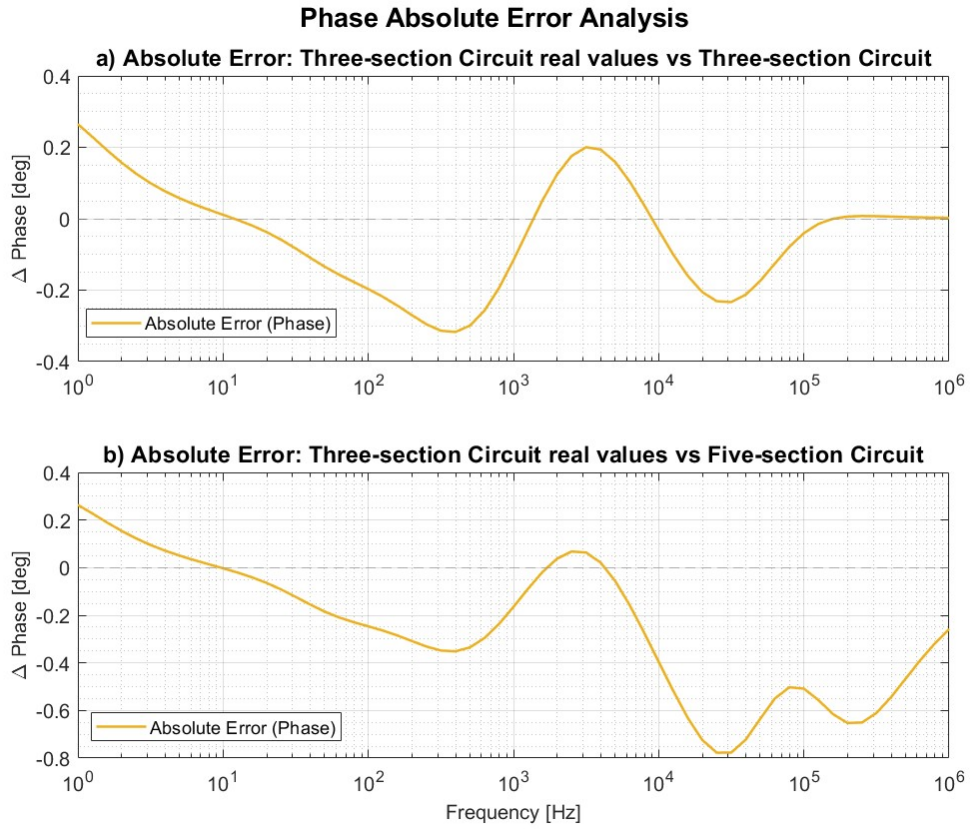


Figure 4.35: Absolute phase error analysis evaluating the dynamic fidelity of the hardware realization across the 1 Hz to 1 MHz frequency spectrum. Panel (a) compares the hardware model (utilizing commercial component values) directly against the theoretical Three-section circuit, showing a phase deviation that oscillates tightly around zero (bounded between +0.25° and -0.32°). Panel (b) evaluates the same hardware model against the complete theoretical Five-section reference. The absolute phase discrepancy remains strictly sub-degree throughout the entire spectrum, peaking at just -0.78°.

4.4.2 PNT Routing

The PCB (Figure 4.36) was engineered within a compact footprint of 10 mm × 10 mm utilizing a dual-layer configuration. To establish a stable reference potential and electromagnetic shielding, a ground plane was structured on the top layer, which accommodates the majority of the signal trace routing. The bottom layer was selectively utilized to resolve routing conflicts and prevent trace intersections, strictly adhering to the design rule constraints (imposing a minimum clearance of 0.15 mm). A uniform track width of 0.35 mm was implemented across all signal

paths, providing an optimal balance that safely supports stimulation currents.

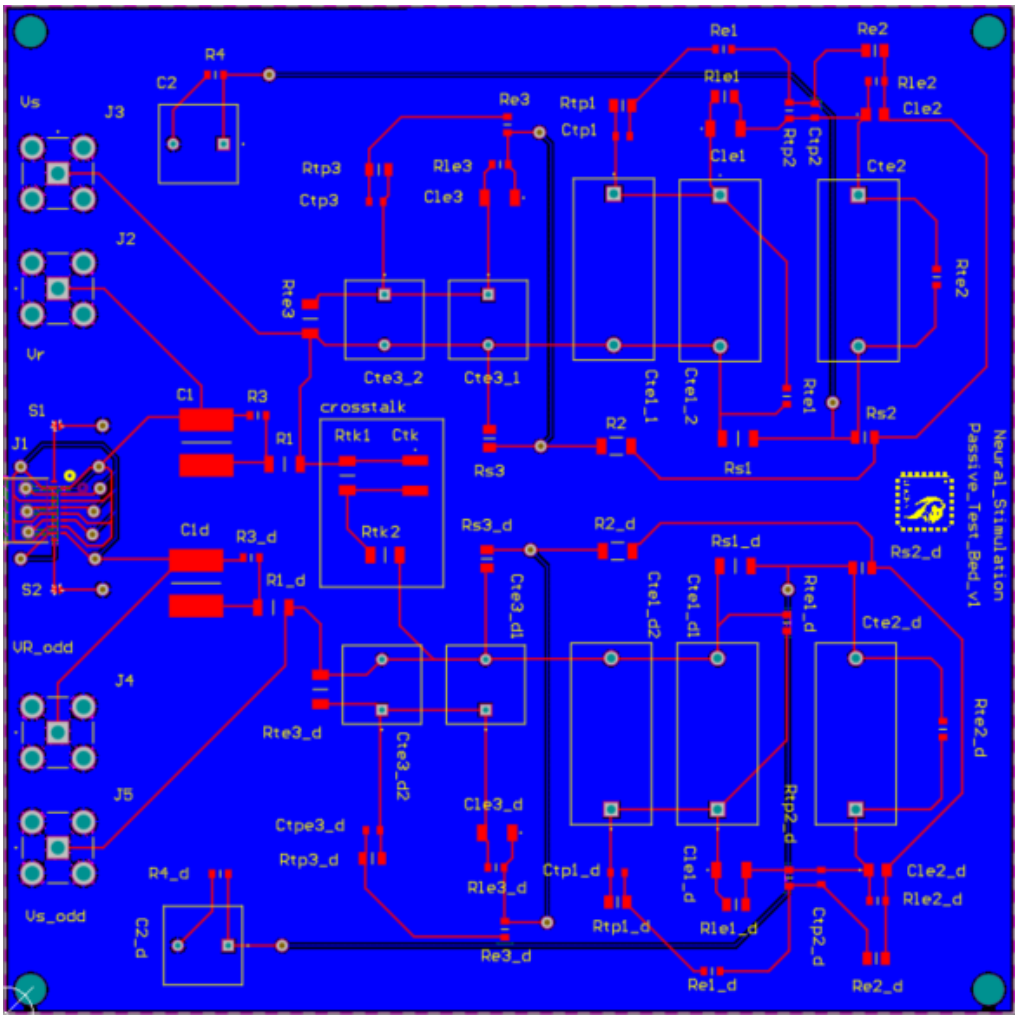


Figure 4.36: Dual-layer PCB layout (10 mm × 10 mm) of the passive test bed for median nerve stimulation. The board features a top ground plane and signal routing primarily on the top layer, with selective bottom-layer bridging to avoid trace intersections.

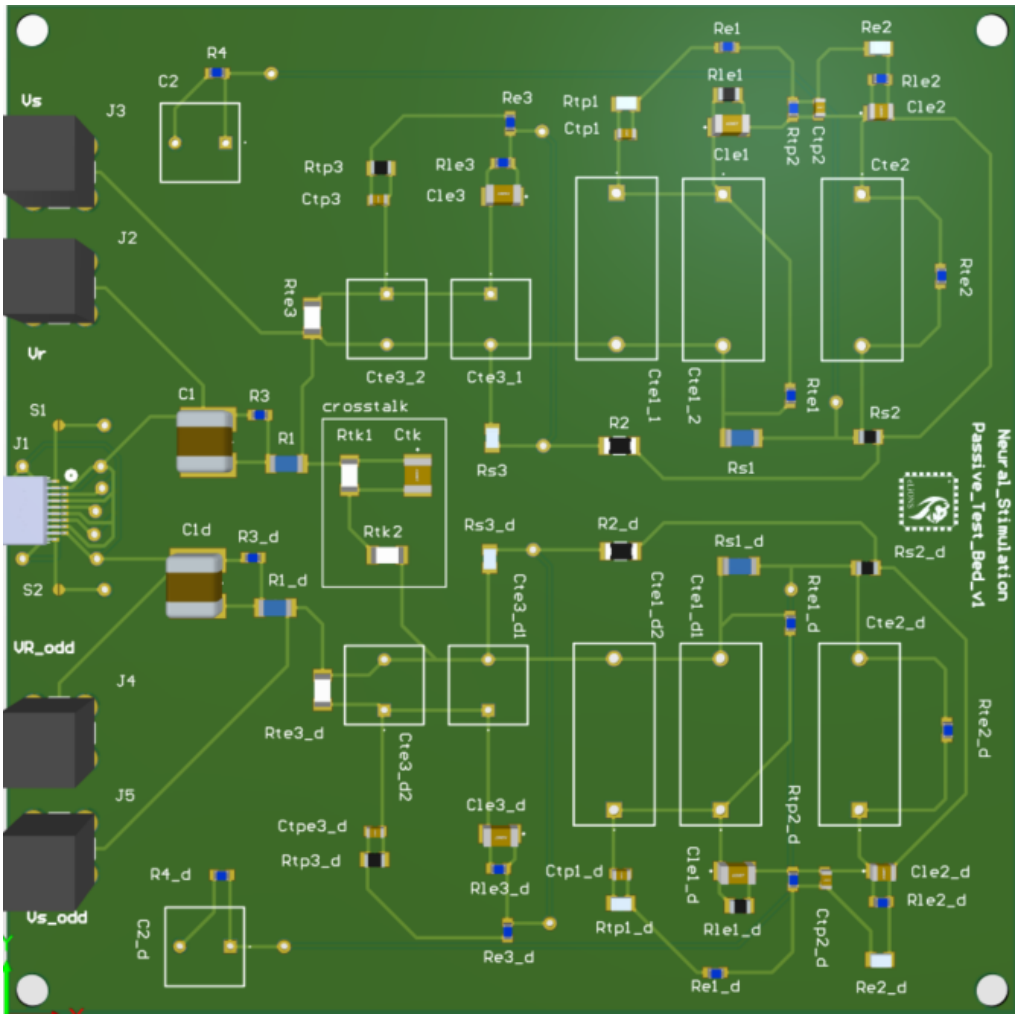


Figure 4.37: Three-dimensional rendered view of the PNT.

Chapter 5

Test and Results

5.1 Test Shield

5.1.1 Acquisition test

An experimental setup was configured to perform an acquisition test with the RHD2132. A Keithley 3390 Arbitrary Waveform Generator provided a controlled reference signal, set to a 1 kHz sinusoidal wave with a 1 V_{pp} amplitude and a 0 V DC offset (Figure 5.1).

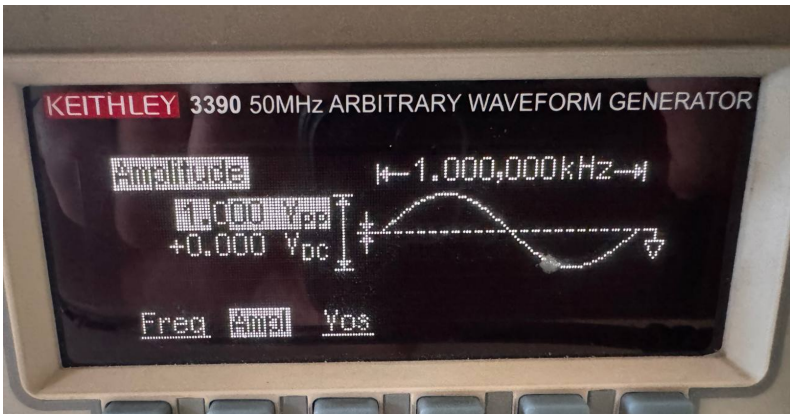


Figure 5.1: Front panel display of the Keithley 3390 Arbitrary Waveform Generator showing the output parameters of the reference sinusoidal signal: a frequency of 1 kHz, a peak-to-peak amplitude of 1 V_{pp}, and a zero DC offset.

The signal generated by the Keithley 3390 is carried via two coaxial cables into a custom hardware voltage divider developed by the research group. This dedicated PCB attenuates the 1 V_{pp} input to the microvolt scale, replicating the dynamics of a physiological neural signal. The scaled output is fed directly into

the Intan RHD2132 headstage through an Omnetics Nano 18-pin male connector. The RHD headstage then interfaces with the Shield mounted on the STM32 Nucleo microcontroller (Figure 5.2). Driven by custom acquisition firmware developed by the research group, the Nucleo board acquires and transmits the digitized data stream via serial communication to a host PC.

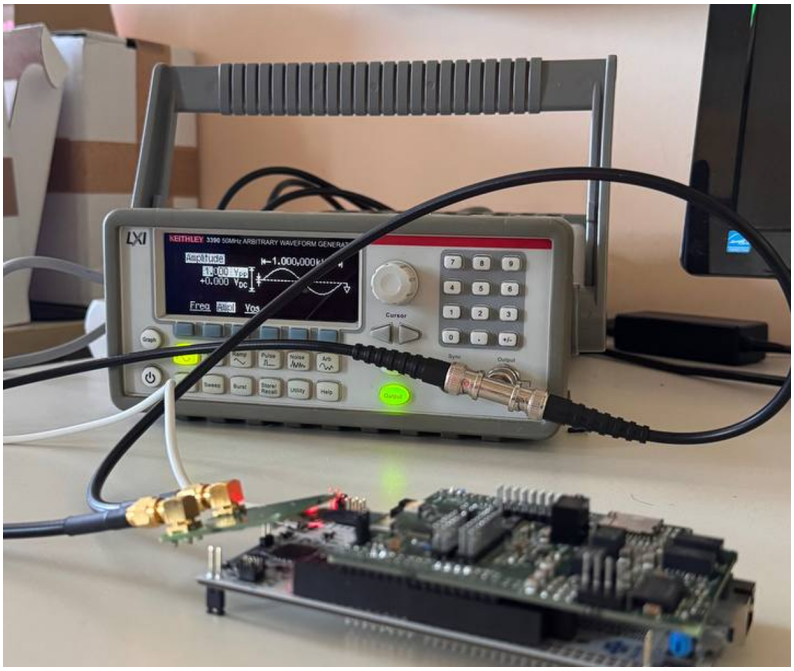


Figure 5.2: Complete experimental bench setup for acquisition validation. A Keithley 3390 Arbitrary Waveform Generator (background) supplies a reference 1 kHz, 1 V_{pp} sinusoidal signal. The output is routed via coaxial cables to a custom voltage divider board equipped with SMA connectors (center-left), which attenuates the macroscopic signal to the physiological microvolt scale. This conditioned signal is then fed directly into the Intan RHD2132 headstage and STM32 Nucleo microcontroller assembly (foreground) for real-time data acquisition and serial transmission.

The data was processed in real time and visualized in MATLAB. The dedicated MATLAB script applies a 50 Hz notch filter to suppress the network interference, and computes the Power Spectral Density (PSD) using Welch's method to evaluate the frequency distribution. The software output in Figure 5.3 illustrates the simulated signals. The left panel displays the filtered time-domain waveform, demonstrating a stable oscillation properly bounded within the targeted physiological amplitude range (approximately ± 100 μV). The corresponding PSD analysis in the right panel reveals a single, sharp power peak located exactly at 1 kHz.

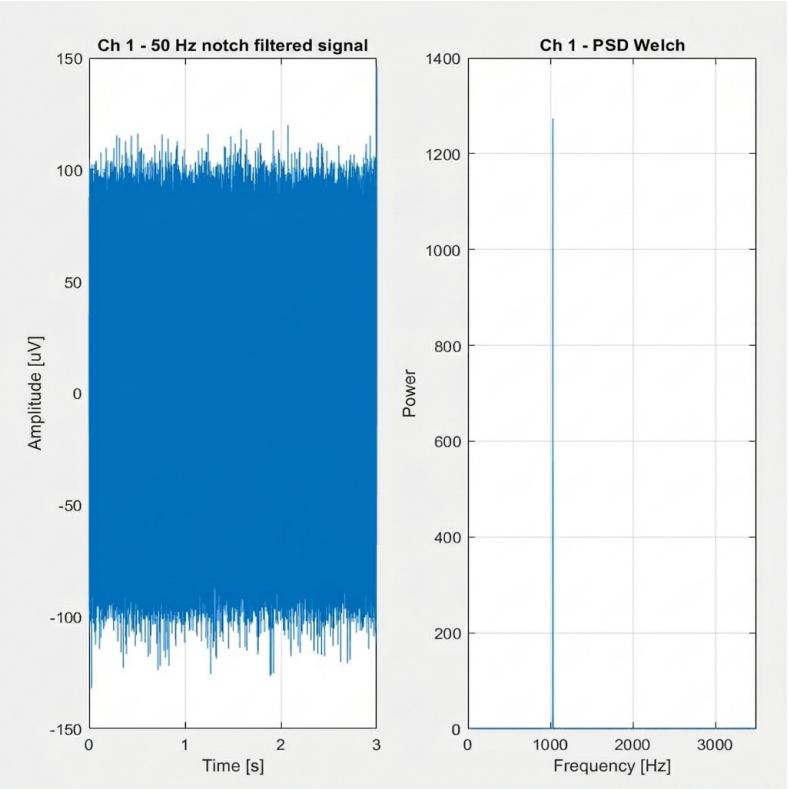


Figure 5.3: Real-time MATLAB processing output of the acquired test signal. The left panel displays the time-domain waveform after the application of a 50 Hz notch filter. The right panel presents the Power Spectral Density (PSD) computed using Welch's method with a single peak at 1 kHz.

5.1.2 Impedence check

The RHD2132 headstage incorporates a built-in impedance measurement feature. Impedance evaluation represents the primary diagnostic procedure conducted following device implantation, providing critical data on the physical condition of the electrode array and the tissue-electrode interface. The experimental setup comprises an STM32 Nucleo microcontroller equipped with a custom shield connected to the RHD2132 headstage. An Intan 18-pin Electrode Adapter Board interfaces with the headstage, routing all electrode contacts, reference, and ground connections to standard solder holes (Figure 5.4). This adapter includes a 16-pin DIP socket, keeping component leads short and preventing open loops susceptible to inductive noise. A discrete through-hole resistor is inserted into the DIP socket across the target channel inputs. The custom firmware running on the Nucleo triggers the internal impedance check routine of the RHD2132 chip. The system acquires the measurement and transmits the data via serial communication to a host PC. A PuTTY terminal emulator displays and logs the numerical output.

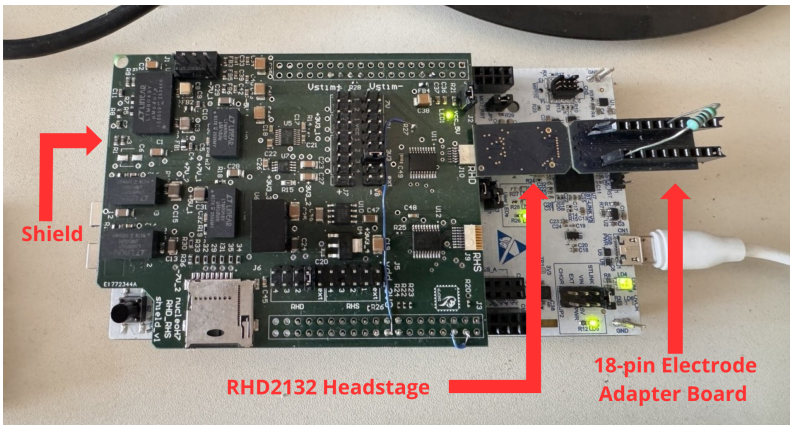


Figure 5.4: Configuration for the impedance measurement test. The setup comprises a custom shield mounted on an STM32 Nucleo microcontroller, interfacing directly with an Intan RHD2132 headstage. An 18-pin Electrode Adapter Board connects to the headstage, featuring a 16-pin DIP socket loaded with a discrete through-hole resistor across the target channel inputs.

The Intan RHD2132 headstage performs the impedance check by introducing an AC current and measuring the voltage drop on the electrode interface. The on-chip 8-bit digital-to-analog converter (DAC) generates a voltage waveform with a maximum amplitude of 1.225 V. A sinusoidal test signal in this range is simulated with a peak amplitude of 0.6125 V. The system routes this AC voltage through a software-selectable series capacitor (C_s) to produce the test current. The injected current amplitude follows the equation $I_{\text{peak}} = 2\pi f C_s V_A$. The hardware features three available capacitance scales for C_s: 0.1 pF, 1.0 pF, and 10 pF. The measured voltage must stay within the physical limits of the amplifier. The lower boundary is the noise floor of 2.4 μV, and the upper boundary is the saturation (5 mV) of the amplifier. A MATLAB script was used to calculate the voltage in comparison to the theoretical electrode impedance for all three capacitance scales at a frequency of 1 kHz. The expected impedance for a peripheral nerve cuff electrode falls between 600 Ω and 5 kΩ. The graphical output (Figure 5.5) incorporates a margin, expanding the observation window from 390 Ω to 6200 Ω. The red line indicates that the 10 pF capacitor keeps the voltage response above the noise floor and below the saturation limit for the entire target band.

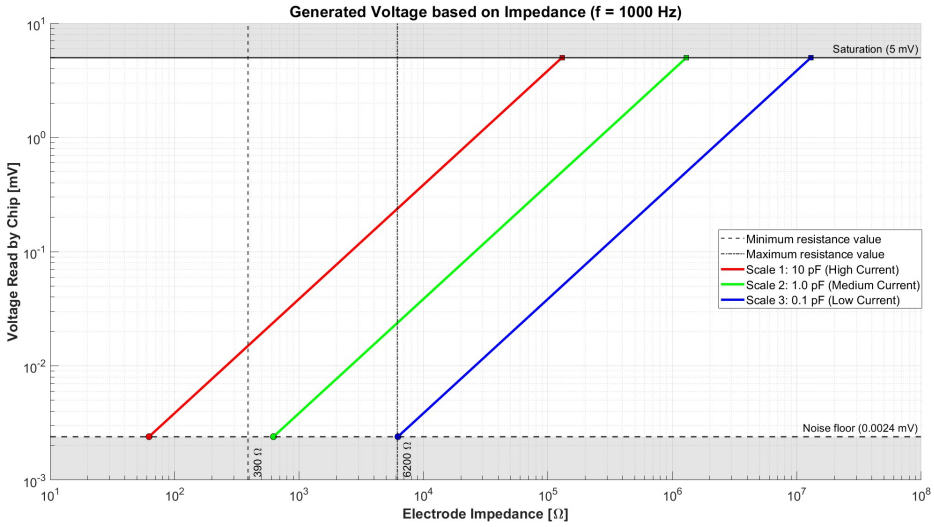


Figure 5.5: MATLAB graphic illustrating the theoretical voltage response versus electrode impedance for the three available RHD2132 series capacitors at 1 kHz. The horizontal boundaries indicate the amplifier's physical limits (2.4 µV noise floor and 5 mV saturation). The vertical dashed lines show the full target impedance range for the peripheral nerve cuff electrode (390 to 6200). The 10 pF capacitor (red line) provides a voltage response in the full target band.

A set of 1% tolerance through-hole resistors was selected from the laboratory stock to cover the range from 390 Ω to 6810 Ω. A Fluke 179 True RMS Multimeter measured every resistor, setting the physical baseline. The Intan RHD2132 headstage performed the internal impedance check on each resistor, recording 1000 samples per component and calculating the mean value. The resulting plot (Figure 5.6) shows the raw mean results against the theoretical response line (X=Y). The visual data reveal a non-uniform deviation across the spectrum. At lower impedance values, the system overestimates the magnitude compared to the reference. As the impedance increases, the measured line is closer to the ideal line, and an underestimation is observed at the highest resistance values.

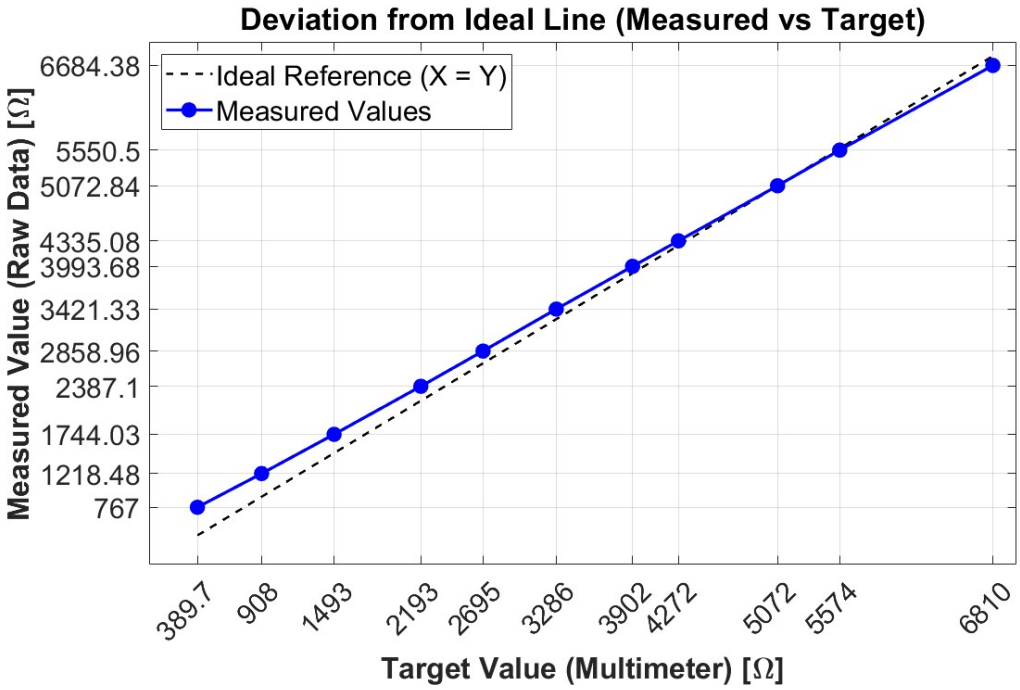


Figure 5.6: The mean raw impedance values of the Intan RHD2132 headstage plotted against the physical reference data from the digital multimeter. The dashed black line shows the expected (X = Y) result. The actual data (solid blue line) shows a systematic deviation with an overestimation at lower resistance values and an underestimate at the upper limit of the target range.

An independent mathematical verification evaluated the validity of the RHD2132 internal impedance model before proceeding with a full system calibration. As illustrated in the hardware block diagram (Figure 5.7), the manufacturer calculates the injected current assuming the series capacitor C_s constitutes the entire load, utilizing the simplified equation $I_{simplified} = 2\pi f C_s V_A$. The actual physical circuit operates as a voltage divider where the total load represents the vector sum of the capacitive reactance X_c and the target resistance R. A custom MATLAB script computed the exact current utilizing the magnitude of the complex impedance, expressed as $I_{exact} = V_A/\sqrt{R^2 + X_c^2}$, and compared the derived resistance values. At a 1 kHz working frequency, the 10 pF capacitor presents a reactance of approximately 15.9 MΩ. This reactance dictates the total current flow and transforms the internal DAC into a near-ideal AC current source. The numerical analysis demonstrated that the theoretical error introduced by the hardware simplification of the chip is on the order of 10^{-6}% (Tab.5.1). This negligible deviation confirms the structural soundness of the fundamental mathematical model, proving that measured discrepancies stem from analog baseline offsets and systemic noise requiring standard calibration.

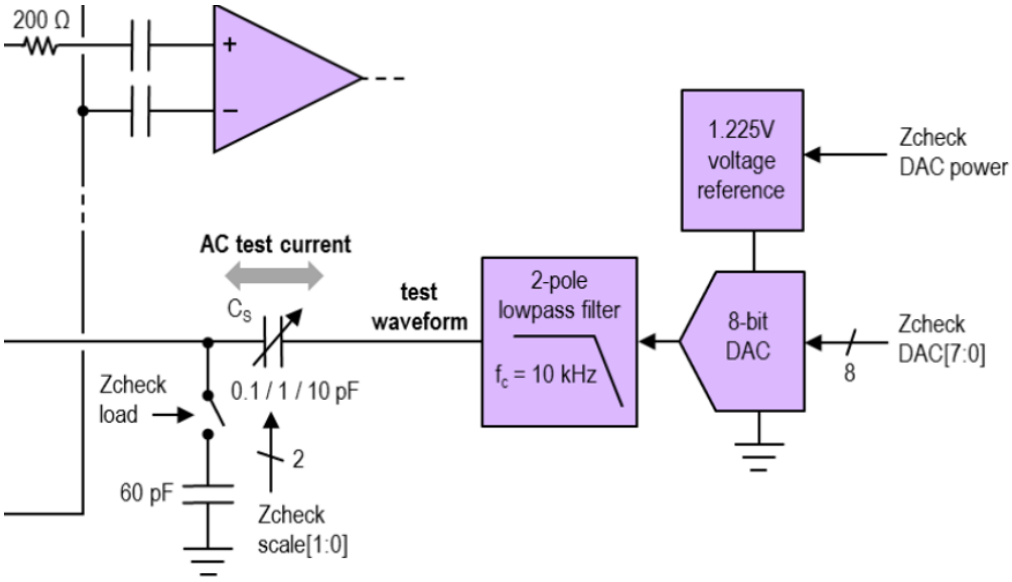


Figure 5.7: Schematic diagram of the RHD2132 on-chip impedance measurement circuitry. The hardware architecture forms a physical voltage divider between the software-selectable series capacitor (C_s) and the external electrode resistance. This structural representation serves as the foundation for the mathematical verification, illustrating how the dominant capacitive reactance of C_s transforms the internal voltage generator into a near-ideal AC current source and validates the simplified current equation.

Table 5.1: Representation of the theoretical error introduced by the manufacturer's simplified current equation ($I_{\text{simplified}} = 2\pi f C_s V_A$). It is negligible for all functional ranges (up to $1.83 \times 10^{-5}\%$).

Target Resistance R [Ω]	**Theoretical Voltage V_{out} [μV]**	**Theoretical Simplification Error [%]**
389.7	15.00	6.00×10^{-8}
908.0	34.94	3.25×10^{-7}
1493.0	57.46	8.80×10^{-7}
2193.0	84.40	1.90×10^{-6}
2695.0	103.72	2.87×10^{-6}
3286.0	126.46	4.26×10^{-6}
3902.0	150.17	6.01×10^{-6}
4272.0	164.41	7.20×10^{-6}
5071.0	195.15	1.02×10^{-5}
5574.0	214.51	1.23×10^{-5}
6810.0	262.08	1.83×10^{-5}

The MATLAB polyfit function performed first-degree polynomial regression on the mean raw data of the RHD2132 chip and the reference values of the digital multimeter. This step extracted the linear calibration parameters for the correction of the acquisition. The algorithm produced the calibration equation Y = 1.0797X - 406.1879 (Figure 5.8). The calibration parameters were embedded into the custom firmware, and the STM32 microcontroller applied the linear correction in real time as data were collected. A subsequent phase evaluated the performance and accuracy of the calibrated system. The test set is based on 1000 acquisitions for each of the 11 resistors used in the polynomial fitting and 7 novel independent resistors that were tested for empirical model validation. Statistical analysis of the sample arrays extracted the mean, median, quartiles, and standard deviation for each value (Tab. 5.2).

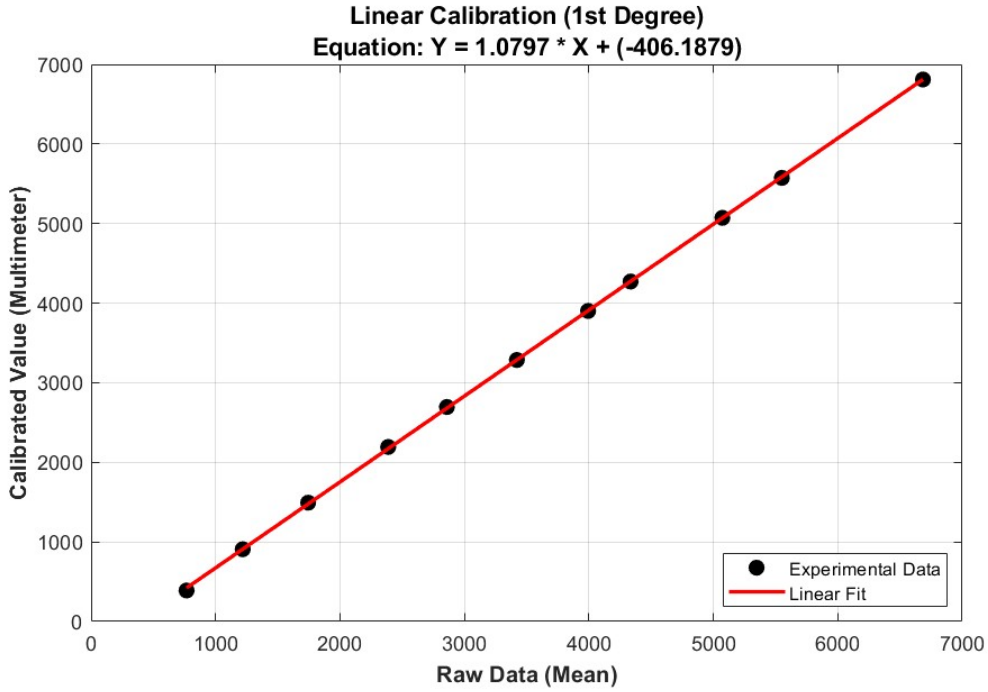


Figure 5.8: Linear calibration model generated in MATLAB. The plot shows the first-degree polynomial regression between the raw mean impedance data obtained by the RHD2132 headstage (x-axis) and the physical reference values generated by the digital multimeter (y-axis). The calibration equation ($Y = 1.0797X - 406.1879$) describes the slope and intercept parameters to correct the systemic hardware errors.

Table 5.2: Statistical summary of the calibrated impedance measurements. The dataset incorporates both the 11 components utilized for the initial linear regression and the 7 independent validation resistors (denoted by asterisks). The system acquired 1000 discrete samples per component to compute the mean, median, interquartile range (Q1, Q3), and standard deviation. The percentage error columns quantify the deviation of the calibrated mean and median values relative to the physical multimeter reference, demonstrating the accuracy of the real-time firmware correction across the entire target impedance range.

Point	Multimeter	Mean	Median (Q2)	Q1	Q3	Std. Dev.	Mean Rel. Error [%]	Median Rel. Error [%]
1	389.70	404.22	405.00	398.00	411.00	10.31	3.73	3.93
2*	618.00	636.96	637.00	632.00	642.00	8.08	3.07	3.07
3	908.00	915.47	915.00	909.00	921.00	9.43	0.82	0.77
4*	1200.00	1196.38	1196.00	1190.00	1202.00	9.94	-0.30	-0.33
5	1493.00	1482.26	1482.00	1475.00	1488.00	11.37	-0.72	-0.74
6*	1789.00	1784.28	1783.00	1777.00	1790.00	10.56	-0.26	-0.34
7	2193.00	2189.64	2189.00	2182.00	2196.00	11.23	-0.15	-0.18
8*	2391.00	2393.29	2393.00	2386.00	2399.00	11.59	0.10	0.08
9	2695.00	2687.97	2688.00	2680.00	2696.00	13.32	-0.26	-0.26
10	3286.00	3287.78	3287.00	3280.00	3294.00	12.84	0.05	0.03
11*	3585.00	3593.21	3592.00	3584.00	3600.00	13.49	0.23	0.20
12	3902.00	3904.35	3904.00	3896.00	3911.00	12.65	0.06	0.05
13	4272.00	4285.42	4284.00	4277.00	4292.50	13.31	0.31	0.28
14*	4681.00	4696.76	4696.00	4689.00	4703.50	12.96	0.34	0.32
15	5071.00	5086.09	5085.00	5078.00	5093.00	12.54	0.30	0.28
16	5574.00	5587.33	5587.00	5580.00	5594.00	12.64	0.24	0.23
17*	6200.00	6219.38	6218.00	6211.00	6226.00	13.14	0.31	0.29
18	6810.00	6839.57	6839.00	6831.00	6846.00	13.61	0.43	0.43

A visual metrological analysis expands upon the tabulated statistical data, providing a comprehensive evaluation of the calibrated hardware (Figure 5.9). Panel A correlates the measured impedance (y-axis) with the physical multimeter reference (x-axis). The empirical data, comprising both the calibration set (blue markers) and the independent validation set (magenta markers), align with the ideal reference line ($Y = X$). All absolute measurements remain confined within the expanding $\pm 5\%$ tolerance band. Panel B translates this absolute deviation into a relative percentage error, standardizing the scale across the entire functional range. The vertical error bars represent the relative standard deviation, derived by normalizing the absolute analog noise over the physical reference value ($\sigma_{\%} = \frac{\sigma}{X_{\text{ref}}} \times 100$). The plot confirms that all measured mean values and their associated noise boundaries remain strictly within the $\pm 5\%$ limit. A global mathematical evaluation extracts two primary performance metrics from the complete dataset: the Root Mean Square Error (RMSE) and the Mean Absolute Percentage Error (MAPE). The RMSE calculates

the absolute systemic deviation, yielding a final value of 12.91 Ω. The formula is:

$$\text{RMSE} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(\mu_i - X_{\text{ref},i})^2}$$

where N represents the total number of tested components, μ_i the measured mean, and $X_{\text{ref},i}$ the physical multimeter reference. This metric defines the physical magnitude of the residual error in Ohms. The MAPE quantifies the relative accuracy of the system, resulting in a global value of 0.65%. The corresponding formula is:

$$\text{MAPE} = \frac{1}{N}\sum_{i=1}^{N}\left|\frac{\mu_i - X_{\text{ref},i}}{X_{\text{ref},i}}\right| \times 100$$

This calculation confirms a 0.65% global average deviation, validating the efficacy of the implemented linear firmware correction across both the fitting and the validation datasets.

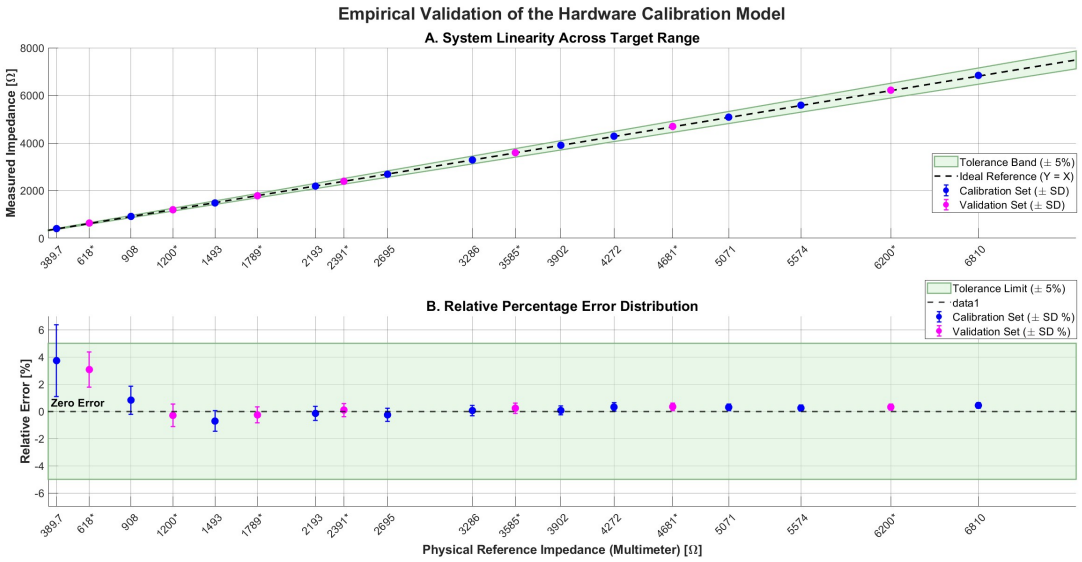


Figure 5.9: Dual-panel metrological validation of the calibrated hardware system. Blue markers denote the original polynomial fitting set, while magenta markers indicate the independent validation set. a) Absolute linear correlation between the measured impedance and the physical reference, featuring a ±5% tolerance band expanding in proportion to the resistance magnitude. b) Relative percentage error distribution, confirming all empirical data points and their associated relative standard deviation boundaries remain constrained within the constant ±5% limit.

An additional analysis was performed to estimate the statistical dispersion of the acquired samples through boxplots (Figure 5.10). The obtained values, the

median and quartiles, are directly compared to the physical reference point. Plotting absolute impedance values on a macroscopic y-axis compresses the distance between the quartiles, obscuring the graphical representation of the data. This scale gap was corrected by subtracting the physical reference point from the median and quartiles. This centers the ideal measurement at 0 Ω and makes the y-axis an absolute deviation scale. The resulting boxplots show the systematic offset and measurement noise. The horizontal line inside each box indicates the median deviation from the baseline. In the low and medium impedance regions, the medians alternate near the zero line. The high-impedance region exhibits a gradual positive drift, reaching a maximum median deviation of +30 Ω at the 6810 Ω target. This absolute deviation remains bounded within the 5% tolerance limit. The uniform height of the interquartile boxes confirms a stable analog noise profile across the entire operative range.

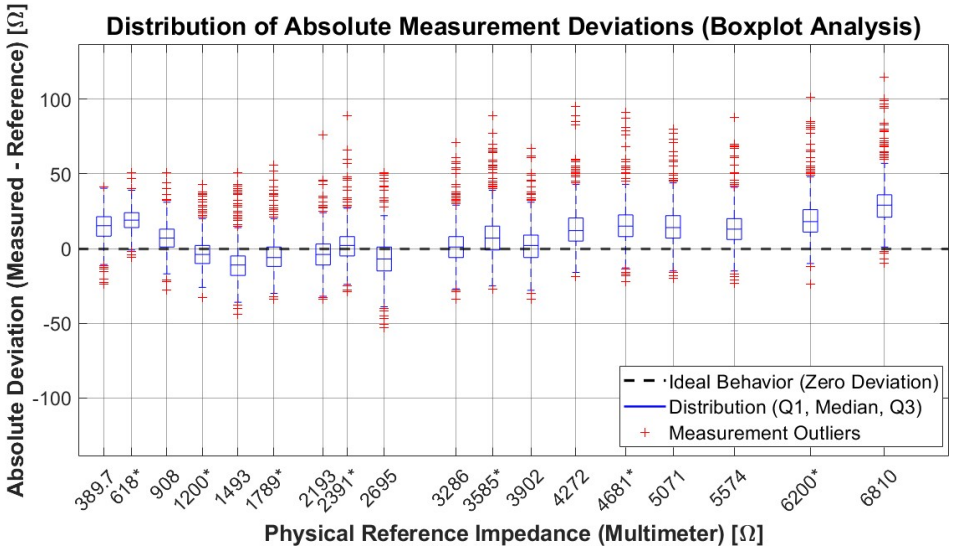


Figure 5.10: Boxplot of absolute measurement deviation. The graph shows absolute error of the collected samples against the physical reference baseline. The horizontal dashed line is the ideal zero deviation point of the experiment. Blue boxes indicate the interquartile range and the median offset, while red crosses indicate the outliers. The horizontal axis is the independent validation data.

All previous impedance analyses used the LTC3246 power supply unit as the primary voltage source. The same process was repeated for all other tested DC-DC converters and LDOs. A total of 1000 consecutive acquisitions per resistance were performed for all components along the impedance spectrum, and the mean value and the relative mean error were calculated. A further parameter was considered, consisting of the percentage difference between the tested module and the

original LTC3246. Figure 5.11 shows the results. At the lowest impedance boundary (618 Ω), all components exhibit their maximum relative mean error, reaching 4.31% for the AZ1117CH device. For target resistances equal to or greater than 1200 Ω, the relative error remains confined within a ±0.61% threshold across all tested units. The performance deviation column shows a maximum 1.21% error at the 618 Ω target. For higher impedance values, the variation with respect to the LTC3246 drops to less than 0.8%, exhibiting multiple negative margin differences. These results demonstrate good systemic accuracy, regardless of the power supply employed.

Component	Validation Point	Physical Reference [Ω]	Mean [Ω]	Relative Mean Error [%]	Deviation vs LTC3246 [%]
LTC3246	1	618	636.9040404	3.058906214	0
	2	1200	1195.872838	-0.343930146	0
	3	1789	1783.620408	-0.300703848	0
	4	2391	2392.420021	0.05939024	0
	5	3585	3592.010277	0.1955447	0
	6	4681	4695.917611	0.318684271	0
	7	6200	6218.282922	0.294885836	0
MCP1253	1	618	643.7182096	4.161522583	1.069889454
	2	1200	1197.991718	-0.167356798	0.177182733
	3	1789	1785.242902	-0.210011056	0.090966331
	4	2391	2395.14375	0.173306148	0.113848293
	5	3585	3594.24456	0.257867771	0.062201439
	6	4681	4701.547071	0.438946189	0.11987988
	7	6200	6208.009434	0.129184419	-0.165214224
MagI3C	1	618	643.5137615	4.128440367	1.037789156
	2	1200	1205.009278	0.417439863	0.763997627
	3	1789	1786.778947	-0.12415051	0.177085841
	4	2391	2395.809626	0.201155402	0.141681018
	5	3585	3596.199148	0.312389066	0.116616329
	6	4681	4697.278742	0.347762057	0.028985414
	7	6200	6201.888179	0.030454499	-0.263653859
AZ1117CH	1	618	644.6738241	4.316152772	1.219930042
	2	1200	1195.328512	-0.389290634	-0.045517035
	3	1789	1778.07837	-0.610487987	-0.310718482
	4	2391	2386.068421	-0.206255916	-0.265488482
	5	3585	3579.8451	-0.143790792	-0.338673234
	6	4681	4707.17616	0.559200178	0.239751856
	7	6200	6194.041009	-0.096112751	-0.389848977

Figure 5.11: Comparative statistical evaluation of the four power supply units. The figure reports the empirical mean, the relative mean error against the physical multimeter reference, and the percentage deviation compared against the primary LTC3246 baseline across seven validation points.

5.2 Test PNT

5.2.1 Electro-electrolyte voltage drop

The first test of the PNT was to assess the voltage drop at the analog electrode-electrolyte interface. A Keithley 3390 waveform generator was used to generate an input sinusoidal 2 Vpp signal at 1 kHz of frequency. Coaxial cables routed the stimulus through the dedicated input SMA connectors on the PCB. As shown in Figure 5.12, a Rigol MSO5104 oscilloscope captured the resulting signal via the

output SMA terminals.



Figure 5.12: Physical instrument configuration featuring the Keithley 3390 arbitrary waveform generator, the Rigol MSO5104 oscilloscope, and the custom PNT board connected via SMA coaxial cables.

The schematic configuration positions the input terminal immediately before the primary RC coupling network and the output terminal after the series access resistor (Figure 5.13). This specific node placement captures the combined impedance of the electrode-electrolyte interface and the adjacent tissue spreading resistance. Measuring this total voltage drop accurately simulates the macroscopic electrical behavior of physical neural interfaces, where the capacitive double layer and the electrolyte access resistance remain physically inseparable from the perspective of the external recording amplifier.

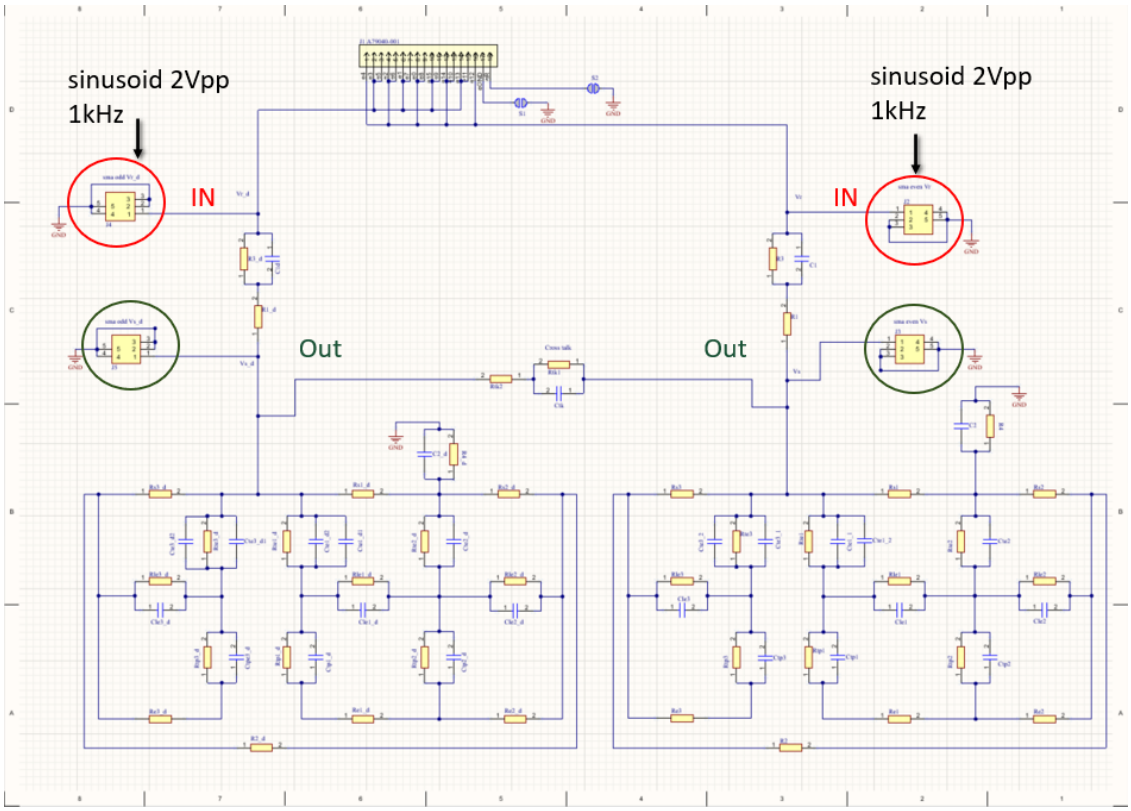


Figure 5.13: Corresponding PNT circuit diagram. Red annotations identify the input nodes for the 1 kHz, 2 Vpp sinusoidal stimulus, and green annotations identify the output measurement nodes located immediately after the series access resistor (R_{acc}).

The experiment was previously performed in the LTspice environment using an ideal voltage source. The output result was 1.367 Vpp with a theoretical voltage drop of 31.65%. At the physical level, this voltage drop models the physiological filtering effect of the neural interface: the double-layer capacitance and spreading resistance dissipate a portion of the stimulation energy before it reaches the nerve tissues. The hardware test produced the empirical waveforms visible on the oscilloscope (Figure 5.14). The cyan trace of Channel 2 represents the even channels and recorded an output amplitude of 1.478 Vpp. The magenta trace of Channel 3 represents the odd channels and recorded an output amplitude of 1.436 Vpp. These empirical values exhibit a positive voltage deviation from the theoretical LTspice model, recording an 8.12% difference for the even channels and a 5.05% difference for the odd channels.

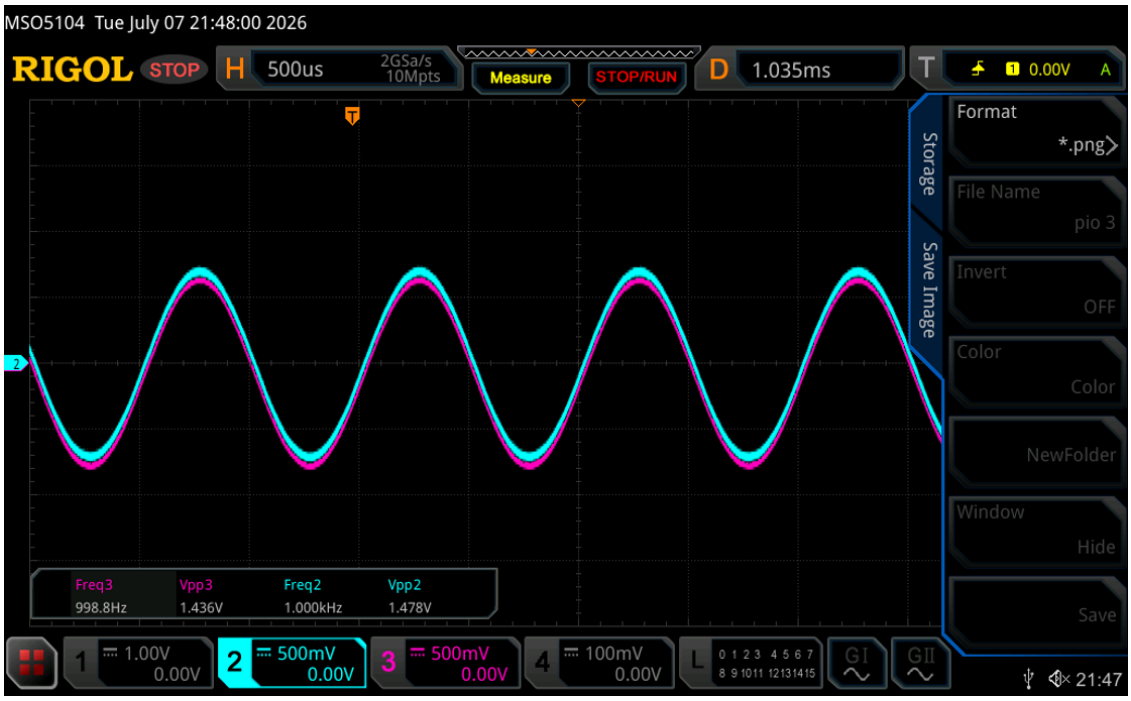
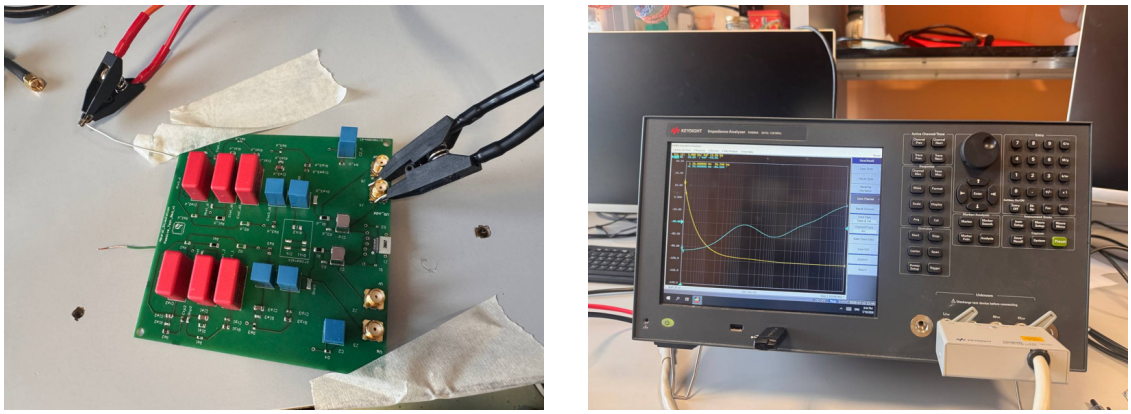


Figure 5.14: Oscilloscope capture of the experimental voltage drop. The cyan waveform (Channel 2) represents the even channels and its output is 1.478 Vpp. The magenta waveform (Channel 3) represents the odd channels, and its output is 1.436 Vpp. These measurements are indicative of the voltage loss of the initial 2 Vpp, 1 kHz sinusoidal stimulus in the hardware interface.

5.2.2 Impedence test

A frequency response analysis was conducted on the macroscopic impedance profile of a PNT circuit. The measurement setup consisted of a Keysight E4990A Impedance Analyzer connected to the PCB by a Keysight 16089B Kelvin Clip Lead (Figure 5.15). The instrument performed a logarithmic frequency sweep from 20 Hz, which is the operating limit of the analyzer, to 1 MHz, acquiring 1601 discrete data points. This provided the empirical Bode plot for comparison with the theoretical LTspice simulation for both the odd and the even channels.



(a) (b)

Figure 5.15: Frequency response measurement setup. **(a)** PNT board connected via the Keysight 16089B Kelvin Clip Lead to the designated SMA input and output terminals. **(b)** The Keysight E4990A Impedance Analyzer executing the logarithmic frequency sweep from 20 Hz to 1 MHz across 1601 data points.

The Bode plots from the analyzer data were generated through MATLAB (Figure 5.16), and the even channels are compared to the odd channels for magnitude and phase. The curves present an overlapping trend, confirming that the electrical response is the same for both paths. The macroscopic magnitude profile highlights a dominant capacitive behavior in the low-frequency spectrum with a steep descent up to the 1 kHz physiological band, recording an impedance of 1317 Ω. Beyond this point, the magnitude continues to drop, approaching a purely resistive plateau in the high-frequency range, with a measurement in the order of 100 Ω. The phase diagram also demonstrates this transition. In the first region of low frequency, the phase angle is $-86°$, rising to $-41.9°$ at 1 kHz and reaching $0°$ at 1 MHz.

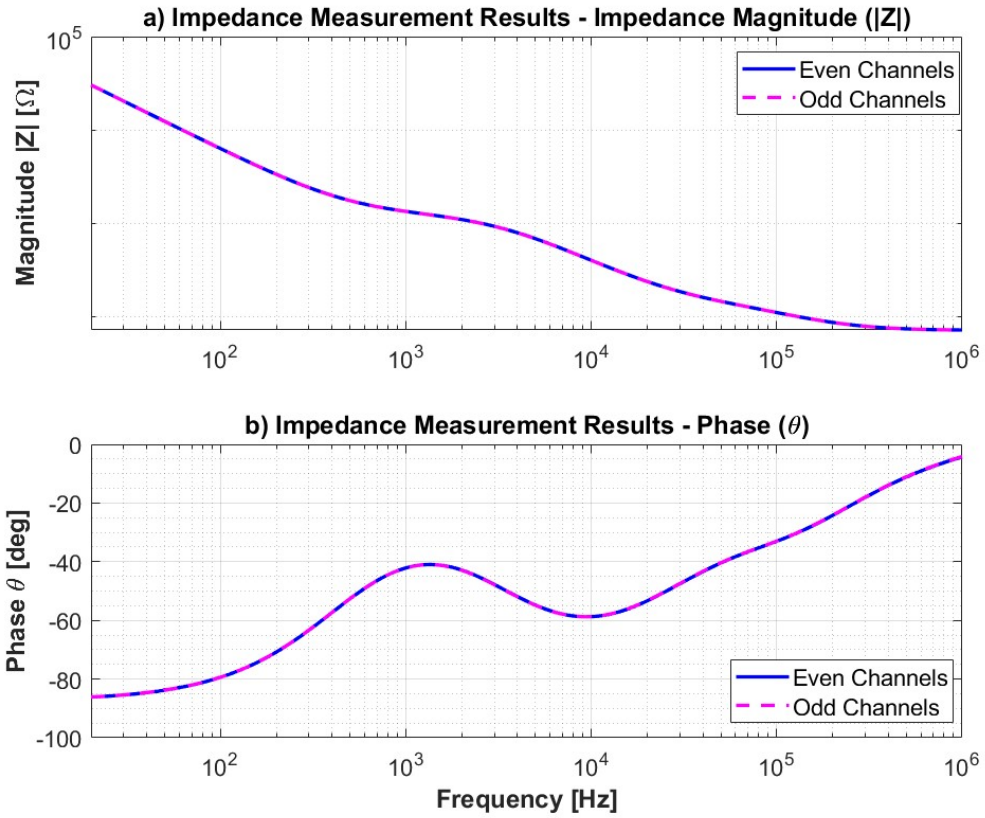


Figure 5.16: Bode plots of the PNT impedance profile of even channels (blue solid line) and odd channels (magenta dashed line) in the 20 Hz - 1 MHz range. (a) Impedance magnitude (|Z|) profile, highlighting the transition from a high-capacitive region towards a low-resistive plateau. (b) Phase angle (θ) profile, corroborating the capacitive-to-resistive transition as the measurement approaches zero degrees at high frequencies.

This macroscopic behavior demonstrates direct consistency with the theoretical Three-Section Circuit diagram detailed in Chapter 4.3. A quantitative analysis evaluated the magnitude percentage error and the absolute phase deviation between the empirical hardware measurements and the Three-Section Circuit LTspice simulation. As shown in Figure 5.17 from 20 Hz up to 10^5 Hz, the magnitude percentage error is within a $\pm 1\%$ limit, and the absolute phase deviation maintains a strict boundary of $\pm 1°$. A divergence appears in the high-frequency spectrum starting at the 100 kHz range. At the 1 MHz range, the magnitude error reaches a maximum negative deviation of 2%, and the absolute phase error approaches a positive 2° variation. An identical methodology evaluated the empirical PNT measurements against the comprehensive Five-Section Circuit theoretical model. The

graphical representation (Figure 5.18) details this comparative analysis. The magnitude percentage error registers a +1% initial offset at the lowest boundary. Across the subsequent spectrum up to the 10^5 Hz mark, the deviation oscillates within a ±1% limit. Beyond this threshold, the magnitude error exhibits a negative trend, reaching a -5% peak at the 1 MHz upper boundary. The absolute phase deviation maintains a near-zero profile up to 10^4 Hz. In the higher frequency decades, the phase curve dips towards a -1° margin before reversing trajectory, culminating in a +2° overestimation at 1 MHz.

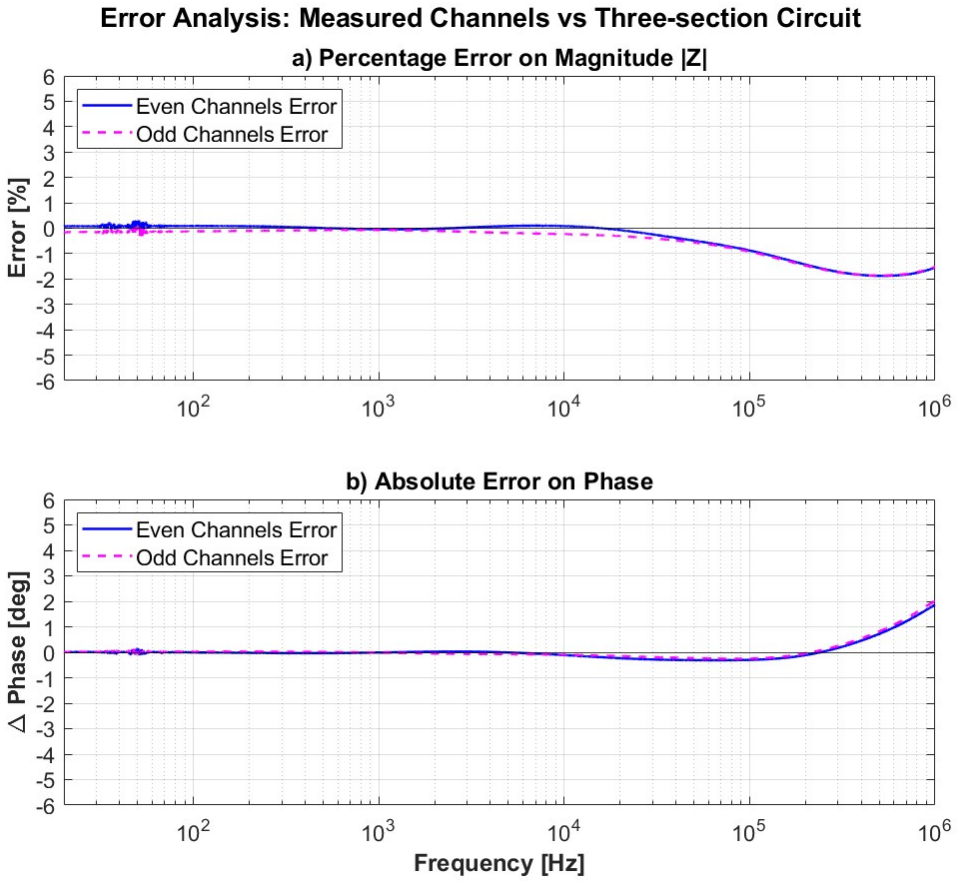


Figure 5.17: Error analysis comparing the empirical PNT measurements the theoretical Three Section Circuit simulation. (a) Percentage error on the impedance magnitude, which is bounded by a ± 1% limit for frequencies up to 100 kHz and a -2% maximum at 1 MHz. (b) absolute error on the phase angle, which is bounded by a ± 1° tolerance on the primary spectrum and a +2° deviation at the upper frequency limit.

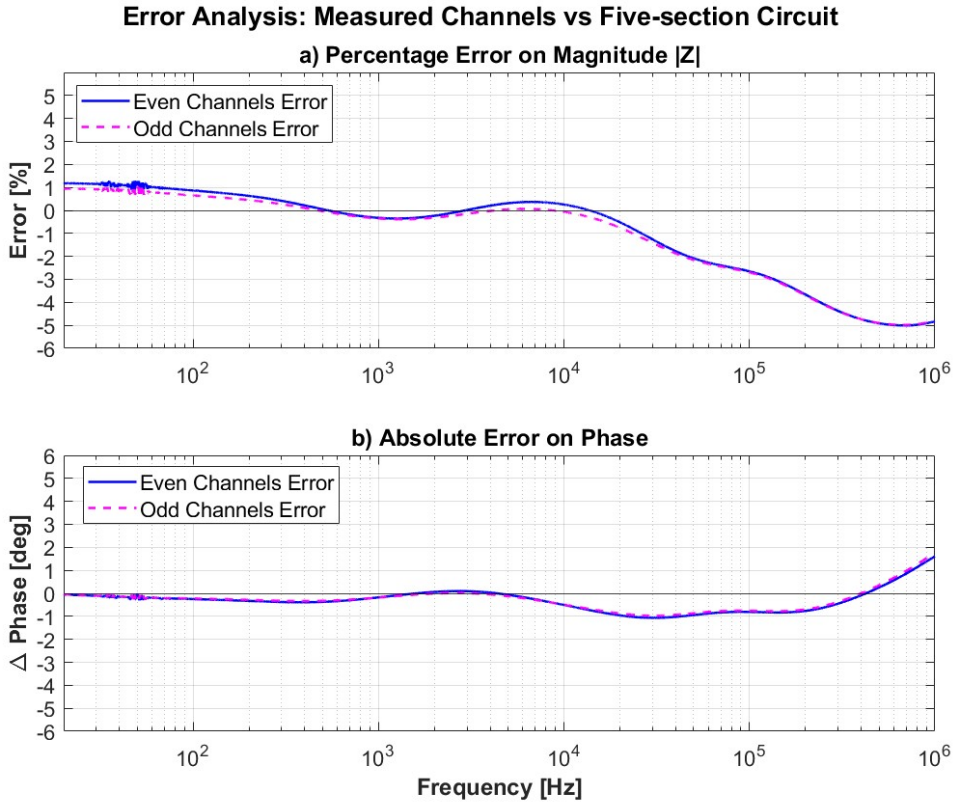


Figure 5.18: Error analysis comparing the empirical PNT measurements with the full Five-Section Circuit theoretical model. (a) Percentage error on the impedance magnitude, which oscillates at ± 1% across the primary spectrum and -5% at 1 MHz. (b) Absolute error of the phase, which is near zero in the low-frequency range and shows +2° divergence at the maximum frequency.

A further impedance analysis with the Keysight E4990A device was performed, isolating the biological nerve tissue circuit on the PNT, bypassing capacitive and resistive components modeling the electrode-electrolyte interface. The aim was to compare the experimental results directly with the theoretical models: the standard Lumped Parameter Circuit, the Simplified Parameter Circuit, and the main COMSOL multiphysics model from Chapter 4.2 (Figure 5.19).

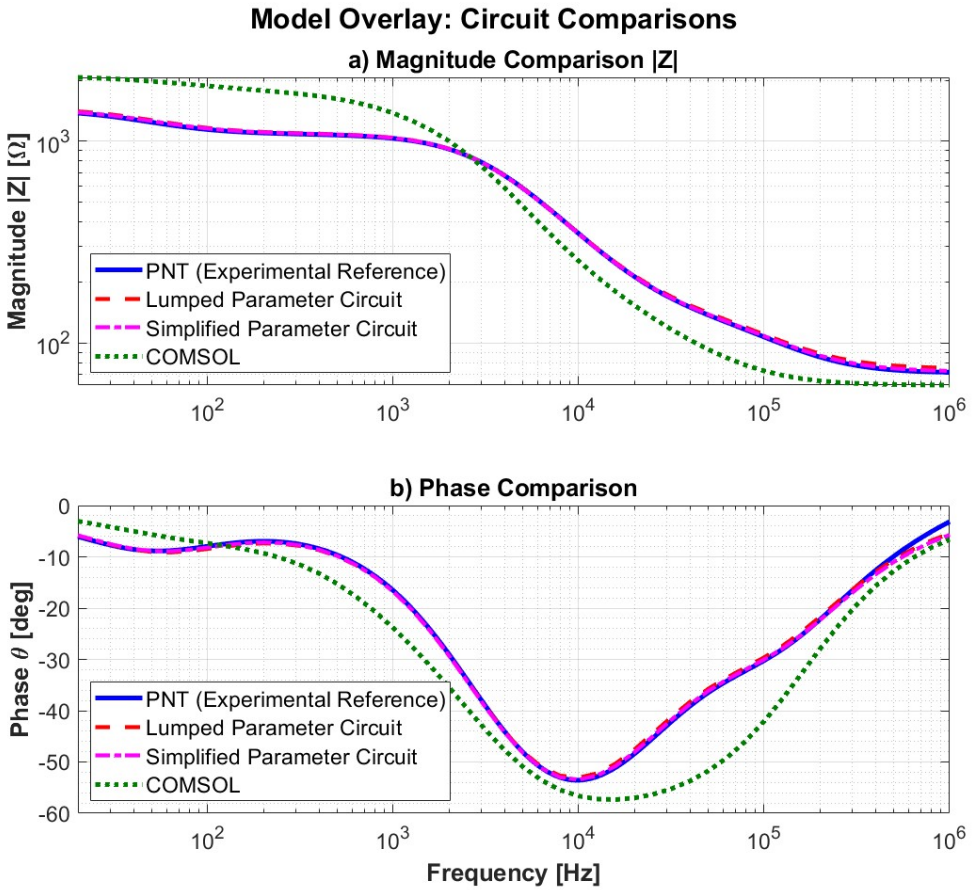


Figure 5.19: Bode plot overlay of the isolated nerve tissue models. The graph displays the empirical PNT reference (blue solid line), the Lumped Parameter Circuit (red dashed line), the Simplified Parameter Circuit (magenta dashed line), and the COMSOL baseline (green dotted line). (a) Impedance magnitude |Z| comparison. (b) Phase angle θ comparison.

The bar chart (Figure 5.20) details the error distribution across five discrete frequency decades. The 10 kHz evaluation point records a 0.3% magnitude error for both comparative models, alongside an absolute phase error below 0.5°. Outside this central band, the Simplified Parameter Circuit yields lower magnitude errors. At 100 Hz, the standard lumped circuit records a 1.7% deviation, whereas the simplified alternative maintains a 1.1% boundary. At the 100 kHz node, the magnitude deviation reaches 2.8% for the lumped model and 1.1 for the simplified model. This performance discrepancy aligns with the physical board architecture. The PNT hardware replicates the component topology of the Simplified Parameter Circuit. At the 1 MHz upper limit, the magnitude error peaks at 4.7% against the standard lumped model and 1.5% against the simplified reference. The phase

diagram displays peak deviations at this identical frequency, recording 2.3° for the lumped circuit and 2.6° for the simplified reference. A final analysis evaluated the PNT hardware against the COMSOL model (Figure 5.21). The magnitude error fluctuates across the frequency range. It starts at 39.2% at 100 Hz, decreases at 1 kHz (25.1%), and reaches a 47.3% peak at 100 kHz. At 1 MHz, the discrepancy drops to 15.9%. The phase error follows a similar pattern. It maintains minimal values at the spectrum boundaries, recording 0.6° at 100 Hz and 3.5° at 1 MHz. The maximum phase divergence occurs at the 100 kHz node, registering an 11.9° discrepancy.

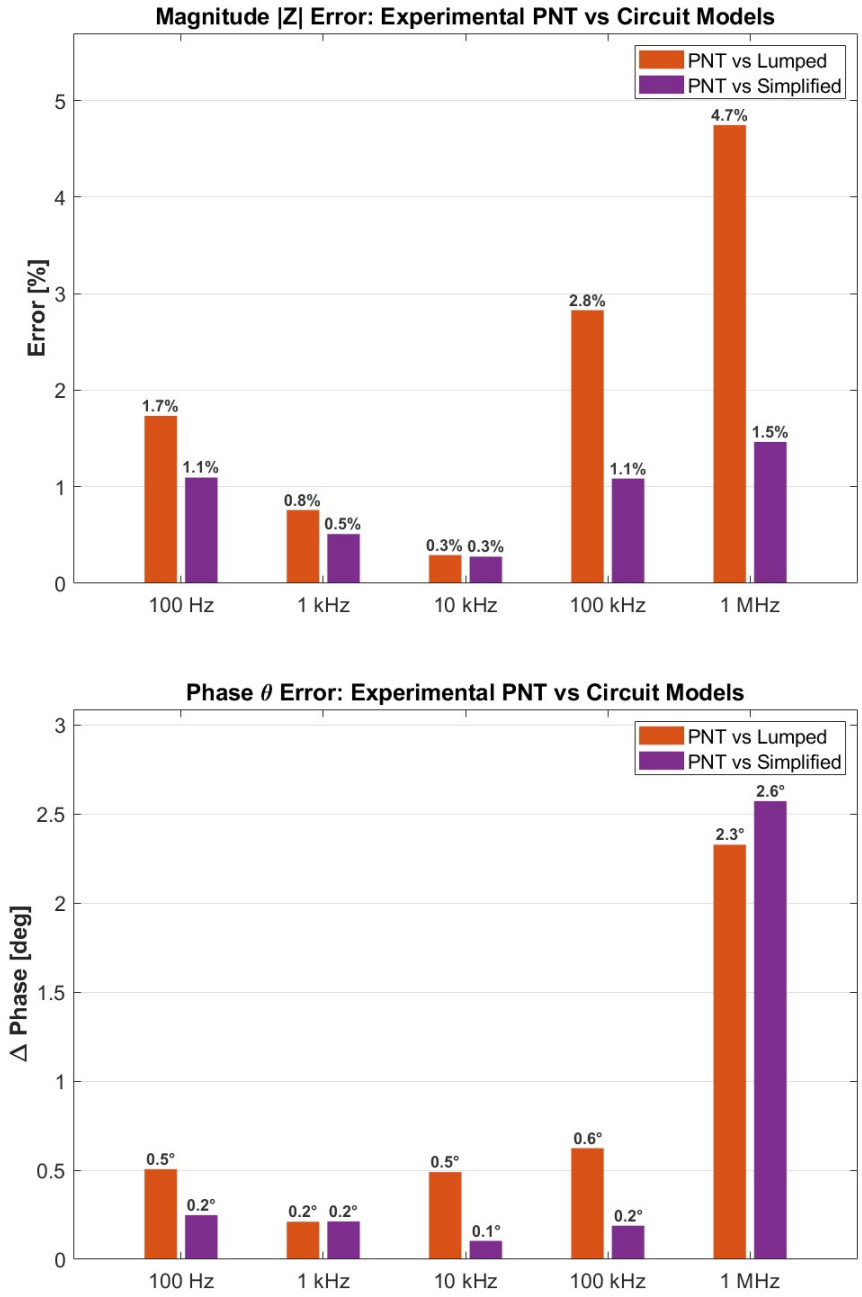


Figure 5.20: Error distribution between the experimental PNT hardware and the mathematical circuit models. The orange bars indicate the deviation from the standard Lumped Parameter Circuit. The purple bars indicate the deviation from the Simplified Parameter Circuit. (a) Magnitude percentage error. (b) Absolute phase error.

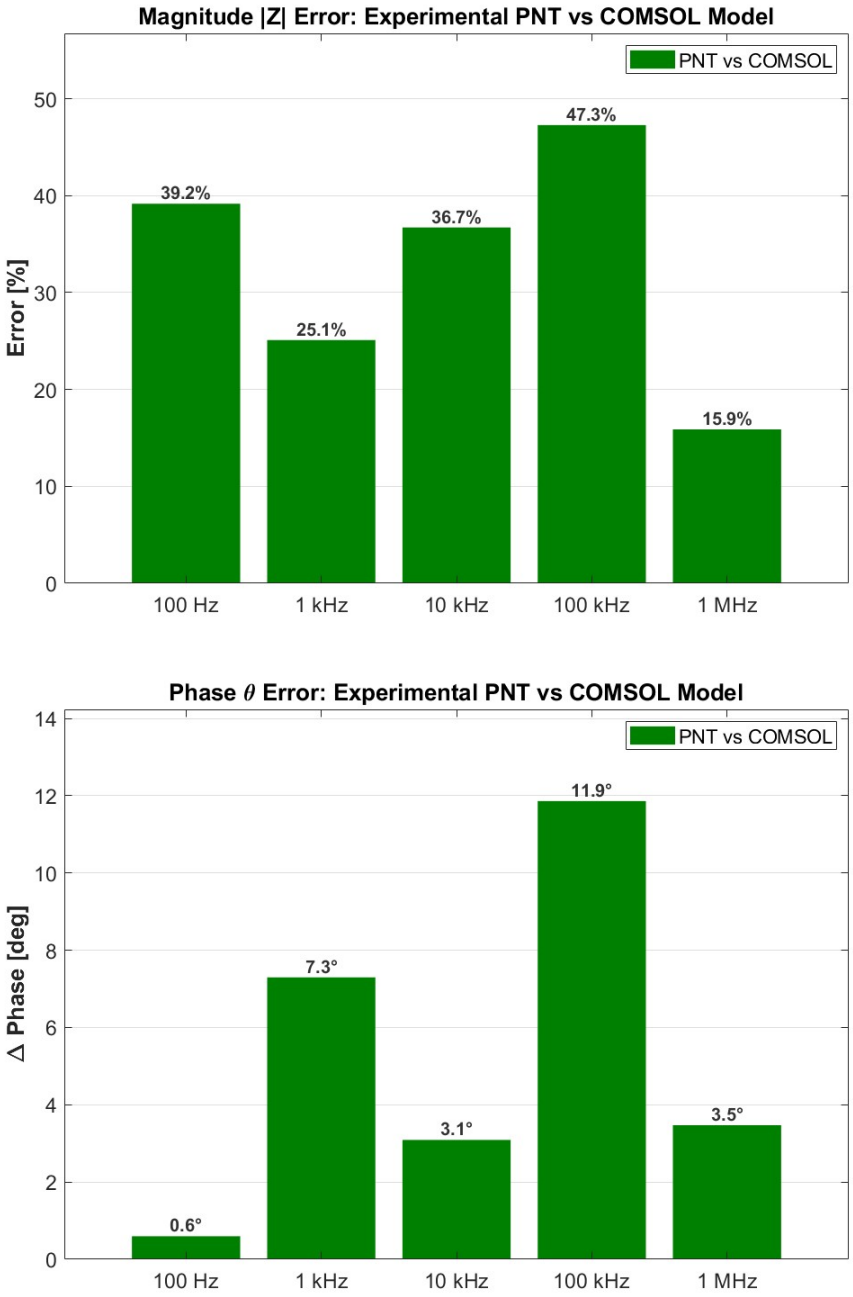


Figure 5.21: Discrete error distribution between the experimental PNT hardware and the COMSOL model. (a) Magnitude percentage error across five frequency nodes.(b) Absolute phase error.

5.3 Comprehensive test bench

5.3.1 Impedance check on the PNT

The whole system of both custom PCBs was tested. The hardware configuration integrated the shield with the Intan RHD2132 headstage, which is connected to the PNT board through the 18-pin Omnetics connector (Figure 5.22). The impedance check test was performed following the procedure detailed in section 5.1.2. This test tried to replicate the clinical procedure impedance check to verify the optimal implantation of the electrode. The RHD chip measured the systemic impedance across the artificial interface and verified the whole measurement chain.

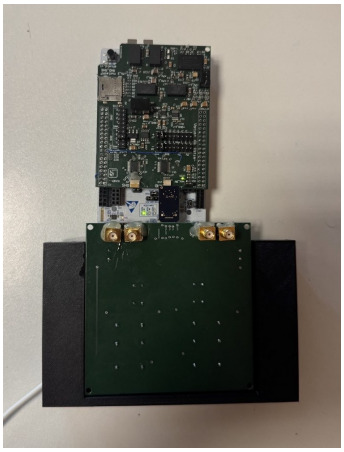


Figure 5.22: Hardware configuration for the integrated system impedance measurement. The custom Shield board is connected with the Intan RHD2132 headstage. An 8-channel Omnetics connector connects the headstage to a PNT board.

The impedance check produced a median impedance of 1353.0 Ω, which is 1.19% higher than the 1337.0 Ω value extracted using the impedance analyzer in Section 5.2.2. Figure 5.23 shows the statistical boxplot of the PNT impedance curve at the 1 kHz frequency node. The data distribution has a 1242 Ω minimum whisker boundary and a 1448 Ω maximum whisker boundary with no outliers.

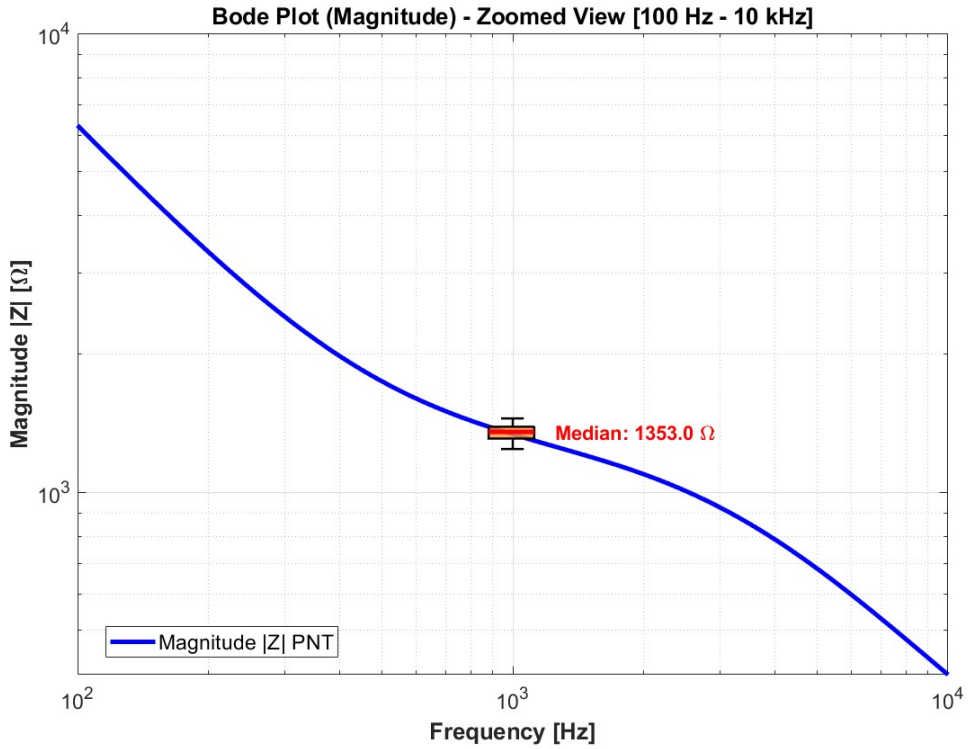


Figure 5.23: Zoomed Bode magnitude plot of the impedance check results at 1 kHz. The statistical boxplot is overlaid on the continuous PNT impedance curve. The 1353.0 Ω median is shown with the 1242 Ω minimum and 1448 Ω maximum boundaries.

5.3.2 Stimulation Test

A stimulation test involving the RHS system and the PNT hardware platform (Figure 5.24) was performed. The experimental setup comprises the STM32 Nucleo microcontroller equipped with the Shield connected to the RHD2132 headstage, providing the stimulation and the supply voltages. The Omnetics 18-channel connector established the physical link between the RHS headstage and the PNT board to stimulate the circuit. Firmware execution within the microcontroller generates the stimulation pulse. Coaxial cables link the board SMA connectors to a Rigol MSO5104 digital oscilloscope, enabling acquisition of the system voltage response downstream of the stimulation chip.

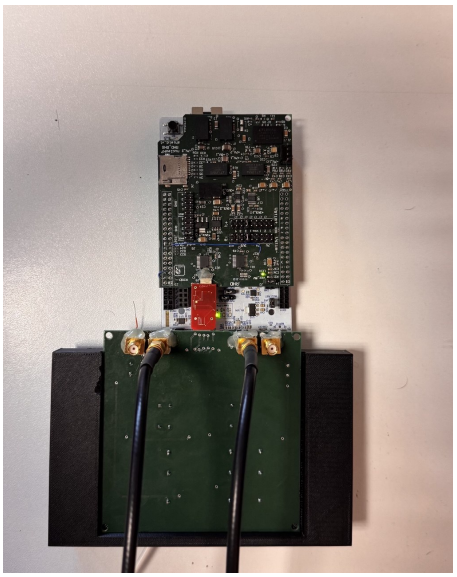


Figure 5.24: Experimental hardware configuration for the RHS stimulation test. Assembly of Shield, Nucleo microcontroller and RHS2116 headstage linked to PNT board via an 18-channel Omnetics connector. Coaxial cables connect the SMA interfaces to an oscilloscope for input voltage acquisition.

The experimental protocol used three different stimulus waveforms. All three variants are biphasic square waves featuring a 150 µs inter-phase delay between the positive and negative pulses:

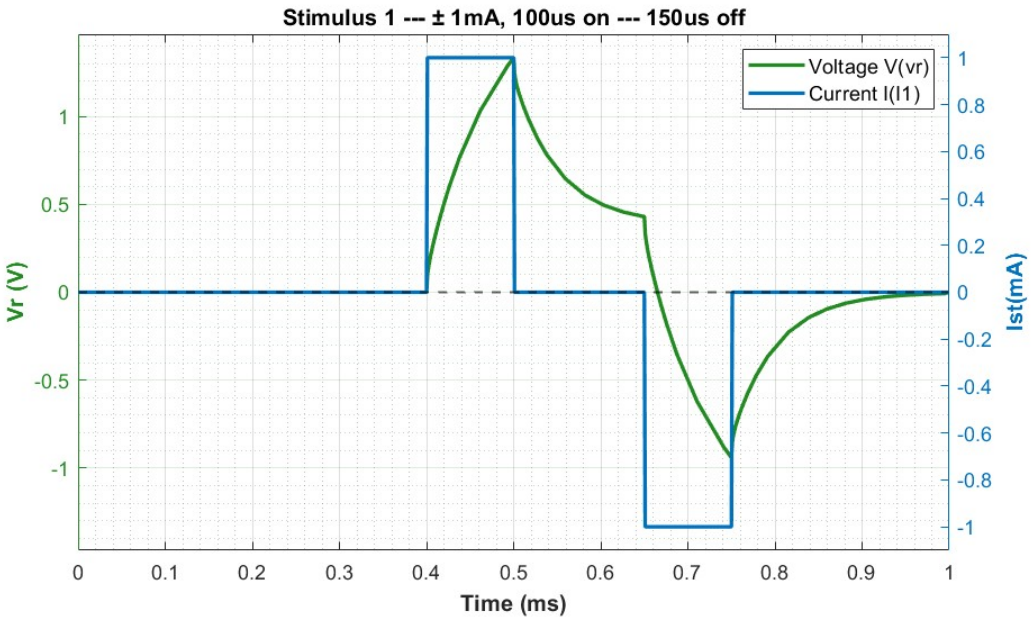
- **Stimulus 1:** ±1 mA amplitude, 100 μs duration per phase.
- **Stimulus 2:** ±1 mA amplitude, 500 μs duration per phase.
- **Stimulus 3:** ±2 mA amplitude, 100 μs duration per phase.

The method involves LTspice simulations of all three stimuli. The simulation was carried out using the three-section circuit described in chapter 4.2, with an ideal

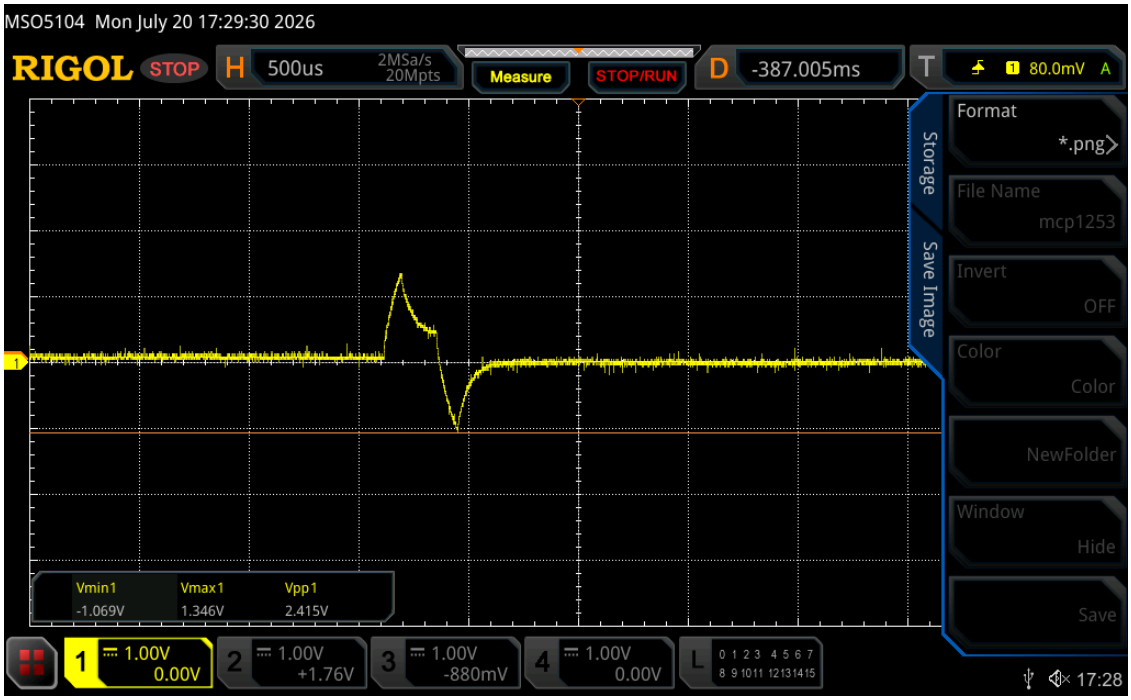
current source, and the waveforms are compared to the physical voltage responses observed on the oscilloscope.

The physical waveforms obtained on the oscilloscope display a shape comparable to the LTspice simulation profiles. The baseline hardware configuration featuring the MCP1253 regulator provides specific voltage deviation metrics. For the first stimulus, the LTspice model computes a positive peak of 1.3348 V and a negative peak of -0.9413 V (Figure 5.25a). The physical acquisition reveals a +0.0112 V variation for the anodic crest and a -0.1277 V variation for the cathodic trough (Figure 5.25b). The second stimulus simulation generates a 3.0198 V positive peak and a -1.0897 V negative peak (Figure 5.26a). The corresponding physical test yields a -0.0898 V discrepancy on the positive front and a -0.3353 V discrepancy on the negative front (Figure 5.26b). The third stimulus computational profile presents a 2.6823 V positive maximum and a -1.8882 V negative minimum (Figure 5.27a). The hardware evaluation demonstrates a deviation of -0.3463 V during the anodic phase and a deviation of +0.0672 V during the cathodic phase (Figure 5.27b). The hardware configuration with Würth Elektronik MagI^{3}C 173950336 power module was the worst-case scenario for Stimulus 3. The physical oscilloscope measurement presented a maximum value of 2.296 V and a minimum value of -1.663 V, with a -0.3863 V deviation on the positive side and a +0.2252 V deviation on the negative side, collectively showing an error of 13.4% in the peak-to-peak output voltage relative to the model simulated in LTspice.

A final test has been performed with Stimulus 1 during a temporal window of 2.86 s at a 24 Hz frequency (Figure 5.28a). It's possible to observe from Figure 5.28b the delay of 41.8 ms between two consecutive peaks, confirming the system's capacity to deliver physiological stimulation throughout that interval.

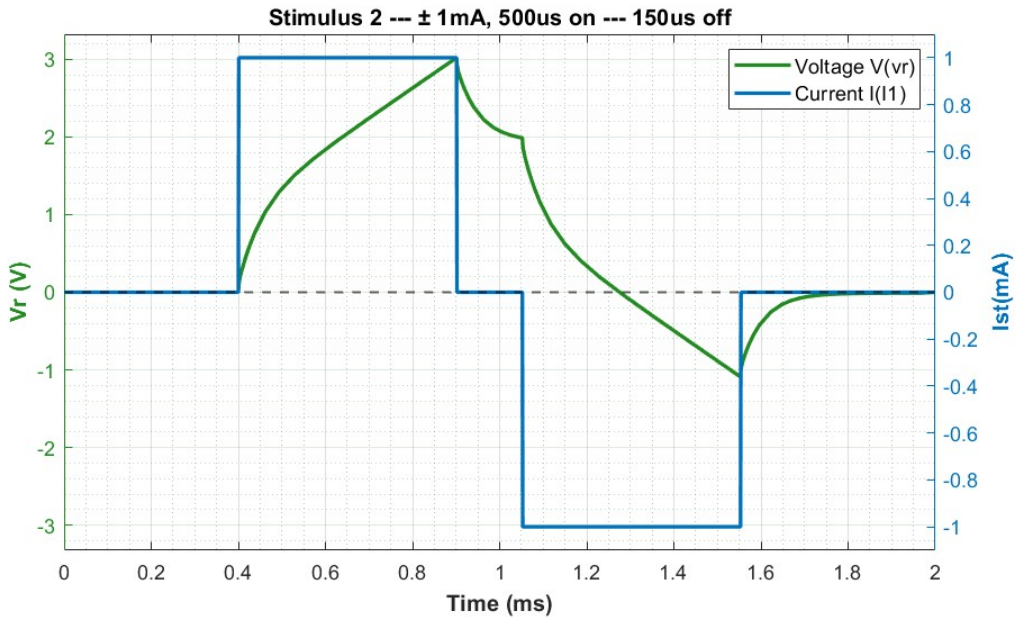


(a)

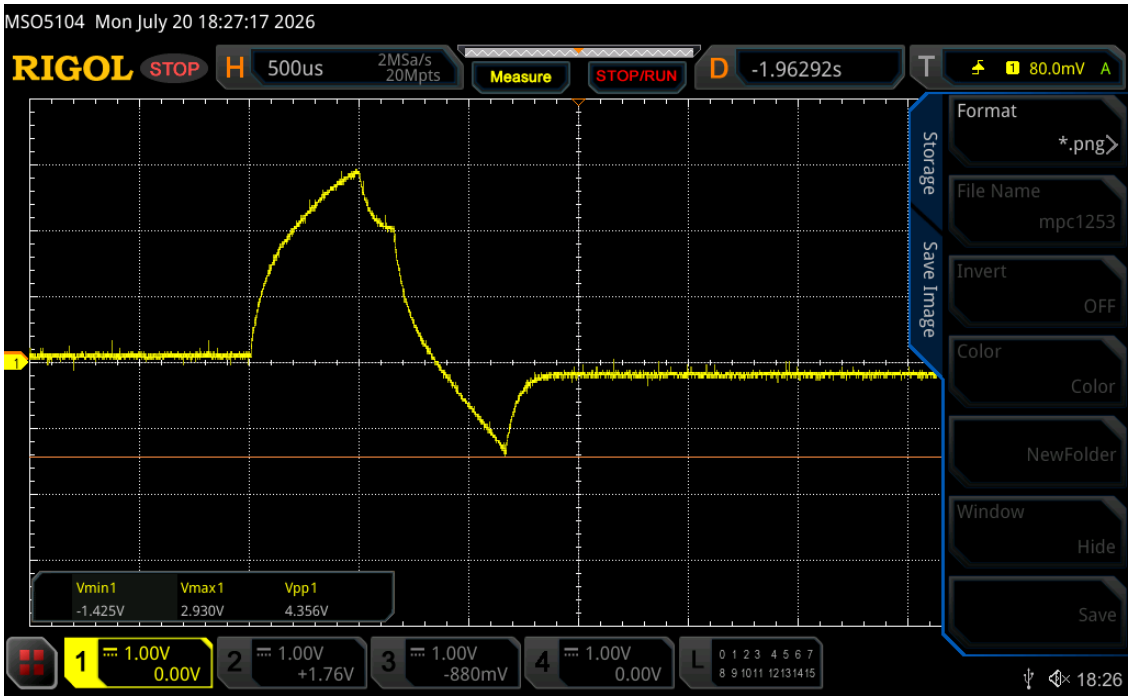


(b)

Figure 5.25: Theoretical and physical voltage responses for Stimulus 1. (a) LTspice computational model generates a positive peak of 1.3348 V and a negative peak of -0.9413 V. (b) Oscilloscope measurement with a positive peak of 1.346 V and a negative peak of -1.069 V, with an anodic deviation of +0.0112 V and a cathodic deviation of -0.1277 V

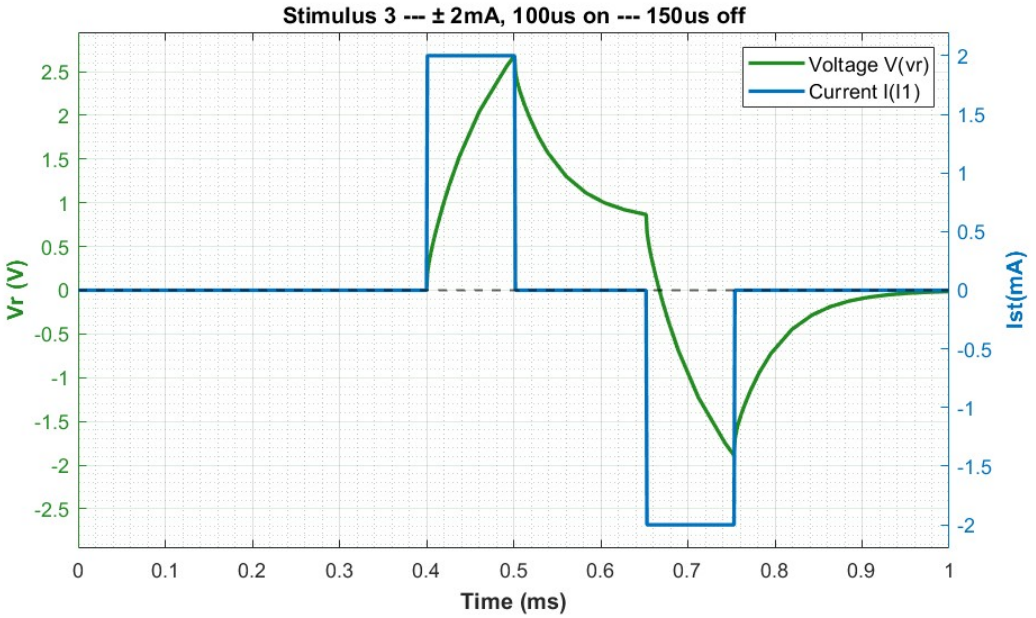


(a)

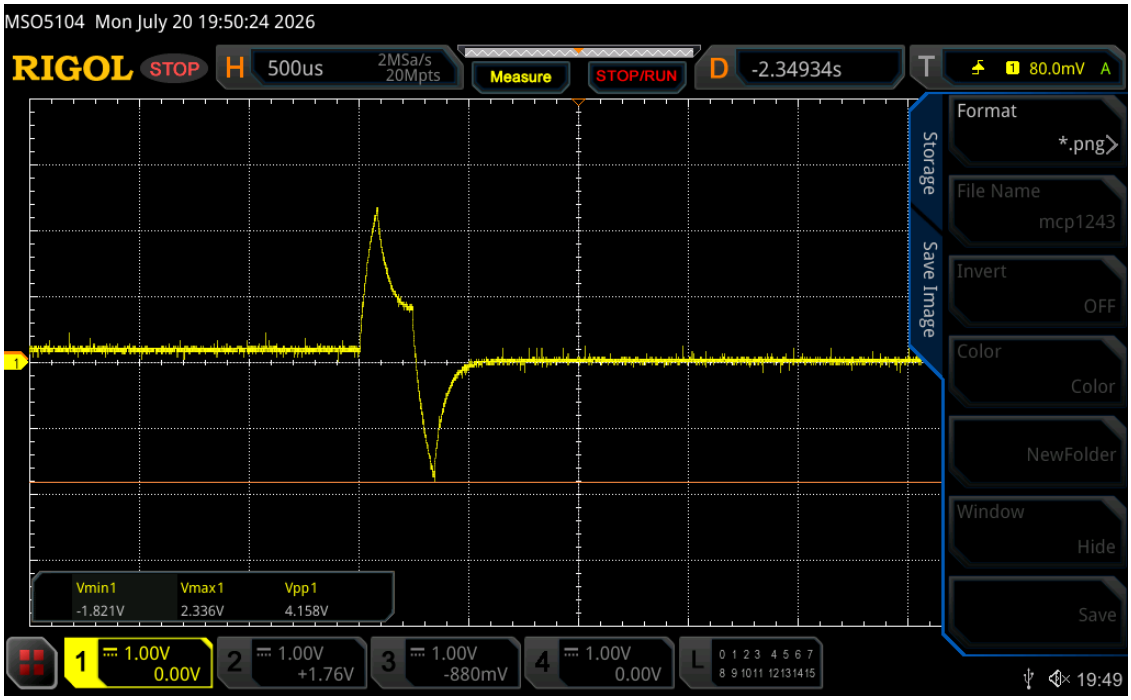


(b)

Figure 5.26: Theoretical and physical voltage responses for Stimulus 2. (a) The LTspice computational model has a positive peak of 3.0198 V with a negative peak of -1.0897 V. (b) Oscilloscope measurement with a positive peak of 2.930 V and a negative peak of -1.425 V. The physical hardware has an anodic deviation of -0.0898 V and a cathodic deviation of -0.3353 V.

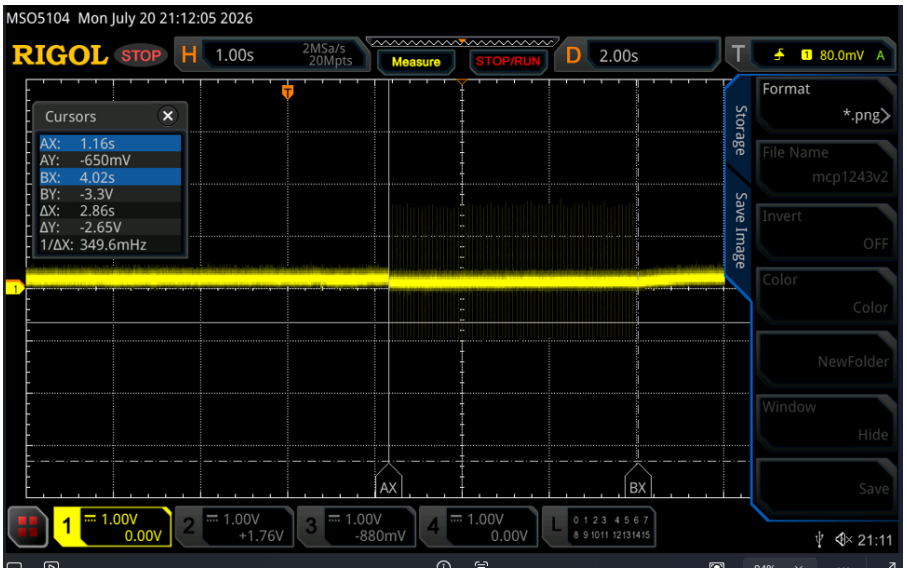


(a)



(b)

Figure 5.27: Theoretical and physical voltage responses for Stimulus 3. (a) LTspice computational model with a positive peak of 2.6823 V and a negative peak of -1.8882 V. (b) Oscilloscope with a positive peak of 2.336 V and a negative peak of -1.821 V. The physical hardware has an anodic deviation of -0.3463 V and a cathodic deviation of +0.0672 V.



(a)



(b)

Figure 5.28: (a)Oscilloscope acquisition displaying a pulse train for Stimulus 1 generated at a frequency of 24 Hz. (b)Oscilloscope detail view showing a 41.8 ms interval between consecutive stimulation peaks.

5.4 Discussion of the result

The mathematical calculation confirms that the capacitive response of the 10 pF series capacitor forces the internal voltage generator into a near-ideal AC source configuration. In fact, as shown in Table 5.1, the manufacturer's current equation produces a calculation error of 10^{-6}%, demonstrating that the actual measurement errors are caused by physical analog baseline offsets and hardware noise. The linear regression model embedded in the STM32 firmware resolves these technical errors. The first raw data have a non-uniform offset (Figure 5.6). The first-degree polynomial correction in Figure 5.8 aligns these digital data with the reference multimeter data, resulting in the mean absolute percentage error (MAPE) of 0.65% and the root mean square error (RMSE) of 12.91 Ω, confirming the correct tuning of the real-time firmware calibration across the target peripheral nerve spectrum. The results obtained from the resistor not used for the calibration establish the reliability of the measurements, as all calibrated mean values and their associated relative standard deviation boundaries remain constrained within a ±5% tolerance limit, as shown in Figure 5.9. This 5% threshold carries physical significance, matching the intrinsic 5% manufacturing tolerance of the discrete components integrated into the PNT hardware platform. The integrated system evaluation on the PNT board in Chapter 5.3.1 confirms this metrological alignment. Replicating the standard clinical impedance check at 1kHz, the complete measurement chain produced a median value of 1353.0 Ω with a 1.19% deviation from the expected value (Figure 5.23). Moreover, the constant height of the boxplot illustrated in Figure 5.10 across the measurement spectrum indicates a stable analog noise profile. The RHD headstage impedance check was tested using all four voltage regulation modules in the experimental setup. Excluding the lowest validation boundary, all components have a relative mean error less than 1% against the reference values. In this range, the correlation between cross-component precision and the LTC3246 baseline calibration is less than 1% for all components, and acquisition accuracy remains constant regardless of the power supply topology (Figure 5.11).

The frequency response of the physical PNT hardware is consistent with the theoretical Five-section Circuit and the Three-section Circuit. The quantitative comparison with the simplified three-section LTspice model shows a magnitude error of ±1% and an absolute phase deviation of ±1°. The comparison with the full five-section circuit also shows similar limits, with magnitude changes of ±1%. The biggest deviations occur at the 1 MHz upper boundary, recording a -2% magnitude error for the three-section circuit (Figure 5.17) and -5% for the five-section network (Figure 5.18). These results show that the physical hardware reproduces the simplified parameter circuit architecture, matching the 5% maximum manufacturing tolerance of the board components. This structural fidelity maintains its highest precision within the 100 Hz and 10 kHz operative band, a critical spectrum concentrating 90.32% of the total stimulus signal power calculated in Chapter 4.3.

The PNT impedance, isolated from the electrode-electrolyte portion of the circuit, is then compared to the theoretical analytic model detailed in Chapter 4.2.6. The magnitude errors of the physical hardware against the lumped-parameter five-section network and simplified three-section network are minimal over the entire spectrum (Figure 5.20): 0.8% error for the five-section network and a 0.5% error for the three-section circuit at the 1 kHz physiological node. At the 10 kHz evaluation point, the magnitude error drops to 0.3 for both mathematical models, alongside an absolute phase deviation below 0.5°. The maximum discrepancies emerge at the 1 MHz upper limit, yielding a 4.7% magnitude error for the standard lumped model and a 1.5% variation for the simplified reference. These variations confirm the structural validity of the circuit simplification highlighted in Chapter 4.2.6a and the alignment of the physical board with the simulated circuits. Comparison of the isolated PNT hardware configuration with 3D COMSOL multiphysics model shows larger numerical discrepancies (Figure 5.20). The empirical data show a 39.2% magnitude error in the low-frequency band, a 25.1% deviation at the standard frequency of 1 kHz, and a 47.3% peak in the high-frequency spectrum. The maximum of the absolute phase difference reaches 11.9° in the high-frequency range. These empirical measurements match the theoretical errors evaluated in Chapter 4.2.6 due the conversion of the continuous FEM simulation into a finite 1D lumped parameter. The theoretical model predicted a 38.08% magnitude offset in the low-frequency band, 24.51% deviation at the standard 1 kHz node and 51.57% divergence in high-frequency spectrum. This baseline offset comes from mathematical discretization of the continuous biological volume. The coincidence between the empirical deviations and theoretical calculations shows that the physical hardware matches the LTspice-simulated circuit.

For the stimulation test (Chapter 5.3.2), the physical waveforms recorded on the oscilloscope follow the general profile of the LTspice simulation and show the required time interval between two consecutive peaks (stimulation at 24 Hz). Despite these consistencies, voltage differences could result from different factors such as baseline noise, capacitive effects from the oscilloscope cables, and resistive-capacitive junctions at both Omnetics connectors. Furthermore, the manufacturer declares a 25% tolerance limit for the internal DC amplifiers, basing the chip design on rough waveform monitoring instead of high-precision measurement. In addition, the MagI^{3}C power module exhibits the highest error during the third stimulus because its topology incorporates an integrated inductor that resists sharp current transients, inducing a transient voltage droop on the power rail that starves the system.

Chapter 6

Conclusion

This thesis describes the design and implementation of a custom hardware platform for the validation of the Intan RHS2116 and RHD2132 integrated circuits in the NerveRepack and ReWiRe projects. The custom PCB Shield, for the STM32 Nucleo-H7 microcontroller, includes LVDS transceivers for conversion of single-ended SPI signals, power management architecture for generating 3.3 V logic supplies, and bipolar compliance rails selectable during electrical stimulation protocols. Additionally, the development of the PNT board, which mimics the complex impedance of the human median nerve with a cuff electrode, is detailed in this work. The design involved the 3D FEM simulation in COMSOL Multiphysics and the translation of the electric tissue properties into a lumped-parameter RC network (1D). Empirical EIS data were used to add the electrode-electrolyte interface, approximating the Faradaic charge transfer and double layer capacitance into physical hardware. The connection of the PCB shield, the PNT board, and the Intan headstages forms the comprehensive test bench. This experimental setup replicates the clinical environment, executing impedance measurements, signal acquisitions, and electrical stimulation. The functional evaluation of these neural interface chips relied on the provision of stable power supplies and the preservation of solid SPI communication. In the absence of in vivo or ex vivo models, this setup provides a physiological equivalent test load with a higher degree of physical reality than a simple resistor, in a preliminary experimental phase. The first constraint regards the assumption of frequency-independent nerve tissue properties up to the 10 kHz boundary. Although the scientific literature supports this approximation, the approach creates blind spots regarding the tissue behavior beyond these boundaries. Also, the model developed in COMSOL remains preliminary, keeping the basic architecture of the simulated electrode with only one active contact disc, neglecting the contribution of the cross-talk, which could affect the value of the impedance. Moreover, the model does not take into account the generation of the action potential, which could have a macroscopic repercussion on the impedance trend of the model. This prevents the determination of the sub-threshold or supra-threshold

nature of the stimulus simulated within the COMSOL simulation and hardware experimental environment. At the end, the method in this framework to translate the COMSOL output to a discrete lumped-parameter circuit results in a maximum error of +38.1% within the 100 Hz to 10 kHz bandwidth. The massive physiological variability of the human nerve mitigates the impact of this mathematical deviation. The expected impedance for a peripheral nerve cuff electrode spans between 600 Ω and 5 kΩ. A 38.1% numerical variation on the nominal model generates an impedance profile remaining within these biological boundaries. The hardware testbed provides a realistic order of magnitude, mimicking a plausible clinical scenario despite the mathematical offset.

6.1 Possible enhancements

This subsection takes room for possible enhancements. First, increase the complexity of the COMSOL model by designing a complete multi-contact cuff electrode geometry. This more sophisticated setup allows the evaluation of crosstalk interference between adjacent stimulation channels. The PNT design includes physical pads on the board for a transverse parallel RC network and a series resistor connecting even and odd measurement channels. It assumes that crosstalk interactions could be equivalent to the lumped-parameter approximation used for macroscopic tissue impedance. A subsequent enhancement dictates the coupling of the macroscopic finite element model with dedicated neural simulation software, such as NEURON. This integration facilitates the microscopic modeling of the endoneurial tissue. The procedure populates the simulated fascicles with explicit mathematical models of myelinated nerve fibers. The application of these biophysical models translates the macroscopic extracellular potentials calculated in COMSOL into dynamic transmembrane responses. This computational step evaluates the behavior of individual neurons under the applied electric field. The approach provides a definitive determination of the axonal activation threshold, confirming the generation of a propagating action potential following the injected electrical stimulus. The generation of a patient-specific digital twin initiates with the acquisition of high-resolution medical imaging, such as magnetic resonance scans. These diagnostic tools provide the custom macroscopic dimensions of the peripheral nerve. The pipeline integrates these anatomical boundaries with established statistical data sourced from bioengineering literature, defining the internal fascicular morphology. The combination of these structural parameters generates a customized multiphysics environment within the COMSOL and NEURON software suites. This virtual platform sustains massive iterative electrical simulations. A machine learning algorithm governs this computational procedure. In the presence of a vast multidimensional parameter space, comprising diverse pulse widths, amplitudes, and electrode configurations,

basic numerical sweeps demand prohibitive computational time. The artificial intelligence operates as an advanced optimization tool, analyzing preliminary iterations and predicting the ideal stimulation profile. The network isolates the precise current injection pattern generating selective target fascicle activation. The completed simulation returns the mandatory current magnitude and the expected tissue impedance under those designated stimulation frequencies. This predictive digital analysis eliminates the necessity of empirical in vivo trial-and-error procedures on the human subject. The extraction of these exact electrical metrics guides the physical configuration of the interfacing hardware. The custom architecture of the power supply incorporates these predicted impedance and current values, ensuring a calibrated and energy-efficient clinical deployment.

Bibliography

[1] Maya Zaidman et al. "Epidemiology of peripheral nerve and brachial plexus injuries in a trauma population". In: *Canadian Journal of Surgery* 67.3 (2024). DOI: 10.1503/cjs.002424.

[2] William M. Padovano et al. "Incidence of Nerve Injury After Extremity Trauma in the United States". In: *HAND* 17.4 (2022), pp. 615–623. DOI: 10.1177/1558944720963895.

[3] Martin Aman et al. "An Epidemiological and Etiological Analysis of 5026 Peripheral Nerve Lesions from a European Level I Trauma Center". In: *Journal of Personalized Medicine* 12 (2022), p. 1673. DOI: 10.3390/jpm12101673.

[4] Solaiman Shokur et al. "Hand prostheses with somatosensory feedback: functional and clinical benefits". In: *The Lancet Neurology* 25 (2026), pp. 421–432.

[5] Elaine A. Biddiss and Tom T. Chau. "Upper limb prosthesis use and abandonment: A survey of the last 25 years". In: *Prosthetics and Orthotics International* 31.3 (2007), pp. 236–257. DOI: 10.1080/03093640600994581.

[6] NerveRepack. *Context & Innovation | NerveRepack*. URL: https://www.nerverepack.eu/copy-of-about-1 (visited on 08/01/2026).

[7] NerveRepack. *Context & Innovation | NerveRepack*. URL: https://www.nerverepack.eu/copy-context-innovation (visited on 08/01/2026).

[8] eLiONS. *ReWire – eLiONS*. URL: https://elions.polito.it/home/biomedical-intelligent-systems/neuroprosthetics/rewire/ (visited on 08/02/2026).

[9] Giacomo Valle et al. "Biomimetic Intraneural Sensory Feedback Enhances Sensation Naturalness, Tactile Sensitivity, and Manual Dexterity in a Bidirectional Prosthesis". In: *Neuron* 100.1 (2018), pp. 37–45. DOI: 10.1016/j.neuron.2018.08.033.

[10] Ian Williams et al. "SenseBack - An Implantable System for Bidirectional Neural Interfacing". In: *IEEE Transactions on Biomedical Circuits and Systems* 14.5 (2020), pp. 1079–1087. DOI: 10.1109/TBCAS.2020.3022839.

[11] Dongxiao Yan et al. "Ultra-flexible and Stretchable Intrafascicular Peripheral Nerve Recording Device with Axon-dimension, Cuff-less Microneedle Electrode Array". In: *Small* 18.21 (2022), e2200311. DOI: 10.1002/smll.202200311.

[12] Lukas Hiendlmeier et al. "4D-Printed Soft and Stretchable Self-Folding Cuff Electrodes for Small-Nerve Interfacing". In: *Advanced Materials* 35 (2023), p. 2210206. DOI: 10.1002/adma.202210206.

[13] Emma K Jacobs et al. "Iris 128x: open-source 128 channel headstages for neural stimulation and recording". In: *Journal of Neural Engineering* 22 (2025), p. 066009. DOI: 10.1088/1741-2552/ae1876.

[14] Daniel R. Merrill, Marom Bikson, and John G.R. Jefferys. "Electrical stimulation of excitable tissue: design of efficacious and safe protocols". In: *Journal of Neuroscience Methods* 141 (2005), pp. 171–198. DOI: 10.1016/j.jneumeth.2004.10.020.

[15] E. T. McAdams et al. "The linear and non-linear electrical properties of the electrode-electrolyte interface". In: *Biosensors & Bioelectronics* 10 (1995), pp. 67–74.

[16] J. Hope et al. "Increasing signal amplitude in electrical impedance tomography of neural activity using a parallel resistor inductor capacitor (RLC) circuit". In: *Journal of Neural Engineering* 16 (2019), p. 066041. DOI: 10.1088/1741-2552/ab462b.

[17] E. D. Musselman et al. *ASCENT: Automated Simulations to Characterize Electrical Nerve Thresholds*. https://github.com/wmglab-duke/ascent. Accessed: 2026-09-08. 2025.

[18] Eric D. Musselman et al. "ASCENT (Automated Simulations to Characterize Electrical Nerve Thresholds): A pipeline for sample-specific computational modeling of electrical stimulation of peripheral nerves". In: *PLoS Computational Biology* 17.9 (Sept. 2021), e1009285. DOI: 10.1371/journal.pcbi.1009285. URL: https://doi.org/10.1371/journal.pcbi.1009285.

[19] Eric D. Musselman, Nicole A. Pelot, and Warren M. Grill. "Validated computational models predict vagus nerve stimulation thresholds in preclinical animals and humans". In: *Journal of Neural Engineering* 20 (2023), p. 036032. DOI: 10.1088/1741-2552/acda64.

[20] M. Ryne Horn et al. "Characterization of the Electrical Properties of Mammalian Peripheral Nerve Laminae". In: *Artificial Organs* 47.4 (2023), pp. 705–720. DOI: 10.1111/aor.14500.

[21] Jason P. Wright et al. "A fully implantable wireless bidirectional neuromodulation system for mice". In: *Biosensors and Bioelectronics* 200 (2022), p. 113886. DOI: 10.1016/j.bios.2021.113886.

[22] Christine Azevedo Coste et al. "Activating effective functional hand movements in individuals with complete tetraplegia through neural stimulation". In: *Scientific Reports* 12 (2022), p. 16189. DOI: 10.1038/s41598-022-19906-x.

[23] Samuel Lienemann et al. "A Soft and Stretchable Multielectrode Cuff for Selective Peripheral Nerve Stimulation". In: *Advanced Materials Technologies* 8 (2023), p. 2201322. DOI: 10.1002/admt.202201322.

[24] N. A. Brill et al. "Evaluation of high-density, multi-contact nerve cuffs for activation of grasp muscles in monkeys". In: *Journal of Neural Engineering* 15.3 (2018), p. 036003. DOI: 10.1088/1741-2552/aa8735.

[25] Francisco Zurita et al. "Fully 3D-Printed Cuff Electrode for Small Nerve Interfacing". In: *Advanced Materials Technologies* 8 (2022), p. 2200989. DOI: 10.1002/admt.202200989.

[26] Alejandro Carnicer-Lombarte et al. "Ultraconformable cuff implants for long-term bidirectional interfacing of peripheral nerves at sub-nerve resolutions". In: *Nature Communications* 15 (2024), p. 7523. DOI: 10.1038/s41467-024-51988-1.

[27] *UM2407 User manual: STM32H7 Nucleo-144 boards (MB1364)*. UM2407. Rev 6. STMicroelectronics. Apr. 2026.

[28] Intan Technologies, LLC. *RHD2000 Series Digital Electrophysiology Interface Chips*. Dec. 8, 2023. URL: www.intantech.com.

[29] Intan Technologies, LLC. *RHS2116 Digital Electrophysiology Stimulator/Amplifier Chip*. May 13, 2021. URL: www.intantech.com.

[30] Intan Technologies. *RHD Recording Headstages*. https://intantech.com/RHD_headstages.html. Accessed: 2026-09-08. 2026.

[31] Intan Technologies. *RHS Stim/Recording Headstages*. https://intantech.com/RHS_headstages.html. Accessed: 2026-09-08.

[32] *SN65LVDxx High-Speed Differential Line Drivers and Receivers*. SLLS373M. Revised March 2024. Texas Instruments. Mar. 2024.

[33] Wendy Franks et al. "Impedance Characterization and Modeling of Electrodes for Biomedical Applications". In: *IEEE Transactions on Biomedical Engineering* 52.7 (2005), pp. 1295–1302. DOI: 10.1109/TBME.2005.847523.

[34] Brittany Hazelgrove et al. "Electrochemical impedance spectroscopy in vivo for neurotechnology and bioelectronics". In: *Nature Reviews Electrical Engineering* 2 (2025), pp. 110–124. DOI: 10.1038/s44287-024-00126-6.

[35] Octavian Ionescu et al. *Deliverable D1.5: Testing and Characterisation*. Tech. rep. D1.5, version 1.5. Nerve Repack Project, Grant Agreement n. 101112347. IMT, Dec. 2025.

[36] Aleksandar Opančar, Eric Daniel Głowacki, and Vedran Derek. "Choosing the right electrode representation for modeling real bioelectronic interfaces: a comprehensive guide". In: *Journal of Neural Engineering* 21 (2024), p. 046049. DOI: 10.1088/1741-2552/adba8b.

[37] M Sawan et al. "Electrode-tissues interface: modeling and experimental validation". In: *Biomedical Materials* 2 (2007), S7. DOI: 10.1088/1748-6041/2/1/S02.

[38] WMGLab-Duke. *ASCENT Scripts Repository*. https://github.com/wmglab-duke/ascent/tree/master/scripts. Accessed: 2026-08-29. 2026.

[39] M. Soubeyrand et al. "Anatomy of the median nerve and its clinical applications". In: *Hand Surgery and Rehabilitation* 39 (2020), pp. 2–18. DOI: 10.1016/j.hansur.2019.10.197.

[40] ASCENT Developers. *sample.json — ASCENT v1.5.0 documentation*. https://wmglab-duke-ascent.readthedocs.io/en/latest/. Accessed: 2026-08-29. 2026.

[41] Christopher J Davis et al. "Fibers in Smaller Fascicles Have Lower Activation Thresholds with Cuff Electrodes due to Thinner Perineurium and Smaller Cross-Sectional Area". In: *Journal of Neural Engineering* 20.2 (2024). DOI: 10.1088/1741-2552/acc42b.

[42] LivaNova, PLC. *VNS Therapy™ Generator and Lead Manual for Epilepsy: Pulse™, Pulse Duo™, Demipulse™, Demipulse Duo™, AspireHC™, AspireSR™, SenTiva™, SenTiva Duo™ Generators and Model 302, PerenniaDURA™, PerenniaFLEX™ Leads*. Document No. 26-0011-0100/9 (US). LivaNova, PLC. London, UK, Sept. 2025.