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A Redundant Synchronous Switching Strategy for Open-Switch Fault-Tolerant Operation of Cascaded Boost Converters in Photovoltaic Systems

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Statement on the Use of Generative AI

During the preparation of this thesis, I used ChatGPT (OpenAI), a generative AI tool, to assist with language refinement and rephrasing, translation, and the preparation of LaTeX/TikZ code and the visual formatting of figures. All AI-assisted material was carefully reviewed, verified, edited, and adapted by me before being incorporated into the thesis to ensure its accuracy, relevance, and consistency with the work presented. I retain full responsibility for the scientific methodology, technical analysis, interpretation of results, and conclusions presented in this thesis.

Abstract

The reliability of multi-stage DC–DC converters is strongly affected by failures of their controlled power switches, since an open-circuit fault in one conversion stage may interrupt the complete source-to-load energy-transfer chain. This thesis proposes a fault-tolerant strategy for a two-stage Cascaded Boost converter used in a photovoltaic energy-conversion system. The first stage is associated with PV-side power control, whereas the second stage regulates the output voltage.

The proposed topology is derived from the source–source common-node configuration of the two original switches. Under synchronous operation, their switching functions can be represented by an equivalent T-type cell composed of one redundant synchronous switch and two auxiliary diodes. During healthy operation, the two Boost stages retain their independent switching commands. Following the detection of an open-circuit fault affecting either main switch, both original switches are disabled and the switching action is transferred to the redundant equivalent synchronous switch through a common post-fault command.

Analytical modeling and MATLAB/Simulink simulations were used to evaluate the converter under healthy and faulty conditions. The results confirm the intended discontinuous and continuous conduction modes of the first and second stages, respectively, as well as the transfer of current to the redundant equivalent synchronous switch after reconfiguration. For faults affecting either main switch, the output voltage experiences only a limited transient and subsequently returns close to its 20 V reference.

A low-voltage prototype and a dSPACE-based real-time control platform were also implemented. The experimental results confirm PWM generation, real-time control operation, and closed-loop output-voltage regulation. The developed platform provides the basis for the experimental evaluation of the converter under healthy and reconfigured operating conditions.

Keywords: fault-tolerant converter; cascaded boost converter; photovoltaic systems; open-circuit fault; redundant synchronous switch; reliability.

Nomenclature

Abbreviations

Abbreviation	Description
CCM	Continuous Conduction Mode
DC	Direct Current
DC–DC	Direct-Current to Direct-Current
DCM	Discontinuous Conduction Mode
FT	Fault-Tolerant
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
OCF	Open-Circuit Fault
PCB	Printed Circuit Board
PV	Photovoltaic
PWM	Pulse-Width Modulation
SCF	Short-Circuit Fault

Symbols and Components

Symbol	Description	Unit
V_{PV}	Photovoltaic-source voltage	V
V_{bat}	Battery voltage at the intermediate DC link	V
V_o	Converter output voltage	V
$V_{o,\text{ref}}$	Output-voltage reference	V
i_{PV}	Photovoltaic-source current	A
i_{L_1}	Current through the first-stage inductor	A
i_{L_2}	Current through the second-stage inductor	A
i_{S_1}, i_{S_2}	Currents through the original controlled switches	A

Symbol	Description	Unit
i_S	Current through the redundant synchronous switch	A
i_{D_k}	Current through diode D_k, $k \in \{1, 2, 3, 4\}$	A
P_{PV}	Power supplied by the photovoltaic source	W
P_o	Converter output power	W
L_1	Inductor of the first Boost stage	H
L_2	Inductor of the second Boost stage	H
C_{PV}	Capacitor connected across the photovoltaic source	F
C_1	Intermediate DC-link capacitor	F
C_2	Output capacitor	F
R_L	Load resistance	Ω
S_1	Switch of the first Boost stage	–
S_2	Switch of the second Boost stage	–
S	Redundant synchronous switch	–
D_1, D_2	Main diodes of the first and second Boost stages	–
D_3, D_4	Auxiliary diodes of the T-type redundant switching cell	–
d_1	Duty cycle of the first Boost stage	–
d_2	Duty cycle of the second Boost stage	–
d	Duty cycle of the common post-fault command	–
f_1	Switching frequency of the first Boost stage	Hz
f_2	Switching frequency of the second Boost stage	Hz
δ_1	Healthy-mode PWM command applied to S_1	–
δ_2	Healthy-mode PWM command applied to S_2	–
δ	Common synchronous PWM command applied to S after fault reconfiguration	–
g_{S_1}, g_{S_2}, g_S	Actual gate signals applied to S_1, S_2, and S	–
F_D	Active-low fault-detection signal	–
M_1	First-stage voltage conversion ratio, $M_1 = V_{bat}/V_{PV}$	–
M_2	Second-stage voltage conversion ratio, $M_2 = V_o/V_{bat}$	–
M_{total}	Overall voltage conversion ratio, $M_{\text{total}} = V_o/V_{PV}$	–

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Chapter 1

Introduction and State of the Art

The increasing integration of renewable energy sources into electrical systems has strengthened the role of power electronic converters as interfaces between energy sources, storage elements, and electrical loads. Photovoltaic (PV) systems are a representative example, since their electrical operating point varies with environmental conditions while the downstream system generally requires controlled power transfer and a regulated voltage. DC–DC converters therefore perform more than voltage adaptation: they also provide the control flexibility required for functions such as maximum power point tracking (MPPT) and output-voltage regulation [1], [2].

When a large voltage step-up ratio is required, the practical limitations of a conventional single-stage Boost converter become more significant. Operation at very high duty cycles may increase semiconductor stresses and losses, which has motivated the development of several high-gain converter families, including quadratic and cascaded structures [3], [4], [5]. A two-stage architecture is particularly attractive when different functions must be assigned to the source and load sides of the conversion system.

The use of several conversion stages, however, also introduces additional power-semiconductor devices whose failure may affect the complete energy-transfer chain. In applications where interruption of power conversion is undesirable, detecting a switch fault is not sufficient by itself; an appropriate remedial action must also be available to maintain an acceptable level of operation after the failure [6], [7].

This chapter establishes the context of the present work, defines the addressed research problem and objectives, and reviews representative fault-tolerant approaches for DC–DC converters. The discussion is organized around the main fault-management and reconfiguration principles rather than as an exhaustive review of individual converter topologies. The chapter concludes with the research methodology and the organization adopted for the remainder of the thesis.

1.1 Context and Motivation

PV sources generally provide a variable DC voltage whose operating point depends on solar irradiance, temperature, and the electrical conditions imposed by the power

converter. At the same time, the load or downstream DC system may require a voltage level that differs significantly from the PV-side voltage and must remain regulated over the intended operating range. The power-conversion interface must consequently coordinate source-side energy extraction with the requirements imposed at the output.

A two-stage DC–DC architecture offers a convenient way to separate these functions. As illustrated in Fig. 1.1, the first conversion stage interfaces the renewable source with an intermediate energy-storage or DC-link element, while the second stage transfers the available energy toward the load. In a PV application, the first stage can be associated with source-side power extraction and MPPT, whereas the second stage can be dedicated to output-voltage regulation [1], [2].

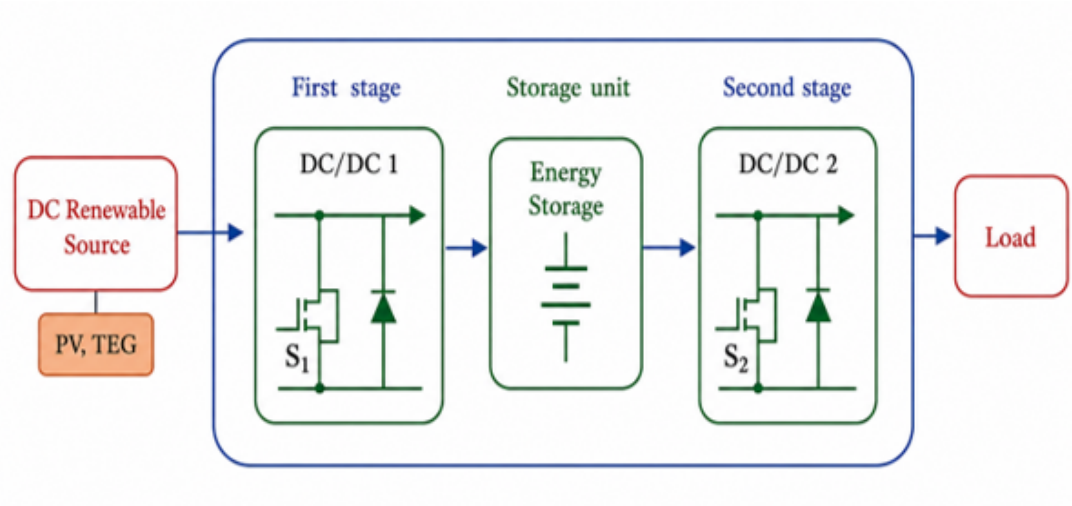


Figure 1.1: General architecture of a two-stage non-isolated DC–DC conversion system with an intermediate energy-storage unit. In the PV application considered in this thesis, the first stage is associated with source-side power extraction and MPPT, whereas the second stage is used for output-voltage regulation.

The converter investigated in this thesis follows this general architecture using two cascaded Boost stages. The first stage interfaces the PV source with the intermediate DC-link, while the second stage transfers energy from the DC-link to the output. The detailed operating modes, analytical models, and control of both stages are developed in Chapter 2.

From a reliability perspective, the active switches are critical components because a loss of switching capability directly alters the converter's current paths. An open-circuit fault (OCF) prevents the affected device from establishing the commanded conduction state. In a two-stage converter, this may disturb the energy transfer of the affected stage and consequently compromise the operation of the complete source-to-load conversion chain [8], [9].

The primary motivation of this work is to ensure continued converter operation following an open-circuit fault (OCF) in either of the two main switches while minimizing

the additional hardware required for fault-tolerant operation.

The work was carried out within the research environment of the Institut Jean Lamour (IJL), Université de Lorraine, in the context of the DENSYS Master's programme. It combines converter analysis and design, fault-tolerant topology development, controller design, numerical simulation, and experimental validation.

1.2 Problem Statement and Research Objectives

The healthy two-stage Cascaded Boost converter contains two active switches, denoted S_1 and S_2, associated respectively with the first and second conversion stages. Under normal operating conditions, each switch controls its corresponding stage, allowing the two stages to fulfill their respective source-side and output-side functions.

An OCF affecting either switch changes this operating condition. A failure of S_1 can interrupt the normal energy transfer from the PV source toward the intermediate DC-link, whereas a failure of S_2 can prevent controlled energy transfer from the DC-link to the output. Without a suitable fault-tolerant mechanism, either failure may therefore compromise the continuity of energy transfer from the source to the load. Similar reliability concerns have motivated fault-tolerant modifications of Boost and multi-stage DC–DC converters [6], [8].

One possible solution is to provide a dedicated backup switching device for each main switch. Although technically straightforward, such an approach increases the number of controlled semiconductor devices and associated gate-drive circuitry. For a compact two-stage converter, it is therefore relevant to investigate whether the required post-fault functionality can be achieved with a lower active-device overhead.

The research problem addressed in this thesis is formulated as follows:

> *How can the operation of a two-stage Cascaded Boost converter be maintained after an open-circuit fault affecting either of its two main switches while limiting the number of additional active semiconductor devices and preserving the principal source-side and load-side functions?*

The proposed solution investigates a fault-tolerant reconfiguration based on a *single redundant synchronous switch*. During healthy operation, S_1 and S_2 retain their normal independent operation. Following the detection of an OCF, the converter is reconfigured and the redundant synchronous switch is used to provide the switching action required for continued operation.

Accordingly, the main objectives of the thesis are:

1. to ensure continuous power delivery following an open-circuit fault affecting either main switch;

2. to limit the number of additional active semiconductor devices and gate drivers required for fault-tolerant operation;

3. to develop a fault-tolerant reconfiguration based on a single redundant synchronous switch while preserving the main source-side power-control and output-voltage-regulation functions;

4. to analyze the proposed converter in healthy and post-fault conditions and validate its operation through theoretical analysis, numerical simulation, and experimental testing.

The scope of the present work is restricted to open-circuit faults affecting the controlled power switches. Short-circuit faults impose different electrical and protection requirements and are not addressed by the proposed reconfiguration strategy. Converter structures capable of accommodating both open- and short-circuit failures have been reported in the literature, but they rely on fault-management requirements outside the scope considered here [10], [11].

The development of a new fault-diagnosis algorithm is also outside the main scope of this thesis. It is assumed that an OCF indication is available from an appropriate diagnostic method. Existing studies have demonstrated fault-detection and identification techniques for PV and Boost-derived DC–DC converters [6], [9]. The contribution of this work concerns the converter reconfiguration applied once the fault information becomes available.

1.3 State of the Art on Fault-Tolerant DC–DC Converters

Fault tolerance in power electronic converters generally involves several complementary functions. A fault must first be detected, and the affected device or electrical path must then be identified or isolated. A remedial action is subsequently required if converter operation is to be maintained. Depending on the converter topology, this action may involve a change in the available current paths, a modification of the switching strategy, activation of additional hardware, or a combination of these measures [6], [9].

Recent reviews classify fault-tolerant non-isolated DC–DC converters according to the adopted active and passive redundancy mechanisms [12].

Figure 1.2 illustrates the three principal functions considered in converter-level fault management: fault detection, fault isolation, and fault reconfiguration.

These functions should be distinguished from one another. Fault detection establishes that an abnormal condition has occurred, while isolation prevents the faulty component

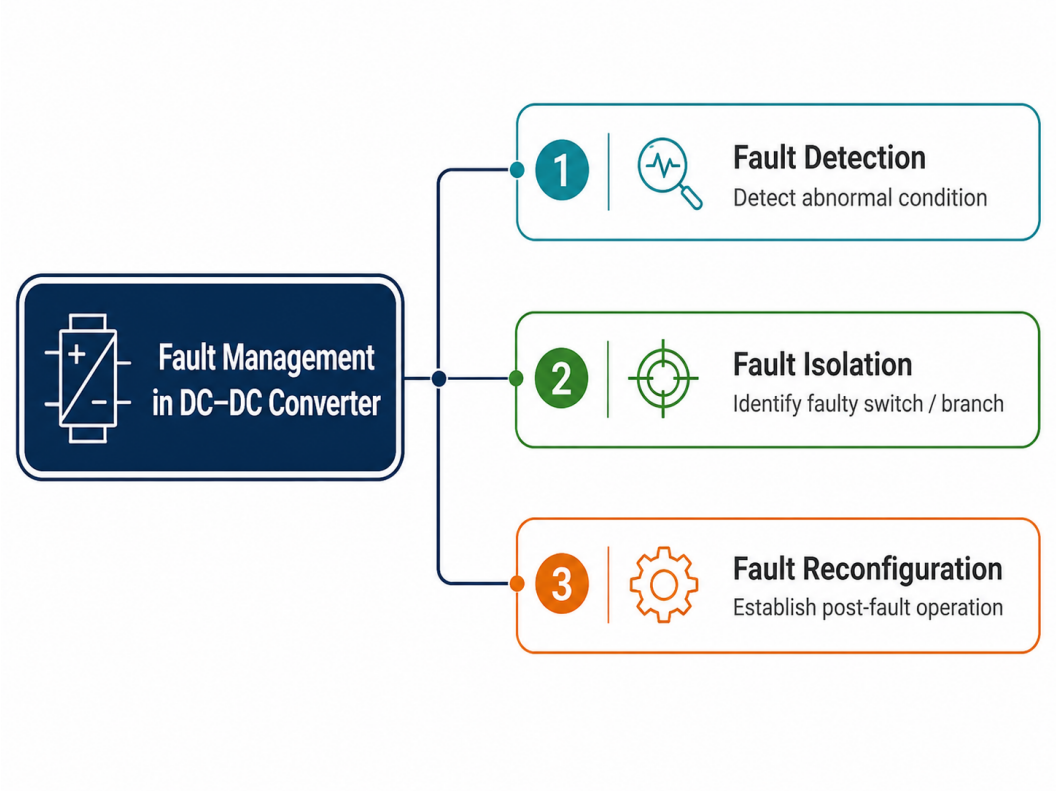


Figure 1.2: Principal functions involved in fault management of DC–DC power converters: fault detection, fault isolation, and fault reconfiguration.

or branch from compromising the remaining converter structure. Reconfiguration concerns the remedial action used to establish a viable post-fault operating condition. The present thesis is mainly concerned with this last function.

Fault-tolerant solutions may be introduced at different structural levels of a power-conversion system. A representative classification is shown in Fig. 1.3, where the remedial action is organized at switch, leg, module, or complete-system level. The most suitable level depends on the original converter architecture, the fault to be accommodated, and the amount of additional hardware that can be accepted.

At the *switch level*, fault accommodation is implemented close to the failed semiconductor device. The simplest approach consists of introducing an alternative controlled switching element or exploiting additional switching states already available in the converter structure. This level of intervention can preserve most of the original power-stage architecture, although dedicated backup devices increase the semiconductor and gate-driver count. Modified Boost converters, converters with inherent redundant switching states, and fault-tolerant switched-capacitor converters are representative examples of this approach [8], [13], [14].

At the *leg level*, an alternative switching leg or branch can be activated when the original one is no longer available. This strategy is particularly relevant to converters that

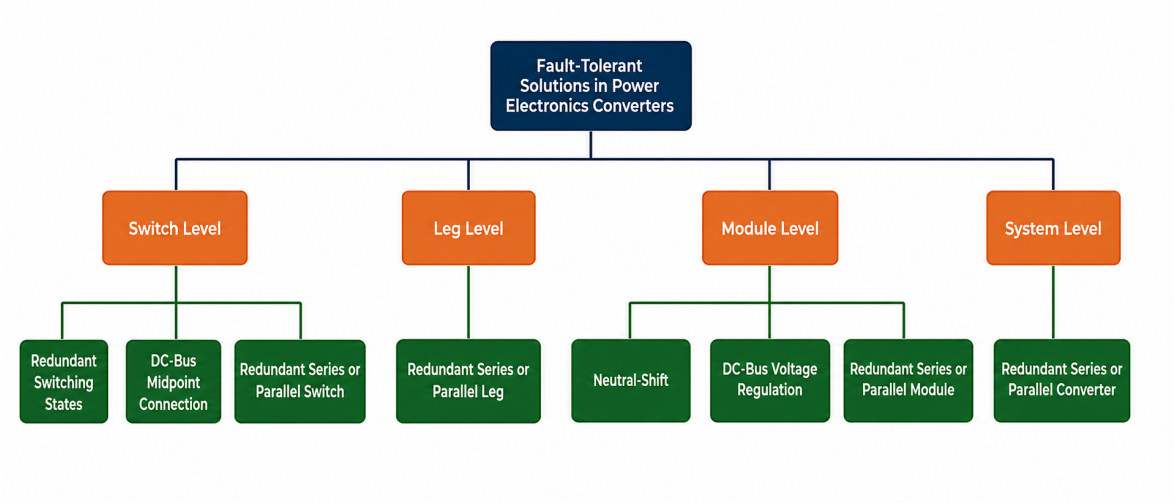


Figure 1.3: Representative classification of fault-tolerant solutions in power electronic converters according to the structural level at which the remedial action is implemented.

already contain several switching legs. It may provide effective fault accommodation, although the post-fault modulation and electrical stresses can differ from those of healthy operation [15].

At the *module level*, complete conversion cells can be bypassed, replaced, or reconfigured. Such strategies are naturally suited to modular architectures in which several cells participate in the overall voltage or power conversion. Fault-tolerant control has, for example, been developed for modular DC–DC structures with series–parallel arrangements and for modular multilevel converters operating under submodule failures [16], [17], [18].

At the *system level*, continuity may be obtained through redundant converter units or through architectures containing several available power-flow paths. Cascaded bidirectional and multiport converters are examples in which reconfiguration can be exploited to preserve operation after a component or switching failure [19], [20], [21].

Cascaded and multi-stage converters present a specific reliability challenge because the stages are functionally connected through the energy-transfer chain. A failure in one conversion stage can therefore affect the operation of the entire converter even when the remaining stage is electrically healthy. Fault-tolerant structures have been proposed for cascaded quasi-Z-source converters and other cascaded architectures in order to preserve operation following semiconductor faults [11], [22].

A particularly relevant previous contribution is the two-stage Buck/Buck–Boost converter proposed by Siouane et al. [7]. The converter uses an equivalent redundant synchronous switch to maintain operation following an open-switch failure affecting either conversion stage. The study demonstrated the feasibility of replacing the post-fault switching functions of the two original stages by a common redundant switching

structure and validated the approach experimentally. Related work also established the electrical equivalence between two-switch and single-switch Buck/Buck–Boost circuits for solar-energy harvesting systems [23].

The present work is positioned in relation to this concept but addresses a different converter architecture. The investigated system consists of two cascaded Boost stages, with the first stage associated with PV-side power control and the second with output-voltage regulation. The objective is to develop a corresponding fault-tolerant solution based on a single redundant synchronous switch while retaining the normal two-switch operation under healthy conditions.

Table 1.1 summarizes a limited selection of representative studies that are particularly relevant to the present work. The comparison is intentionally concise and focuses on the converter type, the considered fault, and the main fault-tolerant principle.

Table 1.1: Representative fault-tolerant DC–DC converter approaches relevant to the present work.

Reference	**Converter / application**	**Fault**	**Fault-tolerant principle**
[6]	PV DC–DC converter	Switch failure	Diagnosis combined with converter reconfiguration.
[10]	Single-switch DC–DC converter	OCF and SCF	Fault-tolerant converter structure for both switch-fault types.
[7]	Two-stage Buck/Buck–Boost converter	OCF	Reconfiguration using an equivalent redundant synchronous switch.
[8]	Modified Boost converter	OCF	Fault-tolerant control and modified converter structure.
[9]	Output-series interleaved Boost converter	OCF	Fault diagnosis combined with post-fault control.
[22]	Cascaded quasi-Z-source converter	Switch fault	Fault-tolerant cascaded converter structure.
[19]	Cascaded bidirectional DC–DC converter	Switch fault	Redundancy-based architecture for improved reliability.

The literature confirms that fault-tolerant design is strongly dependent on the converter architecture and the type of fault considered. Solutions based on modular or multiport structures can exploit the availability of several cells or power-flow paths, whereas compact converters generally require a more localized remedial action. For the two-stage Cascaded Boost converter investigated here, the central question is therefore whether an OCF affecting either main switch can be accommodated using one common

redundant active device rather than duplicating the complete converter or providing a separate backup switching device for every main switch.

This question motivates the single redundant synchronous switching strategy developed in Chapter 3.

1.4 Research Methodology and Thesis Organization

The methodology adopted in this thesis follows a progressive approach from circuit theoretical analysis to experimental validation. The selected Cascaded Boost converter is first studied in healthy operation in order to establish its operating principles, control objectives, analytical model, and design parameters. This healthy configuration provides the reference against which the post-fault behavior is evaluated.

The fault-tolerant study then investigates how the converter can be reconfigured following an OCF affecting either main switch. The proposed single redundant synchronous switching strategy is developed from a topological analysis of the original converter. Its operation is subsequently evaluated through numerical simulation and experimental testing, with particular attention to the preservation of maximum power extraction and output-voltage regulation following fault occurrence.

The remainder of the thesis is organized as follows.

Chapter 2 presents the two-stage Cascaded Boost converter, including its operating principles, healthy-mode control, analytical modeling, and component design.

Chapter 3 develops the proposed fault-tolerant solution. The synchronous-switch principle is introduced, the corresponding equivalent switching structure is established, and the converter reconfiguration following an open-circuit fault is analyzed.

Chapter 4 presents the numerical and experimental validation of the proposed strategy. Healthy and post-fault operation are evaluated and the results are compared in order to assess the effectiveness and limitations of the proposed converter.

The thesis concludes with the principal findings of the work, its current limitations, and perspectives for further development.

Chapter 2

Cascaded Boost Converter: Operation, Modeling and Design

This chapter establishes the electrical behavior of the two-stage Cascaded Boost converter considered in this work under healthy operating conditions. The analysis provides the reference configuration required for the development of the fault-tolerant strategy introduced in the following chapter.

The converter is first presented at system level, with particular attention given to the role assigned to each conversion stage. The fundamental operating principles of the Boost converter are then recalled for continuous and discontinuous conduction modes. These relations are subsequently applied to the two-stage structure in order to establish its overall voltage conversion ratio. The healthy operating sequences and control objectives are then described, followed by the analytical design conditions used to select the inductors and by the control-oriented model of the output-regulation stage.

2.1 Selected Two-Stage Cascaded Boost Converter

The power-conversion structure considered in this thesis consists of two Boost converters connected in cascade, as shown in Fig. 2.1. The first conversion stage is connected to the PV source, while the second stage interfaces the intermediate DC link with the output load.

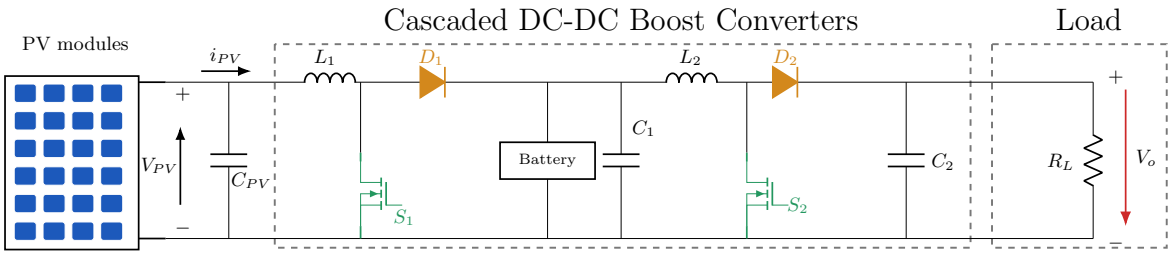


Figure 2.1: Two-stage Cascaded Boost converter considered in healthy operation.

The PV generator provides the input voltage V_{PV} and current i_{PV}. The capacitor

C_{PV}, connected at the PV terminals, limits the high-frequency voltage ripple imposed on the source by the switching converter.

The first Boost stage is composed principally of the inductor L_1, the switch S_1, and the diode D_1. Its output is connected to the intermediate battery/DC-link node, whose voltage is denoted by V_{bat}. This stage governs the power transferred from the PV source toward the intermediate energy-storage element and is consequently associated with the PV-side power-control function.

The second Boost stage contains the inductor L_2, the switch S_2, and the diode D_2. Its input voltage is V_{bat}, and its output supplies the capacitor C_2 and the load R_L. The corresponding output voltage is denoted by V_o. The principal function of this stage is to maintain V_o at the required reference value.

The two stages are designed to operate under different conduction conditions. The current through L_1 is allowed to return to zero during each switching period, and the first stage therefore operates in discontinuous conduction mode (DCM). In contrast, the current through L_2 remains positive throughout the switching cycle, corresponding to continuous conduction mode (CCM).

This choice is directly related to the function assigned to each stage. DCM operation introduces an additional dependence of the first-stage conversion characteristic on the switching frequency, which can be exploited for PV-side power control. The second stage is operated in CCM, where the duty cycle provides a direct control variable for output-voltage regulation.

The two switching stages remain electrically coupled through the intermediate DC link but are controlled independently in healthy operation. Consequently, S_1 and S_2 are not required to have the same duty cycle or switching frequency. This property is important for the control structure developed in Section 2.3.

2.2 Operating Principles and Conduction Modes

The analytical development of the Cascaded Boost converter is based on the standard operating principles of the Boost converter. The fundamental steady-state relations used in this section follow the conventional analysis of switching converters based on the inductor volt-second balance and capacitor charge balance [24].

Figure 2.2 shows the elementary Boost converter used as the basis of the analysis. It consists of an input source V_{in}, an inductor L, a controlled switch S, a diode D_1, an output capacitor C, and a load R_L.

The switching period T_s, switching frequency f_s, and duty cycle d are defined by

$$f_s = \frac{1}{T_s}, \tag{2.1}$$

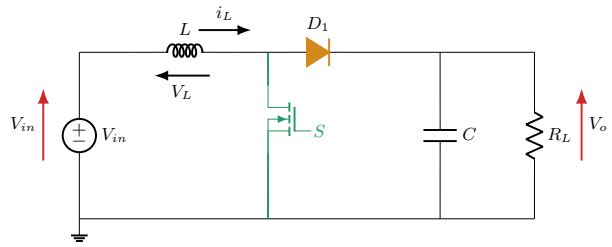


Figure 2.2: Basic Boost converter used for the analysis of the two conversion stages.

$$d = \frac{t_{\text{ON}}}{T_s}, \tag{2.2}$$

with

$$t_{\text{ON}} = dT_s, \qquad t_{\text{OFF}} = (1-d)T_s. \tag{2.3}$$

The inductor voltage and current are related by

$$v_L(t) = L\frac{di_L(t)}{dt}. \tag{2.4}$$

Depending on the converter parameters and operating point, the inductor current may remain positive during the complete switching period or may reach zero before the beginning of the following cycle. These two cases define CCM and DCM, respectively, as illustrated in Fig. 2.3.

Continuous conduction mode. In CCM, the inductor current remains strictly positive throughout the switching period. Two operating intervals are therefore sufficient to describe the converter.

During the ON interval, the switch S is closed and the diode is reverse biased. The input source is directly applied across the inductor, giving

$$v_L = V_{in}. \tag{2.5}$$

The inductor stores energy and its current increases linearly.

During the OFF interval, the switch is open and the diode becomes forward biased. The inductor releases its stored energy toward the output capacitor and the load. Its voltage is then

$$v_L = V_{in} - V_o. \tag{2.6}$$

Under steady-state conditions, the average inductor voltage over one complete switching period is zero. Hence,

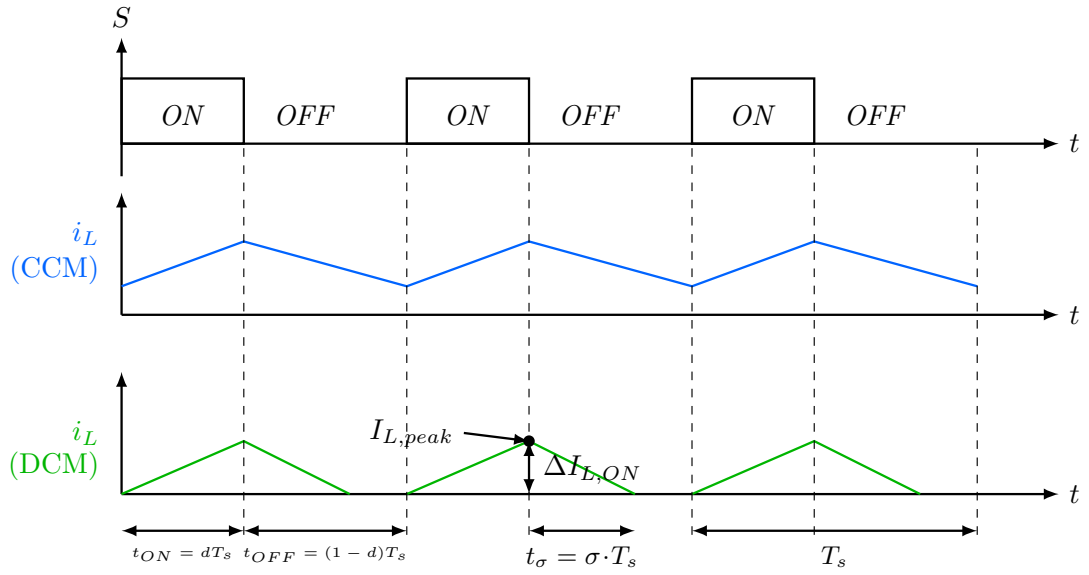


Figure 2.3: Typical switch command and inductor-current waveforms of a Boost converter in continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

$$V_{in} dT_s + (V_{in} - V_o)(1-d)T_s = 0. \tag{2.7}$$

After simplification, the CCM voltage conversion ratio is obtained as

$$M_{\text{CCM}} = \frac{V_o}{V_{in}} = \frac{1}{1-d}. \tag{2.8}$$

Discontinuous conduction mode. In DCM, the inductor current returns to zero before the end of the switching period. A complete cycle therefore contains three intervals.

During the first interval, the switch is ON and the inductor current increases from zero. The corresponding peak current is

$$I_{L,\text{peak}} = \frac{V_{in} dT_s}{L}. \tag{2.9}$$

During the second interval, the switch is OFF and the diode conducts. The inductor transfers its stored energy toward the output, and its current decreases until it reaches zero. The duration of this interval is denoted by

$$t_\sigma = \sigma T_s. \tag{2.10}$$

Applying the inductor volt-second balance over the two non-zero-current intervals

gives

$$V_{in}d + (V_{in} - V_o)\,\sigma = 0. \tag{2.11}$$

Introducing the voltage conversion ratio

$$M_{\mathrm{DCM}} = \frac{V_o}{V_{in}}, \tag{2.12}$$

the normalized diode-conduction interval becomes

$$\sigma = \frac{d}{M_{\mathrm{DCM}} - 1}. \tag{2.13}$$

During the diode-conduction interval, the current waveform is triangular. The average output current can therefore be expressed as

$$I_o = \frac{1}{2} I_{L,\mathrm{peak}} \sigma. \tag{2.14}$$

Using Eq. (2.9) and Eq. (2.13), together with

$$I_o = \frac{V_o}{R_L}, \tag{2.15}$$

the DCM voltage conversion ratio is obtained as

$$M_{\mathrm{DCM}} = \frac{1}{2}\left(1 + \sqrt{1 + \frac{2d^2 R_L T_s}{L}}\right). \tag{2.16}$$

Since $T_s = 1/f_s$, Eq. (2.16) can equivalently be written as

$$M_{\mathrm{DCM}} = \frac{1}{2}\left(1 + \sqrt{1 + \frac{2d^2 R_L}{L f_s}}\right). \tag{2.17}$$

Unlike the CCM relation of Eq. (2.8), the DCM conversion ratio depends on several quantities: the duty cycle, the inductance, the switching frequency, and the load seen by the converter. For the first stage of the Cascaded Boost converter, this dependence provides the additional control degree of freedom required for the PV-side function.

Application to the two-stage Cascaded Boost converter. The preceding relations can now be applied to the converter of Fig. 2.1.

For the first Boost stage, the voltage conversion ratio is defined as

$$M_1 = \frac{V_{bat}}{V_{PV}} \tag{2.18}$$

Since this stage operates in DCM, its gain is written as

$$M_1 = \frac{1}{2}\left(1 + \sqrt{1 + \frac{2d_1^2 R_{\text{eq},1}}{L_1 f_1}}\right), \tag{2.19}$$

where $R_{\text{eq},1}$ denotes the equivalent load seen from the output of the first Boost stage. For the second Boost stage,

$$M_2 = \frac{V_o}{V_{bat}} \tag{2.20}$$

Since the second stage operates in CCM, its steady-state gain is

$$M_2 = \frac{1}{1 - d_2}. \tag{2.21}$$

The two conversion stages are connected in cascade. The overall voltage conversion ratio is therefore obtained directly from the product of the individual stage gains:

$$M_{\text{total}} = \frac{V_o}{V_{PV}} = M_1 M_2. \tag{2.22}$$

Substituting Eqs. (2.19) and (2.21) yields

$$\frac{V_o}{V_{PV}} = \frac{1}{2}\left(1 + \sqrt{1 + \frac{2d_1^2 R_{\text{eq},1}}{L_1 f_1}}\right)\frac{1}{1 - d_2}. \tag{2.23}$$

Equation (2.23) is derived under ideal steady-state operating conditions, with ideal semiconductor devices and passive components, while conduction losses, switching losses, and parasitic elements are neglected. The resulting expression therefore represents the theoretical voltage conversion ratio of the Cascaded Boost converter. It also highlights an important property of the selected structure: the voltage transfer of the two stages is governed by two distinct sets of operating variables. The first-stage gain can be influenced through d_1 and f_1, whereas the second-stage gain is principally determined by d_2. This separation forms the basis of the healthy control strategy described next.

2.3 Healthy Operation and Control

Under healthy conditions, no switch fault is present and the Cascaded Boost converter operates with its two original controlled switches, S_1 and S_2. Each conversion stage is assigned a distinct function and receives its own switching command.

The gate signals are denoted by

$$\delta_1 = \delta_1(d_1, f_1), \tag{2.24}$$

and

$$\delta_2 = \delta_2(d_2, f_2). \tag{2.25}$$

Because these signals are generated independently, the two stages can operate with different switching frequencies and duty cycles. This independent control is referred to in this work as the healthy asynchronous operating mode.

Figure 2.4 shows the corresponding power stage and control architecture.

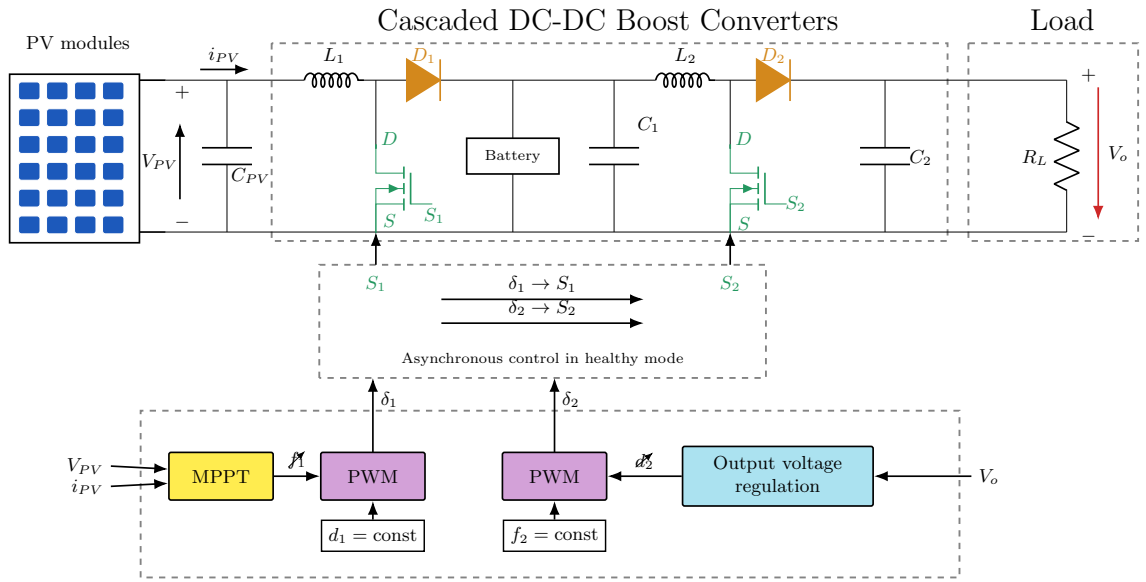


Figure 2.4: Healthy-mode control architecture of the two-stage Cascaded Boost converter. The first stage is associated with PV-side power control and MPPT, while the second stage regulates the output voltage.

First-stage operation. The first Boost stage transfers energy from the PV source to the intermediate DC link. Since L_1 is designed for DCM operation, its current waveform contains three successive intervals.

When S_1 is turned ON, D_1 is reverse biased and the PV source charges L_1. The inductor voltage is

$$v_{L_1} = V_{PV}, \tag{2.26}$$

and the current increases linearly until it reaches

$$I_{L_1,\text{peak}} = \frac{V_{PV} d_1}{L_1 f_1}. \tag{2.27}$$

When S_1 is turned OFF, D_1 becomes forward biased and the energy stored in L_1 is transferred to the intermediate DC link. The inductor voltage becomes

$$v_{L_1} = V_{PV} - V_{bat}. \tag{2.28}$$

Since $V_{bat} > V_{PV}$ during Boost operation, this voltage is negative and i_{L_1} decreases. The normalized diode-conduction interval of the first stage is

$$\sigma_1 = \frac{d_1}{M_1 - 1}. \tag{2.29}$$

Once the energy initially stored in L_1 has been transferred, the inductor current reaches zero. It remains zero during the final part of the switching period before the next cycle begins.

Second-stage operation. The second Boost stage transfers energy from the intermediate DC link to the output. Its inductor L_2 is selected such that the current remains continuous.

When S_2 is ON, D_2 is reverse biased and the intermediate DC-link voltage is applied across L_2:

$$v_{L_2} = V_{bat}. \tag{2.30}$$

The inductor current therefore increases while C_2 supplies the load.

When S_2 is turned OFF, D_2 conducts and the energy stored in L_2 is transferred to the output capacitor and the load. The inductor voltage becomes

$$v_{L_2} = V_{bat} - V_o. \tag{2.31}$$

The current consequently decreases during this interval but remains strictly positive as long as the CCM condition is satisfied.

Applying the volt-second balance to L_2 leads again to

$$\frac{V_o}{V_{bat}} = \frac{1}{1 - d_2} \tag{2.32}$$

Maximum power point tracking. For a given irradiance and temperature, a photovoltaic source exhibits a maximum power point on its power–voltage characteristic. Since the location of this point varies with the operating conditions, the electrical operating point imposed by the converter must be adjusted in order to maintain maximum power extraction from the PV source. Maximum power point tracking (MPPT) therefore constitutes the source-side control objective of the first Boost stage [25], [26].

In the present work, this function is implemented using the Perturb and Observe

(P&O) principle. The PV voltage V_{PV} and current i_{PV} are measured, and the corresponding PV power is calculated as

$$P_{PV} = V_{PV} i_{PV}. \tag{2.33}$$

The controller applies a small perturbation to the operating point and observes the resulting change in P_{PV}. When the perturbation leads to an increase in the extracted power, the following perturbation is continued in the same direction. If the power decreases, the direction is reversed. Repeating this procedure drives the operating point toward the vicinity of the maximum power point. As is inherent in the P&O principle, a small steady-state oscillation around the maximum-power operating point may remain after convergence [26].

In the first Boost stage considered here, the MPPT action is applied through the switching frequency rather than through the duty cycle. The DCM conversion characteristic established previously depends explicitly on f_1; this variable can therefore be used to modify the PV operating point while d_1 is maintained constant. At each MPPT update, the variation in PV power resulting from the preceding frequency perturbation is evaluated. If the resulting power increases, f_1 is perturbed again in the same direction; otherwise, the direction of the frequency variation is reversed. The resulting value of f_1 is supplied to the PWM generator of the first stage.

Accordingly, the MPPT controller determines the switching frequency associated with S_1, whereas the second-stage controller regulates the output voltage through d_2. Their respective positions within the healthy-mode control architecture are shown in Fig. 2.4.

Healthy control objectives. The independent operation of the two stages allows their control variables to be selected according to their respective functions. A similar separation between source-side power extraction and load-side voltage regulation is commonly adopted in two-stage energy-conversion interfaces [7].

For the first stage, the selected strategy keeps d_1 constant and uses the switching frequency f_1 as the principal variable acting on the PV operating point:

$$d_1 = \text{constant}, \tag{2.34}$$

$$f_1 \longrightarrow \text{PV-side power control and MPPT}. \tag{2.35}$$

This choice is consistent with the DCM gain derived in Eq. (2.19), which explicitly depends on the switching frequency.

For the second stage, f_2 is maintained constant while the duty cycle d_2 is adjusted

by the output-voltage controller:

$$f_2 = \text{constant}, \tag{2.36}$$

$$d_2 \longrightarrow \text{output-voltage regulation}. \tag{2.37}$$

The healthy operating characteristics are summarized in Table 2.1.

Table 2.1: Healthy operating characteristics of the two-stage Cascaded Boost converter.

Stage	**Mode**	**Main function**	**Selected control variable**
First Boost	DCM	PV-side power control and MPPT	f_1, with d_1 fixed
Second Boost	CCM	Output-voltage regulation	d_2, with f_2 fixed

This operating mode defines the reference behavior of the original converter. In particular, the two independent switching commands allow the source-side and output-side control objectives to be treated separately. The fault-tolerant strategy developed in the following chapter must preserve these two functions after the converter topology is reconfigured.

2.4 Analytical Modeling and Component Sizing

The passive components of the two Boost stages must be selected in accordance with their intended conduction modes. In particular, L_1 must allow the first-stage current to return to zero before the end of each switching period, whereas L_2 must maintain a positive current over the complete switching cycle. The standard inductor relations and conduction-mode boundary conditions used below follow the analysis presented in [24].

Sizing condition for L_1. For the first Boost stage,

$$M_1 = \frac{V_{bat}}{V_{PV}}. \tag{2.38}$$

The normalized diode-conduction interval is given by

$$\sigma_1 = \frac{d_1}{M_1 - 1}. \tag{2.39}$$

DCM operation requires that the ON interval and the diode-conduction interval end before the completion of the switching period:

$$d_1 + \sigma_1 < 1. \tag{2.40}$$

Substituting the expression of σ_1 gives

$$d_1 < 1 - \frac{V_{PV}}{V_{bat}}. \tag{2.41}$$

The condition should remain satisfied over the complete intended PV voltage range. Accordingly,

$$d_1 < 1 - \frac{V_{PV,\max}}{V_{bat}}. \tag{2.42}$$

From Eq. (2.27), the peak first-stage inductor current is

$$I_{L_1,\text{peak}} = \frac{V_{PV} d_1}{L_1 f_1}. \tag{2.43}$$

At the boundary between DCM and CCM, the triangular inductor current extends over the complete switching period. The corresponding average input current is therefore

$$I_{PV,\text{boundary}} = \frac{I_{L_1,\text{peak}}}{2}. \tag{2.44}$$

To maintain DCM at the maximum PV current,

$$I_{PV,\max} < I_{PV,\text{boundary}}. \tag{2.45}$$

This leads to the following upper limit for L_1:

$$L_1 < \frac{V_{PV} d_1}{2 f_1 I_{PV,\max}}. \tag{2.46}$$

Considering the limiting operating conditions, the design criterion can be written as

$$L_1 < \frac{V_{PV,\min} d_1}{2 f_{1,\max} I_{PV,\max}}. \tag{2.47}$$

A practical value of L_1 is selected below this limit while maintaining an adequate margin with respect to magnetic saturation and peak-current capability.

Sizing condition for L_2. For the second stage, the steady-state duty cycle is related to the intermediate and output voltages by

$$d_2 = 1 - \frac{V_{bat}}{V_o}. \tag{2.48}$$

During the ON interval, the voltage across L_2 is V_{bat}. The peak-to-peak inductor-current ripple is therefore

$$\Delta i_{L_2} = \frac{V_{bat} d_2}{L_2 f_2}. \tag{2.49}$$

At the boundary between CCM and DCM, the average inductor current is equal to one half of the current ripple. CCM operation therefore requires

$$I_{L_2,\min} > \frac{\Delta i_{L_2}}{2}. \tag{2.50}$$

For an ideal Boost stage, the average inductor current is related to the output current by

$$I_{L_2,\min} = \frac{I_{o,\min}}{1 - d_2}. \tag{2.51}$$

Using this relation together with Eq. (2.49), the minimum inductance required to maintain CCM is

$$L_2 > \frac{V_{bat} d_2 (1 - d_2)}{2 f_2 I_{o,\min}}. \tag{2.52}$$

A practical value of L_2 is consequently selected above this limit.

Inductor current verification. Once L_1 and L_2 have been selected, their maximum current ratings must be checked.

For the first-stage inductor,

$$I_{L_1,\text{peak},\max} = \frac{V_{PV,\max} d_1}{L_1 f_{1,\min}}. \tag{2.53}$$

For the second-stage inductor,

$$I_{L_2,\text{peak},\max} = \frac{I_{o,\max}}{1 - d_2} + \frac{V_{bat} d_2}{2 L_2 f_2}. \tag{2.54}$$

The corresponding saturation-current ratings must satisfy

$$I_{\text{sat},L_1} > k_i I_{L_1,\text{peak},\max}, \tag{2.55}$$

and

$$I_{\text{sat},L_2} > k_i I_{L_2,\text{peak},\max}, \tag{2.56}$$

where k_i is a design safety factor.

The principal conduction-mode and inductor-sizing conditions are summarized in Table 2.2.

Table 2.2: Summary of the principal inductor design conditions.

Design condition	**Expression**
First-stage DCM condition	$d_1 + \sigma_1 < 1$
First-stage duty-cycle condition	$d_1 < 1 - \dfrac{V_{PV,\max}}{V_{bat}}$
First-stage inductor	$L_1 < \dfrac{V_{PV,\min} d_1}{2 f_{1,\max} I_{PV,\max}}$
Second-stage duty cycle	$d_2 = 1 - \dfrac{V_{bat}}{V_o}$
Second-stage inductor	$L_2 > \dfrac{V_{bat} d_2 (1 - d_2)}{2 f_2 I_{o,\min}}$

Control-oriented model of the output stage. The second Boost stage is responsible for output-voltage regulation. Since it operates in CCM, an averaged model can be obtained from its two switching states. The state variables considered here are the inductor current i_{L_2} and the output voltage v_o, while d_2 denotes the instantaneous duty cycle. The intermediate DC-link voltage is assumed to be V_{bat}.

When S_2 is ON,

$$\frac{di_{L_2}}{dt} = \frac{V_{bat}}{L_2}, \tag{2.57}$$

and

$$\frac{dv_o}{dt} = -\frac{v_o}{R_L C_2}. \tag{2.58}$$

When S_2 is OFF,

$$\frac{di_{L_2}}{dt} = \frac{V_{bat} - v_o}{L_2}, \tag{2.59}$$

and

$$\frac{dv_o}{dt} = \frac{i_{L_2}}{C_2} - \frac{v_o}{R_L C_2}. \tag{2.60}$$

Averaging the two operating states over one switching period gives

$$\frac{di_{L_2}}{dt} = \frac{V_{bat}}{L_2} - \frac{(1 - d_2) v_o}{L_2}, \tag{2.61}$$

and

$$\frac{dv_o}{dt} = \frac{(1 - d_2) i_{L_2}}{C_2} - \frac{v_o}{R_L C_2}. \tag{2.62}$$

At steady state,

$$V_o = \frac{V_{bat}}{1 - \bar{d}_2}, \tag{2.63}$$

and

$$I_{L_2} = \frac{V_o}{R_L(1 - \bar{d}_2)}. \tag{2.64}$$

For control analysis, each variable is expressed as the sum of its steady-state value and a small perturbation:

$$d_2 = \bar{d}_2 + \tilde{d}_2, \tag{2.65}$$

$$i_{L_2} = I_{L_2} + \tilde{i}_{L_2}, \tag{2.66}$$

$$v_o = V_o + \tilde{v}_o. \tag{2.67}$$

After substitution into Eqs. (2.61) and (2.62), removal of the steady-state terms, and neglect of second-order perturbation products, the linearized model becomes

$$\frac{d\tilde{i}_{L_2}}{dt} = -\frac{1 - \bar{d}_2}{L_2}\tilde{v}_o + \frac{V_o}{L_2}\tilde{d}_2, \tag{2.68}$$

$$\frac{d\tilde{v}_o}{dt} = \frac{1 - \bar{d}_2}{C_2}\tilde{i}_{L_2} - \frac{1}{R_L C_2}\tilde{v}_o - \frac{I_{L_2}}{C_2}\tilde{d}_2. \tag{2.69}$$

Taking the Laplace transform and eliminating $\tilde{i}_{L_2}(s)$ yields the control-to-output transfer function

$$G_{vd}(s) = \frac{\tilde{v}_o(s)}{\tilde{d}_2(s)} = \frac{V_o}{1 - \bar{d}_2} \frac{1 - \dfrac{L_2}{R_L(1 - \bar{d}_2)^2}s}{1 + \dfrac{L_2}{R_L(1 - \bar{d}_2)^2}s + \dfrac{L_2 C_2}{(1 - \bar{d}_2)^2}s^2}. \tag{2.70}$$

This model provides the dynamic relationship between variations of the second-stage duty cycle and the resulting output-voltage response. It therefore forms the analytical basis for the output-voltage regulation loop used in the healthy converter. The averaging and small-signal procedure follows the standard modeling approach for PWM converters [24].

The numerator of Eq. (2.70) also reflects the non-minimum-phase behavior associated with the CCM Boost converter, which must be considered when selecting the closed-loop control bandwidth [24].

At this point, the healthy converter is fully characterized in terms of its steady-state conversion ratios, conduction modes, independent control variables, principal component-design conditions, and output-stage dynamic model. These results constitute the reference against which the synchronous-switch-based fault-tolerant configuration is developed in the next chapter.

Chapter 3

Proposed Fault-Tolerant Strategy Based on a Redundant Synchronous Switch

Chapter 2 established the operation, control, and design of the original two-stage Cascaded Boost converter. In healthy conditions, the two stages are controlled independently by the switches S_1 and S_2. This arrangement provides the control flexibility required for PV-side power extraction and output-voltage regulation, but an open-circuit fault affecting either active switch can interrupt the switching action of the corresponding conversion stage.

This chapter develops the proposed fault-tolerant structure from the topology of the original converter. The derivation begins with the synchronous-switch concept and the identification of the common electrical node shared by S_1 and S_2. The electrical equivalence between the original synchronized switches and a single T-type switching cell is then established. This equivalent cell is subsequently combined with the original Cascaded Boost converter to obtain the final fault-tolerant topology.

The chapter also describes the transition between the healthy operating configuration and the reconfigured post-fault configuration. In healthy operation, S_1 and S_2 retain their independent gate signals, while the redundant switch S remains blocked. Following the detection of an open-circuit fault, the two original switches are disabled and the switching action is transferred to S.

3.1 Synchronous-Switch Principle

The synthesis of the redundant switching structure is based on the synchronous-switch approach originally developed for the systematic derivation of power-converter topologies [27], [28]. The method considers whether several controlled switching devices can be represented by one equivalent switching cell without changing the electrical states of the surrounding converter.

Two conditions must be satisfied for such a transformation:

1. the original switches must share a suitable common electrical node;

2. the switches must be operated synchronously.

The common-node arrangement determines the structure of the equivalent switching cell. Four configurations are commonly distinguished, depending on the terminals connected to the shared node. They are shown in Fig. 3.1.

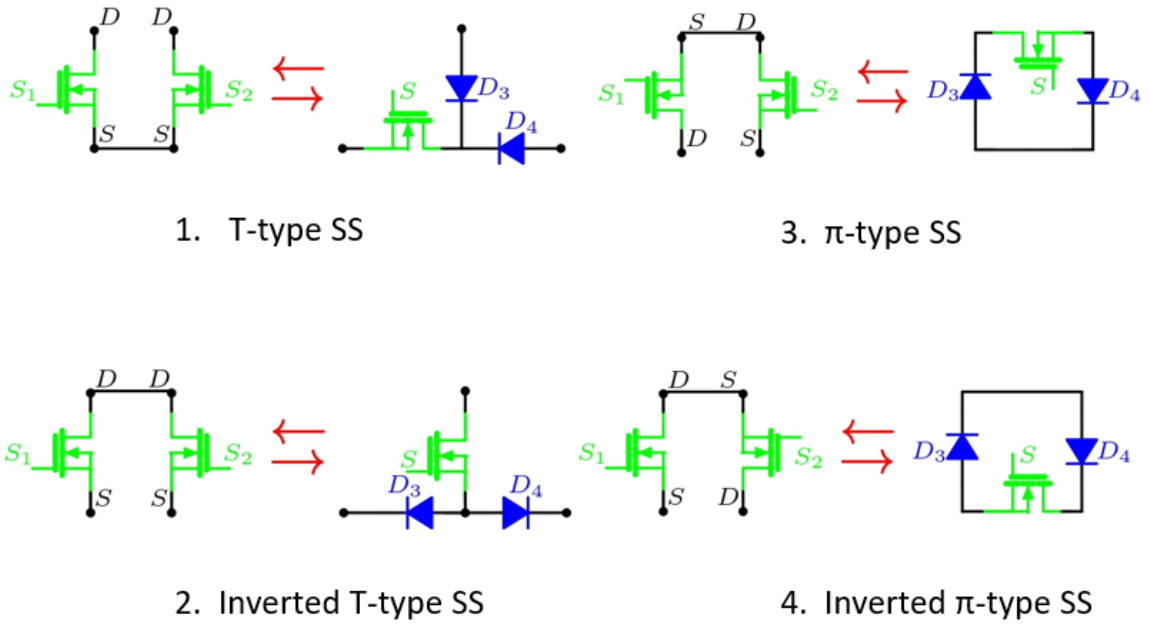


Figure 3.1: Principal common-node configurations and their corresponding synchronous-switch cells: T-type, inverted T-type, π-type, and inverted π-type. Adapted from the synchronous-switch synthesis framework in [27], [28].

The four configurations are:

- source–source common node, leading to a T-type cell;
- drain–drain common node, leading to an inverted T-type cell;
- source–drain common node, leading to a π-type cell;
- drain–source common node, leading to an inverted π-type cell.

Only the source–source configuration is relevant to the converter studied in this thesis.

Source–source common-node condition. In the original Cascaded Boost converter, S_1 and S_2 are connected as low-side switches. Their source terminals are connected to the same negative DC bus, as illustrated in Fig. 3.2.

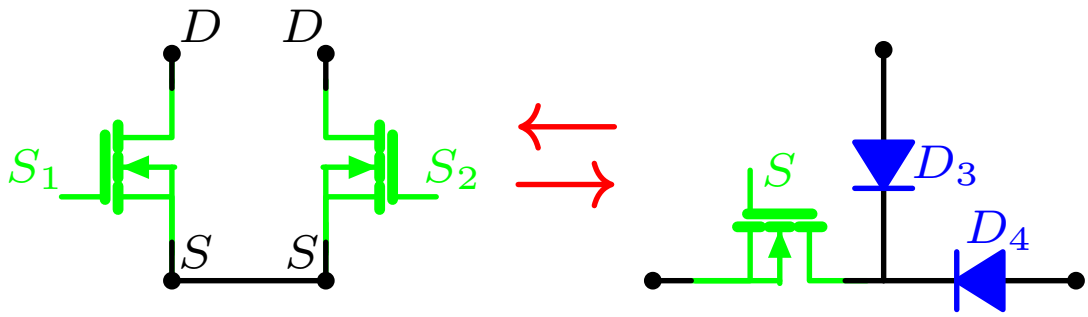


Figure 3.2: Source–source common-node configuration of S_1 and S_2, and the corresponding T-type synchronous switching cell composed of the switch S and the auxiliary diodes D_3 and D_4.

The presence of the source–source common node determines the form of the equivalent cell. In its non-degenerate configuration, the corresponding T-type structure contains one switch S and two auxiliary diodes, D_3 and D_4.

The common-node condition alone does not establish electrical equivalence. Although S_1 and S_2 share the same negative bus, they cannot generally be replaced by one switch while retaining their independent healthy-mode gate signals. A second condition concerning their switching functions is therefore required.

Synchronous-switching condition. For the equivalent representation to be valid, S_1 and S_2 must change state at the same instants. Their switching functions must therefore satisfy

$$g_{S_1}(t) = g_{S_2}(t) = g_S(t), \tag{3.1}$$

where $g_{S_1}(t)$ and $g_{S_2}(t)$ are the switching functions of the two original devices, and $g_S(t)$ is the switching function of the equivalent switch.

Equation (3.1) requires identical duty cycles and switching frequencies:

$$d_1 = d_2 = d, \tag{3.2}$$

$$f_1 = f_2 = f. \tag{3.3}$$

These conditions define a synchronous operating state and must be distinguished from the healthy operation presented in Section 2.3. Under healthy conditions, the two stages receive independent commands and can operate with different duty cycles

and switching frequencies. The synchronous condition introduced here is used to establish the equivalent switching structure and later to define the post-fault operating configuration.

When both the common-node condition and the synchronous-switching condition are satisfied, the transformation can be expressed as

$$(S_1, S_2)_{\mathrm{S-S,sync}} \longrightarrow S + D_3 + D_4. \tag{3.4}$$

The active switch S reproduces the common ON/OFF action of the two original switches. The auxiliary diodes retain the required directional conduction and blocking properties between the two conversion stages.

3.2 Equivalent Single-Switch Operation

The topological transformation of Eq. (3.4) is useful only if the resulting single-switch circuit reproduces the electrical behavior of the original converter under synchronous operation. The equivalence is verified here by comparing the switching states, the inductor voltages, and the corresponding energy-transfer conditions.

Figure 3.3 presents the complete derivation. Figure 3.3(a) is the original Cascaded Boost converter. Figure 3.3(b) is the electrically equivalent circuit obtained after applying the T-type synchronous-switch transformation. The final fault-tolerant circuit, shown in Fig. 3.3(c), combines the original and equivalent switching configurations.

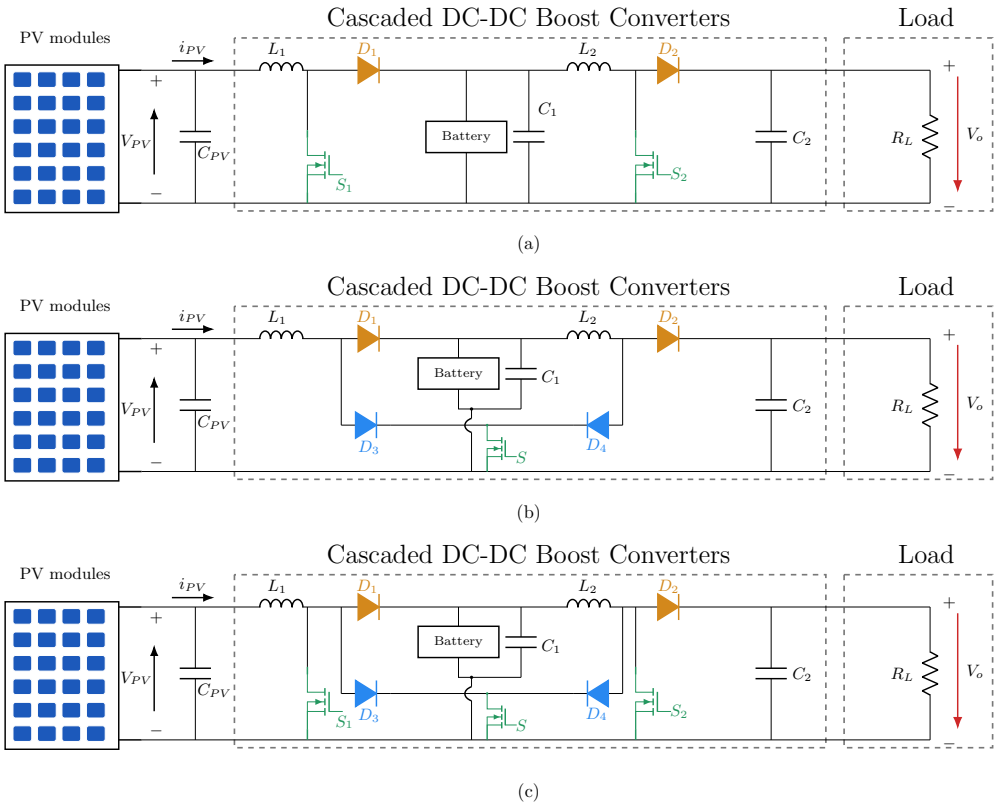


Figure 3.3: Derivation of the proposed fault-tolerant Cascaded Boost converter: (a) original two-switch conversion system, (b) electrically equivalent synchronous single-switch structure, and (c) final topology combining the original and redundant switching configurations.

Switching-state correspondence. Under synchronous operation, the original converter has two principal switching states. The two original switches are either simultaneously ON or simultaneously OFF. These states are mapped directly to the ON and OFF states of S, as summarized in Table 3.1.

Table 3.1: Switching-state equivalence between the original and equivalent Cascaded Boost structures.

State	Original structure	Equivalent structure
ON	S_1 ON and S_2 ON	S ON
OFF	S_1 OFF and S_2 OFF	S OFF

ON-state equivalence. When S_1 and S_2 are simultaneously ON, the main Boost diodes D_1 and D_2 are reverse biased. The PV source applies a positive voltage across L_1, while the intermediate DC-link voltage is applied across L_2. Consequently,

$$v_{L_1} = V_{PV}, \tag{3.5}$$

$$v_{L_2} = V_{bat}. \tag{3.6}$$

The two inductors store energy during this interval.

When the equivalent switch S is ON, the T-type cell establishes the same charging conditions. Diodes D_3 and D_4 connect the corresponding switching nodes to the common controlled device while maintaining electrical separation between the first and second conversion stages. The inductor voltages are therefore identical to Eqs. (3.5) and (3.6).

OFF-state equivalence. When the two original switches are simultaneously OFF, the energy stored in L_1 is transferred through D_1 to the intermediate DC link. At the same time, L_2 transfers energy through D_2 to the output capacitor and the load. The inductor voltages are then

$$v_{L_1} = V_{PV} - V_{bat}, \tag{3.7}$$

$$v_{L_2} = V_{bat} - V_o. \tag{3.8}$$

When S is OFF in the equivalent structure, the same diode conduction states are obtained. Diodes D_3 and D_4 block unwanted current circulation through the common switching cell, while the normal Boost diodes conduct the inductor currents toward their respective outputs.

The principal OFF-state energy transfers are consequently

$$L_1 \longrightarrow D_1 \longrightarrow C_1, \tag{3.9}$$

$$L_2 \longrightarrow D_2 \longrightarrow C_2 \parallel R_L. \tag{3.10}$$

The first-stage current may reach zero before the end of the switching period, as established in Chapter 2. This zero-current interval is determined by the first-stage energy balance and is not altered by the replacement of the synchronized switches. The current through L_2 remains continuous under the design conditions established previously.

The equivalent structure therefore preserves the inductor-voltage relations and the energy-transfer mechanisms of the original converter when S_1 and S_2 are operated synchronously.

Voltage-conversion relationship. Because the switching-state equivalence preserves the electrical behavior of both Boost stages, the conversion relationships derived in Chapter 2 remain applicable.

For synchronous operation,

$$M_{\text{eq}} = \frac{V_o}{V_{PV}} = M_{1,\text{DCM}}(d, f) M_{2,\text{CCM}}(d), \tag{3.11}$$

where the first-stage term follows the DCM relationship of Eq. (2.19), and the second-stage term follows the CCM relationship of Eq. (2.21).

The equivalent switch does not create a new energy-conversion principle. It provides another electrical realization of the same two-stage converter when the switching actions are synchronized. This result is the basis for introducing one common redundant active device in the final fault-tolerant topology. A related use of an equivalent synchronous switch was previously demonstrated for a different two-stage converter architecture in [7].

3.3 Proposed Fault-Tolerant Cascaded Boost Converter

The final fault-tolerant converter is obtained by retaining the original switches S_1 and S_2 and adding the equivalent T-type switching cell derived in the preceding sections. The additional hardware is

$$S + D_3 + D_4. \tag{3.12}$$

The two original switches remain responsible for normal operation, whereas S is reserved for the reconfigured operating condition. The passive components of both Boost stages, the intermediate DC link, and the output stage are shared between the healthy and post-fault configurations.

Healthy configuration. When no open-circuit fault is present, the converter operates exactly as described in Chapter 2. Switches S_1 and S_2 receive their independent commands, and the redundant switch remains blocked:

$$g_{S_1} = \delta_1, \tag{3.13}$$

$$g_{S_2} = \delta_2, \tag{3.14}$$

$$g_S = 0. \tag{3.15}$$

Under this condition, the added T-type cell does not participate in the normal switching action. The original Boost current transfers are therefore retained, and no modification of the healthy operating principle is required.

Post-fault configuration. An open-circuit fault prevents the affected main switch from producing its commanded ON state. In the proposed converter, the same remedial action is applied whether the fault affects S_1 or S_2.

After fault detection,

$$g_{S_1} = 0, \tag{3.16}$$

$$g_{S_2} = 0, \tag{3.17}$$

and the switching function is transferred to S:

$$g_S = \delta. \tag{3.18}$$

During the ON interval of S, L_1 is charged from the PV source and L_2 is charged from the intermediate DC link. During the OFF interval, the inductors transfer their stored energy through D_1 and D_2, respectively. The converter therefore continues operating as a two-stage Boost system, although the two switching actions are now provided by one synchronous active device.

Open-circuit fault affecting S_1. An OCF in S_1 removes the normal charging condition of L_1. Without reconfiguration, the transfer of energy from the PV source to the intermediate DC link is strongly reduced, which subsequently affects the supply of the second conversion stage.

Once the fault flag becomes active, S_1 and S_2 are disabled and S is commanded. The redundant switch restores the ON-state connection required by the first stage, allowing L_1 to store energy from the PV source. During the following OFF interval, the inductor current is transferred through D_1 toward the intermediate DC link.

Open-circuit fault affecting S_2. An OCF in S_2 removes the normal charging condition of L_2. The controlled transfer of energy between the intermediate DC link and the output is consequently lost, and the output voltage can no longer be maintained by the original switching device.

The same reconfiguration is applied. Switches S_1 and S_2 are blocked, and S produces the common switching action. The charging state of L_2 is restored when S is ON, while its energy is transferred through D_2 to the output during the OFF interval.

A separate redundant circuit is therefore not required for each fault location. The two fault cases converge to the same post-fault power configuration and the same synchronous switching sequence.

3.4 Fault-Tolerant Control and Reconfiguration

The converter topology alone does not determine the post-fault operation. A gate-signal selection mechanism is required to transfer the control action from S_1 and S_2 to S after the fault has been identified.

The complete control architecture is shown in Fig. 3.4. It retains the MPPT controller, the output-voltage controller, and the PWM generation functions used in healthy operation. A fault-management block selects which gate signals are applied to the power switches according to the operating condition.

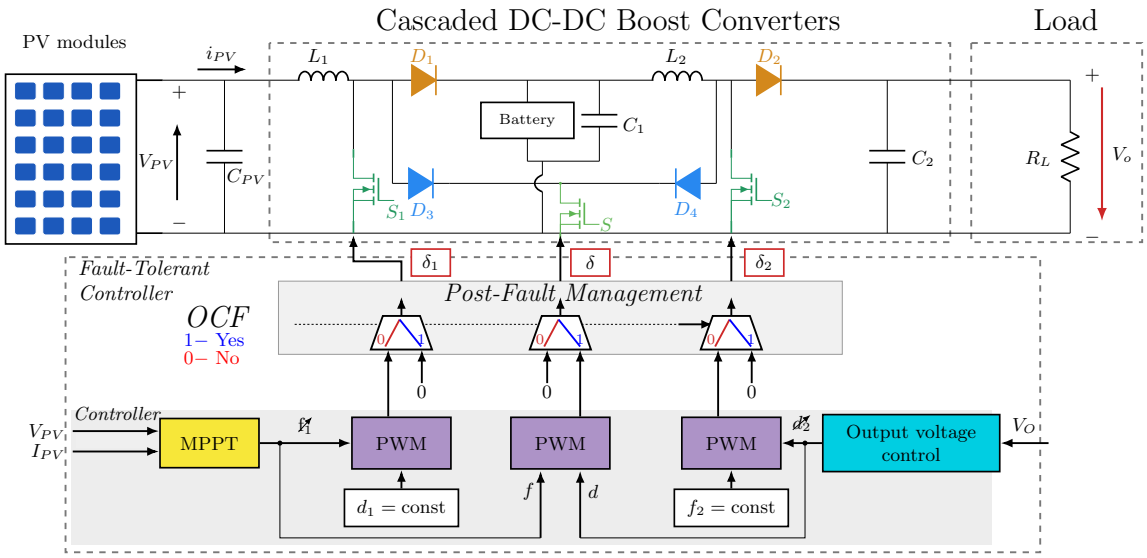


Figure 3.4: Proposed fault-tolerant Cascaded Boost converter and its associated control architecture in healthy and post-fault conditions.

Healthy asynchronous control. As established in Section 2.3, the healthy converter is driven by two independent PWM signals:

$$\delta_1 = \delta_1(d_1, f_1), \tag{3.19}$$

$$\delta_2 = \delta_2(d_2, f_2). \tag{3.20}$$

The first-stage duty cycle d_1 is maintained constant, while f_1 carries the PV-side power-control action. For the second stage, f_2 is constant and d_2 is provided by the output-voltage controller.

Post-fault synchronous control. Following reconfiguration, the converter contains only one active switching command:

$$\delta = \delta(d, f). \tag{3.21}$$

The two available variables must be selected so that the principal functions of the healthy controllers remain represented in the post-fault signal.

The switching frequency is taken from the first-stage control:

$$f = f_1, \tag{3.22}$$

whereas the duty cycle is provided by the second-stage voltage controller:

$$d = d_2. \tag{3.23}$$

The post-fault command is consequently

$$\delta = \delta(d_2, f_1). \tag{3.24}$$

This selection preserves the physical role of the two healthy control variables. The frequency f_1 continues to act on the PV-side energy transfer, while d_2 continues to represent the output-voltage control action.

Using d_1 as the common post-fault duty cycle would remove the direct action of the voltage controller because d_1 is fixed in healthy operation. Similarly, using f_2 would remove the frequency-based action generated by the PV-side controller. The pair (d_2, f_1) therefore provides the appropriate synchronous command for the selected converter.

Fault flag and gate-signal selection. The development of the fault-detection algorithm is outside the scope of this thesis. Its output is represented by the binary variable OCF:

$$\mathrm{OCF} = \begin{cases} 0, & \text{healthy operation,} \\ 1, & \text{open-circuit fault detected.} \end{cases} \tag{3.25}$$

Based on this fault flag, the controller selects between the healthy asynchronous commands and the post-fault synchronous command. The resulting selection logic is illustrated in Fig. 3.5 and summarized in Table 3.2.

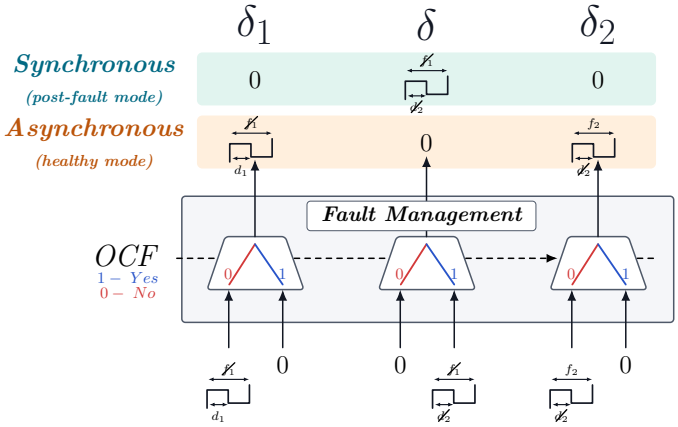


Figure 3.5: Gate-signal selection for the transition from healthy asynchronous control to post-fault synchronous control.

Table 3.2: Gate-signal selection in healthy and post-fault operating conditions.

OCF	**Operating condition**	g_{s_1}	g_{s_2}	g_s
0	Healthy asynchronous operation	δ_1	δ_2	0
1	Post-fault synchronous operation	0	0	δ

When OCF $= 0$, the two original PWM signals are applied to S_1 and S_2, and the redundant switch remains blocked. When OCF $= 1$, the original gate signals are forced to zero and the synchronous command of Eq. (3.24) is applied to S.

The same logic is used for a fault affecting either main switch. Consequently, the controller does not require a separate post-fault switching sequence for S_1 and S_2. Once the fault flag is available, both fault cases are directed toward the same reconfigured operating condition.

3.5 Design Implications and Scope

The proposed topology uses one redundant active switch to recover the switching functions required by both conversion stages after an open-circuit fault. An implemen-

tation based on an individual backup device for each original switch would require two additional active devices and two additional gate drivers. The proposed structure requires one additional controlled device and one associated gate driver, together with the two auxiliary diodes D_3 and D_4.

The reduction in active-device count does not imply that the redundant components can be selected independently of the original power stage. Switch S must withstand the voltage-blocking conditions and current levels imposed by the reconfigured converter. Its current rating must account for the switching actions associated with both inductors. Similarly, D_3 and D_4 must be selected according to their post-fault conduction currents, reverse voltages, and thermal limits.

The auxiliary diodes also introduce additional conduction losses in the reconfigured operating condition. The healthy converter is not affected by these post-fault losses because S remains blocked and the original switches provide the normal switching action. After reconfiguration, however, the efficiency and thermal behavior of the redundant cell become part of the converter performance.

A further consequence is the reduction of control freedom. Healthy operation uses two independently generated gate signals, whereas the post-fault configuration is driven by one synchronous signal. The selection $\delta(d_2, f_1)$ retains the principal source-side and output-side control actions, but the two stages can no longer be adjusted independently after reconfiguration.

The present development considers open-circuit faults and assumes that a reliable fault indication is available. Short-circuit faults require additional protection and physical isolation measures and are not covered by the proposed switching logic. The effectiveness of the topology under healthy and post-fault operating conditions, including the transition following faults in S_1 and S_2, is evaluated in Chapter 4.

Chapter 4

Simulation and Experimental Validation

The analytical developments of Chapters 2 and 3 established the healthy operation of the Cascaded Boost converter and the principle of its reconfiguration following an open-circuit fault. The present chapter evaluates the developed converter through numerical simulation and laboratory experimentation.

The numerical investigation considers healthy asynchronous operation, open-circuit faults affecting S_1 and S_2, the transfer of the switching action to the redundant switch S, and the resulting voltage and current behavior. The experimental investigation presents the implemented low-voltage prototype, the dSPACE-based real-time control platform, and the measured output-voltage response.

Together, the numerical and experimental studies examine the operation of the converter, its control implementation, and the behavior of the principal electrical variables under the considered operating conditions.

4.1 Validation Methodology and Operating Conditions

The complete converter and its control system were modeled in the MATLAB/Simulink environment. The model contains the PV source, the two Boost conversion stages, the intermediate DC link, the resistive load, the healthy-mode controllers, and the fault-management logic developed in Chapter 3.

Three operating conditions were evaluated:

1. healthy asynchronous operation, in which S_1 and S_2 are controlled by the independent signals δ_1 and δ_2;
2. reconfiguration following an OCF affecting S_1;
3. reconfiguration following an OCF affecting S_2.

In both fault cases, the fault is introduced at

$$t_f = 30 \text{ ms}. \tag{4.1}$$

The plotted fault-detection variable F_D is active low. It is equal to one during healthy operation and becomes zero once the fault has been detected:

$$F_D = \begin{cases} 1, & \text{healthy operation}, \\ 0, & \text{fault detected}. \end{cases} \tag{4.2}$$

This convention is related to the OCF variable introduced in Chapter 3 by

$$\text{OCF} = 1 - F_D. \tag{4.3}$$

The nominal parameters used in the simulation are reported in Table 4.1. They correspond to a low-power PV operating point and to the converter values used throughout the analytical development.

Table 4.1: Nominal parameters used for the simulation study.

Parameter	**Value**
PV voltage, V_{PV}	6 V
PV power, P_{PV}	8 W
Battery/DC-link voltage, V_{bat}	12 V
Output-voltage reference, $V_{o,\text{ref}}$	20 V
Load resistance, R_L	56 Ω
First-stage inductance, L_1	15 μH
Second-stage inductance, L_2	1.5 mH
Output capacitance, C_2	120 μF
First-stage switching frequency, f_1	62 kHz
Second-stage switching frequency, f_2	20 kHz
First-stage duty cycle, d_1	0.455
Second-stage duty cycle, d_2	0.4
Nominal output power, P_o	7.12 W

At the selected operating point, the ratio between the reported output power and the PV power is approximately

$$\frac{P_o}{P_{PV}} = \frac{7.12}{8} \approx 0.89. \tag{4.4}$$

This value is reported only as an operating-point power ratio. It should not be interpreted as a complete converter-efficiency characterization unless all semiconductor,

magnetic, switching, and parasitic losses are represented consistently or measured directly.

The simulated PV power–voltage characteristic is shown in Fig. 4.1. The maximum power point is located near

$$V_{PV,\mathrm{MPP}} \approx 6 \text{ V}, \qquad P_{PV,\mathrm{MPP}} \approx 8 \text{ W}. \tag{4.5}$$

This operating point is used as the nominal condition for the subsequent healthy and post-fault simulations.

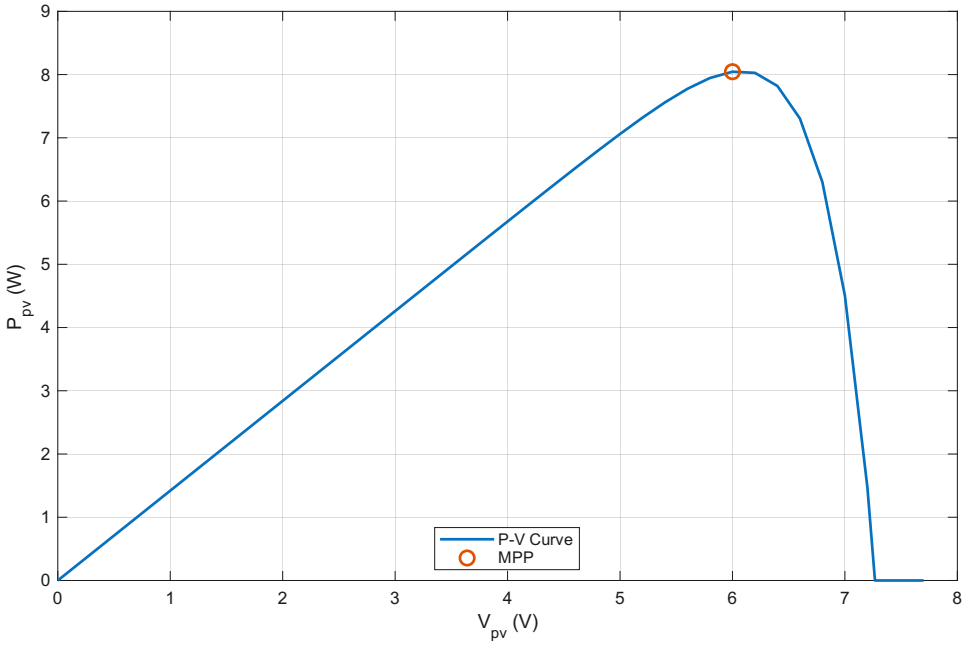


Figure 4.1: Simulated power–voltage characteristic of the PV source and the selected maximum power point.

4.2 Healthy-Mode Simulation Results

The healthy operating condition provides the reference against which the reconfigured converter is evaluated. In this mode, the first and second stages are driven independently:

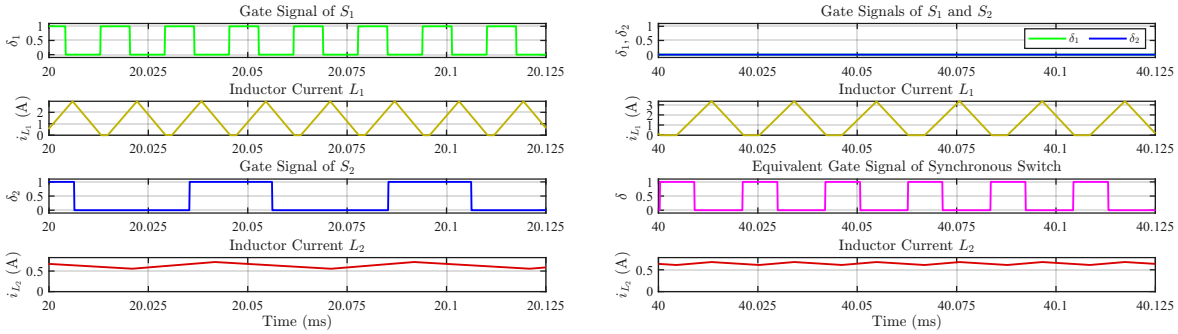
$$g_{S_1} = \delta_1(d_1, f_1), \tag{4.6}$$

$$g_{S_2} = \delta_2(d_2, f_2), \tag{4.7}$$

while

$$g_S = 0. \tag{4.8}$$

The healthy steady-state inductor currents are shown in Fig. 4.2(a).



(a) Healthy asynchronous operation. (b) Post-fault synchronous operation.

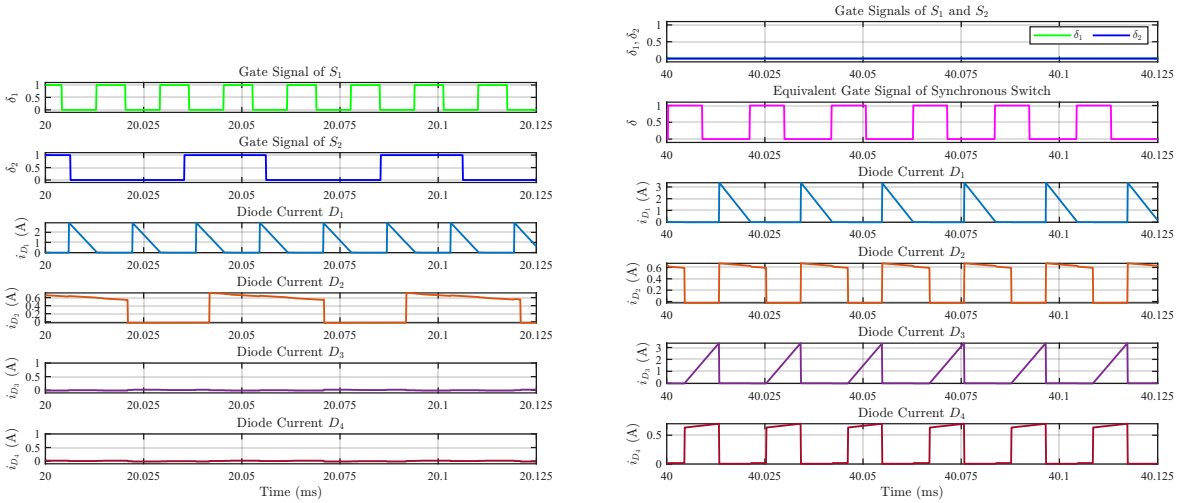
Figure 4.2: Gate signals and inductor currents under healthy and post-fault steady-state operating conditions.

The current i_{L_1} increases while S_1 is ON and returns to zero before the beginning of the following switching period. The existence of a finite zero-current interval confirms that the first Boost stage operates in DCM at the selected operating point.

In contrast, i_{L_2} oscillates around a positive average value and does not reach zero. The second stage therefore remains in CCM, as required by the design condition established in Section 2.4.

The different waveform periods also confirm the independent operation of the two stages. The first stage is driven at approximately 62 kHz, whereas the second-stage command is generated at 20 kHz. The simulation therefore reproduces the healthy asynchronous control defined in Chapter 2.

The diode currents in healthy operation are presented in Fig. 4.3(a).



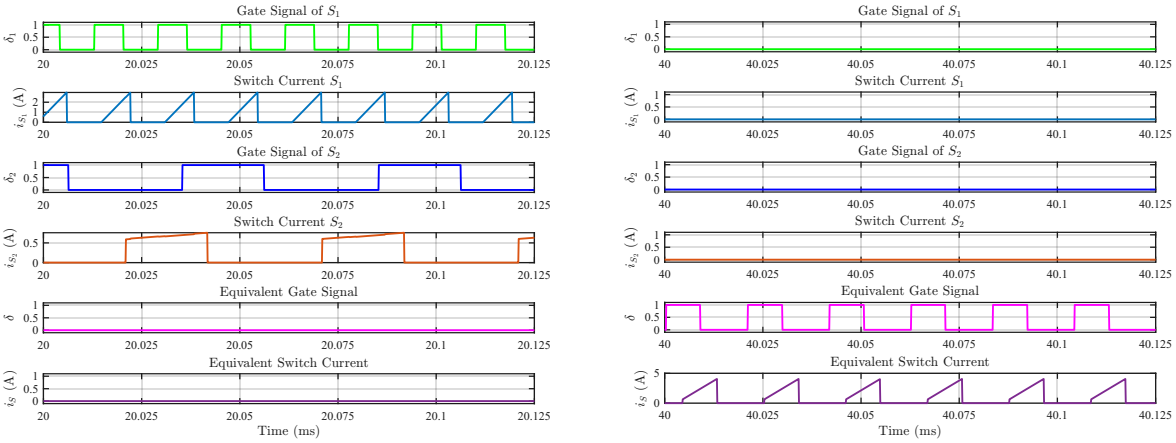
(a) Healthy asynchronous operation. (b) Post-fault synchronous operation.

Figure 4.3: Gate signals and diode currents under healthy and post-fault steady-state operating conditions.

The current through D_1 follows the discharge interval of L_1. Its triangular waveform terminates when the first-stage inductor current reaches zero. Diode D_2 conducts during the OFF interval of S_2 and transfers energy from L_2 toward the output.

The auxiliary currents i_{D_3} and i_{D_4} remain close to zero in the healthy condition. This result confirms that the redundant T-type switching cell does not participate significantly in the normal energy-transfer process.

The corresponding switch currents are shown in Fig. 4.4(a).



(a) Healthy asynchronous operation.

(b) Post-fault synchronous operation.

Figure 4.4: Gate signals and switch currents under healthy and post-fault steady-state operating conditions.

In healthy operation, i_{S_1} and i_{S_2} are present only during the respective ON intervals. The current through the redundant switch remains negligible, in agreement with the imposed condition

$$g_S = 0. \tag{4.9}$$

Taken together, the healthy waveforms verify the three reference properties required before introducing a fault: independent control of the two stages, DCM operation of L_1, and CCM operation of L_2.

4.3 Fault-Tolerant Simulation Results

The fault-tolerant behavior was examined separately for an OCF affecting S_1 and an OCF affecting S_2. In both cases, the final reconfigured state is identical: the original switching commands are disabled and the common synchronous command

$$\delta = \delta(d_2, f_1) \tag{4.10}$$

is applied to the redundant switch S.

The fault-transition signals and output-voltage responses are grouped in Fig. 4.5.

Open-circuit fault affecting S_1. Before the fault, S_1 and S_2 are driven by δ_1 and δ_2, respectively, while the command δ remains zero. At $t = 30$ ms, the command applied to the faulty switch S_1 is removed.

The waveform in Fig. 4.5a shows that the unaffected second-stage command remains active for a short transition interval. Near 30.1 ms, δ_2 is also disabled and the synchronous signal δ is enabled. The transition is therefore completed only after the original switching commands have been separated from the redundant command.

The resulting sequence can be summarized as

$$(\delta_1, \delta_2, \delta) : (\delta_1, \delta_2, 0) \longrightarrow (0, 0, \delta)\,. \tag{4.11}$$

The output-voltage waveform in Fig. 4.5c remains close to the 20 V reference. A small positive deviation appears after the switching transfer, followed by a return to the pre-fault value. From the plotted scale, the deviation is limited to approximately a few tenths of a volt.

The response shows that the energy stored in the intermediate and output capacitors supports the load during the short reconfiguration interval. Once S becomes active, the first-stage charging function is restored and the power-transfer chain is re-established.

The simultaneous PV and output voltages for the same fault case are presented in Fig. 4.6.

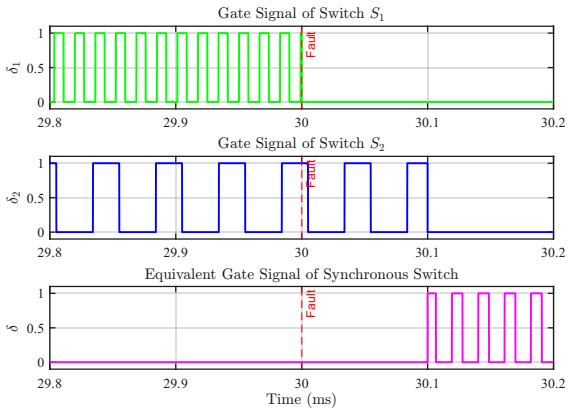
The output voltage remains close to its reference, while the PV voltage experiences a short disturbance before returning toward the nominal operating point near 6 V. This result is important because an OCF affecting S_1 acts directly on the source-side conversion stage. The recovery of both voltages indicates that the reconfigured converter retains the principal source-side and output-side control functions.

Open-circuit fault affecting S_2. For the second fault case, the command δ_2 is removed at $t = 30$ ms. The first-stage command δ_1 remains active during the short reconfiguration interval, after which it is disabled and the synchronous command δ is applied to S.

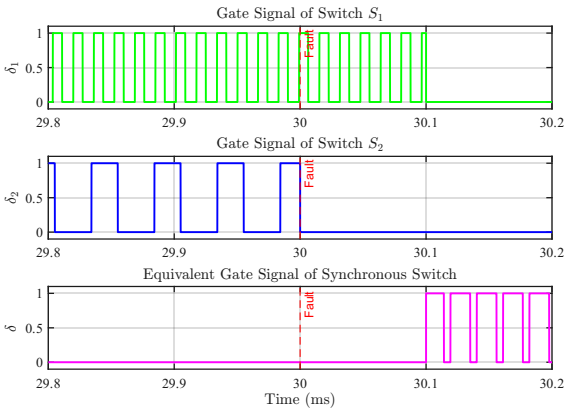
The command transition is therefore

$$(\delta_1, \delta_2, \delta) : (\delta_1, \delta_2, 0) \longrightarrow (0, 0, \delta)\,. \tag{4.12}$$

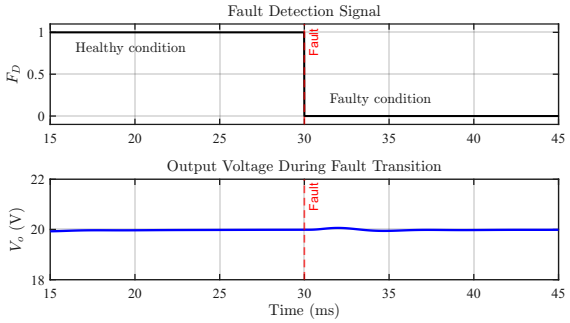
Although the final gate-signal state is the same as in the S_1 fault case, the immediate electrical consequence is different. A fault in S_2 interrupts the normal controlled transfer from the intermediate DC link to the output. The output voltage consequently shows



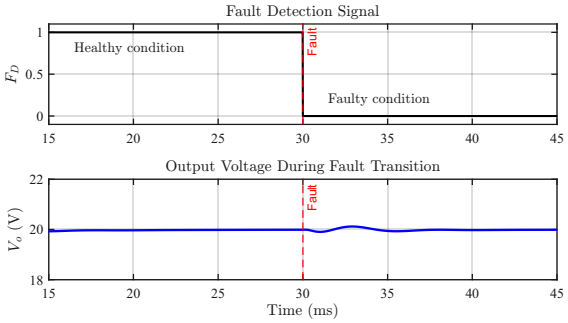
(a) Gate-signal transition following an OCF on S_1.



(b) Gate-signal transition following an OCF on S_2.



(c) Output-voltage response for an OCF on S_1.



(d) Output-voltage response for an OCF on S_2.

Figure 4.5: Simulated fault-management sequence and output-voltage response for open-circuit faults affecting S_1 and S_2.

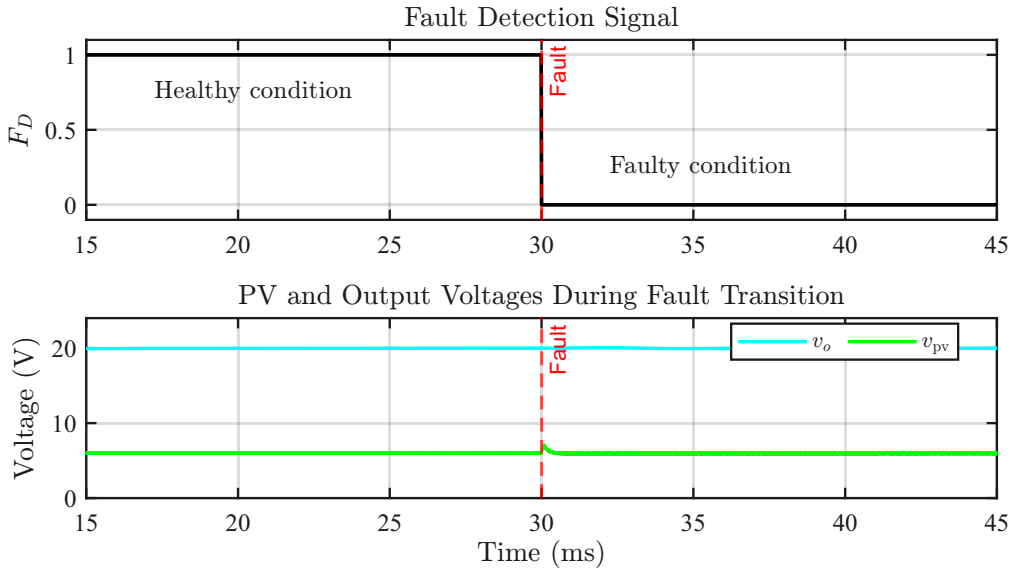


Figure 4.6: Simulated PV and output voltages during the transition following an open-circuit fault on S_1.

a small initial decrease, followed by a limited overshoot when the redundant switch assumes the common switching function.

The response in Fig. 4.5d returns rapidly toward 20 V. The transient remains limited to a few tenths of a volt according to the plotted scale, demonstrating that the same redundant switching cell can accommodate faults in either stage.

Post-fault steady-state behavior. Once the reconfiguration is complete, the original gate signals remain zero:

$$\delta_1 = \delta_2 = 0, \tag{4.13}$$

and the converter is driven exclusively by δ. The post-fault inductor currents are shown in Fig. 4.2(b).

The first-stage current continues to reach zero during every switching period. Its DCM character is therefore preserved after the transfer of the switching function to S. The current i_{L_2} remains strictly positive, confirming continued CCM operation of the second stage.

The two currents now evolve according to the same switching frequency because both stages are controlled through the common signal $\delta(d_2, f_1)$. Their conduction modes nevertheless remain different because of their component values, loading conditions, and energy-transfer relationships.

The diode-current waveforms in Fig. 4.3(b) provide direct evidence that the redundant cell is active. Unlike the healthy condition, both D_3 and D_4 carry non-zero current after the fault. The current commutation has therefore moved from the original low-side switches to the T-type redundant structure.

Diodes D_1 and D_2 retain their original energy-transfer functions. Current through D_1 is associated with the transfer of the energy stored in L_1 toward the intermediate DC link, whereas D_2 transfers the energy of L_2 toward the output.

The post-fault switch currents in Fig. 4.4(b) complete the validation of the reconfiguration. Both i_{S_1} and i_{S_2} are zero, while the redundant switch carries the combined switching current. Its simulated peak current is higher than the current carried by either original switch individually. This observation confirms the rating requirement identified in Section 3.5: the redundant device must be selected for the electrical stresses imposed by both conversion stages.

The simulation results therefore validate the following points:

- the converter operates with independent gate signals in healthy mode;
- the first and second stages satisfy their intended DCM and CCM conditions;
- an OCF affecting either S_1 or S_2 leads to the same final reconfigured topology;

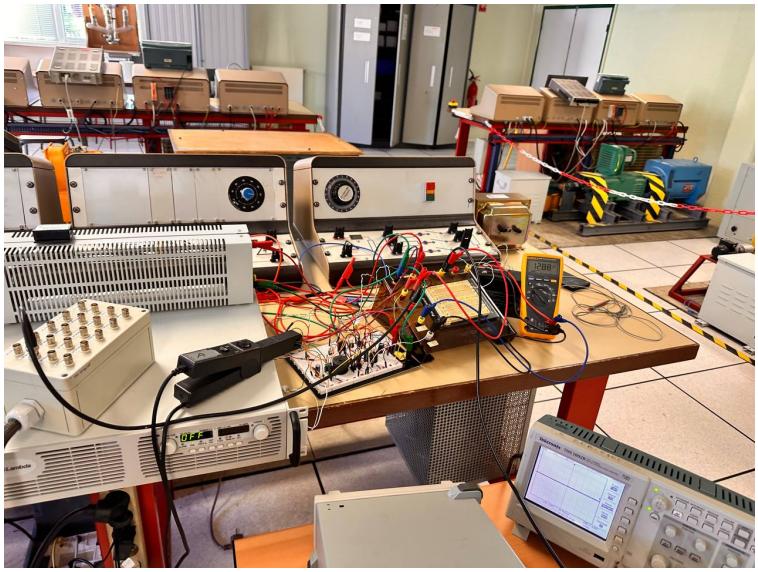
- the currents in D_3, D_4, and S confirm that the redundant switching cell becomes active after the fault;
- the output voltage remains regulated close to 20 V after both fault transitions.

4.4 Experimental Setup and Control Implementation

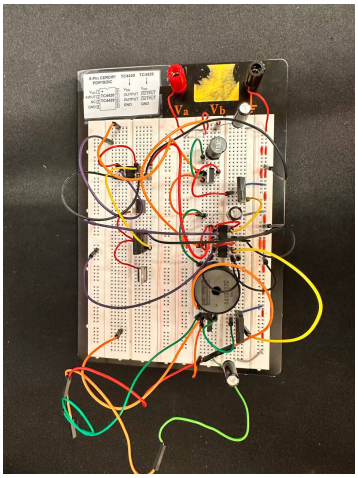
A low-voltage laboratory prototype was assembled to investigate the practical implementation of the Cascaded Boost converter and its digital control. The experimental platform was developed to reproduce the converter power stage, generate the required switching commands, acquire the principal electrical variables, and implement the closed-loop output-voltage controller in real time.

During the experimental tests, the PV source was represented by a regulated DC supply. This approach provides a fixed and reproducible operating condition and separates converter testing from variations associated with an actual PV generator. A similar procedure was used in the experimental study of the related two-stage fault-tolerant converter reported in [7].

The experimental platform and the converter prototype are shown in Fig. 4.7.



(a) Complete laboratory setup.



(b) Breadboard implementation of the converter prototype.

Figure 4.7: Laboratory platform used for the experimental investigation of the Cascaded Boost converter: (a) complete test environment and instrumentation; (b) low-voltage converter prototype.

The setup includes:

- a regulated DC power supply;
- the two-stage converter prototype;
- a resistive load;
- voltage- and current-measurement equipment;
- a digital oscilloscope and associated probes;
- a dSPACE real-time control platform;
- the ControlDesk software interface.

The power converter was assembled using discrete semiconductor devices and passive components on a prototyping board. The board includes the two Boost stages and the additional cell composed of the switch S and the auxiliary diodes D_3 and D_4.

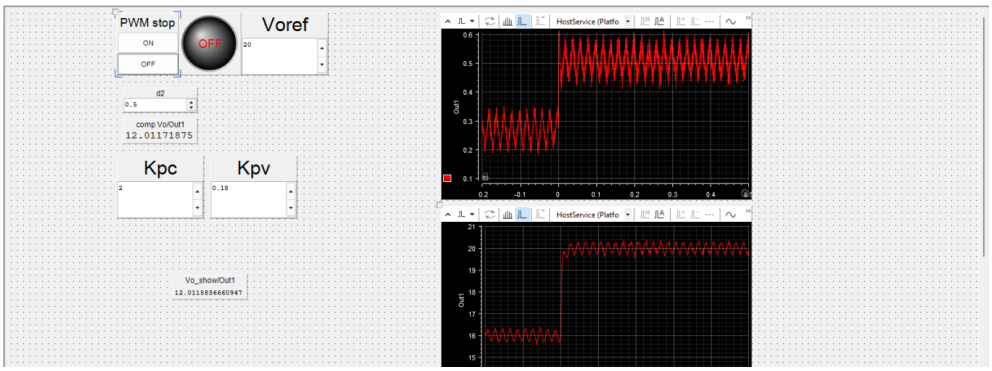
The experimental arrangement is summarized in Table 4.2.

Table 4.2: Main conditions of the experimental investigation.

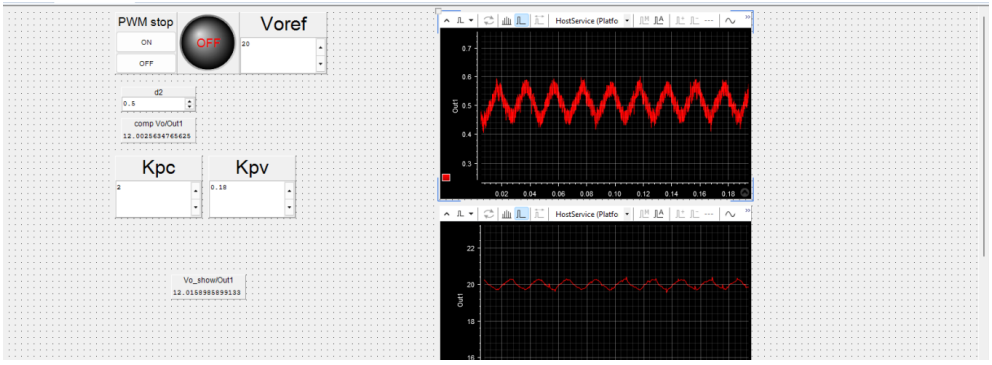
Item	**Experimental implementation**
Input source	Regulated laboratory DC power supply
Intermediate voltage	Approximately 12 V during the initial tests
Output load	Resistive load
Output-voltage reference	Approximately 16 V and 20 V
Real-time control	dSPACE platform
Supervision and acquisition	ControlDesk software
Power-stage implementation	Discrete components mounted on a prototyping board
Experimental objective	Real-time control implementation and closed-loop output-voltage regulation

Real-time control implementation. The converter control was implemented on the dSPACE platform and supervised through ControlDesk. The interface allowed the PWM generation to be enabled or disabled, the output-voltage reference to be modified, controller parameters to be adjusted, and selected internal and measured variables to be monitored.

The two ControlDesk operating views used during the tests are shown in Fig. 4.8.



(a) Steady-state operation near the 20 V reference.



(b) Output-voltage response to a reference transition from approximately 16 V to 20 V.

Figure 4.8: ControlDesk interface and measured output-voltage behavior: (a) steady-state operation near the 20 V reference; (b) response to a reference transition from approximately 16 V to 20 V.

The complete control program generated the signals required by the healthy and post-fault strategies developed previously. The closed-loop test presented in this section considers the regulation of the output stage, which was supplied from an intermediate voltage of approximately 12 V. The duty cycle d_2 was adjusted by the implemented voltage controller while the output-voltage reference was imposed from the ControlDesk interface.

Output-voltage regulation test. The output-voltage reference was first set near 16 V and then increased to 20 V. Before the reference change, the measured output remains near the initial operating point. Following the step, the controller increases the duty-cycle command and the output voltage rises toward the new reference.

The response in Fig. 4.8b reaches approximately

$$V_o \approx 20 \text{ V} \tag{4.14}$$

and remains regulated around this value. A periodic ripple is visible in steady state. It is associated with the switching operation and with the non-ideal behavior of the

prototype and measurement chain.

Figure 4.8 demonstrates the operation of the digital controller, PWM generation, voltage-measurement channel, and power stage. However, it does not provide sufficiently precise time-series data for a reliable evaluation of the rise time, settling time, overshoot, or ripple amplitude. These quantities would require the recorded ControlDesk data to be exported and processed using a defined measurement procedure.

Practical limitations of the initial prototype. Current measurements were initiated to verify experimentally that

$$i_{L_1} = 0 \tag{4.15}$$

during part of each first-stage switching period, while

$$i_{L_2} > 0 \tag{4.16}$$

throughout the second-stage switching period.

During these tests, excessive electrical and thermal stress was observed in several breadboard contacts and laboratory wires. The initial interconnections were not sufficiently robust for the current levels present in the principal switching paths. Their resistance produced additional voltage drops and localized heating, creating a risk of damage to the prototype and measurement equipment.

The current tests were consequently interrupted before a complete and repeatable set of waveforms could be recorded. This limitation concerns the physical implementation of the initial prototype rather than the numerical converter model. Reliable experimental waveforms of i_{L1}, i_{L2}, i_{D3}, i_{D4}, and i_S are therefore not reported in this work.

At this stage, the experimental campaign confirms the implementation of the low-voltage converter, the integration of the dSPACE control platform, the operation of the PWM and measurement channels, and the closed-loop regulation of the output voltage. The limits of the available experimental evidence are discussed in the following section.

4.5 Experimental Results and Discussion

The experimental investigation demonstrates the practical implementation of the converter control platform and the closed-loop regulation of the output stage. As shown in Fig. 4.8, the dSPACE and ControlDesk environment successfully generated the required PWM commands, acquired the output-voltage measurement, and allowed the voltage reference and controller parameters to be adjusted in real time. The reference transition from approximately 16 V to 20 V confirms that the implemented controller drives the

physical output stage toward the imposed operating point and maintains the output voltage around the required reference.

The experimental campaign also identified a practical limitation of the initial prototype. The breadboard contacts and laboratory interconnections were not sufficiently robust for reliable current measurements at the required current levels. The corresponding tests were therefore stopped before a complete and repeatable set of current waveforms and post-fault transitions could be recorded. Consequently, the experimental results reported in this thesis are limited to the real-time control implementation and closed-loop output-voltage regulation. The complete experimental verification of the converter currents and of the post-fault configuration is left as a continuation of the present work.

Chapter 5

Conclusion and Perspectives

This thesis addressed the continuity of operation of a two-stage Cascaded Boost converter following an open-circuit fault affecting one of its main controlled switches. The considered converter is intended for a photovoltaic energy-conversion system in which the two stages perform complementary functions. The first stage controls the power transferred from the PV source, while the second stage regulates the output voltage. Under healthy conditions, these functions are achieved through the independent control of S_1 and S_2.

An open-circuit fault affecting either switch removes one of the controlled current paths and can consequently interrupt the complete source-to-load energy-transfer chain. The work therefore investigated whether the post-fault switching requirements of both conversion stages could be recovered using one common redundant active device rather than a dedicated backup switch for each original device.

The proposed solution was developed from the synchronous-switch principle. The source terminals of S_1 and S_2 are connected to the same negative DC bus, forming a source–source common-node configuration. When the two switching functions are synchronized, the original switches can be represented electrically by a T-type synchronous switching cell composed of the controlled switch S and the auxiliary diodes D_3 and D_4. This equivalent structure was combined with the original converter to obtain the proposed fault-tolerant topology.

The principal findings and contributions of the work are summarized below, followed by the scope of the study and the main perspectives for further development.

5.1 Overall Conclusion and Main Contributions

The healthy Cascaded Boost converter was first analyzed independently of the fault-tolerant structure. Its operating modes, voltage-conversion relationships, control objectives, component-sizing conditions, and output-stage dynamic model were established. The first stage was designed to operate in discontinuous conduction mode, allowing its switching frequency to act on the PV-side power transfer while its duty cycle remained fixed. The second stage was operated in continuous conduction mode and controlled

through its duty cycle in order to regulate the output voltage.

This initial analysis provided a reference configuration in which the two conversion stages retain independent switching commands. The fault-tolerant development did not replace this healthy operating mode. Instead, the equivalent synchronous-switch structure was added as a separate configuration that remains inactive during normal operation and is introduced only after fault detection.

The resulting converter contains the original switches S_1 and S_2, one redundant synchronous switch S, and the auxiliary diodes D_3 and D_4. In the absence of a fault, S_1 and S_2 continue to operate independently, while S remains blocked. Once an OCF is detected, the commands applied to both original switches are disabled and the converter is transferred to the synchronous configuration.

The post-fault command applied to S, denoted by $\delta = \delta(d_2, f_1)$, combines the two control variables that carry the principal functions of the healthy system.

The switching frequency f_1 continues to represent the PV-side power-control action, whereas the duty cycle d_2 remains associated with output-voltage regulation. The number of independently controlled switches is therefore reduced after reconfiguration, but the two principal control objectives remain represented in the common command.

One significant feature of the proposed solution is that the same redundant switching cell is used for both fault locations. An OCF affecting S_1 and an OCF affecting S_2 lead to the same final power configuration and the same gate-signal selection. Consequently, the topology does not require a separate active backup device and gate driver for each original switch. The additional controlled hardware is limited to one redundant switch and its associated driver, together with the two auxiliary diodes required by the T-type cell.

The simulation study verified the converter under healthy and post-fault conditions. Before fault occurrence, the two stages operated with their independent gate signals and switching frequencies. The current through L_1 returned to zero during every switching period, confirming DCM operation of the first stage, while the current through L_2 remained positive and confirmed CCM operation of the second stage.

Following an OCF in either S_1 or S_2, the numerical results showed that the original switch currents disappeared and the switching current was transferred to S. The appearance of current through D_3 and D_4 further confirmed the activation of the redundant cell. Despite the change from two independent switching commands to one synchronous command, the intended conduction modes of the two stages were preserved.

The output-voltage responses provided the main indication of continuity of service. For both simulated fault locations, the output voltage experienced only a limited transient during the reconfiguration and subsequently returned close to its 20 V reference. In the case of a fault affecting S_1, the PV voltage also recovered toward its nominal

operating point after the switching transfer. These results show that the proposed reconfiguration maintains the energy-transfer capability of the two-stage converter in the considered operating condition.

A laboratory prototype was assembled and connected to a dSPACE real-time control platform. The experimental implementation included the converter power stage, PWM generation, voltage measurement, ControlDesk supervision, and closed-loop output-voltage control. A reference transition from approximately 16 V to 20 V demonstrated that the implemented controller drives the physical output stage toward the imposed voltage reference. The experimental results therefore validate the practical control implementation and output-voltage regulation, while the complete hardware verification of the post-fault reconfiguration remains to be completed.

The main contribution of the thesis can therefore be stated as the derivation and application of a single redundant synchronous switching strategy to a two-stage Cascaded Boost converter. The proposed topology retains independent stage control during healthy operation and uses one common redundant switch to restore the switching functions required after an open-circuit fault affecting either original switch.

5.2 Limitations of the Present Work

The conclusions of this study are bounded by the considered fault type, operating conditions, and level of experimental validation.

First, the fault-tolerant strategy was developed only for open-circuit faults affecting the controlled switches S_1 and S_2. Short-circuit faults were not considered. Such failures require rapid protection and electrical isolation because the resulting current increase cannot be managed solely by the reconfiguration developed in this thesis.

Second, the fault-detection and diagnosis function was not developed. The reconfiguration logic assumes that a binary fault indication is available and correctly identifies the need to transfer the switching action to S. The influence of detection delay, incorrect diagnosis, and noise in the fault signal was therefore not evaluated.

The numerical validation was performed around a defined low-power operating point. Although the selected conditions were sufficient to demonstrate the operating principle, they do not represent the complete range of PV voltage, irradiance, load, and output-reference variations that may occur in practice. The robustness of the control and reconfiguration strategy over a wider operating range remains to be established.

The experimental validation was also limited by the current-handling capability of the initial prototype interconnections. Although the converter power stage, real-time control platform, PWM generation, voltage measurement, and closed-loop output-voltage regulation were implemented successfully, the breadboard contacts and laboratory

wiring exhibited excessive electrical and thermal stress during the current measurements. The tests were therefore interrupted before reliable inductor-current and post-fault waveforms could be acquired. Consequently, the post-fault behavior is validated in this thesis primarily through numerical simulation, whereas the available experimental results concern the control implementation and output-voltage regulation.

The post-fault converter also possesses fewer independent control variables than the healthy converter. Before fault occurrence, the two stages can be adjusted independently through δ_1 and δ_2. After reconfiguration, both stages are governed by the single command $\delta(d_2, f_1)$. This arrangement preserves the principal control actions, but it limits the possibility of independently optimizing the dynamic behavior of each stage during post-fault operation.

A complete loss analysis was not performed. In particular, the additional conduction losses introduced by D_3 and D_4, the combined current carried by S, and the corresponding thermal behavior require further investigation. Semiconductor voltage stress, current stress, switching losses, magnetic losses, and post-fault efficiency should therefore be evaluated over the intended operating range before selecting components for a final converter design.

5.3 Perspectives and Future Work

The immediate continuation of this work concerns the completion of the experimental validation. The power-stage interconnections should first be reinforced using conductors and connections suitable for the required current levels. This improvement will allow reliable measurements of the first- and second-stage inductor currents and of the currents flowing through the redundant switching branch. Controlled open-circuit faults on S_1 and S_2 can then be applied in order to experimentally verify the transition from healthy asynchronous operation to the post-fault synchronous configuration. The resulting measurements should be compared directly with the numerical waveforms presented in Chapter 4.

The experimental implementation should subsequently be complemented by a real-time fault-diagnosis method. Such a method would need to distinguish an actual switch OCF from normal transient behavior and provide the reconfiguration signal within a time compatible with the energy stored in the intermediate and output capacitors. The interaction between diagnosis delay and output-voltage deviation would be an important part of this extended study.

Further work is also required on the electrical and thermal design of the redundant cell. A detailed loss model should compare healthy and post-fault efficiency and should include semiconductor conduction and switching losses, inductor losses, diode losses,

and parasitic effects. The resulting current and voltage stresses would provide the basis for selecting S, D_3, and D_4, designing their thermal management, and determining the maximum continuous duration of post-fault operation. Established power-loss analysis methods for single switch non-isolated DC–DC converters provide a relevant basis for conducting this extended evaluation [29].

The possibility of simplifying the auxiliary-diode arrangement may also be investigated. Any proposed diode reduction must preserve the required current directions, voltage-blocking states, and electrical equivalence of both conversion stages. It should therefore be supported by a complete operating-state analysis and subsequently verified through simulation and experiment.

The range of considered faults may be extended beyond single open-circuit failures. Short-circuit faults, sensor faults, gate-driver failures, and combinations of component faults would require additional protection and isolation functions. Their inclusion would broaden the fault coverage but would also modify the required hardware and fault-management logic.

The behavior of the converter should also be evaluated under variations of solar irradiance, PV voltage, load resistance, and output-voltage reference. These tests would determine whether the selected post-fault control variables remain effective outside the nominal operating point and would help establish the practical operating envelope of the proposed topology.

Finally, the synchronous-switch-based reconfiguration may be examined for other cascaded or multi-stage DC–DC converters. The common-node configuration, equivalent switching cell, and admissible post-fault control variables would need to be established separately for each topology. Such an extension would determine whether the approach developed in this thesis can serve as a broader method for reducing active redundancy in multi-stage power converters.

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Appendix A

Simulation Implementation

This appendix provides a concise overview of the MATLAB/Simulink implementation used to validate the proposed fault-tolerant Cascaded Boost converter. Only the complete model, the redundant synchronous switching branch, and the fault-management logic are presented. The simulation parameters and numerical results are discussed in Chapter 4.

A.1 Complete MATLAB/Simulink Model

The complete simulation model is shown in Fig. A.1. It includes the PV-source model, the two-stage Cascaded Boost power converter, the source-side and output-side controllers, the redundant synchronous switching branch, the fault-management subsystem, and the principal voltage- and current-measurement blocks.

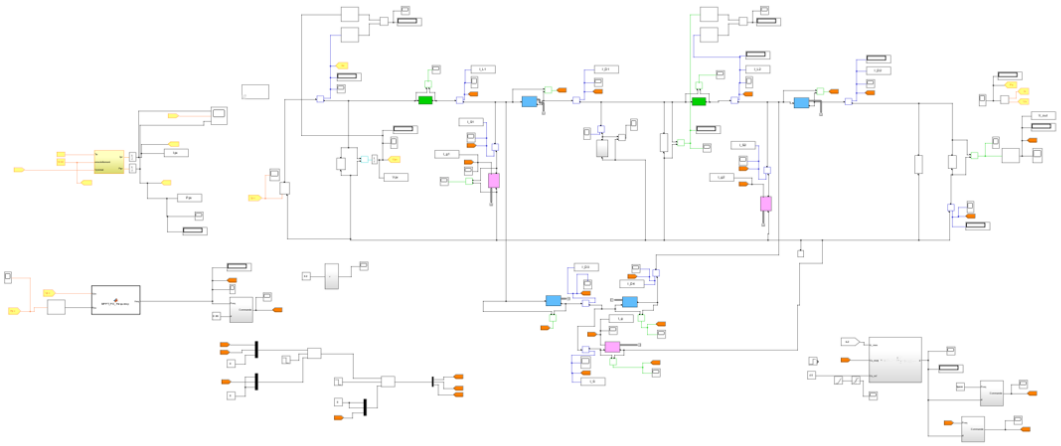


Figure A.1: Complete MATLAB/Simulink implementation of the proposed fault-tolerant Cascaded Boost converter and its control system.

A.2 Redundant Synchronous Switching Branch

Figure A.2 shows the Simscape implementation of the redundant switching branch. The branch consists of the controlled switch S and the auxiliary diodes D_3 and D_4.

The model contains measurement blocks for the currents through the redundant switch and auxiliary diodes, together with the corresponding semiconductor voltages. These variables were used to confirm that the redundant branch remains inactive during healthy operation and carries the required currents after fault reconfiguration.

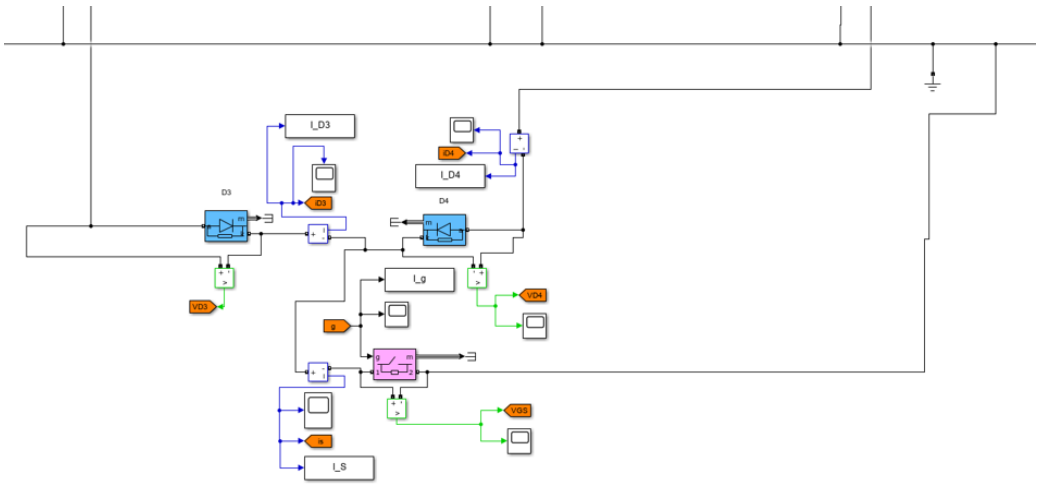


Figure A.2: Simscape implementation of the redundant synchronous switching branch composed of S, D_3, and D_4.

A.3 Fault-Management Logic

The fault-management subsystem used in the simulation is shown in Fig. A.3. During healthy operation, the independent commands δ_1 and δ_2 are applied to S_1 and S_2, respectively, while the redundant switch S remains inactive.

Following fault detection, the commands applied to the two original switches are forced to zero. The common synchronous command δ is then transferred to the redundant switch S. The same selection logic is used whether the open-circuit fault affects S_1 or S_2.

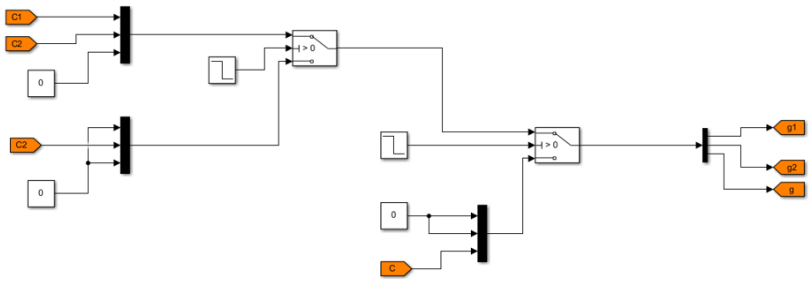


Figure A.3: Implementation of the gate-signal selection between healthy asynchronous operation and post-fault synchronous operation.