MATLAB-based Platform for Accurate Loss Evaluation of Power Electronic Devices in Selected DC/DC and DC/AC Topologies

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Abstract

This thesis presents the creation of a MATLAB application that uses Simulink for estimating semiconductor losses and junction temperature evolution in selected DC/DC and DC/AC power converter topologies. The main goal is to offer a transparent and editable engineering tool that allows different semiconductor technologies and devices to be evaluated under consistent conditions, both electrically and thermally, using parameters available from datasheets.

The implemented tool includes the capacity for estimating losses in asynchronous boost, buck, and flyback converters, as well as single-phase half-bridge, and full-bridge. The backend developed in the App Designer tool manages parameter validation, Simulink model selection, waveform extraction, loss calculation, thermal estimation, and mission-profile processing for supported DC/DC cases. Semiconductor losses are calculated by using the datasheet-based expressions and simulated waveforms, depending on the implemented device model.

The platform was evaluated using three IGBT-based validation cases. For the boost-converter case, the hand calculation, developed application, and Infineon IPOSIM predicted total semiconductor losses of 5.50 W, 5.54 W, and 5.89 W, respectively. The single-phase half-bridge case showed a total semiconductor loss of 10.86 W in the application compared with 11.575 W from the analytical calculation. For the single-phase full-bridge case, the application predicted 14.66 W compared with 13.12 W from IPOSIM.

The results show good agreement at the overall semiconductor-loss level, although larger differences remain in some individual loss components. The developed platform should therefore be interpreted as an engineering-level estimation and comparison tool rather than a replacement for detailed manufacturer or experimental electrothermal characterisation.

Software Availability

The MATLAB App Designer application, Simulink converter models, and supporting files developed as part of this thesis are publicly available in the following GitHub repository:

`https://github.com/walmyfernandez-beep/power-semiconductor-loss-platform/`

The repository contains the source code of the application, the implemented Simulink models, supporting files, and documentation required to reproduce and further develop the loss-estimation platform.

The two-level three-phase inverter is currently supported at the interface and backend level only; a validated Simulink model for this topology is not included in the present version.

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1 Introduction

1.1 Motivation

Renewable-energy systems depend on power electronics to move energy efficiently from its source to a local DC bus, a load, or the electrical grid. Converters regulate voltage in DC systems, set voltage and frequency in AC systems, and provide the DC/AC interface between them. The same devices are central to electric traction and regenerative braking. In each case, semiconductor technology has a direct effect on converter performance.

That performance comes with a practical constraint: semiconductor losses become heat. They reduce conversion efficiency, increase thermal stress and cooling demand, and ultimately affect cost, power density, and reliability. Designers therefore need credible loss estimates early enough to compare components and make these trade-offs before the hardware architecture is fixed.

An open-source, flexible, and transparent tool can make such comparisons more reliable. Comparing specific devices is often difficult because operating points and modelling assumptions vary between tools, datasheet parameters require substantial interpretation, and manufacturer software is usually restricted to the vendor's own devices or predefined topologies. A common calculation framework removes part of that uncertainty.

Wide-bandgap (WBG) devices based on gallium nitride (GaN) and silicon carbide (SiC) make this comparison especially relevant. Depending on the topology and operating conditions, these devices can improve converter efficiency by approximately 1 to 3%. Unlike silicon IGBTs, whose switching losses can include a tail-current component, many WBG power devices—including GaN HEMTs and SiC MOSFETs—operate predominantly as majority-carrier devices and do not exhibit the same tail current. They can also switch faster and incur lower switching- and recovery-related losses. Higher switching frequencies may then permit smaller passive components, lighter systems, and greater power density, which are particularly valuable in electric vehicles.

The relevant question is not simply whether WBG devices outperform silicon devices. It is where, and under which electrical and thermal conditions, they do so. This thesis therefore compares conventional silicon devices with newer WBG alternatives through a consistent, datasheet-based method that accounts for the operating point and temperature effects.

1.2 Objectives

The main objective of this thesis is to develop a MATLAB App Designer application that quantifies semiconductor-switch losses in selected DC/DC and DC/AC converters under different duty cycles, modulation indices, loads, and temperatures.

More specifically, the thesis aims to:

- Develop a generic application that uses datasheet information to simulate selected converter topologies with devices from different manufacturers.
- Include emerging semiconductor technologies, particularly GaN and SiC WBG devices.
- Review the ready-to-use tools currently available from academic, manufacturer, and open-source projects.

1.3 Problem Statement

Although datasheet-based loss estimation is widely used, comparing semiconductor devices across converter topologies remains difficult. Some approaches are too simplified to capture the relevant loss mechanisms; others require detailed device models and extensive parameter identification. Manufacturer tools make device selection easier, but generally restrict comparisons to their own products and disclose little about the underlying calculations. This thesis addresses that gap with a unified, datasheet-based application for estimating conduction and switching losses under defined operating conditions.

1.4 Scope of the Work

The work focuses on steady-state loss estimation for selected DC/DC and DC/AC topologies under defined modulation, duty-cycle, and temperature conditions. The models are limited to continuous-conduction-mode (CCM) operation and, for DC/DC conversion, to asynchronous topologies. Electromagnetic interference (EMI), circuit parasitics, and full electromagnetic device modelling fall outside the scope.

1.5 Thesis Purpose

This thesis develops a transparent MATLAB and Simulink application for estimating semiconductor-switch losses from the parameters available in a device datasheet. It supports several converter topologies and semiconductor technologies, including Si, GaN, and SiC devices.

The application is intended to overcome two common limitations of manufacturer tools: their dependence on predefined devices and topologies, and the limited visibility they provide into modelling assumptions. The proposed workflow instead allows the user to define

the topology, semiconductor technology, circuit parameters, thermal assumptions, and mission profile. After a run, the application reports the principal device-loss components and the resulting thermal evolution.

The main contribution is therefore an open-source, transparent, and reproducible framework for comparing devices from different manufacturers under the same assumptions. Academic users and practising engineers can inspect the calculations, modify the models, and evaluate each device within a common workflow.

1.6 Thesis Structure

Chapter 2 presents the theoretical basis for converter-loss mechanisms and loss estimation. Chapter 3 defines the scope and intended contribution of the application. Chapter 4 explains the MATLAB App Designer backend and the simulation workflow, while Chapter 5 describes the Simulink models for the supported topologies and semiconductor technologies. Chapter 6 evaluates an IGBT boost-converter case study through a hand calculation and comparison with IPOSIM. Chapter 7 closes the thesis with its conclusions, limitations, and directions for future work.

2 Loss Estimation Tools

2.1 General Modelling Approach

Loss estimation is needed to quantify converter efficiency and compare semiconductor technologies under the same operating conditions. Several methods are available. This thesis does not use a full physics-based semiconductor model; instead, it works with practical parameters reported in device datasheets. That level of detail suits a MATLAB-based comparison tool because it captures the main electrical and thermal effects without requiring proprietary device structures or extensive physical-model data.

For the selected DC/DC and DC/AC topologies, the total semiconductor loss can be expressed as the sum of the main loss components:

$$P_{\text{loss}} = P_{\text{cond}} + P_{\text{sw}} + P_{\text{diode}} + P_{\text{Coss}} + P_{\text{gate}} + P_{\text{dt}}$$

where P_{cond} denotes conduction loss, P_{sw} switching loss, P_{diode} diode- or reverse-recovery-related loss, P_{Coss} output-capacitance loss, P_{gate} gate-drive loss, and P_{dt} dead-time or reverse-conduction loss. Not every term applies to every device or topology. An IGBT model, for example, does not use $R_{\text{DS(on)}}$, while a GaN HEMT has no conventional body diode. The application therefore adapts its loss model to the selected semiconductor technology.

Conduction loss is the power dissipated while the device is in the on-state and current flows through it. For MOSFET, including Si MOSFETs, SiC MOSFETs, and GaN HEMTs, conduction loss is usually represented by:

$$P_{\text{cond}} \approx I_{\text{rms}}^2 R_{\text{DS(on)}}(T_j)$$

where I_{rms} is the RMS drain-to-source current and $R_{\text{DS(on)}}(T_j)$ is the on-state resistance at junction temperature T_j. This temperature dependence matters because $R_{\text{DS(on)}}$ rises as the device heats during continuous operation. In high-voltage Si MOSFETs, the drift region contributes substantially to on-state resistance because it must be thick enough to sustain the blocking voltage. SiC's higher critical electric field permits a thinner drift region and lower on-state resistance, which helps explain the use of SiC MOSFETs as replacements for silicon IGBTs in high-voltage applications [1]. In GaN HEMTs, both temperature and dynamic $R_{\text{DS(on)}}$ can affect conduction loss [2, 3].

For IGBTs, conduction loss is calculated from the collector to emitter saturation voltage rather than $R_{\text{DS(on)}}$. A practical approximation is:

$$v_{CE}(i, T_j) \approx V_{CE0}(T_j) + r_{CE}(T_j)i$$

so that the average conduction loss can be obtained from the current waveform. This makes IGBT conduction modelling different from MOSFETs, since the IGBT has a voltage drop.

Switching loss occurs during turn-on and turn-off transitions, when voltage and current overlap for a given time. A practical energy-based expression is:

$$P_{\text{sw}} \approx f_{\text{sw}} \left(E_{\text{on}} + E_{\text{off}} \right)$$

where f_{sw} is the switching frequency and E_{on} and E_{off} are the turn-on and turn-off switching energies. These energies depend on DC-link voltage, current, junction temperature, gate resistance, gate-drive voltage, and loop parasitics. In IGBTs, the turn-off energy is strongly influenced by tail current caused by stored minority carriers. This limits the practical switching frequency of IGBT converters. In Si, SiC, and GaN MOSFET-like devices, switching can be faster because conduction is mainly based on majority carriers, although capacitive effects, layout inductance, and electromagnetic interference become more important at high switching speed [4][5].

Diode-related losses are relevant in topologies where current flows through an external diode, a body diode, or an equivalent reverse-conduction path. The forward conduction loss of a diode may be calculated as:

$$P_{\text{diode,cond}} \approx V_F I_{\text{avg}} + R_{\text{on}} I_{\text{rms}}^2$$

where V_F is the forward voltage drop, R_{on} is the diode on-state resistance, I_{avg} is the average diode current, and I_{rms} is the RMS diode current. In silicon PiN diodes and in the body diode of many silicon MOSFETs, reverse-recovery charge can create additional loss during commutation. This recovery current increases switching stress and can significantly affect the turn-on loss of the complementary switch. By contrast, SiC Schottky or JBS diodes are majority-carrier devices and have negligible stored-charge reverse recovery. Their turn-off transient is mainly related to capacitive charging rather than minority-carrier recovery [6].

Output-capacitance loss is another important component, especially for fast WBD devices. The output capacitance C_{oss} depends on voltage, so its stored energy needs to be properly calculated. An appropriate definition is:

$$E_{\text{oss}}(V) = \int_0^V v C_{\text{oss}}(v)\, dv$$

The corresponding hard-switching loss contribution can be calculated as:

$$P_{\text{Coss}} \approx f_{\text{sw}} E_{\text{oss}}$$

depending on the converter topology and on whether the stored energy is dissipated or recovered. This term becomes increasingly relevant as switching frequency increases, particularly in GaN and SiC converters.

Gate-drive loss is the energy required to charge and discharge the gate of the device every switching cycle. At first, it can be estimated as:

$$P_{\text{gate}} \approx Q_g V_{GS} f_{\text{sw}}$$

where Q_g is the total gate charge and V_{GS} is the gate-drive voltage. This loss is usually small compared with conduction and switching losses in low-frequency converters, but it becomes more relevant in high frequency. Gate resistance also affects the switching transient, reducing gate resistance may reduce switching losses, but it can increase the dv/dt, therefore the voltage overshoot, ringing, and electromagnetic interference [4].

Dead-time loss is especially important in bridge-type converters. Dead time is introduced to avoid shoot-through between the higher and lower side active switches. During this interval the load current must flow through a reverse-conduction path. In Si MOSFETs, this path is usually the body diode. In GaN HEMTs, there is no conventional body diode, but reverse current can flow through third-quadrant channel conduction, producing a diode-like voltage drop [7]. Although GaN eliminates classical reverse-recovery charge, excessive dead time can still create significant reverse-conduction loss. This is why accurate dead-time control is important in high-frequency GaN bridge converters [7].

Overall, the loss mechanisms considered in this thesis are selected to balance model accuracy and implementation. The proposed application does not intend to replace SPICE, or manufacturer-specific electro-thermal simulations. Instead, it provides a transparent and configurable estimation tool that allows the user to compare technologies, converter topologies, and operating points using a consistent framework.

2.2 Datasheet-Based Loss Models

Datasheet-based loss estimation is one of the most common approaches for converter design in the earlier stages. It uses the static and dynamic information provided by the semiconductor manufacturer and the expected converter operating conditions. This method is efficient and suitable for implementation in a MATLAB app because it does not require detailed semiconductor model.

For conduction losses, the required information depends on the device type. For MOSFET-like devices, the main parameter is $R_{\text{DS(on)}}$, as a function of junction temperature. For IGBTs, conduction loss is normally calculated from $V_{CE(sat)}$ curves or from a linearized model of the form $v_{CE} \approx V_{CE0} + r_{CE} i$ [8][9]. For diodes, the equivalent model can be based on a forward voltage drop and a differential on-state resistance.

Switching losses are commonly estimated using the turn-on and turn-off energy values provided in the datasheet. The basic expression is:

$$P_{\text{sw}} = N_{\text{sw}} f_{\text{sw}} \left(E_{\text{on}} + E_{\text{off}} \right)$$

where N_{sw} is the number of devices or commutations considered, depending on the converter topology. In practice, E_{on} and E_{off} are not constant. They are measured under specific test conditions and depend on current, DC-link voltage, gate resistance, gate-drive voltage, and junction temperature [9].

The main advantage of datasheet-based tools is their simplicity. They are fast, transparent, and suitable for comparing multiple devices. However, their accuracy is limited by the information available in the datasheet. The data of the device is often provided only at a couple of operating points, and the real converter may have different parasitic components, gate-drive conditions, and thermal behavior. As a result, the linear approximations may become inaccurate when non-linear effects dominate, such as IGBT tail current, diode reverse recovery, nonlinear output capacitance, dynamic $R_{\mathrm{DS(on)}}$ in GaN devices, or strong layout-dependent overshoot.

For this reason, manufacturers often use Double Pulse Testing (DPT) to characterize switching behaviour under controlled conditions. DPT allows the extraction of turn-on energy, turn-off energy, reverse-recovery behaviour, voltage overshoot, current slopes, and switching waveforms for a specific device and gate-drive configuration. These measurements improve confidence in efficiency and junction-temperature predictions, especially when datasheet conditions are not representative of the final converter design [10].

In this thesis, datasheet-based models are used as the foundation of the MATLAB loss-estimation platform. The objective is to keep the model transparent and editable, allowing the user to modify device parameters directly while still capturing the main loss mechanisms that determine converter efficiency.

2.3 Behavioural and Lookup-Table Approaches

Behavioral models and lookup tables provide more detail than basic datasheet equations without requiring a full physical model of the semiconductor. These methods use measured or manufacturer-provided data to describe how a device behaves under different operating conditions. The data may relate current and temperature to conduction voltage or resistance, switching energy, diode recovery energy, and thermal impedance.

A typical lookup-table model uses current, voltage, junction temperature, and sometimes gate resistance as inputs. During simulation, the model interpolates between stored values to estimate the losses at each operating point. Conduction losses can be calculated from characteristics such as $V_{\mathrm{CE}}(I, T_j)$, $V_{\mathrm{F}}(I, T_j)$, or $R_{\mathrm{DS(on)}}(T_j)$. Similarly, switching losses can be estimated from $E_{\mathrm{on}}(I, V, T_j)$ and $E_{\mathrm{off}}(I, V, T_j)$ data.

This approach is well suited to converter-level simulation because it captures important nonlinear behaviour without modelling the internal semiconductor structure. However, its accuracy depends on the quality and range of the available data. Results become less reliable when the device operates outside the conditions covered by the tables.

In modern power electronics workflows, lookup-table models are often coupled to a thermal network. The electrical model calculates instantaneous or average losses, and the thermal model updates the junction temperature. The updated temperature is then sent back into the electrical loss calculation. This electro-thermal interaction is important because most semiconductor loss parameters depend on temperature. Onsemi, for example, describes PLECS thermal models as lookup tables for conduction and switching losses combined with a thermal model, using interpolation and extrapolation during simulation [11]. Similar table-based approaches are commonly used in system-level studies where loss maps are coupled to thermal models [12]. In some cases, manufacturers directly provide these tables to support high-level simulation workflows [13].

Compared with basic datasheet models, behavioral and lookup table approaches can capture better nonlinear effects on current, voltage, and temperature. They are useful when the device operates over a wide load range. Nevertheless, their accuracy depends strongly on the quality, density, and representativeness of the data. Sparse tables may require extrapolation, which in some cases can introduce significant errors if the converter operates outside the characterized range.

For the MATLAB platform developed in this thesis, lookup-table modelling represents a possible extension of the datasheet-based approach.

2.4 Thermal Modelling Approach

Thermal modelling is necessary because semiconductor losses and junction temperature—the temperature within the active region of the device—affect each other. Electrical losses produce heat, while the resulting temperature rise changes the device's electrical behavior. Parameters such as $R_{\mathrm{DS(on)}}$, $V_{\mathrm{CE(sat)}}$, E_{on}, E_{off}, diode forward voltage, and reverse-recovery characteristics can therefore vary with junction temperature. If temperature effects are neglected, converter losses may be underestimated or overestimated, particularly at high currents or switching frequencies.

The heat-transfer path of a power semiconductor can be represented by an equivalent network of thermal resistances. Under steady-state conditions, where temperatures no longer change with time, the junction temperature can be estimated using:

$$T_j = T_a + P_{\mathrm{loss}} R_{\mathrm{th,ja}}$$

where T_a is the ambient temperature and $R_{\mathrm{th,ja}}$ is the total junction-to-ambient thermal resistance. If the thermal path is separated into different layers, the expression can be written as:

$$T_j = T_a + P_{\mathrm{loss}} \left(R_{\mathrm{th,jc}} + R_{\mathrm{th,ch}} + R_{\mathrm{th,ha}} \right)$$

where $R_{\mathrm{th,jc}}$ is the junction-to-case thermal resistance, $R_{\mathrm{th,ch}}$ the case-to-heatsink thermal resistance, and $R_{\mathrm{th,ha}}$ the heatsink-to-ambient thermal resistance.

For transient operation, thermal impedance models are more appropriate than a single thermal resistance. Foster and Cauer networks are commonly used to represent the dynamic temperature response of the device and heatsink. A Foster network represents the thermal impedance as a sum of exponential terms:

$$Z_{\mathrm{th}}(t) = \sum_{k=1}^{n} R_k \left(1 - e^{-t/\tau_k} \right)$$

where R_k is the thermal resistance of each branch and τ_k is the corresponding thermal time constant. This representation is convenient for fitting manufacturer thermal-impedance curves. Cauer networks, on the other hand, represent the physical heat-flow path more directly, which can be useful when modelling heat propagation through the package, thermal interface material, heatsink, and ambient environment.

In the proposed MATLAB platform, the thermal model is used to estimate the device junction temperature from the calculated losses. This allows the user to evaluate not only efficiency, but also whether the selected semiconductor technology and cooling assumptions are thermally reasonable. The thermal model also provides the basis for future mission-profile analysis, where losses and temperature may vary over time instead of being calculated at a single operating point.

2.5 Functional Requirements for the Proposed Loss-Estimation Platform

The review of the loss mechanisms and existing software tools help define the requirements of the platform developed in this thesis. The objective is not only to calculate a numerical efficiency value, but to create a complete and traceable workflow in which the user can move from a converter specification to semiconductor loss, thermal behavior, and technology comparison. Therefore, the tool must connect four modeling layers: the converter operating point, the semiconductor parameters, the circuit, and the processing stage.

The first requirement is *topology flexibility*. The platform must support more than one converter family, because the relevant loss mechanisms is different in different DC/DC and DC/AC systems. In the implemented version, the selected topologies are the Boost converter, Buck converter, Flyback converter, half-bridge inverter, full-bridge inverter, and three-phase inverter. This selection was made to cover both single switch and multiswitch converters, non-isolated and isolated DC/DC converters, and bridge inverter structures. As a result, the tool can be used to compare how the same semiconductor technology behaves in different electrical conditions.

The second requirement is *technology-dependent parameterisation*. A single device input form is not sufficient if all semiconductor technologies are treated with the same equations. For this reason, the developed platform distinguishes between Si MOSFETs, SiC MOSFETs, GaN MOSFETs, and Si IGBTs. The input fields change depending on the selected technology. For example, an SiC MOSFET or an IGBT can ask and use datasheet switching energies E_{on} and E_{off}, while an Si MOSFET or GaN device can be evaluated from charge-related data such as Q_g and Q_{oss}. This flexible input structure makes it possible to compare technologies even when the datasheet information is not the same.

The third requirement is *explicit modeling of reverse-conduction paths*. In DC/DC converters, the diode fields represent the output rectifier, freewheel diode, or secondary rectifier depending on the topology. In bridge converters, the same fields represent the body diode, antiparallel diode, or GaN reverse-conduction path. This distinction is important because diode-related loss can be one of the dominant differences between Si, SiC, and GaN technologies. In particular, GaN devices do not have a classical body diode, so their reverse conduction must be represented as a third-quadrant conduction path rather than as a stored-charge recovery mechanism.

The fourth requirement is *consistent waveform-based post-processing*. Manufacturer tools frequently hide the internal data flow from the user. In contrast, the application stores the simulation results and then calculates losses from the signals exported to the MATLAB workspace using transparent equations. This makes the result easier to interpret and trace.

It also makes the platform easier to extend, because future lookup-table can replace the present equations without changing the workflow.

The fifth requirement is *thermal and mission profile capability*. A single operating point is useful for preliminary comparison, but many converters do not operate continuously at a fixed load. For this reason, the platform includes a mission profile mode in which the user defines a sequence of operating steps with possibly different voltage, power, duration, and ambient temperature values. The electrical simulation is performed at each operating point, so for 10 operatings points, 10 simulations are done, while the long-duration thermal evolution is propagated using a thermal impedance model, and no thermal network is used.

These requirements help position the proposed application relative to the existing tools. Manufacturers' tools are generally more accurate for specifics models and device library, while the MATLAB platform developed in this thesis is more transparent, easier to modify and to adapt to specific needs. The main contribution is not a replacement of a existing tool, but the creation of an open source and research-oriented application.

2.6 Existing Loss Estimation Tools

Some commercial and manufacturers provide tools to estimate semiconductor losses in power converters. These tools are useful references because they show how industrial workflows combine device parameters, converter operating points, and thermal models. However, many of them are restricted to specific models, and topologies. The MATLAB platform will provide a more transparent and configurable academic tool for comparing different semiconductor technologies across selected converter topologies.

The available tools can be compared using the following criteria:

- **Traceability**: whether the user can view or edit the parameters used for loss estimation of the main switch device, diode recovery, and thermal impedance, or whether the tool only provides final results.
- **Flexibility**: whether the tool supports only one converter type or technology, or allows several configurations.
- **Electrothermal capability**: whether the tool calculates only electrical losses or also estimates junction temperature using a thermal model.
- **Mission profile support**: whether the tool evaluates always a fixed operating point or can process load cycles and variable operating conditions.
- **Integration**: whether the user can integrate the tool with external models.

Manufacturer Tools

- **IPOSIM** is a web-based, PLECS-powered environment for estimating power losses and electro-thermal behavior of Infineon power semiconductors. It allows the user to select a converter topology, define operating conditions, choose a Infineon device, and evaluate the losses and temperatures for a single operating point or a variable

cycle. It can also compare several Infineon devices side by side. Its main limitation is that it is tied to Infineon devices and predefined workflows.

- **STPOWER Studio** is an online electro-thermal simulation tool of STPOWER devices, mainly focused on three-phase, two-level DC/AC applications. It uses a time stepped electrothermal calculation in which conduction and switching losses are calculated as a function of operating conditions. The tool can offer a junction temperature evolution using transient thermal impedance. Its scope is limited to ST devices and supported topologies (DC/AC).

- **Elite Power Simulator** from onsemi is a PLECS-based simulation environment for loss and electro-thermal prediction using onsemi device models. The tool provides estimation of conduction losses, switching losses, and thermal data, and it can use heatsink models based on Foster or Cauer networks. It is limited to the available onsemi device libraries and supported converter structures.

- **Mitsubishi Electric Power Module Loss Simulator** is a tool for estimating losses and junction-temperature rise in Mitsubishi power modules. It is focused on two-level and three-level inverters. The results include separated IGBT and diode losses, temperature rise, and estimated junction or case temperatures. It can also generate characteristic curves, such as loss versus switching frequency or loss versus output current, which is relevant for sensitivity analysis.

- **Fuji IGBT Simulator** is a PLECS-based tool for estimating losses and temperature rise in Fuji IGBT power modules. It is oriented toward inverter applications, particularly two-level and three-level three phase inverters. Therefore, it is very limited, outside IGBT modules of Fuji.

- **SemiSel** is an online tool for selecting power semiconductors based on losses, temperatures, and efficiency under application-relevant conditions. It supports both single operating points and load cycles, making it useful for preliminary device selection and thermal evaluation.

- **GaN Power Bench** provides loss estimation for buck and boost, for EPC eGaN FETs. It also includes a thermal calculator for estimating thermal evolution after the electrical losses have been calculated. Its main advantage is its focus on GaN based converter, while its limitation is that it is restricted to EPC devices and specific converter types (buck and boost).

- **Toshiba Online Circuit Simulator** is an online simulator for MOSFETs. It allows the user to modify the MOSFET and circuit constants, compare waveforms, and evaluate power conversion efficiency. It includes predefined power topologies, including AC/DC PFC stages and DC/DC converter configurations.

- **TI MOSFET Power Loss Calculator** is an online calculator for quick MOSFET selection in synchronous buck converters. The user enters application parameters and selects the relevant controller or device configuration. The tool then estimates MOSFET losses, and ranks candidate devices.

Other Tools

- **PyPowerSim** is a Python library for loss estimation of converters and thermal analysis of them. It implements standard converter architectures such as half-bridge, full-bridge, three-phase inverters, and dual-active bridge converters. It can steady-state studies, and transient simulations, reporting conduction losses, switching losses, and temperatures. Unlike manufacturers' tools, it is script-based without an graphical interface, so it requires more programming effort.

To summarize, existing tools show that loss estimation is normally based on a combination of device data, converter waveforms, and thermal modeling. However, available tools are specific for the manufacturer that designed it, and restricted to specific topologies.

3 Scope and Contribution of the Loss-Estimation Platform

3.1 Existing Tools and the Intended Contribution of the Platform

Several software tools can estimate power losses in semiconductor devices. These range from manufacturer web applications and spreadsheet calculators to PLECS-based environments and open-source packages. They are useful for industrial device selection because they often include validated device data, switching-energy curves, thermal-impedance models, and predefined converter topologies. However, many are tied to one manufacturer's product range, a limited device library, or a fixed set of converter structures.

This restriction becomes important when several semiconductor technologies must be compared under the same assumptions. A comparison of a Si MOSFET, Si IGBT, SiC MOSFET, and GaN HEMT may require different tools, input formats, and calculation methods. The final results can therefore reflect differences between the tools as well as differences between the devices themselves. This makes a direct and transparent comparison more difficult.

The platform developed in this thesis addresses this problem through a common loss-estimation workflow in MATLAB and Simulink. The user selects a converter topology and semiconductor technology, enters the relevant circuit and device data, defines the thermal conditions, and runs the analysis. The overall procedure remains consistent across the supported technologies, while the equations and parameters change according to the selected device type.

The main contribution is a configurable framework for comparing Si, SiC, and GaN devices under consistent electrical and thermal conditions. It allows the user to examine how semiconductor parameters, converter topology, duty cycle, switching frequency, and cooling conditions affect conduction loss, switching loss, diode or reverse-conduction loss, efficiency, and junction temperature. Here, junction temperature refers to the temperature of the active semiconductor region inside the device.

Transparency is a second contribution. The equations, assumptions, parameters, inputs, and outputs remain accessible and editable, unlike in many closed manufacturer tools. The user can therefore trace how the platform obtains its loss and temperature estimates. This is relevant to the thesis because the purpose is not only to produce numerical results, but also to understand how each modelling choice influences the comparison.

The method still has limits. Its accuracy depends on the quality of the datasheet information and on how the user interprets and enters that information. Datasheet values may also represent typical test conditions rather than every operating point reached by the converter. The results should therefore be treated as engineering estimates, not as final design guarantees. Within this boundary, the platform occupies a useful position between idealised hand calculations and detailed proprietary simulation tools. It remains sufficiently open for studying the relative effects of semiconductor technology, topology, operating point, and thermal assumptions in selected DC/DC and DC/AC converters.

A comparison of the available tools is provided in Appendix 8.1, Table 8.1.

3.2 Semiconductor Devices Considered

The platform includes four main semiconductor technologies: silicon MOSFETs, silicon IGBTs, GaN HEMTs, and SiC MOSFETs. SiC cascode JFETs are also considered as a related wide-bandgap alternative. Together, these devices cover common choices across low-, medium-, and high-power conversion, although no single device family is preferable under every operating condition.

Silicon devices provide the reference case. Silicon has a bandgap of approximately 1.12 eV and a critical breakdown field of about 0.3 MV/cm [14]. The bandgap is the energy needed to move an electron into a conducting state, while the critical breakdown field indicates how much electric field the material can withstand. In a high-voltage unipolar device, silicon's relatively low critical field requires a thicker drift region to block a given voltage. This region carries current when the device is on, so increasing its thickness also increases resistance and conduction loss [15]. This trade-off helps explain why silicon MOSFETs are generally more suitable for low- and medium-voltage applications than for very high voltages.

Silicon MOSFETs are available in planar, trench, and superjunction structures. They are widely used in DC/DC converters, synchronous rectifiers, and low- to medium-power inverter legs, particularly when relatively high switching frequency is required. In the platform, they are represented using datasheet parameters such as on-state resistance, internal capacitances, body-diode characteristics, and gate-drive data. These parameters provide a practical description of conduction and switching behaviour without modelling the internal semiconductor structure in detail.

Silicon IGBTs are included because they remain common in high-power converters. An IGBT uses minority carriers to reduce conduction loss at high blocking voltages. However, charge stored in its drift region produces a tail current during turn-off, which can raise switching loss compared with a MOSFET. IGBTs are therefore generally associated with high-power applications that operate at relatively low switching frequencies; the cited manufacturer guidance discusses operation up to approximately 3 kHz [16]. The platform represents an IGBT mainly through its collector–emitter saturation voltage, internal capacitance, switching data, and the parameters of its accompanying freewheeling diode.

GaN and SiC belong to a group known as wide-bandgap semiconductors. Their wider bandgaps and higher critical electric fields allow a thinner drift region for a given blocking voltage. This can reduce resistance and support faster switching than conventional silicon

devices. At converter level, these properties may reduce semiconductor loss and permit a higher switching frequency, which can in turn reduce the size of inductors, transformers, and capacitors. These benefits are not automatic, however, because packaging, gate driving, circuit layout, thermal design, and operating conditions also affect performance.

GaN power switches are commonly produced as lateral high-electron-mobility transistors, usually called GaN HEMTs. They are particularly relevant to low- and medium-voltage converters, commonly in voltage classes up to 650 V, where fast switching can support compact high-frequency designs [17]. Their value is most apparent when switching loss or passive-component size is a major design constraint.

For loss estimation, the platform treats GaN HEMTs as unipolar devices with resistive on-state conduction. Unlike a conventional silicon MOSFET, a GaN HEMT has no body diode, so it does not show the same body-diode reverse-recovery process [18]. Reverse current can still flow through the channel in the third quadrant, producing a diode-like voltage drop during dead time. Dead time is the short interval when both switches in a converter leg are off to prevent a direct short circuit. At high switching frequencies, loss during this interval may become significant [18]. The GaN model therefore uses parameters such as $R_{\mathrm{DS,on}}$, gate charge, output charge or capacitance-related energy, and reverse-conduction characteristics.

SiC devices are considered mainly for higher-voltage and higher-power applications. SiC offers higher thermal conductivity than silicon and GaN and can support higher voltage, temperature, and switching frequency than conventional silicon devices such as IGBTs [17][19]. Commercial SiC devices are widely available in 1200 V and 1700 V classes. These ratings make them relevant to traction inverters, fast chargers, photovoltaic inverters, and other high-power conversion systems.

The main SiC switch modelled in this thesis is the SiC MOSFET, in either planar or trench-gate form. Compared with silicon MOSFETs and IGBTs, SiC MOSFETs can offer lower switching loss, higher blocking voltage, and better operation at elevated temperature. They still contain a body diode, however, and its reverse-recovery behaviour can increase switching loss and voltage stress in a hard-switched converter [20]. The platform therefore represents SiC MOSFETs through on-state resistance, switching-energy data, gate-drive parameters, and body-diode characteristics.

The SiC cascode JFET provides another wide-bandgap option. It combines a normally-on, high-voltage SiC junction field-effect transistor (JFET) with a low-voltage silicon MOSFET, creating a normally-off three-terminal device. This arrangement avoids a SiC MOS gate oxide. At the same time, it behaves as a coupled pair of devices, which can complicate its transient and failure behaviour under severe conditions [21][22]. The platform treats this device at a behavioural level through equivalent conduction and switching parameters rather than through a detailed physical model.

Taken together, these technologies provide a practical basis for comparison. Silicon devices establish the conventional reference, while GaN and SiC represent alternatives that may support faster switching or greater power density. The platform applies the same converter topologies and operating conditions to each technology so that differences in estimated loss, efficiency, and thermal performance can be linked more directly to device parameters. The comparison remains conditional on the selected devices and data, rather than proving that one semiconductor technology is superior in all applications.

3.3 Converter Topologies Included in the Platform

The MATLAB/Simulink application estimates semiconductor losses in a selected set of DC/DC and DC/AC converter topologies. Its purpose is not to complete the electrical design of each converter. Instead, the selected circuits provide a common test environment in which different semiconductor technologies can be compared under equivalent operating conditions.

The DC/DC group consists of buck, boost, and flyback converters. A buck converter reduces a DC voltage, whereas a boost converter increases it. A flyback converter transfers energy through a coupled magnetic component and can provide electrical isolation. These circuits are common in power supplies, renewable-energy interfaces, battery systems, and auxiliary power electronics. They also expose semiconductor devices to different loss mechanisms, including hard switching, diode freewheeling, reverse recovery, and, in the flyback converter, transformer-related effects.

The DC/AC group contains a half-bridge inverter, a full-bridge inverter, and a two-level three-phase inverter. These voltage-source converter structures represent common single-phase and three-phase stages used in motor drives, grid-connected converters, traction systems, and renewable-energy systems. Their semiconductor losses depend on the device parameters and on system-level conditions such as the modulation method, switching frequency, load current, power factor, and DC-link voltage.

For each supported topology, the platform estimates the principal device-level loss components. These include conduction loss, turn-on and turn-off switching loss, diode or reverse-conduction loss, gate-drive loss where relevant, and loss associated with charging and discharging the output capacitance. The thermal model then relates the total dissipated power to the resulting device temperature. Using the same calculation structure across the selected converters provides a consistent basis for comparing silicon, SiC, and GaN devices, while the stated modelling limits remain part of the interpretation.

4 MATLAB App Algorithm and Back-end Implementation

4.1 Backend Architecture

The application was developed in MATLAB App Designer, in which both the graphical interface of the application, and the back-end were written and designed. The logic of the code is not only to collect the datasheet data and run the simulation, but to organise the calculation and collection sequence required to estimate semiconductor losses. This chapter focuses on the internal algorithm used by the app.

The app is implemented as a single MATLAB class. This class contains the graphical components, internal state variables, validation functions, export functions, execution functions, loss calculation functions, and plotting functions. Instead of using independent scripts for each converter topology, the app follows a common backend workflow that adapts itself according to the selected topology and semiconductor technology.

The general backend sequence is shown in Figure 4.1. First, the selected topology, switch technology, and diode type are stored. The app then loads its default values and shows the required parameter groups. Once the circuit, semiconductor, diode, and thermal parameters have been defined, the application validates the input data. If the configuration is acceptable, the parameters are exported to the MATLAB workspace to be then used by the corresponding Simulink model. The selected Simulink model is then executed, and the results stores in arrays are returned to the app. Finally, more functions are used to process the results to calculate the conduction losses, switching losses, diode and reverse-recovery losses, total loss, efficiency, and thermal quantities.

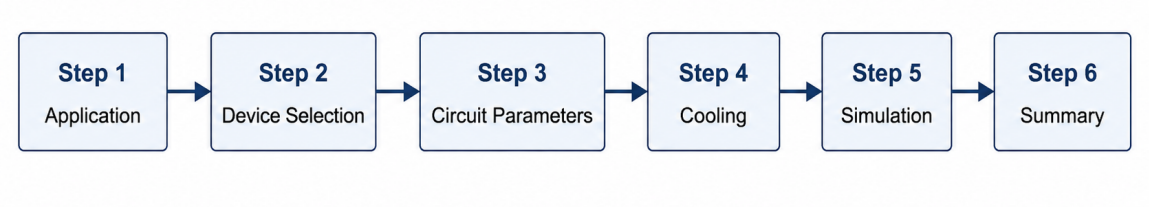


Figure 4.1: Backend workflow from configuration selection to simulation, post-processing, and final results.

A central element of the implementation is the structure `SimulationData`. This structure acts as the data container of the app. Before simulation, it stores the selected topology,

selected switch technology, diode type, circuit parameters, device parameters, diode parameters, and thermal assumptions. After simulation, it is extended with the Simulink output object and the processed results. This avoids recalculating values directly from interface fields after the simulation has finished and ensures that the summary values correspond to the exact configuration that was simulated.

The approach used makes the app easier to extend because new topologies or device technologies can be added by updating the model mapping and parameter export functions without changing the complete workflow.

4.2 Internal Configuration Logic

The first step internally is the converter topology. The selected topology is stored in the variable `SelectedTopology` which is used throughout the program to determine which circuit equations, default values, Simulink model, active switch count, and signal names have to be used.

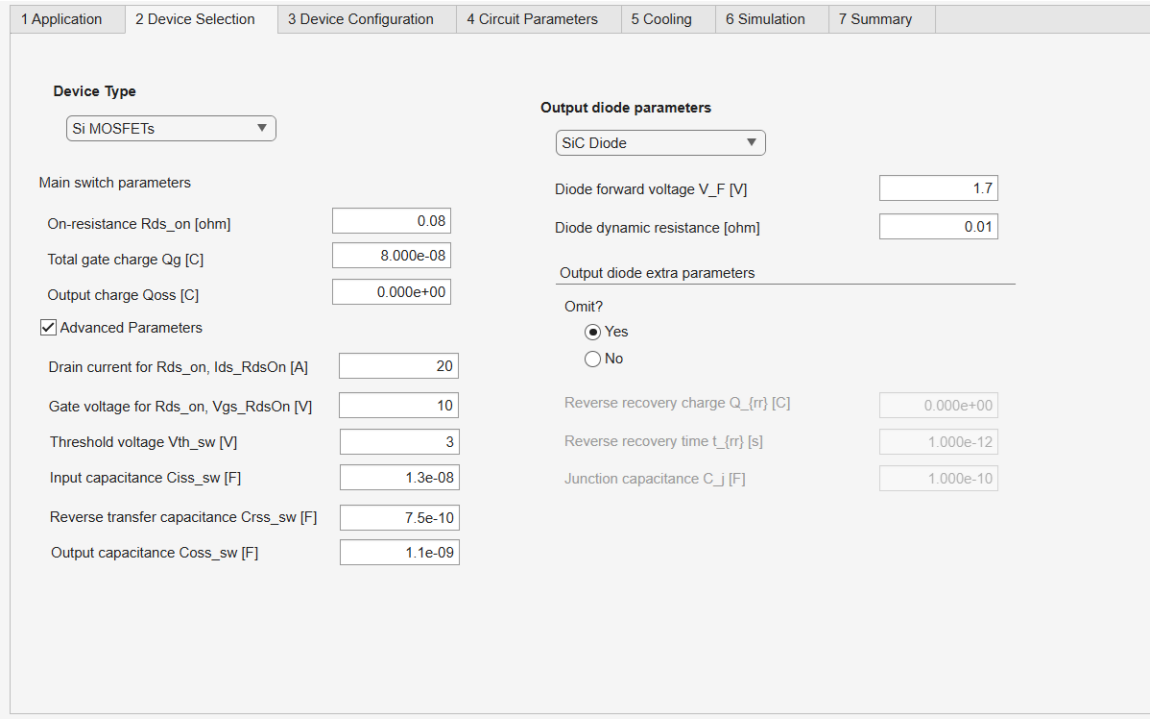


Figure 4.2: Application tab used to select the converter topology and simulation mode.

The topology selections are grouped into DC/DC and DC/AC converters. The DC/DC group includes the Boost, Buck, and Flyback converters. The DC/AC group includes the half-bridge inverter, full-bridge inverter, and a two-level three-phase inverter selection. The half-bridge and full-bridge have corresponding Simulink implementations, while the three-phase selection is currently supported only at the interface and backend level. Although these converters have different electrical circuits, the backend treats them through the same general logic: define an operating point, export the model variables, run the Simulink file, extract the results, and apply the loss model.

The topology selection also considers the number of active switches for the loss calculation. For the Boost, Buck, and Flyback converters, the switch count is one as the models are asynchronous and the diode is considered ideal. For inverter structures, the number of active switches increases according to the converter leg structure: two devices for the half bridge, four devices for the full bridge, and six devices for the 2 level three-phase inverter. This value is important because it defines how the app scales switching losses and how many device-current and device-voltage waveforms must be extracted from the Simulink output.

Table 4.1: Topology-dependent active switch count used by the backend.

Topology	**Active switches**	**Role in the algorithm**
Boost converter	1	Single-switch DC/DC loss calculation
Buck converter	1	Single-switch DC/DC loss calculation
Flyback converter	1	Primary-side switch loss calculation
Half-bridge inverter	2	Two device columns in waveform matrices
Full-bridge inverter	4	Four device columns in waveform matrices
Three-phase inverter	6	Six device columns in waveform matrices

The selected semiconductor technology gives way to the second step. The supported switch technologies are Si MOSFETs, Si IGBTs, GaN HEMTs, and SiC MOSFETs. Each technology requires a different set of parameters. MOSFET-like devices are mainly described by $R_{\mathrm{DS,on}}$, gate charge, output charge, output capacitance, and body-diode or reverse-conduction data. IGBTs are described by collector-emitter saturation voltage, switching energies, and IGBT-specific block parameters. GaN HEMTs are treated as devices without a conventional body diode, but with a relevant third-quadrant reverse-conduction path during dead time.

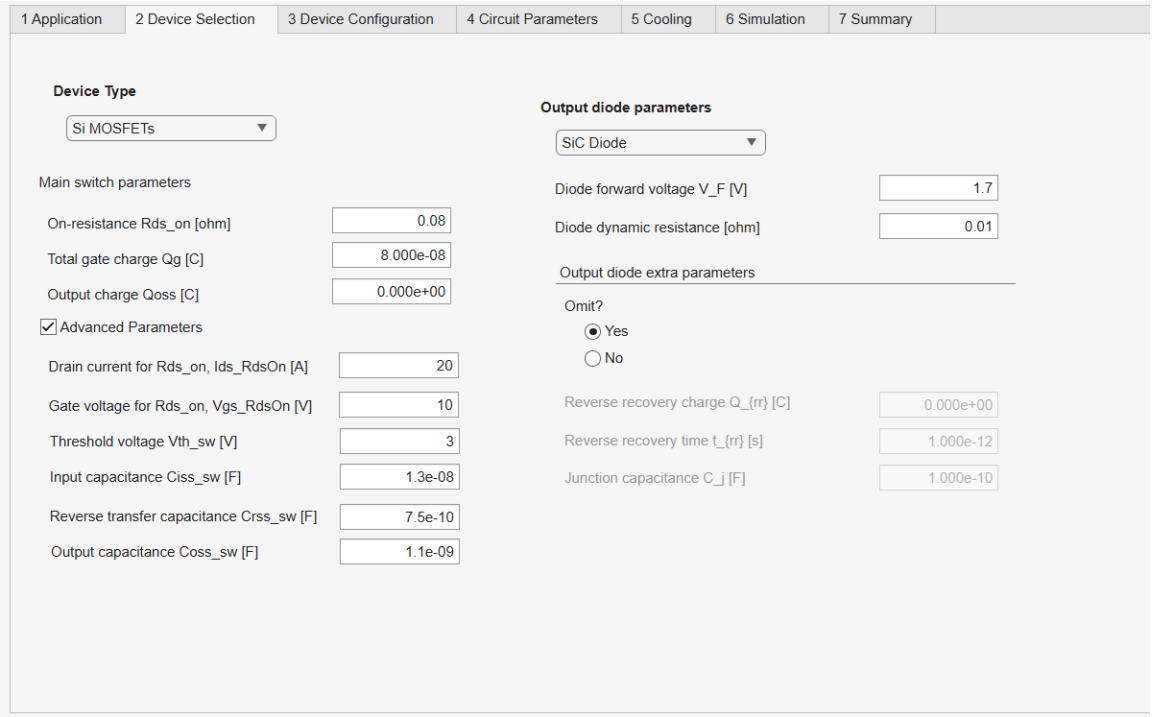


Figure 4.3: Device Selection tab used to define the semiconductor technology and diode configuration.

The diode type is treated separately from the main switch technology. In DC/DC converters, the diode parameters normally represent the internal body diode. In inverter topologies, they can represent an antiparallel diode, a MOSFET body diode, or reverse-conduction path.

4.3 Parameter Definition and Default Values

The backend contains default parameter sets for the implemented converter and semiconductor combinations. These values are used as initial values, and are expected to be replaced by the user. Nonetheless, the application can run the simulation usign these default values.

The thermal default values are stored in the same configuration logic. These include thermal resistance and Foster thermal impedance vectors. The Foster network is described by a vector of thermal resistances and a vector of time constants:

$$Z_{\mathrm{th}}(t) = \sum_{k=1}^{n} R_k \left(1 - e^{-t/\tau_k}\right). \tag{4.1}$$

Using vectors instead of a single thermal resistance allows the backend to represent transient temperature rise during mission-profile operation. If the user does not provide valid Foster vectors, the app falls back to the default thermal impedance value associated with the selected technology.

4.4 Input Validation and Operating-Point Construction

Before running any Simulink model, the backend executes a validation. The objective of this stage is to prevent any invalid value from being used in the simulation and producing an error.

The validation consists of checking if some parameters are numerical and positive, as well as some topology-specific checks. For the Boost converter, the output voltage must be greater than the input voltage, for instance.

For inverter topologies, the validation checks the DC-link voltage, output power, output frequency, switching frequency, output voltage definition, gate-drive voltage, and gate resistances. Device validation is also done by technology. MOSFET devices require a positive on-state resistance and valid charge or capacitance parameters. IGBTs require a positive saturation voltage and valid switching-energy values. When advanced parameters are enabled, those values are also checked.

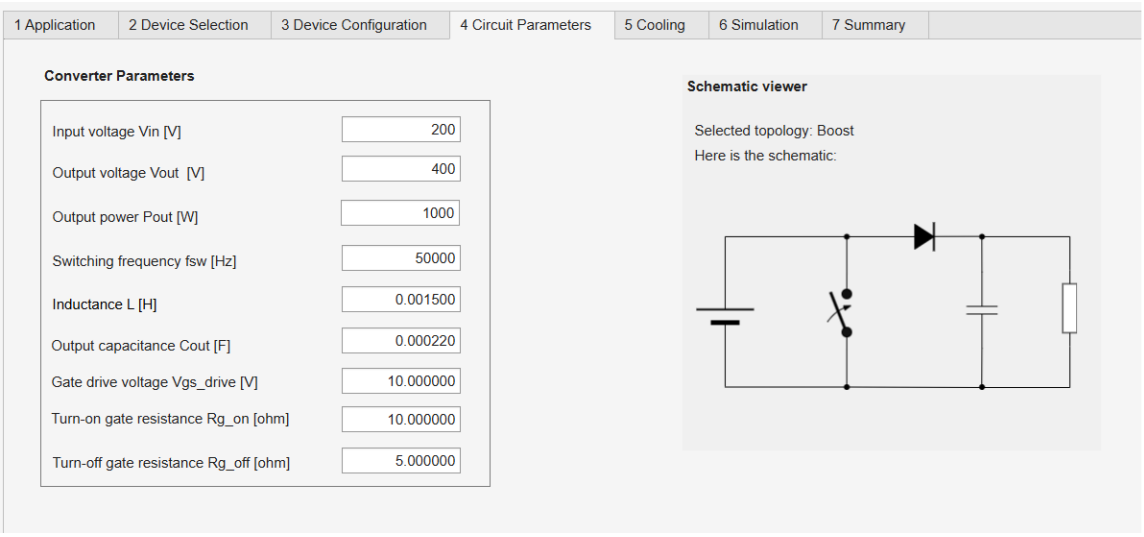


Figure 4.4: Circuit Parameters tab used to define the electrical operating point before simulation.

4.5 Parameter Export and Simulink Model Mapping

After validation, the applications exports the required variables to the MATLAB base workspace and, when necessary, to the model workspace. This design allows the Simulink blocks to remain parameterised using variable names such as `Vin`, `Vout_ref`, `fsw`, `RdsOn`, `Vf`, `RonD`, `Qg_sw`, `Qoss_sw`, `Eon_sw`, `Eoff_sw`, and `Rth_foster_sw`.

The backend assigns a technology-dependent dead time for inverter operation. A shorter dead time is used for GaN devices, an intermediate value for SiC MOSFETs, and a longer default value for Si MOSFETs. The sampling time is then selected as the smaller value between a fraction of the switching period and a fraction of the imposed dead time. This ensures that the dead-time interval is represented with enough numerical resolution in the

switching model.

The Simulink model is selected by the function `getImplementedModelName`. This function maps the pair formed by the selected topology and semiconductor technology to the corresponding Simulink file. This is a central part of the backend because the same application can execute different models. For example, the Boost converter can be simulated using different implementations depending on whether the selected device is a Si MOSFET, SiC MOSFET, GaN device, or IGBT. The same principle is used for the others topologies.

Before starting a simulation, the app loads the selected Simulink model and checks that it is not already running. If the model is active or paused, the app stops the previous execution before launching a new one. This avoids conflicts between consecutive simulations and prevents two executions from using the same model variables simultaneously.

4.6 Waveform Extraction and Signal Normalisation

After the Simulink simulation has finished, the output object is stored in `SimulationData.SimOut`. This is done thanks to the ToWorkspace blocks of Simulink, that sends the measured signals to the workspace, where they are taken for post-processing. For DC/DC converters, signals such as output voltage and current, switch voltage, switch current, body-diode voltage and current, PWM signal, and others are extracted.

4.7 Steady-State Reference Window

A key part of the loss algorithm is the selection of the waveform interval used for averaging. Using the entire simulated waveform would include the initial transient, where the inductor current, output capacitor voltage, or inverter load current may not yet have reached periodic steady state. To avoid this, the backend extracts a steady-state reference window before calculating average losses.

For DC/DC simulations with an available PWM signal, the app detects the rising edges of the gate command. These rising edges define the switching cycles. The default algorithm selects the last ten complete PWM periods as the reference interval:

$$T_{\mathrm{ref}} = t_{\mathrm{end,ref}} - t_{\mathrm{start,ref}}. \tag{4.2}$$

Using several switching cycles instead of a single cycle improves numerical stability, especially when the current ripple or diode recovery transient varies slightly between cycles. If the simulation does not contain enough complete PWM cycles, the backend falls back to the last 20 percent of the waveform.

For inverter models, the final averaging window must also be long enough to represent the fundamental current variation. Since the device current is modulated at the output frequency, the instantaneous losses are not constant from one switching period to the next. Therefore, the backend stores the waveforms over the steady-state part of the simulation and calculates average quantities from the selected interval. This avoids using a short switching-period average that would not represent a full AC operating condition.

The average of a generic waveform $x(t)$ over the selected interval is calculated using numerical integration:

$$\overline{x} = \frac{1}{t_2 - t_1} \int_{t_1}^{t_2} x(t), dt. \tag{4.3}$$

In the implementation, this operation is performed using the trapezoidal rule:

$$\overline{x} \approx \frac{\texttt{trapz}(t, x)}{t_{\text{end}} - t_{\text{start}}}. \tag{4.4}$$

4.8 Loss-Estimation Algorithm

The loss calculation is performed after the waveforms have been extracted and the steady-state interval has been selected. The backend separates the losses into switch conduction loss, switch switching loss, diode forward-conduction loss, reverse-recovery loss, total semiconductor loss, and efficiency.

Switch Conduction Loss

For MOSFETs, the instantaneous conduction loss is calculated from the switch current and the on-state resistance:

$$p_{\text{cond}}(t) = i_{\text{sw}}^2(t) R_{\text{DS,on}}. \tag{4.5}$$

If several active switches are present, the same expression is applied to each device column and then summed. The resulting waveform represents the total switch conduction loss of the converter.

For IGBT devices, the current implementation can use a simplified saturation-voltage model:

$$p_{\text{cond}}(t) = V_{\text{CE,sat}} |i_{\text{sw}}(t)|. \tag{4.6}$$

This is a first-order approximation. A more detailed IGBT model may use a linearised collector-emitter voltage of the form

$$v_{\text{CE}}(i) = V_{\text{CE0}} + r_{\text{CE}} i, \tag{4.7}$$

which would give

$$p_{\text{cond}}(t) = V_{\text{CE0}} |i_{\text{sw}}(t)| + r_{\text{CE}} i_{\text{sw}}^2(t). \tag{4.8}$$

The backend structure allows this extension because the conduction loss calculation is separated from the simulation execution logic.

Switching Loss from Waveforms

The algorithm first converts the PWM waveform into a logical gate signal and detects turn-on and turn-off edges:

$$\text{turn-on edge: } \Delta g(t) > 0, \qquad \text{turn-off edge: } \Delta g(t) < 0. \tag{4.9}$$

Around each detected edge, the algorithm opens a search window equal to a fraction of one switching period. Inside this window, it calculates pre-transition and post-transition median values of switch voltage and switch current. These median values are used instead of single samples to reduce sensitivity to numerical noise or ringing.

For turn-on events, the switch voltage normally decreases while the current increases. The algorithm estimates the beginning and end of the transition using 10–90 percent thresholds of the voltage and current changes. The instantaneous switching power is calculated as the magnitude of the voltage-current product:

$$p_{\text{sw}}(t) = |v_{\text{DS}}(t)|, |i_{\text{sw}}(t)|. \tag{4.10}$$

The switching energy of one event is then obtained by numerical integration:

$$E_{\text{sw,event}} = \int_{t_a}^{t_b} |v_{\text{DS}}(t) i_{\text{sw}}(t)|, dt. \tag{4.11}$$

The same logic is applied to turn-off events, but with the expected opposite voltage and current transition. Each detected event is stored with its type, start time, end time, energy, representative current, and representative voltage. The average switching power is then calculated from the total switching energy observed in the reference window:

$$P_{\text{sw}} = \frac{\sum E_{\text{sw,event}}}{T_{\text{ref}}}. \tag{4.12}$$

Diode and Reverse-Recovery Loss

The intrinsic diode or antiparallel diodes is processed separately from the main switch. The forward-conduction loss is calculated from the diode current as

$$p_{\text{D,fwd}}(t) = V_F I_F(t) + R_{\text{on,D}} I_F^2(t), \tag{4.13}$$

where

$$I_F(t) = \max(i_D(t), 0). \tag{4.14}$$

The reverse-recovery logic assumes that positive diode current represents forward conduction and negative diode current represents recovery current. A threshold is defined as a small fraction of the peak diode-current magnitude. The algorithm then detects continuous intervals where

$$i_D(t) < -I_{\text{thr}}. \tag{4.15}$$

Each detected interval is treated as a reverse-recovery event. Intervals shorter than a few simulation time steps are rejected to avoid numerical noise. For each valid event, the recovered charge is calculated as

$$Q_{\text{rr}} = \int_{t_a}^{t_b} -i_D(t), dt, \tag{4.16}$$

and the reverse-recovery energy is calculated as

$$E_{\text{rr}} = \int_{t_a}^{t_b} |v_D(t)|[-i_D(t)], dt. \tag{4.17}$$

The average reverse-recovery power over the observation window is then

$$P_{\text{rr}} = \frac{\sum E_{\text{rr}}}{T_{\text{ref}}}. \tag{4.18}$$

The backend applies this logic independently to the external diode and to the intrinsic body diode when both current and voltage signals are available. Therefore, the total diode-related loss is divided into forward conduction and reverse-recovery components:

$$P_{\text{D,total}} = P_{\text{D,ext,fwd}} + P_{\text{D,body,fwd}} + P_{\text{rr,ext}} + P_{\text{rr,body}}. \tag{4.19}$$

This separation is important because it allows the results to show whether the diode loss is mainly caused by forward conduction or by reverse-recovery events.

Total Loss and Efficiency

The total semiconductor loss is calculated as

$$P_{\text{loss,total}} = P_{\text{cond}} + P_{\text{sw}} + P_{\text{D,total}}. \tag{4.20}$$

The output power is calculated directly from the simulated voltage and current waveforms. For DC/DC and single-phase inverter cases,

$$p_{\text{out}}(t) = v_{\text{out}}(t) i_{\text{out}}(t). \tag{4.21}$$

For the three-phase inverter,

$$p_{\text{out}}(t) = v_a(t) i_a(t) + v_b(t) i_b(t) + v_c(t) i_c(t). \tag{4.22}$$

The average output power is obtained over the same steady-state reference window. The converter efficiency is then calculated as

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss,total}}} \times 100 \tag{4.23}$$

The processed values are stored in `SimulationData.Results`, including average output power, switch conduction loss, switching loss, external diode loss, body-diode loss, reverse-recovery loss, total loss, efficiency, switch RMS current, average switch current, and peak switch current.

4.9 Thermal Model and Mission-Profile Algorithm

The thermal model connects the electrical loss calculation with the junction-temperature estimation. In single operating-point simulations, the thermal parameters are exported with the electrical parameters so that the corresponding Simulink blocks can use them when thermal ports or temperature-dependent block parameters are enabled. In mission-profile mode, however, the app uses a different strategy.

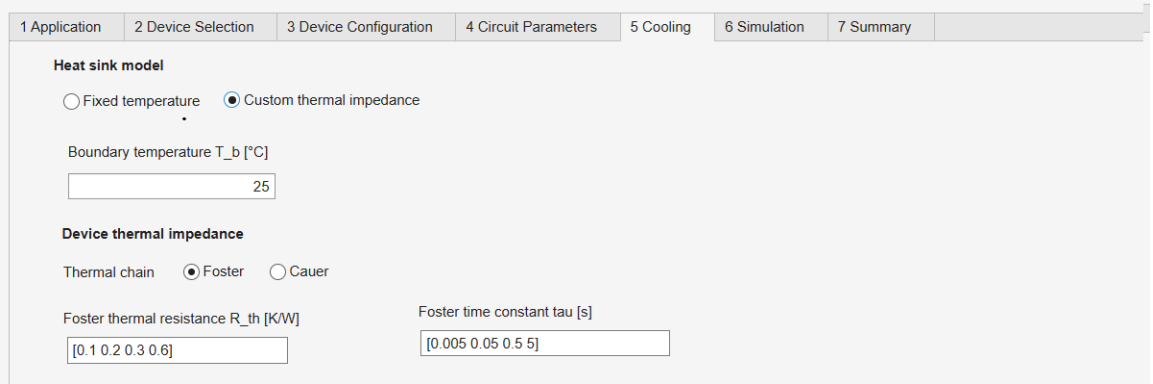


Figure 4.5: Cooling tab used to define the thermal parameters and mission-profile assumptions.

Running the full switching model for the real duration of a mission profile would be computationally inefficient. For example, simulating a converter at switching level for several minutes or one hour would require an excessive number of simulation time steps. Therefore, the backend separates the problem into two parts:

1. A short Simulink simulation is used to extract representative steady-state losses for each operating segment.
2. The real segment duration is used only in the analytical Foster thermal propagation and energy calculation.

Each mission-profile row defines one operating segment. For DC/DC mission profiles, the relevant inputs are segment duration, input voltage, output voltage, output power, and ambient or boundary temperature. For each segment, the backend temporarily updates the operating-point variables, executes a short simulation, extracts steady-state losses, and stores the segment results.

The MOSFET loss used as the heat source for the switch junction is

$$P_{\mathrm{MOSFET}} = P_{\mathrm{cond}} + P_{\mathrm{sw}}. \tag{4.24}$$

The external diode loss is not included in this heat source because the diode is treated as a separate component in the implemented DC/DC models. If the switch and diode were assumed to share the same package or thermal path, a combined thermal model would be required.

The Foster thermal network is implemented using a state variable for each branch. Each state x_k represents the temperature-rise contribution of one Foster branch. At the beginning of the mission profile, the thermal states are initialised to zero. For a segment of duration Δt, the state update is

$$x_{k,\mathrm{end}} = x_{k,\mathrm{start}} e^{-\Delta t/\tau_k} + P_{\mathrm{MOSFET}} R_k \left(1 - e^{-\Delta t/\tau_k}\right). \tag{4.25}$$

The junction temperature at the end of the segment is then

$$T_{j,\mathrm{end}} = T_b + \sum_{k=1}^{n} x_{k,\mathrm{end}}, \tag{4.26}$$

where T_b is the boundary temperature. The final state of one segment is used as the initial state of the following segment. This preserves the thermal memory of the semiconductor device across the complete mission profile.

For plotting, the same Foster equation is evaluated at intermediate time instants inside each segment. This produces a continuous junction-temperature trajectory instead of only one temperature value per segment. The backend also records the peak junction temperature reached during each segment.

The mission-profile algorithm stores both power and energy quantities. For segment k, the output energy and loss energy are calculated as

$$E_{\mathrm{out},k} = P_{\mathrm{out},k} \Delta t_k, \tag{4.27}$$

$$E_{\mathrm{loss},k} = P_{\mathrm{loss},k} \Delta t_k. \tag{4.28}$$

After all segments have been processed, the mission-average loss is calculated by energy weighting:

$$\overline{P}*_{\mathrm{loss,mission}} = \frac{\sum_k P * \mathrm{loss}, k \Delta t_k}{\sum_k \Delta t_k}. \tag{4.29}$$

The mission efficiency is obtained from the total output energy and total loss energy:

$$\eta_{\mathrm{mission}} = \frac{E_{\mathrm{out,total}}}{E_{\mathrm{out,total}} + E_{\mathrm{loss,total}}} \times 100 \tag{4.30}$$

In the current implementation, mission-profile execution is restricted to the DC/DC topologies. The app can define mission-profile templates for inverter cases, but the implemented execution loop currently processes Boost, Buck, and Flyback operating segments.

4.10 Result Generation and Backend Limitations

The final stage of the backend is the generation of summary results. For a single operating point, the app stores and displays the average conduction loss, switching loss, diode or reverse-path loss, total semiconductor loss, output power, and efficiency. For mission-profile operation, it stores the segment-by-segment losses, energy quantities, final junction temperatures, peak junction temperatures, mission-average losses, and mission efficiency.

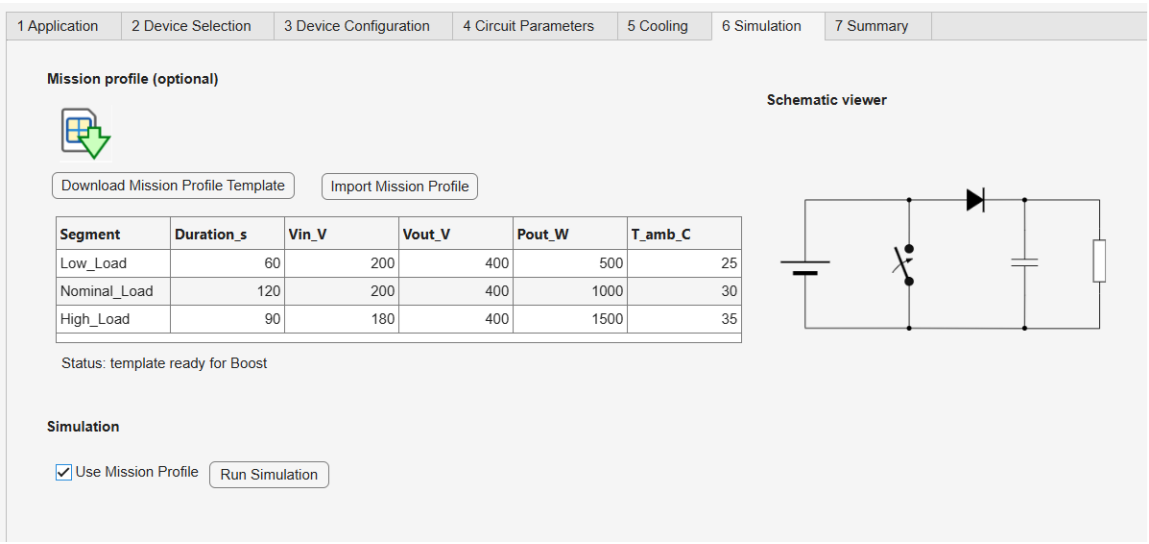


Figure 4.6: Simulation tab used to execute the selected model and display the processed loss-estimation results.

The results are generated from the processed data stored in `SimulationData.Results`. The current implementation should be interpreted as a first-order converter level loss and thermal estimation platform. The main objective is to provide a transparent and modular calculation workflow rather than a manufacturer grade electrothermal simulator. The most important limitations are related to switching-energy scaling, thermal feedback, and parasitic effects.

First, when datasheet switching energies are used directly, the implementation does not fully scale E_{on} and E_{off} with instantaneous current, blocking voltage, gate resistance, and junction temperature. In the waveform-based method, the switching energy is obtained from simulated voltage and current overlap, but the accuracy still depends on the fidelity of the Simulink device model and the available signal resolution.

Moreover, package parasitics, PCB trace inductance, layout-dependent ringing, electromagnetic interference effects, and detailed gate-driver dynamics are not fully represented. These effects are particularly important for fast-switching SiC and GaN devices. Therefore, the numerical results should be understood as engineering-level estimates suitable for comparative analysis, not as final design values.

Despite these limitations, the implemented backend provides a consistent framework for comparing semiconductor technologies under equivalent converter and operating assumptions.

5 Simulink Converter Models

5.1 Model Selection and Workspace Interface

The Simulink side of the application is as relevant as the back-end and the GUI designed in the App Designer. They are connected through the selected topology and technology, and the workspace-based parameter transfer. The function `getImplementedModelName` is the one that finds the correct Simulink model based on the combination of topology and technology. This mapping function is the key link between the App and Simulink, and ensures that the correct model is always loaded without requiring the user to manually open or modify anything.

As mentioned before, the application exports all parameters to the MATLAB workspace. The Simulink models have many blocks that are parametrized using variables, and these variables match those sent by the application, so they are read, and in that process, values are assigned to the different blocks parameters.

Simulink is used to obtain the electrical waveforms required for loss calculation. For mission-profile operation, the Simulink model is not run for the real duration of each segment, but each segment is simulated only a tiny period, enough to reach steady-state. The longer-time thermal evolution is then calculated in MATLAB using the Foster thermal model described in Chapter 4.

The user does not interact with Simulink directly at any point during normal operation. This makes the platform more practical for users who are primarily interested in the loss results rather than the details of the Simulink implementation. Nonetheless, the Simulink models are available for further refining or adaptation to specific needs or variants of topologies.

Dedicated Simulink models are available for the currently supported topology-technology combinations. Some additional combinations are already represented in the application interface and backend but do not yet have a corresponding validated Simulink model.

5.2 DC/DC Simulink Models

The DC/DC part of the platform is implemented using separate Simulink models for the Boost, Buck, and Flyback converters. As described in the previous section, the appropriate model is selected automatically by the app based on the topology and device combination chosen by the user. All converter parameters, device parameters, and diode parameters are passed through workspace variables before the simulation starts.

Boost Converter

For the Boost converter, the steady-state duty cycle is calculated from the voltage conversion ratio:

$$D = 1 - \frac{V_{\text{in}}}{V_{\text{out}}}. \tag{5.1}$$

Before exporting the parameters, the app verifies that $V_{\text{out}} > V_{\text{in}}$, since this is a necessary condition for boost operation. To reduce the simulation time needed to reach steady state, the inductor current is initialised using an estimate based on the input power balance:

$$I_{L,0} \approx \frac{P_{\text{out}}}{V_{\text{in}}}. \tag{5.2}$$

This initialisation does not guarantee an exact steady-state start, since it neglects converter losses and assumes ideal energy transfer, but it substantially reduces the duration of the initial transient compared to starting from zero.

Figure 5.1 shows the Boost converter model. The circuit consists of the DC input voltage source, a controlled semiconductor switch, the passive components, and a resistive load. The switch is driven by a PWM signal generated from the calculated duty cycle, and the relevant waveforms are logged for post-processing.

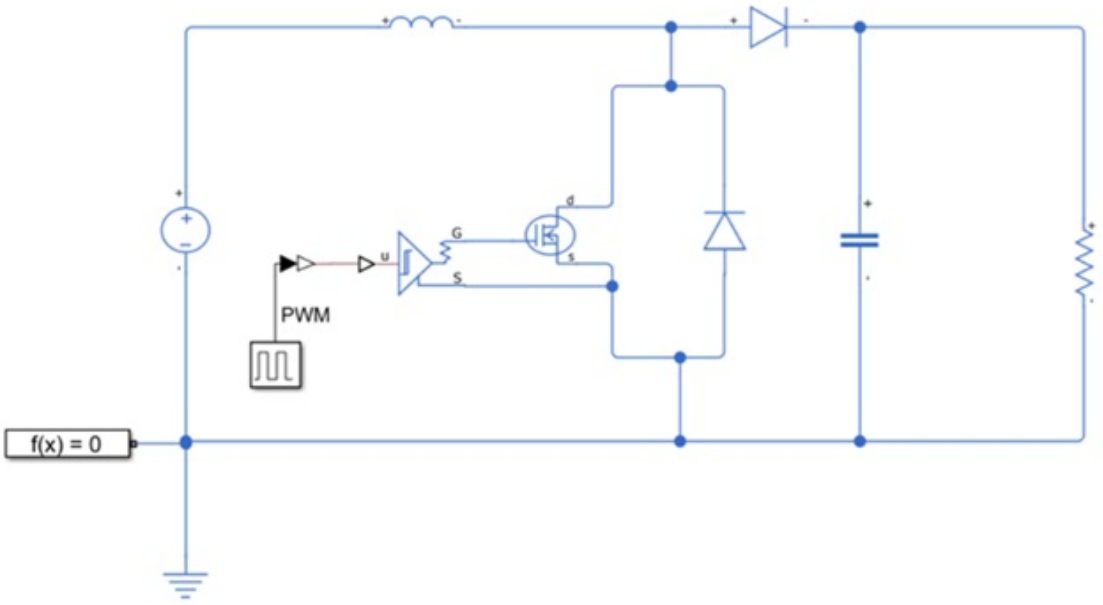


Figure 5.1: Simulink model of the Boost converter with Si MOSFET implementation.

Buck Converter

For the Buck converter, the duty cycle is calculated as:

$$D = \frac{V_{\text{out}}}{V_{\text{in}}}, \tag{5.3}$$

and the app enforces the condition $V_{\text{out}} < V_{\text{in}}$. The initial inductor current is approximated from the expected output current:

$$I_{L,0} \approx \frac{P_{\text{out}}}{V_{\text{out}}}. \tag{5.4}$$

Figure 5.2 shows the Buck converter model for the GaN MOSFET case. The general circuit structure follows the standard Buck topology. In the GaN buck model, the reverse-conduction path is represented through a third-quadrant conduction model rather than a conventional diode, which is an important distinction since GaN HEMTs do not have a body diode in the same sense as Si MOSFETs.

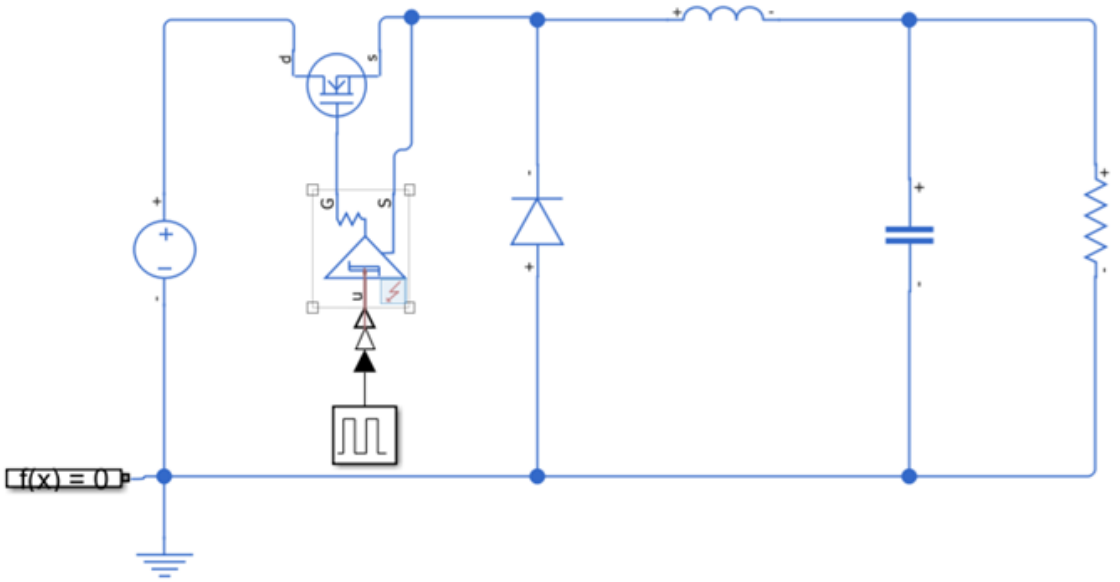


Figure 5.2: Simulink model of the Buck converter with GaN MOSFET implementation.

Flyback Converter

The flyback converter model is the most complex of the three DC/DC implementations because it requires additional transformer parameters: magnetising inductance L_m, leakage inductance L_{lk}, turns ratio $n = N_p/N_s$, and output-capacitor ESR. The primary and secondary turns are exported separately to the base workspace, as required by the Simulink transformer block.

Instead of applying a fixed duty cycle calculated from the ideal conversion ratio, the output voltage is regulated using a proportional-integral (PI) controller. The controller error is defined as

$$e(t) = V_{\text{ref}} - V_{\text{out}}(t), \tag{5.5}$$

and the duty-cycle command is given by

$$D^*(t) = K_p e(t) + K_i \int_0^t e(\tau), \mathrm{d}\tau, \tag{5.6}$$

where K_p and K_i are the proportional and integral gains, respectively. The duty-cycle command is limited to the permitted operating range,

$$D(t) = \text{sat}\left(D^*(t), D_{\min}, D_{\max}\right), \tag{5.7}$$

and is supplied to the PWM generator controlling the primary side MOSFET. This closed-loop approach automatically adjusts the duty cycle until the required output voltage is achieved, accounting for diode losses, transformer parasitics, and changes in the input voltage or load.

Figure 5.3 shows the Flyback converter model. Unlike the Buck and Boost models, it contains separate coupled primary and secondary windings. During the MOSFET on step, the primary current increases as energy is stored in the transformer magnetising inductance. When the MOSFET turns off, this energy is transferred to the secondary winding and the output through the secondary diode. The primary-switch and secondary-diode currents are both logged for use by the loss-calculation routines.

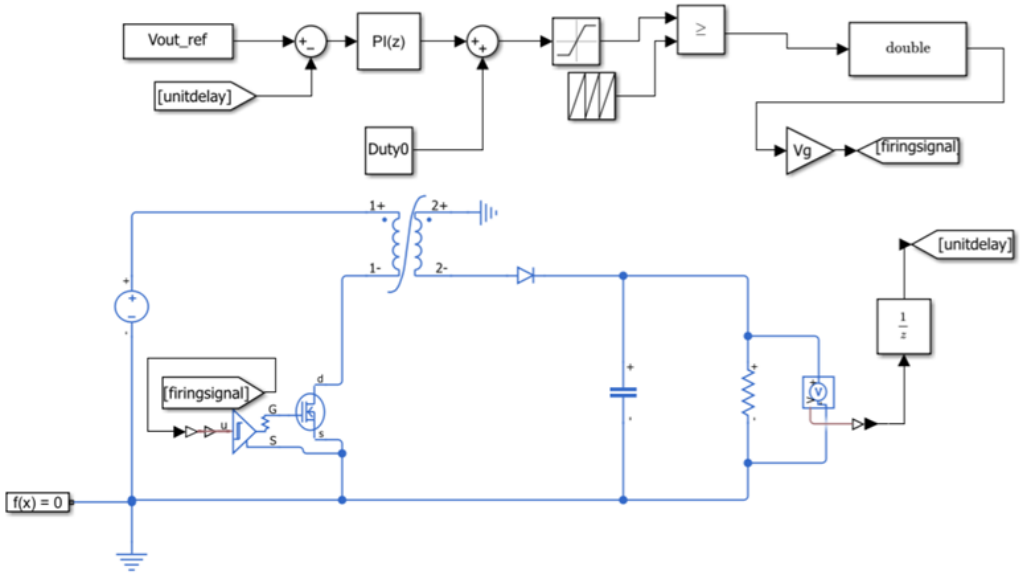


Figure 5.3: Simulink model of the Flyback converter with Si MOSFET implementation and PI-based output-voltage control.

5.3 DC/AC Simulink Models

The currently implemented DC/AC Simulink models are the single-phase half-bridge and full-bridge inverter configurations. The application backend also contains preliminary support for a two-level three-phase inverter, including its parameter definitions and post-processing structure. However, a corresponding validated three-phase Simulink model is not included in the present implementation.

For the half-bridge and full-bridge inverter models, the operating point is defined by the DC-link voltage, output RMS voltage, output power, output frequency, switching frequency, power factor, modulation index, and PWM strategy. These parameters and others

define the voltage and current waveforms that the semiconductor devices will experience during operation.

For the planned three-phase inverter implementation, the backend defines the output voltage as the line-to-line RMS value. This is consistent with the standard way of defining three-phase inverter operating points in industrial applications, and it avoids ambiguity between line-to-line and phase voltages when computing the modulation index.

The inverter models provide device-level voltage and current waveforms for each active switch. After the simulation finishes, the app stores these signals in matrix form, where each column corresponds to one semiconductor device. In the half-bridge case this means two columns, in the full-bridge four columns, and in the three-phase inverter six columns. This matrix representation allows the same post-processing routines to handle all three inverter topologies without modification, since the number of devices is handled implicitly by the size of the matrix.

One important distinction between the inverter models and the DC/DC models is the nature of the current waveforms. In DC/DC converters, the switch current is approximately a piecewise-constant or ramp waveform at the switching frequency. In inverter models, the switch current modulates at the fundamental output frequency as well, which means that the instantaneous loss varies significantly over a full output cycle. The loss averaging is therefore performed over a window that covers at least one complete fundamental period, ensuring that the computed average loss is representative of the steady-state operating condition.

5.4 Implemented Model Mapping

As mentioned before, the MATLAB app does not use a single universal Simulink model. Instead, the selected topology and device technology are mapped to a specific model name. This mapping is necessary because different technologies require different Simulink block parameterisations. For example, an IGBT implementation requires saturation-voltage and IGBT block parameters, while a GaN implementation requires a reverse-conduction representation that is different from the body diode of a silicon MOSFET.

The Simulink models are parameterised through variables exported by the MATLAB app before execution. This design separates the graphical input workflow from the Simulink block diagrams. The block diagrams remain generic, while the app controls the numerical values used for each run. The exported variables can be grouped into electrical, device, diode, timing, and thermal categories.

For DC/DC models, the electrical variables include `Vin`, `Vout_ref`, `Pout`, `fsw`, `Cout`, `Rload`, `Duty`, `Tsw`, and the initial conditions `IL0`, `Vout0`, and `Iout0`. The Boost and Buck converters additionally receive the inductor value `L`. The Flyback converter receives `Lm`, `Llk`, `TurnsRatio`, `Np`, `Ns`, and `CoutESR`.

For inverter models, the exported electrical variables include `Vdc`, `Pout`, `fout`, `fsw`, `PF`, `ModIndex`, `PWMStrategy`, `Irms`, `phi`, `Rload`, and `Lload`. For the three-phase inverter, the app also exports `VLLRMS` and `VphRMS`. The DC-link capacitor is represented by a fixed value `Cdc` in the present implementation.

The device variables include `RdsOn`, `VceSat`, `Eon_sw`, `Eoff_sw`, `Qg_sw`, `Qoss_sw`, `Coss_sw`,

Ciss_sw, Crss_sw, Vth_sw, and measurement-condition variables such as Ids_RdsOn and Vgs_RdsOn. The diode or reverse-path variables include Vf, RonD, QrrD, TrrD, and CjD. The thermal variables include Tamb_C, Th_C, Tboundary_C, Rth_ch, Rth_ha, Cth_h, tau_ha, Rth_foster_sw, and tau_foster_sw.

This explicit workspace interface is useful for verification. If a simulation result is unexpected, the user can inspect the base workspace to confirm which values were actually passed to the Simulink model.

5.5 DC/DC Signal Logging and Loss Interface

The DC/DC models are required to export a common set of signals so that the MATLAB post-processing routine can remain topology independent. The expected signals are listed in Table 5.1. The app searches for alternative names in some cases, which makes the interface more robust during model development.

Table 5.1: Common DC/DC signal interface used by the post-processing routine.

Signal	Purpose in the app
Vout_sim	Output voltage used for output-power calculation
Iout_sim	Output current used for output-power calculation
VDS_sim	Switch blocking-voltage waveform for inspection and debugging
Isw_sim	Switch current used for conduction-loss calculation
VD_sim	Diode voltage waveform for inspection and debugging
ID_sim	Diode current used for diode-loss calculation
IL_sim	Inductor or magnetising-current waveform used for operating-point verification

Once the signals are extracted, the app calculates the instantaneous switch conduction loss and diode loss from the current waveforms. The output power is calculated as $v_{\mathrm{out}}(t)i_{\mathrm{out}}(t)$. The average values are then taken over the final 20% of the simulation time. This is why the Simulink stop time must be long enough to remove the initial capacitor and inductor transient from the averaging window.

5.6 Limitations of the Present Simulink Models

The Simulink models are designed to support the loss-estimation workflow, not to reproduce every physical detail of a hardware prototype. The models are therefore simplified in several ways. First, converter parasitics such as PCB loop inductance, package inductance, transformer winding capacitance, gate driver circuitry are not fully represented. Second, the switching transitions are not calibrated against double-pulse-test waveforms. Third, magnetic saturation and core losses are not included in the present loss summary.

6 Validation and Case Studies of the Loss-Estimation Platform

6.1 Boost-Converter Case Study Scope

This case study applies the developed MATLAB application to a DC/DC boost converter using the Infineon IKQ40N120CT2 silicon IGBT. The study has two aims. First, to check the application loss estimation against a hand calculation based on the same datasheet, and second, compare the application results with the Infineon IPOSIM manufacturer tool.

To ensure a consistent comparison, all three calculation use the same model, operating point, and ambient conditions.

6.2 Converter Operating Conditions

The converter raises the input voltage from 400 V to 800 V and operates at a switching frequency of 1.6 kHz. The output current is limited to 2 A in the selected IPOSIM configuration. Therefore, the common output power is

$$P_{\text{out}} = V_{\text{out}} I_{\text{out}} = 800(2) = 1600 \text{ W}. \tag{6.1}$$

The nominal duty ratio is

$$D = 1 - \frac{V_{\text{in}}}{V_{\text{out}}} = 1 - \frac{400}{800} = 0.5. \tag{6.2}$$

Table 6.1 summarises the conditions used in all three calculations.

6.3 Selected IGBT and Electrical Inputs

The selected device is the Infineon IKQ40N120CT2, a 1200 V, 40 A silicon IGBT with a co-packed fast-recovery diode. The 800 V blocking voltage and the converter current remain below the device ratings.

The IGBT conduction characteristic is represented using

Table 6.1: Boost-converter conditions used in the case study.

Parameter	Symbol	Value
Input voltage	V_{in}	400 V
Output voltage	V_{out}	800 V
Output current	I_{out}	2 A
Output power	P_{out}	1.6 kW
Switching frequency	f_{sw}	1.6 kHz
Duty ratio	D	0.5
Input inductance	L	0.25 H
Gate resistance	$R_{\mathrm{G,on}} = R_{\mathrm{G,off}}$	12 Ω

$$V_{\mathrm{CE(sat)}} = V_{\mathrm{CE0}} + r_{\mathrm{CE}} I_{\mathrm{C}}, \tag{6.3}$$

where the dynamic resistance is obtained from two points on the typical output characteristic:

$$r_{\mathrm{CE}} = \frac{1.75 - 1.37}{40 - 20} = 0.019\ \Omega. \tag{6.4}$$

The corresponding threshold voltage is approximately

$$V_{\mathrm{CE0}} = 0.99\ \mathrm{V}. \tag{6.5}$$

The electrical parameters entered in the application are listed in Table 6.2.

Table 6.2: IGBT inputs used for the IKQ40N120CT2.

Parameter	Value	Reference condition
V_{CE0}	0.99 V	Linearised output curve
r_{CE}	0.019 Ω	Linearised output curve
E_{on}	3.10 mJ	40 A, 600 V, 25 °C
E_{off}	2.90 mJ	40 A, 600 V, 25 °C
Gate resistance	12 Ω	Datasheet test condition
Gate voltage	15 V	Datasheet test condition
Second conduction temperature	175 °C	Datasheet value
$V_{\mathrm{CE(sat)}}$ at 175 °C	2.30 V	40 A and $V_{\mathrm{GE}} = 15$ V

The co-packed diode is represented using the same two parameter conduction model, with $V_{\mathrm{F0}} = 0.84$ V and $r_{\mathrm{F}} = 0.0265$ Ω. The reference recovery values are $Q_{\mathrm{rr}} = 3100$ nC, $t_{\mathrm{rr}} = 298$ ns, and $E_{\mathrm{rec}} = 0.93$ mJ.

6.4 Thermal Model and Cooling

The IGBT junction-to-case response is represented by the five-term Foster network obtained from the datasheet transient thermal-impedance curve.

Table 6.3: Foster network used for the IKQ40N120CT2.

Branch	R_i (K/W)	τ_i (s)
1	0.016055	4.1×10^{-4}
2	0.117494	2.8×10^{-3}
3	0.157560	0.018313
4	0.003300	0.491884
5	0.000340	12.38553

The case-to-heatsink thermal resistance used by the application is

$$R_{\mathrm{th,ch}} = 0.15 \text{ K/W}. \tag{6.6}$$

For this boost-converter case, the thermal comparison uses a simplified package-level representation in the application, whereas IPOSIM reports separate IGBT and diode junction temperatures. In the general mission-profile implementation, a physically separate external diode is not included in the switch-junction heat source unless a shared thermal path is explicitly assumed.

6.5 Datasheet-Based Hand Calculation

At the selected operating point, the average inductor current is

$$I_{\mathrm{L,avg}} = \frac{P_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{1600}{400} = 4 \text{ A}. \tag{6.7}$$

The peak-to-peak current ripple is

$$\Delta I_{\mathrm{L}} = \frac{V_{\mathrm{in}} D}{L f_{\mathrm{sw}}} = \frac{400(0.5)}{0.25(1600)} = 0.5 \text{ A}. \tag{6.8}$$

Therefore, the turn-on and turn-off currents are approximately 3.75 A and 4.25 A. For a triangular current ripple,

$$\overline{I_{\mathrm{L}}^2} = I_{\mathrm{L,avg}}^2 + \frac{\Delta I_{\mathrm{L}}^2}{12} = 16.0208 \text{ A}^2. \tag{6.9}$$

The IGBT conduction loss is

$$P_{\mathrm{cond}} = D\left(V_{\mathrm{CE0}} I_{\mathrm{L,avg}} + r_{\mathrm{CE}} \overline{I_{\mathrm{L}}^2}\right) \quad = 0.5\left[0.99(4) + 0.019(16.0208)\right] \; = 2.13 \text{ W}. \tag{6.10}$$

The switching energies are scaled linearly with current and blocking voltage:

$$E_{\mathrm{on}} = 3.10 \text{ mJ} \left(\frac{3.75}{40}\right) \left(\frac{800}{600}\right) = 0.388 \text{ mJ}, \tag{6.11}$$

$$E_{\text{off}} = 2.90 \text{ mJ} \left(\frac{4.25}{40}\right) \left(\frac{800}{600}\right) = 0.411 \text{ mJ}. \tag{6.12}$$

The resulting IGBT switching loss is

$$P_{\text{sw}} = f_{\text{sw}} \left(E_{\text{on}} + E_{\text{off}}\right) = 1.28 \text{ W}. \tag{6.13}$$

The diode forward-conduction loss is

$$P_{\text{D,fwd}} = (1 - D) \left(V_{\text{F0}} I_{\text{L,avg}} + r_{\text{F}} \overline{I_{\text{L}}^2}\right) \quad = 0.5 \left[0.84(4) + 0.0265(16.0208)\right] \; = 1.89 \text{ W}. \tag{6.14}$$

Using the same recovery-energy scaling as the application gives

$$P_{\text{rr}} = f_{\text{sw}} E_{\text{rec}} \left(\frac{4}{40}\right) \left(\frac{800}{600}\right) = 0.20 \text{ W}. \tag{6.15}$$

The total semiconductor loss is therefore

$$P_{\text{loss}} = 2.13 + 1.28 + 1.89 + 0.20 = 5.50 \text{ W}. \tag{6.16}$$

The corresponding semiconductor-only efficiency is

$$\eta_{\text{hand}} = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} \times 100 = \frac{1600}{1600 + 5.50} \times 100 = 99.66\%. \tag{6.17}$$

This efficiency excludes inductor's parallel resistance, capacitor's series resistance, gate-driver power consumption, wiring, cooling-system, and auxiliary losses.

6.6 Application and IPOSIM Results

Figure 6.1 shows the result obtained from the developed MATLAB application.

The application predicts an IGBT conduction loss of 1.97 W, an IGBT switching loss of 1.28 W, and a combined diode loss of 2.29 W. The resulting total semiconductor loss is 5.54 W, corresponding to a semiconductor-only efficiency of 99.65%.

Figure 6.2 shows the result obtained using IPOSIM under the same electrical operating conditions.

IPOSIM predicts 3.43 W of total IGBT loss and 2.46 W of total diode loss. The resulting total semiconductor loss is

$$P_{\text{loss,IPOSIM}} = 3.43 + 2.46 = 5.89 \text{ W}. \tag{6.18}$$

The corresponding semiconductor-only efficiency is

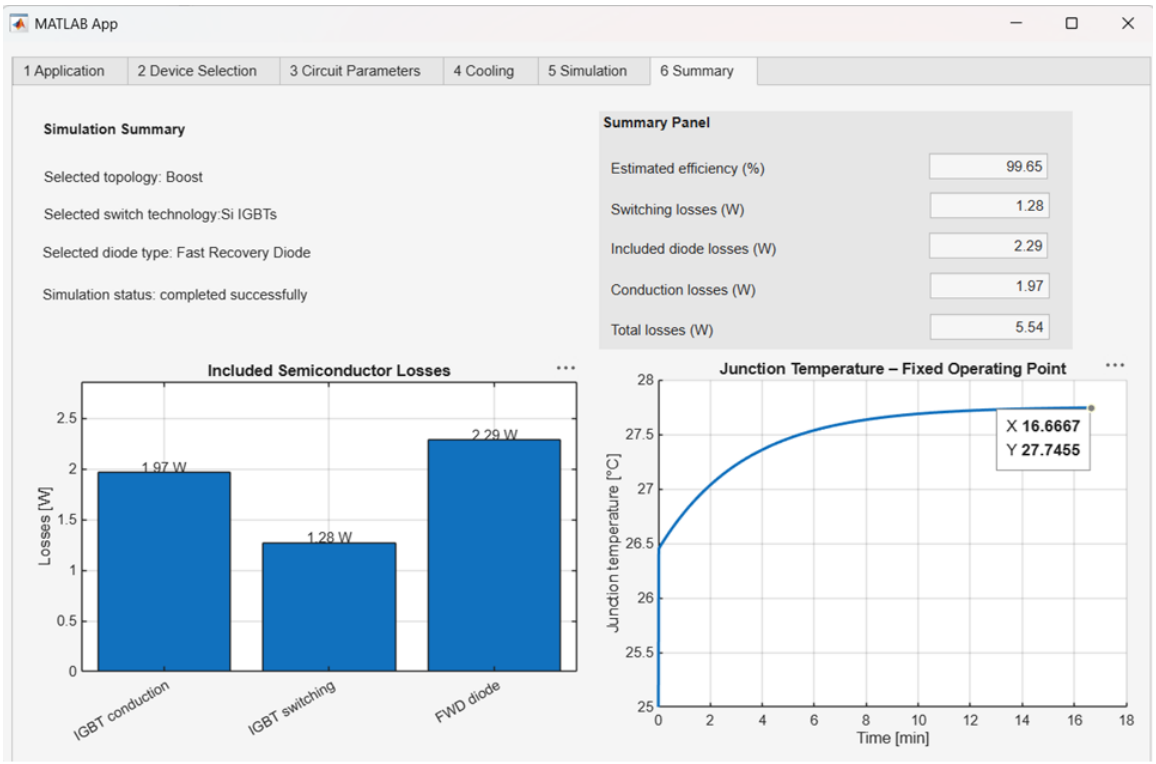


Figure 6.1: MATLAB application results for the IKQ40N120CT2 boost converter at 1.6 kW.

$$\eta_{\text{IPOSIM}} = \frac{1600}{1600 + 5.89} \times 100 = 99.63\%. \tag{6.19}$$

6.6.1 Single-Phase Half-Bridge Validation

The same datasheet-based approach was applied to the single-phase half-bridge inverter using the Semikron Danfoss SKM50GB12T4 IGBT module. The operating conditions are summarized in Table 6.4.

Table 6.4: Operating conditions used for the half-bridge validation.

Parameter	Symbol	Value
DC-link voltage	V_{dc}	400V
Output active power	P_{out}	1000W
Output RMS voltage	$V_{\text{out,rms}}$	115V
Output frequency	f_{out}	50Hz
Switching frequency	f_{sw}	2kHz
Power factor	$\cos\phi$	0.95
Modulation index	m	0.813
Gate resistance	$R_{\text{G,on/off}}$	8.2
Gate-drive voltage	V_{GE}	$\pm 15V$

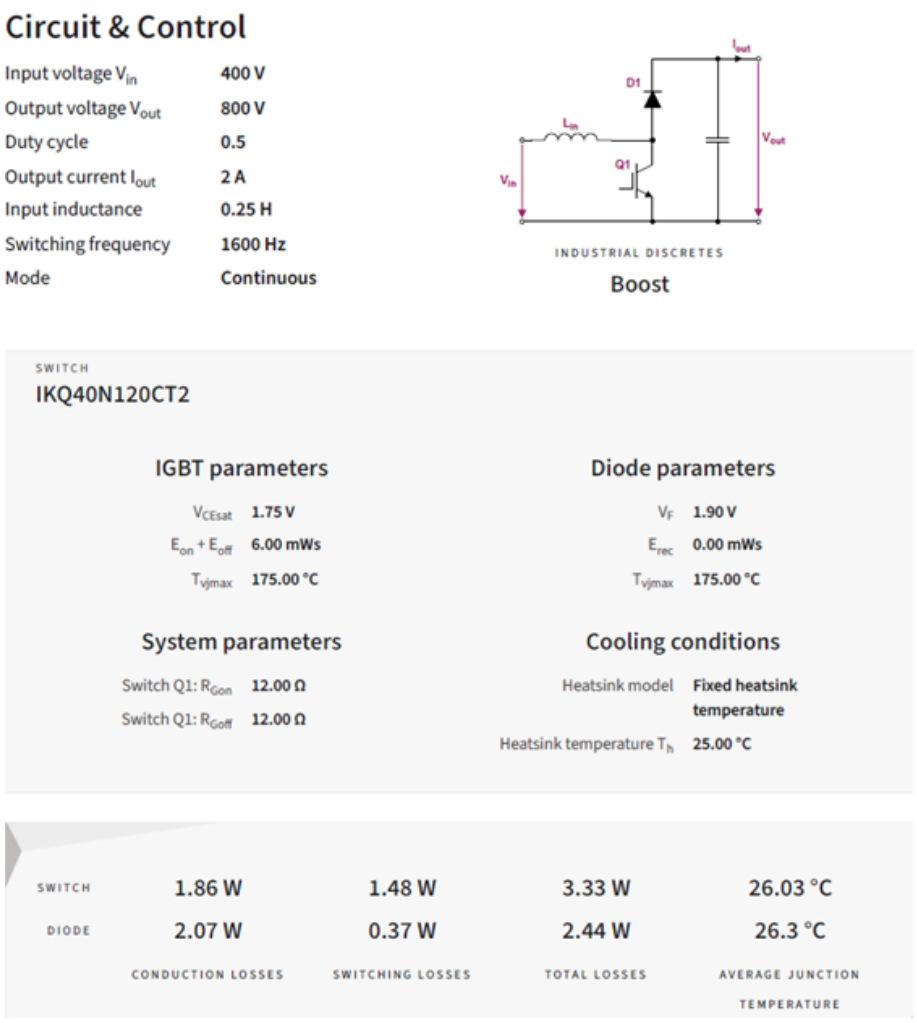


Figure 6.2: IPOSIM results for the IKQ40N120CT2 boost converter at 1.6 kW.

The modulation index and load-current quantities are

$$m = \frac{2\sqrt{2}V_{\text{out,rms}}}{V_{\text{dc}}} = 0.813, \tag{6.20}$$

$$I_{\text{rms}} = \frac{P_{\text{out}}}{V_{\text{out,rms}} \cos\phi} = 9.153 \text{ A}, \qquad I_{\text{pk}} = \sqrt{2} I_{\text{rms}} = 12.945 \text{ A}, \tag{6.21}$$

with

$$\phi = \cos^{-1}(0.95) = 18.19^\circ. \tag{6.22}$$

Using $V_{\text{CE0}} = 0.70$ V and $r_{\text{CE}} = 30$ mΩ, the conduction loss per IGBT is

$$\begin{aligned} P_{\text{cond,T}} = &\left(\frac{1}{2\pi} + \frac{m\cos\phi}{8}\right) V_{\text{CE0}} I_{\text{pk}} \\ &+ \left(\frac{1}{8} + \frac{m\cos\phi}{3\pi}\right) r_{\text{CE}} I_{\text{pk}}^2 = 3.358 \text{ W}. \end{aligned} \tag{6.23}$$

Therefore,

$$P_{\text{cond,T,total}} = 2P_{\text{cond,T}} = 6.715 \text{ W}. \tag{6.24}$$

Using the datasheet switching energies $E_{\text{on,ref}} = 5.5$ mJ and $E_{\text{off,ref}} = 4.5$ mJ at $I_{\text{ref}} = 50$ A and $V_{\text{ref}} = 600$ V,

$$P_{\text{sw,T}} = f_{\text{sw}} \left(E_{\text{on,ref}} + E_{\text{off,ref}}\right) \frac{I_{\text{pk}}}{\pi I_{\text{ref}}} \frac{V_{\text{dc}}}{V_{\text{ref}}} = 1.099 \text{ W}, \tag{6.25}$$

and for both IGBTs,

$$P_{\text{sw,T,total}} = 2P_{\text{sw,T}} = 2.198 \text{ W}. \tag{6.26}$$

For the antiparallel diodes, using $V_{\text{F0}} = 0.90$ V and $r_{\text{F}} = 25.6$ mΩ,

$$\begin{aligned} P_{\text{cond,D}} = &\left(\frac{1}{2\pi} - \frac{m\cos\phi}{8}\right) V_{\text{F0}} I_{\text{pk}} \\ &+ \left(\frac{1}{8} - \frac{m\cos\phi}{3\pi}\right) r_{\text{F}} I_{\text{pk}}^2. \end{aligned} \tag{6.27}$$

The total diode conduction loss is

$$P_{\text{cond,D,total}} = 1.828 \text{ W}. \tag{6.28}$$

Using $E_{\text{rr,ref}} = 3.8$ mJ,

$$P_{\mathrm{rr,D}} = f_{\mathrm{sw}} E_{\mathrm{rr,ref}} \frac{I_{\mathrm{pk}}}{\pi I_{\mathrm{ref}}} \frac{V_{\mathrm{dc}}}{V_{\mathrm{ref}}}, \tag{6.29}$$

giving

$$P_{\mathrm{rr,total}} = 0.835 \text{ W}. \tag{6.30}$$

The total semiconductor loss is therefore

$$P_{\mathrm{loss}} = 6.715 + 2.198 + 1.828 + 0.835 = 11.575 \text{ W}. \tag{6.31}$$

The corresponding semiconductor-only efficiency is

$$\eta_{\mathrm{hand}} = \frac{1000}{1000 + 11.575} \times 100 = 98.856\%. \tag{6.32}$$

Figure 6.3 shows the loss estimation obtained from the developed MATLAB/Simscape platform at the same operating point.

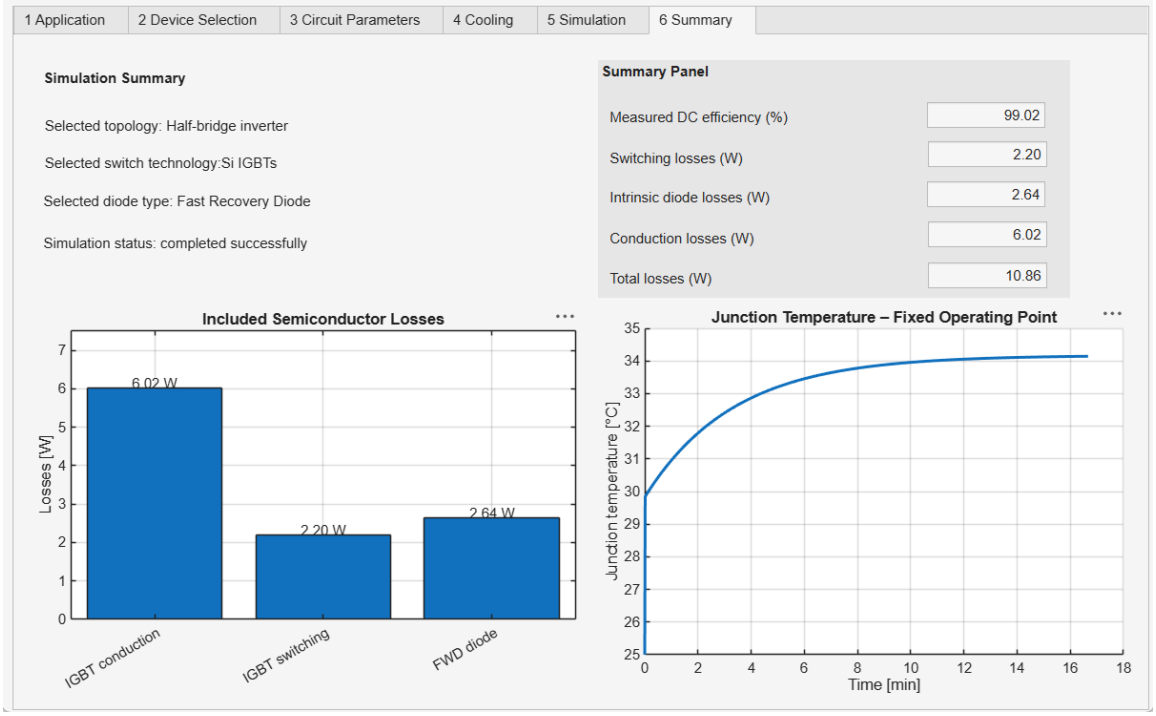


Figure 6.3: Loss estimation obtained from the developed platform for the single-phase half-bridge validation case.

The analytical and simulated results for the boost converter case are compared in Table 6.5. The measured DC efficiency displayed by the application is obtained directly from the simulated input and output powers and is therefore not used for the semiconductor-loss comparison. For comparison with the analytical result, the semiconductor-only efficiency of the application is calculated from the simulated semiconductor losses as

$$\eta_{\text{semi,app}} = \frac{1000}{1000 + 10.86} \times 100 = 98.926\%. \tag{6.33}$$

Table 6.5: Comparison between the analytical calculation and the developed platform for the single-phase half-bridge validation case.

Quantity	Analytical	Application	Difference
IGBT conduction loss	6.715 W	6.02 W	-10.35%
IGBT switching loss	2.198 W	2.20 W	+0.09%
Total diode loss	2.663 W	2.64 W	-0.86%
Total semiconductor loss	11.575 W	10.86 W	-6.18%
Semiconductor efficiency	98.856%	98.926%	+0.07 pp

The total semiconductor loss differs by approximately 6.2%, while the switching and diode-loss predictions are very close to the analytical values. The largest difference is observed in the IGBT conduction loss. Overall, the half-bridge case provides a satisfactory consistency check of the implemented loss calculation at the selected operating point.

6.6.2 Single-Phase Full-Bridge Validation

A second inverter validation was performed using a single-phase full-bridge configuration with the Infineon F4-75R12KS4 four-pack IGBT module. In contrast to the half-bridge case, the switching and diode reverse-recovery losses in this model are obtained directly from the simulated semiconductor voltage and current waveforms.

The operating conditions were selected to reproduce the same case in the Infineon IPOSIM tool. They are summarized in Table 6.6.

Table 6.6: Operating conditions used for the full-bridge validation.

Parameter	Symbol	Value
DC-link voltage	V_{dc}	400V
Output active power	P_{out}	1000W
Output RMS voltage	$V_{\text{out,rms}}$	230V
Output RMS current	$I_{\text{out,rms}}$	4.58A
Output frequency	f_{out}	50Hz
Switching frequency	f_{sw}	2kHz
Power factor	$\cos\phi$	0.95
Modulation index	m	0.8132
PWM strategy	–	SPWM
Gate resistance	$R_{\text{G,on/off}}$	7.5
Semiconductor module	–	F4-75R12KS4

The corresponding RMS and peak output currents are approximately

$$I_{\text{rms}} = \frac{P_{\text{out}}}{V_{\text{out,rms}} \cos\phi} = \frac{1000}{230(0.95)} = 4.577 \text{ A}, \tag{6.34}$$

and

$$I_{\mathrm{pk}} = \sqrt{2} I_{\mathrm{rms}} = 6.472 \text{ A}. \tag{6.35}$$

For the full-bridge implementation, the IGBT conduction losses are evaluated from the simulated device currents together with the linearized on-state characteristic. The switching losses are obtained by integrating the instantaneous device power around each switching transition,

$$E_{\mathrm{sw}} = \int_{t_1}^{t_2} v_{\mathrm{CE}}(t) i_{\mathrm{C}}(t)\, dt. \tag{6.36}$$

The antiparallel-diode forward-conduction losses are likewise obtained from

$$P_{\mathrm{D,fwd}} = \frac{1}{T} \int_{T} v_{\mathrm{D}}(t) i_{\mathrm{D}}(t)\, dt, \tag{6.37}$$

while reverse-recovery losses are calculated from the simulated negative-current recovery transient. For each detected recovery event,

$$Q_{\mathrm{rr}} = \int_{t_1}^{t_2} |i_{\mathrm{D}}(t)|\, dt, \tag{6.38}$$

and

$$E_{\mathrm{rr}} = \int_{t_1}^{t_2} v_{\mathrm{D}}(t) i_{\mathrm{D}}(t)\, dt. \tag{6.39}$$

Figure 6.4 shows the loss estimation obtained from the developed MATLAB/Simscape platform.

The application predicts an overall IGBT conduction loss of

$$P_{\mathrm{cond,IGBT}} = 11.18 \text{ W}, \tag{6.40}$$

and a waveform-integrated IGBT switching loss of

$$P_{\mathrm{sw,IGBT}} = 1.59 \text{ W}. \tag{6.41}$$

The measured forward-diode contribution is

$$P_{\mathrm{D,fwd}} = 1.745 \text{ W}, \tag{6.42}$$

while the simulated reverse-recovery contribution is

$$P_{\mathrm{rr}} = 0.148 \text{ W}. \tag{6.43}$$

Therefore, the total diode loss is

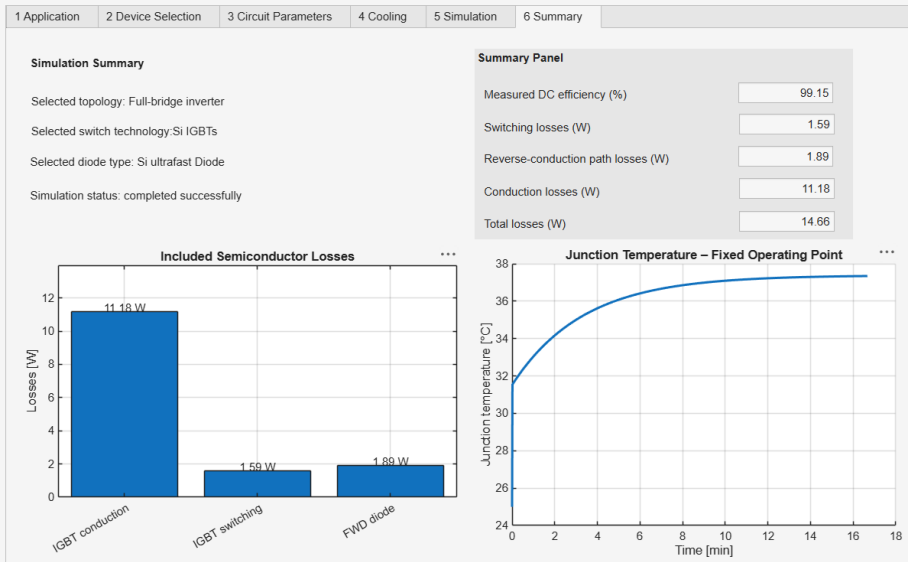


Figure 6.4: Loss estimation obtained from the developed platform for the F4-75R12KS4 single-phase full-bridge validation case

$$P_{\mathrm{D,total}} = P_{\mathrm{D,fwd}} + P_{\mathrm{rr}} = 1.893 \text{ W}. \tag{6.44}$$

The total semiconductor loss predicted by the developed platform is consequently

$$P_{\mathrm{loss,app}} = 11.18 + 1.59 + 1.89 = 14.66 \text{ W}. \tag{6.45}$$

The corresponding semiconductor-only efficiency is

$$\eta_{\mathrm{semi,app}} = \frac{1000}{1000 + 14.66} \times 100 = 98.56\%. \tag{6.46}$$

The measured DC efficiency reported by the application is 99.15%. This value is obtained independently from the simulated input and output powers and is therefore not used for the semiconductor-loss comparison.

The same operating conditions were reproduced in Infineon IPOSIM. IPOSIM reports losses for one IGBT and its associated antiparallel diode. The reported per-device values are 2.06 W of IGBT conduction loss, 0.68 W of IGBT switching loss, 0.33 W of diode forward-conduction loss, and 0.21 W of diode switching or reverse-recovery loss.

Since the full bridge contains four identical switch positions, the complete bridge values predicted by IPOSIM are

$$P_{\mathrm{cond,IGBT,IPOSIM}} = 4(2.06) = 8.24 \text{ W}, \tag{6.47}$$

$$P_{\mathrm{sw,IGBT,IPOSIM}} = 4(0.68) = 2.72 \text{ W}, \tag{6.48}$$

and

$$P_{\mathrm{D,fwd,IPOSIM}} = 4(0.33) = 1.32 \text{ W}, \tag{6.49}$$

$$P_{\mathrm{rr,IPOSIM}} = 4(0.21) = 0.84 \text{ W}. \tag{6.50}$$

The resulting total diode loss is therefore

$$P_{\mathrm{D,total,IPOSIM}} = 4(0.54) = 2.16 \text{ W}, \tag{6.51}$$

and the complete semiconductor loss is

$$P_{\mathrm{loss,IPOSIM}} = 4(2.74 + 0.54) = 13.12 \text{ W}. \tag{6.52}$$

The corresponding IPOSIM semiconductor-only efficiency is

$$\eta_{\mathrm{semi,IPOSIM}} = \frac{1000}{1000 + 13.12} \times 100 = 98.70\%. \tag{6.53}$$

Table 6.7 compares the application and IPOSIM results. The percentage differences use the IPOSIM result as the reference.

Table 6.7: Comparison of the developed platform and IPOSIM for the single-phase full-bridge validation case.

Quantity	Application	IPOSIM	Difference
IGBT conduction loss	11.18 W	8.24 W	+35.7%
IGBT switching loss	1.59 W	2.72 W	-41.5%
Total IGBT loss	12.77 W	10.96 W	+16.5%
Diode forward loss	1.745 W	1.32 W	+32.2%
Reverse-recovery loss	0.148 W	0.84 W	-82.4%
Total diode loss	1.89 W	2.16 W	-12.5%
Total semiconductor loss	14.66 W	13.12 W	+11.7%
Semiconductor efficiency	98.56%	98.70%	-0.15 pp

At the complete-converter level, the agreement is satisfactory. The difference between the total semiconductor losses predicted by the two methods is

$$\varepsilon_{\mathrm{app-IPOSIM}} = \frac{|14.66 - 13.12|}{13.12} \times 100 = 11.7\%. \tag{6.54}$$

The semiconductor-only efficiencies differ by approximately 0.15 percentage points. Therefore, the developed model reproduces the overall semiconductor loss magnitude reasonably well at the investigated operating point.

Larger differences are observed when the individual loss mechanisms are considered. The application predicts higher IGBT and diode forward-conduction losses, while the simulated switching and reverse-recovery losses are lower than the IPOSIM values. The largest deviation occurs in the reverse-recovery component. The full-bridge case can therefore be considered satisfactory at the overall converter-loss level, while further refinement of

the dynamic semiconductor models is still required before claiming agreement at the individual loss-component level. These differences may be related to the semiconductor characteristic representation, temperature-dependent parameters, switching-transition dynamics, diode charge-storage behaviour, and the numerical resolution used to reproduce sub-microsecond switching transients.

6.7 Comparison and Discussion

Table 6.8 compares the three calculation methods. The reported differences use the hand calculation as the reference.

Table 6.8: Comparison of the hand calculation, application, and IPOSIM.

Quantity	Hand	Application	Difference	IPOSIM	Difference
IGBT conduction loss	2.13 W	1.97 W	7.5%	1.81 W	15.0%
IGBT switching loss	1.28 W	1.28 W	0.0%	1.62 W	26.6%
Total diode loss	2.09 W	2.29 W	9.6%	2.46 W	17.7%
Total semiconductor loss	5.50 W	5.54 W	0.7%	5.89 W	7.1%
Semiconductor efficiency	99.66%	99.65%	0.01 pp	99.63%	0.03 pp

The application agrees with the hand calculation. The total semiconductor losses differ by only 0.7 percent, while the calculated efficiencies differ by 0.01 percentage points. The exact agreement in IGBT switching loss is expected because both methods use the same linear switching-energy scaling equation.

The application and IPOSIM total losses differ by

$$\varepsilon_{\text{app}-\text{IPOSIM}} = \frac{|5.54 - 5.89|}{5.89} \times 100 = 5.9\%. \tag{6.55}$$

Although the total losses are close, the distribution between conduction, switching, and diode losses is different. These differences may result from IPOSIM's internal interpolation of the device characteristics, temperature dependent parameters, and more complex and complete switching models. The proposed application in MATLAB instead uses linearised conduction curves and direct scaling of the reference switching energies.

The thermal results are close as well. The application reports a combined junction temperature of approximately 27.75 °C, meanwhile IPOSIM reports separate IGBT and diode junction temperatures of 26.03 °C and 26.30 °C, respectively. Both simulations use a heatsink temperature of 25 °C. The difference can be due to the different thermal network implementations.

6.8 Case-Study Conclusions

The boost converter case provided the first validation of the developed loss estimation tool. At the selected operating point, the hand calculation, MATLAB application, and IPOSIM predicted total semiconductor losses of 5.50 W, 5.54 W, and 5.89 W, respectively.

The application differs from the hand calculation by only 0.7% and from IPOSIM by 5.9%. The thermal results are also reasonably close when the same heatsink temperature is used, although the application and IPOSIM use different thermal representations.

The inverter cases provide an additional check of the waveform-based loss calculation. In the single-phase half-bridge case, the developed platform predicts 10.86 W of total semiconductor loss compared with 11.575 W from the analytical calculation, corresponding to a difference of approximately 6.2%. For the single-phase full-bridge case, the application predicts 14.66 W, compared with 13.12 W from IPOSIM, giving an overall difference of 11.7%.

The three cases therefore show reasonable agreement at the total semiconductor-loss level. However, the full-bridge comparison also shows that good agreement in total loss does not necessarily imply agreement in every individual loss mechanism. In particular, the switching and reverse-recovery components remain sensitive to the semiconductor model and numerical resolution. The validation results should therefore be interpreted as evidence of consistency at converter level rather than as a claim of universal component-level accuracy.

7 Conclusions and Future Work

7.1 Conclusions

This thesis developed a MATLAB App Designer and Simulink platform for the datasheet based estimation of semiconductor losses and junction temperature in selected DC/DC and DC/AC converter topologies. Its workflow links topologies and semiconductor selection, parameter input, validation, model selection, waveform extraction, loss calculation, and thermal post-processing in one configurable application.

The platform supports boost, buck, and flyback converters and half-bridge, and full-bridge. Preliminary interface and backend support has also been developed for a two-level three-phase inverter, although a corresponding Simulink model remains to be implemented and validated. Their device framework covers Si MOSFETs, Si IGBTs, GaN HEMTs, and SiC MOSFETs. This common structure makes the app to handle devices from different manufacturers. Moreover, allows technologies to be studied under consistent operating conditions, provided that datasheet parameters are available.

For single operating points, the application reports the main semiconductor-loss components, total loss, semiconductor-only efficiency, current stress, and junction-temperature evolution. For mission profiles, short simulations until the model reach steady state are combined with a code-based Foster propagation. This makes the computation be lower while preserving the properties of each segments.

The IKQ40N120CT2 boost converter case study gave an initial check with the given operating conditions (400/800 V, 1.6 kW, 1.6 kHz). The hand calculation, the tool developed, and IPOSIM predicted total semiconductor losses in the same range, 5.50 W, 5.54 W, and 5.89 W, respectively. The application differs from the hand calculation by 0.7% and from IPOSIM by 5.9%. With a common heatsink temperature of 25 °C, the application predicted approximately 27.75 °C, while IPOSIM reported 26.03 °C for the IGBT and 26.30 °C for the diode.

The inverter validation cases gave similar converter-level agreement. The single-phase half-bridge application result of 10.86 W differs from the analytical result of 11.575 W by approximately 6.2%. In the single-phase full-bridge case, the application predicted 14.66 W compared with 13.12 W from IPOSIM, corresponding to a difference of 11.7%. The full-bridge case also showed larger differences in the individual switching and reverse-recovery components, which highlights the dependence of these losses on the fidelity of the dynamic semiconductor model.

Taken together, these results support the consistency of the developed loss-estimation workflow at the investigated operating points, while also showing that the platform should

be treated as an engineering estimation tool rather than as a substitute for detailed device characterisation or hardware measurements.

7.2 Limitations

The present implementation cannot achieve a reproduction of a detailed semiconductor physics, PCB and package parasitics, ringing, electromagnetic interference, full gate-driver influence, magnetic losses, or passive-component losses. For conduction losses, its dependence on temperature is based on interpolation or extrapolation between two input points rather than a full curve fitting.

Mission profile execution is currently limited to the DC/DC topologies. Si IGBT inverter models, Cauer thermal-network input, and AC mission profiles are not supported. Several inverter selections share generic models, and the thermal calculation does not yet include a full dynamic heatsink-to-ambient network or the thermal influence of a physically separate external diode. The application interface and backend contain preliminary support for a two-level three-phase inverter, including the required parameter handling, device count, signal-processing structure, and loss-calculation logic. However, a corresponding validated Simulink model has not been implemented in the present version. Therefore, three-phase inverter simulation is not currently functional and is not considered a validated topology of the platform

Cauer thermal-network input is not implemented, and the thermal model uses a simplified thermal boundary rather than a complete dynamic heatsink-to-ambient network. Heating from a physically separate external diode is also not included in the switch-junction thermal model.

Finally, the accuracy of waveform-based switching and reverse-recovery loss estimation depends on the fidelity of the Simulink semiconductor model and on the numerical resolution of the switching transient. This limitation is particularly relevant to the full-bridge validation, where the total semiconductor loss showed reasonable agreement with IPOSIM while larger differences remained in some individual loss components.

7.3 Future Work

Future work should first improve and validate the switching loss calculation through interpolation of datasheet energy curves and comparison with DPT or experiments. Temperature dependence should then be extended to switching and diode losses, and the thermal framework should support both Foster and Cauer networks, separate or shared switch and diode thermal paths, and a dynamic heatsink-to-ambient model.

The application can be extended with dedicated models for the currently unsupported device-topology combinations and with mission profile execution for the inverter topologies. Testing additional devices and operating conditions, followed by comparison with hardware measurements, would clarify the accuracy and practical limits of the application.

8 Appendix

8.1 Comparison of Available Tools

Table 8.1: Comparison of available semiconductor loss-estimation tools.

Software	**Provider**	**Platform**	**Device scope**	**Topology scope**	**Electro-thermal / mission profile**	**Export / integr.**	**Notes / typical use**
IPOSIM	Infineon	Web (PLECS)	Infineon devices only	Broad (DC/DC, AC/DC, DC/AC; many templates)	Steady-state point + load-cycle; thermal calculation; optional lifetime estimation	Report + CSV/PDF; online comparison	Fast early-stage screening and side-by-side comparison (up to 5 devices). Vendor-limited library.
ST-POWER Studio	STMicroelectronics	Web (eDesignSuite)	ST POWER devices only	Focused (power stages; commonly inverter-oriented templates)	Electro-thermal with self-heating; supports application mission profiles	CSV export; online workflow	Good for ST device selection + junction/case temperature estimation; vendor-limited.
Elite Power Simulator	onsemi	Web (PLECS models)	onsemi devices only	Broad (includes hard/soft-switching use cases depending on model availability)	Loss tables + thermal networks (Foster/Cauer); 3D loss/thermal data visualization	Tool-driven analysis; PLECS workflow integration	Strong transparency on loss/thermal datasets (3D plots); vendor-limited library.
MELCOSIM	Mitsubishi Electric	Desktop (Windows)	Mitsubishi modules only	Inverters: 2-level and 3-level (incl. NPC)	Loss + junction-temperature rise; sensitivity curves (e.g., vs. current or f_s)	Graph display + data saving	Targeted to inverter module evaluation; not a general multi-topology environment.
Fuji IGBT Simulator	Fuji Electric	Web (online)	Fuji modules only	Inverters: 2-level and 3-level (multiple PWM methods)	Heatsink/temperature conditions configurable; computes loss + temperature; multi-condition comparison	Waveforms + numerical results (web UI)	Convenient inverter-focused sizing/selection with waveform outputs; vendor-limited.

SemiSel	Semikron Danfoss	Web	Semikron Danfoss products only	Application-oriented templates (converter/inverter selection workflow)	From nominal points/overloads up to full load-cycles/mission profiles; includes cooling requirements	Report-style PDF/CSV export	Strong for module selection under realistic cooling + load profiles; vendor-limited library.
GaN Power Bench	EPC	Web calculators	EPC GaN only	Dedicated: GaN hard-switched Buck/Boost	Loss breakdown + thermal calculator for PCB-mounted GaN (board/heat-spreader/heatsink assumptions)	Calculator outputs (web)	Best for fast GaN device selection in Buck/Boost; not general-purpose.
Toshiba Online Circuit Simulator	Toshiba	Web (login)	Toshiba MOSFETs only	Multiple predefined SMPS templates (incl. AC/DC PFC + DC/DC families)	Primarily electrical simulation for waveform/ efficiency comparison (thermal modeling depends on template)	Waveform/efficiency comparison in UI	Useful for quick MOSFET comparisons without local sim environment; vendor-limited.
TI MOSFET Power Loss Calculator	Texas Instruments	Web tool / spreadsheet	TI MOSFETs / power blocks	Dedicated: synchronous Buck stage	Loss estimation for chosen operating point; loss-vs-load plots; no full electro-thermal network	Spreadsheet-style; plots + ranked device pairs	Very fast MOSFET pair screening/ranking for buck converters; topology-limited by design.
PyPowerSim	Open-source (community)	Python (no GUI)	User-defined (model/config driven)	Standard architectures (HB/FB, 3ϕ B6, DAB, etc.)	Sweep, steady-state, and transient modes; reports losses and temperatures (model-dependent)	Scriptable pipelines; easy automation	Best for reproducible studies + automation; requires coding and validated device models.

8.2 User Manual

8.2.1 Implemented Functions

The following operating modes are currently implemented:

- **Boost, Buck and Flyback converters:** Si, SiC and GaN MOSFET selections and Si IGBT models are available. Mission-profile operation is supported.
- **Single-phase half-bridge:** MOSFET, Si IGBTs, and SiC MOSFETs operation are available. Mission-profile operation is not available.
- **Single-phase full-bridge:** MOSFET and IGBT model are available. Mission-profile operation are not available.
- **Three-phase two-level inverter:** Code is created to support the converter topology, further refinement and validation of it is needed before fully functional.

Normal operation follows the Application, Device Selection, Circuit Parameters, Cooling, Simulation and Summary tabs.

8.3 Basic Operating Procedure

1. **Select the converter.** In Application, choose the topology. The app loads its schematic image, displays the corresponding parameter input boxes in the next tab and fill them with default values.
2. **Select the power switch.** In Device Selection, choose a Si MOSFET, SiC MOSFET, GaN MOSFET or Si IGBT. The input fields change according to the selected technology.
3. **Select the diode or reverse conduction path.** Choose the external diode, body-diode representation or GaN reverse path that corresponds to the selected model.
4. **Enter the device data.** Use values from a datasheet. Enable the advanced fields only when the required data are known.
5. **Define the circuit.** Enter the requested voltages, power, switching frequency, gate voltage and gate resistances, and others parameters relevant.
6. **Define the thermal boundary.** Select either a fixed boundary temperature or a custom Foster thermal network.
7. **Select the operating mode.** Leave Use Mission Profile disabled for a single operating point. Enable it only for a supported Boost, Buck or Flyback mission profile.
8. **Run and review the simulation.** Select Run Simulation. The app validates the configuration, runs the mapped Simulink model in accelerator mode, processes the logged signals and opens Summary if the run is valid.

8.4 Circuit Inputs and Automatic Calculations

8.4.1 Boost and Buck converters

Boost and Buck converters use input voltage V_{in}, output voltage V_{out}, output power P_{out}, switching frequency f_{sw}, inductance L and output capacitance C_{out}.

For a Boost converter, $V_{\mathrm{out}} > V_{\mathrm{in}}$. For a Buck converter, $V_{\mathrm{out}} < V_{\mathrm{in}}$. These relations must remain valid in every mission-profile segment.

8.4.2 Flyback converter

The Flyback converter also requires magnetising inductance L_{m}, turns ratio $N_{\mathrm{p}}/N_{\mathrm{s}}$, leakage inductance and capacitor equivalent series resistance. The magnetising inductance and turns ratio must be positive. Leakage inductance and equivalent series resistance may be zero, but they cannot be negative.

8.4.3 Inverters

The inverter panels require DC-link voltage, output power, output frequency, switching frequency, power factor, modulation index, output RMS voltage and PWM strategy. The three-phase inverter uses line-to-line RMS output voltage. The app calculates the load and LC filter and simulates six fundamental cycles.

Before a normal DC/DC run, the app recalculates the inductance and output capacitance and writes the calculated values back to the interface. For Flyback operation, it also calculates the turns ratio using a target duty ratio of 0.45. Manually entered values in these fields are therefore not always the values used by the model.

8.5 Semiconductor and Diode Data

8.5.1 MOSFET data

All MOSFET selections require the on-state resistance $R_{\mathrm{DS(on)}}$, which is used to calculate conduction loss.

For mission-profile operation, enter $R_{\mathrm{DS(on)}}$ at two different junction temperatures. The second temperature must be higher than the reference temperature, and both resistance values must be positive. During the electrothermal iteration, the resistance is calculated as

$$R_{\mathrm{DS(on)}}(T_{\mathrm{j}}) = R_1 + (R_2 - R_1)\frac{T_{\mathrm{j}} - T_1}{T_2 - T_1}. \tag{8.1}$$

The resulting conduction loss is therefore updated with junction temperature rather than being constant. Values outside the two specified temperatures are extrapolated.

Si MOSFETs use total gate charge Q_g and output charge Q_{oss}. GaN devices use the same charge-based inputs. The GaN gate voltage should remain close to the datasheet test value, commonly between 5 V and 6 V; the app rejects values above 7 V.

SiC MOSFETs use turn-on and turn-off energies E_{on} and E_{off}. Their reference current, blocking voltage, gate resistance and temperature must match the datasheet test conditions used for scaling.

Advanced MOSFET fields include the current and gate voltage associated with $R_{DS(on)}$, threshold voltage, and the capacitances C_{iss}, C_{rss} and C_{oss}. The interface displays capacitances in picofarads, while the internal code stores SI values.

8.5.2 IGBT data

IGBT conduction loss can be defined directly using V_{CE0} and r_{CE}, or derived from two distinct points on a $V_{CE(sat)}$–I_C curve. Switching loss uses E_{on} and E_{off} together with their reference current, blocking voltage and temperature.

For mission-profile operation, enter $V_{CE(sat)}$ at a second, higher junction temperature and at the same reference current as the first point. The app uses these values to update the IGBT conduction loss during the mission profile. A profile cannot be evaluated correctly if the temperature dependence is missing.

When advanced IGBT inputs are enabled, verify that the gate-emitter test conditions, leakage data and the capacitances C_{ies}, C_{res} and C_{oes}. The value of C_{res} must not exceed either C_{ies} or C_{oes}.

8.5.3 Diode and reverse-recovery data

The basic diode model uses the forward voltage V_f and dynamic resistance R_{on}. If reverse recovery is included, enter the recovery energy E_{rr} or E_{rec}, recovered charge Q_{rr}, recovery time t_{rr} and peak reverse current I_{rrm}. Optional reference values for forward current, reverse voltage and current slew rate allow the recovery data to be scaled to the simulated event.

8.6 Cooling Configuration

8.6.1 Fixed boundary temperature

The fixed-temperature option treats the entered heatsink or thermal-boundary temperature as constant throughout the simulation.

8.6.2 Custom Foster network

A Foster network represents transient junction-to-case thermal impedance using resistance and time-constant pairs. Enter the R_{th} and τ arrays with the same number of strictly positive values. For example:

```
Rth = [0.02 0.05 0.13]
tau = [0.01 0.1 1]
```

The case-to-heatsink resistance $R_{\mathrm{th,ch}}$ may be zero, but it cannot be negative.

During a mission profile, the app calculates the Foster model for each segment and takes it to the next. The temperature at the start of a segment includes heat stored during segments before.

The current implementation uses a Foster model and a simplified thermal boundary. Cauer input and a dynamic heatsink-to-ambient network are not implemented. The reported temperature is an estimate of the switch junction temperature. Heat produced by a separate external diode is not added to the switch-junction model.

8.7 Mission-Profile Operation

8.7.1 Creating a profile

1. Enable Use Mission Profile in the Simulation tab.
2. Download the CSV template or edit the mission table directly.
3. Keep the exact CSV headings Segment, Duration_s, Vin_V, Vout_V, Pout_W and T_amb_C.
4. Check every row before running the profile.

The duration, input voltage and output voltage must be positive. The segment could contain names that are descriptive. The voltage relationship for Boost or Buck topologies must be valid in every step.

8.7.2 Running a profile

The app processes the segments sequentially and restores the original interface values when the mission run finishes. For each segment it stores the losses, energies, output power, efficiency, end temperature and peak temperature.

For Boost and Buck profiles, the app calculates the required L and C_{out} for every row and uses the largest required values for the entire mission. The thermal trace is reconstructed at one-minute intervals, with a shorter final interval when necessary. The thermal state is evaluated using the Foster exponential response over each interval, and the conduction parameter is updated iteratively from the calculated junction temperature.

MOSFET conduction loss is scaled using $R_{\mathrm{DS(on)}}(T_{\mathrm{j}})$, while IGBT conduction loss is scaled using $V_{\mathrm{CE(sat)}}(T_{\mathrm{j}})$. Switching and diode losses remain temperature independent.

8.8 Loss Calculation and Result Validation

8.8.1 Reading the Summary tab

The Summary tab reports conduction loss, switching loss, diode or reverse-path loss, total semiconductor loss and efficiency. The efficiency label indicates if the value is based on measured input power, a semiconductor only power balance or an estimate based on output power and calculated losses. Mission profile results also include loss history and junction temperature plots.

8.9 Maintaining the Application

Application changes normally affect the interface, parameter structures, validation, loss calculations and Simulink models.

8.9.1 Main code responsibilities

getDefaultValues Defines startup choices, device datasets, topology operating points, diode data and Foster thermal networks.

applyDefaultValues Writes the selected defaults into the interface.

getSwitchParams, getDiodeParams, getThermalParams Read and validate the visible input fields.

exportDCDCParamsToWorkspace, exportACParamsToWorkspace Create the variables required by Simulink.

getImplementedModelName Maps each supported topology and device technology to a Simulink model.

runDCDCSimulation, runACSimulation, runDCDCMissionProfileSimulation Control simulation execution and result extraction.

8.9.2 Changing default values

1. Edit the appropriate structure: D.Startup for initial selections, D.Switch for semiconductor data, D.Topology for circuit values, D.Diode and D.Reverse for conduction paths, D.Gate for gate resistances, and D.Cooling for thermal data.

2. Keep internal values in SI units unless a field name explicitly states pF, nF, nC or ns.

3. Check whether an automatic calculation overwrites the value during a run. The relevant functions are:

   calculateAutomaticDCDCComponents;

calculateFlybackTurnsRatio; and

calculateAutomaticACFilter.

4. Restart the app or reselect the affected option, then test the change. Do not edit only the .Value assignments in createComponents, because applyDefaultValues may overwrite them.

Store the part number in ReferenceDevice and keep its electrical and thermal values together. Each default dataset should reproduce a documented baseline rather than combine convenient values from several parts or test conditions.

8.9.3 Adding semiconductor data

To replace the reference part within an existing technology, update ReferenceDevice and the matching values in that branch of getDefaultValues. The interface currently selects a technology rather than a catalogue of part numbers, so a new menu entry is not required. Run the existing topology set and compare the result with the previous baseline.

To add a selectable technology or diode type:

1. add its label to SwitchTechnologyDropDown.Items or DiodeTypeDropDown.Items;
2. define complete switch, diode, gate, reverse-path and Foster-network defaults;
3. update updateSwitchTechnologyFields, updateDiodeFields and related visibility helpers;
4. extend getSwitchParams, getDiodeParams and validateSwitchInputs;
5. connect the required conduction, switching and reverse-recovery calculation methods;
6. export any new workspace variables and map a compatible Simulink model;
7. update validateSupportedCombination; and
8. test one valid and one invalid configuration for every affected topology.

8.10 Changing Simulink Models or Converter Topologies

8.10.1 Replacing or adding a model

1. Place the .slx file on the MATLAB path and add its name, without the extension, to getImplementedModelName.
2. Preserve the variables exported by the relevant DC/DC or AC export function. If an input name changes, update both the model and the export code.

3. Preserve the required logged outputs. DC/DC models must provide Vout, Iout, VDS, VD, Isw, IL, ID and PWM, together with intrinsic-diode signals where required. Single-phase models also need Iin, Vout and Iout. Three-phase models need Iin, Va, Vb, Vc, Ia, Ib and Ic.

4. For bridge converters, provide VDSn, Iswn, IDn, VDn, Gn and VGSn signals for each active device, using the _sim names accepted by readDeviceSignalMatrix. The expected device counts are 2, 4 and 6 for half-bridge, full-bridge and three-phase models, respectively.

5. Confirm that time vectors are strictly increasing, all signals are finite, diode polarity matches the loss calculation and complementary gate signals do not overlap. The half-bridge runner includes a shoot-through check.

6. Close or clear the previous loaded model, restart the app and compare voltage, power, current stress, losses and efficiency with a trusted baseline.

8.10.2 Adding a converter topology

Add the topology selector and schematic, return its name from getSelectedTopology, display its parameter panel, define defaults, add validation and workspace export, map the Simulink model, specify the active-switch count and extend result extraction. If mission-profile operation is required, also extend the required columns, CSV template, row validation, segment assignment, result structure and mission runner. The presence of a CSV template alone does not provide mission-profile support.

8.11 Troubleshooting

Unsupported Configuration The selected topology and device combination is blocked, the model mapping is incomplete, or the required .slx file is not on the MATLAB path.

Invalid Inputs A required visible field is empty, non-finite, negative or outside its permitted range.

CSV Error A required heading differs from the generated template, or one or more rows contain invalid data.

No valid switching energy The voltage, current or gate signals do not contain resolvable transitions. Check signal names, polarity, solver step size and dead time.

Model busy Stop or close the loaded model, clear the workspace if necessary and rerun.

8.12 Known Limitations

- Si IGBT inverter models, SiC cascode JFETs, Cauer thermal input and AC mission-profile execution are not supported.

- Several inverter technology selections share generic MOSFET models. The selected label alone does not prove that the corresponding Simulink block represents that device.
- Normal DC/DC runs automatically resize passive components, and the Flyback model uses an automatically calculated turns ratio. To manually fix a passive component value, code change will be required.
- The thermal model does not include a full dynamic heatsink-to-ambient network and does not add external-diode heating to the switch junction.
- Mission-profile switching and diode losses are not temperature-dependent with the present input data.
- Temperature-dependent conduction parameters are based on linear interpolation or extrapolation between two user-provided points; they are not full datasheet curve fits.

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