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MASTER's Degree in ELECTRONIC ENGINEERING



MASTER's Degree Thesis

**Design, Analysis, and Control of a
PV-Fed Resonant Active-Bridge-Based
DC-DC Battery Charger**

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Abstract

During the last few decades utilizing the solar energy has been experiencing vast progress. The conversion of solar energy to electricity is done through photo-voltaic (PV) panels; where, the solar irradiation is converted to direct current (DC) form of electric energy. The solar PV has vast applications in different industries, including renewable energy generation at residential, industrial, and utility scales, aerospace, street lighting systems, etc. In order to harness the energy from the solar PV panels often a DC-to-DC power electronics converter is needed where it should extract the maximum energy. These DC-DC converters should obey different requirements including, but not limited to, efficiency, power density, low electromagnetic interference (EMI), and low cost. The importance of each requirement is dominantly dictated by their application industry, for example, in aerospace applications the performance is the most important factor while other industries might be more cost sensitive. To meet these requirements, this thesis involves modeling, analysis, design, control, and PCB development of a PV-fed DC-DC power electronics converter for battery charging application; where, maximum power point tracking (MPPT), control strategy, and voltage control are explored.

In this thesis a novel resonant-based DC-DC power converter is developed as the interface between a single PV panel and a 4-cell battery to extract the maximum power from the PV panel for charging the battery; while, maintaining a safe charging profile as well. The objectives have mainly been to develop a high-performance DC-DC battery charger, while, attempting to minimize the cost. In order to provide a high performance in terms of efficiency, power density, and low EMI the modulation scheme of the converter plays an important role. The modulation scheme of this resonant topology is based on a combined frequency modulation (FM) and phase-shift modulation (PSM). The FM assure the operation in inductive region; hence, providing a zero-voltage switching (ZVS) for the inverting stage of the power conversion. The ZVS, not only, eliminates the switching losses of the MOSFETs, but also, because of its soft-switching nature it reduces the EMI footprint significantly. The PSM plays an important role on the zero-current switching (ZCS) of the rectification stage contributing to an enhanced efficiency; while, it could also be utilized for power flow control. The thesis also includes designing a control system for this battery charger that extract the maximum power from the PV panel by the use of a MPPT algorithm. In addition, the control system involves a constant voltage (CV) controller, that controls battery voltage when the battery voltage or its state of charge (SOC) reaches within a pre-defined margin to prevent the overcharging of the battery.

This work begins with an introduction and literature review; where, the prior state-of-the-art research works on the DC-DC topologies employed with the PV panels are investigated. According to this investigation the objectives of this research work are defined. The next step in this research work provides the description of the PV panels electrical characteristics, their I-V characteristics, and their maximum power point definition. This step also includes a comprehensive analysis of the commercially available PV panels which is the basis of the electrical specification for the DC-DC battery charger design.

Following the definition of the electrical specification, the mathematical modeling, analysis, and design of the DC-DC resonant battery charger along with its control system architecture are conducted. The modeling includes a detailed switching cycle mathematical representation of the topology along with power flow analysis based on the control parameters. The developed mathematical model is implemented and validated using MATLAB tool. In addition, LTSpice

simulation tool has been utilized throughout the analysis for validation the detailed switching behavior along with the power loss evaluation of key components (e.g., MOSFETs, inductor, gate driving) and efficiency validation for the proposed resonant DC-DC battery charger. The PSIM tool is utilized for implementing the MPPT and CV control schemes along with the topology to validate the effectiveness of the designed close-loop control approaches. The analysis and simulation efforts have been the guide for the selection of the components with the appropriate ratings for developing the schematic in Altium Designer tool; moreover, the PCB layout has been designed with special attention to optimizing the switching loops and gate driving along with proper separation between the PV, battery, and micro-controller domains.

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Acronyms

CV

constant voltage

DAB

dual active bridge

DC

direct current

EMI

electromagnetic interference

EU

European Union

FB

full bridge

FHA

first harmonic approximation

FM

frequency modulation

HB

half bridge

KCL

Kirchhoff current law

KVL

Kirchhoff voltage law

MPP

maximum power point

MPPT

maximum power point tracking

OB2C

on-board battery charger

OB2M

on-board battery module

PSM

phase-shift modulation

PV

photovoltaic

PWM

pulse-width modulation

SOC

state of charge

SR

synchronous rectification

ZCS

zero-current switching

ZVS

zero-voltage switching

Chapter 1

Introduction

1.1 PV Solar Energy Generation Trends and Outlook

During the last few decades utilizing the solar energy has been experiencing vast progress. According to Eurostat, the generated solar energy in European Union (EU) represents 19.9% of total electricity generation in third quarter of 2025 totaling 122,317 gigawatt-hours (GWh), with an steady growth over the last decade [1]. This growth is also evident from Fig. 1.1, depicting photo-voltaic (PV) solar generation in EU since 2017 to October 2025. Moreover, continuous development of electrified technologies such as transportation and artificial intelligence (AI) data centers leads to an increased demand; hence, requiring more energy generation from different resources including solar. The PV solar energy market experiences different growth rate in various geographical location; however, countries like Germany, Italy, Spain, and France are expected to provide an accumulative market more than 150 GW by 20230 [2]. This emphasizes the continuous need for research in the PV solar energy generation filed.

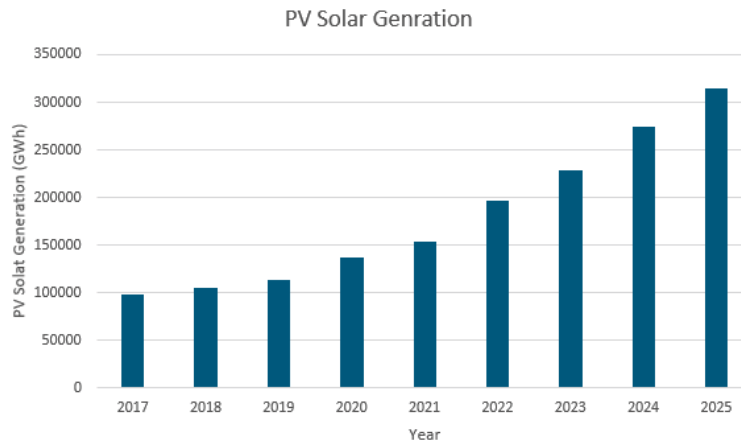


Figure 1.1: Annual PV solar generation, from 2017 to October 2025 in EU.

1.2 PV Solar Energy Conversion and Applications

The conversion of solar energy to electricity is done through PV panels; where, solar irradiation on the PV panels is converted to direct current (DC) form of electric energy. The solar PV has vast applications in different industries, including renewable energy generation, short-range drones, autonomous delivery robots, golf carts, aerospace, street lighting systems, lighting for traffic signs, etc. In order to harness the energy from the solar PV panels often a DC-DC power electronics converter is needed. Because of the natural change in the sun irradiation, the available energy from PV panels has an intermittency nature. For this reason the interface DC-DC converter should extract the maximum energy at each given sunlight condition. Moreover, from electrical perspective, these DC-DC converters should meet different requirements including, but not limited to, efficiency, power density, low electromagnetic interference (EMI), and reliability, while, maintaining the cost effectiveness. The importance of each requirement is dominantly dictated by their application industry, for example, in aerospace applications or flying objects applications the performance and reliability is the most important factor while other industries might be more cost sensitive.

Many applications, including drones, autonomous delivery robots, golf carts, etc., are utilizing a 12V, 24V, or 48V on-board battery module (OB²M) as the sole source of energy. Some of these applications are more sensitive to the weight of their battery module (BM) in order to maximize their range. Extending the range could be made feasible by utilizing a smaller BM, but, with a PV-fed on-board battery charger (OB²C). During daylight the solar energy could be utilized as the source of energy as well as to charge the BM and during night hours or when the sun irradiance is not available the OB²M could be utilized which it will, in turn, extend the range significantly. In this context, a single PV panel could be utilized to minimize the weight and the OB²C will utilize a maximum power point tracking (MPPT) control strategy to extract the maximum power at different sun irradiance conditions for charging the OB²M.

1.3 Background on Interface DC-DC MPPT Converters for PVs

With the increased growth in PV solar energy as mentioned in Section 1.1, the work on developing interface DC-DC converters with MPPT control has also been advancing. In order to identify potential improvement opportunity in the existing MPPT-based DC-DC converters an initial study on the existing research work is necessary. Therefore, this section aims at an introductory review on different type of DC-DC converters and explore their pros and cons. Through this initial review potential improvement and contribution objectives for this thesis are identified. Once the objectives for this research work are defined, a comprehensive literature review that is specifically tailored to this thesis objectives will be provided in Chapter 3.

Depending on the end application, the DC-DC converters could be categorized as either step-up or step-down; where, the PV voltage is increased or decreased, respectively, for adapting to the end application voltage. Both step-up and step-down DC-DC converter architectures could be designed as isolated or non-isolated topologies. Different factors including the required voltage gain, defined as the ratio between the end application voltage and the PV maximum power point (MPP) voltage, and safety requirements dictate if a transformer-based power converter (i.e., isolated topology) is necessary. The galvanic isolation is required in high voltage levels to protect the users against hazardous voltages [3, 4]; however, in applications with high step-up or step-down voltage gains utilizing the transformer turn ratio is also beneficial to enhance the controllability and possibly the efficiency of the DC-DC converter. This means, if the conversion

ratio is very high or very low, for the step-up and step-down cases, respectively, a transformer with appropriate primary-to-secondary turns ratio is needed. It should be noted that utilizing transformer could lead to lower power density; hence, in application with limited required voltage gain, if isolation is not a requirement a non-isolated topology is more desirable. Fig. 1.2 depicts the block diagram for both non-isolated and isolated (transformer based) DC-DC converters for solar PV application.

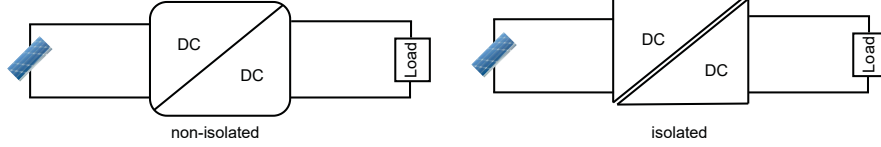


Figure 1.2: Block diagram for non-isolated and isolated DC-DC converter interfacing PV panel to end application.

The non-isolated architecture presented in Fig. 1.2 could be broadly categorized as buck and boost topologies, while the isolated architecture could also be categorized as an isolated extension of these topologies; however, their control strategies and modulation schemes are different. The amount of research work on DC-DC converters for interfacing solar PV is extensive. In order to concentrate the literature review study based on their relevance to the research work in this thesis, the requirements for the subject DC-DC converter in this thesis need to be first defined. These requirements along with their justification are summarized as follows.

- The intended application in this thesis is for a 4-cell Li-ion battery with minimum and maximum cut-off voltages of 10V and 16.8V, respectively. Considering the selected PV panel specification in Table 2.1, the focus of this work will be on the step-down DC-DC topologies.
- Considering the voltage range of the selected single PV panel and the battery voltage range, the voltage ratio is limited; hence, a non-isolated low-voltage MPPT-controlled DC-DC converter will be required.
- Considering the battery size, one possible application of the subject DC-DC converter will be the OB²C. These applications often are accompanied with on-board electronics sensitive to EMI. This brings about the requirement for soft-switching strategies to minimize the dv/dt and di/dt of the conversion stage which lead to reduction of EMI footprint.
- In applications where the weight and power density are important (e.g., short range drone or delivery robots), the efficiency of the DC-DC converter also plays an important role. Increased power density and reduced weight often conflicting with the efficiency, as the former requires an increase of switching frequency. Increased switching frequency leads to higher switching losses in the MOSFETs, reducing the efficiency. To enhance the efficiency, two requirements should be included as:
 - Implementing the ZVS and ZCS strategies to minimize the switching losses in the MOSFETS
 - Utilizing synchronous rectification
- Considering the change in solar radiation along with the change on the battery SOC and its voltage, advanced power flow control to meet both MPPT and voltage regulation is needed.

Based on these requirements, this research work intends to provide a comprehensive literature review in Chapter 3, and through the study of the pros and cons of the research in the reviewed literature, objectives of this thesis are summarized in the following section.

1.4 Contributions of this Research Work

In order to build upon the existing research work in the literature, objectives and contributions of this thesis are summarized as follows:

- The first contribution of this work is the thorough data analysis on the commercially available PV modules. This is key to explore the key characterizations of the available PV panels and to define realistic electric specification for the design of the PV-fed DC-DC battery charger along with specifying its nominal operation parameters and the application case.
- Exploring possible topologies for the intended application case along with a comparative analysis of these topologies is the second contribution of this thesis.
- This research also presents a novel PV-fed active-bridge based DC-DC battery charger approach as a resonant topology with a fresh look into its operation principles. The synchronous rectification (SR) is utilized in the rectification stage to enhance the efficiency. A novel control strategy based on a combined frequency and phase-shift modulations (FM and PSM) is also presented with a switching scheme that ensures the ZVS in the inverting stage as well as both ZCS and ZVS for the SR stage. The modulation scheme combines the dual active bridge (DAB) and resonant (e.g., LLC and CLLC) topologies switching schemes to enhance the power flow control, especially, in corner cases where one of the FM or PSM might outperform the other one. The control strategy aims at MPPT for the PV-panel to extract its maximum power through a frequency modulation scheme; while, utilizing the phase-shift modulation to prevent very high switching frequencies under operation conditions where the battery charging power requires significant reduction. Moreover, depending on the BM state of charge (SOC), a constant voltage (CV) charging profile will be tracked with the help of frequency modulation (FM) to attain the required voltage gain and phase-shift modulation (PSM) for meeting the charging power target. The control approaches aim to maintain the ZVS and ZCS under all operation conditions.
- Comprehensive open-loop and close-loop simulation for evaluating the topology operation and validating the proposed control strategy is another goal in this thesis.
- Key components design, and defining the critical requirements for these components with the aim to meet both desired efficiency and cost objectives are also exercised in this thesis. Using the simulation along with a comprehensive components selection through the comparison across different suppliers the key components are selected for the schematic development in this research work.
- The complete schematic and practical PCB layout design considerations are also explored in this thesis.

1.5 Organization of the Thesis

The remaining of this thesis is organized in the following chapters.

- **Chapter 2:** Chapter 2 provides a comprehensive data analysis on over 25000 commercially available PV panels. The goal of this analysis is providing a background on the key parameters of a PV panel, especially, the maximum power point voltage, current, and power. Through this analysis a foundation for defining the specification of the resonant DC-DC battery charger, as the topic of this thesis, is established. MATLAB¹ scripting tool is extensively used for this analysis in which the data for all the PVs are loaded from a database, then, the post processing and graphical visualization of the data through figures are presented.
- **Chapter 3:** This chapter begins with the requirements definition for the PV-fed MPPT DCDC battery charger, an initial literature review on the DCDC converters, and a second literature review on the active-bridge based DC-DC converters and their application in battery charging. Through this review the potential modifications to these existing topologies are identified with the aim to tailor a topology for the PV-fed low-voltage DC-DC battery charger. Two possible candidates for this research work, namely series resonant topology and resonant topology with dividing capacitors, are proposed, then a comparison of transient performance of both topologies is presented. Based on this comparison an active bridge based PV-fed resonant DC-DC battery charger with dividing capacitors and clamping diodes is proposed for this thesis. The dividing capacitors play the role for the resonant tank; while, the clamping diode prevent excess voltage and current stress on the key components in the proposed topology.

Chapter 3 also presents the principle of operation for the proposed resonant DC-DC battery charger; where, a detailed time-domain operation is mathematically modeled. The modeling includes a switching cycle mathematical representation of the proposed resonant DC-DC battery charger. The time-domain modeling and analysis is followed by the control system architecture development for the selected topology along with the power flow analysis based on the control parameters (i.e., switching frequency and phase-shift). The control strategy involves both MPPT and voltage control modes through FM and PSM; where, different MPPT algorithms are presented along with the conditions for switch-over to voltage control mode.

Then, the mathematical model of the voltage gain, input impedance, and power flow principles based on the first harmonics approximation (FHA) methodology are explored; where, the dependency of the output power on the switching frequency and phase shift is investigated. The required minimum and maximum limits of the switching frequency and the phase shift between the inverting and SR switching stages are modeled and analyzed to assure the ZVS of the inverting as well as the ZCS of the SR stages. The mathematical models for the transient time-domain operation and the FHA analysis of voltage gain, input impedance, and power flow are then implemented and validated using MATLAB tool.

- **Chapter 4:** Chapter 4 begins with a design approach for the resonant tank components based on the defined nominal operation condition of the PV-fed resonant DC-DC battery charger in this thesis. Then, using the designed resonant tank parameters a comparative analysis of the series resonant topology and the resonant topology based on the dividing capacitors is presented. The analysis involves open-loop simulation of the two topologies, using LTspice² tool, under different PV MPP conditions to explore their transient and

¹<https://www.mathworks.com/products/matlab.html>

²<https://www.analog.com/en/resources/design-tools-and-calculators/ltspice-simulator.html>

steady-state behavior. Through this analysis the transient current and voltage stress on the key components including the inductor, capacitors, and MOSFETs are investigated. The SPICE model of the key components is used in the simulation to represent the performance of the components and the topologies as close to the real case scenario as possible.

In addition, an open-loop simulation to evaluate the performance of the proposed resonant DC-DC battery charger under the maximum PV MPP conditions across different battery voltage is conducted in this chapter. This analysis involves investigating the required operation switching frequency and phase shift to maintain the ZVS and ZCS for the inverting stage and SR stage MOSFETs, respectively. The power loss of the key components such as resonant inductor and MOSFETs along with the efficiency for the proposed resonant DC-DC battery charger are evaluated.

In order to validate the effectiveness of the proposed control strategies, including both MPPT controller and constant voltage mode, the proposed topology along with its close-loop control architecture is implemented and simulated in PSIM³ software. The closed-loop simulation results are also provided and analyzed in this Chapter.

- **Chapter 5:** The first step in developing the schematic and PCB for the resonant DC-DC battery charger is the component selection. Chapter 5 provides a comprehensive requirements analysis and the key considerations in selecting the components, with a detailed attention to the comparison of different components across multiple suppliers. The open-loop simulation in LTspice is utilized to evaluate the performance of the proposed topology with different component part numbers along with the cost comparison to select the desired part number. According to the selected components a closed-loop simulation using PSIM is also conducted and the results are presented in this Chapter. Then, the designed schematic in the Altium Designer⁴ software is presented along with the key considerations in the design of each functional circuit block. This chapter also presents a detailed overview of the PCB layout design in Altium; where, the key considerations for the power/grounding domains separations, design rules, components placements, and routing are also provided.
- **Chapter 6:** The last chapter of this thesis (Chapter 6), presents the conclusion and possible extension of this research as future work. The conclusion provides the descriptions on the key finding of each chapter. The future work explores the possible application industries and the extension of the proposed topology to fit the specific industry requirements. Especially, for expanding the topology to an isolated version for higher voltage/power in transportation electrification or energy applications.

³<https://altair.com/psim>

⁴<https://www.altium.com>

Chapter 2

Data Analysis on Commercially Available PV Module

2.1 PV Panel characteristics

A PV panel can be modeled as a non-linear generator from the electrical behavior point of view; where, its current-voltage (I-V) characteristic, and consequently its output power (P), are influenced by sun irradiance, temperature, and shading conditions. In order to model the non-linear characteristics of a PV panel different methods are developed; where, the most common is the current source and single-diode representation with a shunt and series resistances as shown in Fig. 2.1 [5].

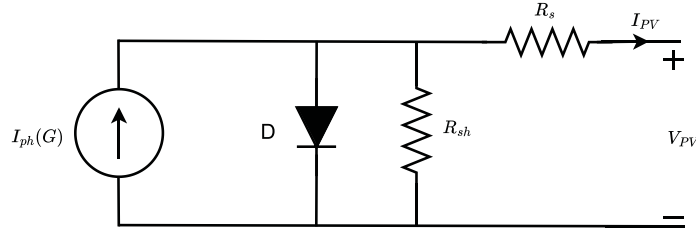


Figure 2.1: PV panel equivalent circuit.

From the equivalent circuit, shown in Fig. 2.1, the PV panel current as a function of its voltage and the circuit parameters could be represented as Eq. 2.1 [5, 6, 7]. In this equation, the temperature-dependent voltage is $V_T = K_B * T/q$; where, K_B , q , and T represent Boltzmann's constant, single electron charge, and temperature, respectively. The description for the remaining unknowns in Eq. 2.1 are described as follows:

- N_s : number of series cell in the PV panel
- I_{ph} : photovoltaic current
- I_0 : diode inverse saturation current
- R_s : the series resistance

- R_{sh} : the parallel resistance
- η : the diode ideality factor

$$I_{PV} = I_{ph} - I_0 \left(e^{\frac{(V_{PV} + R_s I_{PV})}{N_s \eta V_T}} - 1 \right) - \frac{V_{PV} + R_s I_{PV}}{R_{sh}} \quad (2.1)$$

Using the PV panel characteristics given in Eq. 2.1 and $P_{PV} = V_{PV} * I_{PV}$ at $T = 300K$, the PV panel I-V curve along with its output power could be plotted. Using MATLAB¹ tool, a typical I-V and output power characteristics of a PV panel under a certain sun irradiation and specific temperature is depicted in Fig. 2.2. As it could be seen both IV and P curves exhibit a nonlinear behavior. The PV output voltage changes between 0 and its open circuit voltage (V_{oc}), and once the power is drawn from the panel the current changes from 0 to a maximum value of short-circuit current (I_{sc}). As the current and voltage change, the panel output power changes as well, with zero power at $(V_{PV}, I_{PV}) = (0, I_{sc})$ and $(V_{oc}, 0)$ points. In practice the interface DC-DC converter should control the drawn output power between these two points, and ideally at a point referred to as the maximum power point (MPP) associated with the (V_{mpp}, I_{mpp}) on the I-V curve.

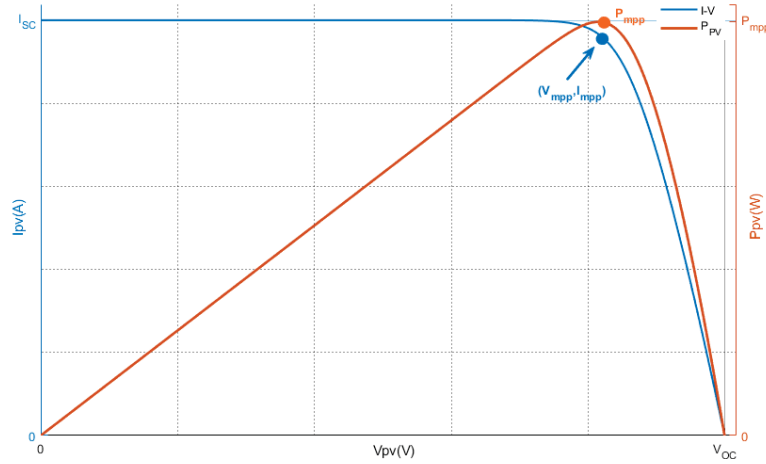


Figure 2.2: A typical PV panel I-V and output power characteristics.

As it is evident from Eq. 2.1, the PV I-V characteristics, and, consequently, its output power are a function of sun irradiation as well as the temperature. This means the I_{sc} and V_{oc} change under different conditions. Fig. 2.3 presents the PV I-V curves at a given temperature. In this figure each I-V curve is associated with a certain sun irradiation with its specific (V_{oc}, I_{oc}) .

Similarly, for each condition the output power curve is different; where, there is an MPP power associated with the (V_{mpp}, I_{mpp}) for each case. The PV output power curves under the same solar irradiation as the I-V curves is depicted in Fig. 2.4. As mentioned before, the PV-fed DC-DC converter is responsible to extract the P_{mpp} from the panel under each irradiation condition.

¹<https://www.mathworks.com/products/matlab.html>

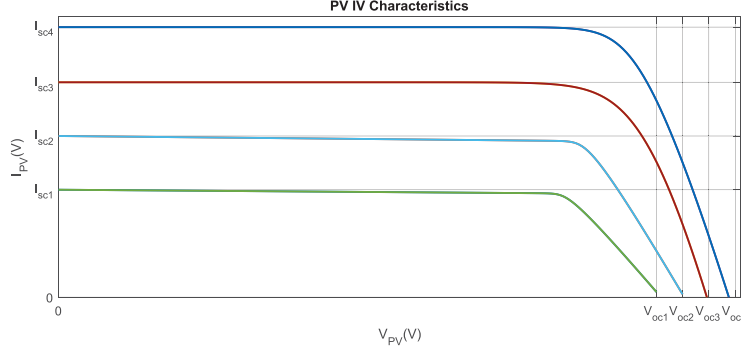


Figure 2.3: PV panel I-V characteristics under different sunlight condition at a specific temperature.

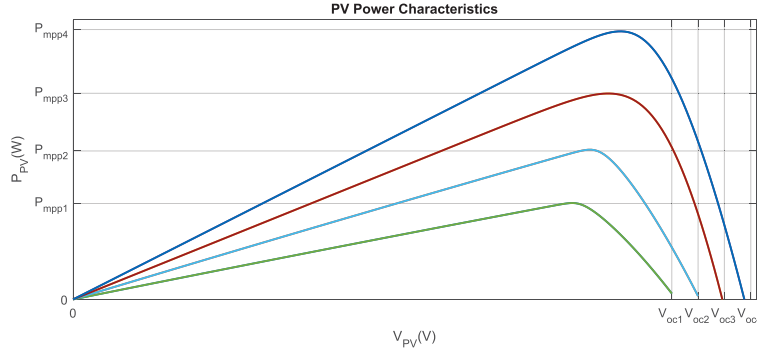


Figure 2.4: PV panel output power curves under different sunlight condition at a specific temperature.

2.2 Benchmarking of commercial PV modules

A list of commercially available PV modules is available on the California Energy Commission website [8], making it possible to conduct an analysis on the commercially available PV panels in this research work and use the results as a guide for defining the specification for the intended DC-DC battery charger design.

The goal of this analysis is to explore that which range of PV panel electrical characteristics (i.e., V_{oc} , I_{sc} , V_{mpp} , and I_{mpp}) are more widely available. The V_{oc} and I_{sc} are key parameters to select the components with an appropriate ratings during the efficiency simulation and analysis. This is also important for components selection during the schematic development phase presented in Chapter 4. The V_{mpp} , and I_{mpp} define the nominal operation power of the interface DC-DC converter critical in the entire design and analysis phase along with controller design presented in Chapter 2. The nominal operation mode is also the most frequent mode at which the DC-DC is operating in MPPT, and, because the converter operates in this mode for extended time period, it has significant implication on the thermal performance of the converter. The thermal behavior dictates that more attention should be paid to the power stage PCB layout and enough heavy copper to be used for handling the current and spreading the heat.

The source data on the available PV modules [8], indicates that there are 230 manufacturers

that have registered PV panels ranging from 2 to 1366 module model numbers, for a total of approximately 25000 units. In order to explore the V_{oc} , I_{sc} , V_{mpp} , and I_{mpp} for all of these units MATLAB tool is used to import the data and the post processing is conducted.

In order to evaluate the voltage range for the PV panel, the number of series cells in the PV panel and their technology should be known. The analysis on all available units revealed that the vast majority of these units (98.6%) are based on the Monocrystalline and Polycrystalline technologies. In more details, 73.3% of the PV modules in the available data belong to the Monocrystalline family; while, 25.3% are based on the Polycrystalline technology. The analysis on the number of series cells in the PV panels, based on these two technologies, is presented in Fig. 2.5. It could be observed that most of these PV panels comprise of 60 - 72 series cells. The typical V_{oc} for each cell of both technologies at 25° under $1000W/m^2$ irradiance falls within 0.55 - 0.66 V range (0.55 - 0.63 V for Polycrystalline and 0.58 - 0.66 V for Monocrystalline) [9], resulting in the V_{oc} for each PV panel within 33 - 47.25 V. The analysis results on the distribution of the V_{oc} for the available PV panels is shown in Fig. 2.6. As it could be seen the V_{oc} for majority of these units falls within 32.8 - 49.9V. The slight difference between the data and the theoretical calculation of $V_{oc,PV} = N_s * V_{oc,cell}$ originates from the fact that solar irradiation and temperature affect the cell V_{oc} [10]. The test conditions for the data are indicated as Standard Test Condition (STC) - 25° ambient temperature under $1000W/m^2$ irradiance, and PVUSA Test Condition (PTC) - 20° ambient temperature under $1000W/m^2$ irradiance [8].

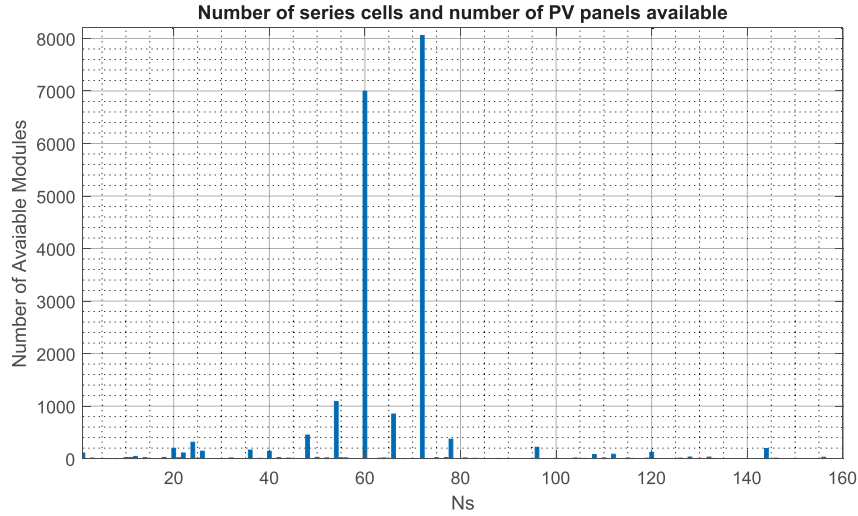


Figure 2.5: Number of series cells in commercially available PV panels.

Analyzing the I_{sc} is important as it is an implication of the transient current sourcing capability of the PV panel ; hence, the DC-DC battery charger along with its PCB should be designed accordingly. It is worth noting that, differently from the panel voltages, the short circuit current depends mainly on the technology and surface area of the cells. The analysis results , as shown in Fig. 2.7, conclude that I_{sc} for the vast majority of the PV panels falls within 8 - 11.8A, with a cluster of data between 13.2 - 14.3A. Since the number of PV panels within 8 - 11.8A range are far more, the bases of the design in this research work is base on this group.

One of the key design specifications for the DC-DC battery charger is its nominal input voltage. In a PV-fed application the nominal input voltage values is imposed by the PV panel mpp voltage V_{mpp} . As it could be seen from Fig. 2.4, the mpp voltage under any irradiance condition will

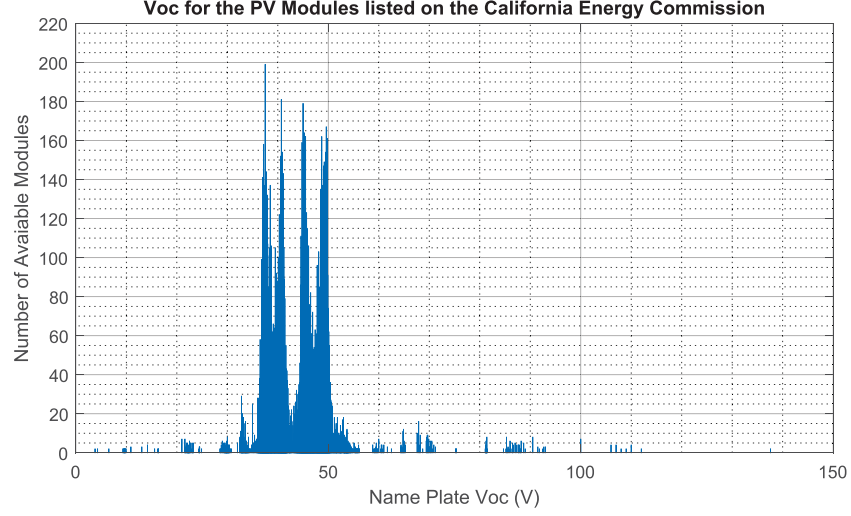


Figure 2.6: The distribution of the available data on the V_{oc} for the investigated PV panels.

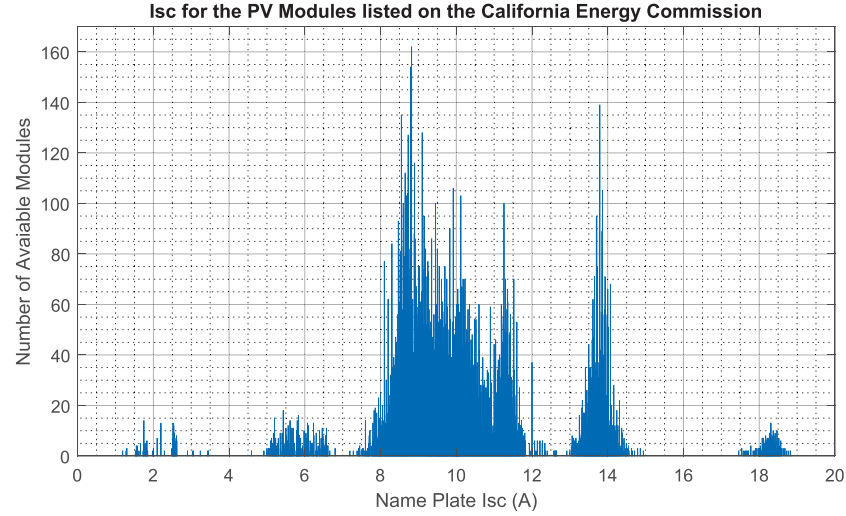


Figure 2.7: The distribution of the I_{sc} for the available data on the PV panels.

be lower than V_{oc} . Fig. 2.8 represents the V_{mpp} range for the PV panels within the data pool. The main cluster of data are in the range of 29 - 42 V. This range is also important, because, it dictates the topology for DC-DC interface converter, and the max allowable battery voltage in case the interface is a buck converter. In a non-transformer base topology, if the inverting stage is a half-bridge, the best case scenario voltage gain is 1/2; hence, the battery maximum voltage should not exceed half of the mpp voltage. In contrary, a topology with a full bridge DC to AC stage has the potential for higher voltage gain; therefore, the battery voltage could be higher.

Another factor to be considered when selecting a PV panel, is the mpp current at which the mpp power could be extracted from the PV while the PV voltage is also at the V_{mpp} . The

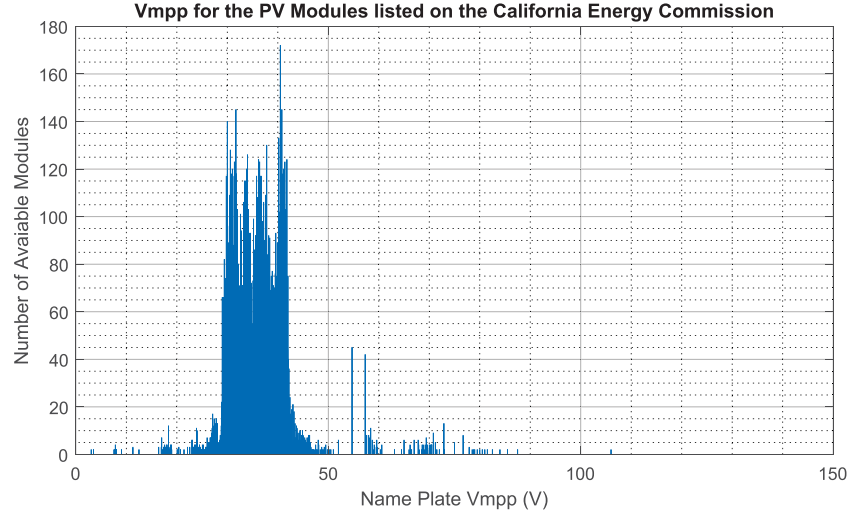


Figure 2.8: MPP voltage range (V_{mpp}) for the available PV panels.

distribution of the I_{mpp} , for the PV modules available in the data pool, is shown in Fig. 2.9. Considering the mpp voltage and current ranges, and according to the data on the available modules the mpp power under the PTC test condition is within a wide range from 20.5 - 706.4 W. This wide range provides the accessibility of PV modules for a wide range of applications; where, depending on the battery module voltage range and its charge current limitation, the appropriate topology for the DC-DC battery charger and its rated power specification are dictated. Based on the conducted analysis, and intended application the desired PV panel specifications for this research work are summarized in Table 2.1.

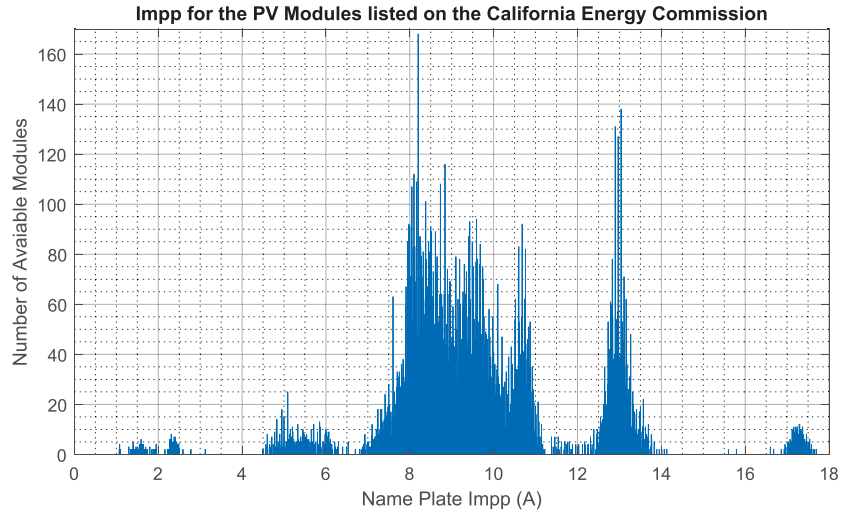


Figure 2.9: The available mpp current (I_{mpp}) range associated with the PV panels.

PV Panel	$V_{oc}(V)$	$I_{sc}(A)$	$V_{mpp}(V)$	$I_{mpp}(A)$	PTC $P_{mpp}(W)$
SF160-24-P165	43.7	5.14	35.5	4.65	145.5

Table 2.1: Parameters for the selected PV in this research work.

Chapter 3

Resonant Battery Charger Topology Analysis and Mathematical Modeling

3.1 Background and Requirements Definition

From the analysis of available PV panels in the market presented in Section 2.2, the target PV module SF160-24-P165 was selected, with the parameters given in Table 2.1. Considering the $V_{mpp} = 35.5V$ and PTC $P_{mpp} = 145.5W$, the topology comparison is conducted under these nominal condition. Note that under sun irradiation different from the PTC condition ($1000W/m^2$), the mpp power is lower than $145.5W$. The nominal input and output parameters used in the comparative analysis are summarized in Table 3.1. Given the parameters in this table and defining an efficiency of η for the DC-DC converter, the battery charging current range could be calculated as $I_{BAT,min} = (\eta \cdot P_{mpp})/V_{BAT,max} \leq I_{BAT} \leq I_{BAT,max} = (\eta \cdot P_{mpp})/V_{BAT,min}$.

PV Parametrs	$V_{mpp}(V)$	35.5
	$P_{mpp}(V)$	145.5
Battery Parameters	$V_{BAT,min}(V)$	12
	$V_{BAT,nom}(V)$	13.2
	$V_{BAT,max}(V)$	16.8

Table 3.1: The input (PV) and output (battery) parameters

To propose an appropriate topology, it should be noted that:

1. Based on the PV and battery voltage parameters given in Table 3.1, a voltage step-down is required.
2. Considering the range for the ratio between battery voltage and PV voltage, the minimum and maximum voltage gains are limited to $0.338 \leq V_{BAT}/V_{mpp} \leq 0.473$. This voltage gain is attainable through a frequency modulation; hence, a transformer is not necessary, and a non-isolated topology with a voltage gain < 0.5 will be sufficient.
3. A voltage gain of < 0.5 means that the inverting stage of the DC-DC converter could be a HB based topology.

4. To enhance the efficiency the rectification stage of the intended DC-DC should be synchronous, meaning, an FB MOSFET-based rectification stage should be utilized.

3.2 Literature Review

3.2.1 General DC-DC Converters Literature Review

Different requirements for the DC-DC battery charger, that is the subject of this thesis research, are described in Section 1.3. Some aspects of the requirements have been explored in literature to some extent; where, different PV-fed battery chargers are also introduced [11, 12, 13, 14, 15]. The authors in [11], have proposed a PV-fed buck resonant converter for battery charging application as shown in Fig. 3.1. It could be seen from this figure that a resonant tank consisting of L_r and C_r along with the diode D_r are added to the traditional buck topology introducing ZVS for the free-wheeling diode (D_m). Although introducing the ZVS reduces the EMI and will eliminate the commutation (switching) losses for the free-wheeling diode, the conduction losses are usually a main contributor to the efficiency, especially where a low duty cycle is used. The lower duty cycle is needed when the PV voltage is at its maximum and battery voltage is at its minimum. This condition is usually accompanied with the maximum PV mpp power along with the minimum battery voltage; hence, the charging current is maximum and the conduction loss in D_m is maximized too, reducing the efficiency. In addition, this topology, similar to the non-resonant buck, operated based on adjusting duty cycle, and hence it provided only one control variable. This will create challenge in terms of accurate power transfer control, especially at the corner cases, where either of PV or battery voltages are at their minimum or maximum limits. The other draw back associated with this topology is the lack of ZCS for D_m , increasing the reverse-recovery losses.

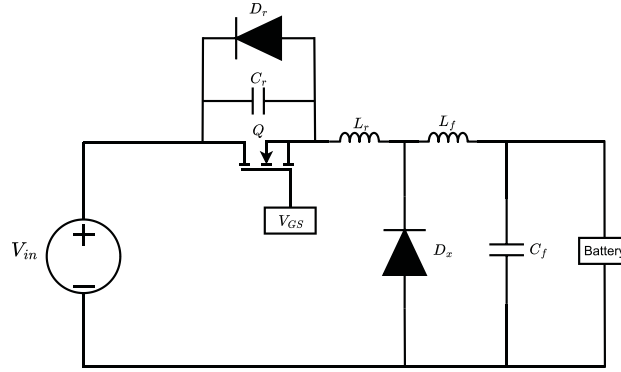


Figure 3.1: ZVS-switched DC-DC buck topology proposed in [11].

A ZCS-based buck topology battery charger is proposed in [12], as shown in Fig. 3.2. The proposed topology also included a resonant tank consisting of L_r and C_r along with the diode D_f . The resonant tank components are an addition to the power stage L_f and C_f (filtering components), increasing the size and reducing the power density. Furthermore, similar to the topology in [11], this buck topology also suffers from high conduction loss for the free-wheeling diode, as well as limiting control parameter to only the duty cycle.

Reference [13] introduces a resonant DC-DC battery charger converter based on the series-parallel resonant tanks. The proposed topology is shown in Fig. 3.3. The inverting stage of this

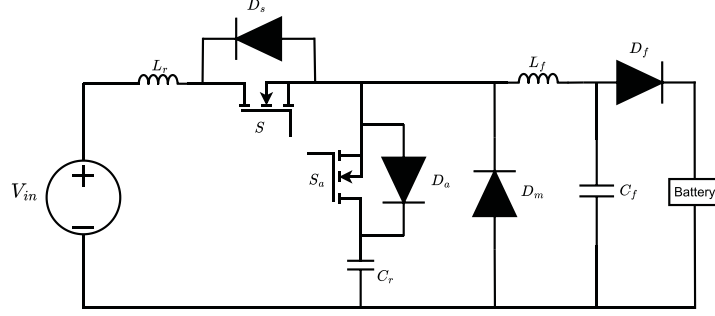


Figure 3.2: ZCS-based DC-DC buck topology for battery charging application [12].

converter is a half-bridge (HB), followed by a series-parallel resonant tank consisting of L_s , C_s , and C_p . The rectification stage of this converter is a full-bridge (FB) diode rectification followed by a large filtering inductor L_o .

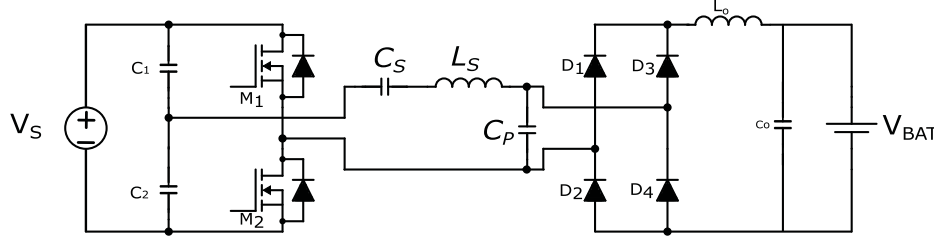


Figure 3.3: Series-parallel resonant DC-DC converter for battery charging application [13].

One immediate drawback of this topology is diode-based rectification; where, their conduction loss has high adverse effect on the efficiency. The output filter inductor L_o is used for a constant DC current charging of battery. Since this inductor carries larger DC battery charging current, it requires high saturation current which often is provided by a large core contributing to a bulky inductor; hence, reducing the power density and increasing the weight. Another characteristic of this topology is the switching frequency as the sole control parameters forcing very high switching frequency in corner cases where the battery voltage is at its minimum or the charging power requires significant reduction. The very high switching frequency contributes to the significant losses in the resonant tank components and the rectification diodes, reducing the efficiency significantly.

Reference [14] presents a parallel resonant DC-DC battery charger (see Fig. 3.4), very similar to the topology in [13], with the exception that only parallel resonant tank is included (L_r and C_r). One of the important aspect of a parallel resonant-tank based topology is the high voltage gain which makes it more suitable for applications where voltage boost is needed. This topology also suffers from the same drawbacks as the one depicted in Fig. 3.3. This resonant DC-DC converter with diode rectification also suffers from low efficiency. The bulky inductor used for maintaining the constant DC output current as mentioned before reduces the power density significantly; while, introducing significant conduction loss associated with its winding dc resistance (DCR).

The authors in [15], present a resonant high voltage gain DC-DC converter with a perturb-and-observe (P&O) MPPT control scheme for solar PV applications. This topology, presented in

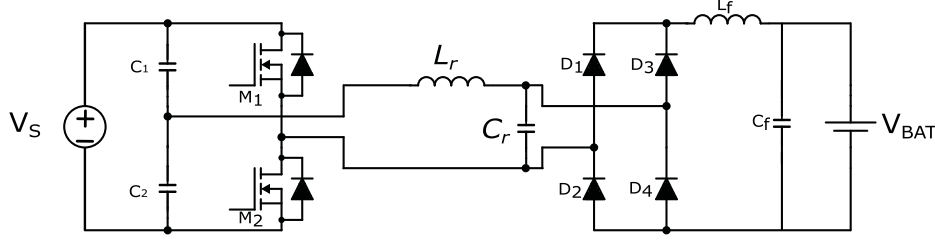


Figure 3.4: Parallel resonant-tank based DC-DC battery charger [14].

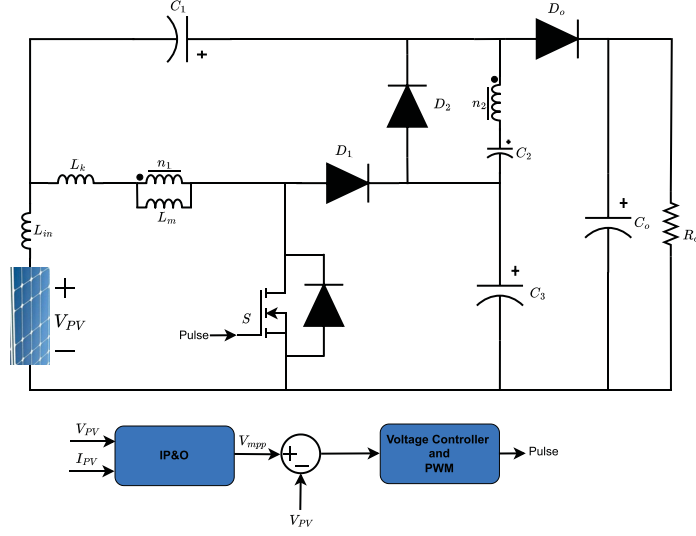


Figure 3.5: PV-fed resonant boost DC-DC converter [15].

Fig. 3.5, is based on the pulse-width modulation (PWM) scheme limiting its control parameters to the pulse duty cycle; while, it is also suitable for voltage boost applications.

References [16, 17, 18] introduce resonant isolated topology based PV-fed DC-DC converters, utilizing a transformer. Given the relative low voltage of the intended application in this thesis as well as the low voltage gain requirement, no galvanic isolation imposed by regulations, and the need to have a compact converter the use of transformer is not justified. The inverting stage for the presented topology in Fig. 3.6 is an FB; however, it could be an HB as well. In this topology, L_r and C_r create the resonant tank while L_m is the magnetizing inductance. Because of the nature of the dual winding, the transformer is often bulky and also exhibits high power loss; hence, in application where isolation is not a must it should be avoided.

3.2.2 Active-Bridge-Based DC-DC Converters Literature Review

Various active-bridge based DC-DC topologies have been introduced in literature; where, their operation principle and control strategies are different. In these topologies, the active bridges, either full bridge (FB) or half bridge (HB), are utilized on both DC to high-frequency AC (HF-AC) (aka., inverting) and HF-AC to DC (aka., rectification) stages. This implies that the design

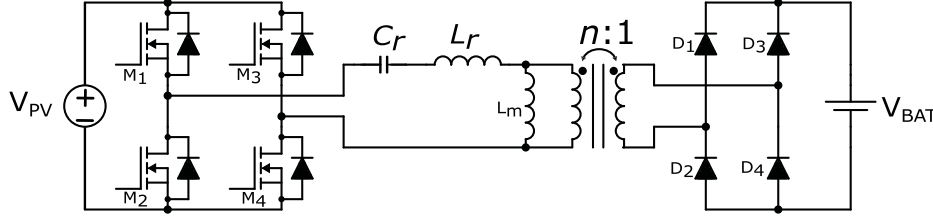


Figure 3.6: A typical DC-DC converter based on LLC topology.

optimization and the performance for these topologies depends on their control as well as the switching schemes for both inverting and rectification bridges. The majority of active bridge topologies are introduced for high voltage application; where, transformer is utilized for providing galvanic isolation and attaining the required voltage gain between the output and input voltages.

A broad family of isolated active-bridge based DC-DC converters are referred to as dual active bridge (DAB) with active bridges in both inverting and rectification stages. The more known DAB term is referred to the topologies that operate at a constant switching frequency and the power flow is controlled through phase shift between inverting and rectification bridges. Both inverting and rectification bridges could be HB or FB as depicted in Fig. 3.7 [19, 20]. In these topologies the two bridges are identical (i.e., both are HB or FB), but could be different as well. Generally, in HB-DAB topology the resonant frequency of the LC tank should be much smaller than the switching frequency. This requires high inductance and capacitance requirements resulting in bulky components. On the other side, a constant switching frequency and phase shift utilization for power control simplifies the control strategy for HB-DAB DC-DC converters. The FB-DAB could be utilized with or without a dc-blocking capacitor (similar to the Fig. 3.7a); however, avoiding the bulky capacitor will be at the cost of more complex control strategies to avoid flux-walking in the DAB transformer. Flux-walking is usually imposed by the mismatch between the positive and negative volt-second across the transformer winding [21]; where, a more accurate switching timing and dedicated control strategy should be utilized to minimize the risk of the transformer saturation.

The second family of active-bridge based DC-DC converters are the isolated resonant converters, namely, LLC and CLLC. This class of converters could be also FB or HB and a combination of both; where, the DC to HF-AC stage is also galvanically isolated from the HF-AC to DC stage as presented in Fig. 3.8 [22, 23, 24]. As it could be seen from Fig. 3.8a, two resonant tanks comprising of L_r and C_r are introduced at the primary and secondary side of the transformer. Even though, the resonant frequency ($\omega_r = 1/\sqrt{L_r C_r}$) of both tanks is considered identical, they could be also different. The dividing capacitors of HB CLLC depicted in Fig. 3.8b along with the inductor L_r created the resonant tank for this topology. From ac perspective the dividing capacitors are in parallel; therefore, the resonant frequency of primary is $\omega_{r1} = 1/\sqrt{L_r(C_{r1} + C_{r2})}$ and the secondary is $\omega_{r1} = 1/\sqrt{L_r(C_{r3} + C_{r4})}$. It should be noted that for these resonant topologies the resonant frequency is high; hence, the LC tank is much smaller than the DAB topologies. On the other side, unlike the DAB topologies the resonant topology control scheme is based on the frequency modulation (i.e., variable switching frequency), making it more complex than the constant switching frequency methods.

As described the two major family of active-bridge based topologies (i.e. DAB and resonant LLC/CLLC), are fundamentally structured around galvanic isolation. The galvanic isolation is a safety requirement in high voltage (HV) applications, the transformer turn ratio could also contribute to either step up or step down gains. On the other side, for low voltage (LV) applications

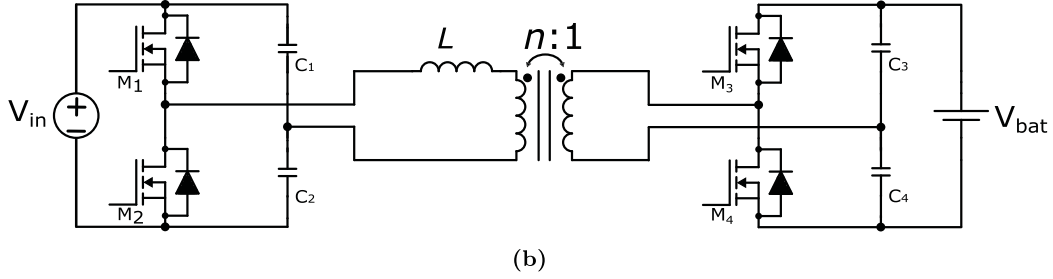
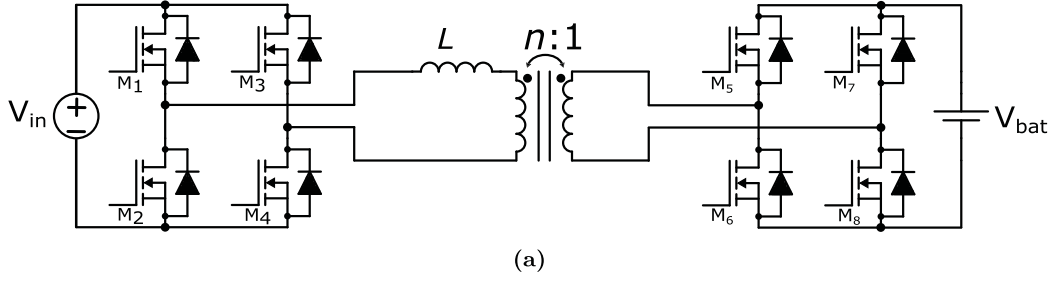


Figure 3.7: Bidirectional DAB (a) FB, and (b) HB.

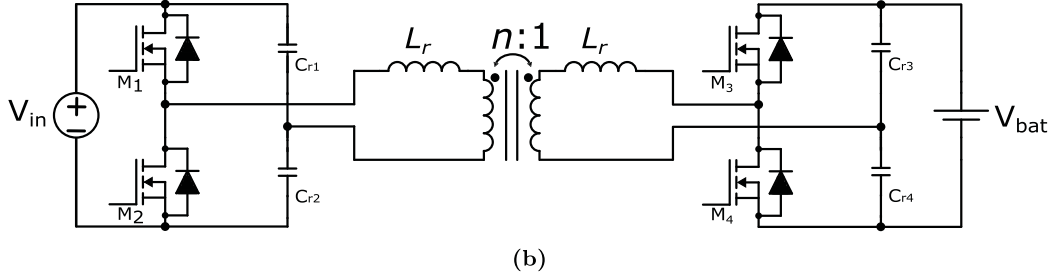
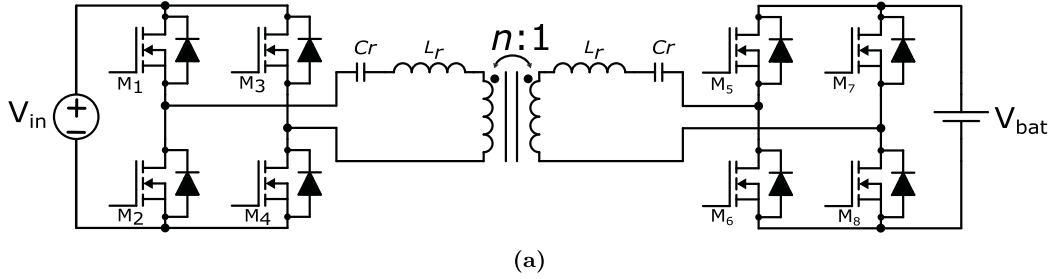


Figure 3.8: Bidirectional CLLC (a) FB, and (b) HB.

or where the ratio between the output and input dc voltages is limited, using a transformer adds unnecessary size, cost, weight, and power loss. Considering the voltage range for the PV panel and battery specified in Table 3.1, a transformer is not necessary; however, a non-isolated topology

based on these active-bridge topologies could be developed. This will provide the advantage of flexibility in the control algorithm, encompassing both MPPT and battery charge control, along with soft-switching scheme to extend the benefit of their low EMI footprint [25]. It should be noted that the soft-switching scheme that provides both zero-voltage switching (ZVS) and zero-current switching (ZCS) will also eliminate the switching losses associated with the power MOSFETs, enhancing the efficiency of the intended topology [26].

Moreover, as mentioned before the required voltage gain, based on the PV and battery voltages subject in this thesis, is less than 0.5. This indicates that the DC to HF-AC bridge could be an HB rather than FB. Utilizing an HB at the DC to HF-AC stage will imply that the HF-AC to DC bridge should be an FB. With an HB inverting bridge and an FB rectification bridge, one possible topology for this thesis research could be the DC-DC resonant battery charger based on a series resonant concept, depicted in Fig. 3.9.

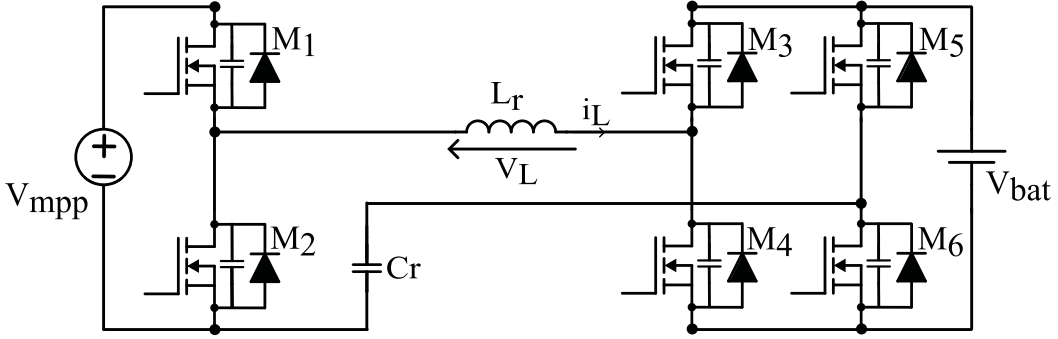


Figure 3.9: PV-fed series-resonant topology for battery charging application.

As it could be seen in Fig. 3.9, the PV voltage is applied to an HB inverting stage; where, the MOSFETs M_1 and M_2 are switching at a frequency of f_{sw} at 50% duty cycle, resulting in a square waveform between the switching node of the inverting stage and the negative terminal of its dc link. This voltage is applied to the resonant tank resulting in a sinusoidal current in the inductor L_r (i.e., i_L) in case the switching frequency is equal to the resonant frequency of the resonant tank. Note that, L_r and C_r create a resonant tank; where, their resonant frequency $f_r = 1/(2\pi\sqrt{L_r C_r})$. In practice f_{sw} should be $> f_r$, so that the inductor current i_L lags the voltage across the SW and PV negative terminal nodes providing ZVS turn-on condition for M_1 and M_2 , effectively eliminating the switching-on losses for these MOSFETs. The main drawback of this topology is high transient current in the inductor during the charging power transient events, resulting in high stress on the resonant capacitor C_r and possibly causing inductor saturation. To prevent inductor saturation, and inductor with high saturation current should be selected, this results in an over sized inductor, consequently, the power density suffers. Alternatively, the soft start algorithms could be utilized that adds complexity to the control algorithm.

3.3 Proposed Topology and Principles of Operation

In order to alleviate the drawback associated with the transient current in the proposed series-resonant topology in Fig. 3.9, the topology depicted in Fig. 3.10 is proposed for this research work. In this figure the input voltage from the PV panel is shown as V_{mpp} . As it could be seen,

the inverting stage includes a half bridge (HB) by MOSFETs M_1 and M_2 . The dividing capacitors C_1 & C_2 are not only participating in the inverting stage, but also, serve as the resonant capacitor forming a resonant tank with the inductor L_r . In addition, the clamping diodes D_1 and D_2 will clamp the transient voltage at node c to either $V_{mpp} + V_{FD}$ or $-V_{FD}$ preventing voltage stress on the dividing capacitors. The figure also represents the synchronous rectification stage which includes M_3 - M_6 followed by the output bypass capacitors and then the BM.

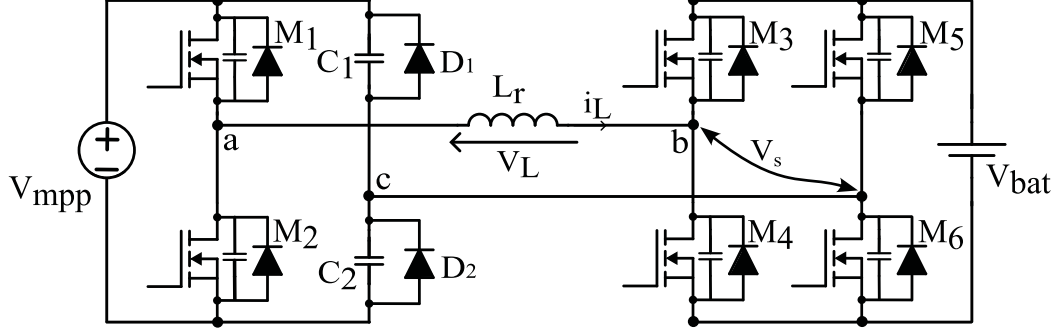


Figure 3.10: Proposed low-voltage PV-fed battery charger.

3.3.1 Time-Domain Analysis

The time-domain analysis and principles of the operation for the proposed topology includes 12 modes that are described in this section. For this analysis a dead time defined as t_{dt} is assumed between the MOSFETs belonging to the inverting HB to prevent a shoot through. In order to improve the efficiency in the SR stage a time delay between the turn-off time of M_3 with respect to (wrt) the turn-off moment of the M_1 is also introduced to maintain the ZCS. By introducing this time delay the ZVS in the SR stage will be automatically guaranteed. Besides, a $t_{d_{SR}}$ between the gate drive pulse signals of the MOSFETs belonging to the same leg, in the SR stage, is also introduced to prevent the short circuit across the battery. It should be noted that the switching frequency in the steady-state operation is assumed high enough that the voltage at node 'c' stays within the clamping levels and hence the diodes D_1 and D_2 do not turn ON. For this reason, the associated circuit for each operation mode is not depicting these diodes.

Mode 1, $t_0 \leq t < t_1$: At the beginning of this mode M_1 from the inverting stage is already ON, and in the SR stage M_3 & M_6 are also ON. During this mode, the voltage at node 'a' (v_a) is clamped at the dc input voltage (V_{mpp}). Fig. 3.11a depicts the state of the devices and current for this mode. By applying the Kirchhoff Current Law (KCL) at node 'c', the inductor current as a function of voltage at this node could be expressed with Eq. 3.1. Moreover, applying the Kirchhoff Voltage Law (KVL) at the input loop, defined by 'a', 'b', and 'c' nodes, and considering the voltage across the inductor as $v_L = L_r di_{Lr}/dt = (L_r \cdot (2 \cdot C)) d^2 v_c / dt^2$, results in the differential equation of Eq. 3.2. Note that in this equation $V_{in} = V_{mpp}$ and $V_o = V_{bat}$.

$$i_{Lr}(t) = 2 \cdot C \cdot \frac{dv_c}{dt} \quad (3.1)$$

$$\frac{d^2 v_c}{dt^2} + \frac{1}{2 \cdot C \cdot L_r} v_c = \frac{V_{in} - V_o}{2 \cdot C \cdot L_r} \quad (3.2)$$

In order to solve the Eq. 3.2 for $v_c(t)$, the initial condition for the voltage at node 'c' and the inductor current are defined as V_{c0} and I_{L0} at $t = t_0$. In addition, From Eq. 3.1 $v'_c(0) = I_{L0} / (2 \cdot C)$

is extracted. Using these initial condition to solve the Eq. 3.2, the governing equations for mode 1 are shown in Eq. 3.3. In this equation the resonant frequency of L_r and dividing capacitors is defined as $\omega_{r1} = \frac{1}{\sqrt{(2 \cdot C) \cdot L_r}}$, $C_1 = C_2 = C$. This mode last until $t = t_1 = (T_{sw}/2) - (t_{dt}/2)$, where $T_{sw} = 1/f_{sw}$ and f_{sw} is the switching frequency. Note that, the voltage at the input of the rectification stage is defined as $v_s = v_b - v_c$. Neglecting the voltage drop across the rectification MOSFETs during their ON state, during mode 1 of the operation the voltage v_s is clamped at V_o .

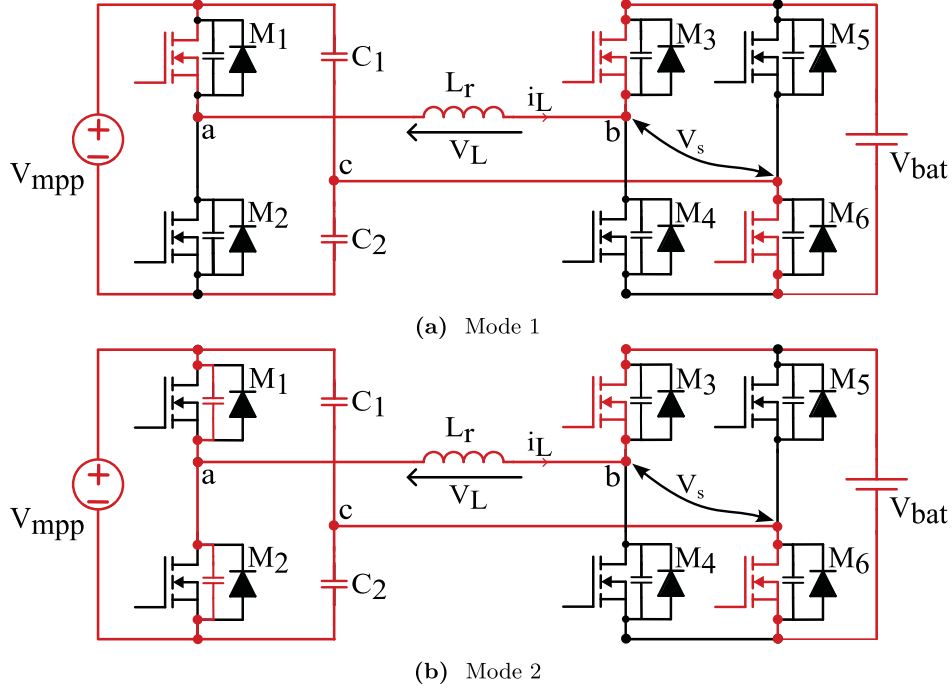


Figure 3.11: Operation modes for the proposed topology: mode 1 & 2.

$$\begin{cases} v_s(t) = V_o \\ i_{M3}(t) = i_{L_r}(t) \\ i_{M4}(t) = 0 \\ v_c(t) = (-V_{in} + V_o + V_{c0}) \cdot \cos(\omega_{r1} \cdot (t - t_0)) + \dots \\ \quad \dots (I_{L0} / (2 \cdot C \cdot \omega_{r1})) \cdot \sin(\omega_{r1} \cdot (t - t_0)) - (-V_{in} + V_o) \\ v_L(t) = -(-V_{in} + V_o + V_{c0}) \cdot \cos(\omega_{r1} \cdot (t - t_0)) - \dots \\ \quad \dots (I_{L0} / (2 \cdot C \cdot \omega_{r1})) \cdot \sin(\omega_{r1} \cdot (t - t_0)) \\ i_{L_r}(t) = -(2 \cdot C \cdot \omega_{r1}) \cdot (-V_{in} + V_o + V_{c0}) \cdot \sin(\omega_{r1} \cdot (t - t_0)) + \dots \\ \quad \dots I_{L0} \cdot \cos(\omega_{r1} \cdot (t - t_0)) \end{cases} \quad (3.3)$$

Fig. 3.12 represents the key waveforms for the time interval of mode 1. As it could be seen from these waveforms, the voltage at node 'c' starts from its initial value V_{c0} corresponding to t_0 , and increases towards V_{in} . Since the operation switching frequency is assumed high enough

wrt the resonant frequency, the final values of v_c is lower than $V_{in} + V_{FD}$; hence, the clamping diode D_1 remains in OFF state. It could also be seen from this figure that during this mode M_3 conducts the inductor current; while, M_4 is in OFF state.

Mode 2, $t_1 \leq t < t_2$: At the end of mode 1, M_1 turns off, M_3 & M_6 remain ON, and mode 2 begins. Fig. 3.11b show the circuit operation in mode 2. During this mode the output capacitances of M_1 and M_2 ($C_{oss1} = C_{oss2} = C_s$) create a resonant circuit with the L_r and exchange energy through the inductor current i_{L_r} . This mode continues until the output capacitance of the M_1 is fully charged while the output capacitance of the M_2 discharges completely. In order to derive the governing equations of this mode, KCL and KVL are applied at node 'a' and the input loop. This results in equations Eq. 3.4 and Eq. 3.5, considering $v_L = L_r di_{L_r}/dt = -(L_r \cdot (2 \cdot C_s)) d^2 v_a / dt^2$. To solve Eq. 3.5 for v_a , the initial condition for voltage at node 'a' is defined as $v_a(t = t_1) = V_{in}$. In addition the initial voltage at node 'c' (V_{c1}), and the inductor current (I_{L1}) could be calculated from the mode 1, Eq. 3.3, at $t = t_1$. From Eq. 3.4, $v'_a(t = t_1) = -I_{L1} / (2 \cdot C_s)$.

$$i_{L_r}(t) = -2 \cdot C_s \cdot \frac{dv_a}{dt} \quad (3.4)$$

$$\frac{d^2 v_a}{dt^2} + \frac{1}{2 \cdot C_s \cdot L_r} v_a = \frac{V_0 + V_{c1}}{2 \cdot C_s \cdot L_r} \quad (3.5)$$

The time duration of mode 2 lasts and the mathematical equations for this mode are presented in Eq. 3.6 and Eq. 3.7, respectively. As described, V_{c1} and I_{L1} are the $v_c(t)$ and $i_{L_r}(t)$ at $t = t_1$, the resonant frequency is $\omega_{r2} = \frac{1}{\sqrt{(2 \cdot C_s) \cdot L_r}}$, and V_{FM} is the forward voltage drop for the MOSFETs body diode.

$$\Delta t_2 = (t_2 - t_1) = (1/\omega_{r2}) \cdot \sin^{-1} ((2 \cdot C_s \cdot \omega_{r2}) \cdot (V_{in} + V_{FM}) / I_{L1}) \quad (3.6)$$

$$\begin{cases} v_s(t) = V_o \\ i_{M_3}(t) = i_{L_r}(t) \\ i_{M_4}(t) = 0 \\ v_c(t) = V_{c1} \\ v_L(t) = -(-V_{in} + V_o + V_{c1}) \cdot \cos(\omega_{r2} \cdot (t - t_1)) - \dots \\ \dots (I_{L1} / (2 \cdot C_s \cdot \omega_{r2})) \cdot \sin(\omega_{r2} \cdot (t - t_1)) \\ i_{L_r}(t) = -(2 \cdot C_s \cdot \omega_{r2}) \cdot (-V_{in} + V_o + V_{c1}) \cdot \sin(\omega_{r2} \cdot (t - t_1)) + \dots \\ \dots I_{L1} \cdot \cos(\omega_{r2} \cdot (t - t_1)) \end{cases} \quad (3.7)$$

Fig. 3.13 depicts the key waveforms for mode 2. This time interval is very short; however, the time axis limits is changed to provide better clarity for the waveforms during this mode. Since the MOSFETs output capacitance (C_{oss}) is much smaller comparing to the dividing capacitors C_1 & C_2 , the inductor current provides a fast discharge of the MOSFET's C_{oss} , resulting in the fast transition of the voltage at node 'a'. This could be seen from the v_L sub-plot in this figure as $v_L = v_a - V_o$. Moreover, the change in the inductor current during this mode is very trivial; hence, to reflect this trivial change the y-axis label is shown as $I_{L1} - - > I_{L2}$. Note that throughout all the time intervals; whenever, the change in a voltage or current is trivial the notation $value1 - - > value2$ is used on the y-axis labels.

Mode 3, $t_2 \leq t < t_3$: At the end of mode 2, while the inductor current is positive, since the gate drive pulse for M_2 is still low, its body diode turns ON and the voltage at node 'a' (v_a) is clamped at $-V_{FM}$. Similar to mode 1, during this mode C_1 and C_2 along with L_r create the

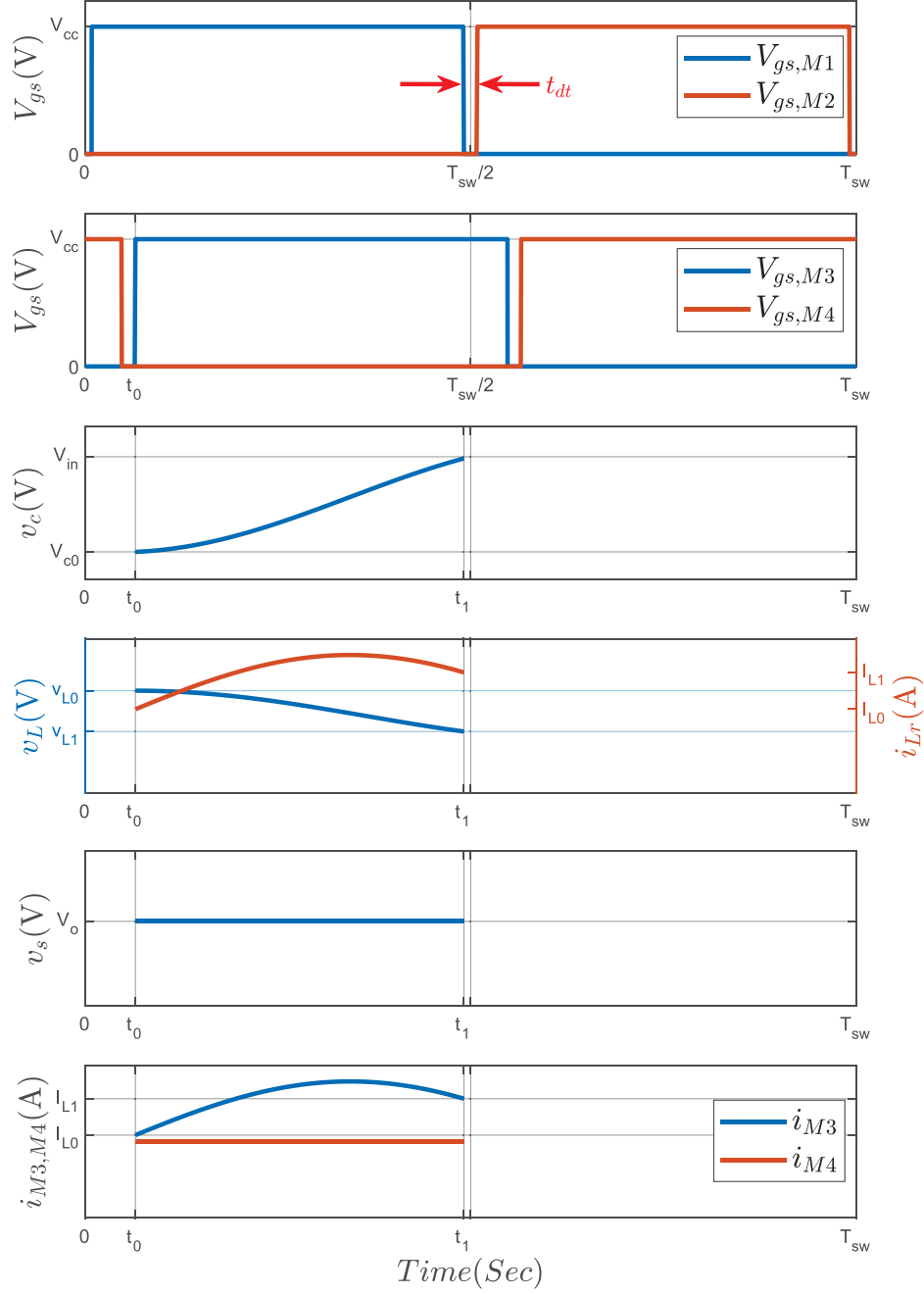


Figure 3.12: Gate drive signals, voltage at node 'c' (v_c), inductor voltage and current (v_L & i_{Lr}), SR stage input voltage (v_s), M_3 and M_4 currents for mode 1.

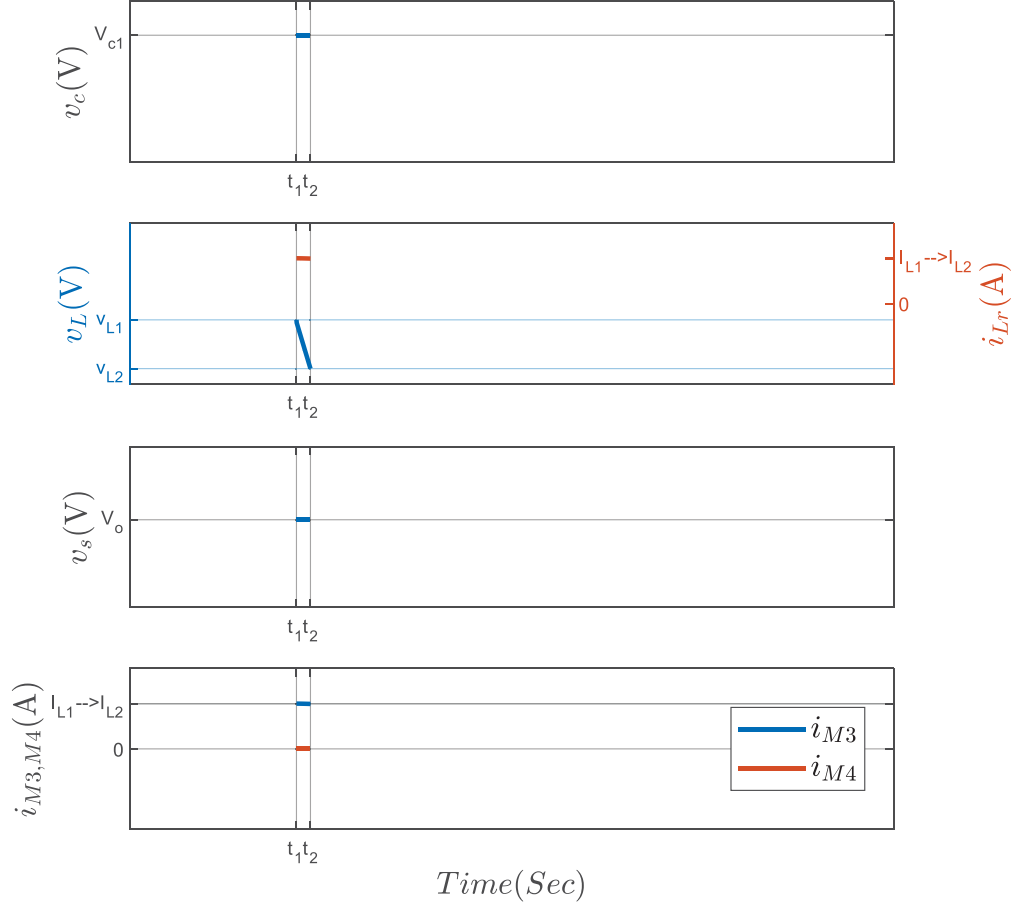


Figure 3.13: Key waveforms for mode 2.

resonant tank. This mode continues until gate-to-source voltage for $M_2(V_{gs2})$ goes high. Fig. 3.14a show different components state in this mode. Using KCL and KVL principles similar to Mode 1, the differential equations during mode 3 are presented in Eq. 3.8 and Eq. 3.9.

$$i_{L_r}(t) = 2 \cdot C \cdot \frac{dv_c}{dt} \quad (3.8)$$

$$\frac{d^2 v_c}{dt^2} + \frac{1}{2 \cdot C \cdot L_r} v_c = \frac{-(V_{FM} + V_o)}{2 \cdot C \cdot L_r} \quad (3.9)$$

The initial condition for solving Eq. 3.9 could be extracted from the equations of mode 2 at $t = t_2$. These initial values are defined as $v_c(t = t_2) = V_{c2}$ and $v'_c(t = t_2) = I_{L2}/(2C)$. The governing equations for mode 3 are shown in Eq. 3.10; where, $I_{L2} = i_{L_r}(t = t_2)$.

$$\left\{ \begin{array}{l} v_s(t) = V_o \\ i_{M_3}(t) = i_{L_r}(t) \\ i_{M_4}(t) = 0 \\ v_c(t) = (V_o + V_{FM} + V_{c2}) \cdot \cos(\omega_{r1} \cdot (t - t_2)) + \dots \\ \quad \dots (I_{L2} / (2 \cdot C \cdot \omega_{r1})) \cdot \sin(\omega_{r1} \cdot (t - t_2)) - (V_o + V_{FM}) \\ v_L(t) = -(V_o + V_{FM} + V_{c2}) \cdot \cos(\omega_{r1} \cdot (t - t_2)) - \dots \\ \quad \dots (I_{L2} / (2 \cdot C \cdot \omega_{r1})) \cdot \sin(\omega_{r1} \cdot (t - t_2)) \\ i_{L_r}(t) = -(2 \cdot C \cdot \omega_{r1}) \cdot (V_o + V_{FM} + V_{c2}) \cdot \sin(\omega_{r1} \cdot (t - t_2)) + \dots \\ \quad \dots I_{L2} \cdot \cos(\omega_{r1} \cdot (t - t_2)) \end{array} \right. \quad (3.10)$$

Fig.3.14 shows the waveforms in mode 3. Similar to mode 1, the x-axis limits in these plots is changes for better clarity of the plots during this mode. As it can be seen, during this interval the change in the voltage across the resonant inductor is not as steep as the mode 2. This stems from the fact that the resonant capacitors are much larger than MOSFET's C_{oss} , resulting in slow voltage changes in node 'c' during the time interval of this mode. Moreover, the same slower dynamic reflects on the less changes in v_c and v_L . Similar to mode 2, as the change in the inductor current from I_{L2} to I_{L3} is low, for better clarity on its y-axis labels the notation $I_{L2} - - > I_{L3}$ is used.

Mode 4, $t_3 \leq t < t_4$: At the end of mode 3, the inductor current is still positive. At the beginning of mode 4, V_{gs2} goes high and M_2 channel is also turned on and the current is transferred from its body diode to its channel. Since the current is still positive, M_3 & M_6 remain ON, but, at the end of this mode when the i_{L_r} reaches zero these two MOSFETs will turn off. Similar to mode 1 and 3, during this mode C_1 , C_2 , and L_r create the resonant tank. Fig. 3.14b represents the circuit state in this mode. During mode 4 the KCL and KVL yield to differential equations presented in Eq. 3.11 and Eq. 3.12, while the voltage at node 'a' (v_a) is clamped to negative terminal of PV defined as reference node 0V.

$$i_{L_r}(t) = 2 \cdot C \cdot \frac{dv_c}{dt} \quad (3.11)$$

$$\frac{d^2 v_c}{dt^2} + \frac{1}{2 \cdot C \cdot L_r} v_c = \frac{-V_o}{2 \cdot C \cdot L_r} \quad (3.12)$$

Defining the initial conditions for this mode as V_{c3} and I_{L3} and solving Eq. 3.12 for $v_c(t)$ results in the governing equations for this mode as shown in Eq. 3.13. Note that the initial conditions are derived from Eq. 3.10 at $t = t_3$.

$$\left\{ \begin{array}{l} v_s(t) = V_o \\ i_{M_3}(t) = i_{L_r}(t) \\ i_{M_4}(t) = 0 \\ v_c(t) = (V_o + V_{c3}) \cdot \cos(\omega_{r1} \cdot (t - t_3)) + (I_{L3} / (2 \cdot C \cdot \omega_{r1})) \cdot \sin(\omega_{r1} \cdot (t - t_3)) - \dots \\ \quad \dots (V_o) \\ v_L(t) = -(V_o + V_{c3}) \cdot \cos(\omega_{r1} \cdot (t - t_3)) - (I_{L3} / (2 \cdot C \cdot \omega_{r1})) \cdot \sin(\omega_{r1} \cdot (t - t_3)) \\ i_{L_r}(t) = -(2 \cdot C \cdot \omega_{r1}) \cdot (V_o + V_{c3}) \cdot \sin(\omega_{r1} \cdot (t - t_3)) + I_{L3} \cdot \cos(\omega_{r1} \cdot (t - t_3)) \end{array} \right. \quad (3.13)$$

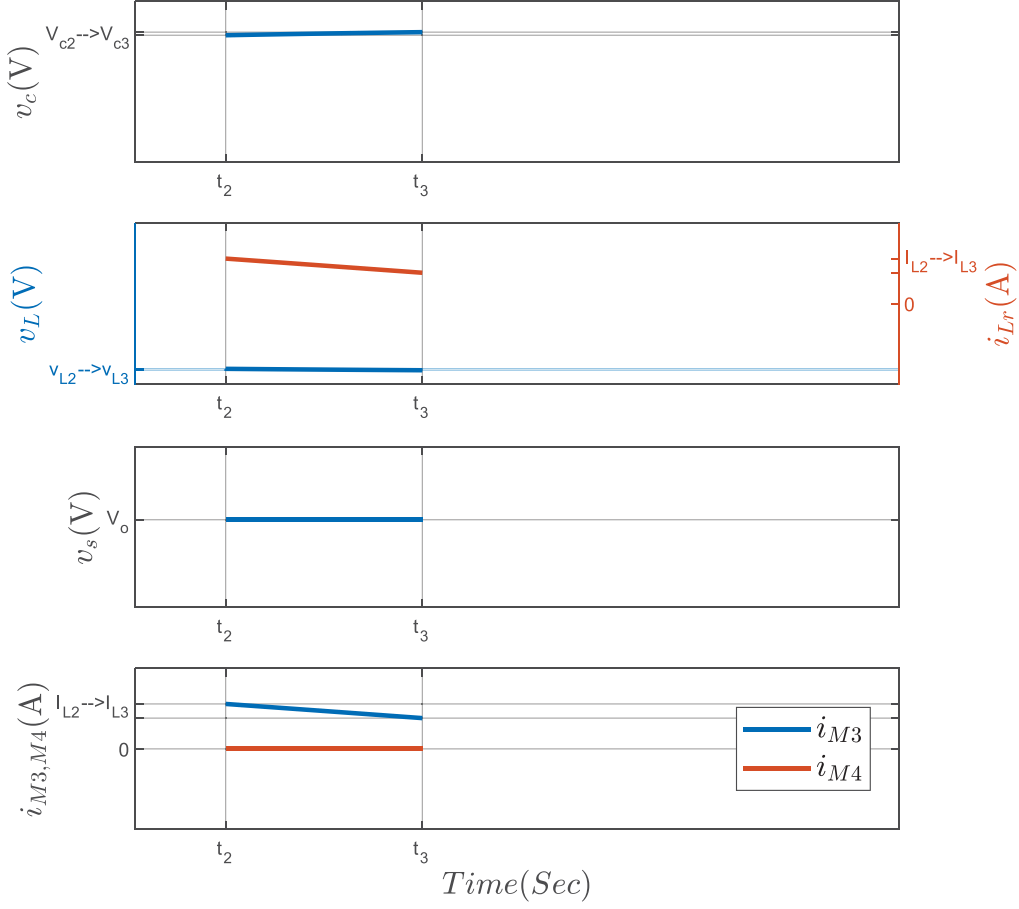


Figure 3.14: Key waveforms during the mode 3 time interval.

At the end of mode 4, the inductor current reaches zero; therefore, the time duration of this mode could be extracted by equating the inductor current of Eq. 3.13 to zero, and assuming $\cos(\omega_{r1} \cdot (t_4 - t_3)) \approx 1$, as show in Eq. 3.14.

$$\Delta t_4 = (t_4 - t_3) = (1/\omega_{r1}) \cdot \sin^{-1}(I_{L3}/((2 \cdot C \cdot \omega_{r1}) \cdot (V_O + V_{c3}))) \quad (3.14)$$

Fig. 3.15 represents the waveforms for mode 4. Note that for this mode also the x-axis limits are adjusted to better present the changes in the waveforms. As expected, at the end of this mode the inductor current reaches to 0, where ZCS condition for turning off M_3 can be achieved.

Mode 5, $t_4 \leq t < t_5$: At the beginning of mode 5, $i_{Lr} = 0$. To maintain ZCS and prevent the short circuit at the battery, M_3 & M_6 turn off. Once these two MOSFETs turn off their output capacitance (C_{oss3} and C_{oss6}) begin to charge; while, the ones of M_4 & M_5 (C_{oss4} and C_{oss5}) begin to discharge, as shown in Fig. 3.15a. The four MOSFETs belonging to the SR stage are identical with the output capacitance of $C_{oss3} = C_{oss4} = C_{oss5} = C_{oss6} = C_{sSR}$. The equivalent circuit is a resonant circuit with the frequency of $\omega_{r3} = \frac{1}{\sqrt{(C_{sSR}) \cdot L_r}}$. The differential equations depicted in Eq. 3.15 and Eq. 3.16 are derived using KCL at the switching node of the rectification

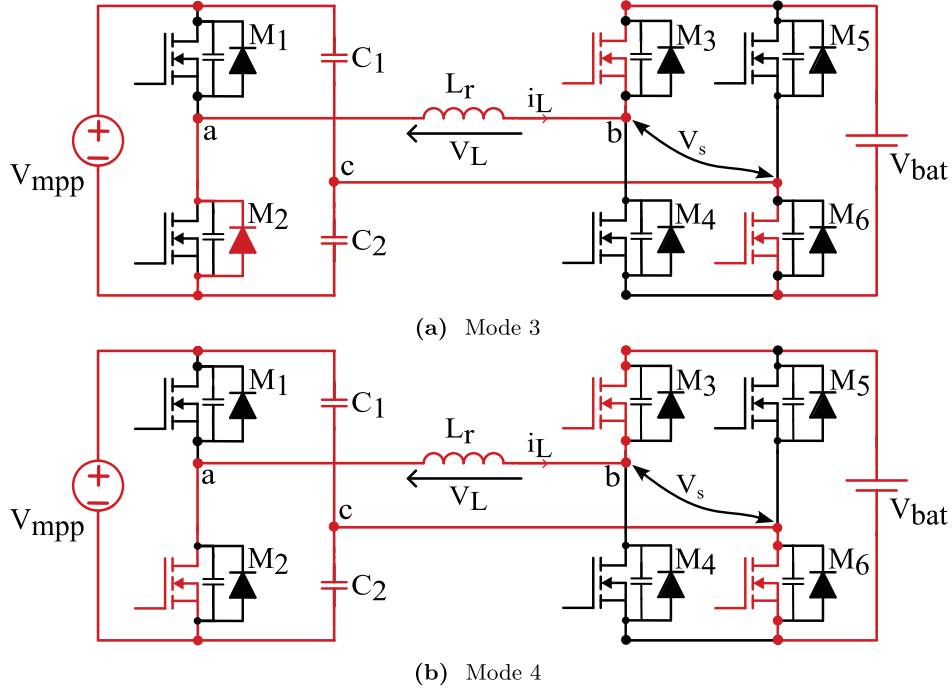


Figure 3.14: Operation modes for the proposed topology: mode 3 & 4.

stage leg 1 ('b') and KVL in the loop consisting of the voltage across M_2 , v_L , and v_s .

$$i_{L_r}(t) = C_{sSR} \cdot \frac{dv_b}{dt} \quad (3.15)$$

$$\frac{d^2 v_b}{dt^2} + \frac{1}{C_{sSR} \cdot L_r} v_b = 0 \quad (3.16)$$

The governing equations for this mode are shown in Eq. 3.17; where, V_{c4} and I_{L4} are the initial value for mode 5 at $t = t_4$. Since the duration of this mode is very short, the changed in the voltage at the dividing capacitors mid point (v_c) is trivial and could be considered constant and remains at V_{c4} . In other words, since $2C$ is much higher than the output capacitance of the SR MOSFETs, the voltage at node 'c' could be assumed constant during mode 5 (i.e., $v_c(t) = v_c(t = t_4) = V_{c4}$). The time duration of mode 5 lasts is presented in Eq. 3.18.

$$\begin{cases} v_s(t) = (V_o + V_{c4}) \cdot \cos(\omega_{res3} \cdot (t - t_4)) - V_{c4} \\ i_{M_3}(t) = 0 \\ i_{M_4}(t) = 0 \\ v_c(t) = V_{c4} \\ v_L(t) = -(V_o + V_{c4}) \cdot \cos(\omega_{res3} \cdot (t - t_4)) \\ i_{L_r}(t) = -C_{sSR} \cdot \omega_{res3} \cdot (V_o + V_{c4}) \cdot \sin(\omega_{res3} \cdot (t - t_4)) \end{cases} \quad (3.17)$$

$$\Delta t_5 = \frac{1}{\omega_{res3}} \cos^{-1} \left(\frac{V_{c4} - (V_o + 2V_{FM})}{V_o + V_{c4}} \right) \quad (3.18)$$

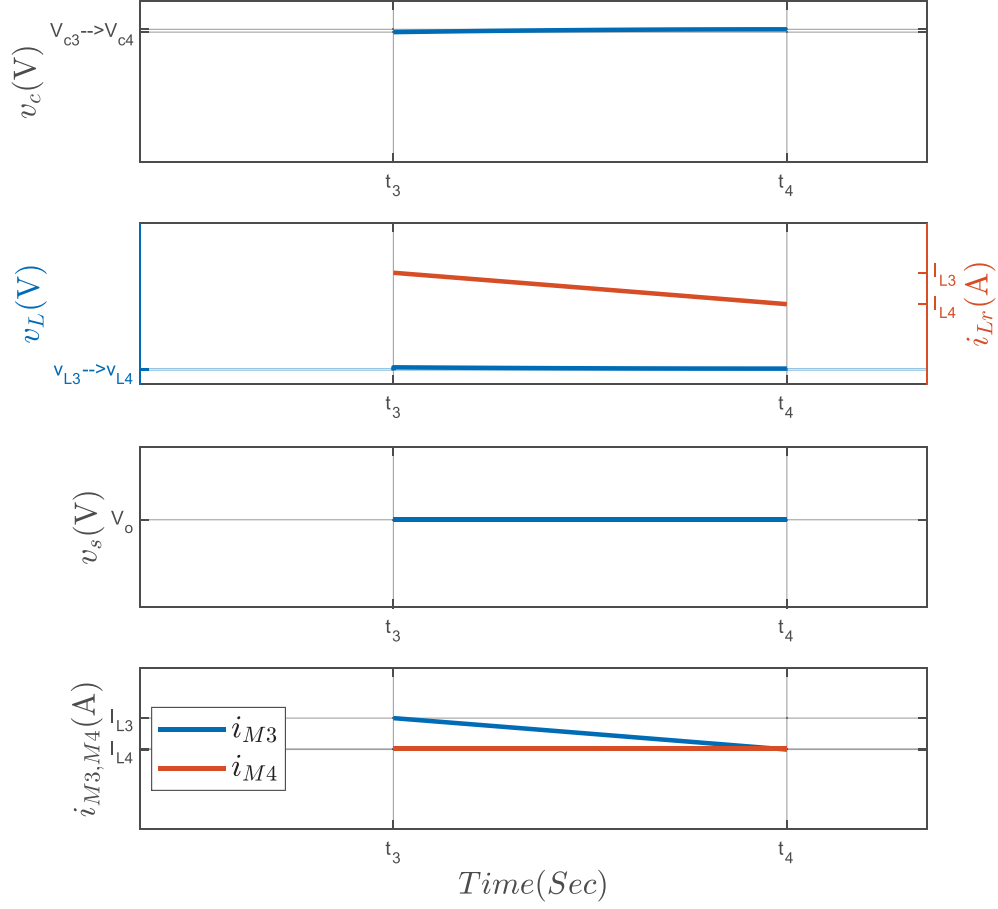


Figure 3.15: Key waveforms for mode 4.

Fig. 3.16 represents the waveforms corresponding to the time interval of modes 5 ($t_4 < t < t_5$); where, the x-axis limits are shortened for better clarity. At the beginning of this mode, M_3 and M_6 are off, and during this mode the output capacitance of M_3 and M_6 are fully charged; while, the output capacitance of M_4 and M_5 are fully discharged. Similar to mode 2, there is a steep transition in the inductor voltage due to fast charging of C_{oss3} and discharging C_{oss4} . This results in a steep decline in the voltage at the node 'b', resulting in the fast transition for ' $v_s = v_b - V_{c4}$ '. As it could be seen from the v_c sub-plot the change in the voltage at node 'c' is negligible.

Mode 6, $t_5 \leq t < t_6$: As mentioned before, at the end of mode 5, C_{oss3} & C_{oss6} are charged to the battery voltage and C_{oss4} & C_{oss5} are fully discharged, while the inductor current i_{Lr} enters into its negative half cycle. This will result in turning ON the body diode of M_4 & M_5 at the beginning of mode 6. This operation mode is shown in Fig. 3.15b. During this mode the voltage at the input of the SR stage $v_s(t)$ is clamped at $-(V_o + 2 \cdot V_{FM,SR})$ and $V_{FM,SR}$ is the forward voltage drop of the body diode for the SR MOSFETs. During this mode the circuit will start resonating with the same frequency as ω_{res1} . Similar to the previous modes, using the KCL and KVL principles the differential equations Eq. 3.19 and Eq. 3.20 are obtained for mode 6.

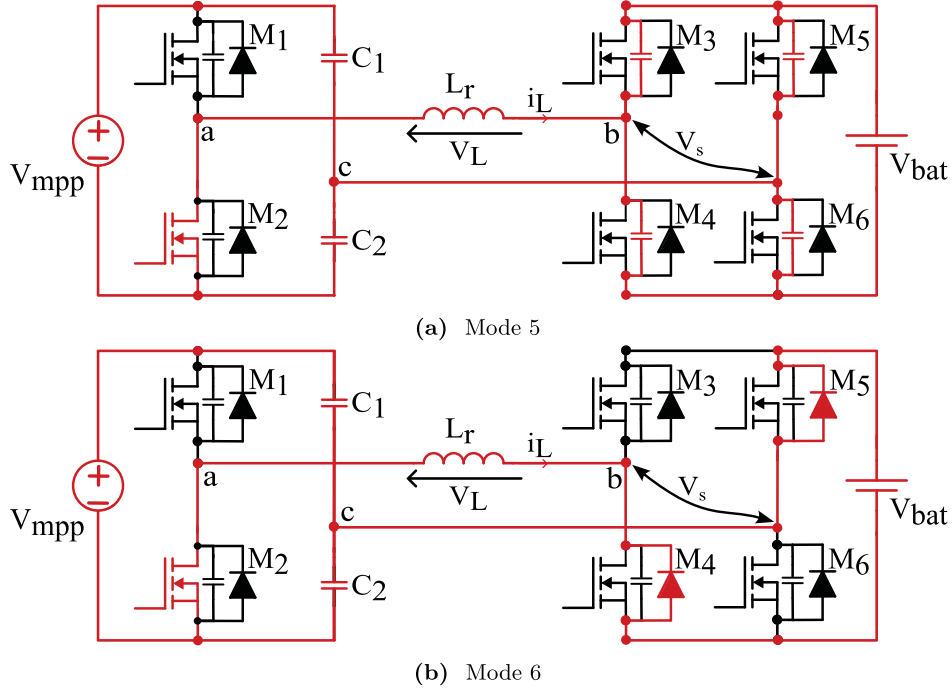


Figure 3.15: Operation modes for the proposed topology: mode 5 & 6.

$$i_{L_r}(t) = 2 \cdot C \cdot \frac{dv_c}{dt} \quad (3.19)$$

$$\frac{d^2 v_c}{dt^2} + \frac{1}{2 \cdot C \cdot L_r} v_c = \frac{V_0 + 2 \cdot V_{FM}}{2 \cdot C \cdot L_r} \quad (3.20)$$

Solving the second order differential equation of Eq. 3.20 yield to the governing equations for this mode as shown in Eq. 3.21. In this equations, V_{c5} and I_{L5} are the $v_c(t)$ and $i_{L_r}(t)$ at $t = t_5$.

$$\left\{ \begin{array}{l} v_s(t) = -(V_o + 2 \cdot V_{FM,SR}) \\ i_{M_3}(t) = 0 \\ i_{M_4}(t) = i_{L_r}(t) \\ v_c(t) = -(V_o + 2 \cdot V_{FM,SR} - V_{c5}) \cdot \cos(\omega_{res1} \cdot (t - t_5)) + \dots \\ \quad \dots \frac{I_{L5}}{2 \cdot C \cdot \omega_{res1}} \cdot \sin(\omega_{res1} \cdot (t - t_5)) + (V_o + 2 \cdot V_{FM,SR}) \\ v_L(t) = (V_o + 2 \cdot V_{FM,SR} - V_{c5}) \cdot \cos(\omega_{res1} \cdot (t - t_5)) - \dots \\ \quad \dots \frac{I_{L5}}{2 \cdot C \cdot \omega_{res1}} \cdot \sin(\omega_{res1} \cdot (t - t_5)) \\ i_{L_r}(t) = (2 \cdot C \cdot \omega_{res1}) (V_o + 2 \cdot V_{FM,SR} - V_{c5}) \cdot \sin(\omega_{res1} \cdot (t - t_5)) + \dots \\ \quad \dots I_{L5} \cdot \cos(\omega_{res1} \cdot (t - t_5)) \end{array} \right. \quad (3.21)$$

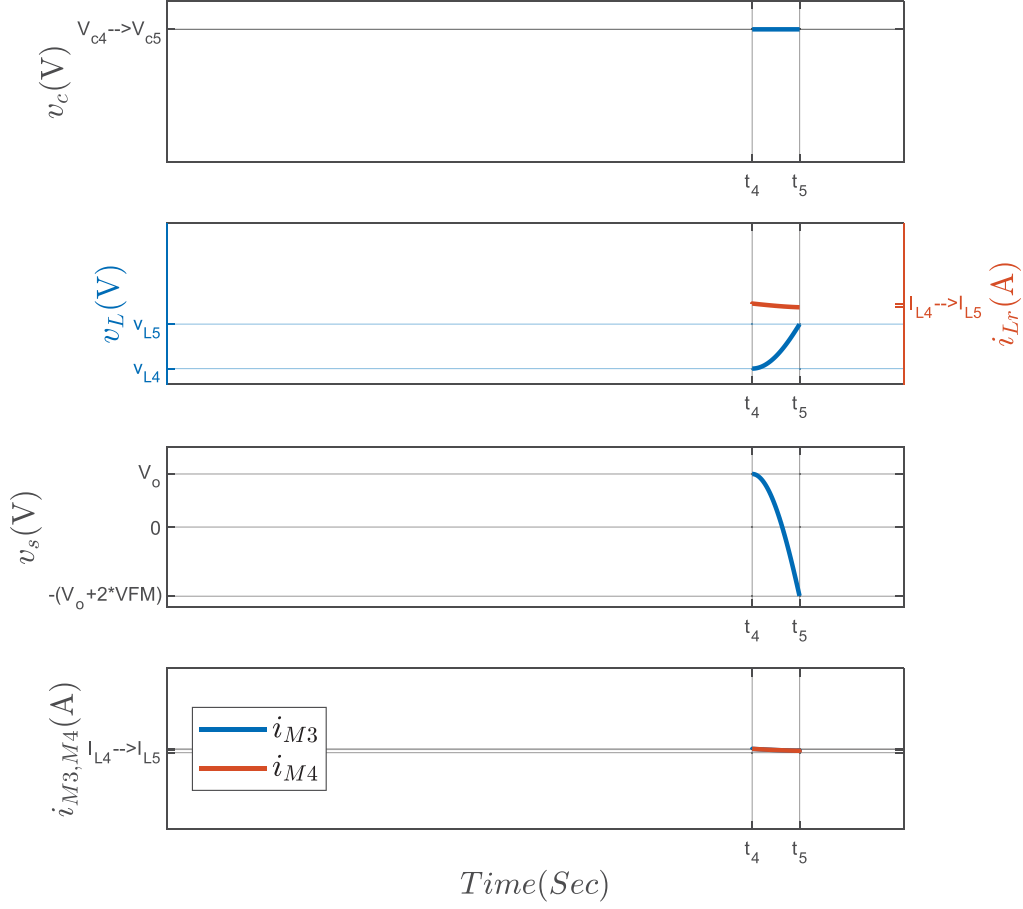


Figure 3.16: Key waveforms for the time interval of mode 5.

Fig. 3.17 shows the waveforms during the time period of mode 6. Considering the short time interval for this mode and larger resonant capacitance wrt the MOSFET's output capacitance the changes in the voltage at node 'c' is trivial. In addition, since the input voltage of the rectification stage (v_s) is clamped to $-(V_O + 2 \cdot V_{FM})$, changes at the voltage of node 'b' is small. With a nearly constant voltage across the inductor, it could be seen that the inductor current change is approximately linear during this mode.

Mode 7, $t_6 \leq t < t_7$: At the beginning of mode 7 the inductor current i_{L_r} is still negative and the dead time between the SR MOSFETs belonging to the same leg will end. This means at the beginning of this mode V_{gs4} and V_{gs5} will go high and; therefore, the channel of these MOSFETs will be also enhanced, and the inductor current transfers from the body diode of M_4 & M_5 to their channels. Fig. 3.17a shows that both M_4 & M_5 MOSFETs are ON during mode 7. Neglecting the voltage drop across M_4 & M_5 MOSFETs ($V_{ds,ON} = R_{ds,ON} \cdot i_{L_r}(t) \approx 0$), during this mode the voltage at the input of the SR stage $v_s(t)$ is clamped at $-V_o$. This mode last until M_2 turns off at $t = t_7 = T_{sw} - (t_{dt}/2)$. The differential equations for this mode are extracted with the same KCL and KVL principles as mode 6 with a key difference that v_s is clamped at

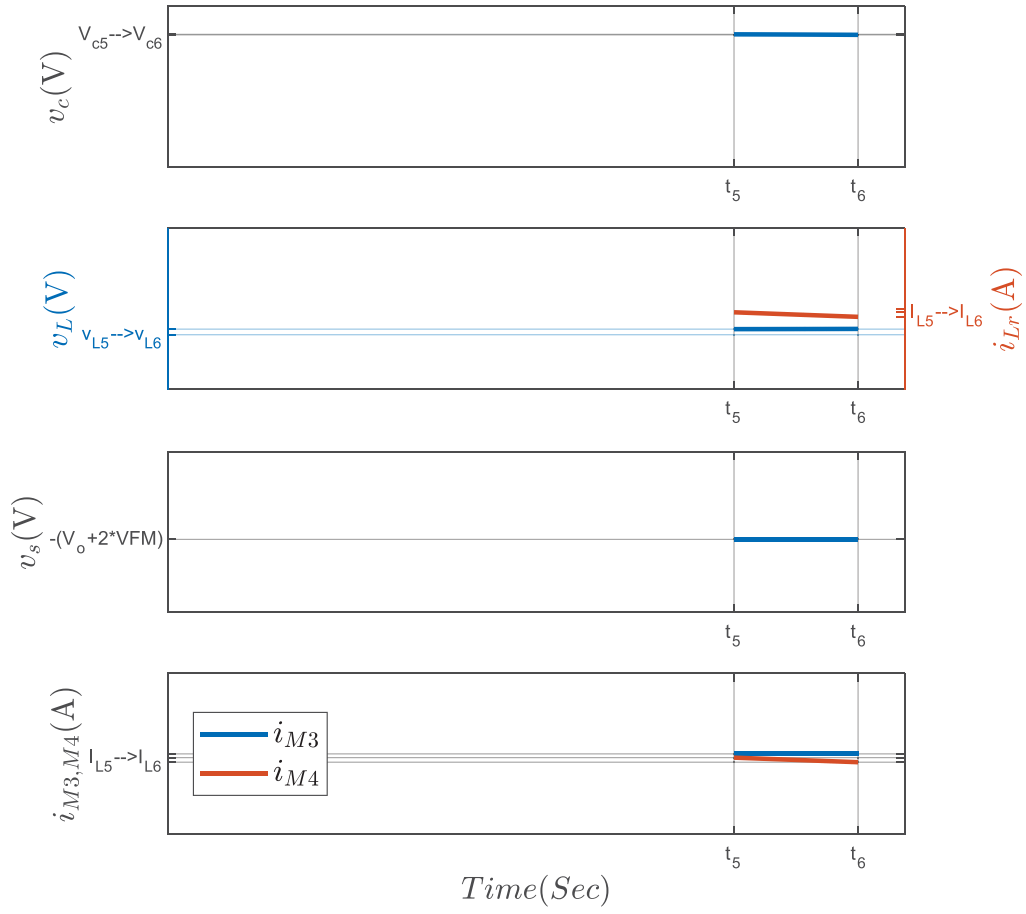


Figure 3.17: Key waveforms of mode 6.

$-V_o$. These equations are presented in Eq. 3.22 and Eq. 3.23. Note that during mode 7 the resonant tank remains similar to mode 6.

$$i_{L_r}(t) = 2 \cdot C \cdot \frac{dv_c}{dt} \quad (3.22)$$

$$\frac{d^2 v_c}{dt^2} + \frac{1}{2 \cdot C \cdot L_r} v_c = \frac{V_0}{2 \cdot C \cdot L_r} \quad (3.23)$$

The governing equations for mode 7 are shown in Eq. 3.24; where, V_{c6} and I_{L6} are the $v_c(t)$ and $i_{L_r}(t)$ at $t = t_6$.

$$\begin{cases} v_s(t) = -V_o \\ i_{M_3}(t) = 0 \\ i_{M_4}(t) = i_{L_r}(t) \\ v_c(t) = -(V_o - V_{c6}) \cdot \cos(\omega_{res1} \cdot (t - t_6)) + \frac{I_{L6}}{2 \cdot C \cdot \omega_{res1}} \cdot \sin(\omega_{res1} \cdot (t - t_6)) + V_o \\ v_L(t) = (V_o - V_{c6}) \cdot \cos(\omega_{res1} \cdot (t - t_6)) - \frac{I_{L6}}{2 \cdot C \cdot \omega_{res1}} \cdot \sin(\omega_{res1} \cdot (t - t_6)) \\ i_{L_r}(t) = (2 \cdot C \cdot \omega_{res1}) \cdot (V_o - V_{c6}) \cdot \sin(\omega_{res1} \cdot (t - t_6)) + I_{L6} \cdot \cos(\omega_{res1} \cdot (t - t_6)) \end{cases} \quad (3.24)$$

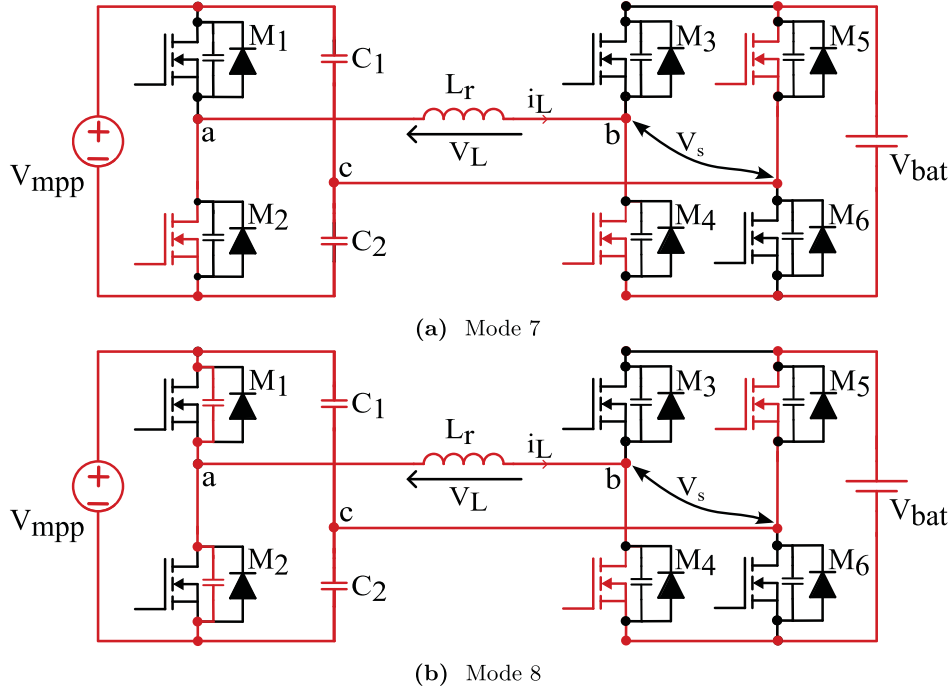


Figure 3.17: Operation modes for the proposed topology: mode 7 & 8.

The key waveform for mode 7 are presented in in Fig. 3.18. It could be seen that during this mode the voltage v_s is clamped to $-V_O$; while, M_4 and M_5 are conducting the inductor current.

Mode 8, $t_7 \leq t < t_8$: At the beginning of mode 8, M_2 turns off and its output capacitance begins to charge while the output capacitance of the M_1 is discharging. The circuit operation of this mode is depicted in Fig. 3.17b. During this mode the circuit is in a resonant state with the same resonant frequency (ω_{res1}) as mode 2. The differential equations for this modes are derived and presented in Eq. 3.25 and Eq. 3.26. In order to solve Eq. 3.26 for $v_a(t)$, the initial value of 0 for the voltage of node 'a' and $-V_o$ for v_s are considered.

$$i_{L_r}(t) = -2 \cdot C_s \cdot \frac{dv_a}{dt} \quad (3.25)$$

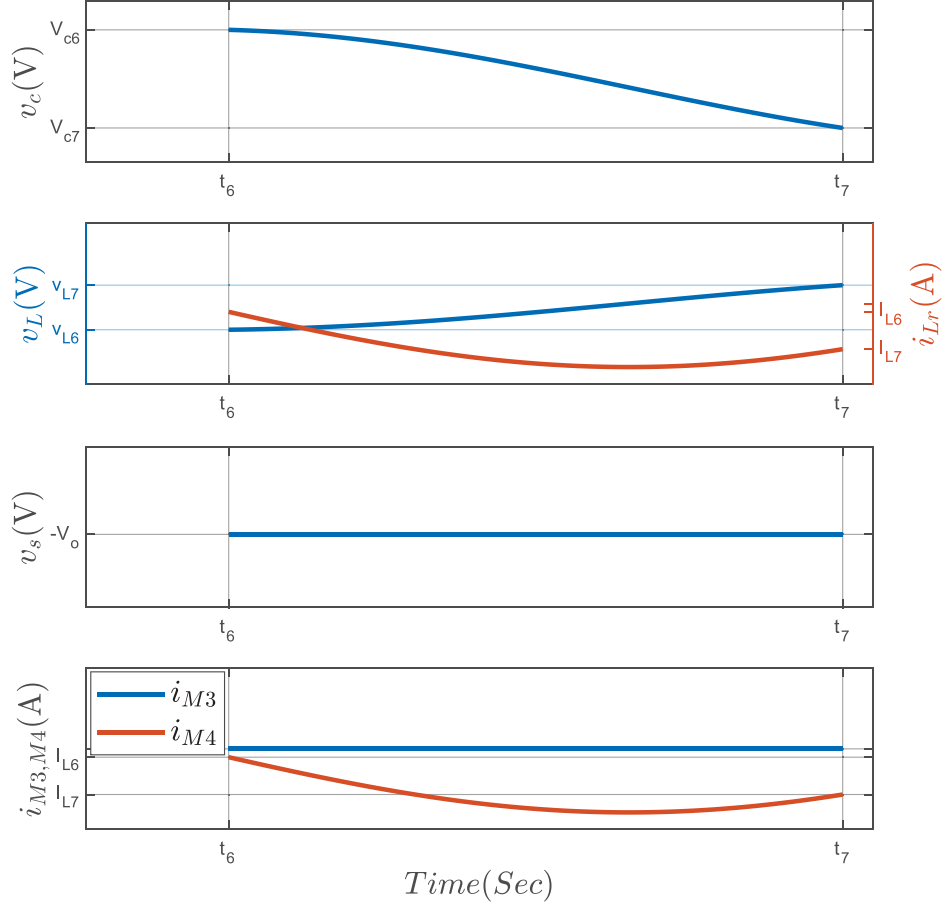


Figure 3.18: Key waveforms for the time interval of mode 7.

$$\frac{d^2 v_a}{dt^2} + \frac{1}{2 \cdot C_s \cdot L_r} v_a = \frac{-V_0 + V_{c7}}{2 \cdot C_s \cdot L_r} \quad (3.26)$$

The governing equations for mode 8 are shown in Eq. 3.27; where, V_{c7} and I_{L7} are the $v_c(t)$ and $i_{L_r}(t)$ at $t = t_7$. Since the time duration for this mode is very short, the change in the voltage at node c is negligible and this voltage could be considered constant at V_{c7} . Considering the fact that at the end of this mode $V_a(t_8) = V_{in} + V_{FM}$, the time duration for which this mode lasts is extracted as shown in Eq. 3.28.

$$\begin{cases} v_s(t) = -V_o \\ i_{M_3}(t) = 0 \\ i_{M_4}(t) = i_{L_r}(t) \\ v_c(t) = V_{c7} \\ v_L(t) = -(-V_o + V_{c7}) \cdot \cos(\omega_{res2} \cdot (t - t_7)) - \frac{I_{L7}}{2 \cdot C_s \cdot \omega_{res2}} \cdot \sin(\omega_{res2} \cdot (t - t_7)) \\ i_{L_r}(t) = -(2 \cdot C_s \cdot \omega_{res2}) \cdot (-V_o + V_{c7}) \cdot \sin(\omega_{res2} \cdot (t - t_7)) + \dots \\ \dots I_{L7} \cdot \cos(\omega_{res2} \cdot (t - t_7)) \end{cases} \quad (3.27)$$

$$\Delta t_8 = (t_8 - t_7) = \frac{1}{\omega_{res2}} \sin^{-1} \left(\frac{(2 \cdot C_s \cdot \omega_{res2}) \cdot (V_{in} + 2V_{FM})}{-I_{L7}} \right) \quad (3.28)$$

Fig. 3.19 depicts the key signals within time interval of mode 8. The time interval of this mode is also short comparing to the switching cycle time period; hence, the limits of the x-axis in this figure are adjusted for better clarity of the waveforms. It could be seen that the change in the voltage at node 'c' remains trivial. On the other side, the voltage at the switching node 'a' transitions from 0 to $V_{in} + V_{FM}$, resulting in a steep transition in the voltage of V_L .

Mode 9, $t_8 \leq t < t_9$: Mode 9 begins when C_{oss1} is fully discharged, and C_{oss2} is charged. The current $i_{L_r}(t)$ is still negative resulting in turning ON the body diode of M1, and clamping $v_a(t)$ at $V_{in} + V_{FM}$. During this mode the circuit enters into a resonant mode dominated by $C_1 || C_2 = 2 \cdot C$ and L_r with the resonant frequency at ω_{res2} . Fig. 3.19a depicts the circuit state in this mode. Applying a KCL at node 'c', and a KVL in the loop consists of node 'a', node 'b', and node 'c', the differential equations Eq. 3.29 and Eq. 3.30 are derived.

$$i_{L_r}(t) = 2 \cdot C \cdot \frac{dv_c}{dt} \quad (3.29)$$

$$\frac{d^2 v_c}{dt^2} + \frac{1}{2 \cdot C \cdot L_r} v_c = \frac{V_{in} + V_{FM} + V_o}{2 \cdot C \cdot L_r} \quad (3.30)$$

The second order differential equation of Eq. 3.30 could be solved for $v_c(t)$ with the initial condition calculated from $v_c(t)$ and $i_{L_r}(t)$ of Eq. 3.28 at $t = t_8$. Eq. 3.31 present the mathematical representation of the key voltage and current signals; where, V_{c8} and I_{L8} are the $v_c(t)$ and $i_{L_r}(t)$ at $t = t_8$. Mode 9 last until V_{gs1} goes high at $t = T_{sw} + (t_d/2)$ ($t = t_d/2$).

$$\begin{cases} v_s(t) = -V_o \\ i_{M_3}(t) = 0 \\ i_{M_4}(t) = i_{L_r}(t) \\ v_c(t) = -(V_{in} + V_{FM} + V_o - V_{c8}) \cdot \cos(\omega_{res1} \cdot (t - t_8)) + \dots \\ \dots \frac{I_{L8}}{2 \cdot C_s \cdot \omega_{res1}} \cdot \sin(\omega_{res1} \cdot (t - t_8)) + (V_{in} + V_{FM} + V_o) \\ v_L(t) = (V_{in} + V_{FM} + V_o - V_{c8}) \cdot \cos(\omega_{res1} \cdot (t - t_8)) - \dots \\ \dots \frac{I_{L8}}{2 \cdot C_s \cdot \omega_{res1}} \cdot \sin(\omega_{res1} \cdot (t - t_8)) \\ i_{L_r}(t) = (2 \cdot C \cdot \omega_{res1}) \cdot (V_{in} + V_{FM} + V_o - V_{c8}) \cdot \sin(\omega_{res1} \cdot (t - t_8)) + \dots \\ \dots I_{L8} \cdot \cos(\omega_{res1} \cdot (t - t_8)) \end{cases} \quad (3.31)$$

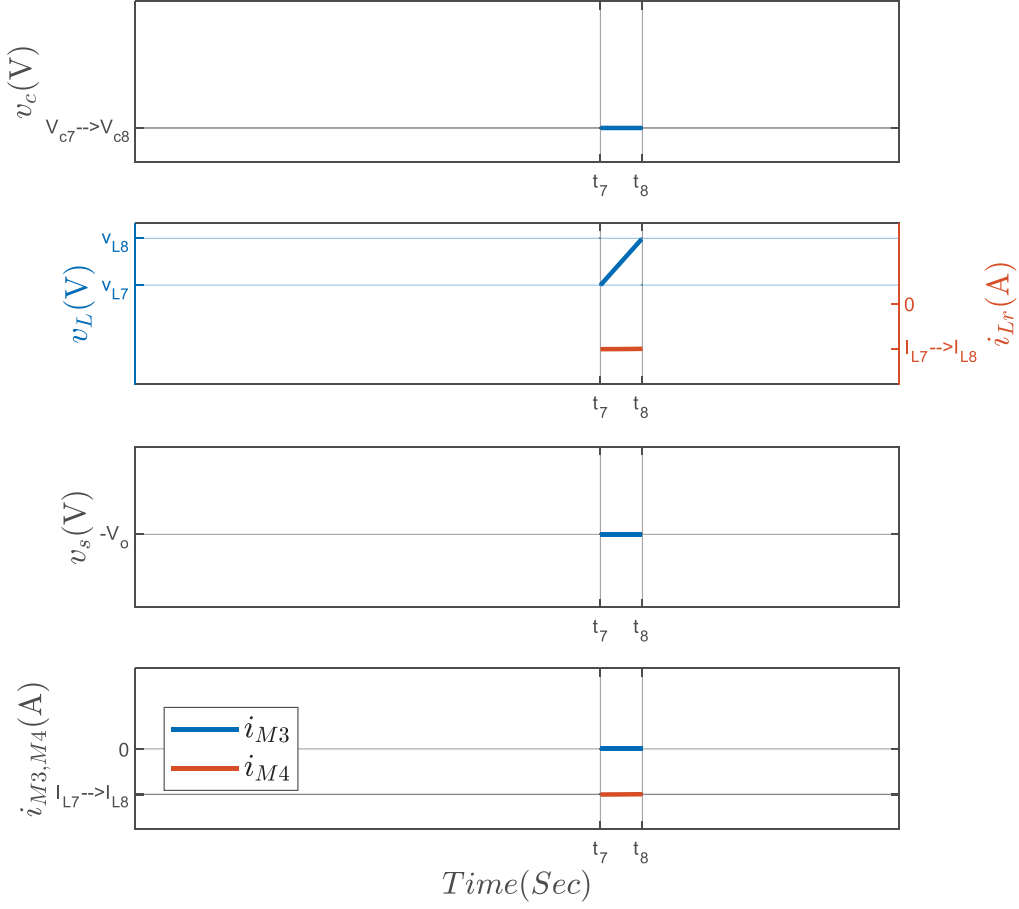


Figure 3.19: Key waveforms during mode 8.

Fig. 3.20 presents the key waveforms during the time interval of mode 9. This mode begins at t_8 and extends beyond the switching cycle T_{sw} until the gate voltage at M_1 goes high at $t = T_{sw} + t_{dt}/2$; hence, this mode is depicted as two separate intervals between 0 to $t_{dt}/2$, and t_8 to $t = T_{sw}$. Similar to mode 3, the change in the voltage at node 'c' is trivial along with small change in the voltage at node 'b'. Since the inductor voltage is almost constant, its current is increasing linearly.

Mode 10, $t_9 \leq t < t_{10}$: This mode begins when V_{gs1} goes high, and M_1 turns ON. At the beginning of this mode the current is still negative and M_4 & M_5 remain ON. The circuit state in this operation mode is shown in Fig. 3.19b. Similar to mode 9, in this mode also there is a resonant between resonant capacitors ($C_1 || C_2 = 2 \cdot C$) and the inductor (L_r) with the resonant frequency at ω_{r1} . The differential equations of mode 10 are presented in Eq. 3.32 and Eq. 3.33.

$$i_{L_r}(t) = 2 \cdot C \cdot \frac{dv_c}{dt} \quad (3.32)$$

$$\frac{d^2 v_c}{dt^2} + \frac{1}{2 \cdot C \cdot L_r} v_c = \frac{V_{in} + V_o}{2 \cdot C \cdot L_r} \quad (3.33)$$

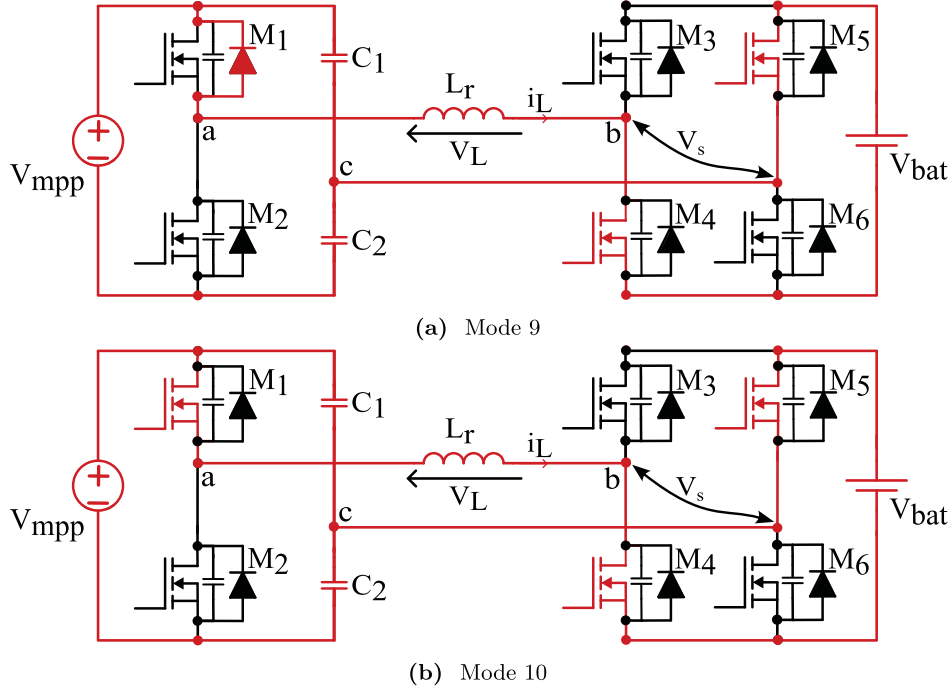


Figure 3.19: Operation modes for the proposed topology: mode 9 & 10.

By solving Eq. 3.33 for $v_c(t)$, the mathematical equations representing mode 10 could be extracted as presented in 3.34. Note that V_{c9} and I_{L9} are considered the initial condition for mode 10. This mode lasts until $i_{L_r}(t)$ reaches zero, the time period can be calculated by equating inductor current of Eq. 3.34 to zero, with $\cos(\omega_{r1} \cdot (t_{11} - t_{10})) \approx 1$, presented in Eq. 3.35.

$$\left\{ \begin{array}{l} v_s(t) = -V_o \\ i_{M3}(t) = 0 \\ i_{M4}(t) = i_{L_r}(t) \\ v_c(t) = -(V_{in} + V_o - V_{c9}) \cdot \cos(\omega_{res1} \cdot (t - t_9)) + \dots \\ \dots \frac{I_{L9}}{2 \cdot C \cdot \omega_{res1}} \cdot \sin(\omega_{res1} \cdot (t - t_9)) + (V_{in} + V_o) \\ v_L(t) = (V_{in} + V_o - V_{c9}) \cdot \cos(\omega_{res1} \cdot (t - t_9)) - \frac{I_{L9}}{2 \cdot C \cdot \omega_{res1}} \cdot \sin(\omega_{res1} \cdot (t - t_9)) \\ i_{L_r}(t) = (2 \cdot C \cdot \omega_{res1}) \cdot (V_{in} + V_o - V_{c9}) \cdot \sin(\omega_{res1} \cdot (t - t_9)) + \dots \\ \dots I_{L9} \cdot \cos(\omega_{res1} \cdot (t - t_9)) \end{array} \right. \quad (3.34)$$

$$\Delta t_{10} = (t_{10} - t_9) = \frac{1}{\omega_{res1}} \sin^{-1} \left(\frac{-I_{L9}}{(2 \cdot C \cdot \omega_{res1}) \cdot (V_{in} + V_o - V_{c9})} \right) \quad (3.35)$$

Fig. 3.21 shows the key waveforms for mode 10; where, the x-axis limits are changed for better clarity. During this mode v_c decreases slightly ($V_{c9} - > V_{c10}$); while, the change in the

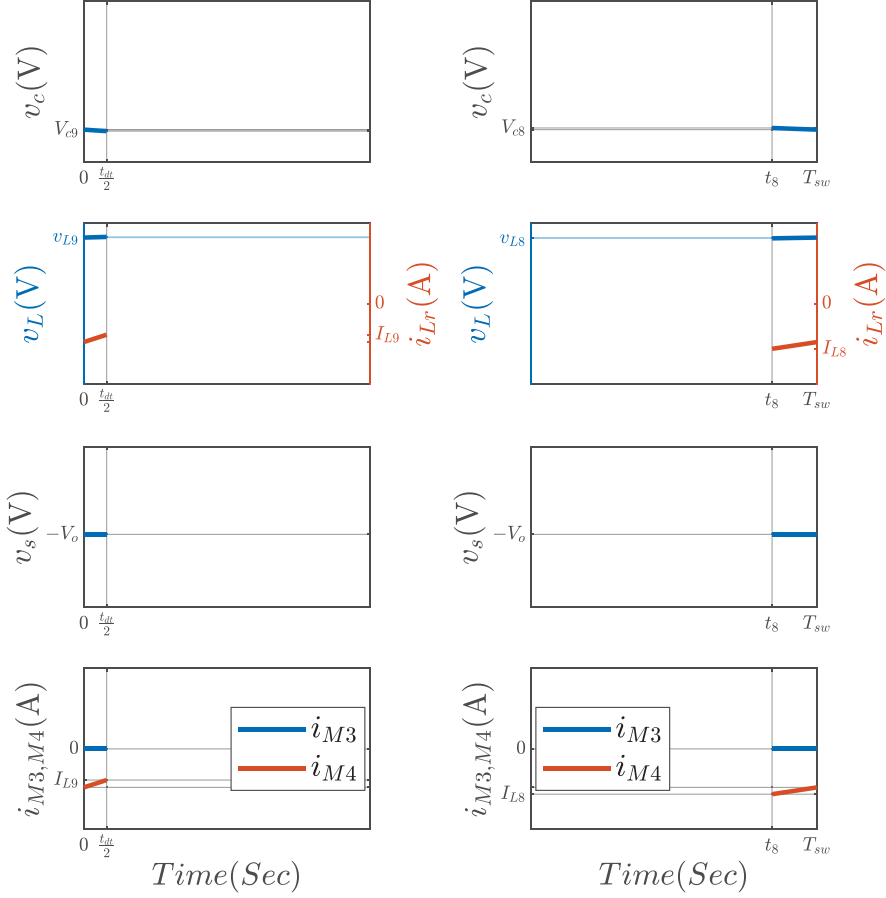


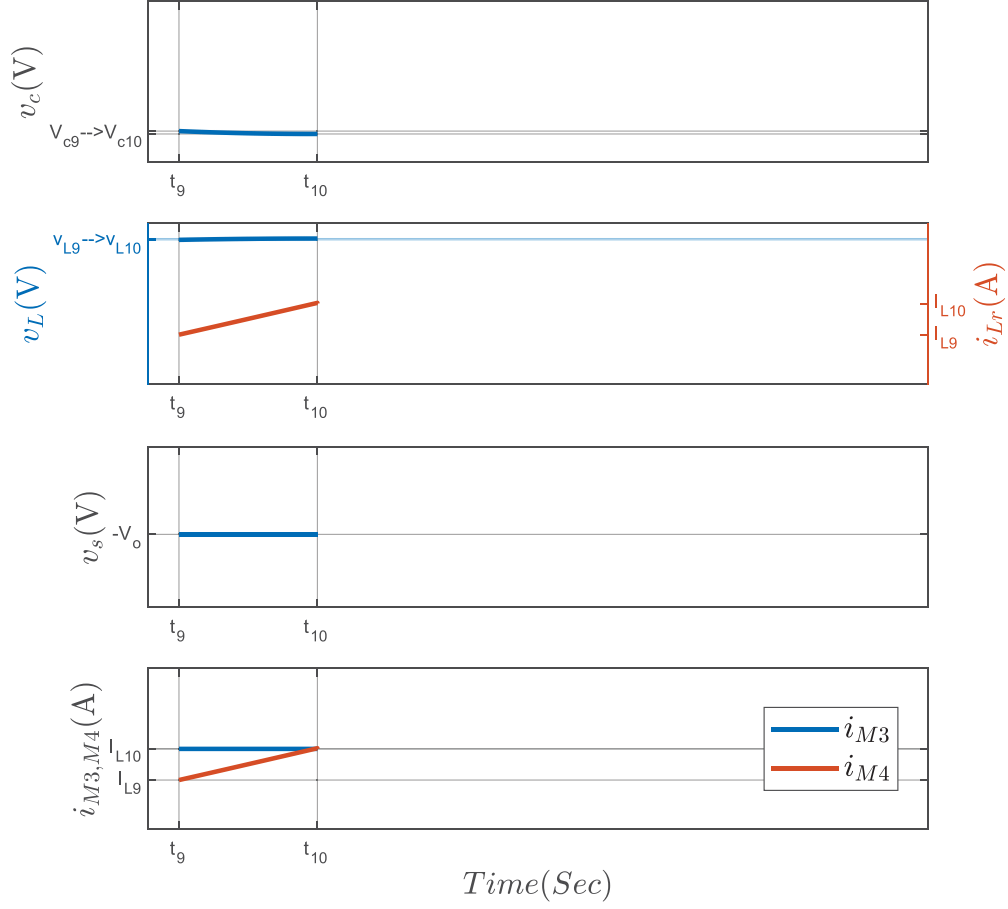
Figure 3.20: Key waveforms for mode 9 within $0 \leq t < t_{dt}/2$ and $t_8 \leq t \leq T_{sw}$.

voltage across the inductor is also small $V_{L9} \rightarrow V_{L10}$. Moreover, the voltage at the input of the SR-stage (v_s) is clamped at $-V_o$ as M_4 and M_5 are still ON.

Mode 11, $t_{10} \leq t < t_{11}$: At the beginning of this mode, the inductor current reaches zero; hence, to maintain the ZCS the gate drive pulses for M_4 & M_5 go low and the gate drive pulse for the M_3 & M_6 are already low. The output capacitances of these two MOSFETs begin to charge; while, the ones of M_3 & M_6 discharge. Fig. 3.21a depicts the circuit state for this mode. Similar to mode 5, the equivalent output capacitance of the SR stage MOSFETs (C_{sSR}) creates a resonant tank with L_r with the resonant frequency of $\omega_{r3} = \frac{1}{\sqrt{(C_{sSR}) \cdot L_r}}$. Applying KCL at node 'b', and KVL in the loop consist of the a,b, and c nodes the differential equations for mode 11 could be depicted in Eq. 3.36 and Eq. 3.37. Note that during this mode, the voltage at node 'a' is clamped at V_{in} .

$$i_{L_r}(t) = C_{sSR} \cdot \frac{dv_b}{dt} \quad (3.36)$$

$$\frac{d^2 v_b}{dt^2} + \frac{1}{C_{sSR} \cdot L_r} v_b = \frac{V_{in}}{C_{sSR} \cdot L_r} \quad (3.37)$$


Figure 3.21: Key waveforms for mode 10.

Solving Eq. 3.37 for $v_b(t)$ leads to the Eq. 3.38 for presenting Mode 11. The time period that this mode lasts is very short and $v_c(t)$ remains constant at V_{c10} . At the end of this mode, since the inductor current is positive, the body diode of M_3 & M_6 turn ON, and $v_s(t)$ will be clamped at $V_o + 2 \cdot V_{FM}$. The time duration of this mode could be calculated using Eq. 3.39, with V_{c10} and I_{L10} representing the initial condition.

$$\begin{cases} v_s(t) = -(V_{in} + V_o - V_{c10}) \cdot \cos(\omega_{res3} \cdot (t - t_{10})) + (V_{in} - V_{c10}) \\ i_{M3}(t) = 0 \\ i_{M4}(t) = 0 \\ v_c(t) = V_{c10} \\ v_L(t) = (V_{in} + V_o - V_{c10}) \cdot \cos(\omega_{res3} \cdot (t - t_{10})) \\ i_{Lr}(t) = (C_{sSR} \cdot \omega_{res3}) \cdot (V_{in} + V_o - V_{c10}) \cdot \sin(\omega_{res1} \cdot (t - t_9)) \end{cases} \quad (3.38)$$

$$\Delta t_{11} = (t_{11} - t_{10}) = \frac{1}{w_{res3}} \cos^{-1} \left(\frac{V_{in} - 2 \cdot V_{FM} - V_o - V_{c10}}{V_{in} + V_o - V_{c10}} \right) \quad (3.39)$$

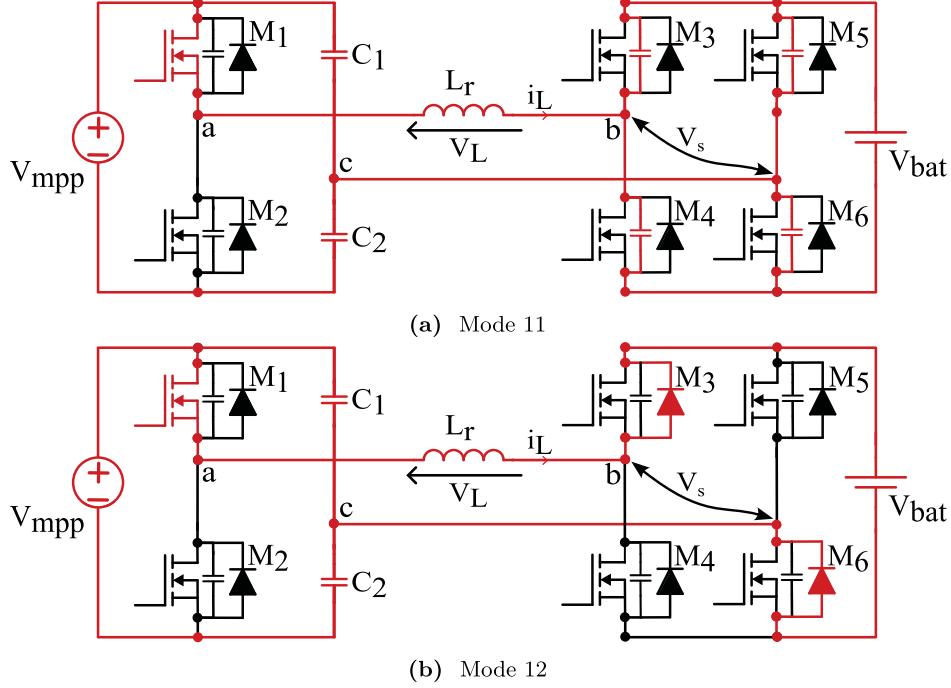


Figure 3.21: Operation modes for the proposed topology: mode 11 & 12.

Fig. 3.22 shows the signal waveforms during the time interval of mode 11. In this figure also the x-axis limits are adjusted to magnify this time interval. The behavior of the signals are similar to mode 5. This is because of the symmetry between the positive and negative half switching cycles. The fast transition of the voltage across the inductor (v_L) is the result of transition in the voltage at node 'b'. This in-turn is the result of M_4 & M_5 turning OFF; while, the body diode of M_3 & M_6 turn ON. At the end of this mode, the inductor current transfers to the body diode of M_3 & M_6 .

Mode 12, $t_{11} \leq t < t_{12}$: As mentioned, at the end of mode 11 the inductor current is positive, and since the charging/discharging cycle of the SR MOSFETs output capacitances is also ended, the body diode of M_3 & M_6 begin to conduct. Similar to mode 6 the resonant tank consists of $C_1 || C_2 = 2 \cdot C$ and L_r with the frequency of ω_{r1} . This mode last until the dead time between the gate-to-source drive signals of the MOSFETs belonging to the same leg in the SR stage is over and V_{gs3} & V_{gs6} change their state to high. At the end of this mode the channel of M_3 & M_6 turn ON, which marks the beginning of mode 1. The circuit operation of this mode is depicted in Fig. 3.21b. The differential equations of this mode could be extracted as presented in Eq. 3.40 and Eq. 3.41. Note that, during this mode the voltages v_a and v_s are clamped at V_{in} and $V_o + 2 \cdot V_{FM}$, respectively.

$$i_{L_r}(t) = 2 \cdot C \cdot \frac{dv_c}{dt} \quad (3.40)$$

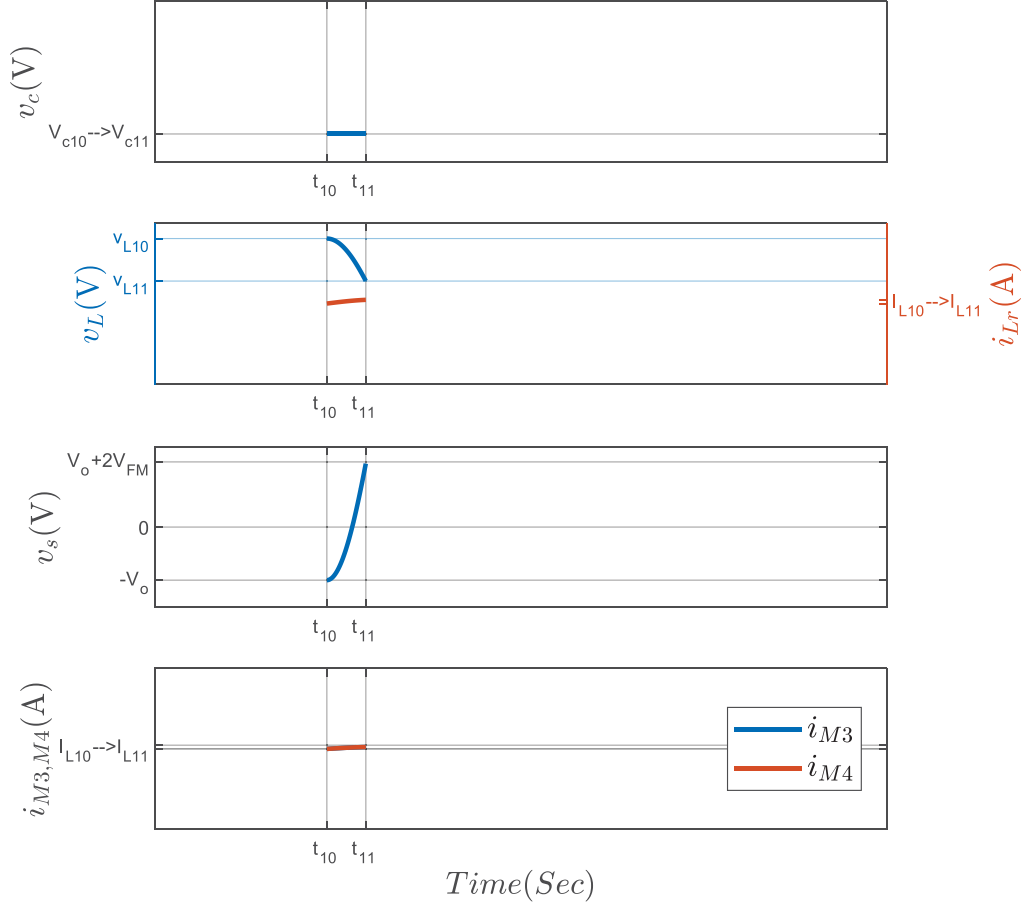


Figure 3.22: Key waveforms with indicated mode 11 time range.

$$\frac{d^2 v_c}{dt^2} + \frac{1}{2 \cdot C \cdot L_r} v_c = \frac{V_{in} - (V_0 + 2 \cdot V_{FM})}{2 \cdot C \cdot L_r} \quad (3.41)$$

By solving the second order differential equation of Eq. 3.41 for $v_c(t)$, the associated mathematical equations of mode 12 for the key signals could be extracted as Eq. 3.42. The initial values for $v_c(t)$ and $i_{L_r}(t)$ at $t = t_{11}$ are indicated as V_{c11} and I_{L11} , and the final values (at $t = t_{12}$) will be the initial condition for mode 1 (i.e., $V_{c0} = V_{c12}$ and $I_{L0} = I_{L12}$).

$$\begin{cases} v_s(t) = V_o + 2 \cdot V_{FM} \\ i_{M_3}(t) = i_{Lr}(t) \\ i_{M_4}(t) = 0 \\ v_c(t) = -(V_{in} - (V_o + 2 \cdot V_{FM} + V_{c11})) \cdot \cos(\omega_{res1} \cdot (t - t_{11})) + \dots \\ \quad \dots \frac{I_{L11}}{2 \cdot C \cdot \omega_{res1}} \cdot \sin(\omega_{res1} \cdot (t - t_{11})) + (V_{in} - (V_o + 2 \cdot V_{FM})) \\ v_L(t) = (V_{in} - (V_o + 2 \cdot V_{FM} + V_{c11})) \cdot \cos(\omega_{res1} \cdot (t - t_{11})) - \dots \\ \quad \dots \frac{I_{L11}}{2 \cdot C \cdot \omega_{res1}} \cdot \sin(\omega_{res1} \cdot (t - t_{11})) \\ i_{Lr}(t) = (2 \cdot C \cdot \omega_{res1}) \cdot (V_{in} - (V_o + 2 \cdot V_{FM} + V_{c11})) \cdot \sin(\omega_{res1} \cdot (t - t_{11})) + \dots \\ \quad \dots I_{L11} \cdot \cos(\omega_{res1} \cdot (t - t_{11})) \end{cases} \quad (3.42)$$

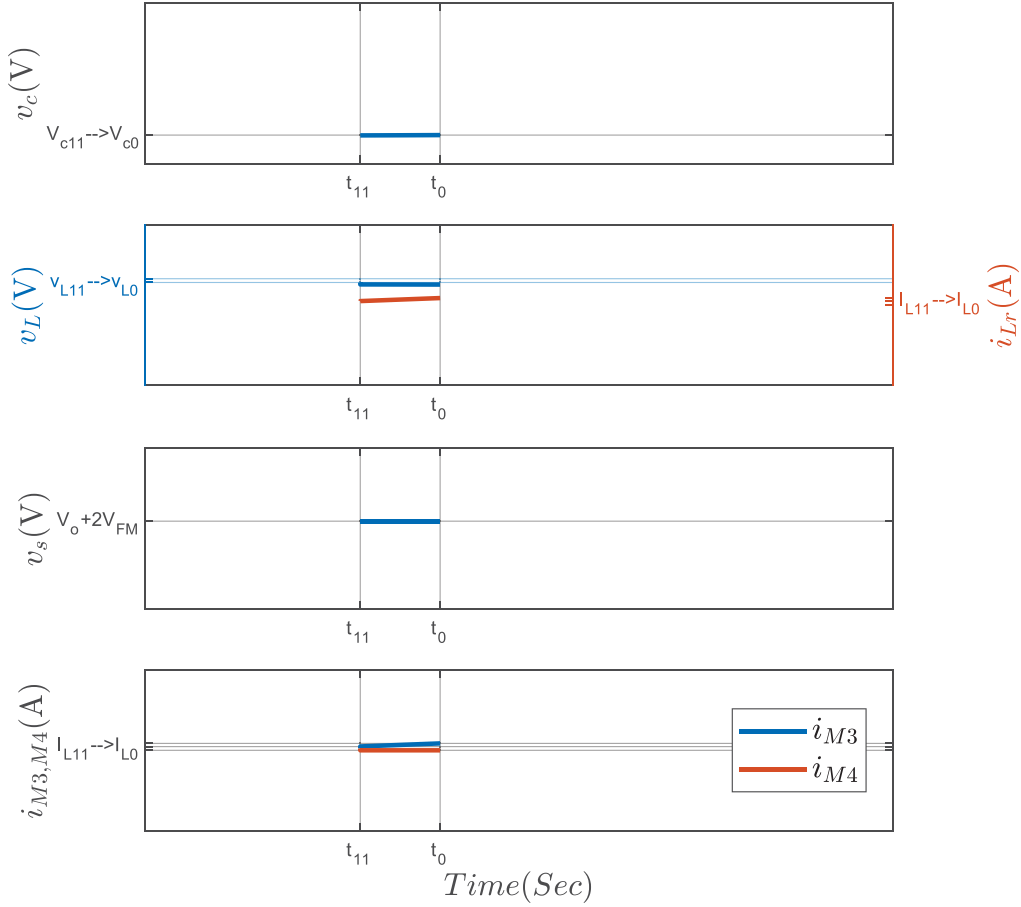


Figure 3.23: Key waveforms for mode 12.

Fig. 3.23 depicts the key waveforms for mode 12. During this mode the body diode of M_3 &

M_6 remain ON; therefore, the voltage v_s is clamped at $V_o + 2V_{FM}$. The time interval for this mode is a small fraction of the switching cycle; hence, the x-axis limits for the plots are adjusted for better clarity. At the end of this mode ($t = t_{12}$) the channels of M_3 and M_6 turn ON; which is the beginning of mode 1 $t = t_{12} = t_0$. Finally, the key signals for all modes (mode 1 to mode 12) that consist of one switching cycle (T_{sw}) are depicted in Fig. 3.24.

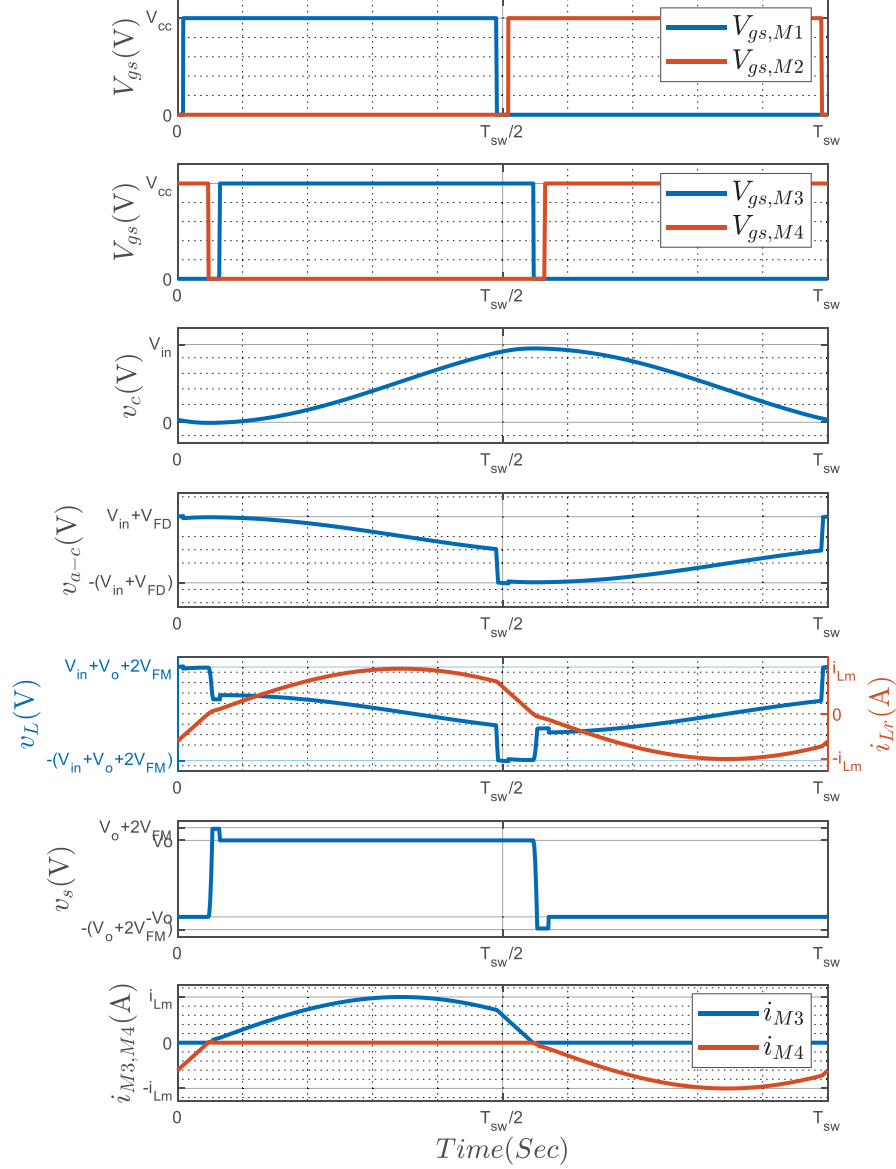


Figure 3.24: Key waveforms for one switching cycle consisting of mode 1 to mode 12.

3.4 Control Strategy and Power Flow

As mentioned earlier, the control strategy for the proposed topology is based on the frequency and phase shift modulations to not only control the voltage gain but also the transferred power. The required voltage gain is dictated by the battery SOC or , in other words, the battery voltage. The targeted transferred power depends on the battery charging profile (i.e., constant voltage (CV) and constant current (CC)). Different control strategies could be utilized for the proposed resonant battery charger. Since the input to the battery charger is a PV module, the control strategy should naturally involve MPPT to extract the maximum available power from the PV panel. On the other side, the load connected to the proposed topology is a battery; hence, the battery limits including the maximum charging current/power and the cut-off voltage should be also taken into consideration. To meet both requirements a combined MPPT and constant voltage (CV) controller could be utilized to track the PV panel MPP as long as the battery voltage is below a set limit, then, once the voltage reaches a pre-set limit (e.g. $V_{bat,max}$) the control loop changes to the CV control until the end of charging process. The CV controller could include a ramp rate through which the battery is gradually charged from the CV control pre-set limit to the battery charging cut-off voltage (e.g. $V_{bat,cut-off}$).

Fig. 3.25 present the overall control structure for the proposed topology. As it could be seen, the feedback signals are the current and voltage of both PV panel (I_{PV} , V_{PV}) and battery (I_{bat} , V_{bat}), along with the inductor current for the zero-crossing detection and preventing the short circuit across the battery. The FM and PSM are used for MPPT and battery charge controller. The duty cycle is constant at 50% ($D = 0.5$). The phase shifts φ_1 and φ_2 are utilized for power flow control.

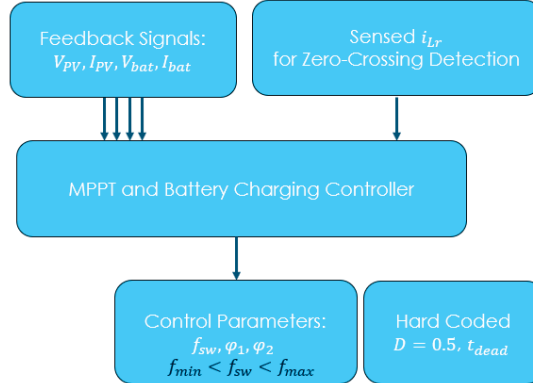


Figure 3.25: Control structure.

Fig. 3.26 depicts the closed-loop control diagram for the proposed topology. As it could be seen the sensed signals, including V_{PV} , I_{PV} , V_{bat} , and I_{bat} , are provided to the controller. The controller include both MPPT and the battery charge controller (i.e. CV control), and the output of the controller is provided to a frequency modulation block where the pulse signals for the MOSFETs are generated.

The next following sub sections aim to describe:

- Different MPPT algorithms that could be modified to fit the frequency modulation scheme for the proposed topology

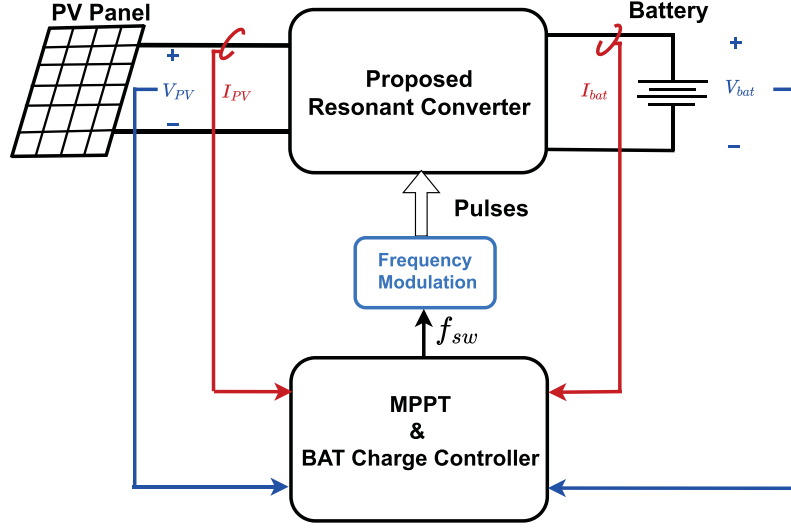


Figure 3.26: Closed-loop control diagram for the proposed topology.

- Equivalent AC circuit of the proposed topology to explore its voltage gain modeling and impedance characteristics
- Power flow modeling and its relationship with the circuit parameters and control variables

3.4.1 MPPT Control Algorithms

Considering the nature of the proposed topology any MPPT control strategy should involve frequency modulation. Various MPPT control algorithms have been proposed in literature; however, mostly involve pulse-width modulation (PWM) switching schemes [27, 28, 29, 30, 31]. It should be noted that the required MPPT algorithm for the proposed topology should be modified to provide frequency modulation making it suitable for the intended control goal of the resonant DC-DC battery charger.

A simple MPPT algorithm is referred to as hill climbing (HC) approach [27]. Fig. 3.27 presents the HC MPPT algorithm flowchart; where, it is modified to be suitable for the frequency modulation of the proposed topology. Based on the operation point of the PV, if the PV power has not reached the MPP the switching frequency is either reduced or increased depending on which side of the PV power curve the operation point is. Since the goal is to change the switching frequency in such a way that PV operation power moves upward towards the maximum point it is referred to as HC algorithm. The HC approach is simple; however, there is a trade-off between the stability of this control algorithm and the fast response. In utilizing this approach for the proposed topology, the steps of the switching frequency in the HC algorithm should be small enough to prevent oscillations in the harvested PV power around the MPP. On the other side, under rapidly changing solar irradiance, the step change in the switching frequency should be high for a fast MPPT tracking.

A widely used MPPT algorithm is referred to as perturb-and-observe (P&O) approach [28]. Fig. 3.28 presents the P&O MPPT algorithm flowchart. This approach is also simple ; however,

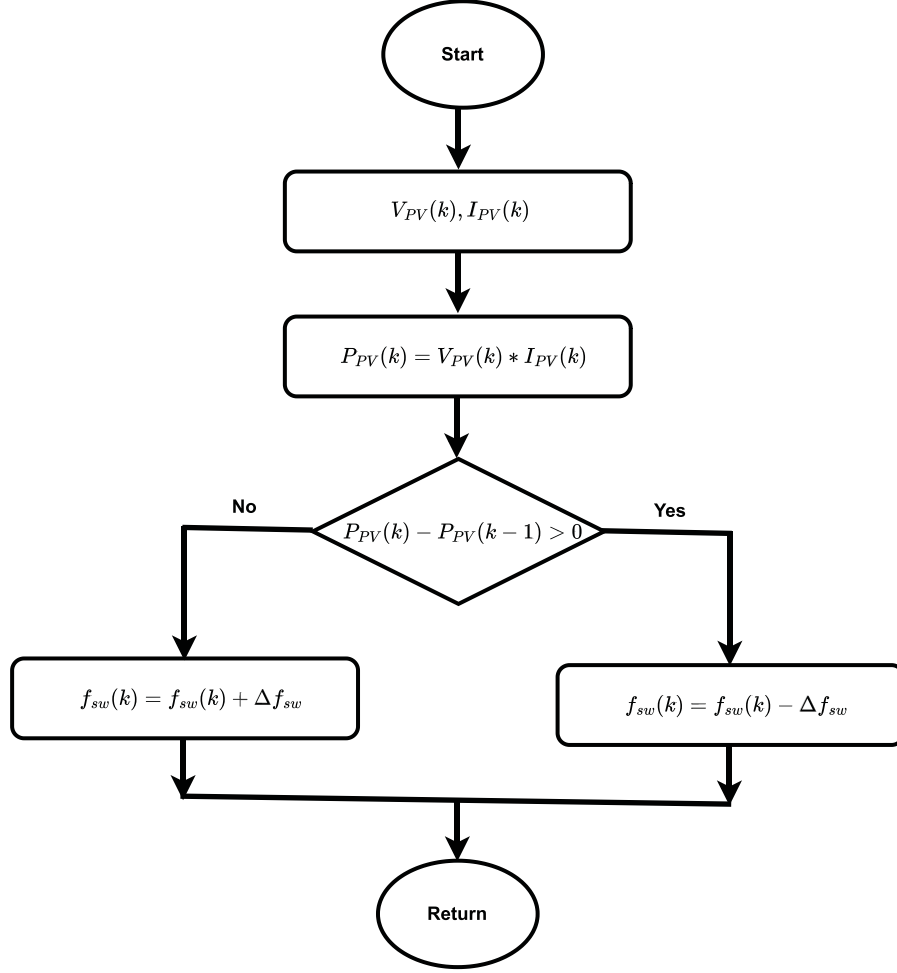


Figure 3.27: Flowchart for the HC MPPT control algorithm modified to frequency modulation.

PV voltage is perturbed every MPPT cycle. This means, when the MPP reaches the output power, it oscillates around the maximum, resulting in power loss in the PV system.

Another MPPT algorithm that is explored in literature is the incremental conductance (INC) approach [29, 30]. Fig. 3.29 presents the INC MPPT algorithm flowchart. The INC method is more complex relative to the HC and P&O algorithms; however, it provides high tracking accuracy at steady state and good adaptability to the rapidly changing solar irradiance conditions.

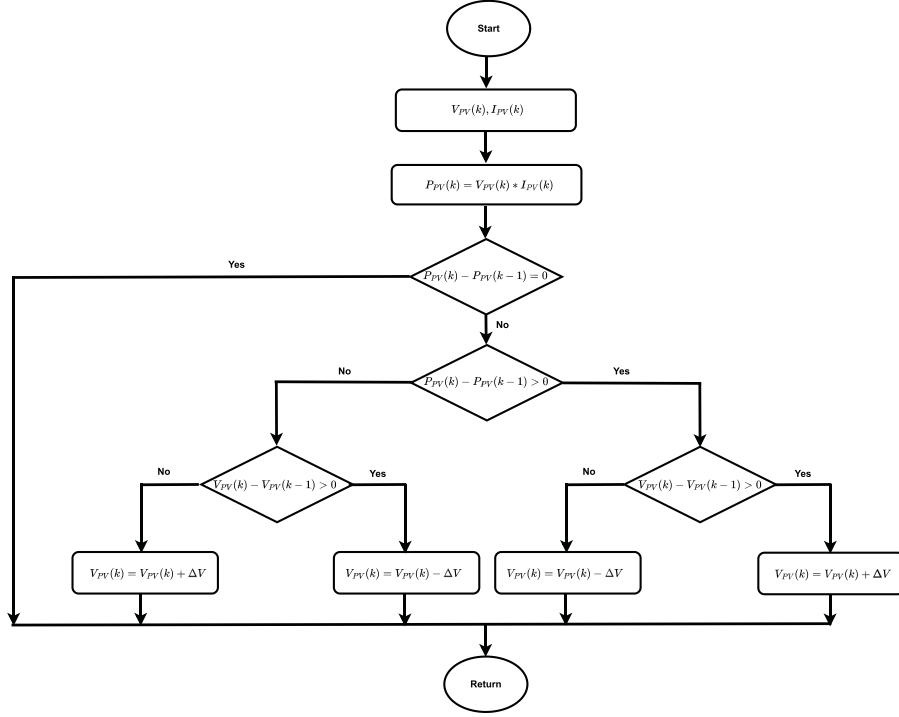


Figure 3.28: Flowchart for the P&O MPPT control algorithm.

3.4.2 Impedance and Voltage Gain Analysis

The dividing capacitor C_1 and C_2 , presented in the proposed topology of Fig. 3.10, not only contribute to the transferred power to the battery, but also, create a resonant circuit with the inductor L_r . A first harmonic approximation (FHA) equivalent circuit of the proposed topology at the high frequencies could be depicted as Fig. 3.30. In this figure, v_{in} is the FHA AC component of the inverting stage voltage, i_{in} and Z_{in} are the input current and impedance, v_o is the FHA AC voltage at the input of the SR stage, and R_{ac} is a resistive load equivalent to the battery charging power reflected to the input side of the SR stage. Note, the two dividing capacitors in the proposed topology from AC point of view are in parallel resulting in $C_r = 2 \cdot C$.

The respective values of the resonant frequency $f_{res} = 1/(2\pi\sqrt{(2 \cdot C) \cdot L_r})$ and switching frequency f_{sw} plays an important role in both battery charging voltage and power. Fig. 3.31 presents the FHA input impedance seen from the output of the half-bridge inverter at different battery charging power (P_o) levels. In this figure the x-axis is the normalized frequency as f_{sw}/f_{res} . As it could be seen from this figure, for the switching frequencies more than the resonant frequency the input impedance is inductive, at the resonant frequency this impedance is resistive, otherwise, it will be capacitive. To maintain the ZVS at the inverting HB the switching frequency should be selected in a region where the input impedance exhibits an inductive characteristics (i.e., $f_{sw} > f_{res}$).

The voltage gain $A_v = v_o/v_{in}$ itself is a function of the switching frequency, where v_{in} and v_o are the FHA ac input and output voltages, respectively, at the output of the inverting stage

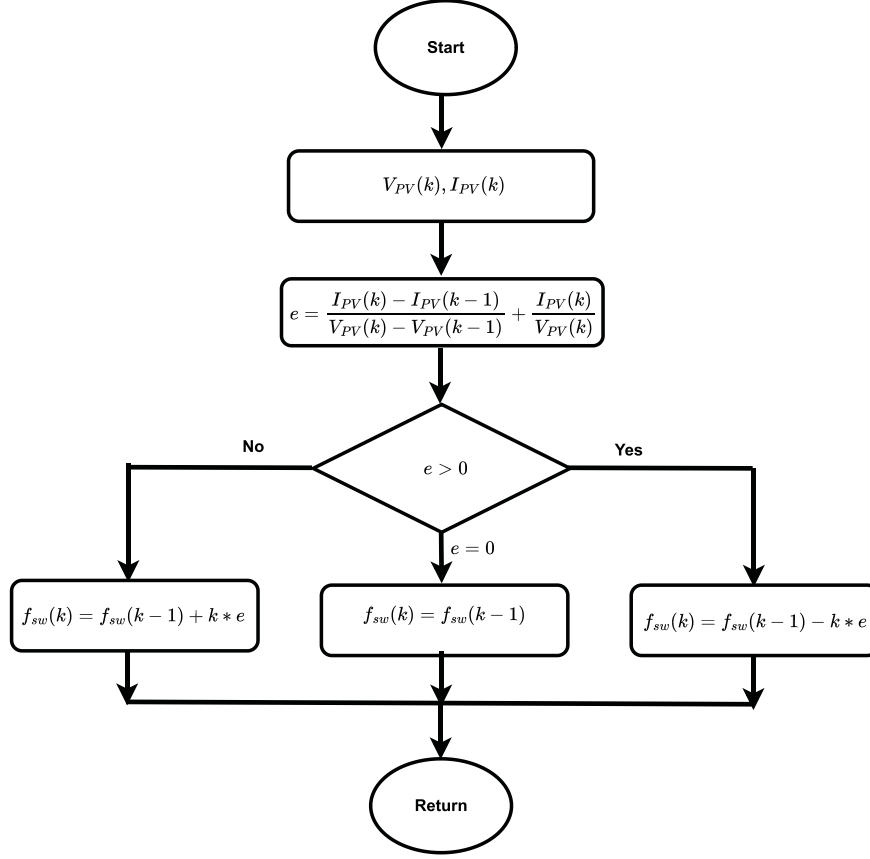


Figure 3.29: Flowchart for the INC MPPT control algorithm.

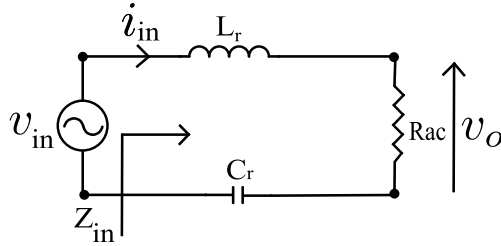


Figure 3.30: FHA equivalent circuit diagram for the proposed topology.

and input of the SR stage. The output voltage v_o is the FHA for input voltage to the SR stage. Considering the circuit diagram of the proposed topology in Fig. 3.10, the node voltages $v_a(t)$ and $v_s(t)$ can be defined by their Fourier series representation as shown in Eq. 3.43, and their FHA is given in Eq. 3.44, respectively. In these equations $V_{bat} = V_o$ is the battery voltage, $\omega = 2\pi f_{sw}$, and d depends on the required time delay for maintaining the ZCS in the SR stage. Defining $t_{d_{SR}}$

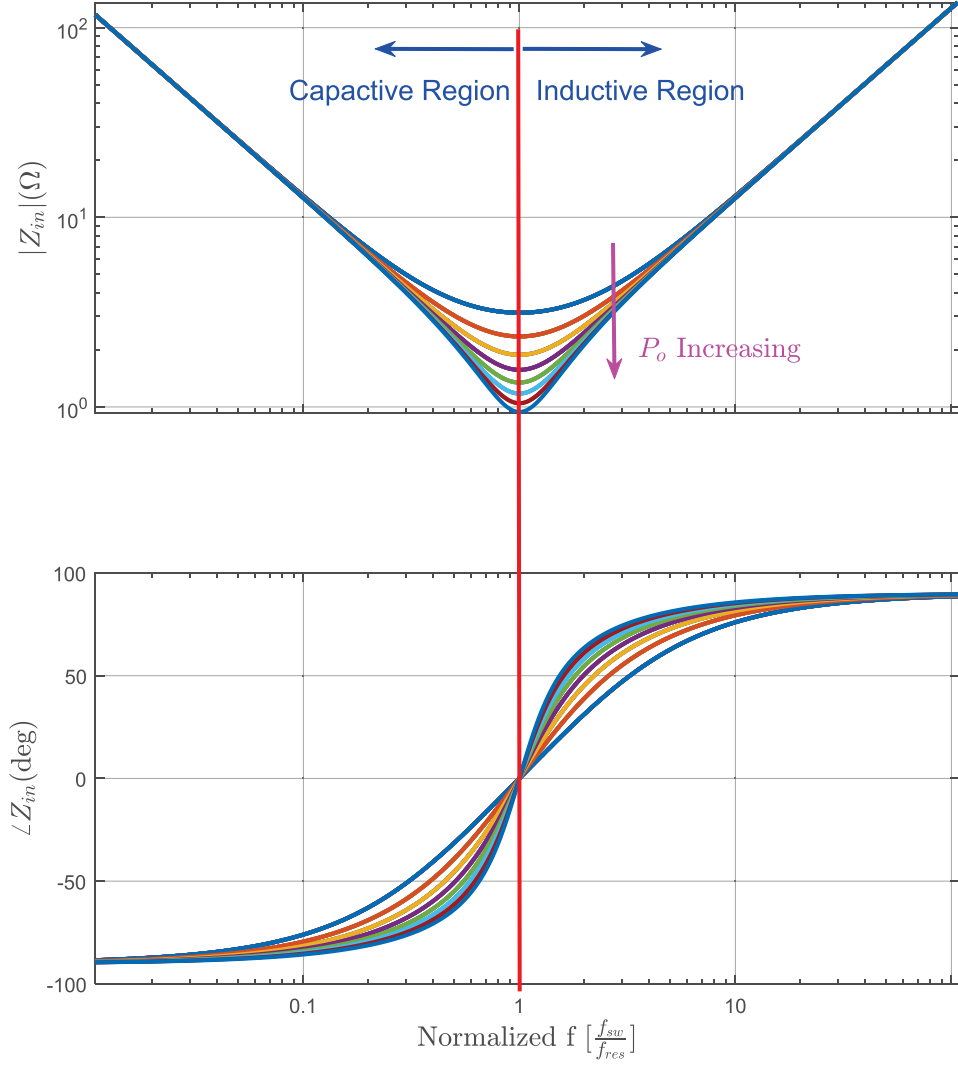


Figure 3.31: Input impedance.

as the delay between the gate drive signal of M_3 with respect to the M_1 , $d_1 = t_{dSR}/(T_{sw}/2)$.

$$\begin{cases} v_a(t) = \frac{V_{in}}{2} + \sum_{k=1}^{\infty} \left(\frac{4 \frac{V_{in}}{2} \sin\left(\frac{k\pi}{2}\right) \cdot \cos\left(k\omega t - \frac{k\pi}{2}\right)}{k\pi} \right) \\ v_s(t) = \sum_{k=1,3,5,\dots}^{\infty} \left(\frac{4V_{bat} \sin\left(\frac{k\pi}{2}\right) \cdot \cos\left(k\omega t - \frac{k\pi}{2} - kd_1\pi\right)}{k\pi} \right) \end{cases} \quad (3.43)$$

$$\begin{cases} v_{a1}(t) = \frac{4}{\pi} \frac{V_{in}}{2} \sin(\omega t) \\ v_{s1}(t) = \frac{4}{\pi} V_{bat} \sin(\omega t - d_1 \pi) \end{cases} \quad (3.44)$$

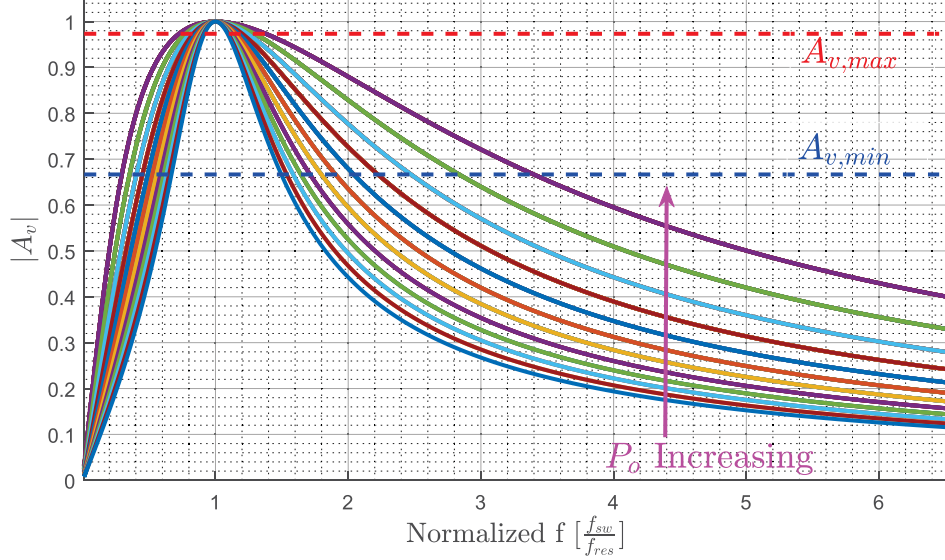


Figure 3.32: Voltage gain A_v .

The voltage gain A_v versus the normalized switching frequency ($f_n = f_{sw}/f_{res}$) for different levels of battery charging power is depicted in Fig. 3.32. As it could be seen from this figure, the voltage gain regardless of the P_o converges to unity at the resonant frequency as expected. On the other side, it is worth noting that the operation region should be limited to $f_n > 1$. Depending on the battery SOC, different voltage gain is needed ($A_{v,min} < A_v < A_{v,max}$), which could be achieved by adjusting the switching frequency $f_{sw,min} < f_{sw} < f_{sw,max}$. When the battery SOC is at very low levels, its voltage will also be low. This means the target voltage gain is low requiring high switching frequencies which will result in high power losses. In the next section a remedy to avoid very high switching frequencies will be presented.

3.4.3 Power flow Analysis

As mentioned, both FM and PSM will be utilized for the MPPT and battery charge controller. The FM is required for both MPPT control and voltage gain; however, to achieve low voltage gains the switching frequency has to increase significantly leading to high power loss and pushing high frequency noise into the EMI spectrum. In order to avoid high switching frequency for voltage regulation, and provide an extra degree of control on the power flow, PSM control strategy is also introduced for the resonant battery charger in this thesis. Two different phase shifts are utilized in the switching scheme; where, both of them affect the power flow, but, they serve different purposes. The two phase shift and their purpose are:

- Primary/ZCS phase shift (φ_1): the main intention of this phase shift is to maintain the ZCS for the MOSFETs of the rectification bridge; however, it also affects the power flow. The effect of φ_1 on the power flow is thoroughly described in Section 3.4.4.
- Secondary phase shift (φ_2): this phase shift is an extra control variable (in addition to the switching frequency) through which the battery charging power is controlled. The battery charging power dependency on φ_2 is fully described in Section 3.4.5.

The gate drive signals for M1 - M6 are depicted in Fig 3.33. Note that the dead time between the gate drive signals for the two MOSFETs belonging to the same switching leg is exaggerated for clarity. The dead time is usually much smaller fraction of the switching cycle (T_{sw}) and highly depends on the parasitic output capacitance of the MOSFETs (C_{oss}), the parasitic of the power stage switching loop, and the inductor current at which a MOSFET is turned off. As it could be seen from this figure two time delays equivalent to the phase shifts φ_1 and φ_2 are introduced between the turn-on time of M3 with respect to the M1 and M6 with respect to the M3, respectively. Note that, because the gate signals for M5 and M6 are complementary, the phase shift between M5 and M3 $\varphi_2' = \pi + \varphi_2$.

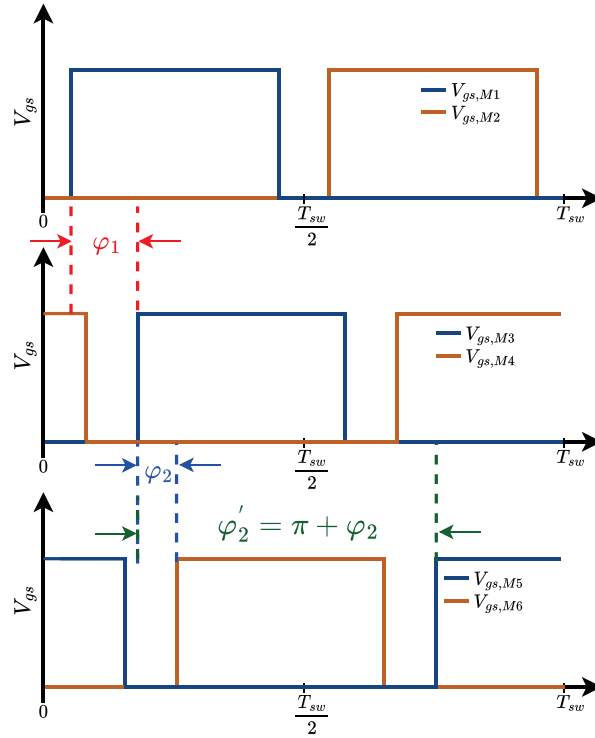


Figure 3.33: Gate drive pulse for M_1 - M_6 .

3.4.4 Effects of ZCS Phase Shift (φ_1) on Power Flow

As described in Section 3.4.3, the primary phase shift φ_1 , also referred to as ZCS phase shift in this thesis, is utilized to guarantee that the synchronous rectification MOSFETs M3-M6 turn off at

zero current reducing their switching losses and enhancing the efficiency. In order to analyze the effect of φ_1 on the power flow, the secondary phase shift is first assumed zero (i.e., $\varphi_2 = 0$). Fig. 3.34 represents the gate driving signals of M1-M6 with zero phase shift between the 2 rectification legs (i.e., $\varphi_2 = 0$). In this figure, φ_1 is the phase shift between the gate drive signals for M_3 with respect to the M_1 . It is worth noting that $\varphi_1 = d_1 \cdot \pi$ not only is utilized for maintaining the ZCS, but also, it affects the power flow as well.

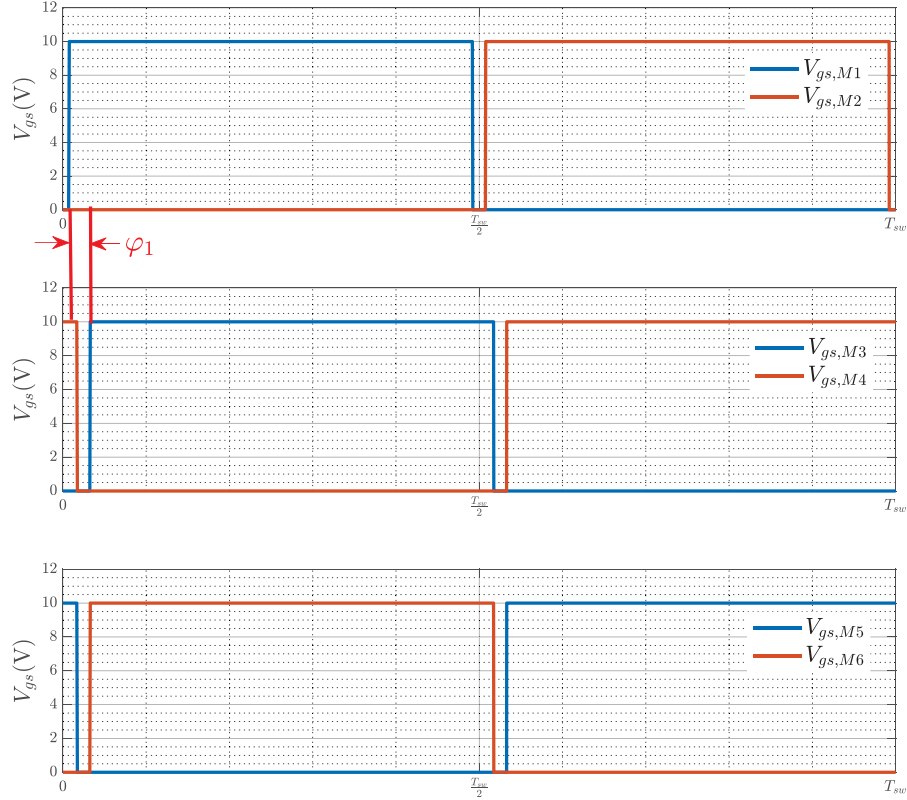
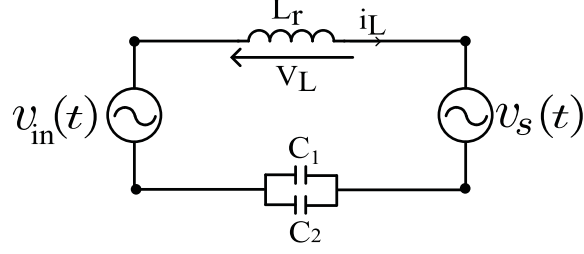
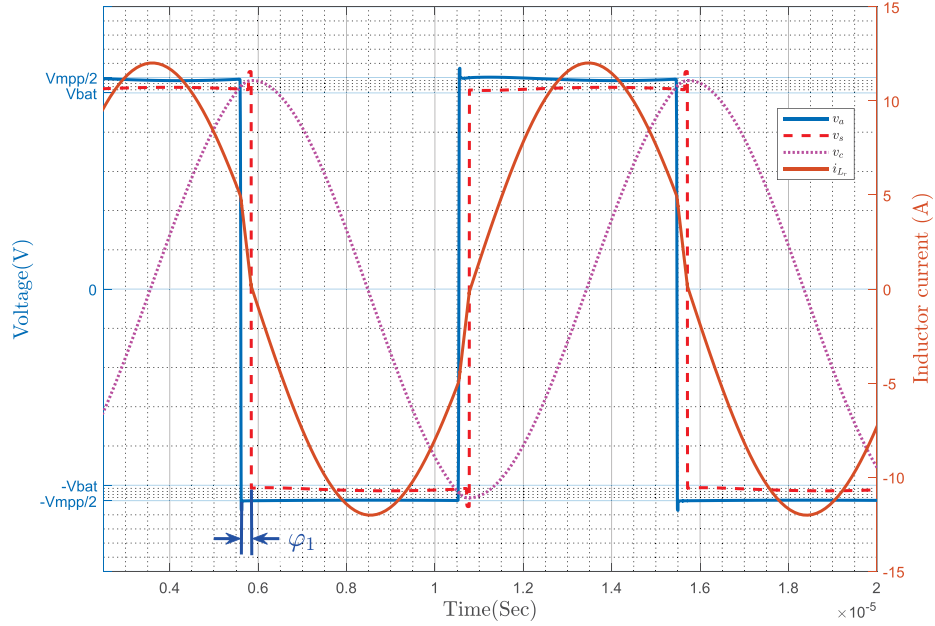


Figure 3.34: Gate drive pulse for M_1 - M_6 with $\varphi_2 = 0$.

Fig. 3.35 depicts the equivalent ac circuit for the proposed topology, where the equivalent driving voltage is defined as $v_{in}(t)$, and the voltage source $v_p(t)$ is representing the ac voltage at the input of the SR stage [19, 22]. It could be seen that the dividing capacitors are presented as the part of series resonant tank along with resonant inductor L_r . As mentioned before, the power flow depends not only on the f_{sw} , but also on φ_1 , V_{mpp} , and V_{bat} . In order to simplify the power flow analysis, case 1 is defined with $\varphi_2 = 0$ resulting in $\varphi_2' = \pi$. For this case, the voltage $v_{in}(t)$ is the ac component of $v_a(t)$, along with $v_s(t)$ both are presented in Eq. 3.43. The FHA of $v_{in}(t)$ is presented in Equ. 3.45; where, its rms value could be derived as $V_1 = \frac{\sqrt{2}}{\pi} V_{mpp}$. It is worth noting that $\varphi_1 = d_1 \pi$, and d_1 are both switching frequency and V_{mpp} dependent. Fig. 3.36 shows the ac component of $v_a(t)$, $v_c(t)$, and $v_s(t)$ along with the inductor current at a given switching frequency and its associated φ_1 to maintain the ZCS for M_3 - M_6 .


Figure 3.35: AC equivalent circuit for the power flow analysis.

$$v_{in}(t) = \frac{4}{\pi} \frac{V_{mpp}}{2} \sin(\omega t) \quad (3.45)$$


Figure 3.36: Voltage (v_{sw}, v_p, v_a) and current (i_{Lr}) waveforms.

Depending on the mpp voltage the switching frequency will be adjusted by the MPPT controller. This means for each given switching frequency its associated φ_1 should also be tuned to maintain the ZCS. On the other side, φ_1 could be limited to a minimum and maximum values to maintain the ZCS or near ZCS. The maximum value for the $t_{d_{SR}}$ (i.e., the delay between the gate drive signal of M_3 with respect to the M_1) could be calculate using the mathematical expression of Eq. 3.46; hence, $\varphi_{1,max} = (t_{d_{SR}} / (T_{sw}/2)) \cdot \pi$. The minimum value will be a phase equivalent of the dead time less than $\varphi_{1,max}$, this means $\varphi_{1,min} = \varphi_{1,max} - \varphi_d$, where $\varphi_d = (t_{d_{SR}} / (T_{sw}/2)) \cdot \pi$. Fig. 3.37 depicts the maximum and minimum limits for φ_1 for different V_{mpp} values at the nominal V_{bat} for a 4-cell LFP battery.

$$\omega_{res1} \cdot \frac{V_{mpp} + V_{bat}}{V_{mpp} - V_{bat}} \cdot t_{dLSR} - \sin \left(\omega_{res1} \cdot \left(\frac{T_{sw}}{2} - t_d - t_{dLSR} \right) \right) = 0 \quad (3.46)$$

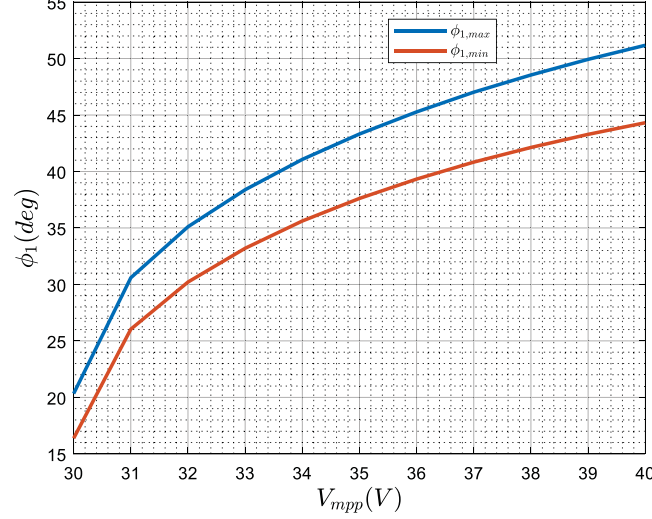


Figure 3.37: Maximum and minimum limits for φ_1 for different mpp voltages.

The output power for charging the battery could be estimated based on the FHA components of $v_{in}(t)$, and $v_p(t)$ using the phasor domain representation of these 2 voltages presented in Eq. 3.47. In this equation, $V_1 = \frac{\sqrt{2}}{\pi} V_{mpp}$ and $V_s = \frac{2\sqrt{2}}{\pi} V_{bat}$ are the rms values for the FHA of $v_{in}(t)$ (Eq. 3.45) and $v_{s1}(t)$ (Eq. 3.44), respectively.

$$\begin{cases} v_{in} = V_1 e^{j0} \\ v_{s1} = V_s e^{-j\varphi_1} \end{cases} \quad (3.47)$$

The active power can be extracted using $P_o = \Re\{v_{in} \cdot \bar{i}\}$, where $\bar{i}$ is the complex conjugate of the inductor current, presented in Eq. 3.48. In this equation X_{eq} is the equivalent reactance of the resonant tank at the switching frequency; hence, $X_{eq} = X_{Lr} - X_C = L_r \omega - \frac{1}{2C\omega}$.

$$i = \frac{(V_1 \cdot e^{j0} - V_s \cdot e^{j\varphi_1})}{jX_{eq}} \quad (3.48)$$

The delivered power to the battery and its dependency on φ_1 is presented in Eq. 3.49 as a function of V_{mpp} , V_{bat} , f_{sw} , and φ_1 . At each given V_{mpp} , there will be a certain f_{sw} for tracking the PV panel mpp; therefore, an associated φ_1 . Fig. 3.38 shows the battery charging power versus φ_1 at a specific V_{mpp} under different V_{bat} and f_{sw} , where for each given sets of $(V_{mpp}, V_{bat}, f_{sw})$ data, φ_1 is calculated based on the Eq. 3.46 as such that M_3 and M_6 turn off exactly at the moment when i_{Lr} reaches zero.

$$P_o(V_{mpp}, V_{bat}, f_{sw}, \varphi_1) = \frac{V_1 \cdot V_s \cdot \sin(\varphi_1)}{X_{eq}} = \frac{\frac{4}{\pi^2} V_{mpp} \cdot V_{bat} \cdot \sin(\varphi_1)}{(2\pi f_{sw})L_r - (1/((2\pi f_{sw})2C))} \quad (3.49)$$

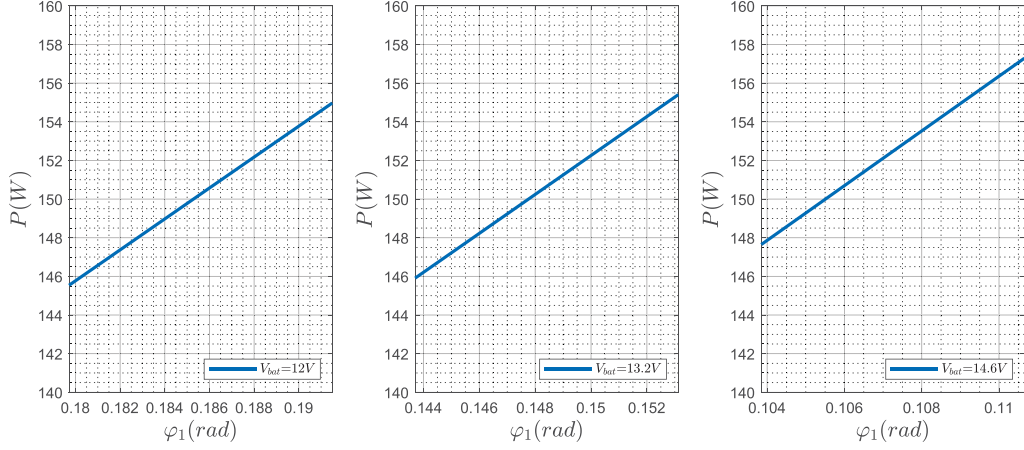


Figure 3.38: Output power at a specific V_{mpp} for different battery voltage.

3.4.5 Phase Shift Modulation (PSM) for Power Flow Control

This section describes how PSM (i.e., introducing φ_2) is utilized as a control variable for the power flow control. This phase shift is a time delay between the two switching legs of the rectification stage, contributing to the battery charging power control while maintaining the MPPT. This is especially useful when the battery is at a very low SOC or its voltage is close to the cut-off charging voltage ($V_{bat,max}$); when, the controller performs in constant voltage control mode. In order to develop a mathematical model for the charging power versus φ_2 , the FHA approximation of $v_s(t)$ could be utilized. From Fig. 3.36 it could be seen that under a perfect ZCS condition for the rectification stage and $\varphi_2 = 0$, the inductor current ($i_{Lr}(t)$) and $v_s(t)$ are in phase. Fig. 3.39 depicts $v_s(t)$ and $i_{Lr}(t)$ under $\varphi_2 = 0, \pi/4, \pi/2, 3\pi/4$ with an approximation in inductor current during the dead time as a sinusoid.

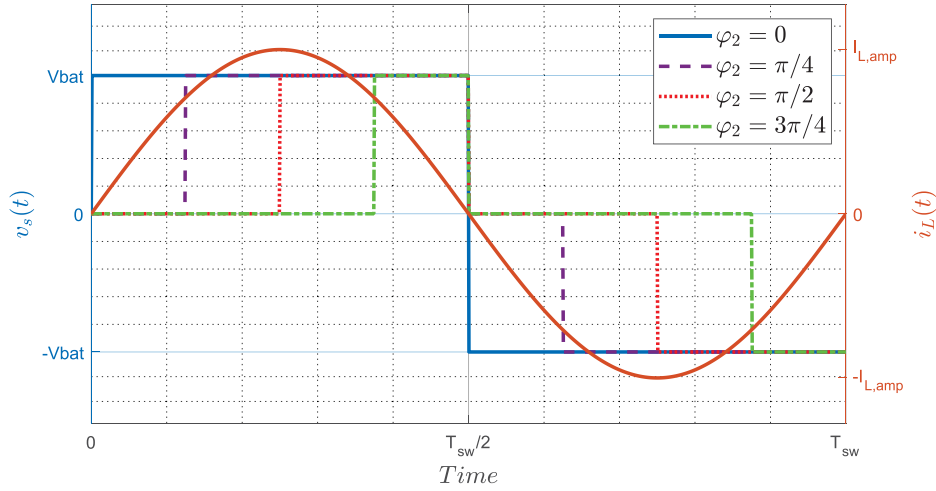


Figure 3.39: $v_s(t)$ and $i_{Lr}(t)$ under different φ_2 phase shift.

In order to present the charging power as a function of φ_2 , the Fourier series representation of $v_s(t)$ in Fig. 3.39 could be derived as a function of φ_2 . The general presentation of Fourier series for $v_s(t)$ is shown in Eq. 3.50. In this equation k represents the k^{th} harmonic with the fundamental frequency of ω .

$$v_s(t) = \sum_{k=1}^{\infty} (a_k \cdot \cos(k\omega t) + b_k \cdot \sin(k\omega t)) \quad (3.50)$$

The first harmonic coefficients a_1 and b_1 , could be extracted from a_k and b_k presented in Eq. 3.51 by replacing $k = 1$. In this equation the time domain representation of $v_s(t)$, presented in Fig. 3.39, should be included. This time domain is shown in Eq. 3.52.

$$\begin{cases} a_k = \frac{2}{T_{sw}} \int_0^{T_{sw}} v_s(t) \cos(k\omega t) dt \\ b_k = \frac{2}{T_{sw}} \int_0^{T_{sw}} v_s(t) \sin(k\omega t) dt \end{cases} \quad (3.51)$$

$$\begin{cases} v_s(t) = 0 & 0 \leq t \leq d_2 \cdot T_{sw} \\ v_s(t) = +V_{bat} & d_2 \cdot T_{sw} \leq t \leq \frac{T_{sw}}{2} \\ v_s(t) = 0 & \frac{T_{sw}}{2} \leq t \leq (\frac{T_{sw}}{2} + d_2 \cdot T_{sw}) \\ v_s(t) = -V_{bat} & (\frac{T_{sw}}{2} + d_2 \cdot T_{sw}) \leq t \leq T_{sw} \end{cases} \quad (3.52)$$

Replacing $v_s(t)$ from Eq. 3.52 in Eq. 3.51 results in Eq. 3.53 for a_k and b_k . It is clear from Eq. 3.53 that the Fourier series coefficients for even values of k are zero (i.e., $a_k = b_k = 0$ for $k = 2, 4, 6, \dots$). Defining $\varphi_2 = d_2 \cdot 2\pi$, the Fourier series of Eq. 3.50 could be re-written as shown in Eq. 3.54. From this equation, the first harmonic of $v_s(t)$, defined as $v_{s, FH}(t)$, is derived as shown in Eq. 3.55.

$$\begin{cases} a_k = \frac{V_{bat}}{k\pi} ((-1)^k - 1) \sin(2k\pi d_2) \\ b_k = \frac{V_{bat}}{k\pi} (1 - (-1)^k) (1 + \cos(2k\pi d_2)) \end{cases} \quad (3.53)$$

$$v_s(t) = \sum_{k=1,3,5,\dots} \left(\left[\frac{-2V_{bat}}{k\pi} \sin(k\varphi_2) \right] \cdot \cos(k\omega t) + \left[\frac{2V_{bat}}{k\pi} (1 + \cos(k\varphi_2)) \right] \cdot \sin(k\omega t) \right) \quad (3.54)$$

$$v_{s, FH}(t) = \left[\frac{-2V_{bat}}{\pi} \sin(\varphi_2) \right] \cdot \cos(\omega t) + \left[\frac{2V_{bat}}{\pi} (1 + \cos(\varphi_2)) \right] \cdot \sin(\omega t) \quad (3.55)$$

The battery charging power could be estimated by multiplying $v_{s, FH}(t)$ and $i_{Lr}(t)$ in time domain. The resulted output power as a function of time is presented in Eq. 3.56.

$$p_{o, \varphi_2}(t) = \left[\left[\frac{-2V_{bat}}{\pi} \sin(\varphi_2) \right] \cdot \cos(\omega t) + \left[\frac{2V_{bat}}{\pi} (1 + \cos(\varphi_2)) \right] \cdot \sin(\omega t) \right] \cdot [I_{L, amp} \cdot \sin(\omega t)] \quad (3.56)$$

Since the inductor current is sinusoid, under full wave rectification $I_{L,amp} = \frac{\pi}{2} \cdot I_{bat}$; where, I_{bat} is the battery dc charging current. Defining the battery charging power under $\varphi_2 = 0$ as $P_0 = V_{bat} I_{bat}$, Eq. 3.54 could be re-written as shown in Eq. 3.57.

$$p_{o,\varphi_2}(t) = -P_0 \sin(\varphi_2) \cdot \frac{\sin(2\omega t)}{2} + P_0(1 + \cos(\varphi_2)) \cdot \frac{1 - \cos(2\omega t)}{2} \quad (3.57)$$

Finally, From Eq. 3.57 the average charging power as a function of φ_2 (P_{o,φ_2}) is derived as presented in Eq. 3.58.

$$P_{o,\varphi_2} = P_0 \cdot \frac{1 + \cos(\varphi_2)}{2} \quad (3.58)$$

Note that in this equation $P_0 = V_{bat} I_{bat} = \eta \cdot P_o(V_{mpp}, V_{bat}, f_{sw}, \varphi_1)$; where, η is the efficiency and P_o is the extracted mpp power derived in Eq. 3.49. Defining the normalized battery charging power as $P_n = P_{o,\varphi_2}/P_0$, this power as a function of φ_2 is presented in Eq. 3.59.

$$P_n = \frac{1 + \cos(\varphi_2)}{2} \quad (3.59)$$

Fig. 3.40 depicts the normalized battery charging power versus φ_2 . As it could be seen from this figure, the normalized power is at unity for $\varphi_2 = 0$ and battery charging power is $P_{o,\varphi_2} = P_0$, as it is expected. Increasing φ_2 , results in a smaller portion of switching cycle during which the power is transferred to the battery, and at $\varphi_2 = \pi$ this power is reduced to 0.

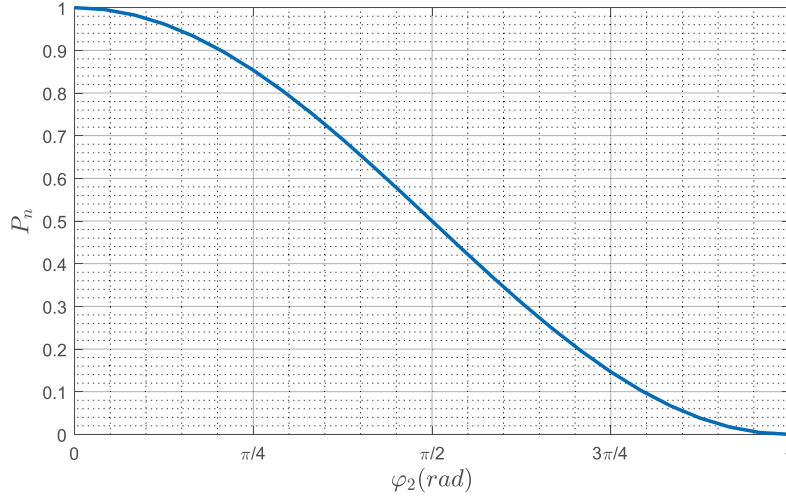


Figure 3.40: Normalized output power versus modulated phase (φ_2).

Chapter 4

Components Design, Simulation, and Results Analysis

4.1 Objectives

To validate the mathematical modeling and control objectives for the proposed resonant battery charger described in Chapter 3, a through open-loop and closed-loop simulation and results analysis using LTspice, PSIM, and MATLAB tools is presented in this chapter. The first step in this analysis is defining the simulation parameters; which, requires designing the proposed topology resonant tank components. Based on the designed resonant tank and simulation results in this chapter, a thorough schematic component selection procedure is presented in Chapter 5. This chapter (Chapter 4) includes:

- Topology key components design: this involves utilizing the mathematical model developed in Chapter 3 in order to design the key components of the topology. This includes:
 - defining the operation range for switching frequency
 - design criteria on the resonant frequency
 - designing the resonant tank components including the inductor and the dividing capacitors
- Comprehensive open loop simulation, using LTspice, and results analysis:
 - to validate the designed parameters
 - comparative power loss analysis for defining the key parameters for the main components (e.g., inductor, capacitor, MOSFETs)
 - to validate the time-domain mathematical model
- Comprehensive closed loop simulation, using PSIM, and results analysis:
 - to validate the mathematical modeling of the power flow
 - to examine the control strategies, including: MPPT, constant-voltage control, and phase shift modulation
 - to examine the efficiency of the closed-loop system.

4.2 Resonant Tank Components Design

In order to design the key components for the proposed topology, the main criteria should be defined first. One of the decisive factors that affects the components design is the intended switching frequency range. Since one of the goals of the design topology is maintaining ZVS for the inverting stage MOSFETs turning-ON transition, the inductive input impedance is a must. As a result, according to the input impedance graph in Fig. 3.31, the switching frequency must be higher than the resonant frequency of the resonant tank. Note that the resonant tank in the proposed topology consists of L_r , C_1 , and C_2 . The component design could be done using the FHA equivalent circuit. The FHA representation of the topology could be depicted as the circuit diagram shown in 4.1. As described in 3.4.2, the FHA representation of the proposed topology could be utilized for the voltage gain and input impedance analysis. This analysis along with the desired operation objectives could be used for designing the key components.

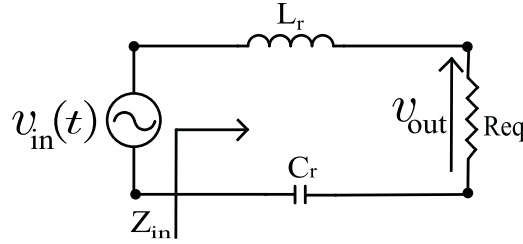


Figure 4.1: Equivalent FHA circuit for the proposed topology in Chapter 3.

In Fig. 4.1, v_{in} represents the FHA of ac representation of the inverted PV voltage, L_r and $C_r = C_1 + C_2$ are the resonant tank components, and R_{eq} is the resistive load equivalent to the battery charging power reflected to the input side of the synchronous rectification stage. In order to design the proper values for L_r and C_r , the desired resonant and switching frequencies, to extract the maximum power from the PV, should be taken into consideration. On the other side the PV MPP voltage and battery minimum and maximum cutoff voltages also dictate the operation voltage gain. The voltage gain, in return, also dictates the required switching frequency range. To simplify the design process and at the same time develop a generalized design methodology the normalized frequency $f_n = f_{sw}/f_r$, and quality factor $Q = 1/(\omega \cdot C_r \cdot R_{eq})$ are defined. Note that f_{sw} , and $f_r = 1/(2\pi\sqrt{L_r C_r})$ are the switching and resonant frequencies, receptively. Defining the voltage gain $A_v = v_o/v_{in}$, using the equivalent circuit of Fig. 4.1, the voltage gain can be express as Eq. 4.1.

$$|A_v| = \frac{1}{\sqrt{1 + (f_n^2 - 1)^2 * Q^2}} \quad (4.1)$$

As it could be seen from Eq. 4.1, the voltage gain is simply a function of f_n and Q . In order to maintain the ZVS operation for M_1 & M_2 , the input impedance Z_{in} should remain inductive resulting in $f_n > 1$ requirement. Fig. 4.2 depicts the voltage gain versus f_n at different values of Q ; where, $Gain = V_{bat}/V_{mpp} = |A_v|/2$ is defined. In addition to the voltage gain the minimum and maximum cutoff gains are also shown in this figure. These gains are associated with the ratio between the minimum discharging and maximum charging battery cutoff voltages and PV MPP voltage. Considering the 4-cell battery voltage parameters and the PV MPP voltage given in Table 3.1, these two gains could be calculated as $Gain_{min-cutoff} = 12V/35.5 = 0.338$ and $Gain_{max-cutoff} = 16.8V/35.5 = 0.473$. Note that under different battery charging power and

solar irradiation conditions the switching frequency should be controlled to provide a proper voltage gain.

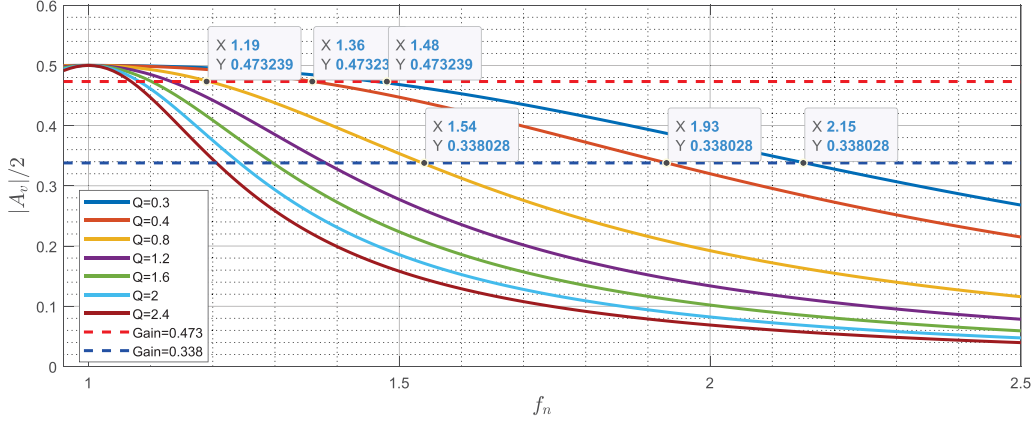


Figure 4.2: FHA voltage gain divide by 2 and the ratio between the battery and PV MPP voltages.

On the other side, the following observations from Fig. 4.2 could be concluded:

- For lower Q values the gain slope variation versus normalized switching frequency is slow; hence, it is necessary to exploit a wider frequency range for obtaining the required voltage ratio. This leads to better MPPT controllability under different sun irradiation condition; however, for lower voltage gains the switching frequency increases substantially.
- For higher quality factor Q , the voltage gain roll-off is much steeper as the switching frequency increases. This provides lower voltage gain without large increase in the switching frequency; however, the voltage gain is much more sensitive to the frequency change. This high sensitivity could create large transients during abrupt load or solar irradiation condition changes.
- As a compromise between the higher limit of the switching frequency under nominal operation condition and the controllability, $Q = 0.8$ is selected for the resonant capacitor (C_r) design purpose.

In order to design C_r , the R_{eq} for nominal operation condition should be calculated along with defining a desired operation frequency range or Q . The nominal conditions are defined as $V_{mpp} = 35.5V$, $P_{mpp} = 145.5W$, $V_{bat} = 14.6V$, and an efficiency of $\eta = 98\%$. Under these condition, the equivalent R_{eq} could be presented as Eq. 4.2. Note that R_{eq} is the equivalent resistance for the battery charging power reflected from the battery side to the primary side of the rectification stage.

$$R_{eq} = \frac{8}{\pi^2} * R_{load} = (8/\pi^2) * (V_{bat}^2 / (\eta * P_{mpp})) = 1.2117\Omega \quad (4.2)$$

In addition to the equivalent resistance under nominal operation condition, the desired switching frequency should be also assumed for calculating the required resonant capacitor. Designing for a switching frequency of $115kHz$ under the defined nominal conditions results in $C_r = 1/(2 * \pi * f_{sw} * R_{eq} * Q) = 1/(2 * \pi * 105 * 10^3 * 1.2117 * 0.8) = 1.42\mu F$. This leads to

the calculating required dividing capacitors $C_1 = C_2 = C_r/2 = 0.71\mu F$, and since the closest standard capacitance value to the calculated number is $0.68\mu F$, $C_1 = C_2 = 0.68\mu F$ are chosen.

In order to guarantee the inductive operation, hence, maintaining the ZVS for M_1 & M_2 , a minimum 20% margin between the switching frequency under the nominal operation condition and the resonant frequency is considered. Note, this margin is necessary for providing enough controllability in the frequency modulation and also accounting for the derating in the dividing capacitors and resonant inductor under different dc bias and operating temperature conditions. The minimum 20% margin between the resonant and switching frequencies results in a resonant frequency of $f_r \leq 0.8 * f_{sw} = 92kHz$ for the resonant tank. Using the selected capacitance for the dividing capacitors and the resonant frequency f_r , the required resonant inductance could be calculated by $L_r \geq 1/((2 * \pi * f_r)^2 * (C_1 || C_2)) = 1/((2 * \pi * 92 * 10^3)^2 * 1.36 * 10^{-6}) = 2.2\mu H$. The calculated minimum limit of $2.2\mu H$ is a standard inductance value results in maintaining the $f_r = 1/(2\pi\sqrt{L_r * (C_1 + C_2)}) = 92kHz$.

In order to validate that the designed L_r value meets the ZVS requirements, it should be noted that the energy storage in the inductor at the time when either of M_1 or M_2 turn OFF should be high enough to support the charge and discharge of the C_{oss} of these MOSFETs. If the stored energy is high enough, sufficient time will be provided for charging/discharging $C_{oss,M1}$ & $C_{oss,M2}$ while also extending an extra time for turning ON the body diode of the MOSFET that is intended to turn ON. The turn ON of the body diode assures that at the time when the gate signal for its associated MOSFET goes high, the voltage across the drain-to-source of the MOSFET is close to zero; hence, resulting in a ZVS turn ON of the MOSFET channel. This requirement introduces a new boundary on the required inductance value as described in Eq. 4.3; where, $I_{L_{ZVS}}$ is the absolute value of the inductor current at the time of turning OFF the MOSFETs M_1 or M_2 . As the output capacitance of the MOSFETs is much smaller comparing to the dividing capacitors, the $L_r = 2.2\mu H$ is still an appropriate design; however, Eq. 4.3 could be utilized to derive the minimum required inductor current to meet the ZVS requirements with the designed inductor as shown in Eq. 4.4.

$$L_r > \frac{2 * C_s * V_{mpp}^2}{I_{L_{ZVS}}^2} \quad (4.3)$$

$$I_{L_{ZVS}} > V_{mpp} \sqrt{\frac{2 * C_s}{L_r}} \quad (4.4)$$

4.3 Simulation Results and Analysis

In this section, considering the designed component values at the previous section, open-loop simulation using LTspice is implemented for the validation of the designed parameters, expected design operation, and the time-domain mathematical models derived in chapter 3. Then, the comparative analysis will be done from the efficiency perspective by employing different component SPICE models from different manufacturers, resulting in the selection of final proper candidate components for the proposed topology.

In addition to the open-loop simulation, the closed-loop simulation is performed in PSIM for validation of the power flow analysis done in chapter 3, and for verifying the performance of the recommended control strategies. This includes validating the performance of the MPPT algorithm and constant voltage mode. Moreover, the proposed phase shift strategies in Chapter 3 are also validated. This includes the phase shift of the SR stage wrt the inverting stage (φ_1), for the purpose of achieving SR ZCS, and the phase shift between leg 2 of SR stage wrt its leg 1 (φ_2)

as the variable for power flow control. In the following sections the simulation results and their analysis are presented.

4.3.1 Open-Loop Simulation Results and Analysis

The open-loop simulation begins with the comparative simulation and analysis on both the series resonant topology presented in Fig.3.9 and the proposed topology in Fig. 3.10, and then focus on the proposed topology and provides a comprehensive simulation and analysis from different aspects.

• Comparative open-loop simulation results and analysis on the series resonant topology and proposed topology

The comparative simulation of the series-resonant topology and the proposed topology involves comparing the switching frequency range under the same output battery voltage and charging power operating points, key component current and voltage stress evaluation, and their implications on the components selection. This analysis and comparison aims to validate the choice of the topology for this thesis research. Both topologies are simulated using the designed resonant tank in Section 4.2. Table 4.1 presents the simulation parameters used for the comparative analysis of both topologies; where, a multi-step simulation is conducted in LTspice, then, the simulation data points are plotted using MATLAB. In this open-loop simulation, associated with each step there is a pair of (f_{sw}, P_{out}) with a constant battery voltage (V_o). Note that at each step the output power P_{out} is a fraction of nominal power P_{nom} within $0.1 \leq P_{out}/P_{nom} \leq 1$.

Parameter	Value
V_{mpp}	35.5V
P_{nom}	142W
V_o	13.2V
L_r	$2.2\mu H$
C_r	$2 \times 0.68\mu F$
$C_1 = C_2$	$0.68\mu F$

Table 4.1: Parameter used in LTspice open-loop simulation.

Fig. 4.3 presents the switching frequency versus the ratio between the output power and nominal power P_{out}/P_{nom} . As it could be seen from this figure as the output power increases the switching frequency for both topologies reduces. Even though the switching frequency for both topologies at a given output power is very close, it is slightly higher for the series resonant topology. It could be also noticed that this difference is more pronounced under lighter loads.

It is worth noting that the switching frequency adjustment at each step of the simulation not only controls the output power, but also, it is the control variable that controls the output voltage at the target level. This target output voltage is given in Table 4.1. Fig. 4.4 depicts the output voltage of the series-resonant and proposed topologies versus the normalized output power; where, the nominal power is considered as the base power. It could be seen that under different output power, as the switching frequency is adjusted, the output voltage is regulated to the target 13.2V.

The open-loop simulation for the series resonant and proposed topologies aims to compare the key components operating voltage and current under both transient and steady-state conditions. This comparison reveals that which topology imposes higher voltage/current stress to the key components.

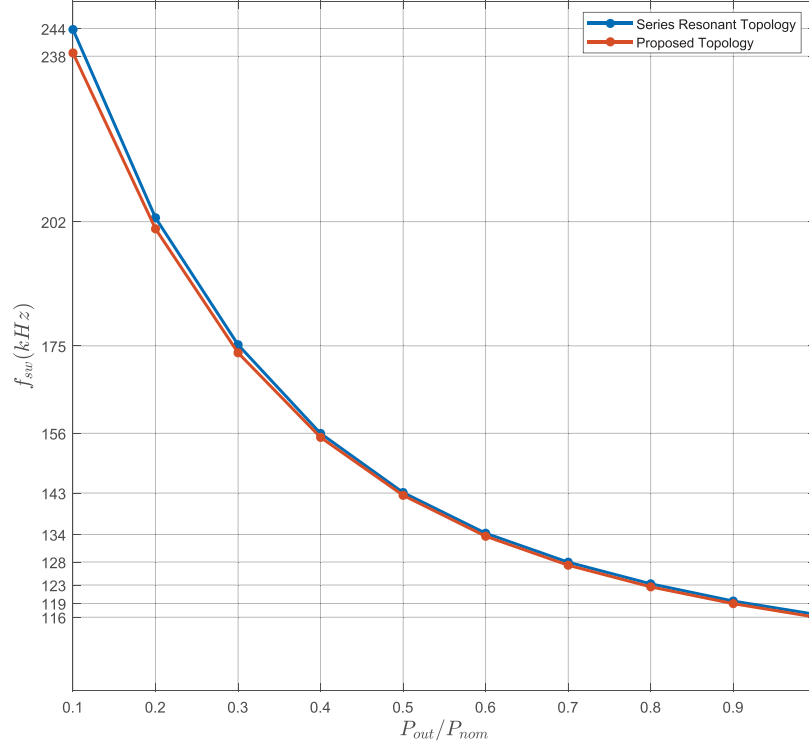


Figure 4.3: Switching frequency versus normalized output power for series resonant and proposed topologies.

Current stress: Note that the effects of the current level contributes to the conduction losses quadratically; hence, maintaining lower level of current for transferring the same level of power contributes to much lower conduction losses resulting in substantially higher efficiency. Also note that, since the two topologies are aimed at ZVS and ZCS operation the key power loss element is the conduction loss; hence, optimizing for conduction loss is the out most important factor for enhancing the efficiency. On the other side, the major conduction loss contributors are the resonant inductor and capacitors, inverting-side MOSFETs, and SR-side MOSFETs. It should be noted that the DC-link capacitors utilized on both PV and battery sides are responsible for bypassing the ac components of the currents; hence, high current stress contributes to higher losses and operating temperature for these capacitors. The high operating temperature contributes to reducing the capacitors lifetime. For example, in the case of electrolytic capacitors every $10^{\circ}C$ in temperature change reduces the life time of the capacitor by half as it could be derived from $L = L_0 * 2^{\frac{T_0 - T_{op}}{10}}$ [32]. In this equation, L_0 and T_0 are the base capacitor life time and ambient temperature, respectively. The term T_{op} is the capacitor operating temperature; hence, a $10^{\circ}C$ increase in the operating temperature wrt the ambient temperature results in a factor of 1/2 of base life time.

Voltage stress: The high voltage stress also has various adverse effects on the performance of the DC-DC battery charger. The high voltage stress on the capacitors contributes to faster degradation of their dielectric [33]; while, also results in the capacitance derating in the case of dc-voltage bias. The high DC and AC voltage stress also affects the capacitor lifetime;

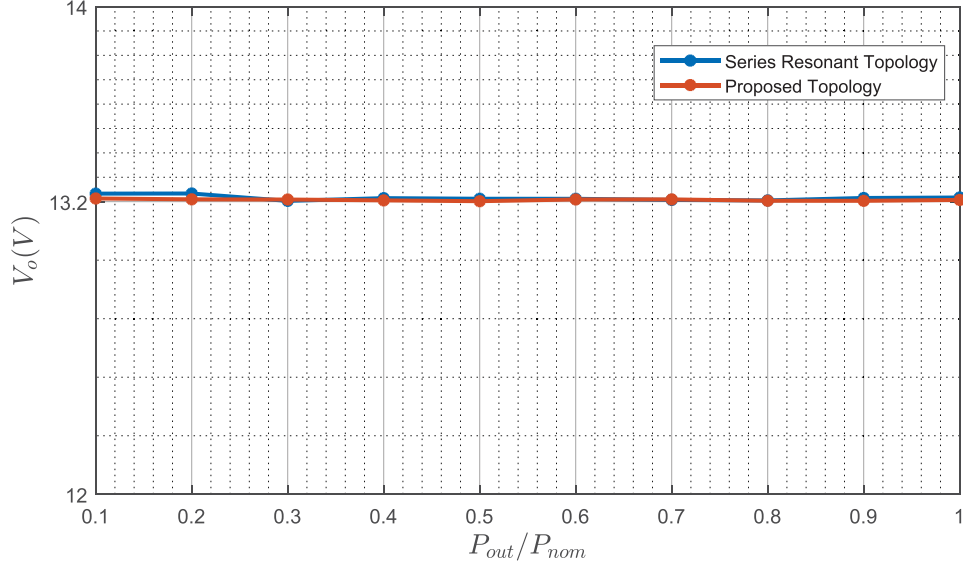


Figure 4.4: Regulated output voltage versus normalized output power for series resonant and proposed topologies at target battery voltage of 13.2V.

where, if the voltage stress is beyond the rated voltage for the capacitors, it reduces their life time substantially [33].

In order to derive the rms and max inductor current during transient and steady state operation conditions at each operating point of the multi-step LTspice simulation the .MEASURE command is utilized. As before, the LTspice simulation data points are plotted using the MATLAB. Fig. 4.5 presents the steady-state inductor rms current for both series resonant and proposed topology. As it could be seen from this figure the steady state rms current at a specific output power data point at the target voltage of 13.2 is very close for both topologies. This is a results is confirming that once the switching frequency for each topology is adjusted to provide the target voltage and power the expected battery charging current and hence the rms inductor current should be almost identical. This could be explained by the the fact that, at steady state the clamping diodes for the proposed topology are not intended to be forward biased; therefore, the FHA equivalent circuits for both topologies become identical. Note that the battery charging current is directly proportional to the inductor rms current as $I_{bat} = (2/\pi) * I_{L,m} \Rightarrow I_{L,rms} = (\pi/(2\sqrt{2}))I_{bat}$; where, I_{bat} and $I_{L,m}$ are the battery charging current and inductor FHA current amplitude, respectively.

Even though the inductor current rms values at the steady state under a certain operation point are almost identical for both series resonant and the proposed topologies, the peak values under the transient condition could be different. Fig. 4.6 depict the transient inductor current amplitude versus normalized output power for both of these two topologies. As it could be seen under light load condition the peak current for both topologies are very close. This behavior could be justified, because, at light load the inductor current is still low ; hence, the voltage at node 'c' of the proposed topology (see Fig. 3.10) does not increase high enough to be clamped. Under this condition, as it is expected, the behavior of the proposed topology and the series resonant topology are very similar. It could be observed that as the power increases the peak currents diverge substantially. It is evident that for the series resonant topology the transient peak inductor current increases rapidly as the output power increases; while, it approaches a

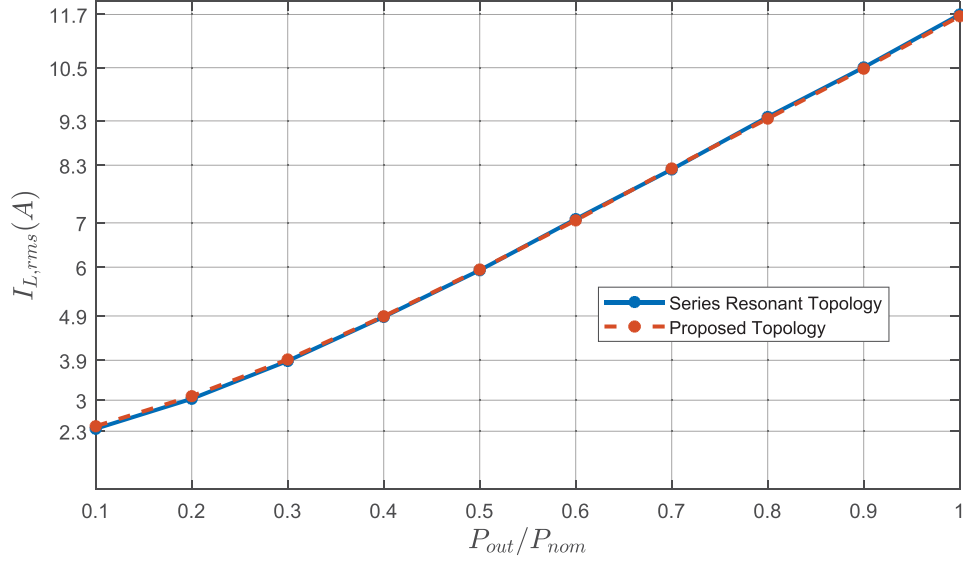


Figure 4.5: Resonant inductor rms current in steady-state condition versus normalized output power for series resonant and proposed topologies at target battery voltage of 13.2V.

constant level for the proposed topology under higher power levels. This is the result of utilizing the dividing capacitor and clamping diodes as under transient condition at higher power the voltage at node 'c' of the proposed topology (see Fig. 3.10) is either clamped or its rate of change decreases substantially preventing further increase in the resonant inductor current. Another important aspect of limiting inductor peak current is that it prevents the inductor saturation; while, for the series resonant topology the inductor has to be over-sized to handle high transient currents. In other words, since the peak transient current in the series resonant topology is high, either an inductor with larger core size should be selected or a core material with higher saturation flux density (i.e., higher saturation current for the same size) has to be utilized. Note that an inductor with high saturation flux density material often is at a higher cost of these material as well. From another point of view, an inductor with high saturation current could be also structures around a core with larger cross-section area, this still translates to larger inductor core dimension and , hence, lower power density of the DC-DC battery charger.

On the other side, it is expected that higher transient resonant inductor current also leads to an increased voltage stress on the resonant capacitors. Fig. 4.7 depicts the peak transient voltage stress on the resonant capacitor C_r of the series resonant topology and the dividing capacitor C_2 of the proposed topology. It could be seen that the capacitor peak transient voltage also follow the same trend as the peak transient inductor current. The resonant capacitor peak transient of series resonant topology and dividing capacitor C_2 of the proposed topology are very close at light load; however, this peak voltage for the C_r of the series resonant increases substantially at higher load. This phenomenon is reasonable as the capacitor voltage has direct relationship with the inductor current under $v_{C,peak} = X_C * i_{L,peak}$; where, X_C is the reactance of the associated capacitor at the switching frequency. It is worth noting the role of the clamping diodes in limiting the current and voltage stresses; hence, these diodes are expected to have power losses during the initial transients.

- **Switching performance and efficiency evaluation of the proposed topology**

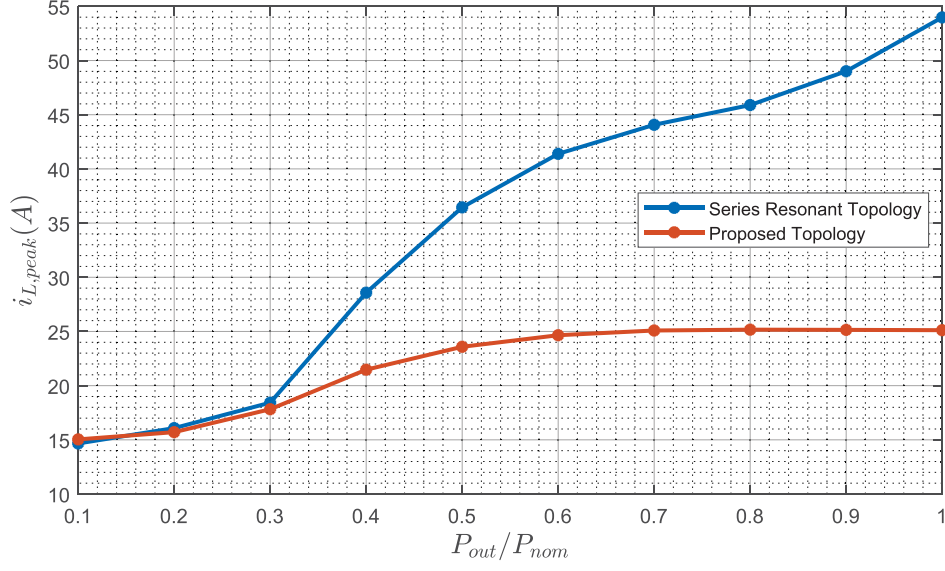


Figure 4.6: Resonant inductor peak transient current versus normalized output power for series resonant and proposed topologies at the target battery voltage of 13.2V.

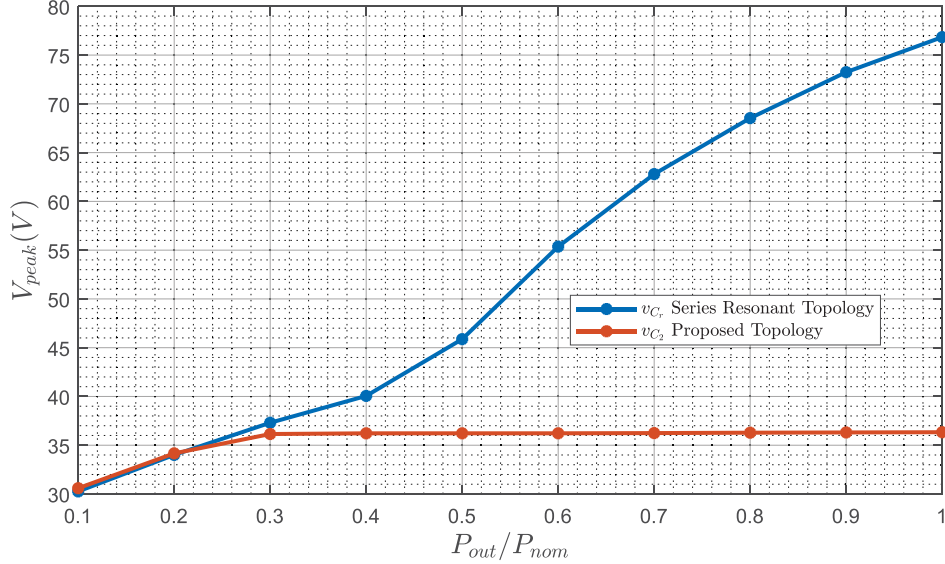


Figure 4.7: Peak transient resonant/dividing capacitors voltages versus normalized output power for series resonant and proposed topologies at the target battery voltage of 13.2V.

As describe before, the proposed topology provides a more moderate operation switching frequency with much lower current and voltage stress comparing to the series resonant topology. The open-loop simulation using LTspice is further utilized to evaluate different aspects of the proposed topology including detailed power loss analysis in the key components and the topology efficiency evaluation; while, adjusting the switching frequency to provide an MPPT operation scenario.

Table 4.2 provide the parameters utilized in the open loop MPP simulation for the proposed topology.

Parameter	Value
V_{mpp}	35.5V
P_{mpp}	145.5W
V_{bat}	[12V 13.2V 13.8V 14.6V 15V]
L_r	2.2 μ H
$C_1 = C_2$	0.68 μ F
inverting-side MOSFETS (M_1 & M_2)	TPH4R10ANL
SR-side MOSFETS ($M_3 - M_6$)	TPH4R10ANL

Table 4.2: Parameters used in LTspice open-loop simulation under MPP operation condition.

Fig. 4.8 depicts the operating switching frequency for the proposed topology versus battery voltage while maintaining the MPP operation condition. In this simulation the switching frequency for each battery voltage is adjusted in such a way that the MPP power condition at the input side is established. As it could be seen at lower voltage; where, the ratio between the battery voltage and the MPP voltage is lower in order to extract the same MPP power the switching frequency is higher. This could also be understood from the voltage gain modeling described before. In other words, at lower battery voltage the equivalent resistance at the input of the SR stage is lower resulting in lower input impedance or the impedance seen from the inverting stage point of view. Since the goal is to maintain the MPPT, the switching frequency should be increased so that the effect of the lower equivalent resistance is compensated and hence maintaining the same MPP power.

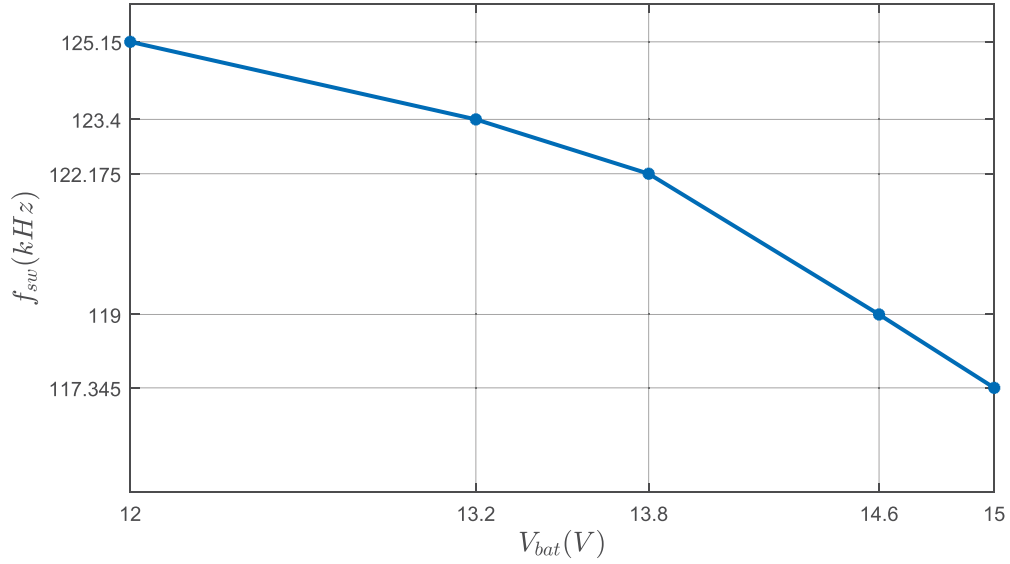


Figure 4.8: Switching frequency versus battery voltage for MPP operation at $(V_{mpp}, P_{mpp}) = (35.5V, 145.5W)$.

Since at each battery voltage the switching frequency is adjusted to extract the MPP power, it is expected that the battery charging current is higher at lower battery voltages. It is evident

that an increase in the battery charging current leads to higher resonant inductor RMS current. Fig. 4.9 depict the inductor rms current for the proposed topology for different values of battery voltage. As expected the increase in the battery voltage results in lower charging current at the same MPP power; hence, leading to lower inductor rms current. This is also evident from Fig. 4.9.

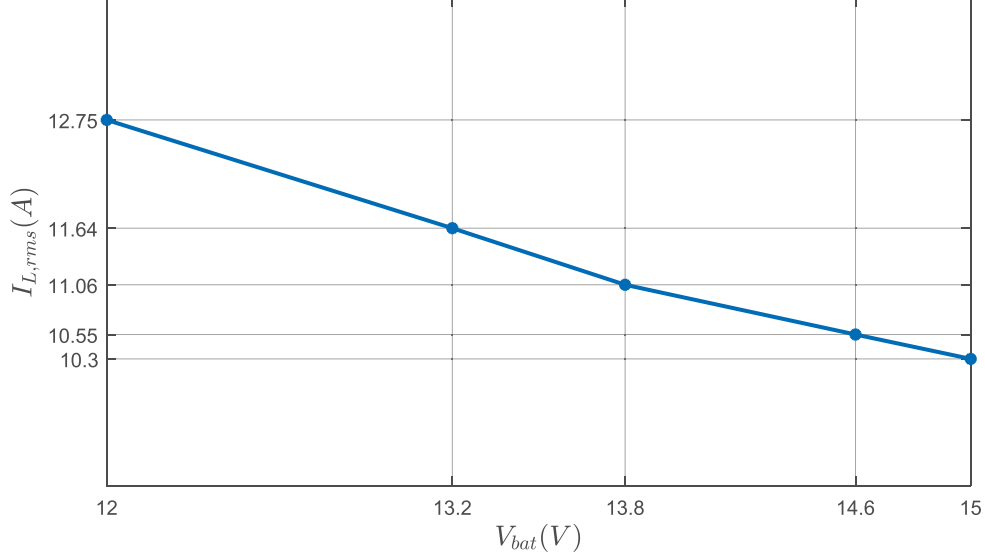


Figure 4.9: Resonant inductor rms current versus battery voltage when $(V_{mpp}, P_{mpp}) = (35.5V, 145.5W)$ is maintained.

As described in Section 3.4.4, the phase shift between the gate signals for the SR stage wrt the inverting stage, defined as φ_1 , is introduced to provide the ZCS condition for the SR stage MOSFETs $M_3 - M_6$. The ZCS reduces the switching losses of these MOSFETs significantly and improves the efficiency. Fig. 4.10 depicts the ZCS φ_1 for different battery voltage while maintaining the MPP operation condition. As it could be seen, the increase in the battery voltage leads to a reduction in φ_1 . This could be justified by the fact that at higher battery voltage the current is lower and shorter time interval is required for the current to reach zero from the moment when either of M_1 or M_2 turns OFF.

As described before, the increase in the battery voltage results in lower battery charging current and the inductor rms current under the same (V_{mpp}, P_{mpp}) . Also, as mentioned before the switching frequency range is within an inductive operation range for the input impedance. This combined with the ZCS phase shift for the SR stage provide a soft-switching operation condition for the proposed topology; hence, the key power loss components for the MOSFETs is expected to be dominantly the conduction loss; while, the inductor power loss includes both conduction and core loss. Fig. 4.11 presents the power loss breakdown for the inverting stage MOSFETs M_1 & M_2 , SR stage leg 1 MOSFETs M_3 & M_4 , SR stage leg 2 MOSFETs M_5 & M_6 , and the resonant inductor. It could be seen that under higher battery voltage and a constant MPP condition, as expected the power loss for the MOSFETs and inductor reduces.

Note that the inductor power loss is a function of both switching frequency and the current. Higher switching frequency not only increases the inductor ac resistance (dominantly because of the skin effect), but also, results in higher core loss. This combined higher conduction loss and core loss coincide at lower battery voltage as both charging current and switching frequency are

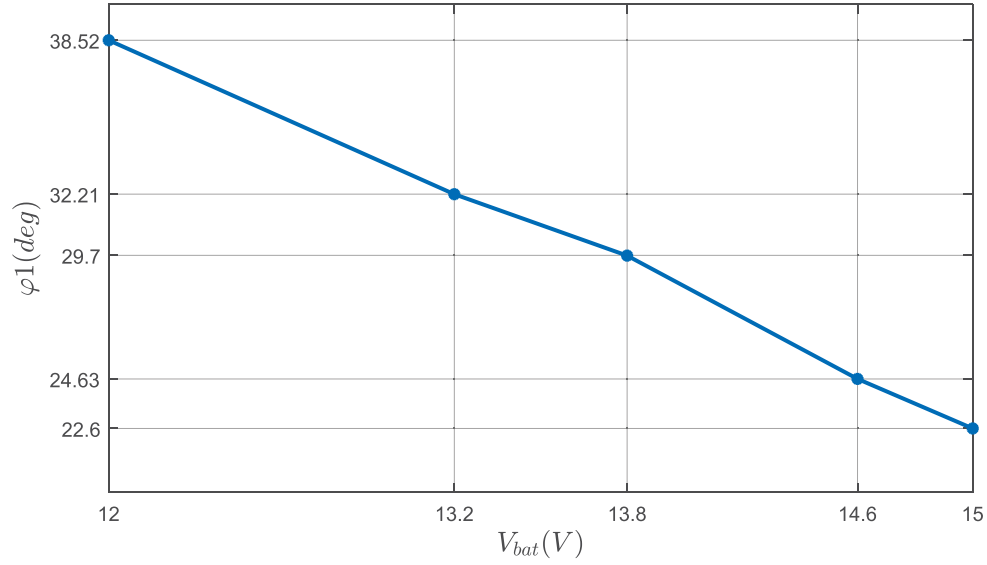


Figure 4.10: ZCS phase shift (φ_1) versus battery voltage under (V_{mpp}, P_{mpp}) operation.

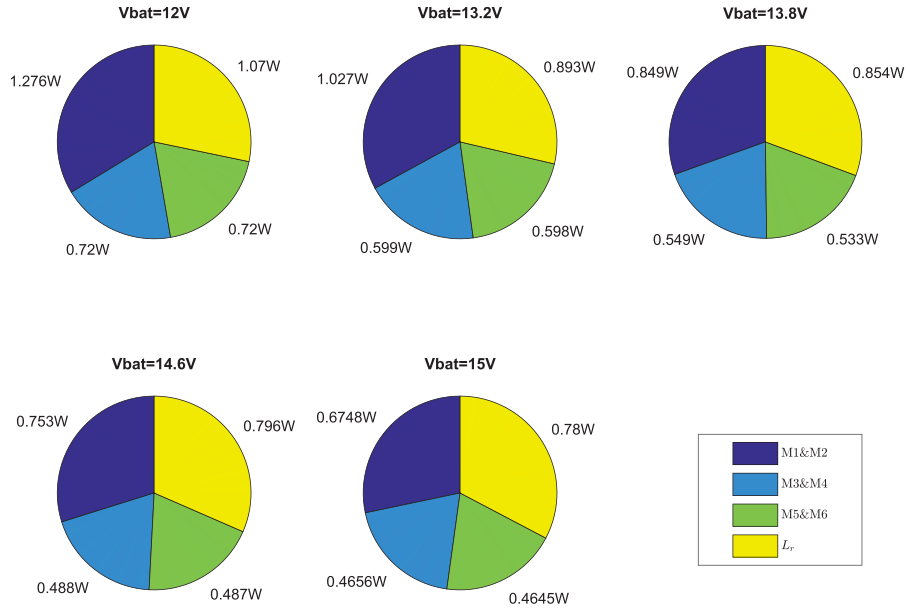


Figure 4.11: Power loss breakdown for the key components versus battery voltage under (V_{mpp}, P_{mpp}) operation.

higher. Besides, low battery voltage and higher current also leads to higher conduction losses. The accumulative higher losses for the MOSFETs and the inductor under lower battery voltage results in the worst case scenario for power loss and efficiency. Fig. 4.12 presents the proposed topology efficiency as the ratio between the battery charging power and the MPP power in %. It is clear that under lower battery voltage; where, the power losses of the MOSFETs and inductor

are at their worst case, the efficiency is at its minimum. The increase in the battery voltage at the same charging power results in higher MPPT efficiency.

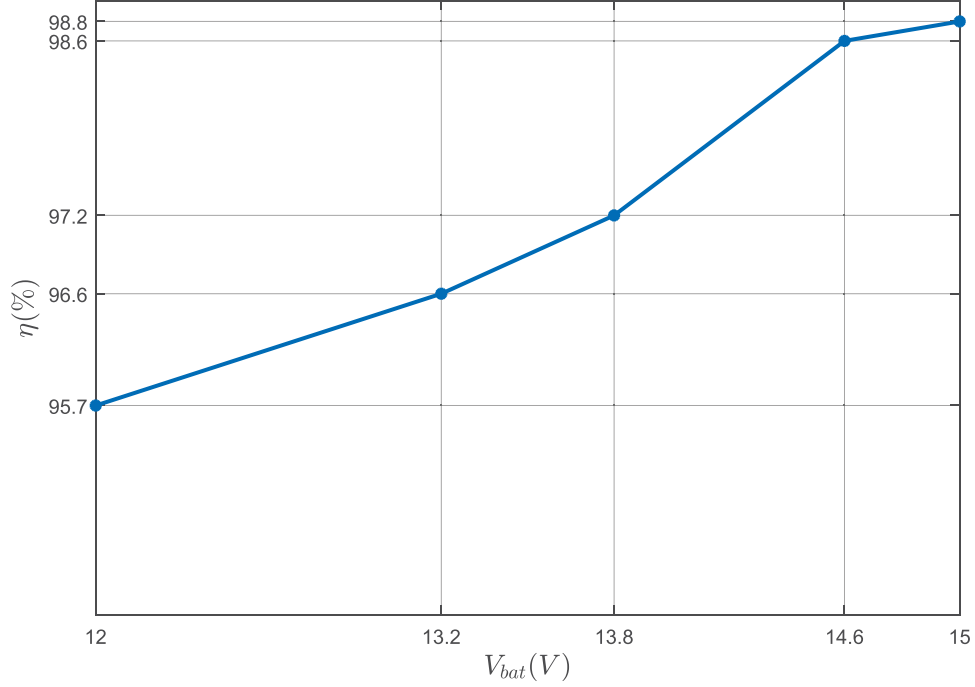


Figure 4.12: Proposed topology efficiency versus battery voltage under $(V_{mpp}, P_{mpp}) = (35.5V, 145.5W)$ condition.

In order to validate the time domain analysis presented in Section 3.3, the LTspice simulation with the same parameters given in Table 4.2 at $V_{bat} = 13.2V$ is conducted. Fig. 4.13 depicts the gate-sources driving signals for M_1 - M_6 MOSFETs; where, the waveform for the high-side MOSFET of each leg is in blue color and the low-side one is in red color. It should be noted that the driving voltage supply of 5V is assumed; where, also a dead time of 90ns between the gate-to-source signals of the MOSFETs belonging to the same leg is introduced to prevent the shoot through across the leg. It could be also seen that the ZCS time delay is introduced between the rectification stage and the inverting stage driving signals. The time delay equivalent to the $\varphi_1 = 32.21deg$ is $t_{delay,SR} = 725ns$ at $f_{sw} = 123.4kHz$.

To further validate the proposed topology operation and its time-domain analysis, the voltage at node 'c', the voltage between nodes 'a' and 'c', voltage across the resonant inductor and its current waveforms are depicted in Fig. 4.14. It could be seen from the voltage at node 'c' that the voltage at this node under the steady state condition does not exceed the V_{mpp} and does not reduce under the clamping diode forward voltage; hence, this voltage is not clamped in either of directions. This is because the switching frequency wrt the resonant frequency is high enough and the time domain analysis holds. On the other side, the voltage $V(a,c)$ as well as the inductor voltage and current follow the expected performance as presented in Section 3.3. It worth to note that the inductor current amplitude under the MPP condition and $V_{bat} = 13.2V$ is 15.8A.

As mentioned before the SR time delay is introduced between the gating signals for the SR stage MOSFETs wrt the inverting stage MOSFETs. This means MOSFETs M_3 & M_6 turn OFF with a delay of $t_{delay,SR} = 725ns$ wrt the turn-OFF time for M_1 . This time delay assures that

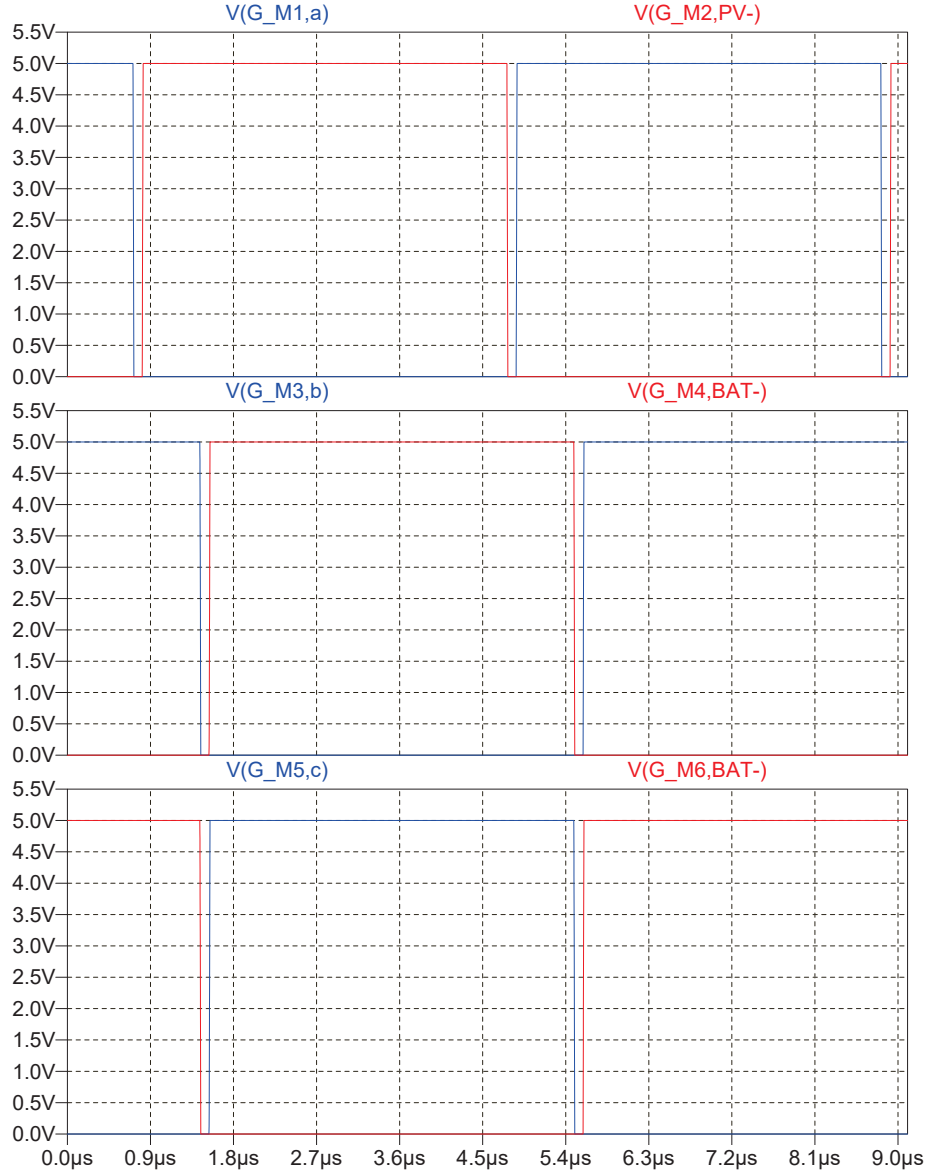


Figure 4.13: Gate drive signals for M_1 - M_6 under $(V_{mpp}, P_{mpp}, V_{bat}) = (35.5V, 145.5W, 13.2V)$ simulation condition. Note: y-axis is in volt and x-axis is in μSec

SR MOSFETs turning-off transition is under ZCS or very low currents minimizing the turn-off switching losses for this MOSFETs. Note that the drive signals M_4 and M_5 are complementary to M_3 and M_6 , respectively. Fig. 4.15 depicts the voltage at the input of the SR stage along with the currents for M_3 and M_4 . It is obvious that M_6 current is the same as M_3 carrying the positive half cycle of the resonant inductor current; while, M_5 current is the same as M_4 conducting during the negative half cycle. It could be seen from Fig. 4.15, during the dead time

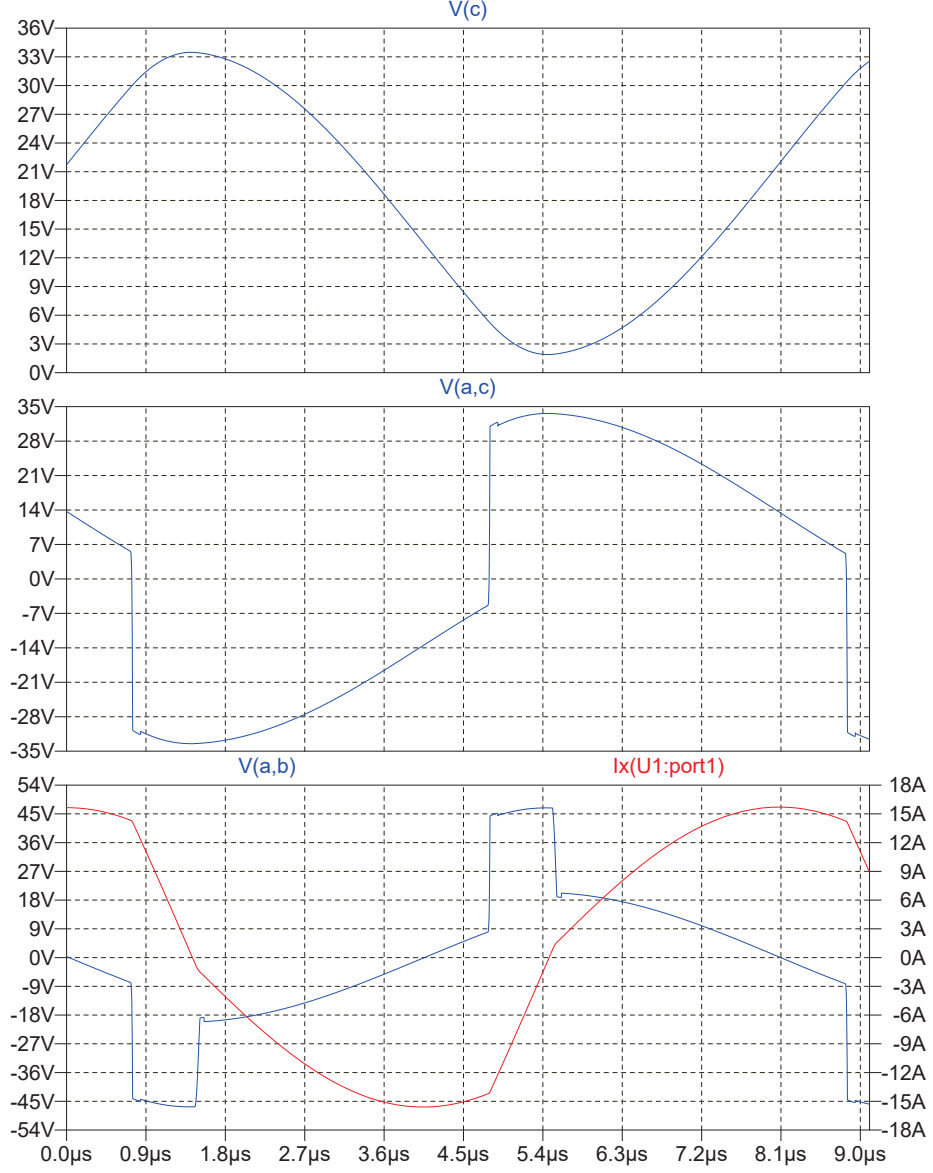


Figure 4.14: Waveforms for node 'c' voltage ($V(c)$), voltage between nodes 'a' and 'c' ($V(a,c)$), voltage across resonant inductor ($V(a,b)$), and the inductor current ($I_x(U1:port1)$) under $(V_{mpp}, P_{mpp}, V_{bat}) = (35.5V, 145.5W, 13.2V)$ simulation condition.

when the body diodes of the SR MOSFETs are ON, the voltage $V(b,c)$ is clamped at $V_{bat} + 2V_{FM}$ or $-(V_{bat} + 2V_{FM})$; where, V_{FM} is the forward voltage drop for the SR MOSFETs body diode. It could be also noticed from this figure, neglecting the voltage drop across the SR MOSFETs channel, during the time intervals other than the dead time, $V(b,c)$ is clamped at V_{bat} (when M_3 & M_6 are ON) and $-V_{bat}$ (when M_4 & M_5 are ON).

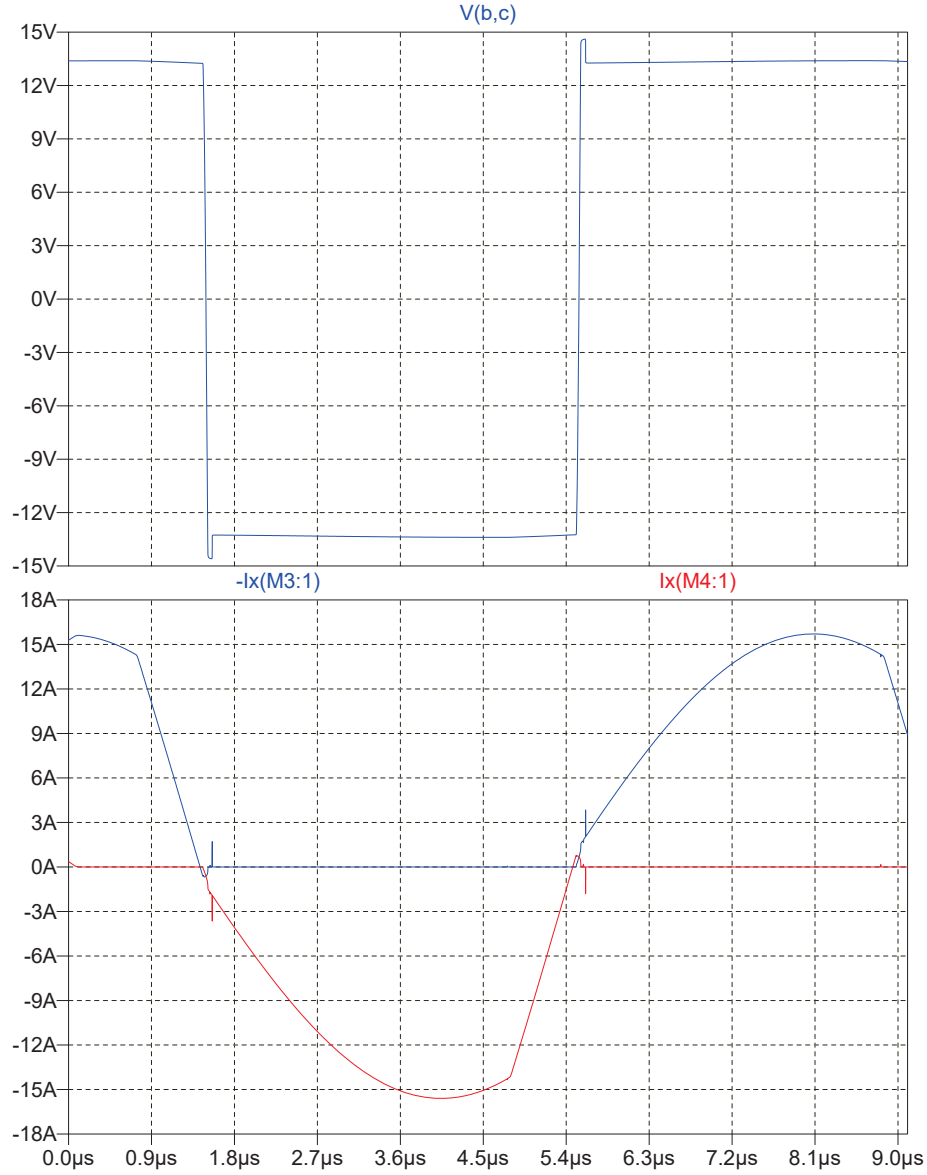


Figure 4.15: Waveforms for voltage between nodes 'b' and 'c' ($V(b,c)$), and SR MOSFETs M_3 & M_4 currents ($-I_x(M3:1)$ and $I_x(M4:1)$) under $(V_{mpp}, P_{mpp}, V_{bat}) = (35.5\text{V}, 145.5\text{W}, 13.2\text{V})$ simulation condition.

4.3.2 Closed-Loop Simulation Results and Analysis

As presented in Section 3.4 different closed-loop control strategies could be utilized for the proposed resonant battery charger. Based on the PV (V_{mpp}, P_{mpp}) operation condition, the MPPT control strategy should extract P_{mpp} from PV while maintaining its voltage at V_{mpp} . Since the MPPT

algorithm for the proposed topology is based on the frequency modulation, the algorithm adjust the switching frequency until it reaches the maximum PV power at V_{mpp} . As long as the battery voltage is less than the voltage control (VC) switch-over limit (defined as $V_{bat,max}$) the MPPT control is maintained. Once the battery voltage surpasses $V_{bat,max}$, the controller changes to VC mode and the VC control gradually charges the battery to its charging cut-off voltage (defined as $V_{bat,cut-off}$). Fig. 4.16 presents the desired charge profile for the battery incorporating both MPPT and VC mode control. The controller operation include multi-steps as described below:

1. As long as the battery voltage is less than the $V_{bat,max}$, the controller is in MPPT mode; where, by adjusting the switching frequency the maximum power based on the irradiance condition will be harvested.
2. If the battery voltage reaches the maxim set point, the controller will be changed to the VC mode; where, the voltage is regulated to the point that keeps the battery voltage under the charging cut-off limit. In this condition the harvested power might not be the max available power
3. If the battery voltage reaches the cutoff voltage, the controller should stops the switching to prevent the battery overcharging.

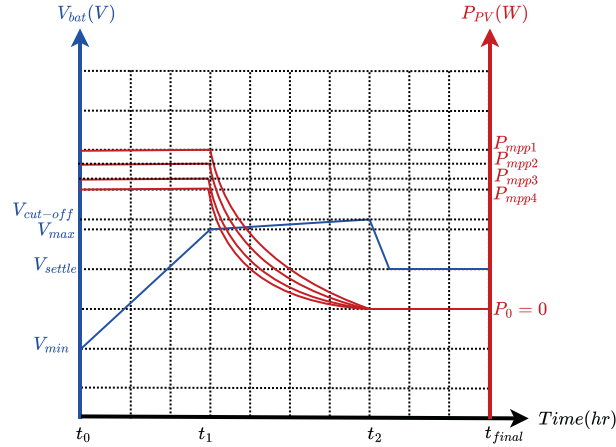


Figure 4.16: Desired battery charge profile under MPPT and VC mode.

The closed-loop simulation for the proposed topology is implemented in PSIM tool involving MPPT and VC controllers through frequency modulation. Furthermore, the simulation also implements both φ_1 for maintaining the SR MOSFETs ZCS, φ_2 as a PSM approach to further enhance the battery charging power controllability. This section presents closed-loop simulation results to evaluate the performance of the presented control approaches for the proposed topology. Fig. 4.17 present the high level control logic that decides between the MPPT and VC control modes.

• Closed-loop MPPT simulation results and analysis for the proposed topology

Different MPPT control algorithms were presented in Section 3.4.1. The HC MPPT algorithm along with the CV control loops are implemented in PSIM, the output of the control loops

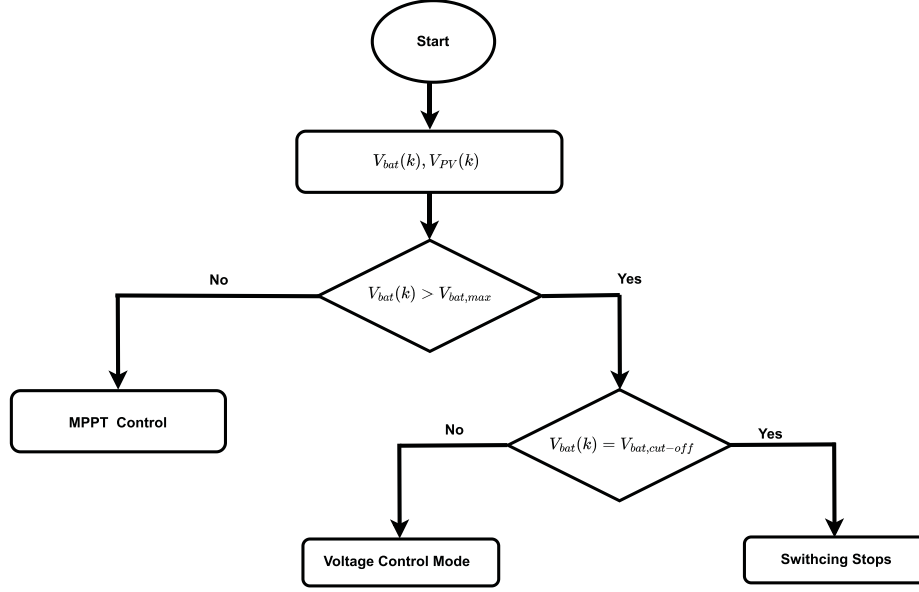


Figure 4.17: High level logic to switch between different control modes in the closed loop simulation.

is provided to the frequency modulation block; where, the gate signals for the inverting stage MOSFETs and the SR stage MOSFETs with the associated φ_1 and φ_2 are generated. These signals are then provided to the MOSFETs gate drivers.

Fig. 4.18 presents the power stage of the closed-loop schematic for the proposed topology in the PSIM tool. This stage include the PV panel at the input side; where, both PV voltage and current are also sensed for the feedback purpose to the controller. The PV is followed by bypassing capacitors $C_{i1} - C_{i3}$ for filtering the AC component of the input current and then the half bridge (Q_1 & Q_2) DC-to-HFAC and the diving capacitor with their clamping diodes. It could be also seen that the resonant inductor (L_r) current is also sensed as i_{tank} , this current could be utilized for zero crossing detection. The SR stage MOSFETs ($Q_3 - Q_6$) are followed with bypass capacitors $C_{o1} - C_{o3}$ to filter the AC component of the rectified current followed by a small values inductor (e.g. 150nH) to represent the impedance of wires used for connecting to the 4-cell Li-ion battery. Note that the battery voltage and current are acquired as feedback signals to the controller. All 6 MOSFETs $Q_1 - Q_6$ receive their gate driving signal followed with a block representing their gate driver stage.

The MPPT algorithm could be implemented using available blocks in the PSIM tool box. Fig. 4.19 depicts the MPPT implementation for the proposed topology along with the driving signal ($V_{gs1} - V_{gs6}$). generation in the PSIM tool. It could be seen from this figure, that the PV voltage and current are first passed to low-pass filter (LPF) blocks for filtering the high frequency noise from these signals. The filtered V_{PV} and I_{PV} are then used for deriving the PV power. Using zero-order hold (ZOH) and delay blocks, the calculated power samples k &($k - 1$) are extracted. The PV power current value and last value are then compared to identify if it is increasing or decreasing; hence, subtracting or adding incremental time step to the switching cycle, respectively.

A limiting block is used to define the minimum and maximum allowable switching frequency.

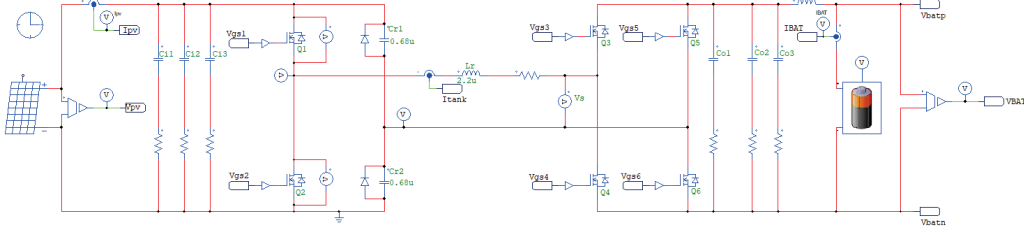


Figure 4.18: Simulation power stage schematic in PSIM environment.

The minimum limit on the switching frequency provides an inductive operation margin to guarantee the ZVS for Q_1 & Q_2 , and the maximum value is defined as a limit that under start-up condition or transition from heavy load to the light load the switching frequency does not exceed this limit. It could be also seen that the result of the frequency modulation (i.e. derived f_{sw}) is provided to an square-wave generator for generating the complementary gate signals for Q_1 & Q_2 with a pre-defined dead time.

As mentioned earlier the ZCS phase φ_1 is introduced to minimize the turn-OFF switching losses for the SR MOSFETs $Q_3 - Q_6$. The time delay blocks equivalent to the required φ_1 are utilized to generate delayed complementary V_{gs3} & V_{gs4} . Similarly using time delay blocks φ_2 is implemented for the complementary V_{gs5} & V_{gs6} . Note that in the case when $\varphi_2 = 0$, V_{gs6} and V_{gs5} are in-phase with V_{gs3} and V_{gs4} , respectively.

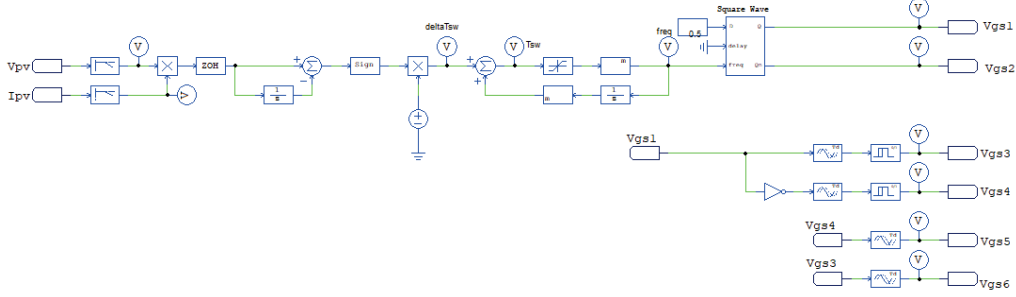


Figure 4.19: MPPT algorithm and gate driving implementation in the PSIM schematic environment.

The PSIM simulation is conducted by assuming a solar irradiation condition that results in $(V_{mpp}, P_{mpp}) = (35.5V, 145.5W)$, and an initial battery SOC of 5%. Table 4.3 provide the parameters used for the closed-loop simulation in PSIM. Fig. 4.20 shows the gate signals for $Q_1 - Q_6$. The dead time between the complementary gate signals for the MOSFETs belonging to the same leg is set at 90ns. The gate signals show a time delay between V_{gs3} wrt the V_{gs1} that corresponds to the required ZCS delay, while the delay between V_{gs6} and V_{gs3} is zero, meaning no φ_2 is introduced. Note that these signals are logic level and are provided to gate driving stage for level shifting and driving the gate-to-source of the MOSFETs.

As mentioned before, a switching frequency limiting block is utilized in the PSIM simulation. The limits are intended to guarantee the inductive operation by setting a minimum switching frequency higher than the resonant frequency of the LC tank; while, the higher 500kHz limit is also limiting the maximum switching frequency during the converter start-up or transition from a high charging power to lower charging power. Note that the 500kHz maximum limit on the

Parameter	Value
V_{mpp}	35.5V
P_{mpp}	145.5W
battery initial SOC	5%
L_r	$2.2\mu H$
$C_1 = C_2$	$0.68\mu F$
MOSFETS $Q_1 - Q_6$, $R_{ds,on}$	$2m\Omega$
MOSFETS $Q_1 - Q_6$, V_{FM}	0.75V
clamping diodes V_{FD}	1V

Table 4.3: Parameters used in PSIM closed-loop simulation under MPPT control mode.

frequency is an operation condition with very low current; hence, the losses in the MOSFETs are minimal. Moreover, the minimum and maximum limits also provide a safe operation region for the proposed converter during the transient events. Fig. 4.21 depicts the switching frequency and PV output power. It could be seen at the start-up, when the PV voltage is at its open circuit voltage and the power is zero, the switching frequency is at 500kHz. The MPPT algorithm incrementally increase the switching cycle translating to reducing the switching frequency from its maximum limit. As the switching frequency continues to decrease the PV power is gradually increasing until it reaches its MPP level. During the steady-state the switching frequency is maintained at a level that maximum power is extracted from the PV. Note that the average steady state switching frequency for this operation condition is $114.3kHz$ at an MPP of $143W$. Note that there is about 1.7% steady-state error in MPPT; however, this error could be further reduced with more computationally intensive MPPT algorithms.

Fig. 4.22 presents the voltage at node 'a' of the proposed topology along with the resonant inductor current. As it could be seen from this figure, the high-side MOSFET of the inverting stage turns off while the inductor current is still positive. This means that the current is lagging the voltage; hence, an inductive impedance provides guaranteeing the ZVS operation for Q_1 & Q_2 . Since at the time when Q_1 turns off the current still is substantially positive, this current provides enough energy for the inductor to charge the C_{oss} of Q_1 and discharge C_{oss} of Q_2 . After this transition the body diode of Q_2 turns on while the inductor current is still positive. The last step is turning ON Q_2 while its body diode is still On, resulting in ZVS for this MOSFET. The negative half cycle operation is symmetrical to the positive cycle with Q_1 turning ON under ZVS.

It also could be seen from Fig. 4.22 that due to the high frequency operation condition the voltage at node 'c' of the proposed topology is sinusoidal and does not clamp. This figure also shows the inductor current and the voltage v_s at the input of the SR stage. It could be seen that the zero crossing of the current coincides with the SR MOSFETs transition time between ON to OFF resulting in ZCS for these MOSFETs. Note that for this operation condition the ZCS time delay is $t_{delay,SR} = 535ns$.

Fig. 4.23 shows the battery voltage, current and charging power. It could be seen at the start up as PV power begins to increase, the battery charging current and power also ramp up from zero; however, the battery voltage begins from a level corresponding to its SOC as expected. While the switching frequency decreases corresponding to the increase in the PV power the battery charging power also increase until it reaches a steady state level equivalent to $P_{bat} = \eta * P_{mpp}$. For this simulation case the steady state efficiency is $\eta = P_{bat}/P_{mpp} = (140.8/143) * 100 = 98.46\%$.

It should be noted that one of the goals for the closed-loop simulation is to validate that the ZVS and ZCS operation conditions in the steady-state operation condition are maintained. From the presented closed loop simulation it is proved that the ZVS for Q_1 & Q_2 and the ZCS for

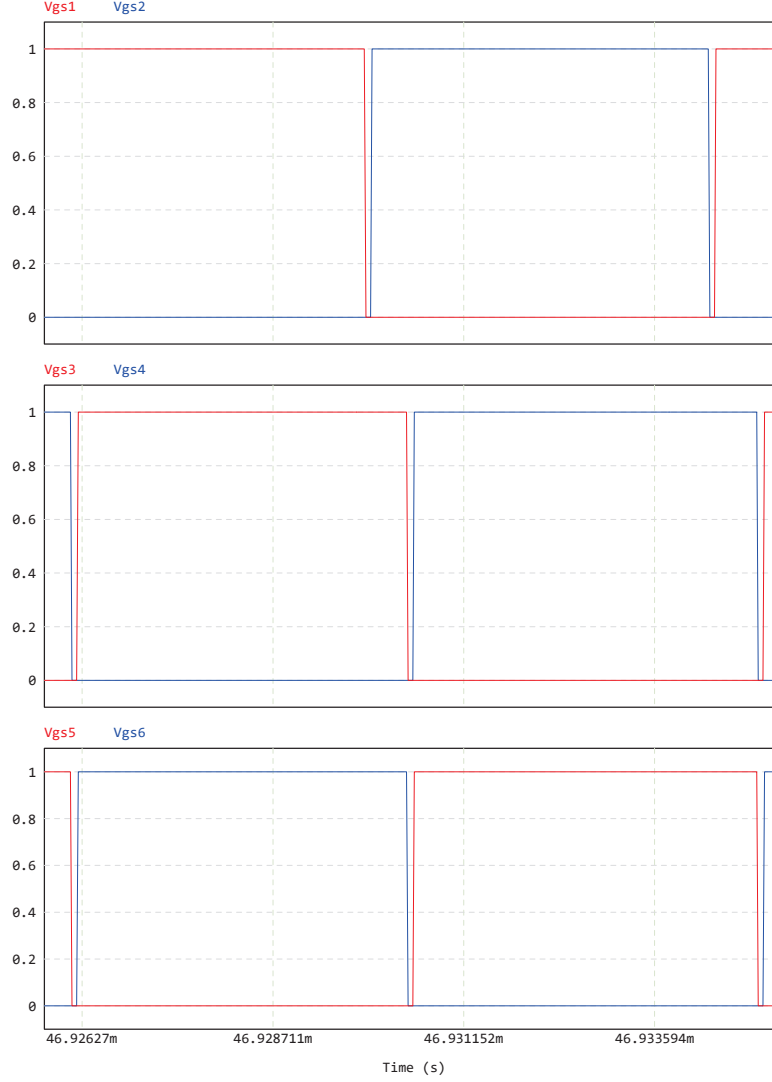


Figure 4.20: Closed-loop MPPT controller simulation results for MOSFETs logic level driving signals.

$Q_3 - Q_6$ are confirmed. The guaranteed soft-switching for the MOSFETs means that the dominant power loss of the MOSFETs for the proposed topology is their conduction loss. This means that if the power loss associated with the MOSFETs body diode during dead time are neglected the MOSFETs conduction loss could be simply estimated by $P_{loss,Q_1-Q_6} = R_{dson,Q_1\&Q_2} * I_{L,rms}^2 + 2 * R_{dson,Q_3-Q_6} * I_{L,rms}^2$. In this estimation the inverting MOSFETs are identical and similarly all the SR MOSFETs are also identical. If all $Q_1 - Q_6$ are identical with the ON state resistance of R_{dson} , the MOSFETs conduction loss is simply $P_{loss,Q_1-Q_6} = 3 * R_{dson} * I_{L,rms}^2$. For a more accurate estimation of the MOSFETs power loss, the losses during the dead time could also be included.

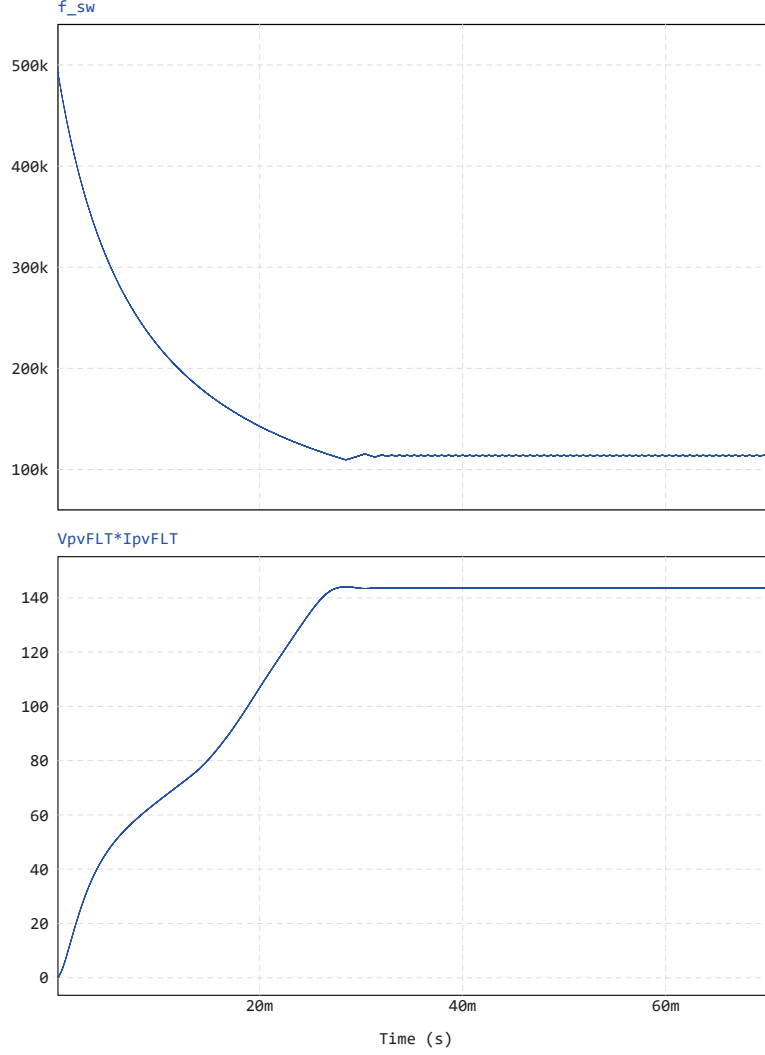


Figure 4.21: Closed-loop MPPT simulation results for switching frequency and PV power $(V_{mpp}, P_{mpp}) = (35.5V, 145.5W)$.

Another main cause of the power loss in the proposed topology is the resonant inductor. The inductor losses include core loss and conduction loss; where, both are a function of the switching frequency. The core loss could be simply estimated using $P_v = K_e * f_{sw}^\alpha * B_{peak}^\beta$ [34, 35]. In this equation K_e , α , and β depend on the core material and mechanical size usually provided by the core manufacturer; while, f_{sw} and B_{peak} depend on the topology and its operation. Note that the core loss equation is valid under sinusoidal excitation; however, since the inductor current for the proposed topology is very close to a sinusoid the core loss calculation still provide close estimation. The conduction loss associated with the inductor is a function of its AC resistance (ACR) at the operating switching frequency that originates from the skin effect and the proximity effect of the inductor winding [36, 37, 38]. Selecting a flat wire inductor could potentially minimize these

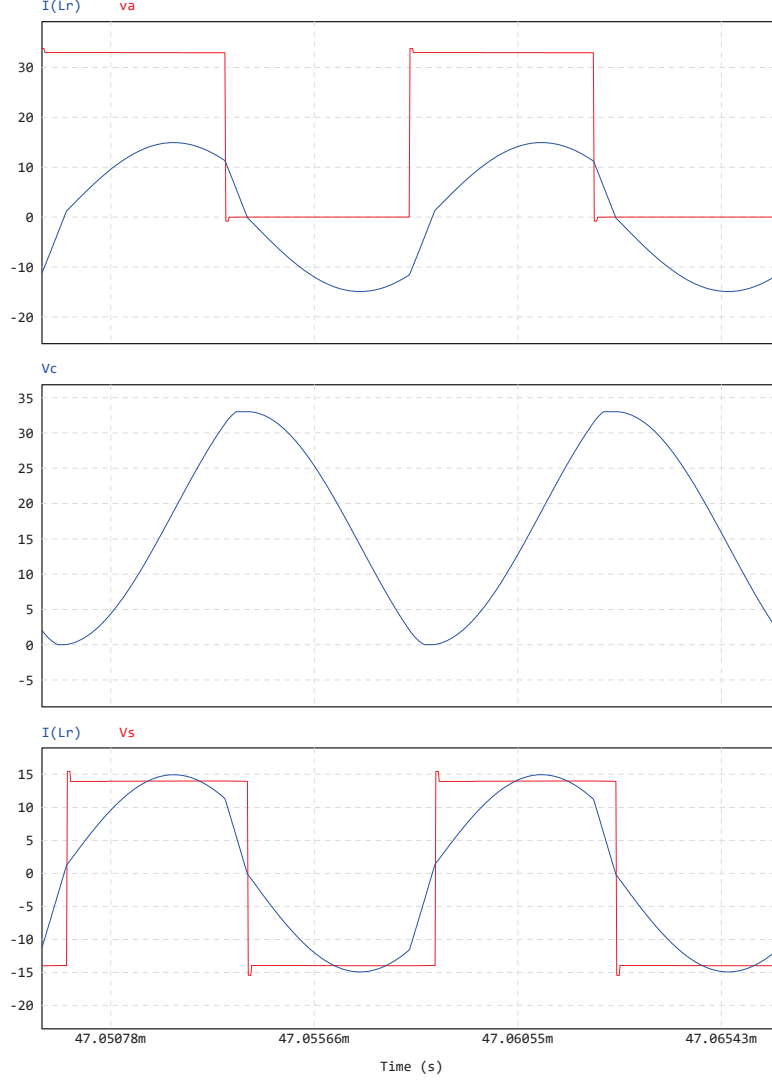


Figure 4.22: Closed-loop MPPT simulation results for switching node, dividing capacitor node, and SR-stage input voltages along with the resonant inductor current.

effects by reducing the proximity effect where with a thin flat wire (thinner than the skin depth), the skin effect related ACR increase could also be minimized.

Defining the inductor loss as $P_{loss,L} = P_v + ACR * I_{L,rms}^2$, the major portion of the power loss for the proposed topology is estimated using $P_{loss} = P_{loss,Q1-Q6} + P_{loss,L}$; hence, the efficiency could be simply estimated by $\% \eta = ((P_{mpp} - P_{loss}) / P_{mpp}) * 100$. Alternatively different closed-loop simulation with different parameters for the inductor and MOSFETs could be run to derive multi-data-point efficiency. In order to select proper MOFETs and inductor across different manufacturer a through efficiency analysis with different part numbers is presented in Chapter 5.

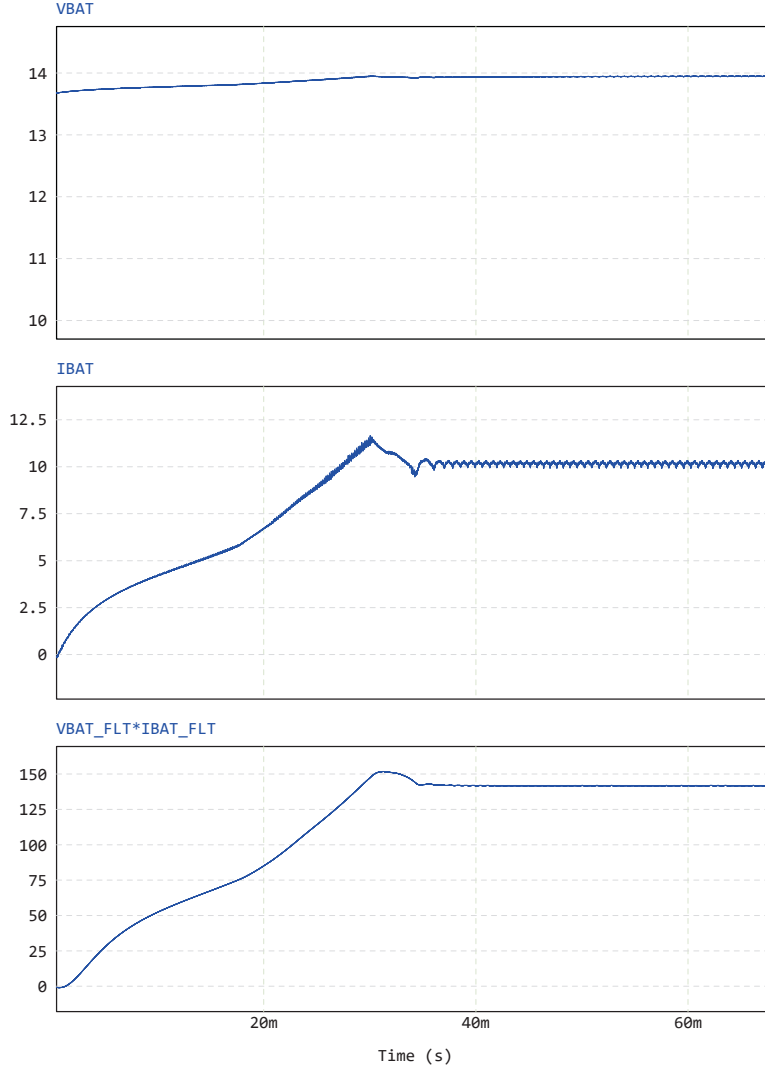


Figure 4.23: Closed-loop MPPT simulation results for battery voltage, current, and charging power.

• **Closed-loop MPPT to VC mode switch-over simulation results and analysis for the proposed topology**

As describe before, as long as the battery voltage is less than the $V_{bat,max}$ it is reasonable to operate the proposed topology for extracting the maximum available power from the PV panel; however, once the battery voltage passes a certain limit in order to provide a more controlled battery voltage "topping-off" and prevent the overcharge the controller changes to a VC mode. Fig. 4.24 shows the VC integration with the MPPT within the PSIM closed-loop simulation. Note that in order to prolong the battery life time the final stage of the charging usually from 80% – 100% SOC (also referred to as topping-off) the constant voltage control should be utilized

[39, 40].

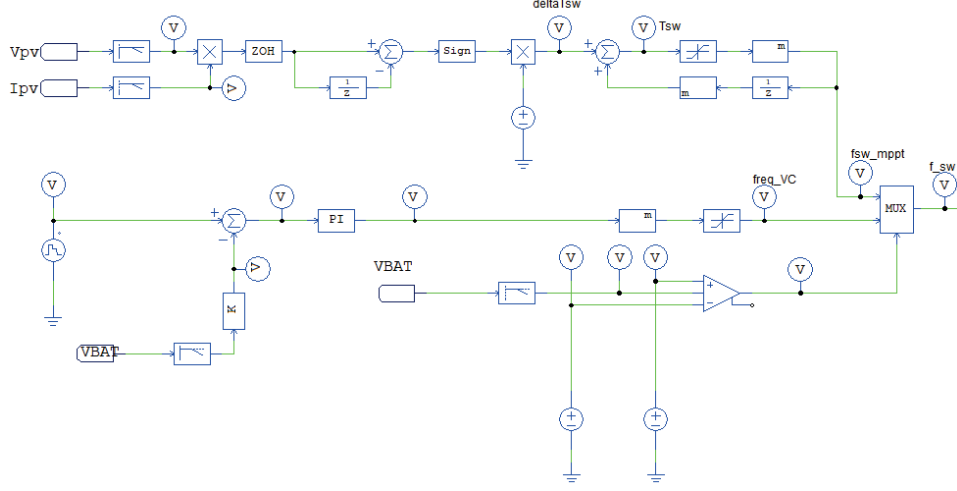


Figure 4.24: Integrating MPPT and VC controllers in the PSIM schematic environment.

The MPPT algorithm is already described; however, to integrate the VC mode, the battery voltage feedback is first applied to an LPF to filter the high frequency voltage ripple cause by voltage across the battery cells series resistance. Then a gain is applied to scale down the battery voltage to the same level as its reference. The error between the feedback signal and its reference is then applied to the input of a proportional-integrator (PI) compensator; where, its output is defined as the switching cycle and converted to the frequency. Similar to the MPPT frequency modulation, the same maximum and minimum limits are also applied to the modulated switching frequency at the output of the VC scheme. A hysteresis boundary range is defined for the $V_{bat,max}$ to prevent oscillation during the controller mode switch over; hence, when the battery voltage passes its limit the switching frequency applied to the pulse generator will be the output of the VC with an smooth transition.

Note that in order to provide an smooth transition along with preventing the voltage gain violation, the initial switching frequency for the VC mode could be placed slightly higher than the last switching frequency from MPPT. In this way, the PV operation point moves towards the right side of the PV MPP operation condition, meaning the PV voltage moves its operation point between V_{mpp} and V_{OC} ; hence, maintaining needed higher PV voltage when the battery voltage is also at higher values.

Fig. 4.25 presents the simulation results for the integration of the MPPT and VC mode. It could be seen at the start up, when the battery voltage is lower than the $V_{bat,max} = 14.917V$, the controller is in MPPT mode and the switching frequency reduces gradually from its maximum 500kHz to an average of 115.25kHz at the steady state. During this transition the PV power increases from zero to its MPPT operation condition. A control flag is introduces so that when the battery voltage exceeds $V_{bat,max} = 14.917V$, the controller switches over to the VC mode. It could be seen from the simulation results that when the controller changes to the VC mode the switching frequency is re-modulated and as the charging continues the battery voltage is topping off to higher values. It should be noted that if the battery voltage reaches $V_{bat,cutt-off} = 16.8V$, the charging stops.

It is expected that as the switching frequency reduces during the start-up transition the PV power increases as it does the battery charging power. Fig. 4.26 depicts the control flag along

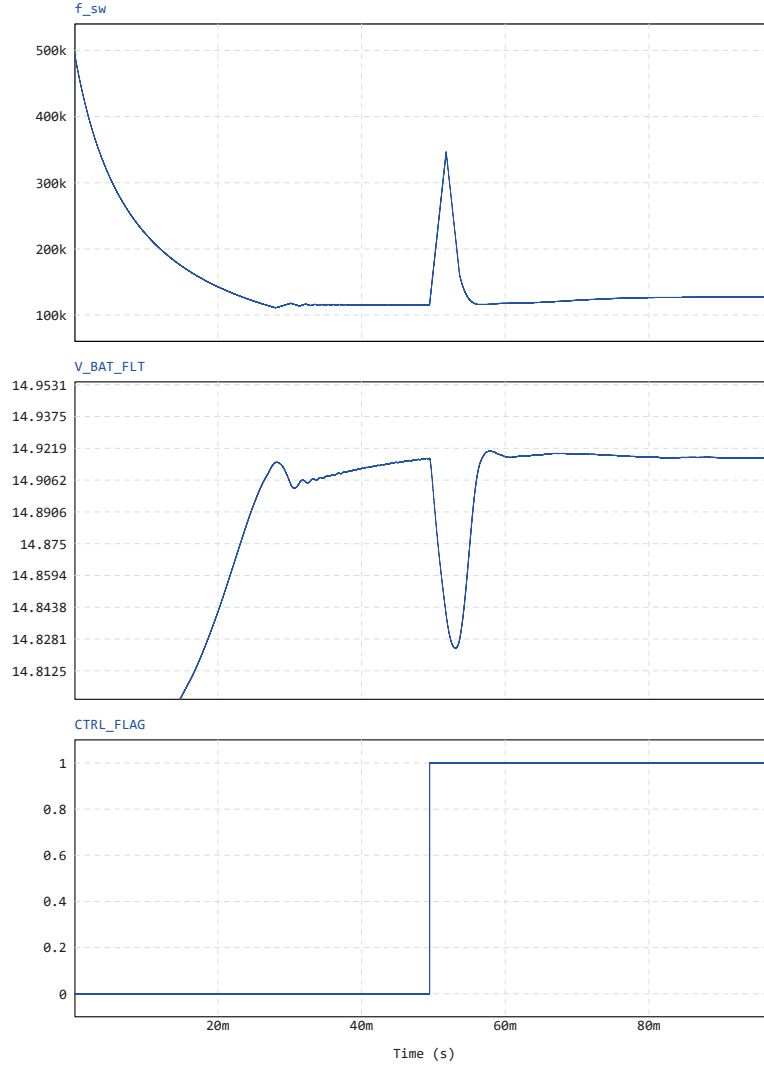


Figure 4.25: Closed-loop MPPT and VC mode simulation results for switching frequency and battery voltage.

with both PV and battery charging powers. As it could be seen from this figure the PV power increases towards its steady state value at 143W. During this time the battery charging power also increases to an average of 140.8W. When the battery voltage passes $V_{bat,max} = 14.917V$ corresponding to the state change of the control flag, as the controller changes to VC mode, the switching frequency is regulated by the VC controller and the PV power in steady state reaches 140W. The battery charging power also settles at 143.8W resulting in an efficiency of 98.78%.

Similar to the MPPT control mode, it is expected that under the VC mode also the ZVS and ZCS condition for the inverting stage and SR stage MOFETs, respectively, to be maintained. 4.27 shows the inductor current along with the node 'a' voltage and the voltage at the input of the

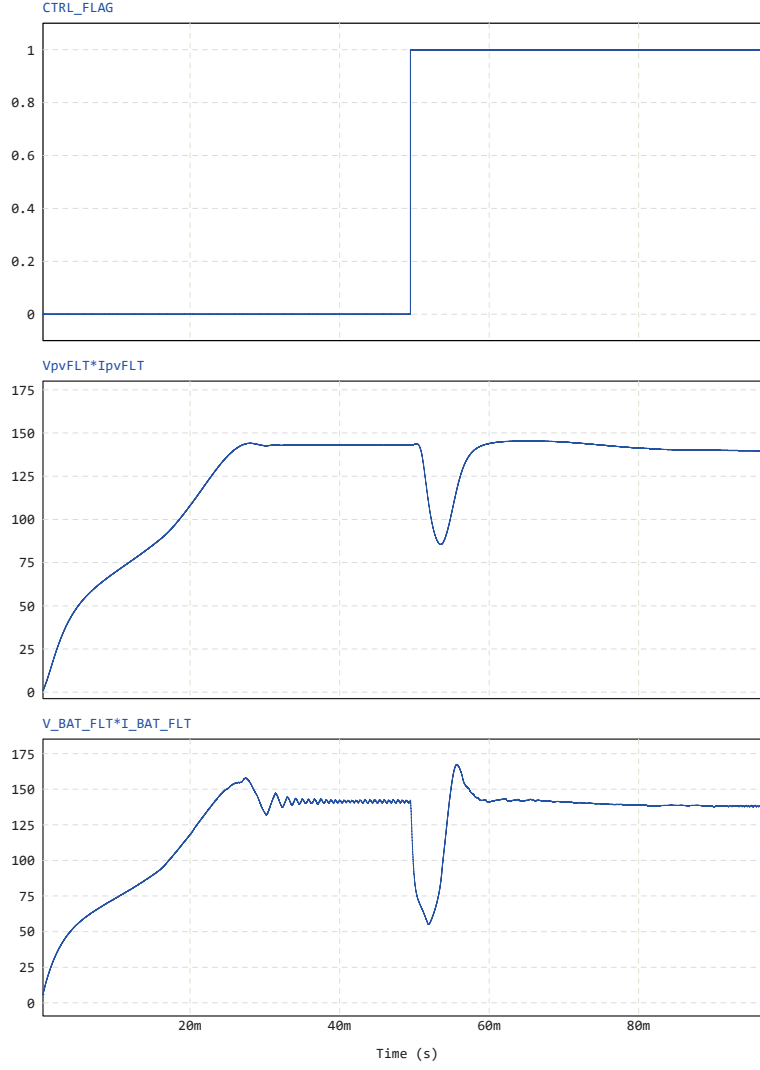


Figure 4.26: Closed-loop MPPT and VC mode simulation results for PV and battery charging powers.

rectification stage (v_s) under steady-state conditions. This figure also includes the steady-state voltage at the node 'c' of the proposed topology. It could be seen from this figure that both ZVS for MOSFETs Q_1 & Q_2 and the ZCS for MOSFETs $Q_3 - Q_6$ are maintained, as intended. It could be also seen that the high frequency operation condition for the v_c is also valid.

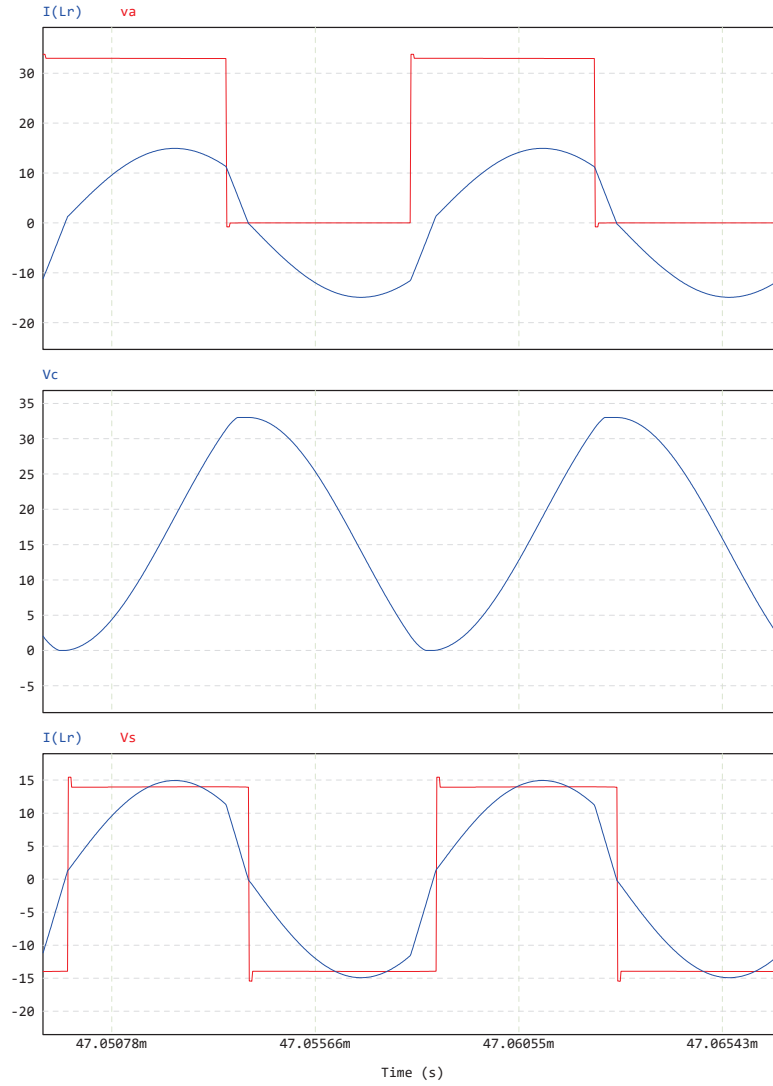


Figure 4.27: Closed-loop MPPT and VC mode simulation results for switching node, dividing capacitor node, and SR-stage input voltages along with the resonant inductor current.

Chapter 5

Components Selection, Schematic Development, and PCB Layout Design

5.1 Power Domains Definition for the Schematic and PCB Layout

In order to develop the schematic and PCB layout for the proposed DC-DC battery charge, different power and grounding domain should be first defined and then according to these domains the requirements for component selection are specified. Defining the ground and power domain depend on the proposed topology and the intended control strategy. From Fig. 3.10 it is evident that there are two main power/grounding domains, namely PV domain and battery domain. On the other side, from the control architecture in Fig. 3.25 and Fig. 3.26 it could be seen that different signals from both PV and battery domains as well as the resonant inductor should be sensed for the purpose of the feedback control. The sensed signals then will be provided to the ADC inputs of a micro-controller unit(MCU) evaluation board. This implies that a third power/grounding MCU domain is required as a common domain for all the sensed and feedback signals. Fig. 5.1 depicts the block diagram for the three domains along with the isolation barrier between the PV and battery domain wrt the MCU domain. This means isolation is needed before the sensed signals V_{PV} , I_{PV} , V_{bat} , I_{bat} , and i_{L_r} are provided to the ADC inputs of the MCU, as it could be seen in this figure.

5.2 Schematic Functional Circuit Blocks and their Components Selection

In this section, different functional circuit blocks of the designed schematic in Altium Designer are presented along with a detailed description of each block. The considerations and criteria for selecting the key components of each block are also presented. This involves comparative simulation results analysis for the key components. According to the circuit operation and intended design functions, the schematic could be divided into 5 main functional circuit blocks, namely:

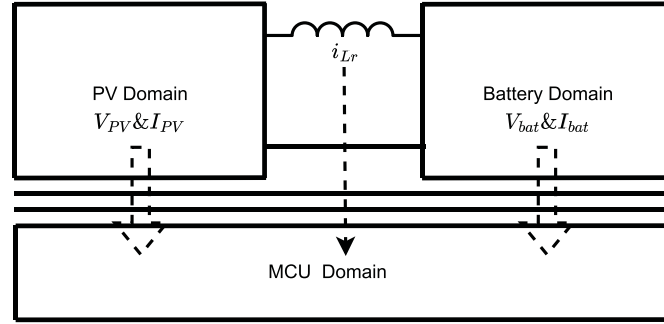


Figure 5.1: Block diagram for the schematic power/grounding domains.

1. Power Stage
2. Auxiliary Power Supply
3. Gate Drive
4. Sensing Circuits
5. MCU Interface

The following sub-sections provide the detailed description of each circuit block and their component selection process. Since the designator assigned to each component in the Altium Designer tool does not include a sub-script for the numbering (e.g., C_1 rather than C_1), when referring to a component in the designed schematic, through out this chapter the same convection is used.

5.2.1 Power Stage

The core part of every power converter is the power stage, where the power conversion happens and provided to the intended application load. Depending on the desired application and its specification, the power stage topology would be different. The power stage for the proposed topology of Fig. 3.10 is implemented in Altium Designer as shown in Fig. 5.2. This functional circuit block consists of:

- Inverting stage half-bridge MOSFETs $M1 - M2$, and the SR-stage MOSFETs $M3 - M6$.
- Resonant tank consisting of the dividing capacitor $C15$ & $C30$ and the inductor $L2$.
- Clamping diodes $D1$ and $D2$.
- Switching stage bypass capacitors on PV side ($C4 - C8$ & $C20 - C24$) and battery side ($C4 - C8$ & $C20 - C24$)
- The shunt resistor $R1$, for measuring the battery charging DC current.
- Connectors $J1$ & $J2$, used as an interface to connect the PV panel and battery module at the input and output of the printed circuit board assembly (PCBA).
- The varistor $VR1$, intended for protecting the input stage against transient events.

- EMI filter consisting of the capacitors $C1$ - $C3$ & $C14$, and the common mode choke $L1$.

Each of these components require the selection criteria specific to their role within the intended functional circuit block. Their function also dictates the required specification for each part.

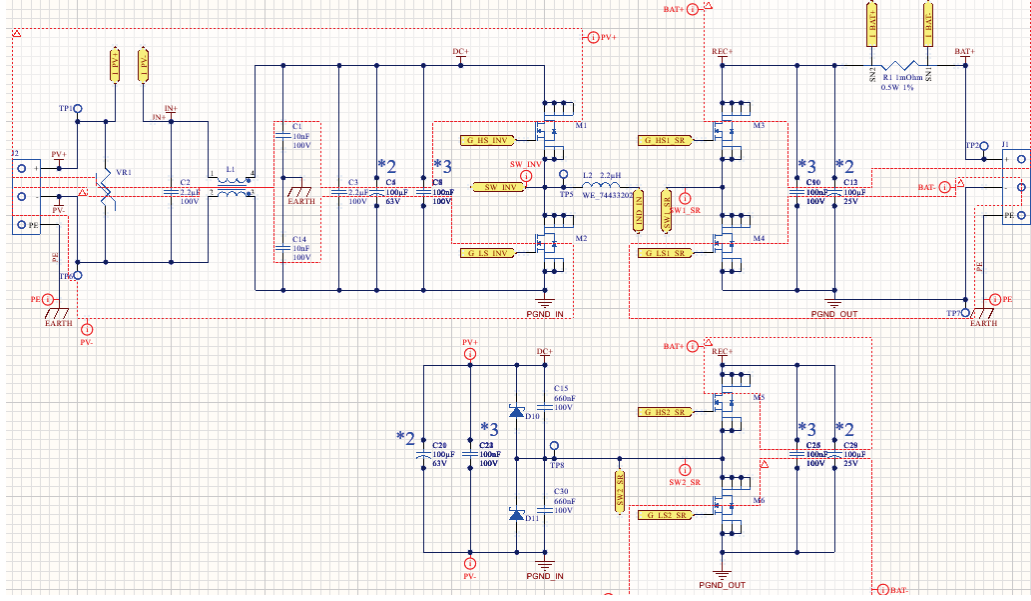


Figure 5.2: Power Stage schematic.

MOSFETs $M1$ - $M6$: As it could be seen from Fig. 5.2, $M1$ & $M2$ are the inverting stage HB MOSFETs for converting the PV DC voltage to the HFAC voltage; while, the FB SR stage MOSFETs $M3$ - $M6$ are utilized for converting the HFAC voltage to the DC voltage for charging the battery.

Different parameters in selecting these MOSFETs should be taken into consideration; where, each parameter has specific implication on the performance of the DC-DC battery charger. The PV and battery voltages dictate the minimum required rated drain-to-source voltage V_{ds} for the MOSFETs. The OFF-state V_{ds} along with the other MOSFET parameters including their ON-state resistance ($R_{ds,on}$), required driving gate-to-source voltage (V_{gs}), and their parasitics input and output capacitances determines the MOSFETs power losses; hence, affecting the DC-DC battery charger efficiency. Note that the main effect of the gate driving voltage V_{gs} manifests on the MOSFET $R_{ds,on}$; therefore, affecting its conduction losses [41]. The higher the V_{gs} is (within the manufacturer's recommended operation range), the lower the $R_{ds,on}$ is, resulting in lower MOSFET conduction losses [42]. The OFF-state V_{ds} accompanied by parasitics input and output capacitances, on the other hand, affect the MOSFET switching transient; hence, their switching power losses.

It worth to note that the proposed topology and the switching scheme ensure the soft switching leading to a negligible switching power losses; hence, the MOSFETs main power loss component is their conduction loss. In order to select a MOSFET for meeting the target efficiency and cost for the resonant DC-DC battery charger, MOSFETs with different $R_{ds,on}$ are evaluated through a comparative open loop simulation in LTspice allowing to utilize their manufacturer's SPICE model for more accurate estimation of the power losses. Through this analysis the optimum range

for the MOSFET $R_{ds,on}$, to meet the target efficiency, is first identified; then, different MOSFETs within the desired $R_{ds,on}$ across multiple manufacturer are evaluated for cost optimization. The comparative efficiency and cost analysis allows an optimum selection for both performance and cost.

Table 5.1 provides the evaluated MOSFETs PN and their key parameters; where, $R_{ds,on}$ varies across different PNs. It should be noted that the change in $R_{ds,on}$ and C_{oss} among these MOSFETs implies that for the simulation of different MOSFETs the switching frequency and ZCS phase shift require adjustment to extract the 145.5W MPP from the PV for all cases. This provides a fair comparison for the effect of each MOSFET on the efficiency. Notice that for all of the MOSFET simulation cases a $2.2\mu H$ resonant inductor (L_r) with PN MSS1278T-222 is used.

PN	Rated $V_{ds}(V)$	$R_{ds,on}(m\Omega)$ at $V_{gs}(V)$	Cost/1kU (€)
TPH3R10AQM	100	3.1 at 10	0.72
TPH4R10ANL	100	4.1 at 10	0.71
TPH5R60APL	100	5.6 at 10	0.54
TPH6R30ANL	100	6.3 at 10	0.47

Table 5.1: List of evaluated MOSFETs and their parameters.

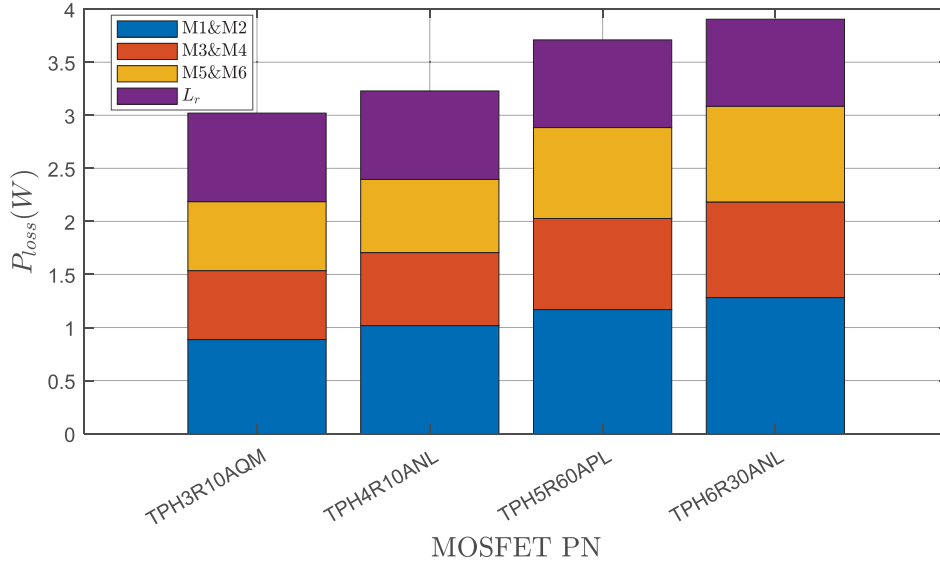


Figure 5.3: Accumulative power loss for the MOSFETs and resonant inductor.

Fig. 5.3 depicts the accumulative power loss for the MOSFETs and the resonant inductor; where, MOSFETs with different $R_{ds,on}$ are used. Note that for all cases the PV MPP voltage is at $V_{MPP} = 35.5V$, battery voltage is at $V_{bat} = 13.2V$, $f_{sw} = 123.4kHz$, and the ZCS phase shift is adjusted as such that the PV power is tracking the maximum point at 145.5W. It could be seen from this figure that for each pair of HB MOSFETs as the $R_{ds,on}$ increases the power losses also increases, as expected. On the other side, it could be seen that for each MOSFET PN, the accumulative power loss of HB MOSFETs for both HB legs of the SR stage are identical. Moreover, as the resonant inductor PN remains identical, under the same operation condition (V_{MPP} , V_{bat} , f_{sw} , P_{MPP}), its power loss remains constant across all simulation cases. Considering

the accumulative power loss and cost comparison, a MOSFET with an $R_{ds,on}$ close to $3.1m\Omega$ at $V_{gs}(V)=10V$ is acceptable. Table 5.2 shows a list of same rated MOFETs with the desired $R_{ds,on}$ range. As it could be seen from this table, the PN TPH3R10AQM from Toshiba provides the most cost effectiveness while meeting the maximum target power loss; hence, this PN is utilized in the designed schematic.

PN	Manufacturer	Rated $V_{ds}(V)$	$R_{ds,on}(m\Omega)$	Cost/1kU (€)
RBE029N10R1SZN6	Renesas	100	2.9	0.92
ISC030N10NM6ATMA1	Infineon	100	3	1.43
TPH3R10AQM	Toshiba	100	3.1	0.72
RJ2P14BBHTRDC	Rohm	100	2.8	1.98
NTMFS10N3D2C	onsemi	100	3.2	2.72

Table 5.2: Cost comparison for MOSFETs within desired $R_{ds,on}$ range from different manufacturer.

Resonant tank capacitors (C15 and C30): Selecting the resonant capacitors relies on defining the required specification for the proposed DC-DC battery charger application. On the other side, different parameters including temperature coefficient, rated voltage, as well as equivalent series resistance and inductance (ESR and ESL) of capacitors should be also taken into considerations. The design goal is to select a resonant capacitor that provides stability under different voltage and current stress.

Different capacitor technologies including the surface mount multi-layer ceramic capacitor (MLCC) and film capacitor are suitable for resonant application. The surface mount ceramic capacitors generally exhibit lower ESL with more compact packaging making them more suitable for the application in this thesis. Moreover, the dividing capacitor along with the resonant inductor define the resonant frequency; hence, dictating the switching frequency operation range for the proposed topology. This implies that minimal capacitance change to minimize the resonant frequency variation is desirable. Among all the ceramic capacitors the temperature coefficient C0G/NP0 provide highest stability in the capacitance drift across their entire operation temperature range [43, 44]. Note that under different battery charging power the current stress; hence, the operating temperature for the dividing capacitors varies, making the C0G/NP0 more suitable for the application in this thesis.

In order the select capacitors that provide the closest capacitance to the deigned value in Section 4.2, an array approach could be taken. Table 5.3 list multiple array options for the dividing capacitors. As it could be seen from this table, that different array options could be utilized (i.e., a single capacitor or a combination of multiple parallel capacitors). It is also evident from this table that a $0.66\mu F$ capacitor in package 2220 or up to 7 of $100nF$ capacitors in 1206 package are options. From the minimum required PCBA area data, for each of these options, it could be seen that the $1 \times 0.66\mu F$ and $7 \times 100nF$ options provide the minimum value. On the other side, each option should also support the maximum nominal inductor rms current; where, from the simulation results in Section 4.3.1, this value is $12.75A$. Note that each of the dividing capacitors current is $I_{L,rms}/2 = 6.375A$. It could be seen from 5.3 that both options also meet the current requirement; however, an array of $7 \times 100nF$ in 1206 package exhibits stray impedance between pairs of capacitors originating from the PCB traces. Moreover different physical location of these capacitors also results in imbalance impedance leading to un-equal current sharing between the capacitors within the array. Since the ESR for these options are not substantially different to provide better balance capacitor current the $1 \times 0.66\mu F$ in 2220 package is used. Note that the selected PN is, in fact, a 2 stacked $330nF$ capacitors; however, because of the nature of their

co-packaging the imbalance impedance is trivial resulting to equal current sharing. In addition, it is also possible to include a 22nF C0G capacitor in 1206 package in parallel with the selected capacitor to provide the possibility of resonant frequency trimming during the PCBA test and validation.

Options PN	Rated Current (A)	P_{loss} (W) $ESR \times I_{rms}^2$	Package (PCB Area mm^2)
1x0.66 μ F C2220C664K1GLCAUTO	11.3	0.283	1x2220 (28.5)
2x330nF+1x33nF C2220C334J1GACTU C1206C333J1GACAUTO	2x5.18+0.693=11	5.625	2x2220+1206 (62.12)
3x220nF+1x33nF C2220C224J1GACAUTO C1206C333J1GACAUTO	3x4.62+0.693=14.553	3.45	3x2220+1206 (90.62)
4x150nF+1*100nF C1812C154J1GACTU CC1206JKNPO0BN104	4x3.16+2.12=14.76	0.054	4x1812+1206 (62.72)
7x100nF C2220C664K1GLCAUTO	7x2.12=14.84	0.027	7x1206 (35.84)

Table 5.3: Dividing capacitors array options.

Resonant inductor L2: Resonant tank inductor is one of the main contributor to the power loss; hence, to the efficiency of the proposed topology. Different inductor parameters including its DCR, ACR, and saturation current play a role in selecting a PN that meets the operation condition and desirable efficiency for the proposed topology. In order to optimize for selecting the resonant inductor L2, its total power loss, mechanical dimensions, and cost should be evaluated.

As described in Section 4.3.2, the inductor power loss is the summation of its core loss and conduction loss (i.e., $P_{loss,L2} = P_v + ACR * I_{L,rms}^2$). On the other side, the ACR depend on the DCR, winding geometry, type of wire, and the switching frequency [45]. On the other side, The core loss depends on the core material and its mechanical dimensions, maximum flux density, and switching frequency. The switching frequency, inductor rms current, and maximum flux density is dictated by the proposed topology; however, in selecting the inductor special attention should be paid to its DCR and mechanical dimension. Table 5.4 provides a list of the inductors evaluated for their power loss through simulation. This table also presents a comparison between the mechanical dimensions and cost for these PNs.

PN	Value (μ H)	DCR ($m\Omega$)	Isat (A)	Volume (cm^3)	Price/1kU (€)
MSS1278T-222	2.2	9.4	22.56	0.327	0.73
IHLP5050CEER2R2M01	2.2	7.2	29	0.596	0.56
VSHB1054T-2R2MC	2.2	4.7	23	0.498	0.69
7443320220	2.2	3.9	24.8	1.3104	1.2

Table 5.4: List of evaluated PNs for resonant inductor.

In order to evaluate the performance of these inductor PNs, the proposed topology power losses is examined under (V_{MPP} V_{bat} f_{sw} P_{MPP})=(35.5V 13.2V 123.4kHz 145.5W) operation

conditions. Fig. 5.4 shows the power loss of these inductors; where, for all cases the selected MOSFET TPH3R10AQM is used; hence, the power loss for the MOSFETs remains constant. As it could be seen from this figure, for inductor with lower DCR the total inductor power loss reduces. Besides, the inductor PN with lower loss also has larger volume, which also results in lower operation temperature. In order to optimize the proposed topology for higher efficiency and lower inductor temperature the PN 7443320220 from Wurth Electronic is used in the designed schematic. It is worth noting that for this inductor, not only the power loss is lower, but also its larger mechanical dimensions results in lower temperature rise.

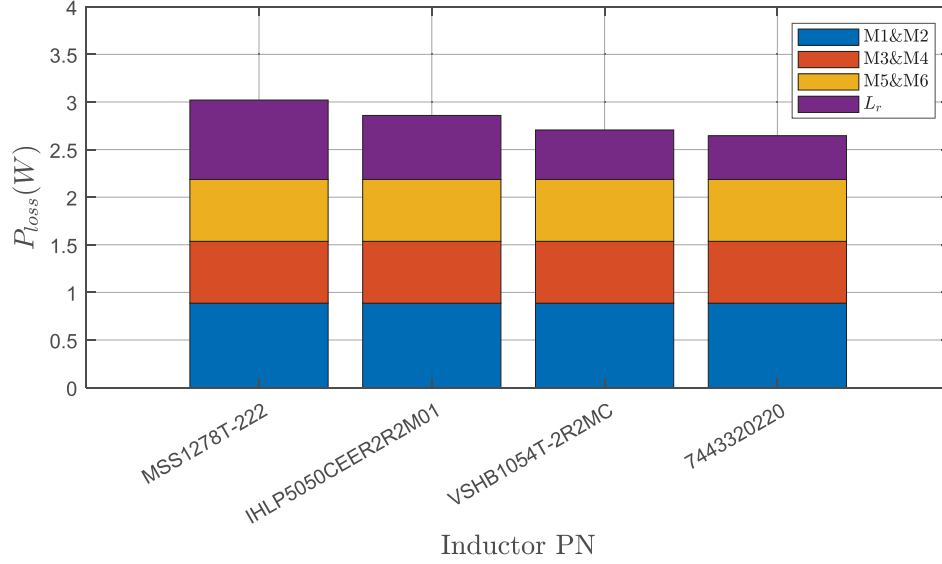


Figure 5.4: Resonant inductor power loss simulated along with the selected MOSFETs PN.

Since the main power loss contributors are the MOSFETs and the resonant inductor, an estimation of the proposed topology efficiency using the selected MOSFETs and resonant tank components for different battery voltage is conducted. Fig. 5.5 depicts the proposed topology efficiency; where, the parameters used in the simulation are given in Table 5.5. As it could be seen from this figure, the increase in the battery voltage results in higher efficiency. As mentioned in Section 4.3.1, at higher battery voltage not only the switching frequency is lower, but also the battery charging and inductors rms currents are lower resulting in lower power loss; hence, higher efficiency. It is worth to note that using the MOSFETs with lower $R_{ds,on}$ and less lossy inductor is also contributing to higher efficiency comparing to the results presented in Section 4.3.1.

Parameter	Value
V_{mpp}	35.5V
P_{mpp}	145.5W
V_{bat}	[12V 13.2V 13.8V 14.6V 15V]
$L2$	7443320220
$C15=C30$	C2220C664K1GLCAUTO
MOSFETS ($M1 - M6$)	TPH3R10AQM

Table 5.5: Parameters used in LTspice simulation for efficiency evaluation.

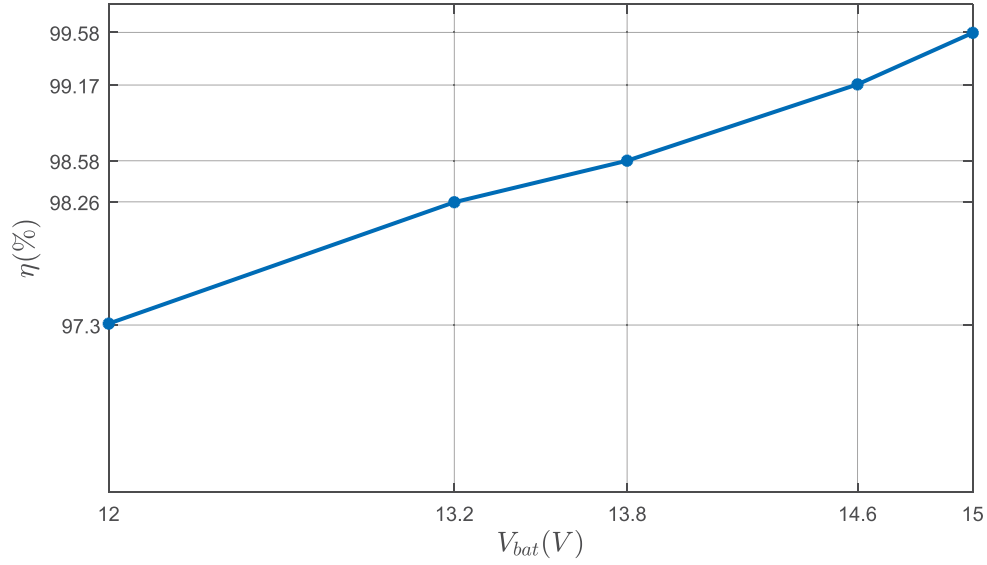


Figure 5.5: Proposed topology efficiency versus battery voltage with selected key components.

In order to validate the close-loop control performance of the proposed DC-DC battery charger according to the selected components, the key components of the power stage are utilized in the PSIM closed-loop simulation. Fig. 5.6 depicts the simulation results for the switching frequency as well as the PV and battery charging power under MPPT control system. As it could be seen the frequency begins from higher values under low power during the start up and reduces according to the MPPT algorithm to extract the maximum power at the steady state, as expected.

Clamping diodes ($D1$ & $D2$): As described in chapter 3 and through the simulation result analysis in chapter 4, clamping diodes play a critical role during the transient events for the proposed topology, by clamping the voltage at the node 'c' and preventing voltage and current stress on the resonant tank. In order to minimize the conduction loss for these diode during their ON-state Schottky diodes with the part number V8PA103-M3/I from Vishay manufacturer is selected. Schottky diodes are more efficient because their conduction loss is lower due to their low forward voltage drop.

Switching stages bypass capacitors: Due to the switching operation, the current at the input of the inverting switching stage and output of the SR switching stage is high frequency with a dc offset. The DC component of these currents is provided by the PV panel and charging the battery, respectively. The AC component, however, should be filtered via the bypass capacitors at the DC link of these stages. The function of the bypass capacitors and the principle for their selection could be described as follows.

- Capacitors $C4$, $C5$, $C20$, $C21$, $C12$, $C13$, $C28$, and $C29$: Surface mount 100uF 63V Aluminum-Polymer capacitors, with the part number A769MS107M1JLAS018 from KEMET manufacturer for the PV side, and surface mount 100uF 25V Aluminum-Polymer capacitors, with the part number RHS1E101MCN1GS from Nichicon manufacturer for the battery side, are employed for filtering the low frequency components of the switching current at the DC link of the inverting stage and SR stage. These capacitors also provide an energy storage

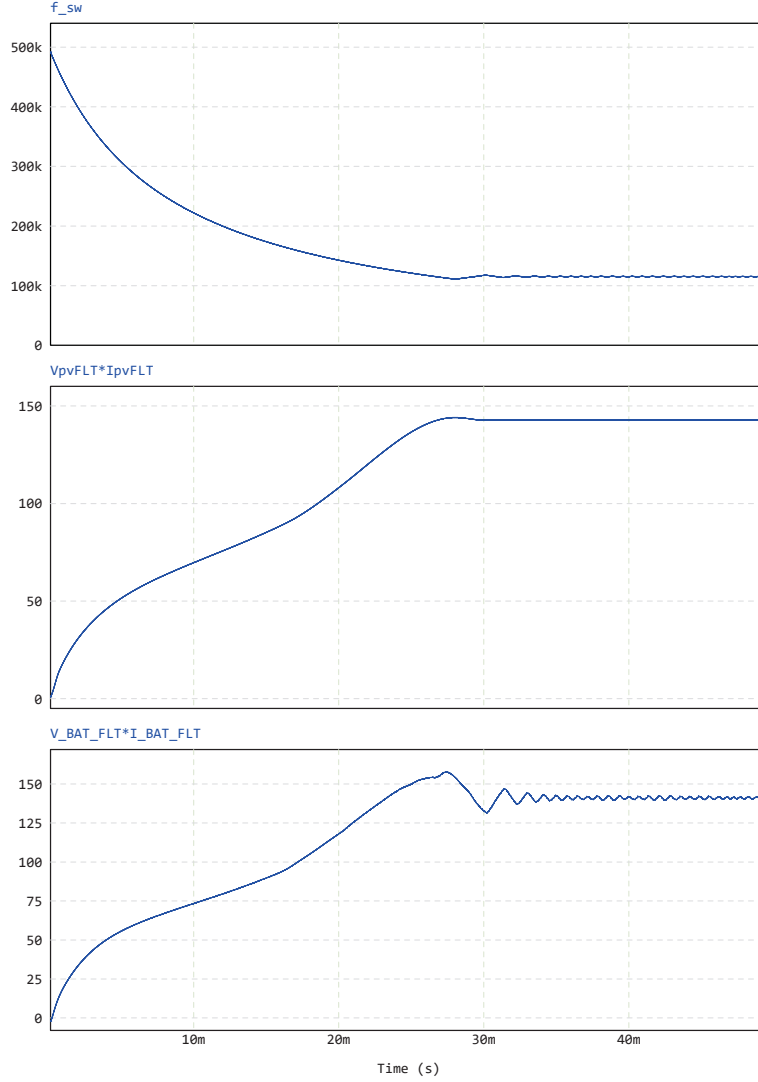


Figure 5.6: Closed-loop MPPT simulation results with the key selected power stage components.

that prevents large voltage swing at the DC link of the inverting and SR stages during the transient events.

- Capacitors C_{46} , C_8 , C_{22} , C_{22} , C_9 , C_{11} , C_{25} , and C_{27} : Surface mount 100nF 100V ceramic capacitors, with part number AC0805JKX7R0BB104 from the manufacturer KEMET, for filtering the high frequency components of the switching current at the DC link of the inverting stage and SR stage. Since the package for these capacitors is smaller they could place closer to the switching HB MOSFETs, effectively bypassing the high frequency current and minimizing the loop stray inductance at the DC link.

In order to reduce the total loss per capacitors multiple capacitors are used in parallel. This

means:

- The total ac current flowing through capacitors will be divided between them, so the reliability will increase as the temperature rise in these capacitors is lower, maintaining more stable capacity.
- The ESR of the parallel array of capacitors decreases significantly resulting in much lower overall power loss in these capacitors.
- Lower ESR of the paralleled capacitors also results in lower voltage ripple at the DC link of both inverting and SR stages. Lower voltage ripple at the PV side results in higher MPPT efficiency.

Resistor R1: As mentioned in Chapter 3, one of the parameters for implementing the proposed control strategy is the battery current which is used as feedback signal provided to the input of the controller. For measuring the current, a resistor with the part number L4CL1206LR001FNR, resistivity of $1\text{m}\Omega$, and rated power of 500mW from the manufacturer Littelfuse Inc. is employed in series with the battery. The tolerance of this resistor is 1 percent, critical for the accuracy in measurement, and moreover this resistor has kelvin connections to prevent the solder joints resistance contribution to the measured voltage.

Connectors J1 and J2: In order to provide both voltage rail and protective earth (PE) interface from PV and battery to the PCBA, three-terminal connectors are needed. The selection criteria for these connectors includes both mechanical sturdiness and their electrical specifications. To provide a reliable mechanical connection to the PCBA while withstanding the mechanical stress, through-hole connectors are a more reliable choice [46, 47]. On the other side, the selecting components should be rated for the required voltage and current operation condition of the PCBA with an extra margin for added reliability. The selected connector part number (PN) for both J1 and J2 is MRR523-5-V (manufacturer euro-block) rated for 15A to handle high battery charging current; while, providing a margin as well. This 3-position wire-to-board terminal block accommodates for standard wire gauge 14-30 for connecting PV and battery to the PCBA and supporting the rated current.

Varistor VR1: Considering the metal frame for a PV panel and its nature of outdoor installation, a PV panel is prone to the lightning strike. This results in high voltage transients at the input of the DC-DC MPPT battery charger. The varistor VR1 is used to absorb the transient energy from the voltage surge at the PV panel interconnection with the PCBA. Steep transient in the voltage results in a high transient current. Using a varistor will help to alleviate this effect, as the current increases the varistor resistivity decreases, leading to more current be conducted by the varistor effectively shunting the transient current [48] and preventing damage to the down-stream components on the PCBA.

Different factor including the operating voltage, surge current, energy absorption, and the average power dissipation should be considered for selecting a varistor [49]. Considering the open circuit voltage on the PV panel, the metal varistor PN of ZV50K1206121NIR1HTa with operating DC voltage of 63V, 1mA voltage of 82V (i.e., the voltage at which the varistor conducts 1mA of current), and clamping voltage of 130V is selected. The maximum allowable peak current and energy absorption for varistors are provided based on standardized $t_1 = 8\mu\text{S}$ - $t_2 = 20\mu\text{S}$ pulse, and $t_1 = 10\mu\text{S}$ - $t_2 = 1000\mu\text{S}$ pulse, respectively, as shown in Fig. 5.7 [50]. The first time, t_1 , in these pulses defines the rise time of the pulse from 10% to 90% of its peak, and the t_2 is the pulse time duration beginning at its rising from 10% and ending at its falling to 50% of the peak. For the selected PN the 8/20 μS clamping pulse current is rated for 1A and the maximum 10/1000 μS pulse energy is rated for 800 mJ.

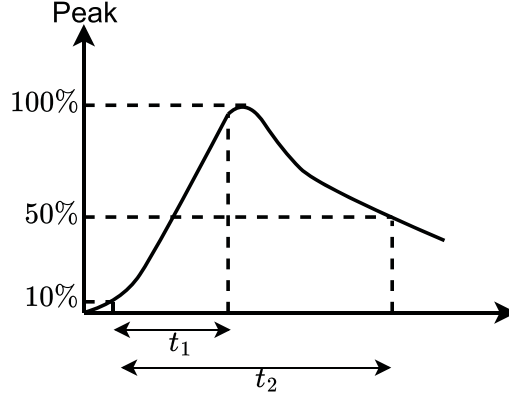


Figure 5.7: Varistor standardized pulse definition.

EMI filter: The fast transition of the power MOSFETs between their ON and OFF states in the switching power converters usually generates high di/dt and dv/dt . These fast transitions of voltage and current accompanied with the circuit parasitic capacitances and inductances usually lead to EMI issues [51] in the switching power converters. Even though the modulation for the proposed topology is mainly based on the soft switching scheme with minimal EMI footprint, the parasitics of the PCBA are not fully controlled. To account for these non-idealities and containing the high frequency conducted EMI within the PCBA a small size EMI filter is utilized. The roles for different parts of this filter are as follows:

- Common mode choke $L1$: PN SRF9045A-701Y, from Bourns, Inc. manufacturer, provides high impedance against conducted common mode current.
- Y capacitors $C1$ and $C14$: 10nF 100V ceramic capacitors with PN D103K43Y5PH6TJ5R, from Vishay manufacturer, along with $L1$ provide low-pass LC filter for the common mode current.
- X capacitors $C2$ and $C3$: 2.2uF 100V ceramic capacitors with PN CL31B225KCHSNN, from Samsung Electro-Mechanics manufacturer, along with the leakage inductance of the common-mode choke $L1$ create differential mode low-pass LC filter for differential current.

Note X and Y refer to safety class for capacitors used in EMI filter application [52]. This classifications requires that the X capacitor failure mode should be short so that the excessive current leads to a fuse opening and prevent fire hazard; while, the Y-rated capacitors that are installed between live rails and PE should fail open to prevent energizing the chassis and the electric shock hazard [53].

5.2.2 Auxiliary Power Supply

As described in Section 5.1, the schematic and PCB layout design for the proposed topology involves three different power/grounding domains. This implies that an auxiliary (AUX) power supply architecture with 3-isolated outputs for supplying the associated functional circuits in each domain is needed. Fig. 5.8 depicts the AUX power tree. In this architecture the input is supplied from the PV, and three isolated outputs (namely V_{CC1} , V_{CC2} , and V_{CC3}) provide the low-voltage supplies for PV, battery, and MCU domains. The isolated outputs V_{CC1} and V_{CC2} are 12V rails to serves as power supply for the PV and battery domains, respectively. Since

the required voltage for the MCU domain is lower, V_{CC1} is converted to an isolated V_{CC3} for providing the power to this domain.

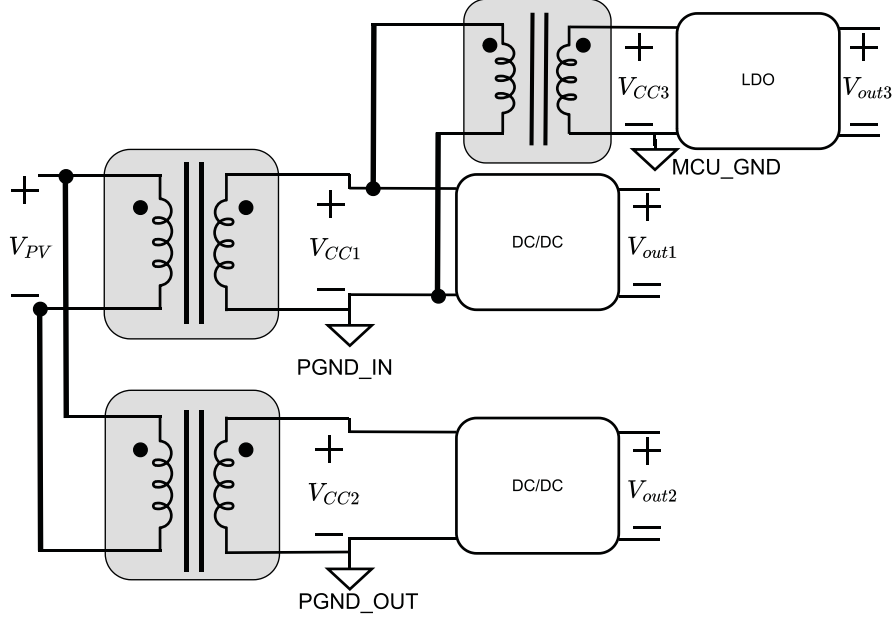


Figure 5.8: AUX power supply architecture for the schematic design.

Since the selected MOSFETs is rated for a maximum gate-to-source voltage of $\pm 20V$ and the recommended MOSFET driving voltage is $10V - 12V$, the V_{CC1} and V_{CC2} are designed to be $12V$. The V_{CC1} and V_{CC2} serve as power supply for the gate drivers at the inverting and SR stages, respectively; where, by accounting for the voltage drop across the gate driver stage the required $10V < V_{gs} < 12V$ is applied between gate and source of the MOSFETs. In order to supply other low voltage circuitry in the PV and battery domains, DC-DC stages is used to convert the V_{CC} to V_{out} . Since the MCU domain and analog sensing circuits are more sensitive to the switching noise, an low dropout (LDO) regulator is used for converting the V_{CC3} to V_{out3} . In addition, the drop out voltage (i.e., difference between V_{CC3} to V_{out3}) is low and the losses in the LDO remain low as well.

Fig. 5.9 shows the designed schematic for AUX power supply. As it could be seen in this figure the PV voltage is converted to $12V_{IN}$, and $12V_{OUT}$ through $U12$, and $U14$, respectively. The $12V_{IN}$, as the V_{CC1} for the PV domain, is then converted to a low-pass filtered $3.3V_{IN}$ via a DC-DC buck module $U13$. Similarly, the battery domain $12V_{OUT}$ (V_{CC2}) is converted to $3.3V_{OUT}$ using the a DC-DC buck module $U15$. It is worth mentioning that the low-pass LC filters provide a voltage with lower ripple at the $3.3V$ rail for the PV and battery domains. As it could be seen from Fig. 5.9c, to generate the AUX supply for the MCU Domain, the $12V_{IN}$ is converted to $5V_{uC}$ through $U17$, then dropped to $3.3V$ via $U16$. Table 5.6 list the PNs for the key components in the designed AUX power supply along with their functions.

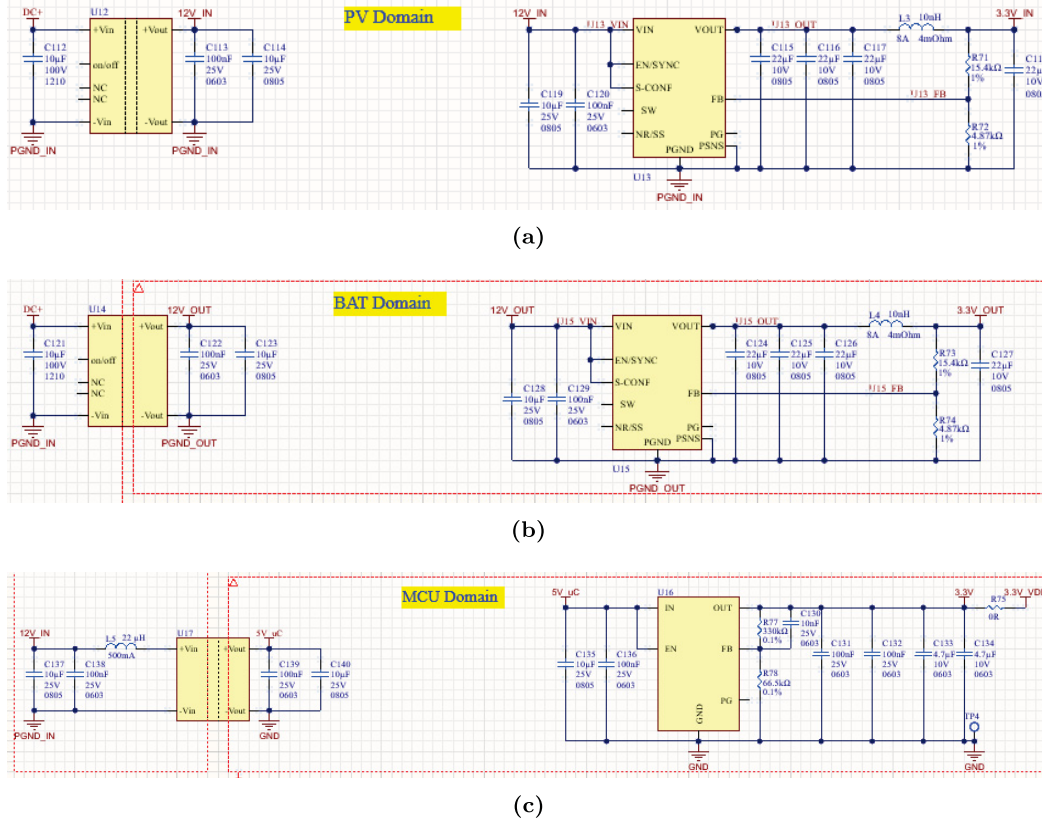


Figure 5.9: Designed schematic for AUX power supply (a) PV domain, (b) battery domain, and (c) MCU domain.

Designator	PN	Function
U12 & U14	TEC 3-2412UI	Isolated DC-DC
U17	SCT01F12S05	Isolated DC-DC
U13 & U15	TPSM82913RDUR	Buck module
U16	TPS74533PQWDRVRQ1	LDO

Table 5.6: Key components PN used in the designed AUX power supply.

5.2.3 Gate Driving

Since the grounding domain on the inverting and SR stage MOSFETs is different, separate gate drivers allocated to driving the MOSFETs in each domain should be used. There are various options for selecting the gate driver, namely:

- Single channel isolated gate driver; where, at its input receives the pulse signals from the MCU domain, and at its output the gate drive signal for the MOSFET is provided.
- Isolated HB gate driver with isolated high side (HS) and (LS) channels
- Isolated HB gate driver with non-isolated high side (HS) and (LS) channels

- Non-isolated HB gate driver for each of HB MOSFETs of the inverting and SR stages along with digital isolator for transferring the pulse signals from the MCU to the PV and battery domains, as depicted in Fig. 5.10. As it could be seen from this figure a bootstrap diode and capacitor provide the power supply network for the HS gate driver. The bootstrap capacitor is charged when the LS MOSFET is in ON-state, to store enough energy for supplying the turn ON state of the HS MOSFET complementary to the LS MOSFET within each switching cycle. Note that, when the HS MOSFET is ON, the bootstrap diode is in reserve bias and OFF state, separating the VCC from the HB switching node domain.
- Non-isolated HB gate driver for the inverting stage MOSFETs, and FB gate driver for the SR stage MOSFETs. This also requires digital isolator.

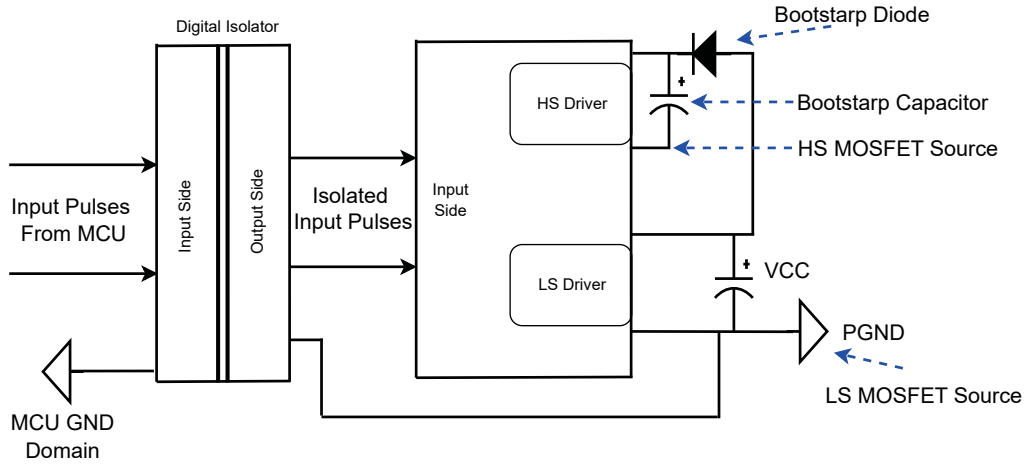
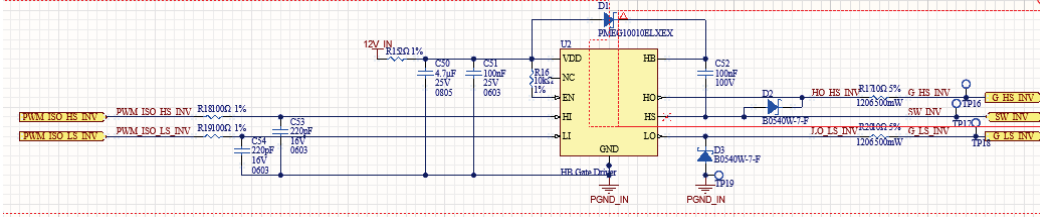


Figure 5.10: HB Gate driver with digital isolator at the input.

Note that each of the options for the gate driver selection provides pros and cons; however, the isolated-based designed AUX power supply provides the possibility of using non isolated gate driver along with digital isolator. In order to simplify the gate driving stage a HB gate driver for the inverting stage, and a FB gate driver for the SR stage is selected. Fig. 5.11 presents the designed schematic for the inverting stage MOSFETs ($M1$ & $M2$) gate drivers. It could be seen from this figure that $12V_IN$ is used to supply the gate driver, and the bootstrap scheme is used for the HS MOSFET driver. It is worth noting that during the ON state for the HS MOSFET within the HB, the switching node is connected to the DC link of the HB; hence, the bootstrap diode should be rated to withstand the high reverse voltage. Moreover, at the input side of the gate driver an RC LPF with very high -3dB frequency is used for filtering very high frequency noise that the pulse signals might be exposed to on the PCB. At the output of the gate driver driving stages Schottky diodes are utilized across the gate-to-source of the MOSFETs to protect the gate oxide layer against transient negative voltage [54].

The SR stage, on the other hand, is an FB; where, either two HB gate drivers or a single HB gate driver could be utilized for driving $M3 - M6$ MOSFETs. Fig. 5.12 depicts the designed schematic for the SR stage gate driver; hence, the battery domain AUX supplies $3.3V_OUT$ and $12V_OUT$ are used to supply the input and output stages of the gate driver, respectively. It could be seen from this figure that a FB gate driver consisting of two HB channels is employed. Each


 Figure 5.11: HB Gate driver for $M1$ & $M2$, MOSFETs.

HB channel requires its dedicated bootstrap diode and capacitor with the negative low side of each capacitor connected to the switching node of its associated HB in the SR stage. The selected FB gate driver has internal bootstrap diodes[55]; hence, no external diode is added in the design. Due to better layout location on the PCB, in the schematic design the HB channel A of the gate driver is used for driving $M5$ & $M6$; while, its channel B drives $M3$ & $M4$.

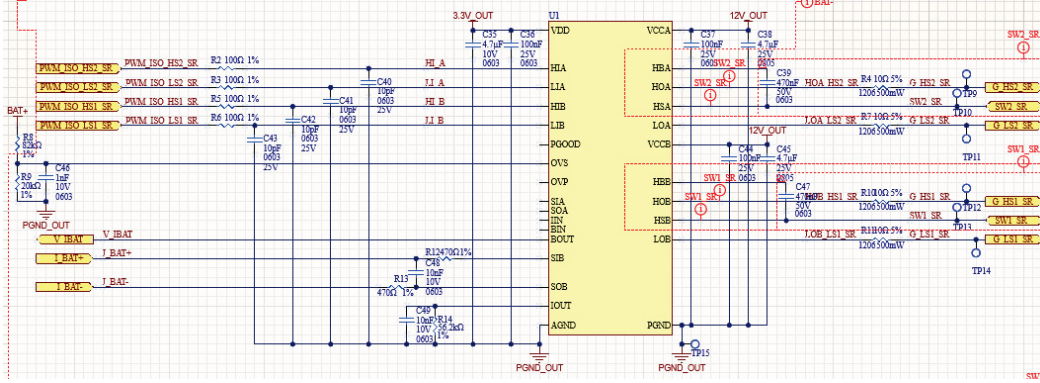

 Figure 5.12: FB Gate driver for $M3$ - $M6$, MOSFETs.

Table 5.7 lists the key components used for the gate driving schematic design. The bootstrap diode on both gate drivers are rated for 100V to withstand the transient voltage spikes at the switching node of each HB MOSFETs. The Schottky diode B0540W-7-F with forward voltage bias of 0.51V clamp the gate-to-source of the MOSFETs to $-0.51V$ during the negative transient events protecting the gate-to-source of these MOSFETs [54]. Even though, the gate resistor in the designed schematic is 10Ω , during the PCBA validation stage this resistor should be adjusted to optimized for the MOSFETs turning ON and OFF transients, which is highly dependent on the HB layout and its stray inductances.

5.2.4 Sensing Circuits

As describe in Section 3.4 different signals including V_{PV} , I_{PV} , V_{bat} , I_{bat} , and i_{Lr} are used for closed-loop control strategy and monitoring purposes. This requires designing sensing network for these feedback signals. However, these signals are in different power/grounding domains from the MCU domain; hence, requires isolated signal transfer to the ADC inputs at the MCU interface. The following describes the sensing strategy for each of these signals.

Designator	PN	Manufacturer
U1	SM72295MAX/NOPB	Texas Instruments
U2	UCC27282DRCR	Texas Instruments
D1	PMEG10010ELXEX	Nexperia
D2 & D3	B0540W-7-F	Diodes Incorporated

Table 5.7: Key components PN used in the designed gate drivers.

PV and inductor currents: As described before, the sensed PV current is used in close-loop feedback control for MPPT control; where, since its is ideally a DC current the required bandwidth on the sensing network does not require to be high. However, the inductor current is utilized for the current zero detection; while, it is also a high frequency current.

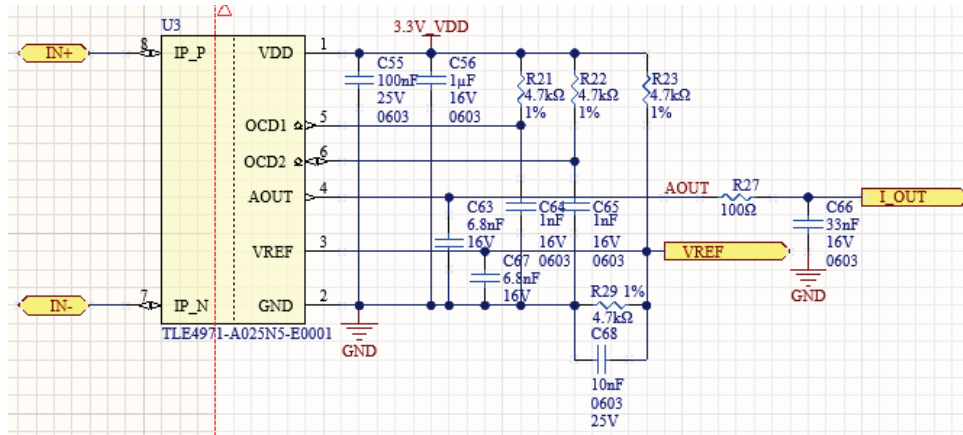


Figure 5.13: Current sensor designed schematic.

In order to simplify the schematic design and at the same time provide the required isolation for sensing these currents, the current sensor TLE4971 shown in the designed schematic of Fig. 5.13 is utilized. This current sensor is a coreless Hall effect technology with functional galvanic isolation between its input and analog output [56]; where, the PN with 25A full scale range is used in the schematic. As the isolate analog output side of the sensor is in MCU domain, it is supplied by its domain 3.3V rail. The analog output provides the AOUT as the sensed signal and the VREF is externally applied as 1.65V via the resistive divider from its VDD supply. It worth to note that the two analog outputs need to be routed closely on the PCB for higher signal integrity and better impedance control. Fig. 5.14 shows the simulation results using the SPICE model provided by the manufacturer. The input current is a 125kHz ac current at an amplitude of 20A representing the worst case maximum inductor current at minimum battery voltage and maximum PV MPP power. As it could be seen from this figure, the VREF is at 1.65V as expected, and the AOUT a 125kHz sinusoid with an amplitude of 0.8V and offset of 1.65V changes between 0.85V to 2.45V well within the 3.3V input range of the ADC.

PV and battery voltages: Both PV and battery voltage sense is done via simple resistive divider; where, the sensed voltage is scaled down within the 2.25V input limit of the isolated analog amplifier used for transferring these signals to the MCU domain.

Fig. 5.15 shows the PV and battery voltage sense resistive dividers followed by isolated analog

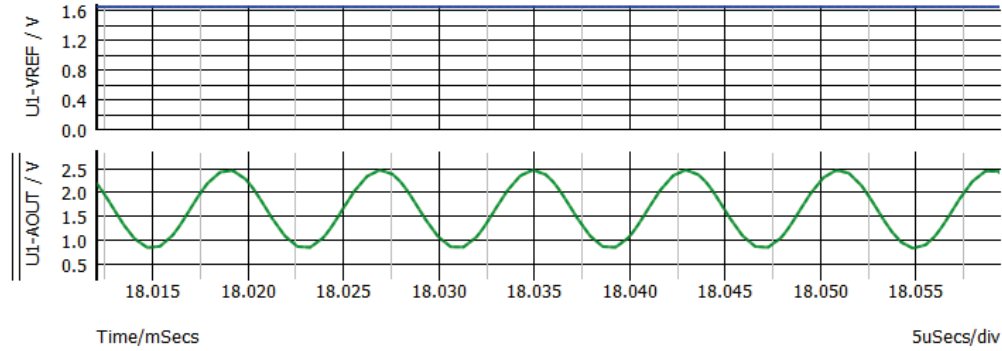


Figure 5.14: Inductor current sensor simulation results.

amplifier $U7$ and $U5$, respectively, with the PN AMC0311 from Texas Instruments. As it could be seen the primary side of the $U7$ is supplied by 3.3V_IN as it is within the PV domain; while, the primary side of the $U5$ is supplied by 3.3V_OUT at the battery domain side. Note that the secondary side of both $U5$ and $U7$ is supplied by the MCU domain 3.3V.

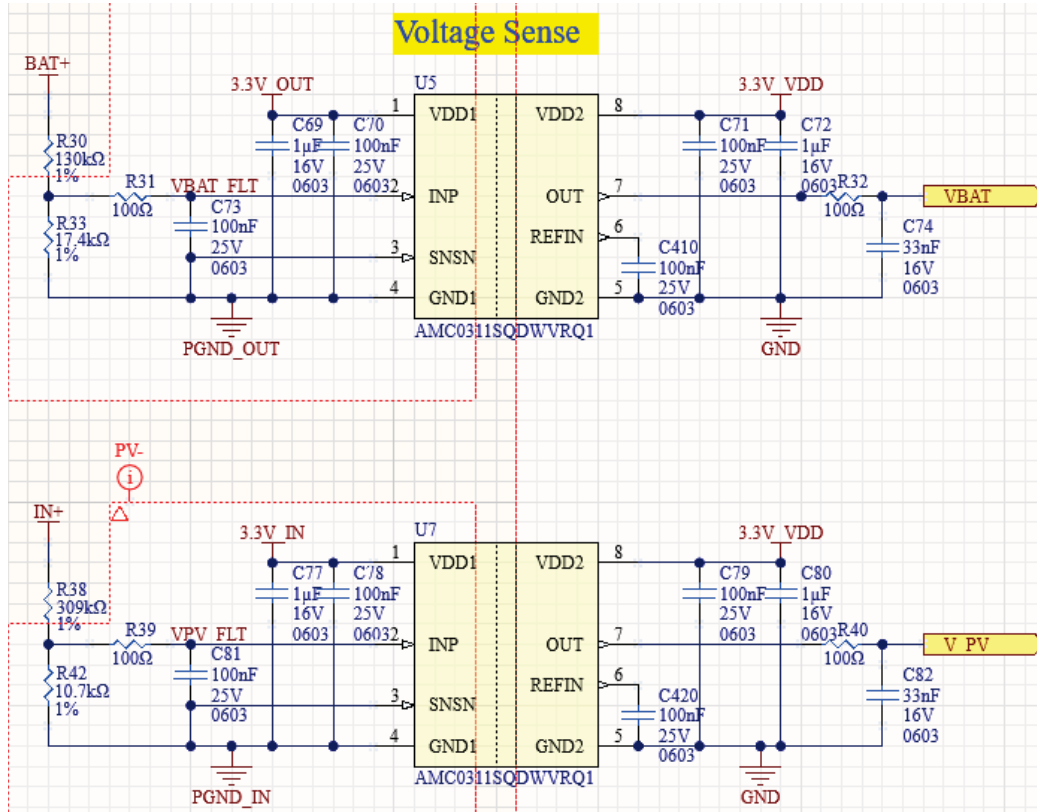


Figure 5.15: PV and battery voltage sense.

Battery current: In order to leverage the current sense amplifiers within the FB gate driver for the SR stage, a shunt resistor is utilized for the battery current sense. As describe in the power stage schematic design in Section 5.2.1, the shunt resistor L4CL1206LR001FNR with kelvin measurement terminals is used to minimize the effect of the resistance change of the solder joints due to the thermal variation and its effects on the measured voltage. Then, the measured voltage at the Kelvin pins, equivalent to the battery charging current with a ratio of $1\text{mV}/1\text{A}$, is applied to the current sense amplifier of the FB gate driver as it could be seen in Fig. 5.12. The amplified voltage with a gain of $119.57\text{mV}/1\text{A}$ is then applied to the isolated analog amplifier AMC0311 for transferring to the MCU domain. This is depicted in Fig. 5.16; where, the primary of the isolated amplifier is supplied by the battery domain AUX supply and its secondary supplied by the MCU domain power supply. Note that by considering the 2.25V input limit on the AMC0311 and the current amplifier gain a 18.83A measurement range for battery current is provided.

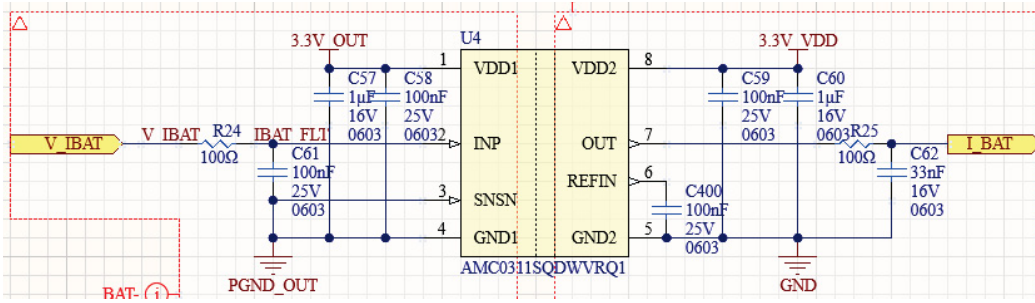


Figure 5.16: Amplified voltage equivalent to the battery current transfer to the MCU domain.

5.2.5 MCU Interface

In the schematic design the goal is to use an off-the-shelf MCU evaluation module (EVM); hence, in this schematic an interface connector for the NUCLEO-G474RE with STM32G4 from ST Microelectronics is used. All the sensed analog signals are applied to the ADC input of the MCU routed to the interface connector and the PWM signals from the MCU are routed to the connector and then to the digital isolator at the input of the gate drivers. Note that the PWM signals for the proposed topology are at fixed 50% duty cycle. Fig. 5.17 depicts the MCU EVM interface along with the digital isolators used to transfer the PWM signals from the MCU domain to the PV and battery gate driver domains.

5.3 PCB Layout Design in Altium Designer

The first step in the PCB layout development is defining the layer stackup based on the design requirements and the available PCB manufacturer minimum requirements. The 4-layer stackup used in the PCB design is shown in Fig. 5.18 that also meets the eurocircuits manufacturing requirements. The stackup is a 4-layer PCB that includes a core panel with additional top and bottom layers added with prepreg layers. A 1 oz copper weight for all the layers is assumed. Moreover, the PCB layout design rules are defined based on the manufacturer minimum requirements along with the defined electrical clearance according to the operation voltages for different circuit functional blocks and power/grounding domains.

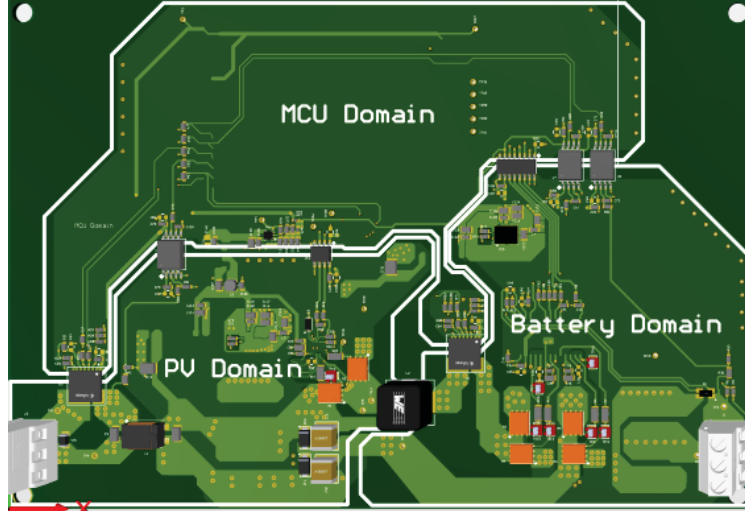


Figure 5.19: PCB planning and domain separation.

is the stray inductance of the switching node routing. These inductances could have adverse affect on the performance of the converter and affecting the lifetime of the MOSFETs by exposing them to a repetitive high voltage transients [57].

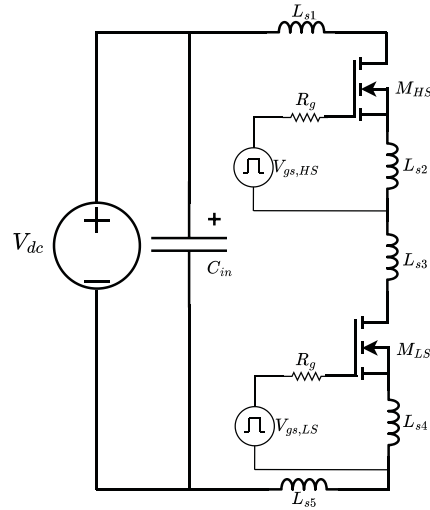


Figure 5.20: High-frequency loop for an HB MOSFETs with stray inductances.

When a MOSFET within the HB turns off the stray inductance that connects the the MOSFETs to the dc link creates a high transient voltage, because of the high di/dt (also known as inductive electromotive force (EMF)), and the summation of this transient voltage and the dc link voltage is the voltage appears at the drain-to-source of the MOSFET (i.e., $V_{ds} = V_{dc} + L_s di/dt$). If the stray inductance is not minimized, a high di/dt could result in substantially larger voltage stress than the dc-link voltage on the MOSFETs; hence, one of the key consideration in PCB

layout for each HB MOSFETs and their bypass capacitors is to minimize the loop stray inductance through placing the bypass capacitors as close to the HB MOSFETs as possible. In this PCB layout design the HB MOSFETs are placed on the top layer the high-frequency bypass capacitors are placed right under them on the bottom layer as it could be seen from Fig. 5.21. Moreover, the MOSFETs and the capacitors are connected via wide and short copper regions, in this way the loop and its stray inductance is minimized.

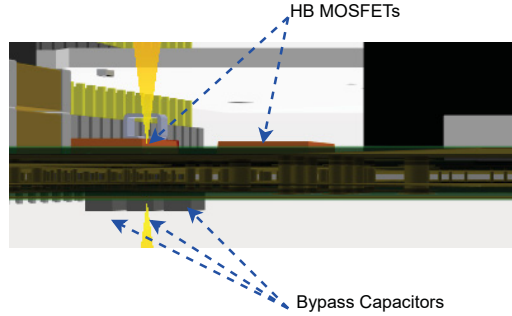


Figure 5.21: High-frequency loop minimization on the PCB.

5.3.3 Gate Driving Layout Considerations

The gate drive circuits and their routing play an important role on the switching behavior of the MOSFETs and the overall reliable and efficient performance of the proposed DC-DC battery charger. There are different considerations when routing the MOSFETs gate driver circuit to ensure desirable switching of the MOSFETs. Minimizing the gate drive loop inductance, by bringing the gate drive stage as close to the MOSFET as possible, is an important consideration. This reduces the gate drive signal ringing; hence, reducing the overshoot on the gate to source of the MOSFETs. Moreover, from the HB MOSFETs of Fig.5.20, it could be seen that L_{s2} and L_{s4} are the stray inductance between the HS and LS MOSFETs' source pin and the return path for their gate driver, respectively. These stray inductances are in the path of the main power stage current; hence, their di/dt during the turn-OFF transition of the MOSFETs could create a negative voltage at the source pin of the turning-OFF MOSFET. If this negative voltage is high enough, the V_{gs} of the MOSFET could increase to the point that it might exceed its gate-to-source turn-ON threshold causing a false turn-ON of this MOSFET. This means the return path of the gate driver should be connected as direct to the MOSFET source pin as possible.

5.3.4 MCU Domain Layout

Fig 5.22 illustrated the MCU domain on the designed PCB in this thesis. As it could be seen from this figure, the components that are within the MCU domain and the connector interface for the MCU EVM are placed at the upper half of the PCB. A boundary between the MCU domain and the PV and battery domains is assumed to not only meet the clearance requirement defined in the design rules but also the digital and analog isolators, for transferring the signals between these domains, are placed across this boundary to minimize the interference between the three domains.

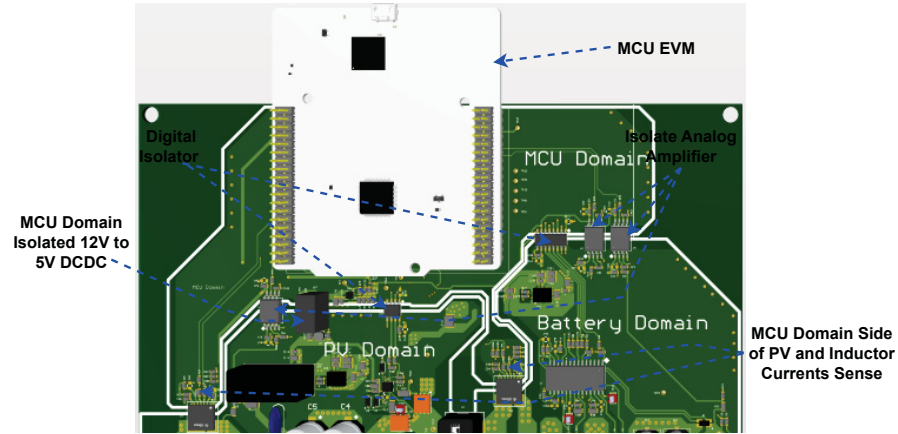


Figure 5.22: MCU domain on the PCB.

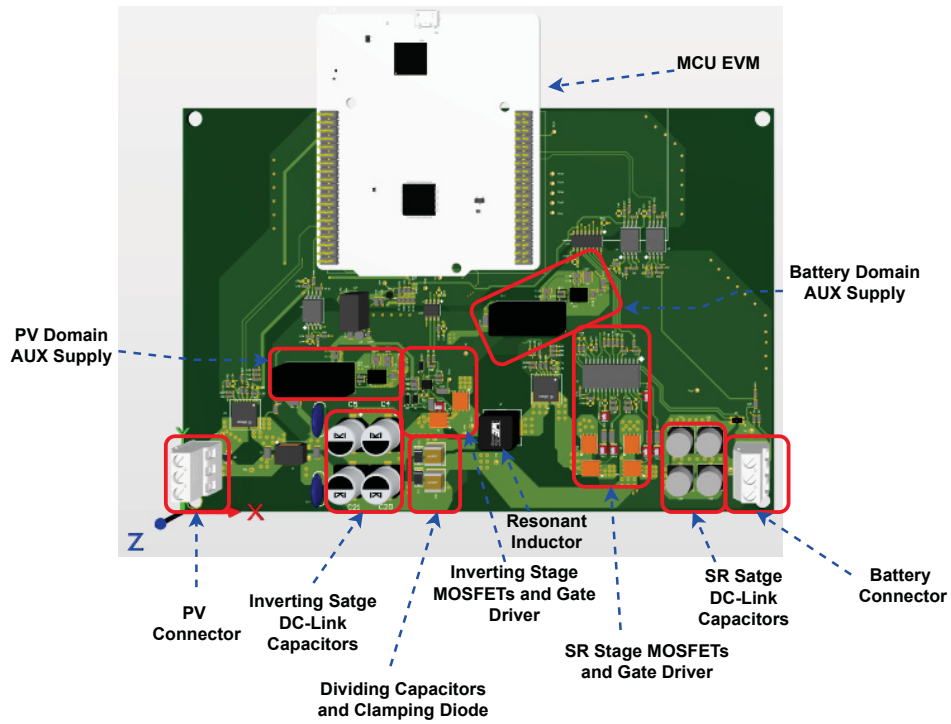


Figure 5.23: 3D view of the designed PCB in the Altium Designer.

5.3.5 Grounding Approach

Grounding in the context of this layout design refers to the GND for the MCU domain, as well as PGND_IN and PGND_OUT for the PV and battery domains, respectively. In this context GND is the reference plane and the return path for all the signals within the MCU domain. PGND_IN

is the negative of the dc-link at the inverting stage that in the designed PCB it is generated with a single plane on the layer 2 and 3 creating the shortest path with the least impedance for the return current to all the capacitors at the dc link of the PV side. Similarly, the PGND_OUT is designed as a solid return plane for the battery domain on both layer 2 and 3 of the PCB. It worth mentioning that physical separations between all three of the ground planes for the three domains are created on the PCB to meet the design rule requirements and the safety on the MCU domain.

5.3.6 3D-Model of the Designed PCB

Fig. 5.23 is an annotated display of the 3D view for the designed PCB. As it could be seen from this figure, the PV connects to the PCB on the left side, followed by the varistor, current sensor and the EMI filter. The dc-link low frequency filtering for the inverting stage are as close to the switching MOSFETs as possible. The MOSFETs orientation and their gate driver location is in such away provided an appropriate gate drive loop; while, minimizing the interference between PWM signals and the power path. The dividing capacitors and their clamping diode location is optimized with respect to the resonant inductor. Similar to the inverting stage, the gate driver and MOSFETs for the SR stage are also placed optimally to ensure desirable performance. The SR stage is then followed by its dc-link capacitors and the battery connector on the right side of the PCB. It is worth noting that the AUX power supplies for the battery domain is placed at the border of this domain and the PV domain to accommodate for the physical separation of these two domain and complying with the design rule; while, the PV domain AUX DC-DC is located within its domain. It is also worth mentioning that the MCU EVM on the upper half of the designed PCB is interfaced with the power PCB via board-to-board connectors.

Chapter 6

Conclusion and Future Work

This thesis began with an introduction on the utilization of solar energy and its growth outlook in the Europe continent and the globe, to justify the need for continuous research in PV solar MPPT power electronics converters and their controller. A first background study on DC-DC converters was conducted to investigate common MPPT power electronics converters and their shortcoming. This included different approaches including non-isolated buck and boost MPPT converters as well as isolated converters. This helped to identify potential improvement opportunities and possible contributions and objectives to be pursued for this thesis research work. More specifically, utilizing active bridge based converters with soft switching scheme along with using FM and PSM control approaches for the MPPT power control and battery charge profile control emerged as an research subject. The main objectives were identified for pursuing goals such as a) extracting maximum power from PV via MPPT control strategy, b) enhancing the efficiency, c) reducing the EMI footprint, and d) better battery charge profile control.

Once the potential objectives and contributions were identified, the next logical step was to explore the electrical specifications of PV panels upon which the requirements for a MPPT-based DC-DC battery charger could be developed. For this purpose an introductory familiarity with different electrical characterizations of a PV panel is first explored, then a comprehensive data analysis on 25000 commercially available PV panels is conducted. Through this analysis a cluster of PV panel modules within a specific electrical parameters including V_{mpp} , P_{mpp} , and I_{sc} were identified, then a PV module was selected as the base for designing a DC-DC battery charger for a single-PV panel based application in this research work.

A broad literature review on different type of DC-DC converters and their applications in MPPT and battery charging is first conducted. According to the first literature review that identified an active bridge based topology as the potential candidate for designing the DC-DC battery charger for this research work, and also based on the electrical characterization of the selected PV panel, a second literature review focusing on these topologies is conducted. In this literature review the isolated active bridge based topologies such as HB and FB based DAB and CLLC as DC-DC converter were studied and the pros and cons of each topology were investigated. Then, by considering the required electrical specifications such as PV and battery voltages ratio an HB on the inverting stage and FB on the SR stage was decided as the base for the proposed topology for this thesis. It was also concluded that the non-isolated approach is better suited for this thesis application. To enhance the power density by pushing the switching frequency to higher range and reducing the size of the passive components, such as capacitors and inductor, a resonant approach was decided. The two unique resonant topologies with an HB for converting the PV DC voltage to an HFAC voltage and the FB SR stage for rectifying the HFAC to DC

voltage for charging the battery were considered as possible topologies. The first topology is based on a series resonant converter; while, the second topology is attempting to utilize dividing capacitors on the inverting stage as resonant capacitor. Through an initial study it was identified that the second topology offers lower transient current and voltage stress; hence, it was decided as the proposed topology for this research work. To further analyze the two topology approach a comparative simulation study was conducted and the results were presented in the Chapters 4 of this thesis.

Once the topology was proposed, a detailed time-domain modeling and analysis using the MATLAB tool was conducted for better understanding transient switching events as well as the dynamics of key signals of the proposed topology. This included the inductor current, dividing capacitors node voltage, SR stage input voltage and its MOSFETs current. This analysis also provided a deeper comprehension of the HF static behavior of the proposed topology as well as identifying the frequency modulation and ZCS phase shift as control variables that should be employed for the ZVS and ZCS of the inverting and SR stages, respectively.

Following the time domain analysis of the proposed topology, a frequency domain analysis was conducted to propose a suitable control strategy for the proposed MPPT-based DC-DC battery charger. A combined FM and PSM scheme is introduced along with the possible MPPT algorithms for providing an effective MPPT control. The constant voltage mode battery charge controller is also introduced to prevent the battery overcharging. The main goals for these control strategies were to provide high efficiency, reliable power flow control, and battery charge profile adjustment when necessary.

In order to validate the proposed topology and control strategies, since the resonant tank plays the main role in defining the operation frequency range, current and voltage stress, as well as the nominal power condition, a design approach for the resonant tank components was presented with the aim to optimize for this part. Then, to validate the time domain analysis and the proposed control strategies comprehensive open-loop and closed-loop simulations were conducted. The open-loop simulation using the LTspice tool first focused on the comparative analysis of the two subject resonant topologies under different MPP operation and load profiles. The results analysis proved that the resonant topology with the dividing capacitors and clamping diodes provide much lower current and voltage stress on the key components such as the inductor, capacitors, and MOSFETs. This helps to avoid the over-sizing of the components like inductor that otherwise needed to handle high transient currents without saturating; hence, improving the power density. Lower voltage stress on the capacitors also improves their reliability and lifetime; while, lower transient current also leads to lower thermal stress on the MOSFETs and capacitors. Another open-loop simulation was conducted specifically for the proposed topology under different battery voltage condition but at the maximum PV MPP condition with the aim of validating the time domain analysis, identifying the operating switching frequency range, finding the required ZCS phase shift, analyzing the maximum power losses in the key components, and evaluating the efficiency. Through the open-loop simulation results analysis the expected operation condition for the closed-loop control architecture was also predicted. The proposed topology, modulation schemes, and control strategies were further investigated through a closed-loop simulation implemented in PSIM simulation. The simulation results validated the performance of the proposed control strategies and provided guidance on how the control system should be implemented to provide a seamless transition between the MPPT and voltage control modes. The consistency for the key waveforms across the time-domain analytical results, open-loop simulation results, and the closed-loop simulation results validates the mathematical modeling and proposed control strategies.

In order to design a schematic and PCB for the proposed topology and accommodating for sensing the signals required for the proposed control strategies, different power domains

were defined. The components design in Chapter 4 was limited to the resonant tank; hence, to design an optimized schematic for the PCB a more extensive component selection approach was taken. Using comparative open-loop simulation, for optimizing the efficiency and cost, key components such as MOSFETs, resonant tank inductor, and dividing capacitors were selected. The analysis included both power loss and the cost comparison for these key components through which the final candidates were selected. Using the SPICE model for these key components the open-loop simulation for the maximum PV MPP condition across different battery voltage was conducted showing efficiency enhancement comparing to the equivalent results that were presented in Chapter 4. Various consideration for selecting different components of the schematic were discussed and the components were selected. Once the designed schematic was finalized based on the selected components, the PCB layout design was planned. Different practical considerations and planning were discussed and attempted to optimize the PCB for different defined power/grounding domains. The PCB is designed for an optimized switching performance of the proposed topology assuring reliable MOSFETs gate drive, minimizing the voltage stress on the MOSFETs, reducing the risk of unwanted MOSFET transition and HB shoot through. Through this endeavor various insight into the PCB layout design for switching power converters were gained.

As a future work, the PCBA for the resonant DC-DC converter proposed in this thesis could be manufactured with the purpose of validating the proposed modulation schemes, control strategies, and its efficiency through experimental test results. Moreover, this thesis focus was on a single-PV fed resonant battery charger with a 4-cell battery at a maximum voltage of 16.8V. There are various applications across energy and transportation electrification that require PV panels array but also include higher battery pack voltage. In these applications the PV array voltage is much higher; while, the battery pack voltage also varies widely. An extension of the research work in this thesis is an isolated topology; where, the turn ratio of the transformer could be utilized for meeting wider voltage gain. Moreover, at higher voltage and power applications the galvanic isolation is a requirements for safety in both energy and transportation charging infrastructure. Another extension of this research work is utilizing it as the front-end MPPT converter for the grid-interfaced or stand-alone DC to AC inverter applications. In this application also a transformer based design will be beneficial to boost the voltage to a dc bus of 400V to accommodate for the single phase inverter with an output voltage of 230VAC.

Appendix A

Time Domain Analysis MATLAB Code

```
1 clear all
2 %% Defining Variabale
3 syms Vmpp Vin Po Vo VFM VFD Lr ESR_Lr C fsw tdead tdead_SR
4 Wres1=1/sqrt(2*Cs*Lr) %resonant frequency of MOSFET's output
5   capacitance with Lr
6 fres1=Wres1/(2*pi);
7 Wres2=1/sqrt(Lr*(2*C)); %resonant frequency of disviding capacitors
8   with Lr
9 fres2=Wres2/(2*pi);
10 Wres3=1/sqrt(Cs*Lr) %resonant frequency of MOSFET's output
11   capacitance with Lr
12 fres3=Wres3/(2*pi);
13 Tsw=1/fsw; % dead time, this is selected based on the
14   minimum needed time for maintaining ZVS (delta_t2+delta_t3)
15 tend=Tsw;
16 t=0:(Tsw/(tend/(100e-12)-1)):tend;
17 t_delay_SR=t0-tdead/2; % time delay between turn on of M3 with respect to the turn
18   on of the M1 (this is to obtain the ZCS turn off of the M3) tdelay_SR=t0_SR+
19   tdead_SR-tdead/2, t0_SR=(t9-(Tsw+tdead/2))
20
21 for nt=1:length(t)
22   if t(nt)<=(t0-tdead_SR)
23     VGS3(nt)=0;
24     VGS4(nt)=10;
25   elseif t(nt) > (t0-tdead_SR) && t(nt)<=(t0)
26     VGS3(nt)=0;
27     VGS4(nt)=0;
28   elseif t(nt) > (t0) && t(nt)<=(Tsw/2-tdead/2+t_delay_SR)
29     VGS3(nt)=10;
30     VGS4(nt)=0;
31   elseif t(nt) > (Tsw/2-tdead/2+t_delay_SR) && t(nt) <= (Tsw/2-tdead/2+
32     t_delay_SR+tdead_SR)
33     VGS3(nt)=0;
34     VGS4(nt)=0;
35   elseif t(nt) > (Tsw/2-tdead/2+t_delay_SR+tdead_SR) && t(nt) <= (Tsw-tdead/2+
36     t_delay_SR)
37     VGS3(nt)=0;
38     VGS4(nt)=10;
```



```

31 elseif t(nt) > (Tsw-tdead/2+t_delay_SR) && t(nt) <= tend
32     VGS3(nt)=0;
33     VGS4(nt)=0;
34 end
35 end
36
37
38 Vx_t0=Vx_t0; % the initial
    voltage for mode 1 at vx(t) (V_X0)
39 I_L_t0=I_L_t0; % the initial
    inductor current for mode 1 at t=t0
40 t_M1_turnsOFF=Tsw/2-tdead/2; % the time
    periode that mode 1 lasts
41 t1=t_M1_turnsOFF; % time at the end
    of mode 1
42 Vx_t1=(-Vin+Vo+Vx_t0)*cos(Wres2*(t1-t0))+(I_L_t0/(2*C))*(1/Wres2)*sin(Wres2*(t1-t0))-(-Vin+Vo); % vx(t) at t=t1
43 I_L_t1=-(2*C*Wres2)*(-Vin+Vo+Vx_t0)*sin(Wres2*(t1-t0))+I_L_t0*cos(Wres2*(t1-t0)); % the inductor current at the end of mode 1
44 delta_t2=(1/Wres1)*asin((2*Cs*Wres1*(Vin+VFM))/I_L_t1); % the time that
    mode 2 lasts
45 t2=t1+delta_t2; % the time at the
    end of mode 2
46 Vx_t2=Vx_t1; % Vx at the end
    of Mode 2
47 I_L_t2=-(2*Cs*Wres1)*(-Vin+Vo+Vx_t1)*sin(Wres1*(t2-t1))+I_L_t1*cos(Wres1*(t2-t1)); % the inductor current at the end of mode 2
48 t3=Tsw/2+tdead/2; % the time at
    the end of mode 3
49 Vx_t3=(Vo+VFM+Vx_t1)*cos(Wres2*(t3-t2))+(I_L_t2/(2*C*Wres2))*sin(Wres2*(t3-t2))-Vo+VFM; % Vx at the end of Mode 3
50 I_L_t3=-(2*C*Wres2)*(Vo+VFM+Vx_t1)*sin(Wres2*(t3-t2))+I_L_t2*cos(Wres2*(t3-t2)); % the inductor current at the end of mode 3
51 delta_t4=(1/Wres2)*asin(I_L_t3/(2*C*Wres2*(Vo+Vx_t3))); % the amount of time that
    takes the inductor current goes from IL3 to zero
52 t4=t3+delta_t4; % the time at the end of
    mode 4 ((Tsw/2-tdead/2)+t_delay_SR), at this time the M3&M5 turn off to
    maintain ZCS
53 Vx_t4=(Vo+Vx_t3)*cos(Wres2*(t4-t3))+(I_L_t3/(2*C*Wres2))*sin(Wres2*(t4-t3))-Vo;
54 I_L_t4=-(2*C*Wres2)*(Vo+Vx_t3)*sin(Wres2*(t4-t3))+I_L_t3*cos(Wres2*(t4-t3))
55 delta_t5_prim=(1/Wres3)*acos((Vx_t4-(Vo+2*VFM))/(Vo+Vx_t4)); % the time at the
    end of Mode 5 when Cs3&Cs5 are fully charged and Cs4&Cs6 are fully discharged
56 t5_prim=t4+delta_t5_prim;
57 Vx_t5_prim=Vx_t4;
58 I_L_t5_prim=-(Cs*Wres3)*(Vo+Vx_t4)*sin(Wres3*(t5_prim-t4)); % the time at
    the end of Mode 5&6 when body diode of M4&M6 turn OFF and their channels
    turn ON
59 t5=t5_prim+tdead_SR;
60 Vx_t5=-(Vo+2*VFM-Vx_t4)*cos(Wres2*(t5-t5_prim))+(I_L_t5_prim/(2*C*Wres2))*sin(Wres2*(t5-t5_prim))+Vo+2*VFM;
61 I_L_t5=(2*C*Wres2)*(Vo+2*VFM-Vx_t4)*sin(Wres2*(t5-t5_prim))+I_L_t5_prim*cos(Wres2*(t5-t5_prim));
62 t6=Tsw-tdead/2; %the time at the
    end of Mode 7 when M2 turns OFF
63 Vx_t6=-(Vo-Vx_t5)*cos(Wres2*(t6-t5))+(I_L_t5/(2*C*Wres2))*sin(Wres2*(t6-t5))+Vo;
64 I_L_t6=(2*C*Wres2)*(Vo-Vx_t5)*sin(Wres2*(t6-t5))+I_L_t5*cos(Wres2*(t6-t5));
65 delta_t7=(1/Wres1)*asin((2*Cs*Wres1*(Vin+VFM))/(-I_L_t6)); %
    the amount of time that Mode 8 lasts
66 t7=t6+delta_t7; %
    the time at the end of mode 8
67 Vx_t7=Vx_t6; %
    the vx(t) at the end of mode 8

```

```

68 I_L_t7=-(2*Cs*Wres1)*(-Vo+Vx_t6)*sin(Wres1*(t7-t6))+I_L_t6*cos(Wres1*(t7-t6)); %
    the inductor current at the end of mode 8
69 t8=Tsw+tdead/2; %
    the time at the end of Mode 9 when the M1 channel turns ON which lasts after
    Tsw (Tsw+tdead/2)
70 Vx_t8=-(Vin+VFM+Vo-Vx_t7)*cos(Wres2*(t8-t7))+(I_L_t7/(2*C))*(1/Wres2)*sin(Wres2*(
    t8-t7))+(Vin+VFM+Vo);
71 I_L_t8=(2*C*Wres2)*(Vin+VFM+Vo-Vx_t7)*sin(Wres2*(t8-t7))+I_L_t7*cos(Wres2*(t8-t7))
    ;
72 delta_t9=(1/Wres2)*asin((-I_L_t8)/(2*C*Wres2*(Vin+Vo-Vx_t8))); %
    the amount of time that Mode 10 lasts
73 t9=t8+delta_t9;
74 t9_2=(Tsw+tdead/2)+delta_t9;
75 Vx_t9=-(Vin+Vo-Vx_t8)*cos(Wres2*(t9-t8))+(I_L_t8/(2*C))*(1/Wres2)*sin(Wres2*(t9-t8
    ))+(Vin+Vo);
76 I_L_t9=(2*C*Wres2)*(Vin+Vo-Vx_t8)*sin(Wres2*(t9-t8))+I_L_t8*cos(Wres2*(t9-t8)); %
77 t0_SR=t9-(Tsw); %
    time at the beginning of Mode 11
78 delta_t10_prim=(1/Wres3)*acos(((Vin+VFM-Vx_t9)-(Vo+2*VFM))/(Vin+VFM+Vo-Vx_t9)); %
    the time that Mode 11 last, when Cs3&Cs5 are fully discharged and Cs4&Cs6 are
    fully charged
79 t10_prim=t9+delta_t10_prim; %
    the time at the end of Mode 11
80 I_L_t10_prim=(Cs*Wres3)*(Vin+VFM+Vo-Vx_t9)*sin(Wres3*(t10_prim-t9)); %
    inductor current at the end of Mode 11
81 Vx_t10_prim=Vx_t9
82 t0_SR_prim=t0_SR+delta_t10_prim;
83 t10=t9+tdead_SR;
84 Vx_t10=-(Vin-(Vo+2*VFM+Vx_t9))*cos(Wres2*(t10-t10_prim))+(I_L_t10_prim/(2*C))*(1/
    Wres2)*sin(Wres2*(t10-t10_prim))+(Vin-(Vo+2*VFM));
85 I_L_t10=(2*C*Wres2)*(Vin-(Vo+2*VFM+Vx_t9))*sin(Wres2*(t10-t10_prim))+I_L_t10_prim*
    cos(Wres2*(t10-t10_prim));
86 for nt=1:length(t)
87     if t(nt)<=(tdead/2) % the time periode between 0 to
        tdead/2 (this is the continuation of Mode 9)
88         vx(nt)=-(Vin+VFM+Vo-Vx_t7)*cos(Wres2*(t(nt)+Tsw-t7))+(I_L_t7/(2*C))*(1/
            Wres2)*sin(Wres2*(t(nt)+Tsw-t7))+(Vin+VFM+Vo);
89         v_Lr(nt)=(Vin+VFM+Vo-Vx_t7)*cos(Wres2*(t(nt)+Tsw-t7))-(I_L_t7/(2*C))*(1/
            Wres2)*sin(Wres2*(t(nt)+Tsw-t7));
90         i_Lr(nt)=(2*C*Wres2)*(Vin+VFM+Vo-Vx_t7)*sin(Wres2*(t(nt)+Tsw-t7))+I_L_t7*
            cos(Wres2*(t(nt)+Tsw-t7));
91         vp(nt)=-Vo;
92         vs(nt)=Vo;
93         iM3(nt)=0;
94         iM4(nt)=i_Lr(nt);
95         V_A(nt)=Vin+VFM;
96         V_AX(nt)=V_A(nt)-vx(nt);
97         elseif t(nt) > tdead/2 && t(nt)<=t0_SR %the time periode from the
            moment M1 turns ON, current is still negative and M4 &M6 are still ON (Mode
            10). At the end of this mode current becomes zero and M4 &M6 turn OFF
98         vx(nt)=-(Vin+Vo-Vx_t8)*cos(Wres2*(t(nt)+Tsw-t8))+(I_L_t8/(2*C))*(1/Wres2)*
            sin(Wres2*(t(nt)+Tsw-t8))+(Vin+Vo);
99         v_Lr(nt)=(Vin+Vo-Vx_t8)*cos(Wres2*(t(nt)+Tsw-t8))-(I_L_t8/(2*C))*(1/Wres2)
            *sin(Wres2*(t(nt)+Tsw-t8));
100        i_Lr(nt)=(2*C*Wres2)*(Vin+Vo-Vx_t8)*sin(Wres2*(t(nt)+Tsw-t8))+I_L_t8*cos(
            Wres2*(t(nt)+Tsw-t8));
101        vp(nt)=-Vo;
102        vs(nt)=Vo;
103        iM3(nt)=0;
104        iM4(nt)=i_Lr(nt);
105        V_A(nt)=Vin;
106        V_AX(nt)=V_A(nt)-vx(nt);

```

```

107     elseif t(nt) > t0_SR && t(nt) <= t0_SR_prim %the time periode from the
moment M4 &M6 turns OFF until Cs3&Cs5 discharged, and Cs4&Cs6 charged (Mode
11)
108         vx(nt)=Vx_t9;
109         v_Lr(nt)=(Vin+Vo-Vx_t9)*cos(Wres3*(t(nt)+Tsw-t9));%-(I_L_t9/(Cs))*(1/Wres3
)*sin(Wres3*(t(nt)+Tsw-t9));
110         i_Lr(nt)=(Cs*Wres3)*(Vin+Vo-Vx_t9)*sin(Wres3*(t(nt)+Tsw-t9));%+I_L_t9*cos(
Wres3*(t(nt)+Tsw-t9));
111         vp(nt)=-(Vin+Vo-Vx_t9)*cos(Wres3*(t(nt)+Tsw-t9))+(Vin-Vx_t9);%+(I_L_t9/(Cs
))*(1/Wres3)*sin(Wres3*(t(nt)+Tsw-t9));
112         vs(nt)=Vo;
113         iM3(nt)=i_Lr(nt)/2;
114         iM4(nt)=i_Lr(nt)/2;
115         V_A(nt)=Vin;
116         V_AX(nt)=V_A(nt)-vx(nt);
117     elseif t(nt) > t0_SR_prim && t(nt) <= t0 %the time periode during which
the body diodes of M3&M5 conduct (Mode 12)
118         vx(nt)=-(Vin-(Vo+2*VFM+Vx_t9))*cos(Wres2*(t(nt)+Tsw-t10_prim))+(
I_L_t10_prim/(2*C))*(1/Wres2)*sin(Wres2*(t(nt)+Tsw-t10_prim))+(Vin-(Vo+2*VFM))
;
119         v_Lr(nt)=(Vin-(Vo+2*VFM+Vx_t9))*cos(Wres2*(t(nt)+Tsw-t10_prim))-(
I_L_t10_prim/(2*C))*(1/Wres2)*sin(Wres2*(t(nt)+Tsw-t10_prim));
120         i_Lr(nt)=(2*C*Wres2)*(Vin-(Vo+2*VFM+Vx_t9))*sin(Wres2*(t(nt)+Tsw-t10_prim
))+I_L_t10_prim*cos(Wres2*(t(nt)+Tsw-t10_prim));
121         vp(nt)=Vo+2*VFM;
122         vs(nt)=Vo;
123         iM3(nt)=i_Lr(nt);
124         iM4(nt)=0;
125         V_A(nt)=Vin;
126         V_AX(nt)=V_A(nt)-vx(nt);
127     elseif t(nt) > t0 && t(nt) <= t1 %mode 1
128         vx(nt)=(-Vin+Vo+Vx_t0)*cos(Wres2*(t(nt)-t0))+(I_L_t0/(2*C))*(1/Wres2)*sin(
Wres2*(t(nt)-t0))-(-Vin+Vo);
129         v_Lr(nt)=(-Vin+Vo+Vx_t0)*cos(Wres2*(t(nt)-t0))-(I_L_t0/(2*C))*(1/Wres1)*
sin(Wres2*(t(nt)-t0));
130         i_Lr(nt)=-(2*C*Wres2)*(-Vin+Vo+Vx_t0)*sin(Wres2*(t(nt)-t0))+I_L_t0*cos(
Wres2*(t(nt)-t0));
131         vp(nt)=Vo;
132         vs(nt)=Vo;
133         iM3(nt)=i_Lr(nt);
134         iM4(nt)=0;
135         V_A(nt)=Vin;
136         V_AX(nt)=V_A(nt)-vx(nt);
137     elseif t(nt) > t1 && t(nt) <= t2 %mode 2
138         vx(nt)=Vx_t1;
139         v_Lr(nt)=(-Vin+Vo+Vx_t1)*cos(Wres1*(t(nt)-t1))-(I_L_t1/(2*Cs*Wres1))*sin(
Wres1*(t(nt)-t1));
140         i_Lr(nt)=-(2*Cs*Wres1)*(-Vin+Vo+Vx_t1)*sin(Wres1*(t(nt)-t1))+I_L_t1*cos(
Wres1*(t(nt)-t1));
141         vp(nt)=Vo;
142         vs(nt)=Vo;
143         iM3(nt)=i_Lr(nt);
144         iM4(nt)=0;
145         V_A(nt)=(-Vin+Vo+Vx_t1)*cos(Wres1*(t(nt)-t1))-(I_L_t1/(2*Cs*Wres1))*sin(
Wres1*(t(nt)-t1))+(Vo+Vx_t1);
146         V_AX(nt)=V_A(nt)-vx(nt);
147     elseif t(nt) > t2 && t(nt) <= t3 %mode 3
148         vx(nt)=(Vo+VFM+Vx_t1)*cos(Wres2*(t(nt)-t2))+(I_L_t2/(2*C*Wres2))*sin(Wres2
*(t(nt)-t2))-(Vo+VFM);
149         v_Lr(nt)=-(Vo+VFM+Vx_t1)*cos(Wres2*(t(nt)-t2))-(I_L_t2/(2*C*Wres2))*sin(
Wres2*(t(nt)-t2));

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150     i_Lr(nt)=-(2*C*Wres2)*(Vo+VFM+Vx_t1)*sin(Wres2*(t(nt)-t2))+I_L_t2*cos(
Wres2*(t(nt)-t2));
151     vp(nt)=Vo;
152     vs(nt)=Vo;
153     iM3(nt)=i_Lr(nt);
154     iM4(nt)=0;
155     V_A(nt)=VFM;
156     V_AX(nt)=V_A(nt)-vx(nt);
157     elseif t(nt) > t3 && t(nt) <= t4 %mode 4
158         vx(nt)=(Vo+Vx_t3)*cos(Wres2*(t(nt)-t3))+(I_L_t3/(2*C*Wres2))*sin(Wres2*(t(
nt)-t3))-Vo;
159         v_Lr(nt)=-(Vo+Vx_t3)*cos(Wres2*(t(nt)-t3))-(I_L_t3/(2*C*Wres2))*sin(Wres2
*(t(nt)-t3));
160         i_Lr(nt)=-(2*C*Wres2)*(Vo+Vx_t3)*sin(Wres2*(t(nt)-t3))+I_L_t3*cos(Wres2*(t
(nt)-t3));
161         vp(nt)=Vo;
162         vs(nt)=Vo;
163         iM3(nt)=i_Lr(nt);
164         iM4(nt)=0;
165         V_A(nt)=0;
166         V_AX(nt)=V_A(nt)-vx(nt);
167         elseif t(nt) > t4 && t(nt) <= t5_prim %mode 5 & 6
168             vx(nt)=Vx_t4;
169             v_Lr(nt)=-(Vo+Vx_t4)*cos(Wres3*(t(nt)-t4));
170             i_Lr(nt)=-(Cs*Wres3)*(Vo+Vx_t4)*sin(Wres3*(t(nt)-t4));
171             vp(nt)=(Vo+Vx_t4)*cos(Wres3*(t(nt)-t4))-Vx_t4;
172             vs(nt)=Vo;
173             iM3(nt)=i_Lr(nt)/2;
174             iM4(nt)=i_Lr(nt)/2;
175             V_A(nt)=0;
176             V_AX(nt)=V_A(nt)-vx(nt);
177             elseif t(nt) > t5_prim && t(nt) <= t5 %mode 5 & 6
178                 vx(nt)=-(Vo+2*VFM-Vx_t4)*cos(Wres2*(t(nt)-t5_prim))+(I_L_t5_prim/(2*C*
Wres2))*sin(Wres2*(t(nt)-t5_prim))+(Vo+2*VFM);
179                 v_Lr(nt)=(Vo+2*VFM-Vx_t4)*cos(Wres2*(t(nt)-t5_prim))-(I_L_t5_prim/(2*C*
Wres2))*sin(Wres2*(t(nt)-t5_prim));
180                 i_Lr(nt)=(2*C*Wres2)*(Vo+2*VFM-Vx_t4)*sin(Wres2*(t(nt)-t5_prim))+
I_L_t5_prim*cos(Wres2*(t(nt)-t5_prim));
181                 vp(nt)=-Vo-2*VFM;
182                 vs(nt)=Vo;
183                 iM3(nt)=0;
184                 iM4(nt)=i_Lr(nt);
185                 V_A(nt)=0;
186                 V_AX(nt)=V_A(nt)-vx(nt);
187                 elseif t(nt) > t5 && t(nt) <= t6 %mode 7
188                     vx(nt)=-(Vo-Vx_t5)*cos(Wres2*(t(nt)-t5))+(I_L_t5/(2*C*Wres2))*sin(Wres2*(t
(nt)-t5))+Vo;
189                     v_Lr(nt)=(Vo-Vx_t5)*cos(Wres2*(t(nt)-t5))-(I_L_t5/(2*C*Wres2))*sin(Wres2*(
t(nt)-t5));
190                     i_Lr(nt)=(2*C*Wres2)*(Vo-Vx_t5)*sin(Wres2*(t(nt)-t5))+I_L_t5*cos(Wres2*(t
(nt)-t5));
191                     vp(nt)=-Vo;
192                     vs(nt)=Vo;
193                     iM3(nt)=0;
194                     iM4(nt)=i_Lr(nt);
195                     V_A(nt)=0;
196                     V_AX(nt)=V_A(nt)-vx(nt);
197                     elseif t(nt) > t6 && t(nt) <= t7 %mode 8
198                         vx(nt)=Vx_t6;
199                         v_Lr(nt)=(-Vo+Vx_t6)*cos(Wres1*(t(nt)-t6))-(I_L_t6/(2*Cs*Wres1))*sin(
Wres1*(t(nt)-t6));

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200     i_Lr(nt)=-(2*Cs*Wres1)*(-Vo+Vx_t6)*sin(Wres1*(t(nt)-t6))+I_L_t6*cos(Wres1
201     *(t(nt)-t6));
202     vp(nt)=-Vo;
203     vs(nt)=Vo;
204     iM3(nt)=0;
205     iM4(nt)=i_Lr(nt);
206     V_A(nt)=(-Vo+Vx_t6)*cos(Wres1*(t(nt)-t6))-(I_L_t6/(2*Cs*Wres1))*sin(Wres1
207     *(t(nt)-t6))+(-Vo+Vx_t6);
208     V_AX(nt)=V_A(nt)-vx(nt);
209     elseif t(nt) > t7 && t(nt) <= Tsw %mode 9
210     vx(nt)=-(Vin+VFM+Vo-Vx_t7)*cos(Wres2*(t(nt)-t7))+(I_L_t7/(2*C))*(1/Wres2)*
211     sin(Wres2*(t(nt)-t7))+(Vin+VFM+Vo);
212     v_Lr(nt)=(Vin+VFM+Vo-Vx_t7)*cos(Wres2*(t(nt)-t7))-(I_L_t7/(2*C))*(1/Wres2)
213     *sin(Wres2*(t(nt)-t7));
214     i_Lr(nt)=(2*C*Wres2)*(Vin+VFM+Vo-Vx_t7)*sin(Wres2*(t(nt)-t7))+I_L_t7*cos(
215     Wres2*(t(nt)-t7));
216     vp(nt)=-Vo;
217     vs(nt)=Vo;
218     iM3(nt)=0;
219     iM4(nt)=i_Lr(nt);
220     V_A(nt)=Vin+VFM;
221     V_AX(nt)=V_A(nt)-vx(nt);
222     else
223     vx(nt)=0;
224     v_Lr(nt)=0;
225     i_Lr(nt)=0;
226     vp(nt)=0;
227     vs(nt)=0;
228     iM3(nt)=i_Lr(nt);
229     iM4(nt)=i_Lr(nt);
230 end
231 end

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