Politecnico di Torino

Master's Thesis

Power Converters Investigation for Hybrid Supercapacitors and Battery Storage System Test Bench

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Chapter 1: Introduction

1.1 Background and Motivation

The increasing integration of renewable energy sources such as photovoltaic (PV) system has created a growing demand for efficient and reliable energy storage solutions. renewable energy generation is inherently intermittent and variable, which makes energy storage essential for ensuring system stability, power quality, and continuous energy supply.

Among the available energy storage technologies, supercapacitors have attracted significant attention due to their unique characteristics. Unlink conventional batteries, supercapacitors store energy through an electrostatic mechanism, which enables very fast charge and discharge processes.

As a result, they offer high power density, long cycle life, and safe operation without thermal runaway risks. These properties make them particularly suitable for applications requiring rapid dynamic response. However, despite these advantages, supercapacitors also present several limitations. Their energy density is relatively low compared to batteries, and their electrical behaviour is highly nonlinear. In addition, accurate estimation of key parameters such as state of charge (SoC) and state of health (SoH) remains challenging. These limitations highlight the need for proper characterization and modelling of supercapacitors in order to ensure their effective use in practical systems.

1.2 Supercapacitor Characterization and Modelling Challenges

To integrate supercapacitors into-world applications, it is essential to accurately characterize their electrical behaviour. This process, often referred to as metrology, involves the measurement of key parameters such as capacitance, equivalent series resistance (ESR), stored energy, and power capability. These parameters directly influence the performance, efficiency, and reliability of the system. In addition to basic electrical quantities, advanced applications require reliable methods to estimate the state of charge and state of health of supercapacitors. Unlike batteries, where voltage can be used as an approximate indicator of charge level, supercapacitors exhibit a nonlinear relationship between voltage and stored energy. This makes SoC ad SoH estimation more complex and requires more sophisticated modelling approaches.[8]

To address this challenges, several electrical models have been developed to represent the behaviour of supercapacitors. Equivalent circuit models are widely adapted because of their simplicity and suitability for simulation and control applications. These models describe important characteristics such as internal resistance, capacitance variation, self-discharge effects, and dynamic response. Accurate modelling is essential for performance prediction and for the design of reliable energy management strategies [3] , [8].

The ideal representation is a ideal capacitor model, which assumes constant capacitance and no losses. More realistic models include an equivalent series resistance to account for voltage drops and energy dissipation.

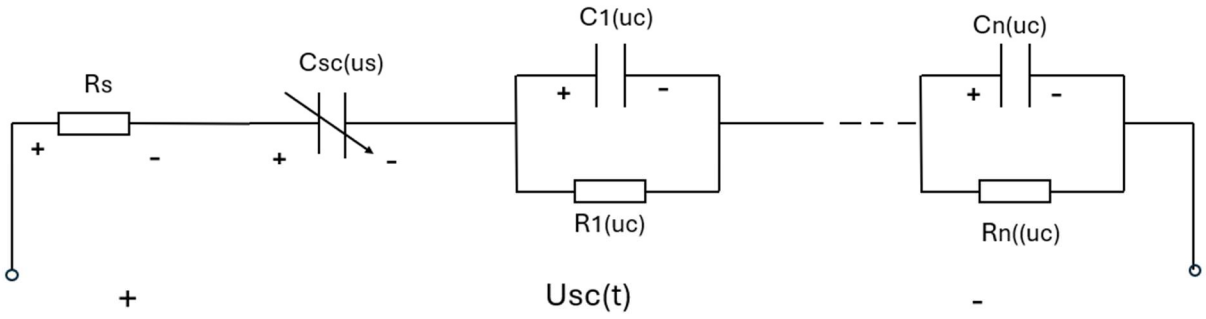


Figure 1. 1 advanced equivalent circuit model of a supercapacitor

Source: reproduce from [3]

In addition to simple equivalent circuit models, several advanced modelling approaches have been proposed in the literature to describe the supercapacitors behaviour with higher accuracy and physical detail. These models aim to capture complex internal phenomenon and nonlinear dynamics that cannot be fully represented by simple electrical circuits.

Examples of advanced modelling approaches include:

- Fractional-order models, which are used to represent the distributed and frequency-dependent behaviour of supercapacitors more accurately.
- Intelligent models, such as data -driven and machine learning-based methods, which rely on experimental data to estimate system behaviour.
- Electrochemical models, which describe the internal physical and chemical processes occurring within the electrodes and electrolyte.

Although these models can provide improved accuracy, they are generally more complex and computationally intensive. Therefore, equivalent circuit models remain the most commonly used approach in engineering applications due to their simplicity and suitability and control design. [7]

1.3 Dynamic Behaviour and Self-Discharge

The dynamic behaviour of supercapacitors plays a crucial role in their performance. During operation, the voltage across the supercapacitor varies continuously as energy is stored or released. This behaviour can be described using classical capacitor equations, where the current is proportional to the rate of change of voltage.[3],[7]

In addition to normal charge and discharge processes, supercapacitors also exhibit self-discharge behaviour, meaning that they gradually lose stored energy even when disconnected from the load. This phenomenon is typically modelled using a leakage resistance in parallel with the capacitor. The presence of this leakage path cause the voltage to decay over time, following an exponential behaviour.[3],[8]

Understanding both dynamic response and self-discharge characteristics is essential for accurate system modelling and for designing energy management strategies.[3],[8]

1.4 Hybrid Energy Storage Systems

Due to the complementary characteristics of batteries and supercapacitors, hybrid energy storage systems have been proposed as an effective solution for modern energy applications. Batteries provide high energy density and are ideal for handling fast transient loads.[1],[2],[5]

By combining these two technologies, hybrid systems can be benefit from both high energy capacity and rapid response capability. In such configurations, the battery typically supplies the average power demand, while the supercapacitor handles peak power and transient fluctuations this approach improves overall system efficiency, reduces stress on the battery, and extends its lifetime.[2]

Hybrid energy storage systems are particularly relevant in renewable energy applications, where power fluctuations are frequent and efficient energy management is critical.[5]

1.5 Objective of the Thesis

The main objective of this thesis is the design and analysis of a hybrid energy storage system based on a supercapacitor and a battery, supported by appropriate power electronics converters. In particular, the focus is placed on the development of a bidirectional energy transfer system using a buck converter for charging the supercapacitor and a boost converter for discharging the supercapacitor to supply energy to the battery.

The work primarily involves the modelling, design, and analysis of the buck and boost converters, including their operating principles, control considerations, and performance under different conditions. The supercapacitor is used to handle high-power and transient energy, while the battery is responsible for long-term energy storage.

The objective is to ensure efficient energy transfer between the storage elements, improve system performance, and enable proper integration of hybrid storage system within modern energy applications.

Chapter2: Energy Storage Systems

2.1 Introduction to Battery Energy Storage System(BESS)

Battery energy storage systems (BESS) are electrochemical devices that store electrical energy in chemical form and release it when required. They play a crucial role in modern power systems, especially in renewable energy applications such as photovoltaic(PV) and wind systems.
Due to the intermittent nature of renewable sources, energy generation is not always aligned with load demand. Batteries help overcome this limitation by storing excess energy during periods of high generation and supplying it when production is insufficient or unavailable. This improves system reliability, stability, and continuity of power supply.
BESS are widely used in standalone and grid-connected systems for applications such as energy management, frequency regulation, and backup power supply.[1],[5]

2.2.Key Battery Parameters

The main parameters characterizing batteries are explained in the following[1],[5]

1) Energy capacity

The stored energy in a battery is given by:

$$E = V * Ah$$

Where:
E = energy (Wh)
V = voltage (V)
Ah =capacity (Ah)

Energy density indicates how long the battery can supply power.

2) Power capability

Determines how fast energy can be delivered.

$$P = V * I$$

3) Energy Density
Measures how much energy is stored per unit mass.

$$\text{Energy density} = \frac{E}{mass} \text{ (wh/kg)}$$

4) Power Density
Indicates how quickly energy can be supplied.

$$\text{Power density} = \frac{P}{mass} \text{ (W/kg)}$$

5) State of Charge
Represents the available energy in the battery.

$$\text{SOC} = \frac{Q_{remaining}}{Q_{nominal}} * 100$$

6) Depth of Discharge

Indicates how much energy has been used.

$$DoD = 100$$

7) Efficiency

Represents losses during charging/discharging.

$$\eta = \frac{Energy_{out}}{Energy_{in}}$$

8) Cycle life

Number of charge/discharge cycles before performance degrades.

2.3.Battery Classifications

Batteries are mainly classified based on their electrochemical composition[4].

a) Lead-Acid Batteries

- Mature and low cost technology.
- Low energy density.
- Limited cycle life.
- Widely used in backup systems.

b) Lithium-Ion Batteries

- High energy density ($\sim 150\ wh/kg$)
- High efficiency and long cycle life.
- Low self-discharge
- Higher cost
- Widely used in Evs and renewable energy.

c) Nickel-Based Batteries (Ni_cd , Ni_MH)

- Good reliability and wide temperature operation
- Moderate energy density
- Environmental concerns(Ni-Cd)

d) Sodium-Based Batteries(Na-S,ZEBRA)

- High energy density
- Suitable for large-scale storage
- Required high operation temperatures

e) Flow Batteries(e.g., Vanadium Redox)

- Energy stored in liquid electrolytes
- Very long cycle life
- Suitable for grid applications

Table 2.1 comparison between different types of Batteries

Battery Type	Energy Density	Power capability	Cycle Life	Main Application
Lead-Acid	Low	Medium	Low	Backup systems
Lithium-Ion	High	High	High	Evs, PV systems
Ni-Cd/Ni-MH	Medium	High	High	Industrial
Na-S/ZEBRA	High	Medium	High	Grid storage
Flow Batteries storage	Medium	Medium	Very High	Large scale

Source: Author

2.4. Electrical Model of a Battery

The electrical behaviour of a battery can be represented using a simple equivalent circuit consisting of an ideal voltage source in series with an internal resistance. The voltage source models the open-circuit voltage of the battery, which depends on the state of the charge, while series resistance represents internal losses due to electrochemical processes and connections.[4]

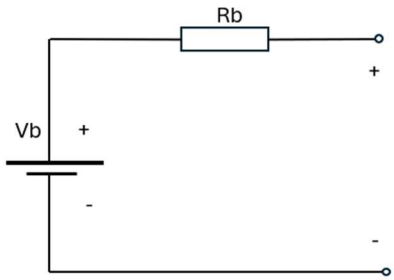


Figure 2.1. electrical equivalent circuit of the battery model
Source: reproduce from [4]

However, batteries are not well-suited for handling rapid power fluctuations, which can accelerate degradation and reduce lifetime.

2.5. Introduction to Supercapacitors:

Supercapacitors, also referred to as ultracapacitors or electromechanical capacitors, are advanced energy storage devices that bridge the gap between batteries and conventional capacitors with regards to energy and power densities. They combine the high power capability of traditional capacitors with a significantly higher energy storage capacity, making them highly suitable for modern energy systems.
Unlike batteries, where energy is stored through electromechanical reactions, SCs store energy electrostatically at the electrode_electrolyte interface . this mechanism enables fast charge and discharge processes, high efficiency, and excellent reversibility, and charging-discharging cycle can be repeated frequently and without limits.

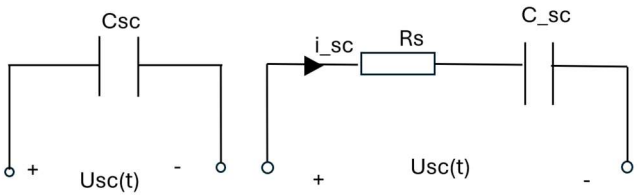
One of the key advantages of SCs is their high power density, which allows them to respond rapidly to transient power demands. However, their energy density is lower than of batteries, which limits their use as a standalone long-term energy storage device. For this reason SCs are often integrated into hybrid energy storage systems, where they complement batteries by handling peak power demands are reducing stress on battery components.[5],[6],[7]

2.5.1 Applications:

Due to their unique properties, SCs are widely used in applications requiring high power density and fast dynamic response, such as electric and hybrid vehicles, renewable energy systems, grid connected systems. Their role is particularly important in systems with fluctuating power profiles, where rapid energy exchange is essential for maintaining system stability and efficiency.[7],[5]

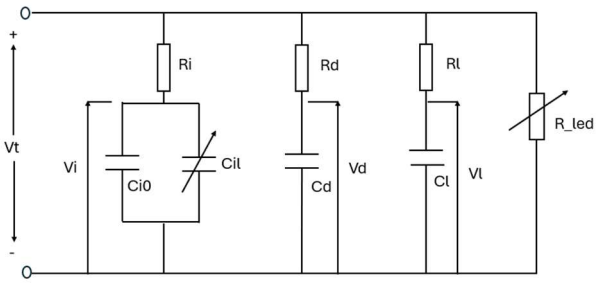
2.5.2 Electrical Model of SCs:

For practical engineering applications, especially in power electronic system and simulation, equivalent circuit models are widely adopted due to their simplicity and effectiveness. SCs exhibit non_ideal behaviour characterized by internal resistance, voltage dependence capacitance, and self_discharg effects. These characteristics require proper modelling approaches, ranging from ideal equivalent circuit models to realistic model.
The ideal model consists of a single capacitance C_{sc}, which assumes perfect energy storage with no losses. However, this model can not accurately describe dynamic behaviour during charge and discharge.
The better representations is non-ideal model includes a series resistance R_s, accounting for internal losses(also known for ESR), which cause voltage drop and power dissipation. This model provides a more accurate description of transient response and efficiency, especially in high-power applications. For higher accuracy, multi-branch models are used to capture short term, and long term dynamic behaviour, as well as self-discharge effects [3],[6],[8].



(a) (b)

Figure 2.2. Common supercapacitor models: (a) ideal model ; (b) nonideal model
Source: reproduce from [1], Supercapacitor energy storage for power system applications



c) multi-branch model

Source: reproduce from [2], metsupercap: metrology for static and dynamic characterisation of supercapacitors

2.5.3 Classification of Supercapacitors:

Supercapacitors can be classified according to their electrode materials, electrolyte type, and energy storage mechanisms. These classifications are essential for understanding their electrical performance, operational characteristics [6], [8].

2.5.4 Different Types of Supercapacitors:

a) Based on electrode materials

According to the materials used in electrodes, supercapacitors are categorized into three main types [6],[8] :

- **Symmetric Supercapacitors**
  Both electrodes are made of the same material, typically carbon-based, and operate mainly through electric double-layer capacitance(EDLC).

- **Asymmetric supercapacitors**
  The two electrodes are composed of different materials, combining double-layer and pseudo capacitive behaviours to improve energy density.

- **Hybrid supercapacitors**
  These devices integrate a capacitor-type electrode with a battery-type electrode, enabling higher energy density while maintaining relatively high power capability.

b) Based on electrolyte type

Depending on the electrolyte used, supercapacitors are classified as [6],[8]:

- **Organic electrolyte-based supercapacitors**

Provide higher operating voltage and improved energy density.

- **Aqueous electrolyte-based supercapacitors**
  Offer higher ionic conductivity and lower cost but are limited by lower voltage.

- **Ionic liquids**
  Allow very high voltage operation but are more expensive and still under development.

c) Based on storage mechanism

From the perspective of charge storage mechanism, supercapacitors are divided into:

- **Electric double-layer capacitors (EDLCs)**

Store energy through electrostatic charge separation at the electrode-electrolyte interface.

- **Pseudo capacitors**

Store energy via fast and reversible surface redox reactions.

- **Hybrid supercapacitors**

Combine both electrostatic and faradic mechanisms to achieve improved energy and power performance.

2.5.5 Operation Principle:

SCs operate based on the electrostatic storage of energy at the interface between the electrode and the electrolyte. A typical supercapacitor consist of two porous electrodes separated by an ion-

permeable membrane and immersed in an electrolyte. When a voltage is applied, ions in the electrolyte migrate toward The electrode surfaces, forming an electrical double layer(EDL). This process does not involve bulk chemical reactions, which enables fast charge-discharge capability, high efficiency, and long cycle life. The physical structure and charge distribution mechanism of a supercapacitor are illustrated in Figure 2.3 [6].

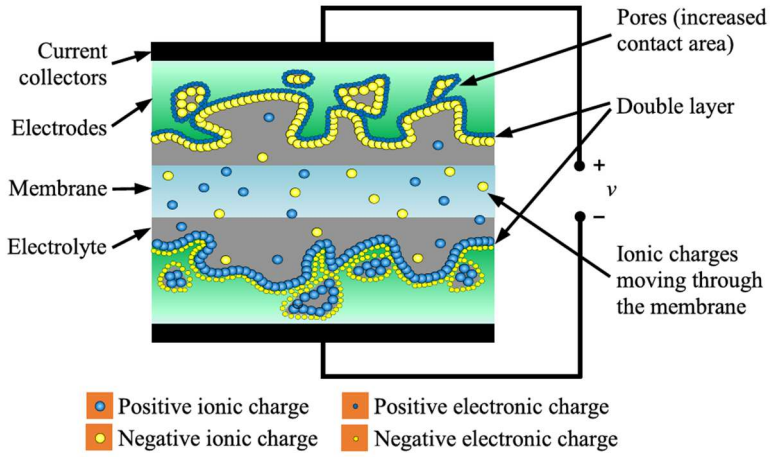


Figure 2.3. Operation principle and structure of a supercapacitor cell
Source: reproduce from [6]

The membrane enables ion movement between the electrodes while preventing direct electrical contact, thus avoiding short circuits.

2.5.6 Electrical Characteristics of Supercapacitors

The electrical performance of supercapacitors is governed by voltage-dependence capacitance, electrode-electrolyte interactions, and environmental conditions, all of which must be considered in system-level applications [6].

a) Voltage-dependence capacitance

Supercapacitors exhibit electrical behaviour that differs from conventional capacitors due to their unique energy storage mechanism. One of their most important characteristics is that the capacitance is not constant but varies with applied voltage. Unlike ideal capacitors, where capacitance remains fixed, SCs show nonlinear relationship between stored charge and voltage, due to the formation of the electrical double layer at the electrode-electrolyte interface.
To describe this behaviour more accurately ,differential capacitance is introduced, defined as

$$C_{dif} = \frac{d_q}{d_v}$$

This parameter represents the variation of stored charge with respect to voltage and is more suitable for describing supercapacitor behaviour than the conventional definition of capacitance:

$$C = \frac{q}{v}$$

As a result, SCs are often modelled as a nonlinear device whose electrical response depends on operating conditions.[6]

b) Interaction between electrodes and electrolyte

Another important factor affecting performance is the interaction between the electrode and electrolyte. supercapacitor electrodes are typically porous to maximize the available surface area for charge storage. The ability of ions to access these pores depends on the compatibility between pores size and ion size, which directly influences the effective capacitance. Therefore, proper matching between electrode structure and electrolyte properties is essential for optimal performance. Furthermore, the very small separation distance between charges at the interface, known as the Debay length, contributes to high capacitance of supercapacitors compared to conventional capacitors.[6]

c) Temperature

Temperature also effects supercapacitor performance. Variation in temperature influence electrolyte conductivity and ion mobility , which may alter capacitance, and overall efficiency. High temperatures can accelerate ageing processes, while very low temperatures may reduce power capability. [6]

2.5.7 Supercapacitor Sizing

The sizing of supercapacitor is mainly based on the energy requirement of the system. The selected supercapacitor must be able to supply or absorb the required amount of energy within the allowed operating voltage range. The energy stored in a supercapacitor is given by:

$$\mathrm{E} = \frac{1}{2}\ \mathrm{C}\ \mathrm{V}^2$$

However, in practical applications, the supercapacitor does not operate over the full voltage range. Instead, it operates between a maximum voltage V_{max} and a minimum voltage V_{min} [3], therefore the useable energy can be expressed as :

$$E_{usable} = \frac{1}{2}\mathrm{C}\ (V_{max}^2\ -\ V_{min}^2)$$

From this expression, the required capacitance can be calculated as:

$$C\ = \frac{2E_{req}}{V_{max}^2\ -\ V_{min}^2}$$

This equation shows that a wider voltage operation range reduces the required capacitance, while a narrower voltage range requires a larger capacitance for the same energy demand.
The choice of V_{max} and V_{min} depends on several design constraints, including the rated voltage of the supercapacitor, the converter operating limits, the DC-bus voltage requirements, and system stability considerations. Typically, V_{max} is selected according to the rated voltage of the supercapacitor, while V_{min} is chosen according to the minimum acceptable operating voltage of the system [3].

2.5.8 Power Capability (ESR Effects)

The maximum power capability of a supercapacitor is limited by its equivalent series resistance (ESR) when current flows through the supercapacitor , the ESR causes internal power dissipation and

produces a voltage drop that reduces the effective voltage available at the output. The maximum theoretical power can be approximated by:

$$P_{max} = \frac{V^2}{4R_s}$$

The voltage drop caused by the ESR is given by :

$$V_{drop} = I \,.\, R_s$$

Therefore, the actual output voltage becomes:

$$V_{out} = V_{sc} - IR_s$$

This shows that higher current values produce larger voltage drops. For this reason, the design must ensure that the output voltage remains above the minimum allowable operating voltage [3]:

$$V_{out} \geq V_{min}$$

the current requirement can be estimated from the power demand using :

$$P = V.I$$

So current is:

$$\mathrm{I} = \frac{\mathrm{P}}{\mathrm{V}}$$

The calculated current should satisfy the ESR limitation and the thermal constraints of the selected supercapacitor. In addition the power dissipated in the ESR can be expressed as [3]:

$$P_{loss} = I^2.R_s$$

As a result, The overall efficiency can be approximated as [3]:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}}$$

This analysis shows that the ESR has a direct impact on voltage drop, power losses, thermal behaviour, and efficiency. Therefore, a supercapacitor with lower ESR is preferable for high-current and high-power applications.

2.5.9 Energy- Voltage Relationship

Since the energy stored in a supercapacitor is proportional to the square of its voltage, a significant portion of the available energy is stored at higher voltage levels. Therefore , the selected operating voltage range strongly affects the usable energy of the storage system. Consequently , choosing suitable minimum and maximum voltage limits is essential for both energy utilization and converter design.[3]

2.5.10 Selected Supercapacitor Model Characteristics

To ensure a realistic implementation of the proposed hybrid energy storage system, a commercial supercapacitor module has been selected based on its datasheet specifications. The chosen device is an Eaton XLM supercapacitor module with a nominal capacitance of 130F and operating voltage in the range of 62V to 69V. the key electrical characteristics of the module, including equivalent series resistance (ESR), sored energy, peak power capability, and current ratings, are summarized in table.1.2. these parameters are essential for accurately modelling the behaviour of the supercapacitor and evaluating its interaction with the buck and boost converters during charging and discharging processes.

Table 2.2 – Electrical characteristics of selected XLM supercapacitor module

parameter	**value**
Capacitance	130 F
Maximum Working Voltage	62.1 – 69 V
Maximum Initial ESR	6.7 $m\Omega$
Nominal Leakage Current	128 - 144 mA
Stored Energy	69.6 – 86 Wh
Peak Power	143.9 – 186 kW
Pulse Current	2157 – 2440 A
Short Circuit Current	9300 A – 10800 A
Operating Temperature Range	-40 ℃ to +65 ℃

Source: Adapted from Eaton corporation, XLM supercapacitor module Datasheet [9]

2.5.11 Complementary Characteristics of Batteries and Supercapacitors

Batteries and supercapacitors exhibit complementary characteristics that make them suitable for hybrid energy storage applications. Batteries provide high energy density, enabling long-term energy storage, but they have limited power capability and slower dynamic response. In contrast, charge-discharge capability , although their energy storage capacity is lower.
The combination of these characteristics motivates the integration of both technologies into Hybrid Energy Storage (HESS), where batteries supply sustained energy demands while supercapacitors handle transient power fluctuations and peak power requirements.

2.6. Introduction to Hybrid Energy Storage System (HESS)

A Hybrid Energy storage system (HESS) is formed by combining two or more energy storage technologies, typically batteries and supercapacitors, to exploit their complementary characteristics.

In renewable energy systems-especially photovoltaic (PV) systems, power generation is inherently intermittent and variable due to changes in solar irradiance and load demand. A single storage technology is often not sufficient to handle both long-term energy supply and short-term power fluctuations efficiently. Therefore, a hybrid system combines the strengths of both technologies while mitigating their individual limitations [9], [10].

In this context, a HESS integrates:

- Battery Energy Storage system (BESS) : provides high energy density and long-duration energy support.
- Supercapacitor Energy Storage System : provides high power density and rapid transient response.

This combination allows the system to :

- Provide stable energy supply
- Handle fast transient power demands
- Improve overall system performance and efficiency

2.6.1 Role of Each Component

a) Battery :

- Supplies average / continuous power
- Stores energy for long duration
- Used for energy balancing

b) Supercapacitor:

- Supplies peak power
- Responds to fast transients
- Protects battery from stress [9],[10]

2.6.2 Advantages of HESS

- Improved power and energy management
- Enhanced system reliability
- Increased cycle life of the battery
- Better efficiency under dynamic conditions
- Capability to handle peak power demands
- Reduced battery degradation
- Improved DC bus voltage stability
- Better integration with renewable sources (PV) [9], [10]

Chapter 3: Complete Test System Overview

This chapter presents the complete test system developed to evaluate the proposed hybrid storage architecture. The system integrates a photovoltaic source , a hybrid storage unit composed of a battery and a supercapacitor, a bidirectional DC-DC converter, a control strategy, and a dynamic load. The objective of the test system is to reproduce realistic operating conditions in which both the input generation and the load demand vary with time, allowing the interaction between the storage elements and the converter to be analysed under transient and steady-state conditions.

In the proposed architecture, the photovoltaic source is connected to a common DC bus and represents the primary energy input. The battery and the supercapacitor are interfaced with the same bus through bidirectional DC-DC conversion stages, enabling controlled charging and discharging. The battery is intended to supply the average or long term energy demand, while the supercapacitor is used to compensate for rapid power variations thanks to its high power density and fast dynamic response. As a result, the complete test system makes it possible to study power sharing, bus voltage stabilization, and converter operation under realistic conditions.

3.1 Photovoltaic Source Modelling

The photovoltaic subsystem is composed of two main parts:
The irradiance profile generator and the electrical model of PV panel. The irradiance is modelled using multiple step blocks whose sum produces a staircase waveform representing time-varying G(t). This signal does not represent the photovoltaic panel itself, but rather the external input corresponding to solar radiation.
The generated irradiance is then used as an input to the PV model, which converts it into an electrical output such as current and voltage based on the equivalent circuit representation. In this work, a simplified electrical representation is adopted, where the irradiance is scaled to produce a current reference, taking into account the measured DC bus voltage . therefore, the step-based subsystem defines the operating conditions, while the PV model describes the electrical behaviour of the source. To prevent instability during simulation, particularly when the bus voltage becomes very small, a protection stage is introduced using a Max block. This block compares the measured bus voltage with a minimum reference value and ensure that denominator used in the scaling never reaches zero. The irradiance signal then processed by a divider and multiplier block in order to generate the photovoltaic current reference. In this way, higher irradiance results in higher injected current, while the scaling also accounts for the measured bus voltage [11], [12].

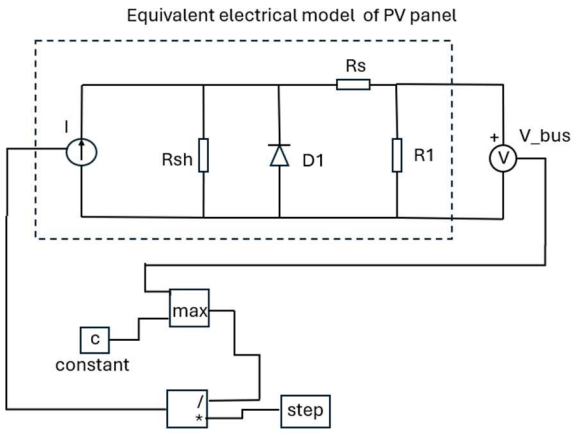


Figure 3.1 PV electrical model of the PV panel with irradiance input generation for dynamic operating condition
Source : Author's own work

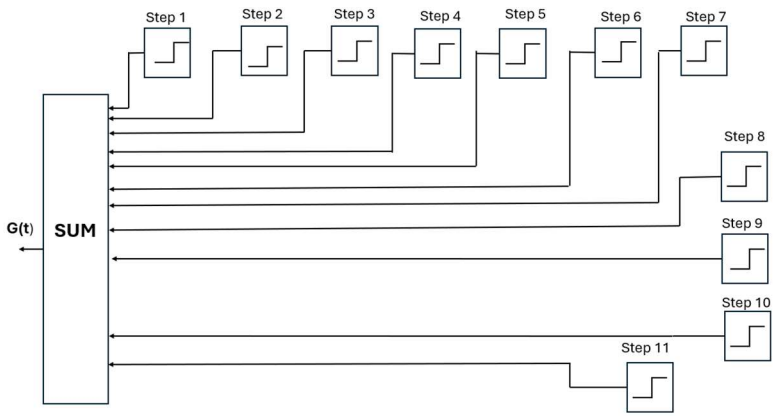


Figure 3.2 Time-varying irradiance generation using multiple step function

Source: Author's own work

The step values that used:

Table 3.1 step variation of solar irradiance used for PV model simulation

Step #	Time(S)	Irradiance level(W/m^2)
Step 1	5	800
Step 2	7	400
Step 3	10	50
Step 4	12	600
Step 5	14	300
Step 6	18	400
Step 7	20	10
Step 8	22	300
Step 9	24	200
Step 10	30	300
Step 11	1	10

Source : Author's own work

3.2 Bidirectional Converter

The bidirectional converter represents the main power electronics interface between the input DC source and the supercapacitor bank. Its function is to control the direction and amount of energy exchanged between these two sides of the system.

3.2.1 Converter Structure

The bidirectional converter is implemented using a half-bridge switching structure in which two switches are connected in series to form a switching pole. The midpoint of the switching pole is connected to an inductor, while the upper and lower nodes are associated with the voltage port and the current port of the converter. Depending on the direction of energy flow, the same physical structure can operate either as buck converter or as a boost converter.

The modelling framework is based on the unitary switching function, averaged expressions over the switching period, and PWM generation. This common framework is used in both operating modes, while the inductor voltage expressions and the conversion ratio change according to the energy flow direction. Such a formulation is well suited for simulation and design because it directly links the switching process to the average converter behaviour .

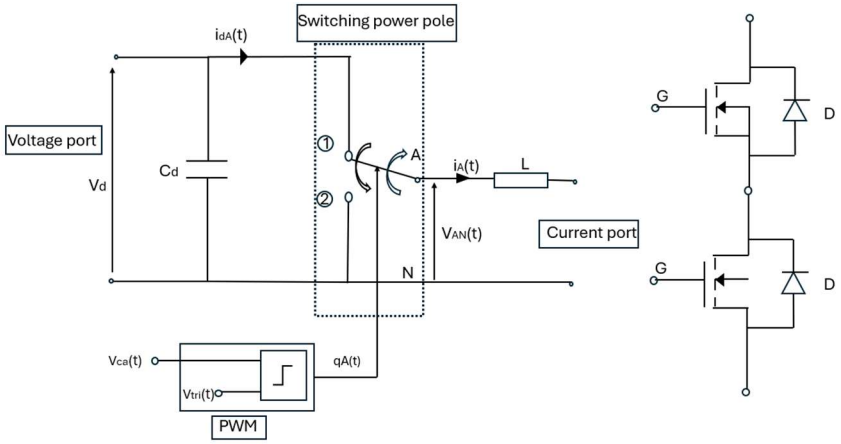


Figure 3.3 physical circuit of bidirectional converter
Source: Author's own work

- Two switches in series (HB1) form a switching pole.
- The midpoints of the pole connects to the inductor.
- The top node is connected to the voltage port (DC bus).
- The inductor leads to the current port (supercapacitor).

Depending on the location of the load relative to the switching port, the bidirectional converter can behave either as a buck like HB1 or boost topology in each direction of power flow.

3.2.2 Buck-Mode Operation

The buck operating mode corresponds to the condition in which energy is transferred from the DC bus to the supercapacitor. In this case, the DC bus acts as the energy source, while the supercapacitor behaves as the storage element.

The converter operates using a half bridge structure composed of two switches forming a switching pole. The midpoint of the switching pole is connected to the inductor, which plays a key role in regulating the current flow.

During buck operation, the upper switch is actively controlled by a PWM signal, while the lower switch provides a freewheeling path for the inductor current. When the upper switch is turned ON, the DC bus voltage is applied to the inductor, causing the inductor current to increase and the energy to be transferred to the supercapacitor. When the upper switch is turned OFF, the inductor current continuous to flow through the lower switch, ensuring continuous current delivery to the storage element.

The supercapacitor is connected to the current port of the converter, meaning that the current flowing through the inductor directly determines the charging process. This configuration allows precise control of the charging current through the modulation of the duty cycle.

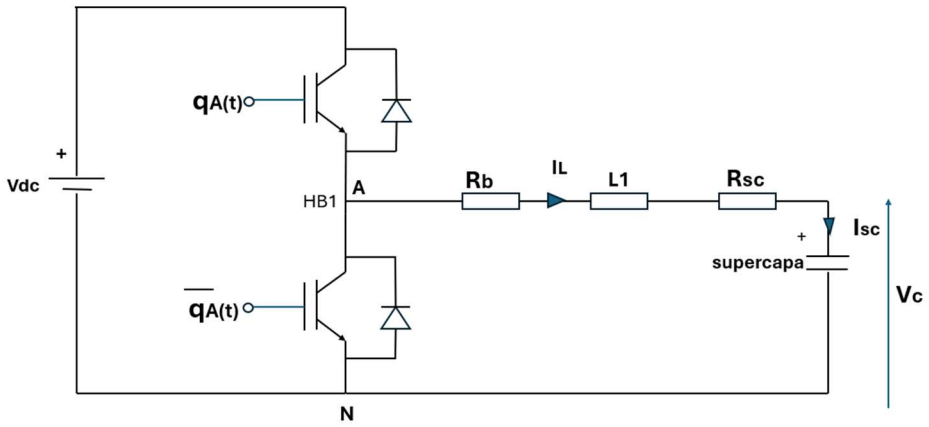


Figure 3.4 Buck mode operation of the bidirectional DC-DC converter
Source: Author's own work

3.2.3 Unitary Switching Function and Instantaneous Model

To analytically describe the switching behaviour, a unitary switching function is introduced.

Switching function $q_A(t)$:

- $q_A(t) = 1$: upper switch ON, lower switch OFF.
- $q_A(t) = 0$: upper switch OFF, lower switch ON.

So we get the instantaneous expression $v_{AN}(t)$:

$$\boxed{v_{AN}(t) = q_A(t)V_{dc}}$$

Clearly the waveform is a square wave, that contains DC + fundamental and harmonics in its frequency spectrum, inductor L1 and supercap acts as a low pass filter and removing the switching harmonics so we obtain only DC and fundamental components.

3.2.4 The Average Expression of V_{AN}

A general instantaneous expression :

$$y(t) = q_A(t)x(t)$$

Can be replaced by the averaged expression

$$\bar{y}(t) = d_A\bar{x}(t)$$

Only when x(t) is either:

- Constant ,or
- Piecewise linear function inside the switching period

Because :

$$\overline{q_A(t)} = d_A = \frac{1}{T_s}\int_0^{T_s} q_A(t)dt$$

The necessary mathematical condition is :

$$\bar{X} = X_d = X_{1-d}$$

3.2.5 Application of Bidirectional Converter

We derived:

$$v_{AN}(t) = q_A(t)V_{dc}$$

Since the DC voltage is constant, so we can use the theorem:

$$\boxed{\overline{v_{AN}} = \overline{q_A}(t)v_{dc} = d_A v_{dc}}$$

This is the classical buck conversion equation.

3.2.6 Boost-Mode Operation

The boost operating mode correspond to the condition in which energy is transferred from the supercapacitor to the DC bus. In this case, the supercapacitor acts as the energy source, while DC bus behaves as the receiving side.
In this operating mode, the direction of power flow is reversed compared to the buck operation. The supercapacitor is connected to the current port, and the energy stored in it is delivered to the DC bus through the converter.
The lower switch of the half bridge is actively controlled using a PWM signal, while the upper switch provides a path for the energy transfer to the DC bus. When the lower switch is turned ON, the inductor is connected to the supercapacitor, and energy is stored in the magnetic field of the inductor. During this phase, the inductor current increases.
When the lower switch is turned off, the stored energy in the inductor is released through the upper switch toward the DC bus. As a result, the inductor voltage adds to the supercapacitor voltage, allowing the DC bus voltage to be higher than the supercapacitor voltage. This is the fundamental principle of the boost conversion. the inductor plays a key role in this process by enabling energy storage and controlled transfer, ensuring a smooth current profile and stable energy delivery to the DC bus.

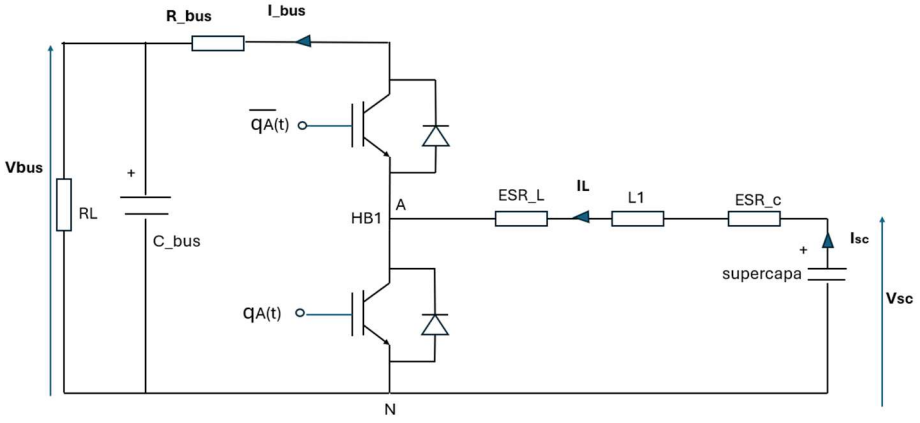


Figure 3.5 Boost mode operation of the bidirectional DC-DC converter
Source: Author

The same switching structure is therefore capable of operating in both buck and boost modes, depending on the direction of power flow, making it suitable for bidirectional energy management.

3.2.7 Instantaneous Midpoint Voltage $V_{AN}(t)$

- When lower switch is ON ($q_A = 1$) :
  $v_{AN}(t) = 0$
- When lower switch is OFF ($q_A = 0$) :
  $v_{AN}(t) = V_{bus}$

3.2.8 Instantaneous Inductor Voltage $v_L(t)$

The inductor L1 is placed between the current port and node AN.

$v_L(t) = v_{sc} - v_{AN}(t)$

Therefore:

a) When lower switch is ON ($q_A = 1$)**:**

$$V_L^{ON} = V_{sc}$$

b) When lower switch is OFF ($q_A = 0$)**:**

$$V_L^{OFF} = V_{sc} - V_{bus}$$

These two slopes generate the inductor ripple in boost mode.

3.2.9. Average Inductor Voltage and Boost Relation

Using two instantaneous intervals:

$\bar{V_L} = d.V_{sc} + (1-d)(V_{sc} - V_{bus})$

In steady state condition requires:

$\bar{V_L} = 0$

Solve for the boost equation and conversion ratio:

$v_{sc} - (1-d)v_{bus} = 0$

$$V_{bus} = \frac{V_{sc}}{(1-d)}$$

This is the classic conversion ratio of Boost converter.

3.3 Control strategy

3.3.1 Introduction to Control Strategy

The control strategy of the proposed system is based on a bidirectional DC-DC converter that regulate the power exchange between the DC source, the supercapacitor, and the DC bus. The main objective of the control system is to ensure stable operation under different condition by regulating the voltage and controlling the direction of energy transfer. Depending on the system requirements, the converter operates either in charging mode or discharging mode.

3.3.2 Operating Modes

The converter operates in two different modes. In the charging mode (buck operation), energy is transferred from the photovoltaic source to the supercapacitor. In this mode, the control system regulates the voltage across the supercapacitor to ensure safe and efficient charging.

In the discharging mode(boost operation), the supercapacitor supplies energy to the bus in order to support the load. In this case, the control system regulates the DC bus voltage and maintains it at the desired reference value [5].

3.3.3 Cascaded Control Structure

The control system is implemented using a cascaded structure composed of two control loops:[5]

- An outer voltage loop
- An inner current loop

The outer loop is responsible for voltage regulation, while the inner loop controls the current flowing through the converter.

The voltage controller is implemented using a proportional-integral (PI) regulator. It comperes the measured voltage with a reference value and generates a current reference. This reference is then used by the inner current loop, which is also based a PI controller, to ensure accurate and fast current tracking.[5]

This cascaded control structure improves the dynamic response and stability of the system, since the current loop operates faster than the voltage loop.

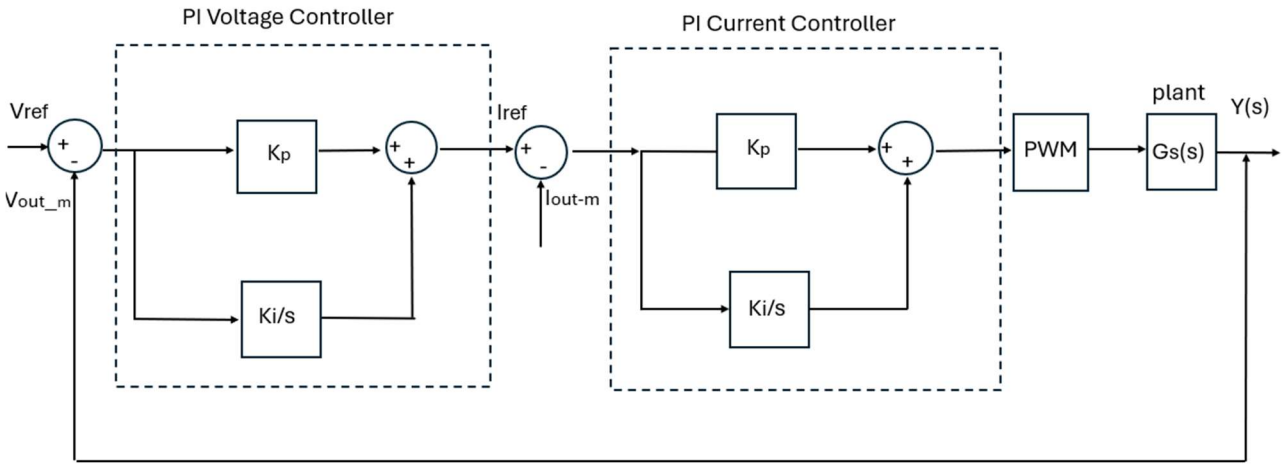


Fig 3.6 cascaded voltage and current control structure of the bidirectional converter

Source: developed by the author

3.3.4 Control Operation

In the proposed control system, the output voltage is continuously measured and compared with the reference voltage. The error signal is processed by voltage PI controller to generate the desired current reference. The current controller then adjusts the converter current to follow this reference.

The output of the current controller is used to generate the duty cycle for the PWM signal. By adjusting the duty cycle, the converter controls the amount and direction of power transferred between the supercapacitor and the DC bus.

3.3.5 Charging Strategy (CC-CV Behaviour)

During the charging process, the system follows a constant current – constant voltage (CC-CV) charging strategy. At the beginning of the charging phase, the supercapacitor is charged with a controlled current, which corresponds to the constant current region.[7]

As the supercapacitor voltage approaches its reference value, the control system naturally transitions to constant voltage mode. In this phase, the voltage is maintained at a fixed level, while the charging current gradually decreases. [7]

This approach ensures safe operation, prevents overvoltage conditions, and improves the lifetime of the supercapacitor. The transition between CC and CV modes is automatically handled by the cascaded structure.[7]

3.3.6 Pulse Width Modulation (PWM) and Switching Signal

a) Introduction to Pulse Width Modulation

pulse width modulation (PWM) is a fundamental technique used in power electronic converters to transform a continuous control signal into a discreate switching signal. In the proposed system, PWM is employed to generate the gating signals for switches of bidirectional DC-DC converter based on the output of the control system.

The control signal, obtained from the cascaded proportional-integral (PI) controllers, is compared with a high-frequency carrier waveform to determine the switching instants. This process allows precise regulation of the energy transfer between the DC bus and the supercapacitor by adjusting the duty cycle of the converter.

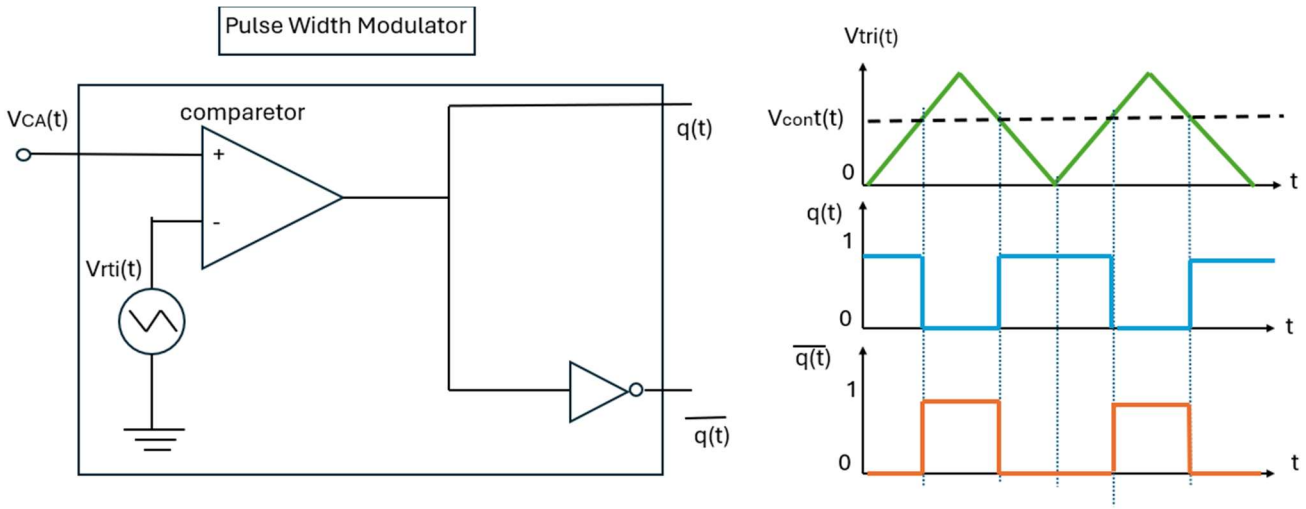


Figure 3.7. PWM scheme based on comparison between the control signal and triangular carrier waveform, showing the generated switching signals and their complementary form.

Source: Author's work

b) Triangular Carrier Waveform

The PWM technique utilizes a high frequency triangular waveform, denoted as $V_{tri}(t)$, as a carrier signal. This waveform is periodic with a switching period T_s and corresponding switching frequency:

$$f_s = \frac{1}{T_s}$$

In this work, the triangular waveform is normalized within the range:

$$0 \leq V_{tri}(t) \leq 1$$

This normalization simplifies the relationship between the control signal and the duty cycle. The triangular waveform provides a stable and linear reference for modulation, ensuring constant switching frequency and predictable system behaviour.

c) PWM Comparator and Switching Function

The switching signal is generated by comparing the control signal $V_{cont}(t)$ with the triangular carrier waveform $V_{tri}(t)$. the resulting switching function $q_A(t)$is defined as :

$$q_A(t) = \begin{cases} 1 & v_{cont}(t) \geq v_{tri}(t) \\ 0 & v_{cont}(t) < v_{tri}(t) \end{cases}$$

This binary signal represents the ON/OFF state of the upper switch in the converter. When $q_A(t) = 1$,

The upper switch is ON and the lower switch is OFF. Conversely, when $q_A(t) = 0$, the lower switch is ON and upper switch is OFF.

For the half-bridge configuration, the lower switch is driven by the complementary signal:

$$\overline{q_A}(t) = 1 - q_A(t)$$

d) Definition of Duty Cycle

The duty cycle d_A is defined as the fraction of switching period during which the upper switch is ON. It can be expressed as :

$$d_A = \frac{T_{ON}}{T_s}$$

Alternatively, using the switching function:

$$d_A = \frac{1}{T_s}\int_0^{T_s} q_A\,(t)dt$$

The duty cycle is the key parameter that determines the average voltage applied to the converter and thus controls the energy transfer between the input and output.

e) Relationship Between Control Signal and Duty Cycle

Due to the normalization of triangular waveform, a direct linear relationship exists between the control signal and the duty cycle:

$$d_A(t) = \frac{V_{cont}(t)}{V_{tri}^{peak}}$$

Since $V_{tri}^{peak} = 1$, this simplifies to:

$$d_A(t) = V_{cont}(t)$$

This relation holds under the condition:

$$0 \leq V_{cont}(t) \leq 1$$

Thus, the output of the PI controller directly determines the duty cycle of the converter.

f) Switching Function Representation in the Converter

The switching function $q_A(t)$ directly effects the voltage at the midpoint of the half-bridge, denoted as $V_{AN}(t)$. this voltage can be expressed as:

$$V_{AN}(t) = q_A(t).V_{bus}$$

Since $q_A(t)$ is a square wave, $V_{AN}(t)$ is also a pulsed waveform containing switching harmonics. However due to the presence of the inductor and capacitor in the converter, these high-frequency components are filtered out.

The average value of the midpoint voltage is given by:

$\overline{V_{AN}}$(t) = d_A . V_{bus}

This average voltage is the effective input seen by the output stage of the converter.

g) Role of PWM in Converter Operation

PWM plays a central role in controlling the operation of the bidirectional converter. By adjusting the duty cycle, the converter can regulate both magnitude and direction of power flow.

- in buck mode, the duty cycle controls the charging of the supercapacitor:
  $V_{sc} = d_A . V_{bus}$
- in boost mode, the duty cycle determines the step-up conversion:
  $$V_{bus} = \frac{V_{sc}}{1 - d_A}$$

Therefore, PWM serves as the interface between the control system and power stage, enabling precise regulation of voltage and current.

3.3.7 Dynamic Load Modelling

In order to evaluate the system under realistic demand conditions, the load is modelled as a time-varying current source rather than a fixed resistor. This approach allows the simulation of dynamic power demand profiles, which are typical in practical applications. The load profile is generated using a dedicated step-based subsystem, where multiple step signals are combined to produce a time-varying power demand.

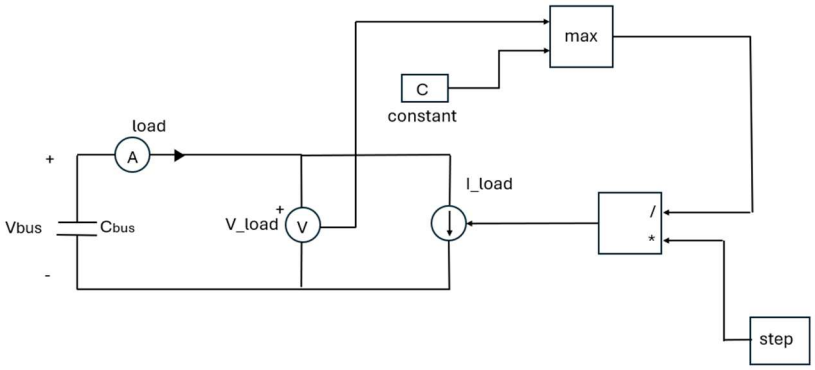


Figure 3.8 Dynamic load model based on step generation power profile and power to current conversion with numerical protection

Source: Author's work

a) Load Representation

The dynamic load profile is constructed using a set of 11 step functions, each activated at a specific time instant and associated with a predefined power level. Each step represents a variation in the load power demand, expressed in Watts. The overall load profile is obtained by summing all step contributions:

$$P_{step}(t) = \sum_{i=1}^{11} p_i - u(t - t_i)$$

Where:

- P_i is the power level of step I
- t_i is the activation time of step i
- $u(t)$ is the unit step function

this method enables the creation of a flexible and realistic load profile, allowing the system to be tested under varying operating conditions.

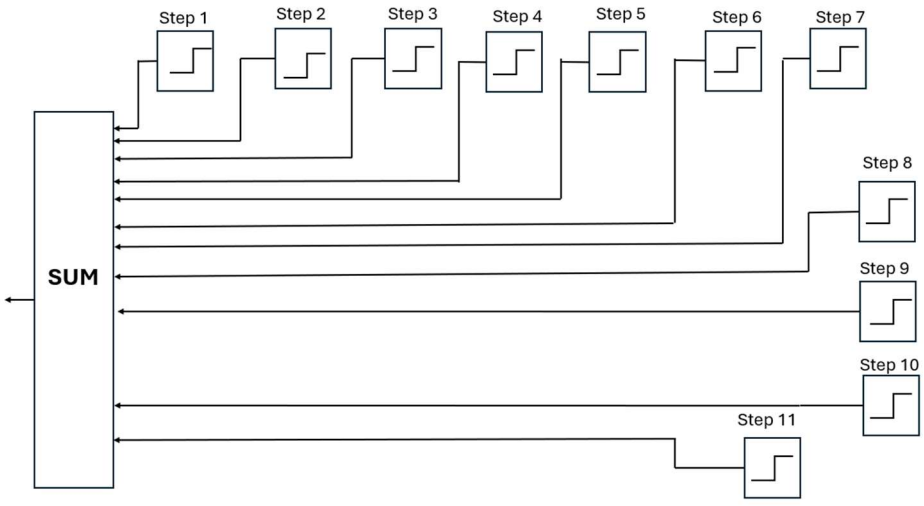


Figure 3.9 step-generation of power profile

b) Conversion from Power to Current

Since the load is implemented as a controlled current source, the desired power profile must be converted into a corresponding current reference.

Using the fundamental relation:

$$P = V \,.\, I$$

The load current reference is obtained as:

$$I_{load,ref}(t) = \frac{P_{step}(t)}{V_{bus}(t)}$$

c) Numerical Stability and Protection

A direct implementation of the previous equation may lead to numerical instability when the bus voltage becomes very small(e.g., during startup condition) , resulting in division by zero or excessively large current values.

To prevent this issue, a protection mechanism is introduced using a maximum block, which ensures a minimum denominator value.

$$I_{load,ref}(t) = \frac{P_{step}(t)}{max(V_{bus}(t), V_{min})}$$

- Where V_{min} is a small positive constant.

3.3.8 Photovoltaic Source Modelling

Photovoltaic (PV) systems are widely used in renewable energy applications to convert solar energy into electrical power. The output characteristic of a PV module depend on environmental conditions such as solar irradiance and temperature. Due to its nonlinear current-voltage characteristic, an equivalent electrical model is commonly used for analysis and simulation purposes.
The single-diode equivalent circuit shown in Figure 3.10 is one of the most widely adapted models for representing PV behaviour. It provides a good compromise between accuracy and modelling complexity and is frequently used in maximum power point tracking (MPPT) studies and renewable energy system simulations.
The following equations describe the current-voltage relationship of the PV source and form the basis of the mathematical model used in this work.

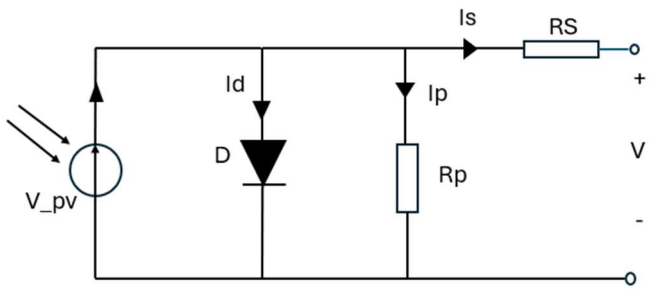


Fig.3.10 single-diode equivalent model of the PV source

Source: reproduce from [8]

a) Photovoltaic Electric Model

The photovoltaic (PV) source is represented using a single-diode equivalent circuit model, as shown in Figure 3.10 this nonlinear model is essential for accurately describing the PV behaviour under varying irradiance and temperature conditions and is typically used in conjugation with maximum power point tracking algorithms [8].

The output current of the PV module is given by:

$$I = I_{ph} - I_D - I_p$$

Where:

- I_{ph} is photocurrent(dependent on irradiance)
- I_D is diode current
- I_p is the current through the parallel resistance

The Diode current is expected as [8]:

$$I_D = I_s\left(e^{\frac{V+IR_s}{n\,V_T}} - 1\right)$$

Where:

- I_s is the diode saturation current
- R_s is the series resistance
- N is the ideality factor
- V_T is the thermal voltage

The shunt current is:

$$I_p = \frac{V + IR_s}{R_p}$$

Where R_p is the parallel resistance.

3.4 Hybrid Energy Storage System Architecture

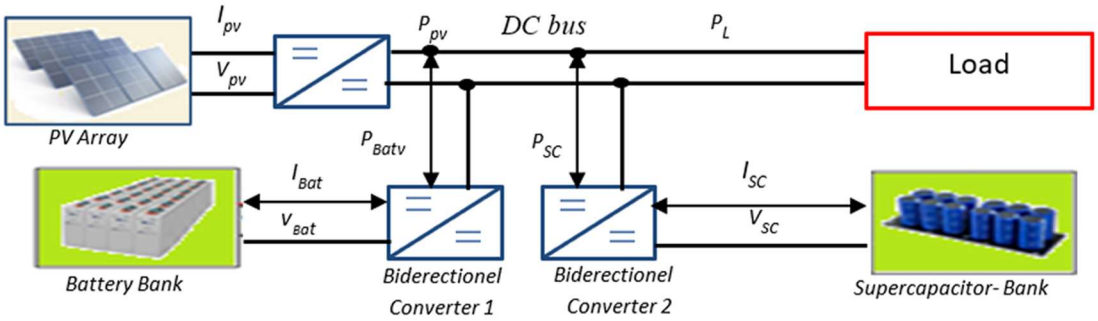


Figure 3.11 general conceptual architecture of the hybrid energy storage system (HESS) integrating a photovoltaic source, battery bank, supercapacitor bank , and bidirectional power converters

Source: reproduce from[5]

Figure 3.11 illustrates a general architecture of a hybrid energy storage system (HESS) commonly used in renewable energy applications. Although the experimental implementation in this work employs a controlled DC voltage source instead of a photovoltaic generator, the PV block is included to represent a realistic application scenario and to illustrate how the proposed converter and control structure can be integrated into complete renewable energy system.

Chapter 4: Buck Converter Modelling and Small-Signal Analysis

4.1 Buck Converter Mathematical Model

The buck operating mode corresponds to the charging phase of the supercapacitor, in which energy is transferred from the DC source to the supercapacitor through the converter structure presented in chapter three. The operating principle and switching behaviour of the half-bridge converter have already been introduced in previous chapter. Therefore this chapter focuses on the mathematical representation of the converter and the derivation of a model suitable for control design.

The modelling procedure begins with a steady-state analysis to determine the DC operating point of the system. The obtained operating conditions are subsequently used for state-space averaging, small-signal linearization, and derivation of the transfer function employed for controller design [10], [11], [13].

The converter model considers the inductance L, the equivalent series resistance of the power path R_{tot}, and the supercapacitor capacitance C_{SC}.

4.1.1 Steady-State Analysis

Steady-state analysis is performed to determine the DC operating conditions of the converter. The obtained operating conditions are subsequently used for state-space averaging, small-signal linearization, and derivation of the transfer function employed for controller design.

4.1.2 Determination of Operating Point

In steady-state operation, the average values of the converter variables remain constant over one switching period. These quantities define the operating point around which small perturbations are later introduced for linearization purposes [10], [13] . The steady-state variables can therefore be expressed as:

$$I_L = I_{L0}$$

$$V_{SC} = V_{SC}$$

$$D = D_0$$

Small perturbations are subsequently applied around these operating quantities for small-signal modelling according to:

$$I_L = I_{L0} + \hat{\imath}_L$$

$$V_{SC} = V_{SC} + \hat{V}_{SC}$$

$$D = D_0 + \hat{d}$$

4.1.3 Steady-State Duty Cycle Relationship

Since the switching operation has already been introduced in chapter 3, only the resulting averaged quantities are considered here. By applying the volt-second balance principle to the inductor voltage over one switching period, the steady-state duty cycle relationship can be obtained [10], [11].

For ideal buck:

$$D = \frac{V_0}{V_{in}} = \frac{V_{SC}}{V_{dc}}$$

Then:

We need to take into the account the parasitic resistances and applying KVL during each interval and driving V_L separately :

During T_{ON} (upper SW is ON and lower SW is OFF) :

KVL)

$$V_L(ON) = V_{dc} - V_{SC} - I_L R_{tot}$$

During $T_{OFF}(upper\ SW\ is\ OFF\ and\ lower\ SW\ is\ ON)$:

$$V_L(OFF) = -I_L R_{tot} - V_{SC}$$

According to the volt-second balance principle, the average voltage across the inductor over one switching period must be zero in steady-state operation. This means that inductor current returns to the same value at the beginning of each switching period. Therefore:

$$\bar{V}_L = D\ V_L(ON) + (1 - D)\ V_L(OFF)$$

In steady state condition the $\bar{V}_L = 0$, therefore:

$$D(V_{dc} - V_{SC} - I_L R_{tot}) + (1 - D)(-I_L R_{tot} - V_{SC}) = 0$$

the practical duty cycle becomes:

$$D = \frac{V_{SC} + I_L R_{tot}}{V_{dc}}$$

Where:

$$R_{tot} = R_b + R_{SC}$$

4.1.4 Inductor Current Ripple

The following ripple-current analysis follows the classical buck-converter derivation presented in [10], [11]. The inductor current exhibits a periodic variation around its average value due to switching action. This variation is referred to as current ripple and depends on the converter operating conditions and passive component values. For Ideal case:

$$\Delta I_L = \frac{(V_{dc} - V_{SC})D}{L\ f_{sw}}$$

The current ripple can be calculated using either the rising (ON-state) or falling (OFF-state) portion of the inductor current waveform. In this derivation, the positive slope is used.

By taking into account the parasitic resistors in practical circuit :

$$V_L = L\frac{dI_L}{dt}$$

$$V_L(ON) = V_{dc} - V_{SC} - I_L R_{tot}$$

$$\frac{dI_L}{dt} = V_L(ON)/L$$

$$\frac{dI_L}{dt} = (V_{dc} - V_{SC} - I_L R_{tot})/L$$

$$\Delta I_{L,ON} = [(V_{dc} - V_{SC} - I_L R_{tot})/L] T_{ON}$$

Where :

$$T_{ON} = D\, T_S$$

$$T_S = \frac{1}{f_{sw}}$$

The final inductor current ripple is obtained as:

$$\Delta I_{L,ON} = \frac{(V_{dc} - V_{SC} - I_L R_{tot})}{L\, f_{sw}}\, D$$

The current ripple is an important design parameter since it affects current stress, converter losses, and component selection.

4.1.5 Average Inductor Current

Unlike a conventional buck converter supplying a resistive load , the present system supplies a supercapacitor, which acts as the load during charging phase. Therefore , the average inductor current corresponds directly to the averaging charging current of the supercapacitor.

The average current can be expressed as :

$$I_{L,avg} = I_{SC,avg}$$

Since the capacitor current follows:

$$I_{SC} = C_{SC} \frac{dV_{SC}}{dt}$$

The average current depends on the desired charging rate and charging requirements rather than on a fixed load resistance.

4.1.6 Maximum and Minimum Inductor Current

The inductor current oscillates around its average value due to the switching action. Therefore the maximum and minimum current value can be calculated as:

$$I_{L.max} = \bar{I}_L + \frac{\Delta I_L}{2}$$

$$I_{L.min} = \bar{I}_L - \frac{\Delta I_L}{2}$$

4.1.7 Continuous Conduction Mode Condition

To ensure proper operation of the converter, the inductor current must remain positive throughout the switching period. Continuous conduction mode (CCM) occurs when the minimum inductor current remains above zero [10], [11].

At the boundary, the converter is exactly between CCM and DCM operation, the selected inductance must be higher than this critical value.

At the boundary condition:

$$\bar{I}_L - \frac{\Delta I_L}{2} = 0$$

After substituting the ripple:

$$\Delta I_L = \frac{(V_{dc} - V_{sc} - I_L R_{tot})D}{L\, f_{sw}}$$

Then :

$$\bar{I}_L - \frac{(V_{dc} - V_{SC} - I_L R_{tot})}{2\, L\, f_{sw}} = 0$$

So the Critical inductance is:

$$L_{Crit} = \frac{(V_{dc} - V_{SC} - I_L R_{tot})D}{2\, \bar{I}_L\, f_{sw}}$$

Then:

Therefore :

$$L > L_{Crit} \rightarrow CCM\ operation$$

$$L < L_{Crit} \rightarrow DCM\ operation$$

4.2 Small-Signal Analysis

The steady-state analysis presented in the previous section establishes the DC operating conditions of the converter and determines the corresponding operating point.

Based on the obtained operating point, the converter dynamics can now be analysed using a small-signal approach. Starting from the switching-state equations obtained for the ON and OFF operating intervals, the converter behaviour can be accurately described. However, these equations are time-varying and nonlinear due to the switching action and interaction between the duty cycle and state variables. Therefore, the state-space averaging method is applied to obtain an averaged model over one switching period, resulting in a time-invariant representation of the converter dynamics. Subsequently, small perturbations are introduced around the steady-state operating point, resulting a linearised representation of the converter dynamics. By neglecting higher order terms, a linear time-invariant small-signal model is obtained, which can then be used for transfer function derivation and controller design [10], [13].

4.2.1 Selection of State Variables and Input

The selected state variables are the inductor current and the supercapacitor voltage, namely

$$X(t) = \begin{pmatrix} i_L(t) \\ V_c(t) \end{pmatrix}$$

Where $i_L(t)$ is the inductor current and $V_c(t)$ is the supercapacitor voltage. The input source voltage is denoted by V_{dc}.

The total series resistance is defined as

$$R_{tot} = R_b + R_{sc}$$

Where R_b represents the parasitic resistance associated with the inductor branch and R_{sc} is equivalent series resistance of the supercapacitor.

4.2.2 Switching Model During T_{ON} Interval

during T_{ON} , the upper switching is commanded to be ON and lower switch is commanded to be OFF .

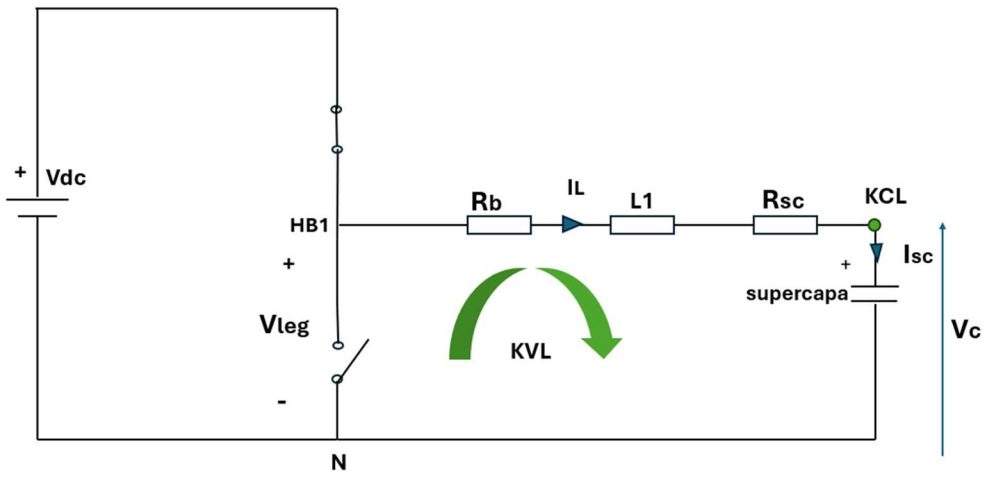


Figure 4.1 circuit during T_{ON}

4.2.3 Switching-State Equations During T_{ON} Interval

- **ON-State Equations**

When the upper switch is ON, the switching node is connected to the DC source, therefore the bridge voltage applied to the inductor side is equal to input voltage,

$V_{leg} = V_{dc}$

By applying Kirchhoff's voltage law along the power path, the inductor voltage is

$V_L = V_{dc} - RI_L - V_c$

$L\frac{di_L}{dt} = V_{dc} - RI_L - V_c$

Hence, the ON-state equations become

$$\frac{di_L}{dt} = -\frac{R}{L}I_L - \frac{1}{L}V_c + \frac{1}{L}V_{dc}$$

By applying Kirchhoff's current law at the supercapacitor node and considering the adopted averaged representation yields:

$$I_{SC} = I_L$$

$$\frac{d_{vc}}{dt} = \frac{1}{C}i_L$$

In state space form, the ON-state model can be written as

$$\dot{X} = A_1 X + B_1 u$$

With

$$\mathrm{A_1} = \begin{bmatrix} -\frac{\mathrm{R}}{\mathrm{L}} & -\frac{1}{\mathrm{L}} \\ \frac{1}{\mathrm{C}} & 0 \end{bmatrix}$$

$$\mathrm{B_1} = \begin{bmatrix} \frac{1}{\mathrm{L}} \\ 0 \end{bmatrix}$$

$$\mathrm{u} = \mathrm{V_{dc}}$$

4.2.4 Switching Model During T_{OFF} Interval

During T_{OFF}, the upper switch is commanded to be OFF and lower switch is commanded to be ON.

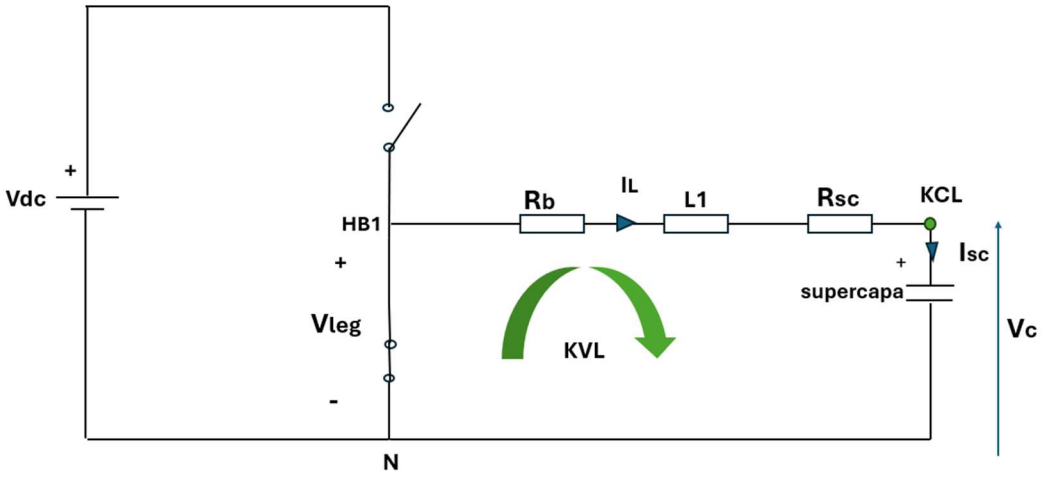


Figure 4.2 circuit during T_{OFF}

Source: Autor's work

4.2.5 Switching-State Equations During T_{OFF} Interval

- **OFF-State Equations**

When the upper switch is OFF, the inductor current freewheels through the lower path and the bridge . therefore:

$V_{leg} = 0$

In this case, the inductor voltage equation obtained as:

$V_L = -RI_L - V_c$

$L\frac{di_L}{dt} = -Ri_L - V_c$

And therefore

$\frac{di_L}{dt} = -\frac{R}{L}i_L - \frac{1}{L}V_C$

The capacitor dynamics remain unchanged.

by applying KCL:

$I_{SC} = I_L$

$\frac{dV_C}{dt} = \frac{1}{C}i_L$

Thus, the OFF state-space equation is :

$\dot{X} = A_2X + B_2u$

Thus, the OFF state model is

$$\mathrm{A_2} = \begin{bmatrix} -\frac{\mathrm{R}}{\mathrm{L}} & -\frac{1}{\mathrm{L}} \\ \frac{1}{\mathrm{C}} & 0 \end{bmatrix}$$

$$\mathrm{B_2} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

It can be observed that the ON-state and OFF-state models differ only in the input matrix, while the state matrix remains unchanged. This property simplifies the state-space averaging procedure.

4.3 Averaged Nonlinear Model

To obtain a control-oriented model, the switching equations are averaged over one switching period T_S

Let D denote the duty cycle of the upper switch. Under the small-ripple assumption, the state variables and the input are considered approximately constant over one switching period, so the averaged model becomes [10], [13] :

$\dot{X} = D(A_1X + B_1u) + (1 - D)(A_2X + B_2u)$

Since $A_1 = A_2 = A$, and $B_2 = 0$ the averaged model reduces to :

$\dot{X} = AX + DB_1u$

Substituting the matrices yields the averaged large-signal model of the buck converter:

$$\begin{cases} \frac{di_L}{dt} = -\frac{R}{L}\, i_L - \frac{1}{L}\, V_c + \frac{D}{L}\, V_{dc} \\ \frac{dV_C}{dt} = \frac{1}{C}\, i_L \end{cases}$$

This is the averaged nonlinear model used as the starting point for the small-signal derivation. It explicitly shows that the inductor dynamics are driven by the averaged voltage applied by the half-bridge equal to DV_{dc}.

4.4 Small-Signal Linearization

For control design, the averaged nonlinear model is linearized around a steady-state operation point. The state and control variables are decomposed into a DC component and a small perturbation as follows:

$$i_L = I_L + \widehat{i_L}$$

$$V_C = V_C + \widehat{V_C}$$

$$D = D + \hat{d}$$

Where uppercase symbols denote steady-state operating values and hatted symbols denote small-signal perturbations.

Substituting these expressions into the averaged nonlinear equations and separating DC and AC terms, the steady-state equations are obtained as

$$\begin{cases} -\frac{R}{L}\, i_L - \frac{1}{L}\, V_c + \frac{D}{L}\, V_{dc} = 0 \\ \frac{1}{C}\, i_L = 0 \end{cases}$$

Since the supercapacitor voltage varies much more slowly than switching dynamics, V_c is treated as approximately constant during the small-signal derivation. The operating point is therefore defined by the selected charging current and supercapacitor voltage.

Retaining only the first-order perturbation terms gives the small-signal model

$$\begin{cases} \frac{\widehat{di_L}}{dt} = -\frac{R}{L}\, \hat{\imath}_L - \frac{1}{L}\, \hat{V}_C + \frac{V_{dc}}{L}\, \hat{d} \\ \frac{\widehat{dV_C}}{dt} = \frac{1}{C}\, \hat{\imath}_L \end{cases}$$

Taking the Laplace transform,

$$\begin{cases} S\, \hat{\imath}_L(s) = -\frac{R}{L}\, \hat{\imath}_L(s) - \frac{1}{L}\, \hat{V}_C(s) + \frac{V_{dc}}{L}\, \hat{d}(s) \\ S\hat{V}_C(s) = \frac{1}{C}\, \hat{\imath}_L(s) \end{cases}$$

From the second equation,

$$\widehat{V_C}(S) = \frac{1}{C\,S}\widehat{i_L}(S)$$

Substituting into the first one leads to

$$LS\widehat{\imath_L}(S) = -R\widehat{\imath_L}(S) - \frac{1}{C\,S}\widehat{\imath_L}(S) + V_{dc}\hat{d}(S)$$

And therefore

$$\left(LS + R + \frac{1}{C\,S}\right)\widehat{\imath_L}(S) = V_{dc}\hat{d}(S)$$

Multiplying by S, the duty-to-inductor-current transfer function becomes

$$G_{id}(S) = \frac{\widehat{\imath_L}(S)}{\hat{d}(S)} = \frac{SV_{dc}}{LS^2 + RS + \frac{1}{C}}$$

This transfer function represents the duty-cycle-to-inductor-current small-signal dynamics of the buck converter.

4.5 Imperix-Oriented Current-Loop Plant Derivation

The controller design follows classical cascaded current-voltage control principles commonly used in digitally controlled power converters [12].

In the adopted control structure, the current controller does not directly generate the duty cycle. Instead, following the Imperix implementation approach [16], [17] the controller output is the averaged bridge-leg voltage (E_b) , and the duty cycle is computed afterward by normalizing with respect to the DC bus voltage. The averaged bridge voltage is defined as

$$E_b = D\,.V_{dc} = \bar{V}_{leg}$$

During the ON interval, $V_{leg} = V_{dc}$, while during the OFF interval, $V_{leg} = 0$. Therefore, in the buck mode , the averaged bridge voltage is $E_b = DV_{dc}$.

This formulation removes the direct dependence of the current-loop plant on V_{dc}. This is particularly convenient in practical digital implementation, where the modulation stage is treated separately from the current regulator [16], [17].

Using E_b as the control input, the averaged nonlinear model becomes

$$\begin{cases} L\dfrac{di_L}{dt} = E_b - V_C - Ri_L \\ C\dfrac{dv_C}{dt} = i_L \end{cases}$$

Now the variables are decomposed as

$$i_L = I_L + \widehat{\imath_L}$$

$$V_C = V_C + \widehat{V_C}$$

$$E_b = E_{b0} + \widehat{e_b}$$

Substituting and retaining only AC terms gives

$$\begin{cases} L\,\dfrac{\widehat{di}_L}{dt} = \hat{e}_b - \hat{V}_C - R\hat{\imath}_L \\ C\,\dfrac{\hat{V}_C}{dt} = \hat{\imath}_L \end{cases}$$

Taking the Laplace transform,

$$\begin{cases} (Ls + R)\,\hat{\imath}_L(s) + \hat{V}_C(s) = \hat{e}_b(s) \\ C\,S\,\hat{V}_C(s) = \hat{\imath}_L(s) \end{cases}$$

For the inner current-loop design, the voltage loop is much slower than the current loop. Therefore , the supercapacitor voltage variation can be treated as a disturbance and neglected in the plant derivation seen by the current controller. In other words, for the inner-loop design one can assume

$\widehat{V_C}(s) \cong 0$

Hence, the current-loop plant simplifies to

$(Ls + R)\widehat{\imath_L}(s) = \widehat{e_b}(s)$

Which yields the first-order transfer function

$$G_i(s) = \frac{\widehat{\imath_L(s)}}{\widehat{e_b(s)}} = \frac{1}{Ls + R}$$

With $R = R_b + R_{sc}$

This is the plant used for PI current-controller design. Compared with the duty-based model, It is simpler and more robust for controller tuning, since the modulator and the input-voltage scaling are moved outside the plant. This is exactly the form indicated in the design workflow for the supercapacitor buck converter.

4.6 Final Remark on Current-Loop Modelling

The derivation above shows that two equivalent modelling views can be obtained for the buck converter. The first is the classical duty-to-current plant, which is second-order and explicitly contains the input voltage. The second is the Imperix-oriented plant, in which the control variable is the averaged bridge voltage E_b. This latter formulation leads to the first-order transfer function. Which is more suitable for the design of the inner current loop. Accordingly, in the following section, the PI current controller is tuned based on this first-order plant and on the total delay introduced by computation and PWM update.

4.7 Current PI Controller Design Using Optimum Magnitude Method

4.7.1 Current-Loop Plant Including Delay

To account for digital implementation effects, the equivalent delay introduced by sampling, computation ,PWM update and ADC conversion is included in the plant [12], [18]:

$$G_i(s) = \frac{1}{Ls + R_{tot}}\, e^{-s\,t_d}$$

Where :

$T_{d,tot} = T_{ADC} + T_{PWM} + T_{ctrl}$

Neglecting the delay term, the first-order plant exhibits a single pole determined by the inductor and total series resistance.

$$s = -\frac{R_{tot}}{L}$$

Therefore the pole frequency is

$$\omega_p = \frac{R_{tot}}{L}$$

4.7.2 PI Controller Structure

The PI controller is expressed as:

$$C_i(s) = K_p + \frac{K_i}{s}$$

Where:

- K_p is proportional gain
- K_i is integral gain

Factoring out K_p

$$C_i(s) = K_p\left(1 + \frac{\frac{K_i}{K_p}}{s}\right)$$

We define the zero of the PI controller $\omega_{z,pi}$:

$$\omega_{z,pi} = \frac{K_i}{K_p}$$

Therefor the final controller transfer function is:

$$C_i(s) = K_p\left(1 + \frac{\omega_{z,pi}}{S}\right)$$

The open-loop transfer function becomes:

$$L(s) = C_i(s) \times G_i(s)$$

4.7.3 Pole-Zero Cancellation

To simplify the system dynamics, the controller zero is placed at the plant pole location:

$$\omega_p = \omega_{z,pi}$$

$$\frac{R_{tot}}{L} = \frac{K_{ii}}{K_{pi}}$$

Which yields:

$$K_{ii} = K_{pi}\,\frac{R_{tot}}{L}$$

After cancellation, the open-loop transfer function becomes:

$$L(S) = K_{pi}\left(\frac{S\ +\ \frac{R_{tot}}{L}}{S}\right) \times \left(\frac{1}{LS\ +\ R_{tot}}\right) \times e^{-sTd}$$

$$L(S) = K_{pi}\left(\frac{S\ +\ \frac{R_{tot}}{L}}{S}\right) \times \left(\frac{1}{L(S\ +\ \frac{R_{tot}}{L})}\right) \times e^{-sTd} = \frac{K_{pi}}{L\ s}\,e^{-sTd}$$

Therefore, the open-loop transfer function after pole-zero cancellation becomes:

$$L(s) = \frac{K_{pi}}{L\ s}\,e^{-s}$$

The system behaves as an integrator with delay.

4.7.4 Crossover Frequency Selection

Since the system is dominated by an integrator and digital delay, the optimum magnitude criterion defines the crossover frequency according to :

$$\omega_{CC} \approx \frac{1}{2\ Td_{tot}}$$

Unlike conventional tuning approaches where the bandwidth is selected directly, the bandwidth in the optimum magnitude method is mainly constrained by the digital delay.

For the controller design, the total delay was assumed to be :

$$Td_{tot} = 50\ \mu s$$

4.7.5 Gain Calculation

The controller gains are obtained by enforcing the unity gain condition at the crossover frequency:

At crossover frequency :

$$|L(j\omega_c)| = 1$$

Substituting the simplified open-loop expression:

$$\left|\frac{K_p}{L\omega_C} \times\ e^{-j\omega_C Td}\right| = \frac{K_p}{L\omega_C}$$

Since :

$$\left|e^{-j\omega_C Td}\right| = 1$$

The delay affects only the phase response and does not modify the magnitude.

Thus:

$$K_{pi} = L\omega_C = \frac{L}{2Td}$$

Using the cancellation condition:

$$K_{ii} = K_{pi}\ \frac{R_{tot}}{L}$$

Which yields:

$$K_{ii} = \frac{L}{2T_d} \times \frac{R_{tot}}{L}\ = \frac{R_{tot}}{2T_d}$$

4.7.6 Numerical values and Final Controller Gains

Substituting the system parameters:

$f_{sw} = 20\ KHZ,\ Td_{tot} = 50\ \mu s,\ V_{dc} = 32V\ ,L_b = 68\ \mu H\ ,R_b = 3\ m\Omega\ ,R_{sc} = 6.7\ m\Omega\ ,C_{sc} = 130\ F$

The total series resistance is therefore

$R_{tot} = R_b + R_{sc}\ =\ 9.7\ m\Omega$

By substituting the system parameters, the controller gains are obtained as:

$K_{pi} = 0.68$

$K_{ii} = 97$

$$\omega_{cc}\ \approx \frac{1}{2\ Td_{tot}}$$

Substituting $Td_{tot} = 50\ \mu s$,

$$\omega_{cc}\ \approx \frac{1}{2\ Td_{tot}}\ =\ \frac{1}{2\ \times 50 \times 10^{-6}}\ = 10000\ rad/s$$

Converting to HZ,

$$f_{cc} = \frac{\omega_{cc}}{2\pi} = \frac{10000}{2\pi}\ \approx 1591.5\ HZ$$

$f_{cc}\ \approx 1.5\ KHz$

After calculating and selecting crossover frequency it is important to make sure that The selected current-loop bandwidth must satisfy the two practical constraints.

1) It must remain well below the switching frequency

For $f_{sw} = 20\ KHz$, a common rule is

$$f_{cc} \in \left[\frac{f_{sw}}{20}\ \ \frac{f_{sw}}{10}\right]$$

Thus,

$f_{cc} \approx 1.5\ KHz$

2) It must respect the digital delay limit

$$\omega_{cc} \leq \frac{1}{2T_d}$$

4.7.7 Anti-Windup Gain

A back-calculation anti-windup method was implemented for the buck-mode current controller. In this case, the PI controller output is commanded leg voltage. However, the available leg voltage is physically limited by the DC source voltage and by the modulation range. Therefore, when the requested voltage exceeds the available limit, saturation occurs.

To avoid integrator windup during saturation, the difference between the saturated and unsaturated controller output is feedback to the integrator. This prevents the integral term from accumulating an excessive error and improves the recovery of the current loop after saturation.

The anti-windup gain is selected as :

$$K_{bc,i} = \frac{K_{ii}}{K_{pi}}$$

Where K_{pi} and K_{ii} are the proportional and integral gains of the buck current PI controller.

4.8 Outer Voltage PI Controller Design

The voltage-loop design follows the cascaded control architecture, in which the current loop is designed and closed before designing the voltage controller. The purpose of the inner current loop is to force the inductor current to rapidly follow its reference value. Consequently, from the voltage-loop perspective, the closed current loop allows the converter to be approximated as an ideal controlled current source [12], [16].

In other words, the voltage controller does not directly control the duty cycle. It generates a current reference, which is sent to the already-designed current controller. The current controller then forces the actual inductor current to follow this reference with much faster dynamics.

Therefore. From the voltage controller point of view:

$$i_L \approx i_{ref}$$

This assumption significantly simplifies the design process. The question for the voltage loop becomes:

‘’ if a certain current is injected into the supercapacitor, how does the capacitor voltage change?’’

Since the capacitor voltage changes according to the amount of charge stored inside it, the voltage dynamics can be derived directly from the capacitor equation:

$$i_C = C_{sc} \frac{dV_{sc}}{dt}$$

Thus, the voltage loop plant is obtained from the relationship between the injected current and the resulting voltage variation. Because the voltage loop reacts to energy accumulation inside the capacitor, its dynamics are naturally much slower than the current loop. For this reason, the voltage

loop bandwidth is intentionally selected much lower than the current-loop bandwidth to preserve the separation between the two control loops

4.8.1 Voltage Control Structure

The buck-mode voltage loop is designed as the outer loop of the cascaded control structure. The voltage controller regulates the supercapacitor terminal voltage by generating the reference current for the inner current loop.

The voltage error is defined as:

$$e_v = V_{ref} - V_{sc,meas}$$

The voltage PI controller generates:

$$i_{ref}(s) = C_V(s).e_v(s)$$

Where $C_V(s)$ is the voltage PI controller.

Because the inner current loop is much faster than the voltage loop, it can be assumed that:

$$\frac{\hat{\imath}_L(s)}{\hat{\imath}_{ref}(s)} \approx 1$$

Therefore, for the voltage-loop design, the closed current loop can be approximated as an ideal controlled current source.

4.8.2 Voltage-Loop Plant Without ESR

The injected current charges the supercapacitor, Therefore :

$$i_L(t) = C_{sc}\frac{dV_{sc}(t)}{dt}$$

Taking the Laplace transform :

$$\hat{V}_{sc}(s) = \frac{\hat{\imath}_L(s)}{s\ C_{sc}}$$

Since :

$$\hat{\imath}_L(s) \approx \hat{\imath}_{ref}(s)$$

The voltage-loop plant becomes:

$$P_v(s) = \frac{\widehat{V_{sc}}(s)}{\widehat{\imath_{ref}}(s)} \approx \frac{1}{s\ C_{sc}}$$

This means that the outer voltage plant behaves mainly as an integrator.

4.8.3 Voltage-Loop Plant Including ESR Effect

In practice, the measured supercapacitor terminal voltage also includes the voltage drop on the supercapacitor ESR:

$$V_{term}(t) = V_c(t) + R_{sc}i_L(t)$$

In the Laplace domain:

$$\hat{V}_{term}(s) = \frac{\hat{\imath}_L}{s\,C_{sc}}(s) + R_{sc}\hat{\imath}_L(s)$$

Therefore :

$$P_v(s) = \frac{\hat{V}_{term}(s)}{\hat{\imath}_{ref}(s)} \approx \frac{1}{s\,C_{sc}} + R_{sc}$$

Or :

$$P_v(s) = \frac{1 + s\,R_{sc}C_{sc}}{s\,C_{sc}}$$

Using:

$R_{sc} = 6.7\,m\Omega\,,\ C_{sc} = 130F$

$$\omega_{z,ESR} = \frac{1}{0.0067 \times 130} = 1.148\,rad/s$$

$$f_{z,ESR} = \frac{1.148}{2\pi} = 0.183\,Hz$$

So:

$f_{,zESR} \approx 0.18\,Hz$

The ESR-inclusive voltage-loop plant is first derived to identify the ESR zero and verify its location.

This clearly shows that the plant consists of:

- An integrator $\frac{1}{S\,C_{sc}}$
- The ESR introduces a zero in the voltage-loop plant.

4.8.4 Voltage PI Controller Structure

The voltage PI controller is written as:

$$C_v(s) = K_{pv} + \frac{K_{iv}}{s}$$

Or :

$$C_v(s) = K_{pv}(1 + \frac{\omega_{zv}}{s})$$

Where :

$$\omega_{zv} = \frac{K_{iv}}{K_{pv}}$$

The open-loop transfer function becomes:

$$L(s) = C_v(s) \times p_v(s)$$

$$L(s) = K_{PV}\left(1 + \frac{\omega_{zv}}{s}\right)\frac{1}{s\,C_{SC}}$$

4.8.5 PI Zero Placement

To ensure good stability and phase margin, the PI zero is placed well below the crossover frequency:

$$\omega_{zv} = \frac{\omega_{CV}}{10}\ or\ \frac{\omega_{CV}}{5}$$

4.8.6 Voltage-Loop Bandwidth Selection

In order to select the voltage-loop bandwidth properly, first the I used the plant with ESR to identify the zero placement introduced by ESR. The selected voltage-loop crossover frequency was then chosen below this ESR zero, so the ESR effect has negligible influence around the control bandwidth and the plant can be approximated as a pure integrator. In addition, the voltage loop must be much slower than the current loop to preserve the cascaded control structure.

Since the current-loop bandwidth is approximately :

$$f_{ci} \approx 1.5\ kHz$$

The voltage-loop bandwidth is selected by knowing:

$$f_{z,ESR} = 0.183\ Hz$$

Then the f_{cv} is selected below the $f_{z,ESR}$

$$f_{cv} = 0.1Hz$$

$$\omega_{CV} = 2\pi\, f_{CV} = 0.628\ rad/s$$

This ensures that :

$$f_{cv} \ll f_{ci} \quad \text{and} \quad f_{cv} \ll f_{z,ESR}$$

Therefore the current loop can track the reference generated by the voltage controller without interaction between the two loops

4.8.7 Gain Calculation Based on Unity-Gain Condition

Although the voltage-loop plant including the supercapacitor ESR was derived in section 4.8.3, the controller tuning was performed using the simplified plant without ESR. The reason is that the selected voltage-loop crossover frequency is very low compared to the ESR zero frequency. Initially, a higher voltage-loop bandwidth (on the order of several hertz) was investigated; however, simulation result showed oscillatory behaviour and insufficient damping. Therefore, a more conservative crossover frequency of 0.1 Hz was selected to guarantee stable operation and a clear separation between the voltage and current control loops. At this frequency, the ESR zero is located far beyond the voltage-loop bandwidth and has a negligible influence on the loop dynamics around the crossover region. Consequently, the ESR effect can be neglected for controller tuning purpose, and the voltage - loop plant is approximated as a pure integrator.

At the selected voltage crossover frequency:

$$S = j\omega_{CV}$$

Imposing unity gain:

$$|L(j\omega_{CV})| = 1$$

The open-loop condition is imposed:

$$|C_v(j\omega_{cv})\, P_v(j\omega_{cv})| = 1$$

$$\left| K_{PV}\left(1 + \frac{\omega_i}{s}\right) \times \frac{1}{s\, C_{SC}} \right| = 1$$

Magnitude:

$$|L(j\omega)| = \frac{K_{PV}}{C_{SC}} . \frac{\sqrt{1 + \left(\frac{\omega_i}{\omega}\right)^2}}{\omega}$$

Thus:

$$K_{PV} = \frac{C_{SC}\, \omega_{CV}}{\sqrt{1 + \left(\frac{\omega_i}{\omega_{CV}}\right)^2}}$$

And :

$$K_{iv} = K_{pv}\, \omega_{zv}$$

4.8.8 Numerical Results

By Substituting the system parameters, the controller gains calculated as:

$$C_{SC} = 130F\ ,\ \omega_{CV} = 0.628\, rad/s$$

$$\omega_{zv} = \frac{\omega_{cv}}{5} = \frac{0.628}{5} = 0.126\, rad/s$$

$$K_{PV} = \frac{C_{SC}\, \omega_{CV}}{\sqrt{1 + \left(\frac{\omega_{zv}}{\omega_{CV}}\right)^2}} \approx 80$$

$$K_{iV} = K_{PV} . \omega_i \approx 80 . 0.126 \approx 10.1$$

4.8.9 Summary of Voltage-Loop Design

The voltage controller was designed considering the ESR of the supercapacitor. After evaluating the ESR zero location, the voltage-loop bandwidth was intentionally selected below the zero frequency. This allowed the plant to be approximated as a pure integrator, simplifying the controller design. The PI controller was then tuned by placing the zero below the crossover frequency and enforcing unity gain at crossover. The resulting controller ensures stable and well-separated cascaded operation.

4.8.10 MATLAB Validation Plots

a) Current-Loop, Open-Loop Response

Figure 4.3 shows the open loop frequency response of the current control loop. The system exhibits a phase margin of approximately $61.9°$, including good stability. The gain margin is about 12dB, confirming sufficient tolerance to gain variations. The crossover frequency defines the bandwidth of the current loop, which is designed to be relatively high for fast current tracking.

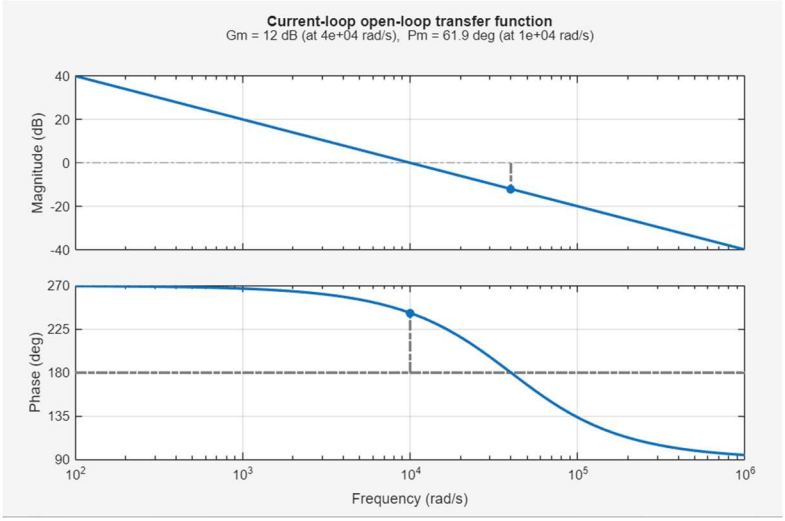


Figure 4.3 Bode plot of the current loo, open loop transfer function Li(s),showing gain margin, phase margin, and crossover frequency

b) Current-Loop, Closed-Loop Response

This Figure 4.4 illustrates the closed loop response of the current control system. The magnitude plot shows a flat response at low frequencies, including accurate tracking of the reference current. The bandwidth of the closed loop system is consistent with the designed crossover frequency. The smooth magnitude roll-off and absence of resonant peaking indicate a stable and well-damped closed-loop response.

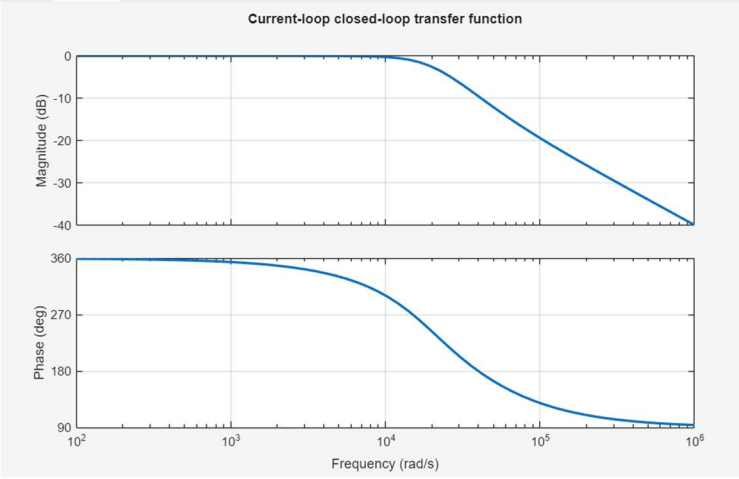


Figure 4.4 Bode plot of current closed loop transfer function Ti(s)

c) Voltage-Loop, Open-Loop Response

Figure 4.5 shows the open loop response of voltage control loop using the exact plant model, which includes ESR effect of the supercapacitor. The system exhibits a very high phase margin(approximately $113°$) indicating highly stable operation. The gain margin is infinite, meaning the system does not reach the instability condition for gain variations. The low crossover frequency

ensure a slower outer loop compared to the current loop, maintaining proper loop separation. The high phase margin confirms that even when the ESR dynamics are included, the voltage-loop design remains stable.

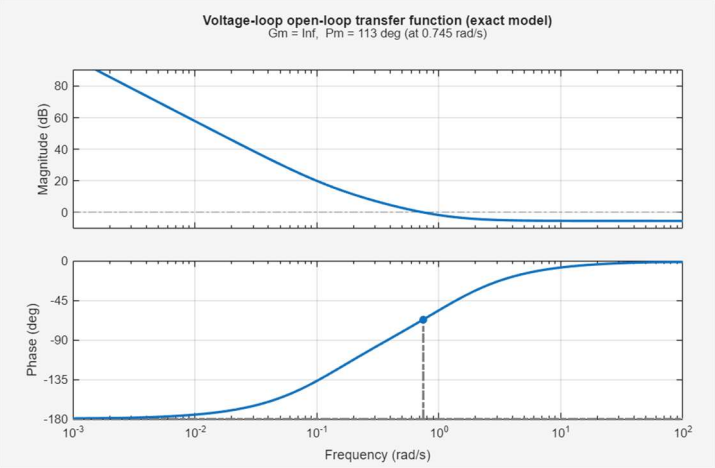


Figure 4.5 Bode plot of voltage loop open loop transfer function, using exact model

d) Voltage-Loop, Closed-Loop Response

Figure 4.6 represents the closed-loop frequency response of the voltage-control loop using the exact plant model. At low frequencies, the magnitude remains close to 0 dB, confirming accurate voltage-reference tracking. A very small resonance peak is visible around the crossover region, indicating a well-damped response without significant oscillatory behaviour. The bandwidth remains limited to a low frequency range, as intentionally selected for the outer voltage loop. The phase response varies smoothly and does not exhibit abrupt changes, further confirming stable operation. These results verify that the voltage controller achieves stable voltage regulation while maintaining proper dynamic separation from the faster inner current loop.

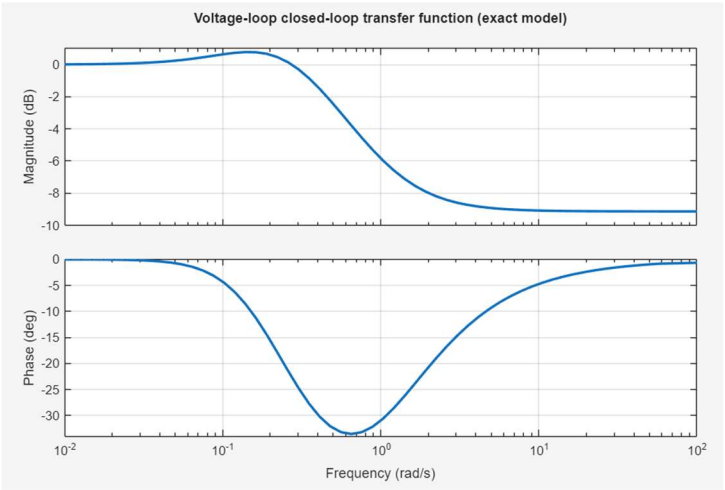


Figure 4.6 Bode plot of voltage loop closed loop transfer function, using exact model

Chapter 5: Boost Converter Modelling and Small-Signal Analysis

5.1 Boost Converter Mathematical Model

The boost operating mode corresponds to the discharging phase of the supercapacitor, in which energy is transferred from supercapacitor to the bus capacitor. The operating principle and switching behaviour of the half-bridge converter have already been discussed in chapter 3. This chapter focuses on the mathematical representation of boost converter and derivation of a model suitable for control design and ultimately designing a PI controller.

The modelling procedure begins with steady-state analysis to determine the DC operating points of the system. The obtained operating point represents the average behaviour of the converter over one switching period and provides the basis for subsequent small-signal modelling procedure. Furthermore, steady-state analysis allows the determination of duty cycle relationships, average electrical quantities, and ripple characteristics [12].

5.1.1 Steady-State Analysis

The goal of performing steady-state analysis is to determine the DC operating point of boost converter. The obtained operating point represents the average behaviour of the converter during one switching period. In addition, steady-state analysis provides information regarding average quantities, ripple characteristics that are required to sizing properly the components.

5.1.2 Determination of Operating Points

In steady-state operation, the average values of the converter variables remain constant over one switching period. These quantities define the operating point around which small perturbations are later introduced for linearization purposes. The steady-state variables can therefore be expressed as:

$$V_{in} = V_{SC} = V_{SC,0}$$

$$V_{out} = V_{Bus} = V_{Bus,0}$$

$$I_L = I_{L0}$$

$$D = D_0$$

Small signal perturbations are subsequently applied around these operating quantities for small-signal modelling according to:

$$I_L = I_{LO} + \hat{\imath}_L$$

$$V_{SC} = V_{SC,0} + \hat{v}_{sc}$$

$$V_{Bus} = V_{Bus,0} + \hat{v}_{Bus}$$

$$D = D_0 + \hat{d}$$

5.1.3 Steady-State Duty-Cycle Relationship

By using the inductor volt-second balance principle, under steady-state conditions, the average voltage across the inductor over one switching period must be equal to zero. This condition provides

the relationship between the converter input voltage and output voltage (conversion ratio), and duty cycle. For an ideal converter, the boost conversion ratio is obtained as:

$$\frac{V_{out}}{V_{in}} = \frac{1}{(1 - D)}$$

Where D represents the duty cycle of the switching signal.

In a practical implementation, parasitic resistances associated with the inductor winding and supercapacitor equivalent resistance introduce additional voltage drops into the power path. Therefore

During T_{ON} (lower SW is ON and upper SW is OFF):

By applying KVL:

$$-V_{sc} + R_{tot}I_L + V_{L,ON} = 0$$

Therefore:

$$V_{L,ON} = V_{sc} - R_{tot}I_L$$

During T_{OFF} (lower SW is OFF and upper SW is ON):

By applying KVL:

$$-V_{sc} + V_{L.off} + I_L R_{tot} + V_{out} = 0$$

$$V_{L,off} = V_{sc} - I_L R_{tot} - V_{out}$$

By applying volt-second balance law:

$$V_{L,ON}T_{ON} + V_{L,OFF}T_{OFF} = 0$$

$$(V_{sc} - R_{tot}I_L)D + (V_{sc} - I_L R_{tot} - V_{out})(1 - D) = 0$$

The final D can be express as

$$D = 1 - \frac{V_{in} - I_L R_{tot}}{V_{out}}$$

Where

$$R_{tot} = R_L + R_{SC}$$

$$V_{in} = V_{sc}$$

$$V_{out} = V_{bus}$$

This expression more accurately represents the practical converter behaviour.

5.1.4 Inductor Current Ripple

The inductor current ripple is determined from the inductor current slope during the ON interval, where the current increases linearly. Using the inductor voltage-current relationship and considering the switching period, the ripple magnitude can be expressed as

$$V_L = L\frac{dI_L}{dt}$$

$$V_{L,ON} = [V_{sc} - \bar{I}_L R_{tot}]T_{ON}$$

Where:

$$T_{ON} = DT_s$$

Therefore :

$$\Delta I_L = \frac{(v_{sc} - \bar{I}_L R_{tot})D}{L\, f_{sw}}$$

For the ideal case:

$$\Delta I_L = \frac{v_{in}.D}{L\, f_{sw}}$$

This parameter is important because it affects current stress and overall converter performance.

5.1.5 Average Inductor Current

In the implemented system, the inner current control loop regulates and force the inductor current to track the desired current reference. Consequently, the average inductor current can be approximated as

$$\bar{I}_L \approx I_{ref}$$

5.1.6 Maximum and Minimum Inductor Current

The inductor current oscillates around its average value due to switching action. Therefore, the peak and minimum current values can be obtained as

$$I_{L,max} = \bar{I}_L + \frac{\Delta I_L}{2}$$

$$I_{L,min} = \bar{I}_L - \frac{\Delta I_L}{2}$$

5.1.7 Continuous Condition Mode Condition

Continuous condition Mode (CCM) occurs when the inductor current remains positive throughout the entire switching period. The boundary between CCM and discontinuous conduction mode (DCM) is reached when the minimum inductor current becomes zero.

At the CCM boundary:

$$I_{L,min} = 0$$

$$\bar{I}_L - \frac{(V_{sc} - \bar{I}_L R_{tot})D}{2\, L\, f_{sw}} = 0$$

This yields the critical inductance:

$$L_{Crit} = \frac{(V_{sc} - I_L R_{tot})\, D}{2\, I_L\, f_{sw}}$$

Thus:

$L > L_{Crit} \rightarrow CCM$

$L < L_{Crit} \rightarrow DCM$

5.2 Small-Signal Analysis

The switching-state equations and steady-state operating conditions derived in the previous sections provide the basis for the development of a control-oriented model of the boost converter. While the switching model accurately describes the converter behaviour, it remains nonlinear due to the multiplication between the duty cycle and state variables. For control design purposes, a small-signal model is therefore developed by linearizing the converter around a selected operating point [12], [13]. Small perturbations are introduced around the steady state values, allowing the converter dynamics to represented by a linear system suitable for state-space averaging and transfer function derivation. The resulting model is then used for the design and implementation of the cascaded control structure. A systematic modelling approach is adopted:

- The system is first described using switching state equations
- Then transformed into an averaged model over one switching period
- Finally, a small-signal linearized model is derived around a steady-state operating point

5.2.1 Selection of State Variables and Input

The system is described using the following state variables:

$$X(t) = \begin{bmatrix} i_L(t) \\ V_{bus}(t) \end{bmatrix}$$

- $i_L(t)$: Inductor current
- $V_{bus}(t)$: DC bus capacitor voltage which is equal to V_o

The input source is defined as:

- $u = V_{sc}$

The supercapacitor voltage V_{SC} acts as the input source of the boost converter.

5.2.2 Switching Model During T_{ON}

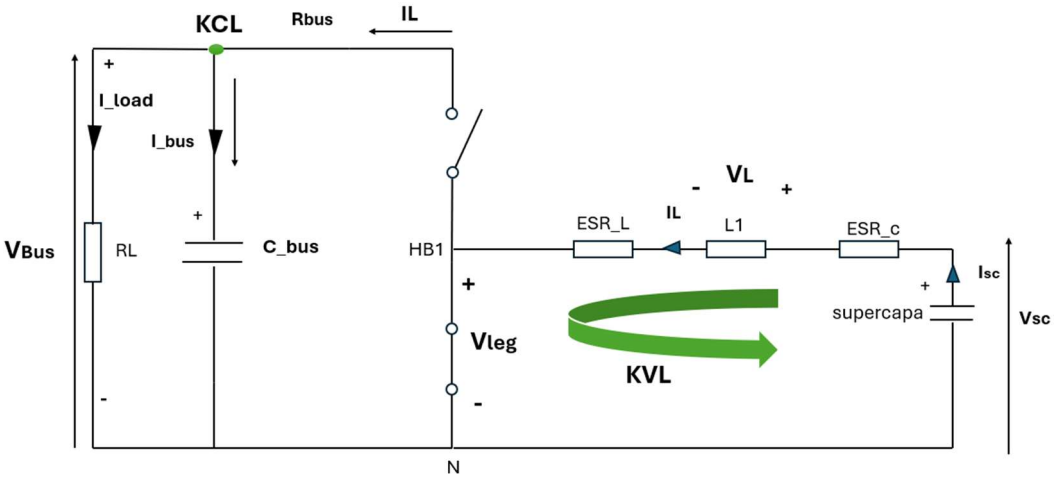


Figure 5.1 Boost-in ON interval

Source: author's own work

5.2.3 Switching-State Equations During T_{ON} Interval

- **ON-State Equations**

When the lower switch is ON and the upper switch is OFF, The inductor is connected to the supercapacitor and energy is stored in the inductor. At the output side, the output capacitor supplies the load. Therefore:

$$V_{leg} = 0$$

Applying KVL:

$$-V_{sc} + V_L + (ESR_C + ESR_L)i_L = 0$$

$$V_L = V_{sc} - (ESR_C + ESR_L)i_L$$

$$L\frac{di_L}{dt} = V_{SC} - (ESR_C + ESR_L)i_L$$

Thus:

$$\frac{di_L}{dt} = \frac{1}{L}(V_{SC} - (ESR_L + ESR_C)i_L)$$

By applying KCL at the output node:

$$I_{Cbus} + I_{load} = 0$$

$$I_{Cbus} = -I_{load}$$

$$\frac{dVc_{bus}}{dt} = -\frac{1}{R_{load}C_{bus}}(V_{bus})$$

Using the state variables defined previously, The state-space equations during T_{ON} interval can be written as:

$$\dot{X} = A_1 X + B_1 u$$

$$A_1 = \begin{bmatrix} -\frac{(ESR_L + ESR_C)}{L} & 0 \\ 0 & -\frac{1}{R_{load} C_{bus}} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

$$u = V_{sc}$$

5.2.4 Switching Model During T_{OFF} Interval

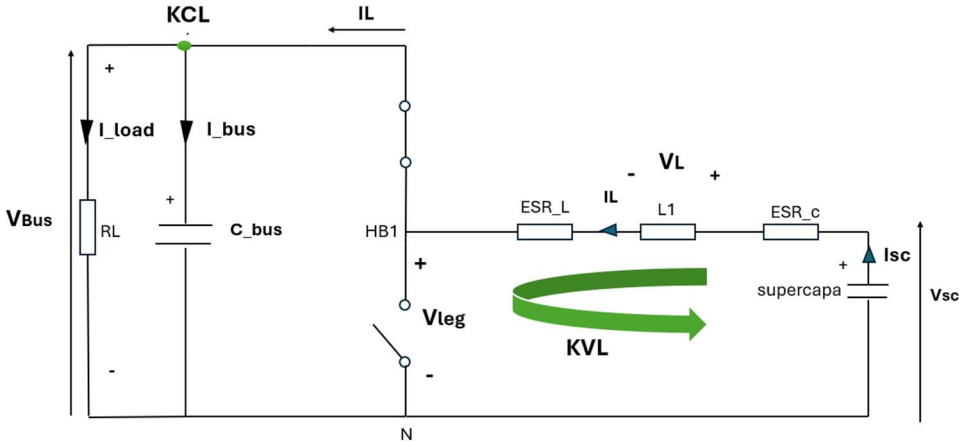


Figure 5. 2 boost in OFF interval

Source : Author's work

5.2.5 Switching-State Equations During T_{OFF} Interval

- **OFF-State Equations**

When the lower switch is OFF and the upper switch is ON, the inductor transfers energy to the output capacitor and the load. Therefore :

$$V_{leg} = V_{Bus}$$

By applying KVL :

$$-V_{SC} + V_L + i_L(ESR_{SC} + ESR_L) + V_{Bus} = 0$$

$$V_L = V_{SC} - i_L(ESR_{SC} + ESR_L) - V_{Bus}$$

$$L\frac{di_L}{dt} = V_{sc} - (ESR_L + ESR_{sc})i_L - V_{Bus}$$

Thus:

$$\frac{di_L}{dt} = \frac{1}{L}(V_{sc} - (ESR_L + ESR_{sc})i_L - V_{Bus})$$

By applying KCL:

$$I_{Cbus} = I_L - I_{load}$$

$$\frac{dV_{cbus}}{dt} = \frac{1}{C_{bus}}\left(I_L - \frac{V_{bus}}{R_{load}}\right)$$

The OFF-State space equations can be written as:

$$\dot{X} = A_2 X + B_2 u$$

With :

$$A_2 = \begin{bmatrix} \frac{-(ESR_L + ESR_{sc})}{L} & -\frac{1}{L} \\ \frac{1}{C_{bus}} & -\frac{1}{R_{load}\, C_{bus}} \end{bmatrix}$$

$$B_2 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

5.3 Averaged Nonlinear Model

The ON and OFF switching-state equations are combined using state-space averaging. Since the duty cycle D represents the fraction of the switching period spent in the ON state, the averaged model is obtained by weighting the ON-state equations by D and OFF-state equations by (1 – D). This results in a continuous-time large-signal model, which serves as the basis for the subsequent small-signal linearization.

$$\dot{X} = D(A_1 X + B_1 u) + (1 - D)(A_2 X + B_2 u)$$

Applying state-space averaging and assuming small switching ripple, the large-signal averaged model becomes:

$$\begin{cases} \frac{dI_L}{dt} = -\frac{(ESR_L + ESR_{SC})}{L} I_L - \frac{(1-D)}{L} V_{bus} + \frac{1}{L} V_{SC} \\ \frac{dV_{Cbus}}{dt} = \frac{(1-D)}{C_{bus}} I_L - \frac{1}{R_{load} C_{bus}} V_{bus} \end{cases}$$

5.4 Small-Signal Linearization

Each variable is decomposed into a steady-state component and a small perturbation:

$$i_L(t) = I_L + \hat{\imath}_L(t)$$

$$v_{bus}(t) = V_{bus} + \hat{v}_{bus}(t)$$

$$d(t) = D + \hat{d}(t)$$

$$v_{SC}(t) = V_{sc} + \hat{v}_{SC}(t)$$

Where uppercase quantities denote the steady-state operating point and hatted quantities denote small-signal perturbations.

Substituting the decomposed variables into the averaged nonlinear equations and separating the steady-state (DC) terms and perturbation (AC) terms and neglecting second order perturbation terms yields the following steady-state equations and small-signal equations.

The steady-state equations are obtained as:

$$\begin{cases} -\dfrac{(ESR_L + ESR_{SC})}{L} I_L - \dfrac{(1 - D)}{L} V_{bus} + \dfrac{1}{L} V_{SC} = 0 \\ \dfrac{(1-D)}{C_{bus}} I_L - \dfrac{1}{R_{load} C_{bus}} V_{bus} = 0 \end{cases}$$

These equations define the steady-state operating points of the boost converter.

Keeping only the first-order perturbation terms leads to the small-signal model:

$$\begin{cases} \dfrac{d\hat{\imath}_L(t)}{dt} = -\dfrac{(ESR_L + ESR_{SC})}{L} \hat{I}_L(t) - \dfrac{(1 - D)}{L} \hat{V}_{bus}(t) + \dfrac{V_{bus}}{L} \hat{d}(t) + \dfrac{1}{L} \hat{V}_{SC}(t) \\ \dfrac{d\hat{v}_{bus}(t)}{dt} = \dfrac{(1 - D)}{C_{bus}} \hat{I}_L(t) - \dfrac{I_L}{C_{bus}} \hat{d}(t) - \dfrac{1}{R_{load}\, C_{bus}} \hat{V}_{bus}(t) \end{cases}$$

This is the linearized small-signal model of the boost converter around the selected operating.

Taking the Laplace transform, assuming zero initial conditions, gives

$$\begin{cases} S\hat{I}_L(S) = -\dfrac{(ESR_L + ESR_{SC})}{L} \hat{I}_L(S) - \dfrac{(1 - D)}{L} \hat{V}_{bus}(S) + \dfrac{V_{bus}}{L} \hat{d}(S) + \dfrac{1}{L} \hat{V}_{SC}(S) \\ S\hat{V}_{bus}(S) = \dfrac{(1 - D)}{C_{bus}} \hat{I}_L(S) - \dfrac{I_L}{C_{bus}} \hat{d}(S) - \dfrac{1}{R_{load} C_{bus}} \hat{V}_{bus}(S) \end{cases}$$

these equations form the basis for the derivation of the inner current-loop and outer voltage-loop transfer functions.

5.4 Current-Loop Transfer Function Derivation

The current-loop is designed first, because it is the inner loop and has significantly higher bandwidth than the outer voltage loop. During the current-loop design , the supercapacitor voltage perturbation is treated as an external disturbance and assumed constant ($\hat{v}_{sc} \approx 0$). This allows the current plant to be derived with duty cycle as the only input. The assumption is also physically justified because the large supercapacitor (130F) causes its voltage to vary much more slowly than the inductor current during the current-loop transient.

Substituting the expression of $\hat{v}_{sc}(s) \approx 0$ into the current-loop equation and simplifying it, yields the following second-order duty-to-current àòtransfer function:

$$(s + \frac{ESR_L + ESR_{sc}}{L})\hat{\imath}_L = -\frac{(1-D)}{L}\hat{v}_{bus} + \frac{v_{bus}}{L}\hat{d}$$

$$\left(s + \frac{1}{C_{bus}R_{load}}\right)\hat{v}_{bus} = \frac{(1-D)}{C_{bus}}\hat{\imath}_L - \frac{I_L}{C_{bus}}\hat{d}$$

Solve for $\hat{v}_{bus}$:

$$\hat{V}_{bus}(s) = \frac{\frac{1 - D}{C_{bus}}\hat{\imath}_L(s) - \frac{I_L}{C_{bus}}\hat{d}(s)}{s + \frac{1}{R_{load}c_{bus}}}$$

Substituting this expression into the first equation gives the second-order duty-to-current transfer function:

$$\frac{\hat{\imath}_L(s)}{\hat{d}(s)} = \frac{\frac{V_{bus}}{L}\, s + \frac{V_{bus}}{LR_{load}C_{bus}} + \frac{(1\ -\ D)I_L}{LC_{bus}}}{s^2\ +\ (\frac{R}{L} + \frac{1}{C_{bus}R_{load}})s\ +\ \frac{R}{LR_{load}C_{bus}}\ +\frac{(1\ -\ D)^2}{LC_{bus}}}$$

Where:

$R = ESR_L + \ ESR_{sc}$

5.5 Analysis of Transfer Function

By substituting the numerical parameters into the derived transfer function, the zero and pole location as well as natural frequency and damping ratio can be evaluated.

Numerical values are:

$L = 68\ \mu H\ , C_{bus} = 1100\ \mu F\ \ , R = ESR_L + ESR_{sc}\ = 9.7\ m\Omega$

Substituting the numerical values gives:

$$\frac{\hat{\imath}_L(s)}{\hat{d}(s)} = \frac{8.82 \times 10^5 s\ + 5.35 \times 10^7}{s^2 + 203.25s + 5.08 \times 10^6}$$

a) Zero Location

The zero is obtained from the numerator:

$8.82 \times 10^5 s + 5.35 \times 10^7\ = 0$

$$S_z = -\frac{5.35 \times 10^7}{8.82 \times 10^5}$$

$S_z \approx -60.6\ rad/s$

Converting to HZ:

$$f_z = \frac{60.6}{2\pi} \approx 9.65\ Hz$$

Therefore, the current -to-duty transfer function has a left half plane zero at approximately:

$f_z \approx 9.65\ Hz$

b) Pole Locations

The denominator is:

$s^2 + 203.25s + 5.08 \times 10^6$

Compare with the standard second-order form:

$s^2 + 2\zeta\omega_n s + \omega_n^2$

Therefore:

$\omega_n^2 = 5.08 \times 10^6$

$\omega_n = \sqrt{5.08 \times 10^6} \approx 2255\ rad/s$

Converting to HZ:

$f_n = \frac{\omega_n}{2\pi} \approx 359\ Hz$

The damping ratio is:

$2\zeta\omega_n = 203.25 \quad \Longrightarrow$

$\zeta = \frac{203.25}{2 \times 2255} \approx 0.045$

Thus:

$\omega_n \approx 2255\ rad/s$

c) the poles are:

$S_{1,2} \approx -\zeta\omega_n \pm j\omega_n\sqrt{1 - \zeta^2}$

$s_{1,2} \approx -101.6 \pm j2252$

Physical interpretation

The system has a pair of complex conjugate poles with a natural frequency around:

$359\ Hz$

And a very low damping ratio:

$\zeta \approx 0.045$

This means that the open loop power stage is weakly damped and can easily show oscillatory behaviour if the controller excites this frequency range.

The exact duty-to-current model of the boost converter is second order because it includes the coupling between the inductor-current dynamics and the DC-bus-voltage dynamics. Its pole pair reveals a lightly damped resonance. Therefore, if this exact model were used directly for current-loop design, the current loop crossover frequency should be selected sufficiently below the resonant frequency to avoid exciting this mode.

In the adopted cascaded control structure, however, the inner current loop is designed to be much faster than the outer voltage loop, typically with a bandwidth separation of about 5-10 times. Under this time-scale-separation assumption, the DC-bus voltage changes only slightly during the fast current-loop transient and can be treated as approximately constant.

Together with $\hat{v}_{sc} \approx 0$, this reduces the coupled second-order model to the first-order current plant.

Final simplified current loop plant calculated as:

$$G_{id}(s) = \frac{\hat{\imath}_L(s)}{\hat{d}(s)} \approx \frac{V_{bus}}{Ls + R}$$

Where:

$$R = ESR_L + ESR_{sc}$$

In the implemented controller, the PI output is voltage-scaled control signal $\hat{u}_i(s)$. it is divided by the measured DC-bus voltage obtain the duty-cycle perturbation:

$$\hat{d}(s) = \frac{\hat{u}_i(s)}{V_{bus}}$$

Therefore:

$$\frac{\hat{\imath}_L(s)}{\hat{u}_i(s)} = \frac{\hat{\imath}_L(s)}{\hat{d}(s)} \times \frac{\hat{d}(s)}{\hat{u}_i(s)} = \frac{V_{bus}}{Ls + R} \times \frac{1}{V_{bus}}$$

Finally :

$$G_i(s) = \frac{\hat{\imath}_L(s)}{\hat{u}_i(s)} = \frac{1}{Ls + R}$$

Therefore, the signal after the $\frac{1}{V_{bus}}$ normalization block is the duty-cycle variation $\hat{d}$, which is subsequently used by the duty-computation and PWM blocks.

5.6 Final Remark on Current-Loop Modelling

The derivation above shows that two equivalent modelling perspectives for the boost converter current loop. The first transfer function is the complete second-order duty-to- current transfer function which captures the coupling between the inductor-current and DC-bus-voltage dynamics and reveals the resonant behaviour of the power stage. The second is simplified first-order model obtained by exploiting the bandwidth separation between the inner current loop and the outer voltage loop. This simplified model is adopted for controller design because it accurately represents the plant within the intended current-loop bandwidth while significantly simplifying the PI controller design. Accordingly, the Optimum Magnitude Method is applied in the following section.

5.7 Current PI Controller Design Using Optimum Magnitude Method

The controller is designed using the Optimum Magnitude Method criterion commonly employed in digital power converter control systems[18].

5.7.1 Current-Loop Plant Including Delay

The inner current loop is designed using the simplified first-order model derived in the previous section. Since the controller is digitally implemented, the effects of ADC sampling and PWM update introduce a finite delay. This delay is represented as a pure time delay and incorporated into the plant model as:

$$G_i(s) = \frac{1}{Ls + R} e^{-sT_{dtot}}$$

Where T_{dtot} represents the total delay:

$$T_{dtot} = T_{ADC} + T_{PWM} + T_{comp}$$

The plant pole:

$$\omega_p = \frac{R_{tot}}{L}$$

With

$$R_{tot} = ESR_L + ESR_{sc}$$

5.7.2 PI Controller Structure

The PI controller is expressed as:

$$C(s) = K_{pi} + \frac{K_{ii}}{S}$$

$$C_i(s) = K_{pi}\left(1 + \frac{\omega_{zi}}{s}\right)$$

The ω_{zi} represents the PI zero location

$$\omega_{zi} = \frac{K_{ii}}{K_{pi}}$$

The open-loop transfer function becomes:

$$L_i(s) = C_i(s) \times G_i(s)$$

5.7.3 Pole-Zero Cancellation

To simplify the system dynamics, the controller zero is placed at the plant pole location:

$$\omega_z = \omega_p$$

$$\frac{K_{ii}}{K_{pi}} = \frac{R_{tot}}{L}$$

Which yields:

$$K_{ii} = K_{pi}\,\frac{R_{tot}}{L}$$

After cancellation, the open-loop transfer function reduces to:

$$L_i(s) = \frac{K_{pi}}{L\,s}\,e^{-s}$$

The system therefore behaves as an integrator with delay.

5.7.4 Crossover Frequency Selection

The crossover frequency is calculated according to below formula

$$\omega_{CC} \approx \frac{1}{2\,Td_{tot}} = 10000\ rad/s$$

The total delay used for controller design is:

$T_{dtot} = 50\mu s$

Where Td_{tot} represent the total delay (PWM + computation + sampling+ ADC conversion).

Convert it to Hz

$$f_{CC} = \frac{\omega_{CC}}{2\,\pi} = \frac{1}{4\,\pi\,Td_{tot}} \approx 1.59\ kHz$$

The second-order current to duty transfer function was first analysed to understand the intrinsic dynamics of the boost power stage. This model shows a lightly damped resonance around 359 Hz. However, for the actual inner current loop controller design, the bus voltage perturbation is assumed negligible because the voltage loop is much slower than the current loop. Under this assumption, the current-loop plant is reduced to a first-order model. Therefore, the controller is designed using this simplified first-order plant, and the crossover frequency is selected according to the Optimum Magnitude Method. With a total delay of $50\mu s$, the selected crossover frequency is approximately 1.5KHz, which is confirmed by the MATLAB Bode plot.

5.7.5 Gain Calculation Based on Unity-Gain Condition

The controller gains are obtained by enforcing the unity gain condition at the crossover frequency:

The open loop transfer function is given by:

$|L(j\omega_C)| = 1$

$L(s) = C(s)G_i(s)$

$$L(s) = K_p\left(1 + \frac{\omega_z}{s}\right).\frac{1}{Ls\ +\ R}.e^{-sT_d}$$

$$\left|\frac{K_p}{L\,j\,\omega_C}\,e^{-j\omega_C Td}\right| = 1$$

Since :

$\left|e^{-j\omega_C Td}\right| = 1$

The pure time delay affects only the phase response and does not change the magnitude response.

Thus:

$$K_p = L\omega_C = \frac{L}{2Td_{tot}}$$

Using the cancellation condition:

$$K_i = \frac{R_{tot}}{2Td_{tot}}$$

5.7.6 Numerical Values and Final Controller Gains

Substituting the system parameters:

$L = 68\ \mu H\ ,\ R_{tot} = 9.7\ m\Omega\ ,\ Td_{tot} = 50\ \mu s$

$$\omega_{CC} \approx \frac{1}{2\ Td_{tot}} = 10000\ rad/s$$

$$f_{CC} = \frac{\omega_{CC}}{2\ \pi} = \frac{1}{4\ \pi\ Td_{tot}} \approx 1.59\ kHz$$

this yields:

$$K_i = \frac{R_{tot}}{2Td_{tot}} = \frac{0.0097}{2 \times 50 \times 10^{-6}} \approx 97$$

$$K_p = L\omega_C = \frac{L}{2Td_{tot}} = \frac{68\ \times 10^{-6}}{2 \times 50 \times 50^{-6}} \approx 0.68$$

5.7.7 Anti-Windup Gain

In this work, a back-calculation anti-windup strategy is used for the PI controllers. Anti-windup is required because the controller output is subjected to physical and PWM modulation limits. When saturation occurs, the integral terms may continue to accumulate error, producing an excessive control action and slowing down the recovery after saturation. The back-calculation method mitigates this effect by feeding the difference between the saturated and unsaturated controller outputs back to the integrator. The anti-windup gain is selected as:

$$K_{bc,i} = \frac{K_{ii}}{K_{pi}}$$

The PI controller generates the voltage-scaled control signal $\hat{u}_i$. After normalization by the measured DC-bus voltage, this signal becomes the small-signal duty-cycle correction Δd.

Then :

$$D = D_{ff} + \Delta d$$

Where:

$$D_{ff} = 1 - \frac{V_{in}}{V_{bus}}$$

This structure allows the feedforward term to define the nominal duty cycle, while the PI controller compensates only the current error around the operating point.

5.8 Outer Voltage PI Controller Design

The outer voltage controller is designed after the inner current loop has been tuned. Since the inner current loop has a much higher bandwidth, it forces the inductor current to rapidly track its reference. Therefore, from the perspective of the outer voltage controller, the boost converter can be approximated as a controlled current source [18].

The voltage loop is designed after the inner current loop has already been tuned. The role of inner current loop is to force the inductor current to rapidly follow its reference value. Therefore, from the

point of view of the outer voltage controller, the converter can be seen as an almost ideal controlled current source.

In the current loop, the control objective becomes :

Duty-cycle variation → inductor current variation

Whereas in the voltage loop, the control objective becomes :

Inductor Current reference → Dc bus voltage variation

Therefore, the voltage controller does not directly generate the duty cycle. Instead ,it generates the reference current i_{ref}, which is then tracked by the inner current controller. Since the inner current loop is much faster than the voltage loop, the following approximation is used:

$\hat{\imath}_L(s) \approx \hat{\imath}_{ref}(s)$

This approximation is valid because the current-loop bandwidth is much higher than the voltage-loop bandwidth.

5.8.1 Voltage Control Structure

The voltage error is defined as :

$e_v(s) = V_{bus,ref}(s) - V_{bus,meas}(s)$

The voltage PI controller generates the current reference :

$\hat{\imath}_{ref}(s) = C_v(s)\, e_v(s)$

Where $C_v(s)$ is the outer voltage PI controller.

5.8.2 Voltage-Loop Plant Derivation

In boost mode, only part of the inductor current reaches the DC bus capacitor. The average current transferred to the output side is :

$i_{bus}(t) = (1 - D) i_L(t)$

The DC bus capacitor current is :

$i_{Cbus}(t) = i_{bus}(t) - i_{load}(t)$

Therefore :

$$C_{bus} \frac{dV_{bus}(t)}{dt} = (1 - D) i_L(t) - \frac{V_{bus}(t)}{R_{load}}$$

For the outer voltage-loop design, the duty-cycle dynamics are already regulated by the inner current loop. Therefore, the current reference is considered as the control input of the voltage loop.

$$C_{bus} \frac{\widehat{dV}_{bus}(t)}{dt} = (1 - D) \hat{\imath}_L(t) - \frac{\hat{V}_{bus}(t)}{R_{load}}$$

Taking the Laplace Transform :

$$sC_{bus}\hat{V}_{bus}(s) = (1-D)\hat{\imath}_L(s) - \frac{\hat{V}_{bus}(s)}{R_{load}}$$

Rearranging :

$$\left(sC_{bus} + \frac{1}{R_{load}}\right)\hat{V}_{bus}(s) = (1-D)\hat{\imath}_L(s)$$

Thus:

$$P_v(s) = \frac{\hat{V}_{bus}(s)}{\hat{\imath}_{ref}(s)} \approx \frac{1 - D}{sC_{bus} + \frac{1}{R_{load}}}$$

Since the voltage-loop operating frequency is selected sufficiently above the load pole, the capacitor impedance dominates the resistive-load term. Therefore, the voltage loop plant can be approximated as a pure integrator :

$$P_v(s) = \frac{\hat{V}_{bus}(s)}{\hat{\imath}_{ref}(s)} \approx \frac{1-D}{sC_{bus}}$$

5.8.3 Voltage PI Controller Design Using the Symmetrical Optimum Method

The outer Voltage controller is designed based on the symmetrical optimum method, which is widely adopted for cascaded control structures with dominant integrator dynamics and inherent delays, as recommended. This method provides a good compromise between dynamic response, stability, and robustness, making it particularly suitable for power electronics converter.

Since the inner current loop has a significantly higher bandwidth than the outer voltage loop, it can be assumed that the inductor current accurately tracks its reference value. Therefore from the perspective of the voltage controller, the inner current loop can be approximated as a unity-gain element with an equivalent delay.

Using the simplified plant derived in the previous subsection, the voltage loop dynamics can be approximated by an equivalent integrator with delay, which satisfies the assumptions of the symmetrical optimum method.

$$P_v(s) = \left(\frac{K_{deq}}{S\,T2}\right) \times e^{(-S\,T_{deq})}$$

Where:

$T2 = C_{bus}$ (capacitor related time constant)

$K_{deq} = 1 - D_{nom}$ (the equivalent gain of the inner loop)

$T_{deq} = 2T_{d1}$

Where T_{d1} is the total delay of the inner loop.

- Sampling
- Computation
- PWM modulation

- ADC conversion

This equivalent model satisfies the assumptions required by the symmetrical optimum method, namely a dominant integrator combined with an equivalent delay.

5.8.4 Selection of Design Parameter a

The parameter a is the main tuning parameter of the symmetrical optimum method and determines the trade-off between dynamic performance and robustness. A smaller value a results in a faster voltage response but reduces the phase margin and increases the sensitivity to modelling errors. Conversely, a larger value of a improves robustness and stability at the expense of a slower transient response.

For power electronics converters, practical recommendations typically suggest values in the range :

$4 \leq a \leq 6$

A value of a=6 was selected to provide a conservative compromise between dynamic response, phase margin, and robustness.

5.8.5 PI Parameter Calculation Using the Symmetrical Optimum Method

According to TN108, the PI controller parameters are defined as:

$T_{n2} = a^2 T_{deq}$

$T_{i2} = \frac{a^3 K_{deq} T^2{}_{deq}}{T_2}$

$K_p = \frac{T_{n2}}{T_{i2}}$

$K_i = \frac{1}{T_{i2}}$

Where:

- a the tuning parameter(typically $a = 4 \sim 6$)
- T_{deq} is the equivalent delay of the closed current loop
- K_{deq} is the equivalent gain of the inner loop
- T_2 is the capacitor-related time constant

The equivalent delay is defined as:

$T_{deq} = 2T_{d1}$

Where T_{d1}represents the total delay of the inner current loop, including sampling, computation, and modulation delays.

5.8.6 Numerical Results

Using the system parameters listed below and the selected symmetrical optimum tuning parameter, the controller gains are calculated as follows.

$C_{bus} = 1100\ \mu F$, $f_{sw} = 20\ kHz$, $T_d = 50\mu s$, $T_{deq} = 2T_d = 100\mu s$, $a = 6$

$T_{n2} = a^2 T_{deq} = 36 \times 10^{-4}$

$T_{i2} = \frac{a^3\, K_{deq} T^2_{deq}}{T_2} \approx 1.96 \times 10^{-3}$s

$K_p = \frac{T_{n2}}{T_{i2}} \approx 1.84$

$K_i = \frac{1}{T_{i2}} \approx 510$

The theoretical gains obtained from the symmetrical optimum method were reduced during practical tuning to mitigate excessive inrush current and improve transient stability.

5.9 MATLAB Validation Plots

a) Current-Loop Open-Loop Response

The open loop frequency response of the inner current loop is shown in Figure 5.3. the controller has been designed using the optimum magnitude method, resulting in a well-shaped magnitude response with a single dominant slope around the crossover frequency.

The Gain margin ($\approx 12\ dB$) and the phase margin ($\approx 62°$) indicate a stable and sufficiently robust system. The crossover frequency is located around $10^4\ rad/s$, which ensures a fast dynamic response while maintaining adequate stability margins.

The relatively high phase margin confirms that the current loop is well damped and not prone to oscillatory behaviour. This is essential since the current loop serves as the inner loop of the cascaded control structure and must be significantly faster than the outer voltage loop.

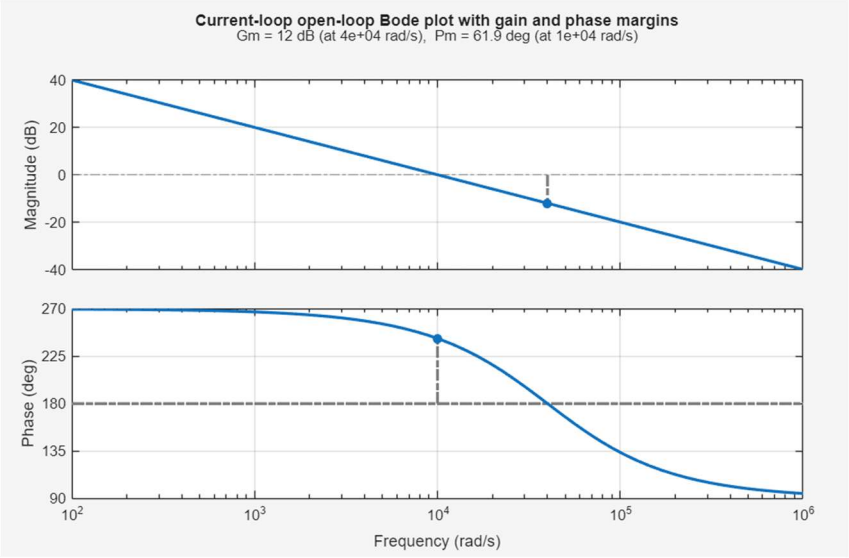


Figure 5.3 Current-loop open-loop Bode diagram with gain and phase margins

b) Current-Loop Closed-Loop

The closed loop frequency response of the current loop is depicted in Figure 5.4. the magnitude response exhibits a bandwidth consistent with the designed crossover frequency. Confirming that the

loop achieves fast tracking performance. At low frequencies, the gain is close to 0 dB, indicating accurate reference tracking with negligible steady-state error due to the integral action of the PI controller. As frequency increases, the response rolls off smoothly, demonstrating effective attenuation of high frequency disturbances and switching noise. The absence of response peaks in the magnitude response confirms a well-damped system, consistent with the phase margin in the open loop analysis.

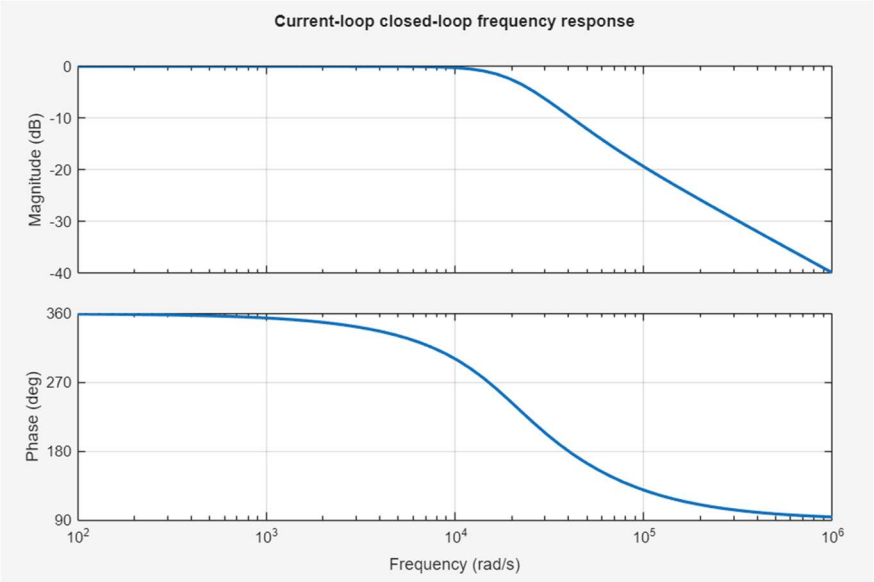


Figure 5.4 Current loop closed-loop frequency response

c) Voltage-Loop Open Loop Response

The open loop response of the outer voltage control loop is presented in Figure 5.5. the voltage loop has been designed using a small signal averaged model of the system.

The phase margin is high ($\approx 87°$), indicating a very stable and conservative design. The crossover frequency is significantly lower than the of the current loop, ensuring proper time-scale separation between the inner and outer loop. This separation is critical in cascaded control structures, as it allows the current loop to be considered instantaneous from the perspective of the voltage loop.

However, it is important to note that these theoretical gains are derived from a linearized model and not account for nonlinear effects such as duty-cycle saturation, discrete implementation, and measurement delays.

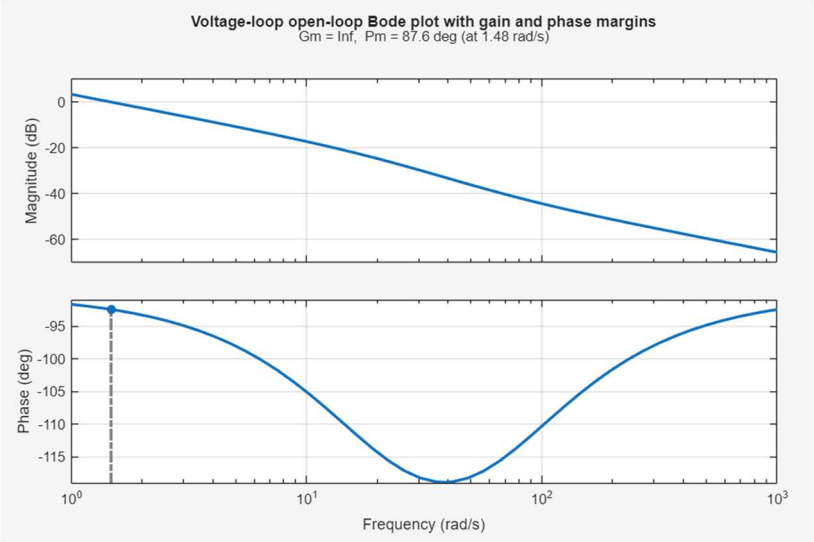


Figure 5.5 Voltage-loop open loop Bode diagram with gain and phase margin

d) Voltage-Loop Closed-Loop

The closed loop frequency response of the voltage loop is shown in Figure 5.6. the system demonstrates stable behaviour with a smooth low pass characteristic, as expected for a voltage regulation loop.

At low frequencies, the gain is approximately 0 dB, ensuring accurate voltage tracking. The bandwidth is significantly lower than of current loop, confirming the hierarchical structure of the control system.

The absence of oscillations or response peaks indicates that the system is well damped under the theoretical design conditions.

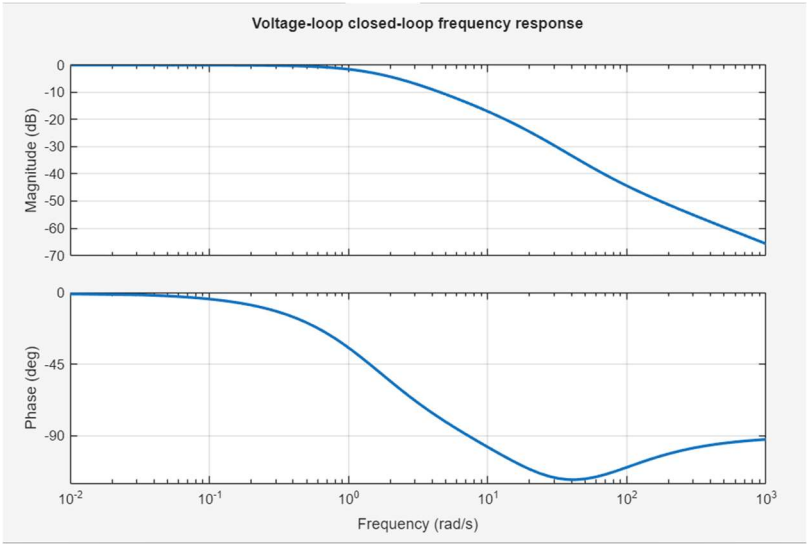


Figure 5.6 voltage loop-closed loop frequency response

Although the theoretical controller parameters provide satisfactory performance in the MATLAB-based small signal model, their direct implementation in the switching model (PLECS) led to instability or excessive oscillations. This arises because the analytical model neglects several practical non-idealities, including duty-cycle saturation, anti-windup dynamics, discrete-time effects, and measurement delays.

Therefore, the theoretical gains were used as an initial design reference, while the final controller parameters were fine-tuned in the PLECS environment to achieve stable operation and acceptable transient performance in the full nonlinear system.

Chapter6: Digital Control and Simulation Implementation of the Buck and Boost Converter

6.1 Digital Control and Simulation Architecture

The proposed bidirectional DC-DC converter was implemented using the PLECS simulation environment together with the Imperix real-time control block set in order to reproduce a realistic digitally controlled power conversion system.

The complete implementation was organized into two main subsystem: the power stage subsystem and the digital controller subsystem. The power-stage subsystem represents the physical converter components, including the switching leg, passive elements, supercapacitor model, input DC source, and measurement sensors and probs. The controller subsystem contains the complete digital control architecture, including signal acquisition, cascaded voltage and current control loops, duty-cycle computation, and PWM generation.

In order to maintain compatibility with the future experimental implementation, the digital controller was developed using the Imperix control block set integrated with the PLECS environment. This approach allows the same digital control structure to be used both simulation and real-time implementation with minimal modifications. The implemented architecture therefore reproduces

important practical aspects of digital controlled power converters, including synchronized ADC acquisition, discrete-time control execution, PWM generation, controller reset management, and real-time parameter monitoring. Figure 6.1 illustrate the overall organization of the developed digital control and simulation architecture, including the interaction between the controller subsystem and the converter power stage.

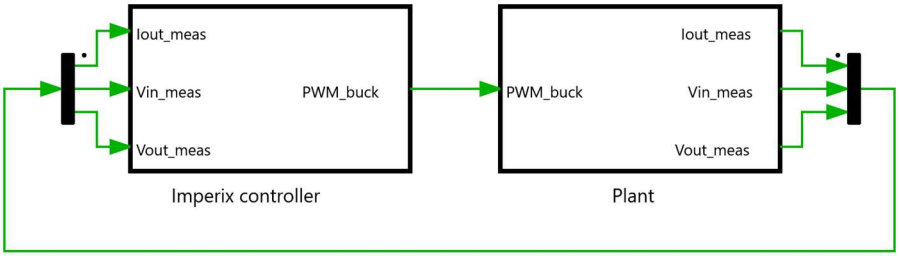


Figure 6.1. Overall digital control and simulation architecture of the bidirectional converter implemented in PLECS using the Imperix control framework

6.2 Buck-Mode Simulation Implementation

The buck-mode operation was implemented to regulate the charging process of the supercapacitor from the DC source. In this operating mode, energy is transferred from the input supply to the supercapacitor through the controlled switching action of the converter. The complete implementation was developed in PLECS using the Imperix digital control framework in order to reproduce a realistic digitally controlled power conversion system. The implemented model includes the converter power stage, synchronized feedback acquisition , cascaded voltage and current control loop, duty-cycle computation, and PWM generation.

6.1.2 Buck Converter Power Stage

The internal structure of Buck converter is shown in the figure.6.2

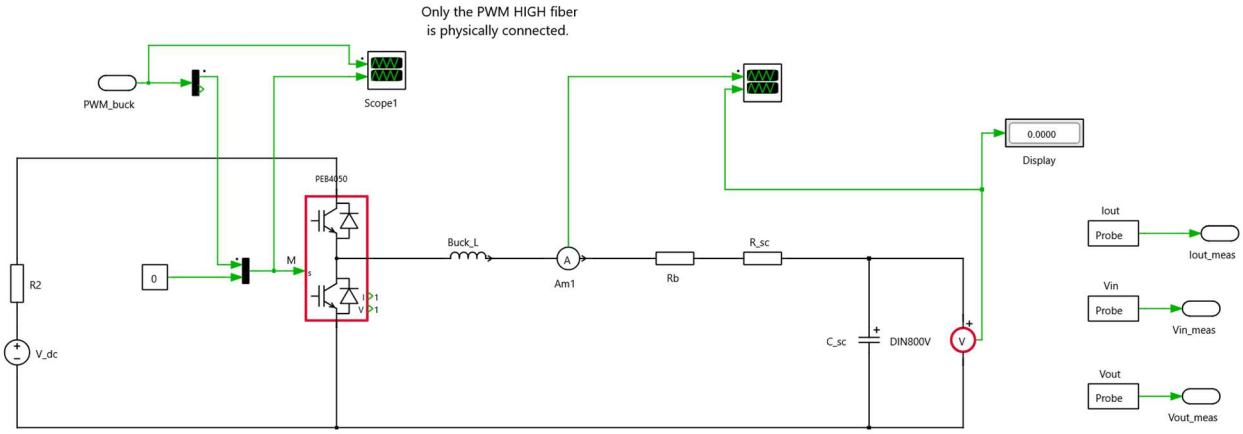


Figure 6.2 . Internal implementation of Buck mode power-stage plant in PLECS

The plant subsystem represents the physical buck converter power stage implemented in PLECS. The converter is supplied by a DC voltage source and uses the Imperix PEB4050 switching leg as the main power switching element. In buck operation, only the PWM high signal is physically connected to the switching module, while the complementary signal remains disabled. The switching node is

connected to the output through the buck inductor, which controls the current dynamics and limits current ripple.

Series resistive elements were included in the model in order to represent conduction losses and parasitic effects. The output stage is composed of the supercapacitor equivalent capacitance and the associated measurement blocks used for voltage and current acquisition. Imperix voltage and current sensor block were integrated into the model in order to reproduce the behaviour of the practical measurement system used for feedback acquisition and closed-loop control implementation.

The switching stage of the converter was implemented using the Imperix PEB4050 switching-leg model shown in Figure 6.3. the block represents a half-bridge power switching structure composed of two complementary semiconductor switching devices with anti-parallel diodes. In buck-mode operation, only the PWM high switching signal was applied to the module, while the complementary switching channel remained disabled. The PEB4050 model was selected in order to maintain compatibility between the simulation environment and the future experimental implementation based on the Imperix hardware platform.

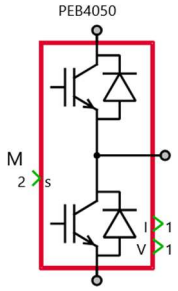


Figure 6.3. Imperix switching leg used in the Buck converter power-stage implementation

6.2.2 Buck Digital Control Structure

The Digital control architecture implemented for buck-mode operation is shown in Figure 6.4. the control system was developed in PLECS together with the Imperix real-time interface blocks in order to reproduce a realistic digitally controlled power conversion system. The implemented structure includes synchronized feedback acquisition, cascaded voltage and current regulation loops, duty-cycle computation, reset management, and PWM signal generation.

The measured converter variables, including the inductor current, input voltage, and output voltage, were acquired through synchronized measurement and ADC acquisition blocks and provided to the digital controller as feedback signals. The voltage and current regulation loops were implemented using the PLECS control library, while the synchronization, PWM generation, and real-time interface functions were implemented using the Imperix control blocks.

The cascaded control structure consists of an outer voltage regulation loop and an inner current regulation loop. The outer voltage controller regulates the supercapacitor voltage by generating the reference current required for the charging process. The generated current reference is then processed by the inner current controller, which regulates the inductor current and generates the required control action for converter operation.

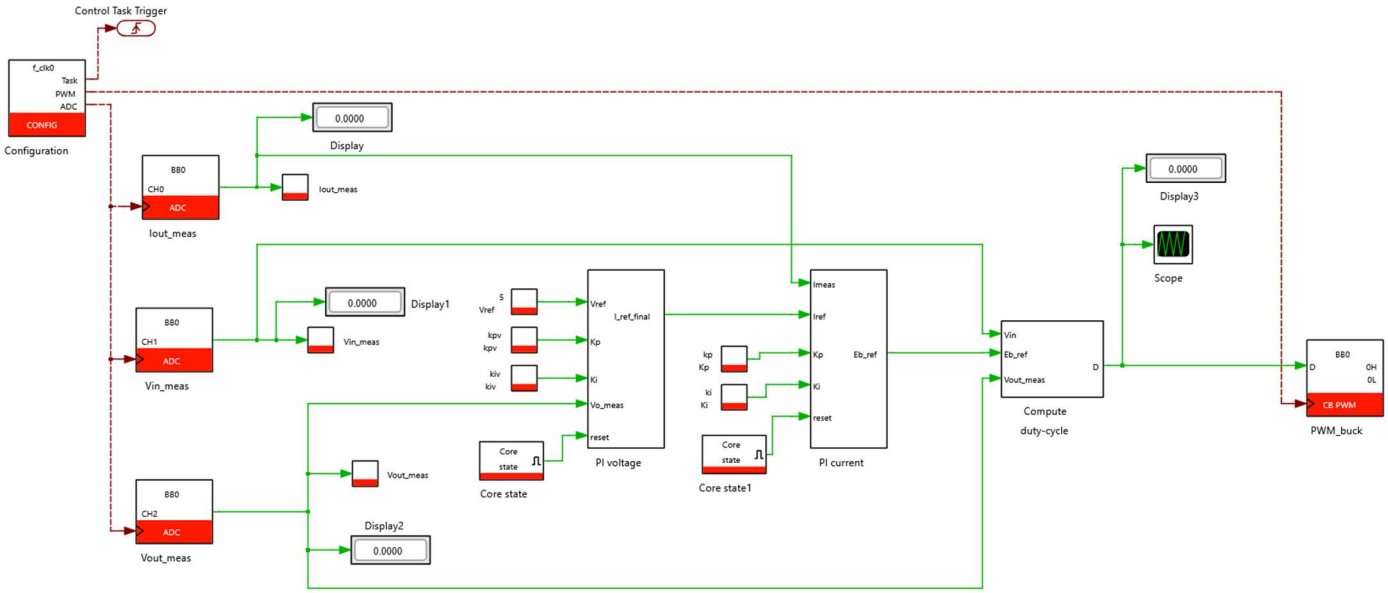


Figure 6.4. overview of cascaded control structure implemented in the Imperix controller subsystem.

Figure 6.5 shown The synchronized feedback acquisition structure implemented for the digital controller is shown in Figure 6.4. the configuration block generates the synchronization signals required for ADC acquisition, PWM execution, and control-task scheduling. The measured converter variables, including the inductor current, input voltage, and output voltage, are acquired through synchronized ADC interface blocks and provided the control algorithm as feedback signals. The control task trigger block ensures deterministic execution of the digital controller during each switching cycle.

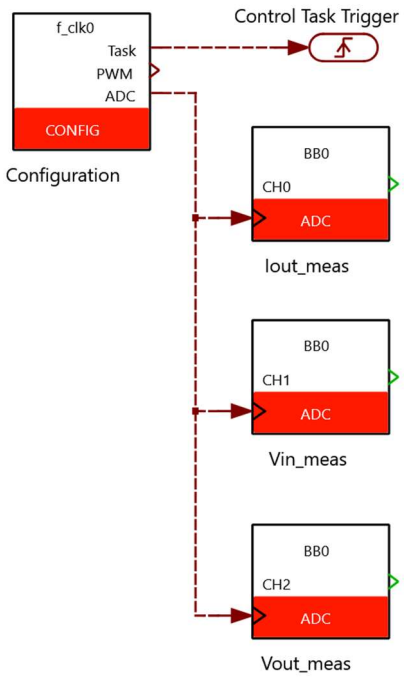


Figure 6.5 synchronized ADC acquisition and control-task implementation using the Imperix interface blocks

6.2.3 Buck Voltage Control Loop

The internal implementation of the outer voltage control loop is presented in the following figure.

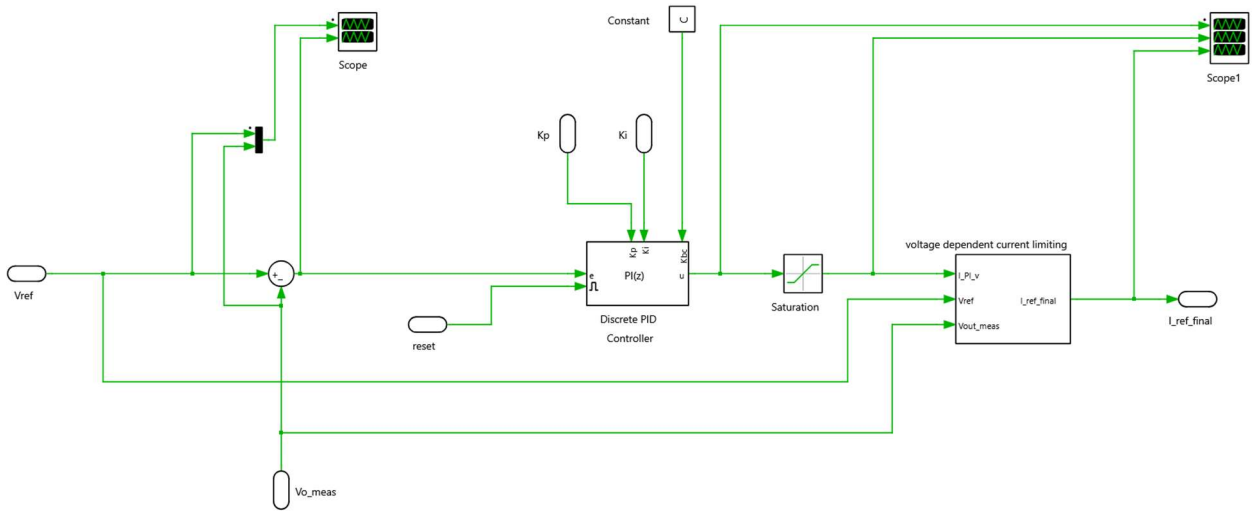


Figure 6.6. implementation of the outer voltage control loop and voltage-dependent current limiting stage

The outer voltage loop was designed to regulate the output voltage of the converter and generate the reference current for the inner current loop. The measured output voltage $V_{o,meas}$ was compared with the reference voltage V_{ref}, and the resulting error signal was processed using a discrete PI controller implemented in the Imperix control structure. The proportional and integral gains of the controller were introduced as a adjustable parameters in order to simplify tuning and stability analysis. A saturation block was added after the PI controller to limit the controller output and avoid excessive reference current generation during transient conditions.

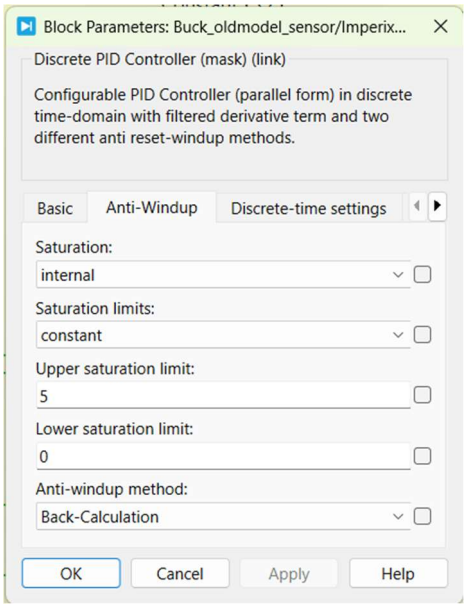


Figure 6.7. parameter configuration of the voltage-loop PI controller

The voltage-loop PI controller was implemented using the Imperix discrete PI structure. The proportional gain, integral gains, saturation limits, anti-windup coefficients were configured to the analytical voltage-loop design discussed previously. The selected parameters were later refined during nonlinear switching voltage-loop design discussed previously. The selected parameters were later refined during nonlinear switching simulations in order to improve transient response and ensure stable interaction with the inner current loop.

In addition, a voltage-dependent current limiting stage was included after the voltage controller. This block dynamically adjusts the allowable current reference according to the operating voltage conditions of the converter. Such an approach improves converter protection and prevents excessive current demand when the output voltage approaches predefined operating limits. The final output of this subsystem in the limited current reference $I_{ref,final}$, which is forward to the inner current control loop.

6.2.4 Voltage-Dependent Current Limiting Algorithm

The internal implementation of the voltage-dependent current limiting algorithm is shown in the figure 6.8

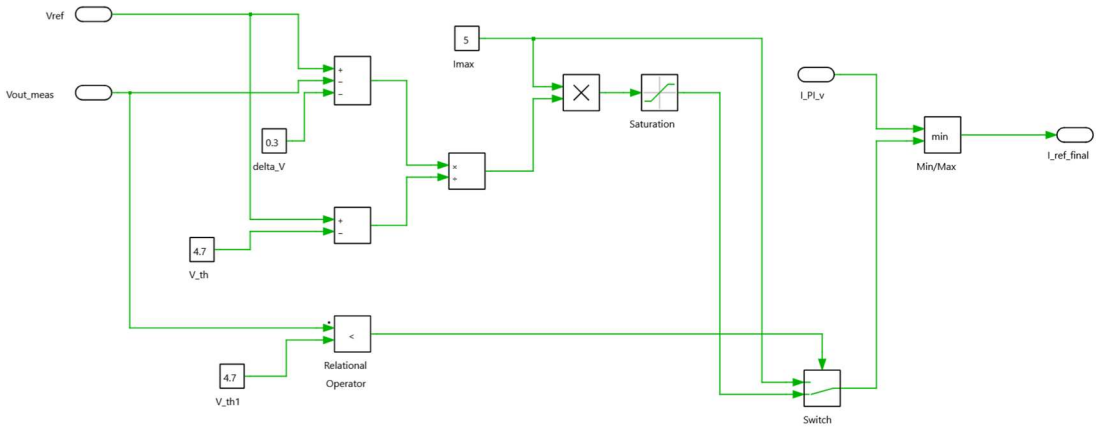


Figure 6.8. voltage-dependent current limiting algorithm implemented in the outer control loop

A voltage-dependent current limiting algorithm was implemented in order to ensure safe operation of the converter under different output voltage conditions. The algorithm dynamically modifies the maximum allowable current reference according to the measured output voltage. Threshold voltages and safety margines were introduced using predefined constants such as V_{th} and ΔV. Based on the comparison between the measured voltage and the defined thresholds, the controller adjusts the admissible current level through relational operators, saturation blocks, and switching logic.

The maximum allowable current value I_{max} was also included in the control structure to prevent excessive current stress on the converter and the supercapacitor. The resulting limited current reference is finally compared with the output of the voltage PI controller through the minimum-selection stage, ensuring that the current demand never exceeds the safe operating region of the converter. This approach improves the robustness protection capability of the overall cascaded control system.

6.2.5 Buck Current Control Loop

The implementation of the inner current loop is presented in the following figure.

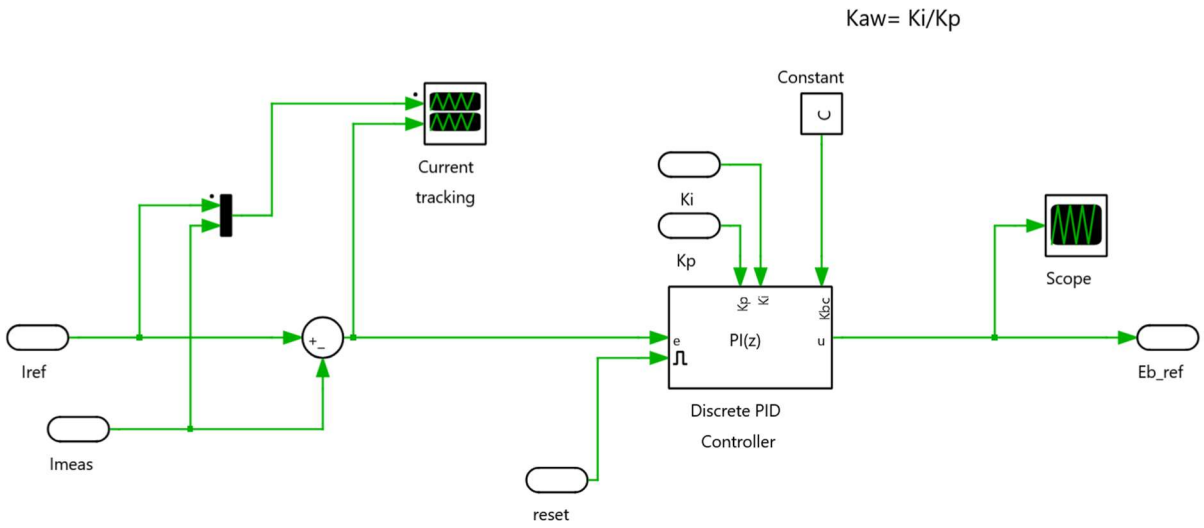


Figure 6.9. implementation of the inner current loop

The inner current loop was designed to provide fast dynamic regulation of the inductor current and guarantee accurate tracking of the reference current generated by the outer voltage loop. The measured inductor current $I_{L,meas}$ was compared with the limited reference current $I_{ref,final}$, generating the current error signal used by the controller. A discrete PI controller was employed to process the error signal and generate the control action required for current regulation. The controller gains were selected based on small-signal analysis and frequency domain design previously discussed. Anti-windup protection and output saturation were included in the control structured in order to prevent excessive controller accumulation during large transient conditions and duty-cycle limitations. The output of the current controller corresponds to the small-signal duty-cycle variation Δd , which represents the dynamics correction applied around the operating point. This signal is then forwarded to the duty-cycle computation stage, where it is combined with the feedforward duty-cycle component used for steady-state operation.

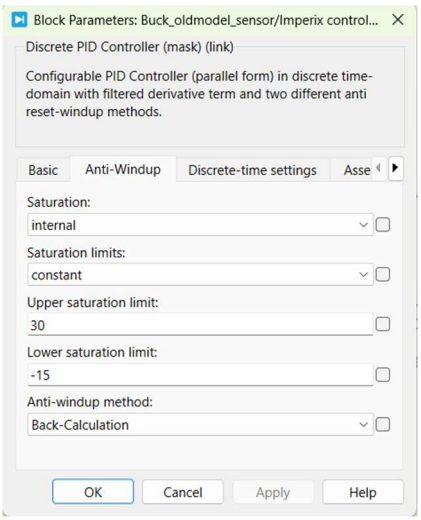


Figure 6.10.parameter configuration of the current-loop PI controller

The current loop PI controller was implemented using the Imperix discrete PI structure. The proportional gain, integral gain, anti-windup coefficient, saturation, limits , and initial conditions were configured according to the analytical design and later refined during simulation validation.

6.2.6 Duty-Cycle and PWM Generation for Buck-Mode

The final duty-cycle generation stage used for PWM modulation is shown in the following figure.

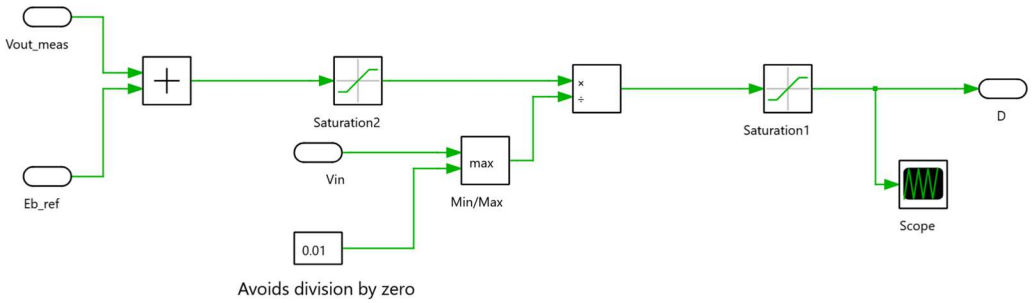


Figure 6.11. Duty-cycle computation and PWM generation stage for buck-mode operation

The duty-cycle computation stage converts the output of the current controller into the final PWM duty-cycle command applied to the switching leg. The current PI controller generates the small-signal duty-cycle variation Δd, which is added to the steady-state feed forward duty-cycle component. The feedforward term was introduced in order to improve the dynamic response of the converter and reduce the control effort required from the PI controller during steady-state operation.

The resulting duty-cycle command was limited using saturation blocks to ensure that the generated PWM signal remains within admissible operating range of the converter. Additional protection and logical blocks were also included to avoid invalid switching conditions during startup and transient operation. Finally, the computed duty-cycle value was sent to the Imperix PWM generation block, which produces the switching signal required to drive the PEB4050 switching leg in buck operation. In the implemented configuration, only the PWM high signal was connected to the switching module, while the complementary PWM channel remained disabled.

The generated PWM signals used to drive the switching leg are shown in Fig.6.12. the duty-cycle command produced by the control system is converted into a high-frequency digital PWM waveform through the Imperix PWM generation block.

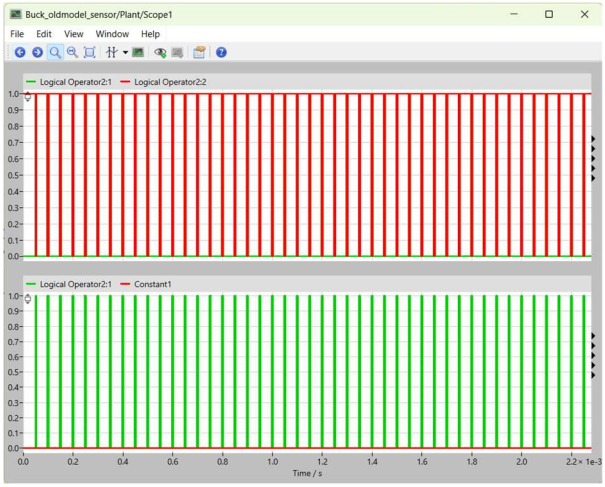


Figure 6.12 PWM modulation signal and switching waveform applied to the buck converter switching leg

The PWM generation block used for buck-mode operation is shown in Figure 6.13. the block receives the duty-cycle command generated by the digital controller and converts it into the corresponding high-frequency switching signal required to drive the converter switching leg. The PWM execution is synchronized with the control task generated by the configuration block in order to ensure deterministic digital control operation during each switching cycle. In the implemented buck-mode configuration, only the PWM high output was connected to the switching module, while the complementary PWM channel remained disabled.

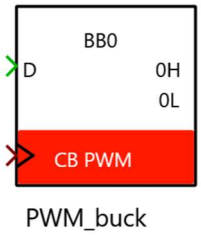


Figure 6.13. Imperix PWM block used for buck-mode switching control

6.2.7 Buck Mode Simulation Results

a) Current Tracking Performance of the Inner Control Loop

The current tracking performance of the Inner control Loop during buck-mode operation is shown in Fig.6.14. the reference current was initially limited to 5A in order to provide a controlled charging process for the supercapacitor. The measured inductor current accurately follows the reference value with a small steady-state tracking error, demonstrating the effectiveness of the designed current controller.

As the output voltage approaches the reference voltage, the voltage-dependent current limiting mechanisms progressively reduces the current reference in order to avoid excessive charging current near the final operating point. Consequently, the measured current decreases smoothly toward zero. The lower plot illustrates the current tracking error $I_{ref} - I_{meas}$, which remains small during the charging interval, confirming the stability and accuracy of the inner current loop.

Figure 6.14 Inductor Current Tracking Performance During the Charging Process in Buck-Mode Operation

b) The Output Voltage Response of Voltage Control Loop

The output voltage response during buck-mode operation is presented in Fig.6.15. the supercapacitor initial voltage was set to 4V, while the reference voltage was fixed at 5V. during the initial charging interval, the converter operates with the maximum allowed charging in an approximately linear increase of the output voltage.

When the output voltage approaches the predefined threshold value of 4.7V, the voltage-dependent current limiting block gradually reduces the current reference in order to ensure a smooth transition toward the final operating condition and to avoid excessive current stress near the voltage reference.

Although the charging current is reduced close to zero before reaching the final reference voltage, the output voltage continues increasing due to the energy previously stored in the inductor. Since the magnetic energy stored in the inductor cannot disappear instantaneously, the remaining stored energy continues to be transferred to the supercapacitor, allowing the output voltage to smoothly converge to the reference value of 5v

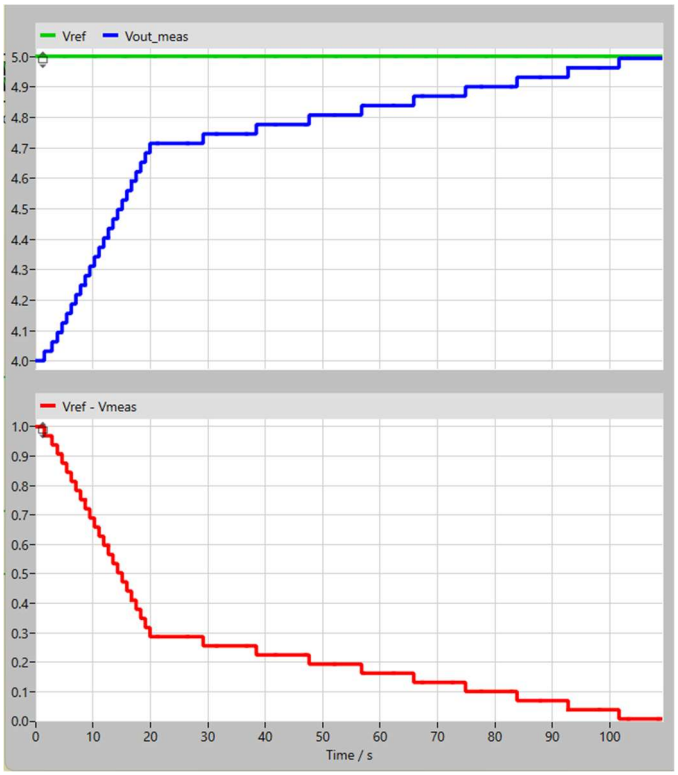


Figure 6.15 Out Put Voltage Response and Voltage regulation behaviour under voltage-dependent current limit

6.3 Boost-Mode Simulation Implementation

The boost-mode operation was implemented to transfer energy from the supercapacitor to the DC bus through controlled bidirectional power conversion. In this operating mode, the converter regulates the DC bus voltage by controlling the energy delivered from the supercapacitor through the switching action of the converter. The complete implementation was developed in PLECS together with the Imperix real-time interface blocks in order to reproduce a realistic digitally controlled power conversion system including synchronized feedback acquisition, cascaded control execution, and PWM signal generation.

6.3.1 Boost Converter Power Stage

The boost-mode power stage used in this work is shown in Figure 6.16. the converter was implemented using the Imperix PEB4050 switching module together with an inductor, DC bus capacitor, load resistor, and supercapacitor model. In the Boost operation, the energy stored in the supercapacitor is transferred to the DC bus through the switching action of the converter. The switching leg is operates as a boost converter by controlling the lower switch of the half bridge module. During the ON state of the switch, energy stored in the inductor. During the OFF states, the inductor releases its stored energy to DC bus capacitor and the load, producing an output voltage higher than the supercapacitor voltage. This operating principle allows the converter to regulate the DC bus voltage even when the supercapacitor voltage is lower than the required bus voltage.

Voltage and current probes were included in the model in order to show the realistic sensor measurements required by the digital controller. The measured signals were then fed back to the control subsystem for closed-loop operation.

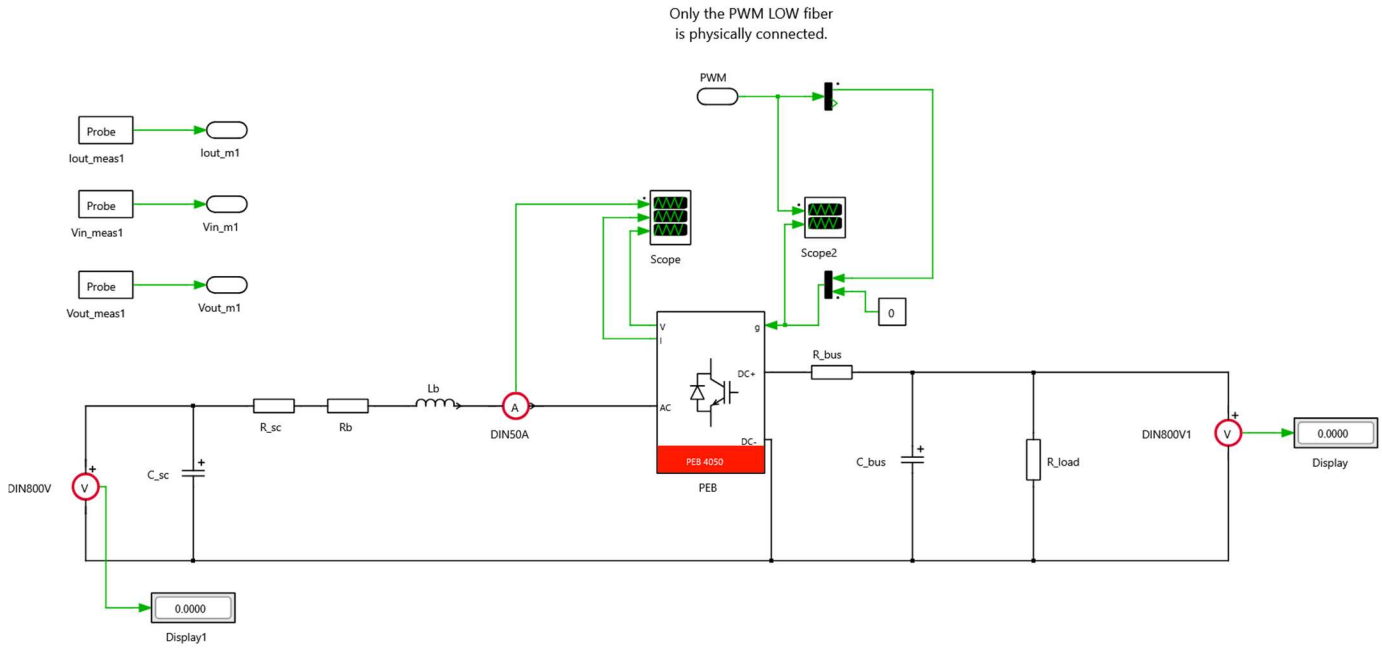


Figure 6.16. Internal implementation of the boost-mode converter power-stage in Plecs

The switching state used for the boost-mode implementation is shown in Figure 6.17. the converter was implemented using the PEB4050 switching-leg model provided within the Imperix example framework in order to maintain compatibility with the adopted digital control structure and switching configuration. Although the graphical representation differs from the standard PEB4050 block available in the Imperix library, both models represent the same half-bridge switching functionality required for converter operation.

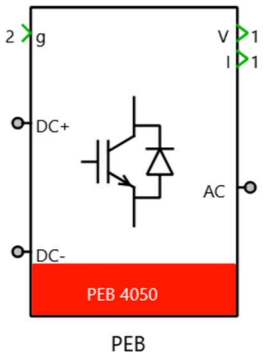


Figure 6.17. PEB4050 switching-leg model used for boost-mode implementation

6.3.2 Boost Digital Control Structure

The digital control architecture implemented for boost-mode operation is shown in Figure 6.18. the control system was developed in PLECS together with the Imperix real-time interface blocks in order to reproduce a realistic digitally controlled power conversion system. The implemented structure includes synchronized feedback acquisition, cascaded voltage and current regulation loops, duty-cycle computation, reset management, and PWM signal generation.

The measured converter variables, including the inductor current, supercapacitor voltage, and DC bus voltage, were acquired through synchronized measurement and ADC acquisition blocks and provided to digital controller as feedback signals. The voltage and current regulation loops were implemented

using the PLECS library, while the synchronization, PWM generation, and real-time interface functions were implemented using the Imperix control blocks.

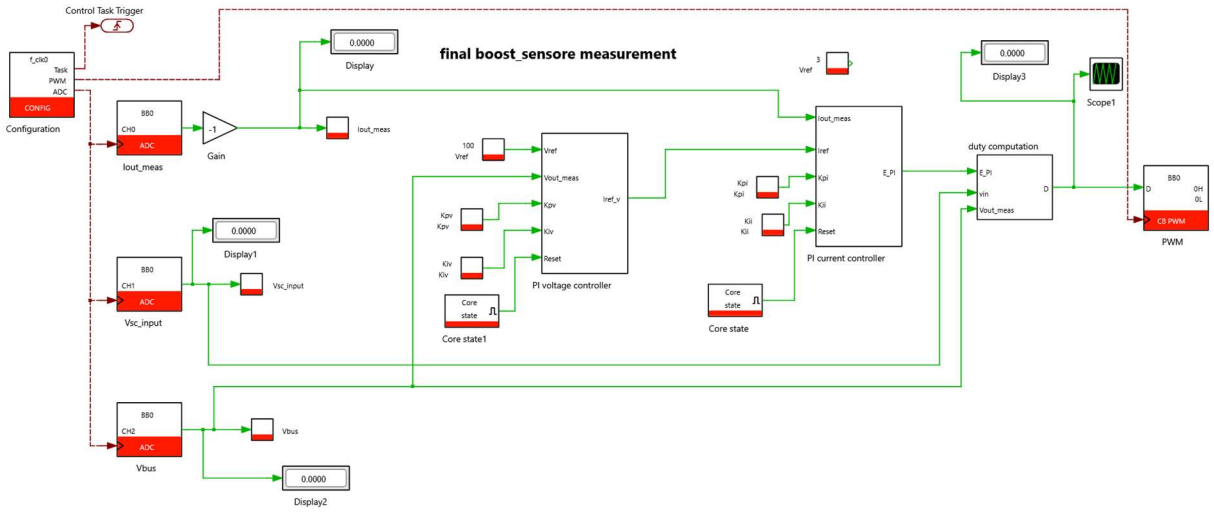


Figure 6.18. Digital control architecture implemented for boost-mode operation using PLECS and Imperix interface blocks

The synchronized feedback acquisition structure used for boost-mode operation is shown Figure 6.19. the configuration block generates the synchronization signals required for ADC acquisition, PWM execution, and control task scheduling. The measured converter variables, including the inductor current, supercapacitor voltage, and DC bus voltage, are acquired through synchronized ADC interface blocks and provided to the control algorithm as feedback signals. The control task trigger block ensures deterministic execution of the digital controller during each switching cycle.

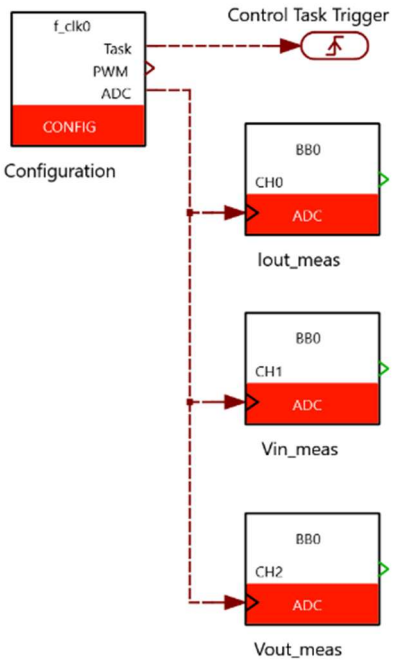


Figure 6.19 synchronized ADC acquisition and control-task implementation using the Imperix interface blocks

6.3.3 Boost Voltage Regulation Loop

The outer voltage regulation loop implemented for the boost converter is shown in Figure 6.20. the objective of this control loop is to regulate the DC bus voltage to the desired reference value by generating the appropriate current reference for the inner current loop. The measured DC bus voltage is continuously compared with the reference voltage, and the resulting voltage error is processed by a discrete-time PI controller implemented using the PLECS control library. The proportional and integral gains of the controller were extremely defined in order to allow flexible tuning and easier controller adjustment during the design process. The controller output corresponds to the reference current required from the inductor in order to maintain the DC bus voltage at the desired operating point. A saturation block was added after the PI controller in order to limit the generated current reference and prevent excessive current demand during transient conditions or startup operation.

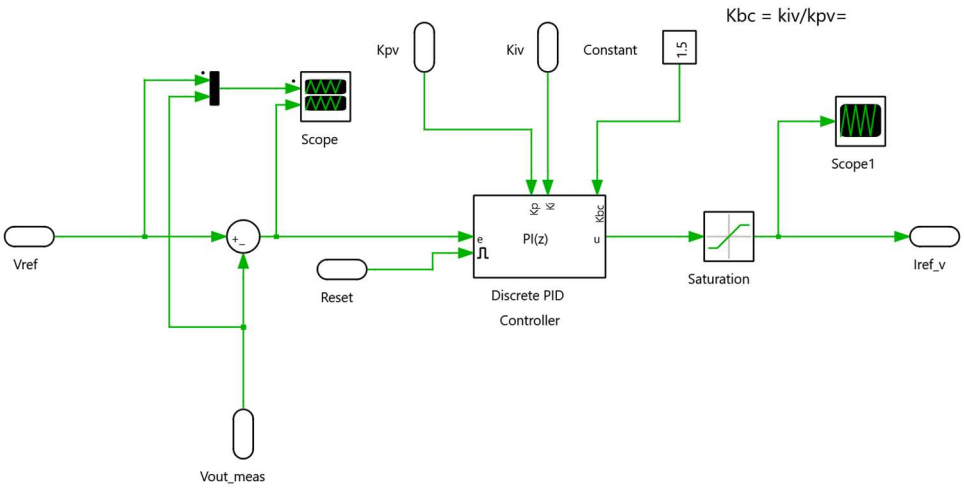


Figure 6.20. Implementation of Boost-mode outer voltage control loop

As shown in Figure 6.21. the PI controller was configured in discrete-time mode with external parameter definition and anti-windup capability. The external reset input was also enabled in order to properly initialize the controller during operating mode transitions and simulation startup conditions. The voltage loop represents the slow dynamics of the cascaded control structure, while the inner current loop provides the fast dynamic response required for stable boost converter operation.

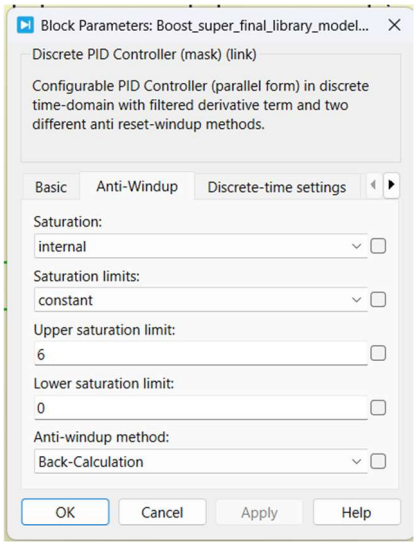


Figure 6.21. configuration parameters of the discrete PI voltage controller

6.3.4 Boost Current Control Loop

The inner current loop implemented for the Boost converter is shown in Figure 6.22. this control loop is responsible for regulating the inductor current and ensuring fast dynamic response during power transfer from the supercapacitor to the DC bus. The measured inductor current ensuring fast dynamic response during power transfer from the supercapacitor to the DC bus. The measured inductor current is continuously compared with the reference current generated by the outer voltage loop. The resulting current error is processed by a discrete-time PI controller implemented using the Imperix digital control library. The proportional and integral gains were externally defined in order to simplify controller tuning and allow independent adjustment of the current loop dynamics. The output of the PI controller represents the control action required to regulate the energy stored in the inductor. Since the current loop is the fastest loop in the cascaded control structure, it directly determines the transient performance and stability of the converter. A gain block was included after the controller output in order to properly scale the control signal before duty generation

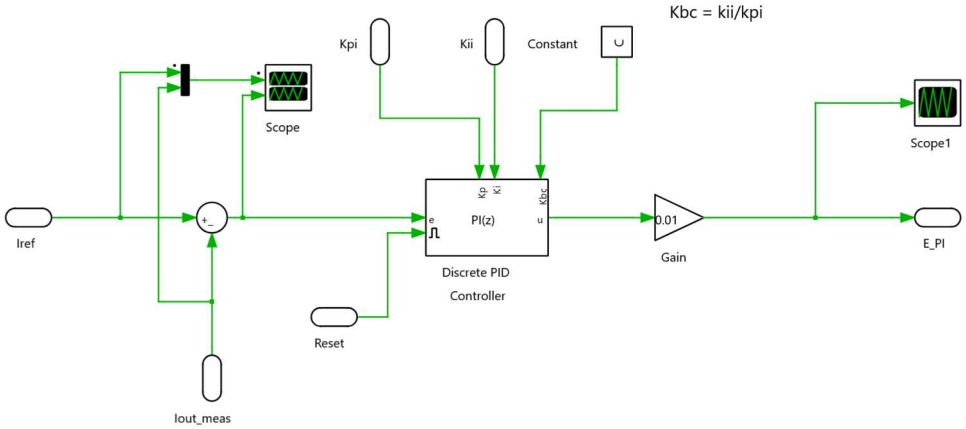


Figure 6.22 Inner current loop implemented for boost-mode operation

Similar to the voltage controller, the PI controller was configured in discrete-time mode with anti-windup capability and external reset functionality to ensure stable operation during transient conditions and startup. The current controller bandwidth was selected significantly higher than the voltage-loop bandwidth in order to maintain proper separation between the fast and slow dynamics of the cascaded control structure.

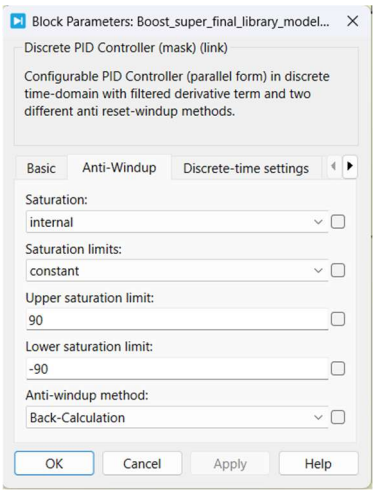


Figure 6.23 configuration parameters of the discrete PI current controller

6.3.5 Boost Duty-Cycle and PWM Generation

The duty-cycle computation stage implemented for the boost converter is shown in Figure 6.24. the objective of this block is to convert the output of the current controller into the final PWM duty-cycle command required to drive the switching leg. The current PI controller generates the small-signal duty-cycle variation Δd, which represents the dynamic correction around the operating point. In order to improve the converter dynamics response and reduce the control effort required from the feedback controller, a feedforward duty-cycle component was also include in the implementation.

The feedforward duty-cycle component was therefore computed using the measured input and output voltages. The final duty-cycle command was obtained by summing the feedforward term and controller-generated variation Δd: $d = D + \Delta d$

A saturation stage was included in order to ensure that the generated duty cycle remains within the allowable operating range of the converter and to avoid invalid switching conditions. Since the implemented boost configuration uses only the lower switch of the switching leg, the final PWM command was applied exclusively to the PWM low output of the Imperix module, while the complementary PWM channel remained disabled.

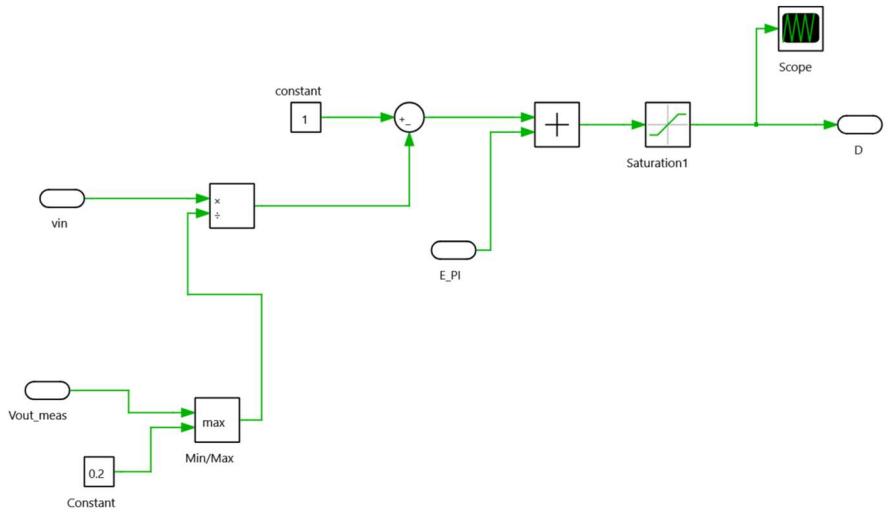


Figure 6.24 Duty-Cycle computation and PWM generation

The figure 6.25 shows the PWM waveform, that applied to the switching pole.

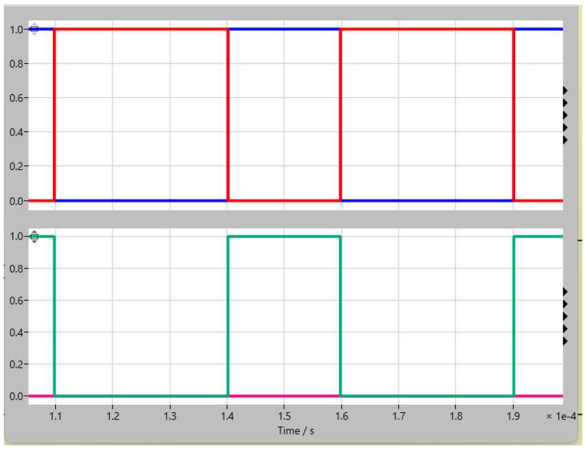


Figure 6.25. Boost PWM waveform generated to

The PWM generation block used for boost-mode operation is shown in Figure 6.26. the block receives the duty-cycle command generated by the digital controller and converts it into the corresponding high-frequency switching signal required to drive converter switching leg. The PWM execution is synchronized with control task generated by the configuration block in order to ensure deterministic digital control operation during each switching cycle. The generated PWM signal is then applied to the PEB4050 switching module to regulate the energy transfer from the supercapacitor to the DC bus during Boost-mode operation.

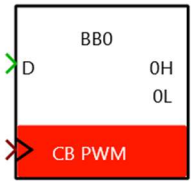


Figure 6.26. Imperix PWM generation block used for boost-mode switching control

6.3.6 Boost-Mode Simulation Results

A) Current Tracking Performance

Figure 6.27. shows the current tracking performance of the inner current loop during boost-mode operation. The upper plot compares the reference current generated by voltage controller with the measured inductor current, while the lower plot shows the corresponding tracking error.

The results demonstrate that the implemented current controller is capable of accurately tracking the reference current generated by the outer voltage loop. During the startup transient, the controller rapidly increases the inductor current in order to transfer energy from the supercapacitor to the DC bus. After the transient period, the measured current follows the reference current with small tracking error, confirming the effectiveness of the implemented cascaded control structure.

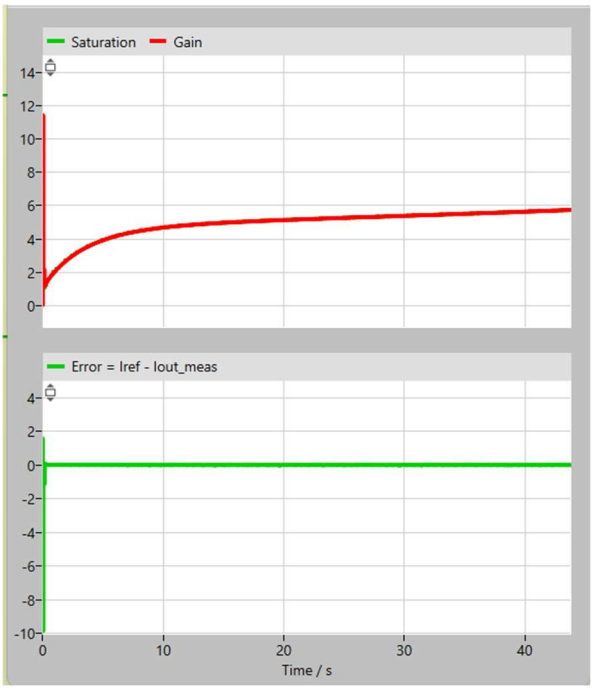


Figure 6.27. Inductor Current Tracking Performance of the Boost-Mode Current controller

B) DC Bus Voltage Regulation

Figure 6.28. presents the DC bus voltage response during boost-mode operation. The upper plot shows the measured Dc bus voltage together with the reference voltage, while the lower plot shows the corresponding voltage regulation error.

At the beginning of the simulation, the controller increases the converter current in order to charge the DC bus capacitor and raise the output voltage toward the reference value. The results show that the DC bus voltage successfully converges to the desired reference voltage with stable dynamic behaviour and limited overshoot.

After the output voltage reaches the desired reference voltage, the controller continuously adjusts the converter current in order to compensate, the load demand and maintain the DC bus voltage close to the reference value. This behaviour demonstrates the effectiveness of the outer voltage loop and confirms the proper interaction between the voltage and current control loops in the cascaded control structure.

The lower plot shows that the voltage error decreases rapidly during the transient response and remains small during steady-state operation, indicating satisfactory regulation performance.

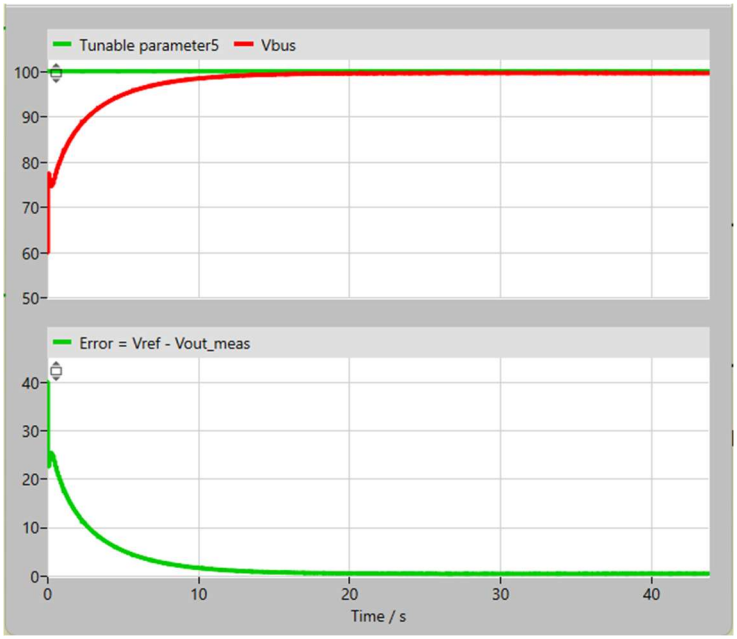


Figure 6.28. DC bus voltage regulation during Boost-Mode operation

Chapter 7: Experimental Setup and Practical Validation

7.1 Experimental Platform Overview

The experimental validation of the proposed bidirectional converter was carried out using the Imperix real-time control platform. The practical setup was based on a B-Box RCP controller, a PEB4050 power module, and a 19-inch rack system used to integrate the converter hardware in a laboratory environment. This platform allows the control algorithm developed in simulation to be implemented on real hardware, while providing synchronized PWM generation, analog signal acquisition, and real-time controller execution . Therefore, the experimental setup represents the practical counterpart of the PLECS-Imperix simulation model presented in the previous chapter.

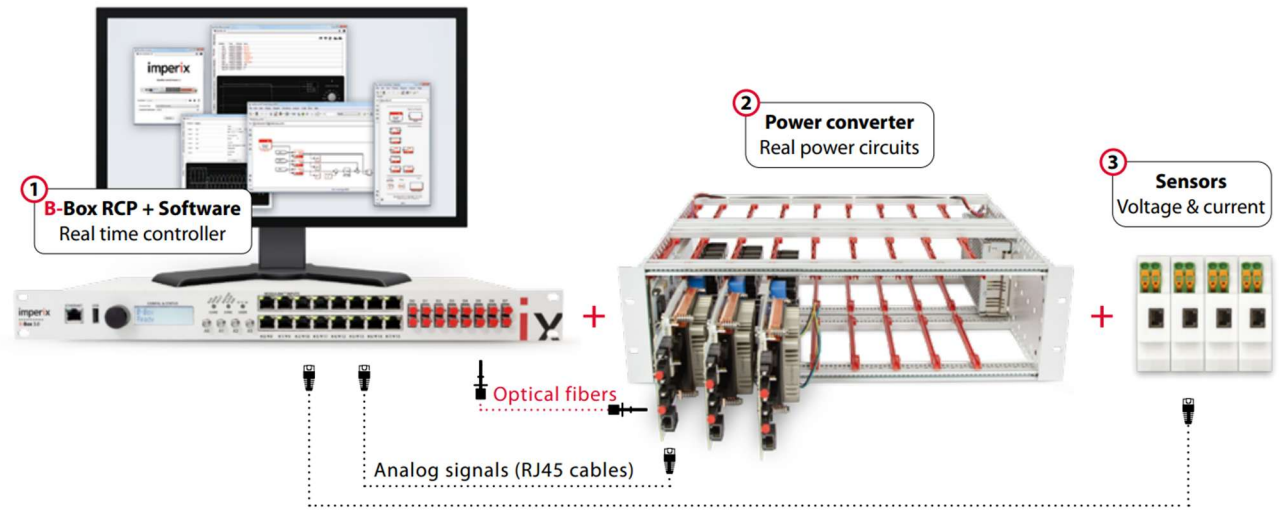


Figure 7.1. the Image showing B-Box RCP controller, PEB4050 power module and 19-inch rack

Source: adapted from [18]

7.2 B-Box RCP controller

The B-Box RCP controller was used as the central digital control unit of the experimental setup. It executes the control algorithm in real time and generates the PWM signals required to drive the power module. The measured current and voltage signals are acquired through the analog input channels of controller and are then processed by the voltage and current regulation loops. In this work, the B-Box controller provides the interface between the control structure developed in software and the physical converter implemented in the laboratory. The following Figure shows the B_Box RCP 3.0

Figure 7.2. B-Box RCP controller used for real-time execution of the converter control algorithm

Source: adapted from [18]

7.3 PEB4050 Power Module

The power conversion stage was implemented using the Imperix PEB4050 module. This module provides the half-bridge switching structure required for both buck-mode and boost-mode operation. In the experimental setup, the PEB 4050 receives the PWM command generated by the B_BOX controller and applies the corresponding switching action to the converter power stage. The same hardware module was used for the validation of both operation modes, which ensures consistency between the simulated switching -leg model and the practical converter implementation. Following Figure shows the power module.

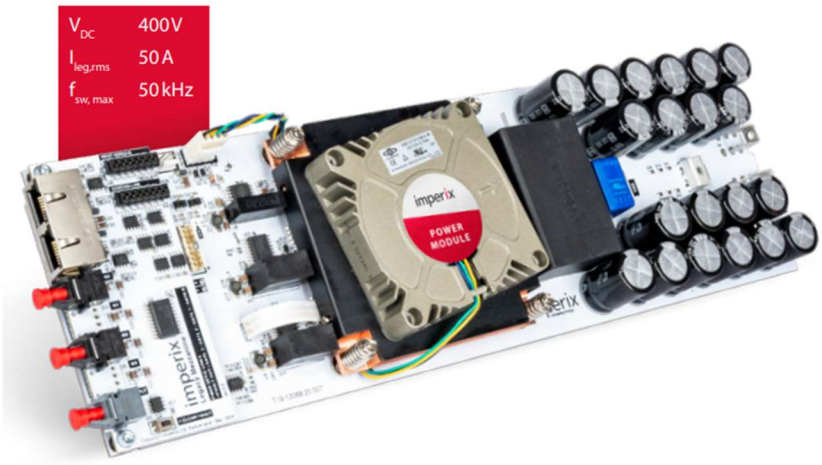


Figure 7.3. PEB4050 power module used as the half-bridge switching stage of the converter

Source: adapted from [18]

7.4 Laboratory Setup

The complete laboratory setup is shown in Figure 7.4. the setup includes the B-Box RCP controller, the half bridge converter module, the supercapacitor bank, the DC power supply, and the oscilloscope used for waveform acquisition. The B-Box controller generates the PWM signals and acquires the measured feedback variables, while the PEB4050 module performs the actual switching operation. The supercapacitor bank represents energy storage element of the system, and the oscilloscope was used to observe the converter current, voltage, and switching waveforms during the experimental tests.

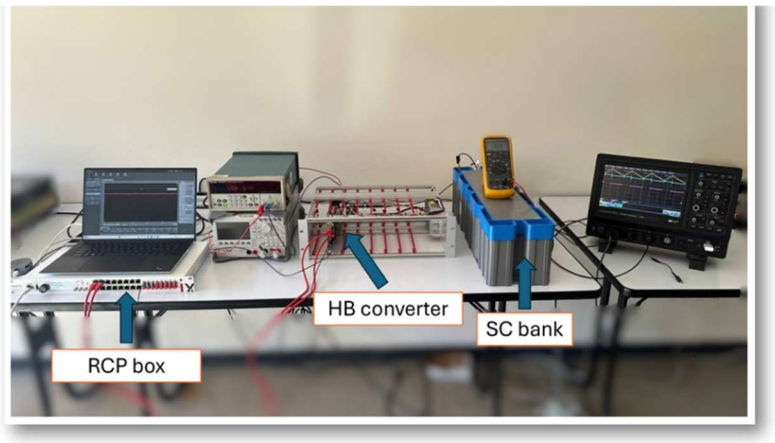


Figure 7.4. Laboratory setup used for the experimental validation of the converter system.

7.5 Experimental Buck-Mode Validation

The buck-mode operation was experimentally tested in order to validate the charging process of the supercapacitor from the DC supply. During this test, the converter was operated with the PWM signal generated by the B-Box controller and applied to the PEB4050 switching module. The measured waveforms confirm that converter operates correctly in buck mode, with the inductor current following the expected behaviour and the switching-node voltage showing the characteristic PWM waveform. This result verifies the practical implementation of the buck-mode control and switching structure.

a) Steady-State Buck-Mode Operation

Experimental measurements were carried out in order to validate the practical operation of the implemented buck converter. The measurements were obtained using the laboratory together with oscilloscope-based waveform acquisition. The experimental results confirm the switching behaviour, inductor current dynamics, and PWM operation predicted by the simulation model.

Figure 7.5 shows the experimental steady-state operation of the buck converter during the charging process. The oscilloscope measurement indicates an average inductor current of approximately 5A, which is consistent with the reference current imposed by the controller. This result confirms the correct tracking capability of the current control loop and demonstrates good agreement between the theoretical analysis, simulation results, and practical implementation.

The switching-node voltage presents the expected PWM switching behaviour, while the inductor current exhibits the characteristic ripple associated with buck-converter operation.

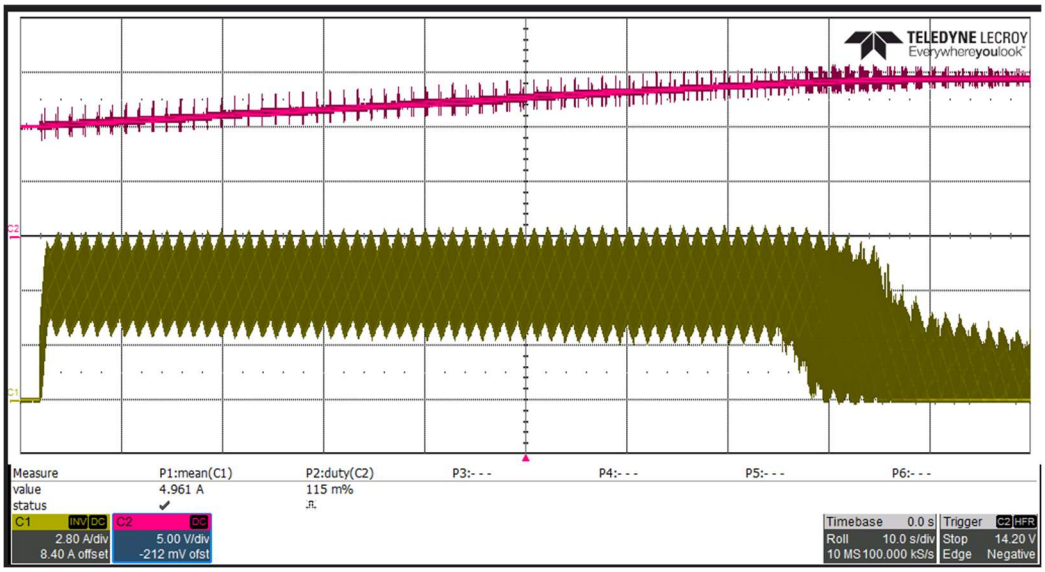


Figure 7.5 experimental measurement of the inductor current and switching-node voltage during steady-state

b) High-Frequency Switching and Inductor Current Ripple

Figure 7.6 presents a zoomed view of the converter switching behaviour during buck-mode operation. Compared with the previous figure, the oscilloscope time scale was reduced in order to clearly observe the high-frequency switching phenomena and inductor current ripple.

The oscilloscope measurement indicates an average inductor current of approximately 6A, which is consistent with the reference current imposed by the controller which again confirms the correct tracking capability of the current control loop.

The switching-node voltage shows the expected square-waveform generated by the PWM control signal, while the inductor current exhibits a triangular ripple caused by the periodic charging and discharging of the inductor during each switching cycle. The experimental waveform validates the expected behaviour predicted by the converter theory and simulation model.

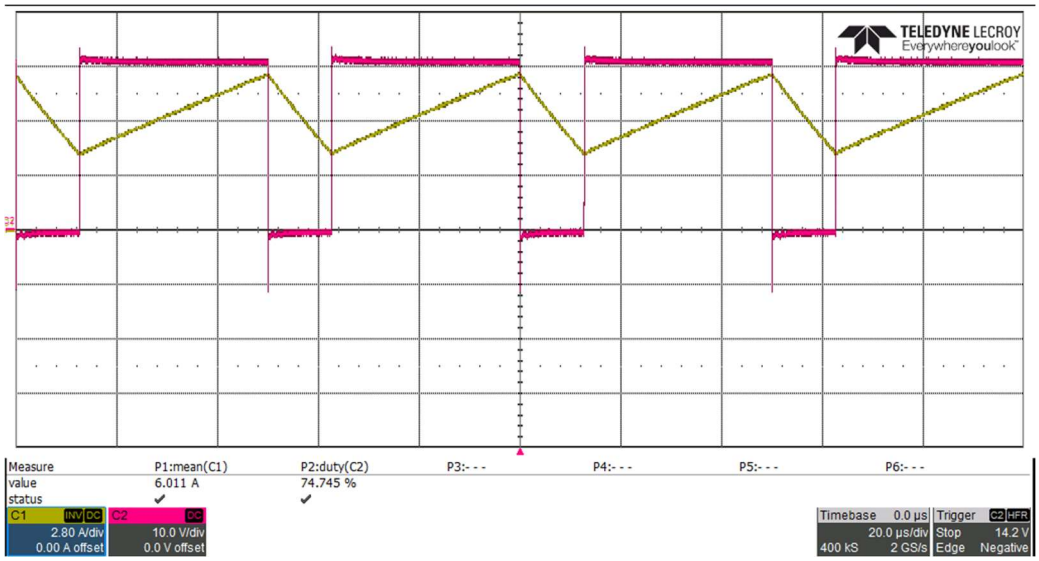


Figure 7.6 zoomed experimental waveform of the inductor current ripple and switching-node voltage

c) Transient Response After Current Reference Reduction

Figure 7.7 experimental transient behaviour of the converter after the supercapacitor voltage reached the reference voltage value. At this operating point, the voltage control loop reduced the reference current toward zero because the desired output voltage had already been achieved. Consequently, the current controller also forced the inductor current to decrease.

As observed in the oscilloscope measurement, the inductor current does not instantly become zero. Due to the energy previously stored inside the inductor, the current requires a finite amount of time to decay. As the current reference is progressively reduced by voltage control loop, the average inductor current decreases to very low values. Under theses light-load conditions, the inductor current reaches zero before the beginning of the next switching period, indicating a transition from Continuous Conduction Mode (CCM) to Discontinuous Conduction Mode (DCM). The DCM operation is clearly visible in following figure, where intervals with zero inductor current can be observed. This behaviour is expected when the power demand becomes very small and confirms the correct operation of the converter during low-load conditions.

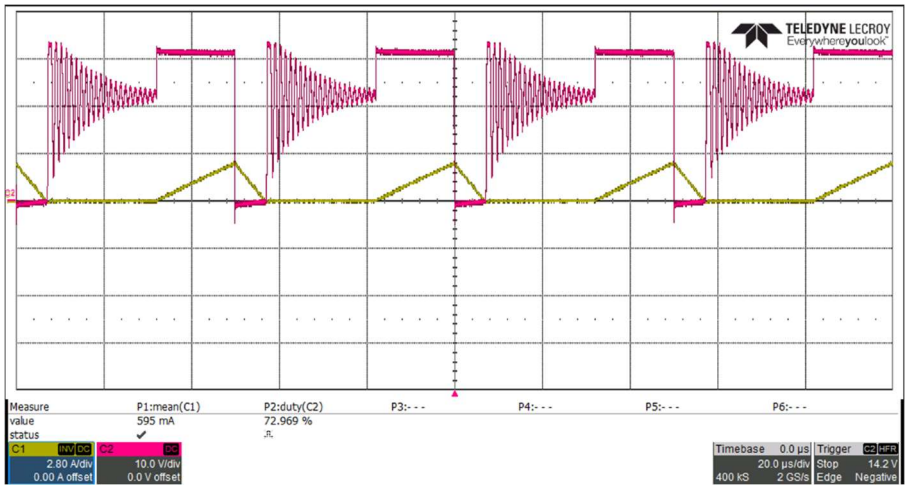


Figure 7.7 experimental transient response after the inductor current reference approached zero

7.6 Experimental Boost-Mode Validation

Figure 7.8 shows the experimental waveforms obtained during boost-mode operation of the bidirectional converter. The supercapacitors delivers energy to the DC bus, resulting in a reverse current direction of inductor with a measured mean value of approximately -14.92 A. the inductor current exhibits the expected triangular waveform due to the periodic charging and discharging process of the inductor during switching operation. During the switch ON interval the stored energy is transferred to the DC bus, leading to a linear decrease of the current. The measured voltage across the supercapacitor remains approximately 24.83 during the observed interval, confirming stable boost operation.

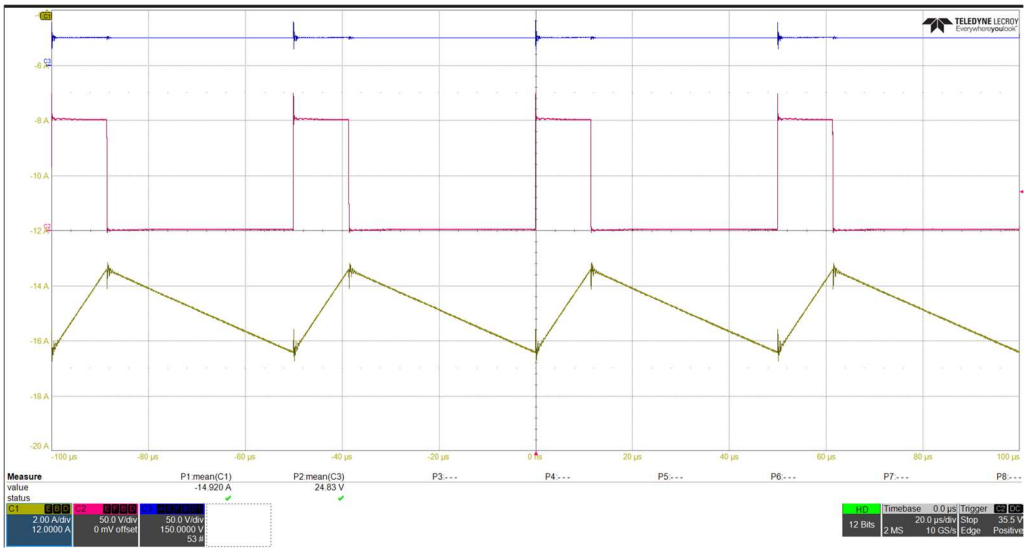


Figure 7.8 experimental boost-mode operation waveforms

7.7 Conclusion

This thesis investigated the design, modelling, control, simulation, and experimental validation of a bidirectional DC-DC converter intended for use in a Hybrid Energy Storage System (HESS) combining a battery and a supercapacitor. The motivation for this work originates from the increasing penetration of renewable energy sources, whose intermittent and highly dynamic nature requires energy storage

systems capable of providing both high energy density and rapid transient response. In this context, batteries and supercapacitors exhibit complementary characteristics, making their integration an attractive solution for modern energy management applications.

The first part of the work reviewed the fundamental characteristics of batteries and supercapacitors, highlighting their advantages, limitations, and electrical modelling approaches. Particular attention was given to supercapacitors due to their high power density , fast charge-discharge capability, and suitability for transient power support. The concept of a Hybrid Energy Storage System was then introduced as a means of combining the long-term energy capability of batteries with the fast dynamic response of supercapacitors.

A complete test system architecture was subsequently developed. The proposed system integrates a photovoltaic source , a battery storage unit , a supercapacitor module, a bidirectional DC-DC converter and a dynamic load. The converter acts as the key power-electronic interface responsible for regulating energy transfer between the DC bus and the supercapacitor. Depending on the direction of power flow, the same half-bridge converter structure operates either in buck mode, during supercapacitor charging , or boost mode, during supercapacitor discharging.

A detailed mathematical analysis of buck converter was carried out . Steady-state equations, averaged models, and small-signal transfer functions were derived. Based on these models, a cascaded control architecture composed of an inner current loop and outer voltage loop was designed. PI controller parameters were calculated using the Optimum Magnitude Method, allowing systematic controller tuning while accounting for converter delay and dynamic characteristics. MATLAB verification confirmed the expected stability margins and dynamic performance.

The same design methodology was then applied to the boost operating mode. Starting from the converter switching states, an averaged nonlinear model and a small-signal representation were obtained. The current-loop and voltage-loop controllers were designed following the same control philosophy used in buck operation. Simulation results demonstrated satisfactory voltage regulation, current tracking capability, and stable converter behaviour under different operating conditions.

The theoretical models and controller designs were implemented within a digital simulation environment based on PLECS and Imperix-oriented control structures. The complete control architecture , including PWM generation, current limitation functions, and cascaded regulation loops, was successfully integrated into the simulation framework. Simulation results validated the effectiveness of the proposed control strategy in both charging and discharging operating modes.

Finally, practical validation was performed using the Imperix B-Box RCP controller and the PEB4050 power converter module. Experimental results confirmed the feasibility of implementing the proposed control strategy on real hardware. The measured converter behaviour showed good agreement with the theoretical predictions and simulation results. Both buck-mode and boost-mode operation were successfully demonstrated, validating the effectiveness of the converter as an energy-transfer interface within a hybrid energy storage system.

Overall, the results demonstrate the proposed bidirectional converter provides an effective solution for controlled energy exchange between a supercapacitor and a DC bus. The combination of analytical modelling, controller design, simulation verification, and experimental implementation

provides a complete engineering framework for the integration of the supercapacitor based storage systems into future renewable-energy and hybrid-storage applications. The developed methodology can also serve as a foundation for future investigations involving advanced energy-management algorithms, larger-scale hybrid storage systems, and real-time optimization strategies.

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