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Design and Validation of a Motor Drive Inverter Board for Robotic Applications using GaN Monolithic Integrated Circuits

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"The progressive development of man is vitally dependent on invention."

— NIKOLA TESLA

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Summary

The topic of this work is to show all the advantages of using GaN based integrated motor drives in low-voltage robotic applications, especially for humanoid robot joints and drone motors. The thesis consists of three main parts: State-of-the-Art of robotic applications and GaN Monolithic Power Integrated Circuits; Motor drive inverter board design using EPC33110; Experimental validation of the evaluation board.

The first part contains an overview of the most advanced robotic applications, from humanoid robots to Unmanned Aerial Vehicles (UAVs), which points out how power converters will have an increasingly crucial role in their development. In particular, the growing usage of Wide-Bandgap Semiconductors (WBG) is revolutionizing the design of integrated motor drives, since the inherent material properties of SiC and GaN enable faster switching speeds, higher operating temperatures, reduced conduction and switching losses and improved power density. For instance, the higher switching frequencies allow for the miniaturization of passive components like capacitors and inductors, while the high-level of integration inside the newest Monolithic Power Integrated Circuits simplifies and optimizes the power converter design, allowing to achieve a compactness never reached in Silicon-based converter designs. Therefore, after a brief overview of GaN Power Devices technologies and typical applications, the focus is moved onto the State-of-the-Art of GaN Monolithic Power Integrated Circuits, highlighting the advantages but also the actual limitations in using this new technology. After that, a detailed description of EPC33110 Three-Phase ePower™ Stage IC is carried out, in order to completely understand the electrical and thermal behavior of the device, and so to properly design the evaluation board.

The second part starts with a preliminary analysis on two commercial integrated motor drives for outlining the mechanical constraints, power requirements and functional block diagram of the evaluation board which will be named EPC91132. The first motor to be characterized is a servo joint motor (LKTECH MG8008E-i9 V3), which has a larger inverter board than the one used in the second motor (Vertiq 23-06 G1 220KV and 2200 KV versions), that is a small drone motor. Due to the large differences in size just as in current and voltage ratings, the evaluation board will be designed to have two possible frame outlines: the bigger one is designed to fit the entire board inside the first motor, while the smaller one can be disconnected and used to drive the drone motor in a standalone configuration. Therefore, an entire chapter is dedicated to show how all the components are chosen and how the design of the PCB is carried out to optimize the arrangement for achieving the highest power density and the best performances in terms of efficiency and motor control. The main concerns are linked to the choice and sizing of micro-controller, current sensing, position sensing, housekeeping power supplies, DC bus capacitors, passive components needed by the 3-phase IC power stage and additional on-board functions, such as temperature sensing, RS485 interface and PWM ESC handling.

The third and last part is entirely focused on the experimental validation of the evaluation board, which has been manufactured and assembled following the standard EPC procedures. Before showing all the tests performed on the power board, an overview of the STM32 Motor Control Firmware Architecture is provided, together with some modifications added to fulfil some additional functions. Then the switching performances of the power devices are evaluated, measuring the voltage slew rates under different conditions and comparing them with equivalent LTspice simulations. Since some problems have come up in closing the speed loop with the position sensing from the magnetic encoder due to mechanical misalignments, a compensation strategy by firmware is showed. After that, the thermal behaviour of the evaluation board is analysed both in steady state conditions and during impulsive tests, in order to find the current ratings based on the type of operation. So, the EPC91132 inverter board is validated in the two low-voltage robotic applications, measuring the performance and efficiency of the GaN integrated motor drive in both servo joint motor and drone motor. In addition, some DC bus voltage ripple measurements are performed in order to verify the previously proposed method used for the DC bus capacitors sizing.

Finally, the main results of the work are highlighted, together with the future prospects for further developments in low-voltage integrated motor drives using GaN monolithic power integrated circuits.

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Chapter 1

Introduction

1.1 Actual Trends in the Robotic Field

Nowadays, robotic applications are experiencing a comprehensive and very fast development, also thanks to the newest technologies introduced in power electronics. On one side, humanoid and quadruped robots already have a pivotal role in national technological advancement, because these applications will have a huge impact on the future global economic and industrial competition. In particular, humanoid robots are gaining the ability to emulate and, maybe one day, also to overcome human capabilities, thanks to the growing adoption of the most innovative technologies in the fields of advanced manufacturing, novel materials, and artificial intelligence.

Starting from the first bipedal robot created in 1969 by Ichiro Kato from Japan's Waseda University [2], humanoid robots have currently entered an industrialization phase in which products and applications are the main driving force, allowing the possibility to achieve low-cost and large-scale production. For instance, the first prototype of its humanoid robot Optimus was introduced by Tesla in 2022, with a height of 173 cm and a weight of about 56 kg, which demonstrated only basic abilities such as walking, watering plants, and moving metal rods. However, in the next year, Optimus Gen2 was able to show more complex tasks: standing still while grabbing some objects; learning human movements through mapping; walking with good stability in factory environments; using autonomous driving technology for environmental perception and intelligent navigation.

Another remarkable example of a humanoid robot with advanced capabilities (such as making coffee and moving materials into bins) is Figure 01, released by the U.S company Figure AI in 2023. Moreover, the following year, Figure AI managed to have a collaboration with OpenAI, and so, thanks to a neural network strategy model, Figure 01 achieved even more complex operations, from the desktop environment perception to facilitating smooth human-robot dialogue, but also arranging cups and plates on a draining rack based on a neural network strategy model. Boston Dynamics started in 1986 with the bipedal walking theory, when Marc Raibert, its founder, introduced the concept of dynamic balance control. Then, in 2013, the first version of the humanoid robot Atlas was developed to accomplish rescue and special operations, with the specific ability to walk stably on rubble-filled terrain. The company gradually enhanced Atlas's dynamic movement capabilities over the next decade, achieving outstanding improvements in virtual model control, nonlinear model predictive control, and full-body control, allowing its

humanoid robot to perform unusual actions such as parkour, triple jumps, whole-body coordinated dances, running and jumping onto steps, and walking on a balance beam. Finally, in April 2024, Boston Dynamics released a fully electric version of Atlas, which can rise from the ground and features joints capable of rotating 360° .

Regarding Chinese companies, in 2023, Unitree launched a general-purpose humanoid robot with a height of 180 cm and a weight of 47 kg, named H1, which was already capable of fast running, stair climbing, and resisting external disturbances. In 2024, Unitree released another humanoid robot, the G1, shorter (127 cm) and lighter (35 kg) than the previous, but with enhanced potentiality, as it can integrate a three-finger force-controlled dexterous hand and demonstrate flexible full-body movement abilities such as getting up and jumping. [2]

As can be seen in Figure 1.1, humanoid robots need a multidisciplinary technological framework to achieve human-like abilities, and so innovation efforts must push in many directions. One of the most important aspect that influence the behavior of the entire system is surely the control and conversion of electrical energy, since it is responsible for delivering power to the electronic components needed for motion control, environmental perception, and sensors. At the same time, most of the actuation methods rely on electrical motors, progress towards new technologies and solutions in power converters (especially for three-phase inverters) is focused on enabling higher operating temperatures, reducing conduction and switching losses, and reaching faster switching speeds, as will be explained in more detail in section 2.3.

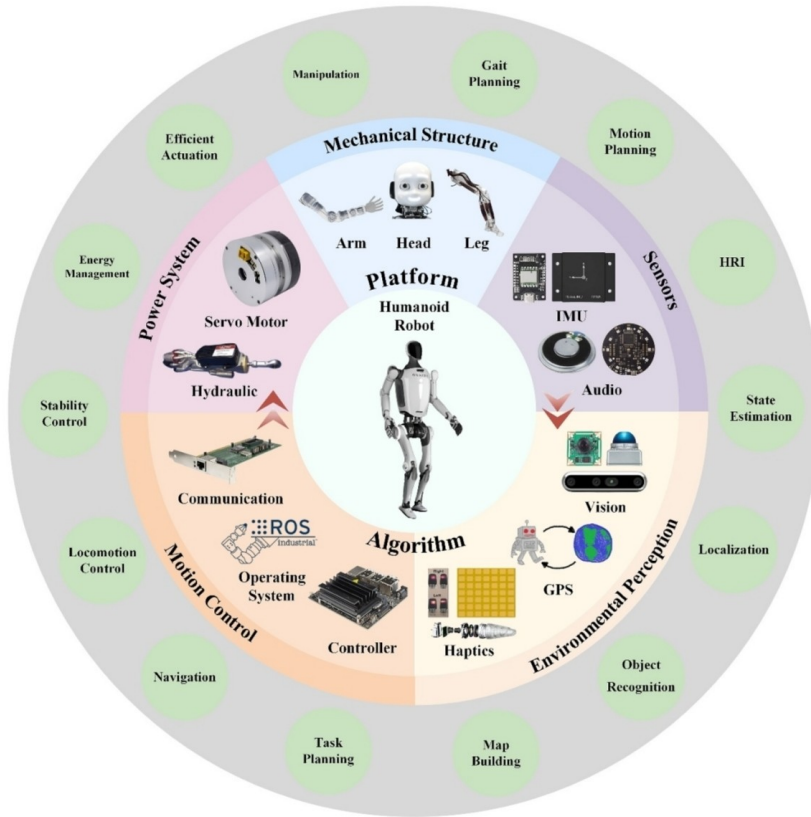


Figure 1.1: Technological framework of humanoid robot [2].

On the other hand, robotic applications also include the so-called Unmanned Aerial Vehicles (UAVs), i.e., drones, which in turn became extremely important throughout a wide variety of fields: from military operations to civilian uses like waste management, agriculture, logistics, surveillance, and entertainment. In fact, thanks to their adaptable capabilities, drones have been initially developed to perform military tasks, such as inspection and tactical strikes, while in the last decades, the focus on unhostile activities has considerably grown. Digital innovations in remote sensing, wireless connectivity, and autonomous flight systems have allowed to achieve great performances in a really wide range of sectors: photography, video shooting during sports events, delivery services, infrastructure inspection, rescue operations, disaster management, and even for cartography and archaeology surveying.

Figure 1.2 graphically represents actual applications of commercial drones in different sectors.

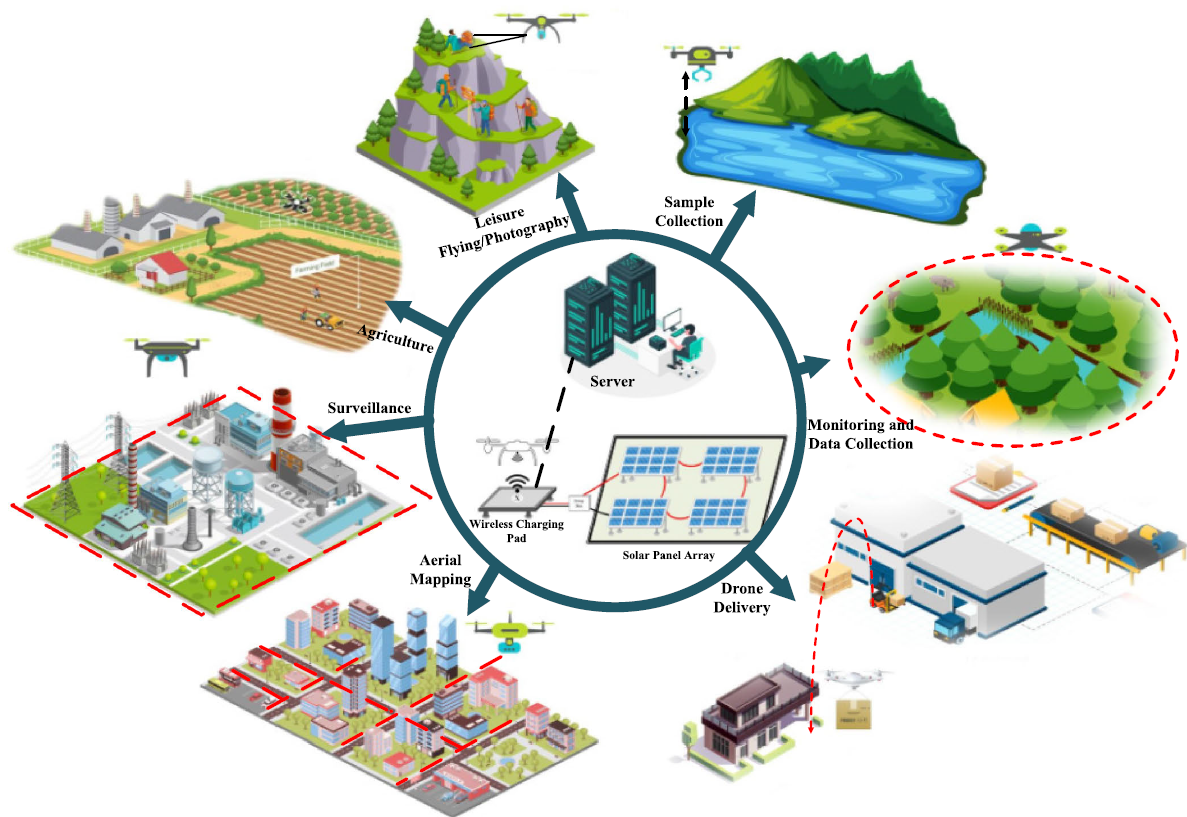


Figure 1.2: Typical applications of commercial drones [3].

Another key index that shows how UAVs are reshaping our world is the global drone market size, which is estimated at \$83.8 billion in 2025 and is projected to double by 2033 [4]. It is also noticeable how this market is highly fragmented, since high-end military UAVs share it with consumer drones, testifying to the great versatility of this robotic application.

In Figure 1.3, the five current most fruitful drone companies in the world are presented. The ranking is led by DJI, founded in 2006 by Frank Wang (Wang Tao), since this Chinese company is the global largest drone manufacturer. This is also obtained because DJI pioneered easy-to-use quadcopters, integrated advanced flight control and AI-assisted functions, maintaining a user-friendly approach in designing new products.

The second one is the European drone leader, which was founded by Henri Seydoux in 1994. This company is focused on providing professional micro-UAVs, in which high-end sensors (4K,

thermal, multispectral) are packed into robust and portable frames. Therefore, these products are suitable for industrial inspection (buildings, powerlines), agriculture mapping (Sequoia sensor), and public safety (police surveillance, firefighting).

Skydio is one of the most important US drone companies in terms of innovation. It was founded in 2014 by MIT roboticists and its focus is on highly autonomous flight, in fact, their drones are able to automatically avoid obstacles and track subjects, even without GPS, since they are characterized by outstanding performances in computer vision and AI autonomy.

The main industrial rival of DJI is Autel Robotics, which was founded in 2014 in Shenzhen (China), while now its labs and distribution are located in both China and the USA. The strength of this company is that it invests heavily in advanced research into cutting-edge drone technologies. Thanks to the superior hardware, in terms of image handling, offered by their products, Autel drones are most suitable for aerial photography and cinematography, but also for rescue operations, surveillance, and agriculture management.

The fifth company (AeroVironment) is mainly involved in manufacturing drones for military purposes, since it is the leading U.S. military supplier for small UAVs. It was founded by a renowned American aeronautical engineer, Paul MacCready, in 1971. AeroVironment claims more than 50,000 lightweight battlefield UAVs delivered during several wars since the 2000s, which are optimized for tactical battlefield ISR, loitering weapons, and counter-drones [4].

A more detailed overview of the various drone types and architectures will be provided in Section 2.2.

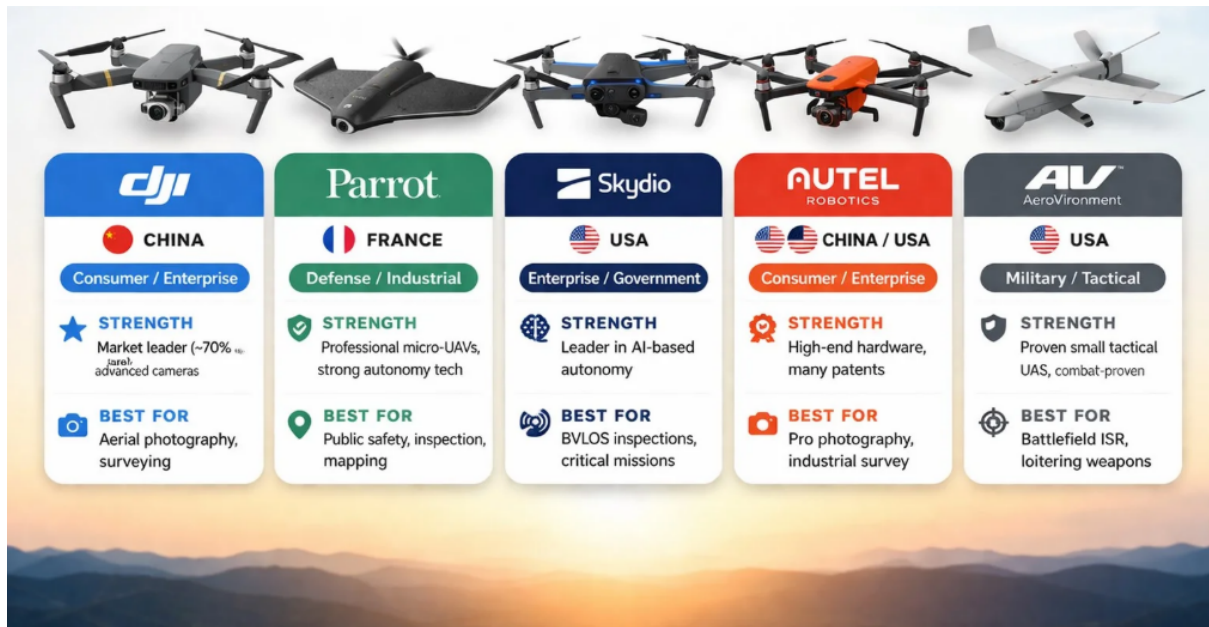


Figure 1.3: Best drone manufacturing companies in 2026 [4].

1.2 Benefits from the Integrated Motor Drive Approach

Traditionally, motor drive systems have their drive units arranged in an external case, and the connection to the motor is made using cables, which can be very long depending on the specific application. This approach has recently been complemented by the Integrated Motor Drives (IMDs) solution, in which the entire drive unit, including the power stage, control electronics, passive elements, and heatsink, can be directly integrated into the motor. In this way, power density can be significantly increased, bringing relevant benefits in certain applications in which this feature plays an important role in the design of the drive system; obviously, robotic applications are among them. In fact, one of the most evident advantages of integrating the drive system into the motor is to eliminate separate enclosures and cables. However, the latter aspect also solves an important issue related to long connection cables, which is the presence of high voltage transients on the motor terminals caused by the fast switching operations of the power devices. Instead of using filters between motor and drive unit (which are costly and bulky), the IMD approach allows for avoiding producing leakage currents through stator winding insulation and therefore the aging of insulations is considerably reduced, together with all the related EMI problems. In addition, the Integrated Motor Drives solution can share the same cooling system between motor and drive units, allowing a further reduction of the overall system size. Other advantages come from the improvements in motor performance, functionality, and efficiency, packaging of power electronics, and minimization of drive system complexity and cost. However, alongside these benefits, the integration of the motor and drive introduces several challenges, starting from managing to fit all the drive components in a very small volume, which requires size optimization and an accurate placement of components. Being able to cool both motor and drive units is quite complicated, and the electronic components are directly subjected to the physical vibration caused by the motor. In fact, unlike electric machines, regarding power electronic components, it is rare to find devices either mechanically or thermally robust [5].

Integrated Motor Drive applications can be divided into three main categories [6].

- **Surface Mount Integration:** the power converter is mounted on the motor housing with different possible solutions, from the simplest one in which the converter is placed on the case of the motor, to the adoption of a modular approach, splitting the converter into smaller converter units and arranging them around the motor housing. This type of integration is the most interesting in terms of simplicity, low cost of manufacturing, and relative ease of implementation. Moreover, in this way, the housing acts as a thermal barrier providing thermal isolation between the converter and the stator windings, and so the casing must be properly designed to guarantee the full absorption of all of the power electronic heating loss and all of the radially conducted heating loss from the electric machine.
- **End Plate Mount Integration:** compared to the previous solution, the power converter is moved onto the end plate, and the actual position is dependent on available space in the axial direction. Also in this case, the choice of the power stage arrangement provides a stable mechanical platform and thermal isolation from the machine for the power converter. An additional cooling system would be necessary in case of an IMD characterized by a machine operating at high torque and low voltage or at very high speed.

- **Stator Iron Mount Integration:** this configuration is specifically designed to produce a more compact IMD, since the power converter is mounted on the stator back iron. This approach is efficient mostly when the height of the converter components (especially the DC link capacitors) is small, because in this way the converter can fit into the space between the stator back iron and endplate.

As mentioned before, modular integration (Integrated Modular Motor Drive, IMMD) involves segmenting the power electronics into smaller modules for driving specific stator winding sections. They are physically independent and are usually connected together in series or parallel to correctly manage the control of the full motor. Depending on the topology needed, an active voltage/current balancer is usually required to balance and regulate the segment voltages/currents during unbalanced or asymmetrical load conditions. Some benefits derived from this approach are the enhanced fault tolerance, better thermal capabilities, and power rating scalability. In addition, drive modularity is independent of the specific type of drive integration, since the power converter mounting can occur on the motor housing, on the stator iron, or on the end plate. A last aspect to take into account is that the size of electronic components can also be reduced as the ratings for independent modules and their passive component sizes are significantly lower compared to a single power converter. This can also be translated into an improved thermal capability thanks to a more evenly distributed heat dissipation. Some drawbacks can be derived from the more complex control system needed for managing the individual power modules and from the structural and mechanical problems in module integration with the motor [6].

In [5], the importance of the miniaturization of IMMD solutions is pointed out, especially trying to find the optimal DC link capacitor volume, since in motor drive systems, heatsinks and passive components (particularly DC link capacitors) occupy a large portion of the converter volume. Usually, these capacitors are the tallest components on the PCB, even if they are used ceramic capacitors instead of electrolytic ones (which are even bulkier), and they often determine the overall height of an IMD. The maximum volume of an IMMD can be approximated by taking the cross-sectional area of the PCB and multiplying it by the maximum height; in this way, its overall volume is directly proportional to the capacitor height, as well as the capacitor volume. Furthermore, if the chosen capacitors have too large sizes and heights, it can cause physical vibration when the motor is running. It is for these reasons that researchers are focusing on proposing new power converter architectures or topologies to utilize wide-band-gap devices and to minimize capacitor sizes.

For instance, in [7] an IMMD structure is proposed in which three half-bridge single-phase power pieces are combined into a three-phase converter module to drive a motor segment. Then, the inverter modules are connected in series to withstand the total DC link voltage required by the motor drive system (see Figure 1.4). In this way, it is possible to take advantage of the low-voltage wide-band-gap GaN device properties, which include the possibility to reduce the DC link capacitors' size by reaching higher switching frequencies. Moreover, as highlighted before, the IMMD approach needs a power electronics designed to survive in a harsh thermal and vibrational environment generated by the motor drive system. Therefore, semiconductor devices must have a superior and higher maximum junction temperature than conventional silicon power devices, and Wide Band Gap devices such as GaN or SiC are the most suitable to meet these stringent requirements. Though the maximum voltages of most commercial GaN devices are less than 200 V, which is too low for many motor drive applications, even if GaN devices can

achieve a maximum voltage of 650 V with a competitive price, this voltage level is still lower than that of IGBTs used in mostly industrial motor drive systems [7].

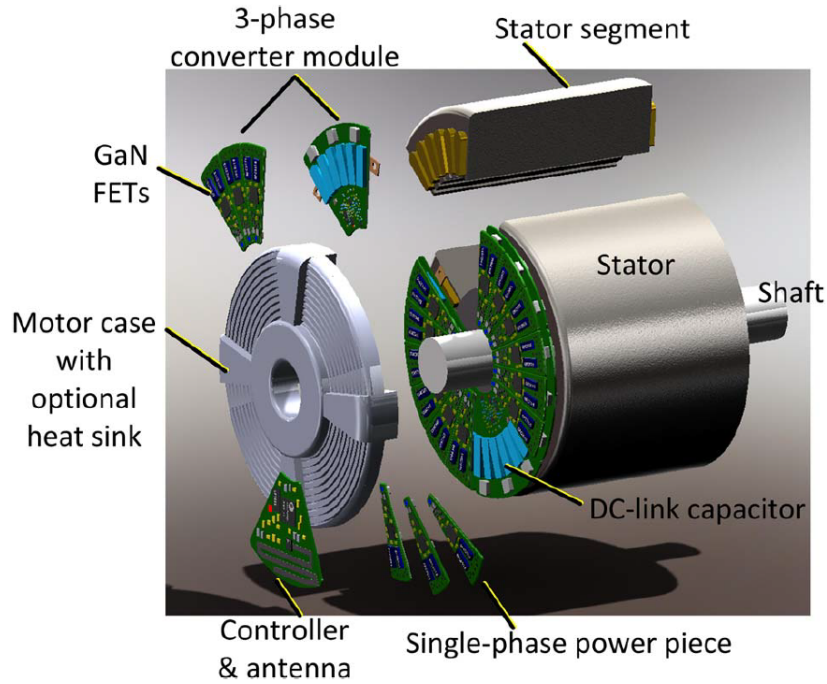


Figure 1.4: Three-dimensional illustration of the GaN-based IMMD structure proposed in [7].

1.3 Wide Band Gap Materials in Power Electronics

Up to some decades ago, power converters were designed using only Silicon-based diodes and transistors, and they have been constantly improved in terms of current and blocking voltage capabilities, heat dissipation, and operating switching frequency. In 1978, the silicon power MOSFET was launched to replace slower and aging bipolar devices in power supply for the first desktop computer applications, and then it rapidly became the power conversion device of choice for the whole semiconductor industry. However, after several years of research and development, nowadays the properties of this semiconductor material cannot be enhanced anymore (unless increasing the manufacturing cost too much), since the theoretical limit has already been reached. Therefore, in the last 20 years, the industry moved towards the introduction of new base materials in order to obtain high-performance power conversion transistors and integrated circuits [8]. These are known as Wide Band Gap (WBG) semiconductor materials, and the most promising ones, in terms of electrical and thermal characteristics, are identified in Silicon Carbide (SiC) and Gallium Nitride (GaN).

On one side, Silicon Carbide (SiC) MOSFETs technology is mature enough to replace Silicon IGBTs and diodes in some power applications, since they allow higher efficiency levels but still offer standard gate terminal requirements, as by now it is possible to drive SiC MOSFETs with the standards +15V/-5V gate voltage levels imposed by IGBT devices. This last feature makes the adoption of SiC devices relatively straightforward, and so the performance and the power

density of the converter can be increased. Indeed, during recent years, the development of both SiC power MOSFETs and SiC power Schottky diodes has obtained important improvements, and therefore, in Medium Voltage SiC devices, can be realized with superior conduction and switching properties than their Silicon-based corresponding power devices.

The second WBG semiconductor material, Gallium Nitride, is achieving an increasingly crucial role in the power electronics scenario, especially for low-voltage applications such as data center servers, consumer electronics appliances, lidar, and robotic motor drives. It is rather surprising to think that only in 2009, Efficient Power Conversion (EPC) developed the first enhancement-mode GaN FET, and then the evolution of GaN devices has continued without slowing down. While the first GaN device appeared five years before, around 2004, as depletion-mode radio frequency (RF) transistors made in Japan by the Eudyna Corporation [9]. Therefore, initially this base material has not been considered suitable for power electronics, but the first power GaN devices immediately showed that the promising conduction and switching characteristics supposed by physics theory could actually be achieved in real devices. However, current GaN power devices are still some steps behind in terms of development and standardization compared to SiC devices, even if commercially available GaN transistors with low on-resistances and fast switching capabilities have already demonstrated their superior characteristics compared to their Si or SiC transistor counterparts, but only in the range from 15V to 650V (because their lateral structure limits the maximum blocking voltage). In fact, the lack of a standard and commonly shared GaN transistor structure, as well as different gate voltage and current requirements (as will be further clarified in Chapter 3), makes the adoption of GaN components in the industry still complicated. This makes their integration into new power applications more challenging for engineers, but the continuous advancement in GaN technology development will certainly bring innovative solutions to overcome these problems [10].

SiC and GaN semiconductors are known as Wide Band Gap materials because they have the inherent feature of a wider forbidden energy bandgap, allowing a more stable electrical behavior, since they are able to maintain their electrical properties unchanged under large external energy stimulus. As the energy bandgap of a material quantifies the amount of energy required by an electron to pass from the valence band to the conduction band, a higher energy bandgap (E_g) means that the material is able to withstand higher electric field maximum values, which in turn is defined by the E_{max} value. As shown in Table 1.1, both SiC and GaN semiconductors are endowed with an energy bandgap value three times higher than that of silicon, while the maximum electric field is 100 times higher for SiC materials and even 150 times higher for GaN. These properties allow the reduction of the device width and of the leakage current, since fewer charge carriers are generated in the depletion region during the blocking state. Therefore, both on-resistance and switching times are reduced, achieving better efficiency and power density in WBG-based power converters.

At the same time, from Table 1.1, it can be observed how GaN and SiC materials have different behaviors in terms of electron mobility μ_n , saturation velocity v_{sat} , relative permittivity ϵ_r , and thermal conductivity λ , making each of them more suitable for different types of applications. The leading GaN peculiarity is its HEMT (High Electron Mobility Transistor) property, which means that the mobility through the transistor channel is very high. In fact, its electron mobility is typically in the range of 1500-2000 cm²/V·s, almost 2 times higher than SiC MOSFETs, which implies a considerable advantage regarding low ON resistance values, and so devices with an even smaller area can be obtained. Moreover, GaN has a higher saturation velocity and lower relative permittivity, which makes the switching transients very short, thus allowing

higher switching frequencies than those achievable with Si and SiC devices. Regarding the thermal conductivity, though, SiC has a value almost 5 times higher than GaN and Si, so the heat transfer from the semiconductor device junction to the case is facilitated, and this enables higher current and power densities for SiC devices.

Figure 1.5 is useful to understand the distance between Si and WBG materials in terms of the achievable theoretical drift region on-resistance of an n-type MOSFET as a function of breakdown voltages. With a minimum drift region resistance about 5.7 times lower than SiC and about 2781 times lower than Si, it can be reaffirmed that GaN material can significantly reduce the conduction losses of the power switching devices with equal breakdown voltage level [10]. This comparison has been made considering 4H-SiC technology, which is used by manufacturers for its isotropic structure [11].

For summarizing and comparing all the key material properties of Si, SiC, and GaN, Figure 1.5a can be used, which contains an explanatory radar chart.

Figure 1.5b graphically explains which applications are typically covered by each of the three power semiconductor materials. While SiC devices can actually offer higher power density operating voltages, GaN devices provide a lower conduction loss and a higher switching frequency [9].

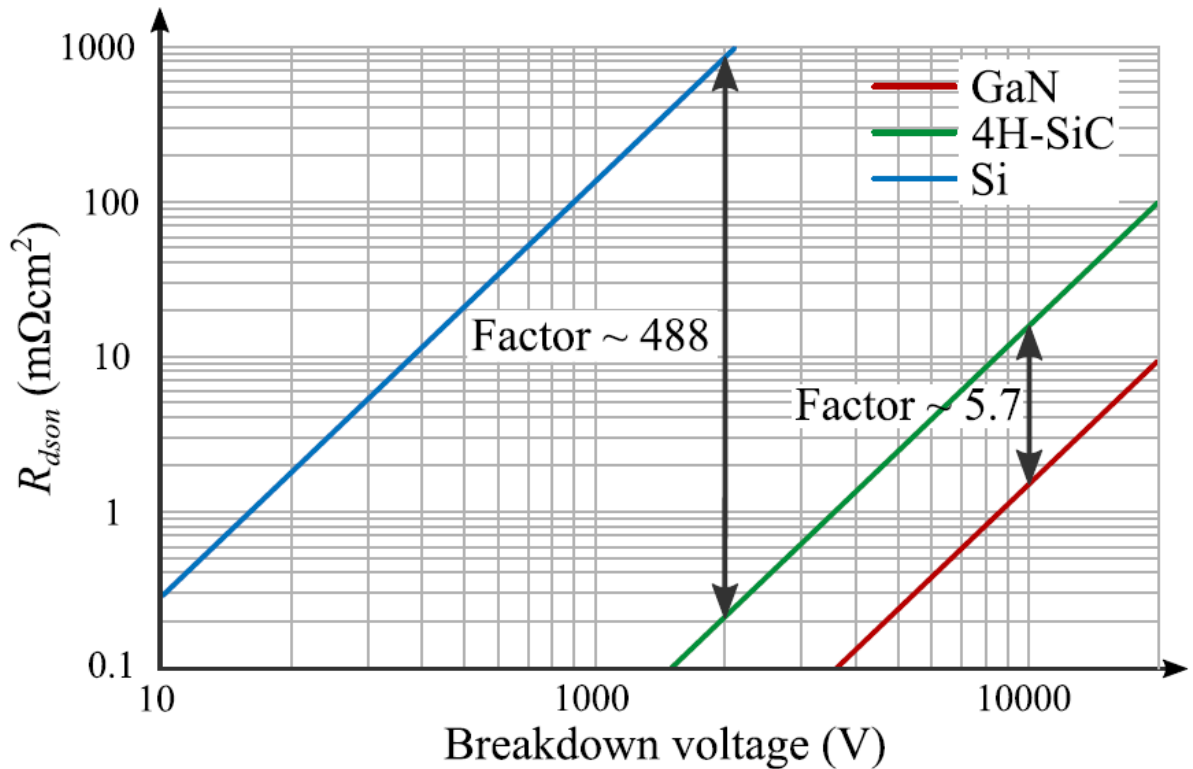


Figure 1.5: Comparison of theoretical on-resistance in one dimension for unipolar Si, SiC, and GaN devices [10].

Table 1.1: Properties of Si, SiC and GaN semiconductors [10].

Parameter	U.o.M.	Si	SiC	GaN
E_g	[eV]	1.12	3.26	3.39
E_{max}	[MV/cm]	0.23	2.2	3.3
μ_n	[cm ² /V·s]	1400	950	1500 – 2000
v_{sat}	[10 ⁷ cm/s]	1	2	2.5
ϵ_r		11.8	9.7	9
λ	[W/cm·K]	1.5	4.9	1.3

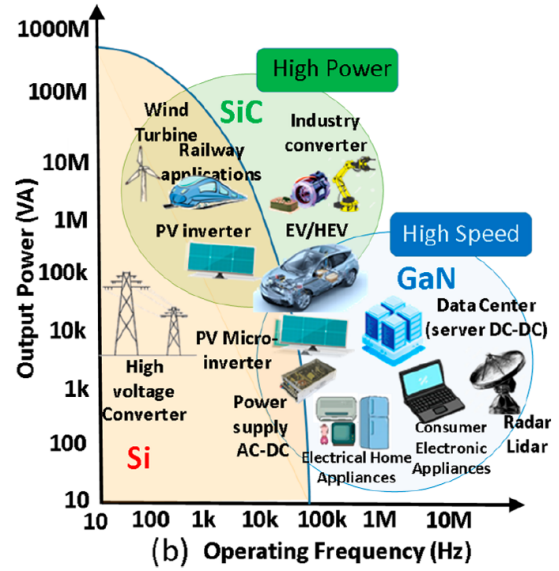
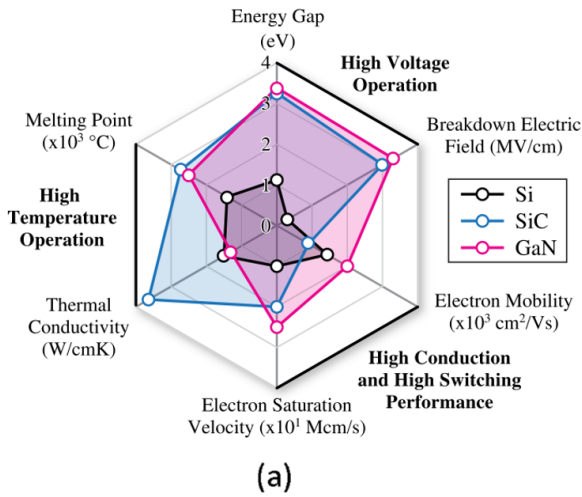


Figure 1.6: (a) Comparison of the main material properties of Si, 4H-SiC and GaN devices at ambient temperature (25°C) [12]. (b) Si, SiC, and GaN power electronics switch applications areas [9].

Chapter 2

Advanced Robotic Applications

2.1 Humanoid Robots

Considering the latest developments in robotic applications, humanoid robots are extremely complex systems that need the integration of many different technologies to operate autonomously and interact properly with the surrounding environment. These technologies belong to multiple fields, such as locomotion control, autonomous navigation, environmental perception, and intelligent manipulation, all of which are related to human capabilities. Without undertaking an in-depth analysis of these vast domains, the focus of this section is to show the main components of a typical humanoid robot body, from the hardware to the software architectures, highlighting the role of power converters in the power system implementation. In addition, Section 2.3 will provide a short investigation into the advantages of using WBG-based converters in robotic applications, especially regarding humanoid robots.

2.1.1 Hardware Architecture

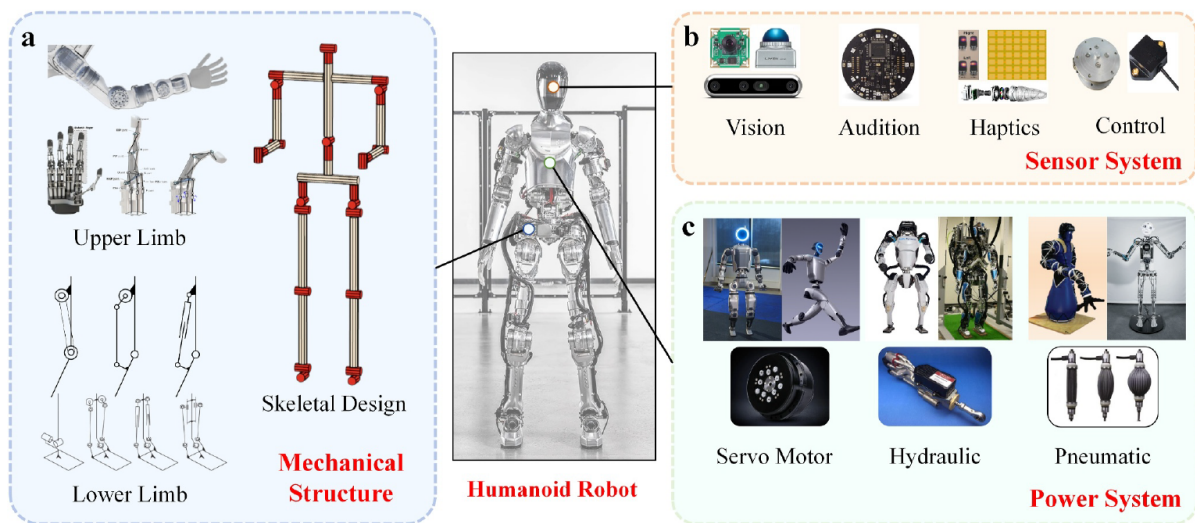


Figure 2.1: Hardware architecture of a humanoid robot. (a) Mechanical structure design (b) Sensor system (c) Power system [2].

Mechanical Structure

As shown in Figure 2.1, the most elementary system that comprises a humanoid robot is the mechanical structure, which must be accurately designed to achieve the required robot's efficiency and versatility in replicating human-like movements. To evaluate the performance provided by a specific mechanical structure, the metric named degrees of freedom (DOF) is used: the higher the DOF, the higher the possible movements performed by the robot. Since a direct replication of the human anatomy is rather difficult to reach yet (due to the current materials and actuators limits), robot manufacturers tend to concurrently limit the number of actuators for reducing weight as much as possible and concentrating mass around the trunk to reduce the limbs inertia. For instance, joints, which play a pivotal role in guaranteeing the robot's mobility, are usually driven by motors through cascaded reduction gears or harmonic drives to increase torque while limiting the motor's size. This is the common approach used for industrial applications (such as those in which robots are used, such as handling, painting, assembling, or welding [13]). The needed drive energy for achieving the required dynamical response is provided by the robot powertrain, which is composed of three subsystems at each actuated joint: servomotor (driver and motor), reducer, and load (see Figure 2.2). In the case of a humanoid robot, although these mechanisms allow for spatial separation between the actuator and the joint, they also introduce non-linearities that make precise control more challenging [2].

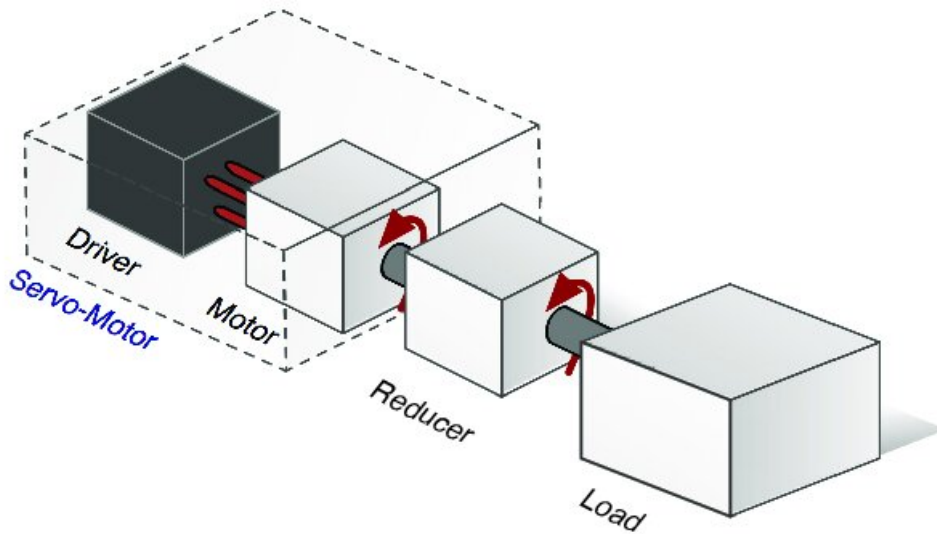


Figure 2.2: Scheme of a powertrain on an actuated joint for robotic applications [13].

Similar to a human body, the mechanical structure of a humanoid robot body is sustained by the torso, to which are attached the upper and lower limbs and the head.

The upper limb is composed of the arm and the gripper, which can also be substituted with a multi-fingered dexterous hand. The arm contains at least three joints for emulating the movements of the shoulder, elbow, and wrist, with different degrees of freedom, depending on its actual implementation, which can reach up to 7-DOFs in recent robots like Unitree G1 and OpenAI Figure 02. For the dexterous hand, each finger is driven by a four-bar linkage mechanism with the actuators integrated within the palm, allowing the MCP (Metacarpophalangeal), PIP (Proximal Interphalangeal), and DIP (Distal Interphalangeal) joints to simulate human-like finger movements in the most accurate way.

Moving to the lower limb, this structure is typically characterized by six degrees of freedom and includes the leg with the hip and knee joint, and the foot with the ankle joint. Obviously, the hip joint is the most stressed in terms of required power and mechanical load; it has to be specifically designed to bear high bending moments (especially when the leg swings down for landing) and to be able to provide very high torque values. The knee joint has only 1-DOF, and its actuators are usually located near the hip joint (for mass optimization) and driven with belts, cranks, or linkages. The ankle joint, instead, usually has 2-DOFs, obtained by using two parallel actuators to drive a spherical joint, which also allows for limiting the foot's inertia, so its movements can be more stable and agile.

Finally, regarding humanoid robot heads, it is possible to distinguish two different implementations, based on the specific application scenario. The first design approach is focused on avoiding the uncanny valley effect, which is obtained by minimizing as many human-like features as possible integrated in the head. Using a non-anthropomorphic head makes it easier to recognize the humanoid as a robot and, therefore, in applications such as industrial manufacturing, commercial services, family companionship, healthcare, and education, people can be less affected by discomfort or fear. On the other side, if the humanoid robot will be used to perform tasks in which the interaction with real people is fundamental, such as shows, customer service, guides, receptions, and commercial promotions, the level of anthropomorphism in humanoid robot heads is extremely increased. In this way, the uncanny valley is avoided by making them as human-like as possible, adding several realistic details such as eyebrows, eyes, nose, mouth, hair, and so on.

Sensor System

Since a humanoid robot must perceive its surroundings, detect objects, and respond to external stimuli, sensor integration has paramount importance. They can be divided into four main categories [2]:

- **Vision:** most of the current advanced humanoid robots use light detection and ranging (LIDAR), RGB(-D) cameras, or a combination of them to implement the sense of sight. LIDAR technology is able to provide highly accurate visual information of the surrounding environment (in fact, it is also largely used in autonomous vehicles), usually achieving a precision of a few centimeters. This feature, though, generates a huge amount of data, which has to be rapidly processed. Unlike RGB cameras, LIDAR operations are inherently independent from ambient light conditions, allowing a reliable behavior also in complex environments. RGB-D cameras are commonly used in humanoid robots because they provide both visual and real-time depth information, although the accuracy and measurement range are limited compared to LIDAR.
- **Haptics:** tactile sensors can be implemented in two different ways. The first to be developed consisted of the adoption of arrayed sensors, which at the beginning could have been based on piezoelectric, capacitive, or resistive phenomena, but recently, also more integrable and flexible arrayed sensors are available, with the use of micro-electro-mechanical systems and flexible electronics. On the other hand, Vision-based tactile sensors (VBTs) have lately emerged as a very promising high spatial resolution and multimodal haptic sensor. Its operation basically relies on the usage of a camera to catch the deformation of the gel and compute the haptic information through a computer vision approach. However, the actual problem with this technology is the need for a large size that makes its integration with a dexterous hand really difficult.

- **Audition:** in order to equip humanoid robots with the sense of hearing, at least one microphone is needed. Nowadays, the number of microphones used in a humanoid robot can reach the value of six, allowing the improvement in localization and recognition accuracy even in noisy environments, evidently with a higher computational cost.
- **Control:** the efficacy of the closed-loop control needs specific sensors to monitor variables regarding the dynamics and kinematics of each robot's component. Strain gauges are used to implement force and torque sensors, which can be single or multi-axis, depending on whether they are placed in single or multiple DOFs joints. While Inertial Measurement Units (IMU) are used to accurately sense robots' motion and actual dynamic behavior in three-dimensional space, integrating multiple inertial sensors such as accelerometers, gyroscopes, and magnetometers.

Actuator System

The third fundamental part of the hardware architecture of a humanoid robot is the actuator system, which is concurrently required for achieving precise movement and efficient operation, and providing proper driving force to support complex dynamic movements. Therefore, the first feature that must be guaranteed by a robot's power system is the adaptability to meet varied task requirements and operational settings. Up to now, drive methods for humanoid robot joints can be distinguished into three main categories, and their main advantage, disadvantages, and typical applications are summarized in Table 2.1.

Table 2.1: Comparison of the actual drive methods used in humanoid robots' power system.

Actuator Method	Advantages	Disadvantages	Typical Applications
Servo Motors	fast response speed, high positional accuracy, excellent control performance	additional cooling mechanisms, high energy consumption, more expensive	highly integrated drive systems for smaller joints and hand components
Hydraulic Systems	higher output forces, precise force control, resistant to high-load operations and extreme environmental conditions	more complexity, low conversion efficiency, noisy, require regular maintenance	high-load-bearing components such as the lower limbs
Pneumatic Systems	excellent flexibility control, quick response characteristics, low maintenance and simple structure	lower output power, highly sensitive to environmental factors, limited positional accuracy	lightweight and flexible-control components such as fingers and arms

Because the topic of this dissertation is oriented to electrical drives rather than hydraulic or pneumatic drives, the focus is moved to the electric joint motor types. Usually, it is preferred to operate AC servomotors (especially synchronous motors) instead of DC motors to drive high dynamic loads (as required by humanoid robot joints), due to a higher torque-to-inertia ratio, higher peak torque capability, higher torque-speed bandwidth, simple design, and less maintenance. They are driven using the Field Oriented Control technique (FOC), which allows for maximizing torque efficiency and presents robustness to model parameter variations [14]. However, permanent magnet DC motors have been widely utilized in robotics for the low initial cost and simple control, especially a few decades ago, when the Permanent Magnet Synchronous Motor (PMSM) technology was not as developed as it is nowadays. In fact, the main drawbacks that make DC motors suitable only for very low-power applications in humanoid robots (such as for driving hand digits) are the low lifespan, high maintenance cost, and the well-known problems caused by the mechanical commutation of the armature current. An intermediate solution is represented by Brushless DC motors, which are driven similarly to a brushed DC motor, but the control algorithm needs hall-effect position sensors (six-step commutation strategy). BLDC motors do not have a brush assembly for mechanical commutation (it is performed through power electronics), therefore they are characterized by higher efficiency, higher reliability, and longer lifespan than DC motors, but they typically have lower power density and higher torque ripple, which substantially affect the smoothness of movements [13].

Moreover, different electric driveline solutions for robotic joints can be used, and so not only servo motors equipped with a gear system. For instance, in direct drive motors, either linear or rotary, the motor is tied directly to the load, and the reduction gear is omitted. This drive method gives improvements in terms of dynamic performance, torque noise, and it is capable of producing high torque at low speeds, but at the same time, it requires a larger dimension of the electric machine due to the scaling law of torque and size. If servo motors can drive an object with high precision thanks to their effective closed-loop positional feedback, stepper motors usually run in open-loop and can have a good response in position control even without any costly sensors. They allow quicker operations, smaller sizes, and lower costs, but they are inferior to servo motors when a high torque at high speed is required [13].

2.1.2 Software Architecture

Operating System

Since humanoid robots constantly need to respond to high-frequency sensory input, process events in real time, and coordinate synchronized motion across multiple joints, a Real Time Operating Systems (RTOS) like QNX and VxWorks is used to implement the operating system. On the other hand, during the preliminary testing phase, when reliability and precision are not so crucial yet, Xenomai and PREEMPT_RT can be chosen as they are open-source, affordable, and more accessible RTOS. These Real Time Operating Systems rely on the Robot Operating System (ROS), an open-source framework used for collecting tools, libraries, and conventions to facilitate the development of complex robotic systems. It offers a middleware layer that includes tools for hardware abstraction, device drivers, message-passing between nodes, and algorithm libraries for tasks like perception, motion planning, and control [2].

Communication Scheme

Obviously, the entire robotic system requires an efficient, reliable, multi-node, and sufficiently fast communication protocol to satisfy its highly demanding real-time capabilities. This requirement is usually managed using EtherCAT, which is a high-performance industrial Ethernet protocol and consists of real-time data transmission between the controller (master) and multiple servo drives and sensors (slaves). EtherCAT works within a low-latency scheme with a refresh rate down to microseconds, since the master continuously sends data frames through the network while each slave extracts only relevant data and responds with its feedback. Another useful feature supported by EtherCAT is the Distributed Clocks, which allows for efficient synchronization and coordinates robots' movements while also offering strong scalability to considerably increase the number of connected devices [2].

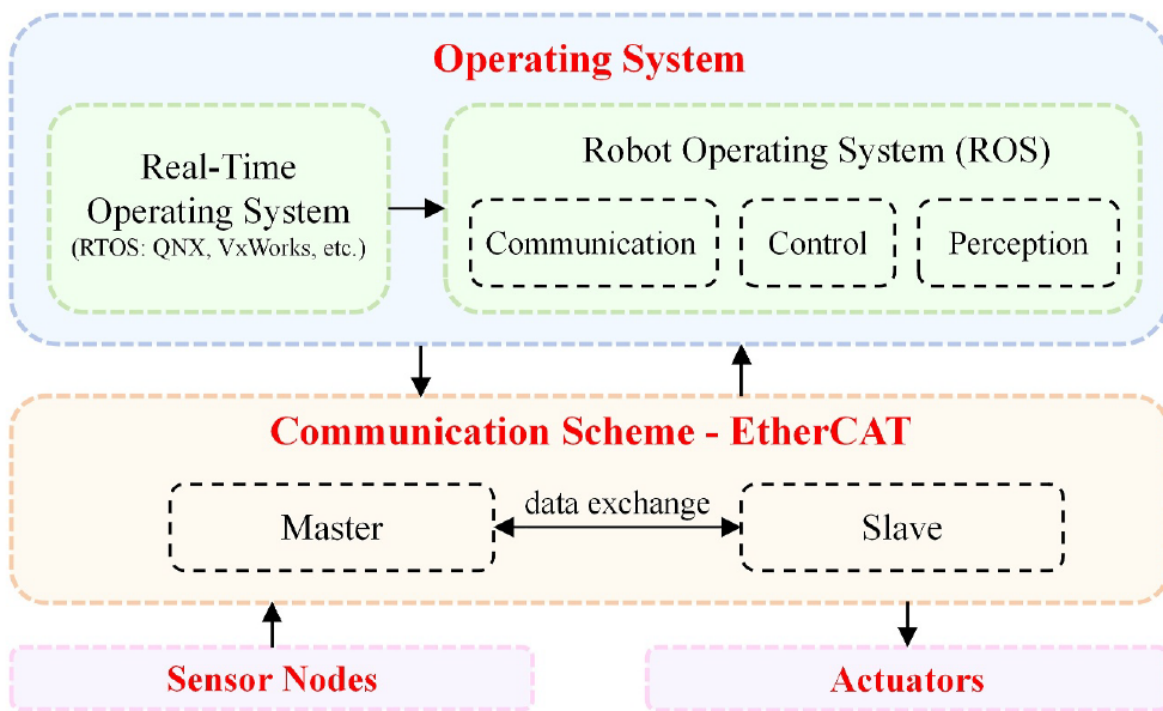


Figure 2.3: Block diagram for the software architecture of a humanoid robot [2].

2.2 Drones

From a historical point of view, UAVs were already defined as aircraft without any onboard crew during the beginning of the 20th century, when the primary applications clearly were focused on military purposes. Only starting from the late 1960s and 1970s, drones were able to deeply infiltrate enemy territory and gather intelligence without involving any human intervention, since they were specifically designed and developed for carrying war-specific equipment, gathering enemy information, and performing reconnaissance operations. These UAVs were capable of long-range missions, even though the power converter technology was still undeveloped and the equipment was heavy, because the propulsion system was realized using jet propulsion technology, instead of electric motors. Nowadays, many air vehicles which can be piloted remotely are

miniaturized thanks to the latest developments in power electronics and electric motors, making these systems more compact, sophisticated, but also economically sustainable for the general public [3].

2.2.1 Classification

Propulsion System

Modern drones can have different propulsion systems, depending on the application requirements in terms of endurance, speed, range, and operational costs.

Battery-powered drones use lithium-polymer (Li-Po) or lithium-ion (Li-Ion) battery technologies. They dominate consumer and commercial sectors due to their high energy density and lightweight, even though they have limited flight time capabilities, thus limiting their applications in long-range operations. Obviously, batteries provide the energy required by the electric motor for generating the needed thrust on the propellers. High-performance drones usually feature BLDC or PMSM motors for better efficiency and higher power density, instead of using DC brushed motors.

Gas turbine systems are used in military-grade or industrial drones. Relying on combustion turbines, they are suited for extended missions or high-speed travel, offering greater cargo capacity and range. However, they result in costly, noisy, and environmentally impactful.

Finally, new technologies are also being developed, such as hydrogen fuel cells, which enable longer range in a sustainable way, and solar-powered drones, which are really beneficial for low-speed, continuous coverage missions like environmental monitoring or communication relays [15].

Flight Mechanics

In general, the UAVs can be distinguished according to the specific flight mechanism [3]:

- **Fixed Wings** (Figure 2.4a): the rigid body structure of this type of drone generates aerodynamic lift under the fixed wing. When subjected to forward airspeed, the wings' tilt control creates a lift to give the required direction to the UAV.
- **Rotary Wings** (Figure 2.4b): compared to conventional fixed-wing UAVs, rotary-wing drones are heavier, but they offer rapid maneuverability thanks to the rotating propellers that generate an upward aerodynamic lift, making them suitable for short-range operations.
- **Fixed Wing Hybrid VTOL** (Figure 2.4c): as the name suggests, these UAVs combine the advantages of both fixed-wing and rotary-wing designs for enhancing the endurance. They can lift vertically thanks to the Vertical Take-Off and Landing (VTOL) propulsion offered by the rotating propellers, while the fixed-wing propulsion is used when no changes in altitude are required.
- **AirShip** (Figure 2.4d): better known as a dirigible balloon or blimp, it relies on filling its envelope with lifting gas (lighter than the surrounding air) in order to make the entire structure sustained by the force generated according to Archimedes' principle.
- **Flapping Wing** (Figure 2.4e): it mimics the biological flapping mechanism of birds and insects, in fact it is also named ornithopter. The aerodynamic lift is generated by pushing the air below its wings synchronously.



(a) Fixed Wings



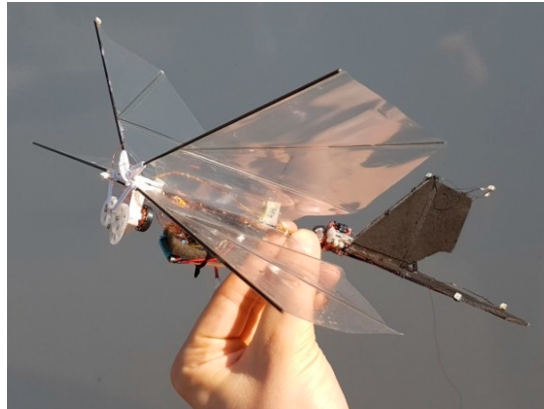
(b) Rotary Wings



(c) Fixed Wing Hybrid VTOL



(d) AirShip



(e) Flapping Wing

Figure 2.4: Categories of UAVs.

2.2.2 Internal Structure

In Figure 2.5, the typical internal structure of a rotary-wing UAV is shown. In particular, the illustrated scheme refers to a quadcopter, which is a category of multi-rotor UAV with four rotors and the related propellers that generate the required thrust. This typology of drones is easy to maneuver in tight spaces, they ensure the ability to lift and land vertically with high precision, and are commonly used for short-range autonomous operations. The best choice for their propulsion system is to have a LiPo battery supplying four brushless motors through the dedicated ESCs.

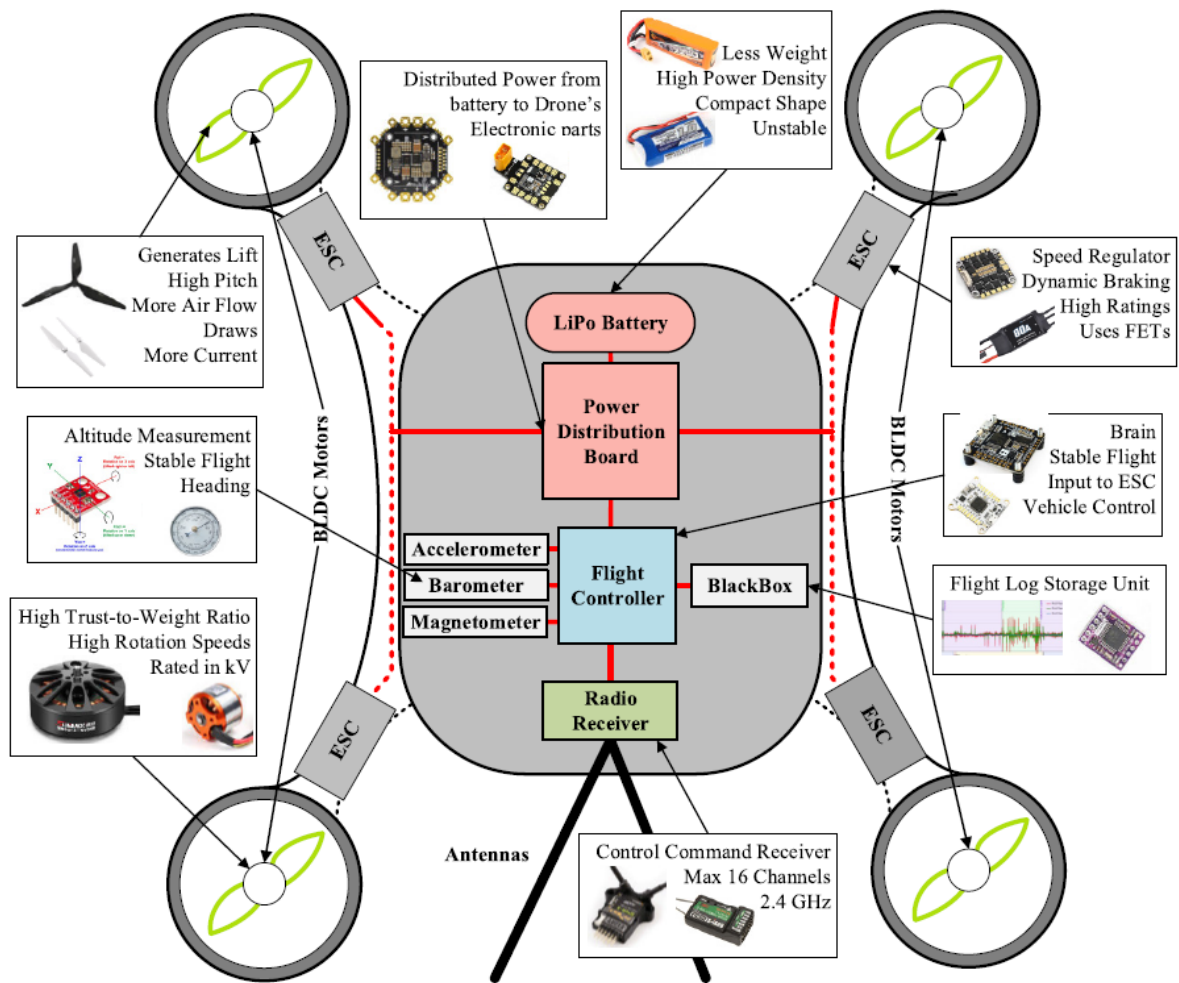


Figure 2.5: Internal hardware structure of a quadcopter [3].

Frame

The frame represents the drone's backbone, since it is the load-bearing structure that will support the aerodynamic stress and the weight of all components. It is typically made of aircraft-grade aluminum, carbon fiber, or ABS, and more rarely fiberglass.

Motors

Regarding the electric motors used in a rotary-wing drone, brushless motors are the most chosen for their improved power and torque density. In addition, since driving a UAV is a robotic application that requires high torques and accelerations from actuators within small packages, these motors have an exterior rotor rather than the more conventional interior one (see Figure 2.6). As analyzed in [16], exterior-rotor motors use PMSM technology to achieve high-torque actuators in a small, lightweight package, which also implies a reduced inertia. In contrast to interior-rotor motors, they are easy to wind by hand thanks to the larger wire diameter and fewer turns per tooth required to achieve high torque. In this way, exterior-rotor motors are typically less expensive than their interior-rotor counterparts.

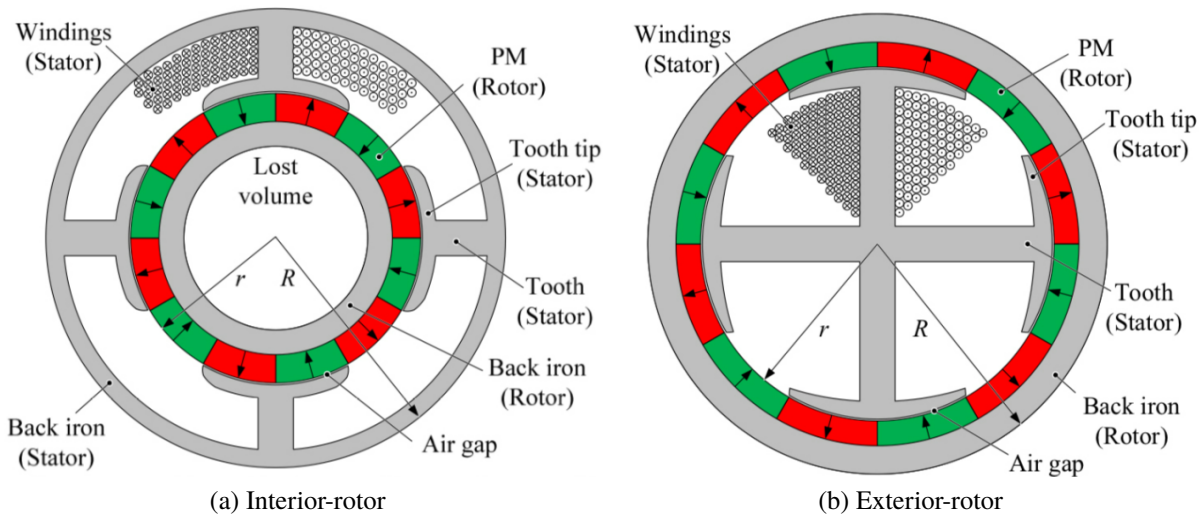


Figure 2.6: Interior vs. Exterior rotors in robotic brushless motors.

Propellers

Propellers can be manufactured in wood, carbon, ABS, and other materials. There are two different types of configurations, depending on the direction in which the propeller rotates when the drone is in flight.

- Right-handed, which rotates clockwise.
- Left-handed, which rotates counterclockwise

This difference is due to the inherent asymmetry in a propeller-driven aircraft. In general, the torque applied to the shaft induces, according to the principle of action and reaction, a torque

with an opposite sign that tends to cause the aircraft to roll. Generally, these imbalances are compensated for by the pilot who properly maneuvers the control surfaces of the wing and tailplane. In a multicopter, instead, asymmetries are compensated for by the aircraft design itself. In fact, as can be seen in Figure 2.7, each electric motor is installed so that adjacent ones have opposite directions of rotation, thus generating equal and opposite reaction torques.

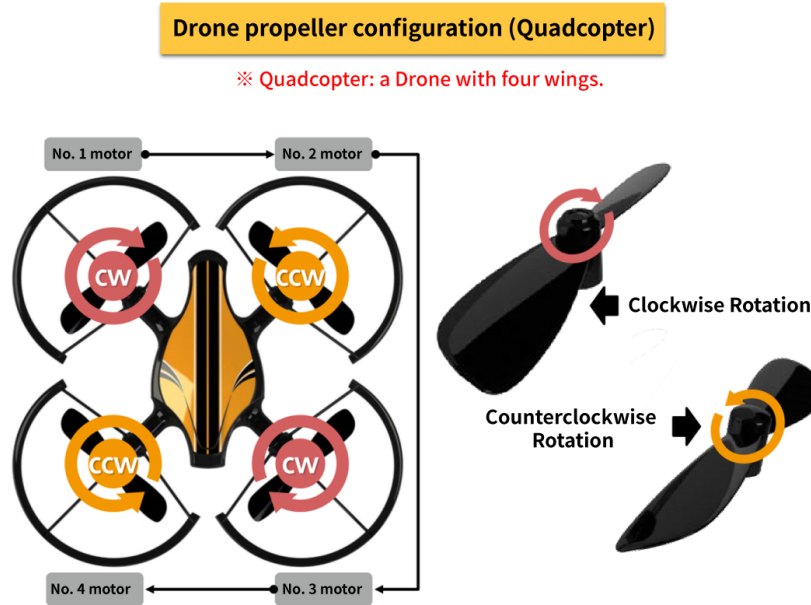


Figure 2.7: Drone propeller configuration in a quadcopter.

Flight Controller

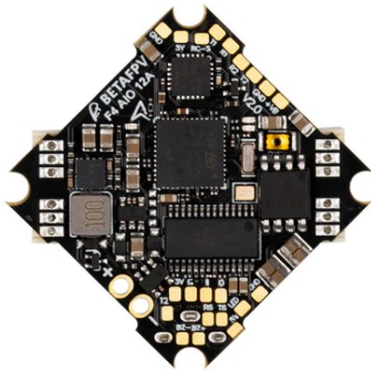
The Flight Control Computer (FCC) is an electronic board featuring a programmable micro-processor that handles digital and analog signals from various sensors and pilot commands, in order to provide the proper outputs for stabilizing and controlling the drone. This demanding control is based on computing the error between the pilot's command and the actual value of the commanded variables and generating the required thrust value for each motor (without exceeding the flight envelope protections implemented in the same firmware) to minimize the error. The control command, before being sent to motor ESCs, is translated into a digital signal whose frequency varies depending on the speed target, implementing a PWM logic. The flight can be performed in different modes (Automatic, Semi-Automatic, and Manual), from the complete control entrusted to the drone pilot (Manual) to storing flights with programmed commands (Automatic).

Electronic Speed Controller

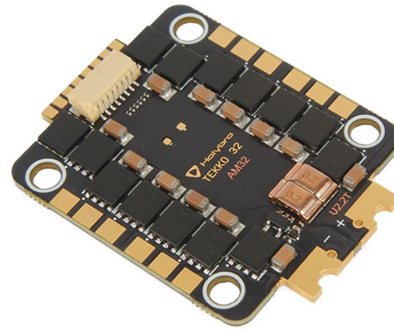
The Electronic Speed Controller (ESC) is responsible for controlling the speed of motors in an FPV drone by driving the brushless motor at the target speed, which depends on the throttle signals received from the flight controller. ESCs are crucial for maximizing drone performance as they handle the input DC voltage supplied by the LiPo battery to inject the proper currents into the three-phase motor winding.

After a brief research on the various commercial ESCs, three main typologies can be recognized:

- AIO (All-in-One) ESCs (Figure 2.8a): integrate both the FCU and the ESC on the same board. They have low current and voltage ratings compared to the other types of ESC, but can simultaneously drive four motors without the need for an external flight controller.
- 4-in-1 ESCs (Figure 2.8b): implement only the ESC part, with four outputs managed concurrently and intermediate current and voltage ratings.
- Single-output ESCs (Figure 2.8c): suited for high current (up to 400 A peak of DC input current from the battery) and voltage ratings (up to 60V with a 14S battery), since only one motor is driven, and so the power stage can be designed for better managing the heat dissipation.



(a) F4 AIO FC 12A V2 (BETA FPV)



(b) Tekko32 F4 4in1 50A ESC (Holybro)



(c) FLAME 180A 12S V2.0 ESC (T-Motor)

Figure 2.8: Commercial ESCs examples.

Inertial Measurement Unit

The IMU (Inertial Measurement Unit) is an electronic device that allows the FCC to detect the UAV's attitude. Generally, it contains three sensors:

- Accelerometer: detects linear acceleration along the three axes.
- Gyroscope: measures angular velocities around the three axes.
- Magnetometer: measures the Earth's magnetic field along the three axes to determine the drone's orientation relative to magnetic north. It helps to improve the precision in determining the drone's orientation and heading, providing crucial data for navigation and stabilization during flight.

GPS

GPS is a satellite navigation system that calculates the precise position of the UAS and allows it to hover even in windy conditions without the pilot's intervention.

Power Management Unit

The PMU (Power Management Unit) is one or more power converters needed to properly distribute the energy coming from the battery to all the on-board electronics (FCC, ESCs, IMU, Radio Receiver, BlackBox, FPV Camera).

Radio Receiver

The receiver is the device connected to the radio control unit that allows the UAV to be commanded and controlled. It usually uses the 2.4 GHz, 5.8, or 5.2 GHz frequency band.

LiPo Battery

The battery represents the powerhouse of the drone. Lithium Ion Polymer (LiPo) batteries are the most used because they have a higher discharge rate compared to NiMH and Lead-acid batteries, they ensure higher power density, and offer the flexibility to be packed into the required shape and size. However, special care has to be given during charging, discharging, and storage, as they are known to fire when mishandled. In fact, these batteries are sensitive to voltage-temperature variations and must operate under defined conditions. LiPo batteries are ideally used between 20-80% of their capacity, assuring that Depth of Discharge (DoD) does not exceed 80% of the battery's capacity for the battery's safe operation. Moreover, their End of Life (EoL) is usually identified as 80% of the battery's Beginning of Life (BoL). Unlike Electric Vehicles (EVs), a drone's depleted battery must be manually detached and swapped with a charged one, limiting the achievable flight range of battery-charged UAVs [3].

BlackBox

A BlackBox is an electronic device for security purposes, which is placed on every aircraft and is generally comprised of two parts: a Flight Data Recorder (FDR) that is responsible for recording data relevant to the aircraft, like its speed, altitude, and heading, and a Cockpit Voice

Recorder (CVR), which captures audio from the cockpit. Obviously, given the unmanned nature of UAVs, there are no cockpit communications that need to be recorded, and thus, the use of a CVR is avoided in drone applications. Therefore, a BlackBox specifically designed for use in UAVs must certainly contain a flight data recorder, which must be stored in a protective enclosure to ensure data safety and recoverability. Indeed, all the components used in this security device are stored in a protective enclosure that can withstand a potential crash and is watertight and fireproof to ensure that the recorded data can be recovered and analyzed after the crash [17].

Payload

The payload transported by a UAV can generally be a camera, a sensor, a container, and so on, which is usually attached to a gimbal. The gimbal is a support that stabilizes the load on the horizontal plane, counteracting turbulence and the motions of the UAV, and allows the payload to be oriented regardless of the drone's operation.

FPV Camera

A FPV camera is used for the experience of controlling the drone from the viewpoint of being inside the drone. In this way, the UAV can be piloted in operations conducted at a distance that does not allow the remote pilot to maintain direct and constant visual contact with the aircraft, i.e., Beyond Visual Line of Sight (BVLOS) operation. The FPV camera is aided by the video transmission-receiver module and powered by the drone's battery.

2.3 Advantages of Using GaN-Based Converters

2.3.1 Power Converters in Robotics

After the previous overview on the actual developments in robotic applications, such as humanoid robots and drones, the pivotal role of power converters in this field appears evident. In fact, these applications require a high level of efficient energy conversion, since power converters serve as the main connection between energy sources and the electrical demands from the various robotic subsystems. Therefore, assuring an efficient power conversion reduces the amount of heat produced by losses, achieving longer operational times and fewer battery replacements, along with a simpler thermal management design of the entire system. On one side, power electronics is used to provide efficient voltage regulation, in order to supply sensors, microcontroller and other electronics components with the appropriate voltages, regardless of the input voltage to the entire system. On the other side, power converters are also the element required by motors and actuators for performing the proper robotic motion and manipulation through correct current management. Finally, a robotic system needs different electrical waveform characteristics for each component; for instance, to correctly drive AC motors, it is crucial to convert DC power to AC, with the specific frequency and amplitude.

Figure 2.9 shows the different types of power converters that can be used in robotic applications, from industrial robots to service robots.

DC-DC converters are almost always used in robotics, since voltage step-up or step-down capabilities are required for many purposes. For example, in battery-powered robots, a DC-DC converter can be employed to maintain a constant voltage even though the battery discharges, or different DC-DC regulators are placed in a robotic system to supply integrated sensors and

actuators which have distinct voltage requirements.

AC–DC converters have the role of supplying a robotic system, taking the required power from an AC source and rectifying it. They are used in charging stations for recharging mobile electric robots, but also for delivering power to industrial robots directly from AC grids.

Probably, inverters (DC–AC converter) are the most demanding power converters in robotics, since their employment relies on converting DC power from batteries to AC power for driving motors and actuators, with the best possible efficiency, precision and responsiveness.

In applications such as high-power robotics arms, the voltages needed to correctly perform the motion control reach high levels, and so multi-level converters are used to guarantee these requirements by generating stepped voltage waveforms. This type of conversion allows for less stress on the components and also improves overall system efficiency, thanks to the minimization of voltage harmonic distortion.

In resonant converters, resonant components Resonant converters utilize resonant components (typically inductors and capacitors) to enhance power conversion efficiency by minimizing switching losses. This is primarily required in charging robotic devices, also in a wireless approach, since they are suited to implement wireless power-transfer applications, avoiding physical connections.

For minimizing switching losses during the power conversion, soft-switching converters employ techniques like Zero Current Switching (ZCS) and Zero Voltage Switching (ZVS). They are usually used for driving high-frequency motor drives and achieving a high level of precision, since this switching behaviour allows for keeping the energy losses and the electromagnetic interference.

For performing an AC–AC conversion without intermediate DC links, matrix converters are the most employed in specific motor drive applications. This approach offers improvements for the efficiency, control strategy, size and total number of components.

Dual Active Bridge (DAB) converters enable the bidirectional AC–DC conversion, which is a fundamental requirement in applications where energy regeneration towards the grid is pivotal, such as grid-powered robots [18].

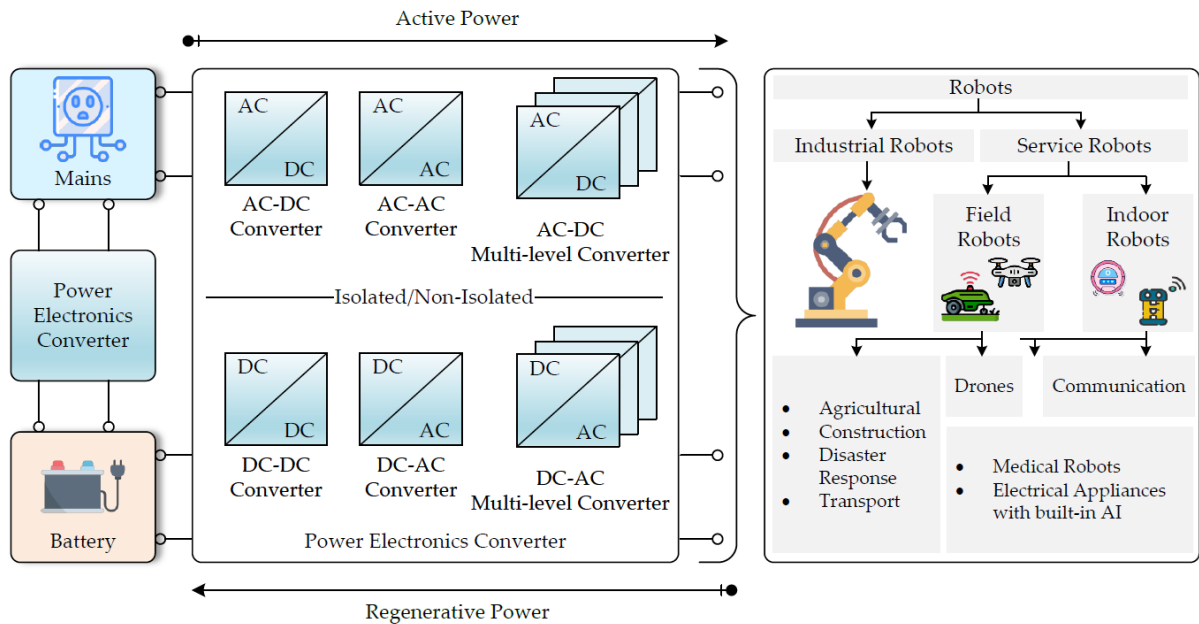
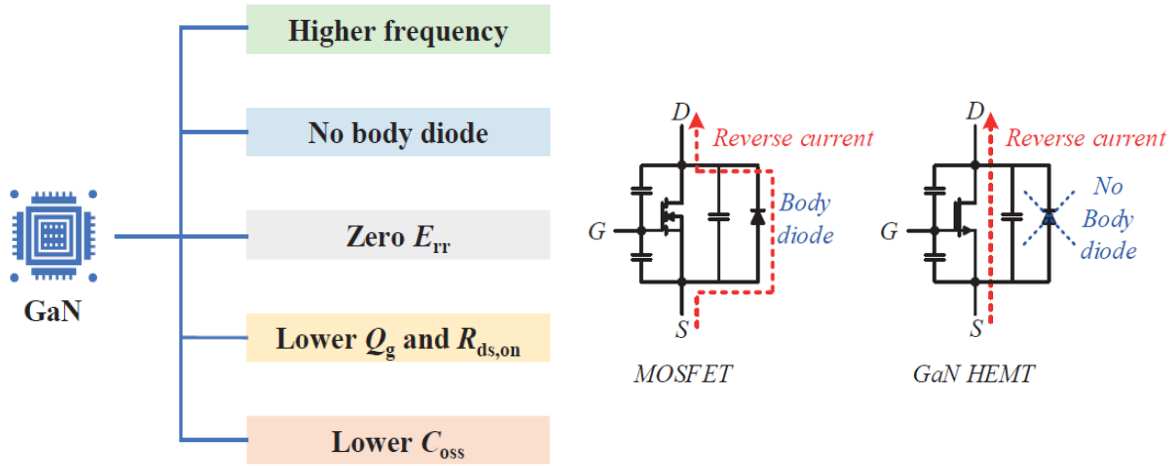


Figure 2.9: Power converters for different robotic applications [18].

2.3.2 GaN HEMTs in Low-Voltage Motor Drive Applications

Actually, power electronics need advanced solutions to increase efficiency and power density. It is particularly true in battery-source motor drive applications, such as humanoid robots and UAVs, where the DC bus voltage is in the range 24V-96V. In fact, the main concern in these systems is achieving the longest possible autonomy by increasing efficiency while also reducing converter size, especially the passive components, which are usually the bulkiest to handle. Since traditional Silicon-based materials have already reached their theoretical performance limits, these challenges can be overcome by using WBG-based semiconductor materials. As stated in Section 1.3, GaN HEMT devices are the most promising technology, especially for low-voltage applications, thanks to their inherent characteristics during switching transients, as well as the possibility of achieving very small packages that maintain the same breakdown capabilities and lower ON-resistance values (see Figure 2.10). However, these benefits come at a higher cost, since eGaN devices in power converters are still an emerging technology.

Below is a more detailed description of the advantages of using GaN HEMTs in low-voltage motor drive applications.



(a) Advantages from GaN technology adoption

(b) MOSFETs vs. GaN HEMTs in reverse conduction

Figure 2.10: GaN HEMTs characteristics [19].

Switching Frequency

In designing a hard-switching inverter topology with MOSFET devices, the PWM frequency cannot be set higher than 40 kHz in order to limit the conduction losses as well as switching losses. With eGaN FETs, instead, switching frequency can be considerably increased (easily up to 100 kHz for motor drive applications), because these devices feature faster commutation transients compared to low-voltage Si MOSFETs counterparts. Indeed, typical eGaN devices' profiles of the input, output, and reverse capacitances show much lower values than MOSFETs, allowing higher voltage and current slew rates with the same gate driver's capabilities. In low-voltage applications, such as battery-powered robotics, these high dv/dt values (which can easily reach 10 V/ns) don't represent a problem in stressing motor insulation systems, unlike what happens in high-voltage motor drives. However, EMI production can assume critical values for the correct operation of surrounding electronic components, and so, output switching legs can be

provided with output filters specifically designed to reduce the impact of these fast transient switching voltages by performing a low-pass harmonic filter.

The main advantage derived from a higher switching frequency is the possibility of reducing the size of the DC input filter. In particular, by maintaining the same maximum voltage ripple on the DC line (since it is inversely proportional to the inverter switching frequency), the bulkier electrolytic capacitors can be replaced with ceramic capacitors, which feature lower series impedance, increased stability in temperature, higher compactness, and enhanced reliability. This improvement is particularly required in IMD design, where power density and reliability are strenuously searched [20].

Motor Drive Efficiency

As will be better explained in Chapter 3, GaN HEMT power devices allow a substantial reduction of conduction resistance, thanks to the planar structure along with the 2DEG phenomenon. Therefore, GaN FETs exhibit higher current density for the same breakdown voltages. This feature is also enhanced by the specific reverse conduction that occurs in a eGaN device. In fact, the HEMT physical structure does not show the p-n junction of the body diode, which is a characteristic of MOSFETs. However, eGaN FET is a bidirectional device, i.e., it lets a negative current flow (natural reverse conduction) when no positive voltage is applied to the gate terminal, showing a similar behavior to a diode on direct conduction, but characterized by a voltage drop higher than that of a body diode inside a MOSFET. If the lack of a body diode removes all the reverse recovery losses in hard switching operation, the higher voltage drop during reverse conduction increases the conduction losses during dead time operation.

Regarding the choice of the optimal dead time to safely and efficiently drive an inverter switching leg, for MOSFETs, this value is usually contained between 200 and 500 ns. Since eGaN FETs feature a very high commutation speed, the minimum dead time achievable before causing short circuits at the input source is down to a few tens of ns. This is beneficial to the motor drive efficiency in two ways. On one side, limiting the dead time automatically produces less reverse conduction losses. Moreover, the reduced dead time allows a better quality of electrical waveforms at the output of the half bridge (i.e., lower THD values). This improvement leads to a more efficient motor driving under the same operating conditions, because the phase current becomes less distorted. Indeed, dead time insertion is the cause for the discontinuity of the voltage modulation during zero crossing of the phase current, and the distortion is also reflected in the other motor phases, thus appearing as the 6th harmonic in the torque applied to the motor [8]. By minimizing this phenomenon, lower motor losses, less vibration, and less acoustic noise can be achieved in the motor's behavior.

Power Stage Integration

In recent years, significant effort has been devoted to integrating a power-stage half-bridge with low-voltage signal control circuitry in a single monolithic circuit using GaN technology. This double integration allows driving eGaN FET gates while controlling some device parameters, such as maximum allowable current, switching speed, minimum input DC voltage, and maximum tolerable IC temperature. Moreover, by integrating the power stage into a single monolithic circuit, the common-source inductance (CSI) can be considerably reduced, as the power and gate loops' inductances are minimized. Therefore, switching performances of GaN FETs can be fully exploited, while limiting EMI emissions.

A system-on-chip (SoC) circuit is also beneficial because it reduces the number of electronic components needed for PCB design, thereby reducing the PCB's overall size and increasing power density. Finally, has also been proven that the integration approach improves the system's reliability [10]. In Chapter 4, this subject will be deepened.

GaN Reliability

Along with new developments in GaN technology for achieving more efficient power devices, deep studies have been carried out to understand the intrinsic failure mechanisms related to the various stress conditions. They have clearly shown that eGaN devices are more robust than Si-based MOSFETs in withstanding extreme and long-term electrical stress conditions [8]. The level of reliability guaranteed by a power device is evaluated by applying many key stress conditions, which involve voltage, current, temperature, humidity, and various mechanical stresses. For instance, voltage stress on an eGaN device can be applied between the gate terminal and the source terminal for testing gate electrode resistance, but also between the drain and source terminals for depicting $R_{DS(on)}$ variations over time. These stresses are usually induced by DC bias, high-speed pulses, or cyclic on-and-off operations. The most disruptive current stress originates from short-circuit conditions, which are the typical tests used to determine how long and at what energy density eGaN devices (and, by extension, power devices in general) withstand before catastrophic failure. Regarding thermal stresses, the devices can be continuously operated at a predetermined extreme temperature for a specific period of time, or the temperature can be cycled in various ways. Furthermore, has been proven that GaN transistors in wafer-level chip-scale (WLSC) have excellent thermo-mechanical reliability according to standard test procedures (AEC or JEDEC): they are capable of -40°C to 150°C in bare die form [8].

If power converters are designed with more reliable power devices, the entire motor drive system will benefit from a longer lifetime, reducing potential replacement costs and ensuring safer operations.

Chapter 3

GaN Power Devices Basics

3.1 GaN HEMT Overview

3.1.1 Crystal Structure of GaN material

The main advantages of using GaN-based transistors rely on the characteristics of the crystal structure that forms Gallium Nitride (GaN) material. It belongs to Group III Nitrides, which is a class of materials characterized by different combinations of group III elements with Nitrogen. Besides GaN, Aluminum Nitride (AlN) and Indium Nitride (InN) materials are other examples of Group III Nitrides. Different crystal structures can be used to synthesize these materials, but the wurtzite structure is the most commonly used, since it is the most thermally stable. In this type of structure, the way in which the atoms tend to arrange themselves forms different three-dimensional patterns known as crystal lattices. The wurtzite structure is usually described as a hexagonal form (Figure 3.1a), but the most basic repeating part is named the unit cell (Figure 3.1b). Crystallography is a branch of science that studies the physical properties of a material, starting with the distribution of atoms in its crystal structure.

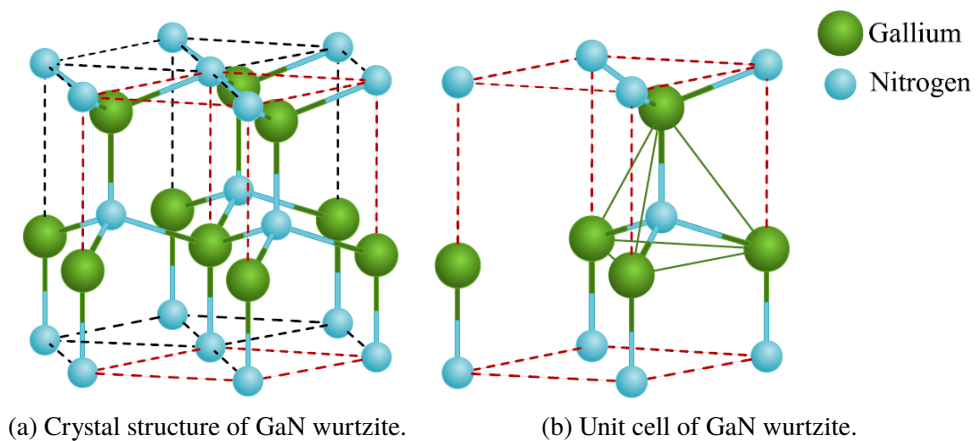


Figure 3.1: GaN wurtzite crystal. [10]

The first fundamental characteristic of GaN wurtzite structure is the spontaneous polarization of the ionic bond between Nitrogen and Gallium atoms, because of the higher electronegativity of the former. The other one is related to the inversion symmetry of a crystal structure, i.e., inside a unit cell each atom has another identical atom equidistant from the inversion center, but on the opposite side [21]. GaN wurtzite is a piezoelectric material because it features a lack of inversion symmetry along one direction, so the distribution of atoms inside its unit cells is not uniform, causing a non-zero piezoelectric polarization, which is also reflected at the material level. Therefore, the unit cell of a GaN wurtzite structure can be depicted as a dipole, where there is a positive charge between the two ends [10].

3.1.2 Lateral GaN Devices

For many years, traditional silicon-based power semiconductor devices have been manufactured as vertical structures, in order to achieve a higher surface area utilization and so to increase the power density. However, with the current technology, manufacturers cannot afford to design vertical GaN devices, even though some innovative solutions are under development [22], because the native GaN wafers are still too expensive and of insufficient quality. This prevents reaching the theoretical performances of GaN devices, especially when high breakdown voltages are needed. In fact, the maximum voltage blocking capabilities of lateral devices are obtained by increasing the length of the transistor structure, but at the same time, the $R_{DS,ON}$ also increases. Therefore, GaN-based transistors are mainly used in low and medium power applications (up to 650 V), where the higher electron mobility and high electron density characteristics can be better exploited to make power devices more competitive than Si or SiC MOSFETs.

Nowadays, all the commercial GaN power devices are synthesized with a lateral structure, which is usually grown on the top of a substrate through epitaxy. The cheapest solution is to use a silicon substrate, but a buffer layer in between is needed to avoid structural imperfections and degradation of the GaN active layer quality. In fact, the silicon substrate has a different atom displacement that interacts with the above GaN layer, without any intermediate layer, causing a reduction of conductivity and switching features of the device. This buffer is usually made of an alternating sequence of GaN and AlGaN thin films [10].

After the buffer, the active GaN layer is grown, and on top of that, an Aluminum-GaN alloy (AlGaN) layer is finally grown. Both layers are characterized by the wurtzite structure, but only the AlGaN layer presents both the spontaneous and piezoelectric polarizations. In fact, the GaN layer does not show any piezoelectric polarization, since the buffer layer is specifically designed to minimize the strain in the above buffer/GaN junction. On the other hand, the AlGaN layer presents a higher spontaneous polarization but also a piezoelectric polarization due to the fact that the above GaN layer has the atoms closer to each other. The overall result is that the junction between the two layers has a positive net charge, which comes from the sum of the positive charge of the AlGaN layer and the negative charge of the GaN layer.

This positive net charge located at the AlGaN/GaN junction causes the accumulation of a large number of free electrons from the material in order to achieve neutrality in the junction. Thus, a high mobility and high density electron channel is formed, and it is named Two-Dimensional Electron Gas (2DEG), because the electrons are free to move only inside a very thin plane, which is the one parallel to the junction surface. The electrons' confinement obtained thanks to the 2DEG phenomenon allows us to achieve very high levels of electron mobility and electron density, without doping the semiconductor material and so without adding impurities that would interact with free electrons.

In Figure 3.2, the representation of a lateral GaN HEMT is shown. Since a transistor usually features three terminals, the manufacturing of a GaN HEMT is finished with the placement of gate, drain, and source terminals. The drain and source terminals can be found at the two ends of the structure, both of which are directly connected to the 2DEG channel, while the gate terminal is placed above the AlGaN layer to give the possibility of controlling the device's conductivity by applying a proper gate-source voltage.

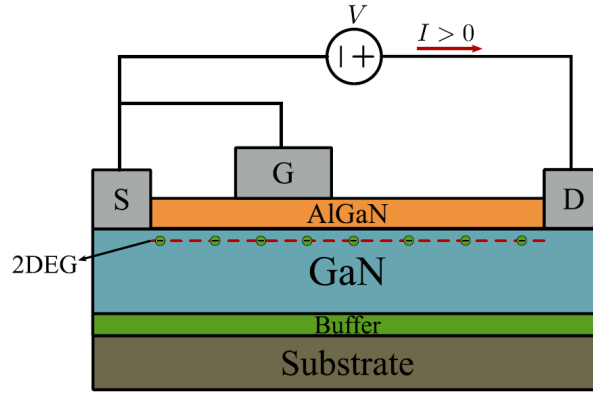


Figure 3.2: GaN HEMT structure (D-mode) [10].

3.2 Enhancement Mode GaN Transistors

As shown in Figure 3.2, a lateral GaN HEMT device has an inherent functionality as a normally ON device, i.e., a depletion-mode (D-mode) transistor. Obviously, in standard power electronics applications, this type of device is avoided due to problems during startup and driver failure events (short-circuit risk). Therefore, different solutions have been proposed to obtain reliable normally OFF GaN devices. The first category relies on enhancement transistors, which require a sufficiently high positive gate-source voltage to switch the device on. This operation is achieved by modifying the gate-terminal structure to interrupt the 2DEG channel when the applied gate voltage is below the corresponding threshold voltage. In particular, the eGaN power transistor is obtained by shifting the threshold voltage to positive levels, in order to create a conductive channel only if a proper positive voltage is applied. Even though some innovative solutions have been introduced in literature, such as MISHEMT (Metal-Insulator-Semiconductor High Electron Mobility Transistors) and MOSHEMT (Metal-Oxide-Semiconductor High Electron Mobility Transistors) [10], all the most used eGaN transistors have significant differences compared to MOSFETs in terms of gate terminal structure and gate voltage levels. Indeed, for instance, their threshold voltage V_{GSth} is very low, between 1V and 2V, and they need a driver circuit that must supply a gate voltage from 0V to +6V. Moreover, the reverse conduction that happens during the dead time operation is performed by an equivalent diode conduction mechanism, which causes a higher voltage drop than a MOSFET body diode, due to GaN's higher energy bandgap capabilities, significantly increasing the reverse conduction power losses. In spite of that, the enhancement-mode GaN transistors are the most widespread category of GaN FET devices in the industry, since their manufacturing is cheaper and ensures a higher reliability.

3.2.1 Recessed Gate Transistor

A first method to positively shift the threshold voltage in a HEMT GaN device is to embed the gate terminal inside the AlGaIn layer (Figure 3.3). In this way, the polarization of the AlGaIn layer under the gate terminal is reduced according to how much the gate terminal is recessed inside it. In fact, the gate contact is specifically designed to obtain a Schottky contact in correspondence with the metal-semiconductor junction, in order to achieve a potential barrier in the opposite direction to the AlGaIn polarization. The final outcome is that the electron density of the 2DEG channel under the gate terminal is lower than in other regions, which is effectively equivalent to applying a negative voltage to the gate terminal. To obtain a normally OFF power device, the AlGaIn layer thickness must be reduced until the Schottky junction potential barrier is able to remove all the electrons from the 2DEG channel under the gate terminal. However, this solution usually generates very low threshold voltage values, because a trade-off must be accepted between the depth level of the gate terminal, which increases V_{GSth} , and the conduction on-resistance, which is penalized by a deeper gate terminal recession, since the electron density under the gate terminal is strongly affected. In addition, due to the reduced isolation capability of the thinner AlGaIn layer, the resultant gate leakage current is too high for most power applications.

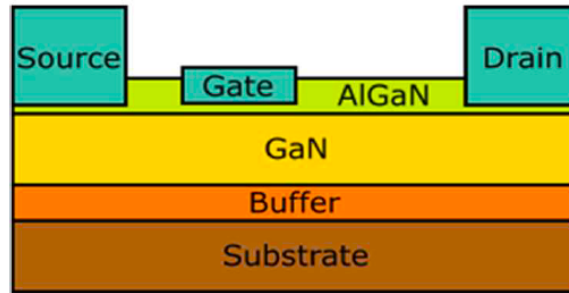


Figure 3.3: Recessed gate HEMT structure.

3.2.2 Fluorine Implanted Transistor

Even though there are no commercially available discrete devices of this type yet, in Fluorine-implanted transistors (Figure 3.4), Fluorine atoms can be introduced inside the AlGaIn layer under the gate terminal, and lower gate leakage current values can be obtained compared with Recessed Gate HEMTs, since the AlGaIn layer behaves as a better insulator if its thickness is not reduced. The 2DEG channel is driven in a cut-off state due to Fluorine atoms' high electronegativity; in fact, these atoms attract negative charge close to the gate terminal, and so electrons are moved away from the 2DEG channel. Also in this case, the gate threshold voltage is very low, and the Fluorine atoms addition process can generate impurities inside the 2DEG channel, reducing the electron mobility and so the R_{DSon} .

3.2.3 p-GaN Gate Transistor

The most common eGaN transistor structure available in the market is the p-GaN gate transistor. This is also known as a Schottky gate transistor, and it is similar to GIT transistors, whose

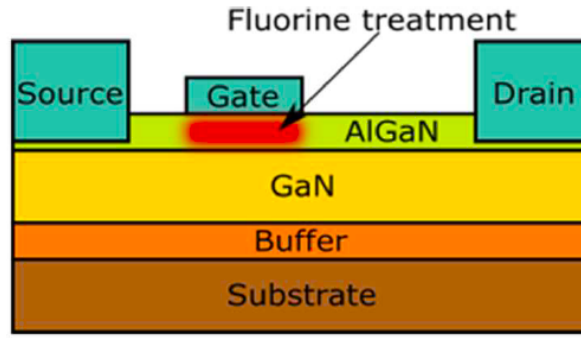


Figure 3.4: Fluorine-implanted HEMT structure.

structure will be described later. To deplete the 2DEG channel under the gate terminal, a pGaN layer is placed beneath it (Figure 3.5). In this way, a fixed negative charge at the junction with the AlGaN layer is established, driving the device into a cutoff state if no voltage is supplied between the gate and the source terminals. Unlike the GIT structure, the gate terminal with the p-GaN layer forms a Schottky contact, and so, when a positive voltage is applied between gate and source, the Schottky diode results in reverse bias, and therefore, only a small leakage current can be measured across the gate terminal. Therefore, p-GaN gate transistors are widely used because a conventional MOSFET driver structure can be used to drive them (a simple resistance at the interface of the gate terminal to adjust the turn-on and the turn-off transitions), with the only care of not exceeding the +6V applied between the gate source terminals. Obviously, to switch on the devices, a sufficiently high gate voltage must be applied, according to the gate threshold voltage, which is similar to that of GIT transistors (around 1.25V).

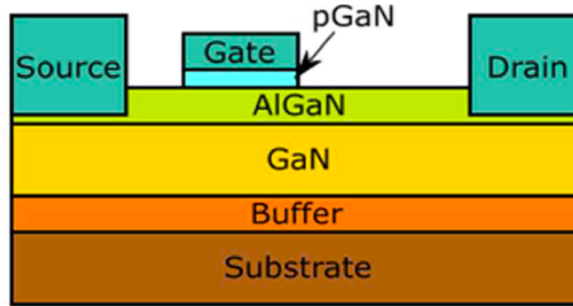


Figure 3.5: p-GaN gate transistor structure.

3.2.4 Gate Injection Transistor

As mentioned before, a further solution to obtain an eGaN device is to use the Gate Injection Transistor (GIT) structure, in which the pGaN layer inserted under the gate terminal is doped. Therefore, the contact formed between the gate terminal and the pGaN layer is an ohmic one, and two PIN diodes between the gate-source and gate-drain terminals are formed (Figure 3.6). Similarly to what happens in a p-GaN Gate Transistor, the p-GaN layer generates a negative fixed charge at the junction between it and the AlGaN layer, repelling electrons from the 2DEG channel. However, the presence of the two PIN diodes introduces an additional operating mode,

which is triggered when the gate voltage exceeds the PIN diode's threshold voltage (around 3V at 25°C). In this condition, the diodes start to conduct, and so a parasitic gate current circulates across the gate terminal, while limiting the V_{GSth} voltage in the gate terminal at their threshold voltage value. Even though this phenomenon increases the on-state gate power consumption, it is beneficial in terms of increasing the electron density in the 2DEG and reducing the R_{DSon} , since the gate current is equivalent to an injection of holes to the 2DEG, which causes additional free electrons to be attracted from the source. However, to keep the gate current low during on-state (a few milliamps), a gate resistance of hundreds of ohms is usually introduced between the gate driver output and the gate terminal. Moreover, to maintain fast switching transients, a parallel branch is added using a smaller resistance in series with a capacitance, with properly chosen values to guarantee that when the device is fully switched on, the driver current flows only in the high-resistance branch, and the gate current consumption would be higher.

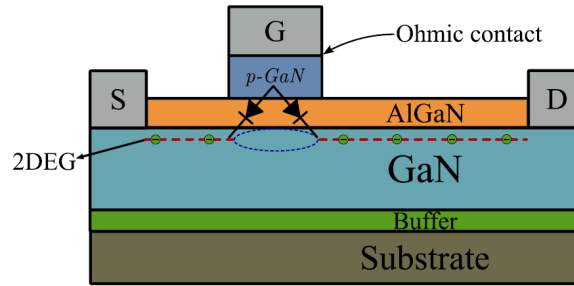


Figure 3.6: Gate injection transistor (GIT) structure [10].

3.3 Hybrid Structure Transistors

The second category of normally OFF GaN devices is made using hybrid transistors, in which a HEMT GaN transistor (D-mode) is combined with a Silicon normally OFF transistor in the same structure. This method allows solving one of the main problems in using eGaN transistors, which is the very low value of their gate voltage threshold. Since GaN devices can be operated at very high dv/dt conditions, a V_{GSth} voltage around 1V can cause crosstalk problems, due to the emission of elevated electromagnetic interferences.

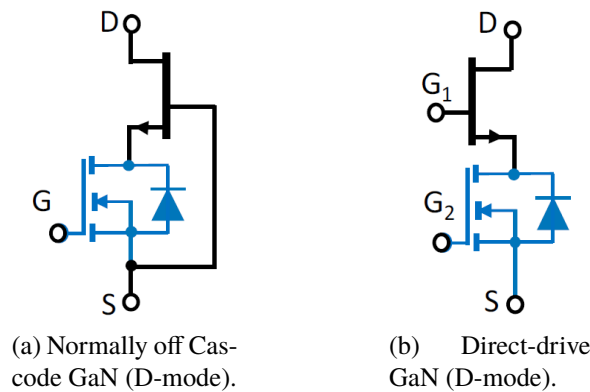


Figure 3.7: Hybrid structure transistors [9].

3.3.1 Cascode Transistor

The schematic representation of a cascode transistor is shown in Figure 3.7a, where it can be seen how it is composed of the series connection of a normally ON GaN HEMT and a Silicon MOSFET. In particular, the drain terminal of the MOSFET is connected to the source terminal of the GaN HEMT, while the gate terminal of the latter is connected to the source of the MOSFET. The operation of this hybrid device is controlled through the accessible gate terminal of the Silicon MOSFET, so the benefits in driving a cascode device come from the higher gate threshold voltage and the negligible leakage gate current, due to the MOSFET's isolated gate terminal. If the MOSFET is driven in the ON state, the gate-source voltage of the GaN HEMT is nearly zero, and so the HEMT is also conducting. Turning off the MOSFET forces the GaN HEMT into a blocking state, because its gate-source voltage is negatively increased by the increase in the drain-source voltage of the MOSFET.

The first problem of this configuration is that the adoption of a Silicon MOSFET increases the total on-resistance of the overall structure and limits its switching dynamics. It is particularly prominent with low-voltage cascode transistors, because both the MOSFET and the GaN HEMT have similar blocking voltage capability. A solution consists of designing the cascode device so that the voltage drop across the GaN HEMT is prevalent compared to the MOSFET during the blocking state, and it is obtained by choosing the proper output parasitic capacitances of the two transistors. In this way, a high-voltage GaN HEMT can be used in combination with a low-voltage MOSFET, which features lower on-resistance values and switching times.

Another problem consists of the larger stray inductances obtained by the higher number of internal connections compared to a single-chip GaN device. Therefore, drain-to-source snubbers and ferrites in the gate terminal must be used to limit large voltage oscillations during the switching transients.

3.3.2 Direct Drive

Figure 3.7b shows a direct drive hybrid transistor, in which a Si-MOSFET is connected in series with a normally ON GaN HEMT, but the gate terminal of the latter is left unconnected, allowing it to be directly controlled. In fact, during the normal operation of this device, the Silicon MOSFET is always kept in the ON state by maintaining its gate-source voltage above the gate threshold, while the GaN HEMT is turned ON and OFF by applying the proper gate-source voltage (negative voltage, about -10V, is needed to switch off the D-mode GaN transistor). To ensure the safe operation during a power supply failure condition, since the D-mode GaN transistor cannot be switched off, the Under Voltage Lockout (UVLO) protection turns off the MOSFET, avoiding a short circuit event. Different from the cascode transistor, this structure always requires that the Silicon MOSFET be able to block the entire operation voltage, and so the R_{DSon} is inevitably higher, even if a GaN HEMT device is used in this hybrid transistor. However, since only the GaN HEMT transistor is used to change the device state during normal operations, direct drive transistors take advantage of the GaN device's fast switching capabilities, along with avoiding resonance problems, since stray inductances are highly reduced.

Chapter 4

GaN Monolithic Power Integrated Circuits

4.1 State-of-the-Art GaN Power ICs

As analyzed in the previous chapters, the main advantage of using GaN devices comes from the possibility of switching at higher frequencies compared to traditional MOSFETs. This feature is really important for applications in which a high power density is essential, because it allows the volume reduction of reactive components, such as inductors and capacitors, which usually determine the overall volume of a power converter. However, the usage of discrete GaN power transistors commonly leads to dealing with parasitic inductances introduced by the numerous interconnections made with copper traces in the PCB. These non-idealities represent the bottleneck that usually limits the switching speed of discrete GaN devices, if the PCB design is not properly carried out. In order to fully use the potential of this technology, but at the same time avoiding voltage signal problems due to stray parameters, monolithic power integration is theoretically the best way, since this approach minimizes the parasitic inductances.

The most typical structure found inside any power IC is the half-bridge circuit, which is composed of a low-side transistor and a high-side transistor. Depending on how many functions are implemented inside the same integrated circuit for controlling and protecting the power stage (HS and LS FETs), two categories of monolithic power integration can be essentially distinguished. Power modules consist only of the power stage integration of one or more half-bridge circuits, with limited integrated functions, because they are rather designed for obtaining high-current power switches in high-power applications. Regarding GaN technology, actually, power devices are made using a cascode configuration, while the development of high-current devices with eGaN power transistors is related to the vertical HEMT structure research, which is in a preliminary phase, yet. Instead, a system-on-chip (SoC) circuit allows for the reduction of required components and overall volume of the converter, since each integrated power device already includes the gate driver and all the necessary detection and protection functions.

Since the last decade, GaN integrated circuits have been studied and developed for demonstrating the feasibility of AlGaIn/GaN heterostructure platform in implementing voltage references, comparators, DCFL inverters, and DCFL ring oscillators. As soon as the p-GaN gate HEMT platform has been commercialized, great developments have been achieved in adding

more integrated components to design more sophisticated GaN power ICs. Moreover, the fabrication of these devices has been strongly influenced by recent improvements in the semiconductor industry, especially regarding the uniformity and yield of manufacturing GaN platforms.

4.1.1 p-GaN Gate HEMT IC Platform

In Figure 4.1, a typical power integration structure using p-GaN gate HEMT technology is shown. On the right are represented the two HV FETs used for implementing the half-bridge topology, which belong to the eGaN power devices' category described in Section 3.2.3. However, besides these transistors, a power IC also needs low-voltage active devices. Thanks to the fact that the voltage rating of a p-GaN gate HEMT almost entirely relies on the gate-to-drain distance, a low-voltage eGaN transistor can be easily obtained by reducing its gate-to-drain distance. Therefore, on the same platform, transistors with multiple voltage ratings can be fabricated with a modular approach. Also, the low-voltage D-mode HEMT can be easily obtained by removing the p-GaN layer under the gate terminal.

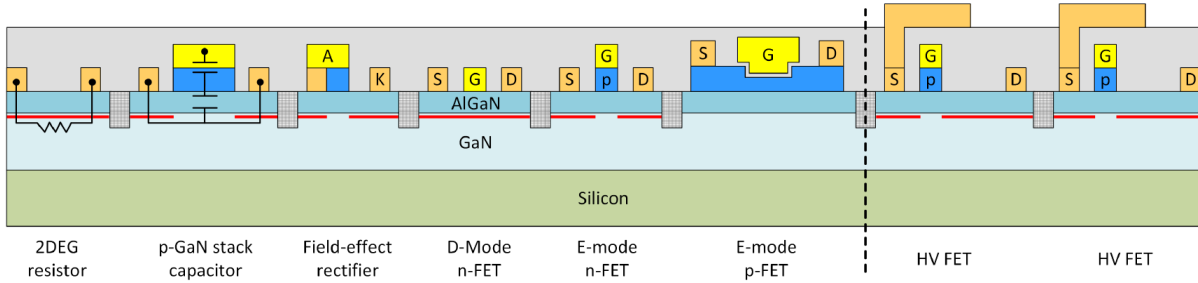


Figure 4.1: Typical power integration structure using p-GaN gate HEMT technology [23].

Field-Effect Rectifier

To obtain a diode from a p-GaN gate transistor, it is sufficient to short the gate and source terminals. The resulting device is a Lateral Field-Effect Rectifier (LFER), in which the original drain terminal has turned to the cathode, while the anode is formed from the connection of gate and source terminals. The LFER thus fabricated has a turn-on voltage lower than the threshold voltage of the original eGaN FET.

Resistor

A resistor can be obtained by etching the p-GaN layer along with the gate terminal, so that the 2DEG channel is fully recomposed and a current can always flow through it. The total resistance value is made up of three contributions:

$$R = 2 \cdot R_c + R_{2DEG}$$

where R_c is the resistance introduced by the two terminals (former drain and source of the original eGaN FET) and R_{2DEG} is the resistance exhibited by the 2DEG channel, which is related to several technological parameters:

$$R_{2DEG} = \frac{L_{2DEG}}{q \cdot \mu_{2DEG} \cdot N_{2DEG} \cdot W_{2DEG}}$$

- μ_{2DEG} : electron mobility
- N_{2DEG} : number of electrons in the 2DEG region
- L_{2DEG} : length of the 2DEG channel
- W_{2DEG} : width of the 2DEG channel
- $q = 1.6 \cdot 10^{-19} C$: charge constant

Moreover, a 2DEG resistor exhibits highly linear I-V curves for various temperatures, which is a very good feature for implementing voltage dividers. These elements are easily obtained by connecting 2DEG resistors in series, and the voltage division obtained in this way is highly independent from the temperature [23].

MIM Capacitor

Another crucial passive component needed inside a power integrated circuit is the capacitor, which should feature a high density to minimize the chip area occupied. The p-GaN gate HEMT technology allows obtaining a Metal-Insulator-Metal (MIM) capacitor, which is formed by the gate metal layer and the field plate layer. But to obtain a high capacitance density, the p-GaN gate-stack structure is preferred for integrating low-voltage capacitors. This component is formed by a metal/p-GaN Schottky junction and a p-GaN/AlGaIn/GaN heterojunction, with an effective oxide thickness less than 20 nm. After turning on the 2DEG channel (i.e., when the voltage exceeds the threshold voltage), its capacity density is more than 200 nF·cm⁻² [23].

4.1.2 Integration of the Gate Driver

Driving a p-GaN gate HEMT introduces some new challenges to face in order to achieve a proper operation in terms of reliability and precise control of the switch. The integration of a GaN gate driver circuit helps to overcome these issues, since this approach allows for minimizing the parasitic inductances of the driving loop. In this way, gate voltage oscillation during any transients can be avoided along with the false turn-on event. In fact, driving a power device at high frequencies makes the gate-source loop more susceptible to exhibiting gate voltage oscillation, which results in a situation that is really dangerous for the gate reliability, especially since p-GaN gate HEMTs can accept a maximum gate bias of 6-7 V. Moreover, these devices are characterized by a very low gate threshold voltage (as explained in Section 3.2, it is about 1.2 V), and so false turn-on events are very likely to happen if gate voltage oscillations are not minimized.

A common topology for integrating a GaN gate driver circuit is shown in Figure 4.2, in which a charge pump unit is present for correctly handling the turn-on operation of the high-side transistor in the buffer stage. As will be deepened in Section 4.2, the use of GaN p-FETs in the buffer stage is not a viable choice yet, while the most used solution is to implement a totem-pole bridge made of two E-mode n-FETs (E_3 and E_4), which is controlled by a pair of Direct Coupled FET Logic (DCFL) GaN inverters (D_1/E_1 for driving E_4 and D_2/E_2 for driving E_3) [24]. The output voltage of the buffer stage is directly fed to the gate of the eGaN power transistor, and depending on the V_i voltage value, it can be promptly commanded.

- Turn-on process: V_i is set to its high value (+5V); E_1 is switched on; E_4 switches in OFF state because its gate is tied to ground due to the low output voltage from the inverter D_1/E_1 ; gate terminal of E_2 is tied to ground and so it is turned off while the coupled D_2 provides the supply voltage V_{DD} to the gate terminal of E_3 ; E_3 is switched on, and so, after the transients of all the aforementioned driving transistors, HV transistor's gate terminal is finally connected to V_{DD} , and it is switched on.
- Turn-off process: V_i is set to its low value (0V); E_1 is switched off; E_4 switches in ON state because its gate is supplied with V_{DD} through D_1 due to the high output voltage from the inverter D_1/E_1 ; gate terminal of E_2 is tied to V_{DD} and so it is turned on; E_3 is switched off because its gate is connected to ground by E_2 , and so, after the transients of all the aforementioned driving transistors, HV transistor's gate terminal is finally connected to ground, and it is switched off.

It is very important to add a charge pump unit in this circuit; otherwise, the V_G voltage would not reach the full supply voltage V_{DD} (+5V), and the charging current during the turn-on of the HV transistor would decrease during the process, resulting in longer switching times. Indeed, if the D_2/E_2 inverter is supplied with a fixed V_{DD} , as V_G increases during the turn-on process, V_{GS3} gate-to-source voltage related to E_3 decreases. Therefore, when $V_G \approx V_{DD} - V_{th}$, $V_{GS3} \approx V_{th}$, and so the driving circuit stops to charge the HV transistor's gate, leading to an increased $R_{DS,ON}$, because V_G cannot reach V_{DD} . With a charge pump (D_B and C_B), instead, E_3 is able to maintain its ON state also if V_G reaches V_{th} , because the capacitor C_B acts as a floating localized voltage supplier, which is charged up to V_{DD} every time V_G is tied to ground (HV transistor in OFF state). In this way, the two problems are solved, since a proper charging current is guaranteed during all the turn-on process, and V_G can finally reach V_{DD} .

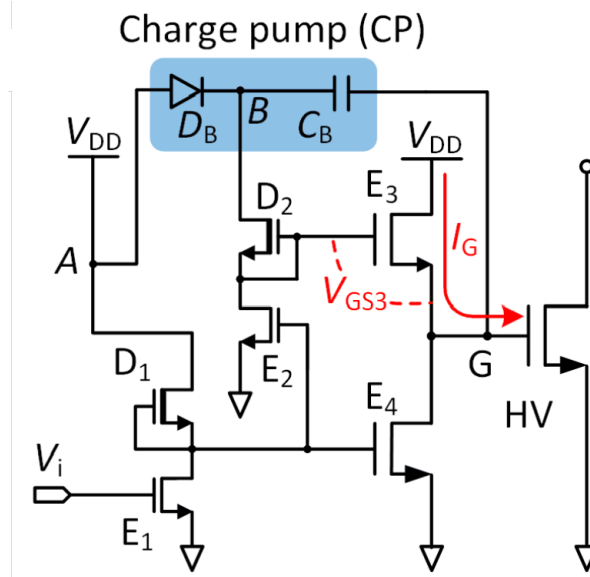


Figure 4.2: Representative topology of an integrated GaN gate driver circuit with a charge pump unit [23].

4.1.3 Integration of UVLO Circuit

The Undervoltage Lockout (UVLO) circuit is one of the fundamental functions needed in a power integrated circuit, since it serves as a detection circuit to shut down the gate driver when the supply voltage V_{DD} becomes lower than a certain value. It is really important because, in case of under-voltage operation, it prevents driving a power transistor that cannot be fully turned on, thus avoiding an excessive increase of its conduction losses (higher $R_{DS,on}$). Usually, this type of circuit implements the under-voltage detection using two threshold voltages V_H and V_L ($V_H > V_L$), so that instabilities during the startup procedure are avoided. If V_{DD} exceeds V_H the UVLO circuit is activated, but only if V_{DD} drops under V_L the UVLO circuit is deactivated. Figure 4.3 presents the schematic design of a typical monolithically integrated UVLO circuit, composed of a resistor ladder, two inverters, and an E-mode transistor.

- UVLO activation: while V_{DD} is rising up and V_1 remains below the threshold voltage of the first inverter (V_{th}), V_2 is tied to V_{DD} , and V_{DD2} is equal to 0 V; E1 is in ON state thanks to V_2 , so R_3 is shorted, and $V_1 = V_{DD} \cdot \frac{R_2}{R_1+R_2}$; V_H can be easily obtained by equating V_1 formula and V_{th} :

$$V_H = V_{th} \cdot \left[1 + \frac{R_1}{R_2} \right]$$

As soon as $V_{DD} > V_H$, V_2 is flipped at 0 V and V_{DD2} is equal to V_{DD} , thus enabling the gate driver operation.

- UVLO deactivation: if V_{DD} is falling down from above V_H , V_2 is still at 0 V, and so E1 is in OFF state; in this case $V_1 = V_{DD} \cdot \frac{R_2+R_3}{R_1+R_2+R_3}$, since R_3 is not shorted by E1; V_L can be easily obtained by equating V_1 formula and V_{th} :

$$V_L = V_{th} \cdot \left[1 + \frac{R_1}{R_2 + R_3} \right]$$

As soon as $V_{DD} < V_L$, V_2 is flipped at V_{DD} voltage, making V_{DD2} equal to 0 V, shorting again R_3 , and thus disabling the gate driver operation.

4.1.4 Integration of OCP Circuit

The other commonly integrated protection block is the Overcurrent Protection (OCP) circuit. It protects the power IC against overcurrent events, which are quite frequent in power switching systems, and the most serious is surely the short-circuit.

Figure 4.4 shows an example of how to design an integrated OCP circuit. This topology consists of two units:

- The sensing unit is used to detect when V_{DS} becomes higher than a certain threshold. In fact, a way to understand if an overcurrent event is ongoing consists of monitoring V_{DS} during the ON operation of the transistor, and when it starts to increase above a certain threshold, it means that the voltage drop across the transistor has been increasing by an anomalous current. In the example shown in Figure 4.4, V_{sense} becomes logic high when V_A rises beyond a predetermined threshold, so Q_1 's output is high, while Q_2 's output is low, disabling the gate driver operation.

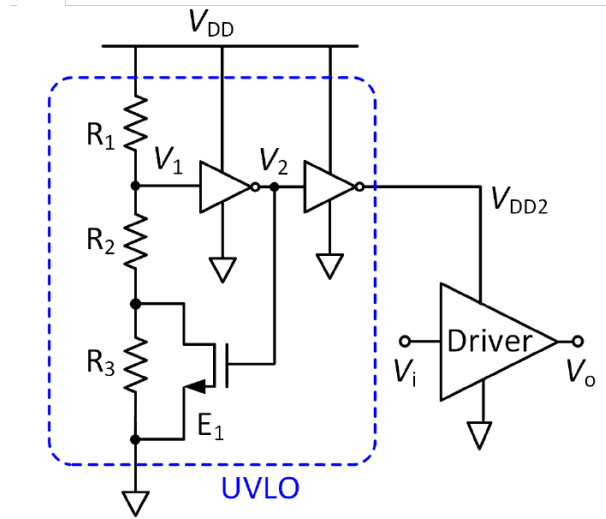


Figure 4.3: Representative topology of an integrated GaN UVLO circuit [23].

- The blanking unit is also important to avoid disabling the gate driver during the turn-on process, as Q_2 's output would always be low, because V_{sense} is logic high when the transistor is in the OFF state. This unit is made of R_1 , C_1 , Q_1 , and Q_2 . When V_i becomes high for switching on the power transistor, the RC low-pass filter introduces a delay in V_{blank} , so that during the turn-on process V_{blank} remains low, keeping Q_1 's output low, and Q_2 's output high. After the RC filter's transient has expired, V_{blank} equals V_i , while V_{sense} returns low because the power transistor is already fully turned on, therefore Q_1 and Q_2 don't change their outputs, keeping the gate driver activated.

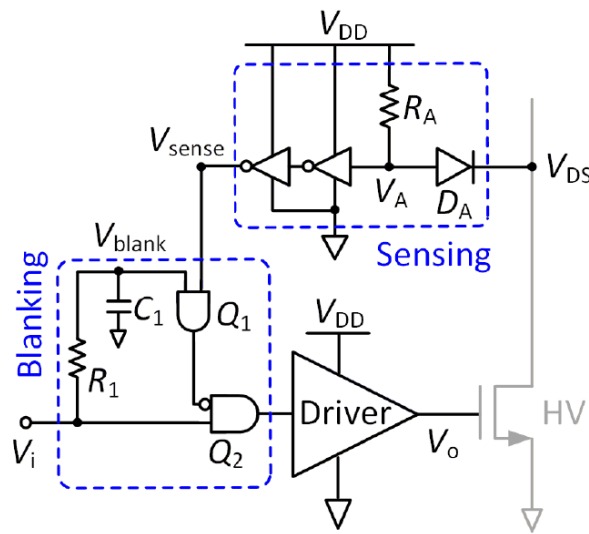


Figure 4.4: Representative topology of an integrated GaN OCP circuit [23].

4.2 Limitations in GaN CMOS Circuits

In Si-based integrated circuits, the use of CMOS technology is widely spread since it has been fully developed. While for implementing logic inverters and buffer stages in GaN-base integrated circuits, nowadays the forced choice is to use only n-FETs, because the p-channel counterparts are still far behind in their technological development. In fact, the main problem in manufacturing compact and efficient p-GaN FETs relies on the difficulty in p-doping, which is caused by the lower mobility of holes with respect to that of electrons; there is a mismatch of two orders of magnitude. Therefore, to obtain the same performance in terms of conduction losses with a p-GaN FET, it has to be designed with a size ten times larger than an n-GaN FET, obtaining an excessive area occupancy of the logic circuitry inside an integrated circuit.

However, using Direct Coupled FET Logic (DCFL) GaN inverters instead of Complementary Logic (CL) GaN inverters, inevitably leads to a higher static power consumption, as can be observed in Figure 4.5. In fact, in a DCFL inverter, the use of a D-mode n-FET causes a non-zero V_o together with a non-zero I_{DD} when the logic input is high, because the high-side transistor acts as a pull-up resistor that is always on. On the other side, if a CL inverter were used, both V_o and I_{DD} would be practically zero when the logic input is high.

Recently, many researchers have been working on improving the performance of p-GaN FETs by introducing innovations in the epitaxial structures, device configurations, downscaling, and ohmic contact formation. The main efforts are focusing on finding the best way of inducing the Two-Dimensional Hole Gas (2DHG) [23]. Moreover, some monolithic CMOS logic circuits have been successively designed and practically demonstrated, showing their implementation feasibility [25], [26]. But more advancements are needed to achieve higher performances while limiting the increase of occupied area, along with the pursuit of guaranteeing the same device stability and reliability offered by n-GaN FET.

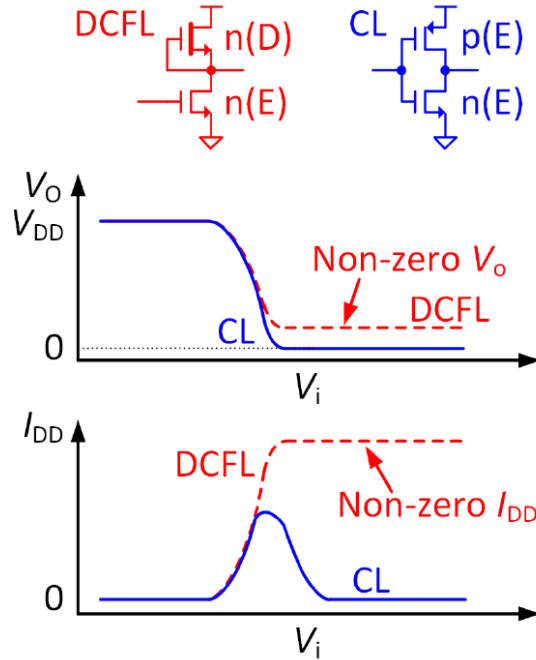


Figure 4.5: Comparison of the static transfer characteristics of DCFL inverter and CL inverter [23].

4.3 Half-Bridge Integration Effects

Regarding discrete GaN-on-Si power transistors, the silicon substrate is usually connected to the source terminal in order to avoid the back-gating effect. This phenomenon is triggered when the substrate/buffer layer starts to trap negative charges, so depleting the 2DEG channel and causing dynamic ON-resistance degradation, since it acts as a parasitic bottom gate where the trapped charges generate a negative potential with respect to the gate-source voltage applied at the gate terminal. However, the back-gating effect is more impactful at high drain voltages, because the electrons are more prone to being injected into the substrate/buffer layer and being trapped by deep-level defects [27].

Since in a monolithic integrated half-bridge circuit, the unique substrate is shared among all the GaN power transistors, there are two main solutions for how the substrate should be terminated. The first one consists of connecting the substrate to the source of the high-side transistor (see Figure 4.6). With this solution, when the HS transistor is switched on, and so the LS transistor is switched off, the latter is subjected to positive back-gating, which causes a severe buffer charge trapping, and consequently an increase of the dynamic $R_{DS,on}$ when the low-side transistor is in the ON state. The second possible choice is to connect the substrate to the source of the low-side transistor (see Figure 4.7). Also, this solution is affected by the back-gating problem, but this time it is related to the HS transistor, which sees a negative bias from the substrate/buffer layer when it is in the ON state, and so its 2DEG channel's conductivity is reduced along with the $R_{DS,on}$.

Latest improvements in the design and manufacturing of GaN-on-Si platforms have allowed to avoid using a single electrical substrate for all the GaN HEMTs used in the power stage. In fact, has been demonstrated that multiple isolated electrical substrates can be implemented on the common mechanical substrate, allowing in this way to eliminate substrate-induced crosstalk effects in high-voltage GaN power integrated circuits.

In [28], a high-voltage GaN integration platform using GaN-on-SOI (Silicon on Insulator) epitaxial layers is discussed. It consists of adding deep trenches of dielectric material into the buried oxide (BOX) for splitting the upper silicon layer into multiple islands. Above each of these silicon islands, a GaN power transistor can be grown, and the Si-island serves as its own local electrical Si-substrate. Instead, the lower silicon layer has the only function of providing mechanical support to all the GaN power transistors, avoiding the high-voltage crosstalk phenomenon.

Another promising solution for obtaining isolated electrical substrates is the GaN power integration platform on Engineered Bulk Silicon substrate (GaN-on-EBUS) [29]. The Si-substrate is doped in order to obtain a p-n junction just under the GaN layer, and by adding deep trenches of dielectric material, the upper p+ silicon layer is split into multiple islands. Above each of these p+ silicon islands, a GaN power transistor can be grown, and the Si-island serves as its own local electrical Si-substrate. Instead, the lower n- silicon layer has the only function of providing mechanical support to all the GaN power transistors, avoiding the high-voltage crosstalk phenomenon. Contrary to the GaN-on-SOI solution, the high voltage between the local electrical Si-substrates is blocked by the p-n junctions inside the Si substrate, and not by the buried oxide (BOX).

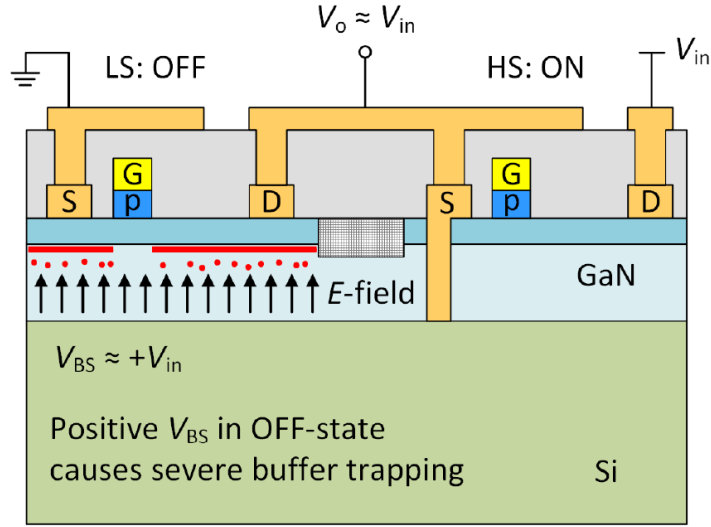


Figure 4.6: Conventional GaN-on-Si platform with substrate connected to HS transistor's source terminal [23].

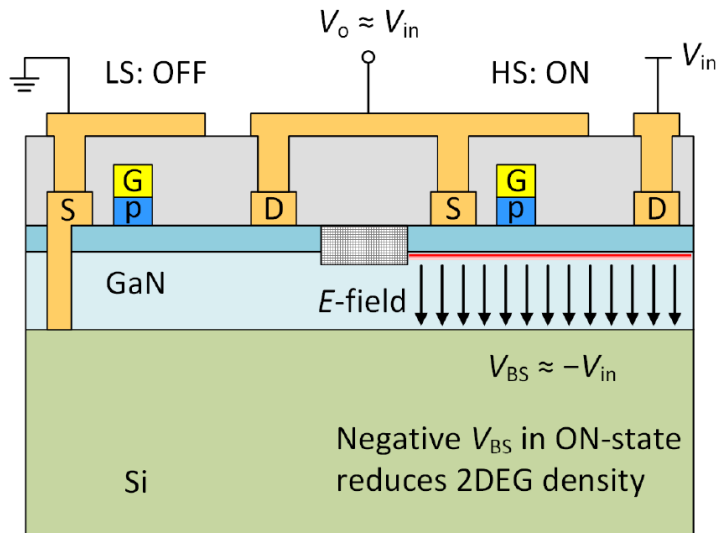


Figure 4.7: Conventional GaN-on-Si platform with substrate connected to LS transistor's source terminal [23].

4.4 Power Stage IC Devices from Different Manufacturers

In 2014, the first monolithic GaN half-bridge without a driver on a single chip was released by Efficient Power Conversion (EPC) [9]. Twelve years later, several GaN power device manufacturers have provided the power IC market with various integrated solutions, featuring not only power stages but also multiple functions, such as driving, control, and sensing, along with protection capabilities. These devices are designed to be used in typical applications of both DC-DC and DC-AC converters, from low to medium voltage applications.

Until now, two main integration approaches have emerged in industry:

- Monolithic Integration (System on Chip - SoC) of power devices, gate drivers, control logic, and auxiliary analog/digital circuits, all of which are co-fabricated on a single semiconductor substrate (usually GaN-on-Si).
- Co-packaging integration of two or more semiconductor dies (System in Package - SiP), which is usually composed of power GaN HEMTs integrated at the package level with silicon-based components for driver and protection circuits

On one hand, the SoC approach aims at minimizing interconnection parasitic inductance for enhancing switching speeds and conversion efficiency. Using GaN platforms, this level of integration is easier thanks to the properties of normally-OFF HEMTs, which feature reduced gate leakage, compatibility with integrated control circuitry, and allow safer operation. Therefore, monolithic GaN SOC's are more suitable for low-voltage and high-frequency applications, in which compactness and power density are crucial. On the other hand, a SiP arrangement allows higher design flexibility and, above all, the possibility to use mature silicon technologies for implementing control functions inside the integrated module. However, they exhibit worse parasitic effects than SoC, due to the higher number of interconnections between chips, limiting the switching performance. Moreover, monolithic SoC devices show less occupied area than SiP ones, considering a similar power capability [30].

In the following sections, some examples of the most recent monolithic GaN half-bridge ICs will be presented, which have been chosen from the actual leading GaN power device manufacturers. Among them, the only device belonging to the SoC category is the EPC23102. In fact, EPC is the only company that is actually offering monolithic GaN ICs in the market, along with Cambridge GaN Devices, while the solutions proposed by the other companies follow a hybrid SiP approach, which consists of integrating at the package level one or more GaN FETs together with silicon technology gate drivers and other functional blocks. CGD offers the single e-mode high-voltage monolithic GaN power stage, ICeGaNTM, which contains a single power GaN FET without an integrated gate driver, but offers an innovative gate structure that can operate up to 20 V, making the products from CGD compatible with traditional Si MOSFET, SiC, and IGBT gate drivers (see Figure 4.8). Moreover, ICeGaNTM features an integrated Miller Clamp to eliminate dv/dt induced shoot through, a Current Sense function to efficiently provide overcurrent protection, and an innovative fully integrated NL (No Load and Light Load) Circuit, which increases energy efficiency by minimizing power losses in light-load and no-load operations [31].

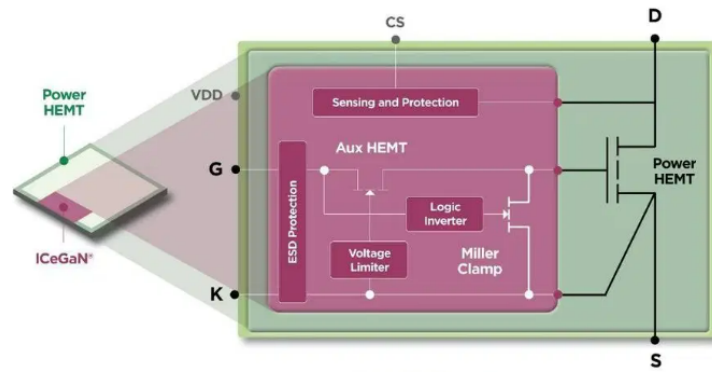


Figure 4.8: 650 V ICeGaN™ Power IC from CGD.

4.4.1 EPC23102 from Efficient Power Conversion

Regarding DC-DC and DC-AC low-voltage applications, EPC23102, from Efficient Power Conversion, is one of the best GaN power stage ICs in terms of integrated functions, performance, and power density. It belongs to the ePower™ Stage IC Product Family of EPC, which integrates many functions, such as input logic interface, high-side level shifting, synchronous bootstrap charging, and gate drivers along with eGaN output FETs. All of these components are included in one monolithic integrated circuit, using an MSL1 QFN (Quad Flat No-Lead) package with a size of 3.5 x 5 mm. Its rated continuous load current at 1 MHz and 25°C is declared 35 A, while its breakdown voltage is defined at 100 V. Both HS and LS FETs have a typical $R_{DS,on}$ at 25°C of 5.2 mΩ [32]

Above are listed all the main features of EPC23102, which can also be identified in the functional block diagram in Figure 4.9, while Table 4.1 summarizes all the key parameters.

EPC23102 Features

- 5 V external bias supply;
- independent high side and low side control inputs;
- 3.3 V or 5 V CMOS input logic levels;
- logic lockout commands both FETs off when inputs are both high at the same time;
- external resistors to tune SW switching times and over-voltage spikes above rail and below ground;
- robust level shifter operating for hard and soft switching conditions;
- false trigger immunity from fast switching transients;
- synchronous charging for high-side bootstrap supply;
- disable input engages low quiescent current mode from VDRV supply;
- power on reset for low side VDD supply;
- undervoltage lockout for high side VBOOT supply;

- active gate pull-down for HS FET and LS FET with loss of VDRV supply;
- thermally enhanced QFN package with exposed top for low thermal resistance from junction to top-side heatsink.

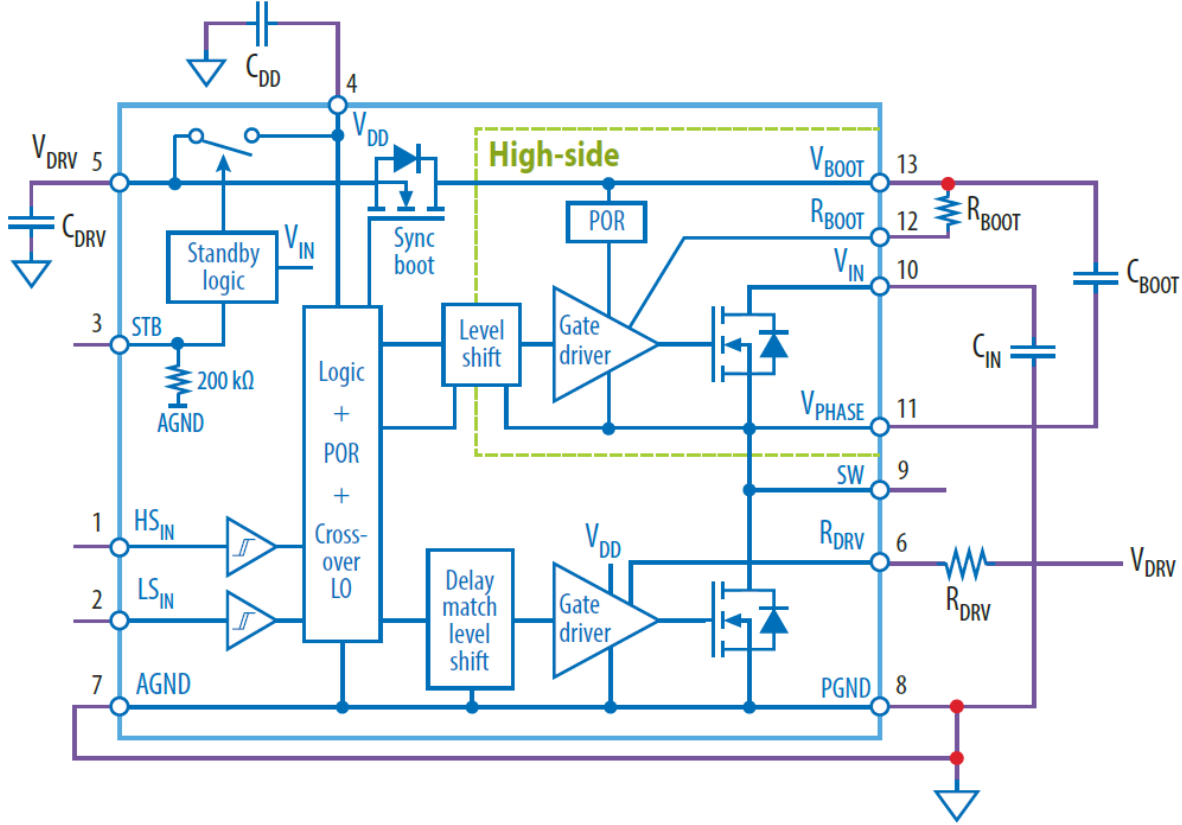


Figure 4.9: Functional Block Diagram of EPC23102 from Efficient Power Conversion [32].

Table 4.1: EPC23102 key parameters [32].

Parameter	Value	Unit
Power Stage Continuous Load Current (1 MHz, 25°C)	35	A
Minimum operating PWM Frequency (25°C)	5	kHz
Maximum operating PWM Frequency (25°C)	3	MHz
Absolute Maximum Input Voltage	100	V
Operating Input Voltage Range	80	V
Nominal Bias Supply Voltage	5	V
R _{DS,on} HS FET at 25°C	5.2	mΩ
R _{DS,on} LS FET at 25°C	5.2	mΩ
QFN package size	3.5 x 5	mm

4.4.2 IGI60L1111B1M from Infineon

In the low-to-medium power area, IGI60L1111B1M shows very good characteristics as an integrated half-bridge power stage in a small 6 x 8 mm Thin-profile Fine-pitch Land Grid Array (TFLGA) package. It consists of two enhancement-mode CoolGaN™ switches with integrated gate drivers, UVLO, internal circuitry for logic handling, high-side gate-drive level shifter, and many other functions that are partially shown in the functional block diagram of Figure 4.10. The two CoolGaN™ switches have a typical $R_{DS,on}$ of 110 m Ω , and can withstand an operating drain-to-source voltage of 600 V. The main advantage in using Infineon's CoolGaN™ switches is related to their very robust gate structures. Moreover, when they are driven in the ON state by a continuous gate current of a few mA, a minimum $R_{DS,on}$ value is always guaranteed. The integrated driver is fabricated using Infineon's SOI-technology to achieve an excellent ruggedness and noise immunity with the capability to maintain operational logic at negative gate voltages through the RC interface between driver and switch made of external SMD resistors and caps. A negative gate drive voltage is required in certain applications to both enable fast turn-off and avoid cross-conduction effects. Finally, the floating channel VB-SW can be used to drive the high-side GaN die with the integrated bootstrap configuration.

Its rated continuous load current at 25°C is declared 7.4 A, while its breakdown voltage is defined at 600 V. Both HS and LS FETs have a typical $R_{DS,on}$ at 25°C of 110 m Ω [33]. Table 4.2 summarizes all the key parameters of Infineon's IC power device under analysis.

IGI60L1111B1M Features

- integrated high-low side gate drivers;
- application configurable turn-on and turn-off speed;
- integrated ultra-fast low-resistance bootstrap diode;
- fast input-to-output propagation (typ. 98 ns) with extremely small channel-to-channel mismatch;
- PWM input signal;
- standard logic input levels compatible with digital controllers;
- single gate driver supply voltage (typ. 12 V) with fast UVLO recovery;
- low-side open source for current sensing with external shunt resistor;
- thermally enhanced 6 x 8 mm TFLGA-27 package;

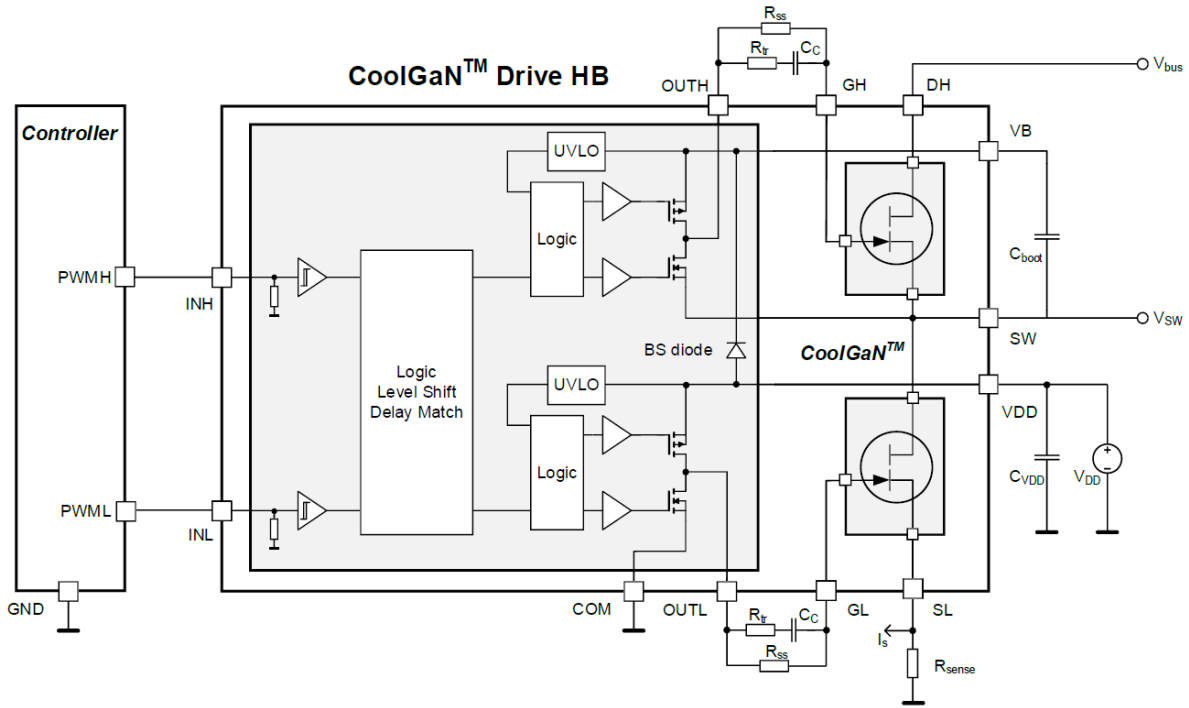


Figure 4.10: Functional Block Diagram of IGI60L1111B1M from Infineon [33].

Table 4.2: IGI60L1111B1M key parameters [33].

Parameter	Value	Unit
Power Stage Continuous Load Current at 25°C	7.4	A
Power Stage Pulsed Load Current at 25°C	30	A
Absolute Maximum Input Voltage (Pulsed)	750	V
Operating Input Voltage Range	600	V
Nominal Bias Supply Voltage	12	V
$R_{DS,on}$ HS FET at 25°C	110	mΩ
$R_{DS,on}$ LS FET at 25°C	110	mΩ
TFLGA package size	6 x 8	mm

4.4.3 LMG2650 from Texas Instruments

The LMG2650 device from Texas Instruments integrates half-bridge power FETs, along with gate drivers, bootstrap FET, high-side gate-drive level shifter, and other useful functions, in a 6 × 8 mm QFN package. It is possible to externally program the turn-on slew rates, providing EMI and voltage ringing control. The low-side current-sense emulation reduces power dissipation compared to the traditional shunt resistor and allows the low-side thermal pad to be connected to PCB power ground, achieving better thermal dissipation. The high-side GaN power FET can be controlled with either the low-side referenced gate-drive pin (INH) or the high-side referenced gate-drive pin (GDH). The former pin is interfaced with the high-side gate-drive signal level shifter, which reliably transmits the INH signal to the high-side gate driver even in harsh power switching environments. The smart-switched GaN bootstrap FET has no diode forward-voltage drop, so it avoids overcharging the highside supply and has zero reverse-recovery charge. The protection functions include FET turn-on interlock, under-voltage lockout (UVLO), cycle-by-cycle current limit, and overtemperature shutdown.

Its rated continuous load current at 25°C is declared 9 A, while its breakdown voltage is defined at 650 V. Both HS and LS FETs have a typical $R_{DS,on}$ at 25°C of 95 mΩ [34]. Table 4.3 summarizes all the key parameters of the TI's IC power device under analysis.

LMG2650 Features

- integrated gate drivers with low propagation delays (< 100 ns);
- programmable turn-on slew rate control;
- current-sense emulation with high-bandwidth and high accuracy;
- low-side referenced (INH) and high-side referenced (GDH) high-side gate drive pins;
- low-side (INL) and high-side (INH) gate-drive interlock;
- high-side (INH) gate-drive signal level shifter;
- smart-switched bootstrap diode function;
- high-side start up (< 8 μs);
- low-side and high-side cycle-by-cycle overcurrent protection;
- overtemperature protection;
- low idle and quiescent currents for the bootstrap (BST) and auxiliary (AUX) voltage rails.
- 6mm × 8mm QFN package with dual thermal pads;

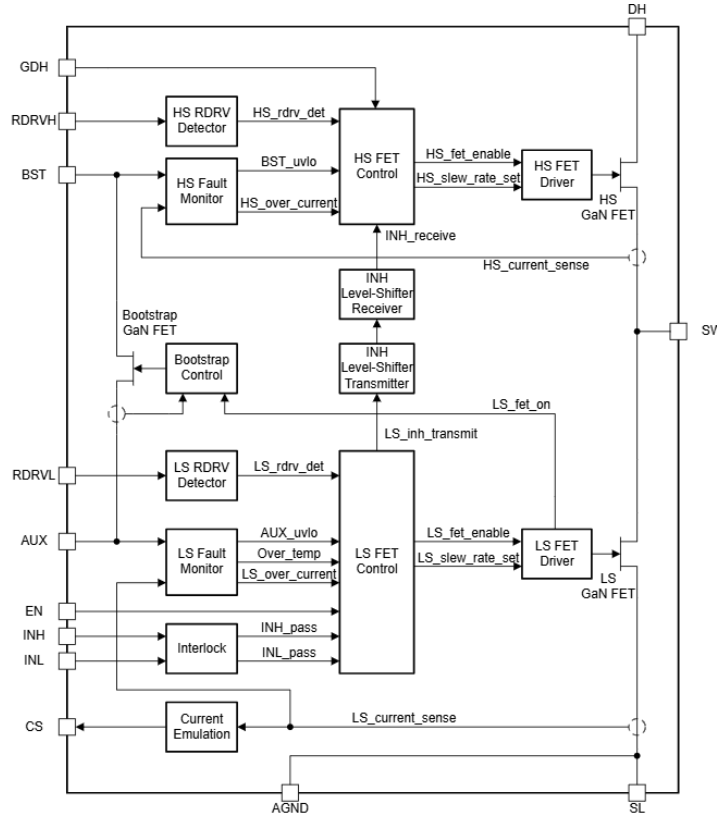


Figure 4.11: Functional Block Diagram of LMG2650 from Texas Instruments [34].

Table 4.3: LMG2650 key parameters [34].

Parameter	Value	Unit
Power Stage Continuous Load Current at 25°C	9	A
Absolute Maximum Input Voltage (Transient)	800	V
Operating Input Voltage Range	650	V
Bias Supply Voltage Range (AUX)	10-26	V
Bias Supply Voltage to SW Range (BST)	7.5-26	V
$R_{DS,on}$ HS FET at 25°C	95	mΩ
$R_{DS,on}$ LS FET at 25°C	95	mΩ
QFN package size	6 x 8	mm

4.4.4 NV6257 from Navitas

Another integrated GaN half-bridge is offered by Navitas, with its NV6257 GaNFast™ power IC, which integrates high-performance eGaN FETs with integrated gate drive, control, and protection to achieve high-frequency and high-efficiency operation in a 6 × 8 mm QFN package. Moreover, GaNSense™ motor drive technology is included in this device, enabling real-time, accurate sensing of voltage, current, and temperature. The integrated current sensing is lossless, since it does not use any shunt resistors, thus increasing system efficiency. GaNSense™ motor drive architecture also enables short circuit, overtemperature protection, and auto-standby mode. Its rated continuous load current at 25°C is declared 6.5 A, while its breakdown voltage is defined at 650 V. Both HS and LS FETs have a typical $R_{DS,on}$ at 25°C of 170 mΩ [35]. Table 4.4 summarizes all the key parameters of the Navitas's IC power device under analysis.

NV6257 Features

- wide input supply voltage range (10 to 24 V);
- accurate loss-less bi-directional current sensing;
- 3.3, 5, 12 V PWM input compatible;
- floating high-side with internal level shift;
- two independent logic inputs with hysteresis;
- 200V/ns common mode transient immunity;
- integrated high-side bootstrap;
- shoot-through protection;
- turn-on and turn-off dV/dt control (low-side and high-side);
- short circuit protection, low-side and high-side;
- overtemperature protection;
- autonomous synchronous rectification mode;
- autonomous low-current standby mode;
- autonomous synchronous rectification mode;
- fault output and enable input;

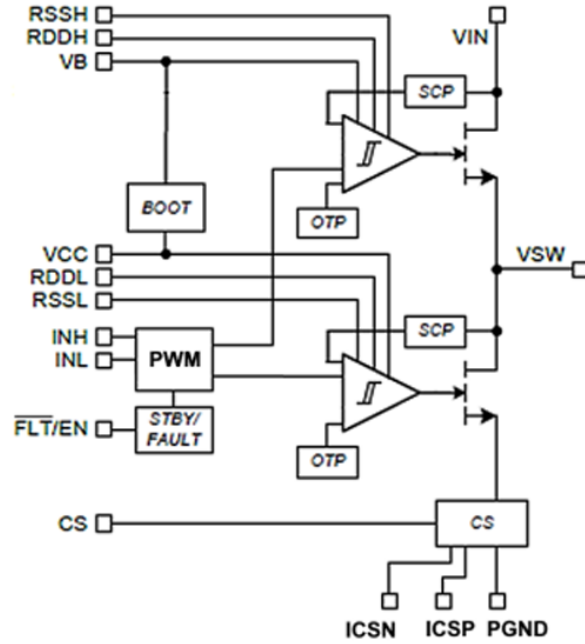


Figure 4.12: Functional Block Diagram of NV6257 from Navitas [35].

Table 4.4: NV6257 key parameters [35].

Parameter	Value	Unit
Power Stage Continuous Load Current at 125°C	6.5	A
Power Stage Pulsed Load Current at 25°C	13	A
Maximum operating PWM Frequency (25°C)	2	MHz
Absolute Maximum Input Voltage (Transient)	800	V
Operating Input Voltage Range	650	V
Nominal Bias Supply Voltage Range	15	V
$R_{DS,on}$ HS FET at 25°C	170	mΩ
$R_{DS,on}$ LS FET at 25°C	170	mΩ
QFN package size	6 x 8	mm

4.4.5 MASTERGAN7 from STMicroelectronics

The MASTERGAN7 power stage IC from STMicroelectronics is an advanced power system-in-package (9 x 9 x 1 mm QFN) integrating two eGaN transistors in a half-bridge configuration driven by a high-voltage, high-frequency silicon-based gate driver. In order to optimize driving efficiency, the MASTERGAN7 features linear regulators on both the lower and upper driving sections. Moreover, the embedded gate driver can receive the power supply voltage from an integrated bootstrap diode for its high-side section. This advanced driver section, thanks to a small propagation delay, has a very short wake-up time, and short, minimum on-times, enable high frequency switching operation. The interlocking function avoids cross-conduction conditions. The extended range of input pins, as well as the remote signaling pin (FLT), allows easy interfacing with controllers, microcontrollers, or DSP units. The standby pin allows for reducing the power consumption of the device during inactive periods.

Its rated continuous load current at 25°C is declared 6 A, while its breakdown voltage is defined at 650 V. Both HS and LS FETs have a typical $R_{DS,on}$ at 25°C of 270 mΩ [36]. Table 4.5 summarizes all the key parameters of the STMicroelectronics's IC power device under analysis.

MASTERGAN7 Features

- power system-in-package integrating 650 V GaN transistors, a half-bridge with high-voltage gate driver;
- linear regulators to regulate high-side and low-side driver supply voltage;
- overall driver's propagation delay of 45 ns and 35 ns minimum pulse;
- very fast wake-up time of high-side driver;
- externally adjustable turn-on resistors;
- UVLO protection on VCC and high-side driver supply voltage;
- interlocking function;
- dedicated pins for standby and shutdown with a fault pin for remote signal;
- 3.3 V to 15 V (typ.) compatible inputs with hysteresis and pull-down;
- thermal shutdown protection;

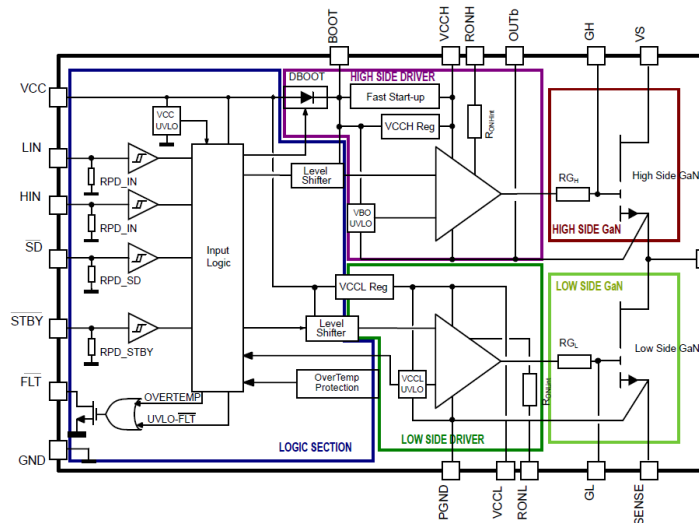


Figure 4.13: Functional Block Diagram of MASTERGAN7 from STMicroelectronics [36].

Table 4.5: MASTERGAN7 key parameters [36].

Parameter	Value	Unit
Power Stage Continuous Load Current at 25°C	6	A
Power Stage Pulsed Load Current at 25°C	8	A
Maximum operating PWM Frequency (25°C)	2	MHz
Absolute Maximum Input Voltage (Transient)	750	V
Operating Input Voltage Range	650	V
Nominal Bias Supply Voltage Range	15	V
R _{DS,on} HS FET at 25°C	270	mΩ
R _{DS,on} LS FET at 25°C	270	mΩ
QFN package size	9 x 9	mm

Chapter 5

Three-Phase ePower™ Stage IC

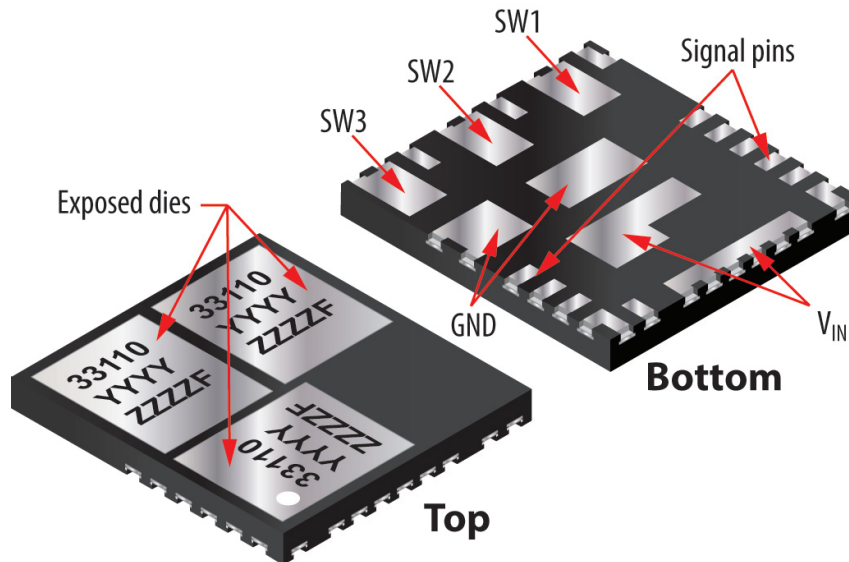


Figure 5.1: Top and bottom view of the EPC33110 module [37].

5.1 General Description

The motor drive inverter board designed and tested for this thesis features the EPC33110, a three-phase co-packaged module that integrates three GaN half-bridges, each with an integrated gate driver, bootstrap circuits, and level shifters. Thanks to the integration of three monolithic half-bridge dies, this device results in a compact, high-power-density solution optimized for robotic motor control applications, such as humanoid robot joints and drone motors. The module operates with a maximum recommended input voltage of 80 V and exhibits a typical on-resistance of $11.7 \text{ m}\Omega + 13 \text{ m}\Omega$ at 25°C per each phase (Table 5.1).

Above are listed all the main features declared by the manufacturer (Efficient Power Conversion) on the EPC33110 datasheet [37].

EPC33110 Features

- each phase integrates high-side and low-side eGaN FET with internal gate driver and level shifter;
- single 5 V external bias supply;
- 3.3 V or 5 V CMOS input logic levels;
- independent high-side and low-side control inputs for all phases;
- logic lockout commands both FETs off when inputs are both high at the same time;
- robust level shifter operating for hard and soft switching conditions;
- synchronous charging for high-side bootstrap supplies;
- standby function for low quiescent current mode;
- fast PWM Shutdown when ($\overline{\text{SD/STB}}$) pulled low;
- power-on-reset for low-side and high-side power supplies;
- power stage high impedance guaranteed in the absence of $V_{\text{DRV}}/V_{\text{BOOT}}$ supplies;
- 0% and 100% duty capable;
- thermally enhanced QFN package with exposed top for low thermal resistance from junction to top-side heatsink.

Table 5.1: EPC33110 key parameters [37].

Parameter	Value	Unit
Power Stage Continuous Load Current (25°C)	20	A
Maximum operating PWM Frequency (25°C)	3	MHz
Absolute Maximum Input Voltage	100	V
Operating Input Voltage Range	80	V
Nominal Bias Supply Voltage	5	V
$R_{\text{DS,on}}$ HS FET at 25°C	11.7	mΩ
$R_{\text{DS,on}}$ LS FET at 25°C	13	mΩ
QFN package size	6.5 x 6	mm

The EPC33110 GaN module is actually the smallest but most powerful micro-module on the market that meets the requirements of robotic applications [30]. In fact, with this device, EPC offers an innovative solution in the market of GaN power stage ICs, since the design of this module combines the latest advances in packaging technology with pure GaN-on-Si monolithic circuit integration. Internally, it includes three monolithic (SoC) GaN half-bridges arranged in a

SiP configuration to form an inverter micromodule. Each monolithic GaN half-bridge is based on the EPC23110 integrated full-GaN smart half-bridge [38], which shows all the features already mentioned for the micromodule's phases. The only difference that can be observed between the monolithic half bridges used in the EPC33110 and the EPC23110, is that with the former it is not possible to tune the switching speed of the three SW nodes because the external RDRV (for the low-side driver) and RBOOT (for the high-side driver) resistances are integrated inside the half-bridge dies (both fixed at $10\ \Omega$) for limiting the package size due to the pins (two for each phase). In Figure 5.2, a simplified structure of the single monolithic half-bridge implemented using full GaN technology in a GaN-on-Si platform is represented. For simplifying the representation, the isolation between the high-side and low-side circuits is not shown, but it is actually carried out by implementing a P-iso Isolation for electrically separating the P-well (P-type region of the substrate connected to GND) and N-well (N-type region of the substrate connected to SW).

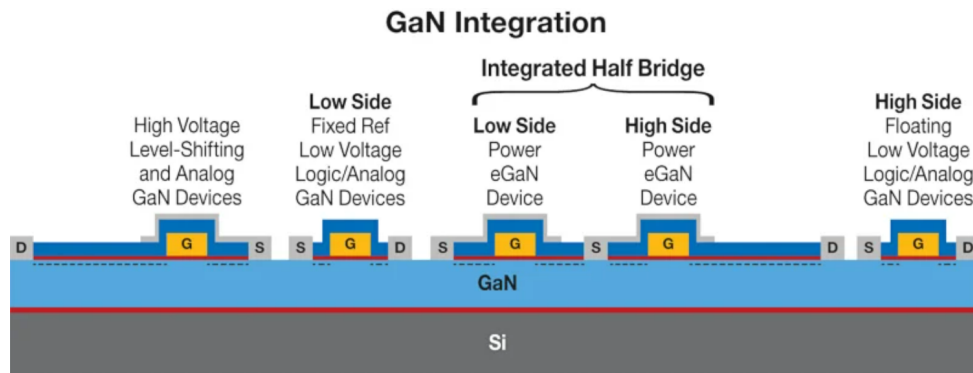


Figure 5.2: Integrated half-bridge (SoC solution) of a monolithic full GaN-based technology.

5.2 Datasheet Specifications

The first important information that can be retrieved from the datasheet of a power stage IC is its pinout description. In Figure 5.2 is shown the Transparent Top View of the EPC33110 module, together with the related pinout assignment, while in Table 5.2 is reported the pinout description, in which are specified the typology and the function of each pin, which will be better analysed in Section 5.4, when the EPC33110 functional block diagram will be described in detail.

In addition, from Figure 5.4, some information about the correct use of the module in a typical motor drive application can be recovered. First of all, for each internal power supply, a bypass capacitor of $100\ \text{nF}$ must be connected between V_{DDX} and GND. Then, at the interface with the external power supply of 5V , it is needed to place a bypass capacitor of at least $6.8\ \mu\text{F}$ between V_{DRV} and GND to supply all the integrated drivers with the required power, guaranteeing a constant voltage during all operating conditions. Finally, the bootstrap capacitors needed by the high-side gate drivers are not integrated inside the monolithic half bridges, so three CBOOT capacitors of $2.2\ \mu\text{F}$ are suggested to be placed between V_{BOOTX} and GND. Obviously, all the aforementioned capacitors must be placed as close as possible to the module's pins in order to minimize the parasitics introduced by the copper traces of the PCB.

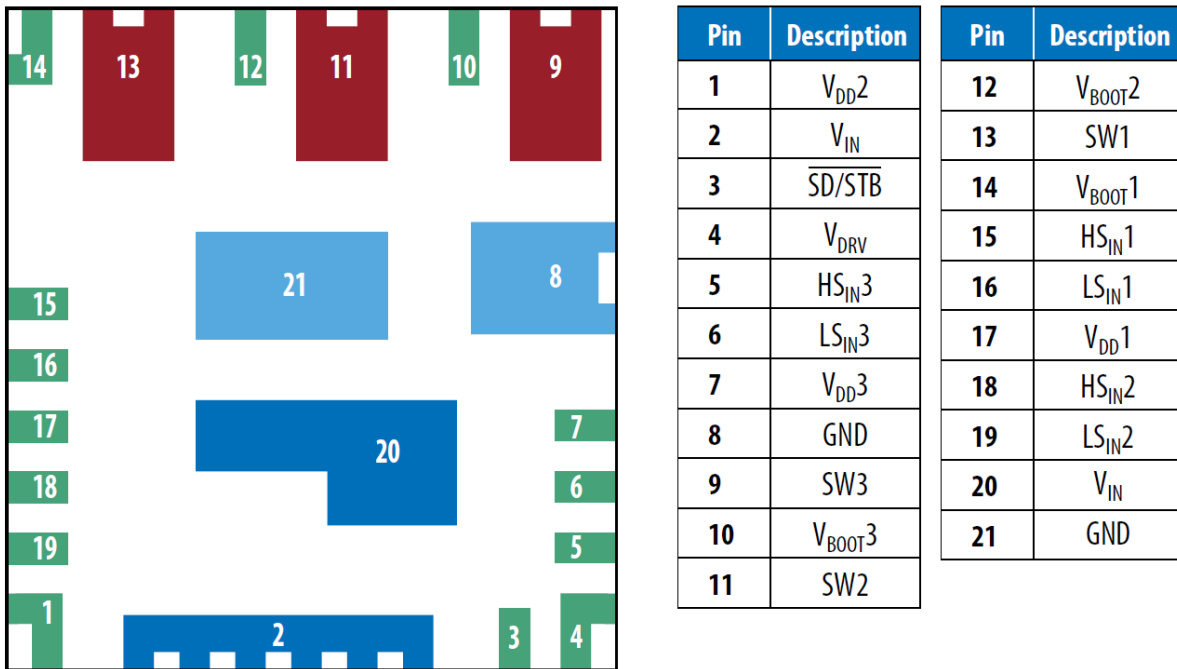


Figure 5.3: EPC33110 QFN Package (Transparent Top View) with the related pinout assignment [37].

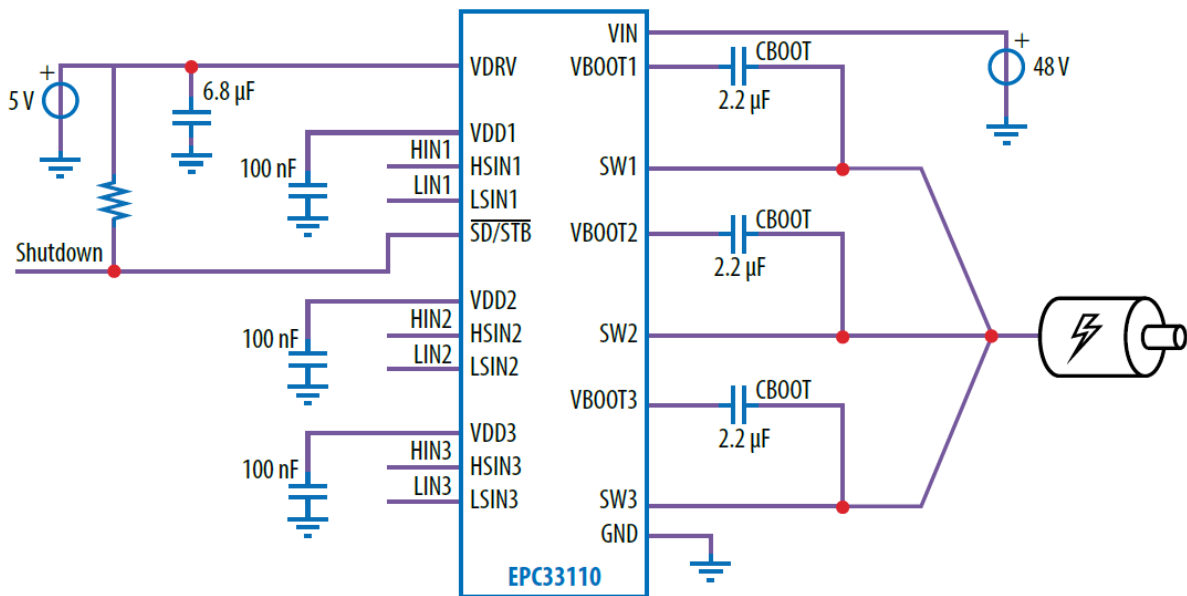
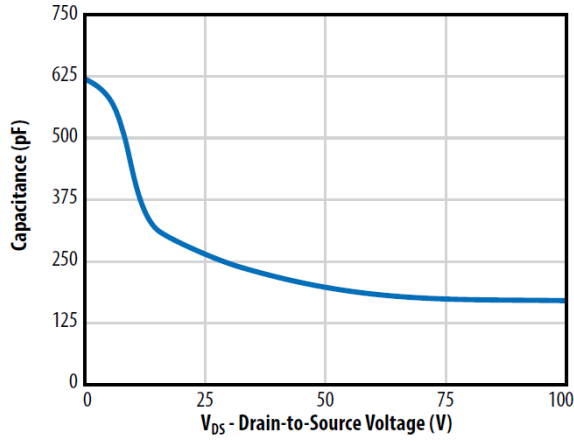


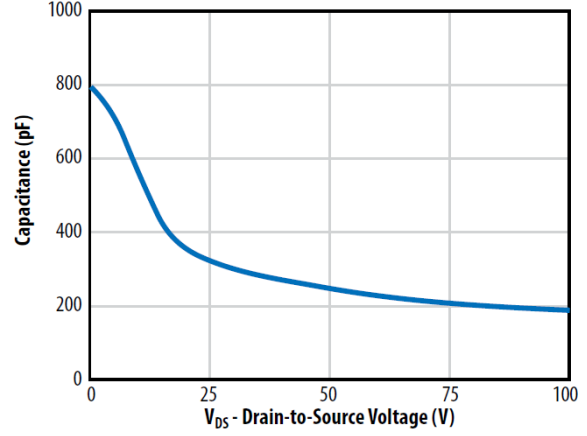
Figure 5.4: Schematic of a EPC33110 Typical Application [37].

Table 5.2: EPC33110 Pinout Description [37].

Pin	Name	Type	Description
1	V _{DD2}	Bias Supplies	Phase 2 internal power supply referenced to GND.
2, 20	V _{IN}	Power	Power DC input connected to the drain terminal of three high-side FETs.
3	$\overline{\text{SD/STB}}$	Logic Inputs/Outputs	V _{DD1} , V _{DD2} , and V _{DD3} standby and PWM fast shutdown input.
4	V _{DRV}	Bias Supplies	External 5 V power supply referenced to GND.
5	HS _{IN3}	Logic Inputs/Outputs	Phase 3 high-side PWM logic input referenced to GND.
6	LS _{IN3}	Logic Inputs/Outputs	Phase 3 low-side PWM logic input referenced to GND.
7	V _{DD3}	Bias Supplies	Phase 3 internal power supply referenced to GND.
8, 21,	GND	Power	Power Ground, connected to the source terminal of three low-side FETs.
9	SW3	Power	Phase 3 switching node, connected to the phase 3 half-bridge power stage output.
10	V _{BOOT3}	Bias Supplies	Phase 3 floating bootstrap power supply referenced to SW3.
11	SW2	Power	Phase 2 switching node, connected to phase 2 half-bridge power stage output.
12	V _{BOOT2}	Bias Supplies	Phase 2 floating bootstrap power supply referenced to SW2.
13	SW1	Power	Phase 1 switching node, connected to the phase 1 half-bridge power stage output.
14	V _{BOOT1}	Bias Supplies	Phase 1 floating bootstrap power supply referenced to SW1.
15	HS _{IN1}	Logic Inputs/Outputs	Phase 1 high-side PWM logic input referenced to GND.
16	LS _{IN1}	Logic Inputs/Outputs	Phase 1 low-side PWM logic input referenced to GND.
17	V _{DD1}	Bias Supplies	Phase 1 internal power supply referenced to GND.
18	HS _{IN2}	Logic Inputs/Outputs	Phase 2 high-side PWM logic input referenced to GND.
19	LS _{IN2}	Logic Inputs/Outputs	Phase 2 low-side PWM logic input referenced to GND.

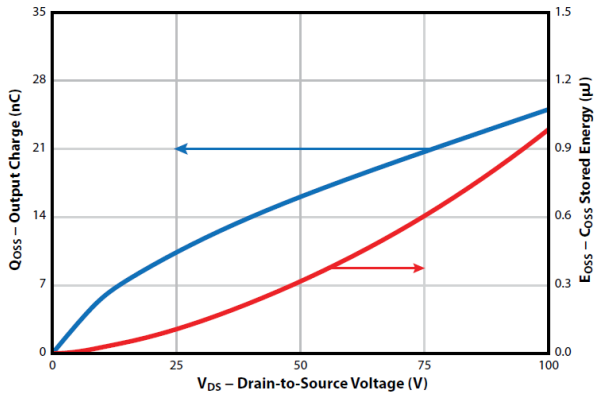


(a) C_{OSS_HSFET} of high-side Power GaN FET

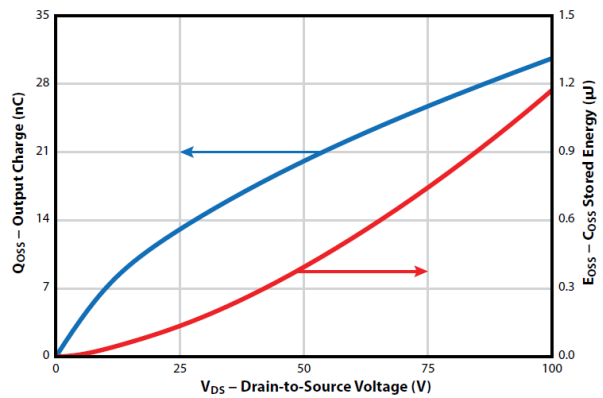


(b) $C_{OSS_LS_Total}$ of low-side Power GaN FET

Figure 5.5: Output Capacitance vs. Drain-to-Source Voltage [37].

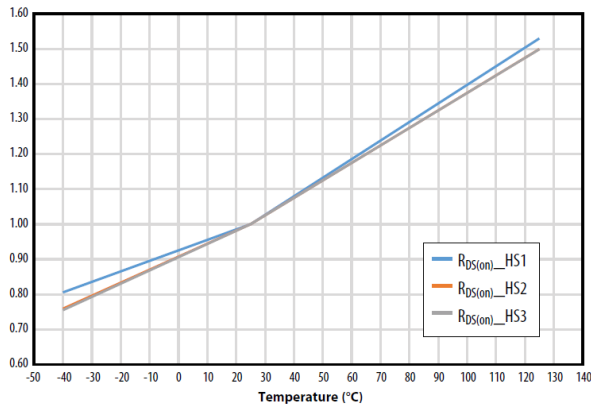


(a) Q_{OSS} and E_{OSS} of high-side Power GaN FET

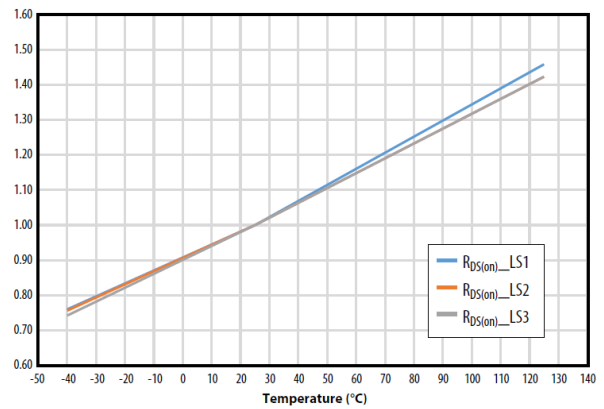


(b) Q_{OSS} and E_{OSS} of low-side Power GaN FET

Figure 5.6: Typical Output Charge and C_{OSS} Stored Energy [37].



(a) HS FETs Normalized $R_{DS,on}$



(b) LS FETs Normalized $R_{DS,on}$

Figure 5.7: Power GaN FETs Typical $R_{DS,on}$ vs. Temperature [37].

Regarding the FETs' parameters that determine their dynamic behavior during switching transients, in the datasheet, the characteristic curves of the output capacitance C_{OSS} , output charge Q_{OSS} , and C_{OSS} stored energy E_{OSS} versus the drain-to-source voltage are inserted. This parameter is really important to determine the power losses $P_{C_{OSS}}$ produced by each FET during commutations:

$$P_{C_{OSS}} = \frac{1}{2} \cdot f_{sw} \cdot C_{OSS} \cdot V_{DS}$$

where f_{sw} is the switching frequency and V_{DS} the drain-to-source voltage [20]. From Figure 5.5a, the typical (i.e., high-voltage value) C_{OSS} value for the internal high-side power FETs is 189 pF, while for the low-side power FETs (Figure 5.5b), it is slightly higher, 221 pF, due to the additional contribution of the well capacitance C_{WELL} . Both values are remarkably lower than in a traditional MOSFET of equivalent electrical characteristics, so higher switching frequencies can be easily used in a motor drive application with the EPC33110, as will be shown in the next chapters. The other two parameters related to the output capacitance are reported in Figures 5.6a-b.

The power FETs $R_{DS,on}$ dependence on the temperature is reported in Figures 5.7a-b, in which the positive temperature coefficient property of GaN devices can be clearly seen. A slightly different thermal behavior can also be observed among the three FETs in both low-side and high-side positions, proving a not perfect symmetry of the three inverter legs in the thermal dissipation, with the FETs of phase 1 more affected by the temperature increase. In any case, above 100°C, all the FETs exhibit a resistance increase of more than 30%, reaching 50% above 130°C.

5.3 Device Footprint

The EPC33110 micromodule comprises three EPC23110 dies arranged in a 6 x 6.5 mm package using a multi-layer interconnection structure. An important process that must be carefully carried out when using a new power device is the definition of its footprint, which is used during the PCB layout. A correct device footprint ensures a proper mechanical fit and electrical connection between the accessible pins of the device and the PCB. It needs the definition of three layers (Figure 5.8):

- Copper layer: it outlines conductive areas in the top/bottom layer of the PCB at which the device's pins will be electrically connected after the assembly process. In Figure 5.9, the recommended copper layer layout present in the EC33110 datasheet is shown, along with its realization in Altium Designer.
- Land pattern: it defines the exposed copper pads that serve as a connection pathway between the power device and the PCB via solder joints. In Figure 5.10, the recommended land pattern layout present in the EC33110 datasheet is shown, along with its realization in Altium Designer.
- Stencil: it is a thin sheet of stainless steel with precision-cut apertures, used to accurately apply solder paste onto PCB pads. In Figure 5.11, the recommended stencil layout present in the EC33110 datasheet is shown, along with its realization in Altium Designer.

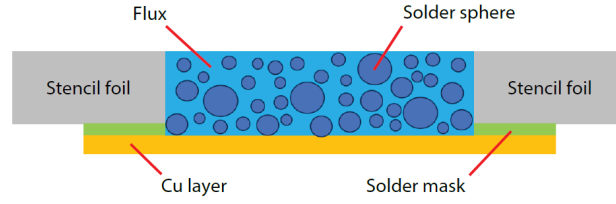


Figure 5.8: Representation of the volume of the solder sphere and flux inside the aperture in the stencil foil [1].

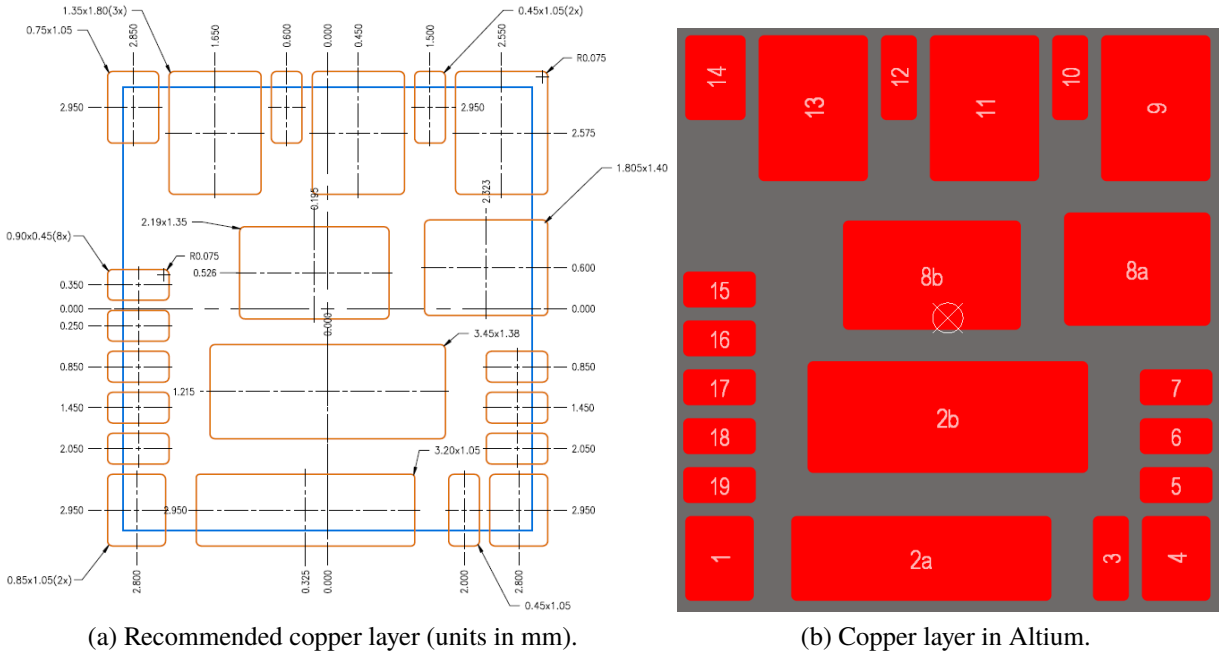


Figure 5.9: EPC33110 copper layer.

5.4 Functional Block Diagram

In Figure 5.12, the functional block diagram of one of the three phases is shown. In particular, the inputs V_{IN} , GND , $\overline{SD}/STB$, and V_{DRV} are common to all phases, while the inputs with an X as subscript are specific for each phase.

5.4.1 Power Supplies

The EPC33110 module only requires an external 5 V power supply via the V_{DRV} pin. The internal low-side and high-side power supplies, which are connected to the V_{DD} and V_{BOOT} pins, are generated from the external power supply via two independent switches, as shown in Figure 5.13.

The internal power supplies can be deactivated to save quiescent power by turning off the series switches Q_{SA} . It can be done by applying 0 V to the $\overline{SD}/STB$ pin. In this chip mode, called standby mode, only a minimum current is drawn from the external V_{DRV} supply, while all three V_{DDx} supplies are open circuits. The charge remaining in the V_{DDx} bypass capacitors is discharged by the quiescent current I_{DRV_Q} required by the internal circuits (typically 30 mA). Then, the V_{DRV} pin draws the standby current $I_{DRV_standby}$ (typical 300 μA). Moreover, the series switches Q_{SA} between V_{DRV} and V_{DDx} are turned off by an internal standby circuit (V_{DDON} drive)

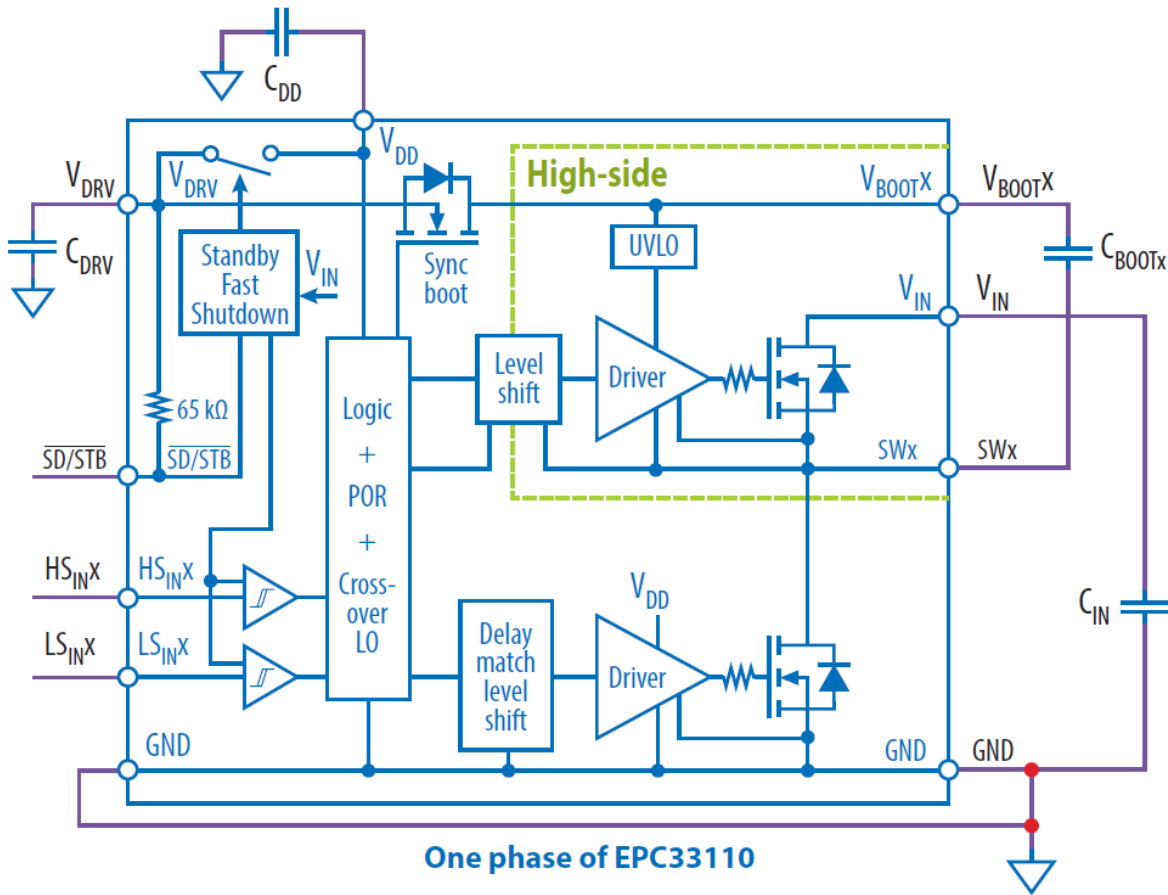


Figure 5.12: Functional Block Diagram of one phase of EPC33110 [37].

shorting the series switches Q_{SA} . In this way, the minimum operating voltage at the V_{IN} pin is reduced down to 0 V ($V_{IN,min,BoostMode}$), which is a mandatory requirement in multi-phase boost converter applications, when DC input voltage applied to SWx pin is lower than 13.5 V [37]. In Figure 5.13, the series high-voltage synchronous bootstrap FETs, Q_{SB} , are also present and are connected between V_{DDx} and V_{BOOTx} . To avoid overcharging during dead time, each high-side floating bootstrap supply is activated only after the respective LS FET (Q_2) is turned on. In addition, by using a GaN FET as synchronous bootstrap in the charging path of the high-side gate drivers, reverse recovery is eliminated, and power dissipation is reduced, since its dropout voltage is about 100 mV, while a typical Si bootstrap diode features a voltage of 0.6 V. So, with this synchronous charging operation, all V_{BOOTx} nodes have a voltage close the V_{DDx} one, allowing the HS FET gate drive circuits to have similar gate drive current and delay performance as the LS FET gate drive circuits.

5.4.2 POR

As shown in the functional block diagram, the EPC33110 integrates both driver protection circuits and POR (Power-On-Reset) circuits for V_{DDx} and V_{BOOTx} . In Figure 5.14, the operation guaranteed by the POR circuits is summarized, ensuring proper driver operation regardless of the power-supply sequencing of V_{DRV} with respect to V_{IN} .

The POR circuit for the low-side internal V_{DDx} supply activates all the HS and LS logic paths

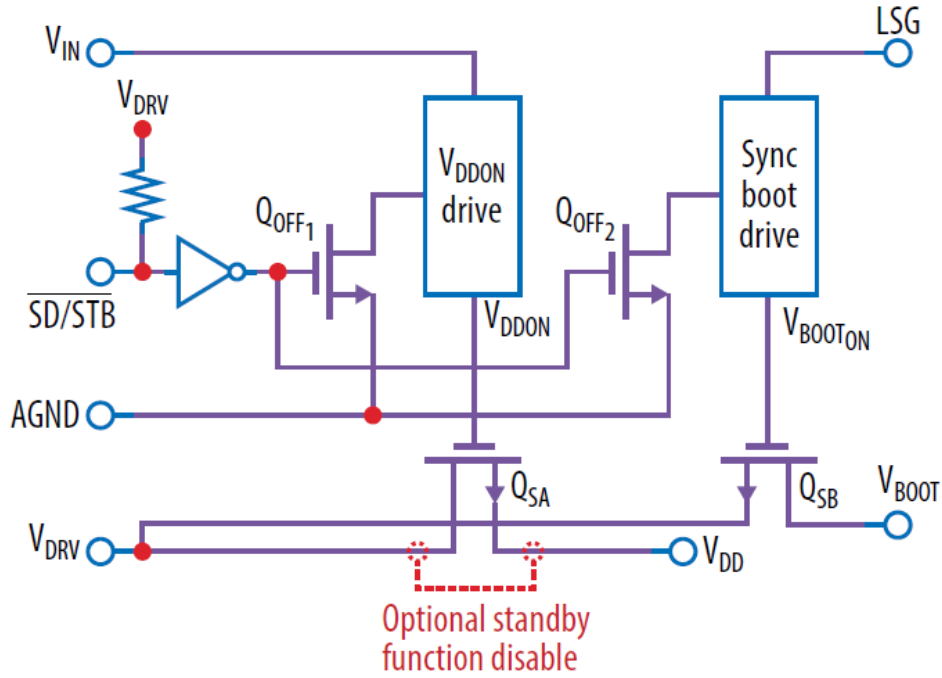


Figure 5.13: Simplified circuit diagram of the EPC33110 power supplies (only one phase is shown) [37].

only when each V_{DDx} voltage rises above the rising threshold V_{DD_POR+} (maximum 4.25 V). When the V_{DDx} voltage falls by $V_{DD_POR_HYST}$ (typically 0.15 V) below the rising supply voltage threshold, the logic paths are deactivated.

Similarly, the POR circuit for the high-side internal V_{BOOTx} supply activates the HS driver path only when each V_{BOOTx} voltage rises above the rising threshold V_{BOOT_POR+} (maximum of 4.25 V). When the V_{BOOTx} voltage falls by $V_{BOOT_POR_HYST}$ (typically 0.15 V) below the rising-supply-voltage threshold, the HS driver path is deactivated.

Obviously, when the SD/STB pin is pulled down, both HS and LS FETs are switched off or remain off regardless of the input pins' state, since the standby/fast shutdown function has been triggered.

SD/STB	V_{DDx}	$V_{BOOTx} - SWx$	HS _{INx}	LS _{INx}	HS FET Phase x	LS FET Phase x
Low ⁽¹⁾	–	–	–	–	OFF	OFF
High	$<V_{DD_POR}$	$<V_{BOOT_POR}$	–	–	OFF	OFF
			–	0	OFF	OFF
	$>V_{DD_POR}$	$>V_{BOOT_POR}$	–	1	OFF	ON
			0	0	OFF	OFF
			0	1	OFF	ON
			1	0	ON	OFF
			1	1	OFF	OFF

(1) SD/STB immediately inhibits PWM inputs when pulled low.

Figure 5.14: EPC33110 truth table for the POR circuits [37].

5.4.3 Gate Drivers

In Figure 5.15, the simplified circuit diagram of the gate-driver output stage for one phase is shown. This is valid for all three integrated HS and LS FET gate drivers, which feature low-impedance, high-pulse-current push-pull n-FET output stages. The gate drive voltage levels for the LS driving circuit are derived from the internal low-side V_{DDx} power supplies, while for the HS driving circuit, they are derived from the internal high-side V_{BOOTx} power supplies. An internal driving circuit has been specifically designed to turn on M_{PO} while simultaneously ensuring that the gate-drive level Q is sufficiently close to both V_{DDx} and V_{BOOTx} . The operation of M_{PO} and M_{SO} is very similar to the half-bridge power stage composed of the Q1 and Q2 output FETs, except for the fact that all the circuitry is internal to the IC.

C_{B1} denotes the internal capacitors used in all six gate-driving circuits. Since this capacitor is not yet fully charged at initial power-up, the propagation delay from HS_{INx} or LS_{INx} to SWx may increase by up to 250 ns, but this may affect only the first one or two pulses.

Moreover, since each gate driver output Q can reach 100% duty cycle thanks to a specific design or the internal driving circuit, the PWM input pulse width for all six output GaN FETs has no maximum boundaries, as long as V_{DDx} and V_{BOOTx} are above the power-on reset threshold limit. Finally, the high-side circuit V_{BOOTx} can alternatively be supplied by an external floating voltage in place of the bootstrap capacitors, thereby allowing infinite ON time for the high-side FET.

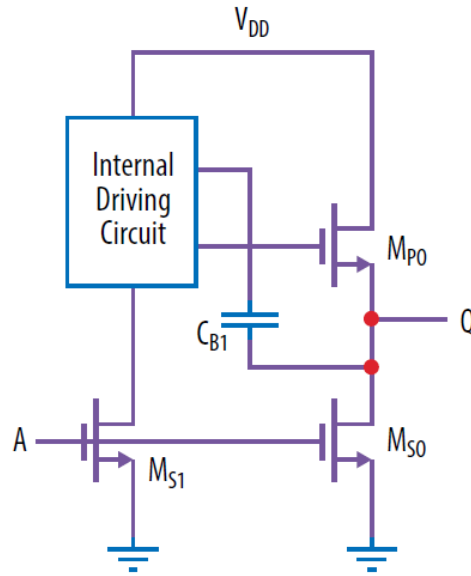


Figure 5.15: Simplified circuit diagram of the EPC33110 gate driver output stage [37].

5.4.4 Logic Inputs

The EPC33110 supports interfacing with digital and analog controllers at both 3.3 V and 5 V standard CMOS logic levels. It is obtained thanks to the integrated logic-level translators placed at the frontend, which level-shift the six PWM signals (HS_{INx} and LS_{INx}) to the appropriate internal voltage levels. In addition, the high-side and low-side logic control inputs are separate and independent, allowing external controllers to set fixed or adaptive dead times to maximize operating efficiency.

When the phase logic inputs are wrongly set simultaneously high, the integrated cross-conduction

lockout logic designed for each phase turn-off both FETs, avoiding the shoot-through condition. Figure 5.16 shows the input-to-output timing diagram of the HS FET Q1 and LS FET Q2 in a half-bridge configuration, with current considered positive as it exits the half-bridge. This illustrates the interactions between the logic inputs of one phase. In fact, when the input signals HS_{INx} and LS_{INx} are driven high simultaneously, both Q1 and Q2 are immediately turned off by the cross conduction lockout logic. Consequently, the output current commutes to Q2 in 3rd quadrant conduction, and so SW is clamped at the negative V_{SD} voltage of Q2, if the current sign is positive, otherwise the current will pass in Q1 and SW will be clamped at V_{in} plus the positive V_{SD} voltage of Q1. As soon as the cross-conduction condition is removed, the turn-ON signal is sent to the respective power FET gate after a built-in $t_{lockout}$ delay (typically 5 ns). Input filters have been added to the PWM inputs HS_{INx} and LS_{INx} to reduce high-frequency noise. They have been designed with a cut-off frequency that, if the input pulses are smaller than t_{Filter} (typically 15 ns), they do not pass through the filter and so do not propagate to the respective power FET gates. The typical minimum pulse width (PW_{min}) after which the filter does not affect the input pulses is 30 ns.

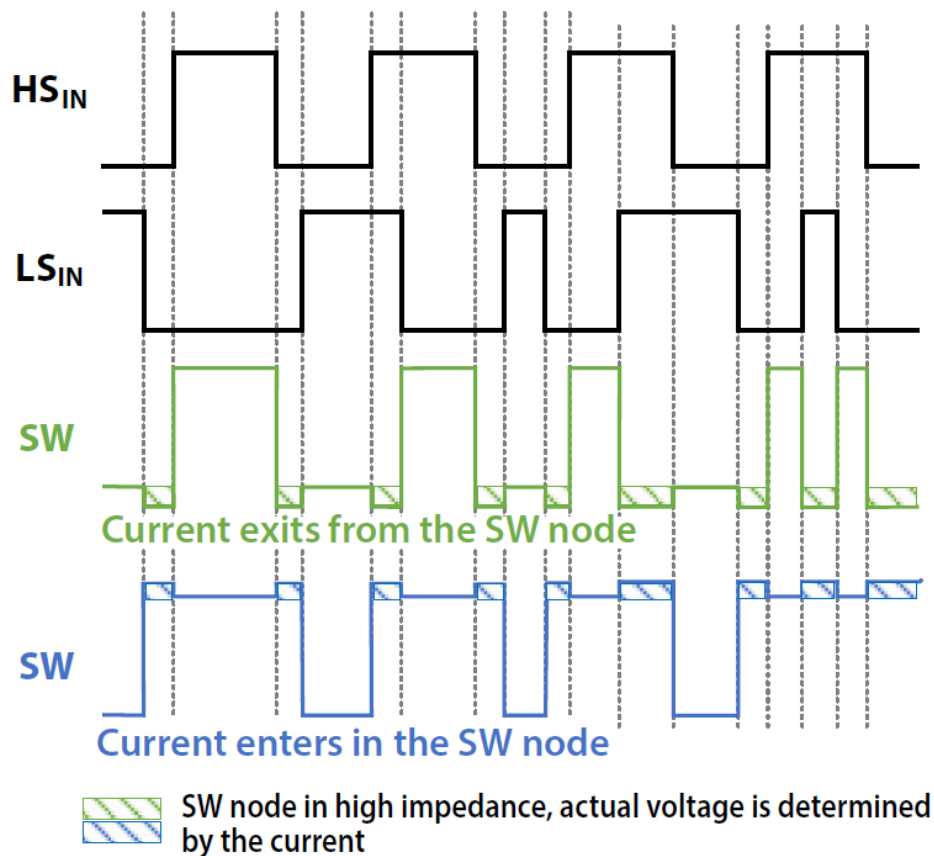


Figure 5.16: EPC33110 input-to-output timing diagram [37].

Chapter 6

Preliminary Analysis on Two Commercial Integrated Motor Drives

6.1 LKTECH MG8008E-i9 V3 Specification

6.1.1 Manufacturer's Information

The first commercial integrated motor drive that will be used as a reference during the design of the evaluation inverter board with the EPC33110 is the MG8008E-i9 V3 servomotor from LKTECH [39]. From the manufacturer's information, it can be retrieved that this motor is a Permanent Magnet Synchronous Motor (PMSM) with an exterior rotor, and as can be seen in Figure 6.1, it is equipped with a driver placed on its back. It features a UART interface, along with a CAN and RS485 interface, guaranteeing multiple communication control handling. For obtaining higher output torque values needed in servomotor applications, such as for humanoid robot joints, the motor is equipped with a 1:9 planetary reducer. The position sensing is performed using two magnetic encoders, since two magnets are installed on the motor's endshaft (Figure 6.2): an 18-bit magnetic encoder for the central magnet, which is directly attached to the exterior rotor; a 14-bit magnetic encoder for the side magnet, which is linked to the planetary reducer. The combination of the two magnetic encoders gives an equivalent 16-bit absolute encoder, which allows only one calibration when the driver is mounted on the motor, since the zero position is never lost, even after the power is removed from the driver.

In Table 6.1 are reported the main parameters of the MG8008E-i9 V3 servomotor declared by the manufacturer, which will be useful in outlining the power requirements needed by the evaluation inverter board with the EPC33110. Some of them have also been experimentally verified to be sure of their correctness, since they have to be inserted inside the motor control firmware when the evaluation board is tested with this motor.

6.1.2 Reverse Engineering

The inverter board included in the MG8008E-i9 V3 servomotor is named DG60RC7-1 V2.4 [39]. Since no documentation is available, this board has been deeply analyzed to understand what

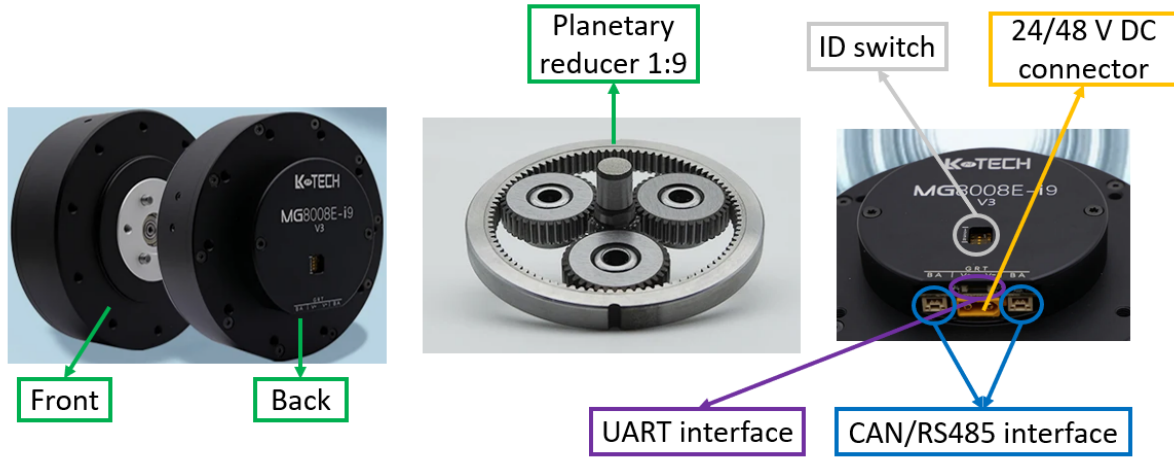


Figure 6.1: MG8008Ei9-V3 images from the manufacturer.

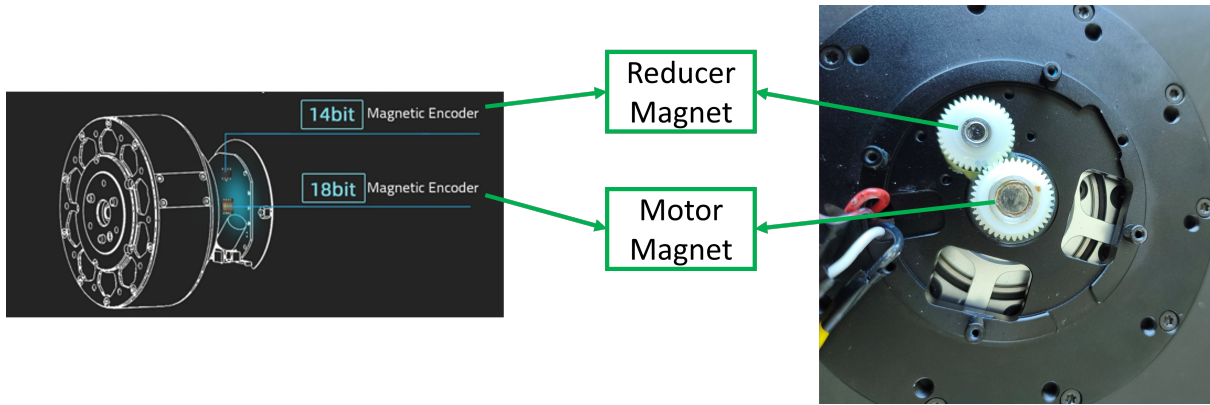


Figure 6.2: MG8008Ei9-V3 position sensing implementation.

Table 6.1: MG8008E-i9V3 motor parameters from the manufacturer [39].

Parameter	Value	Value	Unit
Rated Voltage	24	48	V
Rated Current	4.6	4.9	Arms
Rated Torque	9	10	Nm
Rated Speed	78	178	RPM
Maximum Torque	20	20	Nm
Maximum Speed	112	220	RPM
Maximum Output Power	96	330	W
Speed Constant	42	41.4	RPM/V
Torque Constant	0.22	0.23	Nm/Arms
Phase to Phase Resistance	0.74	0.74	Ω
Phase to Phase Inductance	590	590	μH

components have been used and what solutions have been adopted to realize the integrated motor drive suited for the MG8008E-i9 V3 servomotor. First of all, the board's mechanical dimensions are shown in Figure 6.3: its PCB outline is a circle of 58 mm in diameter delimited by a 50 x 55 mm rectangle, while the power stage's components (power switches + leg shunts) are placed inside an 18 x 33 mm rectangle.

In Figure 6.4, all the main components of the inverter board are pointed out:

- 3x low-side and 3x high-side power MOSFETs from Infineon; OptiMOS™5 Power-Transistor (80 V, 3 m Ω).
- 1x 3-phase bridge driver from Fortior Tech; FD6288T&Q.
- 1x power MOSFET for brake resistor control from Infineon; OptiMOSTM5 Power-Transistor (80 V, 3 m Ω).
- 3x 5 m Ω leg shunts for the current sensing.
- 1x microcontroller from STMicroelectronics; STM32F446RCT6 (LQFP64).
- 1x 18-bit magnetic encoder from MagnTek; MT6825.
- 1x 16-bit magnetic encoder from MagnTek; MT6816.
- 2x 180 μ F DC-link aluminum electrolytic capacitors from LKM.
- 1x Crystal oscillator used by the microcontroller.
- 1x Motor temperature sensor.

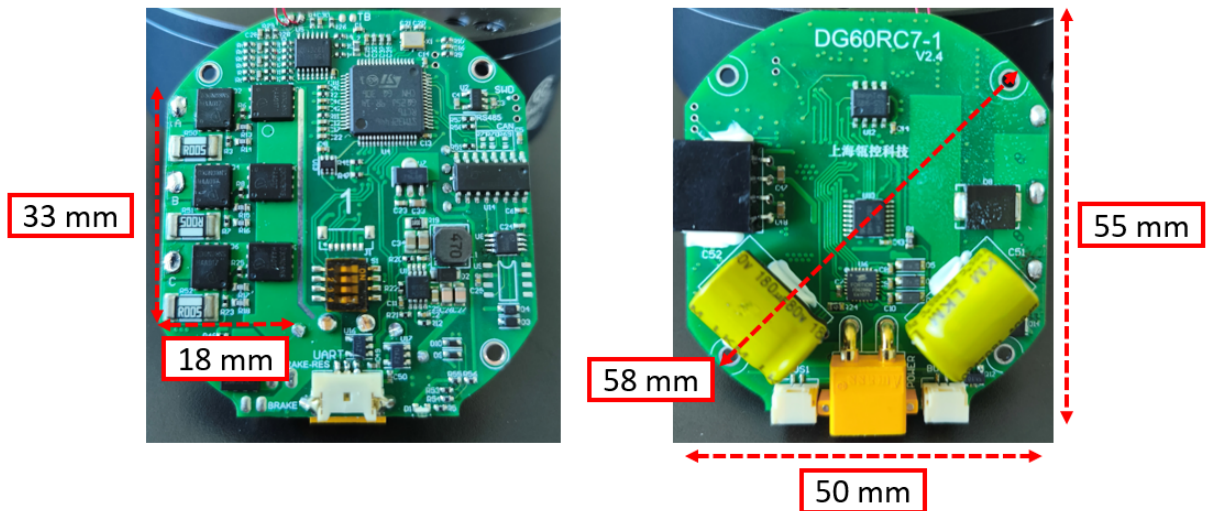


Figure 6.3: MG8008Ei9-V3 inverter board mechanical sizing.

Then, some measures on the motor are carried out. The actual phase resistance is measured using the 4-wire mode of a digital multimeter, while an estimation of the phase inductance is retrieved from the measurement of an LCR meter, computing an average value among the various results obtained, considering all the three-phase combinations, along with different rotor

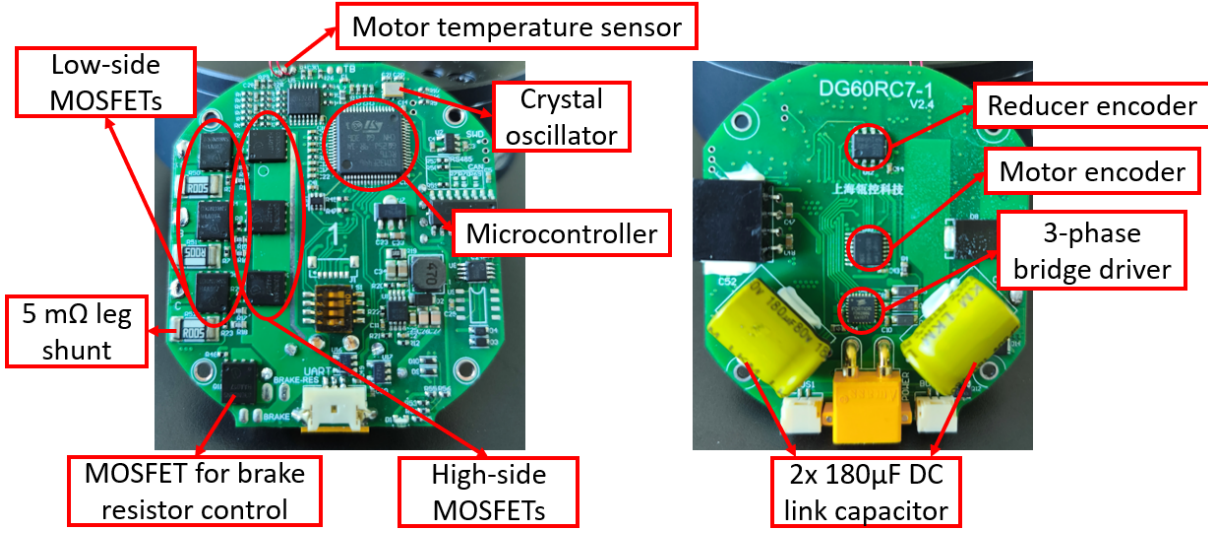


Figure 6.4: MG8008Ei9-V3 inverter board main components identification.

positions, even though the motor showed a negligible saliency, as it features surface-mounted magnets. The pole pairs are determined by counting the number of line-to-line voltage peaks when the rotor is rotated one full rotation by hand.

The line-to-line BEMF constant is computed from the measurement of the line-to-line voltage (with motor phases in open circuit), rotating the rotor by hand (Figure 6.5), using the following formula:

$$K_{e,l-l} = \frac{A_{pp}}{2 \cdot \sqrt{2}} \cdot \frac{1000 \cdot pp}{60} \cdot (2 \cdot T_{half}) \quad \left[\frac{V_{rms}}{kRPM} \right]$$

From this value, the torque constant can be estimated without considering motor losses, and the presence of the motor's planetary reducer:

$$K_t = K_{e,l-l} \cdot \frac{\sqrt{2}}{\sqrt{3} \cdot 1000} \cdot \frac{60}{2\pi} \cdot \frac{3}{2} \cdot \sqrt{2} \quad \left[\frac{Nm}{Arms} \right]$$

To measure parameters that characterize the LKTECH driver, software freely available from the manufacturer's website is used to drive the MG8008Ei9-V3 servomotor. The software is called *LingKong Motor Tool V2.36* and offers various motor control options, from torque control to different types of position control [39]. For testing the DG60RC7-1 V2.4 board, the motor was driven in a speed control loop at a fixed speed of 60 rpm, with the DC voltage bus supplied at 24 V. This software is very easy to use because all the parameters needed for performing the motor control are already saved in the microcontroller, along with the firmware. In Figure 6.6, a screenshot from the settings window used during the speed control test is shown, which includes the basic, limits, protection, and PID settings. Some of that can also be changed and saved into the microcontroller before starting the motor control firmware. Regarding the encoder setting (Figure 6.7), most of the information needed by the microcontroller is already saved and cannot be changed; in fact, it has worked correctly during the speed control test, so the encoder window has not been changed at all. The third software window, useful for motor control (Figure 6.8), is used to select the control mode, set references, monitor motor parameters, and start or stop motor motion.

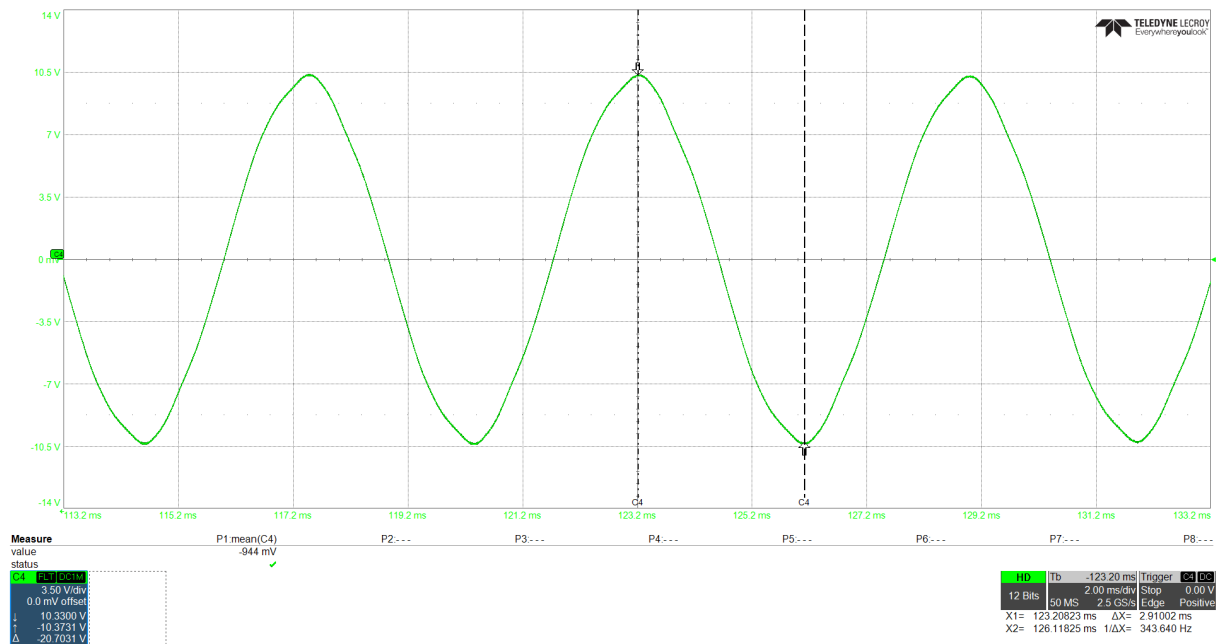


Figure 6.5: Line-to-line voltage measured rotating the rotor by hand.

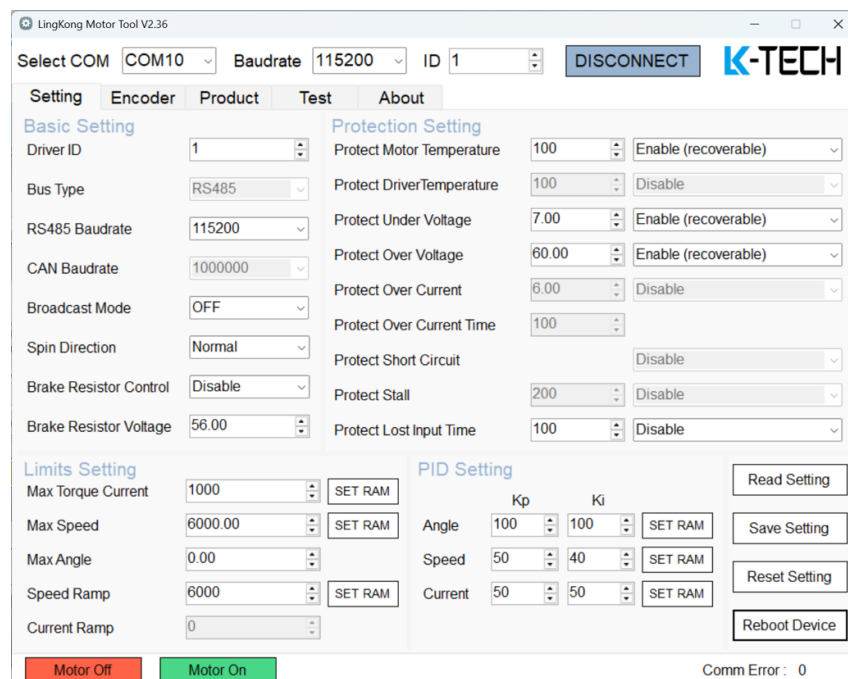


Figure 6.6: LingKong Motor Tool V2.36 setting window.

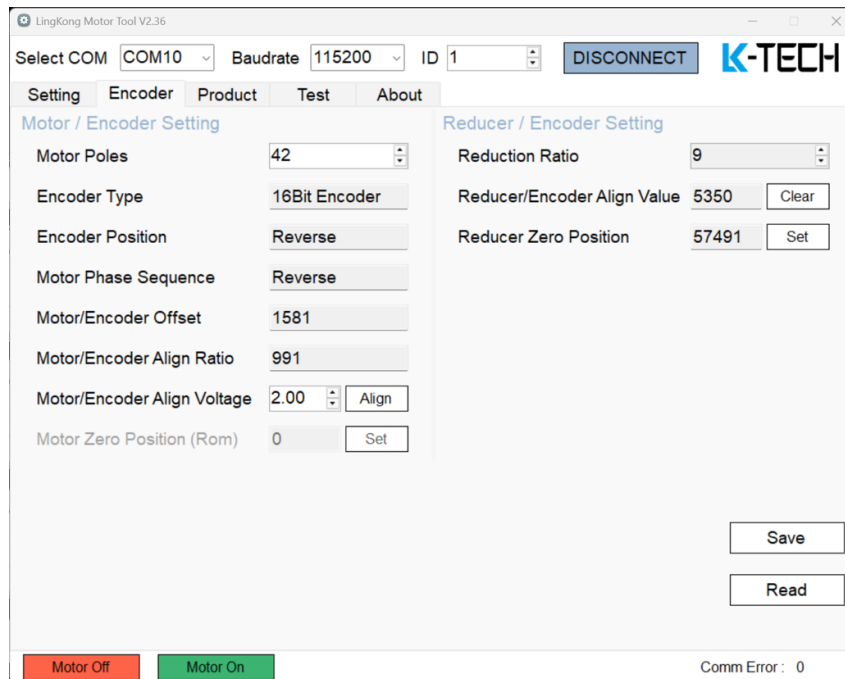


Figure 6.7: LingKong Motor Tool V2.36 encoder window.

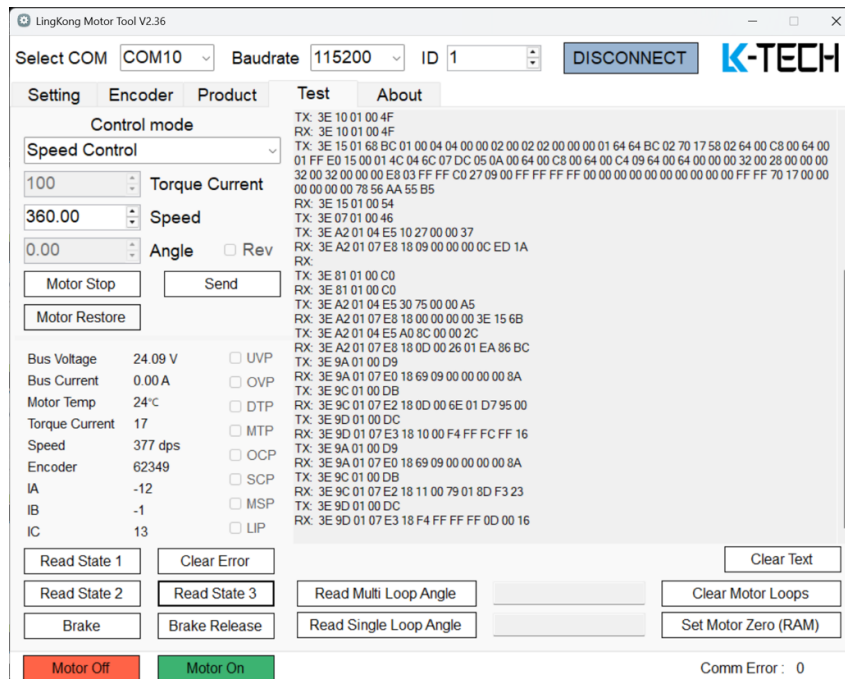


Figure 6.8: LingKong Motor Tool V2.36 test window.

In Figure 6.9, a digital oscilloscope's screenshot is represented during the speed control test. It includes measurements of the three motor phase currents with isolated hall-effect current probes, along with the switching node voltage of phase A and its modulation. In a no-load condition, the motor absorbs only a few tens of mA, but the main information retrieved with this acquisition is the switching frequency used for driving the MOSFETs, which is set at 32 kHz. In Figure 6.10, the gate-to-source voltage used for turning on the power switches is measured across the gate-source terminals of the low side MOSFET of phase A, which is equal 10 V. Figures 6.11 and 6.12 show the turn-on and turn-off transients of phase A high-side and low-side power switches, since their gate-to-source voltages and the switching node voltage were measured with appropriated voltage probes (for the HS v_{GS} was used a differential active voltage probe to reject common mode disturbances to protect the oscilloscope internal circuitry). From these figures, it can be observed that the dead time chosen for driving the MOSFETs is about 700 ns, which is considerably higher than common values used for driving GaN FETs. All the aforementioned measured parameters regarding the motor and the inverter board are summarized in Table 6.2.

Table 6.2: MG8008E-i9V3 motor and driver parameters from the experimental tests.

Parameter	Value	Unit
Phase Resistance	390	m Ω
Phase Inductance	195	μ H
Pole Pairs	21	
BEMF Constant	14.9	V _{rms} /kRPM
Torque Constant	0.2464	Nm/Arms
Gate-to-Source Voltage	10	V
PWM Frequency	32	kHz
Dead Time	700	ns

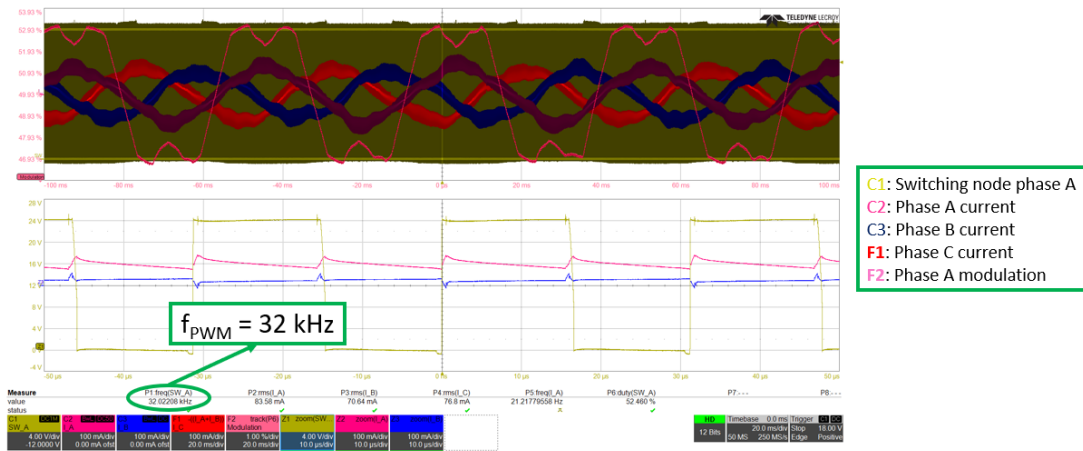


Figure 6.9: Speed control test at 60 rpm and 24V of DC bus voltage.

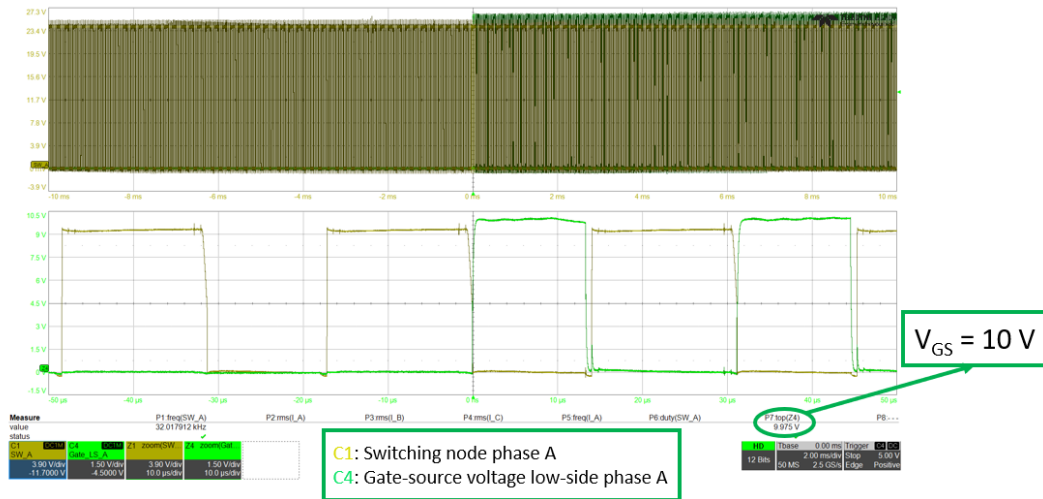


Figure 6.10: Gate-to-source voltage of phase A low-side switch at the startup of the speed control test.

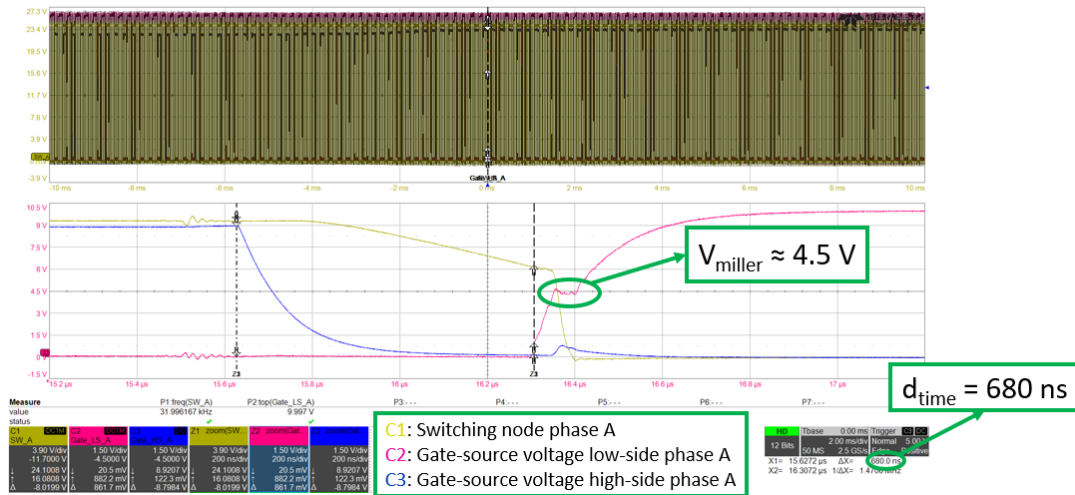


Figure 6.11: Voltage waveforms regarding the LS switch turn-on and HS switch turn-off transients.

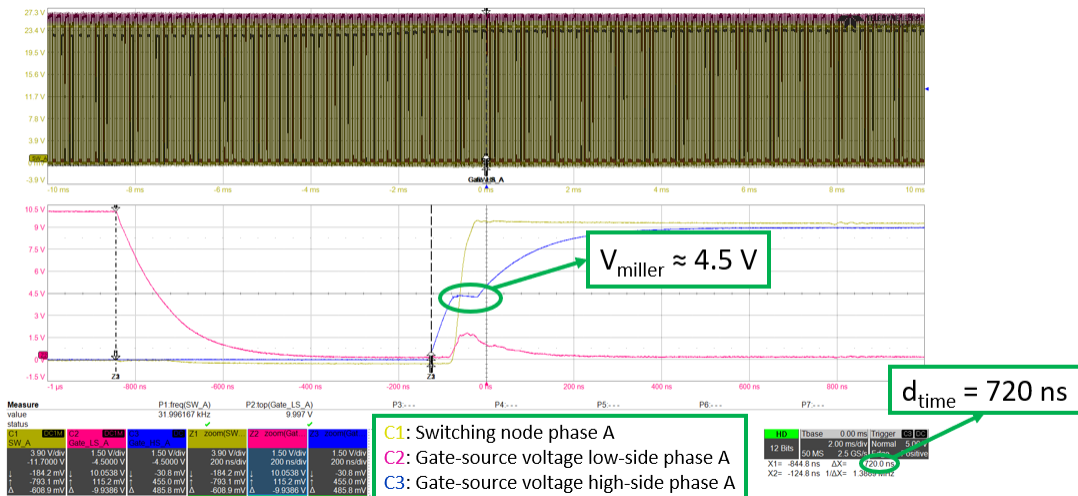


Figure 6.12: Voltage waveforms regarding the LS switch turn-off and HS switch turn-on transients.

6.2 Vertiq 23-06 G1 Module Specification

6.2.1 Manufacturer’s Information

The second commercial integrated motor drive product used as a reference is a module manufactured by Vertiq [40]. The 23-06 G1 Module is designed for industrial sUAS (Small Unmanned Aerial Systems) applications and can be purchased in two variants. The 23-06 220 Kv version, if supplied with the nominal voltage of 24 V, can operate at any speed (at no load) between -4800 and 4800 RPM, while the 23-06 2200 Kv version can reach up to 32000 RPM. The difference between the two motors’ speed range relies on the different speed constant, as suggested by their product name: the 220 KV version has a BEMF constant nearly ten times higher than the 2200 KV, but the latter features a phase resistance nearly 100 times lower, enabling it to reach higher nominal currents than the 220 KV version, but producing the same continuous torque. Both solutions offer a built-in ESC that can deliver up to 30 A and accepts a maximum supply voltage of 30 V, with a position sensor interfaced with a rotor magnet that enables position control (Figure 6.14). As shown in Figure 6.13, the ESC interface comprises the two power supply pads (V+ and V-), the serial UART signal pads (RX and TX) to read/write the control parameters, which can also be used respectively as PWM In and Telem Out, as required by the standard communication protocol of flight controllers in small drones.

In Tables 6.3 and 6.4 are reported the main parameters of the Vertiq 23-06 G1 Module declared by the manufacturer, which will be useful in outlining the power requirements needed by the evaluation inverter board with the EPC33110. Some of them have also been experimentally verified to be sure of their correctness, since they have to be inserted inside the motor control firmware when the evaluation board is tested with this motor.

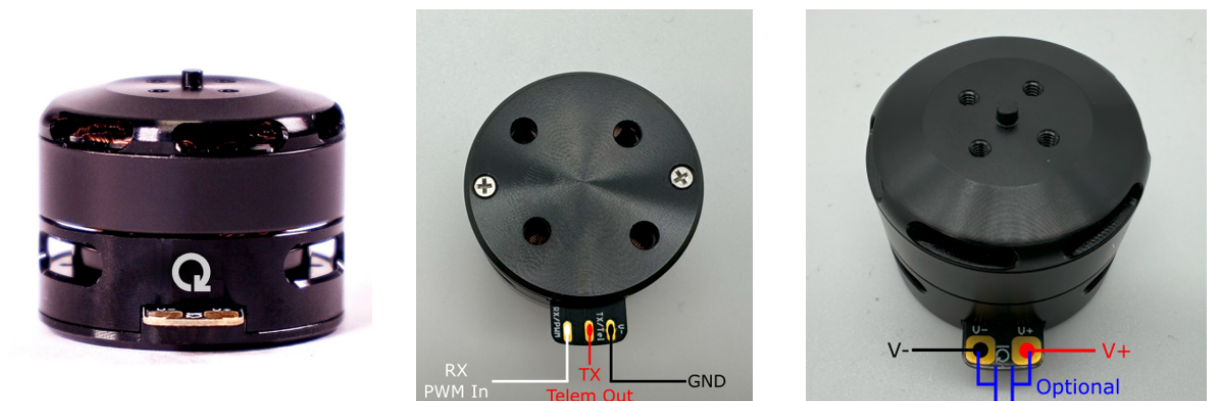


Figure 6.13: Vertiq 23-06 G1 Module photos images from the manufacturer.

6.2.2 Reverse Engineering

The ESC included in both Vertiq 23-06 G1 Modules has been analyzed in a similar way to the DG60RC7-1 V2.4 driver. The Vertiq’s board has a simpler form, but it is much smaller, since its PCB outline is a circle of 26 mm in diameter, in which all the components (power + control) are placed.

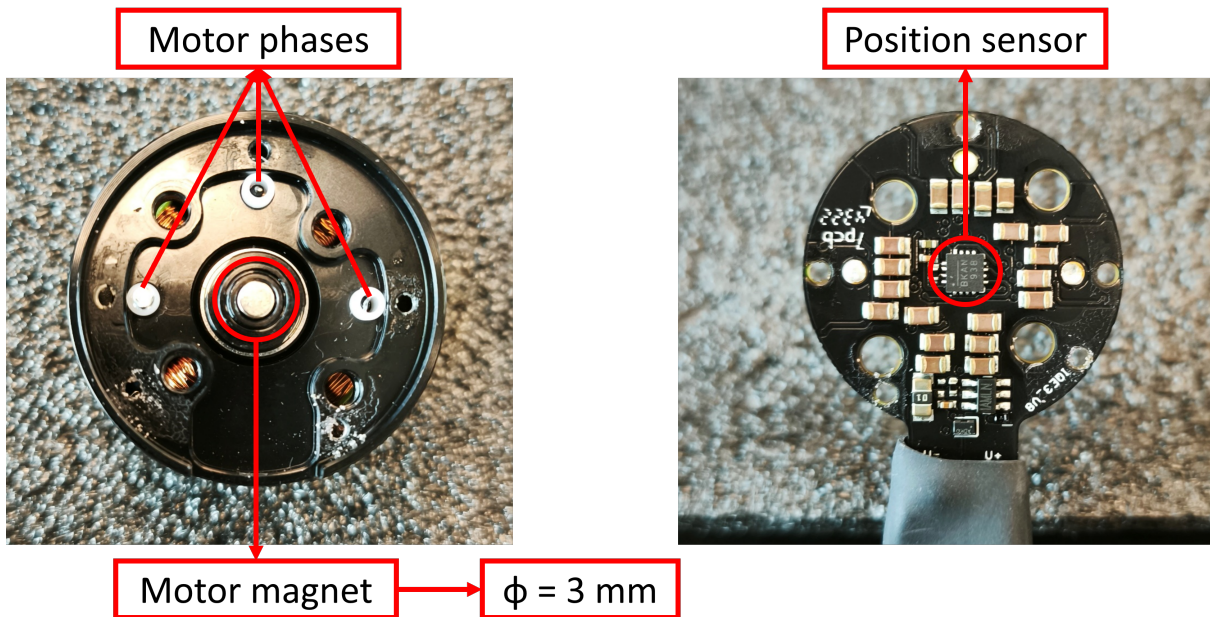


Figure 6.14: Vertiq 23-06 G1 Module position sensing implementation.

Table 6.3: Vertiq 23-06 220 KV motor parameters from the manufacturer [40].

Parameter	Value	Unit
Supply Voltage	5.4 - 24	V
Speed Constant	220	RPM/V
Torque Constant	0.053	Nm/Arms
Phase to Phase Resistance	4.7	Ω
Continuous Torque	0.065	Nm
Continuous Torque in airflow	0.130	Nm
Continuous Current	1.3	Arms
Continuous Current in airflow	2.5	Arms
Pulsed Current	5.3	Arms
Maximum no-Load Speed	4800	RPM

Table 6.4: Vertiq 23-06 2200 KV motor parameters from the manufacturer [40].

Parameter	Value	Unit
Supply Voltage	5.4 - 24	V
Speed Constant	2200	RPM/V
Torque Constant	0.0043	Nm/Arms
Phase to Phase Resistance	0.038	Ω
Continuous Torque	0.065	Nm
Continuous Torque in airflow	0.130	Nm
Continuous Current	15	Arms
Continuous Current in airflow	30	Arms
Pulsed Current	65	Arms
Maximum no-Load Speed	32000	RPM

In Figure 6.15, all the main components of the ESC board are pointed out:

- 3x low-side and 3x high-side power MOSFETs from Alpha & Omega; AON7528 N-Channel AlphaMOS (30 V, 3.4 m Ω).
- 3x dual MOSFET gate drivers from On Semiconductor; NCP81151.
- 1x 1 m Ω DC-link shunt resistor.
- 1x microcontroller from STMicroelectronics; STM32F302K8 (UFQFPN32).
- 1x 14-bit magnetic encoder from MPS; MagAlpha MA330GQ.
- 150 μ F DC-link ceramic capacitors bank.
- 1x Motor temperature sensor.

Then, some measures on both motors are carried out. The actual phase resistance is measured using the 4-wire mode of a digital multimeter, while an estimation of the phase inductance is retrieved from the measurement of an LCR meter, computing an average value among the various results obtained, considering all the three-phase combinations, along with different rotor positions, even though the motor showed a negligible saliency, as it features surface-mounted magnets. The pole pairs are determined by counting the number of line-to-line voltage peaks when the rotor is rotated one full rotation by hand.

The line-to-line BEMF constant is computed from the measurement of the line-to-line voltage (with motor phases in open circuit), rotating the rotor by hand (Figures 6.16 and 6.17), using the formula exposed in the previous section.

To measure some parameters that characterize the Vertiq's ESC, software freely available from the manufacturer's website is used to drive the Vertiq 23-06 220 Kv Module. The software is called *IQ Control Center* and offers various motor control options (speed control, position

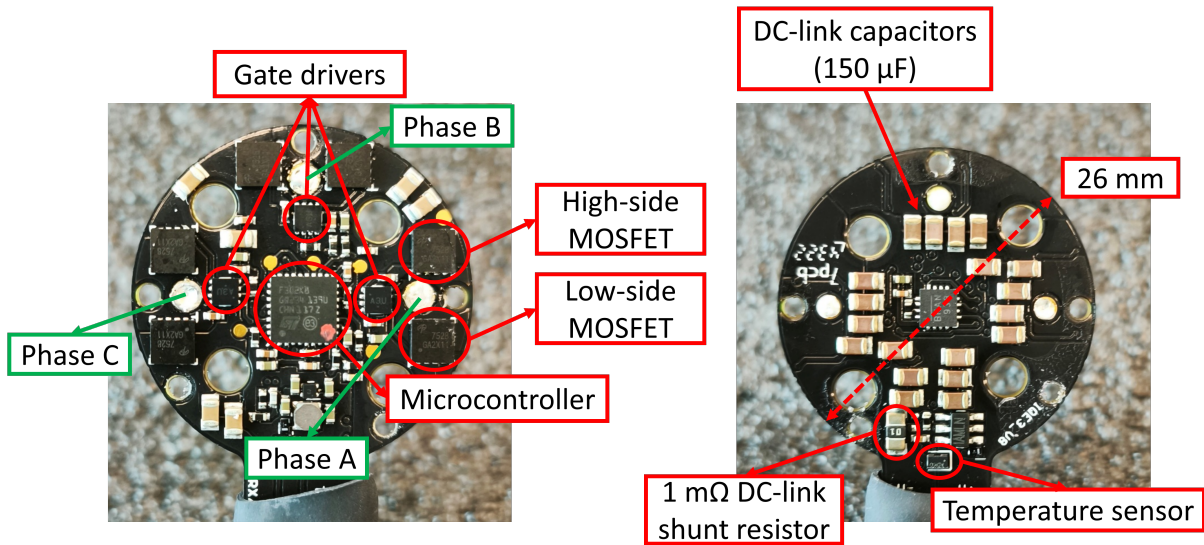


Figure 6.15: Vertiq 23-06 G1 Module inverter board main components identification.

control, PWM open loop voltage, braking, coasting), but also different messaging protocols are supported (IQUART, DroneCAN, PWM, DSHOT) [41]. For testing the ESC board, the motor was driven in a speed control loop at a fixed speed of 5 rad/s (48 RPM), with the DC voltage bus supplied at 12 V. The firmware needed to perform this type of control has been downloaded from the manufacturer's website [40], and flashed into the on-board microcontroller through a USB-to-UART device, selecting the downloaded .bin file in the software's firmware window (Figure 6.18). Since all the control parameters have already been set by the manufacturer, the only software window used to control the motor is the testing window (Figure 6.19), in which the reference speed can be freely chosen in the last row.

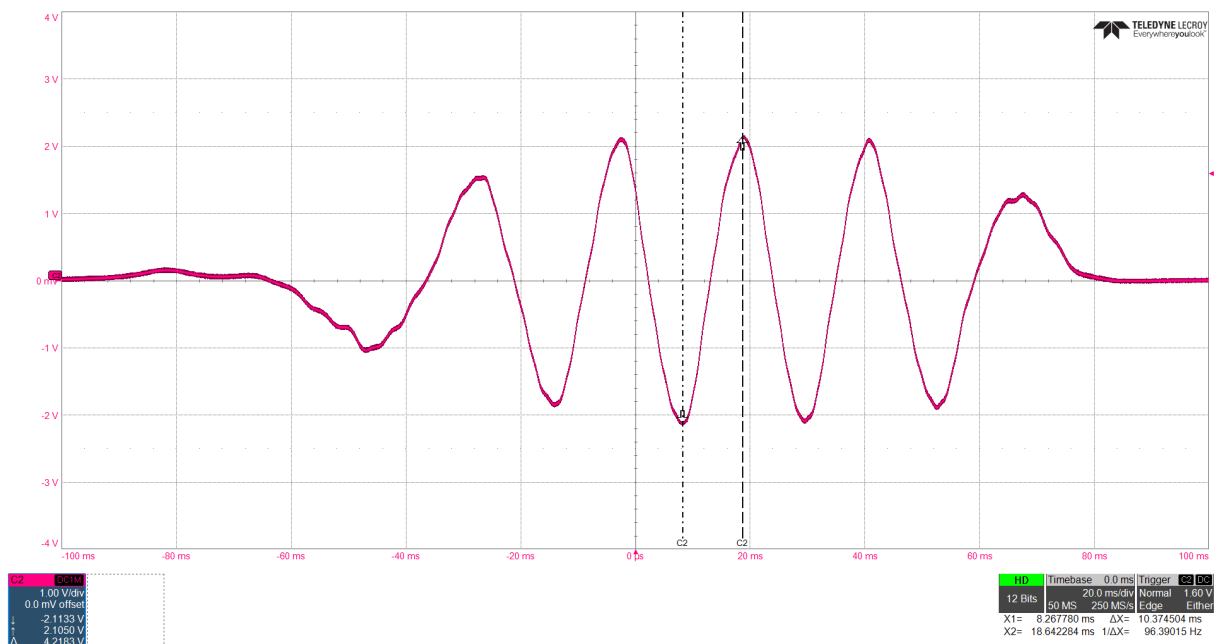


Figure 6.16: Line-to-line voltage measured rotating the rotor by hand (220 KV version).

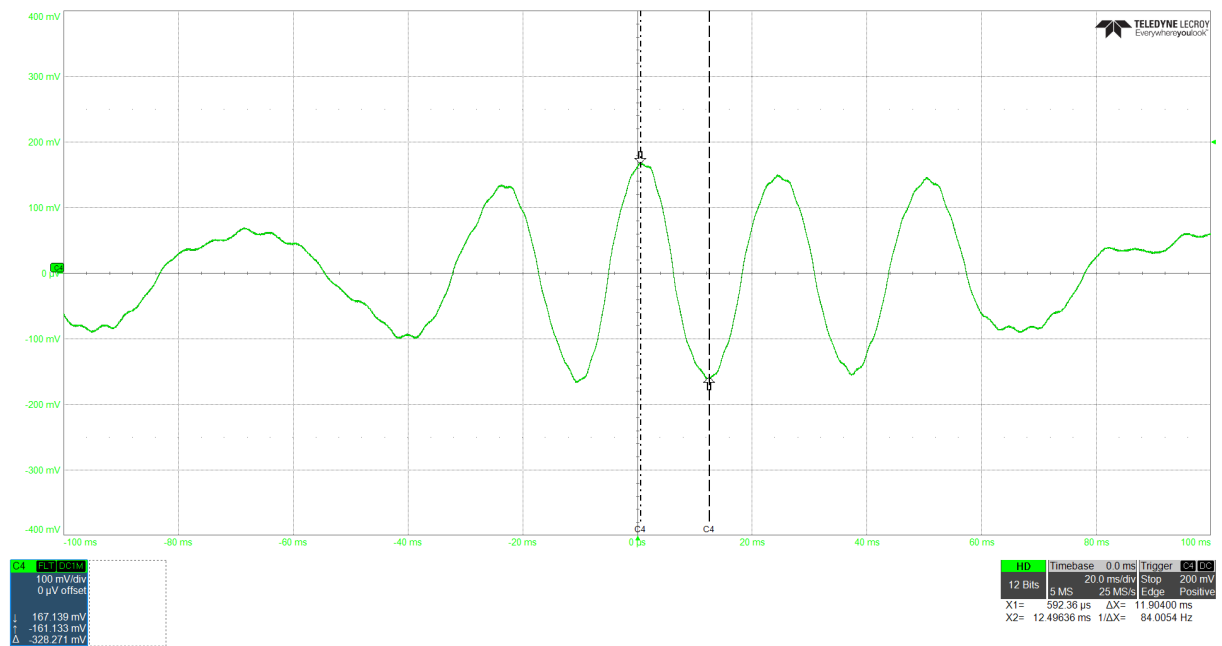


Figure 6.17: Line-to-line voltage measured rotating the rotor by hand (2200 KV version).

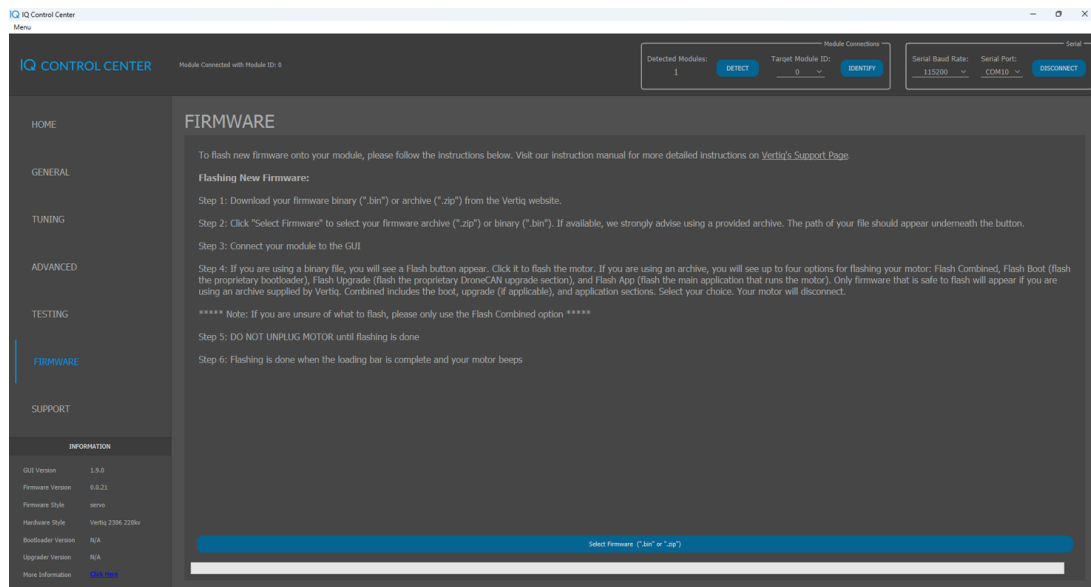


Figure 6.18: IQ Control Center firmware window.

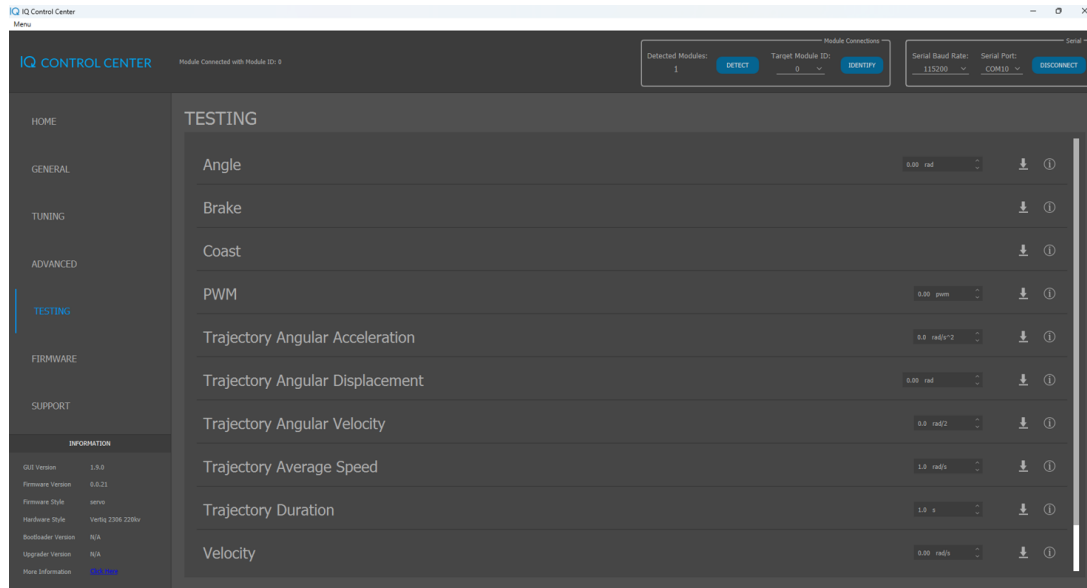


Figure 6.19: IQ Control Center testing window.

In Figure 6.20, a digital oscilloscope's screenshot is represented during the speed control test. It does not include measurements of the three motor phase currents due to the difficulties in accessing the motor's terminals, but the switching node voltage of phase A and the gate-to-source voltage of the phase A low-side MOSFET are measured. From this acquisition, the switching frequency used for driving the MOSFETs has been retrieved, which is set at 22 kHz. In Figure 6.21, the gate-to-source voltage used for turning on the power switches is measured across the gate-source terminals of the low side MOSFET of phase A, which is equal 5 V. Figures 6.22 and 6.23 show the turn-on and turn-off transients of phase A high-side and low-side power switches, since their gate-to-source voltages and the switching node voltage were measured with appropriated voltage probes (for the HS v_{GS} was used a differential active voltage probe to reject common mode disturbances to protect the oscilloscope internal circuitry). From these figures, it can be observed that the dead time chosen for driving the MOSFETs is about 26 ns, which is comparable with common values used for driving GaN FETs. In fact, these power MOSFETs feature better switching characteristics than those used in DG60RC7-1 V2.4 driver, and so they can switch much faster, enabling the reduction of dead time, but showing also some voltage oscillations and overshoots during the transients of both switching node and gate-to-source voltages, because of the presence of parasitic inductances in the PCB layout. All the aforementioned measured parameters regarding the motors and the inverter board are summarized in Table 6.5.

Table 6.5: Vertiq 23-06 G1 Modules parameters from the experimental tests.

Parameter	Value	Unit
Phase Resistance (220KV)	2.4	Ω
Phase Inductance (220KV)	785	μH
Pole Pairs (220KV)	7	
BEMF Constant (220KV)	3.61	Vrms/kRPM
Torque Constant (220KV)	0.0597	Nm/Arms
Phase Resistance (2200KV)	21	m Ω
Phase Inductance (2200KV)	6	μH
Pole Pairs (2200KV)	7	
BEMF Constant (2200KV)	0.322	Vrms/kRPM
Torque Constant (2200KV)	0.0053	Nm/Arms
Gate-to-Source Voltage	5	V
PWM Frequency	22	kHz
Dead Time	26	ns

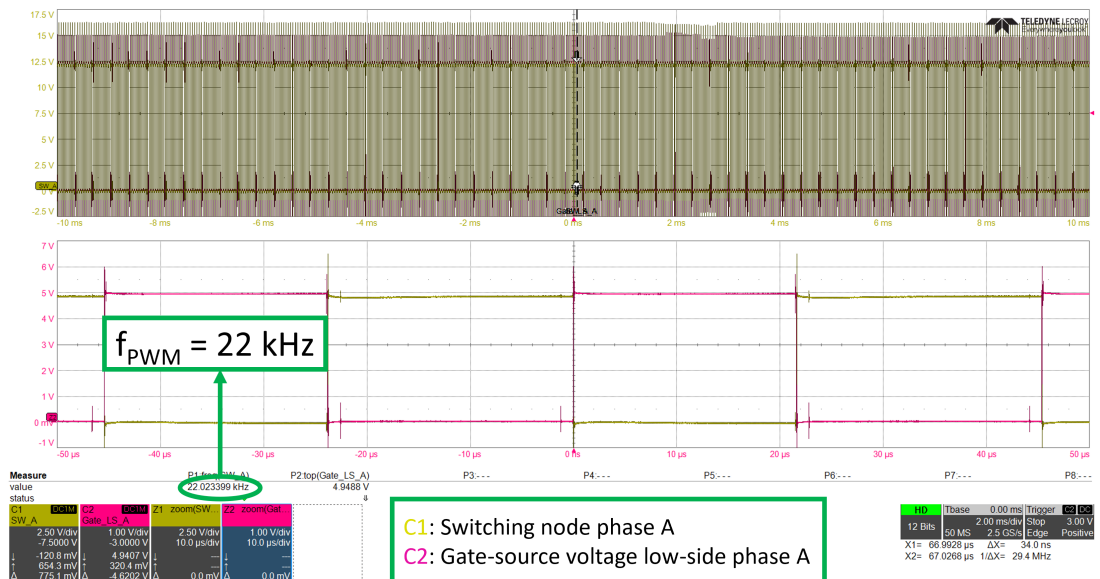


Figure 6.20: Speed control test at 48 rpm and 12V of DC bus voltage.

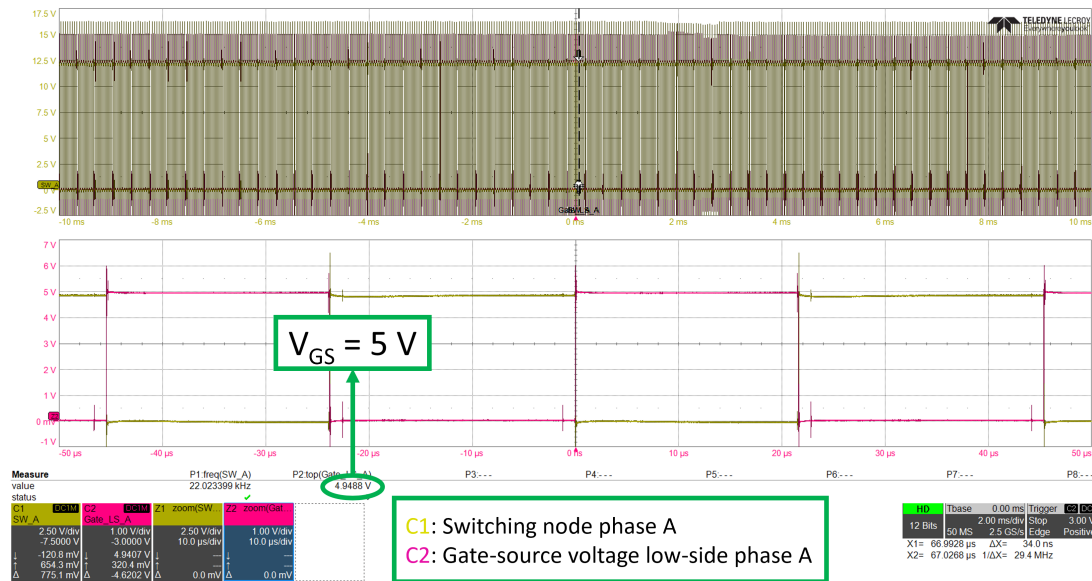


Figure 6.21: Gate-to-source voltage of phase A low-side switch at the startup of the speed control test.

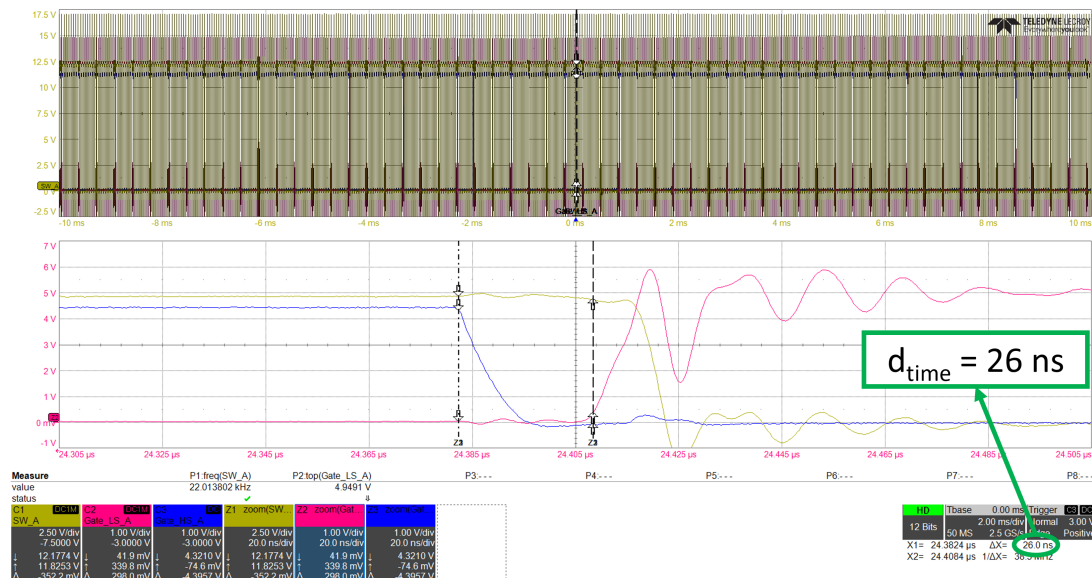


Figure 6.22: Voltage waveforms regarding the LS switch turn-on and HS switch turn-off transients.

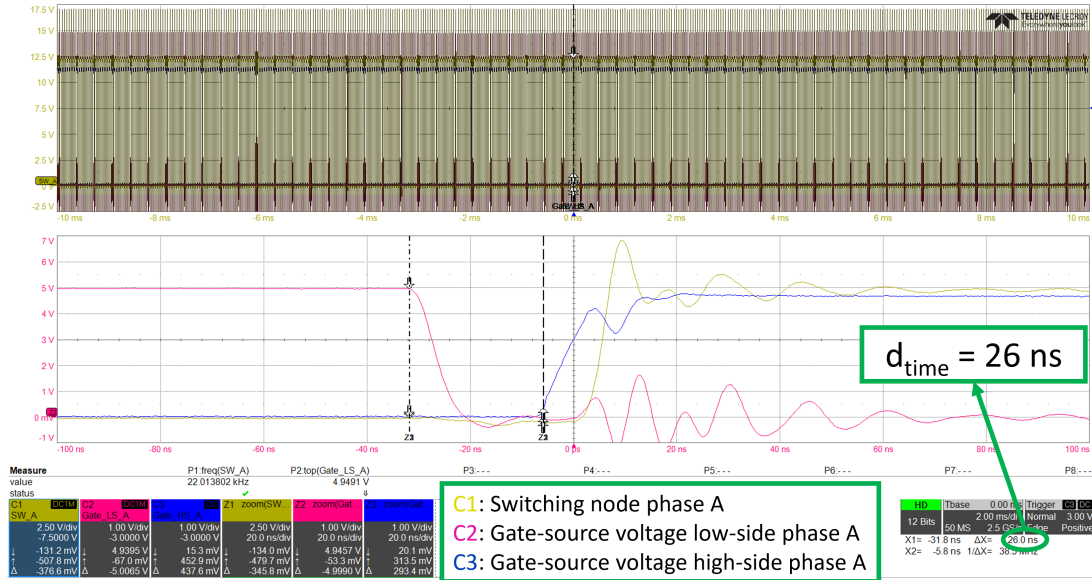


Figure 6.23: Voltage waveforms regarding the LS switch turn-off and HS switch turn-on transients.

6.3 Motors Characteristic Curves

To identify the power requirements needed for driving both motors, their characteristic curves declared by the manufacturer are reported in this section.

6.3.1 MG8008E-i9 V3 Servomotor

For the MG8008E-i9 V3 servomotor, LKTECH provides the motor's characteristic curves at 24 V and 48 V of DC bus supply, before the planetary reducer's effect. Figures 6.24 and 6.26 show the torque and efficiency over the rotor speed, while Figures 6.25 and 6.27 plot the input DC current and the mechanical power. The red lines have been added considering the motor limits included in Table 6.1, which restrict the output torque range at a maximum value of 2.22 Nm for both bus voltage supply values, while the maximum speed is limited at 1008 rpm for 24 Vdc, and 1980 rpm for 48 Vdc. Therefore, the maximum phase current that the motor can withstand is equal to 10 Arms ($K_t = 0.22N/Arms$), while the rated one is about 5 Arms. The maximum output mechanical power that can be extracted from this motor is about 330 W, at 48 Vdc, 1000 rpm, and maximum torque condition. The maximum efficiency (driver + motor) is about 80%, at 48 Vdc, 1750 rpm, and an output torque of 0.75 Nm. Another important consideration is that the maximum speed of 1980 rpm produces a maximum fundamental frequency of the phase voltages equal to 693 Hz, which is sufficiently lower than the current sampling frequency that will be set in the motor control firmware (33.333 kHz), avoiding problems in the current control loop implementation.

6.3.2 Vertiq 23-06 G1 Module

For Vertiq 23-06 G1 Modules, the manufacturer provides different characteristic curves, depending on the DC voltage supply, from 1 V to 24 V. Figures 6.28 and 6.29 show the motor characteristic curves for the 220 KV and 2200 KV versions, respectively, with the rated DC

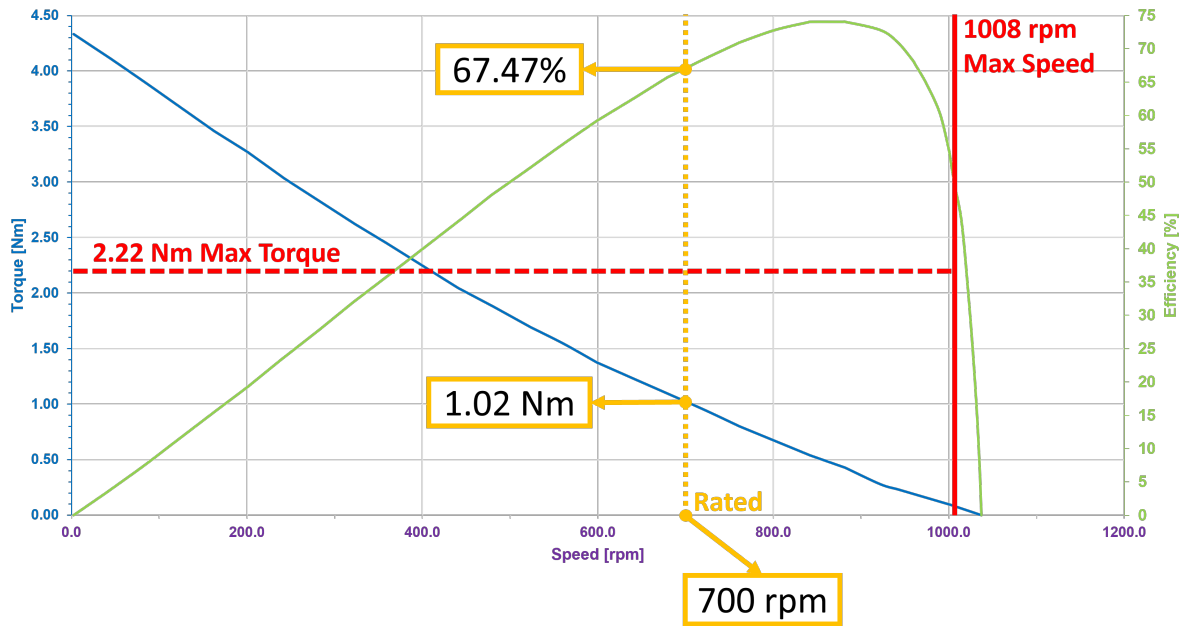


Figure 6.24: MG8008E-i9 V3 characteristic curves at 24 Vdc: torque and efficiency vs. speed.

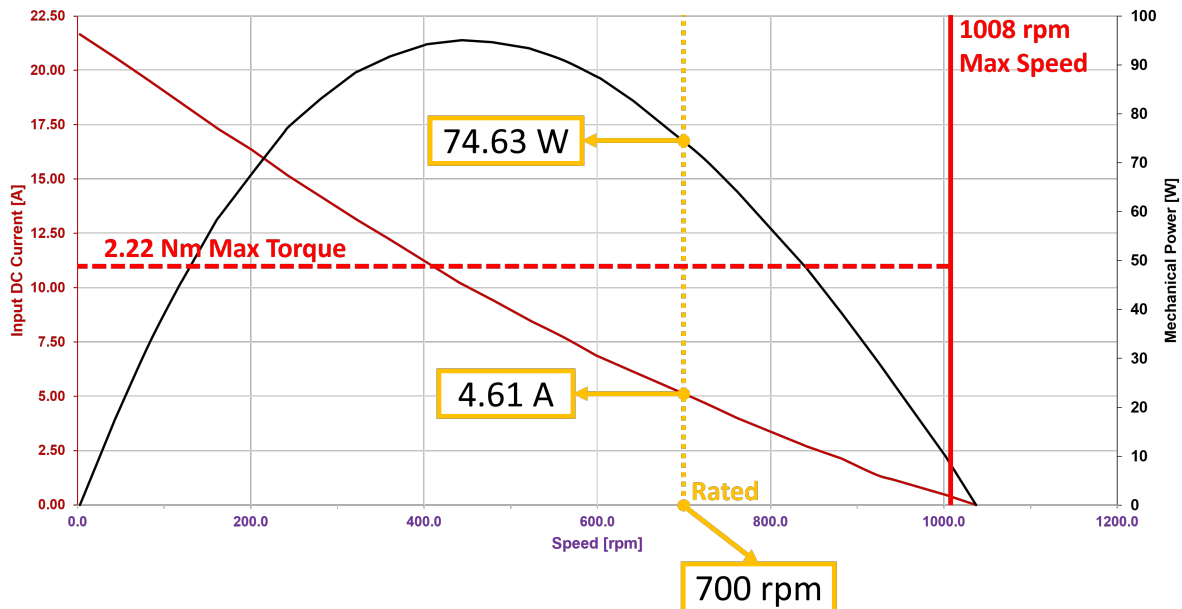


Figure 6.25: MG8008E-i9 V3 characteristic curves at 24 Vdc: input DC current and mechanical power vs. speed.

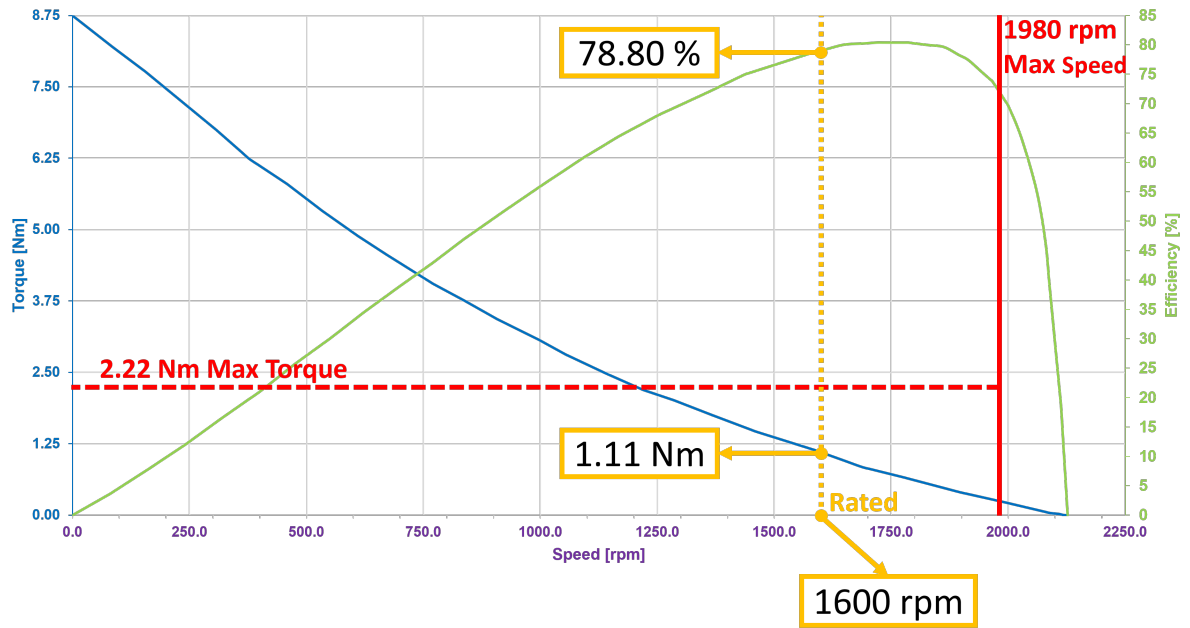


Figure 6.26: MG8008E-i9 V3 characteristic curves at 48 Vdc: torque and efficiency vs. speed.

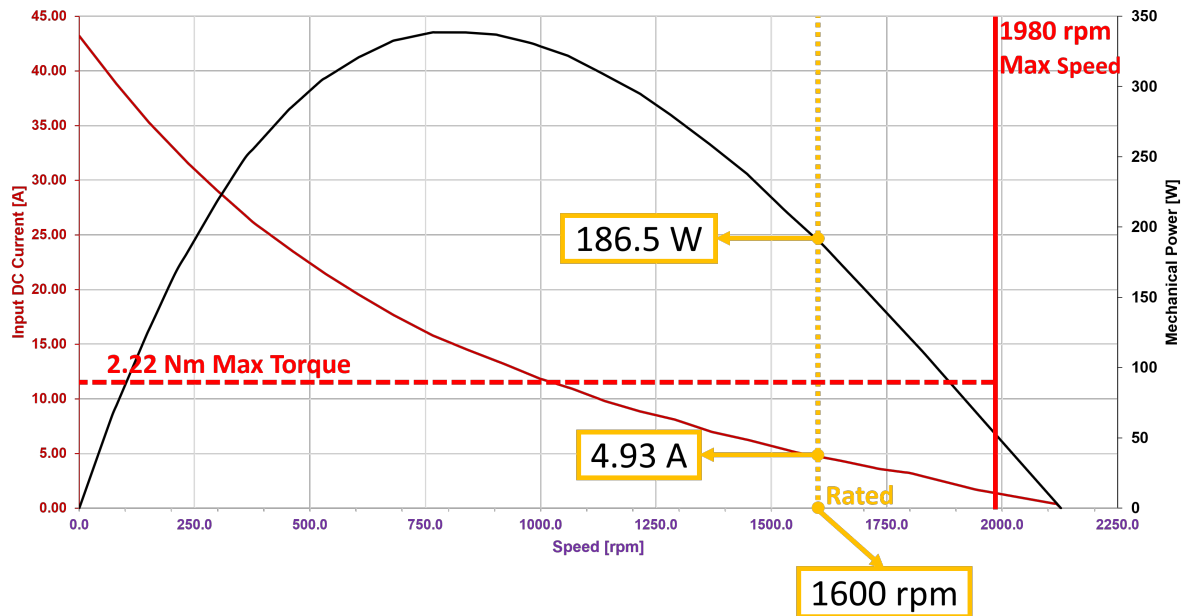


Figure 6.27: MG8008E-i9 V3 characteristic curves at 48 Vdc: input DC current and mechanical power vs. speed.

voltage supply of 24 V. These graphs include rotor speed, mechanical power, and motor efficiency over the output torque. The Vertiq 23-06 220 KV motor can withstand a maximum torque (limited by the red area, which needs an appropriate air flow to cool the motor) of 0.65 Nm, which corresponds to a phase current of 1.23 Arms. Also, the Vertiq 23-06 220 KV motor can withstand the same maximum torque of 0.65 Nm, but the corresponding phase current is 15.1 Arms. The maximum mechanical power delivered by the 220 KV version is about 21 kW at 2800 rpm, while the 2200 KV version can reach up to 320 kW at 25500 rpm. The maximum efficiency for the 220 KV version is slightly higher than 80%, while for the 2200 KV version, it is ideally 85%, but due to the motor overspeed limitations (yellow area) set at 32000 rpm, this condition cannot be reached. The maximum no-load speed achievable with the 220 KV version is 4300 rpm, which corresponds to a maximum fundamental frequency of the phase voltages equal to 502 Hz. Instead, the maximum no-load speed achievable with the 2200 KV version is 52500 rpm, which corresponds to a pretty high maximum fundamental frequency of the phase voltages, which is equal to 6.125 kHz. However, the maximum achievable mechanical speed for the 2200 kV version is limited to 32000 rpm, as said before, so the maximum fundamental frequency of the phase voltages is also reduced to 3.733 kHz, but remains rather high compared to the current sampling frequency of 33.333 kHz. This potential problem can be solved by optimizing the motor control firmware to equal the sampling frequency (and so the frequency of the motor control interrupt service routine) with the switching frequency, which will be set at 100 kHz.

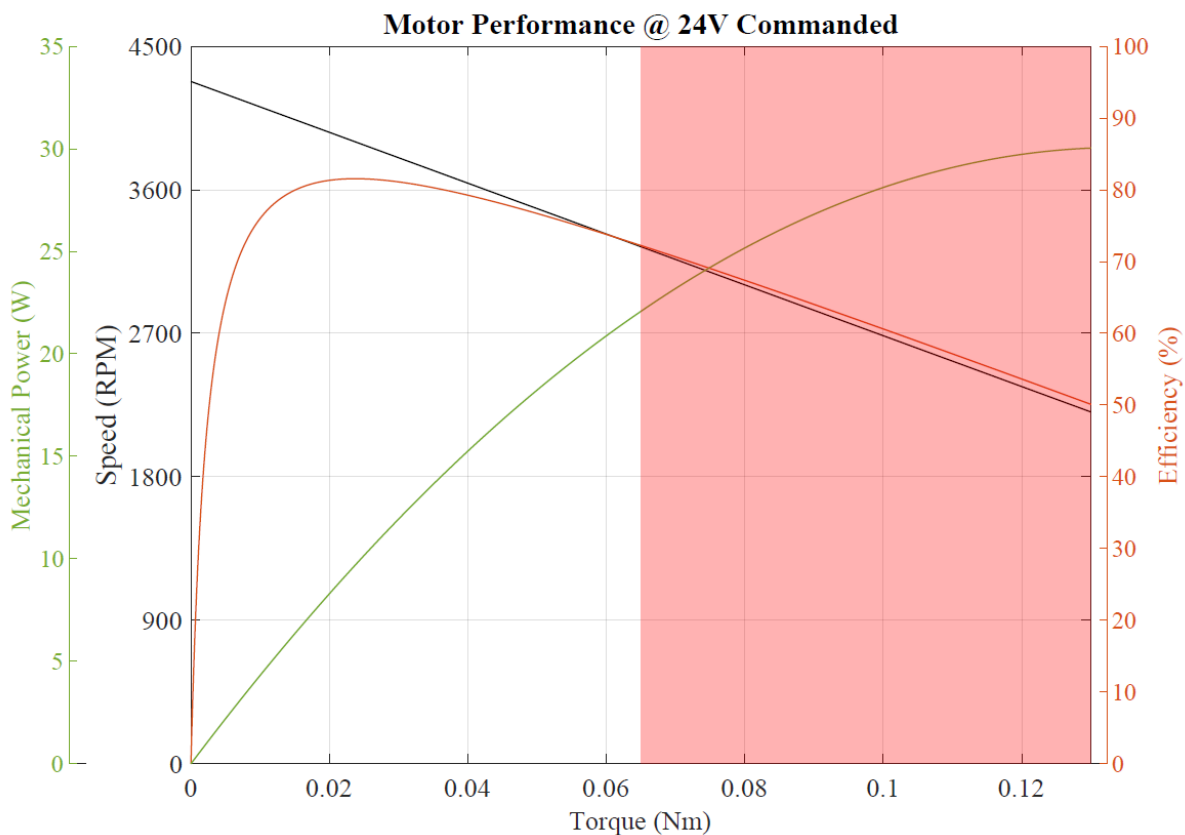


Figure 6.28: Vertiq 23-06 220 KV characteristic curves: speed, mechanical power, and efficiency vs. torque.

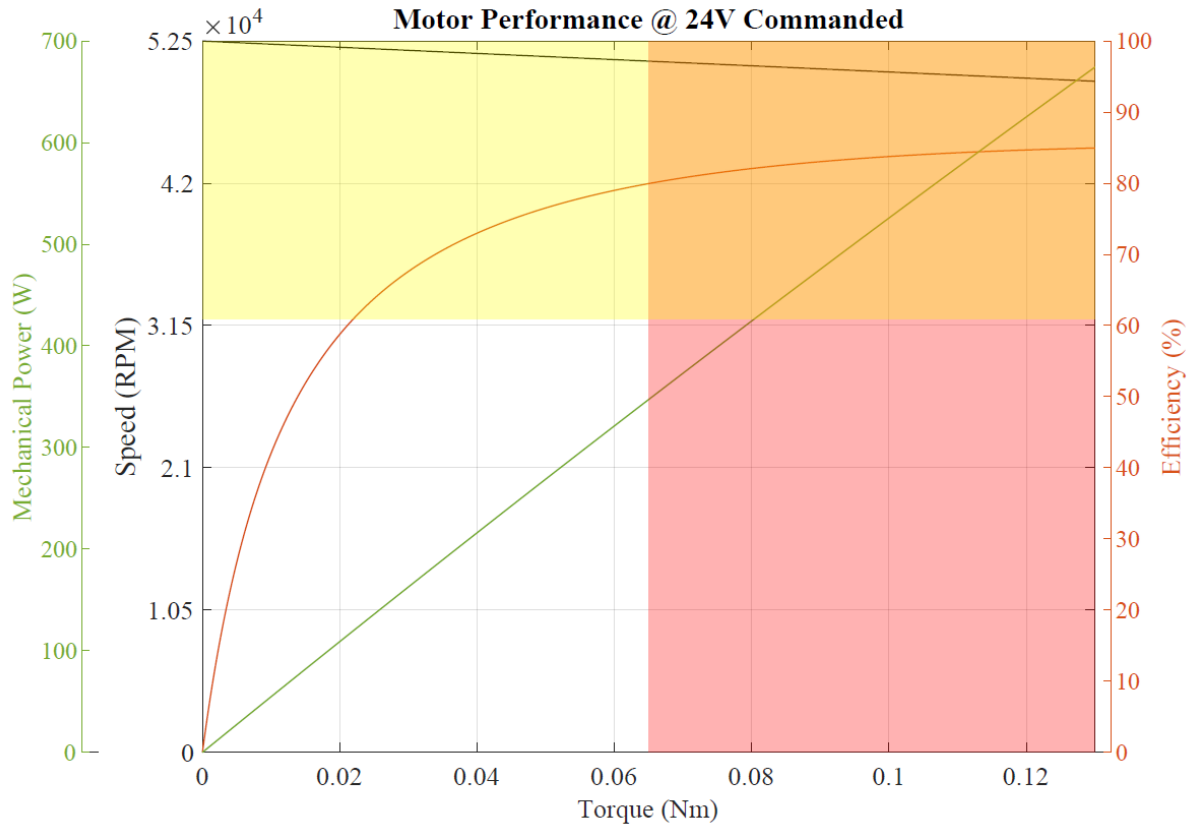


Figure 6.29: Vertiq 23-06 2200 KV characteristic curves: speed, mechanical power, and efficiency vs. torque.

6.4 Mechanical Constraints

The evaluation inverter board EPC91132 has been designed to fit in both the MG8008E-i9 motor and the Vertiq 23-06 G1 Module. Therefore, the first analysis to perform concerns the mechanical constraints that the two motors require, in order to identify the area in which to place the various electronic components, along with the position and diameter of the mounting holes needed to secure the board to the motors' chassis. Since the servomotor and the drone motor have very different mechanical requirements regarding the driver board allocation, the PCB of the evaluation board featuring the EPC33110 has been drawn, giving the possibility of choosing which motor to be driven. In particular, the full-form PCB includes a sort of outer ring that adapts the small-form PCB (based on Vertiq's ESC board) to the MG8008E-i9 motor. This external ring can be easily removed by splitting the PCB in correspondence with the 4 small bridges that mechanically connect the small-form PCB to the outer PCB ring. These bridges are sufficiently weakened by adding some small unplated holes and by minimizing the use of copper. So, the EPC91132 can be fit into the MG8008E-i9 motor as soon as the board has been produced and assembled, while for inserting it into one of the Vertiq modules, the board has to be physically modified in an irreversible way.

In Figures 6.30a and 6.30b are indicated all the fundamental mechanical quotes that have been chosen to draw the PCB outline of the EPC91132 board, respecting all the constraints required by both motors.

The last dimension to respect is the board's thickness. In Figure 6.31, the PCB stackup chosen for designing the EPC91132 is shown, which is composed of six 2oz copper layers, 5 dielectric layers, and two solder masks for the top and bottom sides. The sum of all the layers' thicknesses gives about 0.84 mm. This value is nearly equal to the thickness of the Vertiq's board, which is 0.8 mm, while the DG60RC7-1 V2.4 driver board reaches 1.00 mm. This achievement is really important to fit the small-form PCB of EPC91132 into Vertiq's modules. Moreover, the aforementioned figure also shows the via type used for making the connections among the six copper layers: only through-hole vias have been adopted to reduce the manufacturing costs compared to the blind or buried via types.

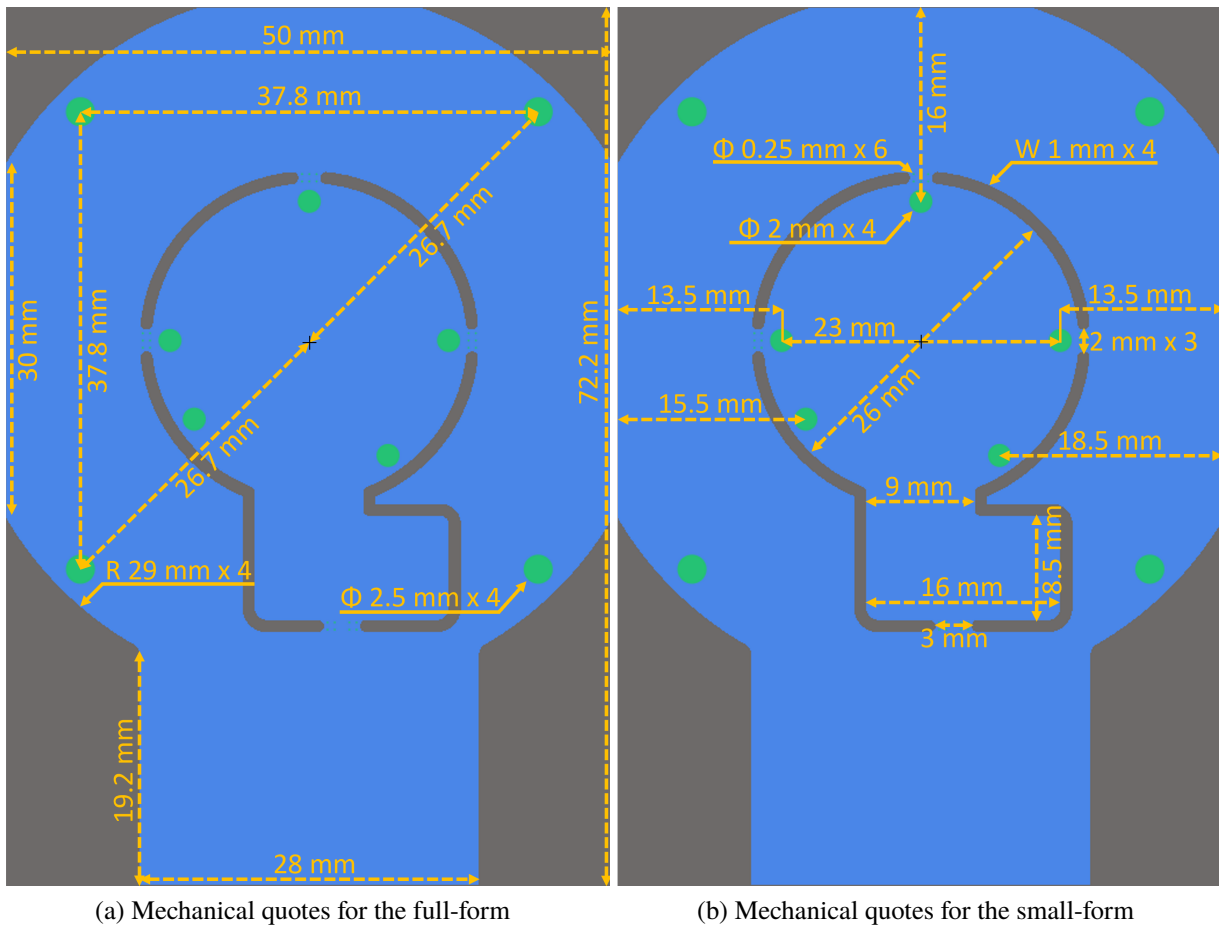


Figure 6.30: EPC91132 PCB outline.

#	Name	Type	Thickness	#	Thru 1:6
	Top Overlay	Overlay			
	Top Solder	Solder Mask	0.709mil		
1	Top Layer	Signal	2.756mil	1	
	Dielectric 1	Core	5mil		
2	Layer 2	Signal	2.756mil	2	
	Dielectric 2	Prepreg	4.016mil		
3	Layer 3	Signal	2.756mil	3	
	Dielectric 3	Core	5mil		
4	Layer 4	Signal	2.756mil	4	
	Dielectric 4	Prepreg	4.016mil		
5	Layer 5	Signal	2.756mil	5	
	Dielectric 5	Core	5mil		
6	Bottom Layer	Signal	2.756mil	6	
	Bottom Solder	Solder Mask	0.709mil		
	Bottom Overlay	Overlay			

Figure 6.31: EPC91132 PCB stackup with via type.

6.5 EPC91132 Functional Block Diagram

Before starting the discussion regarding the design of the inverter board EPC91132, its schematic block diagram is illustrated in Figure 6.32 to identify all the components required by the implemented function of this board.

- **DC link + Connector:** input DC terminals to receive the required voltage from the power supply, followed by a bank of DC bus ceramic capacitors at the interface with the inverter power stage. A voltage divider is interfaced to the microcontroller for sensing the DC bus voltage.
- **On-board power supplies:** DC-DC converters to generate two low voltage rails, for supplying the EPC33110 module with 5.2 V, while current sensors, magnetic encoder, microcontroller, NTC sensor, and RS485 transceiver with 3.3 V.
- **3-phase inverter power stage:** EPC33110 power module for driving the motor according to the PWM signals generated by the microcontroller.
- **Current sensors:** two phase current sensors to provide the motor currents feedback to the microcontroller.
- **Microcontroller + Communication:** a 32-bit microcontroller to perform the FOC motor control in real time. It can be programmed and debugged through a Serial Wire Debug (SWD) interface. The on-board microcontroller can also be accessed through a USART or an RS485 communication interface.
- **Magnetic Encoder:** an absolute magnetic encoder placed close to the rotor magnet to provide the digital signals to the microcontroller, which are used for retrieving the rotor's position. It can be accessed by the microcontroller through an SPI interface for configuration purposes and for reading the angle. The angle can also be computed by sensing the three signals ABZ, as if it were an incremental encoder with a reset index.
- **Temperature Sense:** on-board NTC thermistor adequately interfaced to the microcontroller for having an indication of the board temperature.

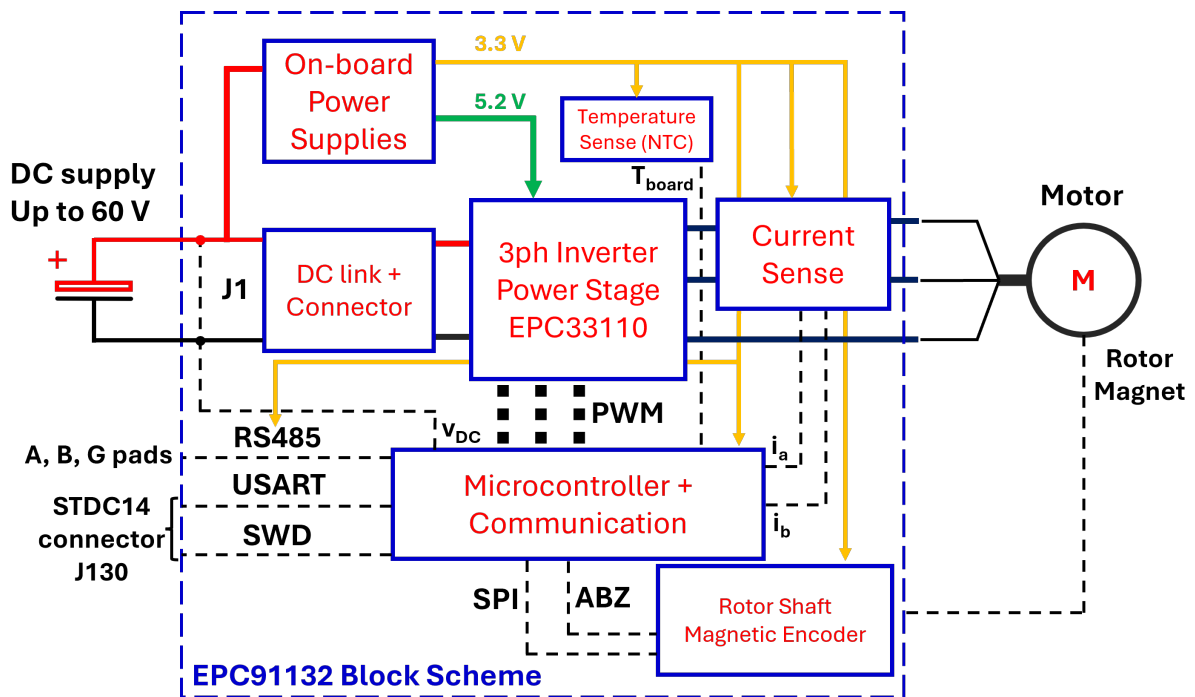


Figure 6.32: EPC91132 functional block diagram.

Chapter 7

Motor Drive Inverter Board Design

7.1 Microcontroller

The inverter board EPC91132 features an STM32 microcontroller from the G431 family. These devices are based on the high-performance Arm[®] Cortex[®]-M4 32-bit RISC core, and they can operate at a frequency of up to 170 MHz. They also embed high-speed memories (up to 128 Kbytes of Flash memory, and 32 Kbytes of SRAM), an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses, and a 32-bit multi-AHB bus matrix. They offer two fast 12-bit ADCs (4 Msps), four comparators, three operational amplifiers, four DAC channels (2 external and 2 internal), an internal voltage reference buffer, a low-power RTC, one general-purpose 32-bit timer, two 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and one 16-bit low-power timer [42].

In particular, the chosen component is named STM32G431KBU6, where the letter 'K' specifies the number of pins (32 in this case), the letter 'B' indicates the size of the flash memory and SRAM (128K and 32K), while the end of the identifier 'U6' is linked to the type of package (UFQFPN32). The choice of using a microcontroller with the least number of external pins was due to the size constraints of placing all the main inverter components inside a 23mm-diameter circumference; in fact, the selected package for the G431 family has a dimension of 5x5mm. The UFQFPN32 pinout description of STM32G431 microcontrollers is shown in Figure 7.1, from which an analysis has been carried out to assign to each pin a specific function, respecting all the programmable internal connections available in the microcontroller. Figure 7.2 reports the final result of the pin assignment process. The Pin Name column contains the manufacturer's pinout description of each pin, as previously mentioned. Each pin can be of three different types: power type for supplying the microcontroller with the nominal 3.3 V voltage (VDD and VSS), also for the analog part (VDDA and VSSA); analog type if the pin can be internally routed to a DAC or ADC peripheral; digital type if the pin is used as a simple GPIO or it is routed to an internal peripheral according to its available alternate functions (including SWDIO and SWCLK input signals for programming and programming the microcontroller).

The microcontroller's configuration for implementing the FOC algorithm freely offered by STMicroelectronics will be better explained in the following chapter, but the peripherals needed for this purpose are listed below.

- Advanced motor control timer TIM1 to generate the three PWM complementary outputs for driving the three inverter legs (CH1/CH1N - CH2/CH2N - CH3/CH3N). It has a counter

resolution of 16-bit, with an integer prescaler factor between 1 and 65536 and 4 capture/compare channels. To implement a hardware overcurrent protection, the related signal from the current sensors is connected to the TIM1 break input, which disables all the complementary outputs as soon as the signal OCDn is pulled down.

- General-purpose TIM2 to implement the PWM control protocol commonly used for ESCs, which consists of varying the duration of the signal's high pulse to set the motor speed. It has a counter resolution of 32-bit, with an integer prescaler factor between 1 and 65536 and 4 capture/compare channels, but it doesn't support any complementary outputs. This timer is properly configured in PWM input mode in order to measure the period value with the TIM2_CCR1 register and to measure the pulse width with the TIM2_CCR2.
- General-purpose TIM3 to handle the incremental encoder signals A (CH1), and B (CH2). It has a counter resolution of 16-bit, with an integer prescaler factor between 1 and 65536 and 4 capture/compare channels, but it doesn't support any complementary outputs.
- Analog-to-digital converter ADC1 to sample the phase V current (IN15) and the NTC voltage for retrieving the board temperature (IN1). The ADC2 is used to sample the phase U current (IN13) and the DC bus voltage (IN10). Both the ADCs have a resolution of 12-bit, with a sampling time set to 6.5 ADC clock cycles and the external trigger source linked to the TIM1 trigger out event for the two-phase currents, while for the other two signals, which are characterized by a much lower dynamic, the sampling time is set to 47.5 ADC clock cycles and the conversion is launched by software.
- Digital-to-analog converter DAC1 for debugging purposes. It features a resolution of 12-bit and up to two output channels, but only one at a time can be used with this pin assignment, due to the limited number of microcontroller pins.
- USART2 peripheral is configured to communicate with the microcontroller with a baudrate of 921600 bits/s, word length of 8 bits, no parity bit, and 1 stop bit. Since an RS-485 transceiver is interfaced with the microcontroller (Figure 7.4), for handling the half-duplex communication required by the RS-485 protocol, the Hardware Flow Control can be enabled when configuring the peripheral, but it requires the additional DE (Data Enable) pin, in addition to the RX and TX pins.
- SPI1 peripheral can be configured to establish a Serial Peripheral Interface (SPI) communication with the magnetic encoder. The full-duplex master mode requires 4 signals: SPI_MOSI (Master Output Slave Input), SPI_MISO (Master Input Slave Output), SPI_SCK (Clock), and SPI_NSS (Net Slave Select).
- CORDIC peripheral enabled for exploiting the hardware acceleration of certain mathematical functions, such as trigonometric ones, which are commonly used in motor control algorithms.

In Figure 7.3, it can be observed how the schematic of the EPC91132 control stage has been realized. The STDC14 connector has been placed in the external PCB frame to ease the programming and debugging process, even though all the required signals can also be provided through dedicated pins placed in the small circular PCB frame. The ESD protections have been added to provide additional protection to the microcontroller's pins, but they are not strictly necessary

because they are already present inside the microcontroller. Some decoupling capacitors (C100-103) are mandatory to provide a sufficiently constant voltage supply to the microcontroller. Since the chosen microcontroller also supports an input analog supply voltage, the 3V3A rail is derived from the 3V3 net generated by the related voltage regulator, placing a ferrite in between to decouple the two supplies. Analog and power ground are connected together with a 0 Ohm resistance, because the low voltages handled by this inverter board do not require insulation between the power and control stages.

In the schematic, some buttons can be seen, which are used to implement two manual triggers for the reset function of the microcontroller (active low) and for the Start/Stop function (PB6 configured as a GPIO that can detect rising edge transitions and generate an external interrupt for starting or stopping the motor control routine).

The encoder Z reset signal is connected to pin PB7, which is configured in the same way as PB6, because it is used to reset the TIM3 counter when one full mechanical turn has been completed by the rotor, when the Z signal generates a short high-pulse.

RuC2/C3/C5/C6/C7 have been added to solve some inevitable conflicts that have emerged during the pin assignment. The default configuration consists of connecting the OCDn signal to pin PA6 and the PWM_ESC signal to PA15, which does not allow for using the SPI communication with the magnetic encoder. To use the latter in the full-duplex master mode, both the resistors RuC3 and RuC6 must be mounted instead of RuC2 and RuC5, but the overcurrent detection and the PWM ESC function are not available.

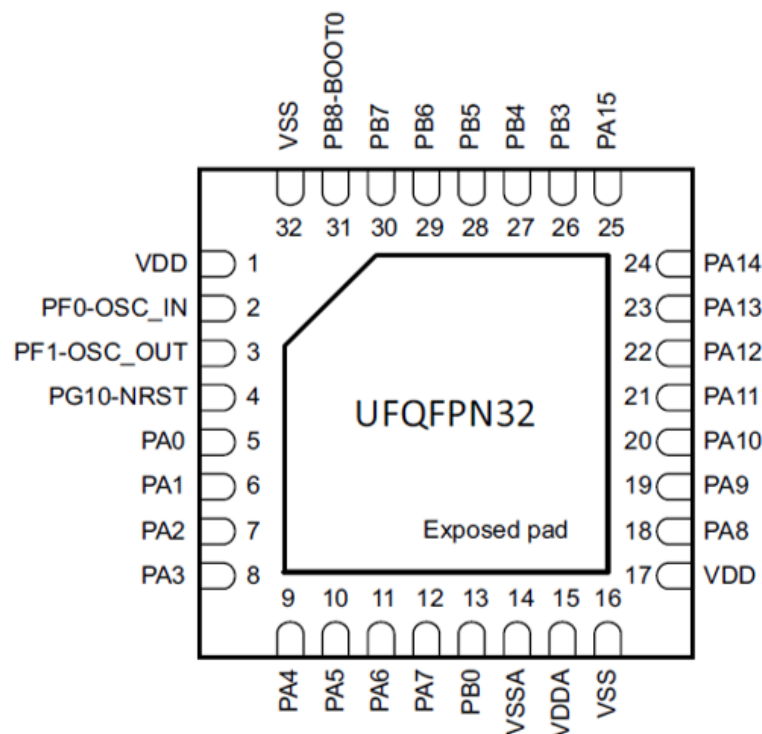


Figure 7.1: UFQFPN32 pinout description of STM32G431 microcontrollers [42].

Pin #	Function Name	Pin Name	Description	Type	Input/Output
1	3V3	VDD	Input supply voltage	Power	Input
2	PWML3	PF0-OSC_IN	Phase W low PWM signal	Digital	Output
3	Vdc	PF1-OSC_OUT	Vdc sense signal	Analog	Input
4	NRST	PG10-NRST	Reset pin	Digital	Input
5	Temp	PA0	NTC sense signal	Analog	Input
6	USART_DE	PA1	Driver Enable (DE) signal for RS485 communication	Digital	Output
7	USART_TX	PA2	Transmitter (TX) signal for USART/RS485 communication	Digital	Output
8	USART_RX	PA3	Receiver (RX) signal for USART/RS485 communication	Digital	Input
9	DAC_CH1	PA4	DAC Channel 1	Analog	Output
10	Isns1	PA5	Phase U current sense signal	Analog	Input
11 ^a	ODCn	PA6	Overcurrent detection signal	Digital	Input
11 ^b	SPI_MISO	PA6	SPI MISO signal	Digital	Input/Output
12	SPI_MOSI	PA7	SPI MOSI signal	Digital	Input/Output
13	Isns2	PB0	Phase V current sense signal	Analog	Input
14	GND	VSSA	Analog ground	Power	Input
15	3V3A	VDDA	Input analog supply voltage	Power	Input
16	GNDP	VSS_1	Power ground	Power	Input
17	3V3	VDD_2	Input supply voltage	Power	Input
18	PWMH1	PA8	Phase U high PWM signal	Digital	Output
19	PWMH2	PA9	Phase V high PWM signal	Digital	Output
20	PWMH3	PA10	Phase W high PWM signal	Digital	Output
21	PWML1	PA11	Phase U low PWM signal	Digital	Output
22	PWML2	PA12	Phase V low PWM signal	Digital	Output
23	SWDIO	PA13	SWD input/output signal	Digital	Input/Output
24	SWCLK	PA14	SWD clock signal	Digital	Input
25 ^a	PWM_ESC	PA15	PWM ESC control signal	Digital	Input
25 ^b	SPI_NSS	PA15	SPI NSS signal	Digital	Input/Output
25 ^c	OCDn	PA15	Overcurrent detection signal	Digital	Input
26	SPI_SCK	PB3	SPI clock signal	Digital	Input/Output
27	EncA	PB4	Encoder A signal	Digital	Input
28	EncB	PB5	Encoder B signal	Digital	Input
29	StartStop	PB6	Start/Stop button signal	Digital	Input
30	EncZ	PB7	Encoder Z signal	Digital	Input
31	BOOT0	PB8-BOOT0	GPIO pin/BOOT function	Digital	Input
32	GNDP	VSS_2	Power ground	Power	Input

11^a) default pin configuration; RuC2 mounted, RuC3 not mounted;

11^b) alternative pin configuration; RuC2 not mounted, RuC3 mounted; needed for SPI communication with the encoder

25^a) default pin configuration; RuC5 mounted, RuC6 not mounted; RuC7 not mounted; needed for PWM ESC control

25^b) alternative pin configuration; RuC5 not mounted, RuC6 mounted; RuC7 not mounted; needed for SPI communication with the encoder

25^c) alternative pin configuration; RuC5 not mounted, RuC6 not mounted; RuC7 mounted; needed for Overcurrent detection when 11^b) is used

Figure 7.2: EPC91132 microcontroller pin map.

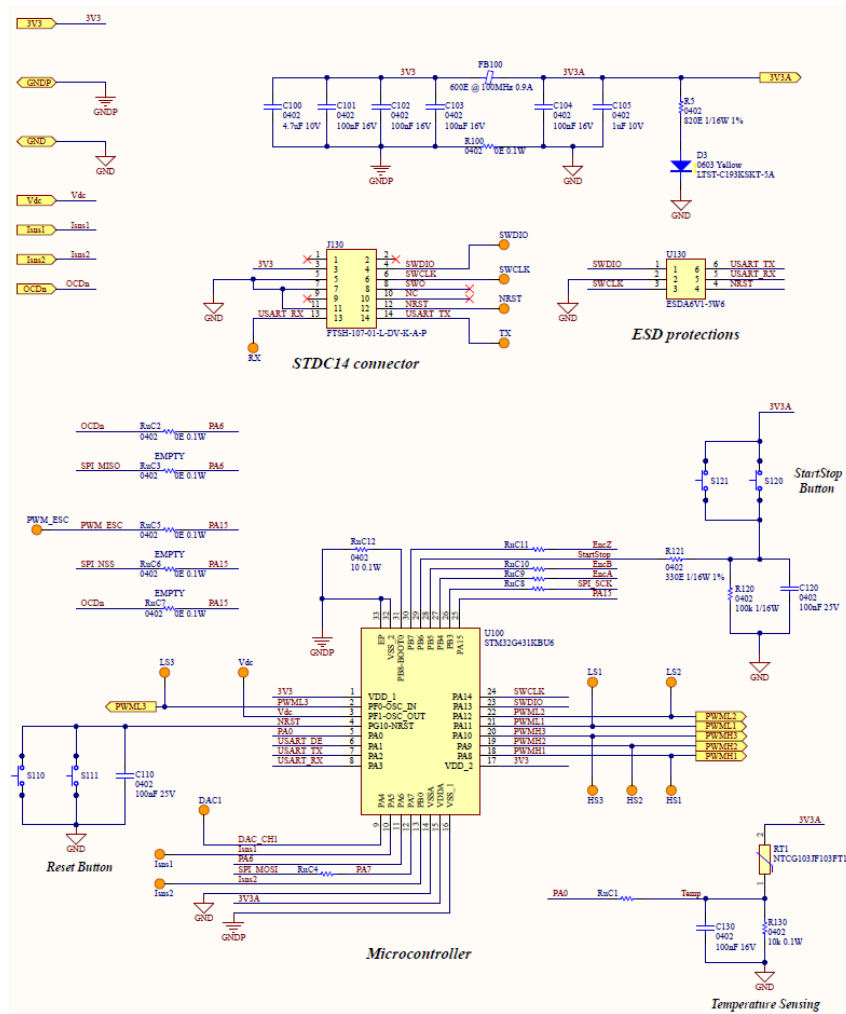


Figure 7.3: EPC91132 control stage schematic.

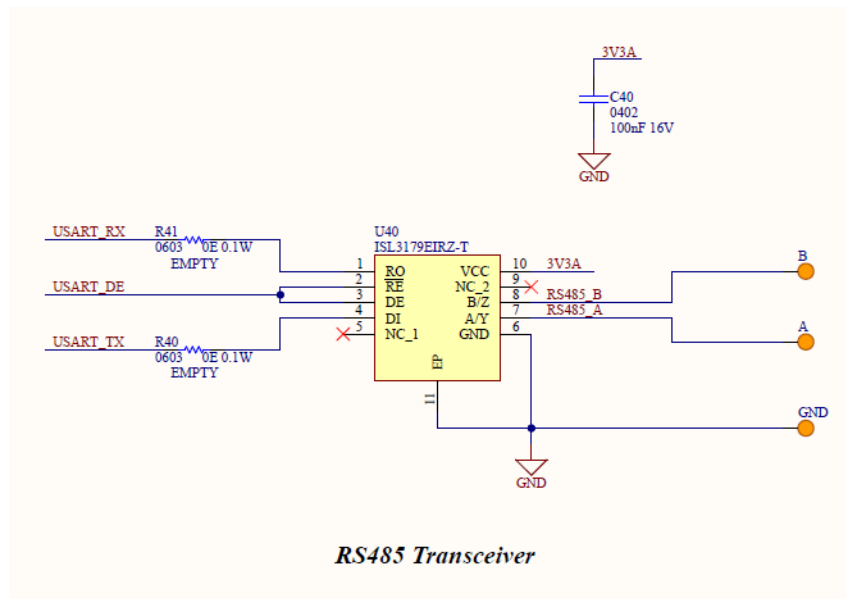


Figure 7.4: RS485 transceiver schematic (ISL3179EIRZ-T from Renesas).

7.2 Power Stage and Current Sensing

The EPC91132 power stage consists of the three-phase micromodule EPC33110, which integrates three half-bridges and many other functions, as explained in Chapter 5. In Figure 7.6, the schematic diagram of the power module and all the necessary passive components are shown to guarantee its correct operation. First of all, four small ceramic capacitors of 100 nF (C80/81/82/83) are placed very near to the device and connected between V_{in} and a dedicated ground plane, in order to make the switching loop as small as possible, thus avoiding voltage oscillations during the transients. C50 (10 μ F) is the bypass capacitor needed between the external 5.2 V power supply and the VDRV pin, while for each VDDx pin (Phasex internal supply), a 100 nF bypass capacitor is sufficient. The three floating bootstrap power supplies have a 2.2 μ F capacitor connected between Bootx and SWx pins, which guarantees the proper voltage level to the high-side gate drivers. The six PWM signals from the microcontroller are interfaced with the EPC33110 pins through a low-pass filter, in order to attenuate high-frequency noise and stabilize the signals. Finally, the VDDx standby and PWM fast shutdown input is directly connected to the overcurrent detection signal coming from the current sensors, so that the device can be disabled as soon as the phase current exceeds the threshold value.

Since the EPC33110 does not provide the source terminals of the three low-side power FETs, the most straightforward current sensing solution is to use two current sensors to measure phase 1 and phase 2 currents. In particular, the current sensors chosen are manufactured by Monolithic Power Systems (MPS), and they belong to the MCS1823 family [43], which includes different variants of linear Hall-effect current sensor ICs for AC and DC current sensing, with a declared bandwidth of 120 kHz. Among their features (see Figure 7.5 for the functional block diagram), these sensors include a differential Hall array that allows to cancel out any stray magnetic field, but they also integrate a fast over-current detection with 1 μ s response time and a predefined threshold, from 50% to 240% of the rated current range of the specific component. The part number chosen is MCS1823-330BRN, which needs a voltage supply of 3.3 V, features a sensitivity of 44 mV/A, and has a rated current range of ± 30 A, with an overcurrent threshold of ± 30 A. As well as all the MCS1823 sensors, it is available in an ultra-small TQFN-12 package, 3x3 mm. The voltage outputs of the two current sensors are routed to PA5 and PB0 pins of the microcontroller through an optional low-pass filter, with a cut-off frequency of about 15 kHz, which helps attenuate PWM frequency noise during the sampling. Both the OCDn signals are pulled up with a 100 k Ω resistance and connected to ground with a 100 nF capacitor for stabilizing the signal, and so avoiding false triggering of the overcurrent protection.

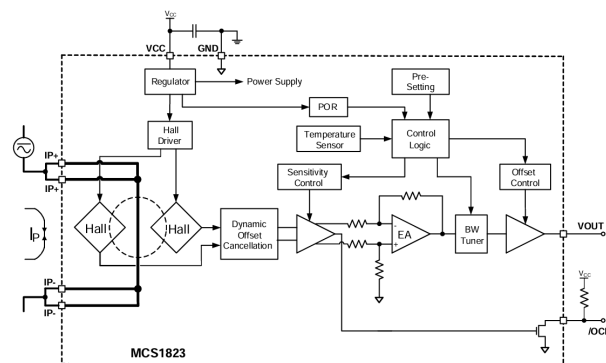


Figure 7.5: MCS1823 current sensor functional block diagram [43].

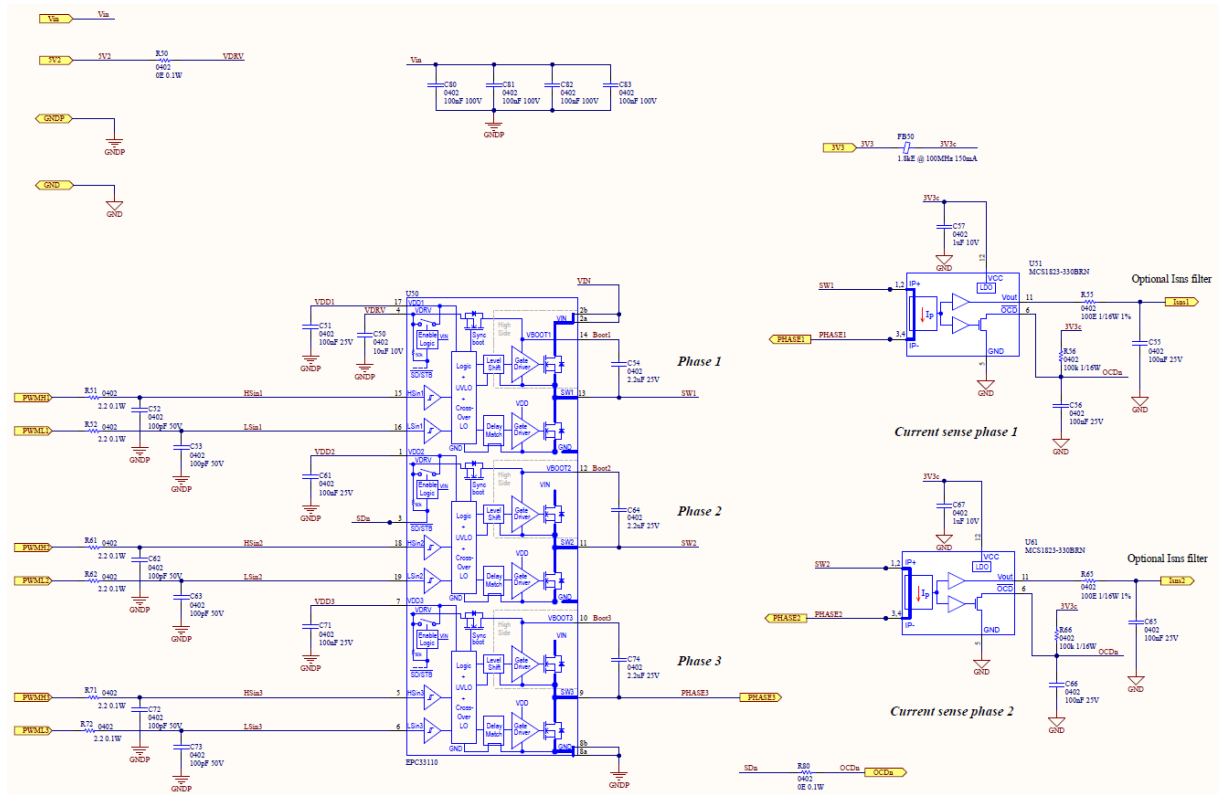
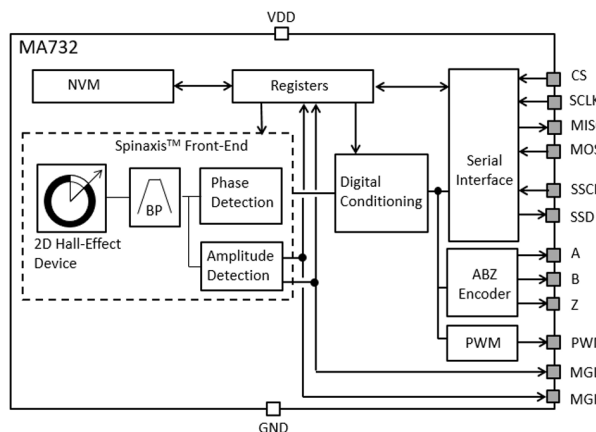
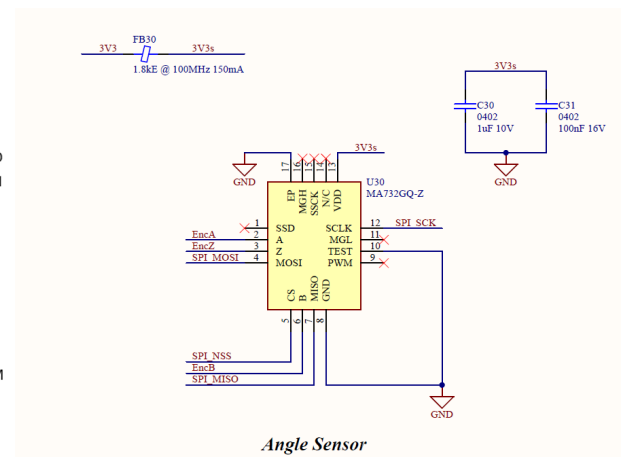


Figure 7.6: EPC91132 power stage schematic.



(a) Functional block diagram [44].



(b) Schematic detail.

Figure 7.7: EPC91132 angle sensor (MagAlpha MA732).

7.3 Position Sensing

To implement a sensed FOC algorithm for driving a PMSM motor, an angle sensor is needed, and the MagAlpha MA732 from MPS was chosen. This IC angle sensor is available in a small QFN-16 package (3x3 mm) and can detect, with a resolution up to 14-bit, the absolute angular position of a permanent magnet, such as a diametrically magnetized cylinder on a rotating shaft, which is available in both the MG8008E-i9 V3 servomotor and the Vertiq 23-06 G1 Module. As can be seen in Figure 7.7a, this sensor can be used with different types of outputs: incremental 12-bit ABZ quadrature encoder interface with programmable pulses per turn from 1 to 1024; 14-bit PWM absolute output, which provides a logic signal with a duty cycle proportional to the angle of the magnetic field; SPI serial interface for digital angle readout and chip configuration, since an on-chip, non-volatile memory is integrated inside the sensor, which provides storage for configuration parameters, including the reference zero angle position, ABZ encoder settings, and magnetic field detection thresholds [44].

In Figure 7.7b, the schematic detail of the angle sensor shows that in the EPC91132 board it can be used only as an incremental ABZ encoder or through the SPI serial interface because the PWM pin is has been left unconnected, even though with the latter solution, neither the over-current nor the PWM ESC functions can be implemented in the microcontroller (Section 7.1). Therefore, it is more advisable to use the SPI serial interface only for configuration purposes, while the angle reading is performed through the ABZ signals, with the maximum pulses per turn set by default at 1024. The chip is supplied with 3.3 V, placing two decoupling capacitors of 1 μ F and 100 nF close to it. The MGH and MGL pins are not used because their function is not strictly necessary; in fact, they indicate whether the field strength is above the MGHT level or below the MGLT level. The TEST pin is connected to ground as specified in the datasheet (it is a factory-use-only pin). The SSD and SSCK are the two pins used for the SSI serial interface (for data reading only), but they are left floating because the full-duplex master SPI solution has been preferred over that.

7.4 Housekeeping Power Supplies

5.2 V Integrated Synchronous Step-Down Converter

The 5.2 V voltage supply needed by the EPC33110 module and the 3.3 V linear regulator are provided by the MP4571 from MPS. It is a fully integrated, synchronous step-down converter, with a configurable switching frequency up to 2.2 MHz. Its rated output current is declared equal to 1 A, while the input voltage range is between 4.5 V and 60 V, which obviously limits the input supply voltage of the EPC91132 board, but it is consistent with the maximum drain-to-source voltage supportable by the power module's GaN FETs. The integrated buck converter features internal high-side and low-side power MOSFETs, and it is available in a 2.5x3 mm QFN-12 package [45]. As can be observed in Figure 7.8, the MP4571 integrates many functions, including built-in soft start, enable control, power good indicator, short-circuit protection (SCP), input under-voltage lockout (UVLO), and auto-recovery thermal protection.

Figure 7.9 shows how the step-down converter has been inserted in the inverter board. All the connections and components have been chosen starting from the typical application circuits illustrated in the datasheet [45]. A 100 nF decoupling capacitor (C11) is placed near the input supply pin and connected to ground to reduce switching spikes. Another 100 nF capacitor is

connected between the SW and BST pins to form a floating supply across the high-side switch driver. A 1 μF capacitor is required by the VCC pin, which supplies power to the internal control circuit and gate drivers. Depending on how is connected the CCM/SYNCO pin, the converter can operate in two different modes under light-load conditions. If the pin is left floating, the MP4571 uses the Advanced Asynchronous Modulation (AAM) during light load, which allows for high efficiency by scaling down the frequency to reduce the switching and gate driver losses. If the pin is connected to ground through a 10 k Ω to 300 k Ω resistor, the converter is forced to work in Continuous Conduction Mode (CCM) also during light load conditions. Since the second modality of operation has been chosen, a 100 k Ω resistor (R11) has been connected between the CCM pin and ground. The enable EN pin must be driven high to turn on the device. Unfortunately, this pin can withstand a maximum voltage of 6 V, so it cannot be directly connected to the input supply voltage. To solve this problem, a zener diode (MMSZ5232BS from Diodes Incorporated [46]) is connected between the enable pin and ground, which guarantees a nominal reverse voltage of 5.6 V at 20 mA and 25°C. To limit the current flowing in the diode, a 100 k Ω resistor is connected between Vin and the diode's cathode.

The feedback pin FB is the negative input of the error amplifier. Connecting the FB pin to the tap of an external resistor divider between the output and ground allows setting the regulation voltage. From the device datasheet, the output voltage is given by the following formula:

$$V_{out} = 0.8 \cdot \left(\frac{R14}{R15} + 1 \right)$$

With R14 set to 56.2 k Ω and R15 to 10 k Ω , the regulation voltage results equal to 5.296 V. The value of resistor R13 has been chosen to ensure the feedback loop stability. A green LED diode (in series with an 820 Ω resistor to limit the current) has been connected in parallel with the output voltage to visually report the presence of the correct level of voltage at the converter's output. The FREQ pin has the function of configuring the switching frequency of the converter by connecting a resistor to GND. The minimum resistor's value is 10 k Ω , which corresponds to the maximum switching frequency of 2.2 MHz, while selecting a resistor equal to 100 k Ω , the switching frequency is set at the minimum value of 300 kHz. In this particular case, the switching frequency has been set at around 500 kHz, since the R12 resistor has a value of 56.2 k Ω (according to the equation reported in the datasheet [45]).

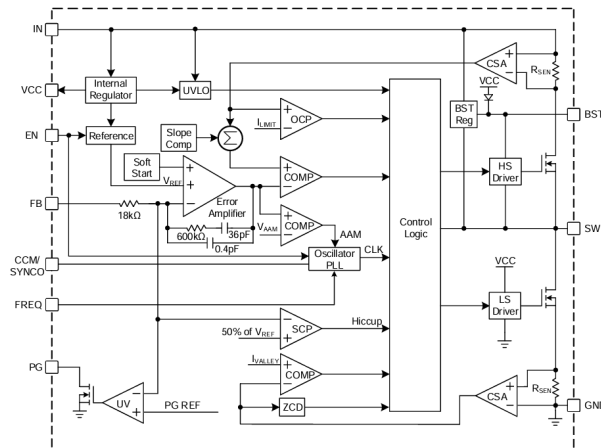


Figure 7.8: MP4571 synchronous buck converter functional block diagram [45].

The last two components needed to complete the 5.2 V power supply are the output inductor and capacitor. The chosen inductor is the VLS201612CX-220M (0806 SMD package) from TDK [47], which has a nominal inductance of 22 μH , a rated saturation current of 0.45 A, and a rated thermal current of 0.57 A. These values are lower than the maximum output current deliverable by the step-down converter, but they are higher than the actual current requirements of all the loads supplied by it. In fact, the overall average load current in the 5.2 V side required by the EPC33110 (≈ 50 mA), the microcontroller (≈ 76 mA), the two current sensors (≈ 36 mA), the encoder (≈ 18 mA), the RS485 transceiver (≈ 6 mA) and the three LEDs (≈ 18 mA) can be estimated considering the rated current consumptions in normal operations declared in the various datasheets, and the result is about 200 mA. This value can also be used to verify that the converter is able to work in continuous conduction mode during normal load operations, by applying the following formula to find the minimum inductance value, in which V_{in} is set to 24 V, V_{in} to 5.2 V, f_{sw} to 500 kHz, and ΔI_L to 400 mA (200 mA considered as the critical current):

$$L = \frac{V_{out}}{f_{sw} \cdot \Delta I_L} \cdot \left(1 - \frac{V_{out}}{V_{in}}\right) = 20.37 \mu\text{H}$$

By choosing a capacitor of 22 μF , the maximum output voltage ripple with V_{in} equal to 24 V and $L = 22 \mu\text{H}$ is given by this simplified formula (valid for ceramic capacitors):

$$\Delta V_{out} = \frac{V_{out}}{8 \cdot f_{sw}^2 \cdot L \cdot C_{out}} \cdot \left(1 - \frac{V_{out}}{V_{in}}\right) = 4.21 \text{ mV}$$

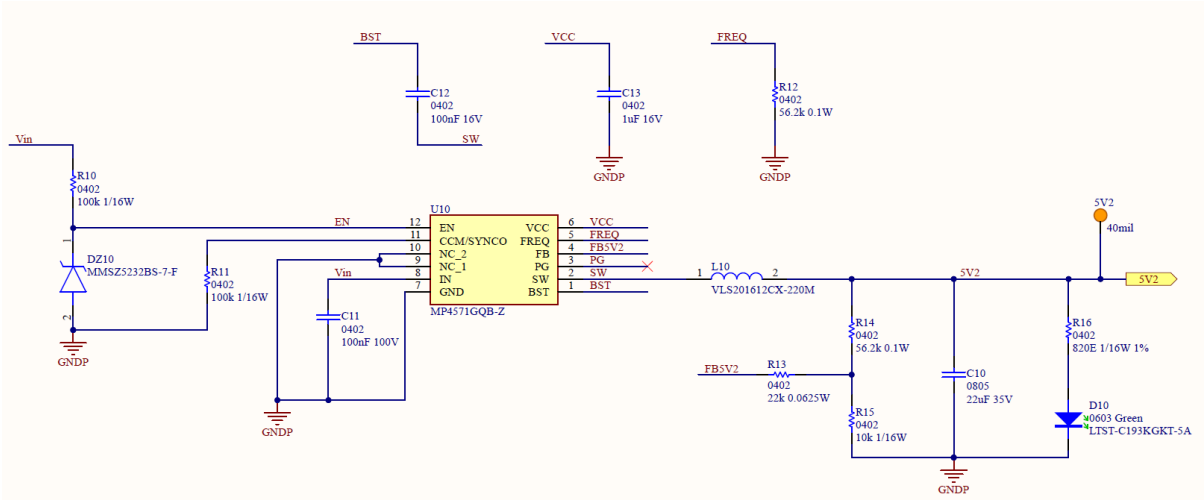


Figure 7.9: 5.2 V synchronous buck converter schematic.

3.3 V Linear Regulator

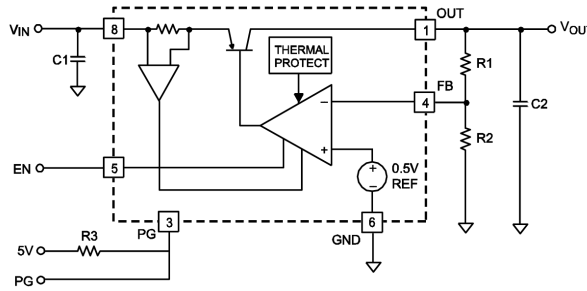
To generate the 3.3 V voltage required by the microcontroller, the two current sensors, the encoder, and the RS485 transceiver, a low-dropout linear regulator has been chosen. It is the MP2002A (2x3 mm QFN-8 package) from MPS, which can operate with an input supply between 1.35 V and 6.5 V, and it can generate an adjustable output voltage from 0.5 V to 5 V using an external resistor divider. It can supply up to 500 mA of load current. As can be seen in Figure 7.10a, it features thermal overload and current limit protection, along with an enable pin

and a power good open-drain output [48].

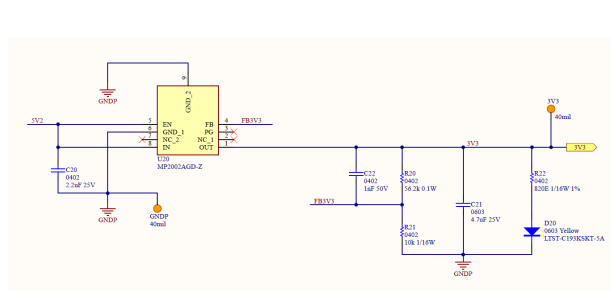
This device shows good stability with very small ceramic capacitors, enabling the limit of the PCB area occupied by the entire 3.3 V power supply circuitry. In fact, Figure 7.10b shows that the voltage regulator needs only an input capacitor of 2.2 μF and an output capacitor of 4.7 μF to work properly. The enable pin has been directly connected to the 5.2 V supply because it can withstand this voltage without any problems, while the power good open-drain output has been left floating since it is not used in this application. To set the regulated output voltage at 3.3 V, R20 was set to 56.2 k Ω while R21 to 10 k Ω , according to the following formula provided by the manufacturer:

$$V_{out} = 0.5 \cdot \left(\frac{R20}{R21} + 1 \right)$$

Also in this case, the presence of the correct level of voltage at the regulator's output is reported by a yellow LED diode (in series with an 820 Ω resistor to limit the current), which has been connected in parallel with the output voltage.



(a) Functional block diagram [48].



(b) Schematic detail.

Figure 7.10: EPC91132 3.3 V linear regulator (MP2002A).

7.5 DC Bus Sizing

Choosing the optimal amount of DC bus capacitors is one of the most crucial design steps of an integrated motor drive. In fact, these components play a preponderant role in determining the overall PCB area for designing an inverter. Since the EPC91132 features GaN FETs in the power stage, ceramic capacitors can be used instead of the bulkier electrolytic capacitors, because the possibility of increasing the switching frequency allows for substantially reducing the DC link capacitance, maintaining the same voltage ripple. To understand which electrical parameters influence the DC link voltage ripple, some simulations on PLECS have been carried out, which helped to find a way to rapidly estimate the maximum voltage ripple across the DC bus capacitors, according to the specifications of an arbitrary motor drive application.

Figure 7.11 reports the PLECS schematic circuit of the three-phase PWM voltage source inverter used for the simulations. It is a simplified circuit, since all the components are idealized, from the DC bus capacitor to the MOSFET switches, along with the motor's windings considered as ideal current sources, which are configured to generate a sinusoidal balanced current triplet. The six power devices are driven through the PWM_modulator block already present in the library, which performs a space vector PWM modulation to produce the six PWM signals,

according to the three sinusoidal voltage references provided at its input. The simulation model allows for freely setting the following electrical parameters:

- DC voltage source: V_{BUS}
- DC impedance: R_{BUS} and L_{BUS}
- DC bus capacitance: C_{BUS}
- PWM frequency: f_{PWM}
- Output RMS current: I_{OUT}
- Output fundamental frequency: f_{OUT}
- Output phase angle: φ
- Modulation index: m

The voltage ripple across the DC bus capacitor has been evaluated over a period of the output current, using the Steady-State Analysis tool available in PLECS. Figure 7.12 shows an example of the voltage ripple evaluation, using as simulation parameters: $V_{IN} = 48$ V; $R_{BUS} = 10$ m Ω ; $L_{BUS} = 100$ μ H; $C_{BUS} = 20$ μ F; $f_{PWM} = 10$ kHz; $I_{OUT} = 1$ Arms; $f_{OUT} = 10$ Hz; $\varphi = 0^\circ$; $m = 0.1$;

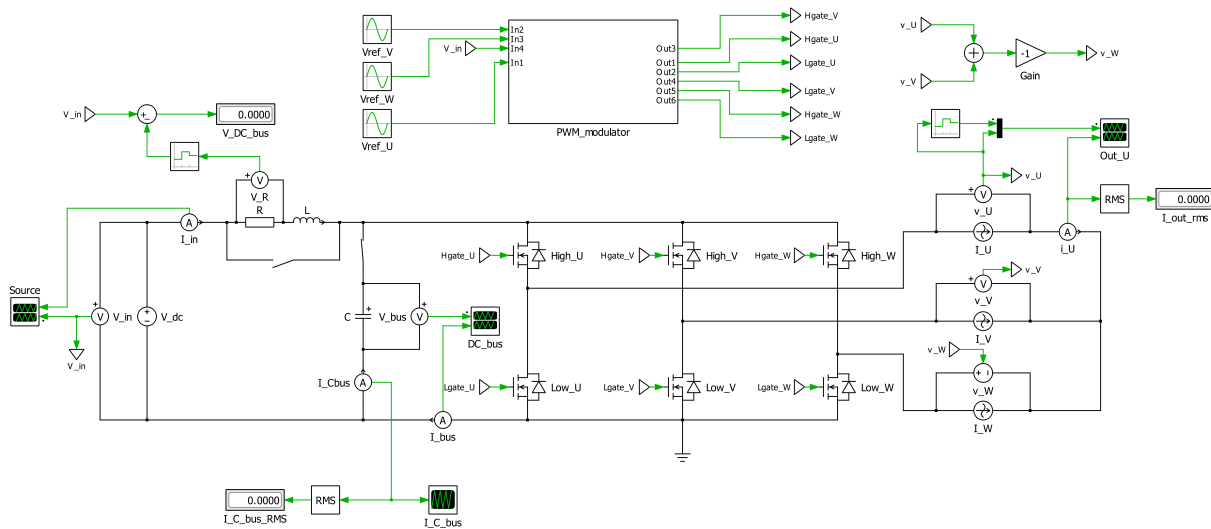


Figure 7.11: PLECS schematic of the simplified three-phase PWM voltage source inverter used for the simulations.

For each of the eight electrical parameters, different simulations have been carried out varying only one specific parameter, in order to highlight its influence on the DC bus voltage ripple. The result of this process showed that the voltage ripple is not influenced by the output fundamental frequency and the DC impedance. The latter statement remains true as long as the DC bus is characterized by a capacitive reactance sufficiently lower than the inductive reactance, both calculated at the switching frequency. Instead, the maximum voltage ripple in the DC bus revealed a direct proportionality with the output current, while an inverse proportionality with the DC bus capacitance and the PWM frequency. The dependence on the output phase angle and modulation is more complicated, since the voltage ripple is simultaneously influenced by

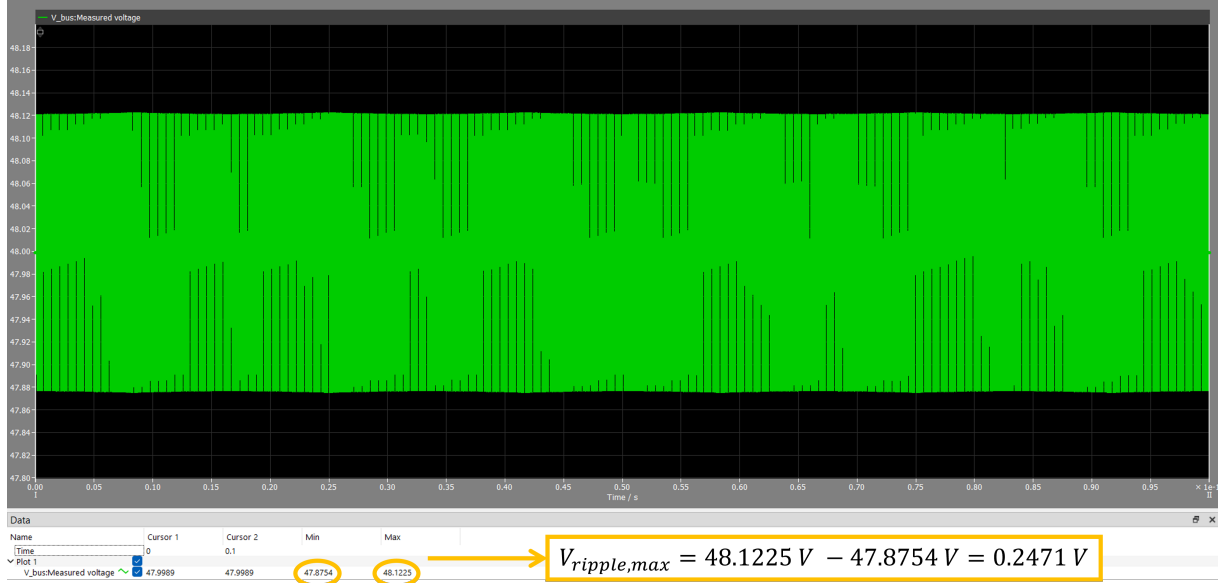


Figure 7.12: Example of the DC bus voltage ripple evaluation with the PLECS model.

both the parameters.

Therefore, combining the results obtained from the various simulation tests, the maximum voltage ripple across the DC bus capacitor can be estimated with the following equation:

$$V_{\text{ripple,max}} = K(m, \varphi) \cdot \frac{I_{\text{out,rms}}}{C_{\text{bus}} \cdot f_{\text{PWM}}}$$

where the function $K(m, \varphi)$ has been introduced to take into account the double dependence of the voltage ripple on the modulation index and the output phase angle. In Figure 7.13 are plotted the K values obtained running the PLECS model with this simulation parameters: $V_{\text{IN}} = 48 \text{ V}$; $R_{\text{BUS}} = 10 \text{ m}\Omega$; $L_{\text{BUS}} = 100 \text{ }\mu\text{H}$; $C_{\text{BUS}} = 500 \text{ }\mu\text{F}$; $f_{\text{PWM}} = 20 \text{ kHz}$; $I_{\text{OUT}} = 1 \text{ Arms}$; $f_{\text{OUT}} = 10 \text{ Hz}$; $\varphi = 0^\circ \rightarrow 90^\circ$; $m = 0.01 \rightarrow 1.1547$. Each value has been computed by dividing the maximum voltage ripple obtained in the simulation by the output RMS current, and multiplying it by the DC bus capacitance and the PWM frequency. The maximum K value is equal to 0.354, and it is obtained at the maximum modulation index (before starting the over-modulation operation) and with an output phase angle of 90° (for both inductive and capacitive load behaviors).

The function $K(m, \varphi)$ can be approximated in order to simplify the maximum voltage ripple evaluation process. In particular, for each simulated output phase angle ($\varphi = 0^\circ \rightarrow 90^\circ$), a third-degree polynomial interpolation has been performed on the data obtained by the simulations, varying only the modulation index.

$$K(m, \varphi = \text{cost}) = a_3 \cdot m^3 + a_2 \cdot m^2 + a_1 \cdot m + a_0$$

In Table 7.1 are listed all the polynomial coefficients for the ten possible output phase angles. For a generic φ value, it is enough to perform a linear interpolation between the two $K(m, \varphi = \text{cost})$ values calculated in correspondence of the two adjacent φ used in the simulations:

$$K_{\text{prev}}(m, \varphi_{\text{prev}}) = a_{3,\text{prev}} \cdot m^3 + a_{2,\text{prev}} \cdot m^2 + a_{1,\text{prev}} \cdot m + a_{0,\text{prev}}$$

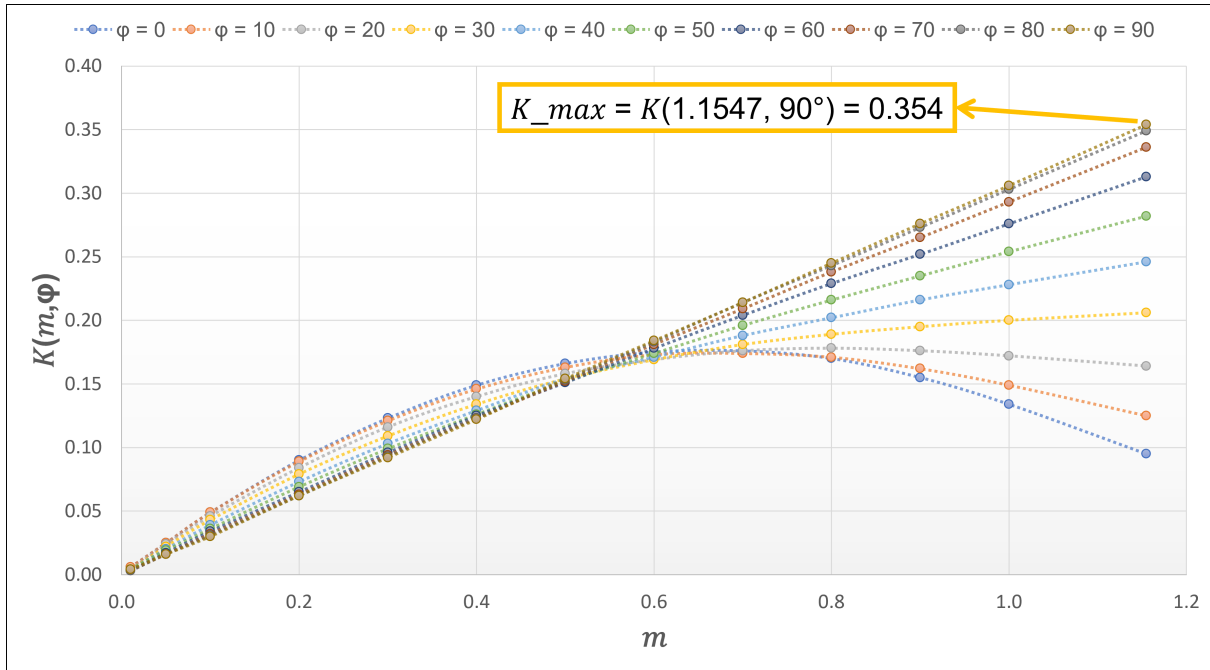


Figure 7.13: 2D representation of the function $K(m, \varphi)$.

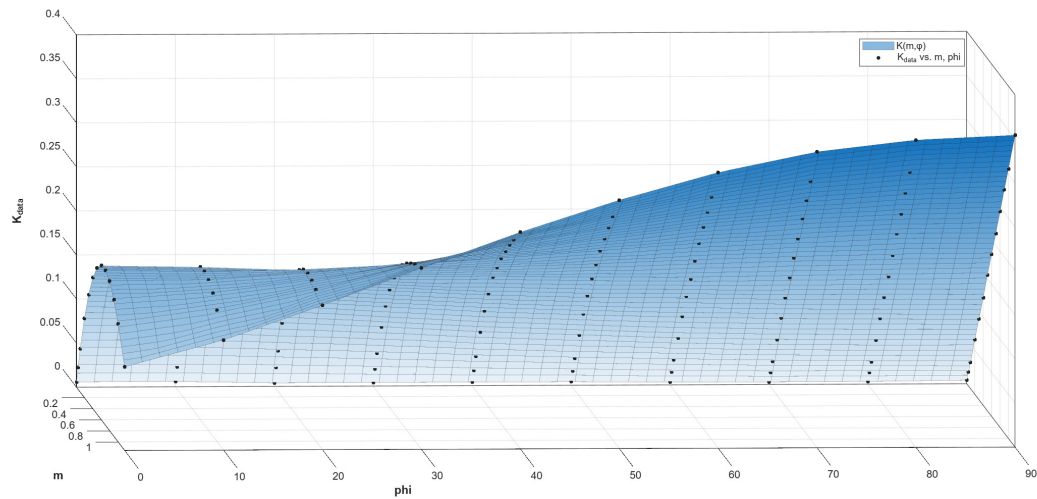


Figure 7.14: 3D representation of the function $K(m, \varphi)$.

Table 7.1: Polynomial coefficients for computing $K(m, \varphi = cost)$.

φ	a_3	a_2	a_1	a_0
0	0.0463	-0.4594	0.5505	-0.0010
10	0.1046	-0.5055	0.5524	-0.0009
20	0.1251	-0.4739	0.5231	-0.0015
30	0.1113	-0.3825	0.4721	-0.0007
40	0.0827	-0.2765	0.4224	-0.0005
50	0.0539	-0.1779	0.3776	0.0003
60	0.0000	-0.0483	0.3238	0.0015
70	0.0000	-0.0199	0.3125	0.0008
80	0.0000	0.0000	0.3021	0.0014
90	0.0000	0.0000	0.3059	0.0004

$$K_{next}(m, \varphi_{next}) = a_{3,next} \cdot m^3 + a_{2,next} \cdot m^2 + a_{1,next} \cdot m + a_{0,next}$$

$$K(m, \varphi) = K_{prev} + \frac{\varphi - \varphi_{prev}}{\varphi_{next} - \varphi_{prev}} \cdot (K_{next} - K_{prev})$$

The ceramic capacitor chosen for sizing the DC bus is the C2012X5R2A475K125AC from TDK. It is a Multilayer Ceramic Chip Capacitor (MLCC) available in an SMD 0805 package with a rated voltage of 100 V, and nominal capacitance of 4.7 μ F [49]. If the maximum tolerable voltage ripple on the DC bus is set to 3 V (6% with 48 Vdc), the phase angle is considered equal to 0° (common value with PMSM motors driven with a FOC control), and the modulation index equal to 0.6 (maximum $K(m, \varphi = 0)$ value from Figure 7.13), the required DC bus capacitance results about 5.8 μ F for an output current of 10 Arms (maximum current for the MG8008E-i9 V3 servomotor) and choosing a PWM frequency of 100 kHz. To achieve this capacitance value with an input DC voltage of 48 V, the number of capacitors is at least 12, because this capacitor suffers from the DC bias derating mechanism. In fact, at 48 Vdc, its capacitance is reduced by about 90%, while at 24 Vdc, the reduction is slightly smaller: with a reduction of 70% of capacitance, when supplied with 24 V, the DC bus features a maximum voltage ripple of about 1 V (4%), because the overall capacitance is triplicated.

So, 12 capacitors of 4.7 μ F (at 0 V bias) have been chosen to design the DC bus. But the other design requirement concerns the maximum allowable RMS current for each capacitor. To evaluate it, some other simulations have been performed with the same PLECS model, but this time for evaluating the maximum RMS current in the DC bus capacitor (Figure 7.15). In particular, the simulation parameters are: $V_{IN} = 48$ V; $R_{BUS} = 10$ m Ω ; $L_{BUS} = 100$ μ H; $C_{BUS} = 5.8$ μ F; $f_{PWM} = 100$ kHz; $I_{OUT} = 10$ Arms; $f_{OUT} = 10$ Hz; $\varphi = 0^\circ \rightarrow 90^\circ$; $m = 0.01 \rightarrow 1.1547$. Figure 7.16 shows that the RMS current across the DC bus capacitor highly depends on the modulation index, with the phase angle maintained constant to 0°. In particular, with a modulation

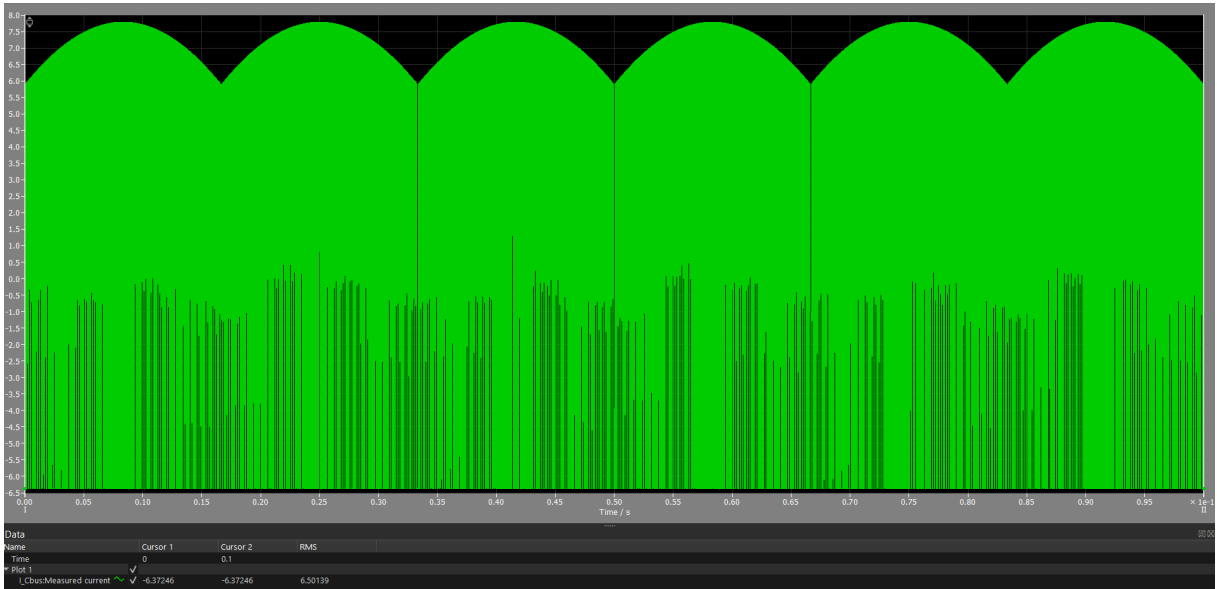


Figure 7.15: Example of the DC bus capacitor RMS current evaluation ($\varphi = 0$ and $m = 0.6$).

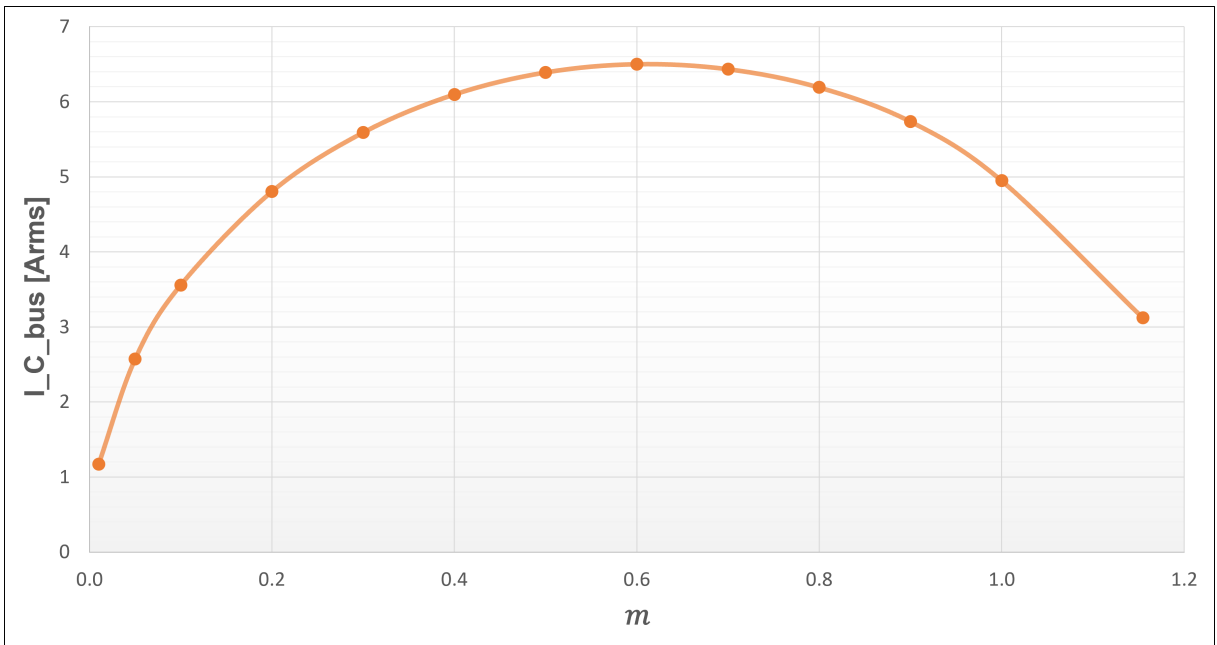


Figure 7.16: RMS current across the DC bus capacitor varying the modulation index ($\varphi = 0$).

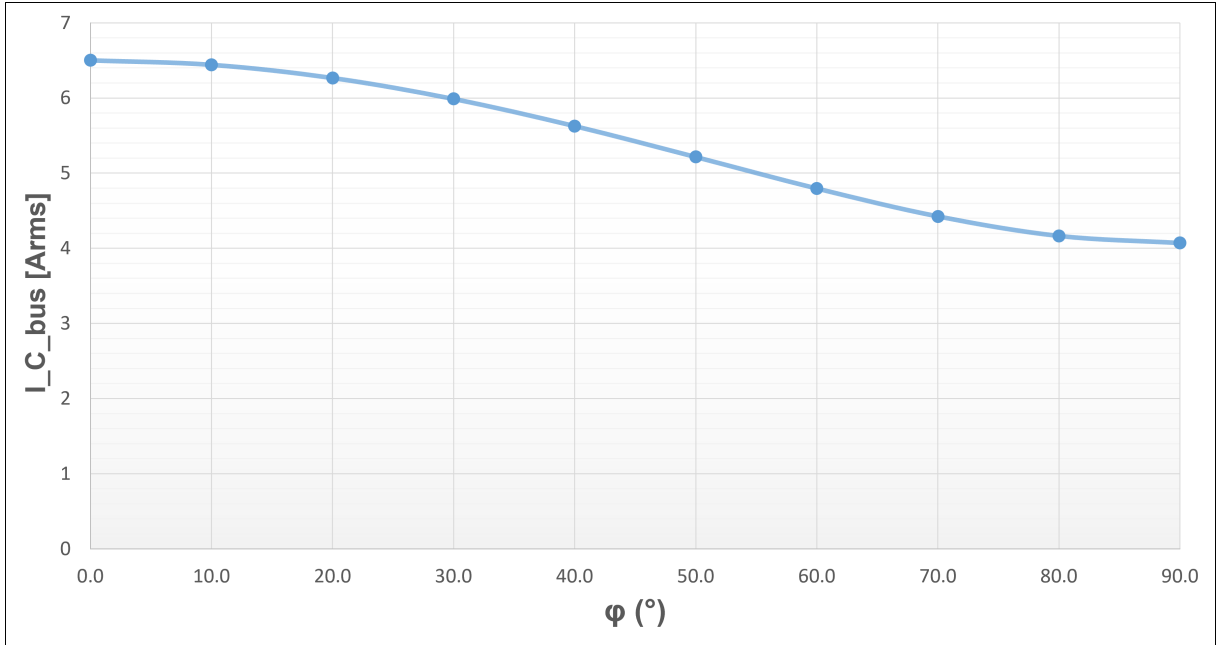


Figure 7.17: RMS current across the DC bus capacitor varying the phase angle ($m = 0.6$).

index of 0.6, the capacitor is more thermally stressed with the maximum RMS current of 6.5 A. If instead the phase angle is varied, maintaining the modulation index at 0.6, Figure 7.16 shows that the condition with 0° between the output voltage and current fundamental waveforms is the worst in terms of RMS current in the DC bus capacitor. Since the C2012X5R2A475K125AC capacitor can withstand an RMS current of 2 Arms at 100 kHz with a temperature increase of 20°C , a bank of 12 capacitors can easily manage a maximum RMS current of 6.5 A.

7.6 NTC Thermistor Temperature Sensor

To measure PCB temperature, an NTC thermistor sensor is placed near the EPC33110 and the microcontroller. NTC (Negative Temperature Coefficient) thermistors are semiconductor resistors whose resistance decreases as temperature increases. The EPC91132 board uses the NTCG103JF103FT1S thermistor (0402 SMD package) from the TDK NTCG series [50]. This series offers sensors with low thermal time constants, resulting in high resistance change rates for accurate temperature tracking. Figure 7.18 shows the characteristic curve of the NTC's nominal resistance versus temperature. The manufacturer provides these data with a step of 1°C , from -40°C to 150°C . The nominal resistance at 25°C is $10\text{ k}\Omega$. This characteristic is highly nonlinear. To retrieve the actual NTC temperature from the voltage drop across the thermistor, a 1-D look-up table was generated for use in the motor control firmware.

As shown in Figure 7.3, the NTC thermistor connects to the microcontroller through a 3.3 V supply and a $10\text{ k}\Omega$ resistor tied to ground. A 100 nF capacitor in parallel filters the sensed voltage signal. This setup ensures neither the NTC nor the resistor exceeds electrical or thermal limits. The NTC's maximum rated power at 25°C is 125 mW , and the maximum operating current at that temperature is 0.31 mA . Solving the voltage divider across all temperature data confirms these limits are not exceeded. At 25°C , the current through the NTC is 0.165 mA , and the power dissipated is 0.272 mW . To generate the 1-D LUT graphically reported in Figure 7.19,

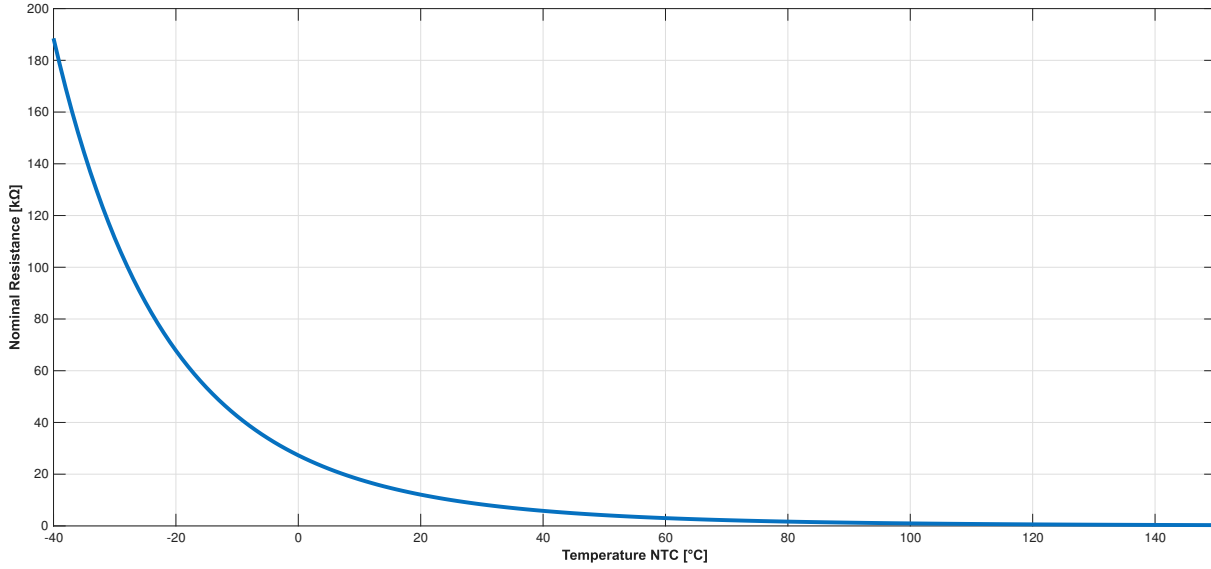


Figure 7.18: Nominal resistance vs. temperature of the NTCG103JF103FT1S thermistor.

the voltage drop across the 10 kΩ resistor has been computed for each temperature, and converted into the u16-bit unit used in the microcontroller:

$$V_{temp} [u16bit] = V_{temp} [V] \cdot \frac{65536}{3.3}$$

Here, 3.3 V is the input dynamic range of the microcontroller's embedded ADC (analog-to-digital converter), and 65536 reflects the fact that during ADC setup, the conversion result is left-aligned in the 16-bit data register, allowing results from 0 to 2^{16} (65536), even though the resolution is set to 12 bits. The input values for the LUT are the u16-bit voltage values across the 10 kΩ resistor. These values are equally spaced from a minimum of 3302 (0.166 V) to a maximum of 63547 (3.2 V), using a step of 317.079 (0.016 V), resulting in 191 values. For each point, the corresponding NTC thermistor temperature was calculated by linear interpolation of the previously obtained $V_{text} [u16bit]$ voltage data.

7.7 PCB Layout

The last part of the inverter board design process consists of placing all components on the board and implementing the PCB layout according to the electrical connections defined in the schematics. It was performed using the software Altium Designer, the industry standard for designing all types of PCBs.

In Figures 7.20a and b, the main components of the EPC91132 evaluation board are highlighted, which represent the functional blocks shown in the block diagram of Figure 6.32. On the top side (a), the EPC33110, the microcontroller, the two current sensors, the NTC temperature sensor, and the RS485 transceiver have been placed, along with the various pads and connectors for easing the debugging process. The DC link capacitors, the angle sensor, and the housekeeping power supplies have been placed on the bottom side (b). The Reset and Start/Stop buttons are present on both sides; in particular, a couple have been placed in the external PCB frame, while the others are in the small PCB frame, as a backup solution.

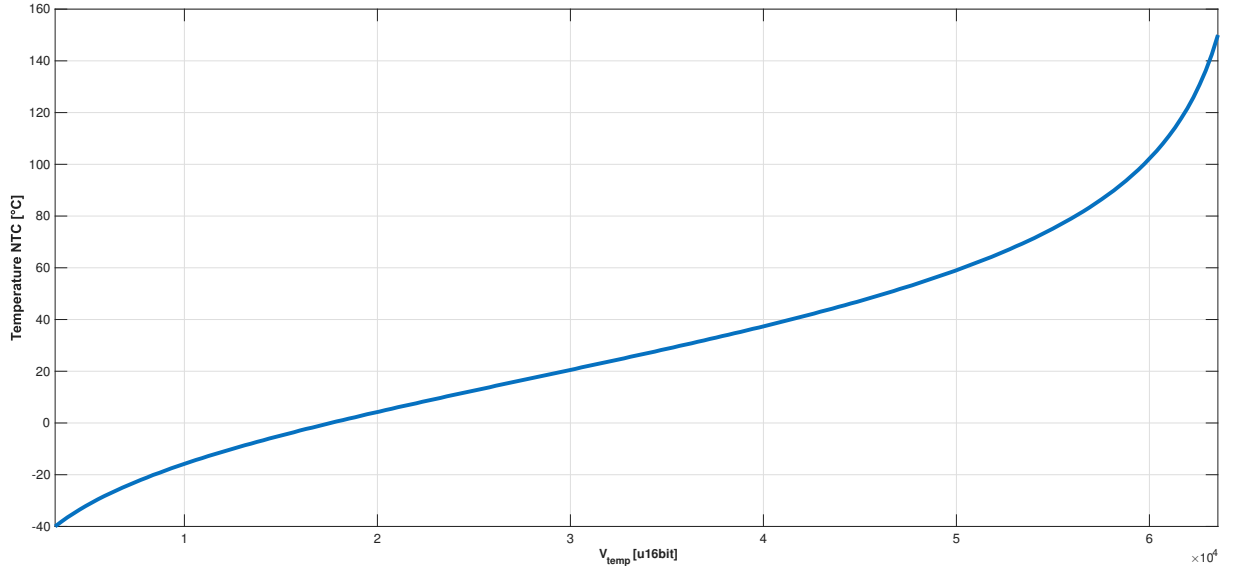


Figure 7.19: Temperature NTC vs. Resistor voltage (1-D LUT).

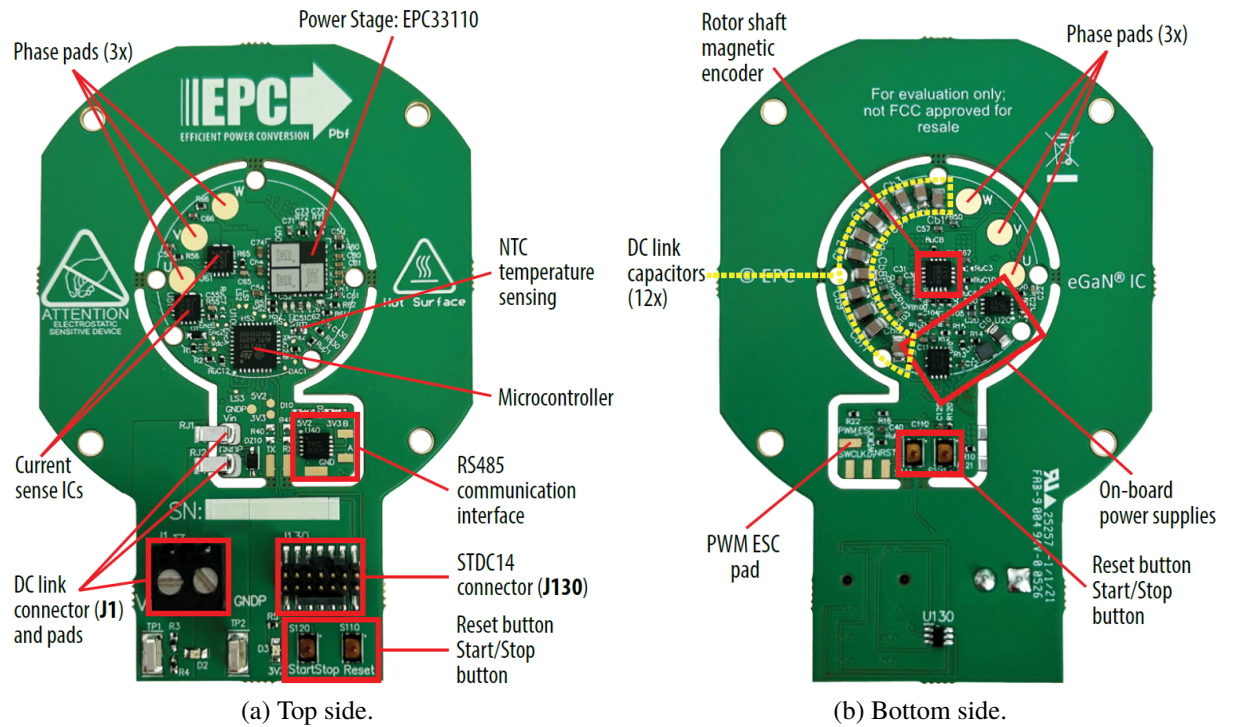


Figure 7.20: Components location on the EPC91132 evaluation board.

Regarding the connections available in the EPC91132 evaluation board, they are shown in Figure 7.21, and the related details are listed below.

1. **STDC14 connector:** J130 is a 14-pin connector of SAMTEC (PN: FTSH-107-01-L-DV-K-A-P) to interface the STLINKV3 programmer to the microcontroller, for programming it via SWD protocol and for communicating with it through the USART interface.

2. **DC input connector:** The DC link connector J1 is a 2-position PCB terminal block, Header, Wire-to-Board, Through Hole (PN: 1776113-2) of TE Connectivity.
3. **DC input pads:** when the board is used in the small form, the DC link can be interfaced through V_{IN} and GND pads, directly soldering the wires for the DC input, after removing the two resistor jumpers.
4. **Phase pads:** The phase connections are made of U, V, W pads on the board, where the connections can be soldered for the motor windings.
5. **USART pads:** The USART communication with the microcontroller can be directly accessed through RX and TX pads. To use the USART communication interface, R40 and R41 must not be placed, but the RS485 communication will not be available.
6. **RS485 pads:** The RS485 transceiver is interfaced through A, B, and G pads. To use the RS-485 communication interface, R40 and R41 have to be mounted, but the USART communication will not be available.
7. **SWD pads:** The microcontroller can be directly programmed using SWDIO, SWCLK, and NRST (optional) pads, especially when the EPC91132 inverter board is used without the outer PCB ring.
8. **PWM ESC pad:** The PWM ESC pad can be used for sending to the microcontroller a PWM signal to set the motor speed, since it is connected to the TIM2 as shown in Section 7.1.

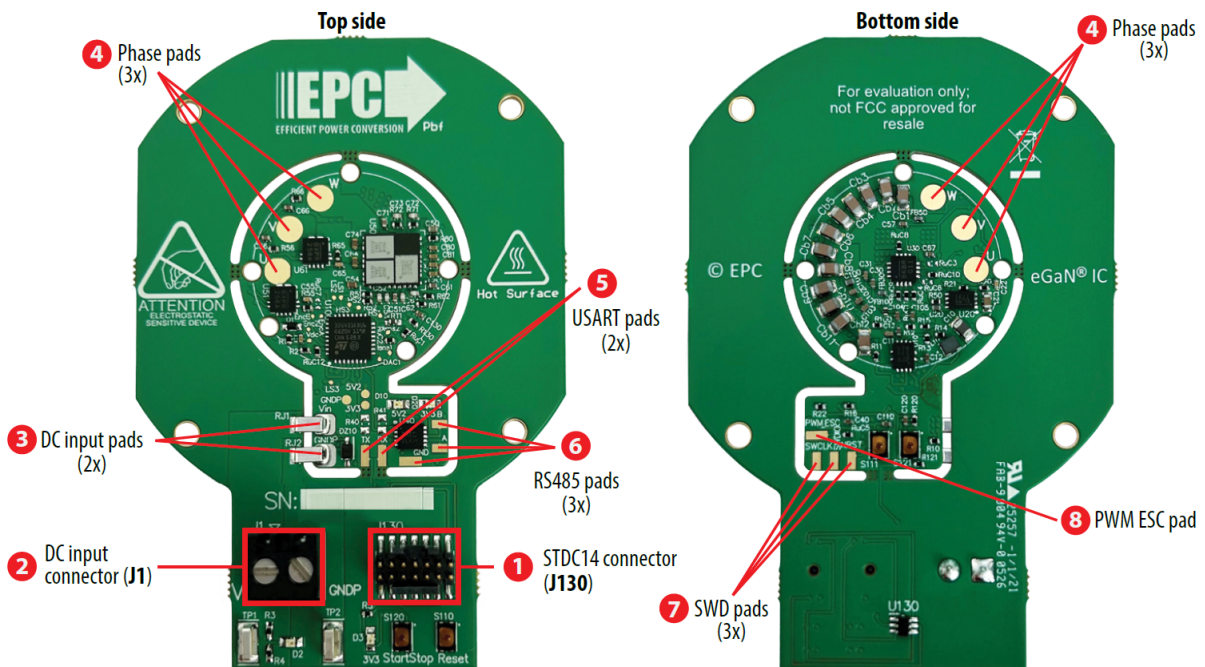


Figure 7.21: EPC91132 connections overview.

Finally, the following figures report how the PCB design of the six copper layers has been performed. The first thing to note is that most of the copper on the outer PCB frame is not connected to any net, as it is electrically isolated from the small-form PCB and from the pads of the DC input connector and STDC14 connector. In this way, even with the full-form PCB, the board's thermal behavior will be comparable to that of the small-form PCB, because all the heat dissipation will be concentrated within the 23mm-diameter circle.

The Top layer, Mid layer 2, and Bottom layer are connected to GNDP, while the Mid layer 1 and Mid layer 3 are connected to Vin. The trace routing has been performed in order to minimize the interruptions of the various planes and ease the current flow through the PCB layers. The mid-layer 4 has been dedicated to the analog ground GND, which contains most of the analog signal traces, such as the current sensor's signals, with the aim of trying to isolate them and so reducing the high-frequency noise due to the switches' operation.

The three switching nodes exiting the EPC33110 have been connected to the phase pads through large copper polygons in the top layer, minimizing their length to avoid too high stray inductances. These polygons have been replicated in the three lower layers and connected in parallel through many vias, in order to facilitate the heat dissipation generated by the phase currents.

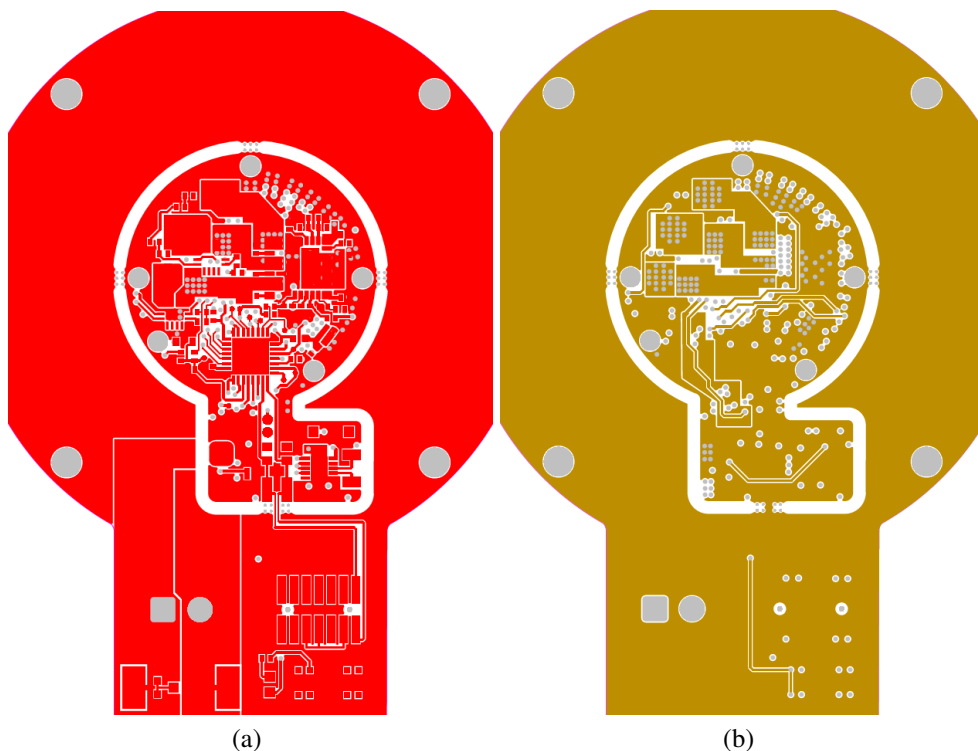


Figure 7.22: Top layer (a) and Mid layer 1 (b) design for the EPC91132 evaluation board.

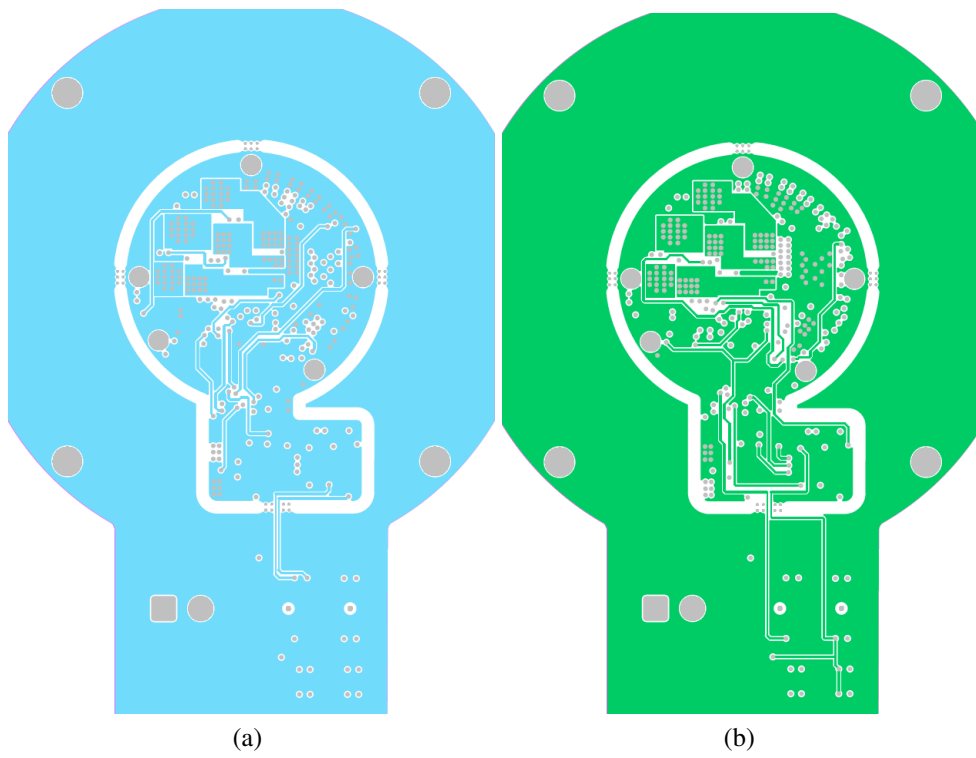


Figure 7.23: Mid layer 2 (a) and Mid layer 3 (b) design for the EPC91132 evaluation board.

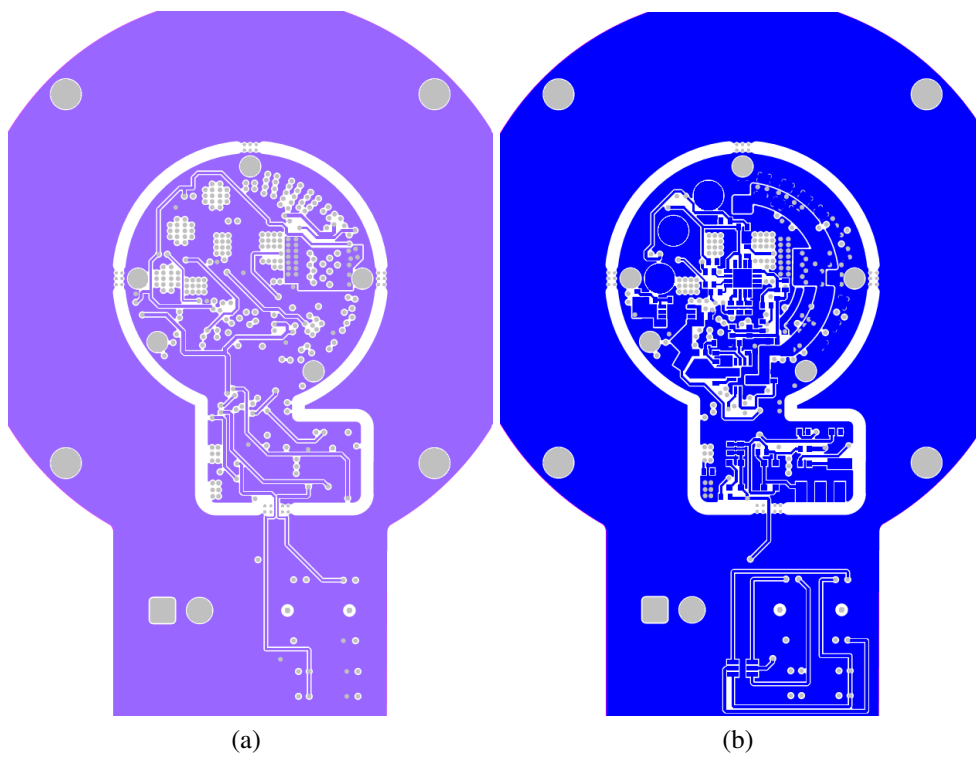


Figure 7.24: Mid layer 4 (a) and Bottom layer (b) design for the EPC91132 evaluation board.

Chapter 8

Experimental Validation of the Board

8.1 STM32 FOC Motor Control Firmware Generation

8.1.1 STM32 Motor Control SDK Overview

To evaluate the functions and performance of the EPC91132 inverter board, a motor control software development kit (SDK) provided free of charge by STMicroelectronics is used to generate the firmware to be flashed into the on-board microcontroller. X-CUBE-MCSDK STM32 motor control SDK is specifically designed for STM32 microcontrollers (including the STM32G431 family) and includes a software library that implements FOC drive for 3-phase permanent magnet synchronous motors (PMSMs), both surface-mounted (SM-PMSM) and interior (I-PMSM). This library enables quick evaluation of ST microcontrollers, completes ST application platforms, and saves time when developing motor control algorithms for applications that don't need high performance, at least in the first evaluation stage. The FOC library can be customized according to user application parameters (such as motor, sensors, power stage, control stage, and pin-out assignment) and provides a ready-to-use application programming interface (API). A PC graphical user interface (GUI), the ST motor control workbench, enables complete, easy customization of the PMSM FOC library. These projects usually include a UART interface that allows convenient real-time fine-tuning of the motor control subsystem with a remote control tool, the STM32 motor control pilot [51].

In Figure 8.1a, a typical workflow for generating motor control firmware within the X-CUBE-MCSDK is outlined. The process starts with the motor control workbench, where the user can configure the MC SDK to match the characteristics of their specific motor drive application, including the control stage, the chosen STM32 MCU, the power stage, and the motor. Based on these characteristics, the motor control workbench automatically selects the appropriate firmware components from the PMSM FOC library, computes the corresponding configuration parameters, generates an STM32CubeMX project file (.ioc extension), and compiles it. The result of this procedure is a complete software project that includes the source code and libraries needed to implement FOC control for the motors used in the application. This project can be opened in the IDE selected in the workbench (for instance, STM32CubeIDE), where users can also modify it to add their own code. However, the automatically generated firmware is often already sufficient to spin a motor with good performance, if all the application's characteristics

have been correctly chosen. In fact, the code generated by STM32CubeMx configures all the peripherals required to control the motor, initializes the MC firmware subsystem, and sets the STM32 clocks and interrupt handlers. Moreover, STM32CubeMX can be used directly to tune other aspects of the driving system related to the STM32 MCU configuration by loading the project generated by MC WB into CubeMX and modifying it; the project is then regenerated.

In Figure 8.1b the STM32 motor control firmware architecture is shown. This firmware, provided by ST, uses the low-level drivers (LL) from the Cube firmware (based on the standard CMSIS library) to implement access to peripherals as needed. This approach allows us to strike a good balance between performance and interface stability over time. However, direct access to hardware registers is sometimes used within the PMSM FOC library to enhance performance. Above the LL drivers, the STM32 MC firmware is the heart of the SDK, as it provides all the software components needed to control the PMSM using the FOC algorithm and integrates them into an MC subsystem. The firmware is divided into three main functional sets:

- The PMSM FOC Library is a collection of software components for implementing specific functions in the motor drive application, such as speed and position sensing, current sensing, and motor control algorithms. For some features, the library provides multiple implementations, enabling rapid firmware adaptation to various hardware configurations.
- The User Interface Library contains software components for communicating between the MC firmware subsystem and the external environment via a serial port or a DAC. In particular, this library is used to connect the STM32 MC WB to the motor drive application and control it through its Monitor feature.
- The Motor Control Cockpit integrates the software components into an MC firmware subsystem and implements the regulation loops. It is generated by STM32Cube to instantiate, configure, and interface the firmware components selected in the PMSM FOC library and the User Interface Library, according to the user's application [51].

Figure 8.2 shows an overview of the motor control firmware subsystem, which results from the configuration and generation of a firmware project using the STM32CubeMX and STM32 MC WB tools. In that image, both the optional and the mandatory functional blocks are shown, along with the interconnections among them. In particular, three sets of functional blocks are highlighted.

- FOC loop: it implements the FOC algorithm; therefore, at each control interrupt service routine (executed at a high rate, usually the PWM frequency), it computes the phase voltages and produces the resulting SVPWM duty cycles to apply to the transistors, for driving the motor's phases. To obtain the phase voltages, it executes all the mathematical transforms (Clarke, Park) needed to go from the measured i_a , i_b , i_c phase currents down to the i_q , i_d currents. These currents are confronted with the reference i_q , i_d by PI current regulators that output the v_q , v_d values, from which the PWM duty cycles are computed and applied to the three-phase inverter's legs.
- Reference computation loop: its aim is to compute the i_q , i_d references based on targets coming from the application, which can be a fixed or a ramp speed or torque reference. This loop first converts the application target into an initial i_q , i_d reference. It then optionally passes this reference through one or more optimization algorithms: Maximum Torque Per

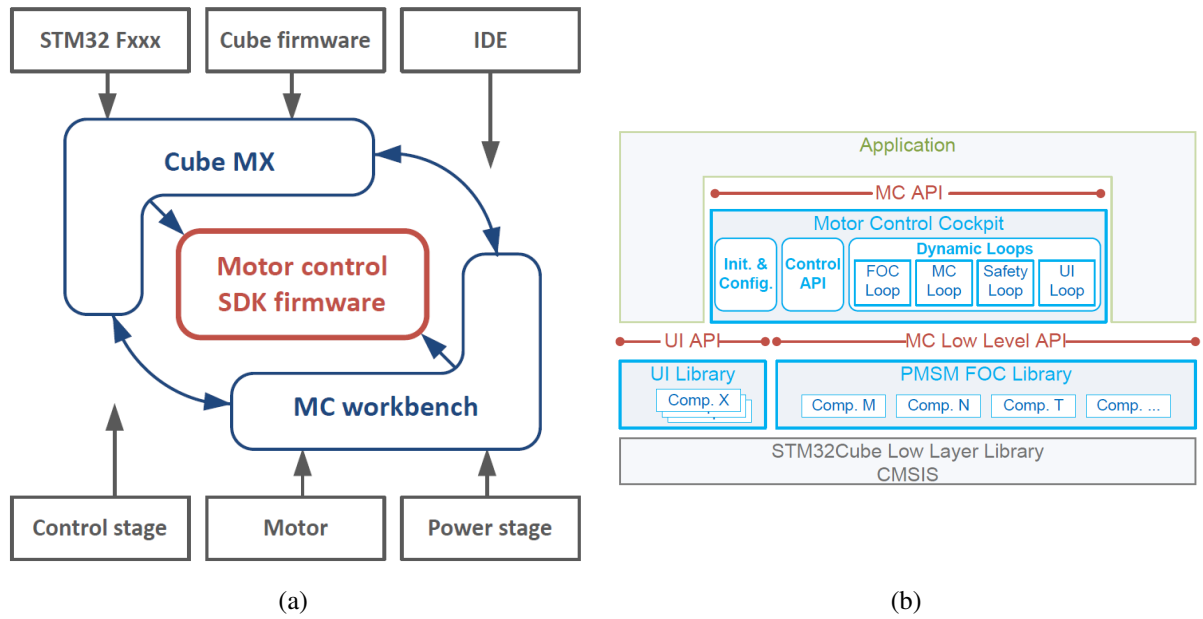


Figure 8.1: STM32 motor control SDK environment (a) and architecture (b) [51].

Ampere, Flux Weakening, or Feed Forward. Finally, the resulting i_q , i_d reference is used by the FOC loop. This process is always followed when the motor control subsystem is executing in closed-loop mode. However, depending on the chosen Speed and Position Feedback technology, a rev-up phase may be needed to take over the process until the rotor Position estimation is deemed reliable. Moreover, some applications may require the motor control to stay in open loop. This case is handled by the Open Loop Control component, which is executed instead of the normal regulation process. The Reference computation loop runs at a medium rate, typically on the SysTick interrupt.

- **Safety loop:** the functional block of this loop addresses features that respond to conditions that may endanger the system from a hardware perspective: Over- and Under-Voltage protection, Over-Heating protection, and Over-Current protection. In the case of Over Current protection, the STM32 MC firmware is designed to leverage hardware mechanisms in STM32 MCUs, such as the Timer Break input, to accelerate the system's response to an overcurrent condition. The latest item, the Safety Routines, is, for the time being, only a provision for inserting user-defined custom code that would add functional safety to the motor control subsystem. The Safety loop is executed at the same rate as the Reference computation loop – that is, at a medium rate, usually with the SysTick interrupt.

Finally, Figure 8.3 represents the motor control state machine used in the STM32 firmware subsystem, in which the blue circles indicate the states, while the arrows mark the possible transitions between the states. The state machine can only be manually changed by the use of some APIs, which can be called from any context:

- `MC_StartMotor()` triggers the target motor's start procedure, switching from IDLE to IDLE_START;
- `MC_StopMotor()` triggers the target motor's stop procedure, switching to ANY_STOP;

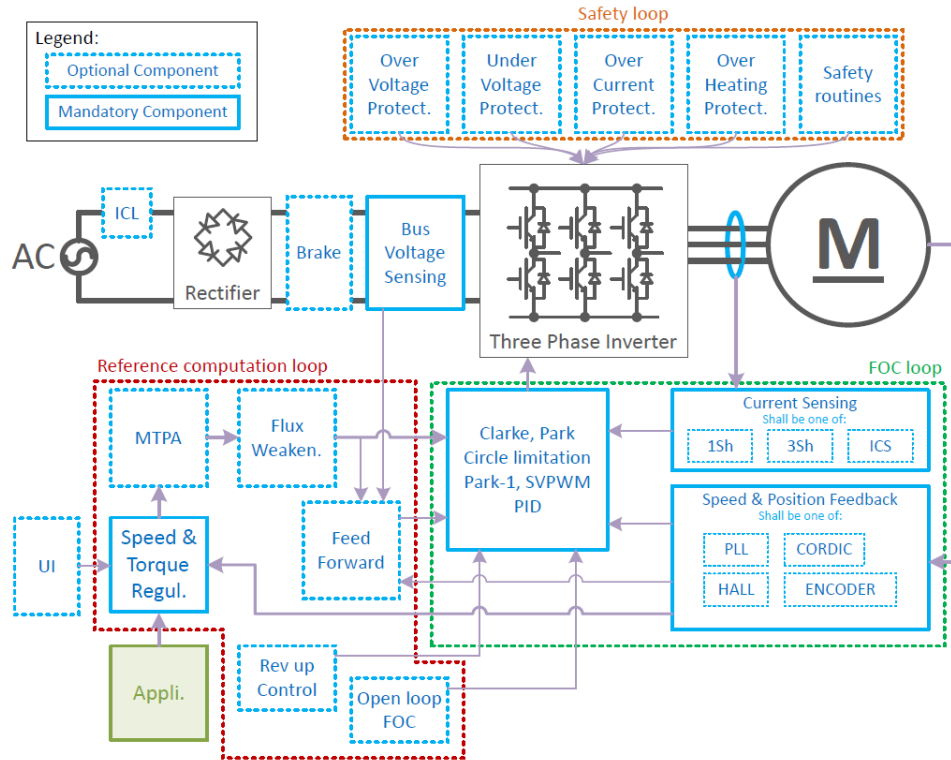


Figure 8.2: STM32 motor control software subsystem [51].

- `AcknowledgeFaultMotor()` acknowledges faults and makes the target motor ready to start, switching to `STOP_IDLE`.

The rest of the management of the motor's state machines is handled by the Reference computation loop, which is in the `TSK_MediumFrequencyTask()` functions.

Below, there is a brief description of each possible state:

- **ICLWAIT**: it is not possible to spin the motor as long as the ICL (Inrush Current Limiter) is still active;
- **IDLE**: the motor is ready to start or align, but it is not spinning;
- **IDLE_ALIGNMENT**: it is a transition state entered on the encoder alignment command;
- **ALIGN_CHARGE_BOOT_CAP**: it is a persistent state where the gate driver boot capacitors are charged before the ALIGNMENT process;
- **ALIGN_OFFSET_CALIB**: it is a persistent state where the offset of motor currents measurements is calibrated before the ALIGNMENT process;
- **ALIGNMENT**: it is a persistent state in which the encoder is properly aligned to set the mechanical angle;
- **IDLE_START**: the code to be executed only once after the start motor command, it's intended to be executed in this state;

- **CHARG_BOOT_CAP**: it is a persistent state where the gate driver boot capacitors are charged after the first start motor command;
- **OFFSET_CALIB**: it is a persistent state where the offset of motor current measurements is calibrated after the first start motor command;
- **START**: it is a persistent state where the motor start-up is intended to be executed;
- **START_RUN**: the code to be executed only once between START and RUN. It's intended to be executed in this state;
- **RUN**: it is a persistent state in which the motor is running, as long as a stop motor command is not executed;
- **ANY_STOP**: the code to be executed only once between any state and STOP; it's intended to be executed in this state;
- **STOP**: it is a persistent state in which the motor is stopped, after passing through the ANY_STOP state;
- **STOP_IDLE**: the code to be executed only once between STOP and IDLE is intended to be executed in this state;
- **FAULT_NOW**: it is a persistent state where the application arrives when a fault is detected, and the state machine remains here until the fault disappears;
- **FAULT_OVER**: it is a persistent state in which the application is intended to remain when the fault conditions disappear, until the user acknowledges the fault condition.

8.1.2 Board Designer

The first step in generating the FOC firmware to flash into the microcontroller is to create a custom board project (i.e., a JSON file) to use within an MC Workbench project. This can be easily done with the Board Designer tool in the same MC Workbench. In particular, since the EPC91132 is an integrated motor drive inverter with an on-board microcontroller, at the beginning of the design process, within the board designer, the "Inverter" type has to be chosen. After choosing the microcontroller (STM32G431KBUx), the clock source (internal RC oscillator), the board rated current (15 A), the voltage range (10 V - 60 V), and the rated power (700 W), the board project has to be configured with all the features, according to the hardware specifications of the EPC91132.

Figure 8.4 shows the "Motor Features" added to the board project. Below are listed their configurations:

- **Current Sensing**: Two insulated current sensors as topology, with an ICS gain of 0.044 V/A. The Phase U current signal is routed to PA5, while the Phase V current is routed to PB0.
- **Over Current Protection**: External comparators OCP mode, with OC signal polarity active low. OCPn signal routed to PA6 or PC15 (for SPI interface with the encoder).

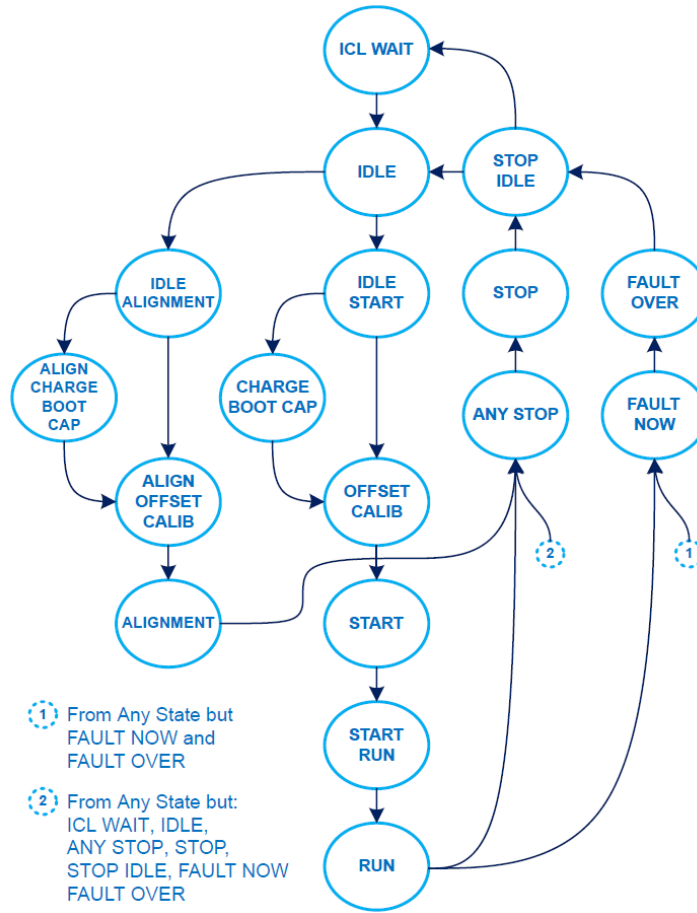


Figure 8.3: STM32 motor control state machine [51].

- Bus Voltage Sensing: VBusSensing type, with a bus voltage divider of $19.658 \left(\frac{R1+R2}{R2} \right)$, $R1 = 100k\Omega$, $R2 = 5.36k\Omega$. The Vdc signal is routed to PF1.
- Temperature Sensing: NTCThermistor type, with $v_0 = 1650mV$, $t_0 = 25^\circ C$, $14.3mV/^\circ C$ as gain, and $150^\circ C$ for the maximum sensor temperature.
- Speed and Position Sensing: Quadrature Encoder as speed sensor mode, with Absolute position. EncA signal routed to PB4, EncB to PB5, and EncZ to PB7.
- Phase Voltage Generation: High- and Low-Side driving topology, with a minimum dead time of 20 ns and a maximum of 100 ns. Both high- and low-side switches are driving polarity-active high, with a maximum switching frequency of 100 kHz. PWMUH signal routed to PA8, PWMVH to PA9, PWMWH to PA10, PWMUL to PA11, PWMVL to PA12, PWMWL to PF0.

Figure 8.5 shows the "Additional Features" added to the board project. Below are listed their configurations:

- StartStop Button: Push-button type, with a rising edge to trigger the button, and no Pull-up/Pull-down for the GPIO configuration. The StartStop signal is routed to PB6.

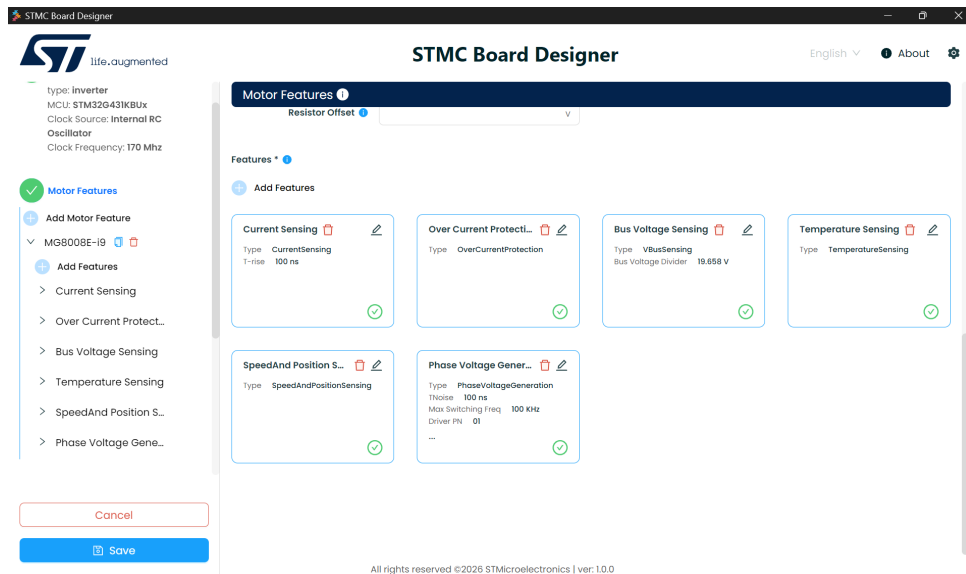


Figure 8.4: STMC Board Designer window showing the motor features.

- Serial Port Communication: Uart2WiresCommunication type, with TX signal routed to PA2, while RX signal to PA3.
- Electronic Speed Controller: ESCPWMControl type, with the PW input signal routed to PA15.

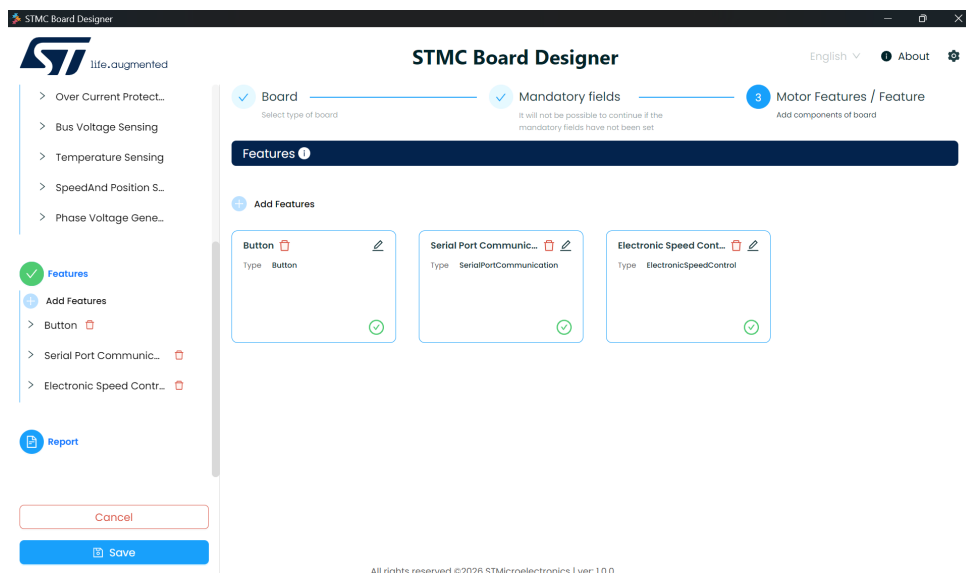


Figure 8.5: STMC Board Designer window showing the additional features.

8.1.3 Firmware Generation

The next step is to configure the MC Workbench project and then generate the motor control firmware, which will use the parameters specified in this project. Since many parameters can

vary depending on the motor and the type of control, the following configuration example focuses on generating firmware to control the Vertiq 23-06 220 KV drone motor, with the option to use the PWM ESC input.

Figure 8.6 shows the main window of the MC Workbench example project, while Figure 8.7 contains the pinout configuration automatically generated in STM32CubeMX from the MC Workbench project. Below are listed the stages' configurations:

- **Motor:** according to the Vertiq motor's parameters exposed in Table 6.5; SM-PMSM as Motor magnetic structure, 7 Pole Pairs, 10 Apk as Max Current, 30 V as Max DC Voltage, $R_S = 2.4\Omega$, $L_S = 785\mu H$, BEMF Constant equal to 3.61 Vrms/kRPM. The maximum application speed has been set to 3400 RPM, and the encoder's pulses per mechanical revolution to 1024.
- **Power Supply:** Max Application Current set to 10 A, with a rated bus voltage of 24 V.
- **PWM Generation:** PWM frequency set to 100 kHz, PWM idle state for both high- and low-side set to turn off, 50 ns of dead time, 10 ms for the Boot Capacitor Charging. All six PWM signals are provided by the Advanced motor control timer TIM1; PWMUH - TIM1_CH1, PWMVH - TIM1_CH2, PWMWH - TIM1_CH3, PWMUL - TIM1_CH1N, PWMVL - TIM1_CH2N, PWMWL - TIM1_CH3N.
- **Speed Sensing Selection:** Quadrature Encoder for the Speed Sensor Mode.
- **Current Sensing:** Regulator execution time is set to 30 μs (3 PWM cycles) because the minimum achievable with this firmware is 29 μs . The sampling time has been configured equal to 6.5 ADC clock cycles (153 ns). The Phase U current signal is read by ADC2_IN13, while the Phase V current signal is read by ADC1_IN15. The OCPn signal is connected to TIM1_BKIN.
- **Bus Voltage Sensing:** The sampling time has been set to 47.5 ADC clock cycles (1 μs). The Vdc signal is read by ADC2_IN10. The overvoltage threshold is 29 V, and the undervoltage threshold is 12 V.
- **Temperature Sensing:** The sampling time has been set to 47.5 ADC clock cycles (1 μs). The Temp signal is read by ADC1_IN1. The over-temperature protection triggers at 130 °C, with a hysteresis of 10 °C.
- **Speed Sensing Configuration:** Max Num. Errors before fault equal 30; Start-up electrical alignment with a ramp of 1000 ms, a final Id current of 1 A, and an angle of 90°. Reverse counting direction is enabled because the magnetic encoder used in the EPC91132 has a default positive rotation opposite to that of the ST motor control firmware.
- **Drive Settings:** Open Loop enabled. Speed control as Control mode. No Modulation flags. $K_p = 100/64$, $K_i = 25/4096$ for both Id and Iq current regulators. $K_p = 8000/512$, $K_i = 500/16384$ for the speed regulator, with an execution rate of 1 ms.
- **Stage Configuration:** Electronic Speed Controller enabled.
- **User Interface:** Start/Stop on Control Board enabled. Motor Control Protocol Over USART A, with a Baudrate of 921600, Data Log enabled, Max Signals to plot equal to 10, and a Buffer Size of 2048.

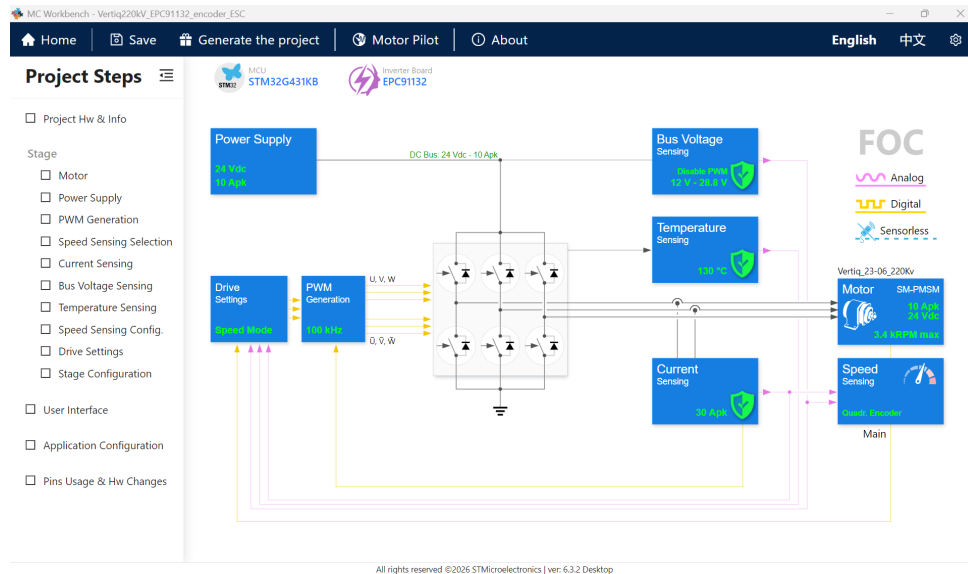


Figure 8.6: STMC Workbench example project window.

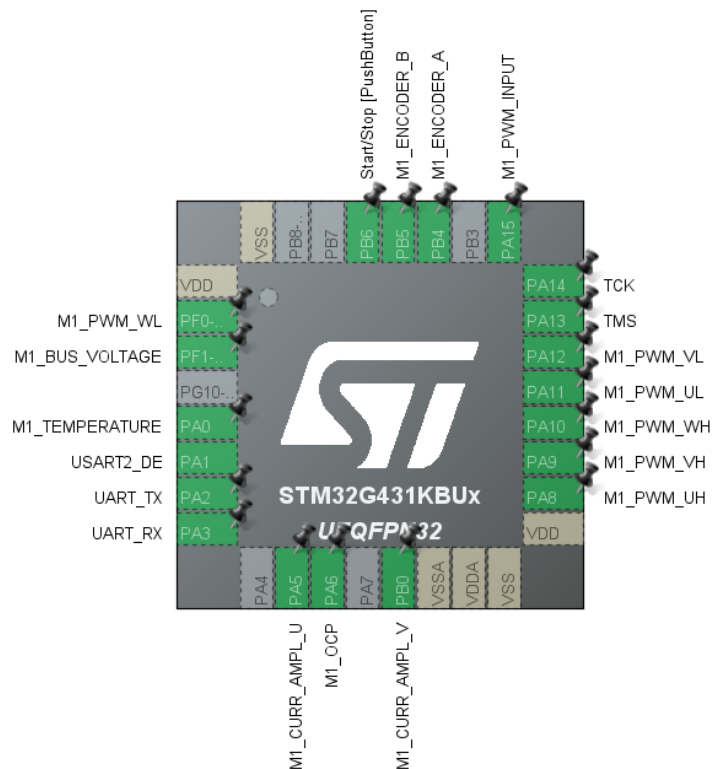


Figure 8.7: STM32CubeMX example project pin configuration.

8.1.4 NTC Temperature Sensing Implementation

Since the implementation of the temperature sensing through the MC Workbench offers only the possibility of choosing a constant mV/ °C gain, some changes to the firmware have been carried out. As has been explained in Section 7.6, a 1-D LUT has been obtained through a MATLAB script, which allows for computing the NTC sensor temperature from the voltage sensed on the

R130 resistor in series with the NTC.

The modifications affect the middleware file related to the MC Workbench implementation of NTC temperature sensing, named *ntc_temperature_sensor.c*. The first step was to add some floating variables to the *NTC_Handle_t* type structure, declared by default. These variables are used by a dedicated function to retrieve the exact NTC sensor temperature. As shown in Figure 8.8a, the new variables are:

- **V_max**: maximum voltage reference;
- **V_min**: minimum voltage reference;
- **dV**: increment between consecutive LUT points, $\frac{V_{\max}-V_{\min}}{\text{length}(\text{Temp_out})-1}$;
- **dV_inv**: inverse of dV, to avoid division operations;
- **temp**: current NTC sensor temperature;
- **Temp_out**: LUT vector used for linear interpolation from the input voltage.

Then, these variables are defined in the *mc_config_common.c* code file, from row 113 to row 119, inside the *TempSensor_M1* structure (Figure 8.8b). Finally, Figure 8.8c shows the NTC sensor temperature implementation. It reads the 1-D LUT and saves the output in both the temp variable (floating number) and the wTemp local variable (integer number). The wTemp variable represents the output of the predefined *NTC_GetAvTemp_C* and is used to show the actual sensed temperature in the MC Workbench real-time GUI (MC Motor Pilot).

(a) *ntc_temperature_sensor.h* (b) *mc_config_common.c* (c) *ntc_temperature_sensor.c*

Figure 8.8: NTC temperature sensing code implementation modifications.

8.2 Switching Performances

The first tests conducted on the EPC91132 inverter board focus on the switching performance of the integrated GaN power FETs. In particular, the commutation transients in the three inverter legs are investigated under different conditions by varying the DC bus voltage and the phase current. These tests aimed to ensure that the switching nodes commuted properly at all operating voltages and currents, without excessive ringing or spikes, and to identify the minimum dead time needed to minimize reverse conduction and motor current waveform distortion while avoiding shoot-through in the inverter legs. As shown in Figure 8.9, these tests were performed using the MG8008E-i9 V3 servomotor, driven in open-loop current mode (I-Hz control), with

the EPC91132 not inserted into the motor's casing because the magnetic encoder was not used in this configuration. The board was supplied with 24 V_{DC} and 48 V_{DC} at a switching frequency of 100 kHz (which does not affect the investigation of the switching transient [52]), a current amplitude from 0 A to 10 A , and a dead time of 50 ns . The voltage waveforms of the switching node shown below were measured with a passive voltage probe connected to a digital oscilloscope. All the acquisitions have been triggered at the specific current value of that test, which has consistently resulted in constant values during the $50\text{ }\mu\text{s}$ acquisition window, since the fundamental current period was considerably higher (about 30 ms).

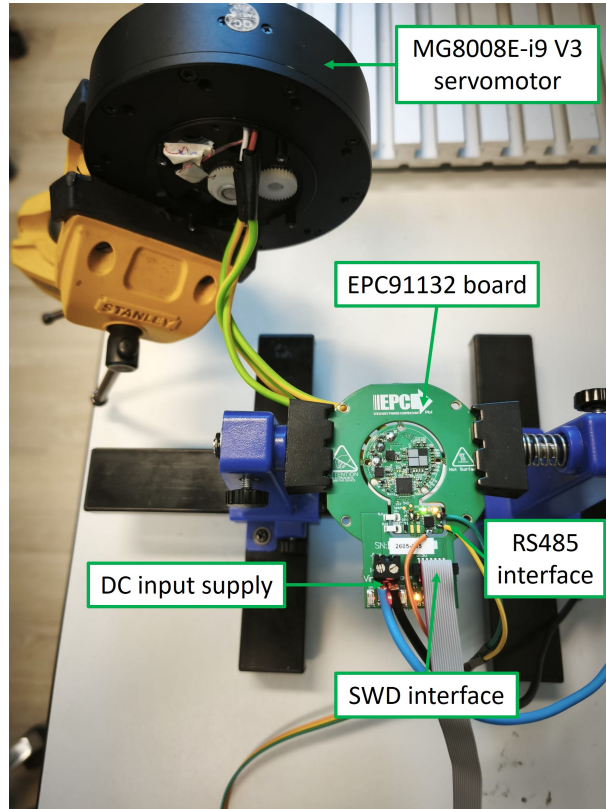


Figure 8.9: Experimental setup during switching tests.

In all the oscilloscope's screenshots shown in the following figures, the channel C1 refers to the switching voltage of phase U, and the channel C2 refers to the phase current of phase U. The zoom Z1 refers to the commutation detail related to the positive voltage slew rate (high-side turn-on and low-side turn-off), and the zoom Z3 refers to the commutation detail related to the negative voltage slew rate (high-side turn-off and low-side turn-on). Moreover, for each acquisition, the following measures have been set up, from which the mean value is considered among all the statistics provided by the oscilloscope's computation tool:

- P1: positive voltage slew rate, 10% to 90%;
- P2: negative voltage slew rate, 90% to 10%;
- P3: positive voltage slew rate, 20% to 80%;
- P4: negative voltage slew rate, 80% to 20%;

- P5: positive overshoot, in percentage;
- P6: negative overshoot, in percentage;
- P7: switching frequency;
- P8: mean value of the phase current;

In Figure 8.10, the SW voltage waveforms for phase U are shown with the load current set to 0 A, obtained by disconnecting the inverter board from the servomotor and applying a 50% duty cycle to all three phases. At 24 V_{DC}, the rising-voltage slew rate was measured at nearly 10 V/ns, which is the switching rate specified in the EPC33110 datasheet and was obtained by internally tuning the switching times. In both figures, it can be observed that the behavior of the switching node at no load shows some ringing and overshoot during the rising slew rate, but they are limited in spite of the high switching rates, attesting that the layout of the board has been properly realized to minimize stray inductances due to the copper traces.



Figure 8.10: Switching node voltage measured on phase U at 24 V_{DC} (a) and 48 V_{DC} (b), with 0 A load current.

Regarding the switching node falling commutation, if the current is positive, three switching events can happen, depending on the dead time and the current:

- Zero-voltage switching (ZVS): this event occurs when the low-side FET turns on exactly as the switching-node voltage reaches 0 V, as shown in Figure 8.12a. So, in this specific case, with a current of 0.6 A, the low-side FET conducts with a drain-to-source voltage of 0 V, minimizing its switching losses.
- Voltage variation and partial hard switching (PHS): if the current amplitude is below the ZVS threshold, a PHS event follows the switching-node transient. As can be observed in Figure 8.11a, during the dead time, the voltage decreases with a slew rate that depends on the actual current amplitude, the devices' parasitic output capacitances (C_{OSS}), and the load. After the dead time, the low-side switch turns on, indicating partial hard-switching commutation, so the switching-node voltage drops to the FET's conduction-state value.
- Voltage-fall transient and reverse conduction (RC): if the current amplitude exceeds the ZVS threshold, the switching node voltage drops to 0 V before the dead time ends. Therefore, the low-side switch operates in RC mode until the high-side FET turns on, with a switching-node voltage equal to $-V_{RC}$ due to the equivalent-diode behavior during the GaN FET's reverse conduction. This switching can even be observed in Figure 8.13a.

On the other hand, if the current is negative, the switching-node waveforms during transients show no differences across different current amplitudes because the difference in slew rates is mainly determined by the device technology. In fact, the parasitic capacitance C_{OSS} of the device affects the voltage falling time. As can be seen in Figures 8.11b, 8.12b, and 8.13b, this switching event is characterized by an RC phenomenon that lasts throughout the dead time. During this time interval, the switching node voltage reaches $V_{RC}+V_{DC}$, after which a hard-switching event with a rapid SW voltage drop occurs, lasting a few nanoseconds [52].

Similar considerations can also be applied to the switching node rising commutation, since its behavior is dual to the falling commutation, with only the current sign changed. Therefore, in Figures 8.11a, 8.12a, and 8.13a, the switching node waveforms are very similar for different current amplitudes, and all the switching events are characterized by an RC phenomenon during the deadtime, in which the switching node voltage assumes the value of $-V_{RC}$, and then a hard-switching event concludes the commutation.

When the current is negative, instead, the switching node rising commutation exhibits a ZVS event in Figure 8.12b, a PHS event in Figure 8.11b, and an RC event in Figure 8.13b.

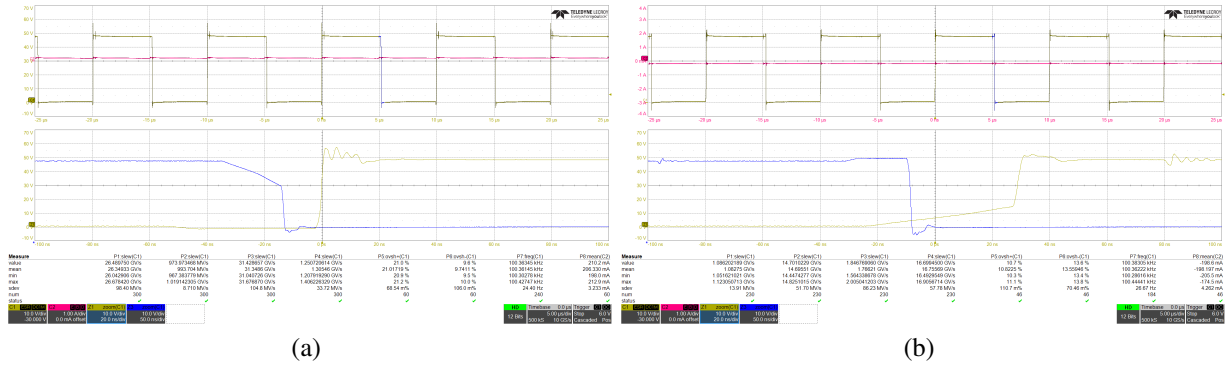


Figure 8.11: Switching node voltage measured on phase U at 48 V_{DC} with 0.2 A (a) and -0.2 A (b) load current.

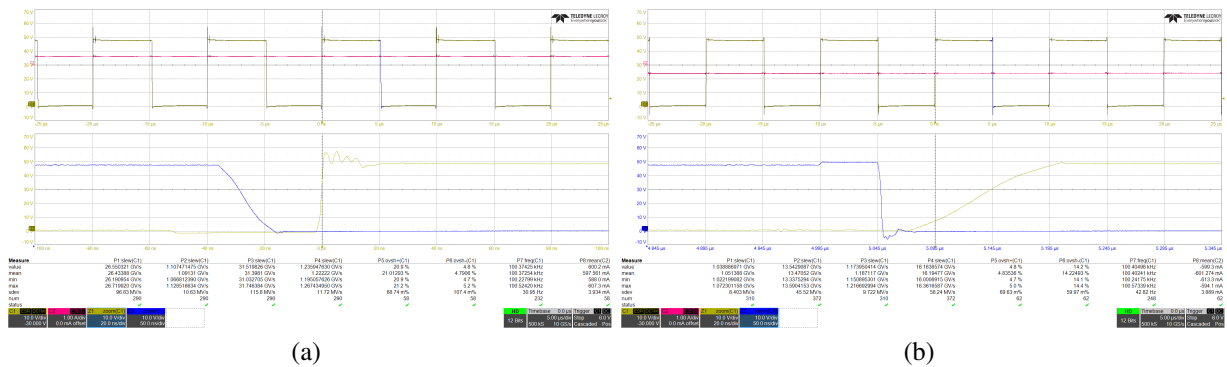


Figure 8.12: Switching node voltage measured on phase U at 48 V_{DC} with 0.6 A (a) and -0.6 A (b) load current.

Tables 8.1 and 8.2 report measurements of the phase U switching-node voltage at 24 V_{DC} and 48 V_{DC}, respectively, for different current levels. The same results have been obtained by inspecting the other two phases, so they have not been included in the tables.


 Figure 8.13: Switching node voltage measured on phase U at 48 V_{DC} with 5 A (a) and -5 A (b) load current.

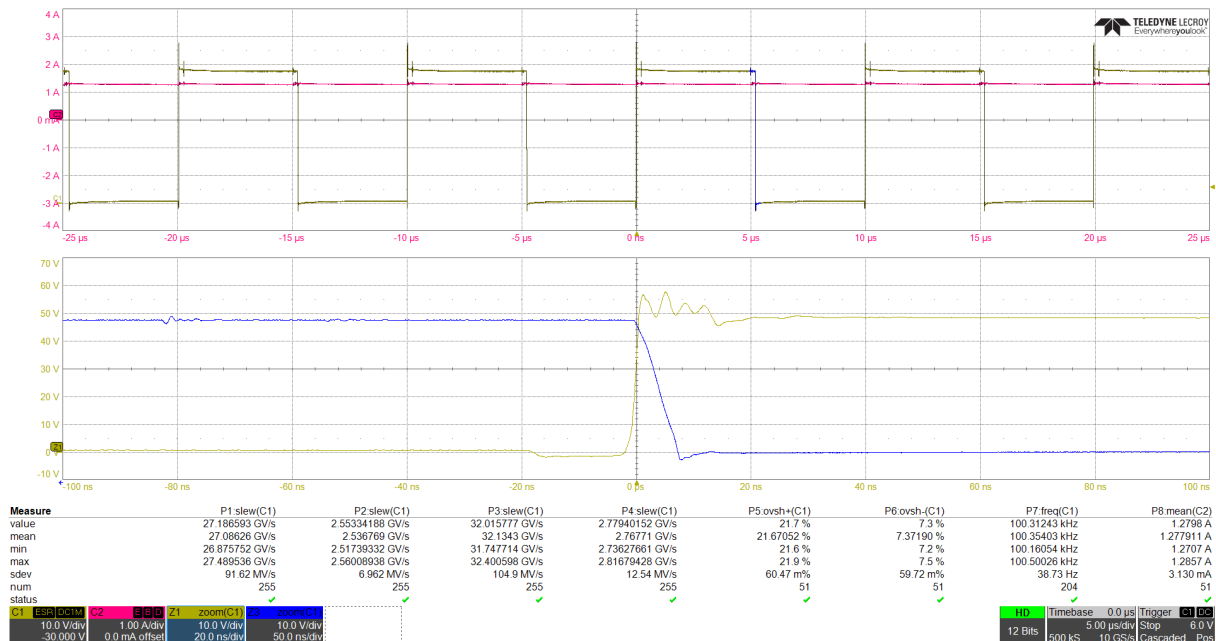
 Table 8.1: Measurements on switching voltage of phase U at 24 V_{DC}.

I_{phase} [A]	slew+90/10 [V/ns]	slew-90/10 [V/ns]	slew+80/20 [V/ns]	slew-80/20 [V/ns]	Overshoot+ [%]	Overshoot- [%]
0	10.634	6.731	12.054	6.959	44.92	13.42
0.1	13.545	0.461	14.844	0.545	38.46	11.37
-0.1	0.595	8.499	1.734	8.938	22.56	17.21
0.4	13.678	0.540	14.908	0.564	39.47	9.53
-0.4	0.471	8.321	0.485	8.717	9.40	17.80
1	13.938	2.048	15.285	2.128	38.15	18.00
-1	1.339	7.932	1.427	8.404	15.76	17.57
2	13.937	2.779	15.310	2.909	38.15	20.14
-2	2.739	7.318	2.933	7.809	22.23	16.45
5	13.431	6.973	15.146	7.352	38.38	22.96
-5	6.684	5.605	7.106	5.928	25.69	16.14
10	11.214	11.305	13.337	13.119	37.58	24.26
-10	13.910	3.487	15.936	3.434	31.05	13.74

Since it has been experimentally proven that the integrated GaN FETs in the EPC33110 can switch at high voltage slew rates, the dead time has been reduced to 20 ns, and this value has been used for all subsequent tests. In Figure 8.14, the switching node voltage waveform is represented at 48 V_{DC} and 20 ns of dead time. Since the time during which both FETs are turned off is shorter than in the previous figures, the ZVS threshold in this condition is 1.3 A, which is higher than the 0.6 A measured with 50 ns of dead time.

Table 8.2: Measurements on switching voltage of phase U at 48 V_{DC}.

I _{phase} [A]	slew+90/10 [V/ns]	slew-90/10 [V/ns]	slew+80/20 [V/ns]	slew-80/20 [V/ns]	Overshoot+ [%]	Overshoot- [%]
0	23.918	11.091	29.180	12.642	24.68	13.01
0.2	26.349	0.993	31.349	1.305	21.02	9.74
-0.2	1.083	14.696	1.766	16.756	10.82	13.56
0.6	26.434	1.091	31.398	1.222	21.01	4.79
-0.6	1.051	13.471	1.187	16.195	4.84	14.23
1	26.695	1.852	31.653	2.066	21.27	8.07
-1	1.803	13.086	2.037	15.908	8.30	14.24
2	26.819	3.956	31.789	4.354	21.45	12.25
-2	4.016	12.219	4.397	15.139	13.02	14.24
5	26.693	10.169	31.719	11.091	21.78	16.71
-5	10.096	10.153	11.148	13.219	18.43	13.79
10	23.769	18.118	29.061	19.917	21.05	19.17
-10	17.759	7.777	18.786	14.654	20.35	13.13

Figure 8.14: Switching-node voltage measured on phase U at 48 V_{DC} with a 1.3 A load current (20 ns dead time).

8.3 Encoder Misalignment Compensation

In order to perform the experimental tests with the MG8008E-i9 V3 servomotor described in Section 8.6, some control problems due to an encoder misalignment were solved by adding some code in the firmware. In particular, as can be seen in Figure 8.15a, large current oscillations are produced by the encoder misalignment with the rotor magnet and by non-idealities errors as soon as the speed loop is closed using the encoder position sensing, also imposing a relatively low speed (500 rpm). These problems have emerged only for the humanoid joint motor, probably because of the different magnet used in the Vertiq motors (smaller and further from the board) and for the smaller number of pole pairs of the latter (7 against 21). To mitigate the current oscillations, a compensation strategy is implemented in the motor control firmware:

- Mechanical angle's reading from the encoder is collected during an Open Loop I-Hz control at fixed speed (800 rpm), and it is compared to an ideal angle ramp to compute the error's profile (Figure 8.16). These data have been collected through the MCUVIEWER tool [53], which allows for debugging the microcontroller via SWD communication. The error between the two ramps has been computed for both the mechanical and electrical domains. In Figure 8.17, it can be observed that the electrical angle errors are 21 times bigger (due to the pole pairs) than the mechanical ones, and the former produce the current oscillations, because the electrical angle is used in the id/iq control loops rather than the mechanical one. So, these oscillations can be interpreted as the result of the oscillations on the id/iq references, which are produced by the measured speed oscillations due to the encoder's errors.
- 1-D LUT of the mechanical angle error is obtained through a MATLAB script, following the same process adopted for the NTC temperature sensing implementation. In Figure 8.18, there is the graphical representation of the 1-D LUT, in which the measured mechanical angle from the incremental encoder is, while the output is the error that must be compensated to obtain an ideal angle ramp at constant speed.
- The code implementation of the 1-D LUT is shown in Figure 8.19. For each measured mechanical angle, the related error is computed from the LUT in real time, paying attention to correctly use the absolute zero position (retrieved from the Z encoder signal at the startup). The modifications affect the middleware file related to the MC Workbench implementation of encoder speed feedback, named *encoder_speed_pos_fdbk.c*. The first step was to add some floating variables to the *SpeednPosFdbk_Handle_t* type structure, declared by default. These variables are used by a dedicated function to retrieve the encoder's angle error depending on the measured mechanical angle. As shown in Figure 8.19a, the new variables are:

- *Theta_max_enc*: maximum theta reference;
- *Theta_min_enc*: minimum theta reference;
- *dTheta_enc*: increment between consecutive LUT points, $\frac{\text{Theta_max_en} - \text{Theta_min_en}}{\text{length}(\text{Encoder_comp}) - 1}$;
- *dTheta_inv_enc*: inverse of *dTheta_enc*, to avoid division operations;
- *enc_error*: current mechanical angle error;
- *enc_corr*: current corrected mechanical angle;

- Mec_enc_offset: mechanical error offset obtained after the parking alignment;
- comp_flag: a boolean flag to activate the compensation after the initial parking alignment;
- Encoder_comp: LUT vector used for linear interpolation from the input mechanical angle.

Then, these variables are defined in the *mc_config_common.c* code file, from row 51 to row 59, inside the *Encoder_M1_Super* structure (Figure 8.19c). Finally, Figure 8.19b shows the encoder angle compensation implementation. In particular, inside the predefined ENC_CalcAngle function, the local variable mecAngle is corrected using the related error obtained from the added ENC_error function, which is shown in Figure 8.19d. This correction is actually used by the motor control firmware only after the completion of the initial parking alignment (monitored by the comp_flag variable), since the data inserted in the 1-D LUT has been obtained by referring to the input mechanical angles to the absolute position measured during the preliminary test with the I-Hz control (stored in the wMe-cAngle variable inside the *Encoder_M1_Super* structure).

In Figures 8.15b and c, it can be observed how this compensation strategy attenuates the current oscillations, also when a load torque is applied at the rotor shaft.

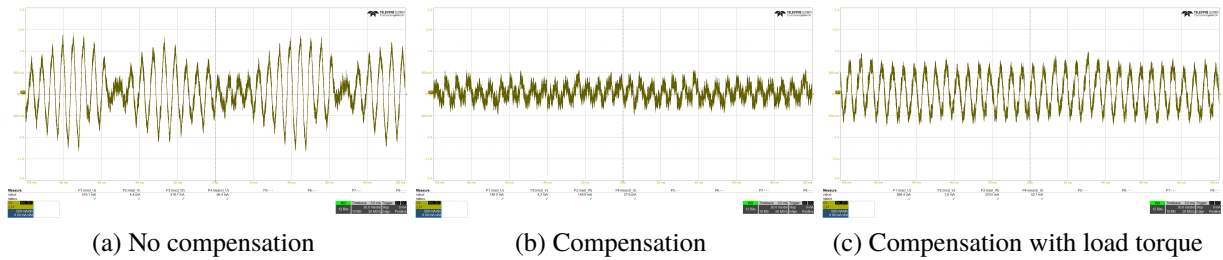


Figure 8.15: Effect of the compensation strategy on the Phase A current measurement.

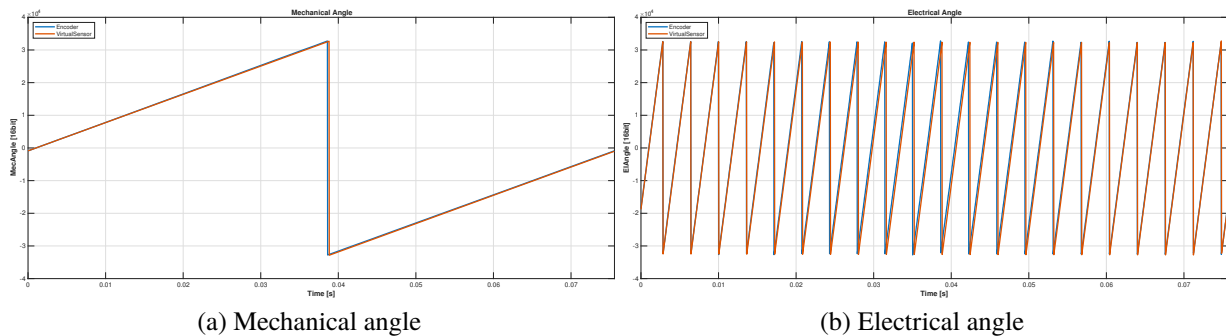


Figure 8.16: Comparison between the measured angle and the ideal angle ramp.

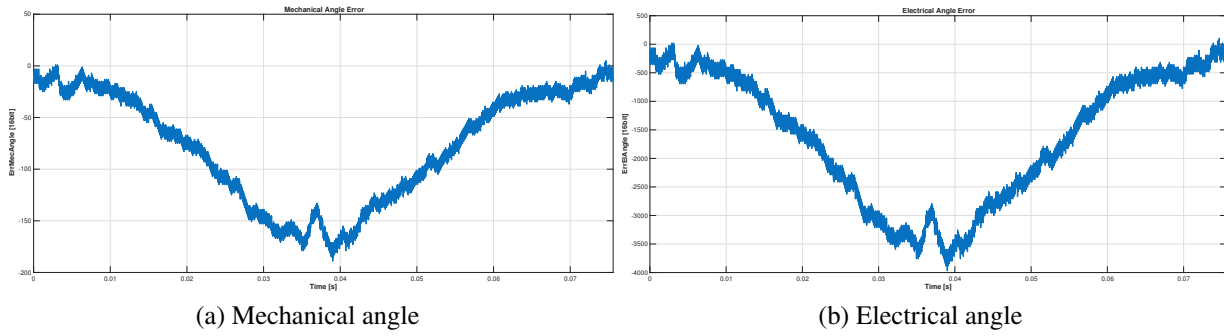


Figure 8.17: Errors between the measured angle from the encoder and the ideal ramp.

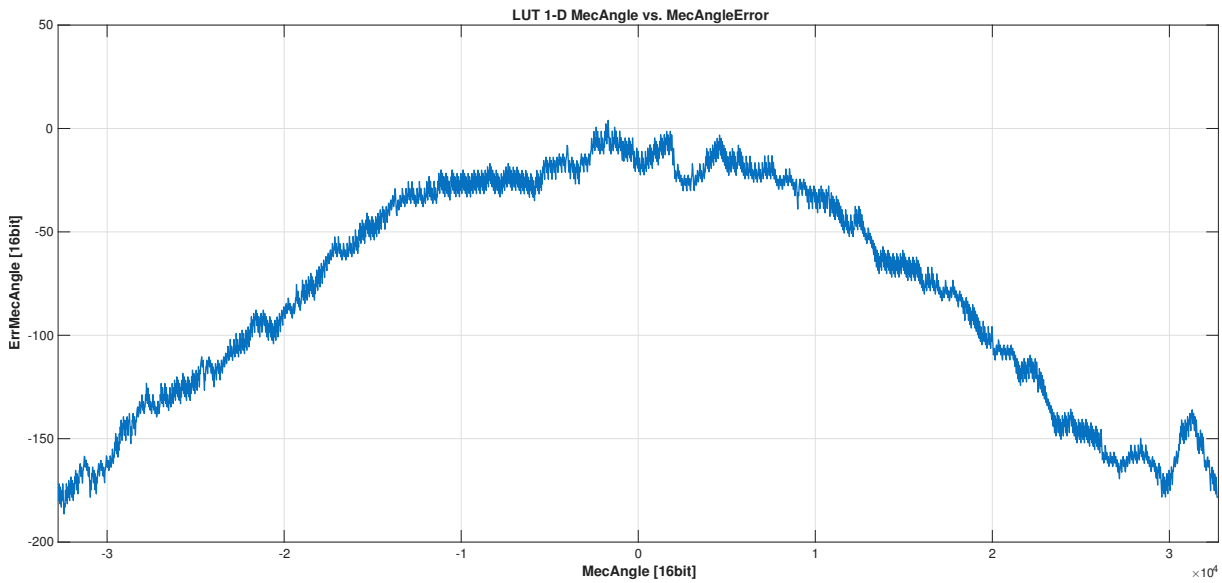


Figure 8.18: Mechanical angle error vs. Measured mechanical error (1-D LUT).

8.4 Thermal Behavior in Steady State Conditions

The EPC91132 motor drive inverter was tested in a steady state condition. This analysis was performed to outline the thermal performance of the board at different RMS phase currents delivered. The tests were carried out using a 24-48 V_{DC} supply voltage while switching at 60 kHz, 80 kHz, and 100 kHz, 20 ns dead-time setting, and powering a 3 kW servo motor at 100 rpm. In particular, the motor is a 48 V PMSM motor from DMKE, with a rated torque of 10 Nm, a rated speed of 3000 RPM, and a rated current of 80 A_{RMS}. The choice of not using the MG8008E-i9 V3 servomotor comes from the fact that these tests were performed in open-loop current mode (I-Hz control), which allows setting any current amplitude without the need for a load. However, since this control bypasses the use of the FOC loop, the imposed current is mainly put on the motor's d-axis, causing higher joule losses. Therefore, the 3kW motor was chosen to avoid overheating the MG8008E-i9 V3 servomotor.

The steady state thermal performance summary for the EPC91132 board is shown in Figures 8.20 and 8.21. When driving the motor (at a fixed speed of 100 RPM) at an ambient temperature of 24°C, with 100 kHz, 80 kHz, and 60 kHz PWM frequencies, 24 V_{DC} supply, and natural convection cooling, the EPC91132 can deliver 7 A_{RMS} per phase without a heatsink with

```

50 typedef struct
51 {
52     /* Number of time the average mechanical speed is not valid. */
53     uint16_t hSpeedFromNumber;
54     /* Coefficient used to transform electrical to mechanical quantities and
55        viceversa. It usually coincides with motor pole pairs number. */
56     uint16_t hElToMechRatio;
57     /* The speed unit value is defined into mc_sts_types.h.
58        [SPEED_UNIT](measurement_units.md) in tenth of Meter. */
59     uint16_t SpeedUnit;
60     /* Maximum value of not valid speed measurements before an error is reported. */
61     int16_t hMaxInvalidSpeedFromNumber;
62     /* Estimated electrical angle reported by the implemented speed and position
63        method. */
64     int16_t hMechAngle;
65     /* Instantaneous measure of rotor mechanical angle. */
66     int16_t hMechAngle;
67     /* Mechanical angle frame based on coefficient hElToMechRatio. */
68     int16_t hMechAngle;
69     /* Average mechanical speed expressed in the unit defined by
70        [SPEED_UNIT](measurement_units.md). */
71     int16_t hAvgMechSpeedUnit;
72     /* Instantaneous electrical speed expressed in Digit Per control Period
73        ([dpp](measurement_units.md)). */
74     int16_t hElecSpeedDpp;
75     /* Instantaneous computed electrical speed, expressed in
76        [dpp](measurement_units.md). */
77     int16_t hInstantaneousElecSpeedDpp;
78     /* Average mechanical acceleration expressed in the unit defined by hSpeedUnit,
79        only reported with encoder implementation. */
79     int16_t hMechAccelUnitDpp;
80     /* Maximum value of measured mechanical speed that is considered to be valid.
81        Expressed in the unit defined by [SPEED_UNIT](measurement_units.md). */
81     int16_t hMaxValidMechSpeedUnit;
82     /* Minimum value of measured mechanical speed that is considered to be valid.
83        Expressed in the unit defined by [SPEED_UNIT](measurement_units.md). */
84     int16_t hMinValidMechSpeedUnit;
85     /* Maximum value that is considered to be valid.
86        Constant value equal to 65535, expressed in the unit defined by
87        [SPEED_UNIT](measurement_units.md). */
88     int16_t hMaxValidMechSpeedUnit;
89     /* Frequency at which the user will request a measurement of the rotor
90        electrical angle. Expressed in PWM_FREQ_SCALING * Hz. */
91     uint16_t hMeasurementFrequency;
92     /* Conversion factor (65536/PWM_FREQ_SCALING) used to convert measured speed
93        from the unit defined by [SPEED_UNIT](measurement_units.md) to
94        [dpp](measurement_units.md). */
95     float Thata_min_enc;
96     float Thata_max_enc;
97     float dThata_min_enc;
98     float dThata_max_enc;
99     int16_t hEnc_err;
100     int16_t hEnc_err_max;
101     int16_t hEnc_err_offset;
102     int comp_flag;
103     float Encoder_comp[252];
104 } SpeedPosIdbk_Handle_t;
105
106 #weak init16_t EMC_CalcAngle(INCODE_Handle_t *pHandle)
107 {
108     int16_t eAngle; /* slddegree format */
109     if(RUNERR_FULL_PTR_CHECK_ENC_SPD_POS_IDBK)
110     {
111         if (NULL == pHandle)
112         {
113             eAngle = 0;
114         }
115     }
116     else
117     {
118         int16_t mcAngle; /* slddegree format */
119         uint16_t uStepCnt;
120         int16_t iAngle;
121         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
122            if the overflow occurs just after the entry in the High frequency task. */
123         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
124         if(RUNERR_FULL_MISRA_C_COMPLAINT_ENC_SPD_POS_IDBK)
125         {
126             /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
127                if the overflow occurs just after the entry in the High frequency task. */
128             uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
129         }
130         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
131            if the overflow occurs just after the entry in the High frequency task. */
132         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
133         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
134            if the overflow occurs just after the entry in the High frequency task. */
135         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
136         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
137            if the overflow occurs just after the entry in the High frequency task. */
138         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
139         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
140            if the overflow occurs just after the entry in the High frequency task. */
141         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
142         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
143            if the overflow occurs just after the entry in the High frequency task. */
144         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
145         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
146            if the overflow occurs just after the entry in the High frequency task. */
147         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
148         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
149            if the overflow occurs just after the entry in the High frequency task. */
150         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
151         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
152            if the overflow occurs just after the entry in the High frequency task. */
153         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
154         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
155            if the overflow occurs just after the entry in the High frequency task. */
156         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
157         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
158            if the overflow occurs just after the entry in the High frequency task. */
159         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
160         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
161            if the overflow occurs just after the entry in the High frequency task. */
162         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
163         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
164            if the overflow occurs just after the entry in the High frequency task. */
165         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
166         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
167            if the overflow occurs just after the entry in the High frequency task. */
168         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
169         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
170            if the overflow occurs just after the entry in the High frequency task. */
171         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
172         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
173            if the overflow occurs just after the entry in the High frequency task. */
174         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
175         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
176            if the overflow occurs just after the entry in the High frequency task. */
177         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
178         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
179            if the overflow occurs just after the entry in the High frequency task. */
180         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
181         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
182            if the overflow occurs just after the entry in the High frequency task. */
183         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
184         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
185            if the overflow occurs just after the entry in the High frequency task. */
186         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
187         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
188            if the overflow occurs just after the entry in the High frequency task. */
189         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
190         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
191            if the overflow occurs just after the entry in the High frequency task. */
192         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
193         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
194            if the overflow occurs just after the entry in the High frequency task. */
195         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
196         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
197            if the overflow occurs just after the entry in the High frequency task. */
198         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
199         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
200            if the overflow occurs just after the entry in the High frequency task. */
201         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
202         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
203            if the overflow occurs just after the entry in the High frequency task. */
204         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
205         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
206            if the overflow occurs just after the entry in the High frequency task. */
207         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
208         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
209            if the overflow occurs just after the entry in the High frequency task. */
210         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
211         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
212            if the overflow occurs just after the entry in the High frequency task. */
213         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
214         /* PR 32058 we need to keep only the 16 LSB, bit 31 could be at 1
215            if the overflow occurs just after the entry in the High frequency task. */
216         uStepCnt = ((L1_TmGetCounter(pHandle->TIM0) & 0xFFFFFFF) / 0x80000000);
217         /* PR 32058 we need to keep only the 16 LSB, bit 3
```

(b) *encoder_speed_pos_fdbk.c* Enc_CalcAngle function

```

40 ENCORDER_Handle_t ENCORDER_H3 =
41 {
42     {
43         .Super =
44         {
45             .iEToMcRatio = POLE_PAIR_NUM,
46             .iMaxLabelSpeedUnit = (uint16_t) MAX_APPLICATION_SPEED_UNIT,
47             .iMinLabelSpeedUnit = (uint16_t) (MIN_APPLICATION_SPEED_UNIT),
48             .iMaxInSpeedErrorNumber = HI_SS_MEAS_ERRORS_BEFORE_FAULTS,
49             .iMaxLabelSpeedUnit = 65535,
50             .iMeasurementFrequency = TP_REGULATION_RATE_SCALED,
51             .iOPFConFactor = OPF_CONV_FACTOR,
52             .iTheta_min_enc = -32768,
53             .iTheta_max_enc = 32768,
54             .iDtheta_enc = 26.0863,
55             .dtheta_inv_enc = 0.0384521,
56             .enc_err = 0,
57             .mc_err_offset = 0,
58             .comp_flag = 0,
59             .Encoder_comp = {-60.9,-60.9,-62.5,-57.6,-56.4,-54.4,-59.3,-59.2,-56.7,-52.8,-57.6,-56.4,-49.4,-51.1,-43,-47.9,-52.8,-57.6,
60             },
61             .PulseNumber = HI_ENCODER_PPR * 4,
62             .SpeedSamplingFreqz = MEDIAN_FREQUENCY_TASK_RATE,
63             .SpeedBufferSize = ENC_AVERAGING_FIFO_DEPTH,
64             .TMD = TMD,
65             .icx_filter = HI_ENC_IC_FILTER_L1,
66         }
67     };
68 }

```

(c) *mc_config_common.c*

```

195 void Enc_err(float *tab0, float Xin, float Xoff, float Xmax, float Xmin, float DX, float inv_DX, int16_t *Yout)
196 {
197     int X0;
198
199     Xin -= Xoff;
200
201     if (Xin > 32768)
202     {
203         Xin -= 2*Xmax;
204     }
205     if (Xin < -32768)
206     {
207         Xin += 2*Xmax;
208     }
209
210     X0 = floor((Xin - Xmin)*inv_DX);
211
212     tab0 = tab0 + X0;
213
214     *Yout = (int16_t)(tab0 + ((tab0 + 1) - *tab0)*inv_DX*(Xin - Xmin - DX*X0));
215
216
217 }

```

(d) *encoder_speed_pos_fdbk.c* Enc_err function

(d) *encoder_speed_pos_fdbk.c* Enc_err function

a temperature increase below 80 °C from the eGaN IC case to the ambient. Under the same conditions, EPC91132 can deliver 11 A_{RMS} per phase with the humanoid joint motor casing acting as a heatsink, in which the ICs were covered using a 1 mm-thick electrically non-conductive thermal interface material (PN: TG-A1780-20-20-1.0), keeping the temperature rise below 80°C from the eGaN IC case to ambient. At 48 V_{DC}, the board reached a higher temperature due to the higher supply voltage. In fact, without a heatsink, the EPC91132 can deliver 6 A_{RMS} per phase at a temperature rise of less than 80 °C, and up to 10 A_{RMS} with a heatsink.

Finally, in Figure 8.24 are shown the thermal photos taken at the end of two thermal tests: 24 V_{DC}, 60 kHz, 6 A_{RMS} without heatsink; 24 V_{DC}, 60 kHz, 10 A_{RMS} with heatsink. The left figure points out how the heat produced by the device and the copper is concentrated in the small PCB frame, since it is thermally isolated from the external ring (lack of copper connections).

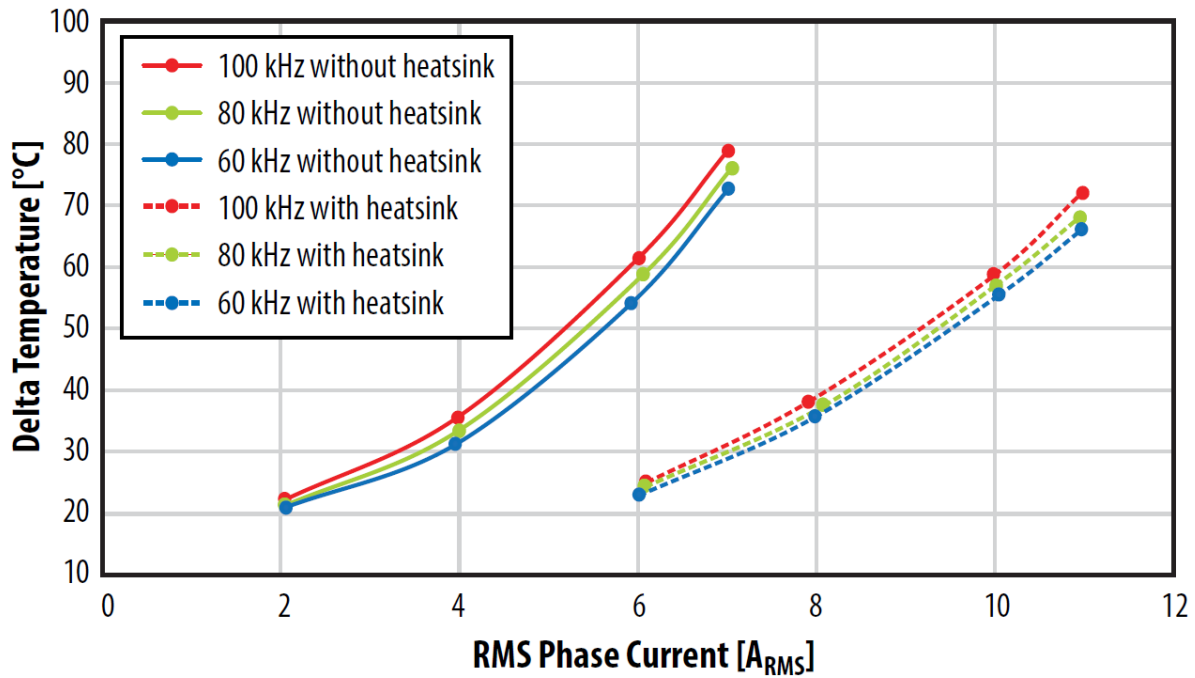


Figure 8.20: 24 V_{DC} EPC91132 eGaN IC temperature increase vs. the ambient temperature (24 °C).

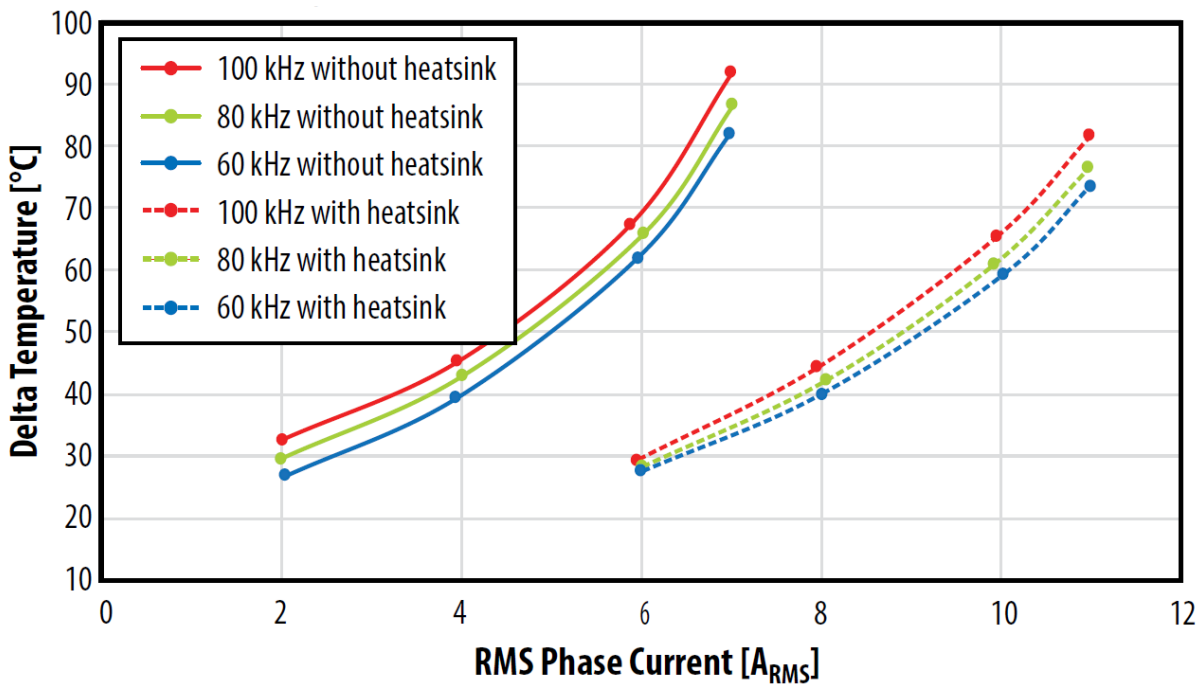


Figure 8.21: 48 V_{DC} EPC91132 eGaN IC temperature increase vs. the ambient temperature (24 °C).

The right figure, instead, clearly shows how the humanoid joint motor casing helps the heat dissipation from the power device, by offering a wider area for the natural convection cooling.

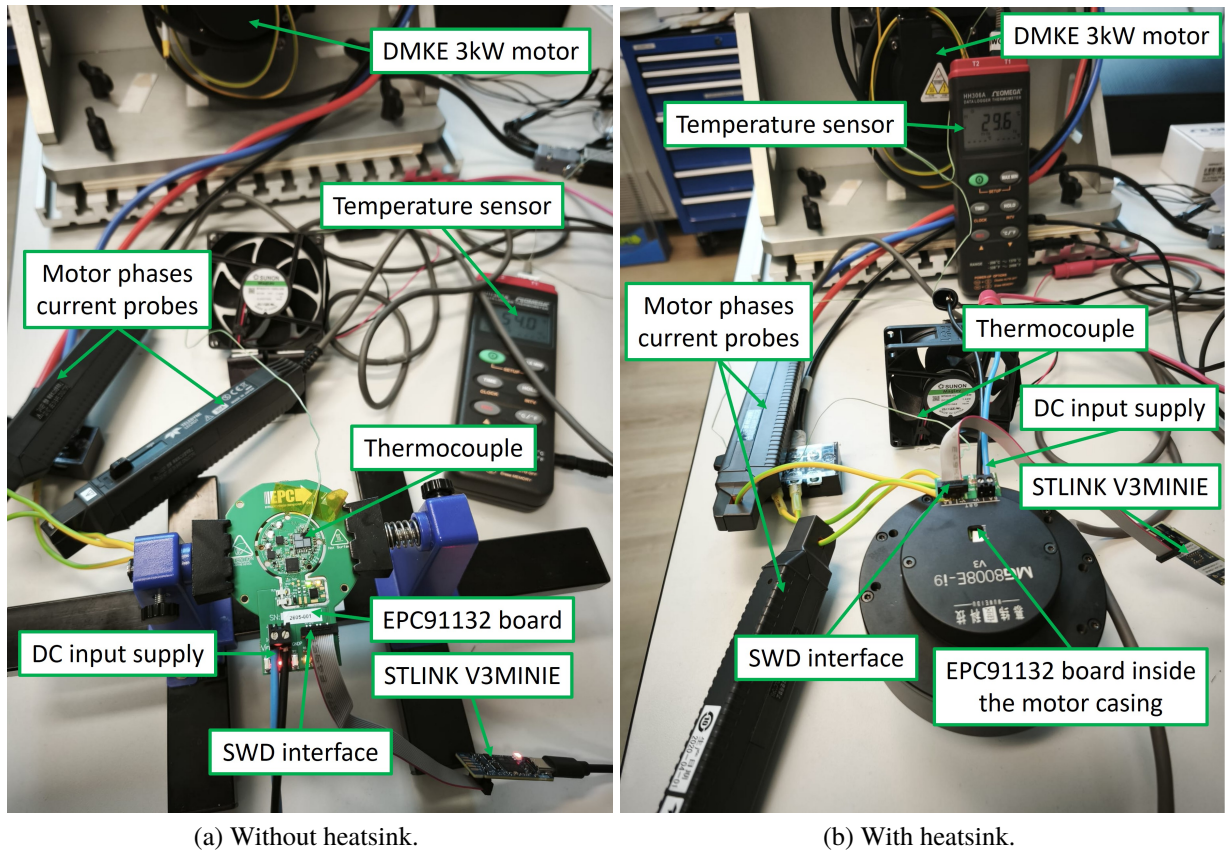


Figure 8.22: Experimental setups during steady state thermal tests.

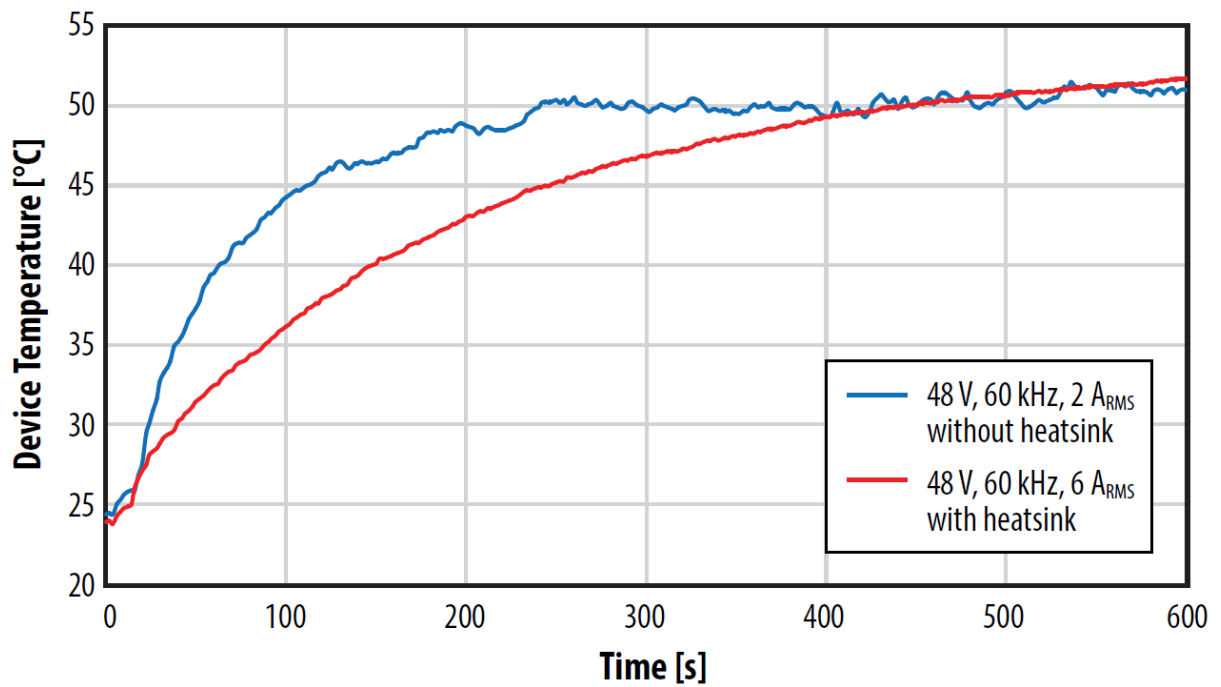


Figure 8.23: 48 V_{DC} EPC91132 eGaN IC thermal transients starting from 24 °C ambient temperature.

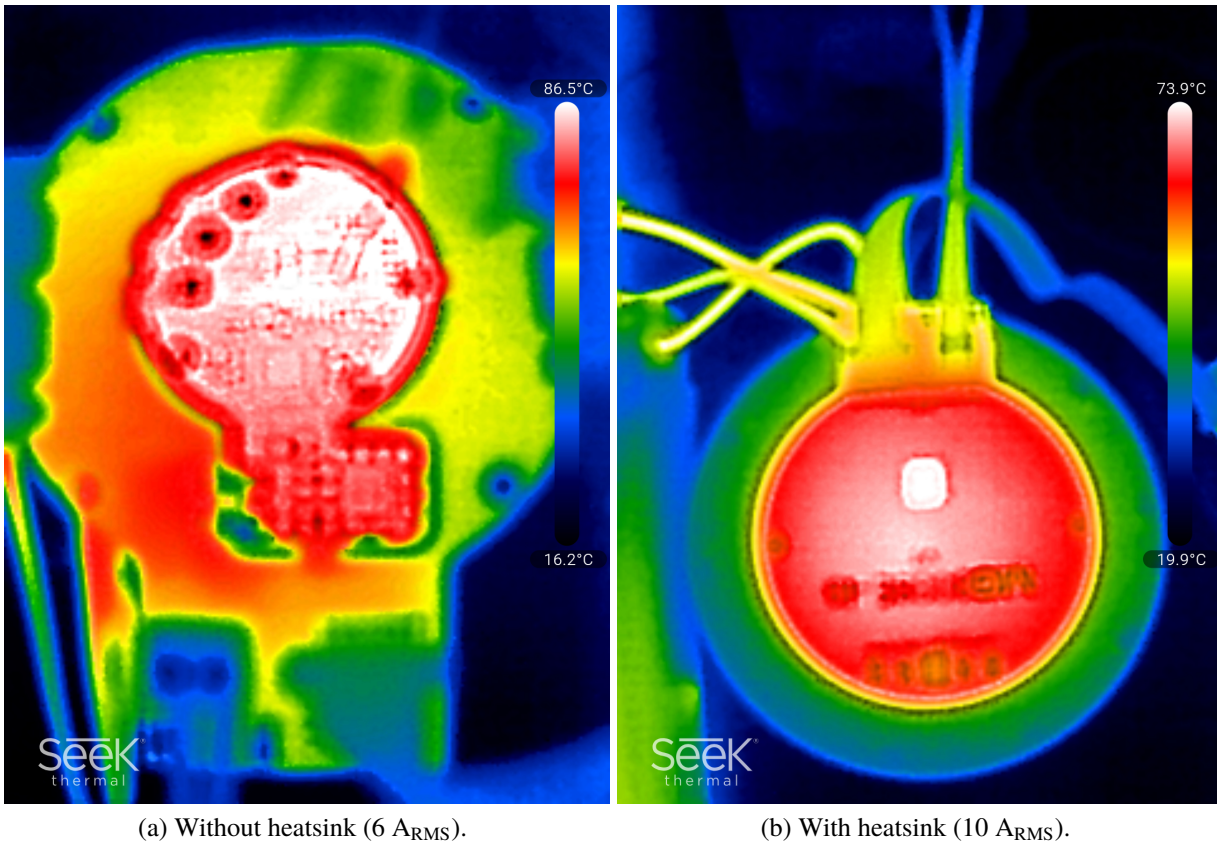


Figure 8.24: Thermal photos during steady state thermal tests (24 V_{DC}, 60 kHz).

8.5 Thermal Behavior in Impulsive Tests

To emulate the performance of EPC91132 in applications subject to a dynamic operation, impulsive tests have been performed following a similar procedure used in the steady state tests: with and without the humanoid joint motor's casing acting as a heatsink; waiting 10 minutes for each test and then cooling the board with a fan to obtain always the same initial device's temperature; 20 ns of dead time, but only at 48 V_{DC} and 100 kHz of PWM switching frequency (worst conditions in terms of switching losses). As shown in Figure 8.25, the experimental setup used during these tests consisted of connecting the 3kW motor to a magnetic powder brake (TPB-050 from Magtrol) to form a dynamometric bench, thereby setting the required load torque to obtain a current pulse of 15 A_{RMS}. The 3kW motor was driven with a sensorless FOC algorithm (Observer + PLL offered by the STM32 MC firmware library) at a constant speed of 200 RPM. The load torque profile consisted of a 5-second period with a variable pulse duty from 100 ms (2%) to 1 s (20%), in which the low value produced a phase current of 5 A_{RMS}, while the high value produced a phase current of 15 A_{RMS}.

The thermal performance summary of the EPC91132 board during pulsed-torque operation is shown in Figure 8.26, where the EPC33110 temperature rise closely matches the steady-state traces. An example of phase current waveforms is shown in Figure 8.27, which is referred to as a pulsed torque test at 20% pulse duty, with the humanoid joint motor casing acting as a heatsink.

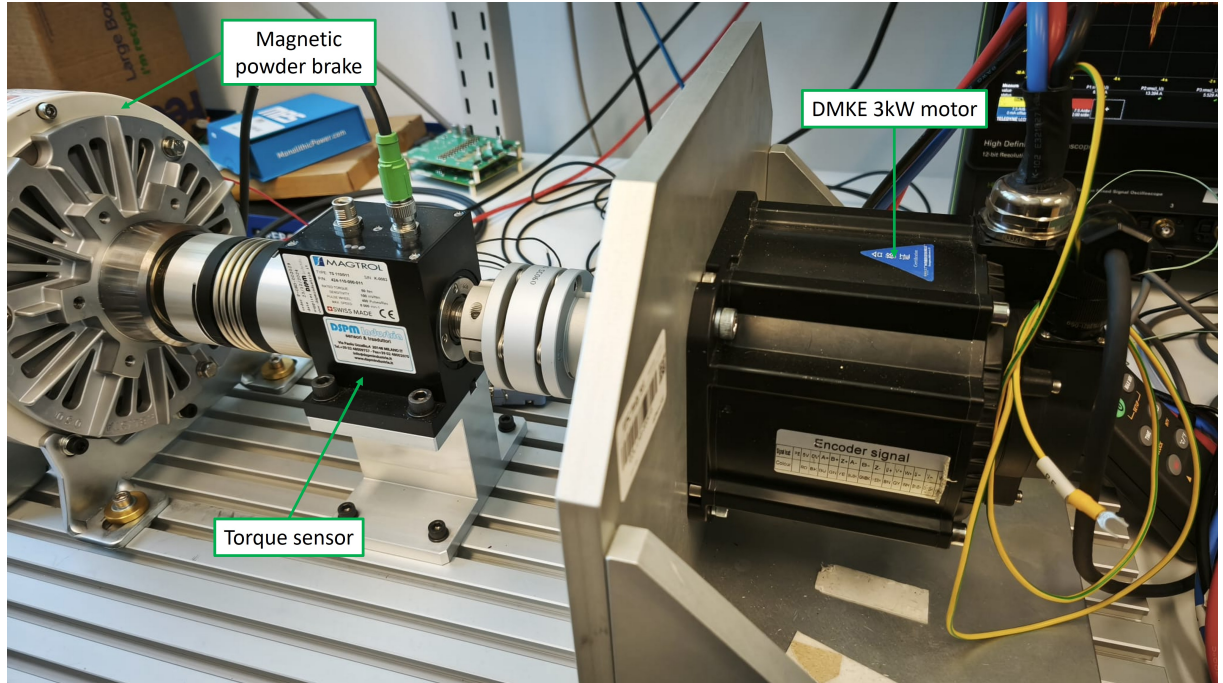
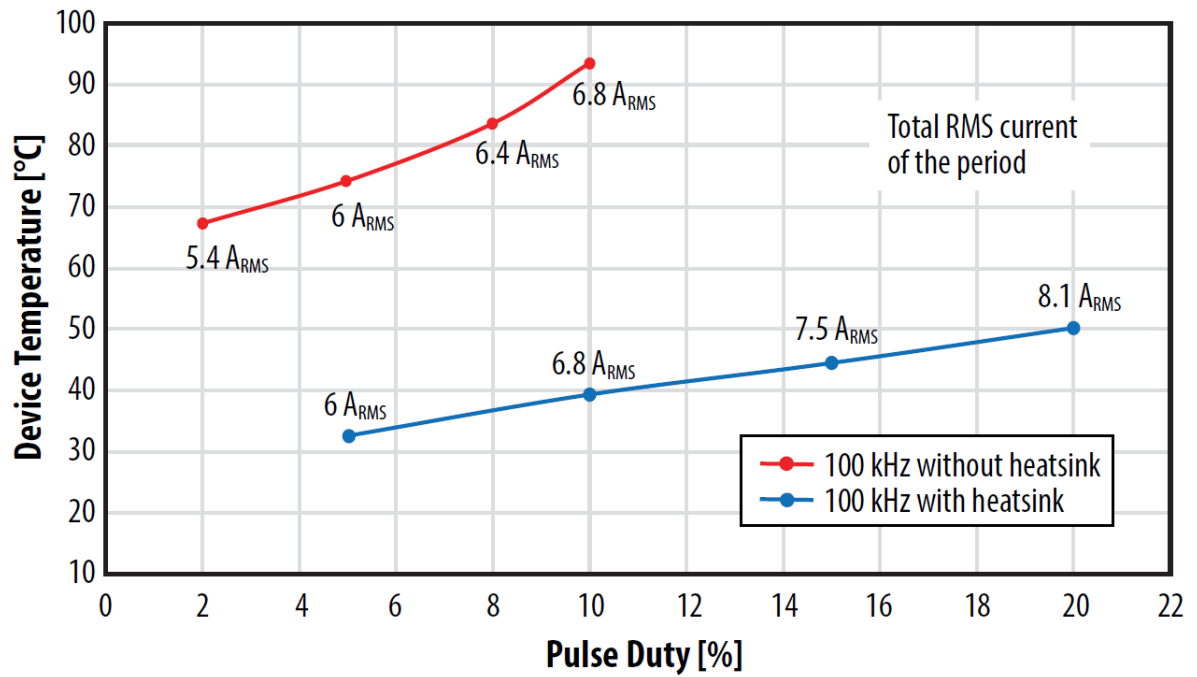


Figure 8.25: Experimental setup during impulsive thermal tests.

Figure 8.26: 48 V_{DC} EPC91132 eGaN IC temperature increase vs. the ambient temperature (24 °C), during pulsed torque tests.

8.6 Case Study 1: Robot Joint Motor Drive Characterization

The EPC91132 was tested in the robot joint motor to validate its operation in a typical humanoid motor drive. The tests consisted of driving the MG8008E-i9 V3 servomotor at different fixed

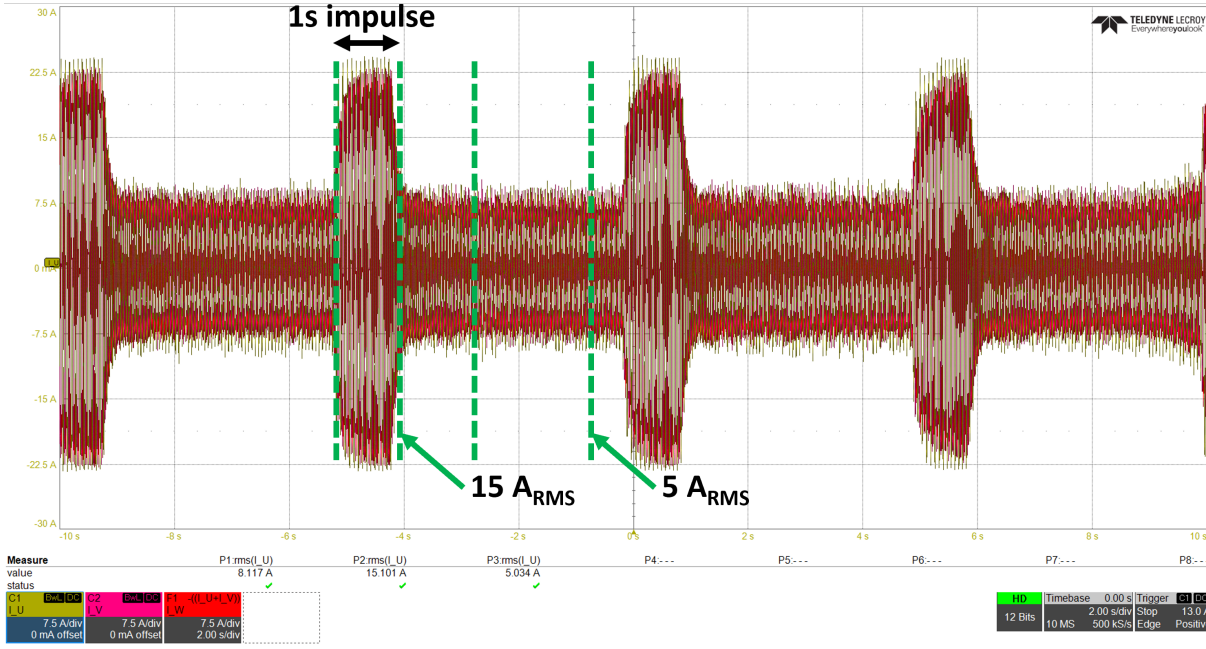


Figure 8.27: Phase current waveforms during pulsed torque test at 20% pulse duty.

speeds with the sensed FOC control exposed in Section 8.3, which includes an encoder compensation strategy to attenuate the current's amplitude oscillations. The motor was inserted in the same dynamometric bench used for the impulsive tests, which features a magnetic powder brake controlled by a programmable power supply, along with a torque transducer to measure the load torque applied by the brake. The complete experimental setup is shown in Figure 8.28. The servomotor was driven at different speeds, from 400 rpm to the rated speed of 1600 rpm (on the rotor side, before the planetary reduction gear), by applying different load torques to reach the rated motor current of 5 Arms, starting from 0.5 Arms. As demonstrated in Section 8.4, the inverter board can easily withstand these current values; no further thermal characterizations have been carried out in these tests. The device temperature was monitored to verify that the board was working below the thermal limits. The EPC91132 was supplied with 48 V, applying a switching frequency of 100 kHz and a dead time of 20 ns. As can be observed in Figure 8.29, from each test, some measures were performed to obtain the overall efficiency of the motor drive, measuring the input DC power from the related voltage and current, and the efficiency from the load torque and the imposed speed. The results of this performance analysis are reported in Figure 8.30, in which it can be noted that the maximum efficiency is about 80 %, which is consistent with the data provided by the manufacturer (Figure 6.26).

Finally, these tests were also used to validate the DC bus sizing strategy exposed in Section 7.5, by directly measuring the DC bus voltage ripple. These measures are compared to the one computed with the strategy proposed during the DC bus sizing procedure, using the formula:

$$V_{ripple,max} = K(m, \varphi) \cdot \frac{I_{out,rms}}{C_{bus} \cdot f_{PWM}}$$

where the output RMS current was measured with a current probe, the switching frequency was imposed at 100 kHz, and the total DC bus capacitance was equal to 6.588 μ H, since the ceramic capacitors chosen for the EPC91132 feature a DC bias derating of nearly 90% [49].

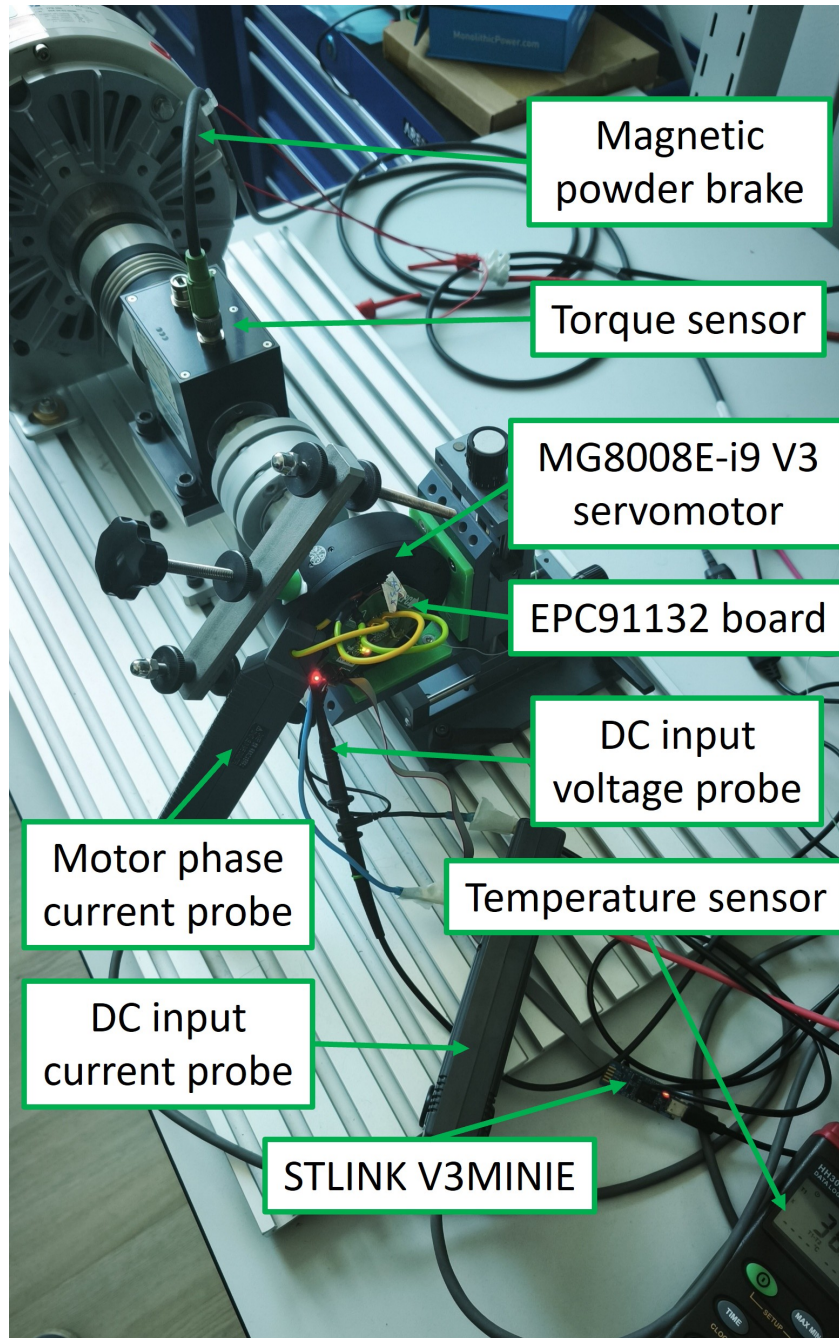


Figure 8.28: Experimental setup during robot joint motor tests.

Regarding the variables that influence the K function, φ was assumed equal to zero, due to the FOC control of a PMSM motor with a flux predominance of the permanent magnets. Instead, the modulation index was measured from the duty cycle waveforms retrieved in real time from the microcontroller using the MCUViewer tool. In Figure 8.31, an acquisition example of the Capture Compare Register (CCR) values computed by the microcontroller to generate the required PWM signals is plotted. The modulation index was computed with this formula, remembering that the clock frequency of the microcontroller is 170 MHz, and the switching frequency is set

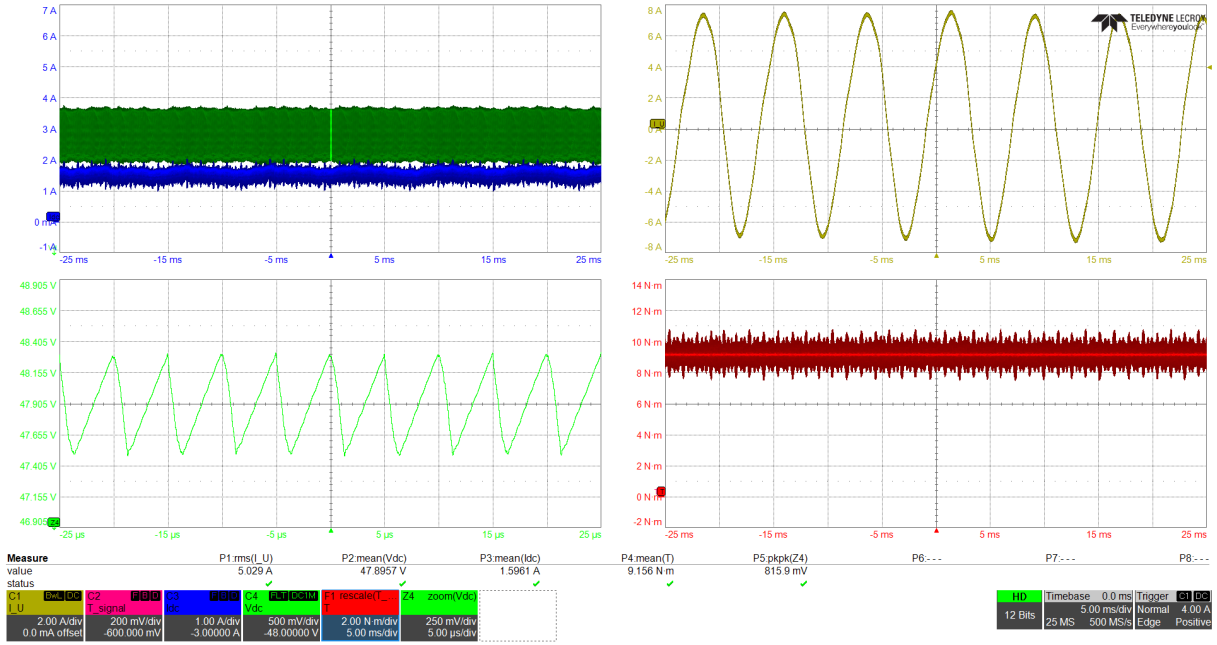


Figure 8.29: Oscilloscope measurements when driving the MG8008E-i9 V3 motor at 400 rpm and 9.2 Nm load torque. C1: Phase U current; C2: Torque signal ; C3: DC input current; C4: DC input voltage; F1: Torque measure [10 Nm/V]; Z4: Zoom on DC input voltage.

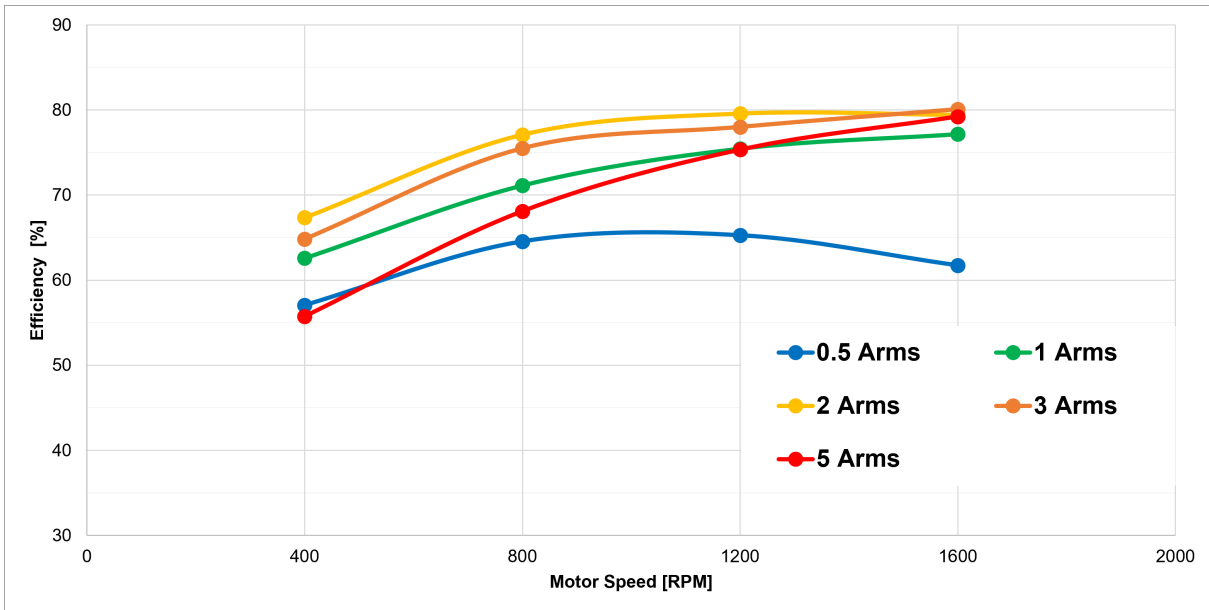


Figure 8.30: Overall efficiency over the motor speed driving the MG8008E-i9 V3 motor at various load torques.

to 100 kHz:

$$m = 1.1547 \cdot \frac{CCR_{max} - \frac{f_{clock}}{f_{PWM}^4}}{\frac{f_{clock}}{f_{PWM}^4}}$$

So, in Figure 8.32, the comparison between the computed and the measured DC voltage ripple over the modulation index and for different output currents is shown. The experimental values show a trend very similar to the model, with a maximum relative error of about 20 % during the

tests at 5 Arms.

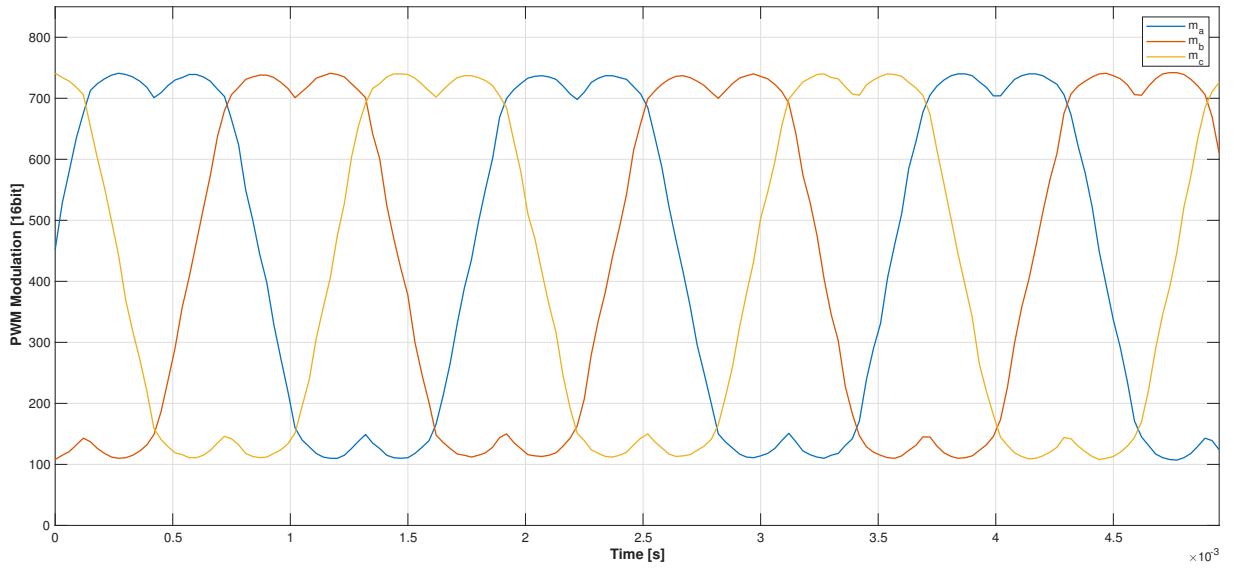


Figure 8.31: PWM modulations imposed by the microcontroller when driving the MG8008E-i9 V3 motor at 1600 rpm and 3 Arms.

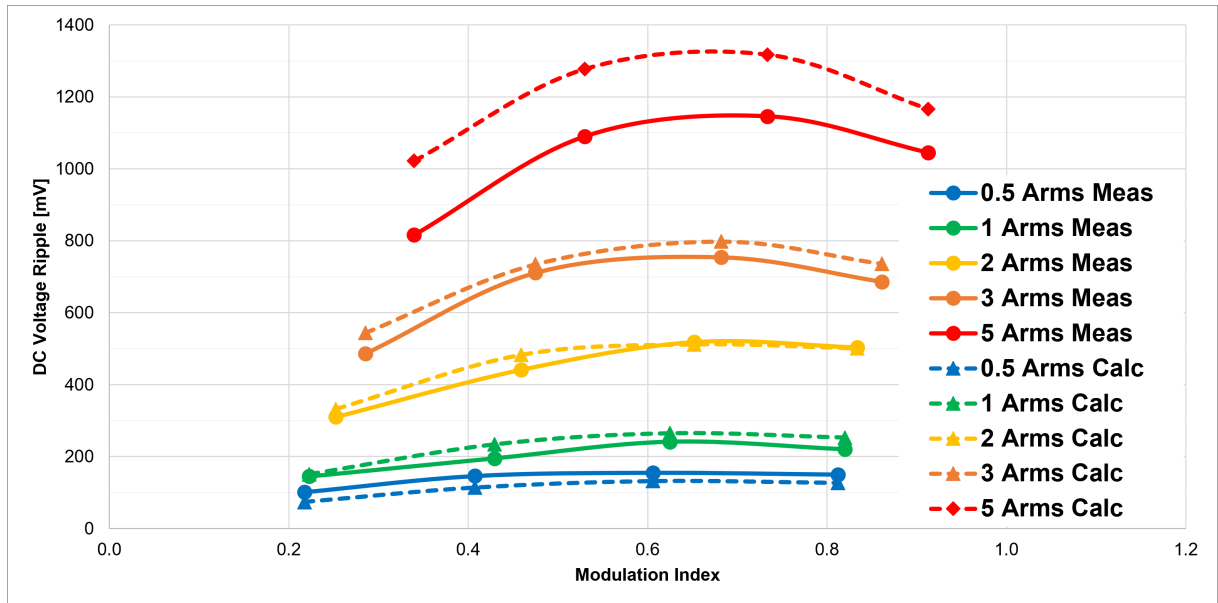


Figure 8.32: Comparison between the measured and the computed DC bus voltage ripple over the modulation index driving the MG8008E-i9 V3 motor at various load torques.

8.7 Case Study 2: Drone Motor Drive Characterization

The EPC91132 was tested on Vertiq motors equipped with an underactuated propeller (UPF-23-12 from Vertiq [54]) to validate its operation in a drone application. The small PCB outline was detached from the outer ring in order to fit the board inside the drone motor, as can be seen in Figure 8.33; the motor's phases are soldered on the bottom side of the board, the two DC supply wires (blue and black on the left) are welded on the dedicated pads, while the other small wires are used for performing the communication with the microcontroller:

- Red wire for supplying the STLINK-V3MINIE Debugger Programmer with 3.3 V;
- Black wire for providing GND connection to the STLINK-V3MINIE Debugger Programmer;
- White wire for connecting the STLINK-V3MINIE Debugger Programmer with the SWDIO pin of the micro;
- Grey wire for connecting the STLINK-V3MINIE Debugger Programmer with the SWCLK pin of the micro;
- Yellow wire for connecting the input A signal (from a USB-to-RS485 converter) with the A pin of the RS485 transceiver;
- Green wire for connecting the input B signal (from a USB-to-RS485 converter) with the B pin of the RS485 transceiver;
- Orange wire for providing GND connection to the USB-to-RS485 converter;

The tests consisted of driving the drone motor at a fixed speed for 10 minutes with a switching frequency of 100 kHz and a dead time of 20 ns, after which the device temperature was measured by means of a thermocouple. In particular, for the 220 KV version, the speed range was from 1000 to 3400 rpm with a step of 300 rpm, with the maximum value limited by the voltage supply of 24 V. For the 2200 KV version, instead, the maximum speed of 3700 rpm was limited by the maximum RMS current deliverable by the inverter board. For each test, the mean values of the input DC voltage and current were measured with a digital oscilloscope to compute the input power required by the motor drive (Figure 8.34). The motor currents were not measured through voltage probes due to the impossibility of accessing the motor's phase, but they were recorded using the MCUViewer tool, and then analyzed with a MATLAB script, which outputs the currents' plot over 10 periods, in both s16A and A units (Figure 8.35), along with the RMS values. The conversion factor between the two units is computed with this formula:

$$curr_{factor} = \frac{V_{cc}}{curr_{gain} \cdot 2^{ADC,bit}} = \frac{3.3}{0.044 \cdot 65536} = 0.0011 \left[\frac{A}{s16A} \right]$$

A photo of the experimental setup used during the tests is reported in Figure 8.36.

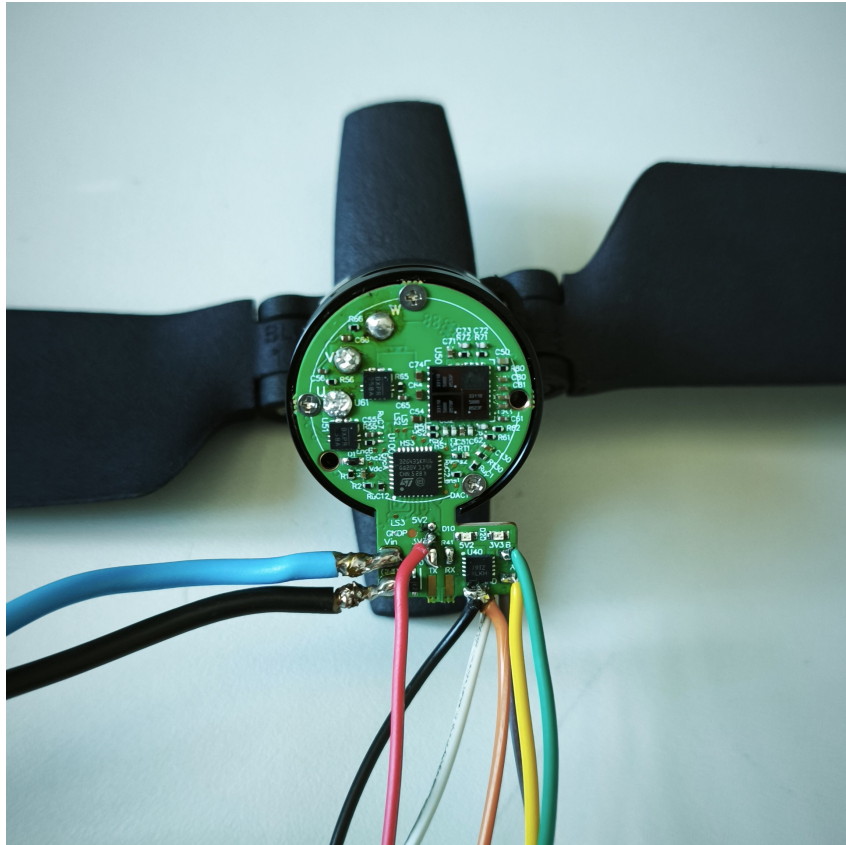


Figure 8.33: EPC91132 small form inside the Vertiq 23-06 G1 module.

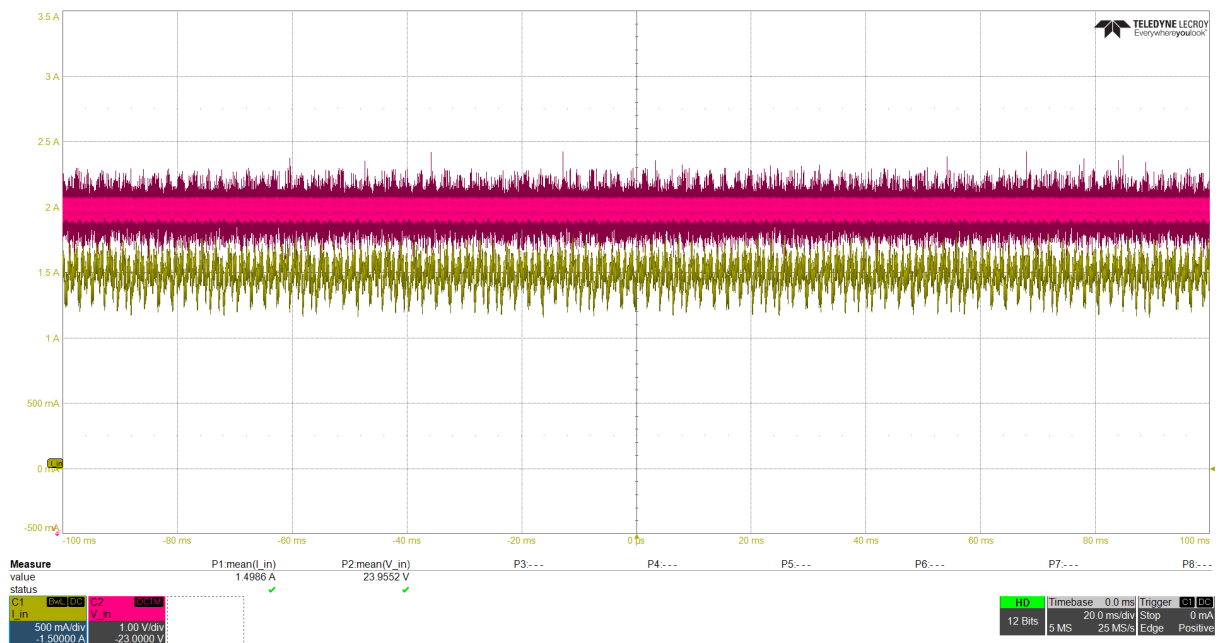


Figure 8.34: DC input waveforms measured driving the Vertiq 2200 KV motor at 3700 rpm. C1: Input DC current; C2: Input DC voltage.

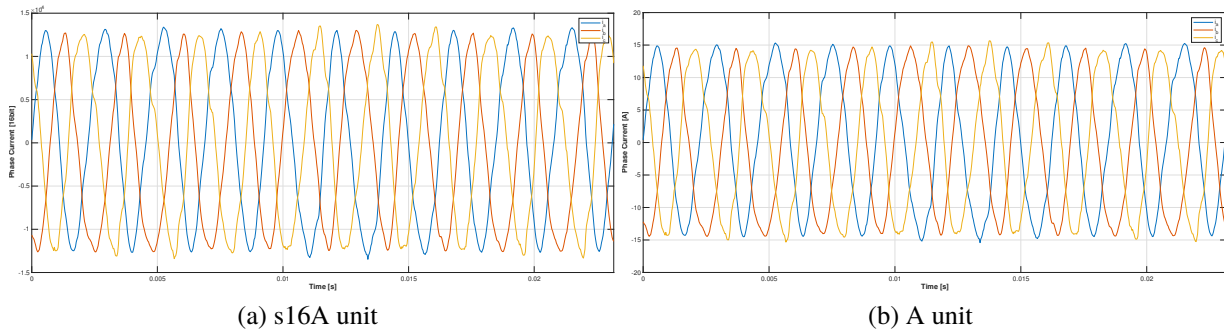


Figure 8.35: Motor currents measured by the microcontroller when driving the Vertiq 2200 KV motor at 3700 rpm.

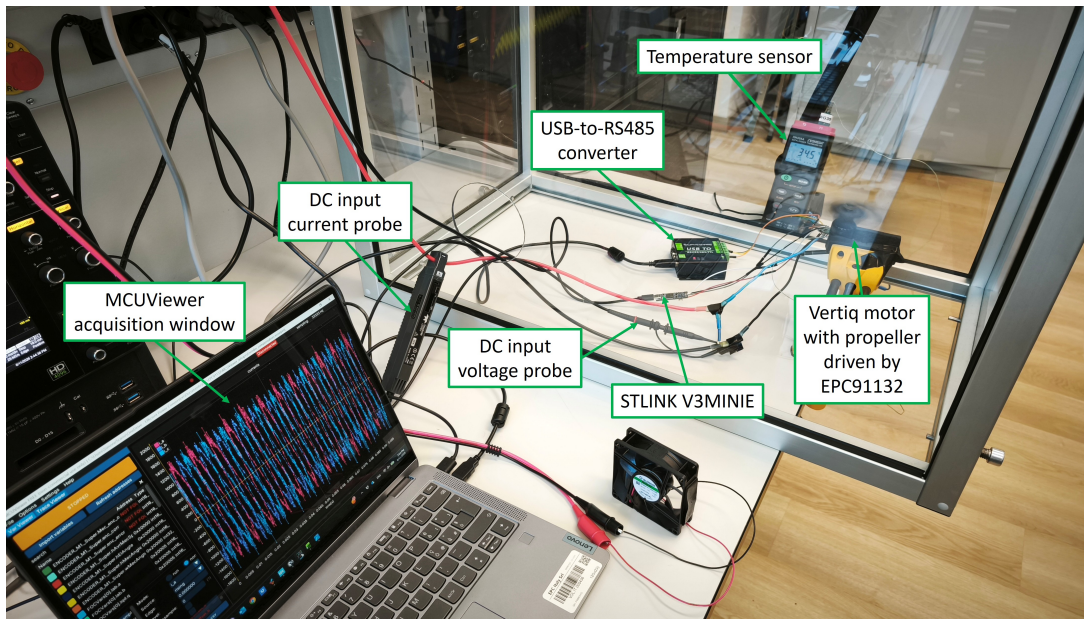


Figure 8.36: Experimental setup during drone motor tests.

In Figure 8.37, the device temperature measurements over the motor speed (a) and the RMS current (b) recorded when driving the Vertiq 220 KV are reported. Since the maximum current required by the drone motor is around 0.9 Arms at 3400 rpm, the rise temperature of the EPC33110 never exceeds 4 °C during all the tests. In Figure 8.38, the device temperature measured during tests with the 2200 KV version is considerably higher. In fact, the maximum RMS current required by the motor reached 10.2 Arms at 3700 rpm. This is due to the different torque constants of the two motor versions. At this value, the module's temperature rose to 63.5 °C, indicating better thermal dissipation than that observed in the steady-state thermal tests (Section 8.4), thanks to the high airflow generated by the propeller.

In Figure 8.39, the measurements over the motor speed of the DC input current and power (a) and the estimation of the propeller torque and the related overall efficiency (b) are reported when driving the Vertiq 220 KV. The propeller torque was computed by multiplying the RMS current by the nominal torque constant, since a direct torque measurement would have been infeasible. So, the efficiency obtained with this method only indicates the motor drive performance. Figure 8.39 shows the results obtained during the same tests with the 2200 KV version motor.

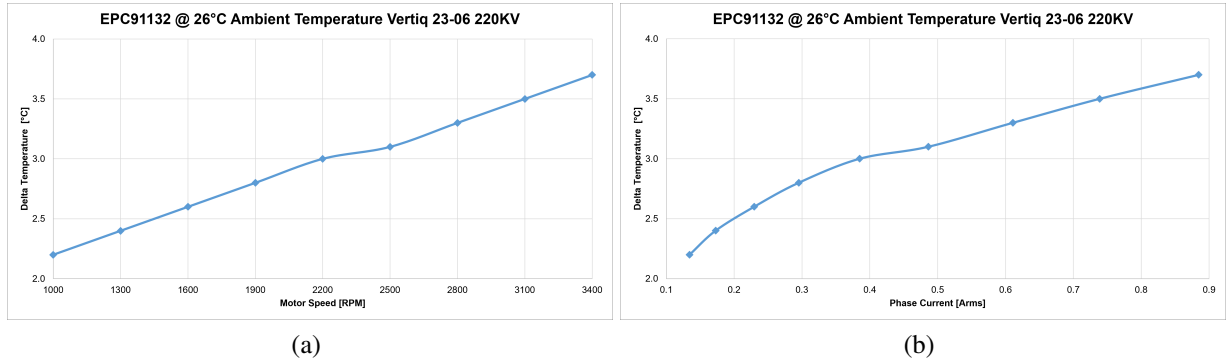


Figure 8.37: EPC33110 temperature during the tests with the Vertiq 220 KV version motor.

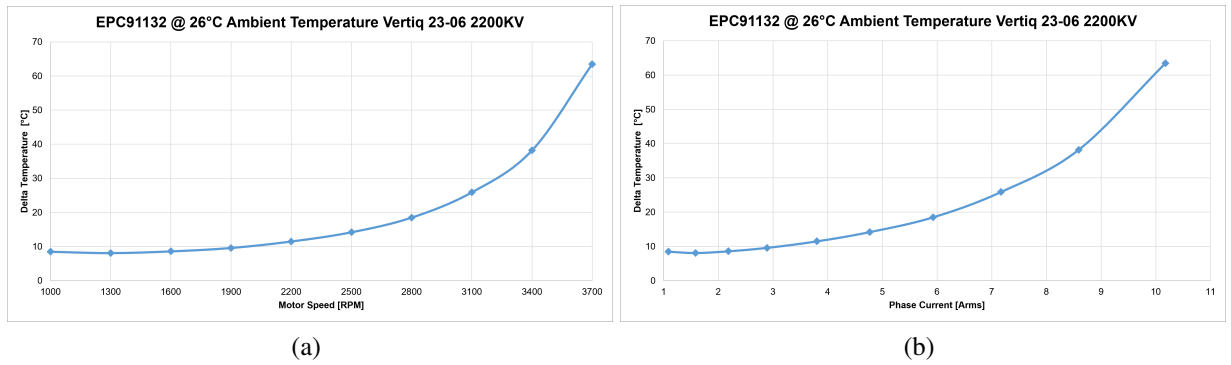


Figure 8.38: EPC33110 temperature during the tests with the Vertiq 2200 KV version motor.

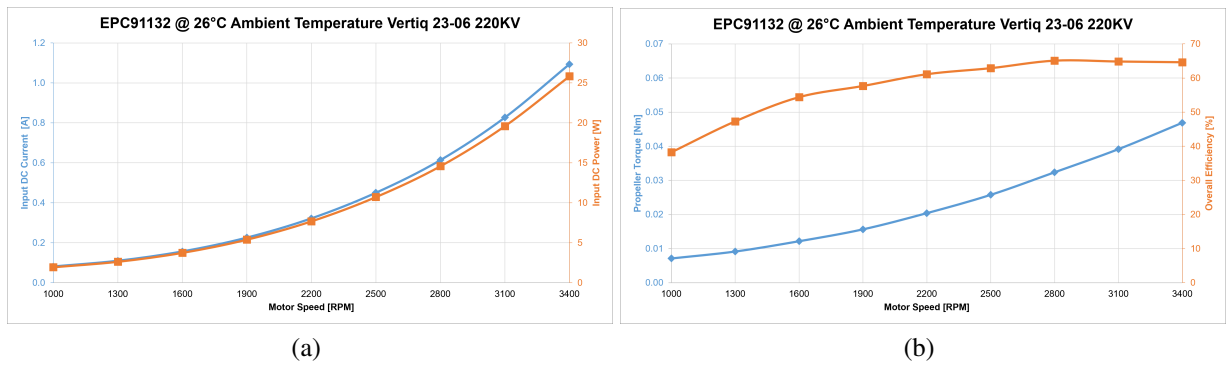


Figure 8.39: Input (a) and output (b) measures during the tests with the Vertiq 220 KV version motor.

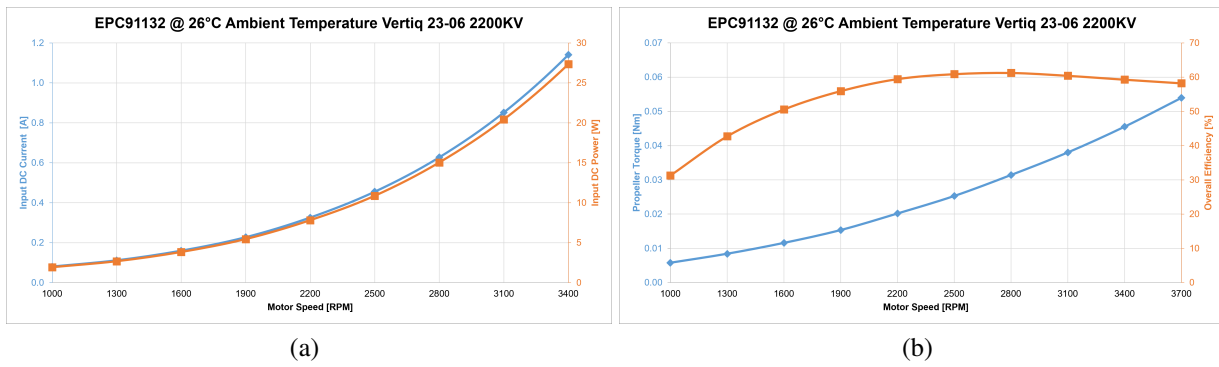


Figure 8.40: Input (a) and output (b) measures during the tests with the Vertiq 2200 KV version motor.

Chapter 9

Conclusions

In conclusion, this thesis has demonstrated the feasibility and advantages of employing GaN monolithic power integrated circuits for low-voltage robotic motor drive applications. Starting from a comprehensive analysis of advanced robotic systems and the evolution of wide-bandgap semiconductor technologies, an inverter evaluation board based on the EPC33110 three-phase ePower™ Stage IC was successfully designed, implemented, and experimentally validated. The developed EPC91132 is a 23 mm small-motor drive inverter reference design for humanoid wrists and hands, as well as for drones. It features a compact and flexible architecture, which maintains fast switching performance, satisfactory thermal behavior, and high efficiency. The heart of the EPC91132 is the EPC33110 GaN module based on Efficient Power Conversion GaN monolithic integrated circuit technology. It is a compact three-phase module in a 6x6.5 mm QFN package that integrates three GaN half-bridges with built-in gate drivers, bootstrap circuits, and level shifters, optimized for motor control. A single 5 V power supply can drive the module up to 80 V, with a typical on-resistance of 11.7 m Ω , and support 3.3 V or 5 V logic inputs.

Some experimental tests were conducted to confirm the effectiveness of the proposed hardware and firmware motor-drive solutions, including the encoder misalignment compensation strategy and the DC-link capacitor sizing proposed methodology. Thanks to top-side cooling optimized by the exposed dies, EPC33110 can deliver up to 11 A_{RMS} continuously per phase, as verified in steady-state tests and also during the drone motor drive characterization.

The work exposed in this thesis shows how the GaN technology can play a pivotal role in the development of the next generation of integrated motor drive for robotics, thanks to its inherent inclination to the high integration level, reduced losses, and increased power density. Future prospects may rely on further miniaturization of motor drives, adding more useful integrated functions, and improving thermal management, with the final aim of achieving a single compact, efficient, and intelligent robotic actuation system.

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