POLITECNICO DI TORINO

Master's Degree in Electronic Engineering for Industrial Applications

Master's Degree Thesis

Design of a NB-IoT/LTE-M module with dual MCU in a medium density, mixed signals PCB for IoT embedded applications

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Acronyms

IoT

Internet of Things

NB-IoT

NarrowBand IoT

4G LTE

Fourth Generation Long Term Evolution

LTE-M

LTE - Machine Type Communication

GPS

Global Positioning System

Rf

Radio Frequency

PCB

Printed Circuit Board

SiP

System in Package

SoM

System on Module

DK

Development Kit

EMI

ElectroMagnetic Interference

TVS

Transient Voltage Suppression

CMSIS

Common Microcontroller Software Interface Standard

GPIO

General Purpose Input Output

ADC

Analog to Digital Converter

LGA

Land Grid Array

BGA

Ball Grid Array

UART

Universal Asynchronous Receiver-Transmitter

USART

Universal Synchronous and Asynchronous Receiver-Transmitter

LPUART

Low Power UART

SPI

Serial Peripheral Interface

I2C

Inter Integrated Circuit

DRC

Design Rule Check

MBC

MBC

MBC-WB

MBC Wireless Bluetooth

MBC-LR

MBC Long Range

MBC-NB

MBC Narrow Band

Chapter 1

Introduction

The Internet of Things is increasingly widespread thanks to rapid technological advancement and a growing need for small devices that can communicate with one another. In this view, the need for wireless communication technologies that will be able to support such a huge network of low-power, low-cost devices also increases. NB-IoT and LTE-M have emerged as promising solutions to address these requirements.

These technologies offer a number of benefits, like low power consumption, wide coverage and scalability.

Both technologies are designed to operate on limited power in order to ensure long battery life for IoT applications deployed in remote or hard to reach locations. It is necessary for such applications because replacing batteries more often would be highly impracticable or expensive. These technologies achieve very low power consumption by employing slower connection speeds. In fact NB-IoT data rate is almost a hundred times slower than the common 4G connectivity that smartphones use. NB-IoT uses existing LTE infrastructure for coverage, even in cases of poor cellular connectivity. Similarly, LTE-MTC, though operating on a different frequency band, will leverage off already rolled-out LTE networks to ensure that IoT devices connect to the network reliably across a wide range of locations, from urban centers to rural areas. These technologies are designed to support a high number of connected devices, making them ideal for large-scale IoT deployments. This is one of the critical requirements of increasingly common applications like smart cities, industrial automation, and agriculture, among others, which may require simultaneous connection of lots of devices.

While both NB-IoT and LTE-MTC hold convenient advantages, building IoT solutions may not be easy due to the complexities of hardware design, software development, and network integration. A dedicated NB-IoT board can make things much easier by providing a ready to use platform that will easily be integrated into any solution.

Besides the NB-IoT chip, the board should include a low power microcontroller, to allow for increased computing power and extra peripherals. Cellular modules often offer quite some flexibility to be employed as stand alone solutions, but more complex applications might require additional channels in shared interfaces or even lower power consumption. So a companion chip should satisfy these requirements by including features that are not commonly available in NB-IoT modules and by guaranteeing high power efficiency. Having two chips on the same board allows for new ways to manage power, like keeping one of the two in sleep mode to save power while the other is working, enabling the IoT device to operate for long lengths of time on a single charge of a battery.

Another important aspect is the development environment, which should include libraries and APIs to interact with peripherals and the cellular modem. Communication with the modem is usually implemented with AT commands, the industry standard for cellular communications.

Finally, companies should be able to easily integrate the module in any device or existing project. So the physical dimensions of the board are critical to make it fit in any design. The more compact the module can be, the easier it is to build an advanced solution around it. This board is in fact intended as a general purpose module with a micro-controller and a cellular modem that is to be mounted on top of a host board, specialized in the particular solution required by the customer.

In this thesis the design of such a board will be addressed, including all the necessary preliminary research on the market, firmware testing on the devkit and the choice of suitable components.

The layout design is based on the BRIKI MBC-LR and BRIKI MBC-WB standardized form factor and pinout, so that it can be interchanged easily on the host board without compromising its functionality.

Chapter 2

Market Analysis

The market of electronic components for IoT devices is relatively new, but it has already a lot to offer. The preliminary research for the MBC-NB design was first aimed to find the most suitable NB-IoT chip for the intended application, which in the end has been the Nordic nRF9160. Then continued with the analysis of already existing solutions based on it, concerning the main features offered and what is missing with respect to the industrial standard proposed by Meteca.

2.1 NB-IoT module choice

The choice of a suitable NB-IoT module was heavily influenced by the requirement on physical dimensions, since the MBC standard requires the board to measure 38 x 16 mm. So the module dimensions must be lower to make it fit correctly, plus the necessary space for traces around it. Several other parameters are relevant in the selection of a suitable NB-IoT module for the MBC-NB design. The most important are: the longevity of the product on the market, completeness of online documentation and the cost of the module.

The design of such a PCB is in fact a long process, which potentially needs some iterations to make it suitable for the market; so it is desirable that the main module of the board will be available on the market for the longest time possible, which usually is 10 years at most. The quality of the documentation and support from the manufacturer is also an important factor in the choice. Since programming the module can be a complex task, finding easily relevant information online about common software errors is essential to guarantee the feasibility of app development. Other parameters considered were supported cellular bands, eSIM compatibility and additional radio protocols like LTE-M or GPS.

Manufacturers producing and selling NB-IoT chips are: Nordic Semiconductor, U-Blox, Quectel, Sequans, SIMcom, ST and others. Unfortunately chips from Quectel, U-Blox and Sequans were excluded at the very beginning since they are too big to fit correctly into the MBC standard, with the smallest one being the Quectel B660K at 17.7×15.8mm which would not allow for enough clearance on the MBC standardized form factor. Among the remaining manufacturers, SIMcom offers the SIM7090G, a chip with many features and interfaces that however seems to lack eSIM support. Also it is available in LGA package only, which would add significant complexity to the design. ST instead has recently rolled out the ST87M01, a potentially suitable chip with minimal dimensions that meets all requirements. Unfortunately at the time of writing it is not yet available on the market. While this means that it will have the longest longevity, the downside is that the documentation needed for the hardware design is not public yet, and so it wouldn't be suitable for ready made solutions in the short term. At last, Nordic Semiconductor offers different chips supporting NB-IoT: the nRF9131 Mini SiP, with its very reduced dimensions would optimal to build the module with a large degree of flexibility in route placement, but is unfortunately still not available on the market. The nRF9160 and nRF9161 on the other hand offer all the required key features in a package that measures 10x16mm, which allows for enough clearance in the MBC standard form factor. Both implements a integrated Arm Cortex-M33 application processor along the cellular modem, which allows for extra computing power and interfaces in a single package.

They are very similar in terms of capabilities, but the nRF9160 was chosen to be integrated in the MBC-NB as more documentation can be found regarding its programming, since it has been released some years before. So it is considered to be the most stable and robust choice. The nRF9161 on the contrary is newer and has additional features, but this means that not as much documentation can be found.

2.2 Boards based on nRF9160

Having chosen the nRF9160 as the NB-IoT module for the MBC-NB the next step is to look for solutions similar to this project that already exist on the market.

This is an important part of the research to confirm that the initial assumption that a NB-IoT module like the MBC-NB is actually needed in the market is true. The competitive advantage is assumed to rely mainly in the high number and variety of interfaces available in a very reduced size, besides offering a electronic standard suitable to match reliability and quality at an industrial level.

- Thing Plus by SparkFun or nRF9160 Feather by CircuitDojo
- Icarus IoT Board v2 by Actinius
- Icarus SoM by Actinius
- Thingy:91 by Nordic
- Walter by QuickSpot, based on Sequans GM02S

These are the most widespread boards that offer NB-IoT support at the smallest size, but none of them is close to the features implemented in the MBC-NB project for several reasons. Most of them don't include a companion micro-controller with extended capabilities in terms of computing power and interfaces availability. All of them are larger in size with respect to the MBC-NB, which limits the flexibility in solution design. Also most of them require proprietary framework like Zephyr and are not compatible to the Arduino IDE.

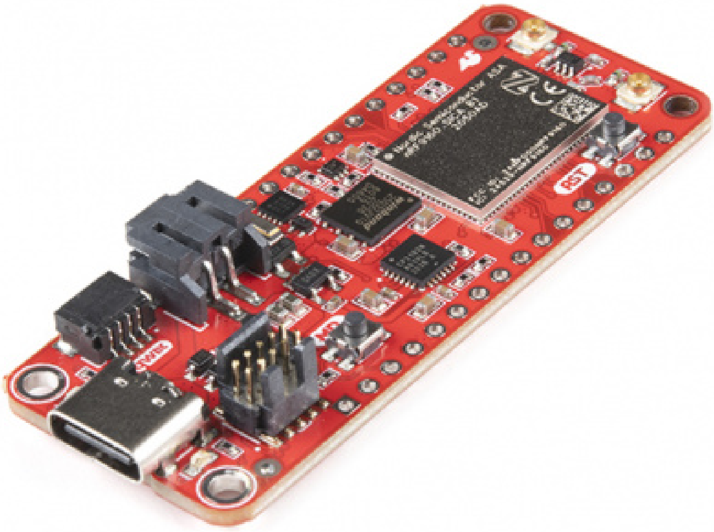


Figure 2.1: Sparkfun Thing Plus nRF9160

Chapter 3

Exploring nRF9160 DK

One of the aims of the MBC series is to offer rapid prototyping through proprietary libraries that include custom API calls to register level code. This accomplishes high performance, low power consumption and easiness of use, as the functions implemented are fine tuned accordingly. The main advantage is that these ready made libraries can be used natively in the Arduino IDE, which is one of the most accessible and easy to use IDEs available. This facilitates the job of customers who need to test ideas and evaluate results quickly in very complex applications.

So in the MBC-NB project it is important to assess if the nRF9160 platform is compatible with register level programming, in order to guarantee that Arduino compatible libraries can be developed without worrying about restriction imposed by the manufacturer. A bare metal embedded system offers in fact much more reliability and flexibility than pre-programmed libraries, that often depend on proprietary source codes that might not be specifically tested for the intended application. Programming directly the functionality at a low level allows to fine tune the execution of microcontroller's processes, in order to optimize power consumption and enable advanced security features. A common configuration used to extend battery life of remote sensors involves the optimization of processes that use radio interfaces, which are usually very power hungry due to high gain power amplifiers, so that they are executed only when it is necessary to transmit or receive data and for the time strictly necessary to carry out the communication. The reliability of remote systems instead can be strengthened by employing custom error-handling routines and watchdog timers tailored to the desired application.

Unfortunately Nordic chips are not intended to be programmed at register level, nor includes APIs to control GPIOs and other interfaces directly, since the manufacturer recommends its proprietary toolchain to develop applications in the Zephyr environment. Zephyr is a Real-Time Operating System (RTOS) that supports a large number of commercial boards. An RTOS is a particular class of operating system that is intended to manage hardware resources and execute tasks with precise timing constraints, ensuring predictable and deterministic behavior. An RTOS will give precedence to one task over another based on their urgency, thanks to features such as preemptive multitasking, real-time scheduling, and low-latency interrupt handling. On the other hand, bare-metal programming consists of writing software straight to the hardware without any abstraction layer. Bare-metal software offers better control of hardware and minimum overhead.

In the MBC-NB project the bare metal approach is more desirable as the integrated Arm Cortex-M33 application processor could be used to offer higher flexibility in terms of peripherals and power optimization. The cellular modem on the contrary can be controlled only through AT commands, so in case of applications based only around radio communications and software, Zephyr higher level approach would be a better choice.

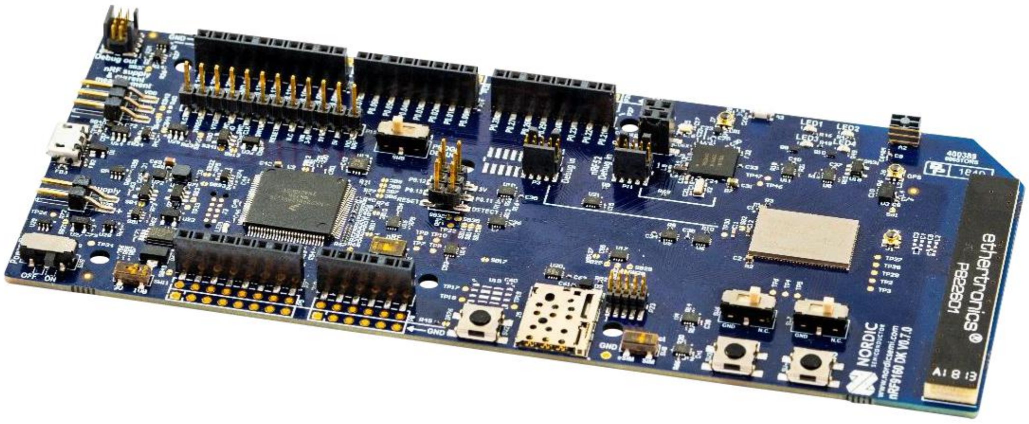
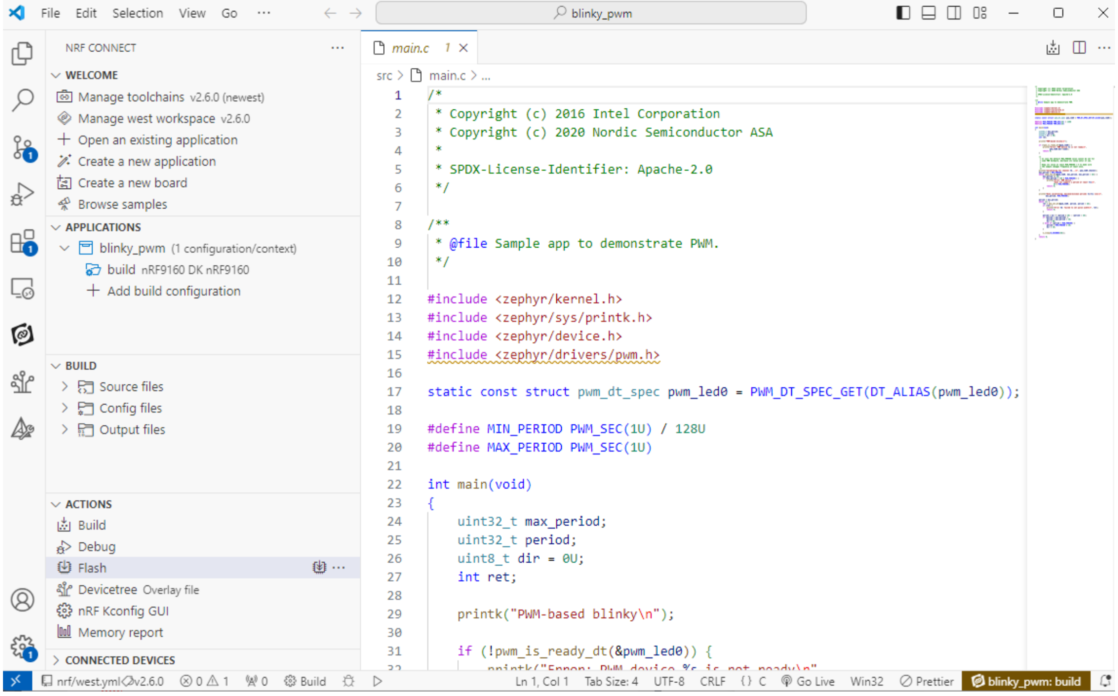


Figure 3.1: nRF9160DK

3.1 nRF Connect environment tests

This and other considerations have been made after thoroughly testing the nRF9160DK through the nRF Connect environment, which includes the Zephyr framework and libraries. Testing with AT commands and basic examples has been conducted to assess the offered functionalities and the feasibility of the project itself.

The nRF Connect environment is implemented as an extension in Visual Studio Code IDE. The toolchain is installed using the software nRF Connect for Desktop, which is then utilized in VS Code to build and flash programs on the device. In the figure 3.2 a PWM blink example ready to get flashed is shown. The example code includes several proprietary libraries from the Zephyr framework, which implement all the necessary functions to manage GPIOs, print statements and timing functions.



```c
/*
 * Copyright (c) 2016 Intel Corporation
 * Copyright (c) 2020 Nordic Semiconductor ASA
 *
 * SPDX-License-Identifier: Apache-2.0
 */

/**
 * @file Sample app to demonstrate PWM.
 */

#include <zephyr/kernel.h>
#include <zephyr/sys/printk.h>
#include <zephyr/device.h>
#include <zephyr/drivers/pwm.h>

static const struct pwm_dt_spec pwm_led0 = PWM_DT_SPEC_GET(DT_ALIAS(pwm_led0));

#define MIN_PERIOD PWM_SEC(1U) / 128U
#define MAX_PERIOD PWM_SEC(1U)

int main(void)
{
    uint32_t max_period;
    uint32_t period;
    uint8_t dir = 0U;
    int ret;

    printk("PWM-based blinky\n");

    if (!pwm_is_ready_dt(&pwm_led0)) {
```

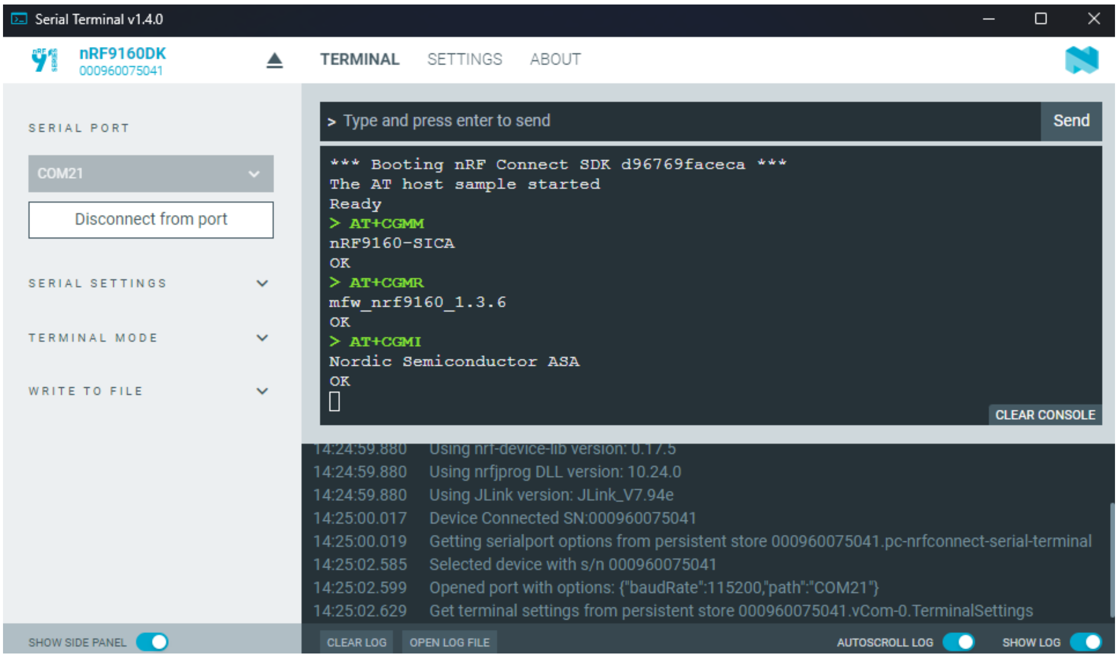
Figure 3.2: nRF Connect environment in Visual Studio IDE

This example was studied to understand the structure of Zephyr libraries and whether a bare metal approach was feasible. Unfortunately these libraries are not open source nor extensively documented, so it is only possible to learn how to use the provided functionality without actually understanding the implementation. This is a huge limit in the pursuit of very low power consumption, since every process run on the microcontroller needs to be under the control of the firmware designer, in order to avoid unnecessary functions running and draining power unless

they are strictly necessary to the application functionality.
After further research in the Nordic documentation, the *nrfx library* on GitHub was found, provided directly from Nordic, that allows fine control on GPIOs and interfaces. Also a *blink example code* is available on their forum. It follows the CMSIS standard for Microcontroller programming. CMSIS (Common Microcontroller Software Interface Standard) is a vendor-independent hardware abstraction layer developed by ARM for ARM Cortex-M microcontrollers. It provides a standardized set of software components, including drivers, peripheral access, and real-time operating system (RTOS) interfaces, to streamline the development process. By offering a consistent API, CMSIS allows developers to write bare-metal code—code that interacts directly with hardware—without relying on a full operating system, thus optimizing performance and minimizing overhead. Its modular design facilitates hardware abstraction, enabling easier portability across different microcontroller vendors while simplifying low-level programming tasks like configuring peripherals, handling interrupts, and accessing registers. The code is reported in the Appendix A.1.
So it is definitely possible to write bare metal code for the Nordic nRF9160 in a way that benefits very low power applications. However this path needs further research to be implemented in a functional product.

3.1.1 AT commands tests

As previously stated the nRF9160 modem can be controlled using standard and proprietary AT commands. AT commands (Attention commands) in the nRF9160 chip are used to control the modem architecture, facilitating communication between the host processor and the modem for cellular operations (LTE-M and NB-IoT) and GNSS functionality. Based on the 3GPP standard, these text-based commands allow the host to manage network registration, send/receive SMS, handle data connections, and control power management, among other tasks. The simplicity of AT commands offers a lightweight and easy-to-implement interface, making it ideal for resource-constrained IoT devices. This approach enables developers to control the modem without having deep knowledge of the underlying firmware. However, they come with restricted flexibility for complex tasks and slower communication compared to more direct, lower-level interfaces. An example would be the Socket API, but using a lower-level API requires a deeper understanding of the modem's internal workings and is more complex to implement.
In the image 3.3 it is shown a basic interaction with the modem through the use of AT commands to fetch informations like firmware version, hardware model and manufacturer.

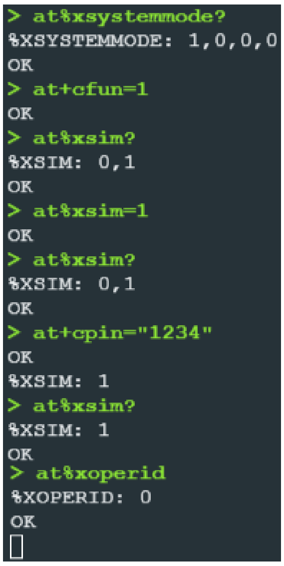


```
*** Booting nRF Connect SDK d96769faceca ***
The AT host sample started
Ready
> AT+CGMM
nRF9160-SICA
OK
> AT+CGMR
mfw_nrf9160_1.3.6
OK
> AT+CGMI
Nordic Semiconductor ASA
OK
```

```
14:24:59.880   Using nrf-device-lib version: 0.17.5
14:24:59.880   Using nrfjprog DLL version: 10.24.0
14:24:59.880   Using JLink version: JLink_V7.94e
14:25:00.017   Device Connected SN:000960075041
14:25:00.019   Getting serialport options from persistent store 000960075041.pc-nrfconnect-serial-terminal
14:25:02.585   Selected device with s/n 000960075041
14:25:02.599   Opened port with options: {"baudRate":115200,"path":"COM21"}
14:25:02.629   Get terminal settings from persistent store 000960075041.vCom-0.TerminalSettings
```

Figure 3.3: Basic AT commands interaction with nRF9160DK

AT commands can be used to connect to the cellular network with a working SIM (Subscriber Identity Module).



```
> at%xsystemmode?
%XSYSTEMMODE: 1,0,0,0
OK
> at+cfun=1
OK
> at%xsim?
%XSIM: 0,1
OK
> at%xsim=1
OK
> at%xsim?
%XSIM: 0,1
OK
> at+cpin="1234"
OK
%XSIM: 1
> at%xsim?
%XSIM: 1
OK
> at%xoperid
%XOPERID: 0
OK
```

Figure 3.4: Connection to cellular network made with AT commands

3.2 Bare metal programming

After deeper research, a library that implements bare metal programming for the nRF9160 was found on GitHub. It is offered by Nordic itself and includes standalone drivers for peripherals, but the manufacturer allegedly does not offer support for custom build environments, so this has been identified as one of the future challenges of the project MBC-NB. The ability to build bare metal code without the use of the Zephyr framework would in fact allow customers to have more control on the chip, enabling potentially lower power consumption and better efficiency overall.

The code cited in the appendix A.1 was successfully tested on the provided nRF9160DK. This shows that bare metal programming is indeed possible on the nRF9160 by using the correct libraries. Here is the source of the code

Chapter 4

MBC-NB secondary components

Having definitely chosen the nRF9160 as the main chip of the MBC-NB, other secondary components must be defined in order to complete the module functionality. As previously said a microcontroller companion chip would offer significant advantages over the application of the nRF9160 only. Even if it already implements one inside the SiP, it has few GPIOs and interfaces and quite limited computing power. It is definitely enough to manage the cellular modem, but could not be adequate to satisfy the requirements of complex applications that require multiple peripherals. Besides, a eSIM is an essential component that works together with the nRF9160 to establish cellular radio communications. As in any cellular device, a Subscriber Identity Module is required, and nowadays it can either be a nanoSIM or a eSIM. At last, other passive components are needed to complete the electrical design of all the main chips mentioned so far, like protection diodes, ferrites and the most obvious capacitors and resistors.

4.1 Microcontroller

There are many microcontroller manufacturers on the market that make a lot of different solutions, and most of them would be probably suitable for the application. However, in this thesis, only chips from ST were considered in this choice, as they are regarded as the potentially most advanced in terms of functionalities and, more importantly, reliable and easy to use.

Chips of different series and kinds were considered, like Cortex M0+, Cortex M4 and Cortex M33 from the lowest power hungry chips produced by ST. As in the NB-IoT module choice, the main requirement is once again the size of the chip, so only packages under 5x5mm were considered. This has significantly reduced the pool of options, but still many potentially suitable chips were found among the low power chips offered by ST. Another essential feature that the companion chip should have is the USB interface, as the nRF9160 doesn't have it. In fact all the commercial boards based around the nRF9160 also include either the nRF52 as companion chip, which has a USB interface, or a UART to USB chip, used to communicate directly with the nRf9160. Initially this last option was briefly considered, as it would provide a more simple solution to program the nRF9160. However it was quickly discarded as a UART to USB chip takes almost as much board area as a microcontroller and has also a similar cost, for a fraction of the functionality. Additionally the most used chip in other nRf9160 boards, the CP2102N, has a current draw of about 10mA in normal operation and around 200uA in standby, which can is not the best choice for very low power IoT devices.

Chips offered by ST were examined not only considering the availability of 5x5mm package or less and the presence of the USB interface, but also regarding power consumption related to clock frequency and in different standby modes. Initally chips from low power series L and series G were considered, as they are quite cheap and come in very small UFQFPN28 or UFQFPN32 packages of 3x3mm and 4x4mm. Those would be particularly suitable to fit in the MBC-NB layout since the available area is very constrained. However the pin count is very low and, more importantly, none of them offered a USB interface, so they had to be discarded. Then chips from series U were examined, as they offer ultra low power consumption and are available in 5x5mm UFBGA64 packages, which is compatible with the available area on the MBC-NB. A Ball Grid Array package surely poses some difficulties in the layout design and in the assembly phase, but is ultimately the best compromise in terms of occupied area and pin count.

In the end, the STM32U545REI6 was chosen to be the nRF9160 companion chip, both for the high clock frequency and low power consumption, which make for a very good efficiency, as stated in its Coremark benchmark results. But, more importantly, it also offers a large number of crypto protocols, including the most advanced ones.

4.2 eSIM

An eSIM has a number of significant advantages over a nanoSIM in several important ways: mainly with flexibility and in space-saving. While the nanoSIM requires a physical card to be inserted into the device, the eSIM is directly embedded into the hardware, thereby doing away with the need for a SIM card slot. This frees up space in compact devices like the MBC-NB, making them more durable with fewer exposed components. Besides, eSIMs also allow for remote provisioning, wherein a user will be capable of changing carriers or turn on plans with the equivalent ease of comfort to not have to replace the SIM card physically. That is pretty helpful for IoT applications and devices that may be deployed to hard-to-reach locations where it would become impractical to change out a physical SIM. Equally, eSIM technology improves security by lessening the risk of SIM card tampering or theft.

A integrated eSIM on the MBC-NB module has therefore been regarded as a essential component for the ease of use of the module, so that a customer would need fewer steps toward building a functioning application. Unfortunately in the retail market there is not much choice in terms of eSIM components, as the only manufacturer selling it in electronic shops platforms seems to be ST with the ST4SIM-220M, a very small in size all-in-all chip that is compatible with the nRF9160 SIM pinout.

4.3 Passive components

In electronic design, selecting and implementing passive components like ferrites, protection diodes, capacitors, and resistors is vital for ensuring stability and protecting circuits. Their correct values, package sizes, and placement can significantly impact performance and reliability. This section highlights the critical role of these components and how they contribute to the overall success of the design.

4.3.1 Ferrites

Incorporating ferrites and protection diodes is critical to enhancing the robustness and reliability of electronic designs. Ferrites, whether in bead or core form, play a pivotal role in mitigating electromagnetic interference (EMI) by filtering out high-frequency noise from power lines or signal traces. This helps shield sensitive signals and prevents external noise from disrupting the system's performance. Protection diodes complement this by safeguarding circuits against voltage spikes caused by electrostatic discharge or switching transients in inductive loads. These diodes clamp excessive voltage to safe levels, protecting delicate components and ensuring stable operation, even in environments prone to power fluctuations. Together, ferrites and protection diodes contribute to creating a more durable design, shielding it from electrical disturbances that could lead to failures or malfunctions.

To choose the correct ferrite to filter noise at high frequencies a tool on the Murata website was used. It allows to choose from the preferred band to filter out, which in this case is in the range 300MHz-1GHz since GPS and LTE communications work around this range. The recommended circuit to address this range is a C Bead C configuration, so a series ferrite bead and two parallel capacitors. The tool then provides the values of said capacitors and their model. Results of the simulation are in figure 4.1 and the recommended circuit is depicted in figure 4.2 as it has been implemented in the final design. Further testing will be needed to confirm the functionality of this filter in the operation of LTE and GPS radio communications.

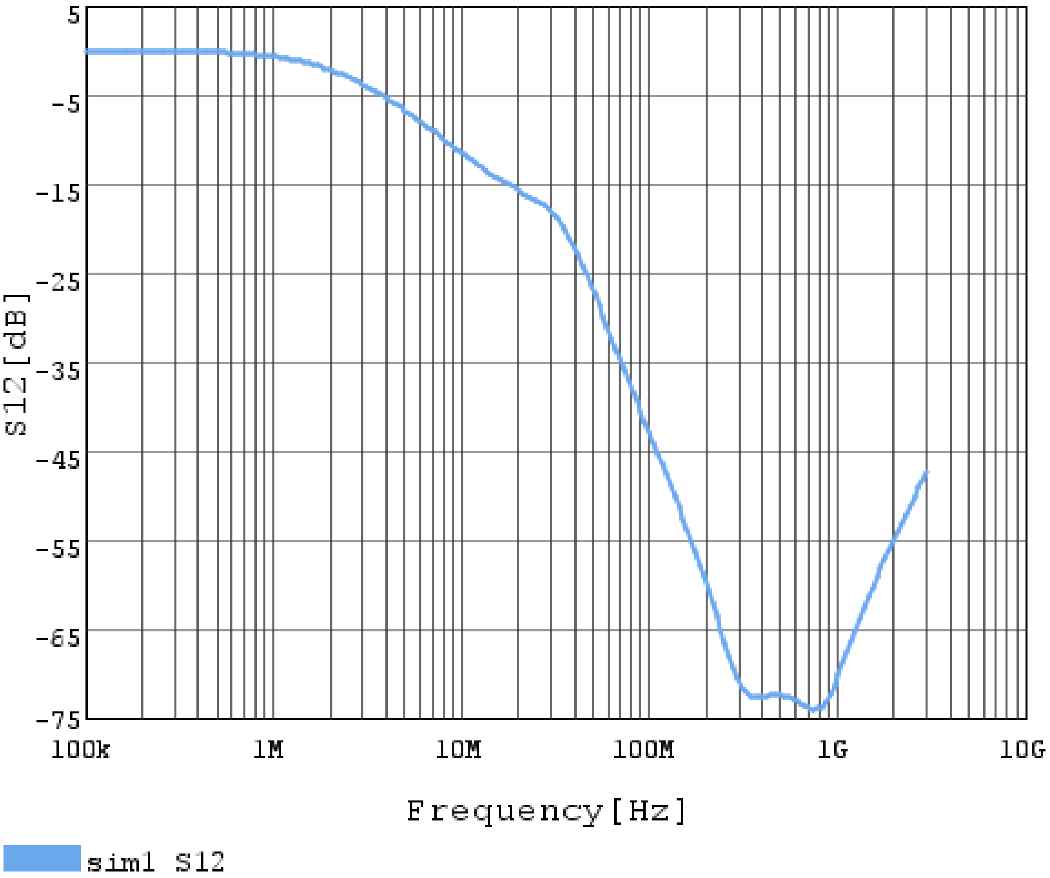


Figure 4.1: Simulation results with a ferrite and two parallel capacitors

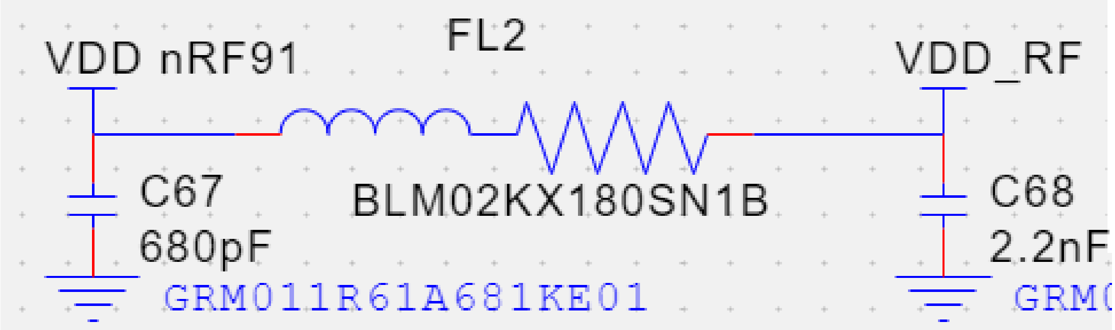


Figure 4.2: Power supply filter configuration

4.3.2 Capacitors

The correct selection and placement of capacitors are equally important for ensuring stable and efficient circuit performance. Bulk capacitors, with their higher capacitance values, are essential for storing and supplying energy to smooth out voltage fluctuations in power supplies. Positioned near the power input or across power rails, these capacitors help maintain a steady voltage, especially during periods of peak demand, preventing sudden power dips (called brownout) that could compromise performance. In contrast, decoupling capacitors, typically smaller in value, are strategically placed near individual integrated circuits (ICs) or other sensitive components. Their primary role is to filter high-frequency noise, ensuring signal integrity and reducing EMI. Proper placement, particularly near IC power pins, enhances their effectiveness. It is crucial to place decoupling capacitors as close as possible to the IC's power pins because parasitic inductance, which is inherent in PCB traces and component leads, must be minimized. Any inductance in the path between the capacitor and the IC can reduce the capacitor's ability to filter out high-frequency noise effectively. High parasitic inductance creates a bottleneck for rapidly responding to sudden changes in current demand, which is especially critical in high-speed digital circuits. As the frequency of operation increases, the inductive impedance becomes more significant, potentially allowing noise and voltage spikes to propagate, which can degrade the performance or even cause malfunction of the IC. High parasitic inductance can also reduce the effectiveness of the capacitor in supplying instantaneous current to the circuit during a switching event, which can result in power integrity problems, such as voltage droops across supply lines. This may be manifested in timing errors, degraded signal integrity, and increased EMI that might raise the possibility of system instability. In high-performance designs, several capacitors of different values (a combination of bulk and high-frequency ceramic capacitors) may be put in parallel to cover the wide range of frequencies for further noise reduction and hence allow reliable operation. Thus, with power integrity improvement by optimization of parasitic inductance in capacitor placement, it directly improves circuit reliability enhancement. By carefully choosing both bulk and decoupling capacitors, signal integrity can be significally improved.

4.3.3 Resistors

Resistor selection is just as crucial, serving various roles such as current limiting and setting logic states in pull-up or pull-down configurations. Choosing the correct resistor value is essential to prevent damage to ICs by limiting current flow within safe thresholds. A resistor with too low a value might allow excessive current, risking damage, while too high a value could impair circuit functionality. In pull-up and pull-down configurations, resistors help maintain correct voltage levels when pins are not actively driven, ensuring proper logic operation without excessive current draw. Finding the balance of performance and power consumption is critical, especially for low-power applications. The resistor should serve its functionality, such as keeping proper voltage levels or current regulation, but at the same time the current through the resistor must be reduced to a minimum in order to achieve maximum battery life. In battery-powered devices, excessive power consumption can drastically reduce the operational time of the system, making it less efficient and reducing its usability. The resistors used shall be balanced between their values for such a balance to be achieved. For pull-up or pull-down applications, for example, it must be low enough so as not to impede reliable logic transition yet as high as possible so that current can keep low when the pin is at a fixed state. However, increasing the resistance reduces the quiescent current, which can extend battery life. But if too large, it may slow down signal transitions or make the logic level vulnerable to noise. On the other hand, a lower resistance might improve its performance at the cost of higher continuous power consumption. It means that the optimum resistor value should be a sort of compromise whereby iw works as expected but consumes the least possible current to maximize battery life. This balance is especially important in modern portable electronics, where every milliamp saved can significantly extend device operation between charges.

4.3.4 Package sizes

In addition to selecting the correct values, choosing the right package size for resistors and capacitors is critical, especially for thermal management and power dissipation. In this project, the smallest package that can be used is the 0201 size, which is sufficient for most low-power duties. However, for areas where higher power dissipation is required, larger packages like 0402 or even 0603 are considered to handle the heat and ensure reliable operation.
This is true especially for capacitors, that may experience less capacitance variation with temperature compared to smaller packages. Smaller packages are in fact susceptible capacitance variation due to thinner dielectric layers, which are more sensitive to temperature and voltage stress, contributing to higher derating rates. This consideration ensures that the components not only meet electrical requirements but also function correctly within the thermal constraints of the board, thus contributing to the overall robustness and longevity of the design.

Chapter 5

MBC-NB Schematic

5.1 OrCad Capture

OrCAD consists of an integrated EDA solution with advanced functionalities of both schematic and PCB design. OrCAD Capture is used widely for the creation and management of a schematic. It is designed for the design of the circuit, management of libraries, and integration of simulations. These support hierarchical designs, constraint management, and full integration with other tools in the OrCAD suite.

Allegro PCB Designer is a feature-rich system for PCB layout and design, part of the OrCAD suite. It allows for signal integrity checking, design rules, and 3D for the best-performing board. OrCAD Capture and Allegro PCB Designer form a complete solution for quality electronic designs.

Online libraries, like SnapEDA, UltraLibrarian or Octoparts, can make it easy to access the schematic symbols, footprint and 3D models that greatly simplify integrating specific components in a PCB design. Besides that, it also ensures at least some of the critical information necessary for a design, which is supplied in that library, such as pinouts and mechanical dimensions. On the other side, they may not be available in the needed configuration for every component. Sometimes, a few of the available parts may be incorrect in pin layouts or need manual edits, which therefore means that the designers should check the correctness on the component datasheet and make appropriate adjustments in the CAD.

5.2 nRF9160

It may happen that components sourced from online libraries require further customization to fit the specific needs of a design.

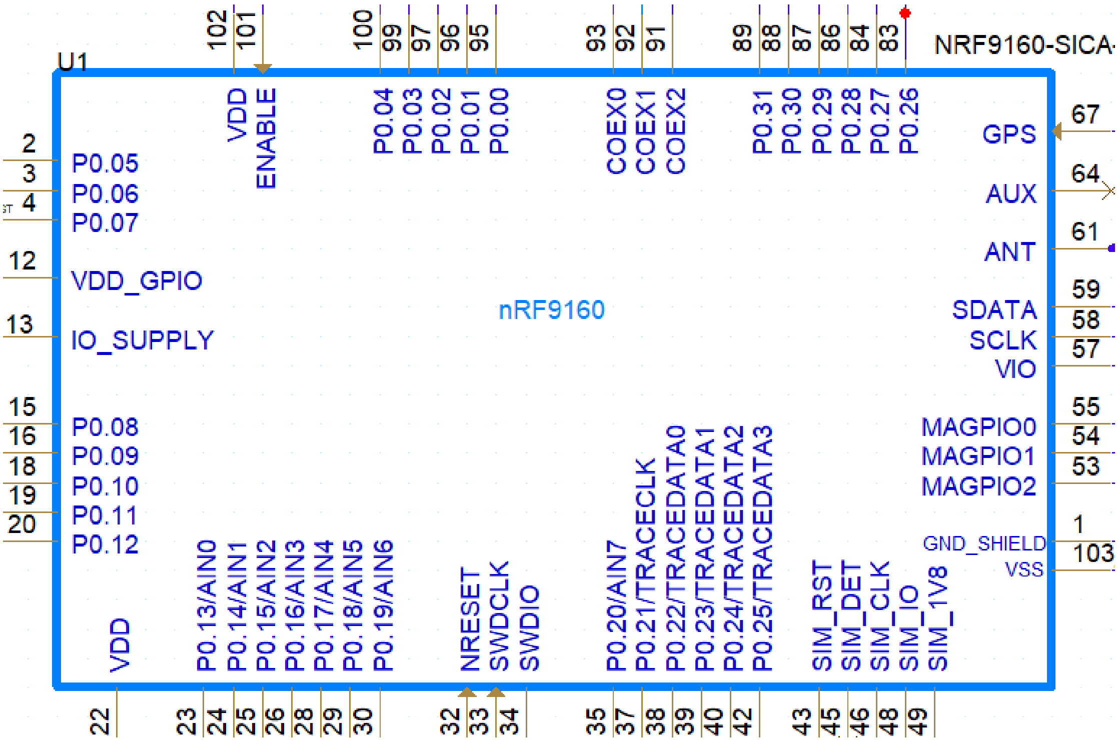


Figure 5.1: Custom made nRF9160 component in OrCAD

Using the "Edit Part" option from OrCAD, the designer can edit such components to make sure the pin-out and the layout exactly meet the project requirements. The process in this thesis has followed that for the nRF9160 quite closely, relying on established reference boards-particularly the nRF9160DK and Nordic Thingy, providing a reliable basis to get started with the schematic design.

5.2.1 Pin Mapping

Mapping the pins of the nRF9160 is one of the important stages of making the design compatible with the Briki standard form factor. The process starts by identifying "reserved" pins, which are disregarded as they are for manufacturer use only, and grouping ground pads and shield pins together, so that they can be easily connected. A defined area on the board will be granted to the analog pins and traces, to mitigate disturbances, whereas digital pins should be sorted by

their alternative functions, such as I2C, SPI, and UART. In the nRF9160 those are actually shared by all the digital pins thanks to multiplexers, so that any pin can be used for any interface, however knowing that the total number of channels is limited.
This mapping also determines the orientation of the chip on the board as the pinout had to align with the Briki standard form factor, which dictates that digital pins should be positioned on one side and analog pins on the other. This greatly helps in keeping analog and digital signals separated to avoid interference. Radio interfaces were also in the right position to comply with the form factor. The nRF9160 pinout resulted to be already compatible as it is with the Briki standard, so in the end the pinout analysis results were used to better understand the chip functionalities and properly design connections to exploit all the chip's features.

5.2.2 Passive Components

After mapping the pins, the next step in completing the nRF9160 schematic is selecting the passive components, with guidance from Nordic's reference boards. Supply capacitors values were chosen accordingly to the reference design, as well as the ferrite bead filtering the main power supply line. Besides the recommended ones, additional components were placed in order to get specific functionalities for the MBC-NB.

Resistors sizing

In particular since the peculiarity of the Briki standard is to have two chips working together, additional connections are designed to allow them to communicate and interact. The standard requires the following:

- LPUART communication lines between the chips, that must also be accessible from external pins
- Mutual reset nRST lines to allow for either of the chips to reset the other if necessary
- Mutual interrupt lines to improve the communication capability among the two chips.

So, resistors are placed on the LPUART lines near the external pins to prioritize communication between the chips first, and secondarily to external devices. So they were placed in series to external pins, with low values of 100Ω in order to give

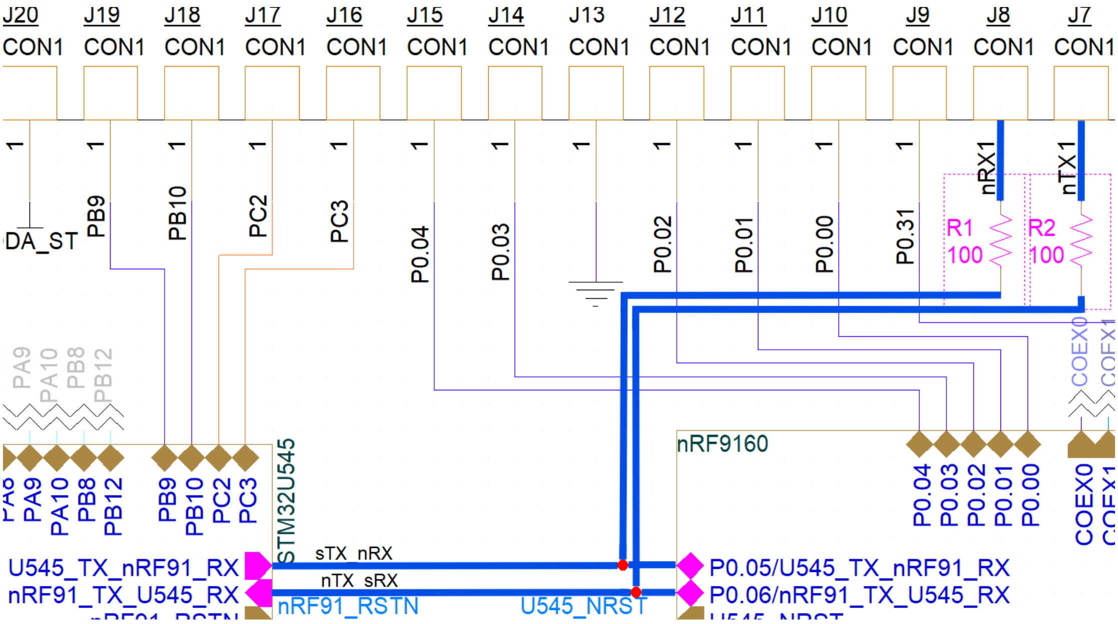
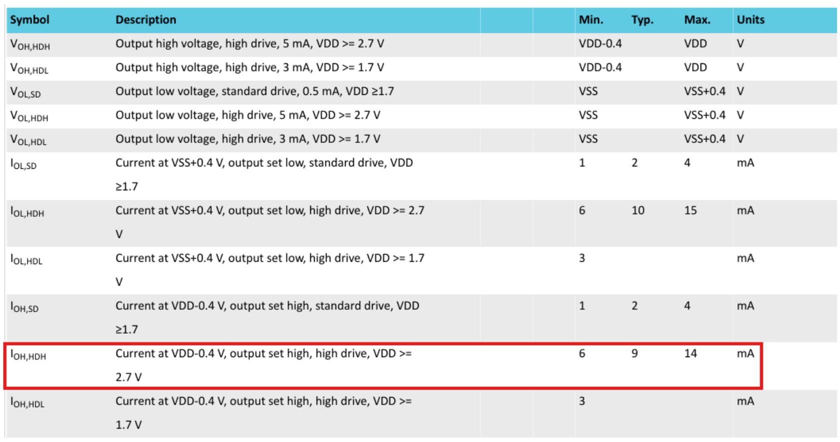


Figure 5.2: LPUART communication line with two 100Ω

them a slightly slower reaction (rise time) than the direct connection between the chips.

Other resistors on the mutual reset lines prevent exceeding the GPIO drivers' current draw threshold in cases where one chip is being reset simultaneously by both the other chip and an external source, which could otherwise cause a short circuit. These resistor were sized according to GPIO drivers current specification from the datasheet. The maximum current that nRF9160 GPIO drivers can provide in high state, supplied at more than 2.7V is 14mA, with the typical value at 9mA, according to nRF9160 datasheet in figure 5.3. A voltage supply of 3.3V was considered in case of a battery powered system. So using a conservative approach, the resistor on the nRF9160 digital pin connected to the STM32 reset pin was sized at 1kΩ so that the maximum current drawn from the nRF9160, in case it pulls simultaneously with the external reset, is around 3.3mA, according to Ohm's law.



Symbol	Description	Min.	Typ.	Max.	Units
$V_{OH,HDH}$	Output high voltage, high drive, 5 mA, VDD >= 2.7 V	VDD-0.4		VDD	V
$V_{OH,HDL}$	Output high voltage, high drive, 3 mA, VDD >= 1.7 V	VDD-0.4		VDD	V
$V_{OL,SD}$	Output low voltage, standard drive, 0.5 mA, VDD ≥1.7	VSS		VSS+0.4	V
$V_{OL,HDH}$	Output low voltage, high drive, 5 mA, VDD >= 2.7 V	VSS		VSS+0.4	V
$V_{OL,HDL}$	Output low voltage, high drive, 3 mA, VDD >= 1.7 V	VSS		VSS+0.4	V
$I_{OL,SD}$	Current at VSS+0.4 V, output set low, standard drive, VDD ≥1.7	1	2	4	mA
$I_{OL,HDH}$	Current at VSS+0.4 V, output set low, high drive, VDD >= 2.7 V	6	10	15	mA
$I_{OL,HDL}$	Current at VSS+0.4 V, output set low, high drive, VDD >= 1.7 V	3			mA
$I_{OH,SD}$	Current at VDD-0.4 V, output set high, standard drive, VDD ≥1.7	1	2	4	mA
$I_{OH,HDH}$	Current at VDD-0.4 V, output set high, high drive, VDD >= 2.7 V	6	9	14	mA
$I_{OH,HDL}$	Current at VDD-0.4 V, output set high, high drive, VDD >= 1.7 V	3			mA

Figure 5.3: Maximum current that can be provided by nRF9160 GPIO drivers when supply is higher than 2.7V

Its counterpart on the STM32 connected to the nRF9160 reset was sized in the same way, with a declared maximum current drawn from any I/O pin of 20mA, as in figure 5.4. So considering the same supply voltage of 3.3V, a resistor of 220Ω was chosen to limit the current at 15mA. However it must be pointed out that the nRF9160 reference design already includes a 1kΩ series resistor on its reset pin, so the current is likely already limited enough. Further testing will prove whether if an additional series resistor is needed or if the reference design one is enough.

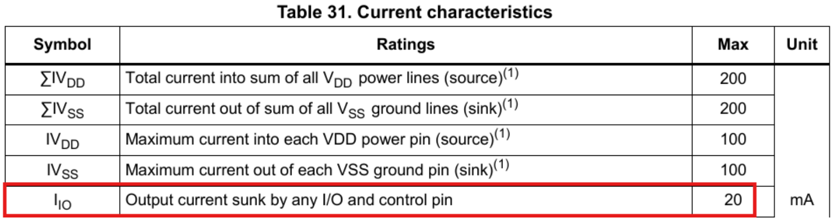


Table 31. Current characteristics

Symbol	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	200	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	200	
IV_{DD}	Maximum current into each VDD power pin (source)(1)	100	
IV_{SS}	Maximum current out of each VSS ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin	20	

Figure 5.4: Maximum current provided by STM32U545 I/O pins

Finally, the interrupt lines network include placeholders for pull-up or pull-down resistors, to allow flexibility in the firmware implementation. A 100kΩ resistor hence connects the interrupt line wither to the supply line or to the ground in order to draw the least amount of current, while ensuring a known state of the signal. The value is chosen to have a balance between a low current draw and a reliable functionality. A pull-up configuration is depicted in the schematic in figure 5.5 as it is usually more commonly used.

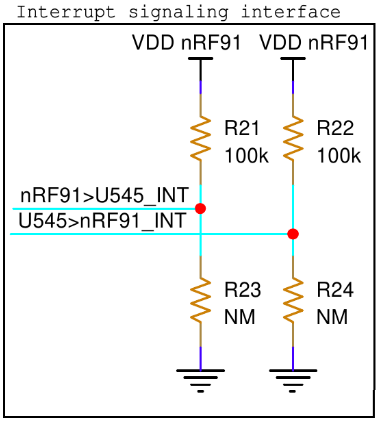


Figure 5.5: Interrupt resistors network

eSIM network

Protection diodes are placed on the pins going to external nanoSIM connector for voltage spike protection, and zero-ohm resistors allow switching between the mounted eSIM and an external nanoSIM connector, providing flexibility in the design of solutions. Initially a array of four zero-ohm resistors was chosen to facilitate the mounting process, however this kind of component is sold in small quantities by few suppliers. So regular zero-ohm resistors were implemented instead, making the mounting process slightly slower but ensuring the availability of all the components, as they are way more common.

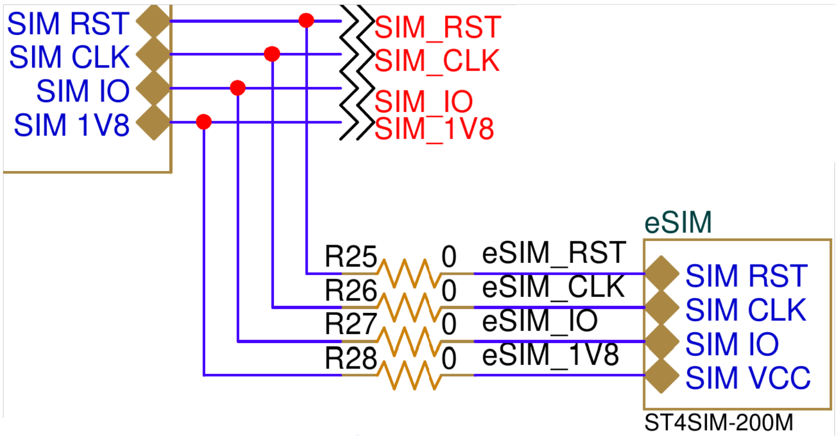


Figure 5.6: Zero ohms resistors to switch between nanoSIM and eSIM

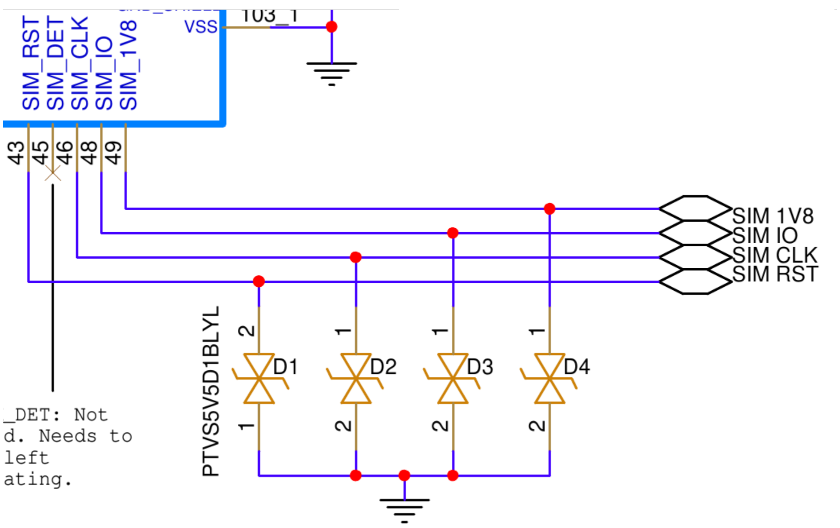


Figure 5.7: TVS diodes protect nRF9160 pins for the external nanoSIM interface

The LPUART series resistors and the eSIM components designs were taken from the MBC-LR design, in the effort to reuse functional designs and to standardize particular components, like protection diodes. This approach speeds up the design processes and minimizes inventory overheads, reducing overall operating costs.

5.2.3 RF Design

The RF network design for the board involves both GPS and LTE connectivity. The GPS network is adopted directly from the reference design, featuring distinct pad and antenna connectors to ensure proper signal routing, as in figure 5.8.

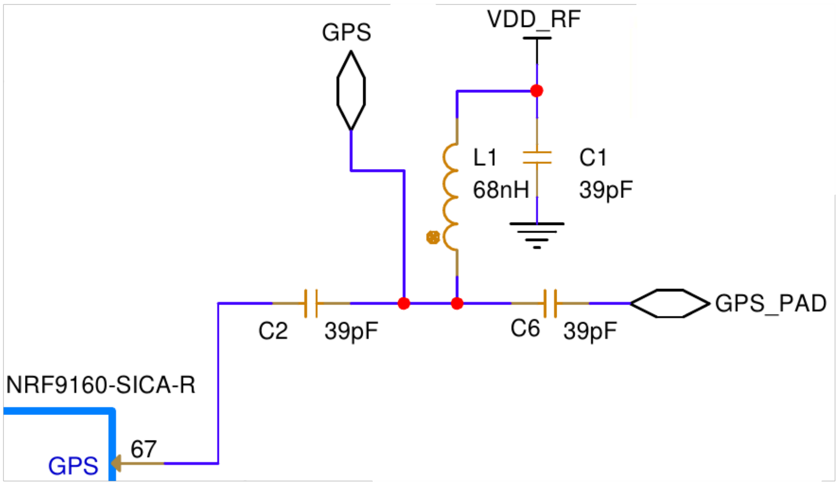


Figure 5.8: GPS matching network

On the other hand, the LTE network has been modified. Instead of placing the antenna connector in series with the pad connector, it is positioned in parallel to the matching network, providing a different signal path, as in figure 5.9.

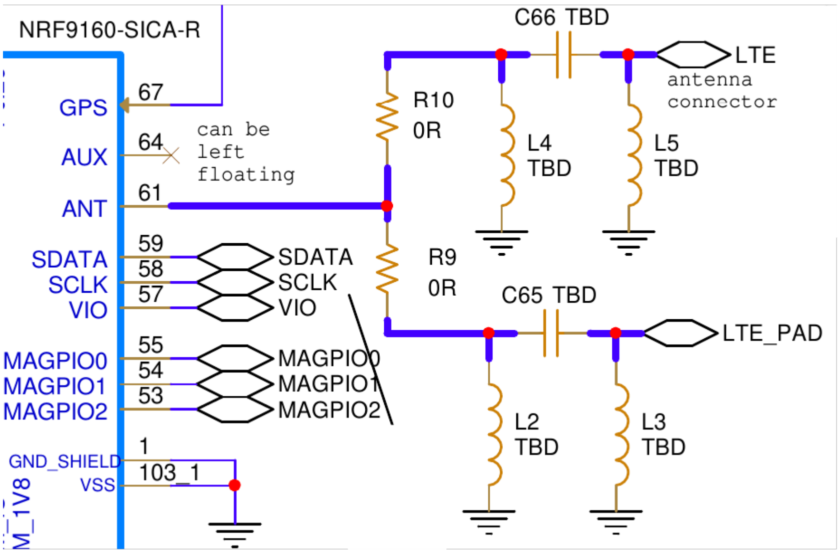


Figure 5.9: LTE matching network

In the current design the impedance matching network on the LTE pin consists of placeholder components in a PI configuration, awaiting further tuning, while the GPS matching network is at the moment implemented with values directly taken from the reference design. These value choices will need to be furtherly tuned after testing the prototype's radio interfaces, as signal quality might be influenced by several other factors, like the ground plane size and the PCB shape and stack-up. The best practice is to start testing the prototype with values proposed by the datasheet or reference designs and then tuning them according to the prototype features.

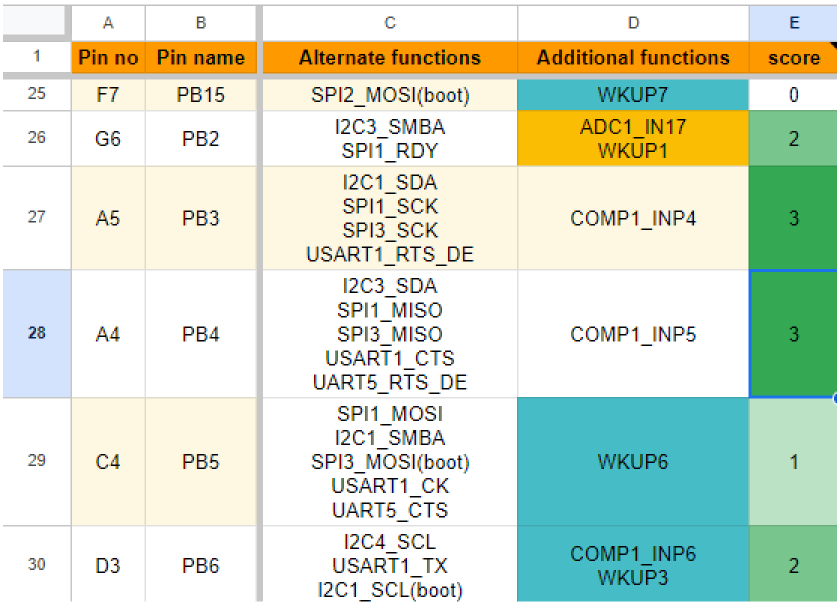
5.3 STM32U545

The STM32U545 MCU is especially notable for the great performance, low power, and enhanced security it provides, thanks to its ARM Cortex-M33 core. A wide range of support for communication interfaces enables wide applications in various scenarios. The most valued pro of this microcontroller in this project is the possibility of its use within a compact 5x5mm BGA package, which is fitted appropriately into the design constraints of the board for compact space. The STM32U545 will be an ideal companion chip to the nRF9160, providing additional processing power and enhanced connectivity options that complement the cellular IoT capabilities of the nRF9160, thus ensuring seamless and robust overall system design.

5.3.1 Pin Mapping

The process of pin mapping for the STM32U545 requires careful planning due to the wide distribution of communication interfaces across its pins, with each pin capable of serving multiple functions. Mapping all possible functionalities is essential, as pins with more versatility are connected to easily accessible castellated pads on the edge of the board for frequent use. Pins with less critical or secondary functions are placed on LGA pads on the bottom layer. LGA pads were chosen to allow for expanded functionality of Briki modules, while guaranteeing compatibility with the standard form factor.

The first step is setting a minimum requirement for the number of interfaces that the ST chip should provide: at least two SPI channels, two I2C channels, and two UART/USART channels. For the sake of this process, each pin is then evaluated and assigned a score based on how many useful interfaces it supports. For example, a pin that handles both a SPI link and a I2C link receives a higher score than one that supports only a single interface link of I2C.



	A	B	C	D	E
1	Pin no	Pin name	Alternate functions	Additional functions	score
25	F7	PB15	SPI2_MOSI(boot)	WKUP7	0
26	G6	PB2	I2C3_SMBA SPI1_RDY	ADC1_IN17 WKUP1	2
27	A5	PB3	I2C1_SDA SPI1_SCK SPI3_SCK USART1_RTS_DE	COMP1_INP4	3
28	A4	PB4	I2C3_SDA SPI1_MISO SPI3_MISO USART1_CTS UART5_RTS_DE	COMP1_INP5	3
29	C4	PB5	SPI1_MOSI I2C1_SMBA SPI3_MOSI(boot) USART1_CK UART5_CTS	WKUP6	1
30	D3	PB6	I2C4_SCL USART1_TX I2C1_SCL(boot)	COMP1_INP6 WKUP3	2

Figure 5.10: Pins get assigned a score depending on the number of useful functionalities

In figure 5.10 it can be seen an extract of the sheet used to evaluate pin functionalities. Data on the alternate functions of every pin has been taken from the STM32U545 datasheet, for the considered chip version. Using this scoring system, pins with higher versatility have higher priority being placed on the castellated pads of the board to allow for easy access, while those with lower scores will be positioned on the bottom layer. This approach optimizes the layout and meets the functional requirements of the design.

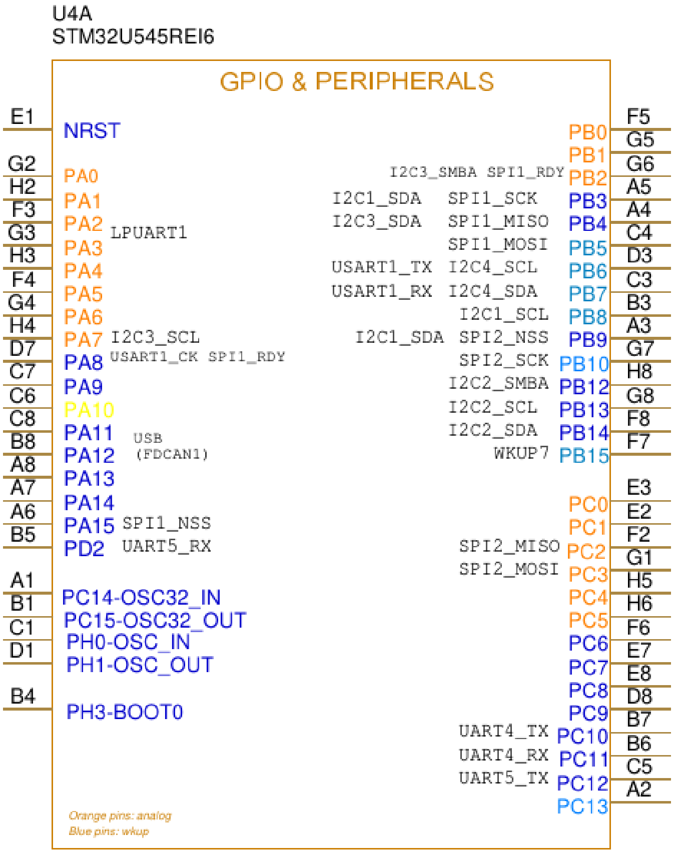
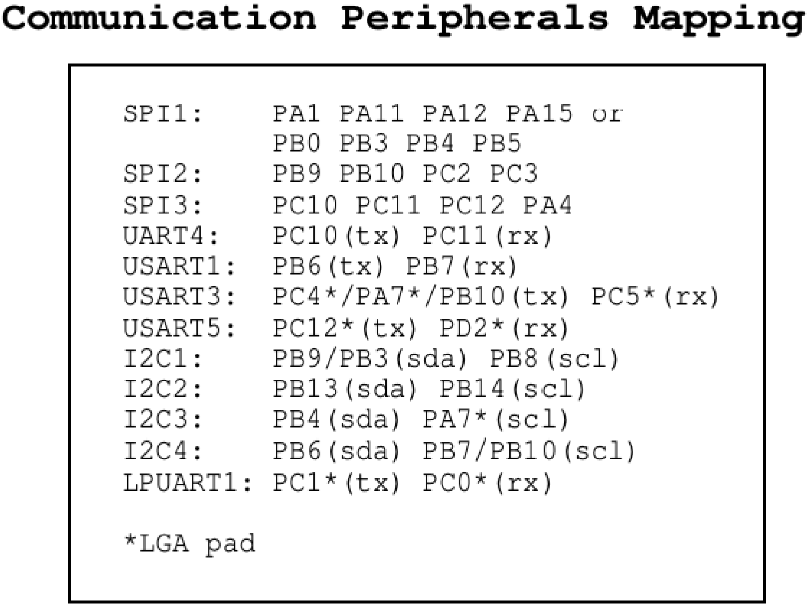


Figure 5.11: STM32U545 pin assignments

At the end of the analysis a total of three SPI channels, four I2C, three UART/USART and an extra LPUART channel were provided among castellated pads and bottom layer pads. Due to interface links distribution among the selected pins, not all the channels will be available at the same time, but this is indeed an important result that allows for maximum flexibility in a four layer design. A comprehensive map of the communication peripherals pins was also documented in the schematic, as shown in figure 5.12.



Communication Peripherals Mapping

```
SPI1:     PA1 PA11 PA12 PA15 or
          PB0 PB3 PB4 PB5
SPI2:     PB9 PB10 PC2 PC3
SPI3:     PC10 PC11 PC12 PA4
UART4:    PC10(tx) PC11(rx)
USART1:   PB6(tx) PB7(rx)
USART3:   PC4*/PA7*/PB10(tx) PC5*(rx)
USART5:   PC12*(tx) PD2*(rx)
I2C1:     PB9/PB3(sda) PB8(scl)
I2C2:     PB13(sda) PB14(scl)
I2C3:     PB4(sda) PA7*(scl)
I2C4:     PB6(sda) PB7/PB10(scl)
LPUART1:  PC1*(tx) PC0*(rx)

*LGA pad
```

Figure 5.12: Final result of STM32U545 peripherals mapping

5.3.2 Passive Components

As in the nRf9160 schematic design process, it is now necessary to address passive components requirements for the STM32U545.

Reset network

The schematic closely follows datasheet's directions, starting from the reset network as in figure 5.13.

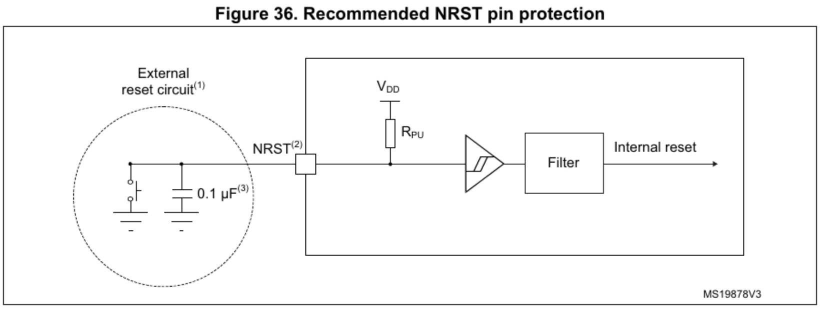


Figure 36. Recommended NRST pin protection

Figure 5.13: Recommended reset network in the SMT32U545

Besides the recommended 100nF capacitor, a TVS diode was included in order to protect the line against ESD transients. Also, since the internal pull-up resistor value is not specified, a additional pull-up resistor is placed to ensure the known state of the reset pin and a reduced rise time in case the internal pull-up resistor is too high for the intended application. If, otherwise, the internal resistor happens to be suitable for a given application, the external one can get removed without consequences on the overall functionality.

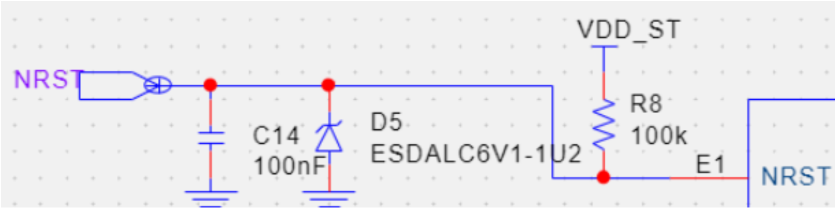


Figure 5.14: Implemented reset network in the STM32U545 design

Supply capacitors

As usual, the STM32U545 datasheet describes in detail all the external components minimum requirements. In particular required supply capacitors are depicted in figure 5.15, where unused pins and the related capacitors have been crossed out according to the chosen part number, which is again the STM32U545REI6 in the package BGA 5x5mm.

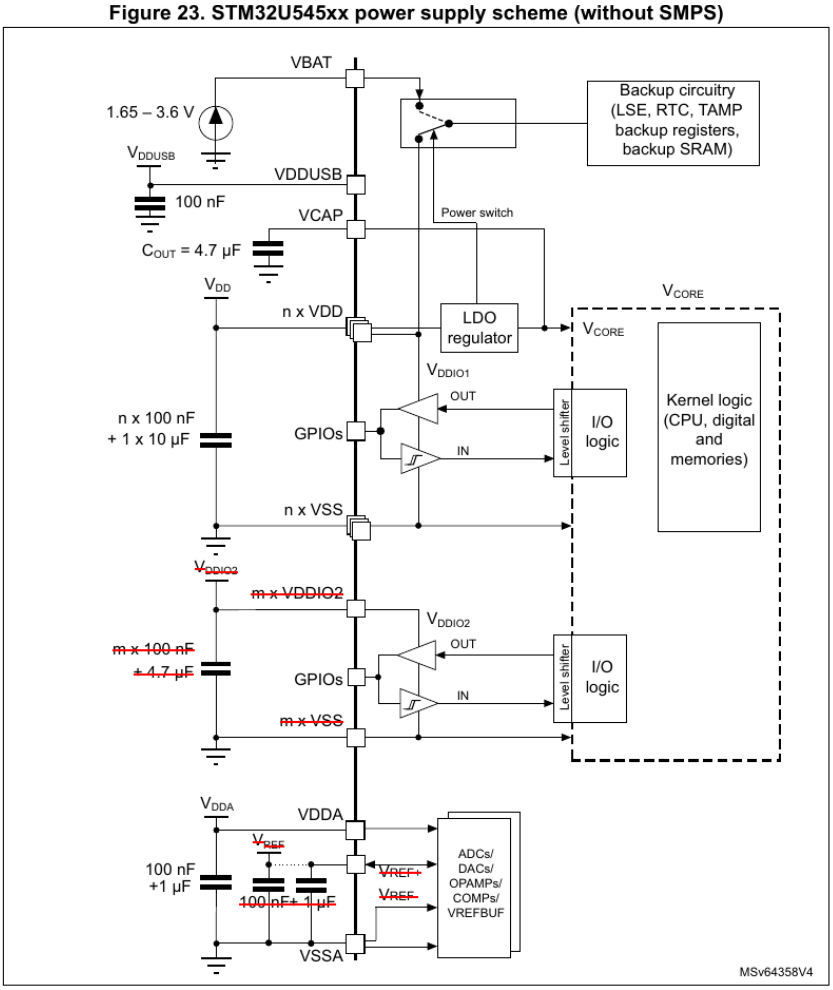


Figure 5.15: Power supply scheme with required capacitors values

The schematic design in figure 5.16 has been hence implemented according to the datasheet scheme, with the only differences that V_{DDUSB} is connected directly to V_{DD} since the USB transceiver does not require a separate supply in this design, and that VCAP capacitor is not implemented as the LDO output will not be needed.

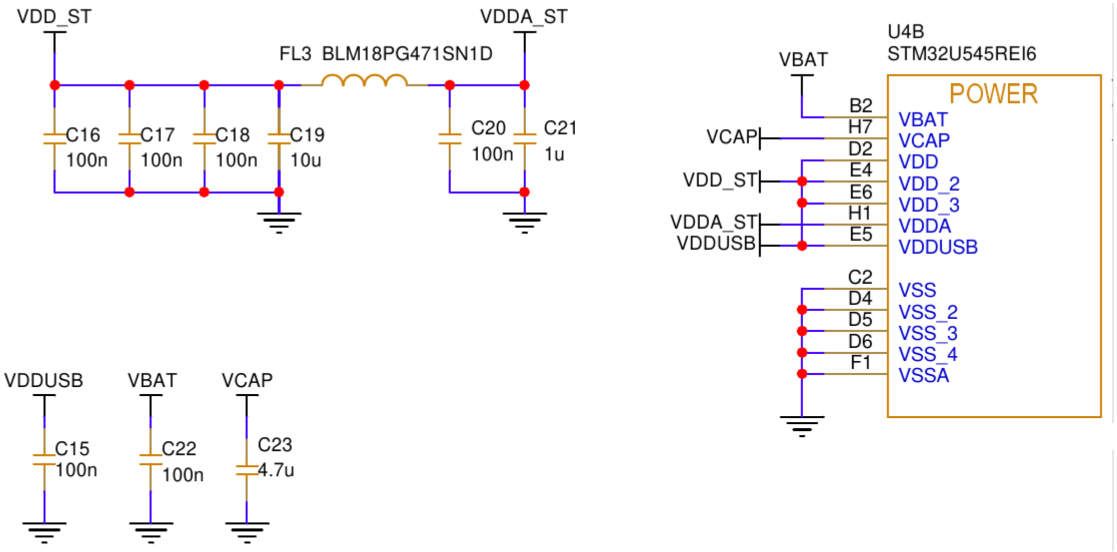


Figure 5.16: Capacitors on the STM32U545 power supply interface

A ferrite bead is also employed to filter noise from the main power supply line VDD_{ST} to the dedicated analog power supply $VDDA_{ST}$ used as voltage reference by the chip's ADC. The ferrite part number is taken from the MBC-LR design, as it is already available and functioning for the same purpose.

Chapter 6

MBC-NB Layout

6.1 Briki MBC form factor

The Briki standardized form factor offers a compact, modular design that facilitates rapid prototyping and transition to production without any hardware changes in the base module. This format supports compatibility across various modules, making it ideal for IoT and professional applications. By maintaining consistent pinouts and geometries, Briki ensures seamless integration with different host boards featuring sensors or communication chips. The standard's flexibility allows developers to easily scale projects, swap components, or adapt configurations based on specific requirements. Additionally, Briki modules come pre-certified for regulatory compliance, streamlining the product development cycle for the European and American markets and reducing greatly certifications costs for the final applications.

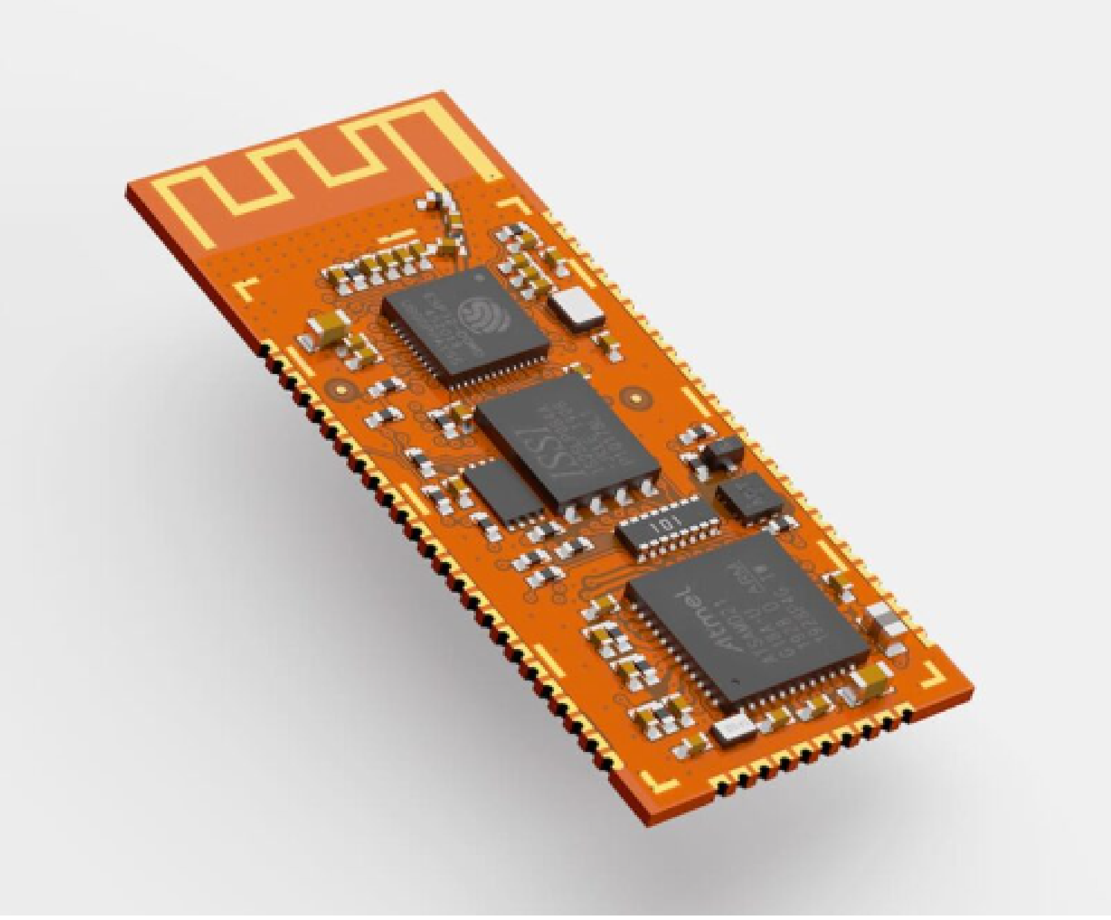


Figure 6.1: Briki MBC-WB

Moreover the Briki family pays a great deal of attention to signal integrity and EMI compliance by carefully designing the PCB. Analog and digital signals are carefully routed in different layers and areas on the PCB for avoiding cross-talk and ensuring clean signal transmission. Supply lines are handled by dedicated power layers, while strategically located ground pins between the major signal groups further help mitigate interference. RF networks are granted their own isolated area on the board to avoid any interference to and from other components. This is a considerate layout that increases the reliability and performance of the modules of Briki, hence making them ideal for applications of high precision in various environments.

6.1.1 Castellated pads

Briki modules feature castellated pads on their edges. Castellated pads are half-plated holes along the edges of a PCB that are normally used for interconnections between more than one board or module. They can also be very useful in surface mount applications where one might attach RF modules or other components on a host PCB. Their most important advantages are that they provide good solder connection and can easily be inspected, while testing the joint. Additionally, they offer more routing flexibility because they can be routed to any layer of the board and their use allows designers to adapt to most routing requirements while sustaining a compact and efficient design.

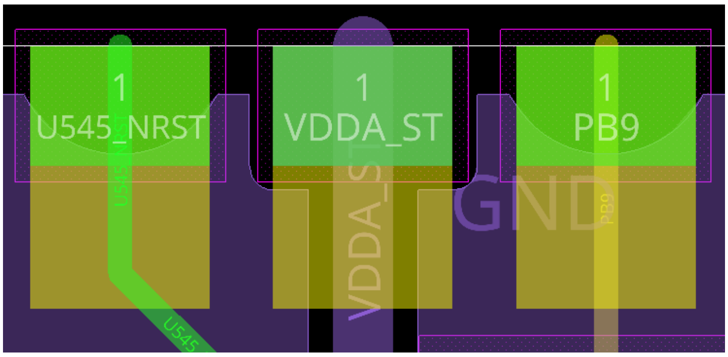


Figure 6.2: Castellated pads can be routed to any layer

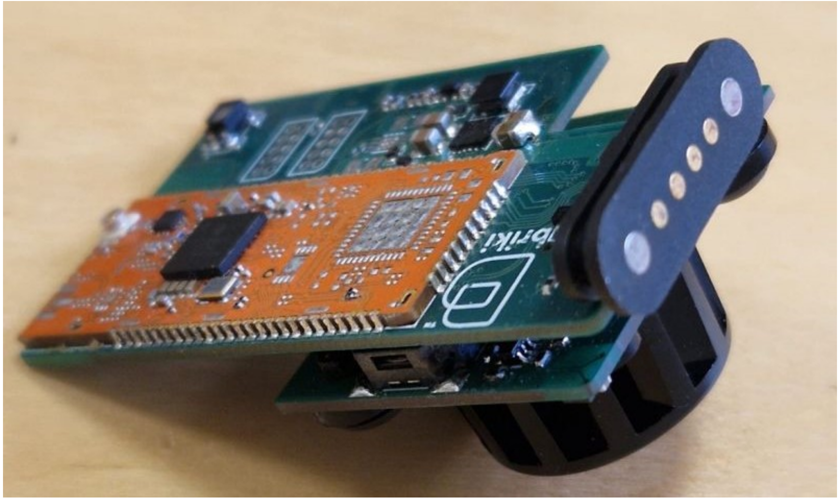
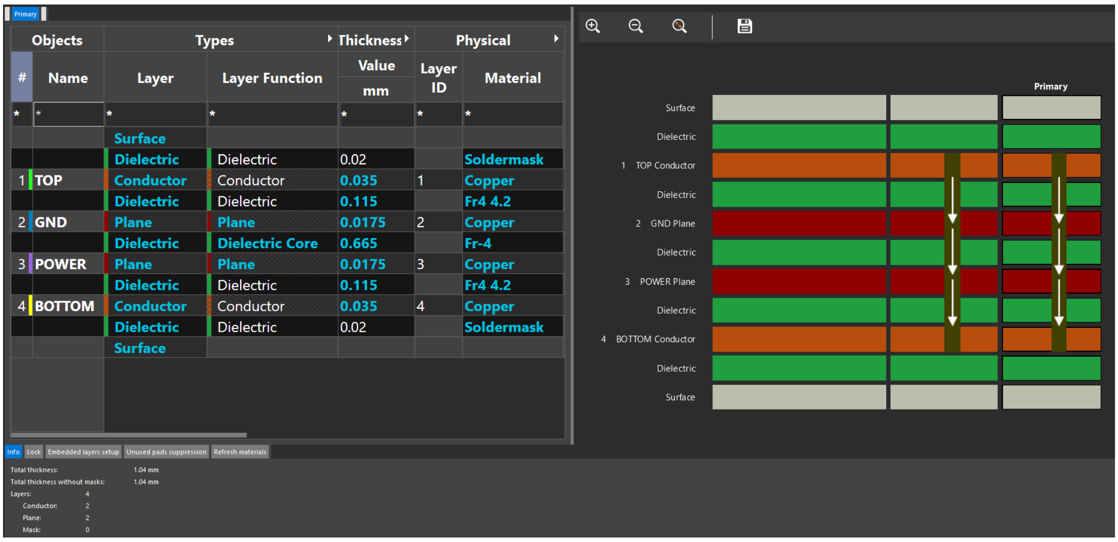


Figure 6.3: Castellated pads allow Briki modules to be mounted on specifically designed application boards

6.2 Stackup

The chosen stackup is the JLC3313, one of the controlled impedance stackups offered by JLCPCB, which is supported by multiple manufacturers. The JLC3313 is a type of prepreg material commonly used in PCB stackups that require controlled impedance. In fact the dielectric constant of the PCB will depend on the prepreg (short for "pre-impregnated"). In such designs, it is critical to manage signal integrity, particularly for high-frequency signals like USB, or RF. The JLC3313 stackup features specific dielectric properties and thicknesses, which contribute to controlling the impedance of signal traces. For instance, in configurations like microstrip or coplanar waveguides, the prepreg's dielectric constant (typically around 4.1) and its thickness help achieve the desired impedance, often set at 50Ω.



Objects		Types		Thickness	Physical	
#	Name	Layer	Layer Function	Value mm	Layer ID	Material
*	*	*	*	*	*	*
		Surface				
		Dielectric	Dielectric	0.02		Soldermask
1	TOP	Conductor	Conductor	0.035	1	Copper
		Dielectric	Dielectric	0.115		Fr4 4.2
2	GND	Plane	Plane	0.0175	2	Copper
		Dielectric	Dielectric Core	0.665		Fr-4
3	POWER	Plane	Plane	0.0175	3	Copper
		Dielectric	Dielectric	0.115		Fr4 4.2
4	BOTTOM	Conductor	Conductor	0.035	4	Copper
		Dielectric	Dielectric	0.02		Soldermask
		Surface				

Total thickness: 1.04 mm
Total thickness without masks: 1.04 mm
Layers: 4
Conductor: 2
Plane: 2
Mask: 0

Figure 6.4: MBC-NB 4 layers 1.04mm stackup

6.3 Layout Design

In this PCB design several strategies are implemented to ensure robust performance and reliable operation across all the board.

6.3.1 Component placing

Placement of components is the first stage in the design cycle of a PCB and, for that matter, should be handled as meticulously as possible before routing the traces. Good placement plays a key role, not only in the physical layout but also in maintaining signal integrity, thermal management, and overall performance. By strategically placing components at the beginning, the designer ensures appropriate separation between analog, digital, and RF signal paths to reduce noise and interference. Careful attention to component placement from the start simplifies routing and helps achieve efficient, functional PCB layouts.

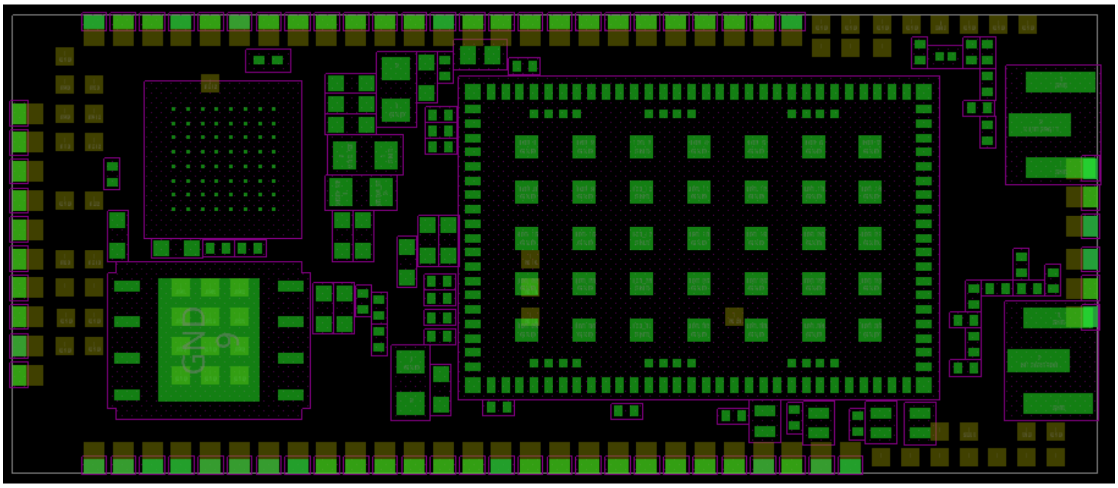


Figure 6.5: Top-left: STM32U545, Bottom-left: eSIM, Right: nRF9160

It is important to fix the position of big footprints at the beginning, in order to avoid complicated re-routing further in the design. The big nRF9160 footprint left little space to other components on the sides, so most of them had to be placed between the two chips. Also the eSIM has a relatively big footprint, but it is however mostly ground, so some LGA pads could be placed on the bottom plane under it. In general, since LGA pads are not part of the Briki standard, they got placed after routing the most important traces, where space was left.

6.3.2 Routing data traces

In PCB layout design, adhering to best practices is crucial for ensuring signal integrity, reducing noise, and optimizing performance. Key practices include separating PCB areas to isolate analog, digital, and RF signals, and external pin separation with ground pins to minimize interference between signal types. A dedicated ground plane provides a stable reference and reduces noise across different layers, while a dedicated power plane ensures clean power delivery across the board. For routing, orthogonal trace crossing between different layers prevents signal coupling, especially when no ground plane is present, like between bottom and power plane in the case of a 4 layer PCB. Additionally, using differential pairs for high-frequency communication traces, such as USB, helps maintain signal integrity and reduce EMI in high-speed data transmission. Follows some examples were these design practices are implemented.

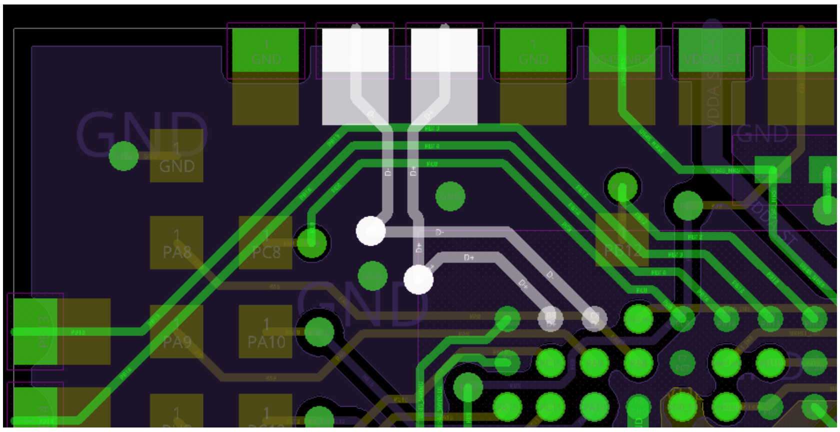


Figure 6.6: USB communication differential pair routed with diagonal via pattern

Designing differential pair traces requires precise routing in order to maintain signal integrity, especially for high-speed interfaces such as USB. In the design presented here, differential pairs are routed with equal length and consistent spacing to provide matched signal timing with minimal noise. OrCAD has automated tools for routing differential pairs, with controlled impedance and trace length to prevent timing skew between the two paired signals. In this case, a diagonal via pattern was also necessary to route the traces according to the Briki standard pins, since D+ and D- USB pins positions are reversed with respect to those of the standard. So a diagonal via pattern was exploited to cross them while keeping the differential pair characteristics.

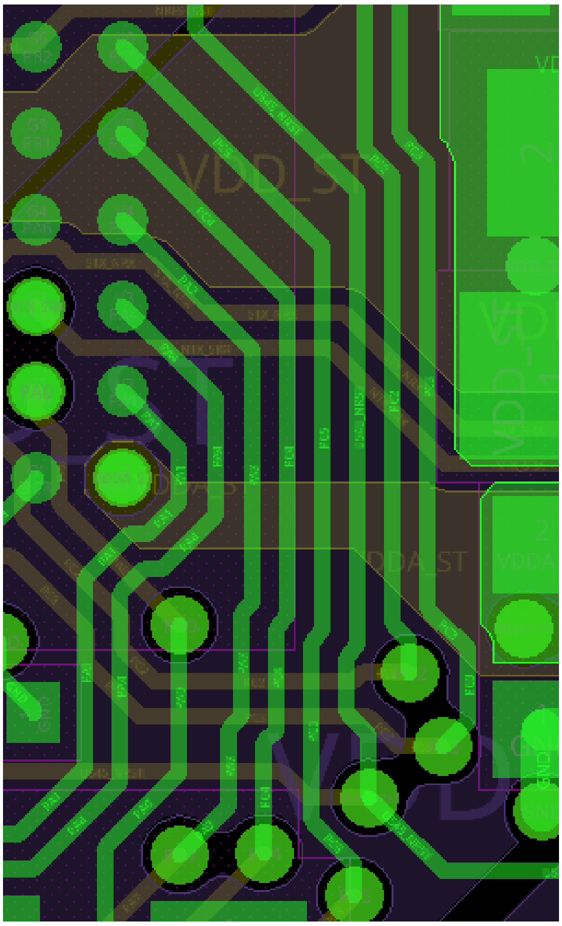
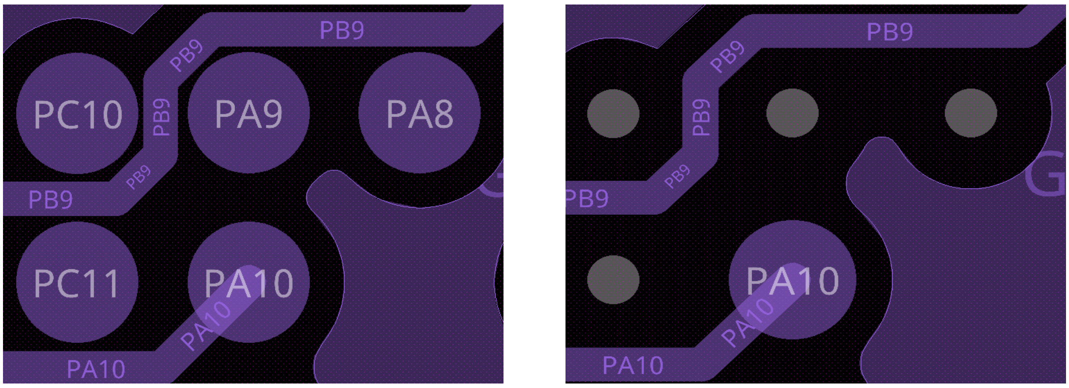


Figure 6.7: Grid of parallel traces in top and bottom layers

To route a connection dense chip like the STM32U545 in 5x5mm BGA package specific approaches are necessary for maintaining signal integrity and minimizing interference. In particular one key practice is ensuring that all traces on a given layer are parallel to each other, while the traces on an adjacent layer are routed perpendicularly, as in figure 6.7, with the aim to avoid parallel traces among different layers. This orthogonal routing pattern helps reduce electromagnetic coupling between layers, especially if there is no ground plane between them to act as a reference. It also makes easier routing traces that are very close to each other, as they all follow the same pattern. Without this approach, parallel traces on different layers can induce crosstalk and degrade performance, making orthogonal routing an effective technique to minimize unwanted signal interactions.

Another option to route dense BGA pins, while meeting manufacturer clearance standards, is to suppress unused via pads. These pads are automatically included on every layer each time a via is placed, but often they are not used on at least one layer, since the via is usually intended to connect one layer to another. After routing the BGA pins both on the top and the bottom layer, the power layer was used where possible as an additional option to route even more STM32 pins, allowing for more communication protocols to be routed externally. In figures **??** it can be seen that most of the vias are not routed on the power layer (purple), so they could be removed, allowing for more central BGA pins to be routed outside the chip, like PA10, which would otherwise be blocked behind other vias. Also in figure 6.9 it can be seen that PB5 and PB7 could be routed outside since PH3 and PB8 were routed on the bottom layer (yellow), leaving their power layer via pads available for suppression.



(a) Here the DRC reports several errors on "Line to Via spacing"

(b) By suppressing unrouted via pads the design meets the 0.1mm clearance requirement

Figure 6.9: Suppressing unused pads allows routing between BGA pins

Signal integrity analysis

In such a dense design some traces had to be routed less optimally. Figure 6.10 shows two traces routed one in the bottom layer and the other in the power layer (since it's an area outside of the main power channels) that run in parallel very close to each other. This can be problematic when they are used together as I2C or USART communication lines, so this aspect will have to be tested in a dedicated setup and the design updated if necessary.

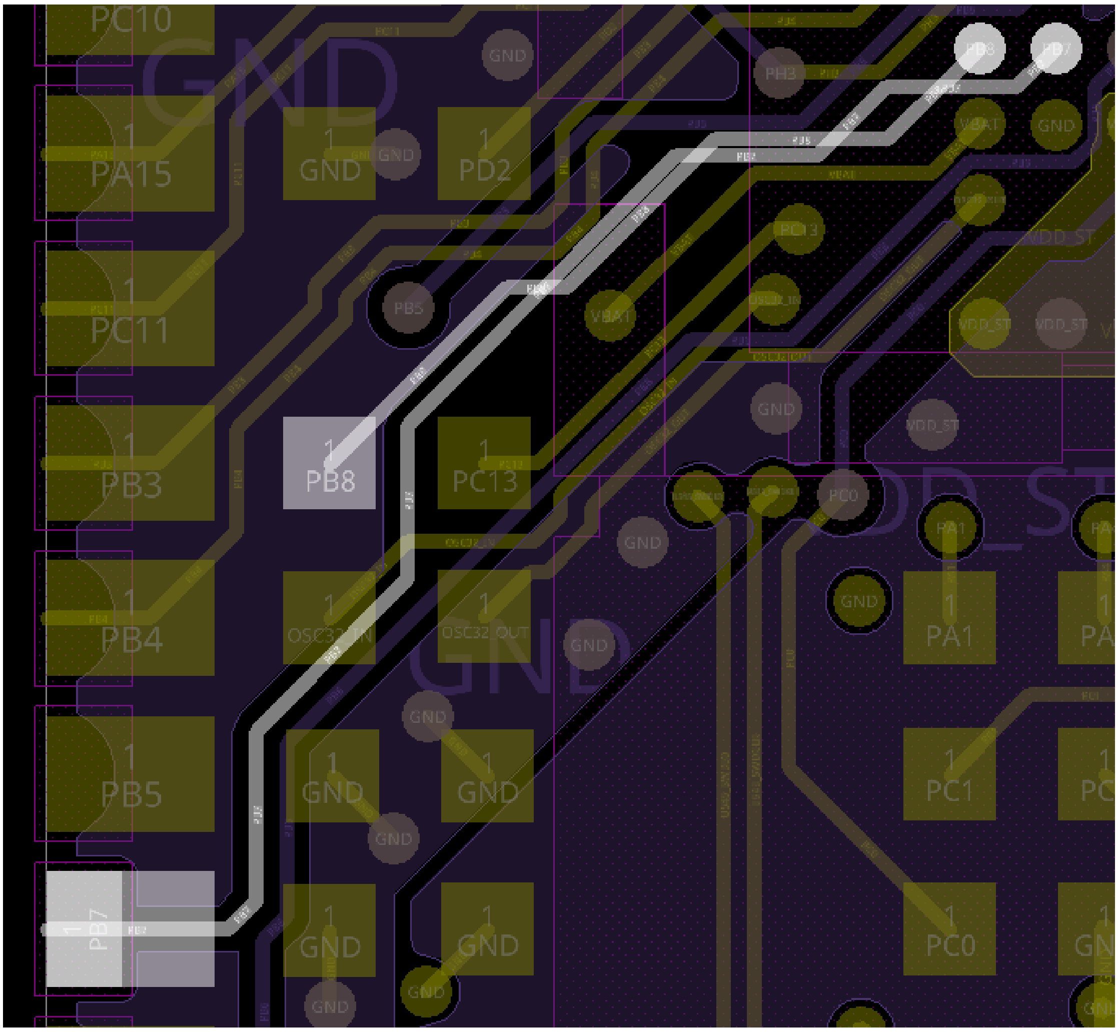


Figure 6.10: Potential crosstalk between two parallel lines running on the power and bottom layer

The impedance analysis in figure 6.11 also shows that those lines have higher impedance due to the absence of a ground layer reference near the traces. The further the reference layer (highlighted by the dotted line), the higher the impedance of the trace is. It only gets lower in spots that run over the ground layer. The minimal distance between the traces and the high impedance will surely cause crosstalk among signals in that area, especially if communication protocols are implemented. Also the impedance discontinuities in the PB8 line will cause voltage reflections that might even make the trace radiate power from those spots. This effect is noticeable at high frequencies, so if communication protocols like I2C or UART (like indicated in figure 5.12) are going to be implemented in those lines, it will be best to make the necessary testing first, to assess the entity of signal disturbances. In the case that crosstalk or radiations will result to influence too much the signal quality, it will be necessary to make design adjustments, like rerouting those lines or increasing the PCB layers to add a reference ground layer between power and bottom layers, so to ensure that every layer has its dedicated ground reference.

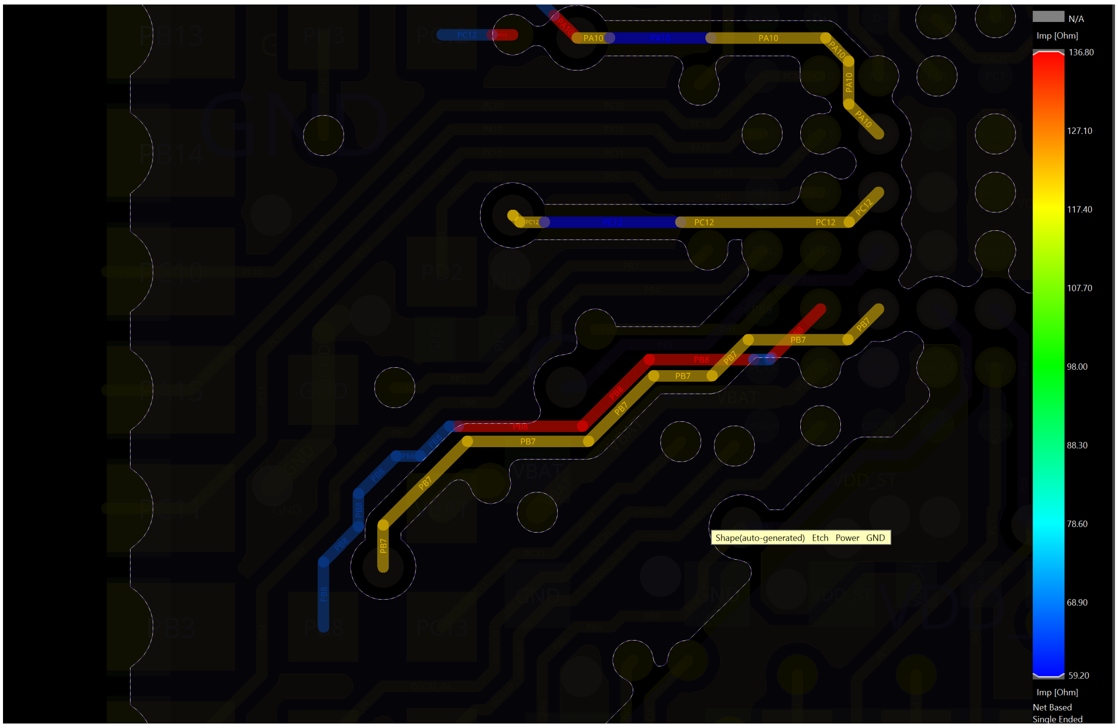


Figure 6.11: Impedance analysis

Increasing the number of layers to have an additional ground reference layer might be useful also to improve signal integrity in spots were signal traces run over layer discontinuities, like shown in the highlighed parts in figure 6.12. Especially for serial communication lines, like the ones highlighted in the lower half of the image, it is important to always guarantee a return path for the current flowing in the traces. A big discontinuity in the path, like shown in the image, causes return currents to seek for alternative paths, so additional stitching vias might have helped to gather those currents to the ground layer. Unfortunately the available area was very limited to implement this solution. An alternative approach to prevent this kind of problems is to reroute potentially disturbed traces together with other data traces that already have a reference ground layer. This shows also that choosing the shortest path is not always the best choice to route signal traces.

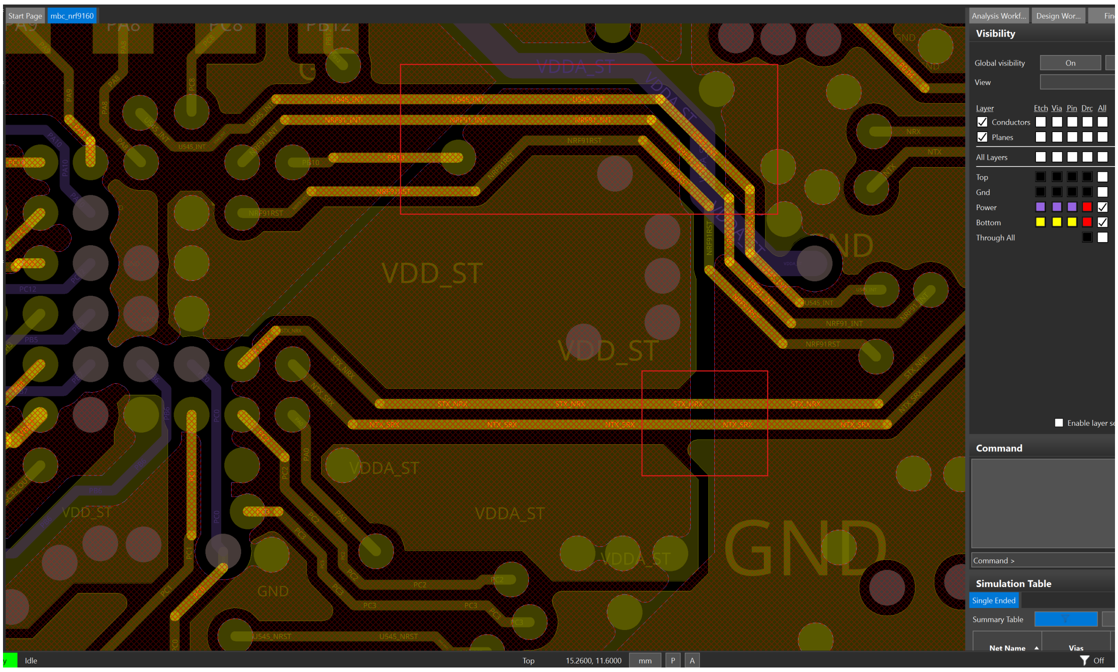


Figure 6.12: Some data communication lines are missing ground plane reference in layer discontinuity spots

6.3.3 Routing power traces

The power network in the MBC-NB brings the required current from the connectors in the bottom left of the board to the supply pins of the two chips. Most of the power traces in this design are implemented as polygonal areas so to increase as much as possible the area of the current channel, effectively decreasing trace impedance and rises in temperature. The required width of the trace can be estimated with the formulas 6.1 provided by the standard IPC-2221

$$A = \left(\frac{I}{k \cdot T_{rise}^{b}} \right)^{\frac{1}{c}} \qquad W = \frac{A}{t \cdot 1.378} \tag{6.1}$$

with $b = 0.44$, $c = 0.725$ and $k = 0.024$ for internal layers, $k = 0.048$ for external layers. Just from the constant values it can be seen that traces in the internal layer must be wider than in the external ones to allow the same heat dissipation. The evaluation was conducted in Saturn PCB Toolkit. It was assumed a ambient temperature of $25°C$, a allowed rise in temperature $T_{rise} = 10°C$ and a copper thickness of $1oz$ for external layers and $0.5oz$ for internal ones. The STM32U545 draws less than $10mA$ in its Run Mode at the maximum clock frequency, so the minimum trace width in this case is negligible. The nRF9160 instead has a maximum current absorption of $500mA$ when the modem is transmitting at full power, so it is important to evaluate the minimum trace width during the design process. So with $I = 500mA$ and the previous assumed values, the minimum trace width resulted to be $0.584mm$ for a internal layer and $0.150mm$ for a external layer. In figure 6.13 are shown the trace areas in the internal power layer that supply the two chips and the GPS antenna, from the bottom left connectors to the top right RF network. The nRF9160 VDD area is much wider than the required minimum width for thermal management, at around $3mm$ in its narrowest point. This also helps against possible brownouts.

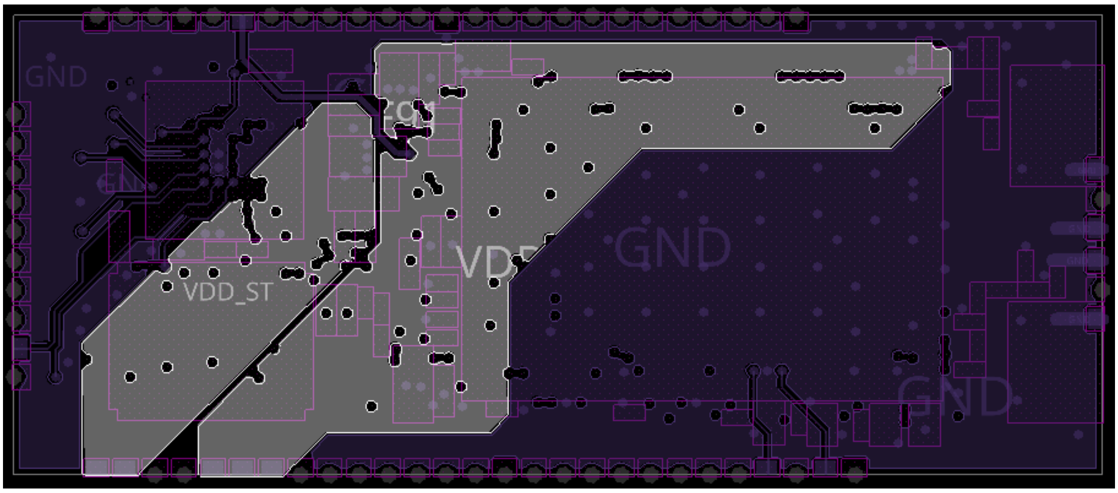


Figure 6.13: Supply areas in the power layer

These areas are then connected through multiple vias to supply bulk capacitors near the two chips supply pin, where other copper areas were designed in the top and bottom layer to allow more current to flow. In figure 6.14 a bulk and a decoupling capacitor are placed very close to one of the VDD pins of the nRF9160.

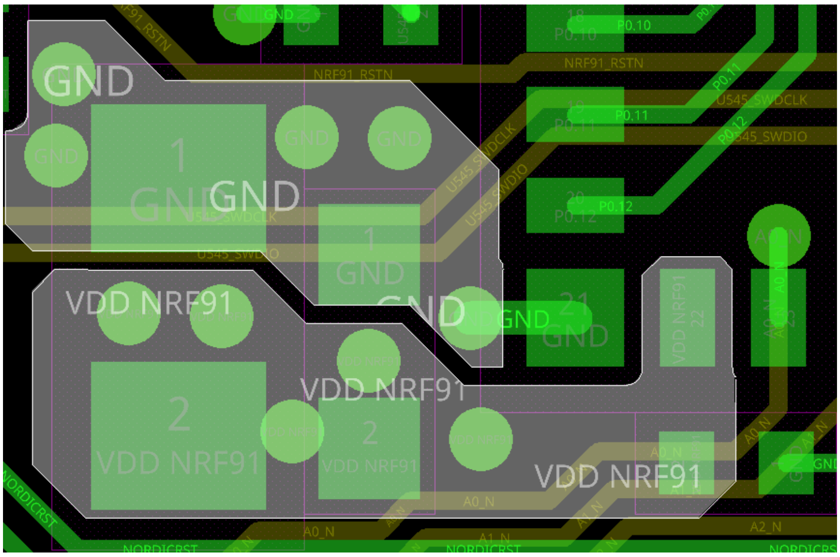


Figure 6.14: Dedicated areas for supply and ground lines for power components

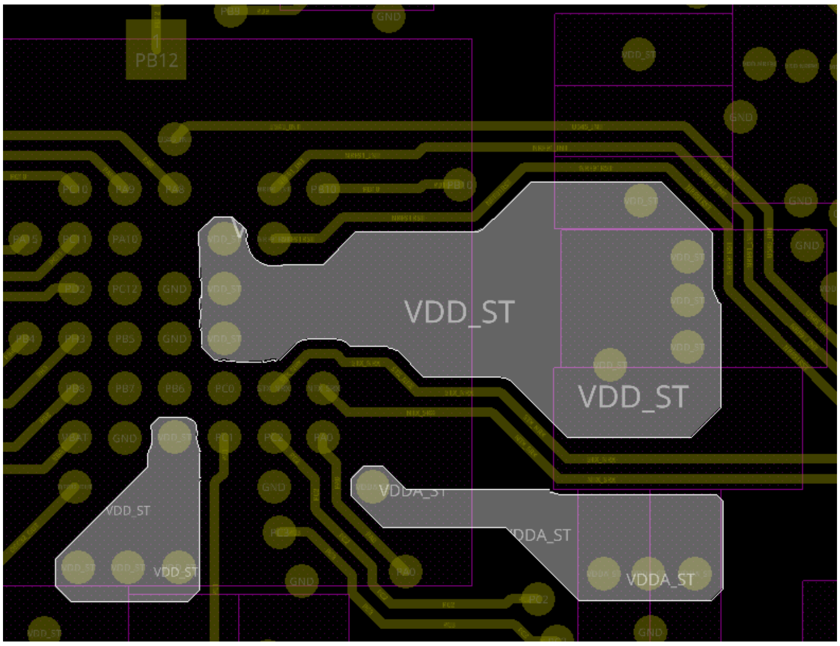


Figure 6.15: Multiple vias on power supply areas

Using multiple vias to connect power supply areas across different layers is important for distributing current more evenly across the channel, which helps prevent overheating and reduces voltage drop occurrences. This design approach enhances the overall current-carrying capacity of the power distribution network by providing multiple paths for current flow, effectively lowering the impedance and ensuring stable power delivery to the related components. In image 6.15 the supply traces of the STM32U545 are showed, getting power from supply bulk capacitors near the chip.

6.4 Electromagnetic compatibility considerations

Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC) are critical factors to consider when designing medium-density PCBs, especially with mixed signal environments that include both analog and digital components. Ignoring EMI/EMC issues can lead to signal disturbances, interference, and cross-talk, which can degrade performance, cause data errors, and even result in complete system failure. In mixed-signal designs, improper layout or routing can allow high-frequency signals to interfere with sensitive analog signals, causing a high noise floor. Too much noise on analog signals deteriorates the information as the Effective Number of Bits is lower than expected. Common strategies to mitigate these risks include careful PCB layout design, such as maintaining proper spacing between signal traces, implementing ground planes, using shielding, and employing filtering components like ferrite beads and decoupling capacitors to suppress noise. Implementing these measures early in the design process helps ensure the board's reliable operation and compliance with EMI/EMC standards.

Especially RF network design requires careful consideration to ensure signals work properly and without interference. Common strategies include impedance matching, using proper ground planes, and carefully routing RF traces to minimize losses and signal reflection. Shielding and the use of low-noise components are also essential to prevent signal degradation.

One specific technique used in the RF design is the implementation of coplanar waveguides. Unlike simple microstrips, which consist of a single conductor trace over a ground plane, coplanar waveguides feature ground planes placed both below and alongside the signal trace. This configuration improves signal isolation, reduces crosstalk, and provides better control of the trace's impedance. Additionally, coplanar waveguides allow for tighter coupling of the signal to the ground, which is particularly useful for higher-frequency signals. This design leads to improved performance in RF circuits, as it helps maintain signal integrity and reduces losses, making it superior to traditional microstrip designs in many applications. This is demonstrated in the simulation results below, conducted with the RF Toolbox in Matlab. A sample line with the following characteristics has been considered for demonstration purposes: $Length = 3mm$, $Width = 0.188mm$, $GroundPlaneWidth = 3mm$, $Height = 0.115mm$ where Length, Width and Height have the same values of the RF network traces in the MBC-NB PCB design. The frequency of the simulated signal is $1227.60MHz$ which is one of the frequencies among the main communication channels of GPS.

The currents distribution around a microstrip line is shown in figure 6.16 where the current is mostly confined in the microstrip and slightly leaks in the ground plane around it. From the annotated data point it can be seen that the magnitude of the current distribution at 1.5mm from the microstrip center is around $1.44\frac{A}{m}$

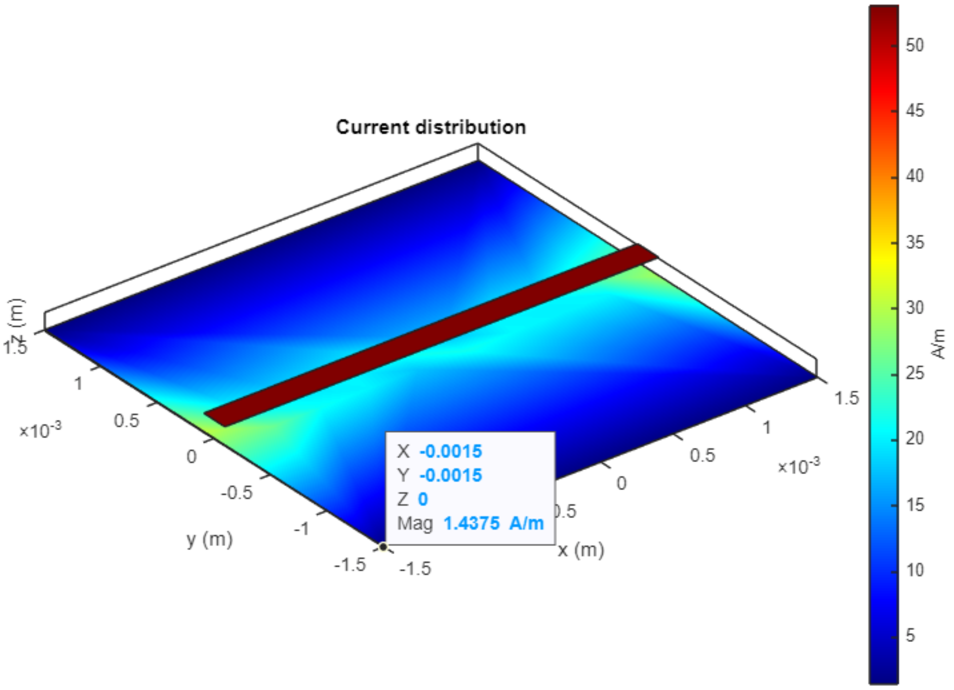


Figure 6.16: Current distribution in a microstrip

In the same conditions a equivalent coplanar waveguide was also simulated, to measure the currents distribution around it. Figure 6.17 shows a coplanar waveguide with vias on the sides, as in the PCB design, which connect the ground plane on the top layer to the reference ground below. The annotated data point at 1.5mm distance from the center of the strip shows that the current distribution magnitude is around $0.08\frac{A}{m}$ which is much less than the value obtained in the microstrip simulation.

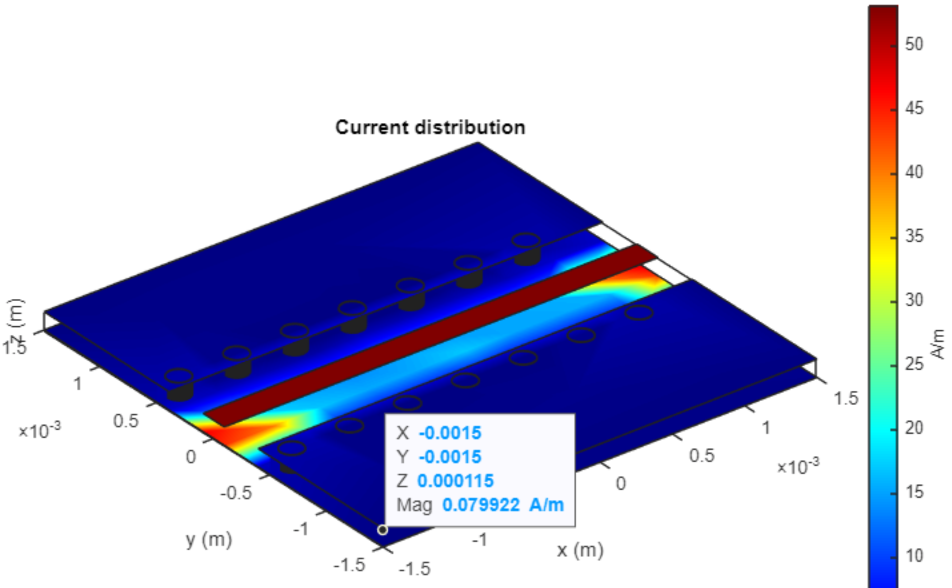


Figure 6.17: Current distribution in a coplanar waveguide

This MATLAB simulation shows that the coplanar waveguide ensures way better signal integrity around the trace with respect to the microstrip, so designs that need tight control over unwanted signal radiations should integrate a coplanar waveguide setup for every RF trace.

As previously said, a very important technique in RF design is via stitching, which involves placing multiple vias around the signal traces to connect different ground planes across PCB layers. This helps to create a continuous, low-impedance path for the return current, reducing potential interference and signal reflection. Via stitching enhances the shielding of RF signals, particularly in designs with coplanar waveguides, by improving the grounding around critical traces. This leads to better signal reliability and less radiations around the trace, especially in high-frequency circuits.

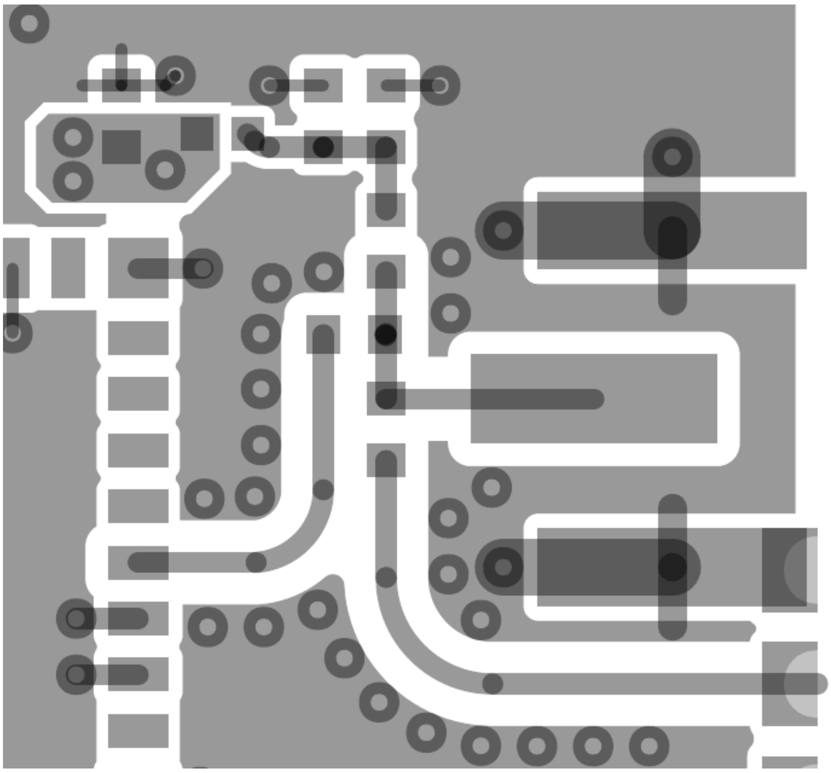
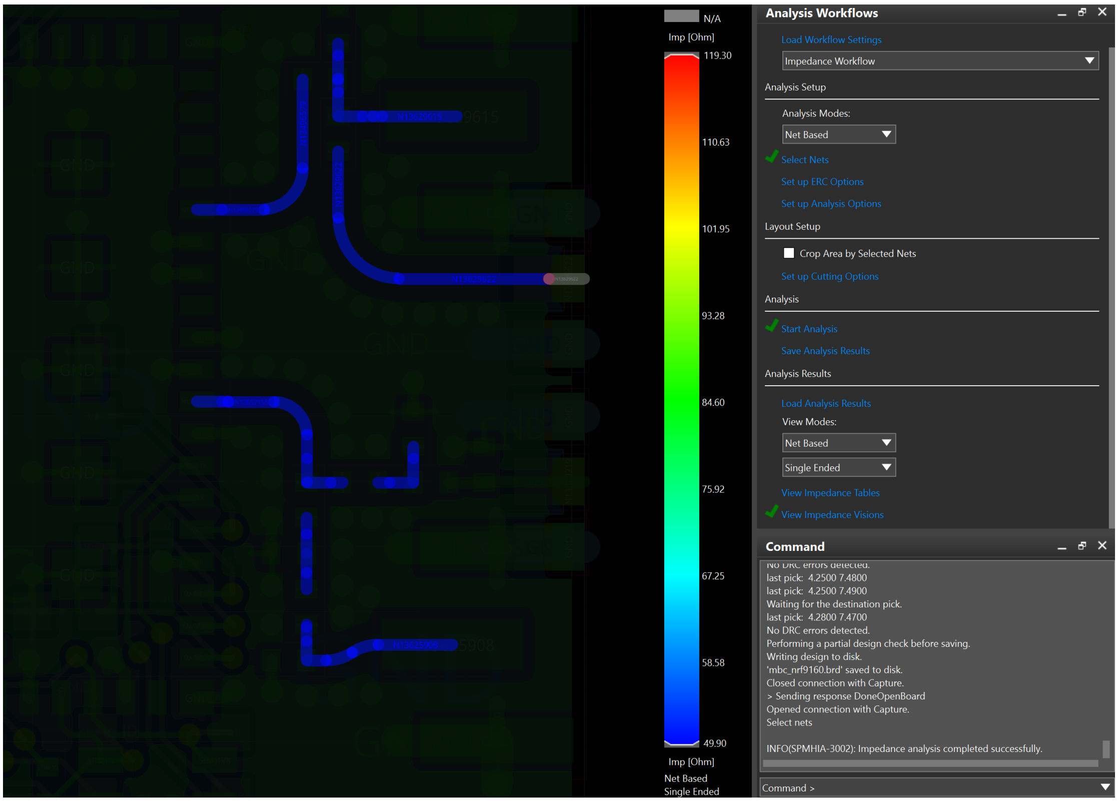


Figure 6.18: All the RF output lines to the antennas are designed as a coplanar waveguide with via stitching

Though via stitching can slightly increase the cost of production due to the added complexity and extra vias, the benefits in terms of signal integrity and noise reduction often outweigh the additional expense. It ensures a more robust design, providing stability in environments where signal reliability is crucial.

6.5 RF Impedance analysis

The image 6.19 from OrCAD PCB shows the RF transmission lines connecting the nRF9160 output respectively to the GPS antenna and the LTE antenna, achieving a stable 50-ohm impedance, a critical parameter for minimizing signal reflections and ensuring efficient signal transmission. The design employs a combination of coplanar waveguide and via stitching, which contribute significantly to this result. The CPW structure, with ground planes flanking the signal trace on the same layer, provides precise impedance control by confining the electromagnetic fields close to the signal path, while the use of via stitching interconnects the ground planes, reducing ground inductance and maintaining a stable reference potential. Together, these techniques create a robust, low-loss transmission environment that ensures the desired impedance profile throughout the RF tracks.



Impedance Workflow

Analysis Modes: Net Based

☐ Crop Area by Selected Nets

View Modes: Net Based, Single Ended

```
No DRC errors detected.
last pick:  4.2500 7.4800
last pick:  4.2500 7.4900
Waiting for the destination pick.
last pick:  4.2800 7.4700
No DRC errors detected.
Performing a partial design check before saving.
Writing design to disk.
'mbc_nrf9160.brd' saved to disk.
Closed connection with Capture.
> Sending response DoneOpenBoard
Opened connection with Capture.
Select nets

INFO(SPMHIA-3002): Impedance analysis completed successfully.
```

Command >

Figure 6.19: Impedance analysis of RF traces

6.6 3D Model

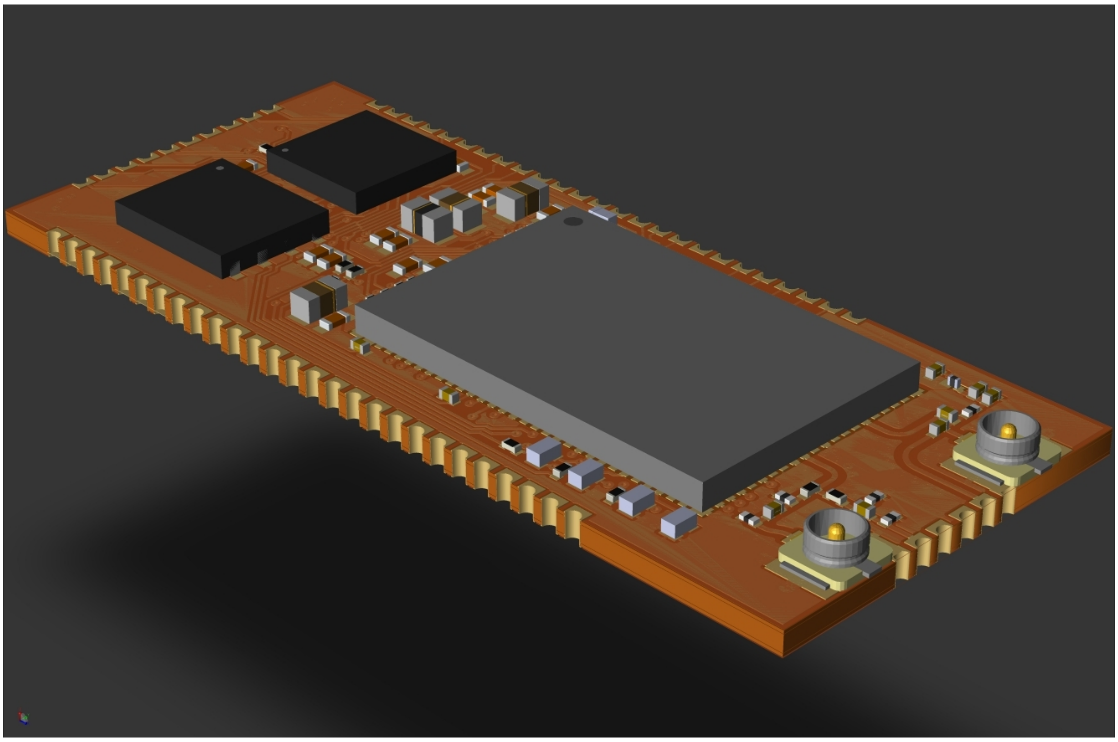


Figure 6.20: Final rendering

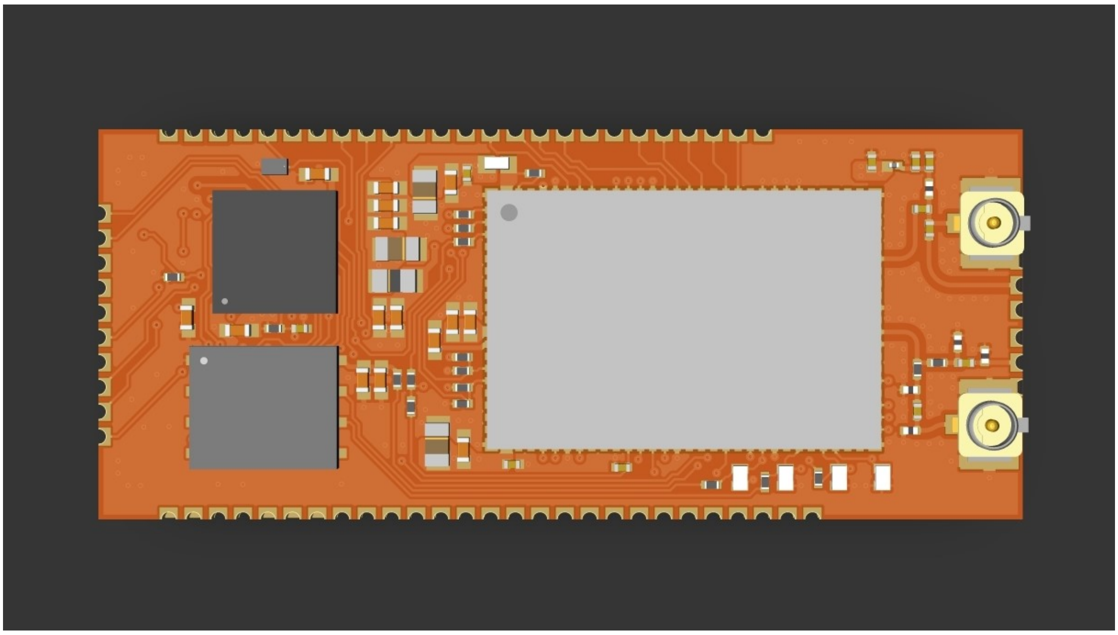


Figure 6.21: Top plane

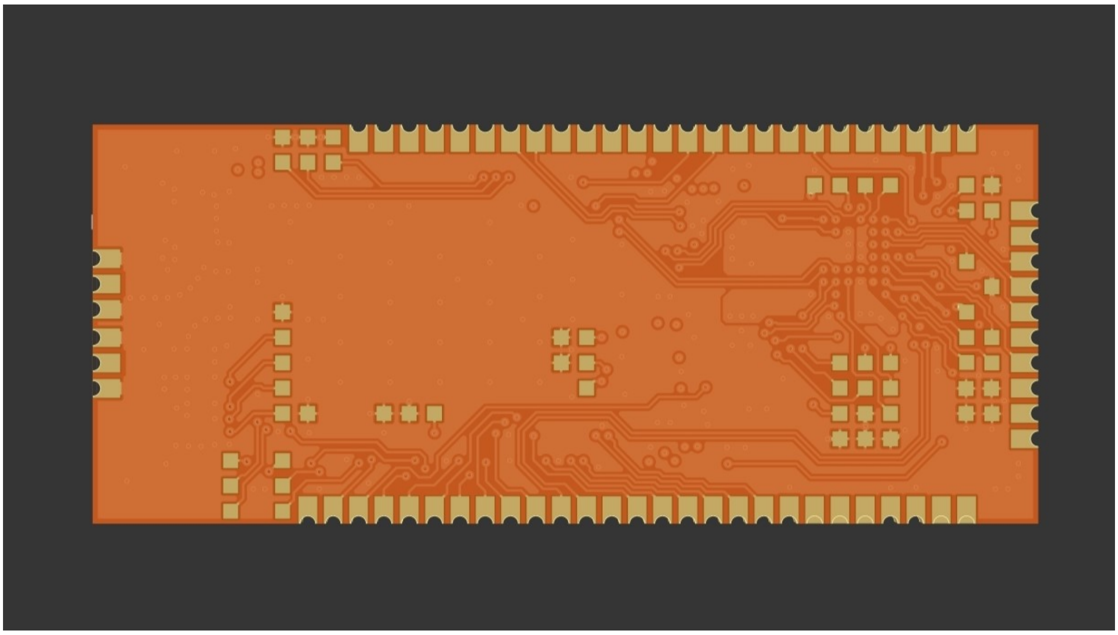


Figure 6.22: Bottom plane

Appendix A

A.1 C code

Listing A.1: Bare metal blink example on nRF9160

```c
// Bare metal nRF9160 DK "Blinky" example
#include "nrfx.h"

int main()
{
    // LED1..4 on the nRF9160 DK are connected to P0.02..P0.05 and
   are active
    // high, so we first configure these pins on P0 as outputs
    NRF_P0->DIRSET |= (1<<5) | (1<<4) | (1<<3) | (1<<2);

    while (1)
    {
        // In the main loop, we make each of the LEDs light up one at
    a time
        for (uint32_t i = 0; i < 4; ++i)
        {
            NRF_P0->OUTSET |= 1<<(i+2);

            // Some delay
            volatile uint32_t j = 1000000;
            while (j > 0)
                --j;

            NRF_P0->OUTCLR |= 1<<(i+2);
        }
    }

    return 0;
}
```

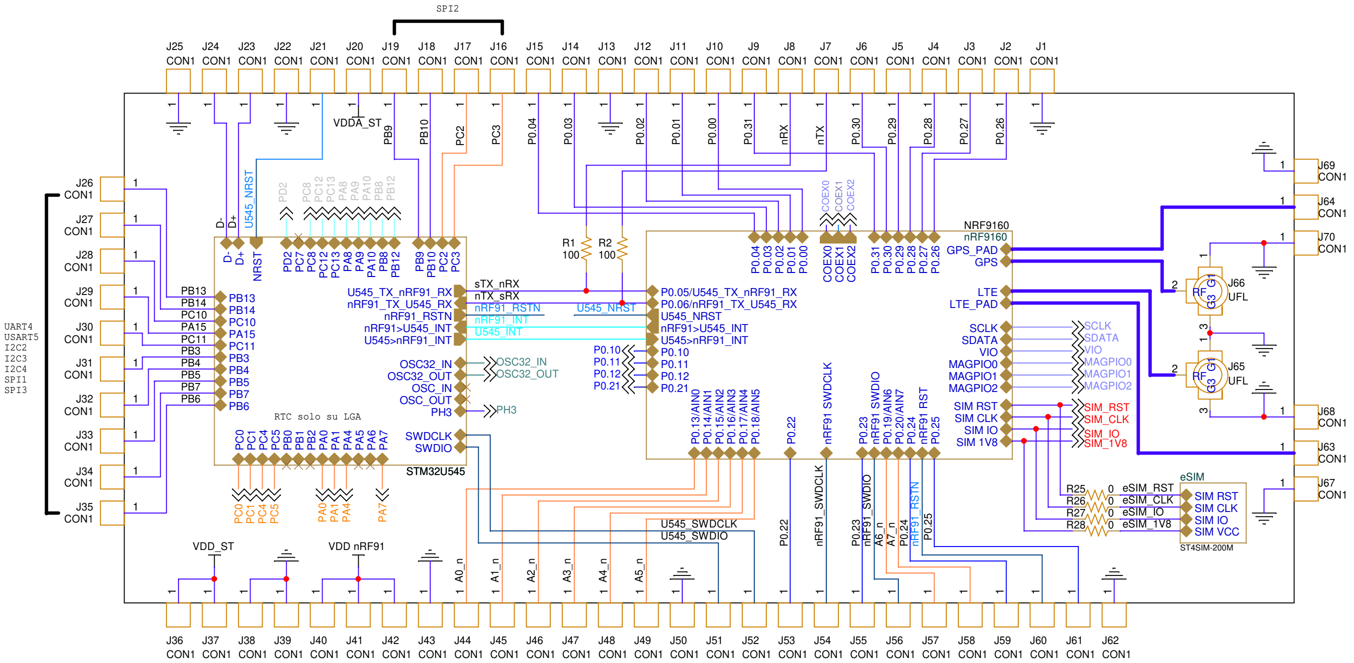
Listing A.2: Matlab RF Toolbox current simulations

```
    clear all

    microstrip = microstripLine(Length=0.003, Width= 0.0001880,
   GroundPlaneWidth= 0.003, Height=0.000115)
    current(microstrip, 1227.60e6)


    waveguide = coplanarWaveguide(Length=0.003, Width= 0.0001880,
   GroundPlaneWidth= 0.0030, Height=0.000115, ViaDiameter=0.00015,
   ViaSpacing=[0.0004 0.001], Spacing=0.0003)
    current(waveguide, 1227.60e6)
   %show(waveguide)
```

A.2 Resources

Here are listed all the tools and resources used in this project:

- Meteca Website
- Orcad X PCB Professional Plus with Academic Program
- Orcad X Capture with Academic Program
- Visual Studio Code
- nRF Connect SDK
- Noise Filter Design Support Tool Plus by Murata
- MATLAB with RF Toolbox
- Saturn PCB Toolkit



Communication Peripherals Mapping

```
SPI1:    PA1 PA11 PA12 PA15 or
         PB0 PB3 PB4 PB5
SPI2:    PB9 PB10 PC2 PC3
SPI3:    PC10 PC11 PC12 PA4
UART4:   PC10(tx) PC11(rx)
USART1:  PB6(tx) PB7(rx)
USART3:  PC4*/PA7*/PB10(tx) PC5*(rx)
USART5:  PC12*(tx) PD2*(rx)
I2C1:    PB9/PB3(sda) PB8(scl)
I2C2:    PB13(sda) PB14(scl)
I2C3:    PB4(sda) PA7*(scl)
I2C4:    PB6(sda) PB7/PB10(scl)
LPUART1: PC1*(tx) PC0*(rx)

*LGA pad
```

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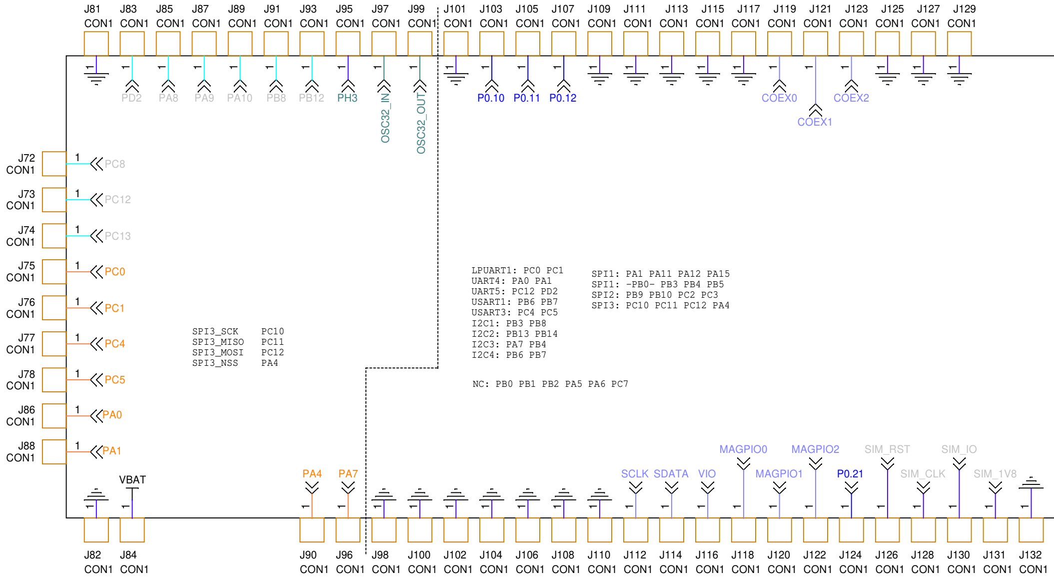
Project

MBC-NB

Size Custom	Schematic Version 1.0	pag.1 - BOARD	Rev 1.0
Date:	Thursday, September 12, 2024	Sheet 1 of 1	



SPI3_SCK	PC10
SPI3_MISO	PC11
SPI3_MOSI	PC12
SPI3_NSS	PA4

LPUART1: PC0 PC1
UART4: PA0 PA1
UART5: PC12 PD2
USART1: PB6 PB7
USART3: PC4 PC5
I2C1: PB3 PB8
I2C2: PB13 PB14
I2C3: PA7 PB4
I2C4: PB6 PB7

SPI1: PA1 PA11 PA12 PA15
SPI1: -PB0- PB3 PB4 PB5
SPI2: PB9 PB10 PC2 PC3
SPI3: PC10 PC11 PC12 PA4

NC: PB0 PB1 PB2 PA5 PA6 PC7

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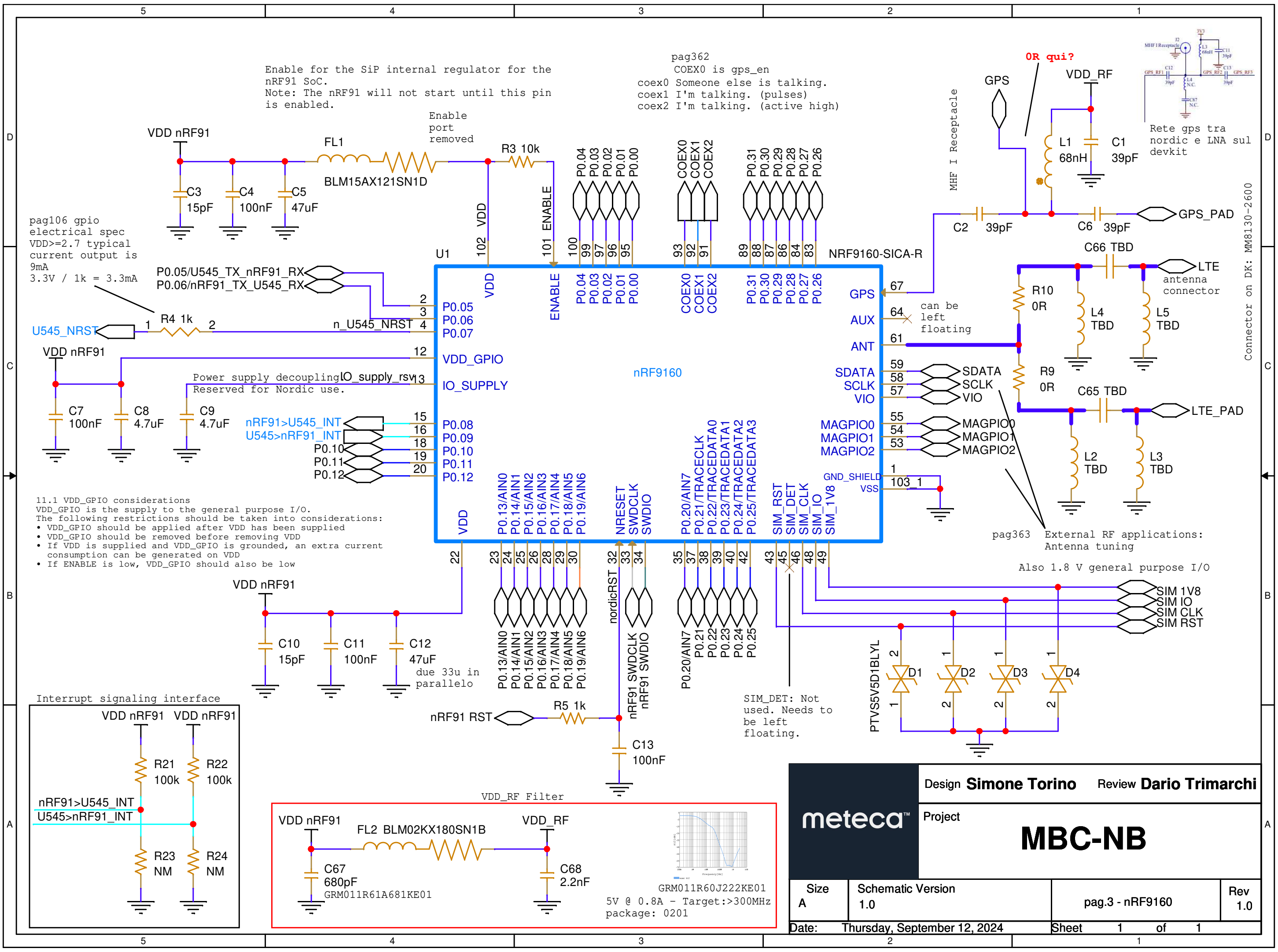
Project

MBC-NB

Size Custom	Schematic Version 1.0	pag.2 - BOARD LGA	Rev 1.0
Date:	Thursday, September 12, 2024	Sheet 1 of 1	



Enable for the SiP internal regulator for the nRF91 SoC.
Note: The nRF91 will not start until this pin is enabled.

Enable port removed

pag362
COEX0 is gps_en
coex0 Someone else is talking.
coex1 I'm talking. (pulses)
coex2 I'm talking. (active high)

pag106 gpio electrical spec
VDD>=2.7 typical current output is 9mA
3.3V / 1k = 3.3mA

Power supply decoupling
Reserved for Nordic use.

can be left floating

Rete gps tra nordic e LNA sul devkit

antenna connector

pag363 External RF applications:
Antenna tuning

Also 1.8 V general purpose I/O

11.1 VDD_GPIO considerations
VDD_GPIO is the supply to the general purpose I/O.
The following restrictions should be taken into considerations:

- VDD_GPIO should be applied after VDD has been supplied
- VDD_GPIO should be removed before removing VDD
- If VDD is supplied and VDD_GPIO is grounded, an extra current consumption can be generated on VDD
- If ENABLE is low, VDD_GPIO should also be low

due 33u in parallelo

SIM_DET: Not used. Needs to be left floating.

Interrupt signaling interface

VDD_RF Filter

GRM011R60J222KE01
5V @ 0.8A - Target:>300MHz
package: 0201

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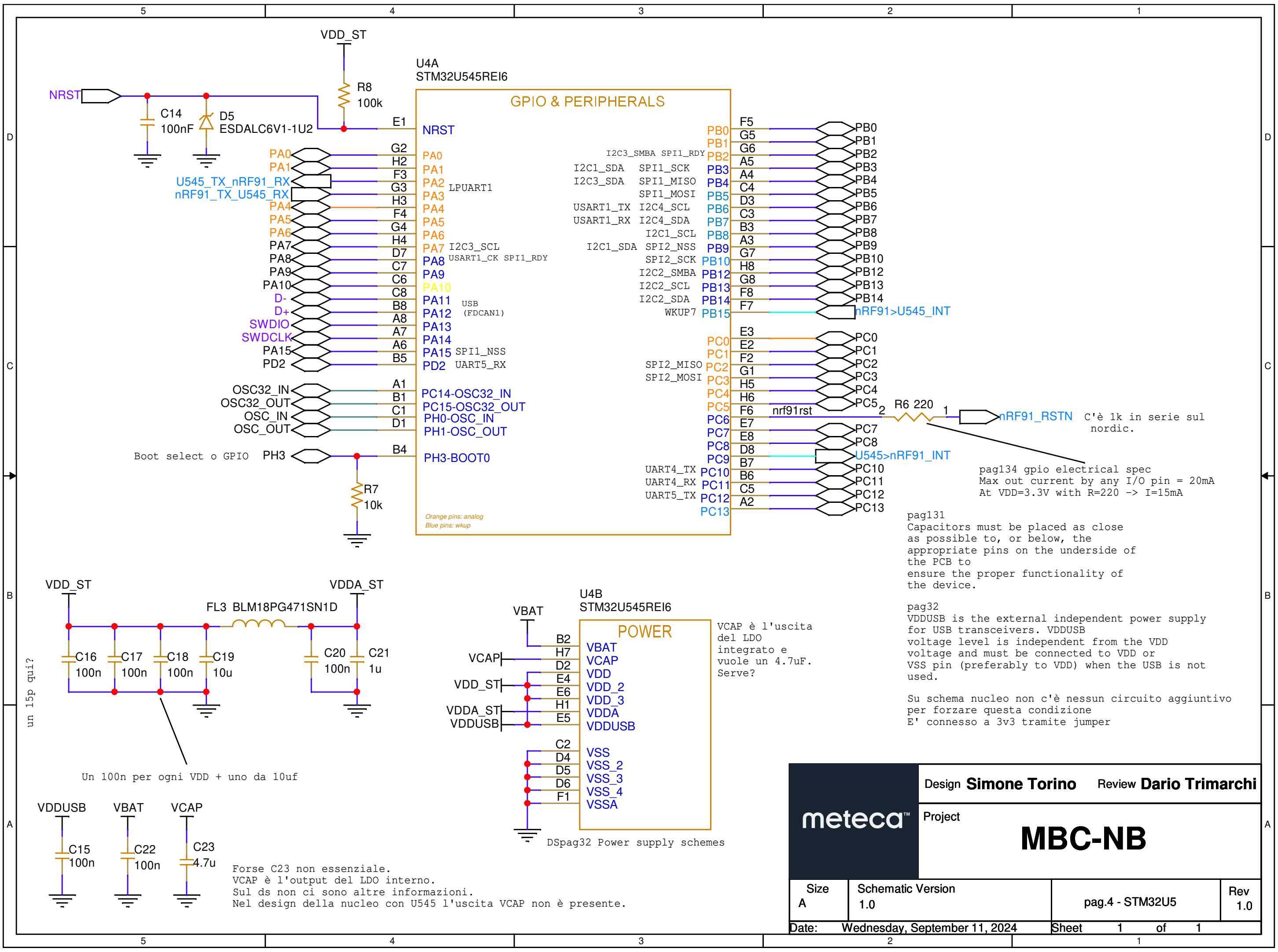
Project

MBC-NB

Size	Schematic Version		Rev
A	1.0	pag.3 - nRF9160	1.0

Date: Thursday, September 12, 2024 Sheet 1 of 1



C'è 1k in serie sul nordic.

pag134 gpio electrical spec
Max out current by any I/O pin = 20mA
At VDD=3.3V with R=220 -> I=15mA

pag131
Capacitors must be placed as close
as possible to, or below, the
appropriate pins on the underside of
the PCB to
ensure the proper functionality of
the device.

pag32
VDDUSB is the external independent power supply
for USB transceivers. VDDUSB
voltage level is independent from the VDD
voltage and must be connected to VDD or
VSS pin (preferably to VDD) when the USB is not
used.

Su schema nucleo non c'è nessun circuito aggiuntivo
per forzare questa condizione
E' connesso a 3v3 tramite jumper

VCAP è l'uscita
del LDO
integrato e
vuole un 4.7uF.
Serve?

Un 100n per ogni VDD + uno da 10uf

DSpag32 Power supply schemes

Forse C23 non essenziale.
VCAP è l'output del LDO interno.
Sul ds non ci sono altre informazioni.
Nel design della nucleo con U545 l'uscita VCAP non è presente.

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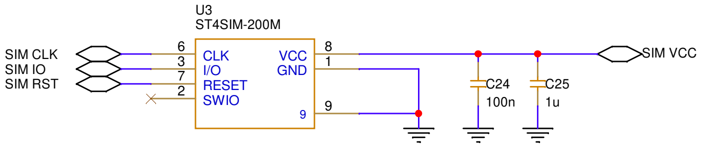
Project

MBC-NB

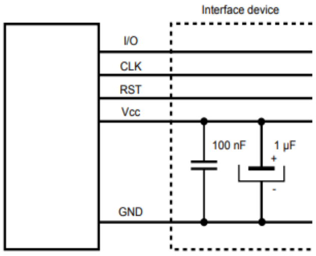
Size	Schematic Version		Rev
A	1.0	pag.4 - STM32U5	1.0

Date: Wednesday, September 11, 2024 Sheet 1 of 1



SWIO is not used
9th pin should be gnd pad in the footprint

Figure 6. Recommended filtering capacitors on V_{CC}



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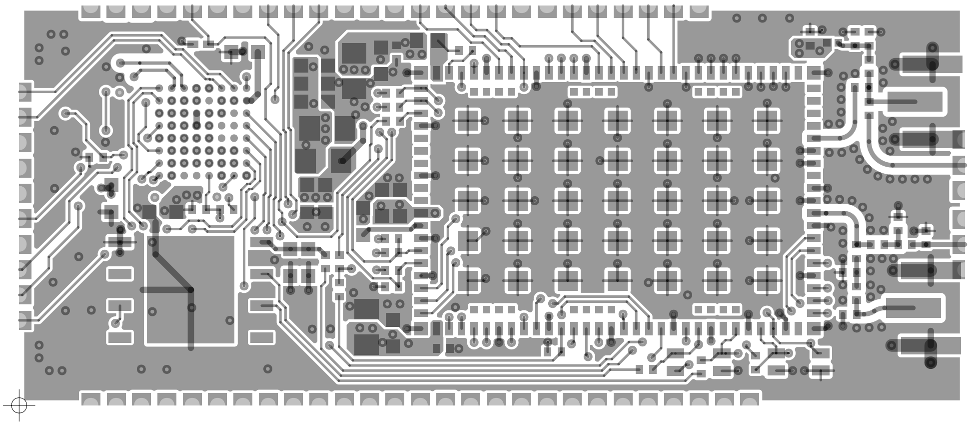
Project

MBC-NB

Size	Schematic Version		Rev
A	1.0	pag.4 - eSIM	1.0

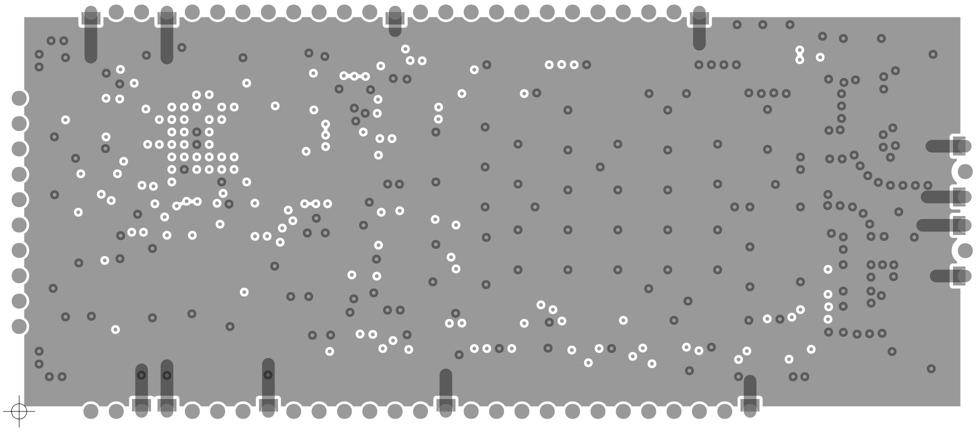
Date: Wednesday, September 11, 2024 Sheet 1 of 1

ART FILM – TOP



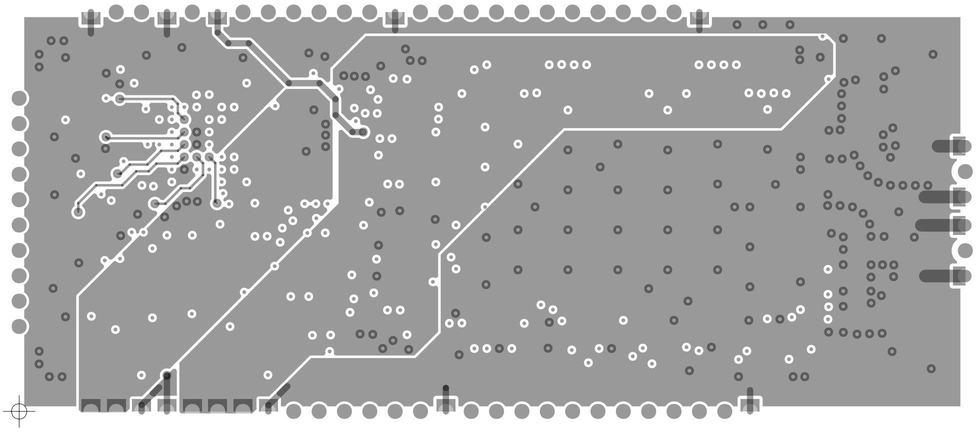
ART FILM – TOP

ART FILM - GND



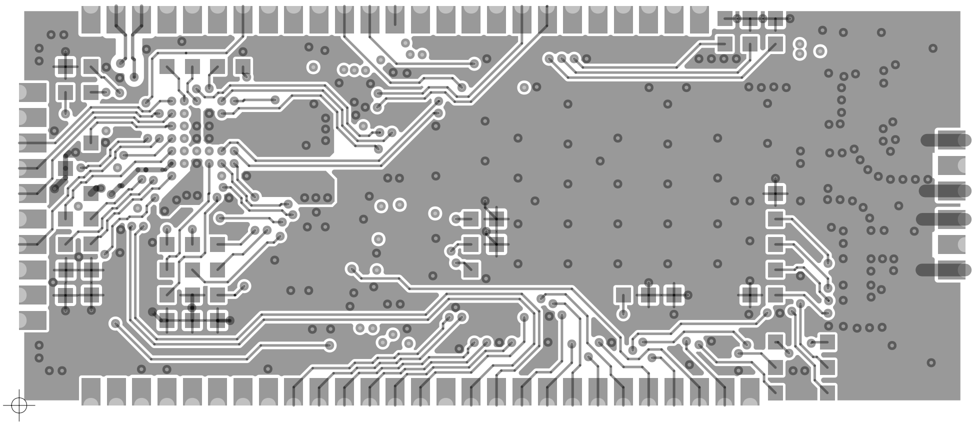
ART FILM - GND

ART FILM - POWER



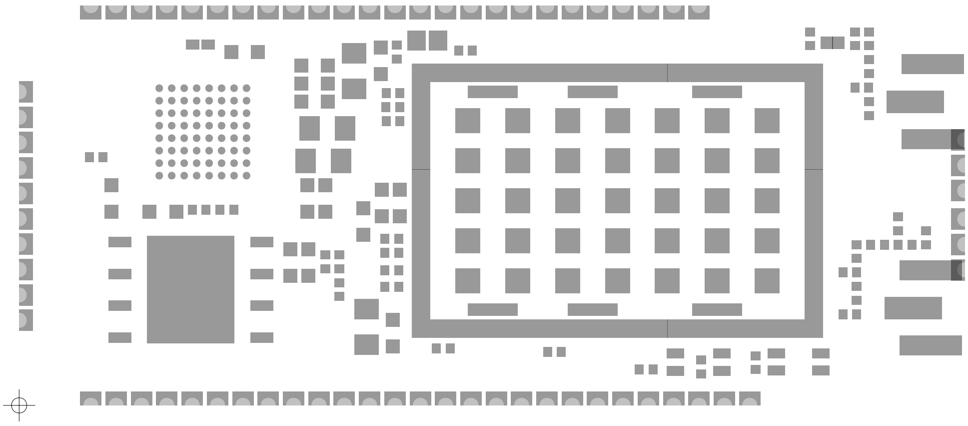
ART FILM - POWER

ART FILM – BOTTOM



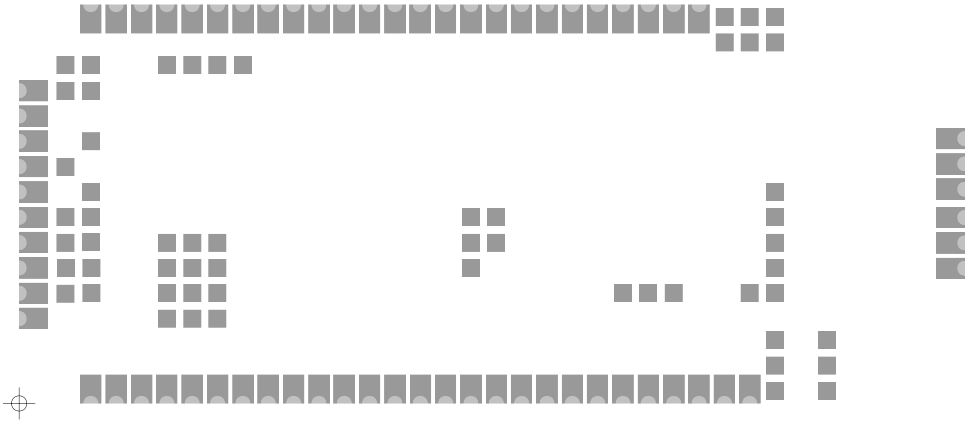
ART FILM – BOTTOM

ART FILM - SOLDER_TOP



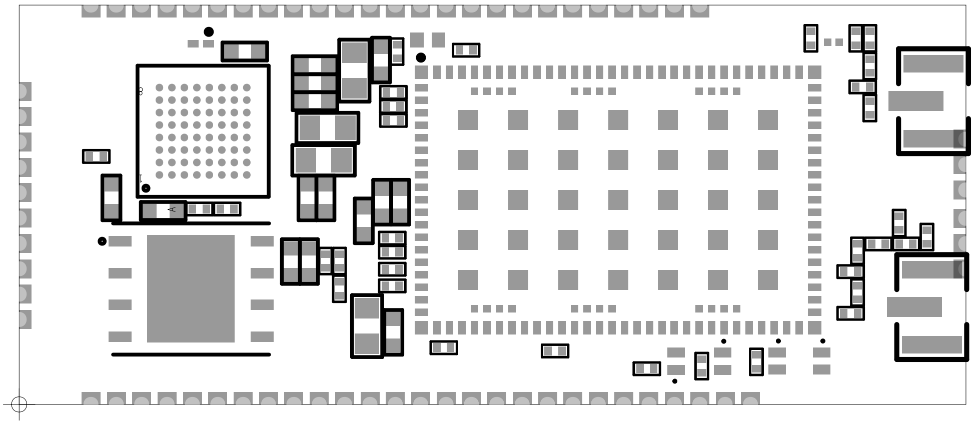
ART FILM - SOLDER_TOP

ART FILM - SOLDER_BOT



ART FILM - SOLDER_BOT

ART FILM - MOUNT_PLANE_TOP



ART FILM - MOUNT_PLANE_TOP