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Analysis and design of a high-precision programmable DC-DC converter

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Chapter 1

Introduction

The ability to convert a direct current (DC) voltage from one level to another while preserving electrical isolation between the input and output makes isolated DC-DC converters crucial components of contemporary electrical systems. In many commercial, industrial, and consumer applications, especially those where dependability, efficiency, and safety are critical, this type of power conversion is essential. Telecommunications, medical equipment, renewable energy systems (including solar and wind power), automotive electronics, industrial automation, and power supply units for servers and data centers are some of the major industries that depend on isolated DC-DC converters.
A DC-DC converter is a power electronics device that may either step up (boost) or step down (buck) a source of direct current from one voltage level to another. These converters are most frequently used in systems where the supply voltage is either too high or too low for the intended use, and where a high conversion efficiency is required to minimize heat production and energy loss. In order to manage the flow of energy, a DC-DC converter's primary operation usually combines switching devices (such as MOSFETs and IGBTs), inductors, capacitors, and control mechanisms. The input and output of non-isolated converters share a common ground, which facilitates energy transmission between the two but may also result in safety and noise concerns. By creating electrical isolation between the input and output, isolated DC-DC converters offer a notable benefit in this situation.
The physical separation of the converter's input and output stages is known as electrical isolation, and it is usually accomplished using a transformer or other isolation techniques. In order to ensure that electrical faults, voltage spikes, or surges on one side of the converter do not impact the other, the isolation's main purpose is to prohibit direct electrical connections between the two sides. In an isolated converter, the transformer shields downstream circuits from potentially harmful voltages by providing galvanic isolation in addition to energy transfer. In many applications, this isolation is essential, especially when the input and output sides are connected to distinct ground references, voltage domains, or even floating power supplies.
In comparison to non-isolated converters, isolated converters have the following advantages:

- Safety: Equipment that is sensitive or accessible by humans is shielded from hazardous primary-side voltages by isolated converters. Isolation guarantees that the user is not exposed to electrical risks, which is crucial in industrial and medical systems.
- Noise reduction and EMI suppression: High-frequency switching noise cannot spread between the input and output stages thanks to isolation. In audio/visual equipment and precision instruments, where noise interference may result in subpar performance or system failure, this is crucial. Additionally, isolation aids in the management of electromagnetic interference (EMI), which is produced during switching and has the potential to interfere with adjacent electronic devices.
- Ground Loop Prevention: Ground loops can develop in systems with several power sources and varying ground potentials, which can cause noise or signal distortion. This risk is removed by an isolated DC-DC converter, which offers a floating secondary side free from problems with ground reference.
- Voltage Level Shifting: Circuits that may use multiple ground references or operate at different voltage potentials can convert voltage levels thanks to isolation. Isolation enables safe

and effective voltage conversion in situations where input and output voltages, for instance, may range significantly, such as in automotive systems or renewable energy applications.

- Improved Fault Tolerance: By stopping faults from spreading throughout the converter, isolation helps safeguard delicate components on the secondary side in the event of electrical failures like short circuits.

An isolated DC-DC converter relies on several critical components to achieve efficient energy conversion and isolation:

- Transformer: The transformer, the central component of an isolated DC-DC converter, provides electrical isolation and transfers energy between the primary and secondary windings. It also plays a crucial part in voltage conversion by modifying the turns ratio to increase or decrease the voltage as necessary.

- Switching devices: Usually, they are fast-switching high-speed transistors (such as MOSFETs, IGBTs, or GaN devices) that regulate the energy flow via the transformer and inductive components. These devices frequently have switching frequencies between tens and hundreds of kHz.

- Control circuitry: To keep the output voltage and current steady, the control circuitry manages the devices' switching. A popular technique for regulating the duty cycle and, consequently, the power supplied to the load is pulse-width modulation, or PWM.

- Reactive elements: Capacitors smooth out voltage and current ripples to ensure a consistent supply of power to the load, whereas inductors store energy during the switching cycles.

- Rectifiers: Rectifiers (often synchronous rectifiers or diodes) on the transformer's secondary side change the AC power back into DC to produce the necessary output voltage.

There are two primary types of conduction modes in all DC-DC converters, including isolated topologies. Two separate operating regimes that affect the converter's behavior, effectiveness, and performance are referred to as Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). A key factor in deciding how energy is transmitted through the converter is the inductor current waveform during the switching cycle, which largely determines these modes. Designing and improving DC-DC converters for a range of applications requires an understanding of the distinctions between CCM and DCM.

- Operating principle of CCM: During the whole switching cycle, the inductor current flows constantly. Even when the switching transistor is turned off, the current never goes to zero and always stays above a specific threshold. As a result, energy moves from the input to the output smoothly and continuously. CCM typically occurs at higher load currents, where the system's power requirements necessitate a steady flow of energy. The inductor value is selected in these circumstances so that the current never drops to zero.

- Operating principle of DCM: There is a portion of the switching cycle where the inductor current falls to zero. This happens when the inductor's "on" phase energy is fully transferred to the load before the cycle is finished, temporarily stopping the inductor's current flow. When the load current is insufficient to sustain a constant current flow through the inductor, DCM is usually reported under low-load circumstances. Additionally, it can happen when the inductance is very low or at extremely high switching frequencies. Because the inductor current periodically drops to zero, DCM tends to cause larger output voltage and current ripples. This may have an impact on the load's power quality, particularly in delicate electronic applications.

The key differences between CCM and DCM operation are summarized in the following table.

Aspect	CCM	DCM
Inductor current	The inductor current is continuous and never drops to zero.	The inductor current drops to zero during part of the cycle.
Energy transfer	Continuous transfer of energy to the load.	Energy is transferred in bursts, with idle periods in between.
Load condition	More common at higher load currents.	Common at low load currents or light-load conditions.
Efficiency	High efficiency at higher loads.	High efficiency at light loads.
Component size	Requires larger inductors to maintain continuous current.	Smaller inductors due to lower average current requirements.
Output ripple	Lower current and voltage ripple.	Higher current ripple and potentially higher voltage ripple.

An illustration relevant waveforms in CCM and DCM operation for a Buck DC-DC converter is shown in [Fig: 1.1]. The picture was extracted from the reference [12], where the differences between CCM and DCM are discussed.

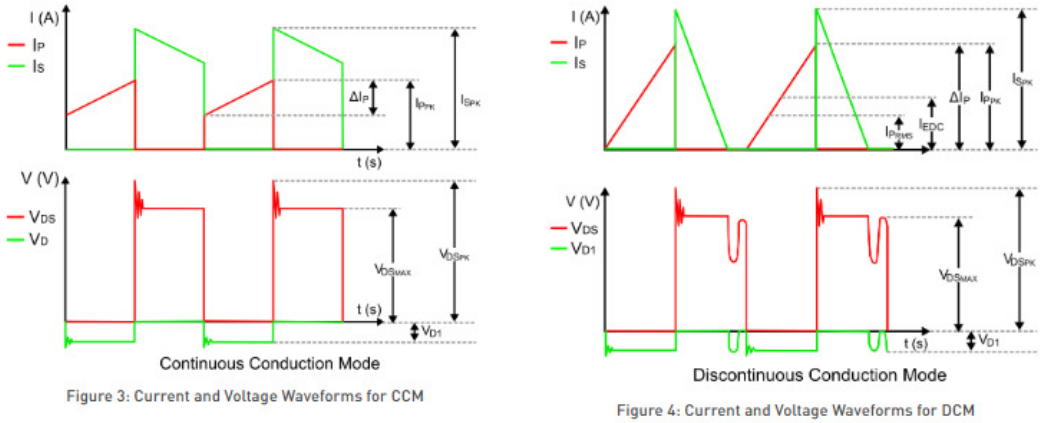

Figure 3: Current and Voltage Waveforms for CCM

Figure 4: Current and Voltage Waveforms for DCM

Figure 1.1: CCM vs DCM inductor current of a Buck converter

The technique used to control the output of isolated and non-isolated converters has a significant impact on their efficiency, output stability, transient responsiveness, and noise reduction. Voltage control and current control are the two main control strategies utilized in converters; each has unique properties and uses. Generally speaking, DC-DC converters' control mechanisms manage the power flow through the converter as well as the relationship between the input and output voltages. The two strategies, which concentrate on regulating the output voltage or the current in the converter's circuit, are founded on distinct feedback mechanisms. This decision has a direct impact on the converter's efficiency, susceptibility to noise and disturbances, stability under changing load circumstances, and dynamic response.

- Principle of voltage control: Regardless of variations in input voltage or load current, the main objective of voltage control is to maintain the converter's output voltage at an established level. The voltage feedback loop continuously compares the actual output voltage with a reference voltage. A controller, typically a Proportional-Integral-Derivative (PID) controller or a more straightforward proportional control scheme, receives the error signal produced by this comparison and modifies the duty cycle of the switching element or elements to keep the output voltage at the appropriate level.

- Principle of current control: Contrarily, current control regulates the current passing through the converter's inductor or other essential parts rather than the output voltage. This control system senses the output current and uses the feedback to modify the switching device's duty cycle in order to keep the current at a specified level.

A more detailed comparison can be found in [3]. The main characteristics of voltage and current control are pointed out in the following table.

Aspect	Voltage control	Current control
Control objective	Regulates the output voltage to a desired value.	Regulates the inductor or output current to a desired value.
Feedback loop	Voltage feedback, comparing output voltage with reference.	Current feedback, comparing inductor or load current with reference.
Transient responce	Slower transient response, less effective for rapid load changes.	Faster transient response, better at handling load variations.
Efficiency	Generally more efficient under steady-state conditions.	More efficient under dynamic conditions with varying loads.
Simplicity	Simpler to design and implement, especially for stable loads.	More complex to design, requires precise current sensing.
Component electricall stress	Lower component stress, especially under steady load.	Higher stress on components due to rapid current changes.
Current protection	Indirect protection against overcurrent.	Direct protection against overcurrent, better for safety.
Noise sensitivity	Less sensitive to noise and disturbances.	More sensitive to noise, particularly in current sensing.

Figures [Fig: 1.2] and [Fig: 1.3] depict the two control methods, which were extrapolated from papers [10] and [9] respectively, where each control method is examined in detail.

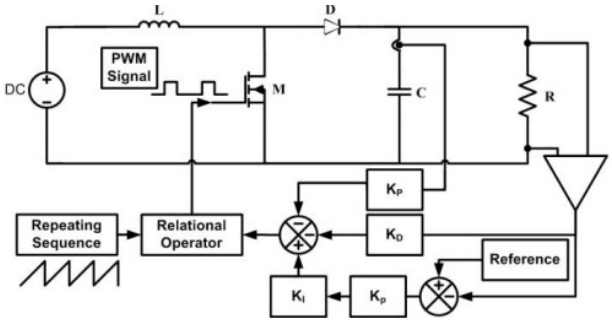

Fig. 6. Proposed Boost converter with PID controller for voltage regulation and overshoot reduction

Figure 1.2: Example of a voltage control block diagram

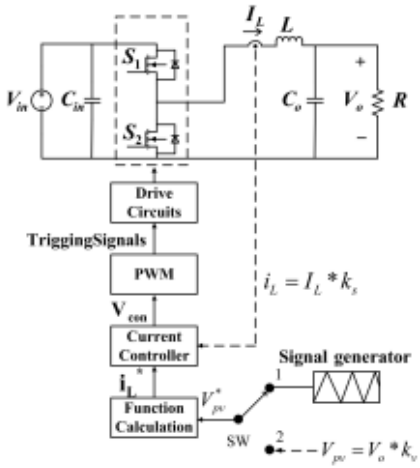

Figure 8. Block diagram of current mode control of synchronous buck converter.

Figure 1.3: Example of a current control block diagram

Chapter 2

State of the art

High-precision DC-DC converters are power electronics devices that regulate voltage or current precisely and steadily, frequently with very low tolerance levels. These converters are crucial for applications including precise instruments, medical devices, communication systems, aerospace, and high-end industrial controls where even slight changes in output power can have a big impact on system performance.
Texas Instruments released the SLVP182 user's manual in 2001, reference [7], which stated as follows: "The SLVP182 synchronous buck converter evaluation module (SLVP182) provides a reference design for evaluating the performance of a high accuracy power supply using the TL5002 pulse-width-modulation (PWM) controller coupled with a REF-1004 voltage reference." Although the manual's output accuracy results are rather impressive, the isolation barrier and the non-fixed output are the two primary distinctions from this master's thesis.
Texas Instruments' DCR01 series is introduced as follows in technical document [6]: "The DCR01 family is a series of high-efficiency, input-isolated, output-regulated DC/DC converters. In addition to 1-W nominal, galvanically-isolated output power capability, this range of DC/DC converters offer very low output noise, thermal protection, and high accuracy". The suggested device introduced an isolation barrier while achieving a worst-case output accuracy of 2% on a fixed output voltage. An article from Energies [14] from 2022 describes the design of a two-stage DC-DC converter that, by limiting its output ripple, may achieve a precision of up to 0.02% at an output voltage of $7kV$.

In conclusion, the limited number of papers available on high-precision isolated DC-DC converters suggests that this area of research may still be emerging. Even though DC-DC converters are a well-established subject, other considerations like efficiency or power density may take precedence over the particular focus on high-precision isolated systems. Given the growing number of high-precision applications in industries including aerospace, medical devices, and precision instruments, this gap offers a chance for additional research. Future studies may be able to address the potential and difficulties of these converters, leading to improvements in their functionality and wider use.

Chapter 3

Project design

3.1 Specification

Developing a DC-DC converter while complying to certain requirements is the purpose of this master's thesis.
Requirements:

- input-output isolation;
- variable input voltage: $V_{in} \in [5, 12]\, V$;
- variable output voltage: $V_o \in [6, 48]\, V$;
- reference voltage supplied via DAC from NUCLEO-F334R8;
- output step: $50mV$;
- maximum average error: $1mV$;
- load resistance: $R_{load} \geq 100\Omega$;
- load capacitance: $C_{load} \leq 1\mu F$;
- settling time: $t_{settling} < 10ms$;
- conversion efficiency: $\eta \geq 95\%$.

Although this type of design is not new in the literature, the project's original features are the accuracy requirement and the input and output voltage variability.
While there are numerous DC-DC converter topologies, the most widely used isolated ones are:

- Flyback;
- Forward;
- Push-Pull;
- Half-Bridge;
- Full-Bridge.

These topologies are separated into three categories according on their suggested operating power: low power, medium power, and high power.

$$P_{out,max} = \frac{V_{out,max}^2}{R_{load,min}} = 23.04W. \tag{3.1}$$

The maximum output power was calculated in equation [Eq: 3.1] and falls into the low power category.
A switching frequency of $1MHz$ has been chosen primarily for two reasons:

- Reduce generally the dimension of the components.
- Reduce the settling time by increasing the system bandwidth.

Finally, the converter will also be a low current converter considering the maximum output current is less than $500mA$. To ensure that the inductor current is always greater than zero, a CCM operation mode with a low output current must drastically reduce the current ripple, which raises the values of the components involved. Consequently, a DCM operation should be selected over a CCM operation in this project, as noted in technical article [2] referring to a Flyback project: "CCM operation is best suited for medium-to-high-power applications, but if you have a low-power application that could use a DCM flyback."
Four converters were initially selected for design in order to offer a wider selection. Respectively two low power:

- DCM-operated Flyback;
- CCM-operated Forward.

and two medium power:

- CCM-operated Half-Bridge;
- CCM-operated Push-Pull.

In order to select the most appropriate circuit topology, all converter designs were made with the goal of achieving the same performances while meeting the requirements. To do this, a few values that are shared by all designs need be previously declared:

- for CCM-operated topologies: $R_{max} = 10k\Omega$;
- maximum output voltage ripple: $\Delta V_o = 10mV$;
- maximum voltage drop on the transistor when active: $V_{on} = 100mV$;
- rise and fall times of the transistor states: $t_{rise} \approx t_{fall} = 2ns$.

3.2 Flyback DCM

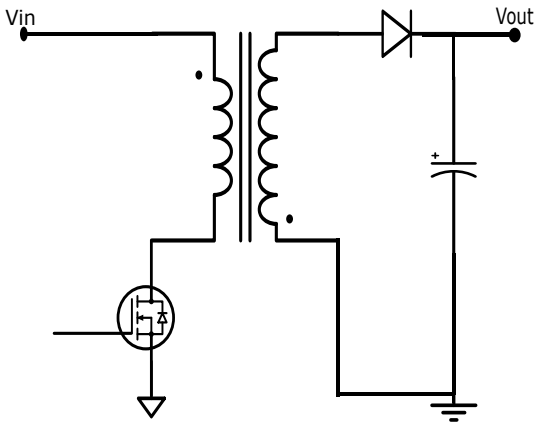

Figure 3.1: Flyback schematic

Description

Only a few components are needed for the Flyback topology, as seen in figure [Fig: 3.1]. Since there is no direct power transmission, the converter is referred to as a '*indirect*' converter. Power accumulates on the primary side during t_{on} and is subsequently transferred to the secondary side during t_{off}. Instead of using a transformer to achieve isolation, two coupled inductors are used because of the two-step power transmission. The coupled inductors have a reduced magnetizing inductance, which raises the magnetizing current and, consequently, the power stored in the magnetic

core. The non isolated topology from which the Flyback originates, the Buck-Boost converter, is the source of all these features, reference [4] provides a detailed description of the complete circuit derivation. Another point of reference is the frequency behavior: the Flyback, as the Buck-Boost, is easier to control in DCM operating mode rather than CCM since we can observe the existence of positive real part zeros in the CCM transfer-function. For this reason, as is commonly done in literature, the Flyback is operated in DCM in this analysis.

Project

To move further with the project, a few assumptions are required:

- diode forward voltage drop: $V_f = 1V$;
- t_{on} maximum duty cycle: $D_{max} = 0.45$;
- t_{off} maximum duty cycle: $D_{2,max} = 0.4$;
- magnetic efficiency: $\eta_{magn} = 0.9$.

The analysis continues by taking into account the output worst-case scenario:

- $V_{out} = 48V$;
- $R_{load} = R_{out,min} = 100\Omega$.

The elements' sizes in accordance with the chosen project flow come next.

Coupled Inductors Since the coupled inductors is the primary constraint on providing the load with sufficient power, its sizing is the first step in the design process and $V_{in} = 5V$ is the input worst-case scenario to ensure that there is adequate power.

$$\frac{N_s}{N_p} = \frac{V_{out} + V_f}{V_{in} - V_{on}} \cdot \frac{D_2}{D_{max}} \cdot (1 + 5\%) = 9.33 \tag{3.2}$$

The required turn ratio is calculated in relation [Eq: 3.2]. The extra 5% term is included in the design to account for the parasitic impact, which will result in a lower effective turn ratio value. The chosen value is: $\frac{N_s}{N_p} = 10$. Selecting the magnetizing inductance to meet the secondary's power request is the next step.

$$P_{secondary} = (V_{out} + V_f) \cdot I_{out} = 23.52W \tag{3.3}$$

$$L_m = \frac{(V_{in} - V_{on})^2 D_{max}^2}{2 f_s P_{secondary}} \cdot \eta_{magn} = 93nH \tag{3.4}$$

The secondary power is computed from relation [Eq: 3.3] and utilized to determine the inductance value with relation [Eq: 3.4]. The existence of a leakage flux as a result of an imperfect coupling between the inductors is taken into consideration by the η_{magn} term. To ensure sufficient power, the calculated value of the needed magnetizing inductance must be equal to or less than the calculated value.
An extensive investigation of the component market revealed nothing that could be substituted, so a custom magnetic component was considered. A toroidal-shaped core with core material 61 was chosen. Figure [Fig: 3.2] illustrates how the material is designed to tolerate such frequency values.

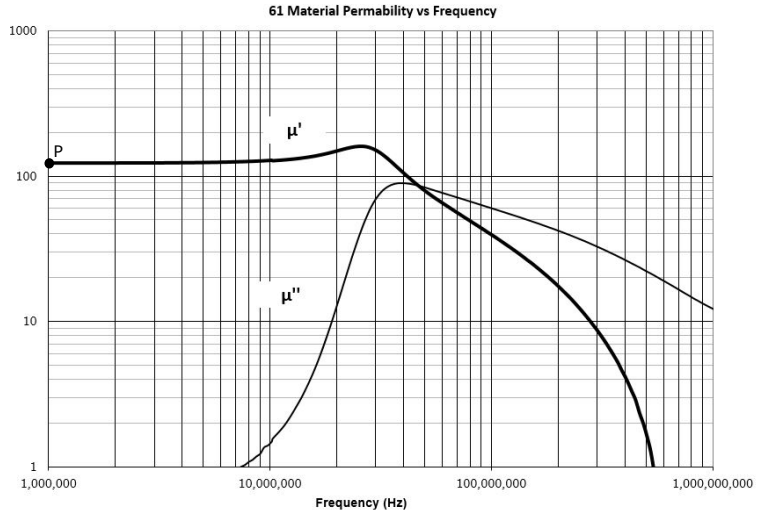

Figure 3.2: Relative permeability from FAIR-RITE

All of the relations were collected from source [4] in order to choose the correct toroid:

$$L_m = A_l \cdot N_p^2 \tag{3.5}$$

$$\Delta B = \frac{V_{in} D}{2 A_e f_s N_p} \tag{3.6}$$

$$P_{cu} = \left(\frac{\rho \lambda^2 I_{TOT}}{4 K_u}\right) \cdot \left(\frac{MLT}{W_a A_e^2}\right) \cdot \left(\frac{1}{\Delta B^2}\right) \tag{3.7}$$

Few new variables were introduced:

- A_l: core inductance factor;
- ΔB: maximum flux density;
- A_e: core cross-sectional area;
- ρ: wire effective resistivity;
- $\lambda = \int Vin(t)dt$: applied volt-seconds balance law;
- I_{TOT}: total rms winding currents, referred to primary;
- K_u: winding fill factor;
- MLT: mean length per turn;
- W_a: core window area.
- P_{cu}: winding dissipated power;
- $A_{w,i}$: wire cross-section.

A satisfying magnetic core is established from the market. These features are the result of the design:

- toroidal core Part Number: 5961004921;
- $B_{max} = 250mT$;
- $P_{diss} = 135mW$;

- $N_p = 1$;
- $N_s = 10$;
- $L_m = 80nH$;
- $A_{w,p} < 15mm^2$;
- $A_{w,s} < 1.5mm^2$.

Finally, new duty cycle values were calculated using equation [Eq: 3.4]:

- $D_{5\to48} = 0.388$;
- $D_{12\to48} = 0.162$.

Transistor The drain-source breakdown voltage is a metric to select the transistor; this is accomplished using relation [Eq: 3.8], where to look for the worst-case $V_{in} = 12V$.

$$BV > \left(V_{in} + (V_{out} + V_f)\frac{N_s}{N_p}\right) \cdot (1 + 30\%) = 21.97V \tag{3.8}$$

The additional 30% factor accounts for spikes produced by the leakage inductance produced by a sudden drop in current.

$$I_{sw,max} = \frac{V_{in}D}{L_m f_s} = 24.3A \tag{3.9}$$

$$I_{sw,rms} = I_{sw,max}\sqrt{\frac{D}{3}} = 8.7A \tag{3.10}$$

The maximum current and its root mean square value are additional factors. When the input voltage is set to $V_{in} = 5V$ for the current computation performed in relation [Eq: 3.9] and [Eq: 3.10], the current will reach higher peaks. The power dissipated in conduction is calculated using the rms value, and the required value of the conduction resistance is estimated using the peak value, as done in relation [Eq: 3.11].

$$R_{on,HOT} = \frac{V_{on}}{I_{sw,max}} = 4.4m\Omega \tag{3.11}$$

It should be remembered that the resistance value that was just calculated refers to a state in which the operation has heated the device; for this reason, it is marked as "HOT." The 'COLD' value, which is the one that manufacturers specify, is typically calculated by halving the hot value. The selected transistor exhibits the following characteristics::

- transistor Part Number: BSC0902NSI;
- $BV = 30V$;
- $I_{sw,max} = 100A$;
- $R_{on,COLD} = 2.8m\Omega$;
- $Q_g = 32nC$.

The total gate charge that the gate driver must charge and discharge is indicated by Q_g. In the dynamic analyses, this value must be taken into account; in fact, it should be kept to a minimum to need lower current spikes to drive the gate terminal or switching the transistor operating stage for a fixed maximum gate current takes longer.
Two components contribute to the overall power dissipated: the switching dynamic and conduction. Accordingly, both were calculated using relations [Eq: 3.12] and [Eq: 3.13].

$$P_{dynamic} = \frac{f_s}{2} \cdot t_{fall} \cdot \left(V_{in} + (V_{out} + V_f)\frac{N_s}{N_p}\right) \cdot I_{sw,max} = 534mW \tag{3.12}$$

$$P_{conduction} = R_{on,HOT} \cdot I^2_{sw,rms} = 333mW \tag{3.13}$$

As a result, $867mW$ of power is dissipated.

Diode Relation [Eq: 3.14] is used to determine the breakdown voltage of the diode initially.

$$BV > \left(V_{in} + (V_{out})\frac{N_s}{N_p}\right) \cdot (1 + 30\%) = 218.4V \tag{3.14}$$

In the current case, $V_{in} = 12V$ also presents the worst situation and Using relation [Eq: 3.15], the maximum current peak is calculated.

$$I_{diode,max} \approx \frac{2I_{out}}{D_2} = 2.4A \tag{3.15}$$

The chosen diode has the following characteristics:

- diode Part Number: BYV10D-600PJ;
- $V_f = 1V$;
- $BV = 600V$;
- $I_{diode,max} = 20A$;
- $t_{rr} = 75ns$.

The reverse recovery time, or t_{rr}, is a crucial factor and must be taken into account for the diode to operate correctly in both the forward and reverse regions.
When the Ampere-second balance law is applied at the output capacitor, the average current entering the diode is simply the output current.
Ultimately, the power wasted is calculated using [Eq: 3.16].

$$P_{conduction} = V_f \cdot I_{diode,average} = 480mW \tag{3.16}$$

Output capacitor Equation [Eq: 3.17] can be used to calculate the capacitor's maximum voltage drop.

$$V_{C_{out},max} > V_{out} = 48V \tag{3.17}$$

Since a high capacitance is anticipated, electrolytic capacitor technology was selected. At such a frequency, the dynamic behavior of these capacitors can be accurately described as resistive. For this reason, calculating the parasitic series resistance, or R_{esr}, as shown in equation [Eq: 3.18], is crucial.

$$R_{esr} < \frac{\Delta V_{out}}{I_{diode,max}} = 41.7m\Omega \tag{3.18}$$

These capacitors also have the peculiarity of adding a zero to the frequency response, which is calculated as in [Eq: 3.19]. Depending on the material, these zeros are typically positioned around specific frequencies. In this case, a zero frequency of $5kHz$ was presumed.

$$f_{ESR} = \frac{1}{2\pi C_o ESR} \tag{3.19}$$

An orientative value for the capacitance, $C_{out} = 1mF$, can be calculated by inverting the upper formula.
The chosen capacitor has the following characteristics:

- capacitor Part Number: EKYB630ELL152MMN3S;
- $V_{C_{out},max} = 63V$;
- $C_{out} = 1.5mF$;
- $R_{esr} = 18m\Omega$.

There will also be a power dissipation because the capacitor contains a parasitic resistive component. The rms value of the current is first calculated using relation [Eq: 3.20], and the dissipation is then assessed using relation [Eq: 3.21].

$$I_{C_{out},rms} = I_{diode,max}\sqrt{\frac{D_2}{3} - \frac{D_2^2}{4}} = 733mA \tag{3.20}$$

$$P_{C_{out}} = R_{esr} \cdot I^2_{C_{out},rms} = 9.7mW \tag{3.21}$$

Efficiency Based on preliminary analysis, the overall power dissipation is $P_{diss} = 1.36W$, and the power given to the load is $P_{out} = 23.04W$. Relation [Eq: 3.22] is used to calculate the efficiency.

$$\eta = \frac{P_{out}}{P_{out} + P_{diss}} = 0.944 \tag{3.22}$$

3.3 Forward CCM

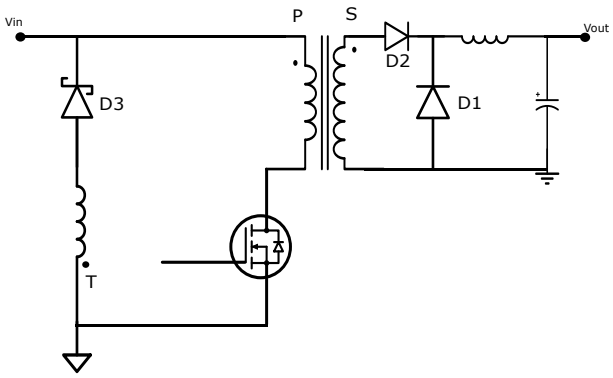

Figure 3.3: Forward schematic

Description

Another low power architecture that can be employed is the Forward. In literature, it is usually used in CCM since it is a Buck-derived circuit that performs well in this operating mode in contrast to Boost and Buck-Boost derivatives.
Since the power is moved straight from the primary to the secondary, this topology is known as a '*direct*' topology. Because of this, a transformer provides the isolation. To avoid non-negligible core magnetizing currents and consequent power loss, it should have a high magnetizing inductance.
The way the magnetic core is discharged is what makes this converter distinctive. In order to discharge the transformer and avoid saturation, a terziary winding, referred to as "t" in this context, is added to give a negative voltage across the transformer's primary terminals. A unitary turn ratio between primary and terziary is frequently used because it can result in a more uniform electrical stress across all of the components.

Project

To move further with the project, a few assumptions are required::

- diode forward voltage: $V_f = 1V$;
- t_{on} maximum duty cycle: $D_{max} = 0.45$;
- primary and terziary turns: $N_p = N_t$.

The analysis continues by taking into account the output worst-case scenario:

- $V_{out} = 48V$;
- $R = R_{min} = 100\Omega$.

The elements' sizes in accordance with the chosen project flow come next.

Turn ratio The transformer is in charge of providing the secondary side with an appropriate voltage. To guarantee that the turn ratio is calculated accurately in relation [Eq: 3.23].

$$\frac{N_s}{N_p} = \frac{V_{out} + V_f}{(V_{in} - V_{on})\, D_{max}} \cdot (1 + 5\%) = 23.33 \tag{3.23}$$

The 5% component is included to account for the presence of parasites, as was previously done and the worst case is exhibited for $V_{in} = 5V$. The chosen turn ratio is $\frac{N_s}{N_p} = 24$.
If used in CCM, all of the Buck-derived topologies have the same conversion factor, as shown by relation [Eq: 3.24].

$$M_{CCM} = \frac{V_{out}}{V_{in}} = D\frac{N_s}{N_p} \tag{3.24}$$

It is straightforward to estimate the duty cycle's extreme values, $D_{input \to output}$, using the relationship above:

- $D_{5 \to 6} = 0.05$;
- $D_{12 \to 6} = 0.02$;
- $D_{5 \to 48} = 0.4$;
- $D_{12 \to 48} = 0.17$;

Inductor The inductor is in charge of maintaining the converter's operation in CCM. Relation [Eq: 3.25] is necessary for this.

$$L > \frac{R_{load}}{2f_s} \cdot (1 - D) = 4.9mH \tag{3.25}$$

The minimum output current represents the worst scenario:

- $R_{load} = 10k\Omega$;
- $D = 0.02$.

To proceed with the analysis, a preliminary inductance selection is needed. It is often advised to choose the new standard inductance value and to ensure that, even with the fabrication tolerances, the value does not exceed the set limit. The chosen inductance is $L = 6.2mH$.
Relation [Eq: 3.26] calculates the inductor current ripple, which should ideally be far less than the average inductor current value.

$$\Delta i_L = \frac{V_{out}}{Lf_s} \cdot (1 - D) = 6.43mA \tag{3.26}$$

The ripple's maximum value is found for $D = 0.17$.
The maximum and minimum current, that are calculated in relation [Eq: 3.27] and [Eq: 3.28], respectively, are additional relevant information.

$$I_{max} = I_o + \frac{\Delta i_L}{2} = 483mA \tag{3.27}$$

$$I_{min} = I_o - \frac{\Delta i_L}{2} = 477mA \tag{3.28}$$

Lastly, by calculating the inductor minimum current, the CCM operation may be confirmed, as done in [Eq: 3.29].

$$I_{L,min} = \frac{V_{out}}{R_{load}} - \frac{\Delta i_L}{2} = 125\mu A > 0A \tag{3.29}$$

The amount given is based on the maximum current ripple and minimum load current:

- $D = 0.02$;
- $R_{load} = 10k\Omega$.

The selected inductor exhibits the following characteristics::

- Inductor Part Number: SS11VL-10062;

- $L = 6.2mH$;
- $I_{l,average} = 1A$;
- $R_{esr} = 440m\Omega$.

The small ripple approximation can be used since the ripple is much smaller than the average current value, as shown in relation [Eq: 3.30].

$$I_{l,rms} \approx I_{l,average} \tag{3.30}$$

The parasitic series resistance is the cause of the power dissipation, and it should be calculated as described in relation [Eq: 3.31].

$$P_l = R_{esr} \cdot I^2_{C_{out},rms} = 101mW \tag{3.31}$$

Output capacitor Equation [Eq: 3.17] can be used to calculate the capacitor's maximum voltage drop, it is of $48V$. Once more, electolytic capacitor technology was selected, hence it's critical to calculate the R_{esr} value, [Eq: 3.32].

$$R_{esr} < \frac{\Delta V_{out}}{\Delta i_L} = 1.7\Omega \tag{3.32}$$

The current ripple value is among the worst-case scenarios that were previously calculated.
Assuming the frequency of the added zeros, [Eq: 3.19], to be $10kHz$, the indicative capacitance obtained is $C_{out} = 9.4\mu F$.
The chosen capacitor has the following characteristics:

- capacitor Part Number: PCM1J120MCL1GS;
- $V_{C_{out},max} = 63V$;
- $C_{out} = 12\mu F$;
- $R_{esr} = 51m\Omega$.

Relation [Eq: 3.33] calculates the rms value of the capacitor current, that is used to compute the power dissipated, $P_{diss} = 1\mu W$, in [Eq: 3.21].

$$I_{C_{out},rms} = \frac{\Delta i_L}{\sqrt{12}} = 1.7mA \tag{3.33}$$

Diodes Three distinct diodes are used in the forward, and each will be examined independently.

- D_1:
  Relation [Eq: 3.34] is used to calculate the breakdown vote.

  $$BV > V_{in}\frac{N_s}{N_p} \cdot (1 + 30\%) = 374.4V \tag{3.34}$$

  Considering $V_{in} = 12V$ as worst-case.
  And the average current is computed by relation [Eq: 3.35].

  $$I_{diode,average} = I_{out}\,(1 - D) = 398mA \tag{3.35}$$

  Considering as worst-case $D = 0.17$ and the maximum output current. The selected diode has the following characteristics:

  - diode Part Number: 1N4004;
  - $V_f = 1.1V$;
  - $BV = 400V$;
  - $I_{diode,max} = 1A$.

- D_2:
  At this diode can be applied relation [Eq: 3.34] too, leading at the same result: $BV > 374.4V$. Instead, we are now taking into account the complementary time frame for the current computation, using relation [Eq: 3.36] and considering $D = 0.17$ as worst case.

  $$I_{diode,average} = I_{out}D = 192mA \tag{3.36}$$

  The selected diode has the following characteristics:

  - diode Part Number: 1N4004;
  - $V_f = 1.1V$;
  - $BV = 400V$;
  - $I_{diode,max} = 1A$.

- D_3:
  The breakdown voltage is computed with relation [Eq: 3.37]

  $$BV > \left(V_{in} + V_{in}\frac{N_t}{N_p}\right) \cdot (1 + 30\%) = 31.2V \tag{3.37}$$

  This diode's current is essentially the magnetizing current, which is negligible in comparison to the other quantities.
  The selected diode has the following characteristics:

  - diode Part Number: SB140S;
  - $V_f = 0.5V$;
  - $BV = 40V$.

The power dissipated by each diode can be computed by relation [Eq: 3.16], leading to a total power lost of $480mW$.

Transformer Its design is required because there isn't a suitable transformer available on the market. Once more, the reference design in [4] serves as the basis.
Toroidal is the chosen core shape, and 75 is the chosen core material. Although this material may operate up to 100 kHz, figure [Fig: 3.4] suggests that it is being used effectively.

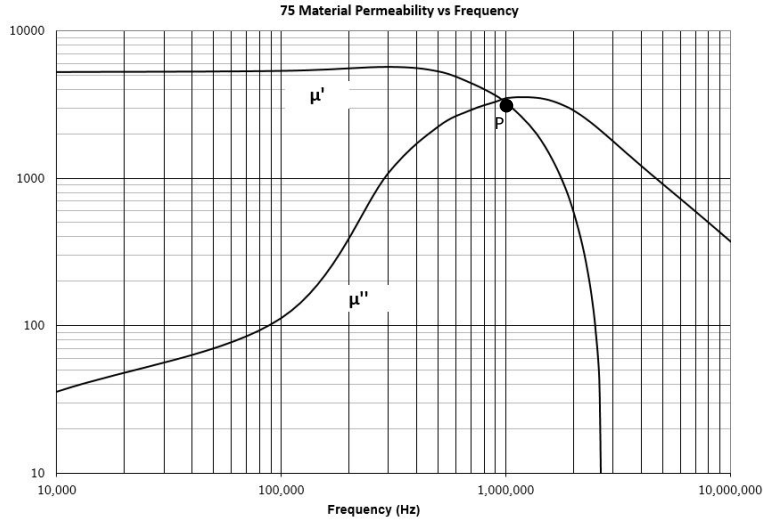

Figure 3.4: Relative permeability from FAIR-RITE

Relationships [Eq: 3.5], [Eq: 3.6], and [Eq: 3.7] were repeated in order to identify the core. As a compromise for low power dissipated, the obtained magnetizing inductance is $2\mu H$, which is a relatively low value.
A satisfying magnetic core is established from the market. These features are the result of the design:

- toroidal core Part Number: 5975000321;
- $B_{max} = 480mT$;
- $P_{diss} = 104mW$;
- $N_p = 1$;
- $N_s = 24$;
- $N_t = 1$;
- $L_m = 2\mu H$;
- $A_{w,p} < 4.08mm^2$;
- $A_{w,s} < 0.34mm^2$;
- $A_{w,t} < 4.08mm^2$.

Transistor Finding the required drain-source breakdown voltage is the first step in choosing a transistor, done in relation [Eq: 3.38], where $Vin = 12V$ is the worst-case scenario.

$$BV > \left(V_{in}\frac{N_p}{N_t} + V_{in}\right) \cdot (1 + 30\%) = 31.2V \tag{3.38}$$

In this instance, the inductor current can be used to calculate the minimum and maximum transistor current, as shown in relations [Eq: 3.39] and [Eq: 3.40].

$$I_{sw,max} = I_{max}\frac{N_s}{N_p} = 11.60A \tag{3.39}$$

$$I_{sw,min} = I_{min}\frac{N_s}{N_p} = 11.45A \tag{3.40}$$

At last, relation [Eq: 3.41] is used to calculate the transistor current's rms value.

$$I_{sw,rms} = I_{out}\frac{N_s}{N_p}\sqrt{D} = 7.3A \tag{3.41}$$

Relation [Eq: 3.11] allows one to figure out $R_{on,HOT} = 6.6m\Omega$. Keep in mind that the manufacturer's stated value relates to $R_{on,COLD}$.
The selected transistor exhibits the following characteristics::

- transistor Part Number: NTMFS5H425NLT1G;
- $BV = 40V$;
- $I_{sw,max} = 118A$;
- $R_{on,COLD} = 2.8m\Omega$;
- $Q_g = 14nC$.

Relation [Eq: 3.13] is used to calculate the power dissipated in conduction, and the result is $299mW$. Instead, relation [Eq: 3.42] is used to calculate the dynamic power dissipated.

$$P_{dyn} = \frac{f_s}{2} \cdot t_{rise} \cdot \left(V_{in}I_{sw,min} + \left(V_{in}\frac{Np}{Nt} + V_{in}\right) \cdot (1 + 30\%)I_{sw,max}\right) = 444mW \tag{3.42}$$

The transistor's overall power dissipation is $743mW$.

Efficiency Based on preliminary analysis, the overall power dissipation is $P_{diss} = 1.47W$, and the power given to the load is $P_{out} = 23.04W$. Relation [Eq: 3.22] calculates the efficiency and returns a value of 0.940.

3.4 Half-Bridge CCM

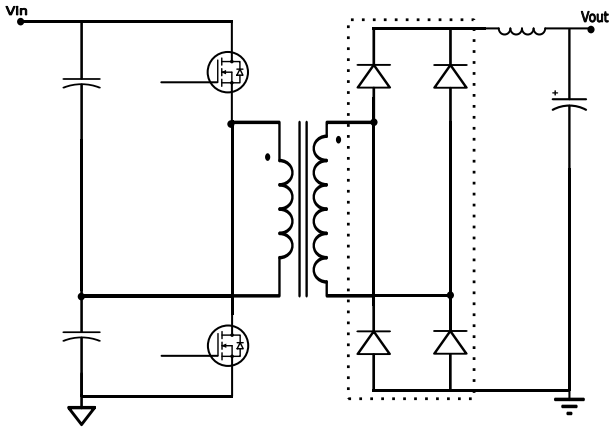

Figure 3.5: Half-Bridge schematic

Description

The Half-Bridge is an isolated topology derived from the Buck converter. It can be operated safely in CCM for the same reasons that have been stated before.
The secondary's ripple frequency is a significant figure of merit because it doubles the switching frequency. This saves money and space by enabling the designer to stick to a simpler output filter. This topology, however, is often employed for circuits with medium power, which is not the case here due to the growing number of components required overall.
For the primary side, duty cycle and frequency values will be indicated by 's', and for the secondary side, by 'b'.
In contrast to Flyback and Forward topologies, the majority of the cycle can be used to transfer power in this architecture, which makes frequency doubling feasible. The important thing to remember is that during toff, a negative voltage is applied at the transformer's primary terminals. In order to supply a negative voltage to the transformer, this architecture employs a capacitor branch to generate a reference voltage.
The rectifying block and the Buck characteristic output filter form the secondary side; the rectifying block can be either a center tapped or a Graetz bridge; in figure [Fig: 3.5], the Graetz bridge is utilized.

Project

For this project, the Graetz bridge onto the center tapped is selected in order to minimize the voltage drop across the secondary.
To move further with the project, a few assumptions are required:

- diode forward voltage: $V_f = 1V$;
- secondary's ripple frequency: $f_b = 2MHz.$;
- duty cycle at the primary: $D_{s,max} = 0.45$;
- duty cycle at the secondary: $D_{b,max} = 0.90$.

The analysis continues by taking into account the output worst-case scenario:

- $V_{out} = 48V$;
- $R = R_{min} = 100\Omega$.

The elements' sizes in accordance with the chosen project flow come next.

Turn ratio The transformer is responsible for supplying a suitable voltage to the secondary side. To ensure that the turn ratio in relation [Eq: 3.43] is computed appropriately.

$$\frac{N_s}{N_p} = \frac{V_{out} + 2V_f}{\left(\frac{V_{in}}{2} - V_{on}\right) D_{b,max}} \cdot (1 + 5\%) = 24.30 \tag{3.43}$$

To provide an appropriate voltage at the secondary, the turn ratio is roughly set at $\frac{N_s}{N_p} = 25$.
Using relation [Eq: 3.24], estimating the extreme values of the duty cycle is simple:

- $D_{b,5\to6} = 0.1$;
- $D_{b,12\to6} = 0.04$;
- $D_{b,5\to48} = 0.77$;
- $D_{b,12\to48} = 0.32$.

Inductor Once again, relation [Eq: 3.44] must be used to get the minimum inductance for CCM.

$$L > \frac{R_{load}}{2f_b} \cdot (1 - D_b) = 1.7mH \tag{3.44}$$

Considering these values as worst-case:

- $R_{load} = 10k\Omega$;
- $D_b = 0.04$.

A $3mH$ inductance has been picked. From relation [Eq: 3.45], the maximum current ripple can be computed, obtained by considering $D_b = 0.32$ as worst-case.

$$\Delta i_L = \frac{V_{out}}{Lf_b} \cdot (1 - D_b) = 5.44mA \tag{3.45}$$

$I_{max} = 483mA$ and $I_{min} = 477mA$ were produced by taking advantage of relations [Eq: 3.27] and [Eq: 3.28].
Additionally, the CCM operation is tested with relation [Eq: 3.29], that gives $120\mu A$, for $D_b = 0.04$ and $R_{load} = 10k\Omega$ as worst-case.
The selected inductor exhibits the following characteristics::

- Inductor Part Number: SC-01-30G;
- $L = 3mH$;
- $I_{l,average} = 1A$;
- $R_{esr} = 120m\Omega$.

The dissipated power that results from applying the small ripple approximation in relation [Eq: 3.30] and taking into account the parasitic resistance is $28mW$, computed with [Eq: 3.31].

Output capacitor The maximum voltage drop of the capacitor can be determined using equation [Eq: 3.17], resulting in $48V$ at maximum.
As has been done, $R_{esr} < 1.78\Omega$ is calculated using relation [Eq: 3.32], $C_{out} = 9\mu F$ is estimated using relation [Eq: 3.19], and $f_{esr} = 10kHz$ is assumed. The chosen capacitor has the following characteristics:

- capacitor Part Number: PCM1J120MCL1GS;
- $V_{C_{out},max} = 63V$;
- $C_{out} = 12\mu F$;
- $R_{esr} = 51m\Omega$.

Relation [Eq: 3.33] calculates the rms value of the capacitor current, $I_{C_{out},rms} = 1.6mA$, that is used to compute the power dissipated, $P_{diss} = 0.1\mu W$, in [Eq: 3.21].

Diodes The Graetz bridge's diode designs are all realizable at once because they all follow the same relationships and outcomes. The breakdown voltage is computed in relation [Eq: 3.46], and imposing $V_{in} = 12V$ as worst-case.

$$BV > \frac{V_{in}}{2}\frac{N_s}{N_p} = 150V \tag{3.46}$$

The absence of spike content in relation [Eq: 3.46] is noteworthy; this is because the Graetz bridge was built to be immune to spikes.
The average current is computed in relation [Eq: 3.47].

$$I_{diode,average} = \frac{I_{out}}{2} = 240mA \tag{3.47}$$

The market offered a bridge diode structure to reduce parasitics:

- bridge Part Number: B380S2A-SLIM;
- $V_f = 950mV$;
- $BV = 800V$;
- $I_{diode,max} = 2.3A$.

The power dissipated by all diodes can be computed by relation [Eq: 3.48].

$$P_{diode,TOT} = 2 \cdot V_f \cdot I_{diode,average} = 456mW \tag{3.48}$$

Transformer Its design is required because there isn't a suitable transformer available on the market. Once more, the reference design in [4] serves as the basis.
Toroidal is the chosen core shape, and 75 is the chosen core material. Although this material may operate up to 100 kHz, figure [Fig: 3.4] suggests that it is being used effectively.
Relationships [Eq: 3.5], [Eq: 3.6], and [Eq: 3.7] were repeated in order to identify the core. As a compromise for low power dissipated, the obtained magnetizing inductance is $2\mu H$, which is a relatively low value.
A satisfying magnetic core is established from the market. These features are the result of the design:

- toroidal core Part Number: 5975000321;
- $B_{max} = 480mT$;
- $P_{dissipata} = 214mW$;
- $N_p = 1$;
- $N_s = 25$;
- $L_m = 2\mu H$;
- $A_{w,p} < 8.168mm^2$;
- $A_{w,s} < 0.327mm^2$.

Transistors Since the two implemented transistors have the same analysis, only one will be designed here.

$$BV > Vin \cdot (1 + 30\%) = 15.6V \tag{3.49}$$

As is usual, the breakdown voltage, computed in [Eq: 3.49], has been increased by 30% and the computation considers $V_{in} = 12V$ as worst-case.
Relationships [Eq: 3.27], [Eq: 3.28], and [Eq: 3.41] lead the current computation, providing $I_{sw,max} = 12.1A$, $I_{sw,min} = 11.9A$, and $I_{sw,rms} = 7.45A$ accordingly, considering $D_s = 0.385$ as worst-case and relation [Eq: 3.11] is utilized to find $R_{on,HOT} = 8.2m\Omega$.
The selected transistor exhibits the following characteristics::

- transistor Part Number: ISC037N03L5ISATMA1;
- $BV = 30V$;
- $I_{sw,max} = 78A$;
- $R_{on,COLD} = 3.7m\Omega$;
- $Q_g = 17nC$.

The conduction power dissipation, $P_{cond} = 411mW$, is calculated using relation [Eq: 3.13], while the dynamic power dissipation is calculated using relation [Eq: 3.50].

$$P_{dyn} = \frac{f_b}{2} \cdot t_{rise} \cdot \left(\frac{V_{in}}{2} \cdot I_{sw,min} + \frac{V_{in}}{2} \cdot (1 + 30\%) \cdot I_{sw,max} \right) = 332mW \tag{3.50}$$

The two transistors' combined power dissipation is $1.486W$.

Capacitor branch Assessing the Thévenin equivalent circuit for the reference voltage is the first stage in the design process.

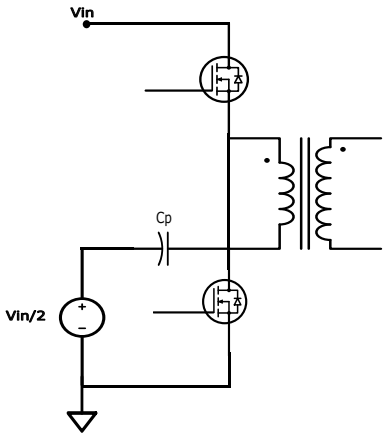

Figure 3.6: Thévenin equivalent circuit

The equivalent value Cp is the double of the single capacitance because both branch capacitors have the same value, which is what is needed to accurately cut the input voltage in half.
The capacitance value can be calculated using relation [Eq: 3.51] assuming the maximum ripple of the capacitor C_p voltage is $\Delta V_{C_p} = 300mV$.

$$C_p = \frac{I_{out} D_s}{f_s \Delta V_{C_p}} \cdot \frac{N_s}{N_p} = 338\mu F \tag{3.51}$$

The value of the single capacitor will be $194\mu F$.
In addition, a non-polarized capacitor is required due to the current's bidirectionality. Using capacitors with low parasitic resistances is also advised.
The chosen capacitors have the following characteristics:

- capacitor Part Number: JMK325ABJ337MM-P;
- $V_{C,max} = 6.3V$;
- $C = 330\mu F$.

Efficiency An efficiency of 0.913 is calculated using relation [Eq: 3.22] considering the total power dissipated is $2.184W$.

3.5 Push-Pull CCM

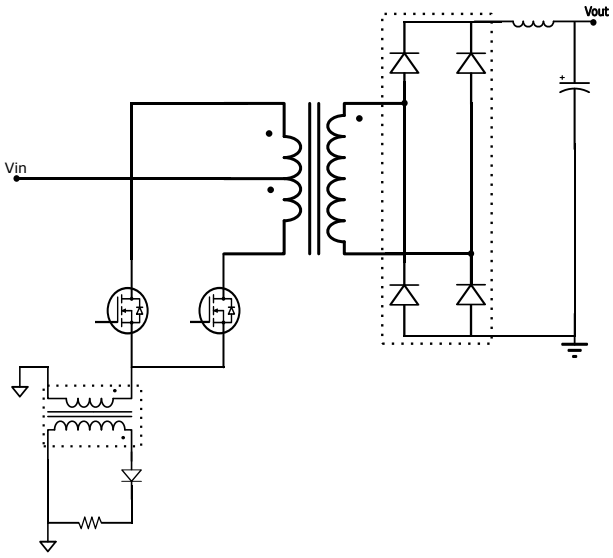

Figure 3.7: Push-Pull schematic

Description

Push-Pull is an isolated topology that is derived from Buck and, as previously mentioned, can easily be used in CCM operation in a straightforward manner.
The frequency doubling at the output is the circuit's primary feature in this configuration as well. Utilizing the majority of the cycle for power transfer is crucial, and this is made feasible by a negative voltage provided at the transformer. Thanks to the center tap at the primary that supplies the input voltage and the two transistors that alternately ground the other two terminals, the transformer primary can receive the negative voltage.
For the primary side, duty cycle and frequency values will be indicated by 's', and for the secondary side, by 'b'.
By design, a voltage control method is not practical, so the Push-Pull is the sole solution offered to adopt a current mode control. The reason for this lies in the proper transformer discharge, that is only possible with current control. The addition of a current sensor is necessary since the current control needs a means of detecting the inductor current. The primary side is the most commonly used location for adding it, as shown in [Fig: 3.7].
The rectifying block and the Buck characteristic output filter form the secondary side; the rectifying block can be either a center tapped or a Graetz bridge; in figure [Fig: 3.7], the Graetz bridge is utilized.

Project

For this project, the Graetz bridge onto the center tapped is selected in order to minimize the voltage drop across the secondary.
To move further with the project, a few assumptions are required:

- diode forward voltage: $V_f = 1V$;
- sensor maximum voltage $V_s = 1V$;
- secondary's ripple frequency: $f_b = 2MHz.$;
- duty cycle at the primary: $D_{s,max} = 0.45$;
- duty cycle at the secondary: $D_{b,max} = 0.90$.

The analysis continues by taking into account the output worst-case scenario:

- $V_{out} = 48V$;

- $R = R_{min} = 100\Omega$.

The elements' sizes in accordance with the chosen project flow come next.

Turn ratio The transformer is in charge of providing the secondary side with an appropriate voltage. To guarantee that the turn ratio is calculated accurately in relation [Eq: 3.52].

$$\frac{N_s}{N_p} = \frac{V_{out} + 2V_f}{(V_{in} - V_{on} - V_s)\, D_{b,max}} \cdot (1 + 5\%) = 14.9 \tag{3.52}$$

The chosen turn ratio is $\frac{N_s}{N_p} = 15$.
Using relation [Eq: 3.24], estimating the extreme values of the duty cycle is simple:

- $D_{b,5\to6} = 0.12$;
- $D_{b,12\to6} = 0.04$;
- $D_{b,5\to48} = 0.84$;
- $D_{b,12\to48} = 0.30$.

Inductor The inductor is in charge of maintaining the converter's operation in CCM. Relation [Eq: 3.44] is necessary for this, with a resulting minimum inductance needed of $1.75mH$ and worst-case represented by $D_b = 0.30$. An inductance of $3mH$ has been selected.
The inductor current ripple, $\Delta i_L = 5.6mA$, is obtained using relation [Eq: 3.45], with $D_b = 0.30$ as the worst-case scenario.
$I_{max} = 483mA$ and $I_{min} = 477mA$ were produced by taking advantage of relations [Eq: 3.27] and [Eq: 3.28]. Finally, the CCM operation is checked using relation [Eq: 3.29] is $120\mu A$, for $D_b = 0.04$ and $R_{load} = 10k\Omega$ as worst-case.
The selected inductor exhibits the following characteristics::

- Inductor Part Number: SC-01-30G;
- $L = 3mH$;
- $I_{l,average} = 1A$;
- $R_{esr} = 120m\Omega$.

Applying the small ripple approximation in relation [Eq: 3.30] and accounting for the parasitic resistance yields a dissipated power of $28mW$, which is calculated using [Eq: 3.31].

Output capacitor The maximum voltage drop of the capacitor can be determined using equation [Eq: 3.17], resulting in $48V$ at maximum.
As has been done, $R_{esr} < 1.78\Omega$ is calculated using relation [Eq: 3.32], $C_{out} = 9\mu F$ is estimated using relation [Eq: 3.19], and $f_{esr} = 10kHz$ is assumed. The chosen capacitor has the following characteristics:

- capacitor Part Number: PCM1J120MCL1GS;
- $V_{C_{out},max} = 63V$;
- $C_{out} = 12\mu F$;
- $R_{esr} = 51m\Omega$.

Relation [Eq: 3.33] calculates the rms value of the capacitor current, $I_{C_{out},rms} = 1.6mA$, that is used to compute the power dissipated, $P_{diss} = 0.1\mu W$, in [Eq: 3.21].

Diodes The Graetz bridge's diode designs are all realizable at once because they all follow the same relationships and outcomes.
Relation [Eq: 3.53] describes the breakdown voltage.

$$BV > Vin\frac{N_s}{N_p} = 180V \tag{3.53}$$

Again, it is significant that there is no spike content in relation [Eq: 3.53], as the Graetz bridge was designed to be spike-immune.
While the average current is calculated in relation [Eq: 3.47], the outcome is $I_{diode,average} = 240mA$.
A bridge diode construction was available on the market to reduce parasitics:

- bridge Part Number: B380S2A-SLIM;
- $V_f = 950mV$;
- $BV = 800V$;
- $I_{diode,max} = 2.3A$.

The power dissipated by all diodes can be computed by relation [Eq: 3.48], resulting in $456mW$.

Transformer Since there isn't a suitable transformer on the market, its design is necessary. Again, the foundation is the reference design in [4].
The selected core material is 75, and the selected core shape is toroidal. Figure [Fig: 3.4] indicates that this material is being used effectively despite the fact that it may operate up to 100 kHz.
The core was identified by repeating relationships [Eq: 3.5], [Eq: 3.6], and [Eq: 3.7]. A comparatively low magnetizing inductance of $2\mu H$ is attained as a compromise for low power dissipated.
A satisfying magnetic core is established from the market. These features are the result of the design:

- toroidal core Part Number: 5975000321;
- $B_{max} = 480mT$;
- $P_{dissipata} = 84.5mW$;
- $N_p = 1$;
- $N_s = 15$;
- $L_m = 2\mu H$;
- $A_{w,p} < 8.168mm^2$;
- $A_{w,s} < 0.327mm^2$.

Transistors Only one transistor will be developed here because the two implemented transistors have the same analysis.

$$BV > 2V_{in} \cdot (1 + 30\%) = 31.2V \tag{3.54}$$

The breakdown voltage, calculated in [Eq: 3.54], has been raised by 30% as is customary, and the calculation takes $V_{in} = 12V$ as the worst-case scenario.
The current computation is led by relationships [Eq: 3.27], [Eq: 3.28], and [Eq: 3.41], which yield $I_{sw,max} = 7.25A$, $I_{sw,min} = 7.16A$, and $I_{sw,rms} = 4.67A$, respectively, taking $D_s = 0.42$ as the worst-case, and using relation [Eq: 3.11] to find $R_{on,HOT} = 13.8m\Omega$. The selected transistor exhibits the following characteristics::

- transistor Part Number: ISK057N04LM6ATLA1;
- $BV = 40V$;
- $I_{sw,max} = 64A$;

- $R_{on,COLD} = 5.75m\Omega$;
- $Q_g = 4.7nC$.

The conduction power dissipation, $P_{cond} = 251mW$, is calculated using relation [Eq: 3.13], while the dynamic power dissipation is calculated using relation [Eq: 3.55].

$$P_{dyn} = \frac{f_b}{2} \cdot t_{rise} \cdot (V_{in} \cdot I_{sw,min} + V_{in} \cdot (1 + 30\%) \cdot I_{sw,max}) = 398mW \tag{3.55}$$

The two transistors' combined power dissipation is $1.3W$.

Current sensor The selected current sensor is resistive; however, a current transformer is employed to lower the dissipation of power, with CST4835-030E as the Part Number.
A 4.3Ω resistance is also implemented by that device in parallel to the output.
Relation [Eq: 3.56] describes the maximum current that the transformer can provide.

$$I_{sensing,max} = \frac{I_{sw,max}}{n} = 241mA \tag{3.56}$$

where n is the selected transformer's turn ratio, which is 30.
Relation [Eq: 3.57] calculates the sensor's observed equivalent resistance.

$$R_{sensing} < \frac{V_s}{I_{sensing,max}} = 4.15\Omega \tag{3.57}$$

It is helpful to add a parallel resistance with a value of 62, Part Number CCF0762R0GKE36, in order to maximize the sensor voltage swing and attain the ideal resistance value.
The calculation of the power dissipated in formula [Eq: 3.59] requires the sensing current's root mean square value, which is determined in formula [Eq: 3.58].

$$I_{sensing,rms} = I_{out} \cdot \frac{N_s}{N_p} \cdot \sqrt{D_b} = 220mA \tag{3.58}$$

$$P_s = R_{sensing} \cdot I^2_{sensing,rms} = 194mW \tag{3.59}$$

Efficiency Based on preliminary analysis, the overall power dissipation is $P_{diss} = 2.06W$, and the power given to the load is $P_{out} = 23.04W$. Relation [Eq: 3.22] calculates the efficiency and returns a value of 0.918.

3.6 Topology comparison

	Flyback	**Forward**	**Half-Bridge**	**Push-Pull**
Control mode	Voltage/Current	Voltage/Current	Voltage	Current
Conduction mode	DCM	CCM	CCM	CCM
Frequency at the secondary	$1MHz$	$1MHz$	$2MHz$	$2MHz$
Maximum load resistance	$\infty\Omega$	$10k\Omega$	$10k\Omega$	$10k\Omega$
Magnetizing inductance	$80nH$	$2\mu H$	$2\mu H$	$2\mu H$
Efficiency	94.4%	94.0%	91.3%	91.8%
Cost	3.24€	5.13€	12.4€	7.74€
Estimated volume	$12.3cm^3$	$7.6cm^3$	$5.8cm^3$	$5.7cm^3$

Important details regarding each suggested circuit are included in the previous table. It's important to compare these in order to make the correct choice. The explanation and discussion of each category come next.

Control mode Current control and voltage control are the two main control modes. Sensing the output quantity is the starting point of voltage control, which regulates the applied duty cycle to the converter using linear elements. This approach is less dissipative than the other and is very linear, which may help achieve the high accuracy specified. A current control method, on the other hand, is faster and useful for identifying overcurrents and other errors in the system. Its important non-linearity makes it less accurate, though, and typically a second simpler voltage control loop is added.

Conduction mode In steady-state conditions, the CCM has less fluctuations in inductor current, which reduces noise from electromagnetic coupling and electrical stress on the components. Since there is a crucial point at which the device transitions from CCM to DCM for low current values, the CCM controller must function by setting a maximum load resistance. Conversely, the DCM operation does not require a fixed maximum load resistance, hence the inductor current is always brought to zero, but it will produce significantly more electromagnetic noise.

Frequency at the secondary As seen with the Half-Bridge and Push-Pull arrangements, a higher frequency at the secondary aids the designer in easing the output filtering constraints. It also makes it feasible to create simpler control components and expand the system's frequency spectrum.

Maximum load resistance Because it determines the current going through the converter, the conduction mode has a strong relationship with the load resistance.

Magnetizing inductance Depending on the intended usage of the magnetic coupling, there are two ways to view the magnetizing inductance values. The inductance is a project parameter that needs to be established and developed with low typical values if the goal is energy storage. Instead, if power transfer is the aim, the magnetizing inductance is a parasitic effect of the transformer that either decreases the total power transmitted or, conversely, increases the input power.

Efficiency One of the most crucial circuit parameters is the efficiency parameter. It shows how effectively circuits are operating within the parameters that have been assigned.

Cost One of a designer's duties is to minimize the design's cost while respecting the specifications.

Estimated volume The device's level of integration into an actual complicated system is indicated by the volume. When a device is a component of a larger project, it should respect physical constraints.

3.7 Converter employed

When comparing the data in the previous section, the Flyback topology was picked primarily because it had no problems with low output current, was very efficient, and had an accessible design cost.

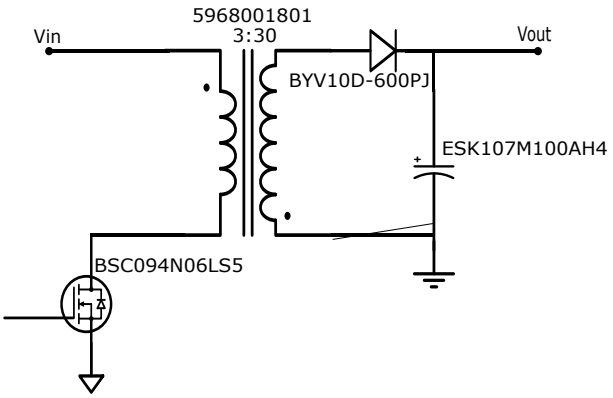

Figure 3.8: Flyback schematic

Due to problems observed during the simulation process, various modifications were made to the intended solution, as shown in figure [Fig: 3.8].

Output capacitor The ESK107M100AH4 is the last model utilized; it has a series parasitic resistance of $130m\Omega$ and a capacitance of only $100\mu F$. Given that there were no output ripple specifications, the capacitance value was not rigidly set and was instead adjusted to reduce the controller's overall complexity.

Transistor The transistor has been modified to BSC094N06LS5 in order to provide a larger safe margin for the drain-source voltage. However, the total efficiency is a little lower because this model dissipates slightly more than the previous one.

Coupled inductors One turn at the primary may not have been enough to provide an adequate coupling flux to the secondary for the magnetic element, and it may also have imposed a limit in the component's mechanical stability. In order to solve this, the coupled inductors were redesigned using the same methodology, resulting in a 5968001801 toroid, a $90nH$ magnetizing inductance, and a primary turn of 3. At the primary and secondary sides the wires' cross sections are categorized as $8AWG$ and $18AWG$, respectively.

3.8 Temperature analysis

In order to verify the idoniety of every component, a temperature analysis will be performed at the converter in this section. Assuming an initial ambient temperature of 50°C, the temperature rises by roughly 20°C at the junction of the devices.

Coupled inductors Figure [Fig: 3.9] shows the relationship between magnetic permeability and temperature sweep, as disclosed by the core producer, FIAR-RITE. As can be shown, the permeability is steady and consistent with the design value at 50°C.

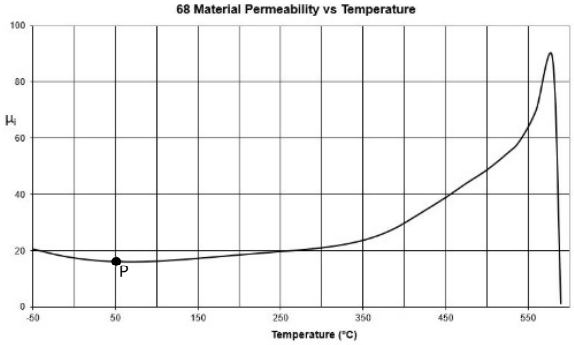

Figure 3.9: Relative permeability from FAIR-RITE

Transistor Figure [Fig: 3.10] illustrates how the transistor can withstand the estimated power dissipation at a junction temperature of 70°C. Instead, figure [Fig: 3.11] illustrates the relationship between temperature and the stated conduction resistance.

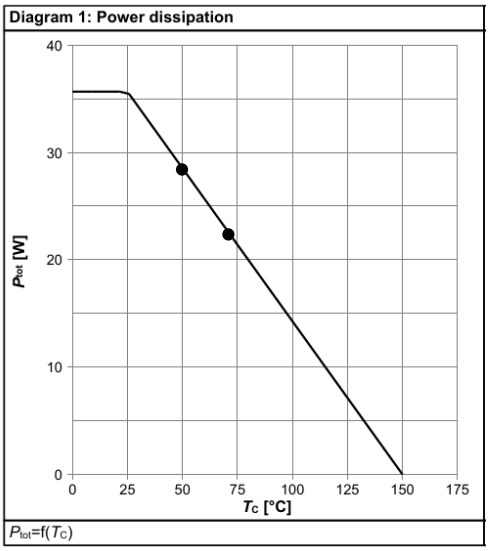

Figure 3.10: Total power dissipated vs Temperature

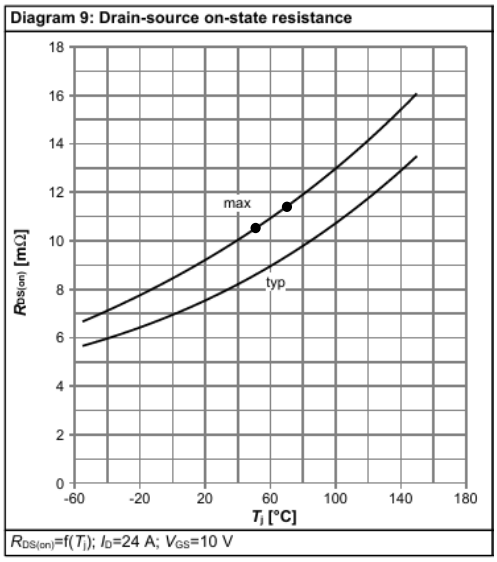

Figure 3.11: Conduction resistance vs Temperature

Diode Until the mounting base temperature reaches 157°C, the diode will continue to operate correctly, as shown in [Fig: 3.12]

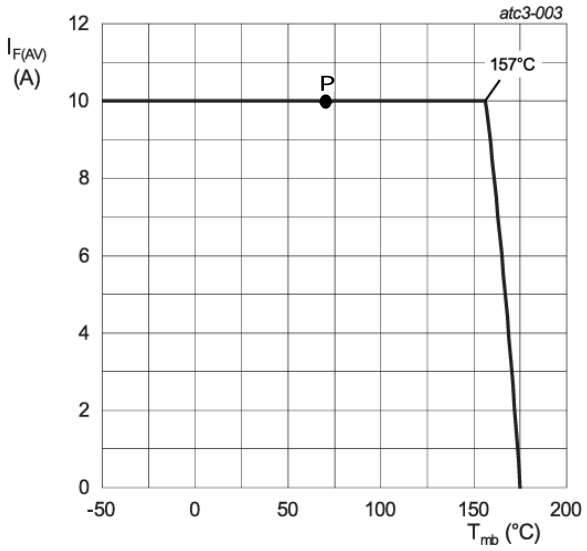

Figure 3.12: Forward current vs Temperature

Output capacitor Until the ambient temperature reaches 85°C, the manufacturer guarantees the proper operation.

Heatsink The following average power was determined in the worst-case scenario from a first circuit simulation:

- BSC094N06LS5: $P = 3.069W$;
- BYV10D-600PJ: $P = 854mW$.

According to the manufacturers, the junction-ambient state thermal resistances were:

- BSC094N06LS5: $\Theta_{j-a} = 50\frac{^\circ C}{W}$;
- BYV10D-600PJ: $\Theta_{j-a} = 60\frac{^\circ C}{W}$.

$$T_j = P \cdot (\Theta_{j-c} + \Theta_{c-h} + \Theta_{h-a}) + T_a. \tag{3.60}$$

The two active devices' junction temperature rises in accordance with equation [Eq: 3.60], where all of the thermal resistances collapse into Θ_{j-a} if it is applied. The calculation produces:

- BSC094N06LS5: $T_j = 203.5°C$;
- BYV10D-600PJ: $T_j = 101.2°C$.

The two fund junction temperatures are far higher than the $70C$ limit that has been set. Moreover, transistor one surpasses the manufacturer's maximum rating. The result of this analysis indicates that a heatsink should be added to their thermal circuit, to reduce the junction temperatures. The following list contains the junction-case resistances as reported by the manufacturer:

- BSC094N06LS5: $\Theta_{j-c} = 3.5\frac{^\circ C}{W}$;
- BYV10D-600PJ: $\Theta_{j-c} = 2.4\frac{^\circ C}{W}$.

It is feasible to calculate the required thermal resistance case-ambient by inverting [Eq: 3.60].

- BSC094N06LS5: $\Theta_{c-a} < 3\frac{^\circ C}{W}$;
- BYV10D-600PJ: $\Theta_{c-a} < 21\frac{^\circ C}{W}$.

3.9 Snubber circuit

The converter's simulations revealed on the primary side some current oscillations and spikes close to the switching sites. They are brought on by the coupling between the transistor's output capacitance and the magnetizing inductance. According to paper [13], these factors may interfere with the proper system's functionality. To reduce current spikes and damp oscillations, an RC snubber was installed in parallel with the transistor; its design was carried out according to the paper's step-by-step instructions of the scattering inductance method.
The resulting snubber is made up of:

- $R = 820m\Omega$;
- $C = 2.2nF$.

It has a pole placed at about $88MHz$, so it will be inert at the switching frequency. Figures [Fig: 3.13] and [Fig: 3.14] show the difference in the transistor's current, before and after the snubber addition.

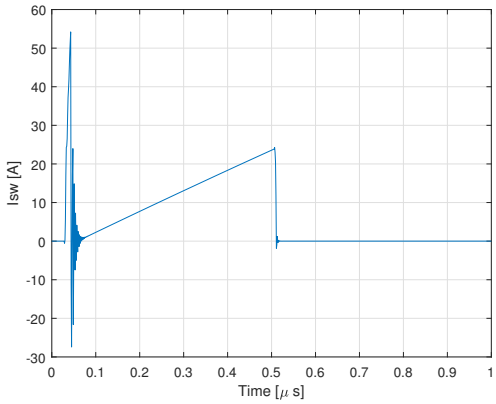

Figure 3.13: Without snubber

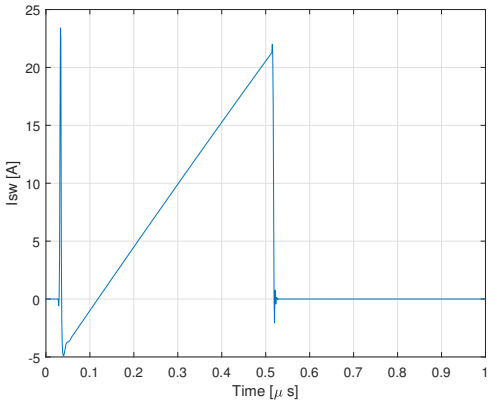

Figure 3.14: With snubber

The components' Part Number:

- R: MFLA1206R8200FS;
- C: 06035C222K4T2A.

3.10 Control loop

Because of its linearity and reduced dissipation, a voltage control approach was chosen over a current control. Despite being slower than the other one, the switching frequency chosen was sufficient to maintain the required settling time.

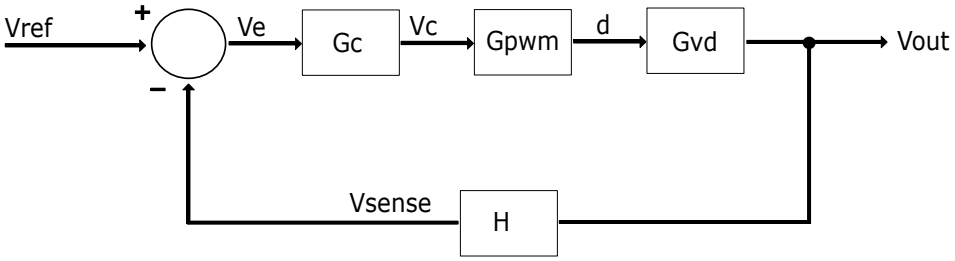

Figure 3.15: Control loop block diagram

Figure [Fig 3.15] displays the voltage control block diagram, which is composed of the following blocks.

- Converter, G_{vd}: it is identified by a transfer function that describes its behavior in terms of frequency.
- Sensor, H: using the sensor, the output quantity is measured and its magnitude is rescaled to a voltage level that is more compatible with the control circuit, V_{sense}.
- Compensator, G_c: its essential function is to determine the error voltage, V_e, and supply the subsequent block with a useful control voltage, V_c. It is also accountable for the output's steady-state error and system stability.
- Pulse width modulator, G_{pwm}: it generates a square wave signal with a useful duty-cycle, d, that will drive the converter's transistor by comparing the control voltage with a reference signal,in this case a saw-tooth wave.

The system's input is V_{ref}, the reference voltage.
Anticipating values before beginning the control design is helpful for a clearer understanding:

- $V_{ref,max} = 3.2V$;
- $\hat{V_{tri}} = 6.6V$;
- $G_{pwm} = \frac{1}{\hat{V_{tri}}} = \frac{1}{6.6V}$.

The final value theorem, which expresses the relationship expressed in [Eq: 3.61], is one theorem that will be extensively utilized in the control design. Its derivation can be found in the handbook [8].

$$\lim_{t->\infty} f(t) = \lim_{s->0} s \cdot F(s) \tag{3.61}$$

3.11 Converter

The DC-DC converter is a non-linear device by design; therefore, a linearization technique is used given that the control loop requires all of its elements to be linear.
Relation [Eq: 3.62] displays the control-to-output transfer function that was generated using the same linearization as in Paper [5].

$$G_{vd}(s) = G_{vd0} \cdot \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}} \tag{3.62}$$

Three components define the function: a DC gain, a pole and a zero. According to relations [Eq: 3.63], [Eq: 3.64], and [Eq: 3.65], respectively.

$$G_{vd0} = V_{in} \cdot \sqrt{\frac{R_{load}}{2L_m f_s}} \tag{3.63}$$

$$f_p = \frac{1}{2\pi C_o \frac{R_{load}}{2}} \tag{3.64}$$

$$f_z = \frac{1}{2\pi C_o ESR_{C_o}} \tag{3.65}$$

An important aspect can be identified by looking at the composition of the transfer function. The converter's operation is the reason for the relation's absence of inductance; it is not a random occurrence. It operates in DCM, which means that no energy is stored in the inductor at the end of the cycle because it will be completely discharged. This results in the frequency behavior showing no inductance.
The transfer function's worst-case scenario is established by:

- $V_{in} = 12V$;
- $R_{load} = 100\Omega$.

Under this scenario, the open loop gain's cutoff frequency is moved to its maximum value.

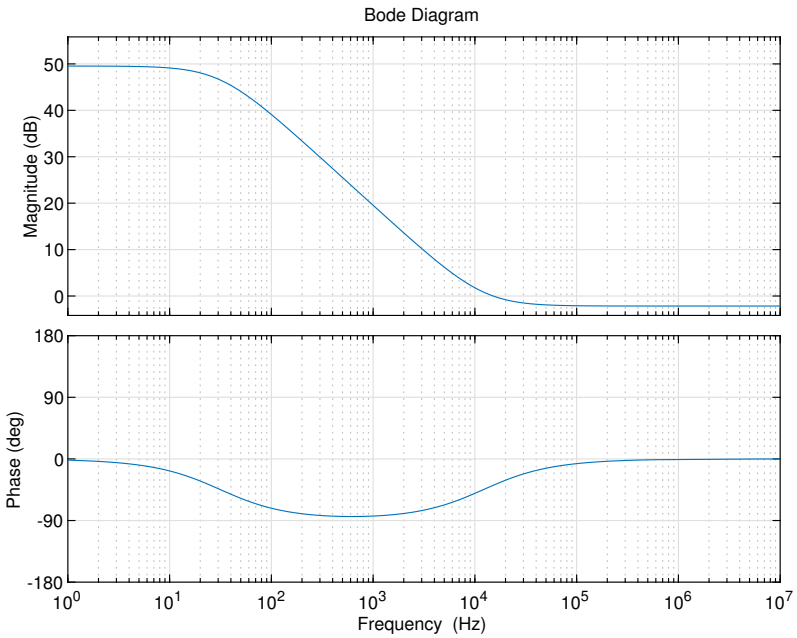

Figure 3.16: Transfer function of G_{vd}

The magnitude and phase of the resulting transfer function are displayed in Figure [Fig: 3.16]. The three components have been calculated here:

- $G_{vd0} = 300V$;
- $|f_p| = 31.8Hz$;
- $|f_z| = 12.2kHz$.

3.12 Sensor

The chosen sensor is resistive, and it works by using a voltage partition to rescale the output voltage level to the reference voltage levels. Figure [Fig: 3.17] shows a representation of the sensor scheme and relation [Eq: 3.66] computes the sensor's transfer function.

$$H(s) = \frac{R_{s2}}{R_{s1} + R_{s2}} \cdot \frac{1}{1 + sR_{s2}C_s} \tag{3.66}$$

The transfer function can be divided into two contributions:

- $H(0) = H_0$:

$$H_0 = \frac{R_{s2}}{R_{s1} + R_{s2}} \tag{3.67}$$

- $f_{p,s}$:

$$f_{p,s} = \frac{1}{2\pi R_{s2}C_s} \tag{3.68}$$

Since the voltage rescale is caused by the DC value of $H(s)$, its value must ensure relation [Eq: 3.69].

$$V_{sense,max} = H_0 \cdot V_{out,max} < V_{ref,max} \tag{3.69}$$

For the maximum output voltage, the previously stated relationship ensures that the sensed voltage does not above the maximum reference voltage.
The DC gain was determined to be $H(0) = \frac{1}{15}$. In addition to adhering to requirement [Eq: 3.69], this specific ratio facilitates the market's resistance search.
The resistance values that have been proposed are:

- $R_{s1} = 14k\Omega$;

- $R_{s2} = 1k\Omega$.

In addition to considering the desired DC gain of the transfer function, this value selection also considers the converter's output's minimum equivalent resistance, which is calculated in [Eq: 3.70].

$$R_{out,eq} = R_{out,min} || \left(R_{s1} + R_{s2}\right) = 99.34\Omega \tag{3.70}$$

The comparable output resistance tends to be $15k\Omega$ when an infinite load resistance is applied.
Since the accuracy requirement is focused on the average error, the pole is used to filter out the DC value of the output voltage. The pole is positioned at $1kHz$ for a suitable filtering action because the main AC component of the output voltage is at the switching frequency, $1MHz$. Equation [Eq: 3.68] is inverted to calculate the capacitor C_s value, which comes out to be about $160nF$.
The sensor's frequency behavior is well-established after the capacitor value selection, as seen by its bode plot in figure [Fig: 3.18].
The presence of an operation amplifier is the final component in figure [Fig: 3.17] to be discussed. The compensator's absorption of current at the V_{sense} terminal will change the current flow in resistance R_{s1}, which will modify the voltage partition and introduce an error at the sensor's output. In order to create an impedance detachment between the sensor and the compensator, the chosen method involves adding an operating amplifier that is connected in voltage follower configuration.

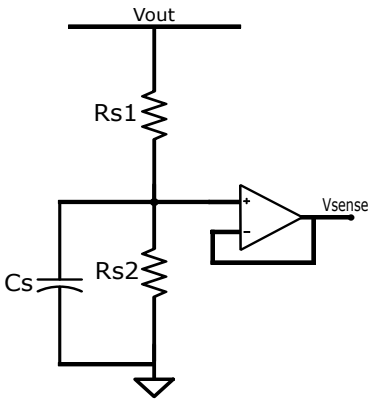

Figure 3.17: Sensor's schematic

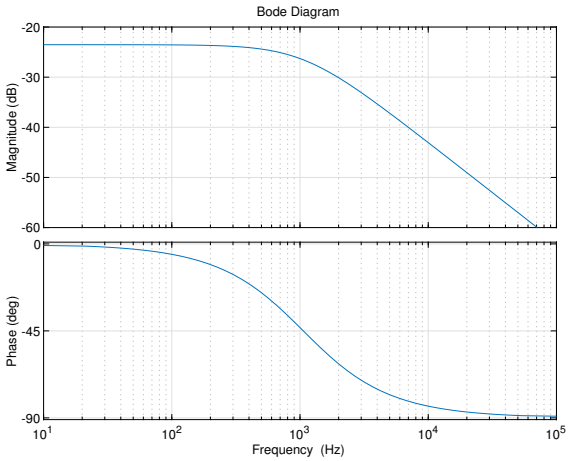

Figure 3.18: Transfer function $H(s)$

Calculating the desired resistance tolerance that permits the appropriate output precision is an additional step that is required.
Relation [Eq: 3.71] is achieved at the output if the final value theorem, equation [Eq: 3.61], is applied.

$$v_{out}(\infty) = \frac{V_{ref}}{H(0)} \frac{T(0)}{1+T(0)} \tag{3.71}$$

Given an extremely high open loop DC gain, the preceding relationship can be reduced to [Eq: 3.72].

$$v_{out}(\infty) \approx \frac{V_{ref}}{H(0)} = \frac{R_{s1}+R_{s2}}{R_{s2}} \cdot V_{ref} \tag{3.72}$$

In relation [Eq: 3.73], which calculates the error propagation into the output voltage, only errors caused by the resistors are included for simplicity's sake.

$$\Delta V_{out} = \sqrt{\left(\frac{\partial V_{out}}{\partial R_{s1}} \cdot \Delta R_{s1}\right)^2 + \left(\frac{\partial V_{out}}{\partial R_{s2}} \cdot \Delta R_{s2}\right)^2} < 1mV \tag{3.73}$$

The following outcomes were obtained from the single partial derivatives:

- $\frac{\partial V_{out}}{\partial R_{s1}} = \frac{V_{ref}}{R_{s2}}$;
- $\frac{\partial V_{out}}{\partial R_{s2}} = -\frac{R_{s1}}{R_{s2}^2} \cdot V_{ref}$.

The tolerances of the resistors are taken to be identical in order to make the calculation easier to perform. [Eq: 3.74] calculates the necessary tolerance of the resistors.

$$\delta R < \frac{\Delta V_{out}}{\sqrt{\left(\frac{V_{ref}}{R_{s2}} \cdot R_{s1}\right)^2 + \left(-\frac{R_{s1}}{R_{s2}} \cdot V_{ref}\right)^2}} = 1.57 \cdot 10^{-5} \tag{3.74}$$

The tolerance value is determined by applying the worst-case scenario, in which the maximum output voltage is supplied, and so $V_{ref} = 3.2V$.
The solution is impractical due to this stringent requirement, however a potentiometer can be inserted and adjusted to compensate for the tolerance's inaccuracy. This would also take into consideration other errors, like the voltage offset, that can come from the operation of the amplifier. The nominal value of the potentiometer is set at twice the R_{s2} value, so $2k\Omega$, and it connects as shown in figure [Fig: 3.19]. As seen in relation [Eq: 3.75], the potentiometer ratio can be derived if the DC value of $H(s)$ is taken to be fixed.

$$x = \frac{H(0)}{R_{s2}\left(R_{s1}+R_{s2}\right)} = 53.3\% \tag{3.75}$$

Although the result shows the ratio's nominal value, slight adjustments must be made to account for errors.
Instead of being connected in parallel to the potentiometer output, the capacitor is connected in parallel to R_{s2}, thus the pole is fixed. The pole is moved at about $500Hz$, as shown in figure [Fig: 3.20], because of this, assuming the capacitance value remains constant.

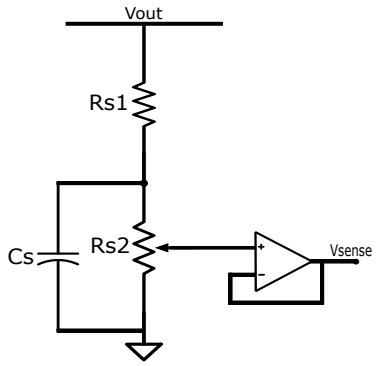

Figure 3.19: Sensor's schematic

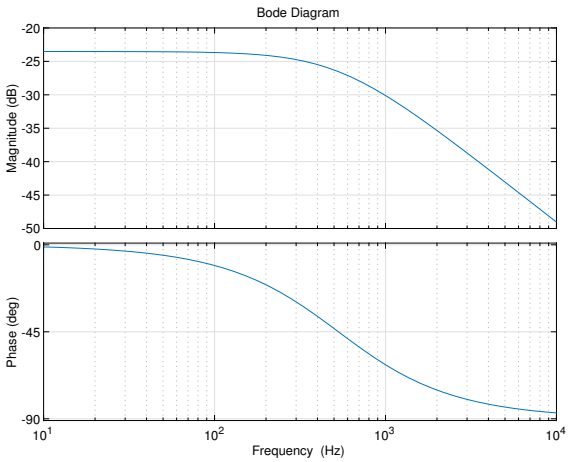

Figure 3.20: Transfer function $H(s)$

The components' Part Number:

- R_{s1}: ERJ-PB3B1402V;
- R_{s2}: PTN10-E02SB10;
- C_s: GRM155R71C154KA12D;
- Operational amplifier: MCP6487T-E/MS.

3.13 Compensator

The frequency behavior of the compensator includes poles and zero that compensate for the ones introduced by the rest of the system, as well as a high enough DC gain.
It is necessary to introduce the open loop transfer function, denoted as $T(s)$, which is the product of all the transfer functions within a system. The computation is based on the block diagram in [Fig: 3.15], and the defined product series is shown in [Eq: 3.76].

$$T(s) = G_c(s) \cdot G_{pwm}(s) \cdot G_{vd}(s) \cdot H(s) \tag{3.76}$$

It is vital to determine the shape of open loop transfer function that has to be reached before beginning the compensator design; equation [Eq: 3.77] points out the desired one in this project.

$$T(s) = \frac{1}{\frac{s}{2\pi f_c}} \tag{3.77}$$

The open loop's cutoff frequency is shown by the f_c term. It also specifies the function's DC gain.The open loop gain's cutoff frequency is shown by the wc word and it also specifies the function's DC gain. It's crucial to calculate an estimated value for the open loop gain in DC before providing any actual numbers, this is accomplished by examining the system's accuracy.
As shown in [Eq: 3.78], the output voltage's final value over time is calculated as the first step from relation [Eq: 3.61].

$$v_{out}(\infty) = \lim_{s \to 0} sV_{out}(s) \tag{3.78}$$

[Eq: 3.79] calculates the $V_{out}(s)$ straight from the block diagram shown in [Fig: 3.15].

$$V_{out}(s) = \frac{V_{ref}(s)}{H(s)} \frac{T(s)}{1+T(s)} \tag{3.79}$$

Relation [Eq: 3.80] results when [Eq: 3.79] is substituted in [Eq: 3.78].

$$v_{out}(\infty) = \lim_{s \to 0} \frac{sV_{ref}(s)}{H(s)} \frac{T(s)}{1+T(s)}. \tag{3.80}$$

When $v_{ref}(t)$ is applied as a step input, its frequency behavior will be $V_{ref}(s) = \frac{V_{ref}}{s}$, which causes equation [Eq: 3.80] to alter in equation [Eq: 3.81].

$$v_{out}(\infty) = \lim_{s \to 0} \frac{V_{ref}}{H(s)} \frac{T(s)}{1+T(s)}. \tag{3.81}$$

The open loop transfer function's DC gain should ideally tend to be infinite with respect to other magnitudes, but as [Eq: 3.77] suggests, it has a finite value, which introduces an error in the output. This output error can be calculated in relation [Eq: 3.82].

$$v_{out,err} = v(\infty, ideal) - v(\infty) = \frac{V_{ref}}{H(0)} \left(1 - \frac{T(0)}{1+T(0)}\right) \tag{3.82}$$

With $V_{ref} = 3.2V$ as the worst-case scenario, the required open loop DC gain to achieve an error below $1mV$ is roughly $94dB$.
Figure [Fig: 3.21] displays the suggested compensator structure, while Figure [Fig: 3.22] shows its transfer function.

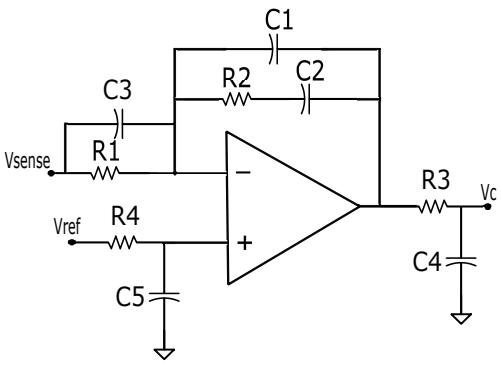

Figure 3.21: Compensator's schematic

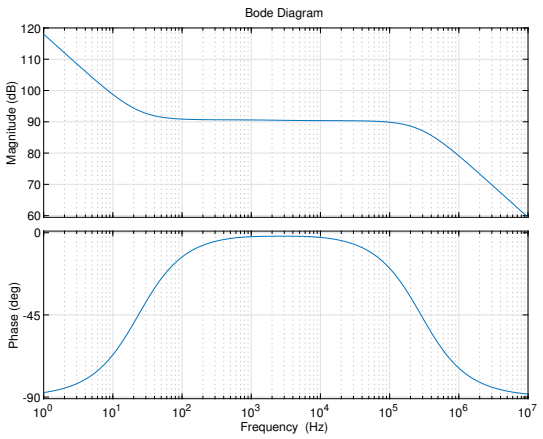

Figure 3.22: Transfer function G_c

The following relationships can be evaluated using a basic circuit analysis:

$$f_{p0,c} = 0Hz \tag{3.83}$$

$$f_{z_1,c} = \frac{1}{2\pi R_2 C_2} \tag{3.84}$$

$$f_{p_1,c} = \frac{1}{2\pi R_2 C_1} \tag{3.85}$$

$$f_{z_2,c} = \frac{1}{2\pi R_1 C_3} \tag{3.86}$$

$$f_{p_2,c} = \frac{1}{2\pi R_3 C_4} \tag{3.87}$$

$$|A| = \frac{R_2}{R_1} \tag{3.88}$$

Only when the $C_1 << C_2$ or C_3 condition applies, these relations can accurately reflect the behavior of the circuit.
For the sake of carrying out a zero-pole cancellation, the locations of the zeros and poles are selected to be:

- $f_{z_1,c} = f_p$;
- $f_{p_1,c} = f_z$;
- $f_{z_2,c} = f_{p,s}$.

Although the pole $f_{p_2,c}$ is not included in the compensation, it is crucial to add a negative slope to the transfer function in order to eliminate any high-frequency noise. The approximate frequency of this pole's implementation was $300kHz$.
The magnitude of the transfer function's plateaux is indicated by the value A and it can be evaluated by looking at the open loop. If $|A|$ is interpreted as $|G_c(f_{z_1,c})|$, the plateaux value in relation 1 can be obtained by inverting equation 1.

$$|A| = \left| \frac{T(f_{z_1,c})}{G_{vd}(f_{z_1,c}) G_{pwm}(f_{z_1,c}) \cdot H(f_{z_1,c})} \right| \tag{3.89}$$

It can be noticed that:

- $G_{vd}(f_{z_1,c}) = G_{vd}(f_p) = G_{vd0}$;
- $H(f_{z_1,c}) = H(0)$;
- $|T(f_{z_1,c})| = \frac{f_c}{f_{z_1,c}}$.

Relation [Eq: 3.89] is reduced to [Eq: 3.90].

$$|A| = \frac{f_c}{f_{z_1,c}} \cdot \frac{1}{G_{vd0} G_{pwm} H(0)}. \tag{3.90}$$

Two conditions were applied to the free selection of the cutoff frequency, f_c:

- f_c needs to be high enough to ensure that the open loop transfer function has a suitable DC gain;
- f_c should not cause the compensator's wind-up, when there is an error accumulation that saturates the output. This happens when the compensator's integration time is significantly longer than $\frac{1}{2\pi f_c}$.

Values for the design parameters were chosen by repeating the required equations ([Eq: 3.84], [Eq: 3.85], [Eq: 3.86], [Eq: 3.87], [Eq: 3.88] and [Eq: 3.90]) :

- $R_1 = 20\Omega$;
- $R_2 = 680k\Omega$;
- $R_3 = 1k\Omega$;
- $C_1 = 100pF$;
- $C_2 = 10nF$;
- $C_3 = 3.3uF$;

- $C_4 = 560pF$.

Figures [Fig: 3.23] and [Fig: 3.24] can be used to assess how well the zero-pole cancellation worked. The worst-case scenario fixed the single moving pole, which is essentially f_p.

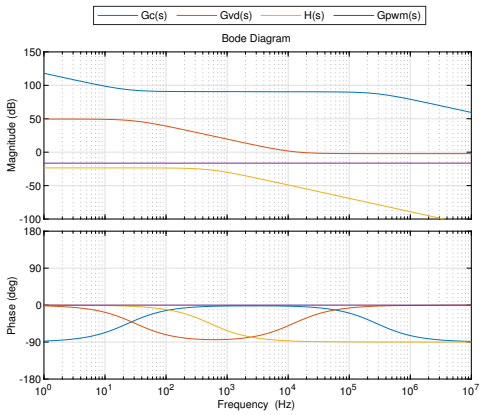

Figure 3.23: Control loop transfer functions

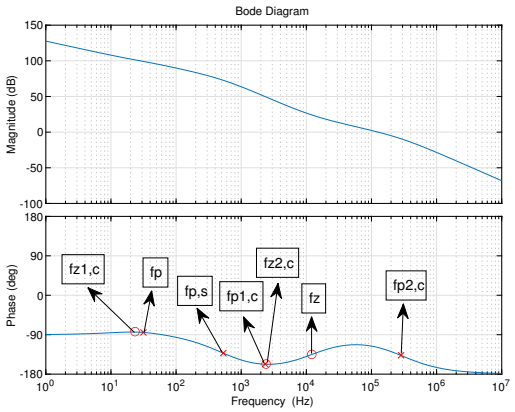

Figure 3.24: worst-case of transfer function of $T(s)$

Figure [Fig: 3.25] shows that changes in the input voltage and load resistance never cause the open loop transfer function to become unstable. Instead, [Fig: 3.26] illustrates that the phase margin obtained in the worst scenario is roughly 60°.

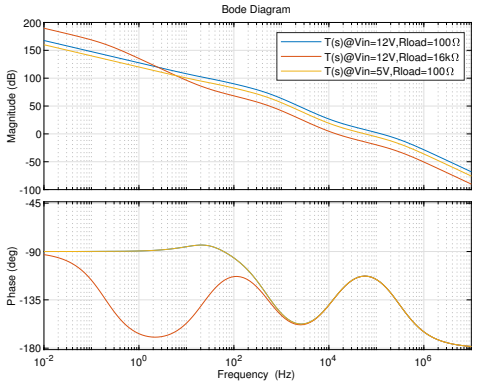

Figure 3.25: Transfer functions of $T(s)$

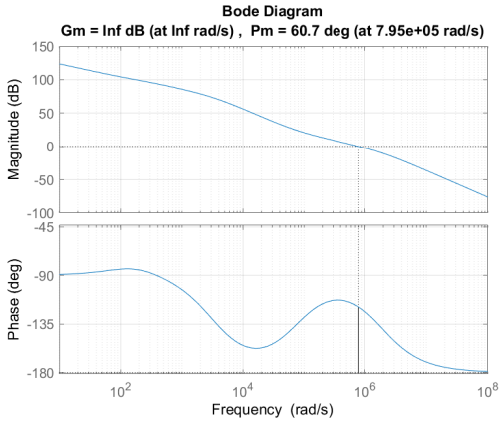

Figure 3.26: Margins of $T(s)$

The open loop transfer function's DC gain is always greater than what is needed.
Figures 1 and 2 illustrate the role of the RC filter introduced at the input V_{ref}, which is to compensate for the pole introduced by the sensor in the closed loop transfer function, A_f. It was therefore sized similarly to the RC filter that was discussed in the sensor section:

- $R_4 = 2k\Omega$;

- $C_5 = 150nF$.

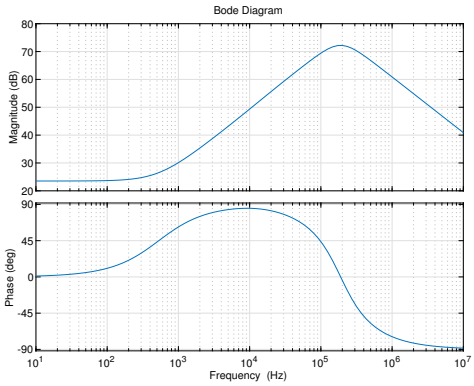

Figure 3.27: A_f without V_{ref} filter

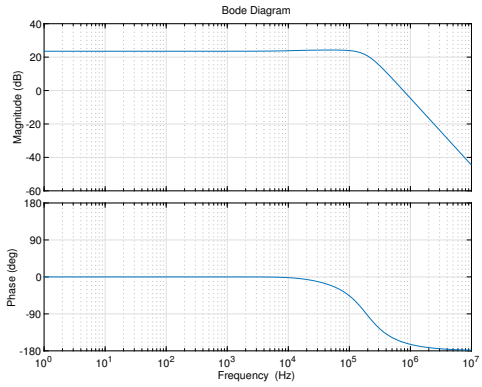

Figure 3.28: A_f without V_{ref} filter

When discussing the operational amplifier, its output voltage, V_c, needs to be kept within the range of $0V$ to $3.3V$, or half of the saw-tooth wave's peak value. This is because a larger duty-cycle is thought to shorten the discharging time, which would prevent the inductor from being completely discharged along with reaching magnetic core saturation. The device receives a single supply of $3.3V$ to apply the output saturation. Furthermore,the manufacturer recommends connecting a $100nF$ capacitor in parallel with the power supply.
The components' Part Number:

- R_1: AC0603JR-0720RL;
- R_2: RC0402FR-7W680KL;
- R_3: RT0805FRD071KL;
- R_4: ERA-6AEB202V;
- C_1: 885012007016;
- C_2: VJ0402Y103KXACW1BC;
- C_3: CL10A335KP8NNNC;
- C_4: C0603C561J5GACTU;
- C_5: GRM155R71C154KA12D;
- Operational amplifier: MCP6487T;
- C_{bypass}: MBAST105SB7104KFNA01.

3.14 Pulse width modulator

The pulse width modulator or PWM block is ideally made by a comparator, as shown in figure [Fig: 3.29].

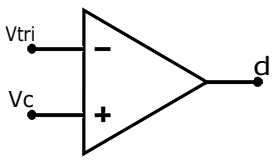

Figure 3.29: PWM schematic

This block's function is centered on comparing the compensator-generated control voltage to the saw-tooth wave reference signal, that produces a square signal which controls the converter's transistor.

Since the square wave's duty cycle varies in response to changes in the control voltage, these two parameters are related by the pwm transfer function.

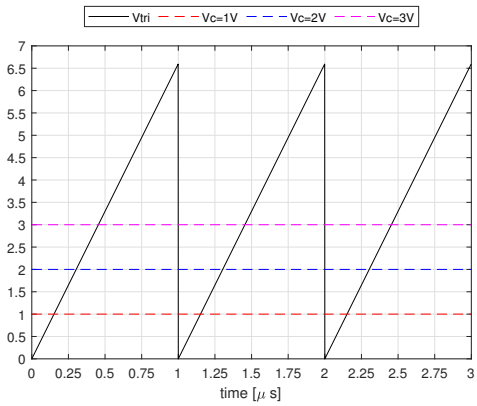

Figure 3.30: PWM input comparison

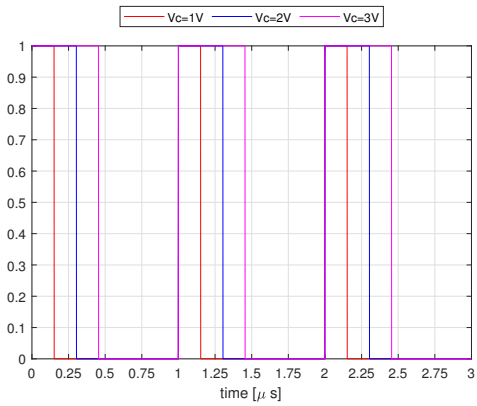

Figure 3.31: PWM output square wave

Figure [Fig: 3.30] and [Fig: 3.31] indicate the relationship between the inputs and the duty cycle of the output square wave. When the applied control voltage is lower than the peak value of the reference wave, the transfer function is linear and can be expressed by [Eq: 3.91].

$$G_{pwm} = \frac{d}{V_c} = \frac{1}{\hat{V_{tri}}} \tag{3.91}$$

Typically, only few steps are required for the PWM embedding:

- saw-tooth wave generation;
- comparator selection;
- gate-driver selection.

3.14.1 Saw-tooth wave generation

The reference saw-tooth signal is produced by the circuit shown in [Fig: 3.32].

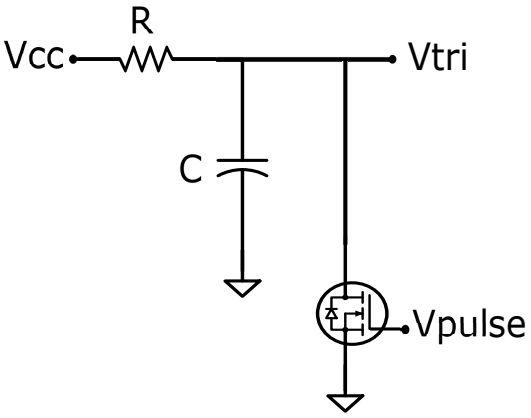

Figure 3.32: V_{tri} circuit generator

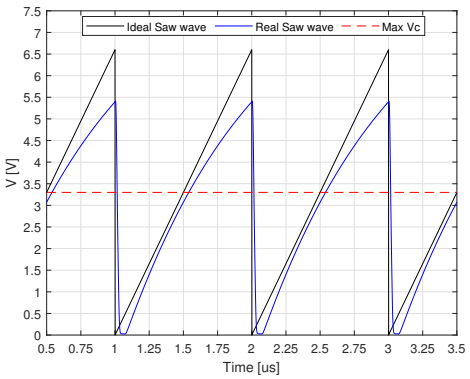

Figure 3.33: Forma d'onda a dente di sega

The core concept is to utilize the exponential charging of a capacitor for the rising section of the wave and a discharging transistor for the falling section. The exponential shape may introduce some linearity error into the system. However, since only the lower half of the waveform is taken into account, for magnetic core saturation issues, and the supply voltage is sufficiently higher than target one, $V_{cc} = 9V$, the exponential portion can be approximated as linear.
During the charging phase, the transistor is off, allowing charge to accumulate across the plates of

the capacitor. The circuit time constant just accounts for the values of the resistor and capacitor: $\tau = C \cdot R$. The capacitor voltage envelope in time can be described by [Eq: 3.92].

$$v_c(t) = [v_c(0) - v_c(\infty)]^{-\frac{t}{\tau}} + v_c(\infty) \tag{3.92}$$

Where the boundaries conditions are:

- $v_c(0) = 0V$;
- $v_c(\infty) = V_{cc}$.

The goal is to reach half of V_{tri} in no more than 500 ns, let's define $t_1 = 500ns$ and $v_c(t_1) = 3.3V$. By flipping equation [Eq: 3.92] into equation [Eq: 3.93] and calculating the value at t_1, the time constant evaluation is completed, resulting in $\tau = 1.1\mu s$.

$$\tau = -\frac{t}{ln\left(1 - \frac{v_c(t)}{v_c(\infty)}\right)} \tag{3.93}$$

Due to the two degrees of freedom of the time constant, the value of the capacitor is chosen arbitrarily. Choosing a number that is significantly greater than the transistor's parasitic drain-source capacitance is essential in order to make that one irrelevant, basically $C >> C_{ds}$.
The resistor of $R = 1k\Omega$ and the capacitor of $C = 1nF$ were chosen. With these values two main results of [Eq: 3.92] were computed:

- $v_c(t_1) = 3.54V$: higher than the imposed limit of $V_c \leq 3.3V$, meaning than the duty cycle will always to less than 0.5.
- $v_c(T_{sw}) = 5.69V$: this value is less than $\hat{V_{tri}}$, so the obtained wave is different from the wanted one, however, since the linearity is almost preserved and the duty-cycle is limited to 0.5, the raised problem can be consider meaningful.

The discharging phase, as anticipated, is controlled by the transistor which introduce a discharging path for the capacitor. The control signal, reported in [Fig: 3.35] ad [Fig: 3.34], is a pulse signal with period equal to T_{sw}, since f_{sw} is the wanted frequency of the converter.

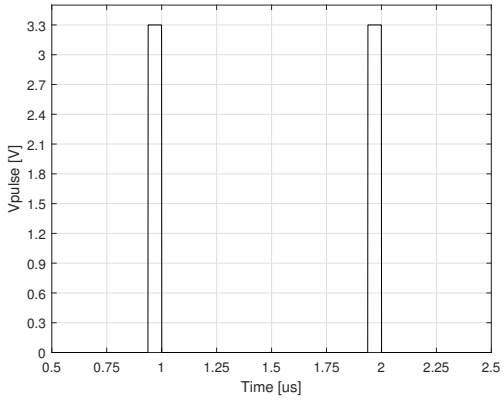

Figure 3.34: Pulse signal

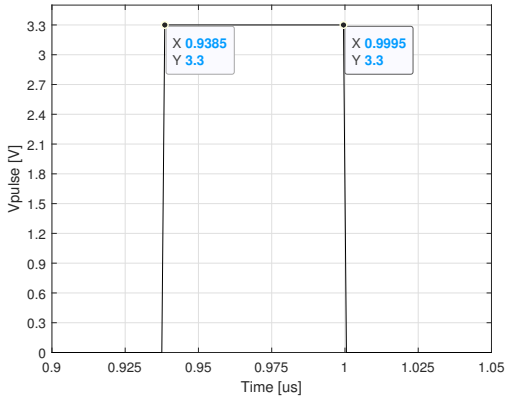

Figure 3.35: Pulse zoomed

The pulse signal is generated by NUCLEO-F334R8 from an internal timer triggered by a $72MHz$ clock . The on time interval was chosen to last about $70ns$, that are equivalent to $5T_{clk}$. The capacitor voltage at the start of the discharging phase is equal to the one at the end of the charging phase, here defined as: $v_c(0) = 5.69V$. In addition the new time constant is including the capacitance and the HOT resistance of the transistor: $\tau = C \cdot R_{on,HOT}$.
The time constant equation [Eq:3.94] can be evaluated again by inverting [Eq: 3.92].

$$\tau = -\frac{t}{ln\left(\frac{v_c(t)}{v_c(0)}\right)} \tag{3.94}$$

At the end of the discharging pulse, an extremely low voltage is desired. This is accomplished by performing the calculation for $v_c(t_1) = 10mV$ and $t_1 = 70ns$, which yields to $\tau = 11.03ns$ and from the time constant definition $R_{on,HOT} = 11.03\Omega$ is computed. Remember that the manufacturer of the transistor specifies the $R_{on,COLD}$.
The components' Part Number:

- R: RT0805FRD071KL;
- C: GRT1555C1H102FA02D;
- R_{gate}: CRCW1206330RFKEAC;
- Transistor: NX138AKHH.

3.14.2 Comparator selection

These kinds of applications require a comparator that can switch between two logic levels in a matter of nanoseconds. The chosen component's Part Number is: ADCMP553BRMZ. According to the manufacturer, the device is capable of high speed comparison, as seen in figure [Fig: 3.36].

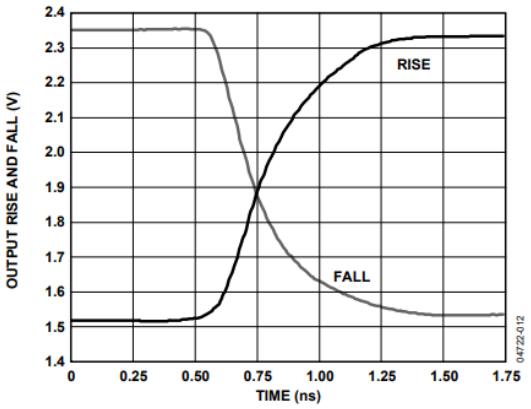

Figure 3.36: Rise and Fall of Outputs vs Time

Furthermore, the manufacturer recommends placing a $100nF$ bypass capacitor as close to the supply terminals as possible. The chosen capacitor has Part Number: MBAST105SB7104KFNA01.

3.14.3 Gate-driver selection

The gate-driver is another addition to the PWM block. In order to control a power transistor, a device that can provide or sink high current from its gate terminal is required. In this project, an isolated gate-driver is necessary since it places the isolation barrier of the control circuit.
Relation [Eq: 3.95] estimates the output current required for the transition.

$$|I_{out}| \geq \frac{t_{tran}}{Q_{g,tot}} = 4.5A \tag{3.95}$$

The stated total gate charge for the transistor is $Q_{g,tot} = 9nC$, and the transition time, $t_{tran} = 2ns$, is the one assumed in the converter chapter.
The chosen gate-driver withstands a current source and sink of $6.5A$ as stated, providing an input-output isolation voltage of $3750V_{rms}$.
Additionally, the supplier suggests using bypass capacitors, precisely two $100nF$ capacitors (C_1 and C_2) and two $10\mu F$ capacitors (C_3 and C_4).
The components' Part Number:

- isolated gate-driver: NCD57080ADR2G;
- $C_1 = C_2$: MBAST105SB7104KFNA01;
- $C_3 = C_4$: CL21A106KOQNNNE.

3.15 Output discharging

The approach adopted to discharge the output capacitor is purely resistive. It is intended to occur when there is a need to reduce the output voltage from a high value.
The dissipation circuit, shown in figure [Fig 3.37], is made by dissipation resistors and a transistor, that enables the discharging phase.

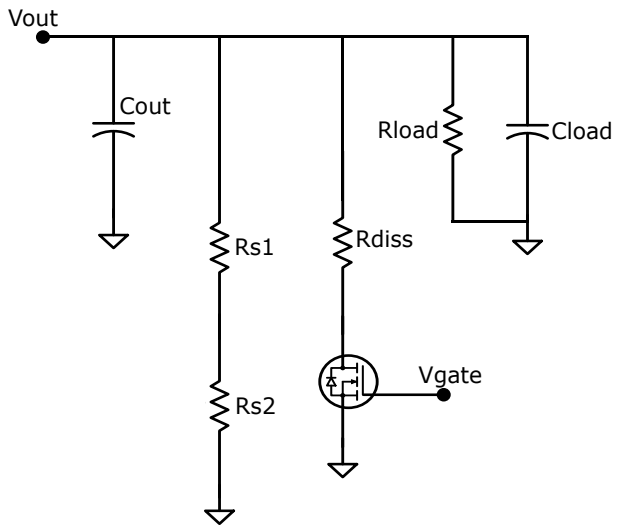

Figure 3.37: Equivalent circuit during output dissipation

According to the specifications, the discharging time should be less than $10ms$, which is the maximum settling time. To provide a safe margin, it was planned for the discharge phase to last no more than $t_1 = 9ms$.
The analysis's worst-case scenario was determined by:

- $v_c(0) = 48V$;
- $v_c(t_1) = 6V$;
- $R_{load} \to \infty$.

The equivalent circuit is made up of an RC equivalent after the transistor is conducting, thus it's critical to assess the equivalent quantities. It is done in relations [Eq: 3.96] and [Eq: 3.97].

$$C_{eq} = C_{out} + C_{load} \tag{3.96}$$

$$R_{eq} = (R_{s1} + R_{s2})||R_{diss} \tag{3.97}$$

Equation [Eq: 3.96] is quite simple to calculate, yielding $101\mu F$, however, for equation [Eq: 3.97], additional steps must be made. Since in the worst-case the load resistance tends to infinite, it is neglected from the operation, leaving as the unknown term the dissipation resistance that has to be inserted to comply the requirement.
Also in this case we are in a discharging phase with $v_c(\infty) = 0V$, so equation [Eq: 3.94] could be applied to compute the needed time constant, resulting in $4.33ms$ at $t = t_1$.
The needed equivalent resistance can be evaluated from the time constant, because it is determined by the two equivalent quantities, resulting in 42.9Ω. Finally looking at [Eq: 3.97], it can be observed that the equivalent resistance tends to R_{diss} because it is much lower than the sensor resistance $R_{s1} + R_{s2}$. 40Ω is the selected value for the dissipation resistance, which results in:

- $I_{diss,max} = 1.2A$;
- $\tau = 4.04ms$;
- $t_1 = 8.4ms$.

Four 10Ω ohm resistors were to be used to implement the dissipation resistance in order to ease power dissipation. The components' Part Number:

- $R_1 = R_2 = R_3 = R_4$: CMP2010AFX-10R0ELF;
- R_{gate}: CRCW1206330RFKEAC;
- transistor: SI2308CDS-T1-GE3.

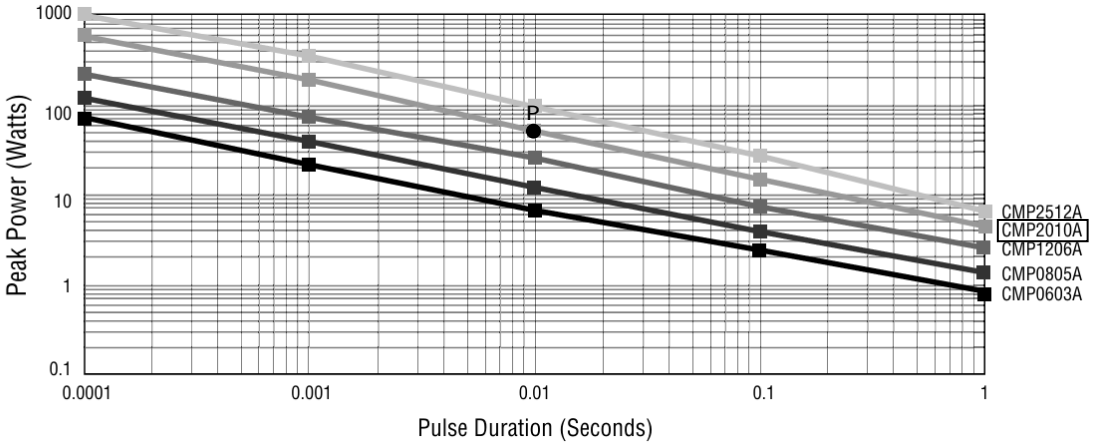

Figure 3.38: Power rating CMP-A series

At its highest, the total R_{diss} power dissipation is $57.6W$, while the power dissipated by a single resistor is $14.4W$. Looking at the power rating stated by the manufacturer [Fig: 3.38], each resistor can tolerate a power dissipation of $50W$ when taking into account the limit case of a constant power pulse, which does not occur here, with a duration of 10 ms.
The microcontroller uses the V_{gate} terminal to control the entire circuit. Its code should compare the real V_{ref} and V_{sense}, that the two ADCs embedded onto the nucleo sense in the system, and the verification of $V_{sense} > V_{ref}$ should trigger the discharge circuit. The discharging procedures may, however, start falsely as a result of this condition, a threshold term needs to be added in order to remedy this. A threshold of $30mV$ is added to the suggested system, resulting in a minimum output voltage voltage difference of $450mV$. The resistive branch of the sensor will dissipate the remaining output capacitor charge.

3.16 Overcurrent protection circuit

When the average output current exceeds the specifications' maximum for any reason, an overcurrent protection circuit is required. This current supply should be restricted to a safe area because it has the potential to harm the device in several ways. The implementation of the circuit is shown in figures [Fig: 3.39] and [Fig: 3.40].

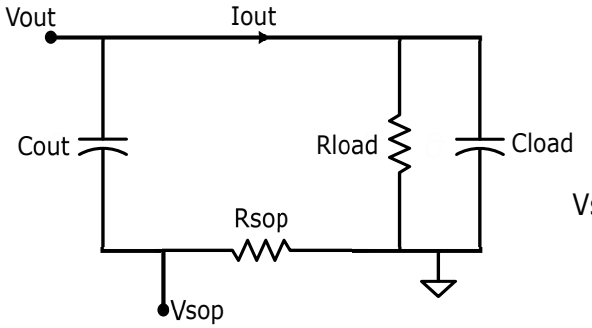

Figure 3.39: V_{sop} sensing

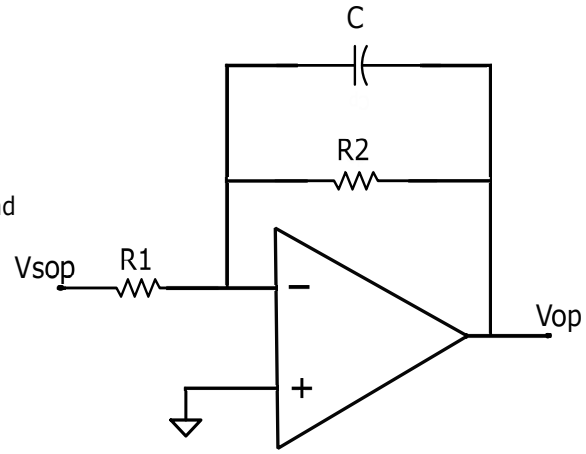

Figure 3.40: Overcurrent protection circuit

A resistance R_{sop} is added to assess the output current; in order to reduce power dissipation, its value should be insignificant when compared to the load resistance, for this reason it has been chosen a $10m\Omega$ resistor. The voltage that results is fed into an integrator, which filters the signal. Finally to determine whether to shut down the system, the microcontroller receives the output signal V_{op} as input. This is the concept that explains how the system operates.
The following factors were taken into consideration when designing the components:

- According to the reference guide, the threshold voltage for a microcontroller's GPIO input terminal is approximately $2.5V$.

- The maximum output current of $600mA$ is selected based on the converter's component.

- The main AC components of the output are switching frequency multiples.

A basic circuit analysis reveals transfer function [Eq: 3.98], which connects the output current I_{out} to V_{op}.

$$G_{op} = \frac{V_{op}}{I_{out}} = R_{sop}\frac{R_2}{R_1} \cdot \frac{1}{1 + R_2 C} \tag{3.98}$$

The analysis starts by assuming that the GPIO pin needs to read 2.5V when the output current is $600mA$. The resistor ratio can be calculated using equation [Eq: 3.98] if just the average values are taken into account, yielding 416.66.
The pole of the integrator, described by [Eq: 3.99], is introduced two decades prior to the switching frequency, in order to calculate the average of the signal while simultaneously providing a sharp response to overcurrents.

$$f_p = \frac{1}{2\pi R_2 C} = 10kHz \tag{3.99}$$

Given the premise that $C = 47pF$, the value of R_2 is $330k\Omega$, and as a consequence, $R_1 = 820\Omega$ is chosen. The frequency behavior and the DC operation are verified by [Fig: 3.41] and [Fig: 3.42] respectively.

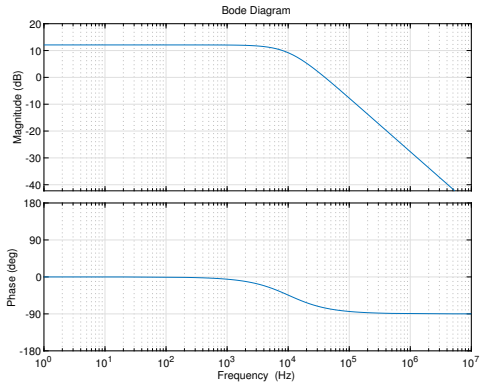

Figure 3.41: Bode diagram of $G_{op}(s)$

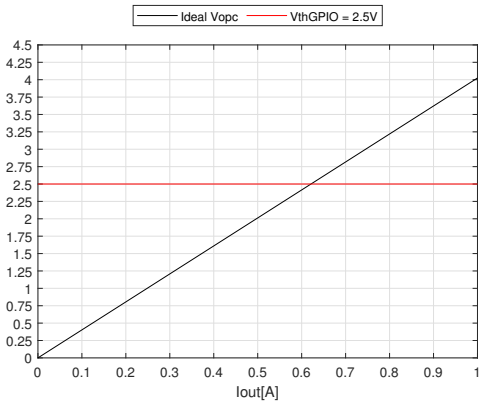

Figure 3.42: V_{op} and $V_{th,GPIO}$ vs I_{out}

The next step is to calculate the error brought on by the offset voltage of the op-amp and the tolerance of the resistors.
Equation [Eq: 3.100] is produced by using the final value theorem, [Eq: 3.61], at $v_{op}(t)$, with a step input of I_{out}.

$$v_{opc}(\infty) = (-I_{out}R_{op} + v_{offset}) \cdot \left(-\frac{R_2}{R_1}\right) \tag{3.100}$$

The error propagation is applied for all relevant variables in equation [Eq: 3.101].

$$\Delta v_{opc}^2 = \left(\frac{\partial v_{opc}}{\partial R_{sop}}\Delta R_{sop}\right)^2 + \left(\frac{\partial v_{opc}}{\partial v_{offset}}\Delta v_{offset}\right)^2 + \left(\frac{\partial v_{opc}}{\partial R_1}\Delta R_1\right)^2 + \left(\frac{\partial v_{opc}}{\partial R_2}\Delta R_2\right)^2 \tag{3.101}$$

Some intermediate results are evaluated here:

- $\frac{\partial v_{opc}}{\partial R_{sop}} = I_{out} \cdot \frac{R_2}{R_1} = 241A$;
- $\frac{\partial v_{opc}}{\partial v_{offset}} = -\frac{R_2}{R_1} = 402$;
- $\frac{\partial v_{opc}}{\partial R_1} = I_{out}R_{sop} \cdot \frac{R_2}{R_1^2} = 2.95mA$;
- $\frac{\partial v_{opc}}{\partial R_2} = I_{out}R_{sop} \cdot \frac{1}{R_1} = 7.32\mu A$.

Substituting the obtained results, [Eq: 3.101] is simplified into [Eq: 3.102].

$$\Delta v_{opc}^2 = (241A \cdot R_{sop}\delta R_{sop})^2 + (402 \cdot \Delta v_{offset})^2 + (2.95mA \cdot R_1\delta R_1)^2 + (7.32\mu A \cdot R_2\delta R_2)^2 \tag{3.102}$$

[Eq: 3.102] can be further simplified into [Eq: 3.103] considering the resistors' tolerance in common: $\delta R_1 = \delta R_2 = \delta R_{sop} = \delta R$.

$$\Delta v_{opc}^2 = (2.41A \cdot \delta R)^2 + (402 \cdot \Delta v_{offset})^2 + (2.41A \cdot \delta R)^2 + (2.41A \cdot \delta R)^2 \tag{3.103}$$

Assuming the resistors' tolerance to be 1% and a voltage offset of $1mV$ the maximum estimated error is $0.4V$, the error is mainly due to the offset of the op-amp. Figure [Fig:3.43] shows the input-output relation with the error addition.

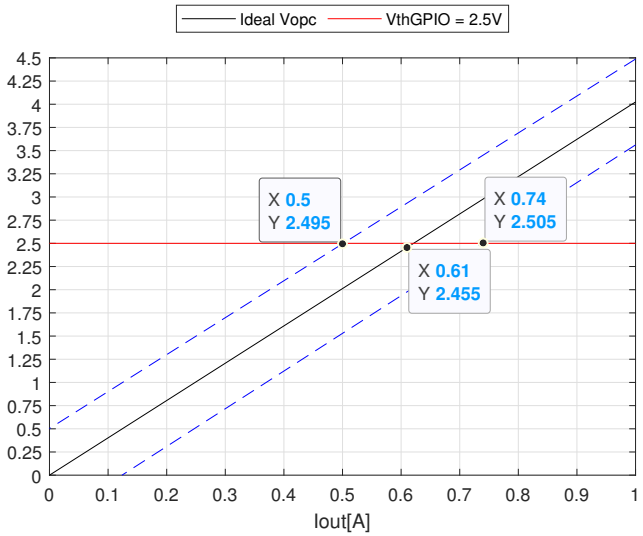

Figure 3.43: V_{op} and $V_{th,GPIO}$ vs I_{out} with error

The components' Part Number:

- R_{sop}: MFL0603R0100FA;
- R_1: RT0603FRE07820RL;
- R_2: MCT06030C3303FP500;
- C: GCM0335C1E470JA16D;
- Amplificatore operazionale: OPA323IDCKR;
- C_{bypass}: MBAST105SB7104KFNA01(100nF).

The code for the microcontroller should check the GPIO state and immediately fall to 0 of V_{ref} to stop the system from operating if an overcurrent is found.

3.17 Reference voltage generation

The microcontroller is in charge of providing the system's reference voltage, as was already mentioned. The voltage must be supplied via DAC in order to produce a variable output. The influence of the DAC's LSB must be less than $1mV$ in order to meet the accuracy requirement.
The microcontroller's reference manual [1] states that there can be no more than 12 bits available, and the maximum DAC voltage is $3.6V$. Equation [Eq: 3.104] uses these values to determine the amount of the LSB.

$$v_{LSB} = \frac{v_{DACmax}}{2^{nbit}} = 879\mu V \tag{3.104}$$

If the open loop gain is considered ideal, it is possible to derive [Eq: 3.105] from [Eq: 3.82].

$$v_{out,err} = \frac{v_{LSB}}{H(0)} = 13.18mV \tag{3.105}$$

From [Eq: 3.105] it can be seen that the number of bits available are not sufficient to stick to the requirement. By inverting the computation it is possible to compute the needed number of bits, which results in 16 bits.
A voltage modulation should be carried out in order to comply with the specified microcontroller type. The main idea is to average a square wave that is supplied by the DAC by using the RC filter that is inserted at the v_{ref} terminal. Given that the microcontroller's clock frequency is $72MHz$ and the filter's pole was positioned at roughly $500Hz$, $1MHz$ may be the potential modulation

frequency.

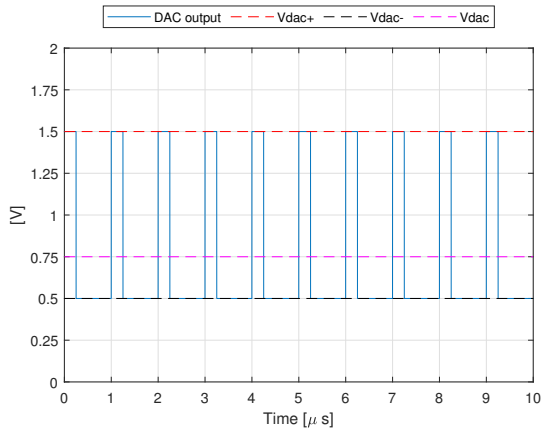

Figure 3.44: v_{DAC} example

Figure [Fig: 3.44] shown an example of the DAC output voltage, it is defined by two voltage levels and a duty-cycle: v_{DAC+}, v_{DAC-} and d.
Relation [Eq: 3.106] is used to compute the output voltage of the DAC, where D refers to its corresponding digital value.

$$v_{DAC} = \frac{v_{DACmax}}{2^{nbit} - 1} \cdot D \tag{3.106}$$

By inverting this equation it is possible to evaluate the digital value corresponding to the voltage to be generated, but because of the discretization, D should have only integer values. When a non-integer value is found two variables are defined: D_+ and D_- which corresponds to the round up or down of the found value. It is feasible to evaluate v_{DAC+} and v_{DAC-}, which refer for D_+ and D_- correspondingly, by using [Eq: 3.106].
The average value of the DAC output can be calculated using equation [Eq: 3.107], assuming an optimal filter averaging.

$$v_{DAC} = d \cdot (v_{DAC+} - v_{DAC-}) + v_{DAC-} \tag{3.107}$$

Since v_{DAC+}-v_{DAC-}=v_{LSB} by definition of D_+ and D_-, equation [Eq: 3.108] is deduced from [Eq: 3.107].

$$d = \frac{2^{nbit}}{2^{nbit} - 1} \cdot (D - D_-) \tag{3.108}$$

Lastly, the duty cycle can be roughly estimated as [Eq: 3.109] because the exponential term is significantly more than 1.

$$d \approx \tilde{d} = (D - D_-). \tag{3.109}$$

The new DAC average can be approximated to [Eq: 3.110].

$$v_{DAC} \approx v_{\tilde{DAC}} = v_{LSB} \cdot (D - D_-) + v_{DAC-}. \tag{3.110}$$

These approximations introduce errors in the output voltage, that could be higher than $1mV$.
Similarly to [Eq: 3.105], equation [Eq: 3.111] can be derived from [Eq: 3.82].

$$v_{out,err} = v_{out} - v_{\tilde{out}} = \frac{v_{DAC} - v_{\tilde{DAC}}}{H(0)} = \frac{v_{LSB}}{H(0)} \cdot \left(\frac{2^{nbit}}{2^{nbit} - 1} - 1 \right) \cdot (D - D_-) \tag{3.111}$$

Since $D - D_- < 1$, it is possible to compute the upper limit of the output error, that is $3.2\mu V$.
The duty-cycle generation should be given further consideration because discretization also takes place in this situation. For the on time t_{on} [Eq: 3.112] is true by construction

$$t_{on} = \tilde{d} \cdot T_{sw} = N \cdot T_{clk} \tag{3.112}$$

The proportionality constant between t_{on} and T_{clk} can be computed by inverting the relation above and, since it has to be integer it is rounded to the nearest side. This approximation introduces an error too, which in the worst-case is $\Delta N = 0.5$.
If the output error propagation is computed with respect to ΔN, it results to be $91.5\mu V$, which is much less than the requirement.
To keep low the computational cost it is advised to save a look-up table in the microcontroller's memory, with values of: D_-,D_+ and N associated to a V_{out} value. With an output voltage step of $50mV$ at the output the table dimensions would be: 961 x 3.

3.18 Supply of the control circuit

When developing an isolated DC-DC converter, one of the fundamental responsibilities is to supply the control circuits with an isolated supply voltage.
Typically, the control supply for a fixed output Flyback is constructed similarly to the one found in article [11], however this design is impractical for this project.
An auxiliary winding of the Flyback transformer is used in some other applications to produce a supply voltage. Because the auxiliary output varies linearly with the converter's major output, as equation [Eq: 3.113] shows , this method is not suitable for this design.

$$V_{aux} \approx \frac{N_{aux}}{N_s} \cdot V_{out}. \tag{3.113}$$

The supply voltage selected for the control is incompatible with the output range, or alternatively, it is impossible to define a turn ratio suitable for both secondaries.
For these reason the supply voltage is provided by an auxiliary DC-DC converter with Part Number TEC2-0919. It is supplied by the input and it provide a fixed voltage of $9V$, that is supplied to the gate driver, the saw-tooth generator and the nucleo. It is feasible to verify from [Fig: 3.45] that the converter voltage input range matches the one specified in the project specifications.

Models

Order Code	Input Voltage Range	Output 1 Vnom	Output 1 Imax	Output 2 Vnom	Output 2 Imax	Efficiency typ.
TEC 2-0910		3.3 VDC	500 mA			78 %
TEC 2-0911		5 VDC	400 mA			81 %
TEC 2-0919		9 VDC	222 mA			84 %
TEC 2-0912	4.5 - 13.2 VDC (9 VDC nom.)	12 VDC	167 mA			84 %
TEC 2-0913		15 VDC	134 mA			84 %
TEC 2-0915		24 VDC	83 mA			85 %
TEC 2-0921		+5 VDC	200 mA	−5 VDC	200 mA	81 %
TEC 2-0922		+12 VDC	83 mA	−12 VDC	83 mA	85 %
TEC 2-0923		+15 VDC	67 mA	−15 VDC	67 mA	84 %

Figure 3.45: TEC2-0919 model specifics

An additional linear voltage regulator with Part Number AP2205-33Y-13 is added to supply all the op-amps and the comparator with a $3.3V$.

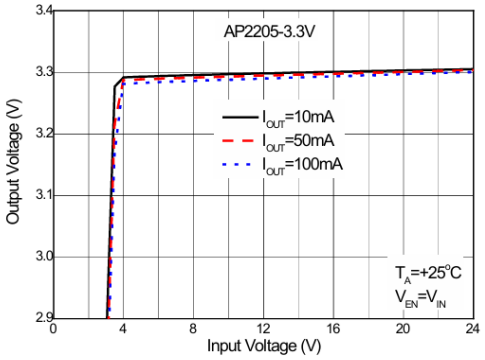

Figure 3.46: AP2205-33Y-13: V_{out} vs V_{in}

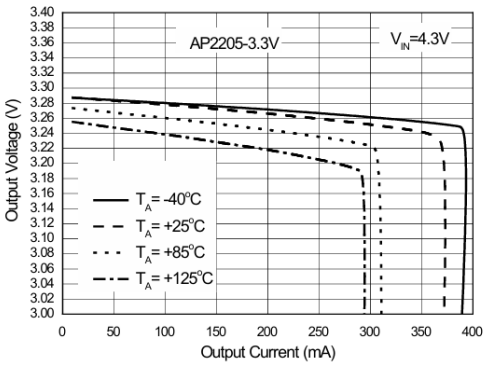

Figure 3.47: AP2205-33Y-13: V_{out} vs I_{out}

Figure [Fig: 3.46] shows that the device's input range is wide, including its input voltage, which is $9V$ net. Furthermore, the device can handle the predicted maximum load current of about $20.5mA$, as shown in [Fig: 3.47].

3.19 Full schematic

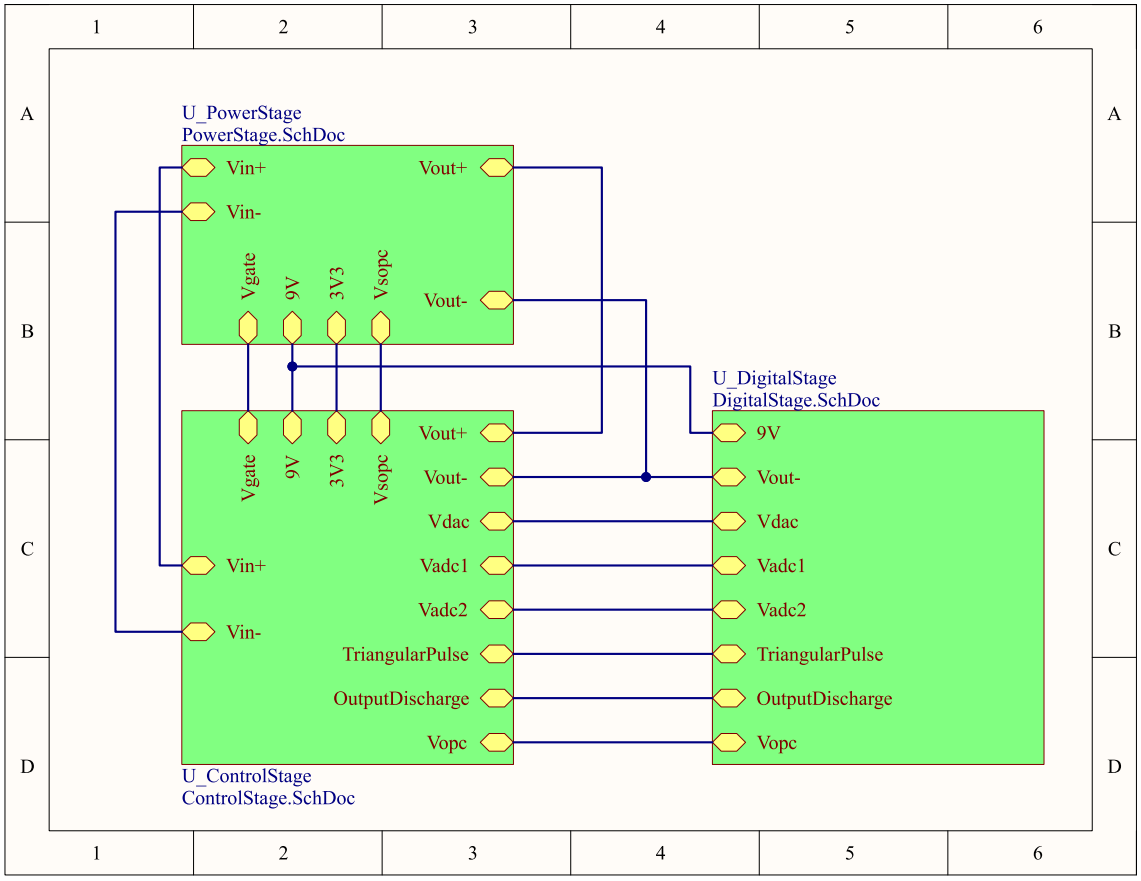

Figure 3.48: Schematic of the complete system

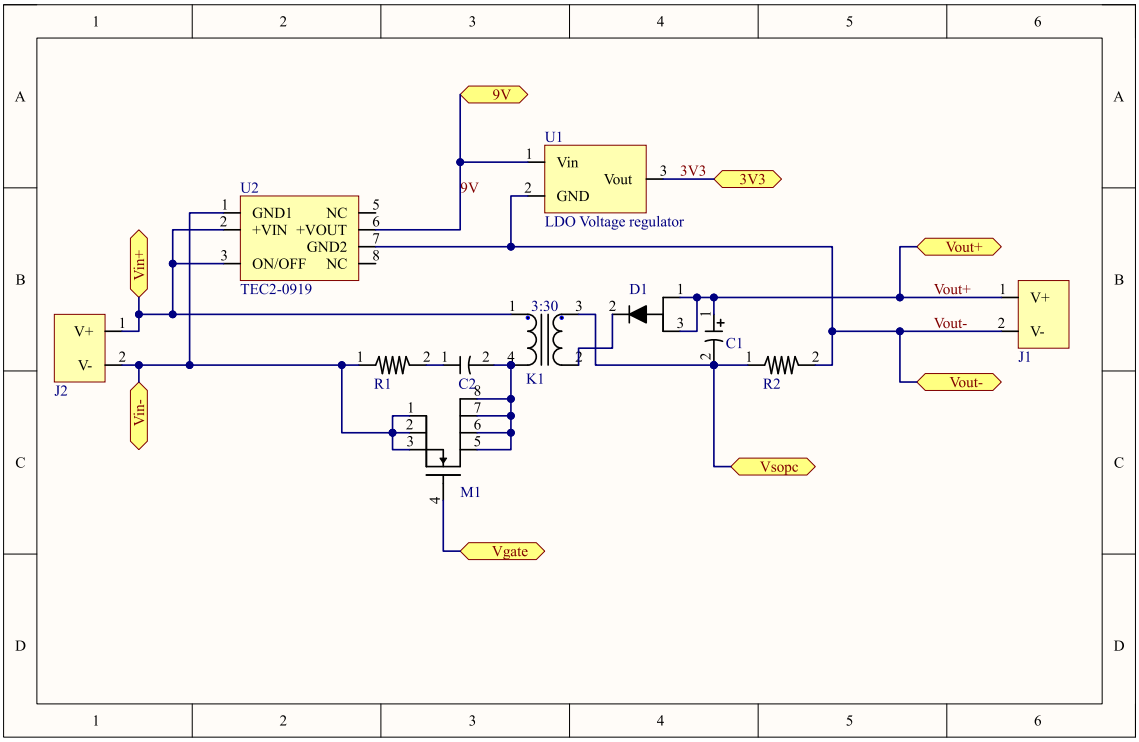

Figure 3.49: Power stage

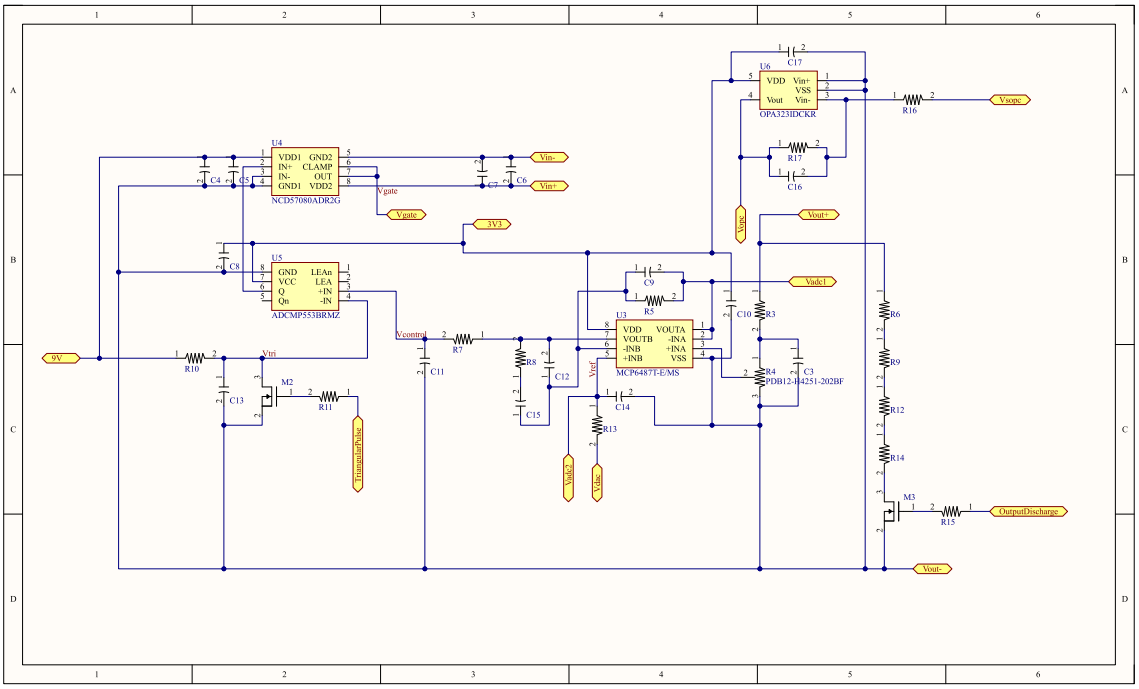

Figure 3.50: Control stage

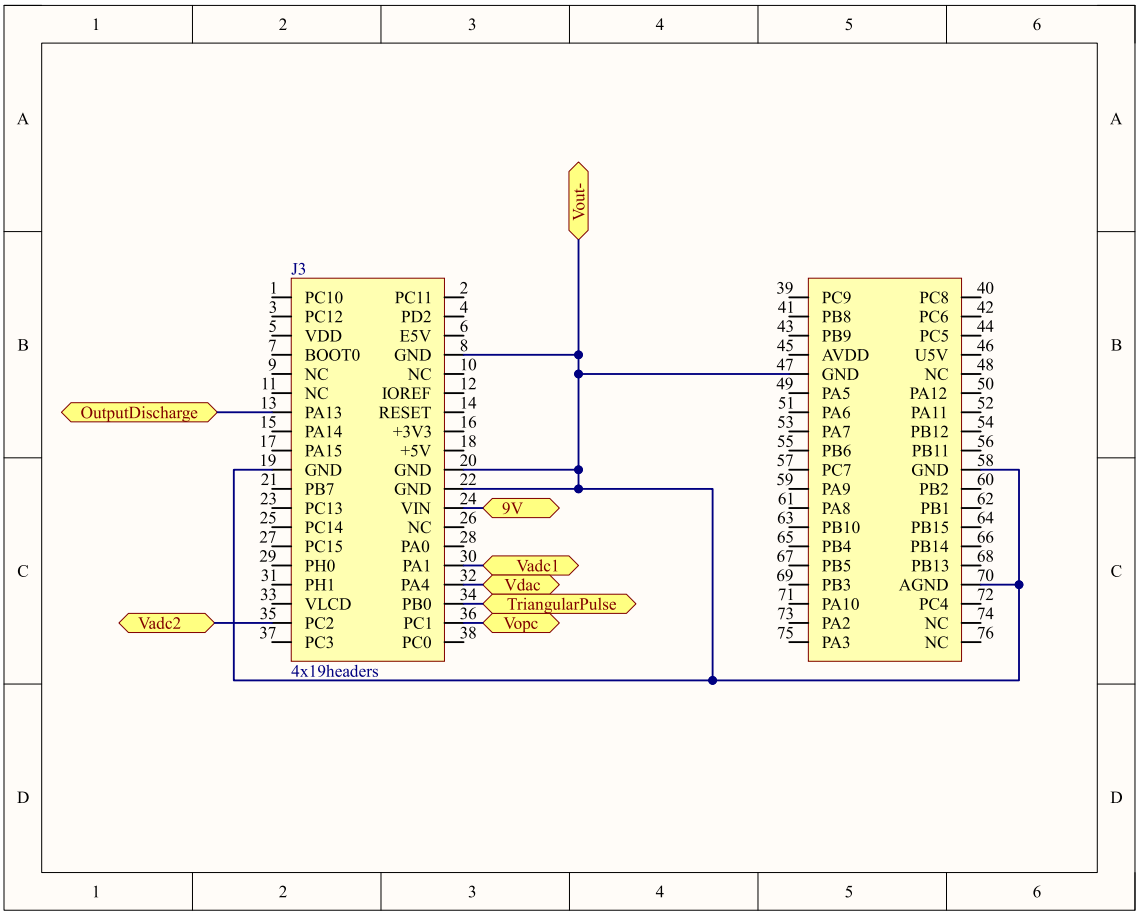

Figure 3.51: Nucleo-F334R8 recommended interface

Chapter 4

Simulation results

This chapter will examine the converter's operation by going over the outcomes. All the data were acquired through Cadence spectre simulation and they were elaborated with Matlab scripts.

4.1 Converter steady-state operation

The two active components of the converter exhibit abrupt changes in voltage and current during the steady-state. Here, their operation is examined to make sure it is operating correctly.
Then the voltage and current provided by the supply are being discussed and finally the converter's efficiency is showed.

4.1.1 BSC094N06LS5

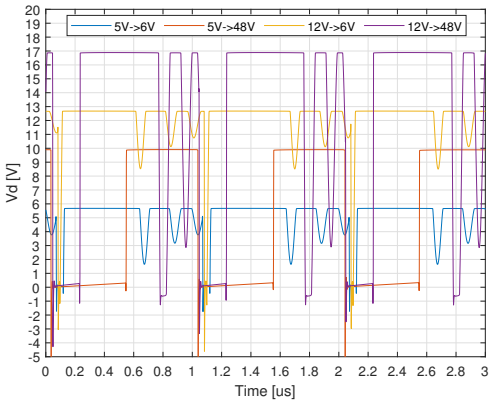

Figure 4.1: Drain-source voltage

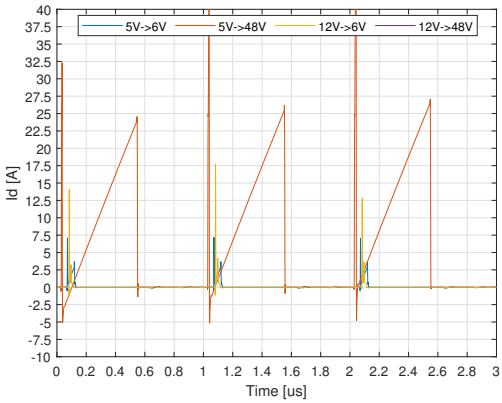

Figure 4.2: Drain current

The drain-source voltage is the same as expected; unlike the drain current, it contains a few peaks or oscillations because of the electromagnetic coupling. Instead, the current is typically higher than expected, sign not ideal efficiency, and exhibits spikes when the transistor begins to conduct.

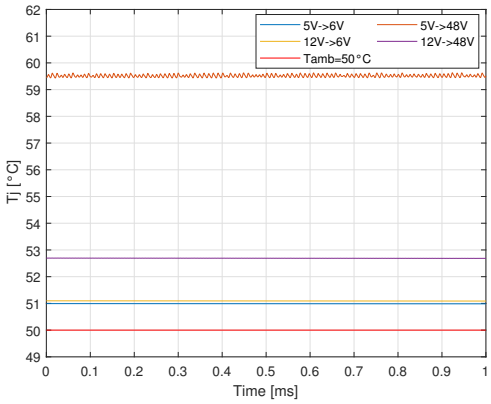

Figure 4.3: Junction temperature

Throughout every operation, the junction temperature remains constant and within the intended range. A perfect case-junction thermal connection is taken into consideration here.

4.1.2 BYV10D-600PJ

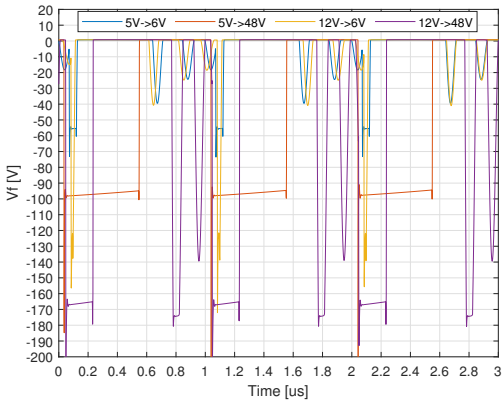

Figure 4.4: Forward voltage

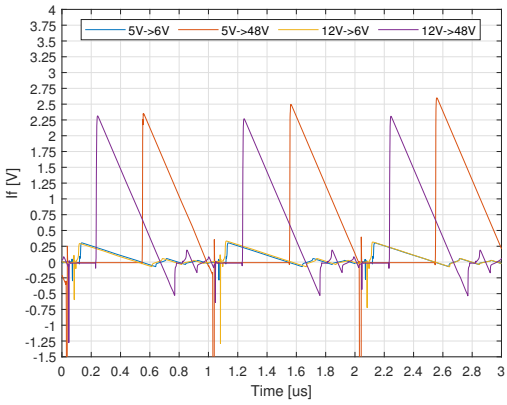

Figure 4.5: Forward current

Same considerations of the transistor voltage and current apply here, where the forward current of the diode presents more spikes due to parasitics.

4.1.3 Efficiency

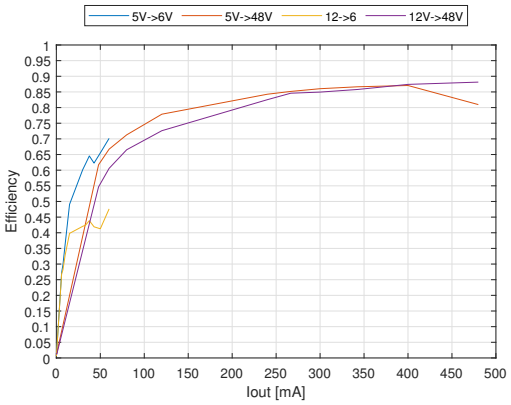

Figure 4.6: Efficiency vs output current

Two main trends can be seen from the efficiency plot:

- The efficiency grows with the output voltage, consequentially with the output current growing. It could be probably a side effect of the current spikes.
- The efficiency grows with the output current. This is due to the sensor construction; the minimum output resistance is defined by the parallel between the load resistance and the sensor one. This for a load detachment tends to $16k\Omega$, setting in this way a lower limit to the current supplied.

4.2 Transients

The goal of this part is to examine the circuit's transition phases with respect to the primary variables' variations across multiple slopes.
The following quantities will be examined:

- V_{out}: to see how the transient impacts on the output voltage;
- V_c: to see how the transient impacts on the linearity of the system;
- $T_{j,BSC094N06LS5}$: to see how the transient impacts on the BSC094N06LS5 transistor operation.

4.2.1 Variation of the input voltage: V_{in}

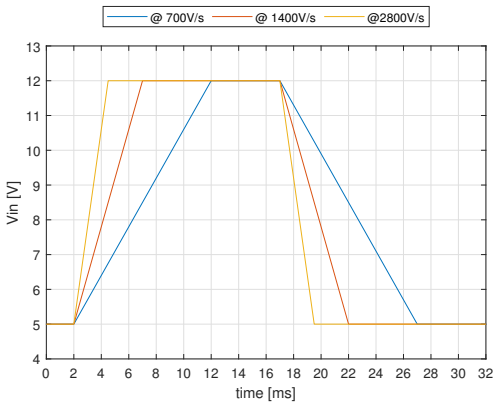

Figure 4.7: V_{in} transient

The input voltage variation used for these simulations, with varying slopes, is shown in [Fig: 4.7]. Because it represents the worst possible scenario, the load resistance was set at 100Ω.

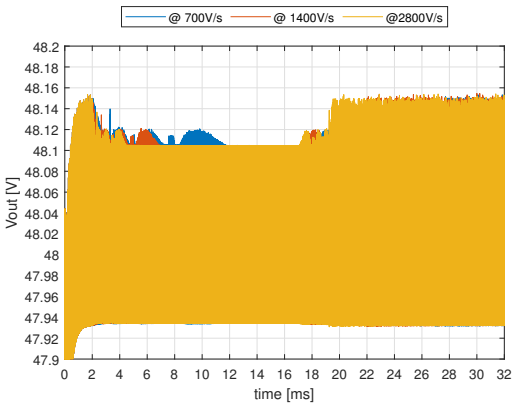

Figure 4.8: V_{out} ($@V_{out} = 48V$)

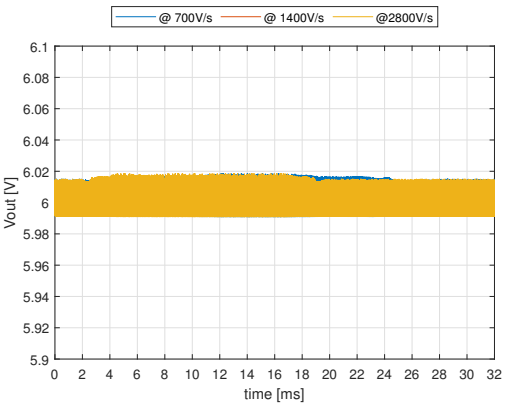

Figure 4.9: V_{out} ($@V_{out} = 6$)

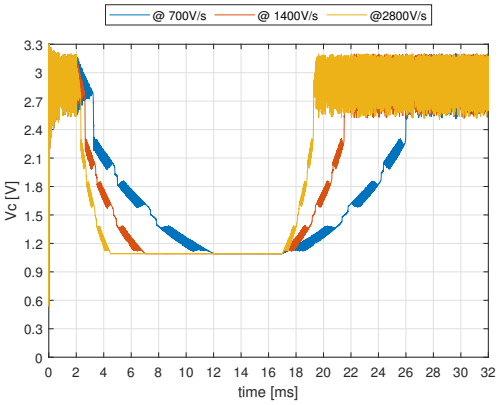

Figure 4.10: V_c ($@V_{out} = 48V$)

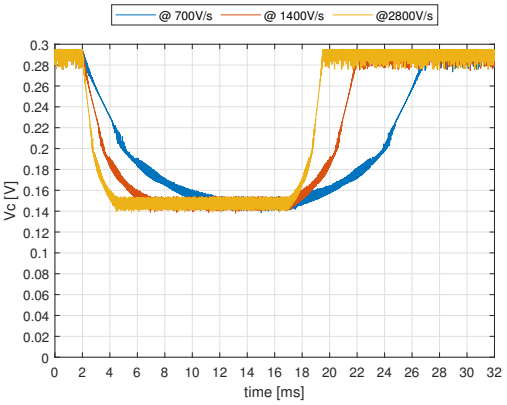

Figure 4.11: V_c ($@V_{out} = 6V$)

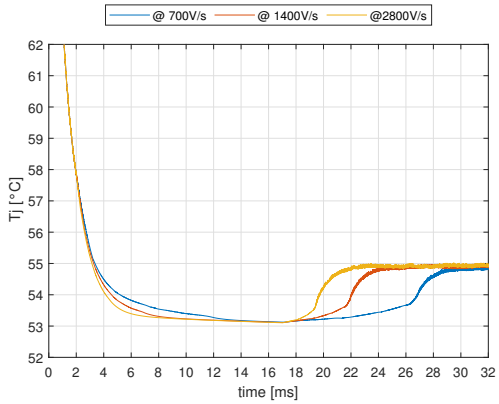

Figure 4.12: $T_{j,BSC094N06LS5}$ ($@V_{out} = 48V$)

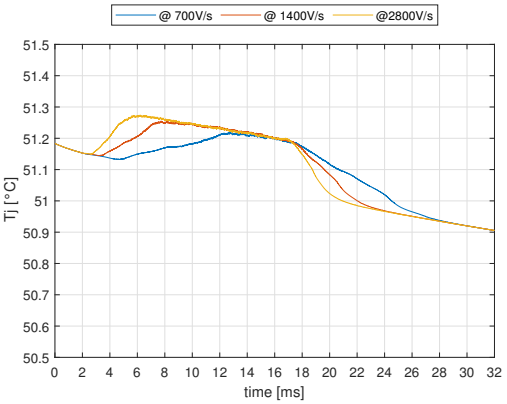

Figure 4.13: $T_{j,BSC094N06LS5}$ ($@V_{out} = 6V$)

There is no critical behavior evident in the simulation's results. The output voltage waveform for $V_{out} = 48V$ in [Fig: 4.8] exhibits a slight overshoot of about $12mV$ regardless of the input slope,

whereas $V_{out} = 6V$ in [Fig: 4.9] does not. The control voltage V_c does not saturate throughout the transitions, maintaining the linearity of the process, as seen in [Fig: 4.10] and [Fig: 4.11]. Finally, as seen in [Fig: 4.13] and [Fig: 4.13], the transistor's junction temperature is not much impacted by changes in the input.

4.2.2 Variation of the reference voltage: V_{DAC}

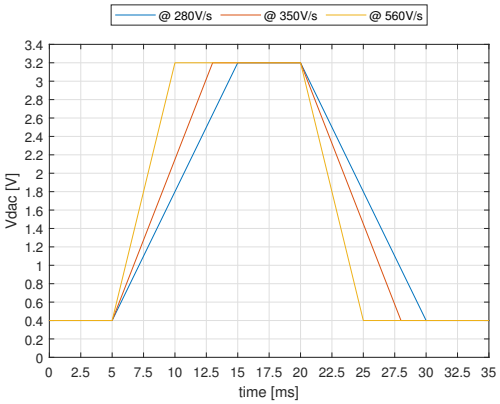

Figure 4.14: V_{DAC} transient

Figure [Fig: 4.14] displays the DAC reference voltage variation with different slopes that was used for these simulations. The load resistance was set at 100Ω since it reflects the worst-case scenario.

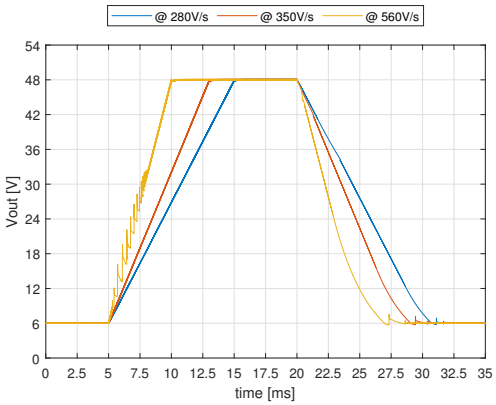

Figure 4.15: V_{out} ($@V_{in} = 12V$)

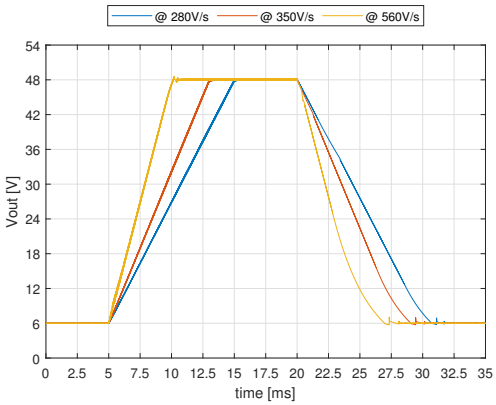

Figure 4.16: V_{out} ($@V_{in} = 5V$)

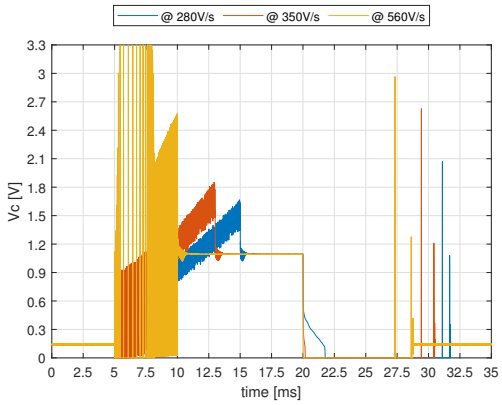

Figure 4.17: V_c ($@V_{in} = 12V$)

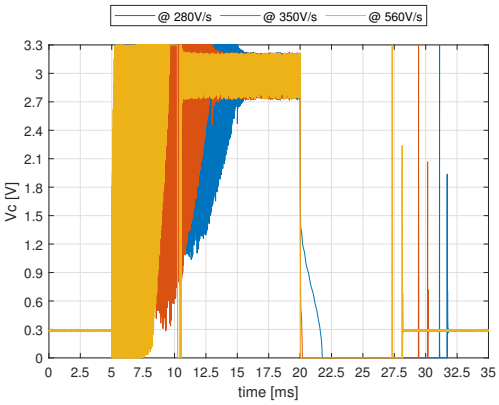

Figure 4.18: V_c ($@V_{in} = 5V$)

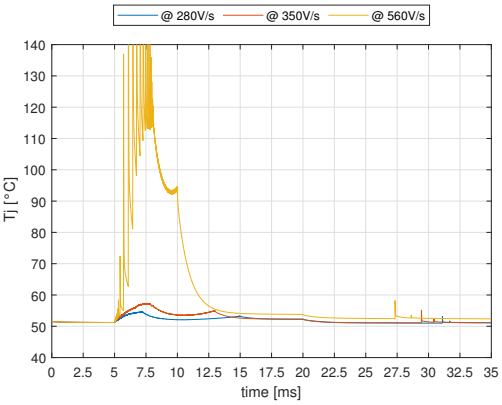

Figure 4.19: $T_{j,BSC094N06LS5}$ ($@V_{in} = 12V$)

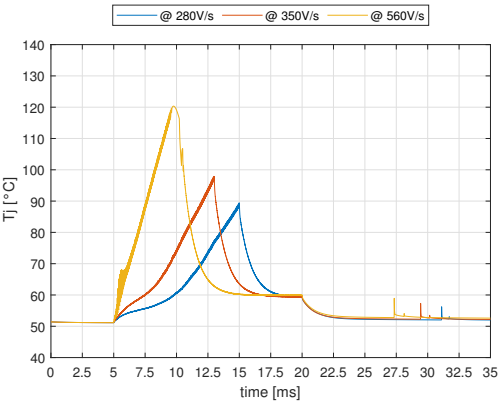

Figure 4.20: $T_{j,BSC094N06LS5}$ ($@V_{in} = 5V$)

Figure [Fig: 4.15] illustrates how the output voltage deviates from linearity during the transient for the slope $560V/s$ track. This can also be deduced from the V_c of figure [Fig: 4.17]. The greater input voltage, high slope, and high loop gain are most likely responsible for this. There are no additional criticalities seen in the other slope tracks, which are likewise illustrated in [Fig: 4.16] and [Fig: 4.18]. With the exception of a small peak in [Fig: 4.16] for the maximum slope, it is evident that the output voltage does not overshoot. It is evident that the discharging phases in [Fig: 4.16] and [Fig: 4.15] are the same as the discharging circuit is independent of the input voltage. The recommended reference voltage slope should be less than 1, primarily because greater values, as shown in [Fig: 4.20] and [Fig: 4.19], cause the transistor's junction temperature to rise excessively and may cause the device to operate outside of a safe operating region.

4.2.3 Variation of the load resistance: R_{load}

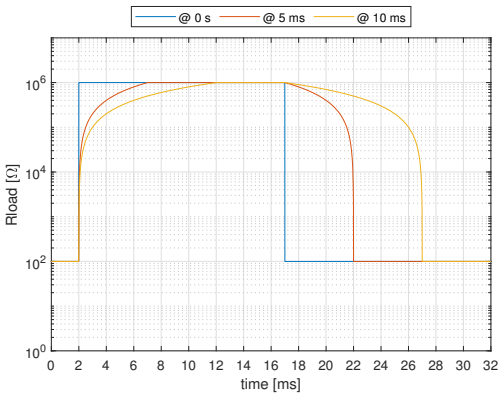

Figure 4.21: R_{load} transient

Figure [Fig: 4.21] displays the load resistance variation with different slopes that was employed for these simulations. The output voltage was chosen at $48V$ since it represents the worst-case scenario.

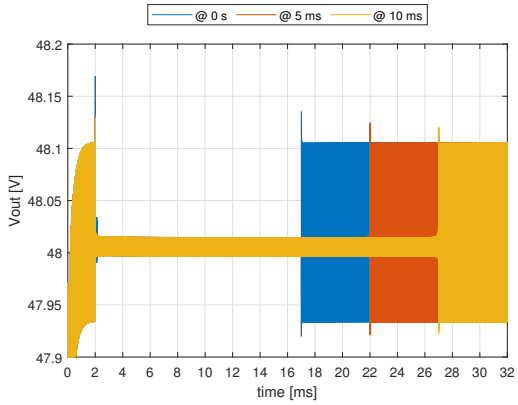

Figure 4.22: V_{out} ($@V_{in} = 12V$)

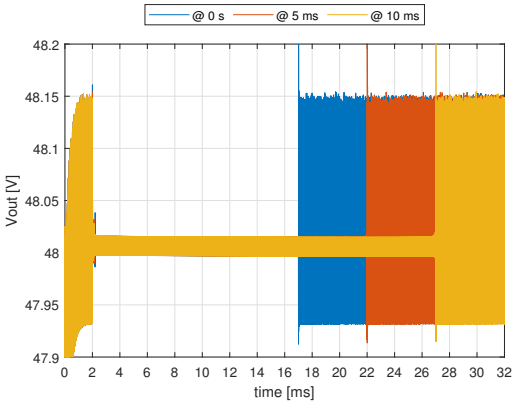

Figure 4.23: V_{out} ($@V_{in} = 5V$)

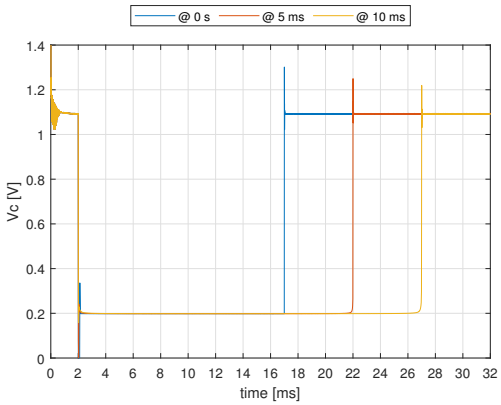

Figure 4.24: V_c ($@V_{in} = 12V$)

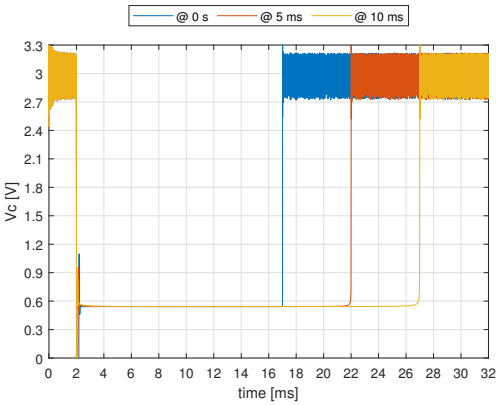

Figure 4.25: V_c ($@V_{in} = 5V$)

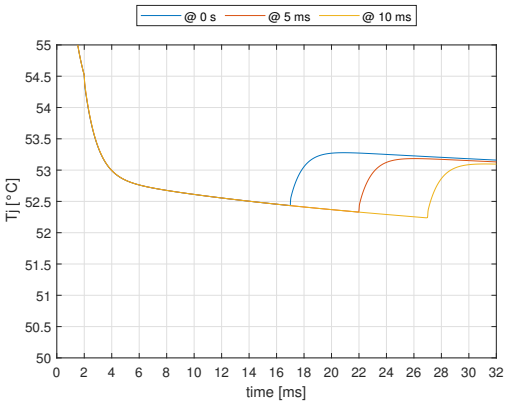

Figure 4.26: $T_{j,BSC094N06LS5}$ ($@V_{in} = 12V$)

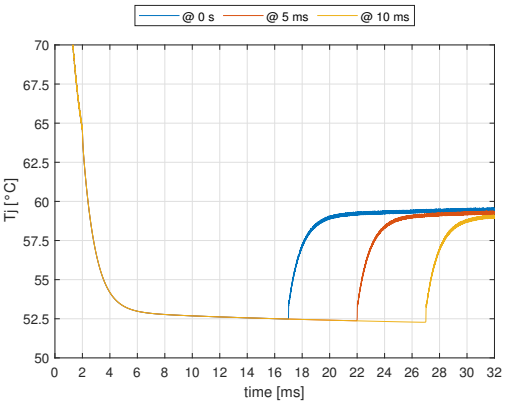

Figure 4.27: $T_{j,BSC094N06LS5}$ ($@V_{in} = 5V$)

The simulation results suggest no critical behavior. As seen in figures [Fig: 4.25] and [Fig: 4.24], the operation is maintained in linearity and there have been no crucial increases in the transistor's junction temperature, as shown by [Fig: 4.27] and [Fig: 4.26].

4.3 Output accuracy

The system's compliance with the output accuracy and settling time requirements is examined in this section. This is accomplished by applying a step variation of the system's primary variables. A Matlab script was used to process the simulation results and return their moving average on $400\mu s$.

4.3.1 Step of the input voltage: V_{in}

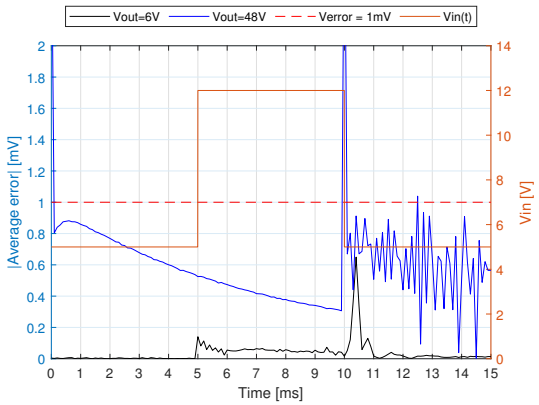

Figure 4.28: Output average error ($@R_{load} = 100\Omega$)

Figure [Fig:4.28] shows that, in the worst-case $V_{out} = 48V$, the output voltage satisfies the precision criteria nearly instantly for both rising and falling steps.

4.3.2 Step of the reference voltage: V_{DAC}

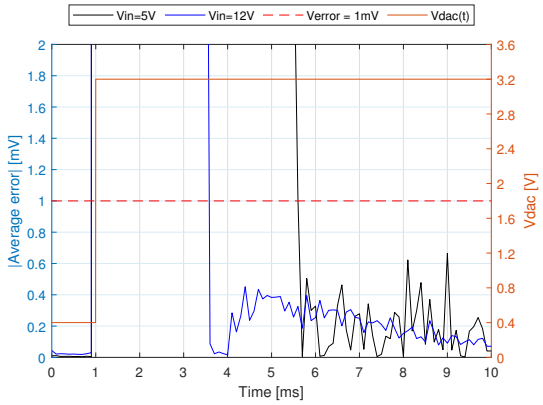

Figure 4.29: Output average error ($@R_{load} = 100\Omega$)

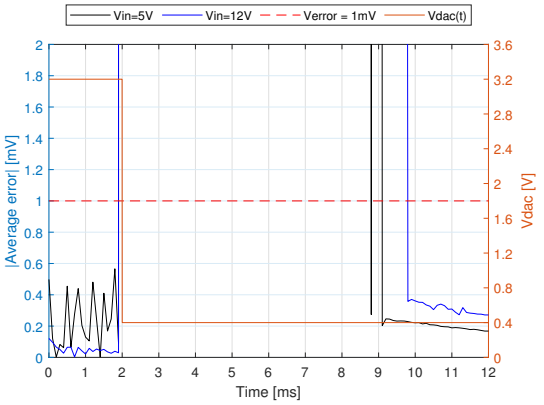

Figure 4.30: Output average error ($@R_{load} = 100\Omega$)

The rising step and the falling step are seen in figures [Fig:4.29] and [Fig:4.30], respectively. The desired precision is exceeded in both situations at worst: roughly $5.5ms$ for the rising step and almost $8ms$ for the falling step.

4.3.3 Step of the load resistance: R_{load}

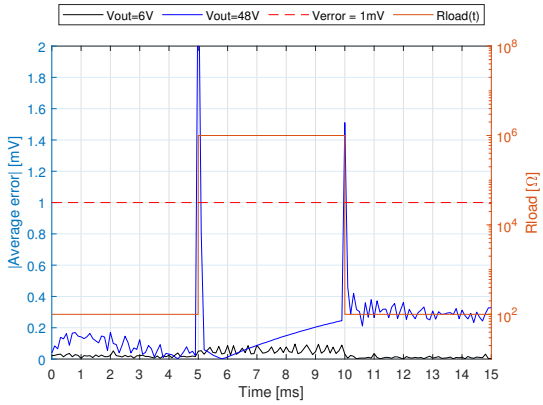

Figure 4.31: Output average error ($@V_{in} = 12V$)

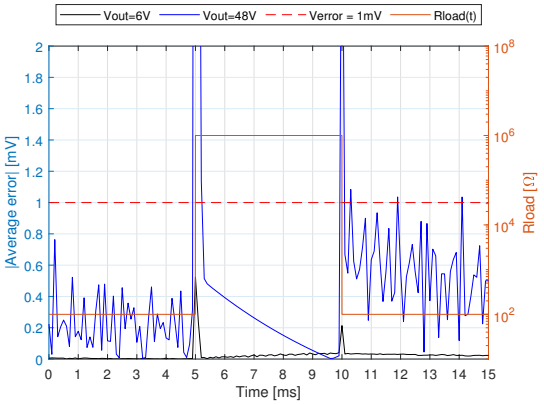

Figure 4.32: Output average error ($@V_{in} = 5V$)

For both stages in figure [Fig:4.31], for $V_{in} = 12V$, the output response is nearly instantaneous. Rather, a settling time less than $500\mu s$ for the rising edge and less time for the falling one is needed for $V_{in} = 5V$ in [Fig:4.32].

Chapter 5

Conclusions

In summary, the simulation results show that the programmable isolated DC-DC converter successfully achieves the necessary level of precision, meeting the main design aim of output accuracy. With the exception of efficiency, which falls short of the target and reaches a maximum value of slightly under 90%, all other performance requirements were met. While this efficiency level is still relatively acceptable, there is room for improvement, particularly in the power conversion stage, to increase overall energy performance. The voltage sensor, which presently requires human tuning, is the system's most notable shortcoming. Over time, this compromises the precision and repeatability of the system by introducing possible inaccuracies and variability. The integration of a microcontroller with a better bit resolution is the suggested enhancement to overcome this constraint and enable more precise voltage measurements. Furthermore, the calibration procedure would be automated with the use of an auto-tuned digital potentiometer, eliminating the need for human adjustments and guaranteeing reliable performance. Moving ahead, the project's next stage entails switching to hardware implementation. This includes creating the printed circuit board (PCB) layout, requiring for meticulous preparation to guarantee the best possible component placement, signal integrity, and power distribution. Following the completion of the PCB and the EMI filter design all components would be mounted into the board, and extensive testing would be conducted to confirm the system's functionality under actual operating conditions.

In conclusion, even if the system effectively satisfies its primary performance goals, there is still room for improvement in terms of efficiency and the voltage sensing method. The precision and reliability of the system can be improved by putting the suggested improvements into practice. To complete the project and enable full operation of the programmable isolated DC-DC converter, ongoing work on PCB layout design, EMI design and component assembly will be crucial.

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