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Technological characterization of a standard Closed cell for Molecular Field-Coupled Nanocomputing

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Abstract

Moore's Law, which has long described the scaling evolution of electronic devices, is now approaching its limit, highlighting the constraints of CMOS technology under extreme miniaturization. The search for alternatives to silicon-based systems has therefore driven research toward new and more promising technologies, capable of complex computation with minimal size and power consumption. One of the most relevant beyond-CMOS approaches is Molecular Field-Coupled Nanocomputing (MolFCN). MolFCN encodes binary information by localizing charges within molecules organized on a substrate to form functional structures, such as wires. The initial MolFCN wire design, known as the trench device, features a core metallic layer hosting molecules deposited at the bottom of a dielectric trench, with two metal electrodes placed at the top of the trench walls. Information propagation in MolFCN occurs through electrostatic interactions between neighboring molecules, making the system current-less. This process relies on the activation and deactivation of the localized charge on molecules by means of the applied vertical electric field, flowing from the top electrodes to the bottom metal substrate. The field effectiveness depends not only on its strength, but also on the geometrical positioning of electrodes with respect to molecules. Simulations of the trench device revealed that the top electrodes have limited influence on the central regions of wider wires, where information propagation becomes unreliable. To overcome these limitations, a new Closed design was introduced, in which the upper part of the trench is completely filled with metal surrounded by dielectric, forming a single continuous top electrode. This work focuses first on the creation and simulation of the Closed structure using Sentaurus Structure Editor. A mono-electrode Closed wire is generated through automated scripts, which define key geometrical parameters—such as wire width, height, and length—and build the structure for subsequent electrical simulation in Sentaurus SDevice. This automation allows rapid simulations of multiple geometries, enabling the identification of structural limits and optimal operating conditions. Once the Closed device is simulated, it is compared with a structurally analogous trench device. The comparison focuses on the analysis of electric field dis-

tribution within the central wire regions. Both devices are simulated using Sentaurus and SCERPA (Self-Consistent ElectRostatic Potential Algorithm), a tool that iteratively solves electrostatic interactions between molecules to model information propagation. A range of wire widths is analyzed to assess propagation efficiency, showing the superior performance in terms of field driving capabilities of the Closed design, particularly for wider wires. Following this comparison, a three-electrode Closed wire is investigated, to study how the spacing between multiple top electrodes affects field distribution in the inter-electrode core regions. Various electrode distances are simulated to identify potential fabrication constraints that could compromise device operation. The analysis is supported by a MATLAB script linking SDevice output fields to SCERPA, automatically extracting the relevant simulation data and generating pre-simulation structures. By examining information propagation across multiple configurations, the study identifies the maximum allowable inter-electrode spacing that ensures correct device operation, thereby defining the geometrical limits of this technology.

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Chapter 1

introduction

The trend of technological evolution in the last decades has been described by Gordon Moore, co-founder of Fairchild Semiconductor and Intel, by formulating the Moore's law. This law is an observation made on historical trend concerning the number of components per integrated circuit; in 1975 G.Moore observed that the number of transistors in a chip doubled every two years and that this trend will continue in the future [1]. This prediction was very accurate and has held since it's formulation, highlighting the constant need to develop smaller and more efficient devices to keep up with this growth.
Being transistor the core component of integrated chips, the evolution imposed by Moore's law have led this kind of devices through a series of significant changes to fabricate increasingly smaller design to be able to fit more components in the same chip area. Starting from the original MOSFET structure, the shrink in dimension has proven a serious challenge, due to unwanted and unexpected effect commonly known as Short Channel effect, which caused a sharp decline in transistors performance. Developments in this regard were made by the introduction of FinFETs and GAAFETs devices, compensating Short channel effects trough a higher electrostatic confinement of the space charge region [2] [3]; in FinFETs the channel is a thin conductive fin built on an insulator substrate and surrounded by the gate on three of its sides. This particular structure allows higher electrostatic control over the channel, reducing Short channel effects and enabling the production of small size transistors. GAAFETs transistors enhance this phenomena with an all around gate configuration, where the channel is completely surrounded by the gate. Although these new solutions partially addressed the limitations of conventional transistors such as MOSFETs, they introduced other issues, mainly related to power dissipation and parasitic components, which in turn limited the further development of this technology.

For all these reasons a new approach has to be found, leading research towards a what's called "more Moore" technological approach, able to overcome the slowdown experienced in this years. This new solution has to be integrable with the current technology, affordable for high volume production, and capable of replacing the current major technological trends. One of the most prominent beyond CMOS technology is Molecular Field Coupled Nanocomputing (MolFCN)[4], a new approach trying to substitute the main CMOS technology present nowdays.

1.1 MolFCN technology

Molecular Field-Coupled Nanocomputing is one of the most promising candidate for beyond-CMOS technology and it's working principle is based on encoding logic information through charge localization onto specific molecules. Information of binary values is encoded by localizing charges within precise molecule sites, codifying logic values of '1' or '0' with specific charge patterns configuration[5]. The molecules, carefully engineered and properly attached to a substrate, are arranged to form specific layouts allowing the creation of wires and logic gates. Molecules are disposed in an organized manner across substrate, and their position development across the devices will dictate how those devices will work. Thanks to electrostatic interaction between nearby molecules, their charge distributions can effect each other due to Coulombic repulsion, leading to information propagation. This phenomena exploit a non conductive mechanism, where input is propagated not trough current motion but with electrostatic interaction, making the system current-less. This offers some advantages with respect to normal CMOS technology, mainly regarding power losses and speed; MolFCN is a very power conservative solution, since no current is involved [6]. It is also extremely fast, since the switching and propagation of information is regulated by the electrostatic interaction of localized charges, that very quickly aligned themselves in the most optimum configuration[7]. This technology also works well at room temperature, without the needs for very specific temperature conditions[9].
In order for the propagation mechanism to be precise and easily controllable, the molecules have to be carefully aligned on the substrate, to ensure the correct Coulombic repulsion between nearby charges. This technology is based on two main components: the molecules and the structure that hosts them. We will analyze these elements in detail to understand the key functioning principle and the role the two components play in MolFCN operations.

1.1.1 MolFCN design: Molecules

Molecules are the core elements of this technology and they need to have certain characteristic to ensure proper device operations[10]: first they need to have an atomic structure that allows electrons to navigate freely from one side to the other; Second, atoms arrangement should create low potential sites in which electrons have lower potential energies. These states are separated by a high enough energy barrier and we can consider them stable; this is important because information is encoded in the charge distribution across the molecule, so we want precise stable molecule sites, called DOTs, that are able to provide regions for electrons to localize. A molecule should posses at least 3 DOTs for the purpose of MolFNC, and the charge localization should produce strong enough dipole that allow the electrostatic coupling between molecules; also the charge should be able to be localized trough the application of external electric field acting on the molecule, controlling this mechanism trough electrodes. Lastly molecules should be chemically and thermally stable, with particular compounds denoted as "anchoring groups" that enable the connection with the substrate.
A MolFCN unit cell it's so composed by two nearby aligned molecules; in this configuration charges of both molecules will organize themselves to minimize the repulsion energy , assuming the two most stable distributions displayed in figure 1.1.

(a) Logic '1' MolFCN charge configuration (b) Logic '0' MolFCN charge configuration

Figure 1.1: Unit cell for MolFCN

Charges will fill the diagonal Dots to minimize Coulombic repulsion, giving the elementary cell a binary nature represented by the only two possible combinations. To each of this two configurations can be arbitrarily assigned the encoding of a specific bit value, '1' or '0', depending on which diagonal axis the charge is found, as represented in the figure 1.1. If a line of this unit cells is built, information will propagate due to the distribution of electrons of one cells influencing the next one, due to electrostatic interaction. This happens only if the molecules are placed close enough and arranged orderly ; with this system further unit cells in the line will be encoded with the same charge configurations (and so the same bit) of the previous ones, thus guaranteeing a correct propagation of information. Another advantage

of this technology will be the speed of propagation, since once influenced by an input all the molecules of a wire will quickly switch under its influence, propagating information very fast[7].
An elementary unit cell composed only by 4 DOTs distributed on two molecules is not sufficient for MolFCN application, for two main reasons: first having only two stable states separated by a very high potential barrier will means high energy cost to perform charge switching, when changing a logic '1' to '0' or vice versa. so we would like a lower energy separation, but this will mean more susceptibility to perturbation, which could cause the accidental switching of the encoded information. Without an intermediate NULL state perturbation anywhere along the line will instantly change the logic information of cells, especially for long wires. Secondly there is no directionality of transmission, since each cell can influence the surrounding ones this system lacks a correct propagation direction control.
To overcome this problems the structure of the cell has to be slightly changed, enriching it of a new set of two DOTs, modifying the final element to have six DOTs in total (3 DOTs for each molecule). This change allow us to localize the charge to an intermediate state, usually located in a specific site in the lower part of the molecule, trough the application of a vertical electric field acting as a RESET signal[16].
When the cell is affected by the reset signal, the state of the cell is considered 'NULL' and charges are localized in a middle stable state configuration, which does not encode any binary value but is essential to guarantee the correct functioning of this system[17]. Cells are kept in the 'NULL' state until there is the need to propagate information; upon reversing the reset signal charges will flow toward the top two stable DOTs, in the HOLD position ready to propagate, switching position based on the driver input configuration. The energy needed for this phenomena is lower when compared to the absence of the 'NULL' state, since we are moving charges out of an intermediate state. The presence of a NULL configuration ensures better information retention and error insensitivity due to the two binary states now being well separated by the intermediate 'NULL' state. The possibility of resetting the cell to a null state also allow the creation of clock zones into the device, where different regions of the chip will be affected by different clock signals to allow information propagation to have directionality. With the subsequent application of clock signals we are able to control the propagation keeping part of the molecules in a null state until transmission is occurring. It comes clear that the choice of a molecule for MolFCN applications is a very careful process, where the properties of the compound are analyzed and studied to guarantee its proper behavior and stability for specific applications[5].

This concept of forcing molecules into reset state is necessary to ensure the basic functioning principle of MolFCN, which rely on the subdivision of logic circuit into zones, called clock zones, where external electric fields are applied in a controlled manner. The circuit is therefore divided into a sequence of zone driven by different electrodes, each one producing a different vertical electrical field on the underlying molecules. A depiction of this area division is depicted in figure 1.2, where different groups of unit cell are controlled by specific clock signals.

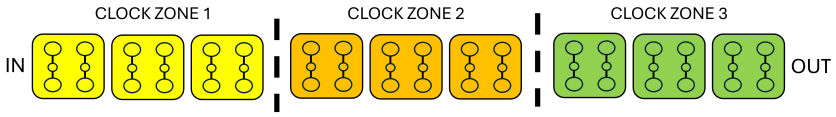


Figure 1.2: Clock zones in a MolFCN circuit

A sequence of cyclic signals can be forced to these electrodes to induce control over the circuit, favoring a correct information propagation and ensuring directionality. The sequence of phases in which a particular clock zone can be brought are:

- Switch Phase: in this phase the reset signal is released and charges localized from the NULL configuration to the HOLD configuration, aligning themselves under the influence of the driving input that precede that particular zone in the line.
- Hold Phase: the zone is kept in the Hold state trough the release of the reset signal, allowing all charges to assume and maintain the correct configuration; the information is carried out to the next zone in line, that is under the Switch phase.
- Release Phase: the electric field is changed to reset the cells once the information is propagated, moving charges towards the NULL state configuration.
- Reset Phase: the zone is completely reset, clearing out the information it stored and readying it to receive a new information in the next clock steps.

This sequence is repeated consistently across all the other clock zone, to move information in a synchronized manner across the circuit (Fig. 1.2). In this way we ensure all bits to arrive coherently at the same time in input to logic gates; in a majority voter for example all 3 inputs must bring information in input at the same clock step to ensure the correct port logic behavior, as depicted in Figure 1.3.

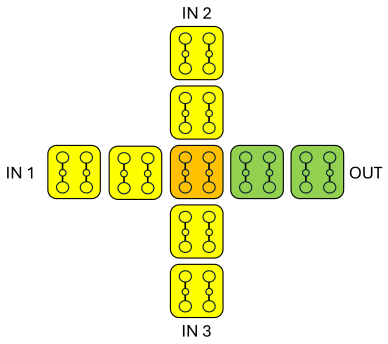
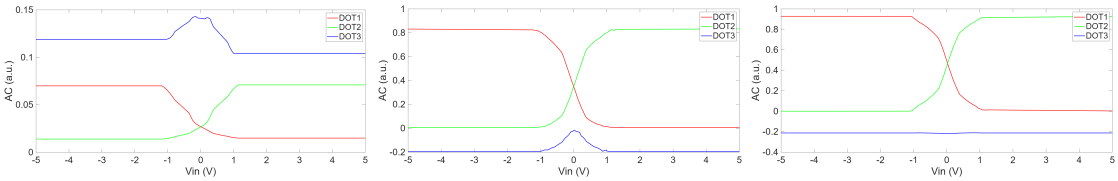


Figure 1.3: Clock zones for Majority Voter circuit

There are different techniques to connect molecules to the substrate, one of which is Self Assembled Monolayer (SAM) [11]. The working principle is to start with a compound formed by two part, an "head" group and a "tail" group; this precursor is brought into gaseous phase and pumped into a reaction chamber, where the substrate is exposed. Thanks to a chemical bond between the head and the substrate, this compound attaches itself to the layer, exposing the tail part to the top. Depending on precursor concentration, temperature, pressure and chemical reaction the compound will orderly attach to the substrate, completely filling the surface. Once attached, the exposed tails serve as mechanical support for the bond of the "Functional Group", the main component of the molecule, completing the structure. By tinkering with material types, chemical bond and reaction parameters we can create different layouts of molecules directly on the substrate, that will in the end serve as the circuital elements of MolFCN technology.
One of the first used compound was Bisferrocene, a molecule composed by 3 fundamental groups. The top active ones are Ferrocene groups, that store charges during the HOLD phase, connected to a third Carbazole group acting as the third NULL group. The Ferrocene group is composed by an atom of Iron in the middle of two cyclopentadiene, and the Carbazole is composed by $C_{12}H_9N$ connected to the Ferrocene trough a CH_3 element. On the bottom the structure is ended by a Thiol group that connected the all molecule to the substrate, acting as an anchoring element. This was one of the main molecule type used [8], but continue development and research is done to ensure better characteristic of molecules, finding new combination of elements best suited for this new kind of technology. The theoretical research of new candidates is done with software like ORCA, where particular molecules are tested and characterized by the means of ab initio simulation. In this study all the simulations were performed with an ideal experimental molecule, which was created using Orca software and integrated into the SCERPA database. This ideal molecule is composed by 3 DOTs, and to better understand it's electrical prop-

erties an analysis on it's V_{in}-to Aggregated Charge Transcharacteristics (VACT) is presented. The VACT is a key parameter in molecule modeling because it relates the input voltage (V_{in}) to the sum of atomic charges (the aggregated charges of the Dots) at a specific E_{clk} [20]. VACT is used inside SCERPA to define the input voltage of each molecule taking into considerations all the elements affecting propagation such as driving voltage, effects of the localized charge of other molecules and so on. The VACT for the ideal molecule are shown in Figure 1.4; in this figure the localization of the charge can be seen as function of input voltage for specific E_{clk}. This molecule will be used for all the design analyzed inside this study.

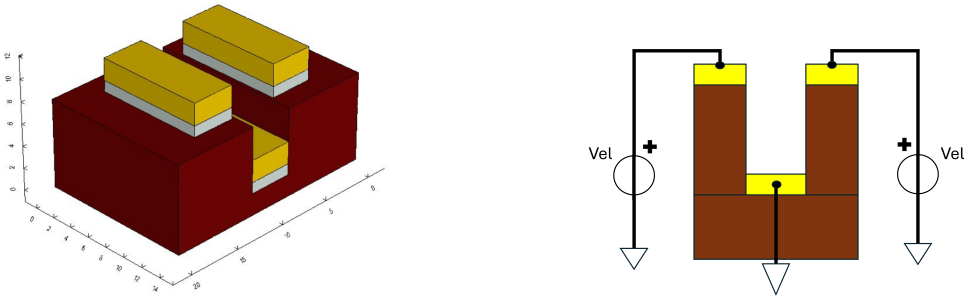


(a) VACT for E_{clk}=-1 V (b) VACT for E_{clk}=0 V (c) VACT for E_{clk}=1 V

Figure 1.4: VACT of the Ideal Molecule

1.1.2 MolFCN design: Cell Structure

Molecular FCN technology relies not only on the presence of molecules capable of storing charge, but also on the appropriate substrate structure that can provide both mechanical support needed to hold molecules in place and proper electrical driving capabilities to apply suitable electric fields to control charge localization. An early version of the structure was the so-called 'Trench' design, figure 1.5, where molecules are deposited onto a metallic substrate (often gold) acting as the bottom electrode. This layer is located at the bottom of a dielectric trench, usually SiO_2, whose side walls surround the rows of molecules [13]. To create the appropriate electric fields, one vertical for resetting the cell and one transversal to perform charge switching, two additional gold layers are deposited at the top of the two sides of the trench. Thanks to this design, molecules can be influenced by both transverse and vertical electric fields, allowing not only information propagation but also switching processes to affect the charge configuration during the HOLD state.

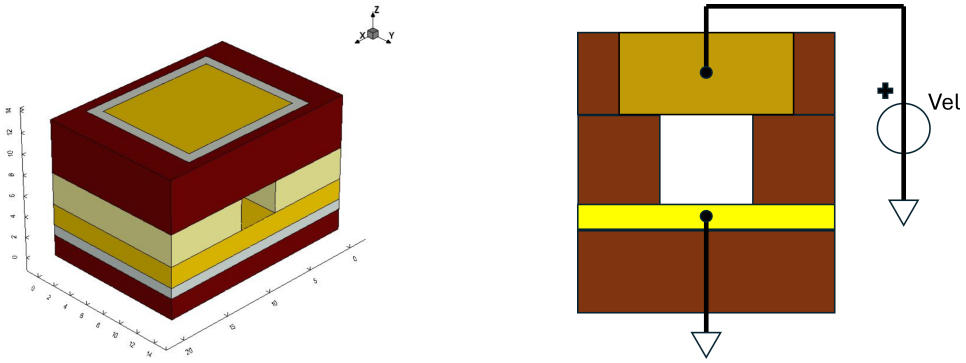


(a) Trench design, general view (b) Trench design schematic

Figure 1.5: Trench cell structure

Due to the particular positioning of the electrodes in such design (Fig 1.5.b), the structure revealed to be insufficient in producing the adequate fields necessary to perform reset operations, often leaving molecules in the center region of the wire unaffected by external control. This problem is accentuated for larger wires, where the rows of molecules carrying bit information are more, and the distance between the two top electrodes start increasing. For larger distances the field produced is insufficient in driving the central regions, leading to problems during propagation. In this study, these problems will be investigated and the trench design compared, with a new design, called Close Cell.

For this particular structure the electrodes are only two, and one directly above the other, engulfed in dielectric material; the Gold substrate on which molecules are attached runs in the core center of the wire, propagating information from one open side to the other. This capacitor-like disposition of electrodes, as depicted in figure 1.6, subjects the wire molecules to very stable and precise vertical electric fields, flowing from top to bottom. The lower electrode, always grounded, will be the reference to the top one, which will be biased up to certain voltage values, in the range from 3 V to -3 V. In the next chapter a detailed analysis on this structure composition is carried out, in order to understand how the electrode positioning on this model affect field distribution in the core of the device, followed up by a comparison with the old Trench design.



(a) Closed design, general view (b) Closed design schematic

Figure 1.6: Closed cell structure

Chapter 2

Closed device Analisys

In MolFCN technology, the application of adequate electric fields to molecules is crucial to ensure the proper operation ; fields must be able to consistently and controllably influence the cell core to localize charges across DOTs during the working cycle of the device. In this regard, the limitations of the Trench design in terms of field control have become evident, especially when considering trench sizes greater than 8 nm (i.e. more than 4 lines of molecules). For this reason, the creation of a new device was necessary, one that could address all these limitations. In this chapter we investigate the Closed design, highlighting it's construction algorithms and simulations parameters in Sentaurus, with a particular focus on electric field distribution results. Starting with Sentaurus Structure Editor tool, a series of automated command script is produced, to easily simulate different geometrical variants of the Closed cell. Electrical simulation is then performed trough Sentaurus SDevice, with a follow up analysis on MATLAB. Lastly, propagation is studied trough the use of the SCERPA tool.

From a structural point of view the Closed cell is built starting from a Silicon Oxide substrate (grown from the Silicon wafer) representing the base substrate, on which a titanium adhesion layer is deposited, followed by a gold layer deposition. The latter will serve as the bottom electrode for the structure, where Titanium will ensure the proper adhesion of Gold to the SiO_2. A second dielectric layer, Al_2O_3, is then deposited and subsequently patterned into rectangular trenches of various sizes (depending on the width of the wire). At this point, the lower half of the device is completed and molecules will ideally be attached through specific attachment processes, such as Self Assembly Monolayer. The upper half is composed by a gold VIA, simulated as a cut top Gold layer embedded in a SiO_2 dielectric layer. The upper structure was designed in this way to realistically simulate a possible

theoretical technological implementation, where the lower and upper structures are produced on separate wafers and then united through wafer bonding. By designing the upper part in this way the vertical VIA connection is represented as a exposed Gold layer, acting as an active contact.

For possible fabrication implementation, the creation of the bottom structure is achieved by starting with an oxide growth on the wafer followed common deposition techniques such as CVD and ALD to deposit the three subsequent layers of Titanium-Gold-Al_2O_3 [18]. As for the patterning of Al_2O_3, precise techniques are required due to the small dimensions of the cell width. One possible technique that can be used to produce such precise patterning is Electron Beam Lithography, with dimension as low as few nanometers[19]. Once the bottom structure is created, it's time to place the molecules on the gold substrate; this can be done using well-known techniques like SAM (Self Assembled Monolayer) or other attachment techniques. In order to preserve the integrity of the molecule structure, fabrication with high temperatures and high chemical concentrations should be avoided. Instead, it would be necessary to create the upper half of the device on a second wafer using similar fabrication techniques and, once the upper half is done, join the two halves trough a wafer bonding process; This will ensure the presence of molecules in the empty space at the core of the device without unwanted exposure to heat or chemical reagent.
From a simulation perspective, Sentaurus Structure Editor was used to create a flexible project capable of generating and adapting to changes in the main geometrical cell parameters (such as length and width, trench walls height, layer thickness, and so on). To achieve this, each sde.cmd file starts with the definition of the so-called primary parameters, which define the key characteristics of the structure. From these parameters, a series of secondary parameters were derived, useful for setting the various geometric positions to define the different material blocks of the structure.
Once the structural simulations for both the closed device and the trench device are completed, the next step is to run the electrical simulation on Sentaurus SDevice. By applying a voltage to the upper electrodes of both structures, the electric field is simulated by solving it in a quasistationary manner; we can then work on the .tdr file containing all the simulated electrical properties, including the vertical value of the electric field, expressed as $[\frac{V}{cm}]$, to extrapolate useful information for the SCERPA tool. Using all the collected data we can make conclusions on the performance of Closed device for different width configurations, setting the bases for the confrontation with the Trench design in the next chapter.

2.1 Cell creation with Sentaurus Structure Editor

Sentaurus Structure Editor is a Sentaurus tool that allows the creation of 3D structures starting from a command script file; the structure is built in an iterative manner, based on the different geometrical instructions defined in the command file. Thanks to this feature we can simulate different versions of the same device by varying the numerical parameters such as trench width, trench height, cell length, clock region length ecc...
We begin our study with the creation of a single phase Closed wire, which structure is a Closed cell with only one top electrode. At the start of every command script it's useful to define a series of primary parameters, numerical constant values expressed in μm that describe the main geometrical characteristic of the cell (such as wire width, length, core region width, ecc...). The main parameters definition is performed with the command:

```
(sde::define-parameter "TrenchMiddleWidth" @W@ )
```

This command save a numerical quantity as a labeled variable, so it can be easily recalled further in the script by other function as geometrical point in space. In this particular example a main variable is defined, namely the width of the wire section, giving it a generic μm value so different sizes of device can be quickly simulated inside the same Sentaurus project. To keep the results on the field distribution inside Closed cell consistent throughout all the future analysis, the main parameter changed is the core region width, keeping all other geometrical ratios constant. Details about the numerical values of the dimension involved for this devices are detailed later in this chapter, once the full structure is built.

Once all the primary parameters have been defined, they are used as basis to define a series of secondary parameters, useful for expressing space points necessary for the automated creation of the device updating their value when the main parameters are changed. Secondary parameters are derived from the main one to express volatile geometrical points that define geometric positions not directly related to the intrinsic characteristics of a wire (such as the wire's length or width), but rather derived from them (for example, the point that marks the beginning of the first trench wall). These parameters are the result of algebraic operations performed on primary parameters; secondary parameter are defined by the following command:

```
(sde::define-parameter "BottomDielectricWidth" (+ TrenchMiddleWidth
TrenchWallWidth TrenchWallWidth))
```

Here the parameter expressing the bottom SiO_2 width (and in this work basically the total width of the cell) is defined as the sum of the trench width and the left and right walls of Al_2O_3 (previously defined as main parameter). This characterization of primary and secondary parameter was done to link the most important characteristic of a cell to direct numerical values, so they can be quickly changed being associated with project parameters in Sentaurus, simulating all together a lot of cell variants. After all the parameters describing the geometric spacing of the device have been defined, we can proceed to the creation of the material blocks, defined with the command:

```
(sdegeo::create-cuboid ( position xi yi zi) ( position xf yf zf) "material")
```

This instruction creates a block of the specific material in the shape of a parallelepiped, whose dimensions fill the space between two diagonally opposite vertices, specified by their x, y, and z coordinates; each block can be also uniquely labeled to facilitate the definition of contacts and merging operations between different blocks. Once all the materials blocks are defined, it's time to identify and activate electrical contacts with the command:

```
(sdegeo:define-contact-set "BottomContact" 4 (color:rgb 1 0 0) )
(sdegeo:set-current-contact-set "BottomContact")
(sdegeo:set-contact BOTTOMCONTACT "BottomContact")

(sdegeo:define-contact-set "TopContact" 4 (color:rgb 0 0 1) )
(sdegeo:set-current-contact-set "TopContact")
(sdegeo:set-contact TOPCONTACT "TopContact")
```

With this command the material block matching the name, in this case the two Gold block, is identified and activated as the structure contact. Being the Closed device formed by only two electrodes, the top one and the bottom one, we need to define and activate both of them for SDevice simulations to characterize the region into which apply the voltage. The last thing we need for the electrical simulations is the definition of the mesh. Since the mesh is the grid of geometrical points on which the complex semiconductor equations such as Poisson and continuity equations are

solved, its setup is essential to optimize the trade-off between simulation speed and result accuracy. The finer the mesh grid is, the more precise the results are at the cost of higher computation time. Since the critical region to analyze in this kind of devices it's the central core region (i.e. the region in which molecules are attached), we are interested in precise electric field simulation results in this area. For this purpose a ref/val window was used; this is a specific 3D region in which we can refine the standard Sentaurus mesh, to make it more precise along specific axis. For a Closed cell, the ref/val window was defined inlcuding all the core region of the wire, running across the entirety length of the wire, wide as the trench and filling the space between the top and bottom electrodes. This allows us to freely adjust the mesh parameters in the region of interest only, without unnecessarily refining the mesh in outer regions (such as the lateral Al_2O_3 regions or the underlying layers).

Once the .cmd file for Sentaurus Structure Editor has been compiled and run, we have a solid starting point for the iterative development of the models. The dimensions of a standar single phase Closed cell are described in the following:

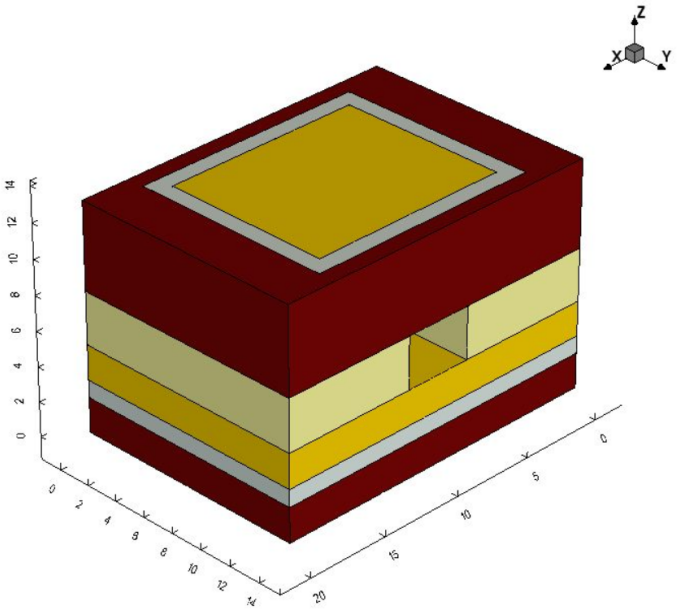
- **Y-axis**: the Closed wire longitudinal axis is oriented along the y direction, following information propagation. In the lower part, the device is composed by 3 layers which extend for a total of 14 nm in length. In the upper part, the device extend along this axis for 14 nm total, with 10 nm occupied by the gold top electrode , 2nm for the surrounding layers of Titanium and 1nm of SiO_2 at each sides for separation.

- **X-Axis**: the Closed device total width is the sum of the wire width and the Al_2O_3 wall thickness; the simulated dimensions are 8nm for the walls thickness and a variable size range for the width, ranging from 4nm to 32nm (4nm, 8nm, 16nm, 24nm, 32nm). In the first chapter of the study only dimension of 4,16 and 32nm are considered.

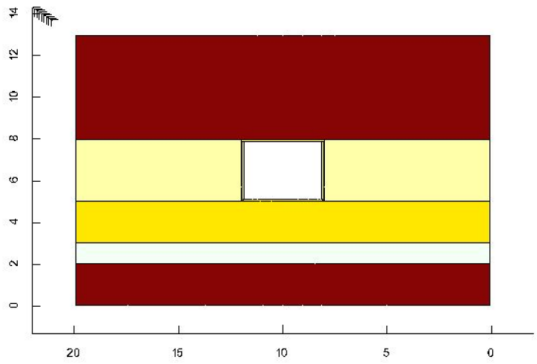
- **Z-Axis**: This axis in Sentaurus define the height development of the device. A 2nm thick SiO_2 bottom layer was considered, with a 1nm Titanium and 2nm Gold layers deposited on top. The height of the Al_2O_3 is 3 nm, leading to the upper part of 3 nm total height. The top Gold electrodes are buried in SiO_2 and emerge from it only in the top face, exposing the contact to emulate the presence of a Gold VIA.

This dimension are kept consistent throughout the initial analysis, with width being the only parameter changed for all the variants. The void core region of the wire is completely filled with Vacuum material, to represent the condition in which the

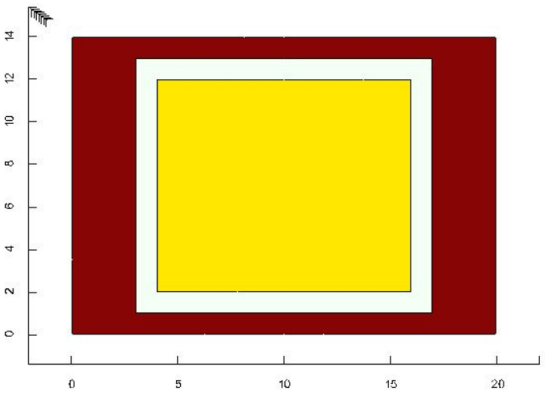
molecules ideally would be. The structural simulation result for a W=4 nm wide wire with the aforementioned dimensions is shown in Figure 2.1. In the Figure SiO_2 is depicted as reddish brown, Titanium as light grey, Gold as yellow and Al_2O_3 in Beige.



(a) Closed cell 4nm wide, general view



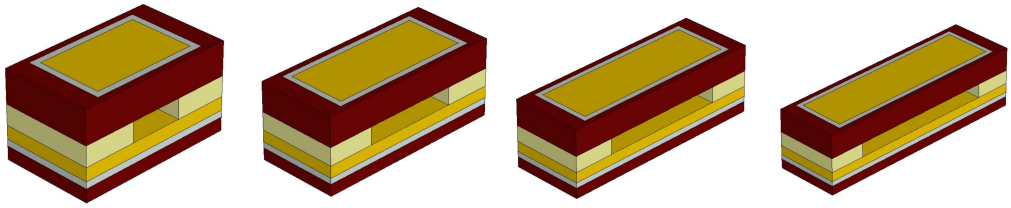
(b) Closed cell 4nm wide, frontal view



(c) Trench device top view

Figure 2.1: Closed cell 4nm wide

By varying the Sentaurus parameter associated to the device core width we can quickly simulate larger or narrower wires; in Figure 2.2 are presented the major combinations of width W used for this study.



(a) 8nm width (b) 16nm width (c) 24nm width (d) 32nm width

Figure 2.2: Closed cell dimensions range

At the end of the Structure Editor simulation a .tdr file is produced, containing all the geometrical information and the mesh layout, needed for the electrical simulation. This design is intended to host molecules in its core region, the central void channel that runs across the entire length of the cell. The molecules, attached to the Gold bottom layer, should ideally be arranged in longitudinal lines, with a x=2 nm step between each of them. This can be quickly related to the width of the cell in order to understand how much lines are expected for each variant, and how much information is carried trough the device. Each line representing a bit of information we can consider that the number of bits/lines is half of the width. For a W=4 nm cell for example two lines and therefore two bits are propagated.

2.2 Electrical simulation with Sdevice

Electrical simulation of the device is performed with Sentaurus SDevice and, similarly to Structure Editor, the simulation instructions are written in a command file. The tool takes as input the .tdr file produced by Structure Editor containing all the information about the geometry and mesh structures, and performs a serious of electrical simulations on the model. Once the simulation is finished the output is another .tdr file containing all the relevant computed electrical data. The Sdevice command script file is divided into different section where all main parameters of the simulation are specified. The first section is the File section, where input and output files are specified to the tool. As input, we have the Structure Editor .tdr file containing the structure and the mesh, as well as the file with material properties. This specific .par file includes all the physical and chemical properties of the materials used, along with all the relevant physical constants.

```
File {
*Input files
Grid ="@node| − 1@_msh.tdr"
Parameter ="sdevice.par"

* Output files
Plot ="Quasistationary_n@node@_des.tdr"
Current ="Quasistationary_n@node@_des.plt" }
```

The command GRID is associated with the device mesh file while the command PARAMETER provide as input the list of materials physical properties. For the output files we use the command plot to obtain a final model where all the interesting electrical properties are simulated. For what concern the sdevice.par file it is necessary to make some clarifications on how Sentaurus stores material parameters, and more importantly, which materials are included in the software's standard libraries. Most of the materials used for the wire are considered standard by Sentaurus, and therefore do not need to be explicitly defined within sdevice.par (Those are the most common material like Gold, Titanium, SiO_2, Air, Vacuum ecc..). The only exception is Al_2O_3 dielectric used for the trenches, which must be defined separately because it is not included in Sentaurus's internal libraries. To include this material, it was sufficient to copy the structure of an existing .par file, in this case that of Si_3N_4 and use it as a template to create our custom material file for Al_2O_3 . This choice was done due to the physical similarities between the two dielectrics. The physical constants changed to express the Al_2O_3 parameter file starting from the Si_3N_4 one are:

- Energy Band Gap, defined in the file as <Eg0>, set to 8.72 [eV]
- Electric Permittivity, defined in the file as <epsilon> set to 9.8
- High frequency Permittivity, defined in the file as <epsilon_inf> set to 3.2

All the values were found referred to Al_2O_3 at room temperature [15]. To complete the procedure we must now link this new material .par file to a existing template inside Sentaurus. We can exploit the generic template "Anyinsulator.par" for storing Al_2O_3 properties, so when we reference the Anyinsulator material inside "sdevice.par" we are correctly using Al_2O_3 properties.
The next section is the Electrode section, where the contacts are specified and assigned with an initial bias, in this case to 0 V.

```
Electrode {
Name="TopContact" Voltage=0.0
Name="BottomContact" Voltage=0.0
}
```

In the Physics section, the physical models used during the simulation are specified.

```
Physics {
Mobility(DopingDependence,HighFieldSaturation(GradQuasiFermi),Enormal)
Fermi
}
```

Mobility keyword express the use of the mobility model, which allow the user to include different phenomena in the study of carriers mobilities. The constant mobility model which accounts for phonon scattering is always active by default, but with the DopingDependence specification the mobility degradation due to impurity scattering is considered; HighFieldSaturation takes into account the velocity saturation of carriers when influenced by an electric field and Enormal takes into account transverse variations of the mobility. Fermi command instructions impose the use of Fermi-Dirac statistics for electron and hole concentration instead of the default Boltzmann statistic, this will ensure more accurate results for the simulation.
In the Plot section the user can define a series of quantities that must be plotted in the results at the end of the simulation, with the following commands:

```
Plot
{
eDensity hDensity
TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
eMobility/Element hMobility/Element
eVelocity hVelocity
BandGap
ConductionBandEnergy
ValenceBandEnergy
ElectricField/Vector Potential
}
```

For our needs it essential to plot the Electric field to study the electrodes driving

capabilities. The next one is the Math section in which the user must specify the settings for the numeric solver as follow:

```
Math
{
Extrapolate
Derivatives
RelErrControl
Digits=5
Iterations=20
Wallclock
ExitOnFailure

}
```

Sentaurus device solves dynamic equation self-consistently on a discrete series of points described by the mesh. Iteratively the software tries to converge on a solution within a particular tolerance; By specifying Extrapolation we ensure that during a simulation step Sentaurus try to find a new solution based on the previous solutions found. With the command Derivatives the solution convergence is pursued with Newton's method with full derivatives. The other parameters are just to properly set the maximum number of iterations, the error tolerance, the dimension of the solution and the forced an eventual exit due to inability to reach a converged solution after the maximum number of iterations. The last section of the SDevice command file is dedicated to the Solving parameters as follow:

```
Solve
{
Coupled (Iterations= 100) Poisson
Coupled  Poisson Electron Hole

Quasistationary (InitialStep=1e-3 MinStep=1e-5 MaxStep=0.05
Goal Name="TopContact" Voltage= 3 )
CoupledPoisson Electron Hole
}
```

The solve section defines a sequence of consecutive operation to be performed on the device by the solver. The instruction are executed sequentially from top to

bottom. The first instruction solve Poisson equation for the initial biases condition defined in the ELECTRODE section, for both electrons and holes. In the Quasistationary section we define an appropriate goal for the electrodes biases, which it's reached in certain defined time conditions. Initially the voltage can be brought directly to 3 V, but in later chapters a variable generic value will be assigned as goal to allow the simulation of different biases exploiting the parameter function of Sentaurus project, allowing the goal definition as following:

```
Solve
{ ...

Quasistationary (InitialStep=1e-3 MinStep=1e-5 MaxStep=0.05
Goal Name="TopContact" Voltage= @V@ )
CoupledPoisson Electron Hole
}
```

By changing the internal parameter V in the project we are able to simulate different bias voltages, mainly 3V, 0V and -3V to simulated different phases useful during device characterization. This procedure is similar to the generic definition of the cell width used before. The voltage goal will be reached in a certain number of steps defined by the parameter in the round brackets, and at each steps Poisson equations are solved. In this case the simulation will reach the goal voltage around $1\mu s$.

2.3 Data Processing with SVisual and MATLAB

Once the electrical simulations on the structure have been completed, it is time to extract the simulated electric field data for post-processing. To do this, it is necessary to use the Sentaurus SVisual tool, which allows us to extract the required data directly from the simulated structure. By simply performing a series of axial cuts, we can obtain the electric field present in the central region of the device during the driving phase (that is, when the voltage on the top electrode has reached its maximum goal value). However, it must be taken into account that the field is simulated for every point of the mesh, resulting in a huge number of field values to work with. It is therefore appropriate to define a method for managing these simulation data, starting by determining at which height along the z-axis it is most suitable to take the field values. The vertical field is of critical importance for the proper operation

of the Reset command; if positive the electrodes driving voltage applies the 'NULL' state to the wire cell, causing molecule charges to delocalize toward the lower part, interrupting propagation. If the voltage is negative the molecule will be affected by a positive field and retrieved to an HOLD state when electrostatic interaction can happen and so propagation. The measurement procedure first involves selecting the correct height at which to make a cut and obtain all the values of the cross-sectional plane at that height. The point chosen for this operation is 1 nm from the bottom gold electrode, since this value was found to be most significant to study driving properties of molFCN cell [12]; as depicted in figure 2.3 the cell is vertically cut at z=6 nm to account for the 5 nm $SiO_2 - Titanium - Gold$ block. This value was obtained by examining the structure of the molecules typically used in this technology and determining the height at which a hypothetical field would have the greatest influence on driving the molecules . For a Closed design the particular structure, however, makes the electrodes configuration similar to that of a capacitor, ensuring, at least in theory, the uniformity of the field in the region of space between the electrodes.

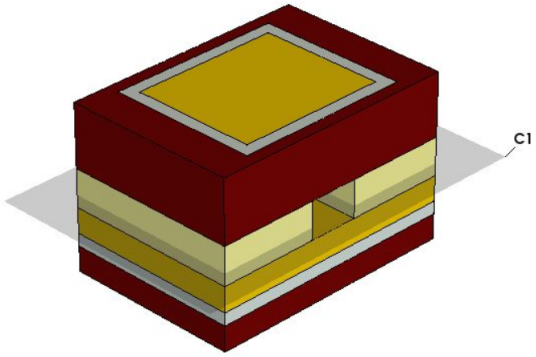
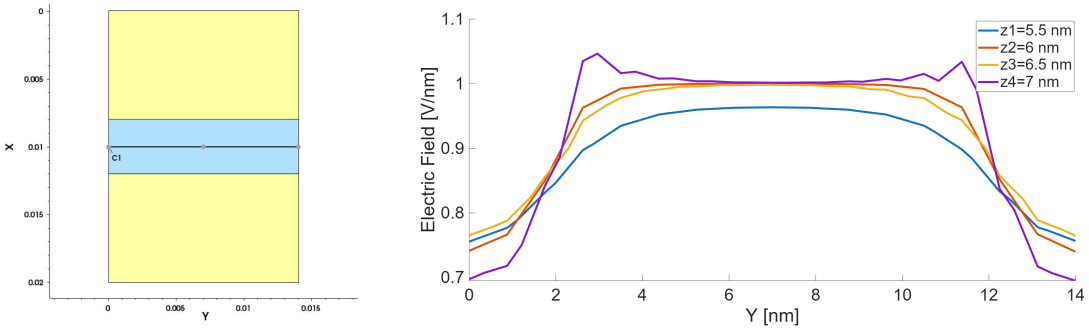


Figure 2.3: Z cut plane at z=6 nm

The z-cut performed at z=6 nm will be the standard for all simulations performed, to keep all future result consistent throughout the tests. Once performed the z-cut we are left with a plane in the x-y axis, so the next step will be to cut again along the x direction to obtain information about the longitudinal field distribution, and in the y direction to obtain information on the transverse field distribution.
A first analysis at the longitudinal field distribution along y is performed, to understand is role in affecting the longitudinal field distribution.

A comparison between z component of Electric field for different heights is shown in Figure 2.4, for a voltage applied of V_{el}=-3 V. The distribution along the middle point of the cell at x=10 nm for values of $z_1 = 5.5$ nm, $z_2 = 6$ nm, $z_3 = 6.5$ nm and $z_4 = 7$ nm shows good consistency, with maximum and minimum fields values differing only by $\Delta V = V_{z4} - V_{z1} \approx 0.05 V/nm$. By taking into account the ideal molecule VACT, as in figure 1.4, this ΔV variation is insignificant in terms of driving force needed to properly locate charge across DOTs.

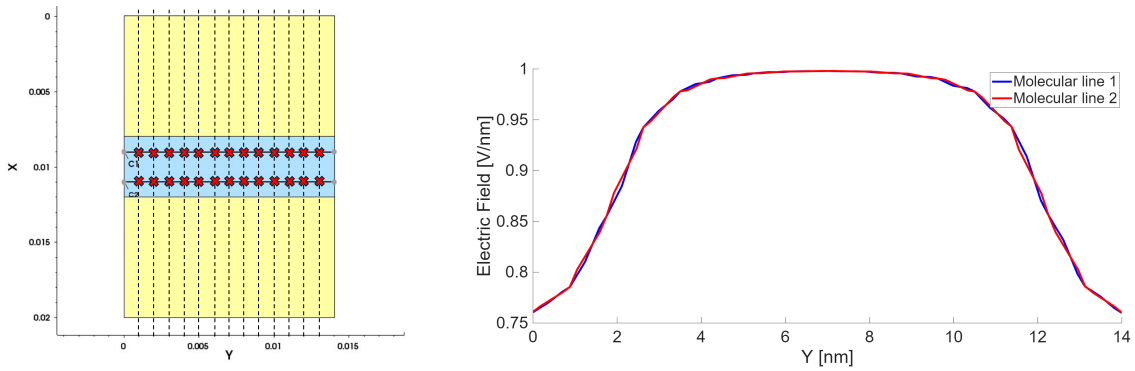


(a) x=10 nm cut

(b) E_z electric field

Figure 2.4: Longitudinal field distribution at different heights, 4 nm Wire

The field show consistency along the z range going from z=5.5 nm to z=7 nm, a characteristic guaranteed thanks to the electrodes capacitor-like structure; from this point forward a height of z=6 nm will be taken as the standard height for the field analysis. Regarding the field distribution along the y-axis, it is appropriate to relate it to the molecular distribution along the wire. For this study, it will be considered that the molecules are already attached along the lower electrode and distributed in a specific manner. The molecules are assumed to be arranged in an ordered grid, with a spacing of 1 nm between them along the y-axis and 2 nm along the x-axis; they are also positioned at a distance of 1 nm from the trench sidewalls. As example, this arrangement would results in two ordered rows of molecules located respectively at 1 nm and 3 nm from the trench sidewall for a 4nm wide wire, as depicted in Figure 2.5a; the red cross would be the ideal molecular position, in which the field values must be considered. The number of molecular rows is therefore always equal to the wire width in nanometers divided by two.

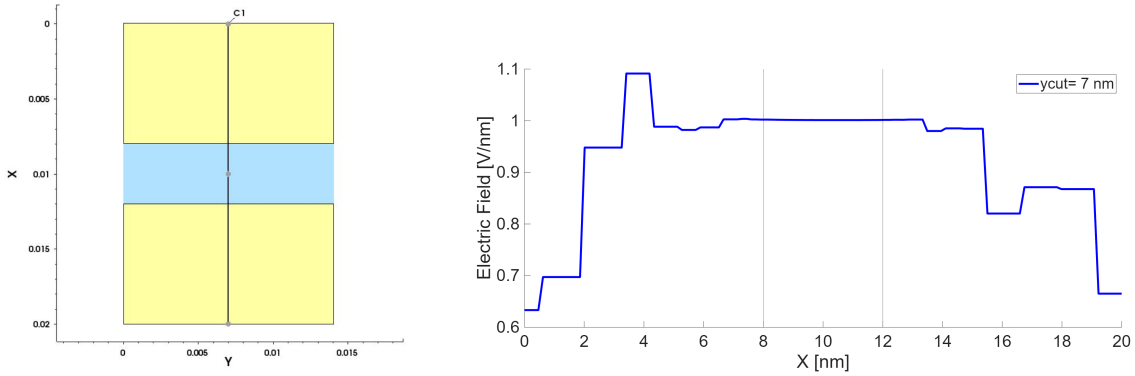


(a) Molecular position along x-cut (b) Lines E_Z field distribution along y-axis

Figure 2.5: X-cut field distribution, 4 nm wire

As it can be seen from the results in Figure 2.5b, the electric field is very consistent across the y axis in the range of space directly under the top electrode ($2nm \div 12nm$), expressing the capabilities of the Closed cell to drive the core region of the wire. This extraction procedure is performed automatically for all wire width variants of the closed cell by the Sentaurus Svisual tool. With a command script the correct number of cuts are performed on the structure, and the field extracted as .csv files, named accordingly after the cell type, its width and the line of molecules considered. For example in the aforementioned case, the first line of Ez values will be saved as "$CD\_4nm\_line1.csv$" array. This labeling enable a much more quicker post process in Matlab and SCERPA, including the main informations on the array of fields value directly in their name.

From the x-y plane originated from the zcut also the transversal electric field distribution can be analyzed, using the same driving conditions as before. By cutting the plane across y=7 nm the middle distribution can be extracted, in Figure 2.6:



(a) y-cut at y=7 nm (b) E_Z field distribution along x-axis

Figure 2.6: Y-cut field distribution, 4 nm wire

Apart from the perturbation on the external side of the cell, the stability of the field in the central core region ($8nm \div 12nm$) is evident from Figure 2.6b. The subdivision of the field values extracted from Svisual will be carried out in MATLAB, where, given the large number of values extracted from the respective .csv files, a discretization will be performed along the grid molecular positions. All these operations can be carried out directly within Sentaurus using Svisuals, a tool that not only allows us to graphically visualize the simulated structure, but also to perform a series of automated analysis operations through the use of a .tcl command file. Within this file, the coordinates at which to make the cuts are specified, as well as the quantities to extract and the data saving options. In this way, we can extract the absolute values of the electric field in the regions of interest and export them as .csv files for further analysis using data processing software such as MATLAB.
With this data analysis procedure, we will obtain a vector for each molecular line containing, for every grid position along the y-axis, a value of the Clock field acting on that specific point. In this way, we will be able to automatically handle these field values in the SCERPA tool to study wire propagation, determining whether, for the different structures under analysis, the fields will be sufficient to correctly influence the molecules.

2.4 Cell Simulation with SCERPA

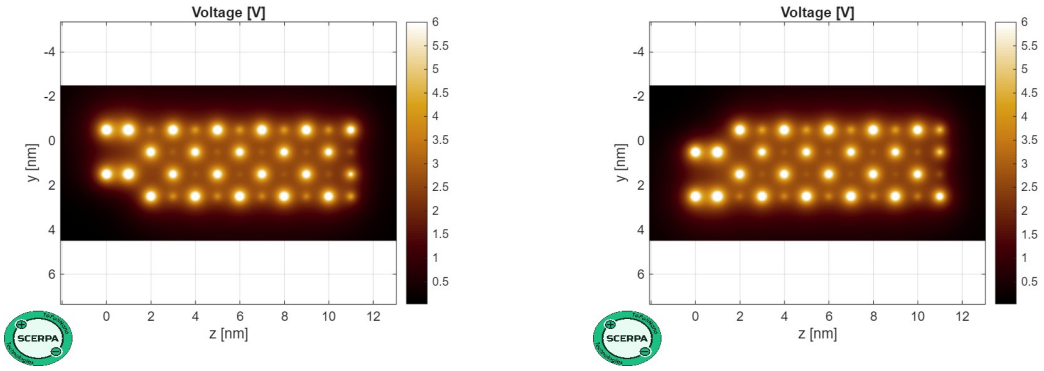
Electric Fields results are used with Self-Consistent ElectRostatic Potential Algorithm (SCERPA), a tool that simulate the charge localization of molecules in MolFCN circuits in an iterative manner. The tool is a series of Matlab scripts that, starting from ab initio simulations of molecule properties and electric field information, it calculates the electrostatic potential of the device layout, giving a qualitative description of how the design works [21]. This tool is essential to understand the wire behavior, especially to the different driving signals on the electrodes to force a particular state, such as RESET or HOLD states [14][12]. If a design is not capable of correctly propagating information or to guarantee the proper resetting, is not suitable for MolFCN, since the original information will be lost/changed. The way the fields are integrated in such tool is simple: once electrically simulated with SDevice and properly extracted trough Svisual, the field arrays ideally represent the electric fields along the y axis lines in which molecules are all placed trough the entire length of the device. In order to insert this field values inside SCERPA to simulate propagation, we need to first discretize them, considering only the values where we a molecule will be ideally place along the Gold layer. With this approxi-

mation we are capable of producing an array of EF value matching each molecules position; This is essential in building the proper set up for SCERPA, in which field distribution is integrated as arrays of field values. Since each pair of consecutive molecules represent a codified bit, it's good norm to consider only an even number of position across the longitudinal direction, to avoid inverting the original input. The fields data extracted and post processed into orderly arrays are now ready to be inserted inside the SCERPA tool. The script works starting with the definition of the main struct, called circuit; it contains all the relevant information about the device like its length, molecule type and geometrical disposition, Clock mode, phases step to simulate and input driver characteristic. All this specifics are saved within the same circuit struct to be easily accessible throughout the algorithm. The main parameters are defined inside the code as such:

- **circuit.name**: indicates the name of the circuit, which express in its form informations regarding it's properties, like phase distance, electrode length, cell width, ecc...
- **circuit.structure** : is a cell array that defines the device layout, expressing the geometrical grid of molecules and input drivers and their position inside the wire.
- **circuit.components**: is a cell array defining the type of molecules present in the wire; in this study it was the ideal molecule described in the introduction.
- **circuit.ClockMode**: defines the type of clock resolution used for starting the simulation. For this study a custom clockmode was developed for the inclusion of personalized phases steps.
- **circuit.stackstep/ circuit.inputseq**: two arrays of the same size that define a series of step to be simulated. Thanks to this variables a sequence of consecutive phases can be simulated, where each phase is characterize by a logic input (the same input for all the lines) and a state. The state is referred to a particular driving combination for the electrode, and it's identified by letters. More details on this will be delivered in chapter 4.
- **circuit.PhaseDistance**: indicates the distance between top electrodes for a multi electrode structure, or just the initial and final spacing for a single electrode cell.

Defined all the parameters of our design SCERPA algorithm can be launched. The main results of SCERPA simulations are represented by the potential plot, a plot

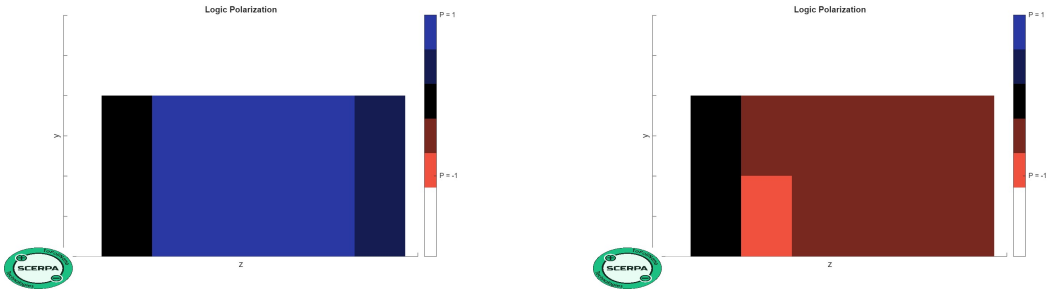
in which the potential peaks originated by localized charge are highlighted in the y-z plane (which correspond to the x-y plane of Sentaurus). One Potential plot is produced for every single clock step that was defined. This can be useful when studying multiple steps, allowing the user to get information about every single step. Another interesting plot is the Logic plot, which highlights the logic value associated with the different regions of the device, assigning for each clusters of nearby molecules a logic value based on the average charge configuration of that cluster. These plots are essential to verify the performances of a particular design, graphically showing how the circuit respond to the conditions imposed. As an example, the simulation of a W=4 nm cell gives the following plot:



(a) '1' Propagation Potential plot (b) '0' Propagation Potential plot

Figure 2.7: Example of potential plots for a 4nm Closed wire

In figure 2.7 the Potential plot for the '1' input configuration (on the left) and for the '0' input configuration (on the right) are shown; it can be appreciated how the charges on molecule react to the presence of a driving input, positioning themselves under the influence of electrostatic interactions induced by all the charges around them. Once the charges have localized, they will give rise to potential peaks arranged in the manner shown by the potential plots. To verify that the logical information propagates correctly, it is also possible to refer to the Logic plots, in which the logical values assigned to the molecular regions of the wire are highlighted, in blue for the logical value '1' and in red for the logical value '0', as shown in figure 2.8.



(a) '1' Propagation Logic plot (b) '0' Propagation Logic plot

Figure 2.8: Example of Logic plots for a 4nm Closed wire

The intensity of the color denotes the intensity of the charge localization. In our study, two factors are important for determining the performance of a wire: The first is whether the information provided as input at the beginning of the structure is correctly transmitted. This can be determined from both the Potential plot and, more importantly, the Logic plot. The second is whether the reset is performed correctly, that is, whether there is no residual potential in the Potential plot and no logical value in the Logic plot in the wire during the application of the reset signal.

2.5 working principle: Cell behavior

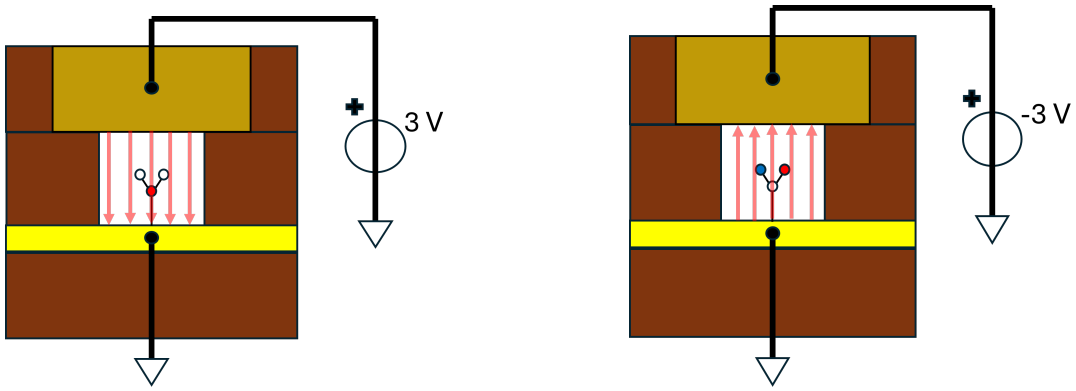
Having described all the procedure used to simulate the cell it is now important to express its operational conditions under which the analysis are conducted. In MolFCN logic circuits are divided into clock zone to control directionality and propagation of logic information; the delimitation of the clock zones are defined by the electrodes influence region. In the Closed cell design, the top electrodes exercise field control over the beneath wire region, defining the delimitation of clock zones. Only molecules that are influenced by the field distribution can be properly piloted, localizing charge into DOTs. Introducing single phase cell, we can study simulation of only one clock zone, instead of three like in the case of triphase wire. Indipendently from the number of phases the driving voltage applied to the top contact will produce effects on molecules governed by that particular electrode. The two main driving voltage simulated are 3 V and -3 V. The effect induced by this range of values are:

- 3 V applied: piloting the contact with a positive voltage values will produce a negative electric filed inside the core region, localizing charges in the lower section of the molecule and resetting information. This condition is used after information is propagated through the section, and there is the need to ready

it for the next one.

- -3 V applied: piloting the contact with a negative value will produce a positive electric field in the core region, localizing charge towards upper part of the molecule, thus holding information. This condition is used to hold the charge configuration during electrostatic interactions, to allow all the charge to correctly polarize, reproducing input configuration.

A schematic representation of the two possible solutions for the applied bias is depicted in Figure 2.9.



(a) Positive bias applied (b) negative bias applied

Figure 2.9: Phase schematic representation

If the device is a triphase wire, meaning that the upper part is composed of three electrodes, the combinations of the three field will defined how the sections of the device will behave in time.

Chapter 3

Trench and Closed design comparison

In this chapter a performance comparison between the Trench and the Closed design is presented, in order to demonstrate how the structural differences between the two configurations affect the electric field distributions and, consequently, their driving capabilities. We will begin with a brief analysis of the trench structure, highlighting its main characteristics and the advantages it offers in terms of fabrication compared to its counterpart. This will be followed by electrical simulations similar to those performed for the Closed cell, studying the results. Once the electric field values have been obtained, a direct comparison with the closed device will be carried out, analyzing the performance of devices for different widths, specifically 4 nm, 16 nm, and 32 nm. This will allow us to understand how the difference in terms of electrodes arrangement influences the field distribution, especially for different width. Lastly cells simulations are carried out in SCERPA, to better understand how the devices behave in terms of resetting capabilities, driving behavior and information propagation.

3.1 Trench Design

The structure of the device consists of a trench etched into a SiO_2 layer, onto which gold electrodes are subsequently deposited. The gold layers are placed on the floor of the trench and on its two sidewalls, with adhesion ensured by a titanium layer acting as an adhesion layer. From a fabrication standpoint, the structure offers significant advantages over closed designs, as it does not require techniques such as wafer bonding. Moreover, the open configuration allows for the attachment of molecules after fabrication is complete, rather than in the middle of the process. This aspect is crucial, as once positioned on the substrate, the molecules are very sensitive to processes involving heat or chemical agents that could damage them.

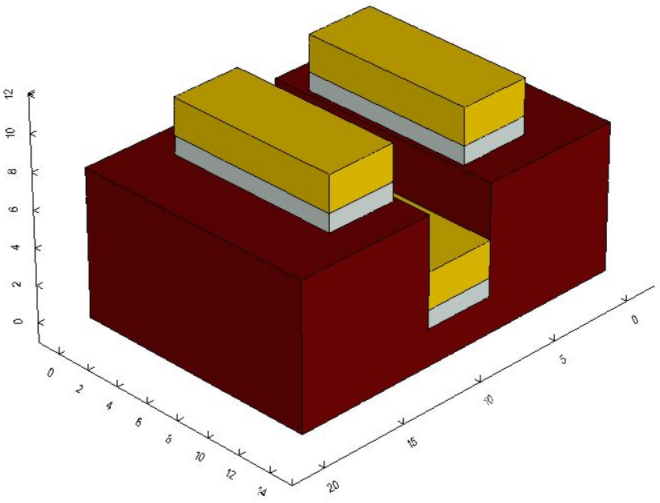
The device was simulated using procedures very similar to those described in the second chapter, with the only differences being a different SDE file for generating the trench structure and a different SDevice file to account for the presence of three electrodes instead of two. Conceptually, however, the procedures remained the same in order to ensure the comparability of the results. Some important notes must be reported: firstly, the open structure without an upper boundary layer required a decision regarding the upper limit of the simulation domain, which was defined by the geometry of the vacuum material used to fill the intermediate space of the device. For this particular application the trench was filled with Vacuum up to 2 nm over the top electrodes, completely engulfing the core region of the device; by doing this we are sure to match the simulation conditions of the Trench design with the Closed one for proper confrontation.

Secondly, to account for errors and imperfections of deposition processes, a small spacing of 0.01 nm on the x-axis was introduced between the top electrodes and the edges of the two vertical walls of the trench. For what concern the geometrical dimensions of such device they are kept as close as possible to the Closed design, in order to work with cells that are very similar in terms of length, width and height. The dimension used for a 4 nm wide Trench cell are :

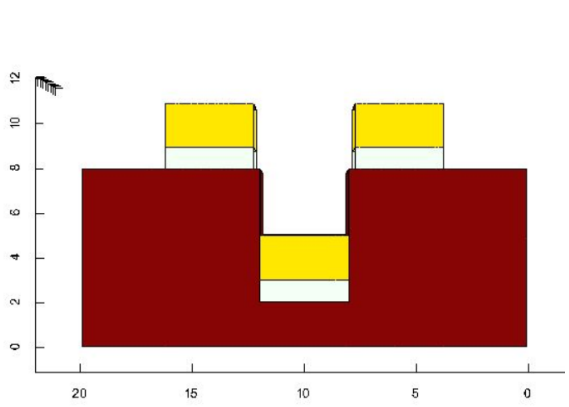
- **Y-axis**: The device extend along y for 14 nm total, with 10 nm occupied by the gold top electrodes on top of the trench. The bottom gold layer runs for the entirety of the device length.
- **X-Axis**: the Trench device total width is defined by the wire width and the SiO_2 wall thickness; the simulated dimensions are 8 nm for the walls thickness and a variable size range for the width, ranging from 4 nm to 32 nm (4 nm,16 nm and 32 nm).
- **Z-Axis**:A 2nm thick SiO_2 bottom layer was considered, with a 1nm Titanium and 2nm Gold layer on top, in the middle of the trench. At the top of the walls 2 electrodes of the same thickness of the middle one are placed, and the structure is filled with Vacuum 2 nm over the top.

The complete structure is shown in Figure 3.1; apart from the attachment processes, the Trench cell offers advantages from a fabrication point of view, not requiring additional wafers for the complete structure; since the top electrodes are the driving contacts producing the electric field in the core region, their position with respect to the bottom grounded Gold layer is crucial. As it will be analyzed in this chapter,

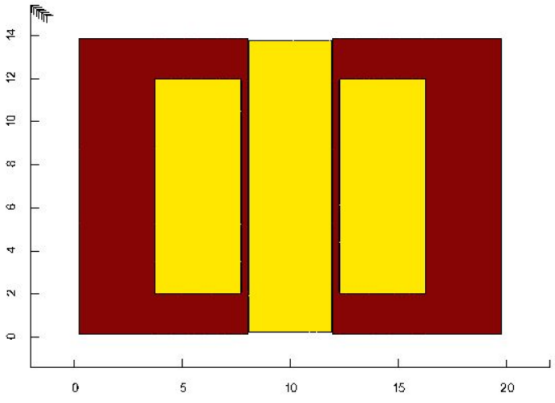
the Trench design electrode positioning is detrimental for field distribution the more the width of the cell width increase.



(a) Trench Device general view



(b) Trench Device frontal view



(c) Trench device top view

Figure 3.1: Trench Device Structure

3.2 Longitudinal Electric Field analysis

In this first section, a study on the y-direction distribution of the field is carried out, comparing both designs to highlight their differences; the confrontation is performed on two geometrically similar cells, for different widths ranging from W=4 nm to W=32 nm. The longitudinal field is taken from a cut performed in the middle of the core region, at z=1 nm. Due to the presence of the dielectric walls, the cut is performed at x=10 nm for W=4 nm, x=16 nm for W= 16nm and x= 24 nm for 32 nm wire. The absolute electric field distribution for applying a voltage of 3 V to the upper electrodes of both design is then analyzed for the aforementioned widths.

3.2.1 Single phase 4nm wire

For a W=4 nm wire the obtained distribution is depicted in Figure 3.2:

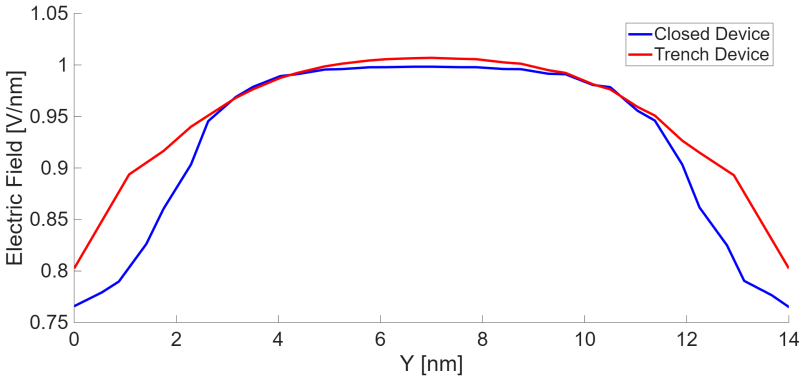


Figure 3.2: Y Electric Field distribution, 4 nm wire

The small trench dimensions of a 4 nm wire ensure that the longitudinal field distribution of the Trench device is very similar to the Closed one. At z= 1 nm for both devices we obtain field values around 1 V/nm in the middle region, which are adequate to properly drive the ideal molecule considered for this study. This results highlight similar working conditions for the designs, so their propagation behaviors in SCERPA simulation are expected to be similar. From the graph a drop can be appreciated in the boundary regions external to the 10 nm clock zone range along y axis; the field in this region will be important later in determine the performances of a Triphase wire. For this kind of device the interstitial region between two consecutive electrodes is critical in determining propagation behavior, since the core section in this area will not be directly driven by the top field. For this comparison however the distribution in the external region is not important, since the focused is given to the distribution inside the clock region, to study how electrodes positioning with respect to the grounded bottom affect performances.

3.2.2 Single phase 16nm wire

For a W=16 nm wire the obtained distribution is depicted in Figure 3.3:

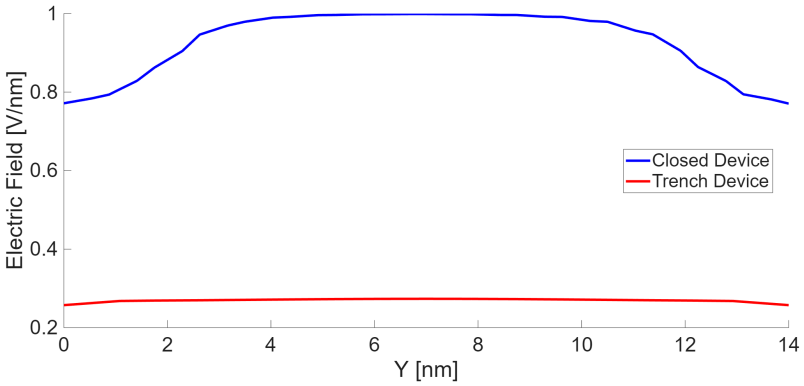


Figure 3.3: Y Electric Field distribution, 16 nm wire

With a larger gap between the bottom electrode and the top ones, the Trench design struggle to keep consistent it's performance, with electric field strength dropping rapidly as the wire gets larger. By looking at figure **??** the difference between distribution of the two design are quite clear, the Trench one struggles to reach values of 0.3 V/nm, with the maximum being 0.25 V/nm at the center. The Closed one keep it's field distribution consistent with the 4 nm width Closed one at 1 V/nm.

3.2.3 Single phase 32nm wire

For a W=32 nm wire the obtained distribution is depicted in Figure 3.4:

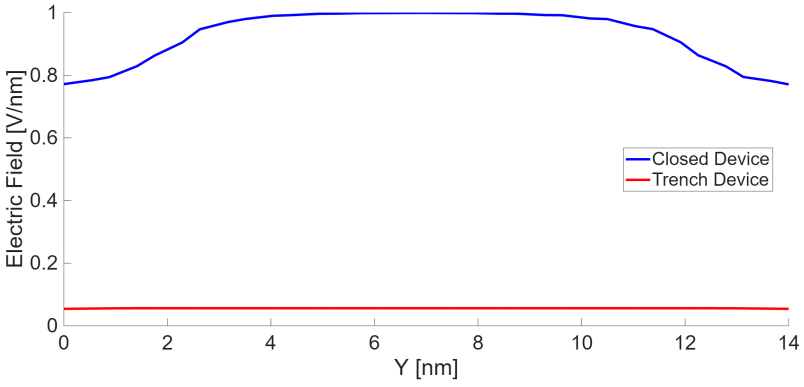


Figure 3.4: Y Electric Field distribution, 32 nm wire

The trend continues for the W=32 nm wire, where the field reaches values near 0.05 V/nm along the entire length of the device. Molecules along this direction will basically be unaffected by the electric field, making impossible to control the allocation of their charge through electrodes force. In these points reset will not be

possible.
The Close model, on the other hand, is consistent with the previous W=16 nm and W=4 nm results.

3.3 Cross Electric Field analysis

As previously defined, the electric field of the two structures is taken at a height of 1 nm from the bottom electrode to which the molecules are attached, which in both cases corresponds to the gold layer at the base of the devices. Once the x–y plane intersecting the z-axis at the desired height is obtained, the analysis along the two axes can proceed to evaluate the field distribution. The field considered along the x-axis is useful for understanding the driving force within the internal regions of the wire, particularly for very wide wires since the number of adjacent molecular lines increases linearly with the width. In general, we expect the molecules to be laterally spaced 2 nm apart between them, 1 nm from the edges of the structure, and 1 nm longitudinally. Therefore, for a 4 nm wire, we will expect two molecular lines along y direction, for the 8 nm wire we expect four lines and so on. We begin with an initial simulation of the electric field of the two devices and compare the electric field along the x-axis by fixing y=6 nm, positioning ourselves at the center of the clock region. As done for the longitudinal analysis, these simulations are performed for increasing wire widths, starting from 4 nm to 16 nm to 32 nm.

3.3.1 Single phase 4nm wire

In this section a 4 nm wide, 3 nm heigth Trench and Close cell are simulated , with the upper electrodes of both design set to -3V. The quantity analyzed is the absolute Electric Field computed at y=7nm and z=1nm, so we are looking at the transverse field in the core region. We can observe in figure 3.5 how both devices provide a stable and uniform field in the region of interest, with some expected differences in the distribution due to the different electrode spatial configurations. As anticipated, the field of the Closed device is very uniform and constant, expressing its capacitor-like configuration capabilities. As for the trench device, we can observe peaks in correspondence of to the x positions of the upper electrodes; this peaks tend to diminish toward the central region. This was an expected result, confirming the lower driving force for molecules located at the center. The graph highlights the points of interest where molecules are expected to be present by marking them as dots on the field distribution; these dots are placed in compliance with the molecule line position expressed in the previous chapter, i.e. the x points where the lines should

run . In this case, since the internal region is 4 nm wide, we expect molecular lines to appear at x_1=9 nm and x_2=11 nm positions (assuming, of course, lateral dielectric wall of width equal to 8 nm). This graphing method is useful to immediately assess the driving strength of the fields at the points that will later be used in SCERPA simulations, forming the specific electric field input applied to the molecules. Regarding the 4 nm device, we can observe that the differences are minimal in terms of absolute field value and its stability, emphasizing how a trench-based technology is capable of providing sufficiently strong fields for very narrow wires, with absolute values higher than 1 V/nm. Given its simpler construction compared to the closed counterpart, this could suggest a the possible implementation of the design for thin wire applications.

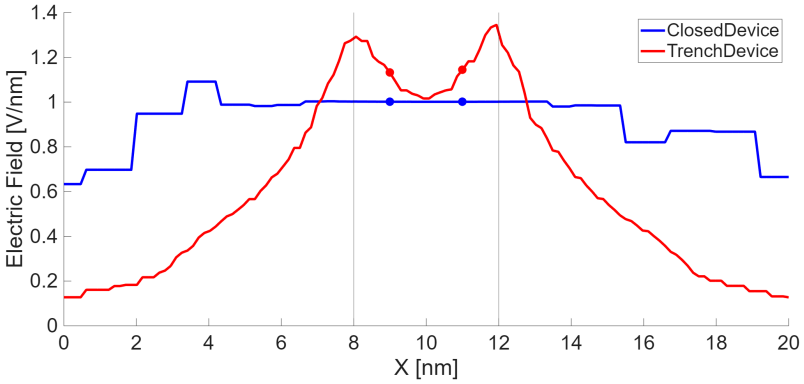


Figure 3.5: 4nm Wires x-Electric Field comparison

3.3.2 Single phase 16nm wire

In this section a 16 nm wide core is simulated for both design, with their upper electrodes set to -3V. As we can see from the simulation results 3.6, by increasing the width of four times with respect to the 4nm width already produces a huge drop in the strength of the field in the central region of the trench structure, with values reaching a 0.3 V/nm. From the simulations results we can appreciate how the molecules closer to the edge in Trench cell are affected by a field comparable to the Closed design, due to their proximity to the upper electrodes. The closed device on the other hand keeps it's consistency of 1 V/nm across the 16 nm core length.

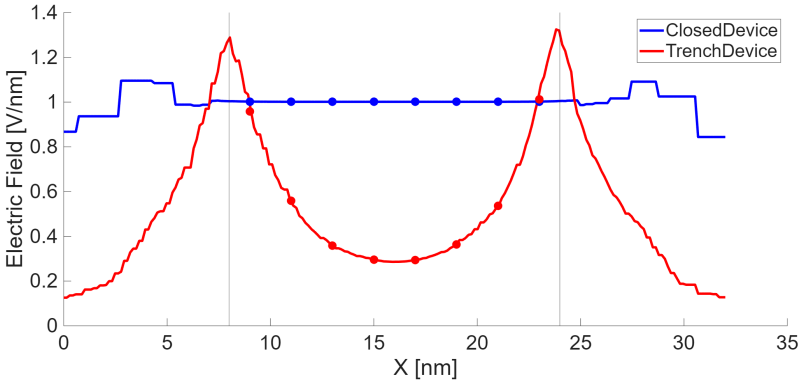


Figure 3.6: 16nm Wires x-Electric Field comparison

3.3.3 Single phase 32nm wire

In this section a 32 nm wide, 3 nm heigth trench is simulated , with the upper electrodes of both design set to -3V. As we can see from the field distribution of the trench device 3.7, there is a significant drop in the center region, highlighting a poor driving capability of molecules due to the excessive distance from the top electrodes, with values below 0.2 V/nm. In contrast, the superior design of the closed device shows excellent and consistent driving capabilities of roughly 1 V/nm along the entire cross-section of the wire. This result clearly confirms what was expected, emphasizing the limitations of an open design as the wire size (and consequently the number of encoded bits and the amount of transmitted information) increases.

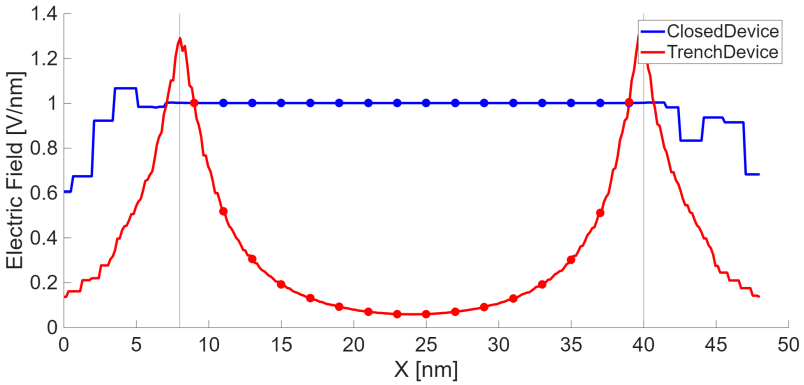


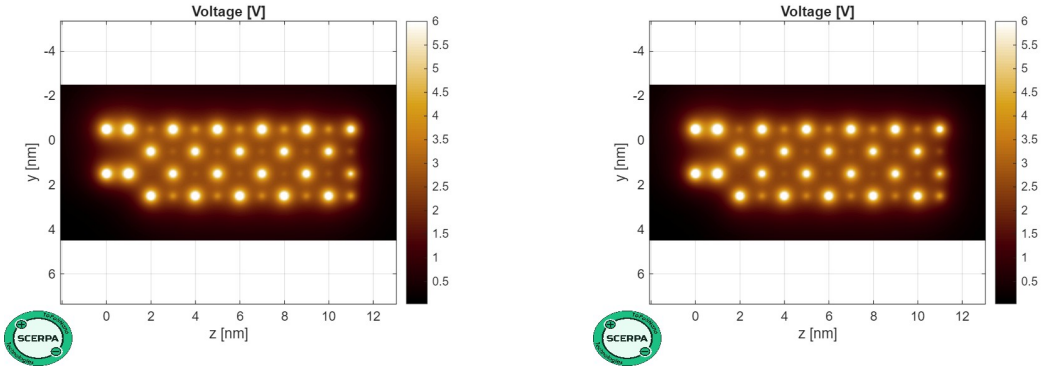
Figure 3.7: 32nm Wires x-Electric Field comparison

3.4 SCERPA simulation: Driving capabilities

In this section the comparison is carried on to SCERPA, where the electric field values across the y axis are used as input to study charge aggregation and propagation across all the molecules of the wire. For each width the electrodes of both design are changed from 3V to 0V to -3V in order to simulate a proper set of states to study information propagation and understand wire behaviors. For a driving value of 3V the resulting electric field on the molecule will be negative, around -1 V/nm or higher depending on width and design choice as seen in the previous graphs. This field describe a RESET state, a state in which the charge is localized towards lower DOTs on the molecule, cutting off information propagation. This is used in combination with multiple electrodes to built clock zones useful to impose directionality and control over the bit travel across the wire. For 0 V the state is described as NULL, with basically no electric field active in the structure; This state is useful to ensure an intermediate field value on the molecules, in order to avoid abrupt transitions between HOLD and RESET states, giving the simulator time to adjust the involved charge values. Finally with -3V on the top electrodes the electric field will be positive describing a HOLD state. Here the charges are distributed in the upper DOTs of molecules ready for propagation. The difference in terms of field strengths and distribution cross the structure of the two design will also dictate how the wires will behave when cycled trough the different states.

3.4.1 single phase 4nm wire

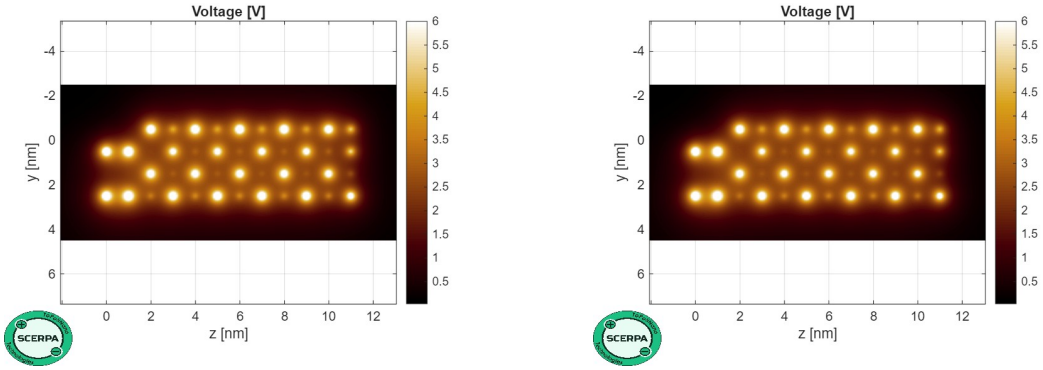
In this section a 4nm wide, 14nm long Trench and Closed wire structure are simulated; the results of the SCERPA simulations for input logic '1' input are depicted in figure 3.8, where the Potential plots on the y-z plane (which is corresponding to the x-y plane of Sentaurus) of the 2 design are shown. It can be observed the two main rows of molecules traversing the entire length of the device as potential points, propagating the logic input from the drivers on the left to the output on the right. In the HOLD state, when a -3V is applied to the upper electrodes, both layouts offer great driving capabilities, allowing electrostatic interaction between charges along the wire. For this comparison a logic '1' configuration of drivers was used (on the far left).



(a) Closed Design (b) Trench Design

Figure 3.8: Driving voltage distribution HOLD state, logic '1', 4nm wire

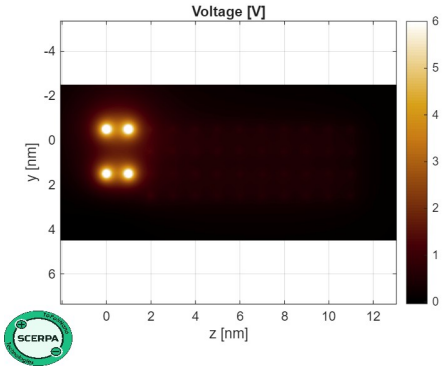
The propagation of logic '0' is also very good for both devices, as it can be seen from the following potential plots in Figure 3.9:



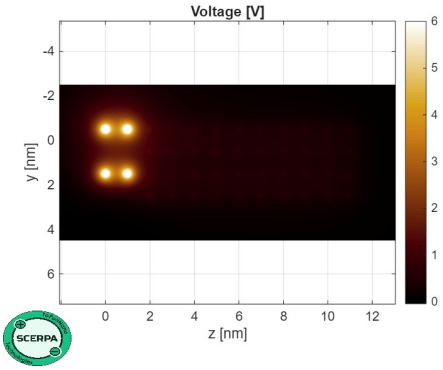
(a) Closed Design (b) Trench Design

Figure 3.9: Driving voltage distribution HOLD state, logic '0', 4nm wire

A RESET state can be imposed by applying a positive voltage to the upper electrodes, setting electrodes at 3V. SCERPA results for this case are shown in figure 3.10. Here the reset capabilities allow both design to properly reset thanks to the high influence of the electric field inside the core region of such narrow wire, so the lines are completely reset with no information propagated.



(a) Closed Design

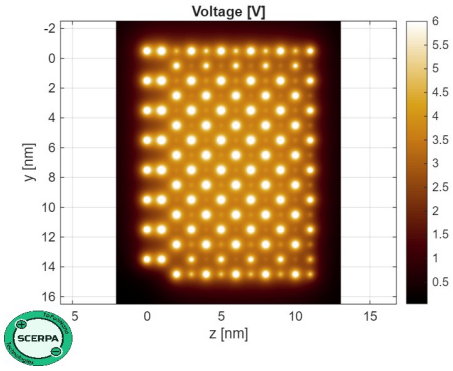


(b) Trench Design

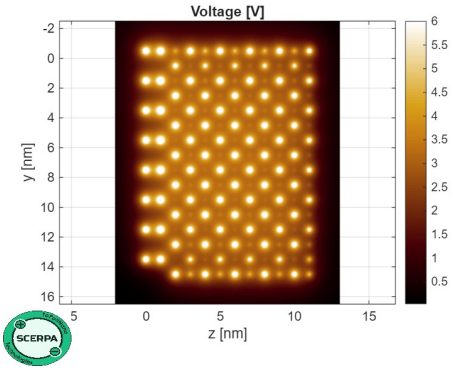
Figure 3.10: Driving voltage distribution RESET state, 4nm wire

3.4.2 single phase 16nm wire

For Trench and Closed wires of 16nm width the results obtained are shown in Fig.3.11; for what concearn the HOLD state the two designs behave quite good, thanks to the small driving voltage needed to localized charge in the ideal molecule used for the simulations (as stated by the VACT graph). Both layouts are capable of propagating logic '1' across the wire for a driving voltage of -3V.



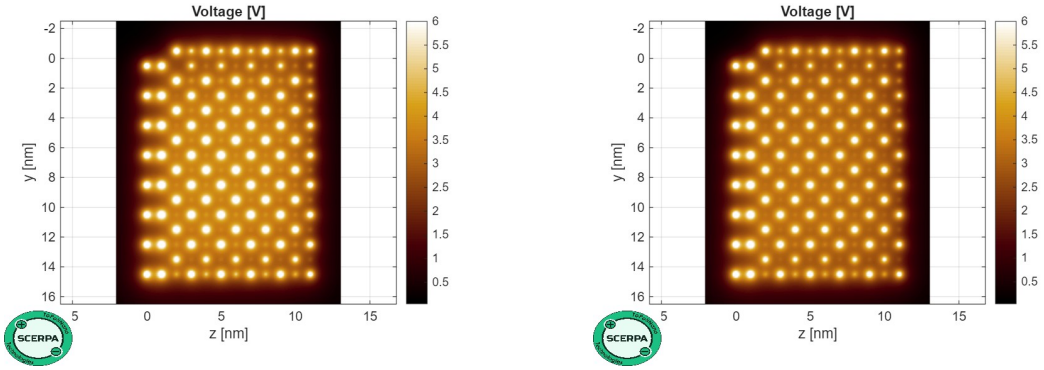
(a) Closed Design



(b) Trench Design

Figure 3.11: Driving voltage distribution HOLD state, logic '1', 16nm wire

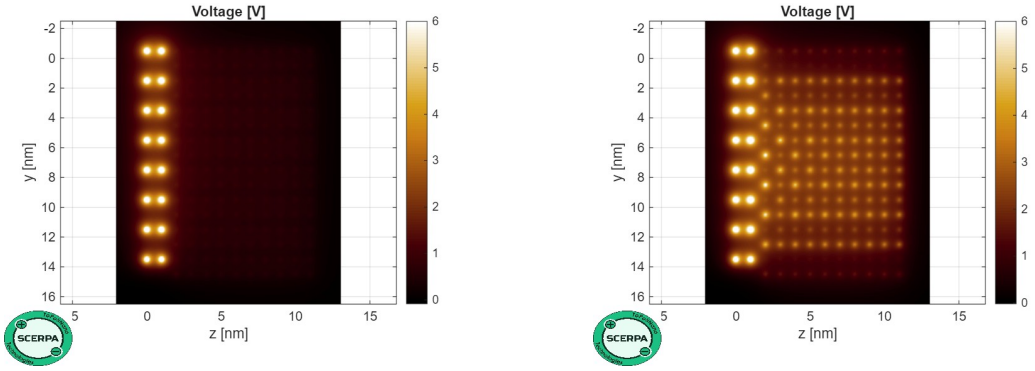
The same can be said for the propagation of the logic '0', again shown in the following potential plot, Fig.3.12:



(a) Closed Design (b) Trench Design

Figure 3.12: Driving voltage distribution HOLD state, logic '0', 16nm wire

By looking at the RESET state, in Fig. 3.13, the limits of the trench design start to show. In fact the wire cannot be properly reset, with only the molecule lines near the trench wall be correctly affected by the vertical electric field. The inability to perform the reset by this design it's an indication on it's limits when approaching high widths, resulting in poor performances. An improper reset of the cell can lead to residual information left in the wire, affecting the next propagation cycle and creating unwanted output.

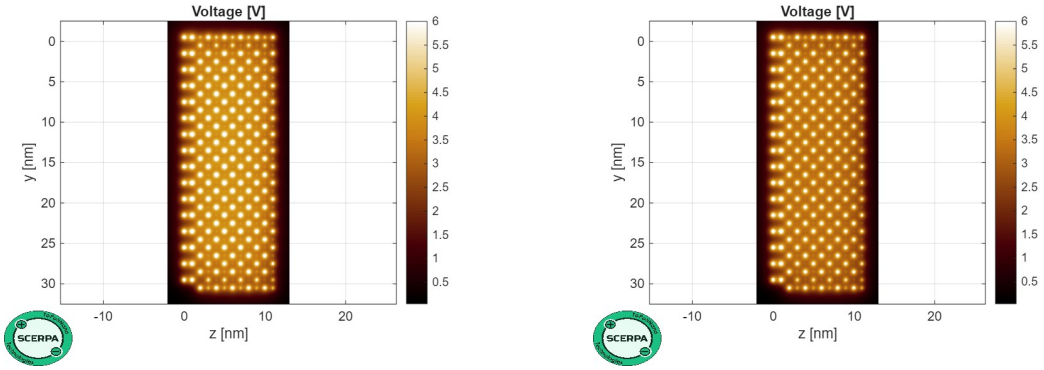


(a) Closed Design (b) Trench Design

Figure 3.13: Driving voltage distribution RESET state, 16nm wire

3.4.3 single phase 32nm wire

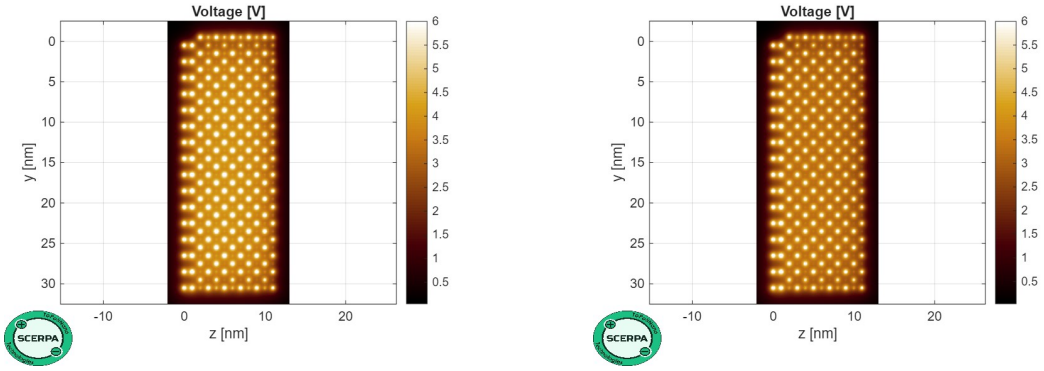
For a width value of 32 nm both designs show the proper capability in holding charges during HOLD state, correctly propagating the input to the end of the line. The behavior in the HOLD state is depicted in Fig. 3.14 and like for the previous results, is quite consistent for both cells. This is again thanks to the low V_{in} needed to locate charges in the ideal molecule.



(a) Closed Design (b) Trench Design

Figure 3.14: Driving voltage distribution HOLD state, logic '1', 32 nm wire

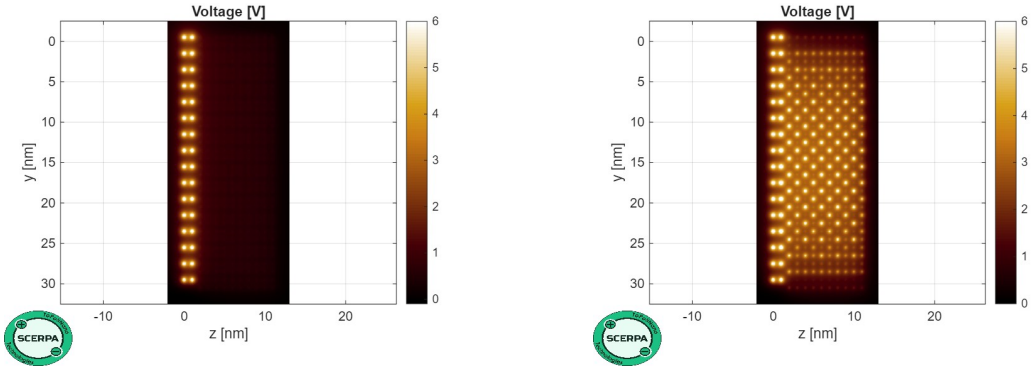
Same thing can be observed for the logic '0', information is correctly propagated trough the wire, as in Figure 3.15.



(a) Closed Design (b) Trench Design

Figure 3.15: Driving voltage distribution HOLD state, logic '0', 32 nm wire

The difference between cells during RESET state is more marked at this width, figure 3.16, showing that the trench device design is completely inadequate in properly reset the central molecules in the core, resulting in incorrect behavior during the reset cycles. As shown in the previous section this is due to the high distance between the deep central molecules and the top side electrodes, which cannot produce high enough fields in the inner regions of the wires. Due to the capacitor nature of the closed device electrodes, this problem is not present in this kind of device.



(a) Closed Design (b) Trench Design

Figure 3.16: Driving voltage distribution RESET state, 32nm wire

3.5 SCERPA simulation: Input change

In this section a sequence of clock steps was simulated to analyze the input switching behavior of the two designs, by changing the input drivers from a logic '1' configuration to a logic '0' configuration during a reset state. The wires analyzed in this part will be only the 16nm and 32nm ones, since for a width of 4nm the two layout perform very similar. A 8 clock steps sequence is applied, changing the electrode voltage 8 times to simulate 8 clock steps that will corresponds to a HOLD-HOLD-NULL-RESET-RESET-NULL-HOLD-HOLD chain of states. During simulations on SCERPA is better to avoid abrupt change between states, that could lead to errors during charge propagation due to molecules reaction time. For this reason, a third NULL state is introduced, corresponding to a 0 V applied to the electrodes: this will smoothen the transition from between RESET and HOLD states, allowing time for the molecules to be correctly influenced by the fields. For this particular section, the input is change from '1' to '0' at the second reset step, followed by a null state for the aforementioned reasons. A diagram for the applied voltages and input is represented in Fig. 3.17.

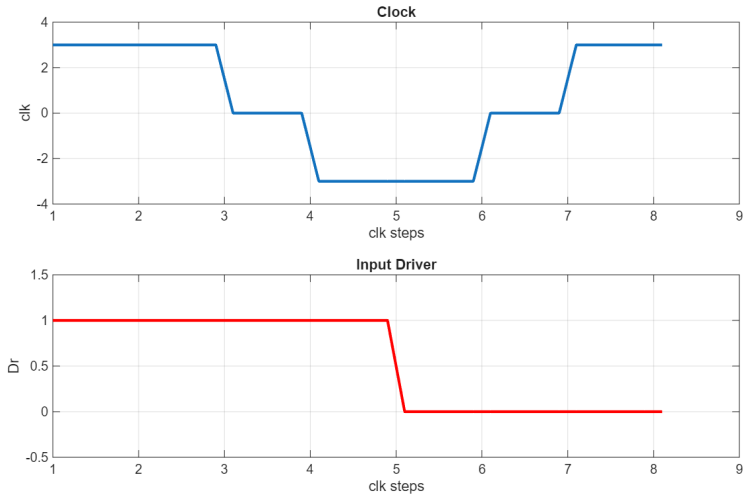


Figure 3.17: Input and States sequence Diagram

During input switching analysis we are simulating trough a series of phases a logic change in the input information, so it will be necessary to identify if the analyzed designs presents critical failure in propagating such change across the entire wire length. If a wire is not capable of propagating the new changed value, is not suitable for technological application. To better understand the differences between Closed device and Trench device we will study both potential and logic plot resulting from SCERPA. The results shown in the potential plots and logic plots in this chapter, concerning input switching, refer only to specific steps of the simulation, in order to

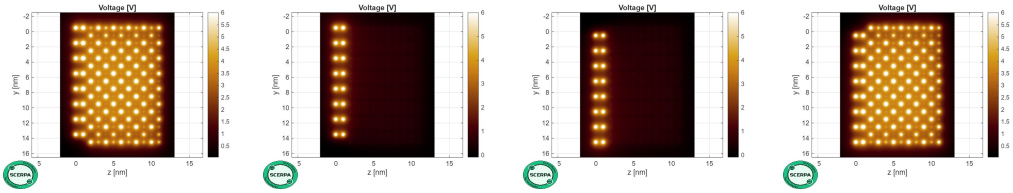
highlight the critical transitions that determine whether correct propagation occurs within the wires or not. These steps, numbered from 1 to 4, refer to:

- **Step 1)** : Initial HOLD state to propagate logic '1' across the wire
- **Step 2)** : First RESET state to stop the propagation '1'
- **Step 3)** : Second RESET state while input changes from '1' to '0'
- **Step 4)** : Final HOLD state to propagate logic '0' across the wire

As mentioned above, these steps are not the only ones simulated, but only the most significant ones. It should be noted that a series of intermediate NULL steps were included to facilitate the molecules response time and improve propagation before each input change.

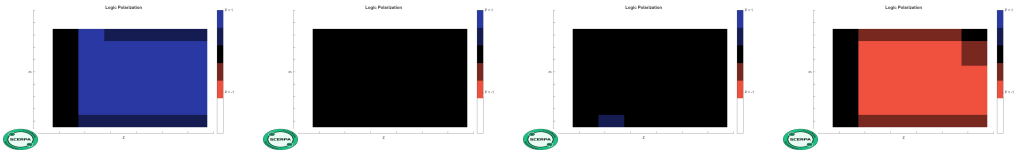
3.5.1 single phase 16nm wire

Starting with the 16nm wide, 14nm long single phase Closed wire, the results obtained by SCERPA simulation are collected in Figure 3.18, followed by the Logic plots of the same step in Figure 3.19 :



(a) step 1 (b) step 2 (c) step 3 (d) step 4

Figure 3.18: Input switching Closed wire 16nm width

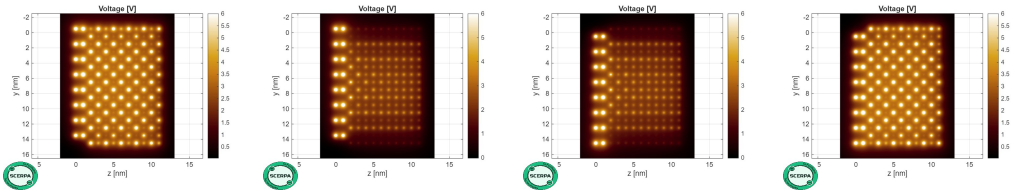


(a) step 1 (b) step 2 (c) step 3 (d) step 4

Figure 3.19: Input switching Closed wire 16nm width Logic Plot

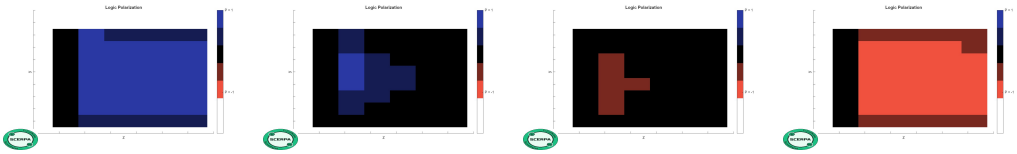
For what concern the input switching, the potential plot in figure 3.18 highlighting the 4 main steps show how the Closed device is able to properly reset the wire, propagating correctly both logic '1' and '0' to the output. This results can be better appreciated trough the Logic Plots in figure 3.19; here the propagation of

'1', represented by the blue zones, and '0' represented by red zones, are shown. By looking at the 4 steps both inputs are correctly propagated trough the wire and the switching is successful.
The same simulations for the analogous Trench device are repeated. The results represented by the Potential plots are depicted in Figure 3.20, followed again by the Logic plots in Figure 3.21:



(a) step 1 (b) step 2 (c) step 3 (d) step 4

Figure 3.20: Input switching Trench wire 16nm width



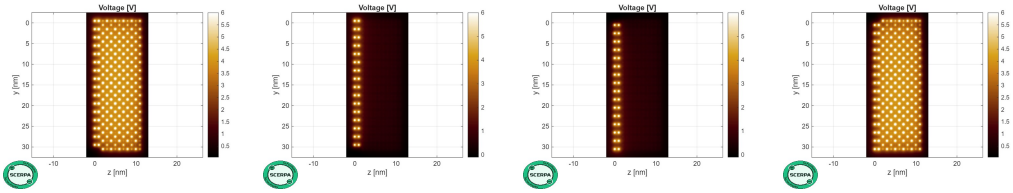
(a) step 1 (b) step 2 (c) step 3 (d) step 4

Figure 3.21: Input switching Trench wire 16nm width

From the simulation results in figure 3.20 we can understand how the resetting of the trench design is problematic; even if the propagation of both '1' and '0' is successful across the wire the inability to reset charges in the central molecule rows could lead to errors in a complete circuit, especially for longer wires. The incorrect reset behavior is shown in figure 3.21, during the reset cycle at steps 2 and 3 the presence of a residual logic value can be seen. This means that in this specific clock zone, the wire is not reset completely. We further our investigation with the study of the 32nm wire, to better appreciate the detrimental effect on field control of Trench design for wider wires .

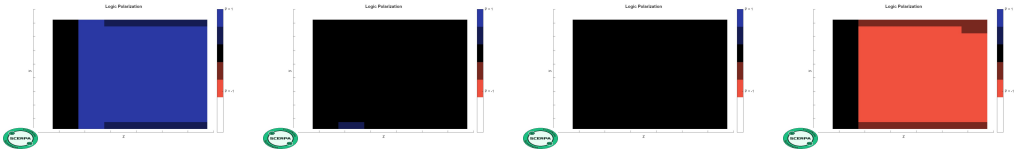
3.5.2 single phase 32nm wire

We repeat the same simulation procedure for a 32nm wide, 14nm long wire, trying to understand how width affect input switching. All the other parameters are left untouched from the previous analysis. For the Closed device the results are depicted in Figure 3.22 and Figure 3.23:



(a) step 1 (b) step 2 (c) step 3 (d) step 4

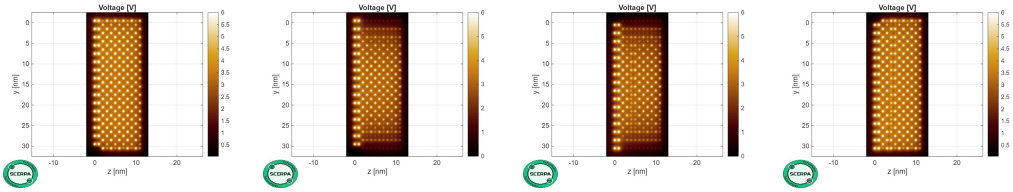
Figure 3.22: Input switching Closed wire 32 nm width



(a) step 1 (b) step 2 (c) step 3 (d) step 4

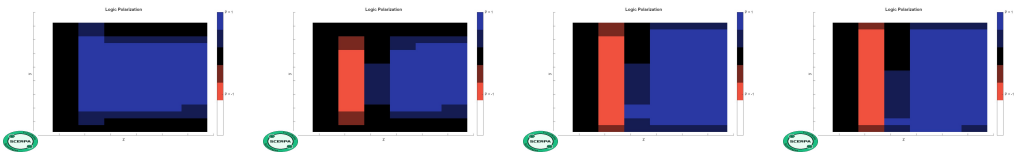
Figure 3.23: Input switching Closed wire 32 nm width

From figure 3.22 it can be verified that the input switching occurs without any error across the entirety of the wire, correctly propagating both '1' and '0'. The Logic plots conferm the correct wire behavior for the Closed design. The simulations are repeated for the similar Trench wire, obtaining the results depicted in Figure 3.24 and 3.25:



(a) step 1 (b) step 2 (c) step 3 (d) step 4

Figure 3.24: Input switching Trench wire 32 nm width



(a) step 1 (b) step 2 (c) step 3 (d) step 4

Figure 3.25: Input switching Trench wire 32 nm width

As it can be seen in figure 3.24 at step 4, the input is not correctly propagated to the output end of the wire due to an improper reset between step 2 and 3; W=32

nm is a too wide dimension for this kind of design to guarantee the proper working mechanism. A further analysis of this can be carried out analyzing the logic plots, in figure 3.25, which indicates the presence of both logic '1'and '0' regions overlapped in the middle zone after step 2, denoting a failure in propagation. This device is not suitable to operate in MolFCN logic circuits.

3.6 Results

A detailed comparison between the trench and closed designs has been presented, highlighting the key differences in structure and performance. The results from the electric field simulations and SCERPA analyses show how the Trench design, while advantageous in terms of simpler fabrication processes, faces significant failures as the width increases. For narrow wires (4 nm), both designs perform similarly, providing sufficient driving capabilities and stable electric fields for proper information propagation and resetting capabilities. However, as the wire width expands (16 nm and 32 nm), the Trench ability to deliver a consistent driving force deteriorates. This is caused by the increasing distance between the central molecular regions and the top electrodes, leading to insufficient field strength for effective charge localization.

The SCERPA simulations further illustrate these limitations, particularly in terms of reset performance. In wider wires (16 nm and 32 nm), the trench design struggles to reset the central molecules correctly, resulting in incorrect propagation during the reset cycle. On the other hand, the closed design maintains robust performance across all wire widths, demonstrating consistent field strength, excellent reset capabilities, and efficient information propagation. In conclusion, while the trench design offers certain advantages in terms of fabrication simplicity and potential for thin wire applications, its performance in wider wire configurations is limited. As the width increases, the trench design becomes less viable for practical applications, especially in circuits where reliable logic state propagation is required. The closed design, with its more consistent and uniform electric field distribution, proves to be a more suitable choice for larger wire widths.

Chapter 4

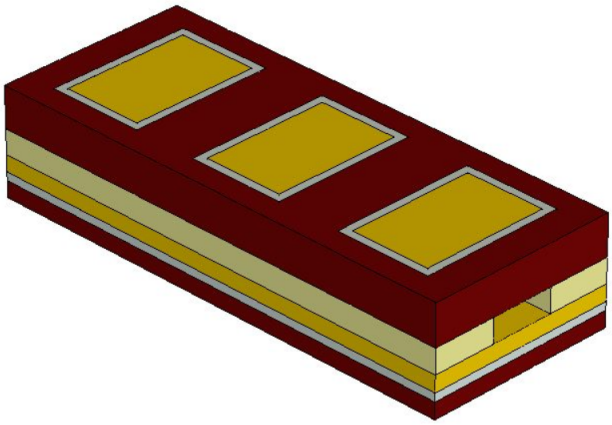
Three-phase wire analysis

In this chapter the three-phase Closed wire is analyzed; it consists of a wire device composed by three single-phase cells united together to form a single structure, characterized by a common gold bottom electrode and three top electrodes. Thanks to the possibility to simulate each top electrodes with different voltages we can create a system that ensure information propagation thanks to the clock zone mechanism described in chapter 1. The device has 3 clock zones, one for each top electrode, that drive the region below them with a proper electric field. The information can be controlled trough voltages combination of the three electrodes, resetting and propagating when needed. In the first part a brief description on the procedure used to manage the field data from SDevice and integrate them into SCERPA is provided, with highlights on a MATLAB scripts that allow the connections between the two tools. With this program we can simulate different number of time steps with different driving combinations to better study propagation. An analysis on the geometrical parameters variations is then carried out, studying how variations of geometrical characteristics of the wire such as interphase distances and top electrodes length affected the device performances. From this considerations we can stipulate a Safe operating area excluding certain dimensions combinations from operational use.

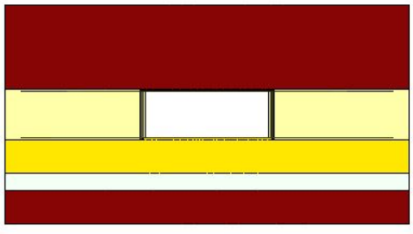
4.1 Structure simulation

The structure of the wire is essentially composed of a sequence of three closed cells, which share a common bottom gold electrode as a base and three gold VIAs serving as top electrodes. In this particular design, it becomes necessary to introduce a parameter that expresses the distance along the y-axis between two adjacent clocking regions. Since the molecules must be connected along the entire length of the lower

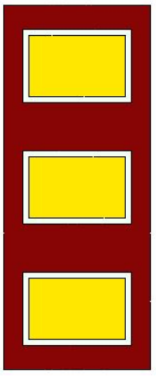
gold layer, it is crucial to verify that the molecules located in the areas between two clocking regions are properly influenced by the electric fields, in order to ensure correct propagation and reset within those zones. The parameter in question, introduced as D, represents the distance between two top electrodes in micrometers, and also it's half value D/2 defines the spacing between the edges and the clocking regions at the ends of the wire. This was done to allow continuity in the connection of multiple structures in sequence for the eventuality of simulation of more complex circuits. By setting the offset to D/2, once two triphase wires are connected, a distance D between their respective top electrodes is maintained. Another important parameter that will be changed is the electrode length, defined with the E variable, affecting the length of the clock zone. Enlarging this parameter will produce longer region where molecules are directly driven by the electric fields. For reference a wire of dimensions W=8 nm, D= 8 nm and Clock length of 10 nm is depicted in Figure 4.1.



(a) Triphase 8nm wire, general view



(b) Triphase 8nm wire, frontal view



(c) Triphase 8nm wire, top view

Figure 4.1: Triphase 8nm wire

The differences between the single phase device in terms of simulation are represented by the presence of three electrodes, which require each a proper definition and activation, but other than that the definition procedure are quite similar to previous chapter. The geometrical dimensions of the wire no longer depend on the width chosen, but also on the interphase and clock region length, which cause the variation of the entire device length. For what concern voltages three values where used for each electrode, allowing the application of individual state for each clock zone; the values used are the same as chapter 3, we can impose a RESET of the zone with 3 V, we can impose a HOLD/SET state applying -3 V and a third NULL state at 0 V. As done before for the single phase case, this third state is used to ensure the correct molecules simulations in SCERPA, giving time to the algorithm to reach result convergence with an intermediate state to avoid abrupt switching from 3V RESET state to -3V HOLD state, which causes errors in the propagation. Before showing the results it's necessary to describe certain algorithm solution adopted for this part, both for the electrical simulation in SDevice, the data analysis in SVisual and the simulation in SCERPA.

4.1.1 SDevice simulation

For all the aforementioned devices a small change was introduced in the SDevice command code, to allow the individual definition of voltages across the three electrodes, simply by defining them separately:

```
Solve
{
...
Quasistationary (InitialStep=1e-3 MinStep=1e-5 MaxStep=0.05
Goal Name="TopContact_p1" Voltage= @V1@ )
CoupledPoisson Electron Hole

Quasistationary (InitialStep=1e-3 MinStep=1e-5 MaxStep=0.05
Goal Name="TopContact_p2" Voltage= @V2@ )
CoupledPoisson Electron Hole

Quasistationary (InitialStep=1e-3 MinStep=1e-5 MaxStep=0.05
Goal Name="TopContact_p3" Voltage= @V3@ )
CoupledPoisson Electron Hole

}
```

By doing this we can assign and simulate different voltage values directly inside the same Sentaurus project, analyzing the 27 different devices combinations for driving voltages (3,-3,0).

4.1.2 SVisual analysis

For the SVisual scripts a few changes were applied to manage data for the new parameters introduced. An inside function is introduced to allow the code identification of the voltage combinations applied to the electrodes. This function take as input one voltage value and return a letter based on the value introduced, ensuring the following code codification:

- **3 V applied** : for this case the function assign the code H, stating that the particular electrode is at it's high value and it's resetting the zone.
- **-3 V applied** : for this case the function assign the code L, stating that the particular electrode is at it's low value and it's keeping in hold the zone.
- **0 V applied** : for this case the function assign the code N, stating that the particular electrode is at it's null value, useful as intermediate step to use between high and low state.

The SVisual script take the simulated structure, assign the coding to the driving voltages and place the extracted line field in the appropriate folder, saving in its name the line and the sequence of electrode states applied. For example a .csv file saved as "$CD\_16\_2\_NHH.csv$" is the array containing the electric field values of the second molecule line for a 16 nm wide wire, i.e. at xcut of x=11 nm, for the driving combination of voltages $V_{FirstPhase} = 0V$, $V_{SecondPhase} = 3V$ and $V_{ThirdPhase} = 3V$. This coding protocol of the driving voltages will be useful to define a sequence of state that are sequentially applied during the simulation in SCERPA, emulating a series of clock steps imposed onto the triphase wire each one defined by a specific combination of electrode voltages applied. With this method any number of consecutive time steps can be simulated for the particular structure, enabling detailed analysis of various phenomena like information propagation.

4.1.3 SCERPA simulation

Propagation simulation are carried out into SCERPA as usual, but this time a custom MATLAB script has been developed to allow an automated selection of the most important device characteristics, exploiting a database system. Basically the electric field for every single wire model is simulated and saved into specific named folders . The folder are organized as a ramified database where all the simulated fields for any combination of width (W),interphase distance (D) and clock region length (E) can be stored. Thanks to this feature all the needed information are orderly saved for SCERPA, allowing quick recalling of them. This Database is filled thanks to Sentaurus SVisual script and constantly updated the more the simulations in SDevice are completed.

Once all the useful geometrical variation of width,Clock length and interphase distance are electrically simulated and the proper field extracted and saved in the database, the MATLAB script question the user to provide the main characteristic of the wire that need to be simulated. The user can define the device type, width, E and D parameter, together with the time steps sequence and the input. Following the user request, the script indexes to the corresponding folder and automatically extract the field information. The extracted .csv data related to the field distribution are organized in an array of matrices, where each matrix is the spatial distribution of the Electric field along the y direction across the different molecule lines for a particular state of electrode voltages.

For each driving combination of the top electrodes a *stack_clock* matrix is con-

structed within the database data. This particular matrix have as rows the total number of molecules of the wire, and as columns the field acting on each single molecule for each time steps of the simulation. This procedure is needed for the simulation of a sequence of clock steps, where the user can define in the script a succession of states applied to the device together with a succession of input (both sequence have to be consistent one another). By doing this, a particular set of clock steps can be applied, one in which for each step a particular state can be imposed and simulated. In the geometrical analysis performed int this chapter, the main state sequence used is:

"NHH"->"LHH"->"LNH"->"LLH"->"NLN"->"HLL"->"HNL"->"HHL".

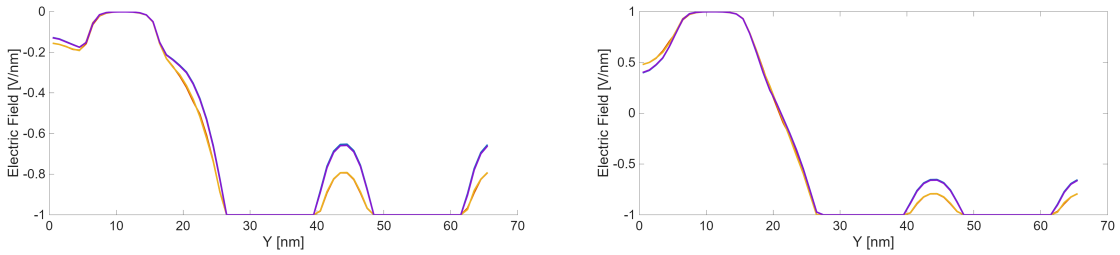
This sequence is imposed to properly simulate a realistic state transitions regarding input propagation; the information is propagated only when the specific zones are is kept in a HOLD state, for which electrostatic interaction between localized charge on molecule can happen. Once the logic values is passed across that zone, to impose directionality, it is reset. The intermediate N state is very useful to soften the transition between the 2 main H and L states, allowing the tool to correctly simulate parameters of the wire during each clock steps. The input on the circuit driver is kept steady at '1' or '0' during the entire cycle (similar to what was already done for the single phase wire). With the aforementioned sequence we first propagate the input trough the first phase, then to the second resetting the first and the third one and then to the output.
With all this procedure the user can quickly simulate device that differs from small geometrical variations, applying a specific phases pattern to study how the small variation in the geometry really affect mechanisms of the wire. The working principle of the script is based on the existence of an already simulated database of field values, where the devices electrical simulation results are kept, and upon the user request they are extracted and integrated into SCERPA.

4.2 Simulation: Interphase distance change

In this first part only effects of interphase distance (D) changes are studied, to understand how the distance between top electrodes affects propagation, especially on the interstitial molecules not covered by any top electrode. What is expected is to find harder resetting the interstitial molecule in the zone between electrodes the more the distance D increases. In this first analysis, a small range of distances will be simulated, from 4nm to 10nm, to ensure there are no error in the propagation of

both logic '1' and '0' along the wire. All the analysis will be carried out on 8nm, 16nm and 32nm wire. The interphase distance will be increase up to 10 nm maximum and then it will be proceed with the next analysis. This is done to ensure that the device are working up to an interphase distance similar to the standard length of the clock zone.

During this analysis only the most significant steps of the simulation will be shown, which are the LHH->LLH->HLL->HHL steps, leaving out the intermediate states. For reference the graph depicting the electric field distribution of the first two states of the chain is shown in Figure 4.2 for a W=8 nm, D=10 nm wire ; as it can be appreciated the wire region directly under the influence of the electrodes driving bias are reaching the values of -1 V/nm for H state (3 V applied), 1 V/nm for L state (-3 V applied) and 0 for N state (0 V applied). Also the fields distribution across different molecular lines (in different colors in the graph) is identical. In the transition region between electrodes the acting field is decreasing/increasing when passing from one state to another along the y direction. The higher the distance D the larger this transition zone will be, possibly affecting propagation, since molecules around this space will be affected by fluctuating field values.



(a) E_z for NHH state (b) E_z for LHH state

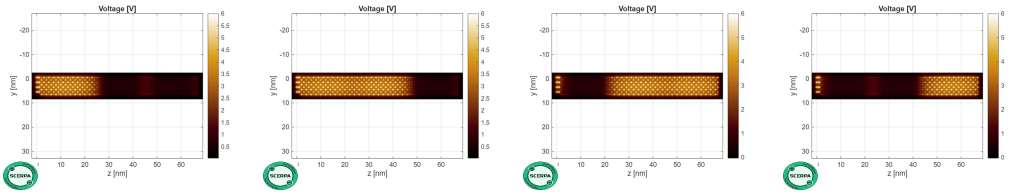
Figure 4.2: Ez field distribution across Y, triphase wire 8nm

The simulations results demonstrated that all the wires worked perfectly up to the top interphase distance of 10 nm, correctly propagating both '1' and '0'; in this section, as reference, only the top D=10 nm simulation results will be shown.

4.2.1 8 nm wire

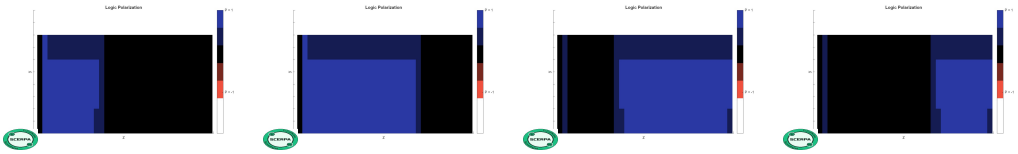
In this section a 8nm wire is analyzed. The device worked correctly for D up to 10 nm, correctly propagating both logic '1' and '0' to the output. Figure 4.3 shows the Potential plots related to propagation for this configuration, Figure4.4 shows the

Logic plots. The sequence of states applied to this wire successfully carries input information to the output, for all logic combinations.



(a) step LHH (b) step LLH (c) step HLL (d) step HHL

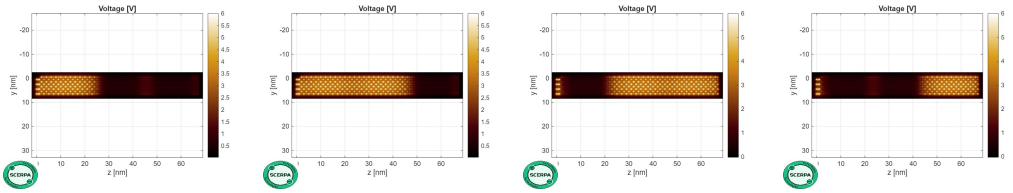
Figure 4.3: Triphase 8 nm wire, D=10 nm SCERPA Potential plots, input '1'



(a) step LHH (b) step LLH (c) step HLL (d) step HHL

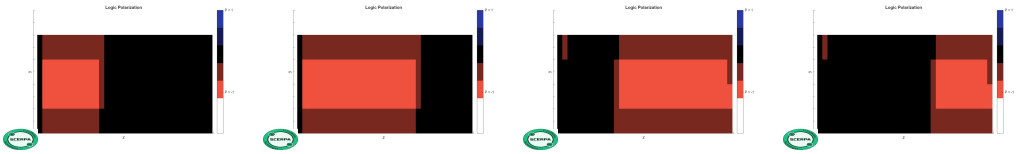
Figure 4.4: Triphase 8 nm wire, D=10 nm SCERPA Logic plots, input '1'

The same test is repeated for input 0 across all molecules lines, imposed for all the time steps simulated, results are shown in Figure 4.5 and 4.6.



(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.5: Triphase 8 nm wire, D=10 nm SCERPA Potential plots, input '0'



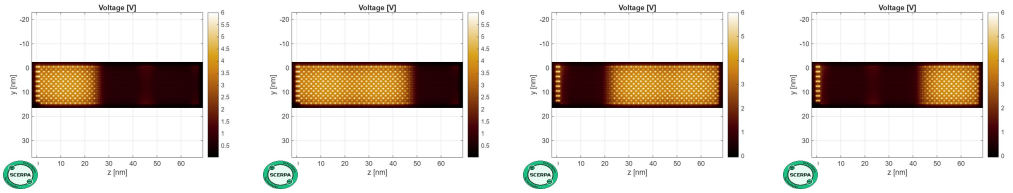
(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.6: Triphase 8 nm wire, D=10 nm SCERPA Logic plots, input '0'

This SCERPA simulations demonstrated that for a 8 nm wire the interphase distance can reach the same dimensions as the clock zone length, relaxing limitations concerning fabrications constrain for this geometrical parameters.

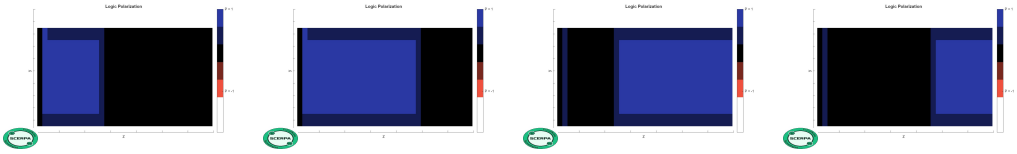
4.2.2 16 nm wire

In this section a 16nm wide device is simulated and tested, and the results for a logic '1' input are depicted in figure 4.7 and 4.8:



(a) step LHH (b) step LLH (c) step HLL (d) step HHL

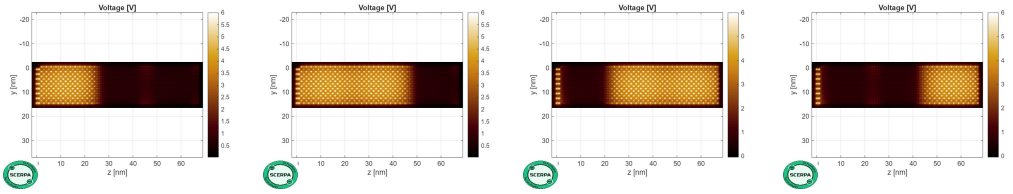
Figure 4.7: Triphase 16 nm wire, D=10 nm SCERPA Potential plots, input '1'



(a) step LHH (b) step LLH (c) step HLL (d) step HHL

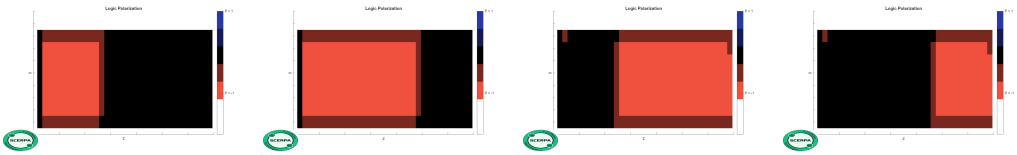
Figure 4.8: Triphase 16 nm wire, D=10 nm SCERPA Logic plots, input '1'

As done for the previous configuration, same simulations are repeated for input '0', in Figure 4.9 and 4.10:



(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.9: Triphase 16 nm wire, D=10 nm SCERPA Potential plots, input '0'



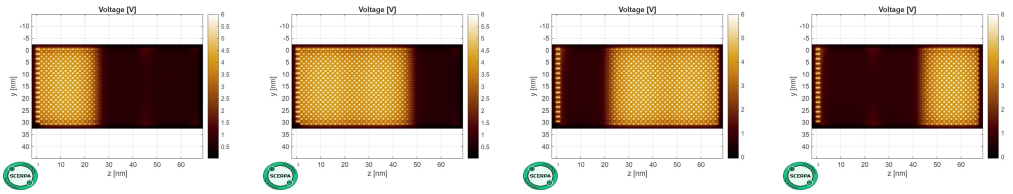
(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.10: Triphase 16 nm wire, D=10 nm SCERPA Logic plots, input '0'

The W=16 nm wire shows consistency in propagation for interphase distance values up to D=10 nm, consistent with the results obtained for the W=8 nm design.

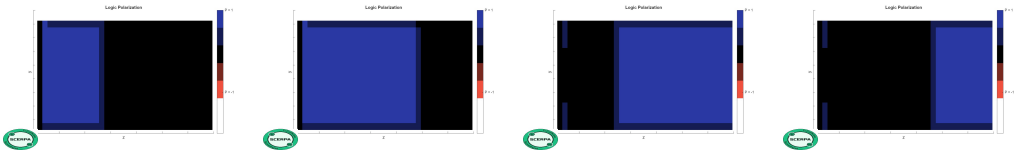
4.2.3 32nm wire

Lastly a W=32 nm wire is simulated, all the results are shown in figure 4.11 and 4.12 for '1' input:



(a) step LHH (b) step LLH (c) step HLL (d) step HHL

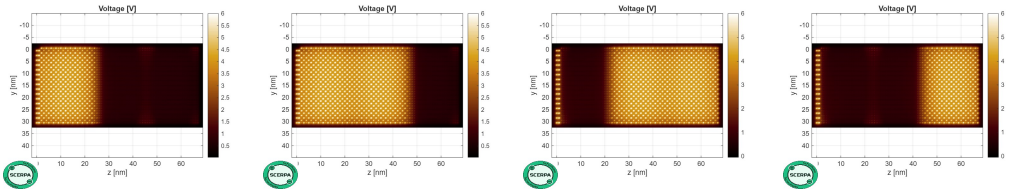
Figure 4.11: Triphase 32 nm wire, D=10 nm SCERPA Potential plots, input '1'



(a) step LHH (b) step LLH (c) step HLL (d) step HHL

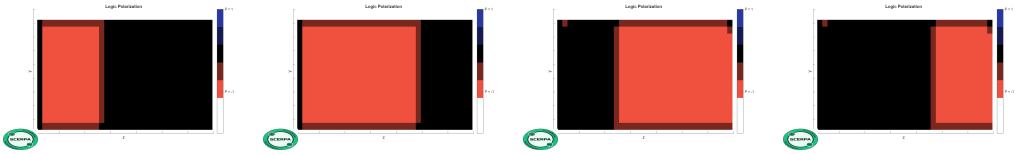
Figure 4.12: Triphase 32 nm wire, D=10 nm SCERPA Logic plots, input '1'

Results for input '0' are shown in Figure 4.13 and 4.14:



(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.13: Triphase 32 nm wire, D=10 nm SCERPA Potential plots, input '0'



(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.14: Triphase 32 nm wire, D=10 nm SCERPA Logic plots, input '0'

At this point all the devices present good propagation capabilities up to values of D=10 nm, correctly propagating the information across the entire wire length

without any error; the Closed design is able to provide good driving field in the interstitial region between electrodes. Once the interphase distance D start to reach values comparable to the Clock region length E, we can start to study small variations effect on this two parameter together.

4.3 Simulation: Interphase distance and electrodes length change

Once it has been demonstrated that, up to an interphase distance of D=10 nm, there are no evident effects on device performance, we can proceed with the gradual and combined variation of the electrode length in order to establish possible operational ranges. In this section, similar analyses are therefore carried out, simultaneously changing D interphase distance and E electrode length. By imposing the same phases sequence as before, the limiting geometric designs that will induce problems for information propagation are identified, thereby defining the so-called safe operating areas.
If increasing the interphase distances could result in a problematic resetting of the molecules not directly covered by the clocking regions beneath the electrodes, extending the electrodes length could lead to issues related to the incorrect switching of the molecule furthest from the input; the charge on these molecules, not affected by the reset signal anymore, will quickly assume a random stable configuration if the input doesn't reach them in time. Although the analyses were conducted over a variety of size values, only the key cases will be reported in this section, highlighting the most significant episodes and the most common errors encountered.

From all the collected data, a boundary curve graphically representing the safe operating areas concerning geometrical dimensions of the wire will be built, allowing the identification of major differences or common trend between different width. As done in previous part, a device is defined as WORKING if it's able to propagate the appropriate input across its entire length without changing/modifying the initial information. The axis of the Boundary curve will represent D/E parameters, green dots show the dimensions combination for a working triphase wire, which correctly propagates both '1' and '0'. The red cross will indicate the first pair of parameters for which the device failed in propagation. From this list of status points we can define a curve interpolating the working device points as upper limits of the safe operating area, i.e. the zone in which we can guarantee a working device. The analysis on these curves will provide insight about recurrent behavioral trends regarding

propagation between the different variants of Closed wire.
In order to show as reference the results obtained, only four wires for each width variants will be shown, two working and two not working. These four wires will provide insight on the extreme side of the boundary curve, being the last working and the first not working wires for the lowest D value (10 nm) and the last working wire and the first not working wire for the highest D supported by that wire. With this procedure the main common errors encountered can be shown for reference.

4.3.1 8 nm wire

From all the simulations performed on a 8 nm wide wire the trend is clear, increasing too much both interphase distance or Electrode length is detrimental for the performances, resulting in errors in propagation. From the computed data we can extract a boundary curve, graphically representing the encountered geometrical limitations affecting the wire behavior, in Figure 4.15.

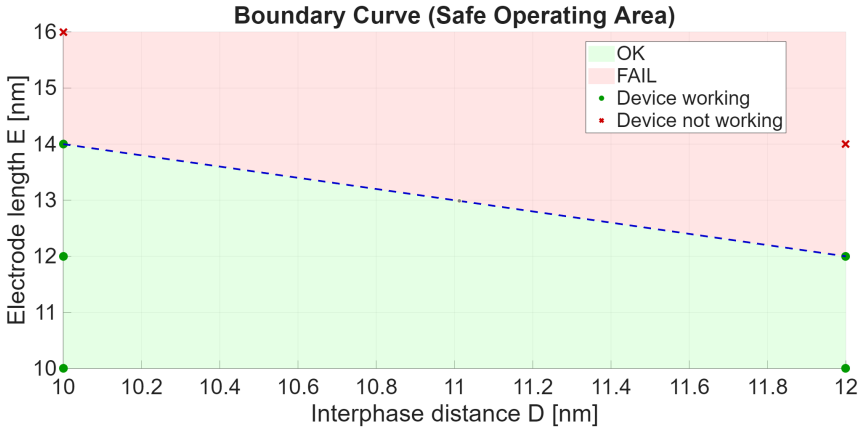
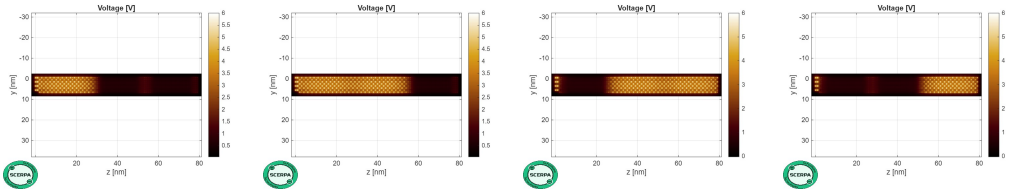


Figure 4.15: Boundary curve, 8 nm triphase Closed wire

From figure 4.15 we can appreciate the distribution of geometrical parameters that define working wires from not working wires; the trend is clearly showing correct working performances for similar E and D values, but contained around the 12/14 nm mark. Increasing both dimensions behind that point will results in a non functioning wire, producing errors in the first or last phase of propagation. After ranges around 12/14 nm, it's impossible to make the device works for the voltages and construction criteria used in this study. This results highlight the limitations in terms of sizes of a 8 nm wide wire.

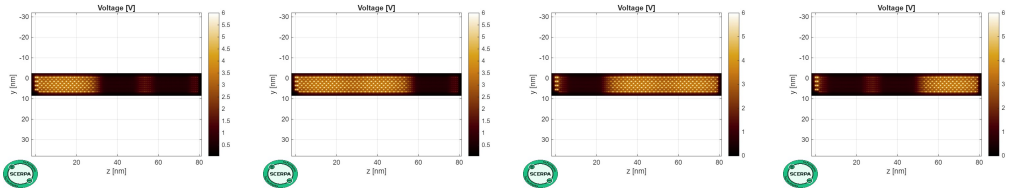
As reference the results for input '1' of working devices (10;14)/(12;10) are compared with their not working nearest configurations in the boundary curve graph

(10;16)/(14;10).



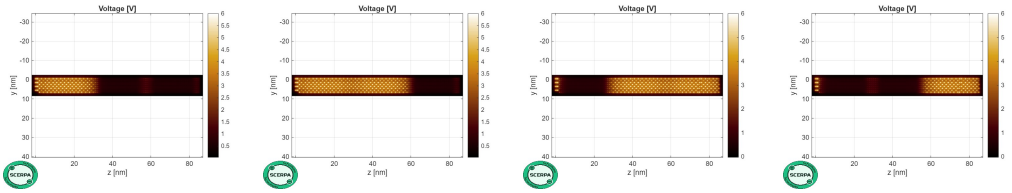
(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.16: Triphase 8 nm wire, D=10 nm/E=14 nm SCERPA Potential plots



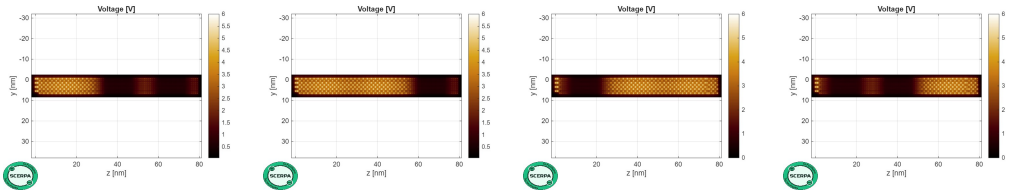
(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.17: Triphase 8 nm wire, D=12 nm/E=10 nm SCERPA Potential plots



(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.18: Triphase 8 nm wire, D=10 nm/E=16 nm SCERPA Potential plots



(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.19: Triphase 8 nm wire, D=14 nm/E=10 nm SCERPA Potential plots

The two top configurations show good behavior when propagating the input, Figures 4.16 and 4.17, instead the last two fail the propagation at the end of the wire, as in Figures 4.18 and 4.19. In this case the error is similar for both configuration, occurring in the last zone during the HLL step; for these wires the driving capabilities

induced by too large interphase distances and perturbations induced by a longer clock zone make device fail, inverting the input in the last section of the device. For clarity, the Logic plots for the critical phases of the two aforementioned not working cases are included, in order to highlight the type of errors that occurred. As it can be seen from Fig.4.20, both devices fail during HHL step:

(a) D=14 nm,E=10 nm wire error input '1' (b) D=10 nm,E=16 nm wire error input '1'

Figure 4.20: Logic Plots for W=8 nm wire, Propagation errors

4.3.2 16 nm wire

From all the simulations performed on a 16 nm wide wire the obtained boundary curve is depicted in Figure 4.21:

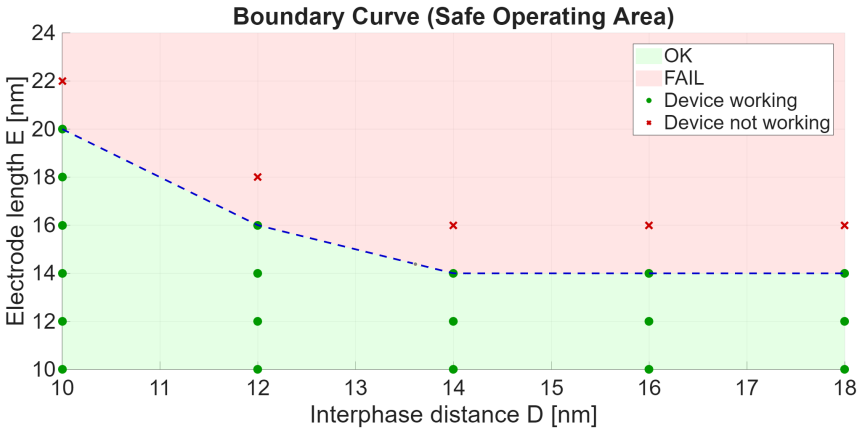
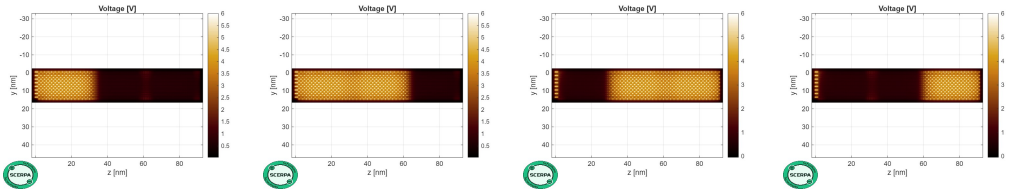


Figure 4.21: Boundary curve, 16 nm triphase Closed wire

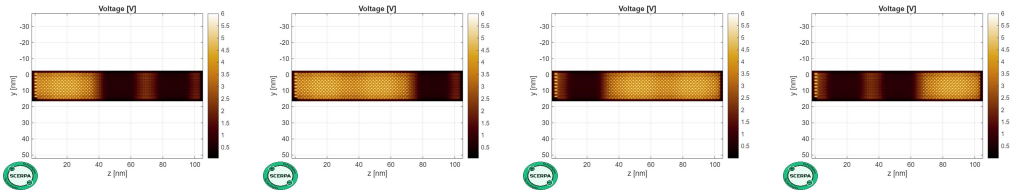
From figure 4.21 an interesting observation on boundary trend can be made, since for a larger wire much higher dimensions regarding D and E can be reached. This limit relaxation with respect to the previous design depends on the capability of molecule charge distribution to strengthen itself if a high number of molecules are put close to each other. Due to the huge amount of localized charge involved in the electrostatic interaction, the potential retention is higher, producing a more stable configuration. As a consequence of this, values up to 18 nm for D and 18 nm for E can be reached without compromising performances. This is an important results, since it indicates that wire carrying more information are also more stable, with less

strictly safe operating areas. As reference wire of dimension (10;20) and (18;14) are depicted in Figure 4.22 and 4.23 as the last extreme working cases for a W=16 nm wire, with (10;22) and (20;10) being the first not working devices, as in Figure 4.25 and 4.24.



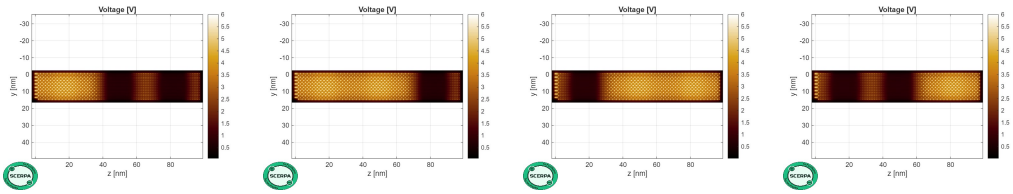
(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.22: Triphase 16 nm wire, D=10 nm/E=20 nm SCERPA Potential plots



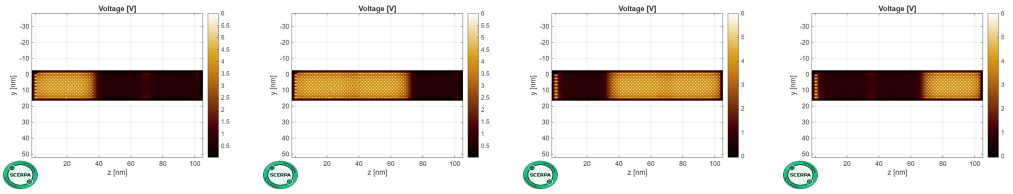
(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.23: Triphase 16 nm wire, D=18 nm/E=14 nm SCERPA Potential plots



(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.24: Triphase 16 nm wire, D=20 nm/E=10 nm SCERPA Potential plots



(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.25: Triphase 16 nm wire, D=10 nm/E=22 nm SCERPA Potential plots

As it can be seen from the collected data the device safe operating area is enlarged, allowing bigger dimensions for both interphase distance and electrodes

length; errors in propagation are present if both D and E are increased too much, as it was for the 8 nm design, but the reached values for this dimensions are higher. The stability induced by the high concentration of a huge number of localized charges near each other is augmented, making the performance better for bigger wires. The D=20nm E=10 nm fails the correct polarization of charges, Fig.4.24, creating a '0' charge configuration propagation inside the '1' region, due to the high inter-phase distance. For what concern the wire D=10 nm E=22 nm, in Fig.4.25, fails in propagating correctly the '0' across the initial region of the wire, during step LHH, resulting in an inversion at the output. The two errors are detailed in the Logic plots, in Fig.4.26:

(a) D=10nm,E=22nm wire Errors input '0' (b) D=20nm,E=10nm wire Errors input '1'

Figure 4.26: Logic Plots for W=16 nm wire, Propagation errors

On the left, in Figure 4.26a, the wire fails at D=10nm/E=22nm, not propagating correctly the input '0' across, inverting its logic value during middle steps LHH->LLH. This is caused by the incorrect switching of molecules further away from the input due to the higher clock zone length; these molecules are susceptible to perturbations and variation during input propagation, due to their metastable condition. Once the reset is released, they will tend to randomly polarized quickly if not properly driven by the input. On the right, in Figure 4.26b, the device fails at D=20nm/E=10 nm due to unwanted presence of a wrong logical value during first steps of propagation, not polarizing correctly the molecule charges; this could lead to error especially if multiple copies of this variant are present inside the circuit.

4.3.3 32 nm wire

The boundary curve obtained with all the simulation for a 32 nm wide wire is depicted in Figure 4.27:

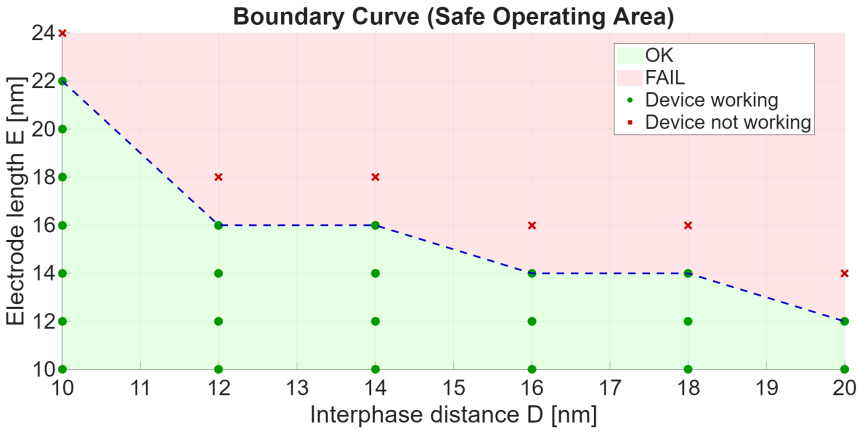
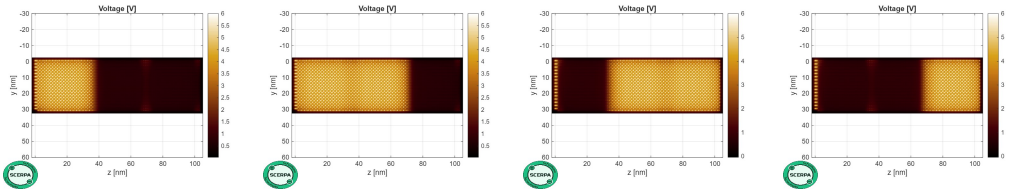


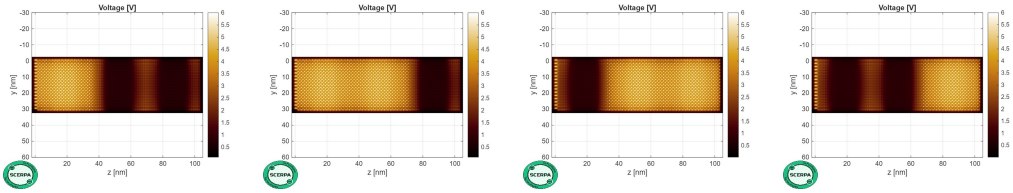
Figure 4.27: Boundary curve, 32 nm triphase Closed wire

From the Boundary curve the trend continues, demonstrating that larger wires are more stable in terms of information propagation. For what concern geometrical limits of this variant, the maximum achievable working interphase distance is found at D=20 nm, with wire [22:10] being the first not working device. As in the previous cases, the devices at the extremes of the curve are chosen as references, namely the last functioning and the first non-functioning ones for D = 10 nm, and the last functioning and the first non-functioning ones on the right-hand limit. These devices are (10;22) and (20;12) as OK devices, in Fig.4.28 and 4.29, (10;24) and (22;10) as FAIL devices, in Fig.4.30 and 4.31.



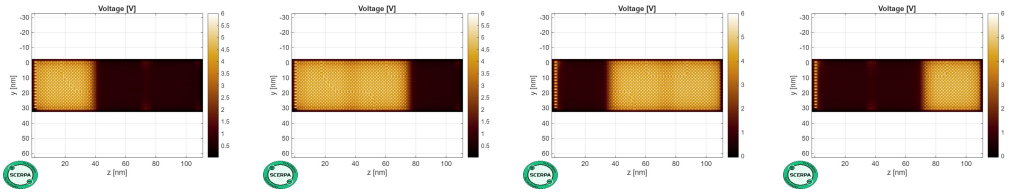
(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.28: Triphase 32 nm wire, D=10 nm/E=22 nm SCERPA Potential plots



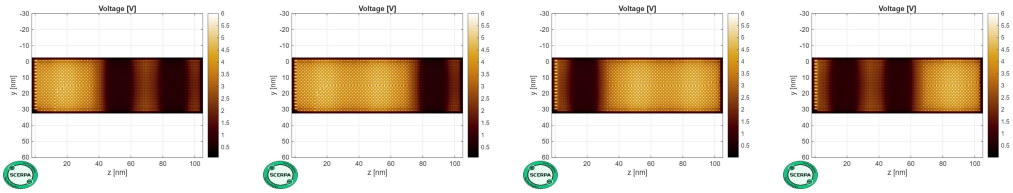
(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.29: Triphase 32 nm wire, D=20 nm/E=12 nm SCERPA Potential plots



(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.30: Triphase 32 nm wire, D=10 nm/E=24 nm SCERPA Potential plots



(a) step LHH (b) step LLH (c) step HLL (d) step HHL

Figure 4.31: Triphase 32 nm wire, D=22 nm/E=10 nm SCERPA Potential plots

For what concern errors for this variant, they are better shown in the Logic Plots in Figure 4.32:

(a) D=10 nm,E=24 nm wire error input '1' (b) D=22 nm,E=10 nm wire error input '1'

Figure 4.32: Logic Plots for W=32 nm wire, Propagation errors

On the left, in Figure 4.32a, the propagation of input '0' fails during first simulation steps, with the wire not being able to sustain the correct charge polarization across the entire length; this will result in an invertion of the input at the end of the wire. For the (10;16) device, in Figure 4.32b, a similar error occur.

4.3.4 Results

From the simulation results performed for triphase wire a clear trend emerges: wires that carries more information in terms of bit number are the ones that can guarantee more stable propagation conditions, allowing higher dimension to be reached without sacrificing performance. The Closed cell demonstrated to be a good candidate for triphase application, ensuring that the clock zone are properly influenced by the field distribution. The device proved to be suited for possible applications as an interconnection element, ensuring correct info propagation for dimension included in the safe operating area range. Still, both D and E parameters remain the limiting conditions for the proper behavior of the wire, and their choice will vary depending on the intended application.

Chapter 5

Parasitic Capacitances analysis

In this chapter a small electrical analysis on the parasitic capacitance of the system is carried out, focusing the attention on the tri-phase Closed wire, extracting its capacitance matrix. To extract the C matrix, a small signal AC analysis must be performed on the device. For a given frequency f the small signal current and voltages excitations are linked to the admittance matrix Y by Equation 5.1:

$$\delta I = Y \delta V \tag{5.1}$$

Y admittance matrix can be represented by Equation 5.2:

$$Y = A + i2\pi fC \tag{5.2}$$

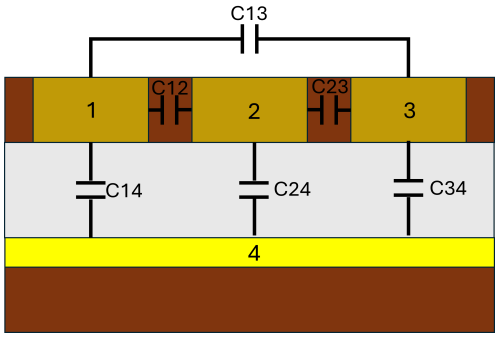
C is the capacitance matrix and A is the conductance matrix. The excitations are driven on the electrical nodes of a circuit system, so to perform this analysis it was necessary to express inside SDevice the wire structure in a circuital Spyce-like formulation, one that defines the electrodes as electrical nodes and perform a small signal analysis on the device. To do this the SYSTEM command has to be used inside the sdevice.cmd script:

```
System {
Cell "closed" ("TopContact_p1"=1
"TopContact_p2"=2
"TopContact_p3"=3
"BottomContact"=4
) }
```

In this way every electrode is expressed as a circuital node and the AC simulation can be carried out in the Solve section:

```
Solve
{ ...
ACCoupled(
StartFrequency=1e9 EndFrequency=1e9
NumberOfPoints=1 Decade
Node(1 2 3 4)
ACExtract = "C@node@"
)
{Poisson Contact Circuit}
}
```

From the results the capacitance matrix elements can be directly derived, allowing a quick study on how the geometrical parameters investigated in the previous chapter affect parasitic capacitance of the device. For the triphase wire the system in Figure 5.1 can be considered as a reference:



(a) System node reference

$$\begin{pmatrix} C11 & C12 & C13 & C14 \\ C21 & C22 & C23 & C24 \\ C31 & C32 & C33 & C34 \\ C41 & C42 & C43 & C44 \end{pmatrix}$$

(b) Capacitance matrix C

Figure 5.1: Parasitic Capacitance analysis system

As it can be seen from figure 5.1, the four electrodes of the wire are labeled numerically from 1 to 4, with 1 being the first top electrode and 4 being the bottom grounded Gold layer. On the right the classic Capacitance matrix structure is presented: it is a 4x4 matrix (number of nodes x number of nodes) where each C_{ij} element represent the parasitic capacitance calculated between the node i and j. The matrix is symmetric, since $C_{ij} = C_{ji}$, and the diagonal elements C_{ii} represents the self-capacity of a particular node with respect to the mass of the circuit. The

capacitance values follow the classic definition capacitor equation 5.3:

$$C = \epsilon_0 \epsilon_r \frac{A}{d} \tag{5.3}$$

Where ϵ_r is the dielectric constant of the material between the plates, A is the area of the plates and d is the distance between them. What is expected changing the geometrical dimensions of the wire is to have a certain dual effect from the change of the interphase distance (D) and the electrode length (E). The first one will affect mainly $C_{23} = C_{32}$, $C_{13} = C_{31}$ and $C_{12} = C_{21}$, because changing the distance will affect the distance of the plate capacitor in the equation 5.3, lowering its value. On the other hand increasing the length of the clock region will increase the capacity of the upper nodes with respect to the bottom one, increasing $C_{14} = C_{41}$,$C_{24} = C_{42}$ and $C_{34} = C_{43}$, due to the bottom face of electrode being larger. The AC analysis are conducted on the different width variants of the wire, to understand also the role played by their width in the study. For what concern the parasitic capacitance only C_{12}, C_{23},C_{24},C_{14} and C_{34} will be analyzed in this chapter, being the most critical ones of the structure; for what concern materials the main dielectric is SiO_2 for capacities between top electrodes, while instead the main contribution for the top-bottom capacity comes from the lateral walls of Al_2O_3, which posses a dielectric constant far superior that the one of air.

5.0.1 Parasitic Capacitance 8 nm wire

In this section the geometrical parameters of a 8 nm Closed wire are changed to study parasitic capacitance behavior. Starting with consideration on the parasitic capacitance between the first and the second top electrodes, the main geometrical parameter affecting it's value is the interphase distance D. From the result Table 5.1 the dependence of C_{12} by D is clear; the higher the distance between the plates, the lower the capacitance will be. The dimensions choices are taken to match as close as possible the safe operating area range.

$D[nm]\backslash E[nm]$	10	12	14
10	0.245	0.246	0.245
12	0.156	0.156	0.156

Table 5.1: C_{12} [aF] for different D and E

The capacitance C_{23} follows a similar trend, as it can be seen from Table 5.2; again here the higher distance between plates will directly relate to a lower capaci-

tance value.

$D[nm]\backslash E[nm]$	10	12	14
10	0.245	0.245	0.246
12	0.157	0.159	0.158

Table 5.2: C_{23} [aF] for different D and E

An alternate trend can be appreciated when considering C_{24}, since E will be the most important parameter affecting this parasitic Capacitance. A longer electrode produce a larger top electrode area, increasing the C_{24}. From 5.4 this increase can be appreciated for higher Clock length. D produces a small effect on the top-bottom parasitic capacitance.

$D[nm]\backslash E[nm]$	10	12	14
10	7.78	8.72	9.6
12	7.88	8.84	9.75

Table 5.3: C_{24} [aF] for different D and E

Also the capacitance $C_{14} = C_{34}$ is reported :

$D[nm]\backslash E[nm]$	10	12	14
10	7.76	8.68	9.61
12	7.96	8.86	9.79

Table 5.4: $C_{14} = C_{34}$ [aF] for different D and E

5.0.2 Parasitic Capacitance 16 nm wire

In this section the geometrical parameters of a 16 nm Closed wire are changed to study parasitic capacitance behavior. Again the analyzed dimensions are consistent with the boundary curve expressed in chapter 4 for a 16 nm wire; the trend is similar to the 8 nm device, where C_{12} and C_{23} are the same and very affected by parameter D (see results in Table 5.5 and 5.6). With respect to the results of the 8 nm wire a higher Capacitance between electrodes is found, highlighting the larger electrode x-dimension needed to properly cover a larger trench hole.

$D[nm]\backslash E[nm]$	10	12	14	16	18	20
10	0.361	0.361	0.361	0.361	0.361	0.362
12	0.245	0.245	0.245	0.245	0.245	0.245
14	0.169	0.169	0.169	0.169	0.169	0.169
16	0.117	0.117	0.117	0.117	0.117	0.116
18	0.085	0.085	0.085	0.085	0.085	0.085
20	0.057	0.057	0.057	0.057	0.057	0.057

Table 5.5: C_{12} [aF] for different D and E

The trend is identical to the 8 nm wire, with D being the top parameter affecting C_{12} and C_{23} and E affecting mainly C_{24}.

$D[nm]\backslash E[nm]$	10	12	14	16	18	20
10	0.361	0.361	0.361	0.361	0.362	0.362
12	0.245	0.245	0.245	0.245	0.245	0.245
14	0.169	0.169	0.169	0.169	0.169	0.169
16	0.117	0.117	0.117	0.117	0.117	0.118
18	0.085	0.085	0.085	0.085	0.085	0.085
20	0.057	0.057	0.057	0.057	0.057	0.057

Table 5.6: C_{23} [aF] for different D and E

Same trend also for the top-bottom capacity, with slightly higher values of parasitic capacitance with respect to 5.4 due to the larger area of the electrode plate. As expected, E is the main parameter affecting C_{24}, pushing the capacitance values up to 11.1 aF for E=16 nm, as in Table 5.7:

$D[nm]\backslash E[nm]$	10	12	14	16	18	20
10	8.23	9.18	10.1	11.1	12.27	13.07
12	8.41	9.36	10.35	11.12	12.27	13.2
14	8.55	9.51	10.49	11.48	12.47	13.36
16	8.66	9.66	10.56	11.52	12.53	13.47
18	8.73	9.68	10.7	11.63	12.53	13.57
20	8.84	9.79	10.69	11.7	12.64	13.54

Table 5.7: C_{24} [aF] for different D and E

We can express also the $C_{14} = C_{34}$ matrix elements:

$D[nm]\backslash E[nm]$	10	12	14	16	18	20
10	8.23	9.18	10.14	11.1	12	13
12	8.41	9.37	10.34	11.32	12.24	13.22
14	8.54	9.55	10.49	11.42	12.42	13.32
16	8.66	9.55	10.43	11.4	12.5	13.42
18	8.75	9.71	10.63	11.61	12.59	13.52
20	8.78	9.77	10.71	11.67	12.63	13.60

Table 5.8: $C_{14} = C_{34}$ [aF] for different D and E

5.0.3 Parasitic Capacitance 32 nm wire

In this section the geometrical parameters of a 32 nm Closed wire are changed to study parasitic capacitance behavior. By looking at the previous results the trend is consistent with what was expected, with D playing the major role in changing C_{12} and C_{23} values and E for C_{24}. Again the overall larger side and bottom faces of the top electrodes induced by a width of 32 nm affect all the results, increasing the parasitic capacitance between every node of the structure. The results for all the important parasitic capacitance are collected in Tables 5.9,5.12,5.10 and 5.11:

$D[nm]\backslash E[nm]$	12	14	16	18	20	22	24
12	0.42	0.42	0.42	0.42	0.42	0.42	0.42
14	0.304	0.304	0.304	0.304	0.304	0.304	0.304
16	0.221	0.221	0.221	0.221	0.221	0.221	0.221
18	0.162	0.162	0.162	0.162	0.162	0.162	0.162
20	0.121	0.121	0.121	0.121	0.121	0.121	0.121

Table 5.9: C_{13} [aF] for different D and E

$D[nm]\backslash E[nm]$	12	14	16	18	20	22	24
12	0.42	0.42	0.42	0.42	0.42	0.42	0.42
14	0.304	0.304	0.304	0.304	0.304	0.304	0.304
16	0.221	0.221	0.221	0.221	0.221	0.221	0.221
18	0.162	0.162	0.162	0.162	0.162	0.162	0.162
20	0.121	0.121	0.121	0.121	0.121	0.121	0.121

Table 5.10: C_{23} [aF] for different D and E

$D[nm]\backslash E[nm]$	12	14	16	18	20	22	24
12	10.5	11.74	12.67	13.78	14.77	15.82	16.96
14	10.72	11.8	13	13.95	14.98	16.12	17.2
16	10.8	11.9	13	14.16	15.35	16.42	17.4
18	11	12.1	13.1	14.2	15.37	16.57	17.11
20	11.2	12.5	13.27	14.32	15.4	16.13	17.24

Table 5.11: C_{24} [aF] for different D and E

$D[nm]\backslash E[nm]$	12	14	16	18	20	22	24
12	10.5	11.58	12.65	13.78	14.83	15.84	17.1
14	10.82	11.8	12.84	13.89	14.97	16.1	17.3
16	10.9	12.07	13.1	14.2	15.34	16.38	17.1
18	11	12.07	13.1	14.2	15.34	16.38	17.1
20	11.1	12.23	13.27	14.45	15.38	16.15	17.5

Table 5.12: $C_{14} = C_{34}$ [aF] for different D and E

5.1 Power dissipation analysis

Power dissipation in MolFCN is not originated by conductive phenomena, due to the particular way in which information is propagated, but rather by dynamic power contribution, when changing from one state to another. Power consumption is related to the creation of the electric field needed in the clocking mechanism, where electrodes are continuously piloted to different voltage values during the cycling of the circuit. The parasitic capacitance build up charges to their respective plates when subjected to a potential difference, with a capacitative value expressed by $C = \epsilon_0 \epsilon_r \frac{A}{D}$. From the building of charges onto the plates energy is dissipated; the power lost in this way can be found by considering the infinitesimal work needed to move a charge q to the plate surface. This work can be expressed with Equation 5.4 :

$$\Delta W = \Delta V dq \tag{5.4}$$

where ΔV is the potential difference involved in the charge build up; by completing 5.4 using the capacitance-voltage relation $q = CV$ we obtain:

$$\Delta W = \frac{q}{C} dq \tag{5.5}$$

To obtain the total work W is sufficient to integrate equation 5.5 between 0 and the maximum build up charge, defined as Q_{max}. This will give us the Equation 5.6:

$$W = \int_0^{Q_{max}} \frac{q}{C}\, dq = \frac{Q_{max}^2}{2C} = \frac{(CV)^2}{2C} = \frac{1}{2}CV^2 \tag{5.6}$$

The energy provided by the voltage source can be expressed trough Equation 5.7:

$$E = \int_0^T IV\, dt = CV \int_0^V dV = CV^2 \tag{5.7}$$

where T is the total time involved into the charging and V it's the maximum voltage reached. This means that half of the energy is dissipated to heat and the other half is involved in building up capacitance charges. Since power is energy delivered over a certain amount of time we can express the power dissipated by the parasitic capacitance with Equation 5.8:

$$P = \frac{E}{T} = CV^2 f \tag{5.8}$$

Dissipated power it therefore dependent on working clock frequency, capacitance value and voltage difference applied. This relation immediately connects with the parasitic capacitance trough C contribution in Equation 5.7; the higher this capacitance value is the more power will be dissipated. Since the major parasitic capacitance were analyzed in the previous section, it's clear how choosing the proper geometrical parameters for the triphase wire is very important in determine the dissipated power.

For what concern power analysis we can estimate the power consumption of a triphase wire by considering the worst state scenario during simulation, that is the worst combination of driving voltages across the top electrodes. This happens for the state LHL, when $V_1 = -3V$, $V_2 = 3V$ and $V_3 = -3V$, so the contribution of all the parasitic capacitance in term of dissipated power is maximized.

In this conditions the total power dissipated can be expressed by Equation 5.9

$$Ptot = 2P_{14} + P_{24} + 2P_{12} = 2C_{14}V_{14}^2 f_{clk} + C_{24}V_{24}^2 f_{clk} + 2C_{12}V_{12}^2 f_{clk} \tag{5.9}$$

In this equation the double contribution between node 1 and 2 is induced by the relation $C_{12} = C_{23}$, same thing can be said for the capacitance $C_{14} = C_{34}$. From this formula we can study the power dissipated by a particular wire integrating all the tabled C values obtained with the Ac analysis with the worst case scenario for driving voltages. Looking at our analysis on how dimensions affect parasitic capacitance in

the cell, the wire with the longest E and lowest D posses higher capacitance overall, but for the confrontation of dissipated power the biggest device will be considered, as they are the easiest to fabricate. This for varying widths wires are:

- **8 nm Width**: for this width the largest device possible is for D=12 nm, E=12nm.
- **16 nm Width**: for this width the largest device possible is the D=18 nm, E=14 nm.
- **32 nm Width**: for this width the largest device possible is the D=20 nm, E=12nm.

By taking the C matrix values of the aforementioned device and integrate them into Equation 5.9, the behavior with respect to the frequency can be plotted, as in Figure 5.2:

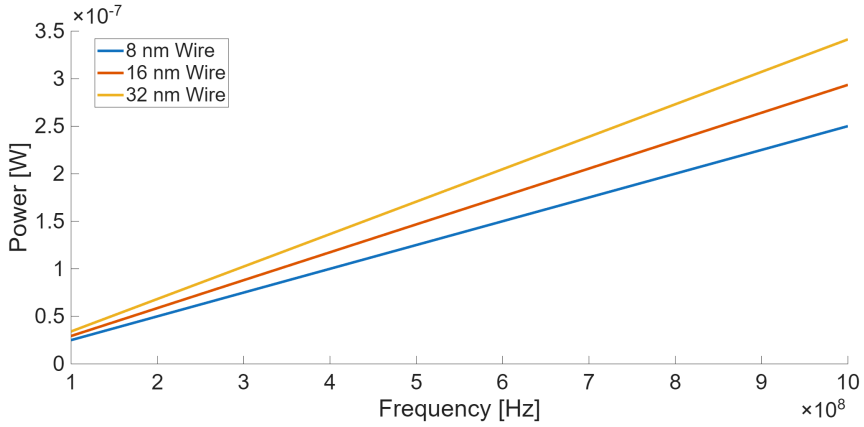


Figure 5.2: Power dissipated for different variants of wire

5.1.1 Results

In conclusion, from a geometrical point of view the possibility of reaching higher dimensions for interphase distance and electrode length have different effect not only on performances but also on the main parasitic capacitance. The trade off on tinkering with this geometrical parameters is evident. Larger dimensions regarding interphase distances D will mean easier fabrication techniques, lower capacitance between top electrodes but worse performance in driving the interstitial molecules in the interphase region. Electrode length E will follow a dual trend, with larger values being preferable in terms of fabrication, but worse control over longer lines of molecules also producing higher parasitic capacitance, especially between top-bottom parts. Regarding W it's increase surely relate to larger and more stable

information carried but also to much higher parasitic capacitance between all electrodes. It's clear from all this results that attention need to be used when deciding the proper dimensions of the wire, choosing for the right application the right set of parameters balancing pros and cons.

Chapter 6

Conclusion

To address the decline that Moore's law has experienced over the past decade, new technological solutions have been investigated. Among these, and within the broader family of Quantum Cellular Automata, Molecular Field-Coupled Nanocomputing stands out as one of the most promising and compelling implementations in recent years. This technology offers several advantages that could play a decisive role in surpassing the CMOS paradigm. Despite several benefits,including extreme miniaturization of these devices, their low power consumption, and the high speed at which information is propagated, technological developments are still required to achieve practical realization.

In this work, a possible implementation of a standard Closed cell has been presented and simulated using the TCAD Sentaurus software, with subsequent post-processing performed in MATLAB and SCERPA. Results concerning the electric field distribution within the internal regions of the cell have been reported and used for comparison with the previous Trench cell model. Through the combined use of these tools, a study on the propagation effectiveness of the two designs was carried out, to understand how the cell width affects the performance of both models. The obtained results showed the inadequacy of the Trench model in ensuring proper wire operation for widths greater than 16 nm. Since cell width is directly correlated with the number of transmitted bits, the Closed design outperformed the Trench configuration for wires ranging from 8 to 16 bits. Nevertheless, the Trench model remained suitable for narrower wires, around 4 nm wide, leaving room for possible implementations regarding thin cells.

Following this comparison, an analysis on a triphase Closed wire is carried out to understand how geometrical dimensions of the structure affect propagation for a wire composed by three top electrodes. Several device were simulated in order to formulate possible safe operating area, focusing on the maximum achievable inter-

phase distances and clock-zone lengths. The results indicated that wider wires are able to operate properly for higher dimensions due to the self stabilization effect exhibited by the device's molecules: the presence of large amounts of localized charge, oriented to minimize Coulomb repulsion, lead to highly stable polarization of the information that is less susceptible to perturbations; this effect resulted in larger safe operating area for the 16 nm and 32 nm wire.

Lastly, simple considerations on power dissipation for a triphase wire were carried out through the formulation of a parasitic capacitance model. Exploiting an AC analysis, the capacitance matrix is extracted for all the device variants, and its values integrated to calculate the power dissipated as function of clock frequency. From the results a trade off regarding dimensions choices emerges, highlighting how larger wires, that are easier to fabricate and provide more information stability, are also the ones who dissipate more energy over time.

Possible future development on the model can be directed towards finding new molecule structure that can support even smaller driving fields, or higher bias values to increase field control in the interstitial region.

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