Politecnico di Torino

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Nanotechnologies for ICTs

Die Attach Process Optimisation for System-in-Package modules

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Abstract

The evolution of electronic packaging has progressed through distinct technological phases, each addressing the increasing demands for miniaturization and performance. Starting from traditional Printed Circuit Board (PCB) technology, to Multi-Chip-module (MCM) to more modern technologies such as System-on-a-Chip (SoC), System in Package (SiP) and Heterogeneous Integration (HI) however what has not changed is the need to create stable connections between devices and substrates and the different die attach processes are what enables these advanced packaging approaches.

The selection of appropriate die attach materials and methods directly impacts device performance, reliability, and manufacturability of an entire system or device. Therefore for consumer applications the die attach is essential for everything ranging from smartphones, smart-appliances, wearables to Internet of Things (IoT) sensors where thermal mangment and miniaturization are critical. Similarly for High Performance Computing and Data Centers, Medical and Health sector, Aerospace, Defense and Automotive sector are required die attach materials capable of surviving harsh environmental conditions and extended operational lifetimes while, particularly in power electronics and high-frequency devices, are necessary solutions that can withstand extreme operating conditions while maintaining electrical and thermal performances since the attach material is the first point of contact with the device and its predominant path for heat dissipation in the majority of packaging geometries for semiconductors applications. Choosing the most suitable die-attach method is essential and the possibilities are many depending on what parameters and properties are deemed more important for the desired application.

In this thesis will be first presented some the most commonly used techniques for establishing stable physical, thermal, and electrical connections, among them i will discuss Adhesive die attach, Eutectic die attach, Sintering and Cu-Cu hybrid bonding while for the Soldering process there will be a deeper dive into its elements, regulations, materials and with the trial of optimization of a reflow profile for two different solder pastes (SAC305 and Sn57Bi42Ag1) initially by attaching a die onto a DBC-like substrate (created by depositing a Copper layer over a Titanium layer for adhesion on an alumina substrate) then onto real DBCs and characterizing the resulting solders by means of a visual analysis and a Shear test. The Soldering was done in an Infrared reflow oven and, in order to match the temperatures inside the oven with the ones recommended in the data sheets of the two pastes, I employed both an external pt1000 thermoresistor connected to a multimeter and a thermocouple read by the oven itself. After these initial reflow profiles were found, I optimized them in order to reduce visible defects such as flux residue, solder balling and dull appearance of the solder. For a visual analysis of the results I used SEM imaging and optical imaging (DSX1000). For testing the adhesion strength of the soldering layer, a specific set up has been developed to perform a shear test, using additive manufacturing technology and a load cell.

Results: for the Sn57Bi42Ag1 solder paste I was able to obtain visually clean and shiny solders while for the SAC305 I was not able to obtain satisfying results for similar paste volumes. During the shear test on the DBC-like the copper layer was peeling off from the alumina before the solder broke while for the dbc the result were comparable values found in literature.

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Acronyms

ADAS Advanced Driver Assistance Systems. 13

BEOL back-end-of-line. 22

BGA Ball Grid Array. 43

CMP chemical mechanical polishing. 24, 25

CTE Coefficient of Thermal Expansion. 17, 20, 29, 30, 46

DBC Direct Bonded Copper. 2, 7, 8, 11, 48, 50–53, 55, 56, 59, 64, 69, 70

DIW Direct Ink Writing. 7, 41

ECE Electrically conductive Epoxies. 13

EDX Energy Dispersive X-ray Spectroscopy. 49

EEE Electrical and Electronic Equipment. 35

EU European Union. 35

HI Heterogeneous Integration. 2, 11, 21, 24

IMC Inter-Metallic Compound. 36, 39

IoT Internet of Things. 2, 11

IPC Institute of Printed Circuits (now Global Electronics Association). 6, 27, 28, 43

IR Infrared. 44

LED Light-Emitting Diode. 38

LFS Lead-Free Solder. 36, 38, 39, 49, 52, 53

MCM Multi-Chip-module. 2, 11

OEM Original Equipment Manufacturer. 20

OI Optical Inspection. 42, 43

PCB Printed Circuit Board. 2, 8, 11, 26, 30, 31, 33, 40–46, 58

ppm Parts Per Million. 35

PVD Physical Vapor Deposition. 51, 69

RDRP Ramp-Dwell-Ramp-to-Peak. 32, 46

RE Rare Earth. 28

RMS root mean square. 24

RoHS Restriction on Hazardous Substances. 35, 36

SAC tin-silver-copper Alloy. 38, 39

SAC305 tin-silver-copper Alloy. 2

SEM Scanning Electron Microscope. 8, 66, 67

SiP System in Package. 2, 11, 21, 48

SMT Surface Mount Technology. 26–28, 40, 44

SoC System-on-a-Chip. 2, 11

TAL Time Above Liquidus. 45

TDS Technical Data Sheet. 6, 8, 48, 53, 58, 60–62, 74

THT Through Hole Technology. 26

VPS Vapor Phase Soldering. 44

WEEE Waste from Electrical and Electronic Equipment. 35

Introduction

The evolution of electronic packaging has progressed through distinct technological phases, each addressing the increasing demands for miniaturization and performance. Starting from traditional Printed Circuit Board (PCB) technology, to Multi-Chip-module (MCM) to more modern technologies such as System-on-a-Chip (SoC), SiP and Heterogeneous Integration (HI) where bare dies, ICs, chiplets, sensors and other elements are all mounted together, what has not changed is the need to create stable connections between devices and substrates and the different die attach processes are what enables these advanced packaging approaches. The selection of appropriate die attach materials and methods directly impacts device performance, reliability, and manufacturability. [1].

Therefore for consumer applications the die attach is essential for everything ranging from smartphones, smart-appliances, wearables to Internet of Things (IoT) sensors where thermal mangment and miniaturization are critical, similarly for High Performance Computing and Data Centers, Medical and Health sector, Aerospace, Defense and Automotive sector are required die attach materials capable of surviving harsh environmental conditions and extended operational lifetimes[2][3] while, particularly in power electronics and high-frequency devices, are required die attach solutions that can withstand extreme operating conditions while maintaining electrical and thermal performance since the attach material is the first point of contact with the device and its predominant path for heat dissipation in the majority of packaging geometries for semiconductors applications[4][5].

For all this reasons choosing the most suitable die-attach method is essential and the possibilities are many depending on what parameters and properties are deemed more important for the desired application.

In this thesis will be first presented some the most commonly used techniques for establishing stable physical, thermal, and electrical connections that as shown by the analysis in figure3.1 share the entirety of the market. Among them will be discussed **Adhesive die attach**, **Eutectic die attach**, **Sintering** and **Cu-Cu hybrid bonding** and **Soldering** whose properties are briefly compared in the table below3.1. Then for the soldering process there will be a deeper dive into its elements with the trial of optimization of a reflow profile for two different solder pastes (SAC305 and Sn57Bi42Ag1) initially by attaching a die onto a DBC-like substrate then onto real DBCs and characterizing the results by means of a Shear Test.

Parameter	Solder	Ag Sinter	Cu Sinter	Cu-Cu Hybrid	Epoxy	Thermocomp.
Min. pitch (μm)	40-100	50-150	50-150	1-10	50-100	10-30
Thermal cond. (W/m·K)	50-60	130-250	200-300	400	1-5	200-400
Process temp. (°C)	180-260	200-250	250-300	200-400	90-200	250-400
Pressure required	No	Yes/No	Yes	No	No	Yes
Cost (relative)	1×	3-5×	2-4×	5-10×	0.5×	2-3×
Reliability	Good	Excellent	Excellent	Superior	Good	Excellent

Table 3.1: Comparison of die attach technologies. Good, Decent, Poor.

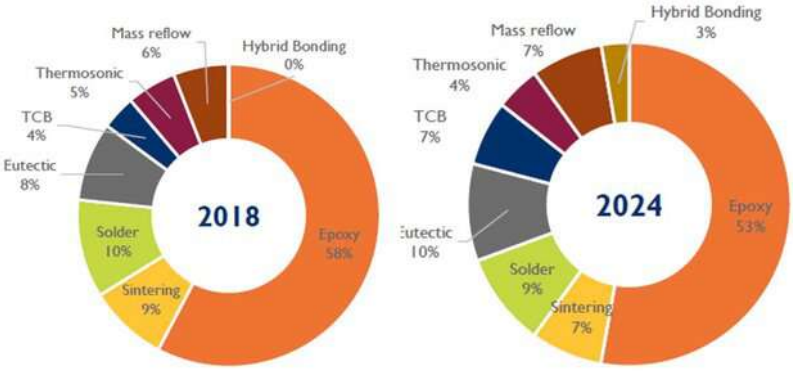


Figure 3.1: Market analysis and market prediction for die attach techniques by YOLE Development[6]

Adhesive Die Attach

Adhesive die attach techniques are used in applications where high thermal conductivity and high-speed operation are not critical and thus the main concerns are the mechanical bond and the cost. Adhesive Bonding relies on adhesive materials to secure the die to the substrate. It can be conducted at room temperature and depending on the adhesive can be electrically conductive or insulating. Adhesive bonding offers advantages like low curing temperatures, reduced die stresses and the ability to bond a wide range of die sizes. However, adhesive bonding has drawbacks like outgassing, contamination/bleed, inferior thermal/electrical conductivity, dimensional changes during processing and sensitivity to harsh environments. Die attach adhesives are available in two main forms:

- **Pastes:** Flow readily and conform well to substrate surfaces with the ability to provide large contact areas. They are cost-effective for low volumes but can suffer from sagging, resin bleed-out, and bond-line thickness control issues.
- **Films:** Come as pre-cut pieces (different shapes can be requested to specialized manufacturers) with controlled thickness (10-40 μm). Films need to be positioned with a pick and place machine and allow for better alignment control and cleaner process albeit not fit for mass productions.

The prevalent type of adhesive Die attach method used are the **Epoxy Thermoset Resins**.

4.1 Epoxy Die Attach

Epoxy die attach has dominated semiconductor packaging markets over recent years due to its versatility and cost-effectiveness compared to alternative bonding methods. The process involves dispensing a controlled amount of epoxy adhesive onto the package substrate using specialized dispensing tools, followed by precise die placement. The assembly is then heated to a specific temperature profile to adequately cure the epoxy according to the adhesive manufacturer's specifications[7].

4.1.1 Electrically conductive Epoxies

Epoxies offer excellent formulation flexibility, allowing incorporation of conductive fillers (silver, copper) for electrical applications or insulating fillers (silica, alumina) for isolation requirements. They provide cost-effectiveness and capability to accommodate larger dies and substrates compared to eutectic alternatives.
In order to accommodate the thermal end electrical management requirements of high power applications, the epoxies formulations have been enhanced by integrating conductive fillers such as silver, aluminium and nickel. If non conductive epoxies reach low thermal conduction values around 0.14-0.5 W/m·K their conductive counterparts have a tenfold improvement[8].
Electrically conductive Epoxies (ECE) are ideal for use in processes where the risk of mechanical and thermal cracking is high and where the components are heat sensitive making them unsuitable for soldering or other techniques.
Some of this applications include Advanced Driver Assistance Systems (ADAS) components such as cameras, radar, lidar, and ultrasonic sensors.
Despite these enhancements, epoxy-based die attach materials still show significantly lower thermal conductivity compared to the majority of solder pastes, as also shown in the table4.1, which typically

range from 40-400 W/m·K. This critical behaviour makes adhesive die attach unsuitable for most thermally demanding applications, where other techniques are the preferred choice.

4.2 UV-Curable Epoxy Die Attach

UV curing technology represents an advanced approach for controlling adhesive properties in semiconductor assembly applications. This technology leverages photo-polymerization reactions initiated by specific wavelength exposure (365nm-400nm[7]) to achieve rapid, controlled curing of acrylic and epoxy-based adhesives.
In order to speed up even more the process some die bonding equipments have incorporated dedicated UV sources directly into the bond head assembly allowing for in-situ curing of the epoxies while keeping the component in place ensuring an higher degree of placement precision[9].
Similarly to other methods the best performing parameters are to be found experimentally to better fit each production[7].

4.2.1 Improvements

This type of epoxies have all the advantages at the cost of needing an UV source: they require shorter cure times since the gel formation occurs within seconds of exposure, they can be cured in-situ eliminating problems of drift or thermal expansion and their lower temperature requirement allow for them to be suitable for thermally sensitive assemblies, particularly in medical and precision optical applications (many adhesive cure to optically transparent materials).
Moreover some of these compounds allow for a dual-cure meaning that can support both thermal and UV curing, this allows for a rapid "tacking" with minimal UV exposure (1-2 seconds) followed by final thermal cure in batch ovens for optimized throughput [9]

4.3 Market Available Adhesives

As we have seen in figure3.1 the adhesives dominate the die attach market and this also stems from the wide range of choices available allowing producers to easily find the option that better suits their requirements.
In the table4.1 below we can see the comparison of properties between some market available conductive adhesive materials and Sn63-Pb37 solder paste. It is clearly visible how the thermal and electrical properties are orders of magnitude worse than the solder paste, however their advantages lies in their lower curing temperature (especially with respect to other die attach methods and lead-free solder pastes), low prices, ease of use and low prices making them suitable for the majority of consumers' applications.

	SHIELDOKIT 3980 [10]	LOCTITE ABLESTIK 85-1 [11]	LOCTITE ABLESTIK C990J-584 [12]	LOCTITE ABLESTIK 2000T [13]	EP3HTSDA-2 [14]
TYPE	Glue	Epoxy	Epoxy	Proprietary Hybrid Chemistry	Epoxy
FILLER	Silver	Gold	Silver	Silver	Silver
CURING PARAMETERS	15 min @65°C 7 min @125°C	1 hour @150°C 2 hours @125°C	60 minutes @150°C	30 minute ramp to 175°C + 15 minutes @175°C	20-30 min @120°C or 5-10 min @150°C +1 hour at the same T
ELECTRICAL RESISTIVITY (Ω·cm)	7	≤0.001	2.00×10^{-4}	0.0004	¡0.001
THERMAL CONDUCTIVITY (W/m·K)	1.4	2.07	—	1.7	6.5-7

	FL901S[15]	EP76M[16]	EP79FL[17]	LOCTITE ABLESTIK 3290P [18]	Sn63-Pb37 [19]
TYPE	Film	Epoxy	Epoxy	Epoxy	Solder Paste
FILLER	Silver	Nickel	Silver coated Nickel filled	Silver	—
CURING PARAMETERS	1 hour @120°C 40-45 min @150°C	3-5 days @25°C 2-3 hours @93°C	8 hours @25°C + 2-3 hours @93°C	30 minute ramp to 175°C + 60 minutes @175°C	Reflow peak temp. 183°C
ELECTRICAL RESISTIVITY (Ω·cm)	<0.002	5-10	<0.005	0.02	1.45×10^{-5}
THERMAL CONDUCTIVITY (W/m·K)	2-2.1	1.15-1.30	1.73-2.16	1.73-2.16	50

Table 4.1: Market available conductive adhesives properties comparison to Sn63-Pb37 solder paste

4.4 Conclusion

PROs	CONs
Low-temperature processing: Epoxies cure at significantly lower temperatures than solder reflow processes, making them suitable for temperature-sensitive components	**Low Thermal & Electrical Conductivity**: Even the Epoxies with high metallic component have a low thermal and electrical conductivity with makes them unsuitable for high power applications.
Electrical isolation: non-conductive adhesives have high dielectric strength and resistivity which makes them excellent for electrical isolation of components from substrates	**Cure time requirements**: Unlike solder joints that solidify immediately upon cooling, epoxies require extended setting time for complete polymerization, potentially impacting high-volume manufacturing throughput.
Cost-effectiveness: the materials are cheap and the process does not require heavily specialized equipment moreover the possibility easily rework errors before curing make it very low cost compared to other methods	**Limitation of hermetic sealing properties**: epoxy bonds show problems of permeability to moisture and gases over extended periods of times making them unsuitable where an hermetic sealing is required.

Table 4.2: Pro & Cons table for die attach epoxies.

The strengths of adhesive die attach, as are listed in Pro&Con table4.2 above, lie in their low requirements in terms of cure temperature, equipment and cost while having good mechanical strength and high dielectric strength while on the other hand even the best conductive filled epoxies cannot meet the standards of high-power applications making them suited towards low-end and consumer oriented applications.

Eutectic Die Attach

An eutectic material is a mixture of different metals which, when combined in a specific ratio, have a lower melting point than the individual base materials that make up the alloy. This unique property allows for strong, low-void bonds to be formed without the use of flux, making it particularly suitable for high-reliability applications [9].

5.1 Process Fundamentals

Eutectic die attach is accomplished by placing a chip or die, which has been either plated with the eutectic alloy or by using pre-forms, on the desired pad then while heat is applied to reach the melting temperature of the eutectic alloy both vertical and lateral forces (Scrubbing step) are used to force out air pockets and to displace surface oxides that may be present during the attachment process.

The process requires the heat source to be located within close proximity of the bonding area while the heat can be delivered in a pulsed or steady manner by the heated stage[20] and to have a controlled atmosphere (usually nitrogen/hydrogen combination) to prevent oxidation of the substrate during bonding [7].

Once the Scrubbing step has ended, force is applied to keep the component in place while the joint solidifies. Thanks to the eutectic properties of the alloy the resulting connection will have a melting temperature more similar to the separate elements thus allowing for high operating temperatures.

5.2 Common Eutectic Alloys

The two most widely used eutectic alloys in die attach applications are Au-Sn and Au-Si. Both alloys have extremely high thermal conductivity (Au-Si→170 W/m·K, Au-Sn→57 W/m·K), correspondingly high electrical conductivity and can be used without the need for flux . Not having the need for Fluxing is optimal for applications where the tolerance contamination is very low. low)[5].
The main draw backs are that their composition is high in gold (Au-Si → 97.15 wt% Au and 2.85 wt% Si and melting point of 363°C[21], Au-Sn 80 wt% Au and 20 wt% Sn and melting point of 280°C[5]) which makes them very costly, moreover compared to other low temperature solders they have low ductility which can create CTE stress an issue especially in high temperature applications such as high power modules.

5.3 Conclusion

PROs	CONs
Excellent thermal and electrical conductivity	**Very high cost**
High mechanical strength and reliability	**Need for specialized equipment**
Hermetic sealing capability	**CTE mismatch issues**
No organic compounds or outgassing	**Need for precise temperature control**
Long-term stability at elevated temperatures	

Table 5.1: Pros & Cons table for eutectic die attach die attach solder.

As reported in the table5.1 above, the eutectic die attach method offers very good properties all around however its very high demands in cost of materials and equipment make it difficult for it to ever be a widely used method outside of applications where high performance and reliability are essential such as automotive or aerospace and even there the sintering process may become the preferred choice.

Sintering

6.1 Fundamentals

Sintering is a thermal process in which a powder mixture, sometimes suspended in a liquid solution, is heated and subjected to pressure to create a solid material through compaction. While not a new technology, having been applied to ceramics for 26,000 years and used by Egyptians for metallic tools 5,000 years ago, its application in electronics is relatively recent[22]. Despite its novelty in this field, sintering has already achieved performances and reliabilities superior to soldering, albeit at increased cost.
The driving principle behind sintering is the system's tendency to reduce total interface energy to achieve thermal equilibrium[23]. When heated, materials undergo three distinct stages characterized by changes in porosity and density:

- **Initial stage**: Single-crystal particles in contact cannot undergo grain growth, with the boundary initially confined to the neck area. As the neck surface becomes blunted through growth, inhibition to boundary motion decreases until grain growth becomes possible, marking the end of this stage.
- **Intermediate stage**: in the second stage the contact area between particles increases furthermore, with the density rising from approximately 60% to 90%. Some continuous pore channels along grain edges are still present.
- **Final stage**: The pores shrink and close completely while the grains continue growing in size, reaching up to 99% density.

6.2 Application in Electronics

Sintering has become prominent in electronic die attach because, unlike soldering, it has the advantage of using material such as silver which have superior electrical and thermal properties, without needing to reach its high melting point of 961°C but much lower temperatures therefore avoiding thermal damage to the components.

6.2.1 Materials and Process

For semiconductor chip bonding, sintering typically employs pastes containing the silver particles whose dimension and shape may vary depending on fabrication process, an organic solution to improve the paste adhesion to metallic surfaces and evaporates during the process and optionally some reducing agents aimed at preventing oxidation.
The temperature application, usually done by heating the pressure tip acting on the components, acts as driving force of the sintering process this means that its use has to be carefully controlled: if the heating is lacklustre then the joint does not form correctly while on the other hand an extreme application may compromise the strength of the sintering layer[24].
The applied pressure, which can reach several tens of MPa, has the objective of enabling the bonding and inter-diffusion of atoms at lower temperature and reducing the formation of voids that could lead to delamination and cracking by propagating over thermal cycles[25].

Most sintering tools use single, flat punches to apply force to die tops. However, die thickness variations can result in inconsistent compression across different dies. Multi-punch systems partially address this by applying force to die groups, though thickness variations within groups remain problematic[25].

6.2.2 Performance Advantages

The sintered materials offer significant advantages over traditional solder due to their properties behaving more similarly to bulk silver than an eutectic alloy. For example the melting point of sintered joins is over 900°C (pure Au is 961°C) with thermal conductivities in the range 130–250 W/(m·K) which is around three times the one of the most common solder alloys[26] with thinner bondlines(20–30 μm) and a Coefficient of Thermal Expansion similar to copper which reduces thermal mismatch defects due to strees in the materials. These advantages are particularly more evident with SiC substrates, which have thermal conductivity more than twice that of silicon, where the traditional solders' have a limiting effect on the performances of the devices[26].

6.2.3 Industry Adoption and Cost Considerations

Several leading Original Equipment Manufacturers, such as Tesla, VolksWagen, and BYD, have made the transition from solder alloys to Ag sintering technologies thanks to its increased reliability and thermal stability. However, the primary drawback remains the cost of materials and equipment since silver high price makes sintering economically unsustainable for many applications despite the superior results.

To address cost concerns, manufacturers have developed tin-containing mixtures that reduce material costs while enabling lower processing temperatures and producing compounds with higher electrical and thermal conductivity than pure silver. Recent improvements, including nano-inks and dry film transfer techniques, have reduced sintering times to 2–5 minutes with mild pressures (significantly less than 30 MPa), making the process suitable for ultra-thin dies. IDTechEx analysis suggests that Ag sintering will primarily serve mid- to high-end vehicles from leading automotive OEMs, while low-end vehicles will continue using traditional solders due to cost considerations[27][28].

6.3 Copper Sintering

Copper sintering represents an emerging alternative that could potentially address the high costs associated with silver sintering. Cu-sintering theoretically offers the cost advantage that would make sintering the preferred technology for die attach however with it come the technological challenges of keeping the copper from oxidizing which greatly reduces the joint strength. To try and avoid copper oxidation there is the need of highly controlled N_2 or H_2 environments.

6.3.1 Advantages and Challenges

Copper sintering theoretically offers significant cost advantages, with leading suppliers reporting costs as low as half those of Ag sintering. However, the technology faces substantial challenges due to the copper tendency to easily oxidate reducing the joint strength

- Copper oxidation significantly reduces bond effectiveness
- Process complexity exceeds that of silver sintering
- Current paste costs remain similar to or higher than silver alternatives due to early development stage

6.3.2 Adoption Timeline

As of 2024, large-scale adoption of Cu sintering in EV power electronics has not occurred, though companies like VW are conducting tests. IDTechEx projects potential adoption beginning in late 2024 or early to mid-2025, contingent on overcoming technical challenges and achieving cost reductions[27].

6.4 Conclusion

While sintering technologies offer superior performance compared to other die attach methods, their adoption remains limited by cost and technical challenges. As for now only high-end application justify the premium performances of sintered connections while in the meantime the research in the field goes toward cheaper paste formulations (lower silver concentrations) and to machinery able to apply pressure in a non-uniform way in order to account to differences in thickness of components, different temperature and pressure requirement which is paramount for SiP and HI where different elements are placed together.
Once these improvements have been made sintering will surely become one of the more commonly used methods, if not the preferred one, as also projected by market analysis6.1.

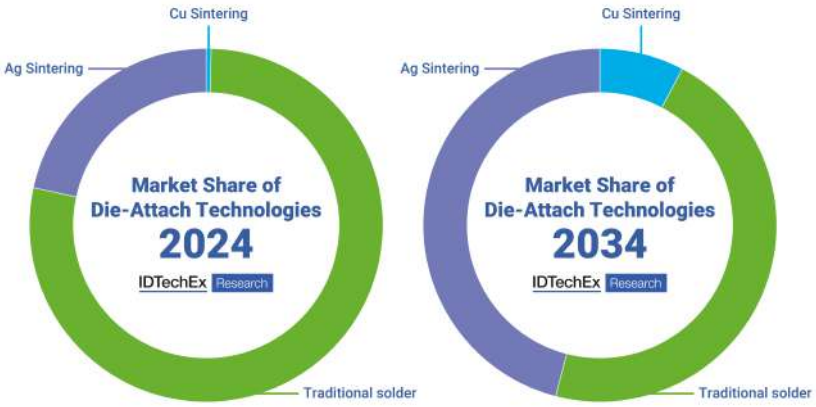


Figure 6.1: 2024 market analysis and 2034 market prediction by IDTechEx[28] projecting a doubling of Ag sintering share

Thermocompression Die Bonding

Thermocompression bonding, also known as diffusion bonding, pressure joining, thermocompression welding, or solid-state welding [29], is a flip chip assembly process where heat and pressure are simultaneously involved during the bonding phase of a pick and place process[30]. The force and temperature cause lattice vibrations at the interface between the two metal brought in contact in such a way that the atoms are able to diffuse and migrate between lattices[7].
The results are highly thermally and electrically conductive bonds, free from flux, lead or adhesives otherwise needed to join the die and the package with the exception of under-fill materials used to make the joint more stable and structurally robust.

In die attach applications, this technique typically requires temperatures as high as 350-400°C and forces of as much as 100 g/bump for flip-chip applications while lasting only a fraction of a second[9][31].
Thermocompression bonding is mainly used in key applications such as the vertical stacking of devices and wafer-level packaging in CMOS processes, in flip-chip application to bond the solder bumps to the corresponding pads and it's the preferred method for performing wire bonding. Moreover recent advances in TCB equipment offer solutions for all chip-to-chip (C2C), chip-to-substrate (C2S) and chip-to-wafer (C2W) bonders[31].

7.1 Materials

Thanks to their high diffusion rates, gold (Au), aluminium (Al), and copper (Cu) are the most commonly used materials in thermocompression bonding[29].

- **Gold**: Au still remains the most established material for thermocompression bonding, particularly in high-reliability applications where it offers excellent thermal and electrical conductivity paired with strong oxidation resistance, allowing for the bonding to occur in ambient atmosphere without special protection. Gold forms highly reliable bonds, though its high cost limits use to specialized applications like aerospace, medical devices, and high-frequency RF components.
- **Aluminium**: Al is widely used in power electronics and wire bonding applications despite its tendency to form a native oxide layer. For this reason aluminium bonding benefits from ultrasonic energy assistance to break through the oxide layers enhancing atomic interdiffusion[32].
- **Copper**: Cu has gained significant traction as a more cost-effective alternative to gold, especially in advanced packaging. The main challenge lies in preventing oxidation by performing surface treatments and bonding in ultra high vacuum. Cu-Cu thermocompression bonding is very important for the stacking of dies since the back-end-of-line (BEOL) interconnections are usually made in copper.

PROs	CONs
High thermal and electrical conductivity	High temperature and force requirements may damage sensitive dies
Excellent mechanical strength and structural integrity	Dies that are thinner, brittle, or intolerant of high heat may not be suitable
Clean bonds free from flux or lead contamination, no organic compounds or outgassing issues	Requires precise control of surface conditions and oxide removal (requires extremely smooth surfaces with microroughness <0.5 nm[33])
Fast processing time	High equipment and tooling costs for specialized bonding systems

Table 7.1: Pro & Cons table for thermocompression die attach.

7.2 Thermosonic Bonding

Thermosonic bonding is an advanced variant that combines thermocompression bonding with sonic vibrations in order to reduce the high temperature and pressure requirements of the process.
This simultaneous application of thermal energy, mechanical force, and ultrasonic vibration (ranging in between 60-132 kHz, with higher frequencies showing better reliability) creates an "ultrasonic softening effect"[34] by interacting at the atomic lattice level, dramatically facilitating the deformation and atomic contact at lower temperatures (100-160°C compared to around 300°C for thermocompression) and forces (20-50 g/bump (compared to more than 100 g/bump for thermocompression).
The optimal bonding window requires careful balance of all parameters, as excessive ultrasonic power or force can cause bump collapse or electrical shorts between adjacent connections [35].

7.3 Conclusion

Industry experts still see thermocompression bonding as an attractive prospect because of its high performance yield however there is the need for the future applications to develop into more cost effective solution for a broader range of applications and for even smaller bump pitches.

Cu-Cu Hybrid Bonding

8.1 Technology Overview

Hybrid bonding interconnection enables a connection from a silicon chip to another with direct metal pad to pad connection of the planar damascene surface[36]. The hybrid bonding interconnection considers both Cu-Cu bonding and dielectric-dielectric bonded interfaces, requiring detailed process controls with handling copper and dielectric materials, which can be performed by thermal compression bonding(TCB) and direct bonding interconnection (DB or DBI)[37] creating connections at atomic level removing the need of additional solder/sintering materials.
Hybrid bonding connects the of the integrated circuit without the need for any intermediate materials like solder or adhesives. Instead an instantaneous chemical bond is formed between the mating dielectrics on each wafer. As the temperature increases in the batch anneal process, the bond strength between the dielectrics increases With hybrid bonding it is possible to perform both wafer to wafer and die to wafer bonding which are essential for 3D stacking and for Heterogeneous Integration The process begins with meticulous surface preparation using chemical mechanical polishing (CMP) to achieve surface roughnesses below 0.5 nm RMS. Following this preparation, plasma activation treatments enhance the bonding capability of the surfaces without damaging the copper structures. The activated dies must then be precisely aligned with accuracies within $\pm 0.5\ \mu m$ and brought into contact at room temperature. Once in contact, an annealing process at temperatures between 200–400°C promotes Cu atom diffusion across the metal interface, while simultaneously enabling dielectric fusion of the surrounding materials to create a hermetic seal[37][38][39].

8.2 Technical Advantages

Cu-Cu hybrid bonding offers new advantages over both traditional flip-chip soldering and sintering approaches, particularly in terms of dimensional capabilities, electrical performance, and thermal management[40].

The electrical performance benefits stem primarily from the elimination of intermediate materials and by the creation of direct copper pathways. By removing underfill materials, parasitic capacitance can be reduced by up to 90%, while the direct Cu-Cu contact provides resistance values approximately ten times lower than typical solder joints. The shorter connection paths inherent to this technology also reduce inductance by 70–80% compared to traditional approaches. These improvements collectively enable the interconnects to support current densities higher than $10^6 A/cm^2$ without suffering from electromigration damage, which is a critical advantage in high-performance applications.

From a thermal perspective, Cu-Cu hybrid bonding excels due to the superior conductivity of the direct copper pathways, which at 400 W/m·K significantly outperforms both solder joints (50–60 W/m·K) and sintered connections (130–250 W/m·K). The elimination of thermal interfaces between copper and solder removes additional thermal barriers, while the continuous copper network enhances lateral heat dissipation throughout the package structure.

8.3 Process Considerations and Challenges

Surface Requirements

The extreme surface quality requirements present significant manufacturing challenges that must be carefully managed. Surface roughness must be maintained below 0.5nm RMS, requiring sophisticated CMP while the particle contamination tolerance is near zero, necessitating Class 1 cleanroom environments throughout the process. Additionally, copper oxidation must be prevented through careful atmospheric control and surface passivation techniques.

Alignment Precision

Due to its small pitch size hybrid bonding demands sub-micron alignment accuracy achievable only with sophisticated equipment such as advanced optical or infrared alignment systems that must work in conjunction with specialized bond tools capable of positioning accuracy greater than 100 nm. This process requires active compensation for thermal expansion effects during the heating, along with real-time alignment verification. These requirements represent a significant increase in complexity compared to traditional die attach methods.

8.4 Applications and Implementation

Current Applications

Cu-Cu hybrid bonding has found initial adoption in several high-performance applications:
In 3D NAND memory, the technology enables high-density memory stacks while CMOS image sensors benefit from the fine-pitch connections between pixel arrays and logic chips. High-bandwidth memory (HBM) implementations achieve bandwidths greater than 1 TB/s through the high-density interconnects, and advanced logic applications utilize the technology for 3D integration of chiplets in high-performance processors.

8.5 Conclusion

Cu-Cu hybrid bonding is poised for broader adoption as equipment costs decrease with volume production and process windows expand through continued technology improvements. The development of industry standards for hybrid bonding interfaces will facilitate wider implementation, while the evolution of design tools specifically supporting hybrid bonding architectures will ease adoption barriers. Key development areas driving future advancement include room temperature bonding processes that would eliminate annealing requirements for temperature-sensitive applications. Selective bonding approaches that combine hybrid bonding with other attachment methods on the same substrate offer flexibility for heterogeneous integration. Scaling the technology beyond current wafer capabilities will be essential for large area applications. Cost reduction remains a priority, with research focusing on alternative surface preparation and activation methods that could reduce the stringent requirements while maintaining bonding quality.

Soldering

Soldering is the most common and cost-effective method to create mechanical, thermal and electrical interconnections between metallic material. The process involves the use of a molten metallic compound that, when solidified, bonds different components, substrates or, more in general, two different metallic elements together.
In Electronics we can have Through Hole Technology (THT) or Surface Mount Technology (SMT), in the former the elements are inserted in pre-drilled holes in the PCB and soldered on the other side, it was predominant until the 1980s however nowadays is preferred only for those components requiring enhanced mechanical stability. Once the circuits became more complex and more dense of components the THT could not keep up with the demands and thus, by the late 1990s SMT, where, as the name may suggests, the components are mounted and soldered directly on the surface of the PCB, dominated high-tech electronic assemblies with surface-mounted components accounting for over 75% of electronic manufacturing by 2024.
Moreover the transition from THT to SMT was also driven by several factors other than the higher component density such as: improved electrical performance due to shorter lead lengths, reduced parasitic inductance and resistance, and better automation capabilities for mass production.

For both THT and SMT there are several different soldering techniques that can be applied each with distinct advantages and limitations:

- **Dip Soldering** $\Longrightarrow$ useful for the THT where, after the components are inserted, the PCB is fluxed and then manually dipped into molten solder. Upon lifting, the solder will remain attached to the metal contacts where the solder mask of the PCB is not present then it cools down forming the connection.
- **Wave Soldering** $\Longrightarrow$ is the "automated bulk version" of dip-soldering where PCBs are placed on a conveyor belt and, after being sprayed with flux, will pass over a reservoir where molten solder is pumped up creating a "wave". Similarly to dip solder the solder material will bind only where the solder mask is not present.
- **Reflow Soldering** $\Longrightarrow$ the primary technique for SMT assembly where a solder paste (solder powder + flux) is deposited (different application methods are available) in correspondence of the PCB pads, then the electronic elements are positioned, held in place by the paste's tackiness, then the board undergoes a controlled thermal process inside a reflow oven where the solder powder will melt while the flux evaporates leaving behind the metal connection.
- **Soft Soldering** $\Longrightarrow$ is one of the more popular choices best suited for attaching small and fragile components onto a PCB. Soft soldering liquid needs to stay below 400°C to avoid breaking down the board and components. In this process a metal alloy, usually tin-based, in the form of wire or paste is heated until it melts and creates a solid connection between elements when cooled. The resulting joints are usually not as strong as other techniques giving it its name. [41].
- **Hard soldering** $\Longrightarrow$ is not used for electronic application but rather metal working, where soldering iron is not enough a torch is used to create sufficient heat (between 450°C and 900°C) to melt a solid solder to produce joints with significantly higher mechanical strength (200-300 MPa) compared to soft soldering (<50 MPa). It is generally used for combining metal parts such as copper, brass, silver, or gold.

The selection of appropriate soldering technique depends on several factors including the component thermal sensitivity, the required joint strength, the production volume, the devices' assembly complexity, and the environmental operating conditions. Most modern industrial electronics manufacturing adopted automated SMT mass reflow processes due to their precision, repeatability, and cost-effectiveness in high-volume production.

9.1 Solder Materials

The soldering material can come in different mediums, namely:

- Wire
- Powder
- Paste

while soldering wire is more suited for a manual soldering of big components and solder powder needs the extra step of being mixed with flux, solder pastes are the most commonly used for electronic applications, especially in industrial environments, due to their ready-to-use nature and tackiness that keep component in place.

9.2 Solder pastes

Solder pastes are composed by 2 elements already mixed together: the metal alloy powder and the flux (by volume it is usually 50/50 while by weight is around 90% metal[42][43]).
The metallic powder are usually composed of several elements, the more common formulations are tin-based with additions of copper, silver, gold and bismuth to provide the thermal and electrical properties required by the soldered joints. On the other hand the flux job is to clean the surfaces and prevent further oxidations while increasing the wetness of the paste making it adhere better to the components and pads.
During the reflow process while the powder melt the flux evaporates leaving behind only the joined metallic elements creating the electrical and mechanical connections essential for the proper functioning of the electronic device.

9.2.1 Pastes Classification

According to Institute of Printed Circuits (now Global Electronics Association) standard J-STD-004 "*Requirements for Soldering Fluxes*", the solder pastes can be classified depending on their flux properties making the distinction between rosin based, water soluble and no-clean fluxes. A similar classification is done regarding the size of the powder particles, under the IPC J-STD-005 standard the pastes can be divided as depicted in the table9.1.

Type	Particle Size Range (μm)	Typical Application
Type 1	75-150	Large pads, not common
Type 2	45-75	General purpose, older designs
Type 3	25-45	Standard for most SMT
Type 4	20-38	Fine pitch
Type 5	15-25	Ultra-fine pitch
Type 6	5-15	Specialized applications
Type 7	2-11	Specialized applications
Type 8	2-8	Specialized applications

Table 9.1: IPC J-STD-005 Solder Powder Classification by Particle Size
. The highlighted types are the most commonly used in applications ranging from industrial to research.

For a paste to fall inside one of the types at least 80% of the powder particles must fall into the size range and there are also imposition on how much of the solder can be above or below the limit with the allowed percentage shrinking the further the size is from the stated one.

The choice of grain size are still dependent on application, a bigger grain like Type 3 is cheaper but still suited for most application while the finer grains, more costly, are used to improve printability for smaller components since they can pass uniformly through smaller stencil apertures[44].

However an higher type does not have only advantages at a monetary cost, since a smaller powder size corresponds to a significantly higher surface area (20% and 75% more than T3 for T4 and T5 respectively[44]) which proportionally relates to the rate of chemical reactions that can occur leading to potential issues such as oxidation.
Therefore the shelf life of pastes with finer grains is usually shorter due to reaction between powder and flux and generate more random solder balling and graping than other, bigger, pastes[44].

9.3 Solder Paste properties

Many high power semiconductor packages primarily dissipate heat through the Die Attach material as it is typically the first material between the die and heat spreader and thus must provide critical thermal characteristics in order for the die to perform at its peak operating levels.
Several characteristics of a paste contribute to the performance of the devices which has to be taken into consideration since usually "the perfect paste" does not exist and there is the need to find the best compromise suited for the desired application. The most important properties are dependent on the paste composition, the materials that make up the paste are what set its eutectic melting temperature, electrical behaviour and mechanical stability, for instance, adding small amount of micro or nanosized metallic particles such as nickel (Ni), silver (Ag), copper (Cu), antimony (Sb), zinc (Zn), silicon (Si), cobalt (Co), chromium (Cr), titanium (Ti) and Rare Earth elements into the solder matrices is an effective way to improve the mechanical properties without significantly alter the melting point, on the other hand materials such as indium (In) or bismuth (Bi) are used as as melting point reducers while adding oxide nanoparticles such as zirconia (ZrO2), alumina (Al2O3), cerium oxide (CeO2), fullerenes (FNSs) and multi-wall carbon nanotube (MWCNT) could refine the final microstructure improving joint strength[45].
Generally what are considered the most important properties of a solder paste are:

- Thermal Conductivity since the solder paste is the first point of contact of the device it needs to be able to dissipate heat efficiently (most solder pastes' thermal conductivity is in the range 40 W/m*K to 80 W/m/K depending on composition).
- Electrical conductivity is a critical in the performance of high power semiconductor applications since the joints also need to provide a path for electrical signals without creating noticeable distortions or delays and with little resistance is also promoted a better thermal dissipation through the package. [46]
- Mechanical Stability and reliability, the die or device needs to be securely kept into place in order to work. Joints can be more or less brittle, susceptible to rupture due to vibrations or thermal cycling in working regimes which can cause poor performances or critical failure such as delaminations.
- Wettability is needed to create good adhesion between the device, substrate and paste to ensure the correct formation of a stable joint.
- Coefficient of Thermal Expansion is important to know in order to avoid having too great of a mismatch between solder/device and solder/substrate interfaces which can cause failures in devices with high operational temperatures.

9.4 Flux

Flux is the non-metallic component of solder paste that enables a reliable solder joint formation. While nearly inert at room temperature, flux becomes strongly reducing when heated, allowing it to clean surfaces by removing oxides, preventing the re-oxidation during the heating process while facilitating the solder flow and wetting allowing an uniform distribution.

9.4.1 Chemical Composition

The flux is composed of a complex mixture of chemicals[47] that give it its properties whose amounts may vary from formulation to formulation. The solvent job is to control the viscosity and keep the other elements suspended in the solution, then the rosin or resin, depending of flux type, provide the primary protection from oxidation of the hot metal component while the activators (organic acids or halides) dissolve the metal oxides to clean the surface, on the other hand the surfactants are used to lower the contact angle of the paste to improve wettability and rheology modifiers are used to improve the non-newtonian properties of the paste which are essential during printing and to keep components in place.

9.4.2 Classification of fluxes

Following the IPC J-STD-004 standard "Requirements for Soldering Fluxes" the categorization of fluxes depends on composition, activity level, and reliability characteristics:
the flux composition can differentiate between rosin (RO) which is naturally extracted from pine trees, resin (RE) which is the synthetic counterpart to rosin and inorganic (IR) or Organic (OR) which are usually water-soluble.
The activity level can be either low (L), medium (M) or high (H) and depending on halides presence 1 or 0.
For example a rosin based low activity flux with halides would be referred to as ROL1.
The reliability requirements refer to corrosion resistance, electromigration resistance and surface insulation resistance.

Another Classification of fluxes that can be made depends on the residues left after the soldering is completed. In fact the standard paste require cleaning of the flux my means of some cleaning agent such as isopropyl alcohol while the no-clean formulation leave behind small to none residue and lastly there can be water-soluble fluxes that don't require specialized cleaning agents other than deionized water.

9.5 Common Defects and Failures

Soldering defects can compromise both the electrical functionality and mechanical reliability of electronic assemblies. These failures can be categorized by their root causes and manifestation mechanisms.

9.5.1 Thermal-Related Failures

Cold Solder Joints

Cold joints form when the solder fails to reach proper liquidus temperature or solidifies prematurely, resulting in weak electrical and mechanical connections (high electrical resistance) characterized by a grainy and dull appearance instead of smooth shiny finish.
They may be cause by an insufficient temperature reached by the component, a contaminated surface or an inadequate flux activation.

Overheated Joints and Component Damage

When on the other hand we have an excessive thermal exposure the resulting in charring and destruction of components, excessive intermetallic growth (layers 4μm weaken the reliability[48]), weakening of adhesion forces between device and PCB causing Pad lifting or overheating of the flux which results in poor wetting.

Thermomechanical Stress Failures

Particularly critical in power modules and die-attach applications depend on CTE mismatch between chip (CTE $\approx$ 3 ppm/°C) and substrate (CTE $\approx$ 17 ppm/°C) which induces cyclic stress[49] that can cause Delamination, Void growth and crack propagation over multiple thermal cycles.

9.5.2 Printing, Wetting and Reflow Defects

Tombstoning (a.k.a. Manhattan or crocodile Effect)

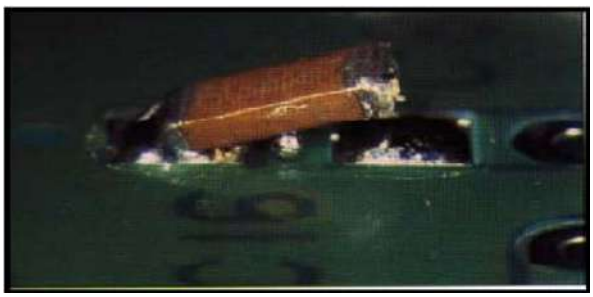


Figure 9.1: Tombstoning image[50] where the component is lifted similarly to a drawbridge.

Defined when small components (like 0402 or 0201) are lifted almost vertically as a tombstone which is caused by an imbalanced surface tension forces due to an uneven solder paste melting between the different pads. The resulting torque imbalance lifts one end while only the other one undergoes normal soldering[48]. This imbalance can depend on differences in paste volume between pads (errors in printing), uneven heating of the solder in the oven or component placement offset exceeds 30% of pad width.

Solder Bridging

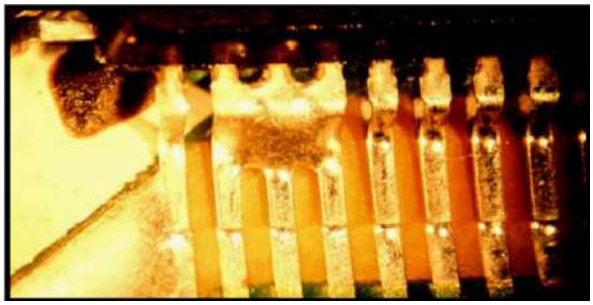


Figure 9.2: Bridging image[50] where solder meant to be separated joined together with the risk of forming short circuits.

Bridging, as in figure9.2, happens when an unintended connections between adjacent pads is formed causing short circuits and unwanted electrical connections.
It can be caused by several factors such as excessive paste volume (stencil aperture too large), poor thixotropic properties of the paste causing slumping, presence of contaminants reducing the paste surface tension, misalignments or insufficient pad spacing for the chosen paste type in the design.

Wicking (Solder Thiefing)

Figure 9.3: Wicking image from [50]

Properly wetted solder naturally aligns itself on the PCB pads, however due to defect in the PCB design, thermal imbalances in the reflow process or exposed copper traces near the pads that act as thermal sinks, can sometimes make the molten paste flow away from the intended site creeping up onto the devices9.3 resulting in and insufficient amount of solder which can cause open circuits and/or weak mechanical connections[48]

Reflow profile problems

If the reflow Profile is not optimized for the solder paste and devices/components-to-be-soldered many of the different, already cited defect may arise, for example the Ramp-Dwell-Ramp-to-Peak profile, while historically common, has extended dwell times that can causes premature flux exhaustion (poor wetting equals weak joints), and a rapid final ramp that may induces spattering and thermal shock in the components and the overall long exposure promotes oxidation and intermetallic growth which causes brittleness in the connections.

Solder Balling

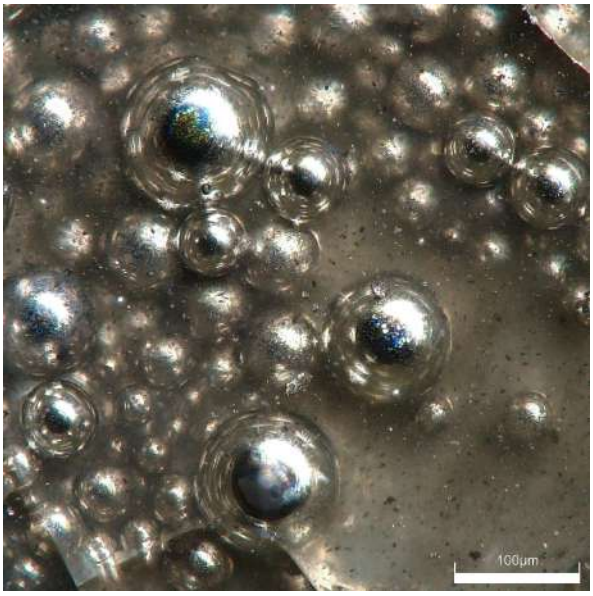


Figure 9.4: Solder Balling obtained during my tries.

Solder balling consists in the formation of isolated solder spheres adjacent to joints caused by rapid solvent evaporation (rise in temperature >3°C/s) which disperses paste particles (Spattering mechanism), or extended dwell times that oxidizes dispersed particles preventing the coalescence[51] (Oxidation mechanism) as in the case in figure9.4 and RDRP profile particularly exacerbates both mechanisms[48].
Solder balling can either be negligible or be the cause of bridging and thus short circuits. Balls $> 150\mu$m violate IPC-A-610 Class 2 requirements.

Solder Splashes

Figure 9.5: Solder splashes obtained during my tries.

Finer and more dispersed solder droplets as seen in figure9.5 than solder balling scattered across the PCB or substrate, caused by violent flux outgassing during rapid heating, moisture in paste causing explosive evaporation or contamination lowering surface tension.
Similarly to solder balling can cause electrical shorts if bridging fine-pitch traces[52]

Graping

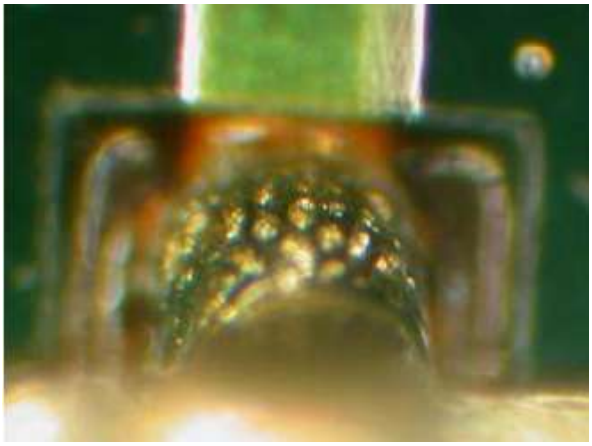


Figure 9.6: soldered joint showcasing graping[53].

Is the formation of clusters of un-coalesced solder spheres, similar to solder balling with the difference that the particles remain partially agglomerated to the joint as in figure9.6.
It is more common with Type 4 and Type 5 pastes due to higher surface area oxidation and is caused by an insufficient flux activity to reduce oxide layers between particles.
It can often be the tell tale of an expired paste or presence of contamination.

Insufficient Solder Volume

Results in weak joints with poor mechanical strength, caused by:

- Stencil aperture clogging (requires cleaning every 10-20 prints)

- Excessive squeegee speed (>50mm/s)
- Poor paste release (area ratio <0.66 for fine-pitch)
- Paste viscosity changes due to aging or temperature

9.5.3 Voids

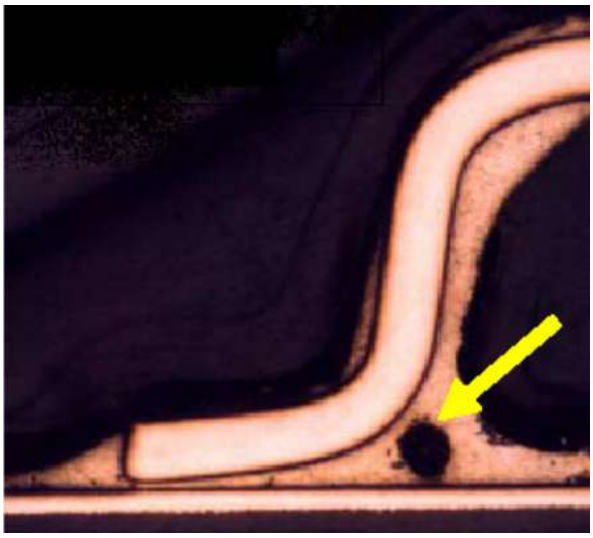


Figure 9.7: Void image from [50]

Voids form when gases become trapped in solidifying solder. Voids can create cracks, propagate and can grow during thermal after working cycles and can lead to breaking of the soldered joints. Voids cycling and can be differentiated between:

- **Macro voids** ($> 100\mu$m): Flux outgassing trapped by rapid solidification
- **Micro voids** ($< 100\mu$m): Dissolved gases precipitating during cooling
- **Shrinkage voids**: Volume contraction during solidification

9.6 Mitigation Strategies

Most of these defects are fairly easy to incur and can greatly undermine the devices and the whole system ability to perform thus it is of the upmost importance to implement as much care and attention to the prevention of mistakes.
The key points to follow are:

- **Process optimization**: Profile development based on paste specifications
- **Design for manufacturing**: Appropriate pad sizes and spacing
- **Material control**: Paste storage, handling and shelf life management
- **Environmental control**: Temperature, humidity and contamination management
- **Regular maintenance**: Stencil cleaning and equipment calibration

9.7 Sustainability of Die Attach Materials

With the ever increasing demand for electric and electronic devices in the every-day life the electronic components waste has become one of the fastest growing waste contributor with the possibility of releasing hazardous substances during the handling and disposal creating risk for health and for the environment.

9.7.1 RoHS

In order to prevent and reduce these risks at the source the Restriction of Hazardous Substances Directive 2002/95/EC (RoHS) was adopted in February 2003 by the European Union and later revisited with the RoHS 2 directive (2011/65/EU)
RoHS is often referred to as the "lead-free directive" since lead was the most widely spread material among the 10 elements banned by this directive. For these prohibited substances the Maximum Permitted Concentration is of the 0.1% or 1000 ppm while for Cadmium it is even lower at 0.01% or 100 ppm[54].

9.7.2 Exemptions

There are exemptions for applications where no Pb-free solution is known, the manufacturer have to regularly apply to renovate them after five to seven years and are regularly reassessed based on if the possible substitutions are available, practical, consumer safe and if the substitution may have adverse socio-economic impact[54].

9.7.3 Waste from Electrical and Electronic Equipment (WEEE)

On the other hand the Waste from Electrical and Electronic Equipment (WEEE) aims to improve the collection, treatment and recycling of electrical and electronic equipment at the end of their life going towards a more circular economy. Following the directive as a guide each European Union member state will have to adopt its own enforcement and implementation to address environmental and other issues caused by the increasingly higher number of discarded electronics. The objective is to reach a sustainable a production by firstly reducing the amount of WEEE created, by ensuring that a circular economy is implemented where raw materials are retrieved and re-used and by improving the life cycle and environmental impact of every stage of the production processes[55].

The WEEE directives requires European countries to properly collect and separate wastes for their recovery and recycling, fight against illegal waste export and to create more standardized national EEE registers and reporting format.

The overall aim was for the EU to recycle at least 85% of electrical and electronics waste equipment by 2016 but after some dispute over its efficiency the Commission started an evaluation of the WEEE Directive in order to assess whether the Directive is still fit for purpose, explore possibilities to simplify it and determine whether a review is needed[55]. The outcome of this evaluation came out in 2025 and it stated that albeit the overllall amount of WEEE collected increased significantly between 2012 and 2021 (due to an increase in production of electronic material in those years) only very few countries were able to meet the recycling quota and nearly half of the WEEE generated is still not being collected[56].

9.8 Lead-Free Solders (LFS)

For what concerns the Solder Pastes the implementation of the RoHS directives meant the transition from an almost totality of leaded pastes to lead-free alternatives.
However, the removal of lead from the pastes formulations has resulted in worse electrical and mechanical properties, increase of melting points and thus thermal burden onto the devices, worse wetting properties, increased formation of Inter-Metallic Compound (IMC) causing brittleness[46] and a general higher cost of pastes due to the inclusion of valuable materials (usually gold and silver) to improve the paste electrical and thermal properties to meet the standards for functioning joint.
[57]

- Degraded electrical and mechanical properties.
- Increased melting points.
- Enhanced formation of Inter-Metallic Compound (IMC)
- Inferior wetting characteristics, particularly on oxidized surfaces.
- Reduced spread compared to lead-based alternatives.
- Increased component joint stress due to higher temperature .requirement
-

To improve wettability a more aggressive flux can be used but this implies a thorough post-solder cleaning in order to prevent flux-related problems such as corrosion, dendritic growth, poor adhesion of the coatings and electromigration which can cause short circuits between circuit traces.
As we can see in the market analyses in figure9.8,9.9 and 9.10 even if, as of 2024, the implementation of LFSs covers almost 3/4 the market, the same cannot be said when all types of soldering materials are considered were two fifths are still containing lead and are projected to not decrease (only in percentage with respect to lead-free solders) unless the discovery of some new material or technique isn't made.

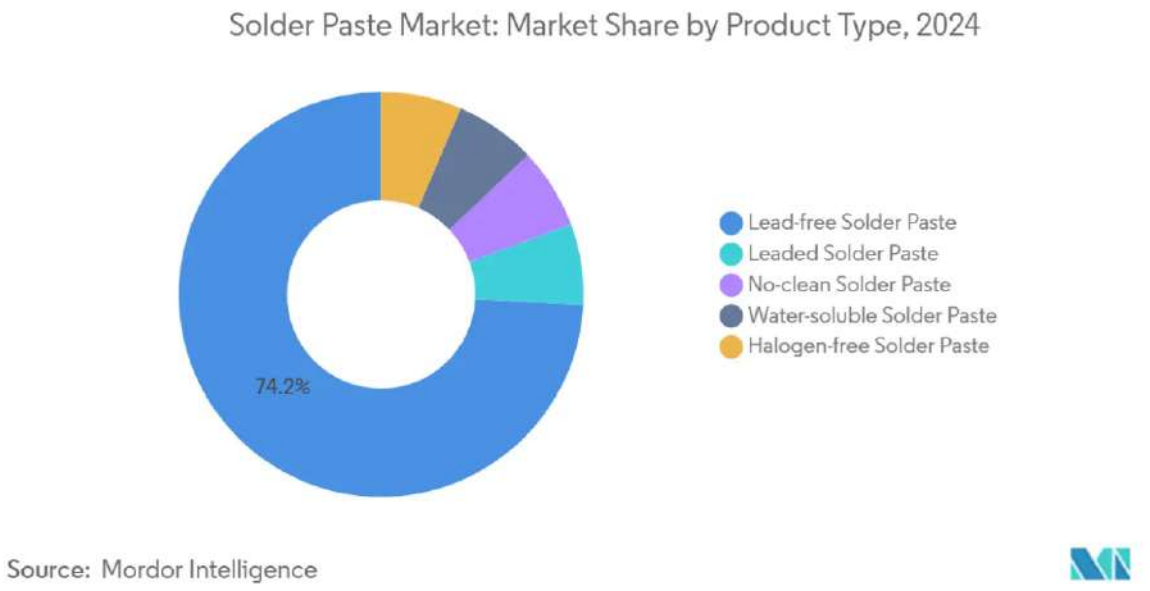


Figure 9.8: Market analysis showing the market share of lead vs. lead-free solder pastes as of 2024[58]

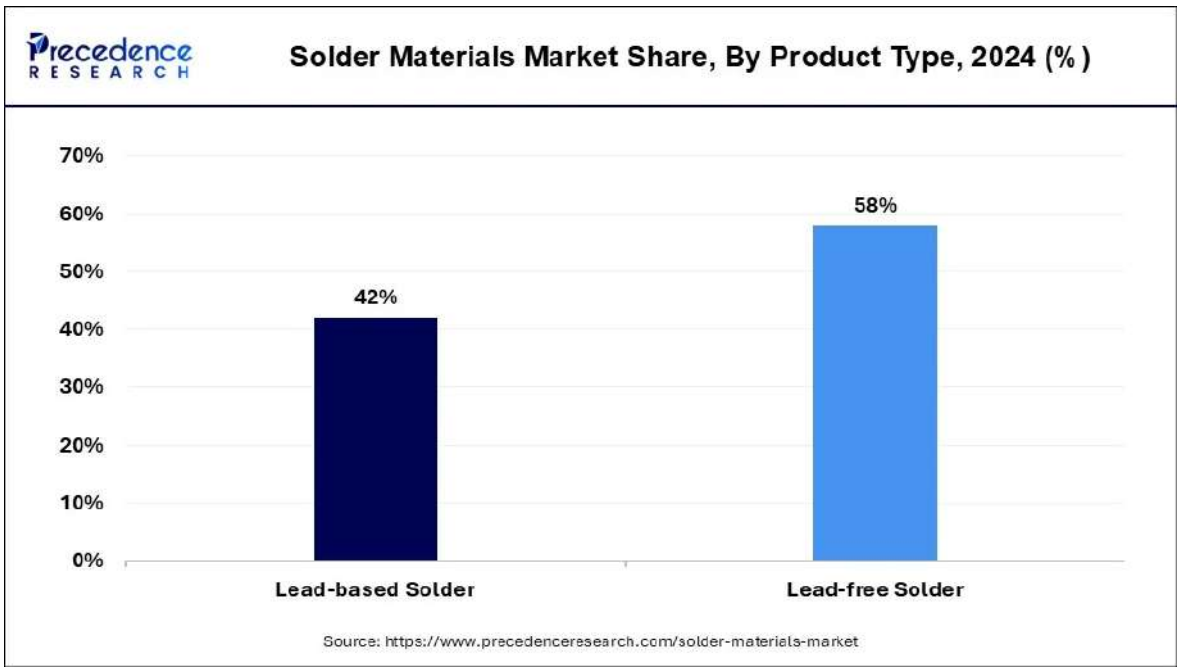


Figure 9.9: Market analysis showing the market share of lead vs. lead-free solders as of 2024[59]. In this case are not considered only the solder pastes but solders materials of every form (powder, paste and wire).

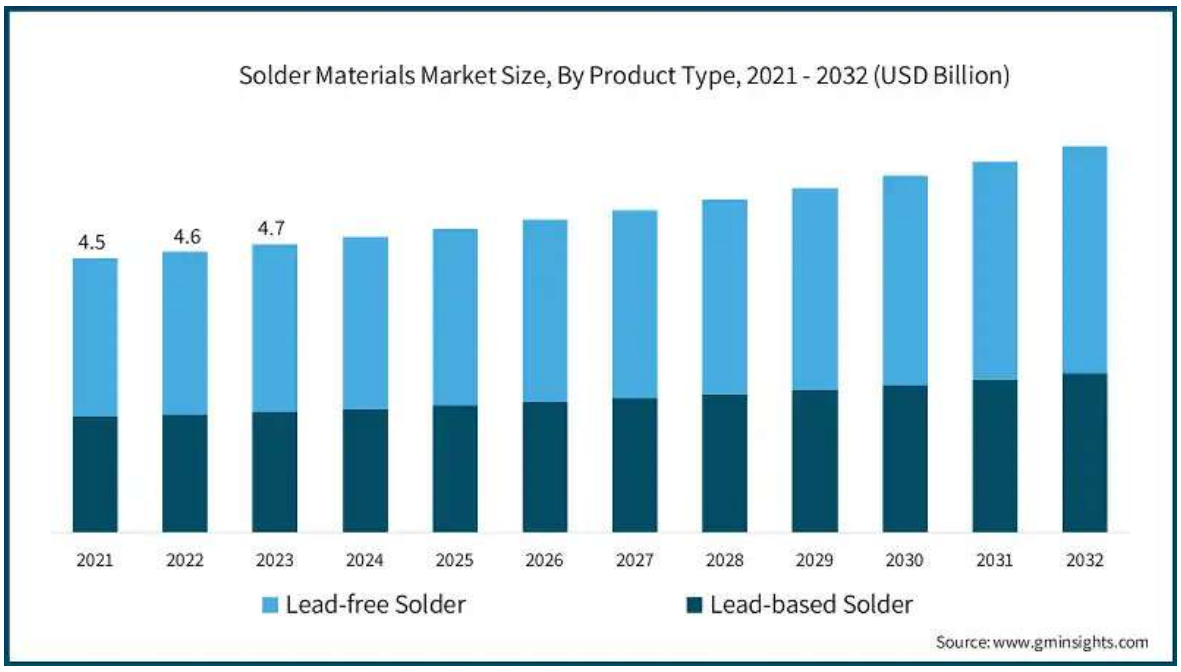


Figure 9.10: Market analysis showing the market of solders material with growth prediction up to 2032[60]

9.8.1 SAC

The most promising LFS are almost exclusively made of Tin (Sn) plus other compounds, most notably the one considered most suitable as replacement of leaded solders is the tin-silver-copper Alloy (SAC) which depending on the relative quantity of silver and copper changes name and properties slightly (e.g SAC305 has 3% of silver and 0.5% of copper is the most widely used, while cheaper alternatives with less silver are also used in some applications, such as SAC105[61] 1% silver and SAC0307[62] with 0.3% silver, 0.7% copper, at the expense of a somewhat higher melting point. On the other hand are also available some alternatives with increased silver presence in order to have a better electrical and thermal performance such as SAC387[63] where silver content is increased to 3.8%
SAC305 is considered one of the most reliable alternatives with the better properties, responsible for its popularity.

9.8.2 Sn-Bi-Ag Alloys

Among the emerging LFS technologies, low-temperature bismuth-based alloys, and in particular Sn42Bi57Ag1 (42% tin, 57% bismuth, 1% silver), represent a significant shift from traditional high-temperature lead-free solutions in fact this eutectic composition exhibits a very low melting point of 137-139°C, approximately 80°C lower than SAC alloys and 45°C lower than traditional Sn-Pb eutectic solder[64]. The substantial reduction in processing temperature offers compelling advantages for temperature-sensitive applications and energy conservation in manufacturing. The low processing temperature of Sn-Bi-Ag alloys enables several critical advantages in modern electronics assembly. Components with limited thermal tolerance, such as Light-Emitting Diode (LED)s, optical sensors, and certain polymer-based devices, can be successfully soldered without degradation. Additionally, the reduced thermal stress minimizes substrate warpage, particularly beneficial for thin or large-format boards where traditional reflow temperatures induce significant mechanical deformation. Energy consumption during reflow is reduced by approximately 20-30% compared to SAC processing, contributing to manufacturing sustainability goals[65].

However the high bismuth content introduces inherent brittleness, particularly at low temperatures, making joints susceptible to fracture under mechanical shock or vibration[66]. Moreover when bismuth-containing solders come into contact with some elements it can for ternary phase alloys with melting points as low as $\approx$ 96°C (Sn-Bi-Pb) this property is know as the "bismuth effect" and need careful planning in the materials involved in the various processes where bismuth is present[67].

Another critical concern with Sn-Bi-Ag alloys is their incompatibility with existing Sn-Pb and SAC solders in mixed assemblies.

The application window for Sn-Bi-Ag alloys continues to expand as process understanding improves. These alloys excel in specific niches including consumer electronics with limited thermal cycling requirements, first-level interconnects in multi-chip modules, and step-soldering applications where components must be attached sequentially at different temperatures. Recent developments in flux chemistry and reflow profiling have demonstrated that properly optimized Sn-Bi-Ag processes can achieve reliability comparable to SAC for certain product categories, particularly those with operating temperatures below 80°C[68].

9.8.3 Sn100C

Sn100C, based on tin (99.3%) also contains 0.7% copper, 0.05% nickel and 0.009% percent germanium Has gained a lot of popularity recently due to its very low cost and good properties. The inclusion of nickel reduces the copper erosion and produces a bright shiny solder while the effect of germanium reduces dross (crusty oxide residue) formation and promotes solder flow[69]. Since Sn100C solidifies

nearly isothermally there are no shrinkage cavities and the surface is smooth and bright which facilitates visual inspection.
In contrast to SAC, Sn100C has a high ductility factor, can accommodate substantial strain, without embrittlement and cracking and has a slower growth of interfacial Inter-Metallic Compound (IMC) during aging. Sn100C showed less erosion of copper slower than SAC.

	Sn63-Pb37	SAC305	Sn100C	Sn42Bi57Ag1	Sn42Bi58	Au80Sn20
TEMPERATURE (°C)	183	217	227	139	138	280
ELECTRICAL RESISTIVITY ($\mu\Omega$·m)	0.145	0.132	0.126	0.345	0.383	0.164
THERMAL CONDUCTIVITY (W/m·K)	50	58	66	35	19	57
COST (€/100g)	15	40	30	70	46	1300

Table 9.2: Comparison of solder paste properties. Good, Decent, Poor. The prices are based on the solder paste version and are a mean value between prices for differente packaging sizes.

9.8.4 Other Tin-based Alloys

Some other examples of Sn based LFS developed and their melting point are listed in the table 9.3 below.

Alloy Composition	**Melting Point** [°C]	**Key Characteristics**
Sn-37Pb (reference)	183	Eutectic, excellent wetting
Sn-3.5Ag	221	Good strength, high cost
Sn-0.7Cu	227	Low cost, high melting point
Sn-3.0Ag-0.5Cu (SAC305)	217-220	Industry standard
Sn-58Bi	139	Low temperature, brittle
Sn-35Bi-1Ag	187	Moderate temperature
Sn-Bi-Cu	190-200	Variable properties
Sn-Bi-In	143	Low temperature, expensive
Sn-9Zn	198	Oxidation issues
Sn-5Sb	232-240	High temperature
Sn-0.5Au	217	Expensive, niche applications

Table 9.3: Tin-based solder alloys and their eutectic melting temperatures[64, 70]

While some alloys offer lower melting points (e.g., Sn-Bi systems), their overall properties as solders are not yet up to par with SAC which remains the preferred choice for most applications, though some alternative formulations may become interesting alternatives in the future.

9.9 Solder Paste Printing

Solder paste printing is the critical first step in the SMT assembly process, as the quality of printing directly affects the rate of SMT soldering defects. Research indicates that between 60 to 70% of soldering defects are related to printing quality issues[71][43].
A correctly performing printing process aim at depositing the designed amount of paste precisely on the PCB pads where even slight misalignments can result in poor resulting joints and a non consistent deposition may cause weaknesses and open circuits if insufficient or bridging and short circuiting if excessive.
Solder Pastes are thixotropic meaning materials whose viscosity drops when a force is applied. This makes solder pasted able to be easily dispensed in various methods while regaining the tackiness necessary to keep the devices in position after being places avoiding misalignments[72].

9.10 Solder Paste Dispensing Techniques

Modern electronics manufacturing employs several techniques for solder paste application, each with distinct advantages and applications:

9.10.1 Screen Printing

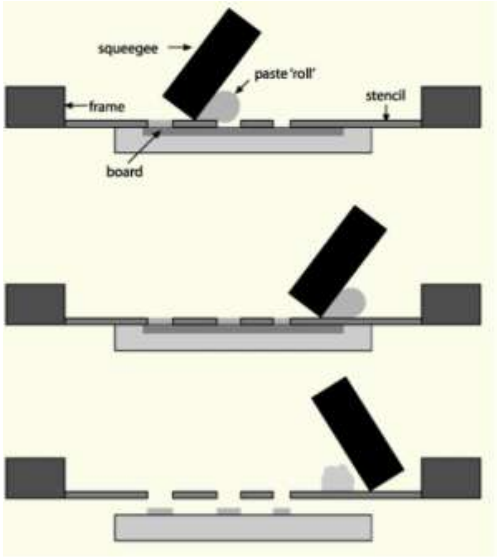


Figure 9.11: Screen printing schematic from I-Connect007[73]

Screen printing is the most traditional and widely used method that employs a stencil with patterned openings to transfer solder paste onto a PCB. This technique offers excellent throughput for industrial high-volume production however it has limitation in what the minimum pitch can be creating problems for the more miniaturized applications[74]. Most industrial processes require stencil with high precision apertures which can influence the total cost of a production when needing a constant replacements due to them wearing out over time.

9.10.2 Direct Ink Writing (DIW)

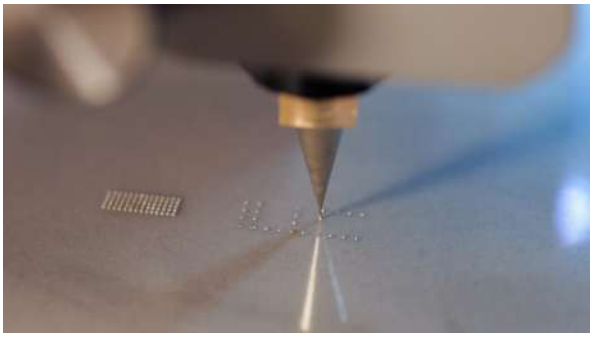


Figure 9.12: DIW NOVA dispensing system from Voltera[75]

Direct Ink Writing is done by dispensing solder paste throug a fine nozzle directly onto the PCB similarly to how a pencil works. In this way a great amount of precision is obtained ideal for application requiring high precision and minimizing waste[74]. However its throughput fall shorts other methods making it not yet suited for high volume industrial productions.

9.10.3 Jet Dispensing

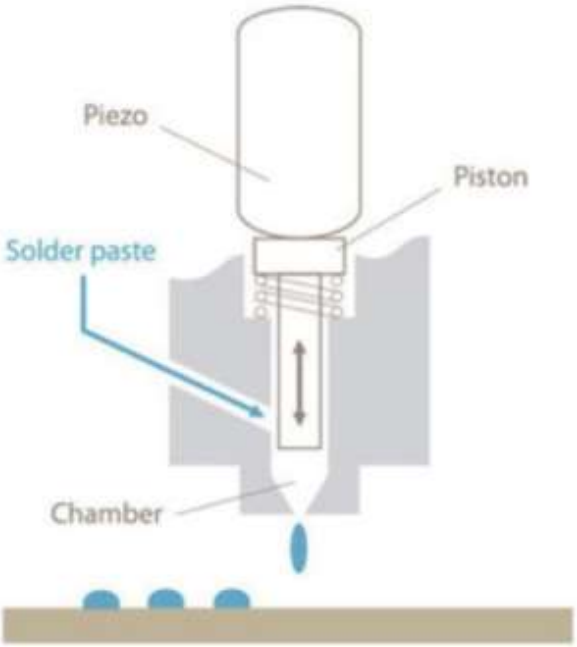


Figure 9.13: Jet printing schematic from I-Connect007[73]

Jet dispensing is more advanced technique that uses a nozzle to eject droplets of paste onto the PCB at high speeds without requiring a stencil. The jet dispensing offers the ability to apply solder paste to fine pitches and densely packed sections at the cost of an increase cost of equipment and maintenance[74].

9.11 Stencil Design and Optimization

In order to properly transfer the desired amount of paste onto the substrates is required a stencil which is a thin sheet of material where have been cut out some openings that match the areas of the pad in the case of a PCB.
Having a properly design stencil is paramount to reduce the amount of defect.
The key parameter of a good stencil is the aspect ratio, the ratio between the stencil thickness and the aperture width, that under the IPC-7525 stander has to be greater than 1.5 in order to ensure that the solder paste can correctly pass through the openings.
The stencil thicknesses usually range between 0.1 mm and 0.2 mm [76] depending on application and paste used (finer pastes can be correctly deposited with smaller aspect ratios) however if the stencill is too thick for the aperture the surface tension forming between the stencil's walls and the paste can cause it to not be deposited onto the substrate.
Usually the apertures are 1:1 to the pads (or slightly smaller) however in order to have a better deposition it is possible to implement special features into the stencil such as the "squircle" aperture which is a square qith rounded corners that improves the paste release and reduces the problematic effects that may rise from sharp corners such as paste retention, or stepped stencils that can accommodate for different paste thickness requirements.

9.11.1 Speed and Pressure

Other import parameter for the solder paste printing are the speed and pressure applied by the squeegee which influence the thixotropic behaviour of the paste and can be detrimental to the paste deposition if not following the recommended values given by the manufacturer for their specific formulation. an average speed for fine pitch applications is usually between 50–100 mm/s while pressures can hover between 20-100N[77].
The pressure should be the lowest possible because after repeated steps it coulc cause abrasion in the stencil.

9.12 Solder Paste Inspection

The Optical inspection step in an industrial die attach process is seemingly not related to electronic or nano-technological properties of devices, substrates or solder pastes but nonetheless holds great importance for the throughput of the production. In fact the ability to discern if the quantity, volume, position, area and shape of the deposited solder paste are satisfying the requirements is critical in understanding if something is not working properly and in reducing product failures which could be costly to fix (especially after the assembly process is complete) or require to scrap the board completely since it is estimated that between 60-80%[71] of defects are linked to the printing process.
Since so many defect can be traced back to the paste deposition, having a way of detecting these errors as early as possible is becoming and industry standard to improve yield and reducing the cost of post-reflow reworks which greatly out-cost a rework done before assembly and can sometimes result in the scrapping of the entire board.
Initially the OI was performed by technicians who would have to check one by one the solder paste application while nowadays Modern software tools are used which greatly increase the speed, number and precision of the inspection by capturing a profile then automatically optimizing it by using mathematical simulations.
Standard 2D system can still be functional for relatively simpler application with large pads and components where small deviations of solder volume are not impactful. However with the shrinking down of components the influence that changes in solder thickness bring may be of the same order of

magnitude of its other dimensions which can be detrimental for the correct functioning of the device by causing warpage of keeping sone pins from soldering in the case of Ball Grid Array (BGA).
For these fine pitch applications are necessary 3D inspection systems able to scan for the smaller volume inconsistencies.
The most important parameters of an Optical Inspection are the accuracy of the measurement, the speed at which the measurement are done to not influence negatively the production and the ability to analyse different types of substrate and PCB with different shapes color and eventual warpages[71].
Performing an accurate Optical Inspection other than preventing failures like bridges between neighboring pad and mis-alignments from passing through can also help to improve the overall printing process. In fact by measuring the solder paste volume and area modern systems are able to detect if the stencil is starting to clog before paste retention defects begin to form this can also lead to an improvement of stencil washing policies reducing its cleaning only to when necessary before printing related errors begin to show. Similarly modern system and softwares are able to detect and predict if there are problems with the squeegee speed or pressure and if the paste is showing signs of ageing allowing for the users to quickly act before critical errors arise.
Advanced systems correlate pre-reflow paste measurements with post-reflow joint quality, establishing transfer functions that predict final assembly yields. This enables optimization of paste volume specifications for specific component types and board designs[71].

9.12.1 Industry Standards and Best Practices

9.12.2 IPC Standards Compliance

SPI implementation should align with established industry standards:

- **IPC-7527**: Requirements for solder paste printing
- **IPC-9850**: Surface mount placement equipment characterization
- **J-STD-001**: Requirements for soldered electrical assemblies

9.13 Reflow Oven

9.13.1 Oven types

The selection of reflow oven technology significantly impacts the soldering process quality and manufacturing capabilities. the three primary types of ovens are:

Convection Reflow Ovens

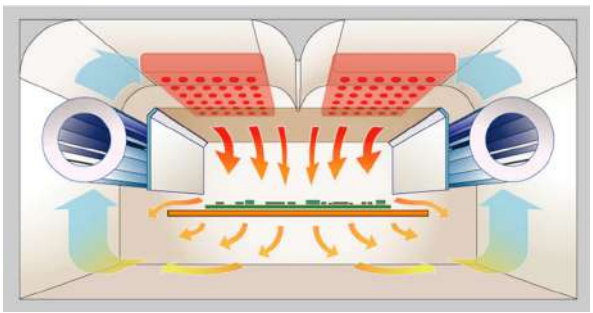


Figure 9.14: Convection oven's chamber schematic[78]

Convection technology represents the industry standard for SMT reflow soldering, utilizing forced air circulation to achieve uniform heat distribution across the PCB assembly ensuring consistent heating of all board areas thus preventing cold spots where solder paste might fail to reach melting temperature. To achieve uniform heating characteristic, however, it is necessary precise thermal control since all PCB components experience similar thermal exposure, it can potentially risk damaging temperature-sensitive parts. Modern convection ovens typically achieve temperature uniformity within ±2-5°C across the board surface [79].

Infrared (IR) Reflow Ovens

Infrared reflow systems employ radiant heating through IR emitters, enabling a more targeted thermal energy application. This selective heating capability significantly reduces thermal stress on sensitive components by allowing differential heating zones. However, IR technology presents challenges including potential shadowing effects from tall components and critical requirements for precise board alignment. Temperature variations can occur due to differences in component colour and thermal mass, as darker surfaces absorb more IR energy than lighter ones. These limitations make IR systems less suitable for complex assemblies with varied component heights and thermal masses.

Vapour Phase Soldering (VPS)

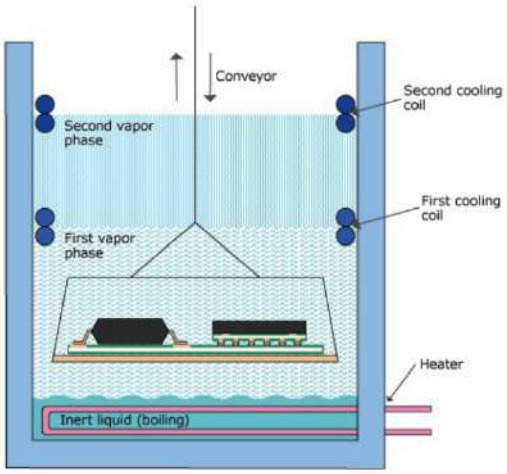


Figure 9.15: Vapor Phase oven's chamber schematic[80]

Also known as condensation soldering, utilizes the latent heat of vaporization from specialized fluids with precisely knows and engineered boiling points. This method inherently prevents overheating since the maximum temperature cannot exceed the fluid's boiling point, typically set 20-40°C above the solder melting temperature. VPS eliminates both the risk of thermal damage and the possibility of incomplete solder melting. However, implementation requires expensive specialized equipment (up to $100,000 vs $15,000 for convection) and careful handling of fluorocarbon compounds due to environmental considerations. The process also demands proper ventilation systems and recovery mechanisms for the working fluids[81].

9.13.2 Reflow Profile Design

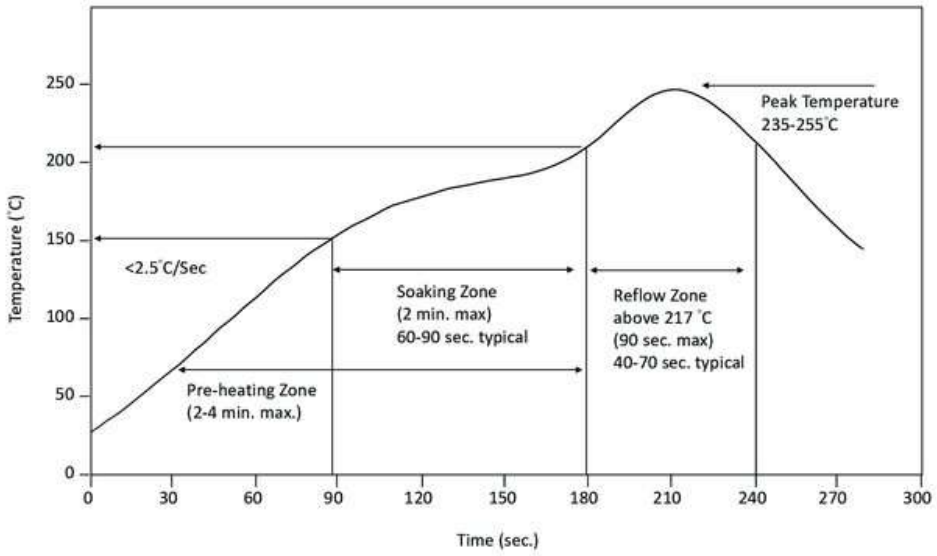


Figure 9.16: typical reflow profile for solder pastes[82].

The reflow profile usually consists of four distinct zones, depicted in figure9.16 and their optimization requires balancing multiple factors including the solder paste specifications, the PCB complexity, and the components thermal sensitivity.

Preheat Zone

The pre-heat zone objective is to raise the PCB and components' temperature from the initial room temperature to the soaking temperature. To this zone correspond the beginning of flux activation and the evaporation of volatile compounds from the solder paste[83].

Soak Zone

The soak zone goal is to gradually increase the temperature of all the elements in order to ensure an uniform temperature without gradients between PCB, paste and mounted devices while allowing for the complete flux activation and removal of remaining solvents from the paste.
This zone is usually the lengthier phase both in time (60-120 seconds) and in actual dimension in conveyor belt ovens.

Reflow Zone

The reflow zone, also called spike zone, rapidly increases the temperature inside the oven in order to reach above the liquidus point of the solder paste then usually this temperature is maintained, the so called dwell zone, in order to ensure the complete melting of the paste. For a proper optimization the peak temperature must be sufficient to ensure the full paste volume reaches the melting point while at the same time minimizing component exposure to the higher temperature may cause thermal damages. Moreover an extended Time Above Liquidus (TAL) promotes better wetting while on the other hand increasing inter-metallic layer thickness and component stress which may causes brittleness in the solder.[79].

Cooling Zone

A controlled cooling solidifies solder joints establishing the final microstructure, a rapid cooling within acceptable limits, usually around 3°C/s prevents excessive grain growth and produces a finer microstructure which has better mechanical properties.
The solder finish should exhibit a shiny appearance while a duller finishes indicate crystallization from slow cooling.
Lead-free solders require particular attention to cooling rates due to a larger temperature differential from liquidus to ambient (217°C to 25°C = 192°C for SAC305) compared to tin-lead systems (183°C to 25°C = 158°C)[71].
Moreover a proper cooling also inhibits excess intermetallic formation and thermal shock to the components.
While sometimes the cooling rate is considered almost a negligible aspect of the process in industrial processes it cannot be neglected to maximise the yield and it is usually performed by means of fans and forced air.

9.13.3 Profile Types and Evolution

Ramp-to-Spike (RTS) Profile

The modern convection ovens typically employ the ramp-to-spike profile, featuring a linear temperature increase from ambient to peak with reduced soak time minimizing the total thermal exposure while still providing an adequate flux activation and heating uniformity.

Ramp-to-Dwell-Ramp-to-Peak (RDRP) Profile

The RDRP profile was originally developed for infrared reflow ovens to compensate for uneven heating. The extended soak is aimed to ensuring uniform temperature distribution before the final ramp to peak[84]. However, this profile can cause issues with modern miniaturized components such as increased oxidation, excessive oxidation growth and exhaustion of the flux before the reflow temperature is reached.
The modern convection systems with superior thermal uniformity have largely eliminated the need for extended dwell times[48].

9.13.4 Profile Optimization

When deciding on the reflow profile other than the solder paste temperature requirement it is essential to verify the thermal tolerances of all the element involved. A temperature too high and devices may be damaged, PCBs too thick may act as thermal sinks reducing the actual temperature reached by the paste and mismatch in the CTE of elements may induce stresses detrimental to the final performances or cracking.
The use of sophisticated thermal monitoring system can help identify errors ensuring a more consistent quality of the process.

9.13.5 Conclusions

A fault that is identified only after reflow costs 10 times more to rework than one identified before, this emphasizes the critical importance of proper profile development and process control balancing multiple variables to obtain a successful reflow soldering. The transition to lead-free soldering has narrowed the process windows and increased the thermal demands on both equipment and components. The future developments in low-temperature solders and advanced heating technologies promise to

address current limitations while enabling the assembly of increasingly complex and thermally sensitive devices.

Experimental Part

10.1 Materials and Methods

The objective of this experimental study is to find suitable parameters for a die attach soldering reflow process suitable for SiP, high power application and onto ceramic substrates that can subsequently laser cut without harming the solder.
This goal was achieved in different steps: firstly by matching the temperatures inside the reflow oven with the suggested reflow profiles in the TDS of two solder pastes (SAC305 and Sn42Bi57Ag1) then using some expressly crafted DBC-like substrate onto which carry out the soldering process until suitable results are obtained. The results are then characterized to verify their successful outcome.

10.1.1 Substrate Preparation

For the creation of the DBC-like substrates were used some $50.8mm \times 50.8mm \times 0.63mm$ alumina substrates from Alutron to act as the ceramic element of a DBC and 25mm x 0.07mm adhesive kapton[85] to be used as protective mask for the copper deposition. For later trials instead of the DBC-like substrate were used Rogers Curamik (0.3 copper - 0.63 alumina - 0.3 copper) DBCs[86] with the copper pattern in picture10.1.

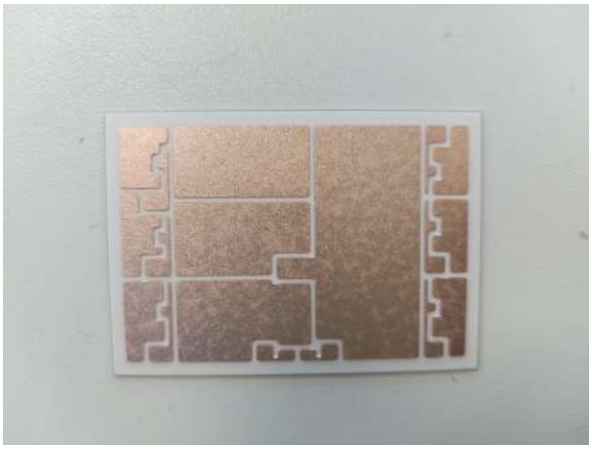


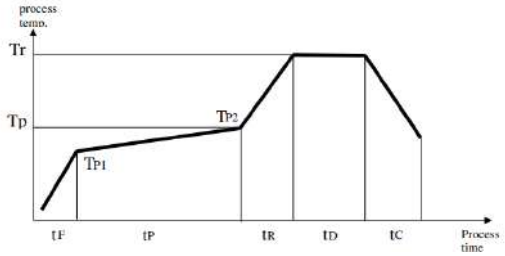
Figure 10.1: Rogers Curamik DBC.

10.1.2 Reflow Oven and profile characterization

To perform the soldering was used a Mechatronika MR10A IR reflow oven with four processing sections namely initial preheating, preheating, soldering and dwell areas, in the manual mode the parameters it allows the user to set are 5 time periods (t_f, t_p, t_r, t_c) and 2 temperatures of the IR sources (T_P max. 250°C and T_R max. 430°C) as we can see in picture10.2b while in the auto-profile mode it allows the user using the control panel10.2a to set just the 2 temperatures of the heating elements and additional 4 temperatures $(t_{p1}, t_{p2}, t_r$ and $t_c)$ that once measured by a thermocouple connected to the oven itself (it came with it) will make the oven go to the subsequent reflow profile section and

at the end the times needed to reach those temperature will be displayed with the possibility to be automatically saved.
For the characterization of the flow profiles and the temperatures reached inside the oven were used both the oven own auto-profiling mode and a set up made by a Emko Elektronik Pt1000 thermo-resistor[87] connected to a Mitek MK1320 multimeter.

(a) MR10A control panel.



(b) MR10 settable reflow profile

10.1.3 Solder pastes and deposition process

During this thesis where used 2 different solder pastes: a SMD291SN SAC305 which is still considered the golden standard and most reliable among the LFS, the formulation used is a t3 with synthetic no-clean flux[88] with a melting temperature of 217-220°C and as a low temperature counterpart a 4902P T3 Sn42Bi57Ag1 with a rosin M1 flux and a melting point temperature of 138°C[89] stands as one of the better alternatives for heat sensitive components.
For the deposition of the pastes were used the syringes they came into and a plastic squeegee to push the paste through the apertures of one of three metallic stencils.
The dies used during the attach process came from a silicon wafer with a aluminium metallization on the back and silver on the topside as per an EDX analysis were not functioning and were used only to simulate the presence of real components.

10.1.4 Shear Test set-up

In order to quantitatively and qualitatively measure the adhesion strength of the solder it was created and used the set up in image10.3 where a load cell is mounted onto a rod suspended vertically by the metallic structure, the load is connected to a circuit board that, thanks to a standard software, is able to measure and save into a .csv file the forces at which the load cell is subjected. The measure force is in mV and has to be converted in Newtons by using the formula:

$$y = 1,924x + 3,306 \tag{10.1}$$

where x is the value in mV and y is the result in Newtons and then converted into MPa by dividing the force by the contact area between the die and the solder paste in mm (the average die I used was $5mm \times 5mm \times 0.25mm$ therefore divide by $25mm^2$). Since with these setup the force is applied vertically I created a support with additive technology to keep the substrate in place as seen in figure10.4a, the central disc is able to rotate in order to accommodate for non-perfect alignment of the die with respect to the alumina sides and is then set in position by up to two screws on each side. This 3D printed support was then secured onto an aluminium metal profile by 2 screws allowing for x-axis alignment while the y-axis alignment was done by moving the metal profile by unscrewing the lateral 3D printed support. The last element of the set up is depicted in figure10.4bwhich is the 3D

printed point with a die-shaped notch for the rod to allow for better grip onto the component. This component was later substituted by an Aluminium component of similar geometry.

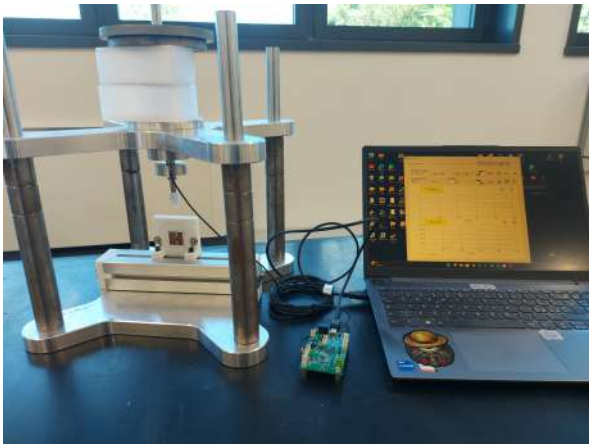
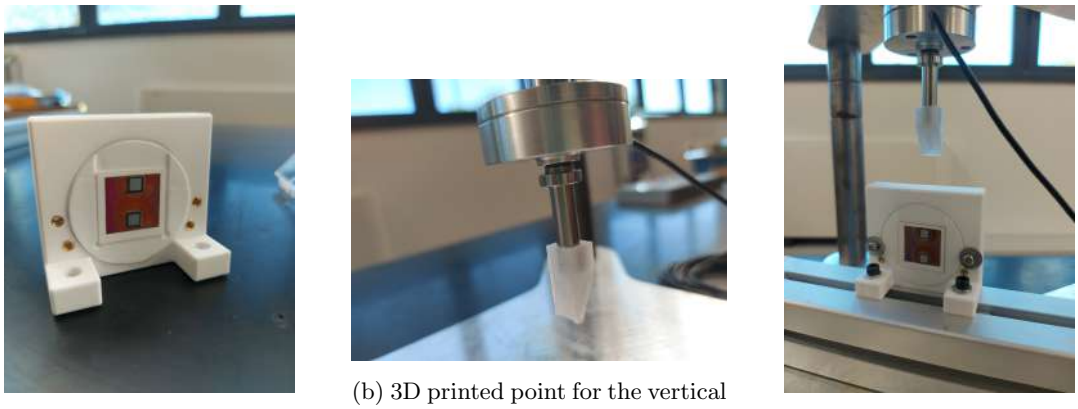


Figure 10.3: Complete setup for Shear Testing the soldered dies.



(a) Vertical support.

(b) 3D printed point for the vertical rod.

(c) Zoom on the set up.

Figure 10.4: Shear test set-up components

This set-up allows for the positioning of weights in the upper part, however for my measurements the force is manually applied through the steel bar and it is gradually increased until failure occurs. The load cell however allows for precise record of the applied force ramps.

10.2 Experiment preparation

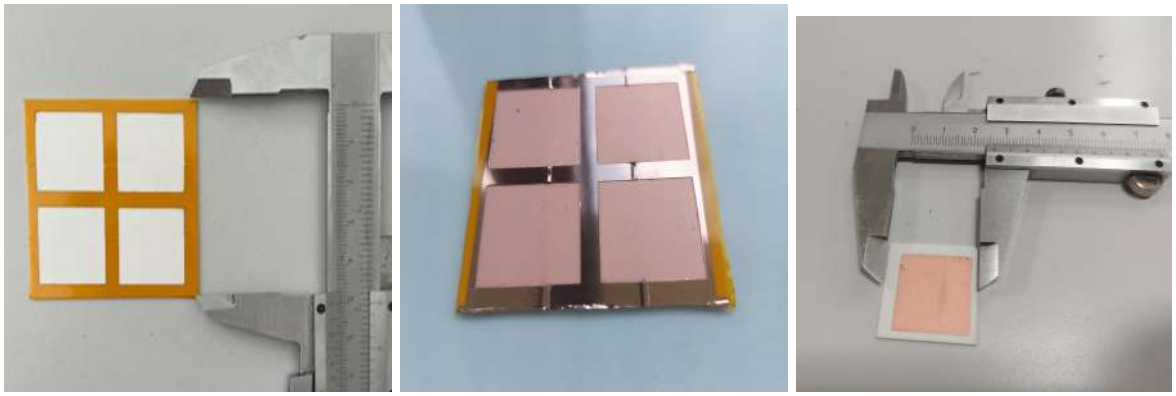
10.2.1 Die-Attach Equipment

With the objecting of crafting a cheaper alternative to a DBC onto which starting to perform the first trials of reflow soldering in order to obtain the conductive layer the initial step was to create a deposition mask, this was obtained by using the adhesive kapton tape, in favour of the non-adhesive one which would have create some shadowing effect The application of the kapton was done by carefully overlapping the tape strips in order to not allow for exposed sections of alumina. Once the kapton fully covered the alumina it was used a CO2 laser scriber Mic-LS0002 to cut into it the layers and strip them manually with the help of tweezers, to create 4 square apertures as seen in picture10.5a.

Multiple of these masked substrate were sent to PiQuET laboratories where, by means of Physical Vapor Deposition (PVD) where deposited a layer of namely 100nm of Titanium and a layer of namely 1μm, the result is shown in picture10.5b and, once the remaining kapton was carefully removed in such a way not to peel the copper, the effective thickness of these layers have been measured with a KLA Tencor P17 profilometer.
Lastly, from each 5x5 alumina sheet, four single 2.5x2.5 substrates can be obtained. The singulation process is achieved through the use of a SPI 1064nm 50watt nanosecond near-Infra-Red pulsed laser (parameters in table10.1) to cut along the central cross of exposed alumina until the result in figure10.5c is obtained.

Current	Frequency	Pulse Width	Mark Times	Mark Speed
90 A	55 kHz	2 μs	500	1400 mm/s

Table 10.1: SPI 1064nm 50watt nanosecond near-Infra-Red pulsed laser parameters for lase cutting the alumina substrate.



(a) Kapton masked Alumina substrate (b) Substrate after deposition of Titanium and Copper. (c) Laser cut "single" DBC-like substrate.

Figure 10.5: DBC-like substrate process steps.

To perform a die-attach process is essential to have the dies therefore, starting from the full wafer, I used a Datalogic green 532nm 10watt nanosecond laser to cut multiple $5mm \times 5mm$ dies (laser parameters in table10.2) to be soldered onto the substrates.

Power	Frequency	Emission Time	Mark Times	Mark Speed
90%	20 kHz	2 μs	10	20 mm/s

Table 10.2: SPI 1064nm 50watt nanosecond near-Infra-Red pulsed laser parameters for lase cutting the alumina substrate.

Finally to complete the equipment need to perform the die attach process I created the three metallic stencils in picture10.6 in brass and steel, with different sized apertures and different thickness (150μm, 100μm and 50μm) to analyse the solder behaviour for different volumes of paste, however during the analysis (other than some tries with only the paste and no die) only the smaller apertures $5mm \times 5mm$ (1-to-1 with the dies) were used.
To correctly deposit the solder paste I created a simple set up using tape and some alumina substrates

to keep the simil-DBC in place and similarly used tape to keep the stencil in contact and aligned.
After squeezing some solder paste onto the stencil I used the squeegee back and forth until an uniform layer inside the aperture was achieved.
Pick and place of the components on the deposited solder paste is performed manually using small tweezers. Since the component is squared and the solder paste tends to self-align, other aligning tools are not needed during this step.

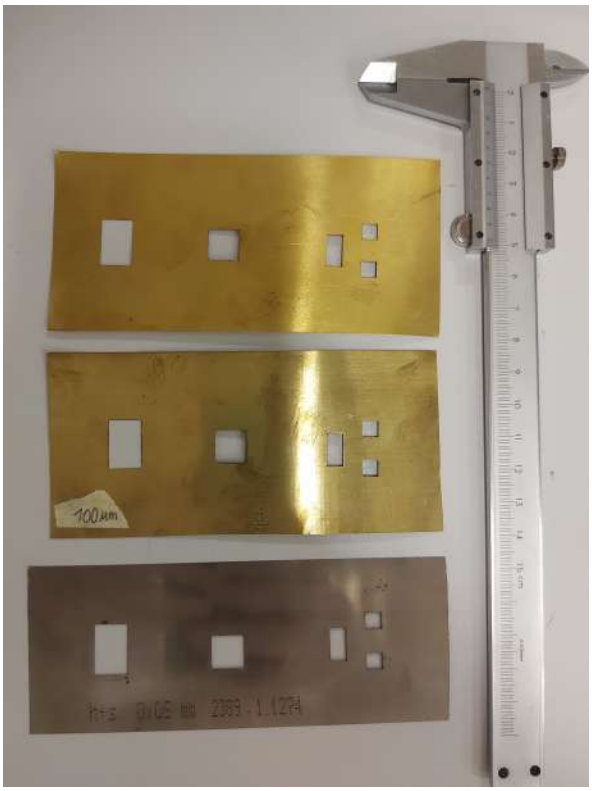


Figure 10.6: Metallic stencils, from top to bottom: brass 150μm, brass 100μm and steel 50μm.

10.2.2 Reflow profile Characterization

In order to test the accuracy and precision of the oven, a complete characterisation is performed. This is a precise requirement to achieve reliable and stable solutions independently from the substrates or the components. In fact, as can be understood by looking at the suggested parameters for the reflow profile of a LFS paste in figure10.7a where the reflow temperature T_r is 430°C the actual temperature inside the oven is vastly different from the one set in the control panel which should only refer to the temperature of the actual IR source of the oven otherwise we would observe charring instead of soldering.
Therefore, in order to gauge the temperatures reached, was used the already mentioned in the "Reflow Oven and profile characterization" section set-up consisting of a thermo-resistor connected to a multimeter that can be observed in picture10.7b to measure the temperature reached by the components inside the oven.

Lead free solder paste

temperature	time
T_P=190°C	t_F=0s t_P=150 - 180s
T_R=430°C	t_R=30s t_D=20s t_C=30s

(a) Suggested reflow parameters for Lead-Free Solder for the MR10 infrared reflow oven

(b) MR10A oven and Thermoresistor/multimeter setup for temperature measurments.

As per initial test, the lead-free solder parameters from the MR10A manual10.7a were set into the oven. The sensor was positioned in the oven tray and then connected to the multimeter, whose screen was recorded for the whole duration of the reflow profile, approximately between 300 and 600s. The recording was sampled with a sampling frequency of $f_{sampling} = 1Hz$ using an online software[90] and post-processed in order to extract the temperatures using the Pt1000 conversion chart[91] linearized in a Matlab[92] script (all matlab scripts and data files are in the github repository https://github.com/PPiqwert/Thesis.git). The converted values were used to reconstruct the curves of temperature measured inside the oven and iteratively compared them to a schematized version (datasheet curve in figures11.5b,11.5c,11.9b,11.9c,11.9d) of the one suggested by the Technical Data Sheet of the two pastes following the MR10A reflow profile scheme10.2b where the reflow curve is divided into preheat, soak, ramp-up, dweel and cooling.
This process was repeated several times changing the MR10A reflow parameters until the behaviour of the curves measured by the pt1000 closely matched the one of the TDS by reaching a $\pm 5C$ of the values stated as recommended for soak temperatures and reflow temperature denoted as T_{p1},T_{p2} and T_R.
Only at this point I started to make the die-attach trials using the DBC-like substrates and dies: for each one of the substrates i deposited two $5mm \times 5mm$ squares of solder paste and placed a die only in one of them in order to have a non destructive way to see how the soldering was occurring below the die by looking at the "bare solder" without one.
Based on the visual analysis checking the presence of defects in the soldering quality of each try the reflow parameters were varied in order to minimize the defects.
For example if an incomplete flux evaporation is noticed causing defects such as graping, solder balling or solder splashes the soak and dwell times were increased properly remove the flux, if there was incomplete melting the temperature was increased while cracking meant that the temperature or dwell times has to be reduced, these reasonings were done for each die attach trial until the resulting soldering yielded a satisfying result free of defects. The parameters found were used to perform the soldering onto the real DBC, cut using the already mentioned SPI 1064nm 50watt nanosecond near-Infra-Red pulsed laser in order to have multiple smaller DBCs at my disposal. The results obtained, both on the real ad simil-DBC, were analysed both visually and by means of a shear test to measure their adhesive strength..

10.2.3 Visual analysis

The visual analysis to better understand if and what defects were present, was done with an optical microscope (Olympus DSX1000) with different lenses (1x, 10x and 40x) and with SEM imaging (Thermo Scientific Phenom XL) from the front and in section (obtained by cutting the substrate, die and solder by means of a die cutting machine).

10.2.4 Shear Test

For the shear test the 3D manufactured components of the set-up where designed using Solidworks ver.2024 and created using a Bambu Lab 3D printer. The readings of the loading cell were read and saved into .csv file by a Microla OptoElectronic srl. owned software and were then analysed, converted and reconstructed into curves using a Matlab[92] script.

Results

11.1 Profilometer Characterization

In order to characterize the DBC-like substrates deposited layers was used a profilometer. However due to the difference between the vertical dimensions order of magnitude in the microns range and the y dimension of 22mm, for many of the measurements the instrument was not able to level the datas resulting in obtuse curves where even the exposed alumina section are not planar as for the two graphs in figure 11.1 and show layers too thick with respect to the nominal values of the deposition (100nm of Ti and 1μm of CU)

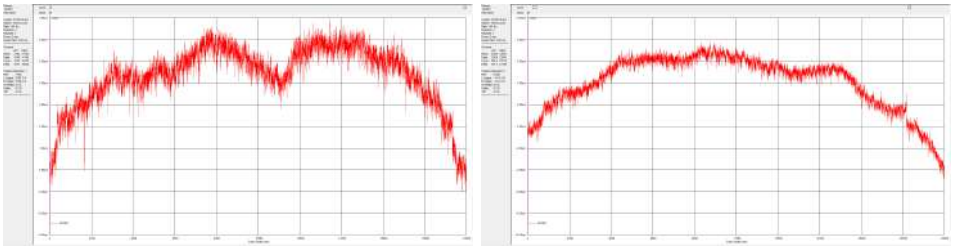


Figure 11.1: Erroneous profilometer readings.

More accurate readings can be seen in the figure11.2 below where heights of less than 2μm are measured more in line with the nominal values.

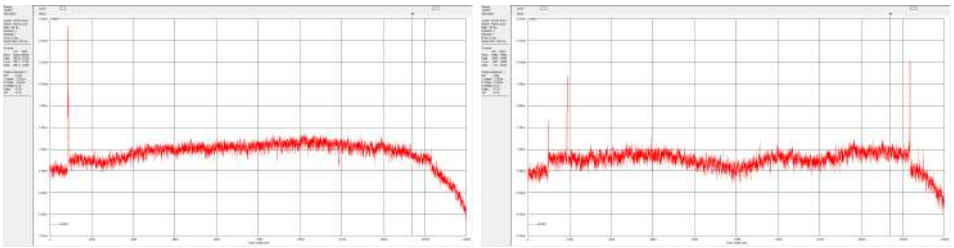


Figure 11.2: Correct profilometer readings.

None the less these curves dos not clearly show how planar is the result due to the already mentioned disparity in x and y dimension order of magnitude.
The conformity of the layer is better visualized in figure 11.3 where it was conducted the measurement of sample #7, in this case where the y dimension is of the order of hundred of microns it is visible how the copper layer appears planar.

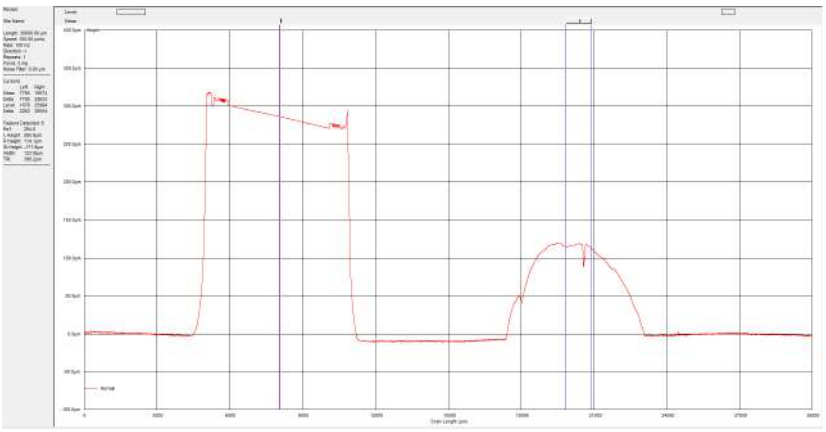


Figure 11.3: Measurement of sample #7 showing the attached die on the right and the bare solder slump on the right.

The profilometer measure was also done on the commercial DBC and, as shown in figure 11.4 the copper layer height correspond to the advertized 0.3mm, two orders of magnitude more than the crafted DBC-like which was enough to perform and analyse the soldering joint but not enough for the shear test as will be later discussed.

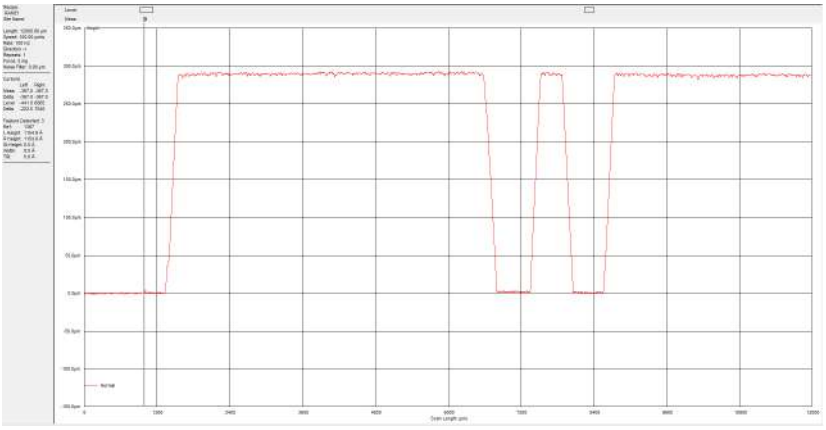


Figure 11.4: Commercial DBC profilometer measurements showing conformity to the nominal 0.3mm copper layer.

11.2 SAC305

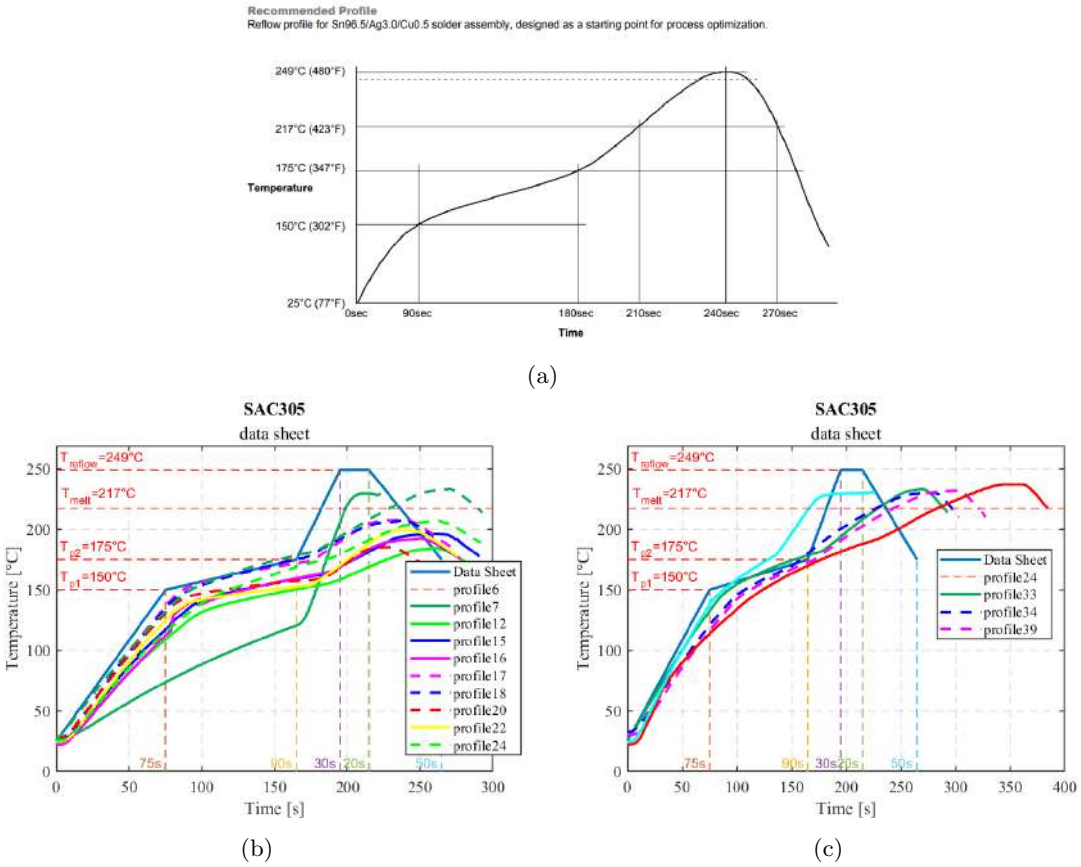


Figure 11.5: SAC305 flow profile from data Sheet 11.5a and reconstructed profile on Matlab with trials of matching 11.5b 11.5c.

For the SAC305 T3 paste the results obtained during the reflow profile showed an incorrect solder, based on the measurements done with the Pt100011.5 the reasoning explaining the unsuccessful results was that, as can be seen in figure11.5 where the Pt1000 curves are compared to the data sheet suggested values, the temperature reached inside the oven was not enough to completely melt the solder and reach the reflow Temperature of 249°C. Even setting the temperatures of the oven to the maximum possible and increasing the reflow times near the maximum available, almost doubling the time suggest yielded the results shown in figure 11.6. In both samples there is an evident residual presence of the flux which has not evaporated and turned brownish, in sample #9 instead of forming an uniform layer the paste contracted and agglomerated forming craters formations, in sample #10 the die drifted from its position while where there was only the solder paste was presents it formed a clustered structured and the solder appears to be mixed with the Ti and Cu layers having removed them from the alumina substrate.

(a) Sample#9. (b) Sample#10

Figure 11.6: Sample #9 (left) and sample #10 (right) showing an incorrect soldering

Other than an incompatibility with the deposited conductive substrate it was also investigated if the actual measurement done with the Pt1000 where not correctly mirroring the temperature reached by inside the oven due to a slower response to temperature gradient or a different thermal behaviour than the used substrates. To perform this analysis where used a PCB onto which where deposited small amount of solder paste and small components using a pick and place machine and for the reflow profile used the auto-profiling mode of the MR10A oven setting as temperatures $T_{p1} = 150C$, $T_{p2} = 175C$, T_R taken from the TDS. In this way once the thermocouple connected to the oven and fixed to the PCB reached those temperature the oven automatically goes to the next reflow zone, the resulting solders weren't shiny but rather dull in appearance but did not show any of the drift and flux residue problems of the previous samples as can be seen in figure11.7.

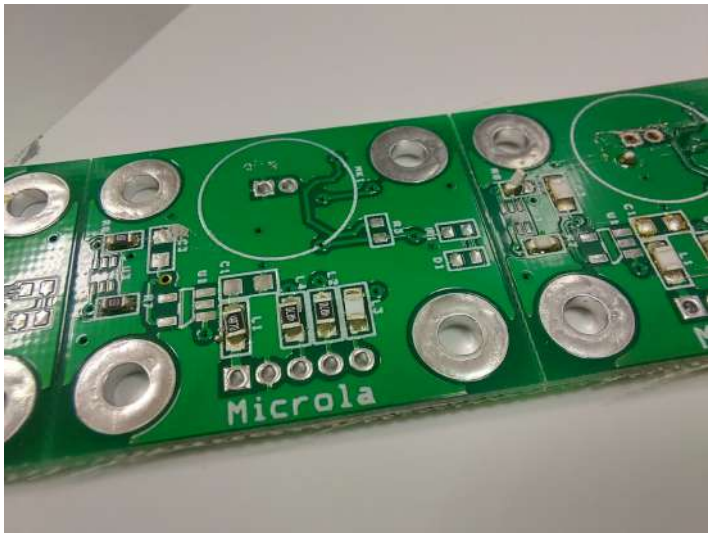


Figure 11.7: Soldering of small components on a PCB done using the auto-profiling of the oven. The joints are not shiny and somewhat dull however the components remained in position and the soldering seems complete with no residues.

The times found with the auto profiling mode are reported in the Appendix A table #43 and are considerably shorter (221s) then the ones previously considered such as #35 (375s) or #40 (335s) where samples #9 and#10 were obtained.

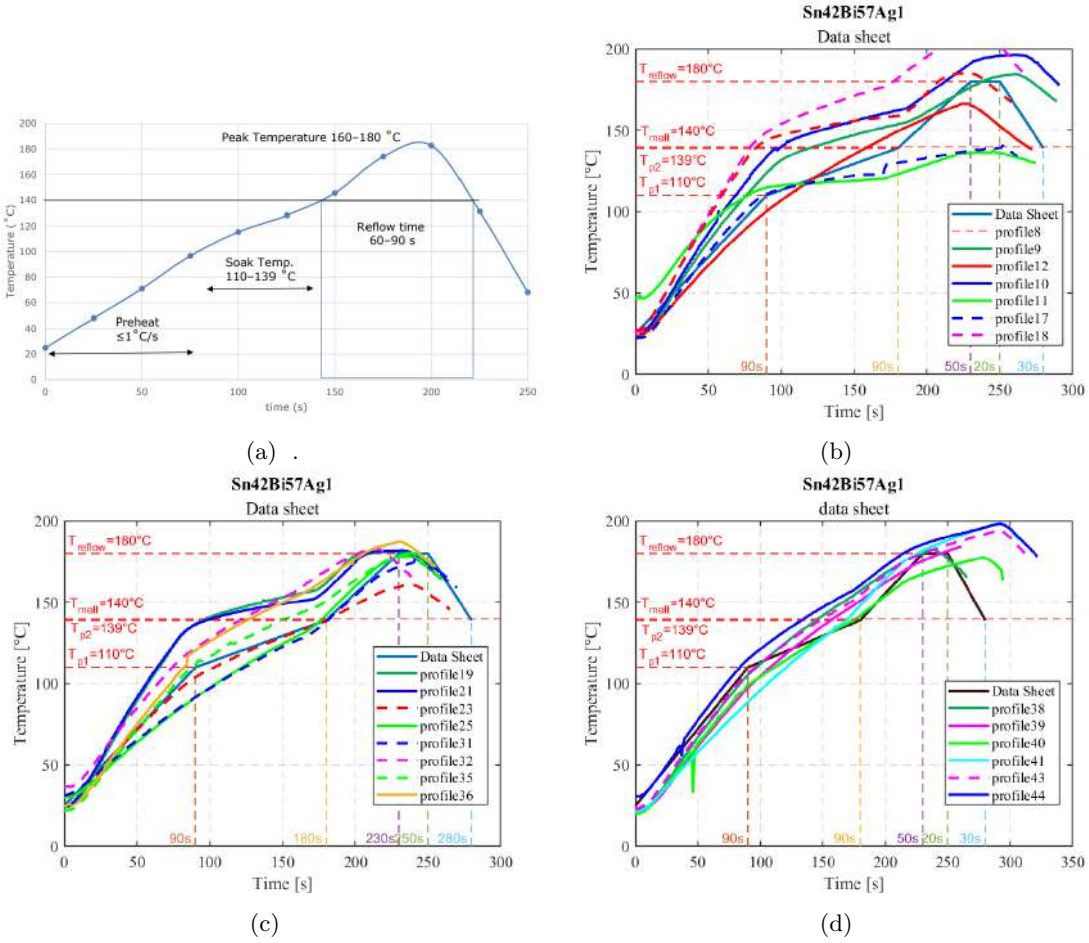
However, repeating the trial onto other DBC-like substrate using those parameters resulted in similar behaviours to samples #9 and#10 as seen in figure 11.8a showcasing similar die drift fro sample#20 performed on a recycled substrate after shear testing was previously done onto it, and for sample #21 in figure 11.8b where the reflow times where slightly increased to try and obtain better flux removal with no avail.

(a) Sample#20. (b) Sample#21.

Figure 11.8: Sample#20 and sample#21 obtained by using the auto-profiling-obtained reflow parameters.

Due to these unsuccessful results more trials with the SAC305 where put aside in favour of the Sn42Bi57Ag1 solder paste, the autoprofiling-mode was not used again and no-shear test has been performed for this solder paste. Future trials with different substrates and a better characterization system for the oven are required to understend if the the defective soldering was due to the oven, substrate compatibility or user errors in the paste use and reflow parameters setting.

11.3 Sn42Bi57Ag1



(a) . (b)

(c) (d)

Figure 11.9: Sn42Bi57Ag1 flow profile from data Sheet 11.9a and reconstructed profile on Matlab with trials of matching 11.9b 11.9c 11.9d.

Starting from the values from the TDS11.9a, which has to be considered as suggestion from where to start experimenting for the desired application, and initially using the values suggested in the oven manual10.7a were measured the temperatures reached inside the oven with the the Pt1000 and was done the very first try sample#1, shown in figure 11.10, where the flux has not been removed and even where the solder has a shinier appearance is clearly visible the graping effect. From just this result can be deducted that the reflow times need to at least be increased in order to try to completely remove the flux and have a complete solder all around.

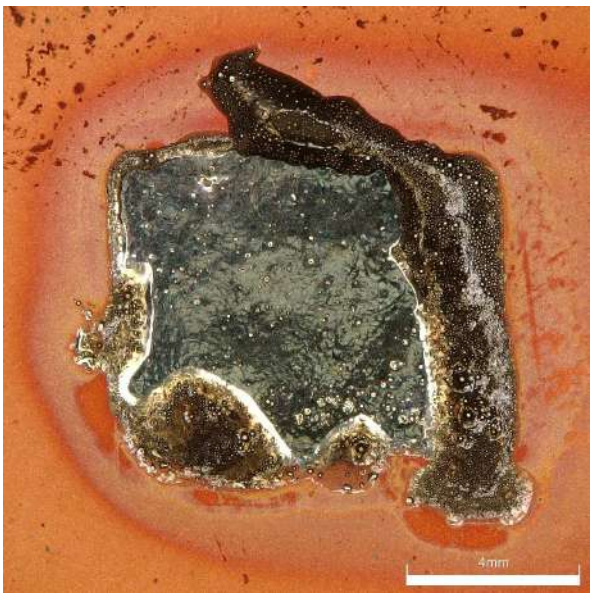


Figure 11.10: Sample #1 showing acceptable solder appearance toward the centre but also defects such as graping and heavy presence of flux residue.

On the other hand sample number #2 was done obtained using as temperatures $T_p = 150$ and $T_r = 240$ the ones from the SAC305 TDS just in order to test that the temperature set is only refered to the heating sources of the oven while the temperature reached inside is much lower. As can be seen in figure 11.11 even if the melting point temperature for the Sn42Bi57Ag1 is 139°C and the suggested reflow temperature is 160-180°C (60°C lower than the set T_R) the solder was not able to completely melt, the presence of flux is much more evident than sample #1 and where the flux was not evaporated there was the formation of spherical coalescences as zoomed in figure 11.12. This spherical formation is typical of insufficient flux activation[51].

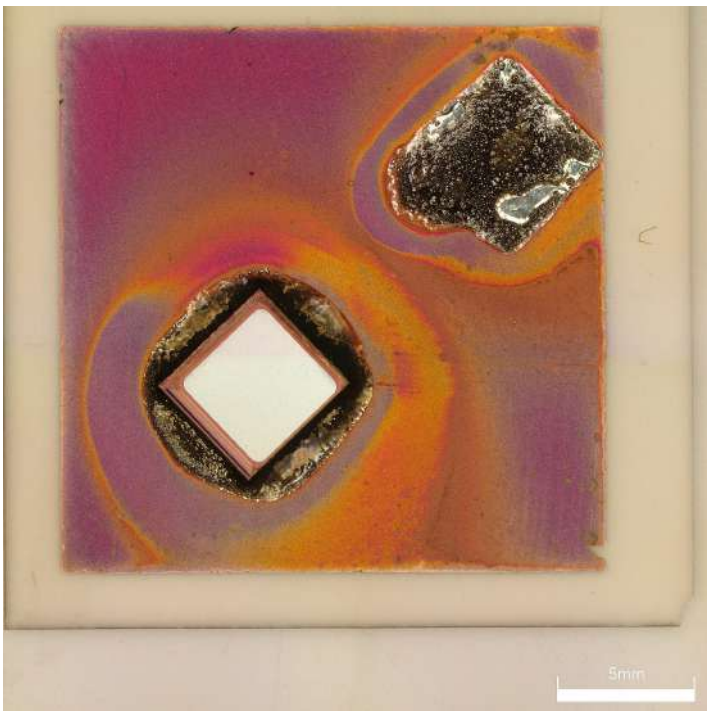


Figure 11.11: Sample#2 was done setting as temperature the exact values suggested in the SAC305TDS

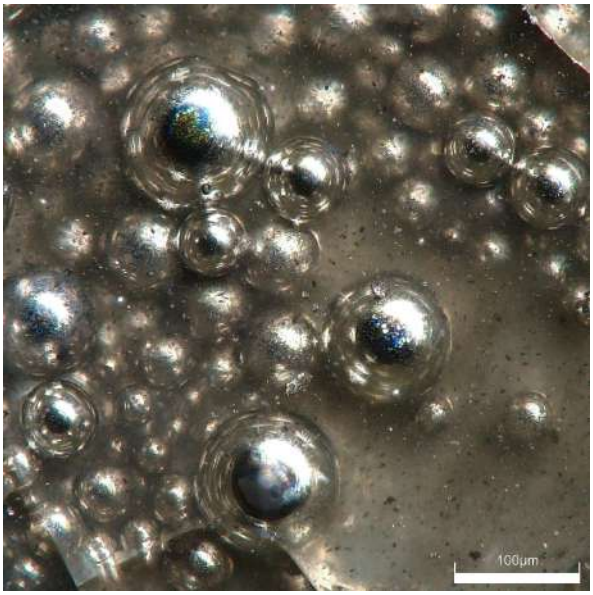
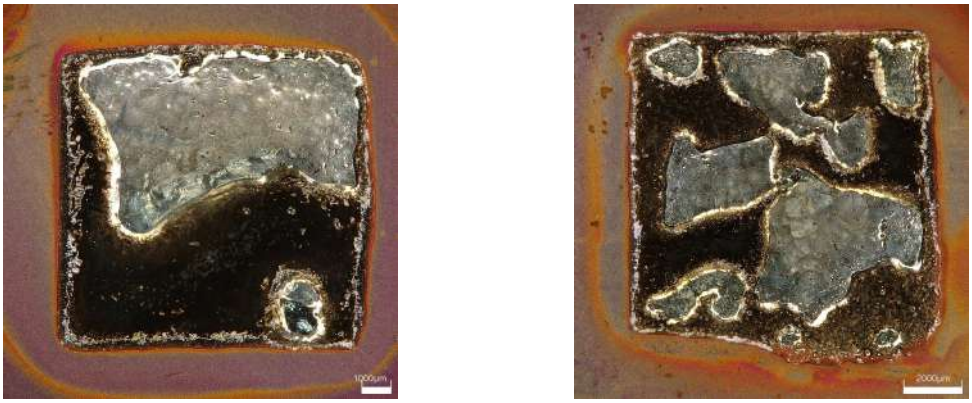


Figure 11.12: Sample#2 40x zoom on spherical coalescence where flux was not evaporated

After these 2 tries the objective became to find the parameters which actually resulted in reaching the required temperatures inside the oven measured with the Pt1000 thermoresistor.
only after iteratively measuring the curve temperatures and confronting them with the one in the Sn42Bi57Ag1 data sheet i was able to find parameter with on paper allowed for the suggested curve to be met. In the case of Sn42Bi57Ag1 this was achieved by increasing T_p to 250 (the maximum value

settable) and decreasing T_R to 365°C while adding the preheat zone that was not used for sample #1. However as can be seen in figure11.13 in both cases the flux was not removed.



(a) Sample#3. (b) Sample#4.

Figure 11.13: Sample#3 (left) and sample#4 (right) both showing incomplete flux activation.

In figure 11.14 is showed the interface between the shiny side where flux is removed with the are where flux is present. the are where flux is present show the formation of solder balls.

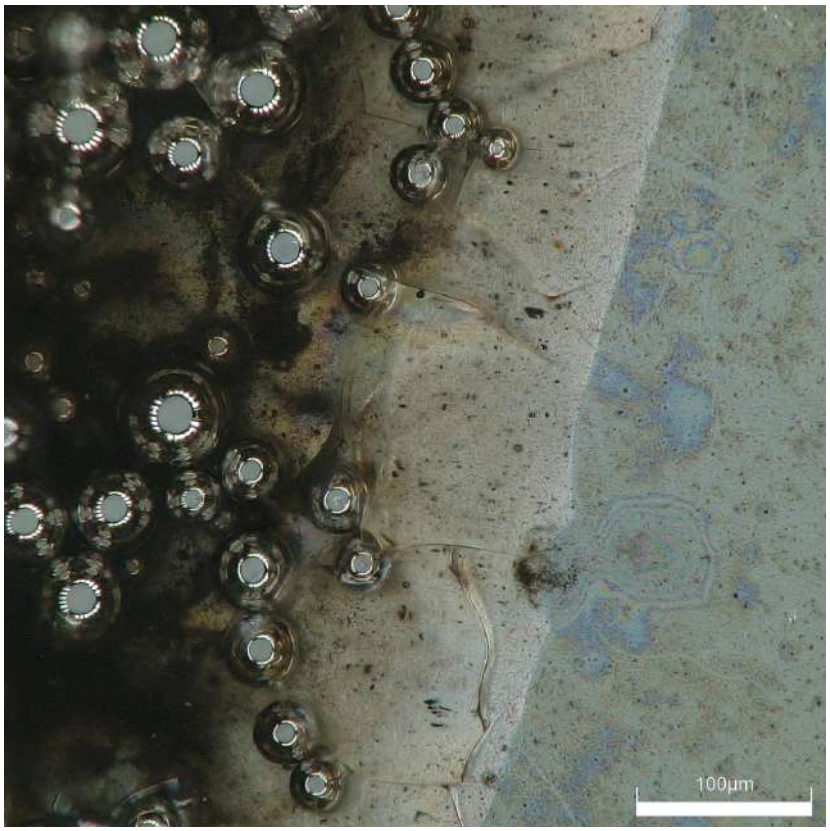
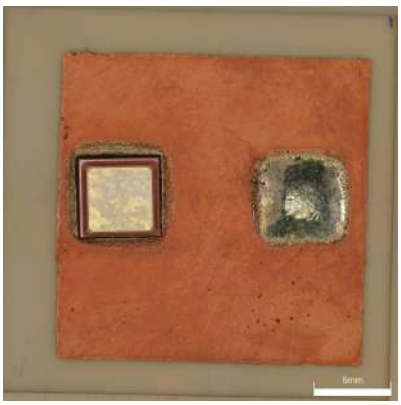
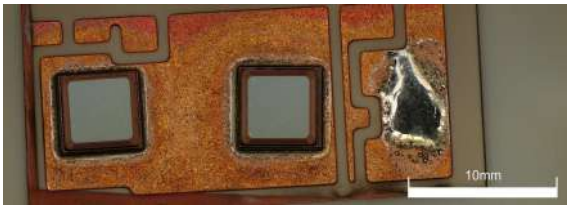


Figure 11.14: Sample#4 interface between shiny solder and area with incomplete evaporation

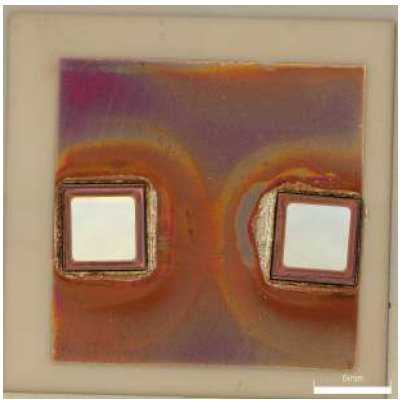
Only by further increasing soak time and dwell time i was able to obtain shiny result with no presence of flux and minimal defect such as splashes.



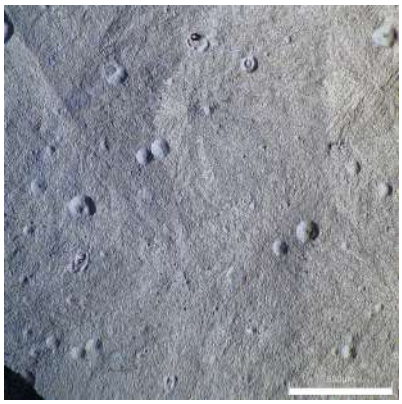
(a) Sample#13 was also cleaned with Isopropyl alcohol in order to remove some flux traces. This paste is a no-clean formulation so small traces of flux organic residue are not relevant.



(b) Sample#22 had been done on a cut out from a real DBC, the solder near the die still shows presence of splashes, the solder paste on the right has a very shiny appearance and does not present flux residues suggesting good solder parameters have been found.

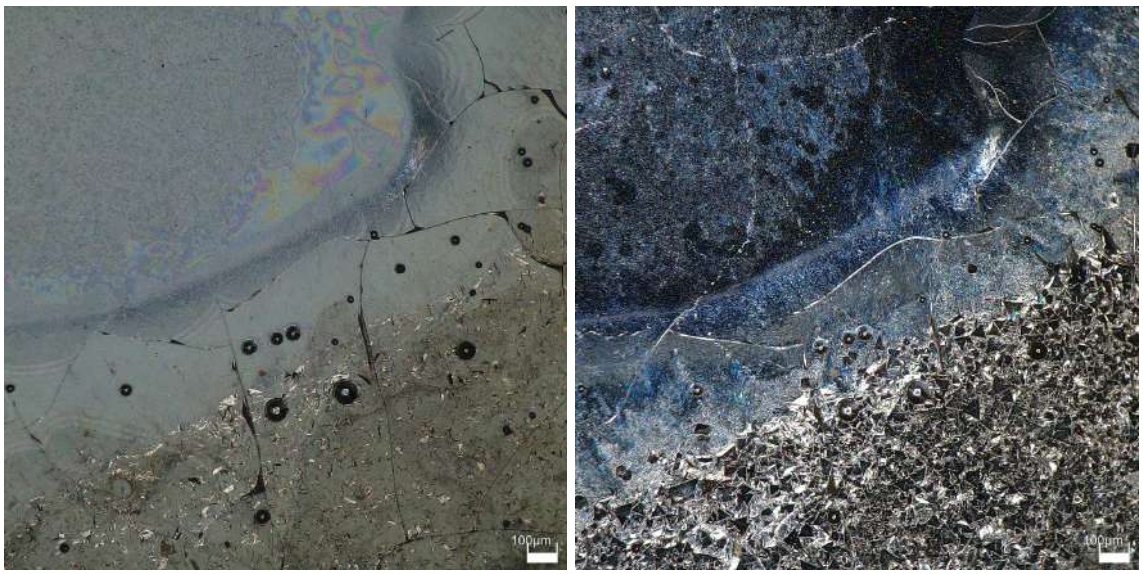


(c) Sample#11 shows a good solder appearance, the dies are slightly misplaced on purpose in order to show the behaviour of the underlying paste.



(d) Sample#12 40x zoom on a bare solder shows good amorphous behaviour is still present some graping probably due to the fact that no die was mounted so the metal alloy had nowhere to bond and formed the ball structures.

However as we can see in the microscope images the results still for call for improvements since are still present solder splashes and some cracks due to a still not perfect ramp up profile and to the intrinsic uncleanliness of the process, and the presence of some crystalline microstructure, instead of more amorphous appearance, due to the cooling rates just depending on the exposure to the air temperature of the clean room and not to a controlled process.



(a) (b)

Figure 11.16: Comparison of sample#11 with different illumination under the microscope. on the left we can better see the remaining flux contamination while on the right is more evident the underlying structure of the solder: where the flux was almost all removed we have an amorphous behaviour (better) while where the flux was not fully evaporated we have a crystalline structure (worse). This may be caused by an uneven heating inside the oven which resulted in an uneven evaporation of flux which lead to different cooling rates, with the slower one causing crystallization in the solder.

11.3.1 SEM Imaging Analysis

For this thesis it was performed a SEM analysis of only some of the earlier samples created of solder paste after the reflow both from the surface and from the section of sample#511.22 and #711.21 (both where the die attach was performed and on the bare solder paste). Using SEM imaging it's possible to clearly see the microstructure formed by the solder paste after the reflow process and to better visualize some of the defect that may happen.
In figure 11.17 is shown a wider shot of a solder to showcase the conformed amorphous behaviour over greater areas while in figure11.18 the microstructure formed by the different compounds in the paste are more visible, in this figure is also tried to be displayed the interface between the area where all the solder was removed (left) and the side where flux was still present however while the paste does not seem to behave differently the right side happears all black out due to a difference to great of height for the SEM to keep them in focus simultaneously and due to the non conductive nature of the flux.

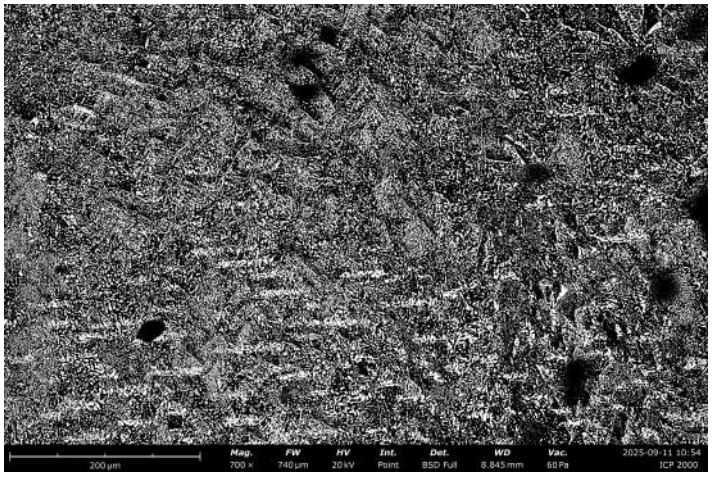


Figure 11.17: SEM image showing the amorphous microstructure forming where a correct soldering process is performed.

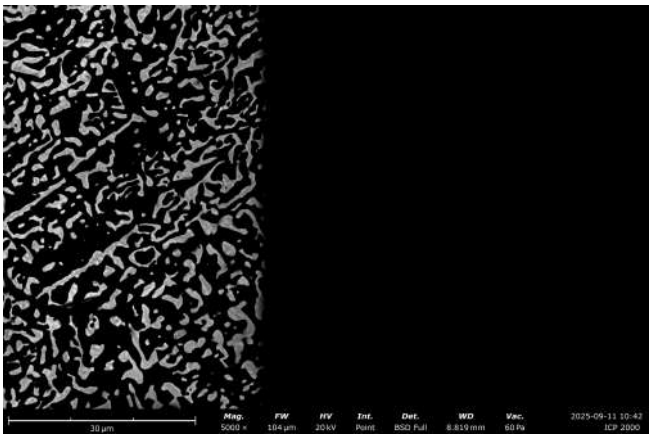


Figure 11.18: SEM image of the interface between where the flux was completely removed (left) and where it was present (right) which appears as black because of different height needing different focus.

Using SEM even defects can be observed more in detail, in figure11.19 is shown the presence of graping in the finished solder in the form of the small spherical protrusions, the whiter the are in

the image the closer it is to the microscope due to more electrons being reflected, and the presence of what seems like a crack. In this image is also clearly visible an interesting effect, not related to the soldering, the charging effect of the SEM which is caused by the impinging electron negatively charging conductive surfaces causing a whiter colouring as in the rectangular shape visible near the center where the SEM was zoomed in before the acquisition of this picture.

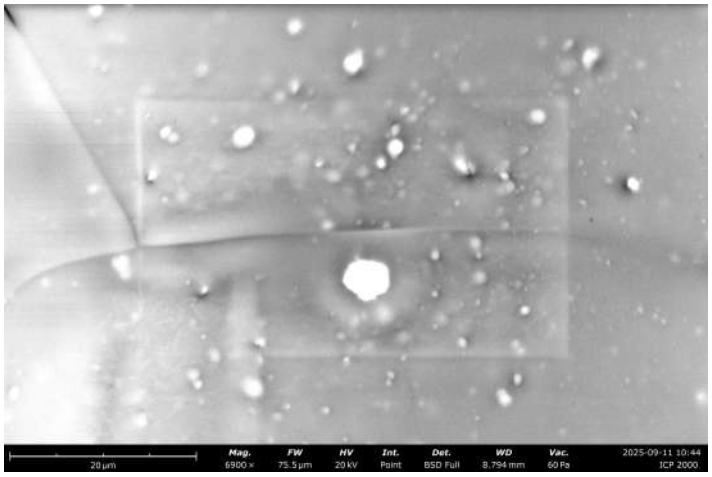


Figure 11.19: SEM image showing the graping effect. Moreover in this picture is noticeable the charging effect of the SEM onto a conductive surface.

The section images allows for a destructive analysis of the the behaviour of the paste in its bulk other than the surface. As seen in figure11.20 where the die was not attached the microstructure is finer more in depth while in figures 11.21 and 11.22 where also the die was present the microstructure appears to have the same dimension along the whole thickness. In all three of these section images no voids are present (in figure11.22 the darker spots are more likely copper residues from the cutting). In figure 11.21are clearly visible the "scallop-like" structures of the inter-metallic Cu_6Sn_5[93] at the solder-copper interface.

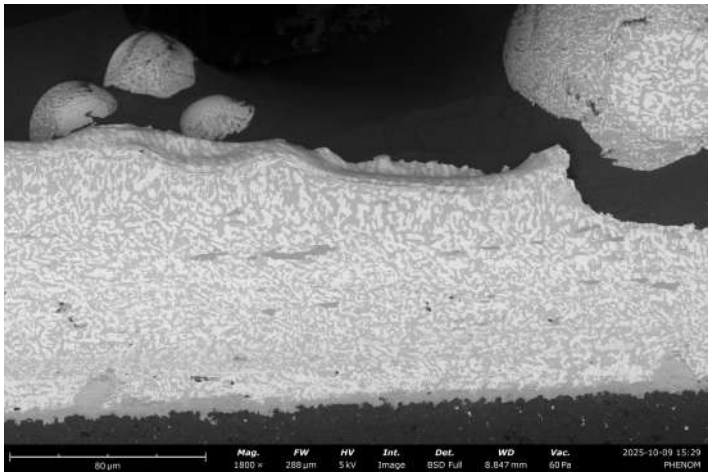


Figure 11.20: Section image showing solder microstructure and the clustering into balls that happened when flux was not completely removed

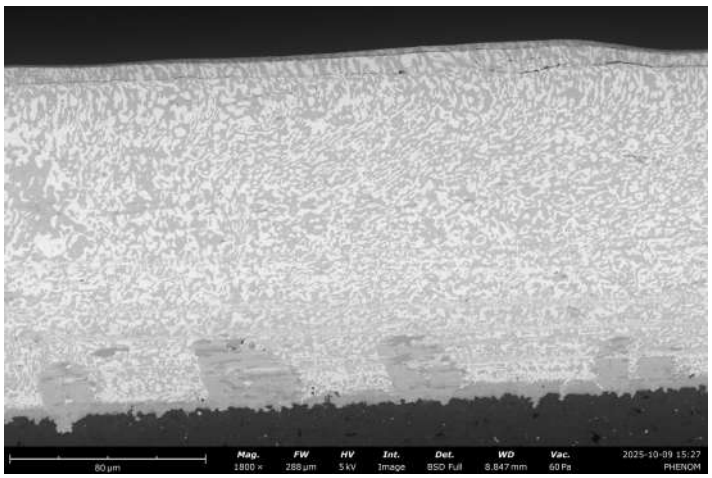


Figure 11.21: Section image showing the amorphous microstructure of the solder and at the bottom the "scallop-like" Cu_6Sn_5[93] grains at the solder-copper interface

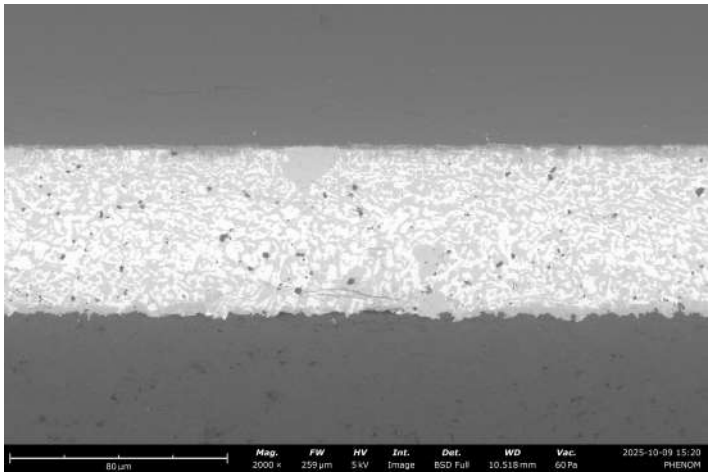


Figure 11.22: Section image, Die on top, solder material in the middle and copper layer below. The image shows no presence of void or other defects.

11.4 Shear test

In the section below are shown and commented the curves measured during the shear test, converted into MPa and plotted into MATLAB graphs.

When the shear test was performed onto the dies attached to the DBC-like substrate the obtained result were either the dislodgement of the pressure applying set up from the die (measurements from this cases are not analysed but are reported inside the github repository https://github.com/PPiqwert/Thesis.git) the delamination of the Ti-Cu layers from the substrates as depicted in figure11.24 where is visible how the dies, upside down on the right have the layers still attached while on the left we can see the bare alumina where the dies where positioned.
This de-attachment was obtained on the DBC-like regardless of the thickness of the deposited solder paste and reflow parameters for measured forces averaging around 5MPa as shown in figure11.23.
For this reason these values are more related to the adhesion strength of the PVD process used for the Ti and Cu layers than the effective solder. However, the clean cut in which those layers have been removed may also suggest that the formation of intermetallic-compounds that might have created brittleness.
Some further composition analysis on the back of the removed die could be useful to pin point the real reason of the delamination however this was not done in this thesis.

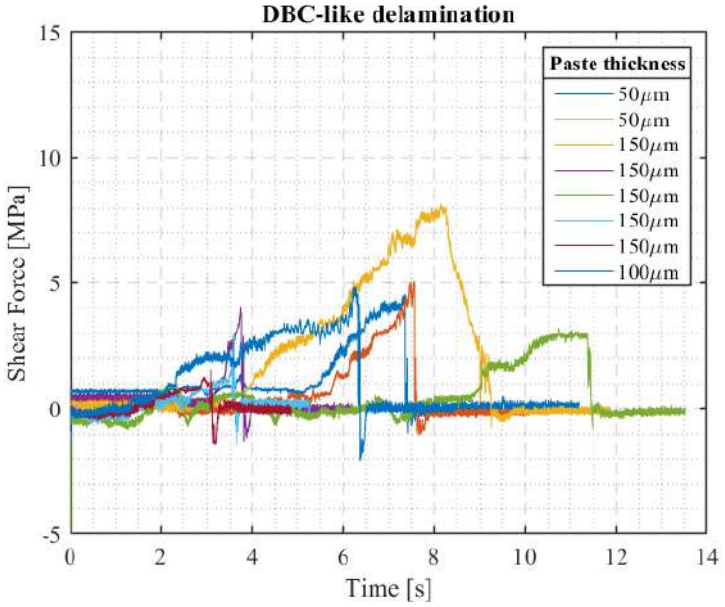


Figure 11.23: Curves measured when the delamination of the copper and titanium layers occurred.

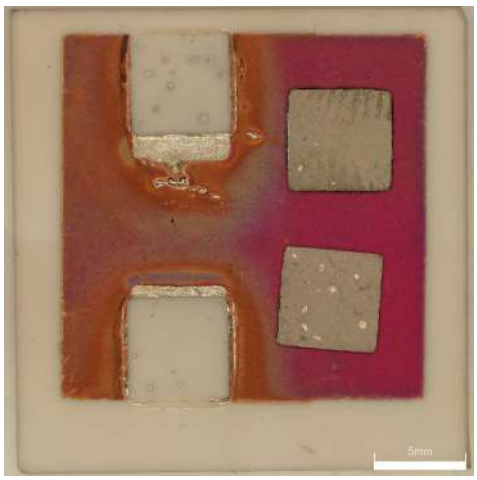


Figure 11.24: De-laminated dies on the DBC-like substrate.

Since using the DBC-like substrates has proven not indicative of the real adhesion strength of the same test has been carried out on the commercial DBCs.
In this case the obtained results were either the dislodgement due to the die cracking or the dislodgement shear test apparatus without breaking the die. Similarly to the DBC-like case the values obtained seems to not be dependent on the deposited paste volume and cannot quantitatively tell the exact strength of the obtained joints since the die broke before the solder was sheared. In the figure11.25 below are shown two examples of chipped dies attached onto the DBC which made further testing on the same sample impossible due to causing dislodging of the pressure-applying rod.

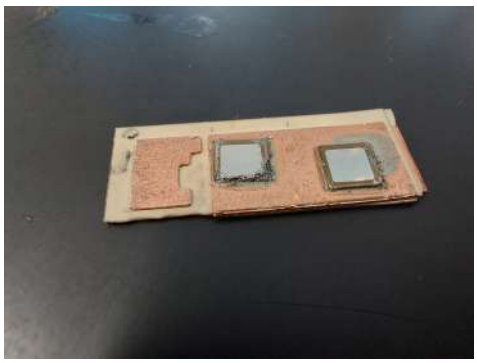


Figure 11.25: Images showing two of the dies chipped during the shear testing.

The measurements shown in figures11.2611.2711.28 average between 5 and 8 MPa which compared to literature values for solder ball grid arrays[94] and small components[95] are an order of magnitude smaller. At least qualitatively, a soldered joint that does crack before the attach component breaks means that it is able to perform its job without being the failure point of the system. However further samples, done specifically for the sake of the shear test, substituting the die with a sturdier piece of material of easier grip, in order to have the effective solder as the weaker element should be conducted to better gauge the real adhesive strength of the soldering done with these parameters.

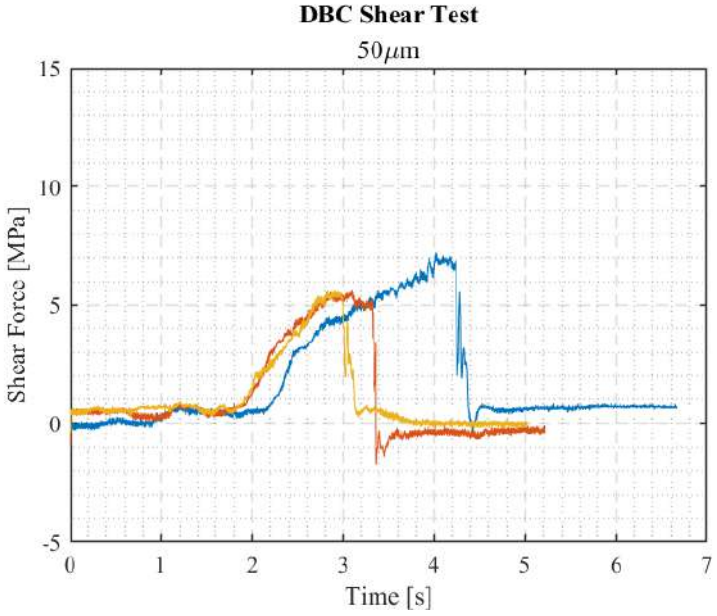


Figure 11.26: Curves for soldering done depositing the paste using the 50μm stencil.

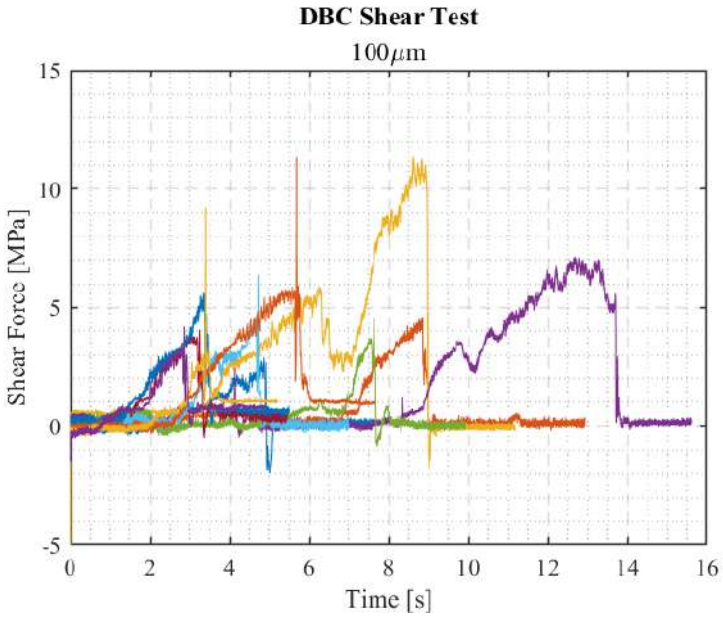


Figure 11.27: Curves for soldering done depositing the paste using the 100μm stencil. In 4 of the measured curves are noticeable big spikes right after the dislodgement that have been cause in an error of the set up where the load cell was hitting on the supporting structure causing an error which did not however influenced the correctness of the previous measure.

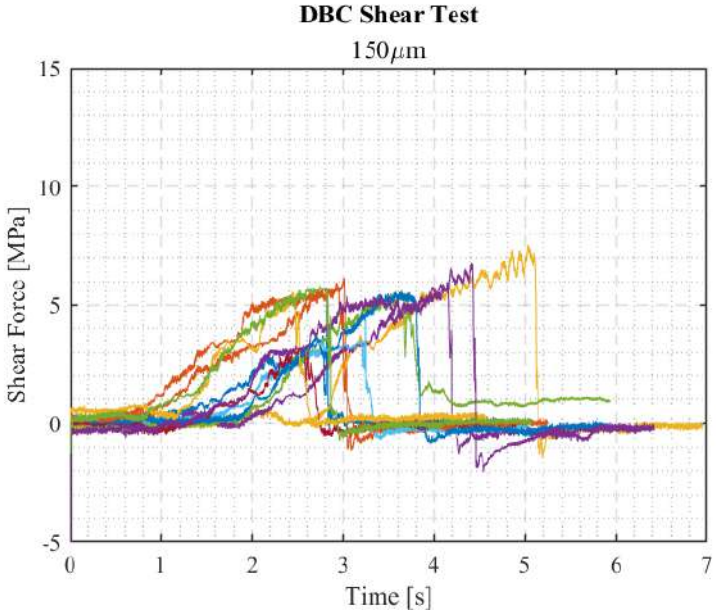


Figure 11.28: Curves for soldering done depositing the paste using the 150μm stencil.

Appendix A

12.1 Reflow Parameters

Table 12.1: Process parameters. In green are highlighted the parameters that both gave the best result for the Sn42Bi57Ag1 solder paste while in orange are highlighted the parameters obtained with the Auto-profiling mode of the oven by setting as temperature to be reached the ones suggested in the pastes TDS. The sample # correspond to the tries done depositing the solder paste and die instead of just measuring the temperature inside the reflow oven.

#	T_p	T_r	t_f	t_p	t_r	t_d	t_c	sample
1	190	430	0	160	30	20	30	1
2	150	240	30	90	30	90	5	2
3	175	249	90	180	50	20	30	
4	139	170	75	100	30	20	30	
5	250	430	0	160	30	20	30	
6	230	430	75	100	30	20	30	
7	200	400	90	90	50	20	30	
8	175	249	90	90	50	20	30	
9	139	180	75	90	30	20	50	
10	250	350	75	90	30	20	50	
11	180	400	75	90	50	20	30	
12	230	430	90	90	50	20	30	
13	210	400	75	90	50	20	30	
14	230	430	90	90	30	30	30	
15	210	430	75	90	40	25	30	
16	230	430	75	90	40	25	30	
17	210	430	75	100	25	20	30	
18	210	430	75	90	20	35	30	
19	180	430	75	90	50	20	30	
20	180	430	75	90	30	30	30	
21	250	430	90	90	45	25	30	
22	250	365	75	90	40	20	30	3,4
23	250	430	90	90	70	20	25	
24	250	430	0	160	45	20	30	
25	180	400	0	145	20	20	30	
26	250	380	75	90	40	20	30	
27	250	430	90	90	85	25	25	
28	250	430	90	70	70	25	25	
29	250	430	0	160	45	30	30	
30	250	380	75	90	40	20	30	
31	250	430	90	50	100	30	25	
32	250	430	90	70	100	30	25	
33	250	380	75	90	40	20	30	
34	250	370	75	90	40	20	30	
35	250	430	100	125	100	25	25	
36	250	365	75	90	40	20	30	
37	250	365	75	90	40	40	30	5
38	250	360	75	90	40	60	30	
39	250	425	0	160	45	75	30	6
40	250	430	90	90	45	85	25	9,10
41	250	360	75	90	40	75	30	7,8
42	250	430	90	70	45	75	25	11
43	250	405	0	160	45	75	30	12,14,22
44	250	430	37	51	69	0	64	20
45	250	430	18	22	9	0	40	21
46	185	280	44	67	78	0	40	13,16
47	185	280	44	67	78	25	40	17,19

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