POLITECNICO DI TORINO

Master's Degree in Electronic Engineering

Master's Degree Thesis

LDO Voltage Regulator Design for the Power Management of a Wearable Electrochemical Biosensor

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"That love is all there is,
is all we know of love;
it is enough, the freight should be
proportioned to the groove."

— Emily Dickinson

To my parents

Abstract

Progress in material science, electronics, wireless communication and biotechnology has paved the way for the advent of wearable devices.These portable systems consist of sensors integrated in electronic gadgets such as patches, tattoos, smart contact lenses and bands. Their main purpose is to support home based healthcare, lowering the burden on the healthcare system and facilitating early intervention to prevent pathologies that are typically discovered when the disease is at an advanced stage.

Wearable devices represent a promising and emerging domain, enabling non-invasive measurement of physiological parameters that reflect the health condition of the patient, without the need to schedule a clinical appointment. Furthermore, with this technology, medical practitioners are able to garner a richer data set for tailored diagnosis and treatment.

From an electronics perspective, power consumption is a critical aspect, given that these systems need to operate continuously over a long period. This is why an ASIC (Application-Specific Integrated Circuit) module is chosen over a general-purpose counterpart for the power management system. A tailored design enables high performance without wasting resources because, unlike Off the Shelf (OTS) electronics that offer a wide range of applications, it is optimised for a specific one.

The work of this thesis is part of a larger project that aims to develop a sweat-based biosensor for continuous monitoring of biomarkers related to the well being of expecting mothers.

In particular, this contribution concerns the design of a voltage regulator which is part of the power management system of the device. After analysing key requirements including low power consumption, limited silicon area and stable output voltage, several architectures have been considered. The most suitable solution was found to be a Low Dropout (LDO) voltage regulator with a single stage error amplifier and a beta multiplier for current and voltage reference generation. The circuit design and layout have been implemented using the Cadence Virtuoso Platform. To assess the performance of the regulator, DC, AC and transient analyses have been performed. The final design achieves a quiescent current of 16.6 μA and occupies an area of only 0.03 mm^2. Moreover, the regulator features a dropout voltage of 100 mV and is characterized by 8.7 mV/V for line regulation and 1 mV/mA for load regulation. These performances demonstrate that the requirements have been met and that the design is suitable for the intended application.

Keywords: Wearable Devices, Sweat Sensing, Power Management, ASIC Design, LDO Voltage Regulator

Sommario

I progressi nella scienza dei materiali, nell'elettronica, nella comunicazione wireless e nella biotecnologia hanno spianato la strada all'avvento dei dispositivi indossabili. Questi sistemi portatili sono costituiti da sensori integrati in gadget elettronici quali cerotti, tatuaggi, lenti a contatto intelligenti e braccialetti. Il loro scopo principale è supportare l'assistenza sanitaria domiciliare, riducendo l'onere sul sistema sanitario e facilitando l'intervento precoce per prevenire patologie che vengono tipicamente scoperte quando la malattia si trova in uno stadio avanzato.

I dispositivi indossabili rappresentano un settore promettente ed emergente, che consente la misurazione non invasiva di parametri fisiologici che riflettono le condizioni di salute del paziente, senza la necessità di programmare un appuntamento clinico. Inoltre, grazie a questa tecnologia, i medici sono in grado di raccogliere un set di dati più ricco per una diagnosi e un trattamento personalizzati.

Dal punto di vista dell'elettronica, il consumo energetico è un aspetto critico, dato che questi sistemi devono operare continuamente per un lungo periodo. Per questo motivo, per il sistema di gestione dell'alimentazione, viene scelto un modulo ASIC (Application Specific Integrated Circuit) rispetto a una controparte per uso generale. Un design su misura consente alte prestazioni senza sprecare risorse poiché, a differenza dell'elettronica Off the Shelf (OTS) che offre un'ampia gamma di applicazioni, esso è ottimizzato per una specifica.

Il lavoro di questa tesi si inserisce in un progetto più ampio che mira a sviluppare un biosensore basato sul sudore per il monitoraggio continuo di biomarcatori relativi al benessere delle future mamme.

In particolare, questo contributo riguarda la progettazione di un regolatore di tensione che fa parte del sistema di gestione dell'alimentazione del dispositivo. Dopo aver analizzato i requisiti chiave, tra cui il basso consumo energetico, l'area ridotta su silicio e la tensione di uscita stabile, sono state prese in considerazione diverse architetture. La soluzione più adatta è risultata essere un regolatore di tensione Low Dropout (LDO) con un amplificatore di errore a stadio singolo e un beta multiplier per la generazione della corrente e della tensione di riferimento. Il design del circuito e il layout sono stati implementati utilizzando la piattaforma Cadence Virtuoso. Per valutare le prestazioni del regolatore, sono state eseguite analisi DC, AC e transitorie. Il design finale raggiunge una corrente di quiescenza di 16.6 μA e occupa un'area di soli 0.03 mm^2. Inoltre, il regolatore presenta una tensione di dropout di 100 mV ed è caratterizzato da 8.7 mV/V per la regolazione di linea e 1 mV/mA per la regolazione di carico. Queste prestazioni dimostrano che i requisiti sono stati soddisfatti e che il design è adatto all'applicazione prevista.

Acknowledgement

Desidero esprimere la mia profonda gratitudine a coloro che hanno reso possibile la realizzazione di questo lavoro di tesi e, più in generale, il completamento del mio percorso di studi.
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Chapter 1

Introduction

1.1 Wearable devices for medical healthcare

Technological advancements have led to the advent of devices that facilitate personalised, accessible healthcare through wearable devices. This term refers to all devices that can be worn and that help individuals monitor their health in order to identify risk factors early on and support the timely diagnosis of potential diseases. [1]

The applications of these devices extend beyond basic physical activity tracking, embracing a broad spectrum of specialized functions, thereby highlighting their versatility within the health sector. This technological capacity significantly enhances users' ability to self-manage their health and incorporate effective preventive measures to maintain wellness. Fundamentally, wearable technology facilitates the empowerment of individuals, enabling them to participate actively in their own care. It is essential to maintain a critical perspective,recognizing that while these instruments powerfully support clinical judgments, they cannot substitute the expertise of a medical specialist.[1]

In particular, the fundamental advantages of adopting wearables can be summarized as follows:

- **Long-Term, Detailed Self-Monitoring**: wearable devices enable continuous collection of physiological parameters both during daily activities and at rest. This generates a richer set of individual health data with greater temporal continuity than the instantaneous readings obtainable in a clinical setting. It would in fact be impractical for healthcare facilities to manage such a high frequency of repeated measurements over long periods.
- **Comfort and Economy**: the use of these tools ensures greater convenience for the user and reduces the need to visit the clinic for routine check-ups. This results in considerable savings in terms of time spent on scheduling and travel, as well as significant benefits in terms of financial resources.
- **Early Intervention and Identification**: the constant acquisition of data acts as a predictive alert mechanism, allowing timely identification of signs of potential risk. This makes it possible to recommend the necessary clinical investigations at an early stage, preventing the progression of pathological conditions to advanced and less reversible stages.

[1]

From the perspective of healthcare providers, the introduction of wearables generates benefits that improve both the efficiency and the quality of care delivered:

- **Objective Data and Remote Monitoring**: wearables provide clinical staff with objective, real-time data on patients, allowing remote monitoring of progress.[2] This builds trust in patients, who are not limited to communicating only their subjective perceptions.
- **Highly Personalized Care**: access to longitudinal data provides clinicians with a comprehensive and holistic picture of an individual's health. On this basis, it is possible to adopt a more personalized therapeutic approach tailored to the specific needs of the patient.
- **Increased Organizational Efficiency**: widespread adoption has the potential to reduce doctor-patient contact time and represent a more cost-effective solution for providers. This eases the overall burden on healthcare systems by shifting part of the management of care to the individual.
- **Improved Engagement and Communication**: the availability of real-time data for patients themselves facilitates communication with clinicians and promotes health education. In this way, patients can contribute more knowledgeably to clinical discussions, promoting greater adherence to agreed treatment decisions. Furthermore, the patient participation in the therapeutic process has the potential to enhance the effectiveness of the treatment itself. In the context of home-based rehabilitation, the proper execution of the exercises is of paramount importance. Failure to perform these exercises correctly, or the loss of motivation to progress, can have a detrimental effect on the patient.[2]

[1]

1.1.1 Biosensor Wearable Devices

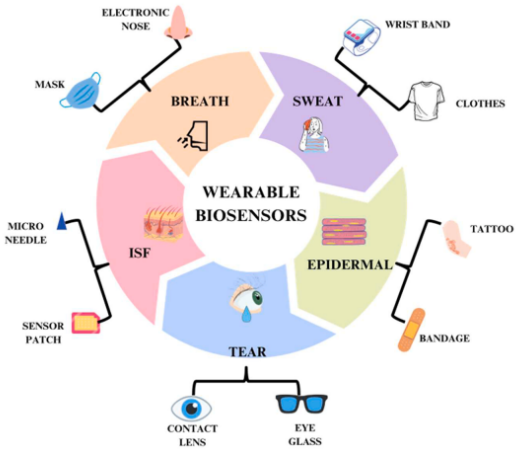


FIGURE 1.1: Schematic representation of wearable sensor systems utilizing various biological fluids [3]

As human knowledge in the scientific fields progresses, the technological devices obtained are becoming increasingly sophisticated. In the context of wearables, if at the beginning they could measure only simple physiological parameters, predominantly associated with sport activities, new sensors are emerging that can track complex, medically significant biomarkers in a non-invasive way. [4] The body fluids utilized for this molecular analysis are various, including sweat, interstitial fluid, tears [5], breath and epidermal fluids. [3]
Table 1.1 provides a comparative analysis of the cited biological fluids highlighting the related challenges, advantages and limitations associated with each.

TABLE 1.1: Comparison of various biological fluids for wearable biosensing applications [3]

Biological fluid	Key Source	Accessibility	Biomarker Accuracy	Analytical Complexity	Advantages	Limitations
Tear	Lachrymal Glands	Moderate (via eye-wearable devices)	High-due to direct diffusion of analytes from blood	Low-streamlined detection of proteins, electrolytes, and metabolites	High precision and specificity, similar composition to blood	Limited volume, collection can be challenging without irritation
Sweat	Eccrine and apocrine sweat glands (via skin)	High-readily available across the body surface	Moderate-concentrations can vary based on activity and hydration	Moderate-influenced by sweat rate, evaporation, and contamination	Non-invasive, widely accessible, suitable for continuous monitoring	Biomarker concentration variability, potential environmental interferences
ISF	Between skin cells and capillaries	Moderate-accessed via microneedles or skinpermeable patches	High-closely reflects blood analyte levels	Moderate to High-requires minimally invasive access tools	High biomarker relevance; stable composition	Requires specialized access methods; slower sample replenishment
Epidermal	Outer skin layers	Low-small quantities	Low to Moderate	High-complex matrix and low volume	Potential for superficial, noninvasive sampling	Low fluid volume; difficult to isolate specific analytes
Breath	Lungs (exhaled air)	High-easy collection	Low to Moderate-depends on target gases (e.g., VOCs)	High-complex and variable due to environmental and physiological factors	Non-invasive; continuous sampling possible	Variability due to diet,environment, and metabolism

These biosensors are then integrated with the electronic and wireless communication system into a device that is able to collect data coming from chemical reactions and converted into electrical signals. The latter are transmitted to a mobile or portable device that is capable of elaborating and performing complex analysis of the information using artificial intelligence. [6] [3]

The quality of the device depends principally, among all the parameters, on the accuracy of the biosensor, meaning the capacity to detect unambigously and precisely the target, which could be a an enzyme, nanoparticle, protein ecc. Wearable biosensors devices include three fundamental elements (see 1.2):

- *bioreceptor*: which is the element that selectively senses the biomarker
- *physicochemical transducer*: which converts the chemical change into a measurable electrical signal
- *signal processing system*: which determines the concentration of the analyte based on the data acquired

[3]

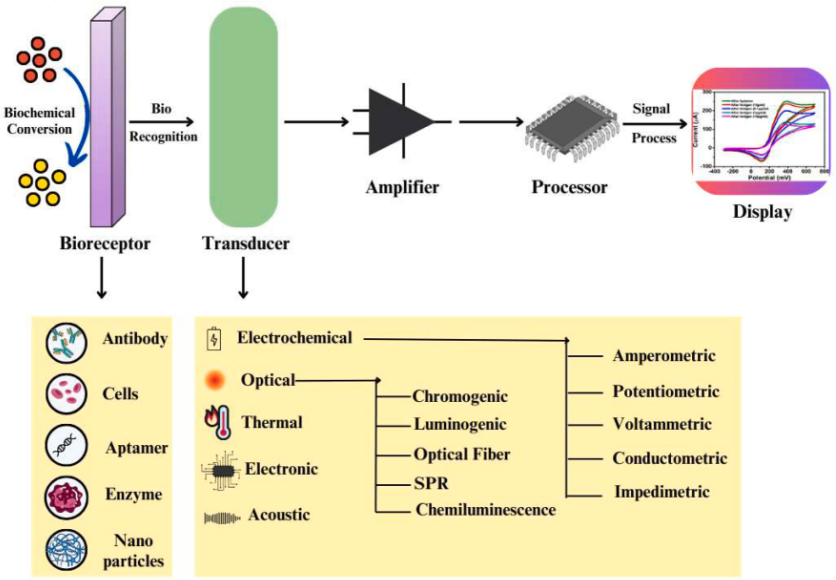


FIGURE 1.2: Schematic representation of conventional biosensors comprising of distinct bioreceptors and different type of transducers [3]

Sweat-based biosensors

Of the cited biofluids, sweat is the most promising due to the numerous advantages it possesses. Firstly, it contains a high quantity of substances that offer physiological information, thereby providing a detailed overview of the patient's well-being. The biomarkers that can be detected include electrolytes, metabolites, drugs, trace metals, proteins, hormones and small molecule compounds, which can be correlated with pathologies and diseases. (see Table 1.2). [7]

A biosensor collecting sweat is less invasive and the probability of having an infection is lower when compared to traditional procedures. [8] The chemical composition of sweat is similar to that of blood, but with a reduced concentration. However, the acquisition of blood samples requires a professional operator, and using a needle could cause discomfort to the patient. Moreover, it takes

TABLE 1.2: Key analytes in sweat and associated health conditions [7]

Analyte category	Analyte	Health condition
Electrolytes	Na^+	Dehydration, hyponatremia, electrolyte imbalance
	Cl^-	Dehydration, cystic fibrosis
	K^+	Hypokalemia, muscle cramps
	Ca^{2+}	Myeloma, cirrhosis, renal failure, acid-base balance disorder
	NH^{4+}	Shift from aerobic to anaerobic metabolic conditions
	PH	Pathogenesis of skin diseases, wound healing
Metabolites	Glucose	Diabetes
	Lactate	Shift from aerobic to anaerobic metabolic conditions
	Alcohol	Inebriation
	Uric acid	Renal dysfunction, gout
Drugs	Caffeine	Coronary syndrome, hypertension, Depression
	Levodopa	Parkinson's disease
Trace metals	Zn^{2+}	Stress and immune system-induced muscle damage
	Cu^{2+}	Rheumatoid arthritis, Wilson's disease, cirrhosis of the liver
Other analytes (hormones, cytokines, proteins, etc.)	Interleukin 6	Insulin activity, immune responses in cancer therapy
	Cortisol	Stress
	Tyrosine	Metabolic disorders, tyrosinemia
	Neuropeptide Y	Stress

several days for the laboratory to analyse the samples and obtain the results. Urine is another biofluid that could be considered for sampling, given its extensive use in conventional clinical analysis. Despite the abundance of biomarkers, it is proven to be inappropriate for real-time continuous monitoring. Sweat based-biosensors, conversely, execute the same task but autonomously, without causing the slightest unease to the patient.

There are two possible methods for the extraction of sweat from the human body. The first method is passive and involves the execution of intense physical exercise to induce perspiration. The second option is an active one, and the production of sweat is induced by means of electrical stimulation. The latter approach is the most suitable in the context of health monitoring.

Iontophoresis is a method that can be used to obtain sweat on demand. First an agonist, defined as chemical substance or drug that stimulates the sweat glands to produce sweat (such as pilocarpine molecules), needs to be placed on the appropriate electrode. Subsequently, a voltage is applied between two electrodes positioned on the skin surface in close proximity to a sweat gland. The low current generated at this point flows under the skin enabling the agonist to reach the sweat glands at the anode.[7] Sweat extraction is relatively easy since sweat glands are well distributed across the human body, with the highest density on the palms and soles [9]. It has to be noted that the sweat secretation rate is subject to interpersonal variability (e.g. pH) and is influenced also by the environment (e.g. temperature). Furthermore, the composition of the sweat obtained with the two approaches is different: the passive approach typically yields higher concentrations

of metabolites. [7]

FIGURE 1.3: The basic principle of iontophoresis [7]

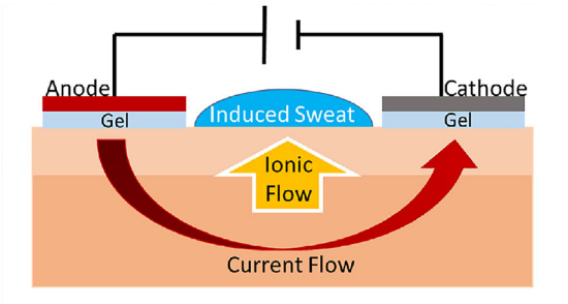


TABLE 1.3: Comparison of sweat sensing methods [8]

Method	Sensitivity and sensibility	Real time monitoring capability	Response time	Cost	Limitations
Colorimetric	high	limited	fast	low	dependent on the lightnig conditions
Fluorometric	high	possible	fast	high	pH, temperature, background fluorescence and photobleaching impact the performance of the sensor, large scale optical equipment needed
Plasmonic	high	possible	moderate	high	large scale optical equipement, dependent on the lightnig conditions
Electrochemical	high	possible	fast	low	-

Different methods for sweat sensing are available including electrochemical, fluorometric, plasmonic and colorimetric approaches. Electrochemical sensing is often the preferred one since it is simple, cheap, doesn't require bulky equipment and it has high performance [8] (see Table 1.3). Once perspiration has produced the biofluid, the challenge lies in safely collecting it avoiding evaporation or mixing with other particles irrelevant for the purpose. Furthermore, preventing mixing fresh sweat sample with the old one is essential. Interfering chemicals could, in fact, influence the sensor readings producing unexpected results. The analysis of the target concentration needs to be evaluated using always the same quantity of fluid, losing a part of the sample by evaporation could mean, losing also part of the analytes.

Microfluidic technologies allows the transportation of the sample to reservoirs exploiting capillary forces to drive the fluid along the channels. This expedient guarantees data integrity, accuracy in the measurement and detection of the analytes at low concentration. Further control over sweat flow direction is achievable by implementing either valve mechanisms or modifying the channel surface with a hydrophilic coating. Continuous sweat delivery can be maintained by designing an evaporation-driven micropump using micropores placed at the microfluidic chip's output. These microperforations offer simple control over the flow rate by altering their quantity or geometry.

Hydrogel can be implemented to reduce the sampling time and increase the efficiency. Due to the osmotic pressure difference between the hydrogel and the sweat, the fluid is pumped into the microchannels.

To perform the sensing it is used a three electrode structure that consists of

- working electrode: where the chemical reaction occurs
- reference electrode: at a known potential to be compared with the working electrode
- counter electrode: used as a collector for the current

When the circuit is open, the reduction or oxidation of the target at the working electrode will alter the electrical characteristics allowing to find the concentration of the target evaluating the difference with the reference.

There are three types of measurements: potentiometry, amperometry and voltammetry. The choice of the proper one is based on the concentraction and the properties of the analyte. The last method, unlike the others, can measure multiple analytes simultaneously and can be of three types: CV (cyclic voltammetry) and DPV (differential pulse voltammetry) that can be used for drug detection, and SWASV (square wave solvation voltammetry).

Wearable biosensing technologies must maintain continuous and reliable detection of the wearer's physiological data while minimizing disruption to their daily activities, as the devices are in constant contact with the skin. Consequently, a fundamental requirement for wearable sweat sensors is the ability to adapt to the skin's complex geometry. This means the sensor substrate must possess adequate flexibility and stretchability, alongside robust electrochemical and mechanical stability. Currently, flexible substrates are typically fabricated from polymers. These polymer films are highly advantageous for wearable devices due to their affordability, excellent physical and mechanical characteristics, strong electrical insulation, and good biocompatibility.[7] The PCB (Printed Circuit Board) that hosts all the electronic modules including the power management, the programmed microcontroller and the wireless communication component, needs to be flexible as well (FPCB). [8]

From an electronic perspective, when sensing is performed, an Analog Front-End (AFE) first conditions the signal. This conditioned signal is then digitally converted by an Analog-to-Digital Converter (ADC). The digital signal is subsequently transmitted to the microcontroller, which processes and calibrates the data to determine the analyte concentration. The final result is then communicated wirelessly to a smartphone or other portable device. Wireless communication is essential for real-time data transmission and typically relies on protocols such as Bluetooth Low Energy (BLE) or Near-Field Communication (NFC). While BLE offers an extended range, its high-frequency data transmission can significantly increase the overall power consumption of the device. Conversely, NFC operates over short distances (only a few centimeters) and requires minimal, or even zero, power consumption in the case of passive tags. Despite these advantages, NFC is not suitable for continuous monitoring since requires the partecipation of the user to transfer the data. [7]

Since the wearable device should operate for an extended period of time, a key challenge is represented by the power consumption. Currently, energy sources for these devices are divided between lithium-ion (Li-ion) batteries and energy harvesting technologies. Li-ion batteries are often utilized for their benefits, which include a long operational lifespan and fast recharge capability. [10] However, scaling Li-ion technology down to the necessary small form factors while

mitigating the inherent risks of overheating, expansion, and explosion remains a significant design challenge. To address these safety concerns, protective layers that facilitate automatic power cut-off during overheating events are often incorporated.

Seeking alternatives to conventional power sources is crucial for miniaturization and safety. Zinc-manganese batteries,which rely on quasi-solid water electrolytes—represent a highly promising successor, as they eliminate the typical safety concerns associated with Li-ion technology while offering the desired high output voltage, high capacity, lightweight nature, and environmental friendliness.

Furthermore, to satisfy the increasing power demands of wearable electronics and reduce the inconvenience of frequent charging or cumbersome wired power delivery, wearable systems are increasingly integrating energy harvesting devices. Sources like solar cells, and microbial biofuel cells (BFCs) are utilized to achieve self-sustainable operation. Flexible photovoltaic cells, for instance, capture solar energy to provide stable self-powering and high energy storage capacity for continuous system function. Notably, BFCs can generate power for sensors and implantable devices (such as pacemakers or stimulation electrodes) by converting molecules like glucose, lactate, uric acid, or ethanol found directly within biofluids. Given its abundance, human sweat serves as an ideal sustainable bioenergy source for powering wearable sweat sensors. [7]

1.2 Wearable devices to support women pregnancy

A systemic disparity exists in the funding and investment allocated for health research and medical innovation, demonstrating a clear bias based on biological sex. Healthcare systems have historically favored cisgender males, often leading to the generalisation of product development and research results derived primarily from their biological characteristics to the rest of the population.[11] Furthermore, global investment tends to be more heavily weighted toward male prevalent pathologies, which results in neglecting or understudying conditions prevalent in women. [12]

These considerations clearly highlight a critical gap in the current healthcare system and are correlated with the increased prevalence of ineffective, harmful, or inappropriate treatment strategies implemented for females. The consequence is that women often feel limited in their understanding of their own bodies and are frequently unaware of their full health choices.

The necessity for such tools is tragically underscored by statistics regarding fertility and maternal health: the WHO (World Health Organization) reports that 40 million women annually develop long-term health conditions during pregnancy. If left unaddressed or improperly diagnosed, these conditions can negatively impact women's lives for years after childbirth, thus highlighting an urgent need for dedicated health monitoring solutions.[12]

Wearable devices can be particularly useful for expecting mothers, as they can be used to track the baby's development by monitoring the well-being of both mother and child through daily measurements of various parameters. Until recently, the predominant options for monitoring pregnancy were to consult a doctor and undergo regular check-ups or to read specialised books. However, today wearable devices and smartphones can be used to support personalised medical care, as the recommendations received are based on the data collected. As a result, if problems arise, precautions can be taken well in advance to prevent worse repercussions. The utilization of these devices could significantly transform the maternity experience. Providing continuous, real-time feedback on the pregnancy's progression serves to reassure mothers, thereby mitigating anxiety and enhancing the perceived sense of security among expectant mothers.

1.3 MoleSense project and outline of the thesis

MoleSense, the project I had the opportunity to be involved in, addresses the problem of women healthcare gap. The aim is to develop an electrochemical wearable sensor, sweat-based, capable of analyzing relevant maternity biomarkers and providing personalized diagnosis to assess women health state.

The contribution of this thesis focuses on the power management module of the biosensor and it is arranged into the following chapters

- **Chapter 2 - Current reference**: presents and characterizes the designed current reference and assesses perfomances pre and post layout.
- **Chapter 3 - Design and analysis of the low dropout (LDO) regulator**: delves into the definition of a power management system contextualizing the role of LDO regulators. After analyzing the state of art architectures, the design methodology is presented. Subsequently, the designed architecture is explained and the performance verified with DC, AC and transient simulations pre and post layout.
- **Chapter 4 - Conclusion**: summarizes the results obtained and discusses possible future optimizations.

Chapter 2

Current reference

Bandgap reference circuits are fundamental components in analogue and mixed-signal electronics, ensuring the correct behaviour of the circuits. These modules generate a DC voltage or current independent of the voltage supply and process variations, ensuring consistency across different operating conditions and preventing unexpected performance issues. The temperature dependency is well defined, and three different categories can be designated:

- proportional to absolute temperature (PTAT)
- constant Gm behavior
- temperature independent

As wearable devices are designed to be worn, it is reasonable to assume that they will not be subjected to a wide range of temperatures. For this reason, temperature dependence is not a key feature and the most appropriate solution can be selected from the PTAT branch.

A beta multiplier reference represents a valid option, having an acceptable temperature coefficient, and giving its simplicity it occupies a restricted amount of area and has low power consumption.

2.1 Beta multiplier current reference

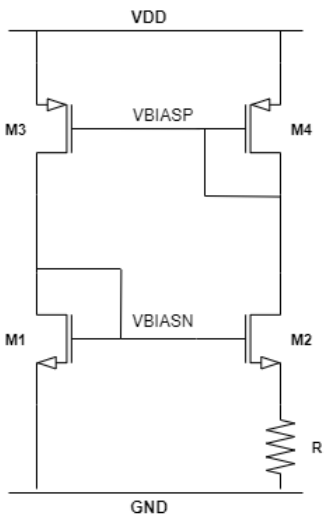


FIGURE 2.1: Beta multiplier current reference schematic

The schematic of the beta multiplier current reference is shown in figure 2.2. The circuit is constituted by four mos transistors and a resistor. The ratio between the sizes of the transistors

defines the ratio between the currents in the two branches and can be defined as

$$\left(\frac{W}{L}\right)_{M1} = k\left(\frac{W}{L}\right)_{M2} \tag{2.1}$$

$$\left(\frac{W}{L}\right)_{M3} = m\left(\frac{W}{L}\right)_{M4} \tag{2.2}$$

The value of k will be discussed later while that of m is set to 1.
Considering that all the transistors work in saturation, the current flowing in each mos can be generally written as:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{th}\right)^2 \tag{2.3}$$

obtaining that

$$V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}} + V_{th} \tag{2.4}$$

The Kirchoff voltage law in the mesh that includes M1, M2 and R is:

$$V_{GS1} = V_{GS2} + RI_{D2} \tag{2.5}$$

Substituting the result of Eq. 2.4:

$$\sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{M1}}} + V_{th1} = \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} k\left(\frac{W}{L}\right)_{M1}}} + V_{th2} + RI_{D2} \tag{2.6}$$

Since m = 1, $I_{D1} = I_{D2} = I_D$. The sources of M1 and M2 are at different voltages, resulting in a different threshold voltages but in this discussion, for simplicity, they are assumed to be equal. From Eq. 2.6 it is possible to obtain:

$$I_D^2 - \frac{2}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{M1} R^2}\left(1 - \frac{1}{\sqrt{k}}\right)^2 = 0 \tag{2.7}$$

The equation has two solutions:

- $$I_D = 0 \tag{2.8}$$

- $$I_D = \frac{2}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{M1} R^2}\left(1 - \frac{1}{\sqrt{k}}\right)^2 \tag{2.9}$$

Considering the non trivial solution (Eq. 2.9) the voltages in the two branches are:

$$V_{BIASN} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{M1}}} + V_{th1} \tag{2.10}$$

$$V_{BIASP} = V_{DD} - \left(\sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{M4}}} + |V_{th4}|\right) \tag{2.11}$$

As can be seen from from Eq. 2.10, neglecting channel length modulation the voltage V_{BIASN} is independent of the voltage supply. Nevertheless, the architecture is temperature dependent due to the dependence of electrical parameters such as μ, R and V_{th} and the behavior is slightly influenced by process variations. [13]

A start up circuit is typically used to prevent the degenerative bias point ($I_D = 0$). It is worth noting that this is only a mathematical solution, since the desired stable point is reached due to leakage currents, but it takes an unbearable amount of time. The primary requirement of a start up circuit is that it should not interfere with the behavior of the current reference. Moreover it should be low power and occupy a limited amount of area, not more than the main circuit.

2.1.1 Design considerations

The circuit has been implemented using TSMC 180nm muse BCD technology.

The value for the resistance can be computed from Eq. 2.9. Some considerations must be taken into account regarding the choice of sizes and the value of the k parameter. Increasing the channel length improves performance by reducing flicker noise and enhancing matching, since the size of the gate area is inversely proportional to the variation of the threshold voltage. Furthermore, it has been demonstrated that increasing the value of k, reduces the dependence on the voltage supply[13].

Table 2.1 reports the sizes chosen to obtain a nominal value of 1.2V for V_{REF} and 6 μA for I_{REF}.

Component	Value	
R	48 kΩ	
MOS	W (μm)	L (μm)
M1	2·3.2	4
M2, M5, M8	8·6.4	4
M3, M4	2·4.5	4
M6	3.2	4
M7	6·4.5	4
M9	0.7	4
M10	0.7	10

TABLE 2.1: Transistor dimensions for the beta multiplier reference

Figure 2.2 shows the complete schematic of the beta multiplier reference including the start up implementation.

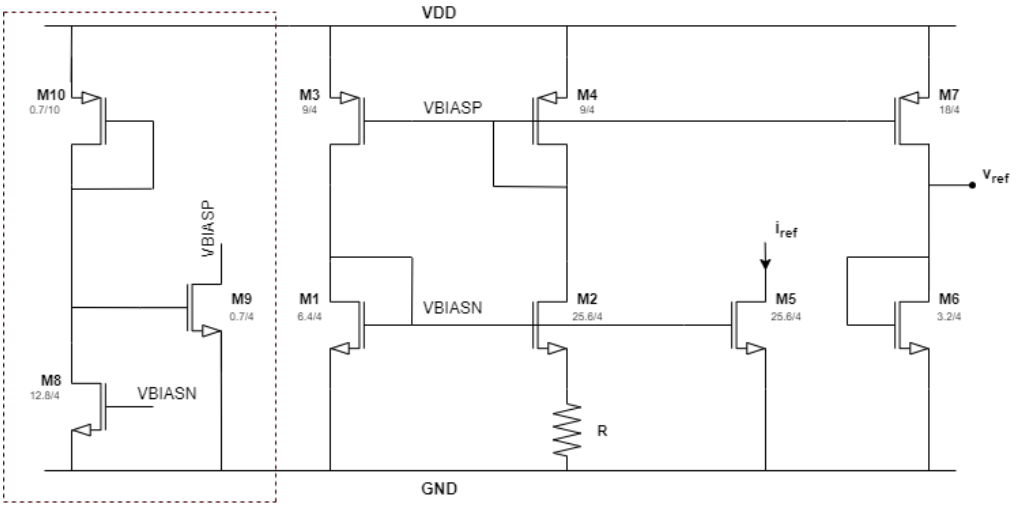


FIGURE 2.2: Schematic of the designed beta multiplier current reference with start up circuit (red box)

Start up circuit

The start up circuit consists of a resistence impemented using a diode connected pMOS, and two other transistors connected each one to a branch of the current reference.

When the power supply is switched on, V_{BIASP} is at V_{DD} while V_{BIASN} is at ground. A current flows through M_{10}, raising the voltage of $V_{STARTUP}$ and switching on M_9. Consequently, a small current flows through the latter transistor, which contributes to decrease the value of V_{BIASP}. Meanwhile, the value of V_{BIASN} raises, switching on M_8 which contributes to lowering the value of $V_{STARTUP}$. Once the system has reached the stable point, M_9 is switched off. However, a subthreshold current will still flow. For this reason the transistor should be designed so that at the start up, the current is high enough to accelerate the achievement of the final value. Then, when this part of the circuit is no longer needed, the current should be low enough not to interfere with the rest of the circuit.

2.2 Pre-layout simulations

The adopted sizing aims to optimise the circuits for wearable device applications. In comparison to the design proposed in [13], the W/L ratio has been reduced to minimize power consumption and noise. To characterize the designed component, DC and transient simulations have been performed.

2.2.1 DC analysis

Voltage dependence

Figures 2.3 and 2.4 illustrates respectively, the dependence of the voltage and current reference with respect to input voltage variations. The results show that the line regulation requires a certain voltage supply threshold, meaning that the beta multiplier only works properly after 1.5 V.

Table 2.2 outlines the values obtained considering the range between 1.5V and 5V.

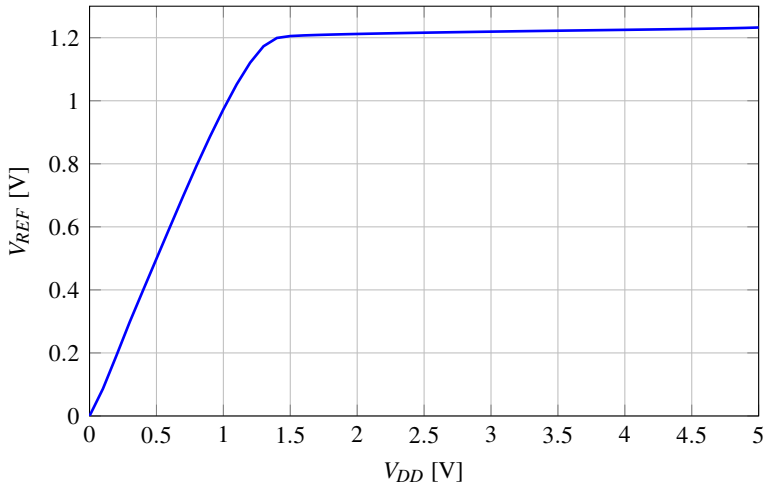


FIGURE 2.3: Voltage reference dependence on the supply voltage

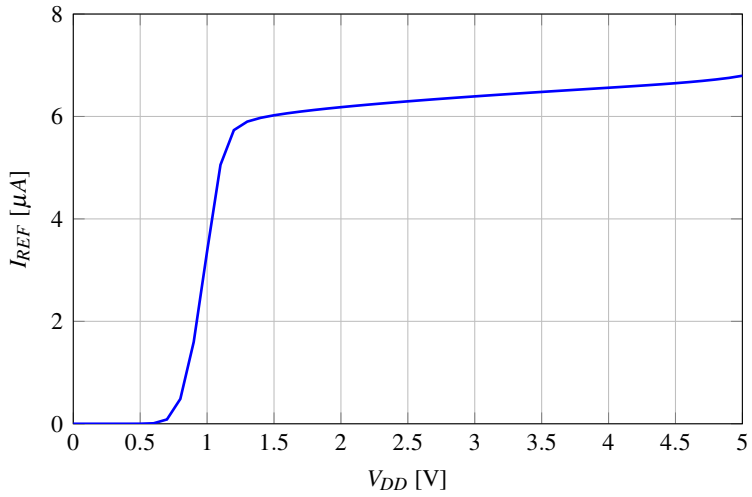


FIGURE 2.4: Current reference dependence on the supply voltage

Temperature dependence

Figures 2.5 and 2.6 depict how the current and voltage references vary with temperature. The range used is for industrial devices to better characterize the component. However, the expected temperature variation is only a couple of degrees.

The computed values of the temperature coefficients are presented in Table 2.2.

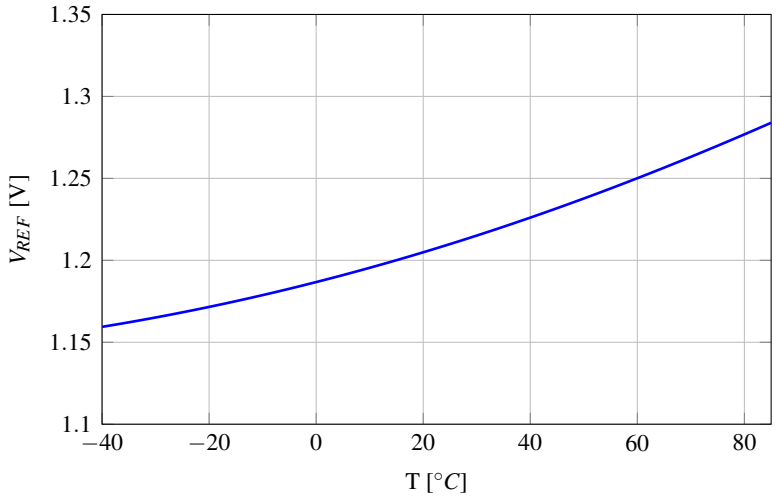


FIGURE 2.5: Voltage reference dependence on temperature

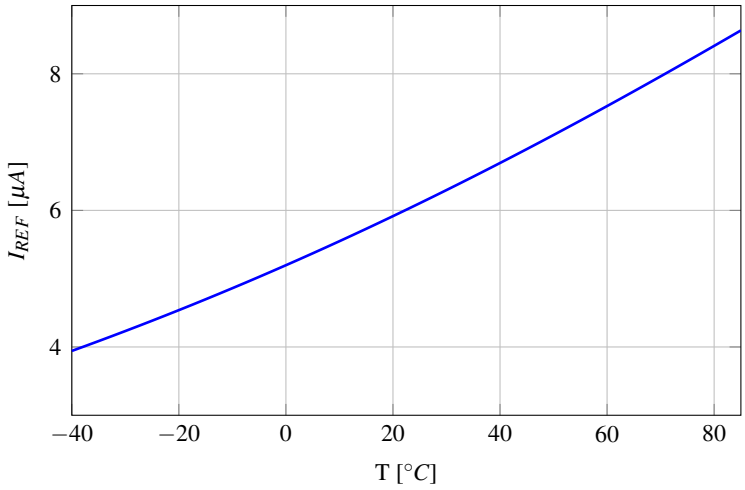


FIGURE 2.6: Current reference dependence on temperature

Variable	Parameter	Value
V_{REF}	Line reg. TC	7.8 mV/V 815 $ppm/°C$
I_{REF}	Line reg. TC	220 nA/V 5971 $ppm/°C$

TABLE 2.2: Summary of line regulation and temperature coefficients obtained from DC analysis

2.2.2 Transient analysis

Figure 2.7 and 2.8 show the transient response to a voltage supply step. The waveform transitions from a low level of 0V to a high level of 3.7 V with a rise time of $1\mu s$ to simulate the behavior of the beta multiplier reference when the system is switched on. In particular, the start-up time is compared with and without the start-up circuit.
It is evident that including this component, the time required to reach the nominal value is significantly reduced. The time scale has been expanded in Figure 2.9 to effectively show the actual amount of start up time required without the enhancing component.
The numerical values derived from the graphs are reported in Table 2.3. The parameter was measured considering the duration from when the circuit is switched on to when it reaches and remains within $\pm 1\%$ of the final value.

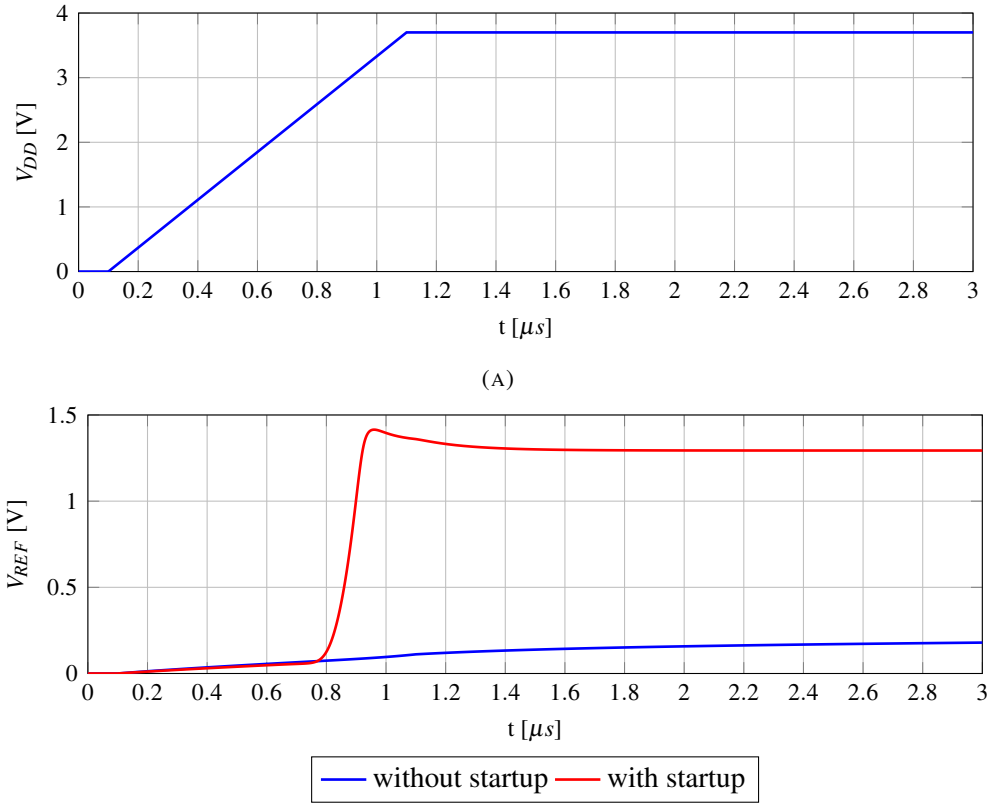


FIGURE 2.7: Transient response at start up: (a) Voltage supply; (b) Voltage reference with and without startup circuit

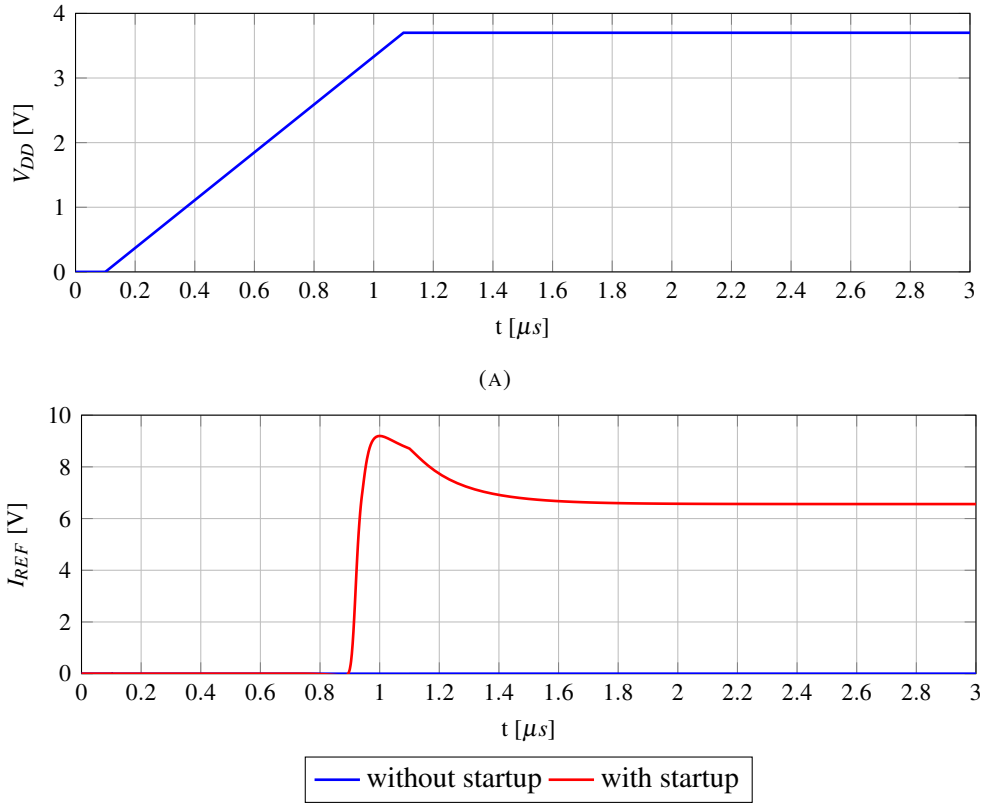


FIGURE 2.8: Transient response at start up: (a) Voltage supply; (b) Current reference with and without startup circuit

Implementation	Startup Time	
	V_{REF}	**I_{REF}**
with start up	1.2 μs	1.6 μs
without start up	1.9 ms	1.9 ms

TABLE 2.3: Comparison of startup time pre and post startup circuit obtained with transient analysis

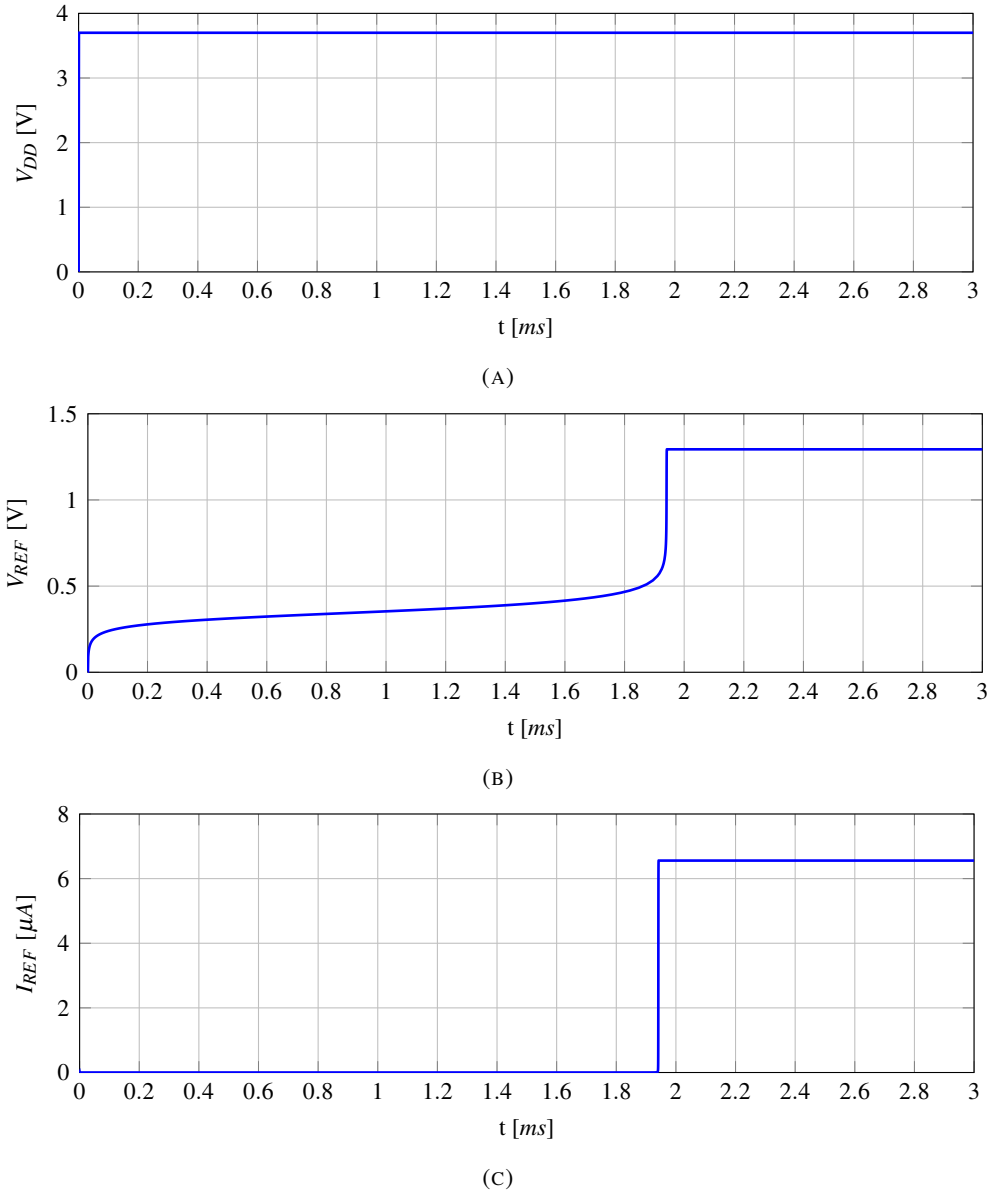


FIGURE 2.9: Transient response at start up without startup circuit: (a) Voltage supply; (b) Voltage reference; (c) Current reference

2.2.3 Process corners

During IC fabrication, factors such as temperature, pressure and chemical composition can introduce uncertainty into the design parameters of the circuit. These variabilities are systematic and affect all the transistors on a single wafer. For this reason, they are also referred to as inter-die variations. Deviations from nominal values in variables such as channel length, channel width, gate oxide thickness, resistivity, doping concentration and body effect may influence the device's expected performance.[14] In some cases, these systematic variations could jeopardise the circuit's correct operation. To verify the extent of these variations, it is important to perform a worst-case analysis considering the worst-case fluctuations in an IC process. Four process corners can be identified: SS, which corresponds to slow nMOS and pMOS; FF, which corresponds to fast nMOS and pMOS; SF, which corresponds to slow nMOS and fast pMOS; and FS, which

corresponds to slow pMOS and fast nMOS. The circuit's correct behaviour is verified in all four conditions before proceeding with the layout step. [15]

Figure 2.10 illustrates the line regulation for the voltage and current references in the five process corners including the typical one (TT). The results demonstrate the robustness of the beta multiplier across all conditions.

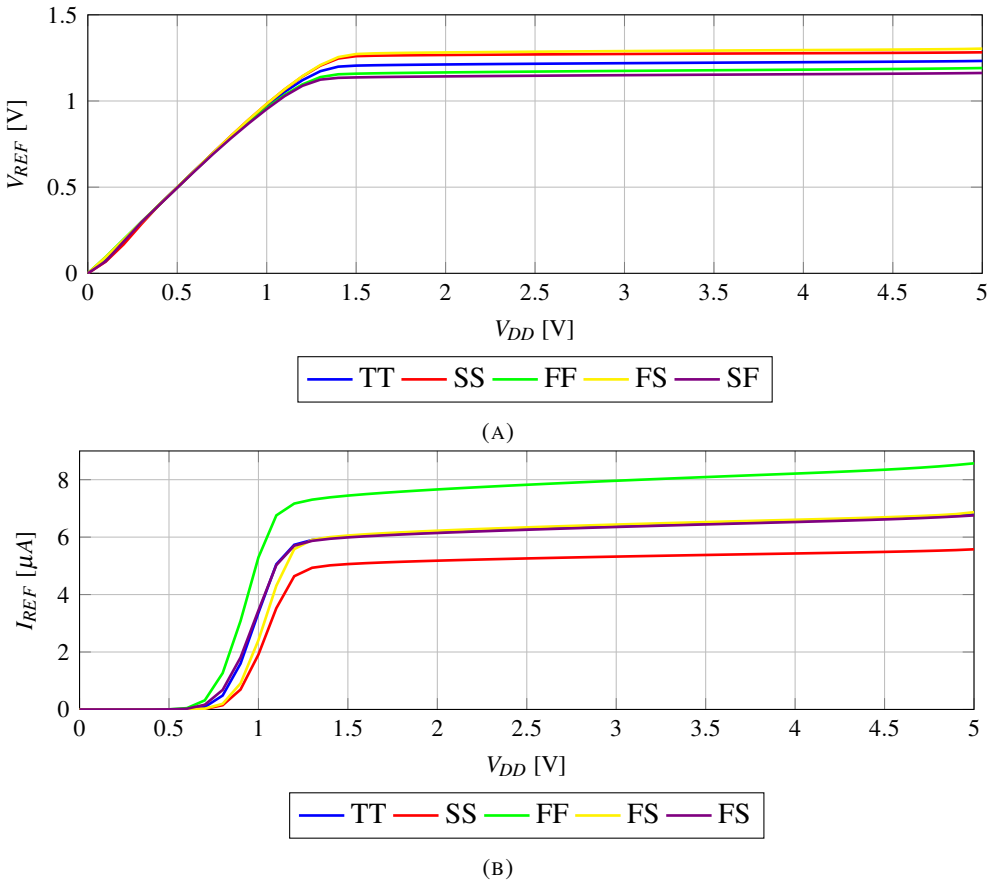


FIGURE 2.10: Line regulation for all the process corners: (a) Voltage reference; (b) Current reference

Variable	Variation	Value	Percentage	Process corner
V_{REF}	max	1.29 V	+5.7%	SF
	min	1,15 V	-5.7%	FS
I_{REF}	max	8.1 μA	+25%	FF
	min	5.4 μA	-17%	SS

TABLE 2.4: Worst case performance of current and voltage references at $V_{DD} = 3.7V$

2.3 Layout

Figure 2.12 shows the realised layout of the beta multiplier reference.
During IC fabrication, the processes used to produce the die can create discrepancies between the layout's elements. These mismatches fall into two categories: absolute, which affect all elements in the same way; and differential, which involve random variations between closely placed elements. The latter are the most difficult effects to reduce, and they significantly influence the performance of analog circuits, especially highly sensitive ones.[16] Several techniques aim to limit the impact of local variations:

- **Clustered layout**: grouping all the elements of the same type together (e.g. AABB). This scheme is most sensitive to process gradients and is commonly used when matching is not critical
- **Interdigitated layout**: elements are alternated (e.g. ABAB). This scheme effectively compensates for one-dimensional process gradients
- **Common-Centroid layout**: symmetric disposition with respect to a geometric center (e.g. ABBA). This scheme is suitable for two-dimensional process gradients

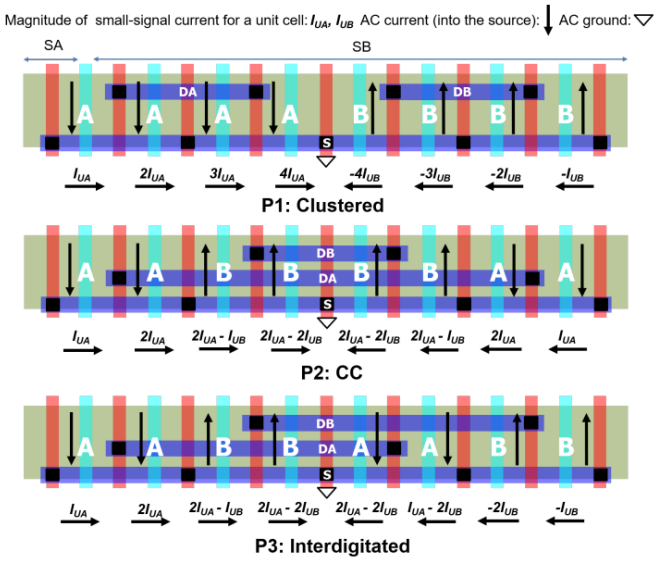


FIGURE 2.11: Clustered, CC, and ID layouts with routing connections [16]

Of these three schemes, the common-centroid layout is the most suitable for this application, as it averages local variations on both the x and y axes, ensuring an optimal match.[16] The number of transistors used in the design has been set to facilitate the adoption of this technique, and additional dummy devices have been placed on both edges of each line to enhance matching. Furthermore, guard rings are implemented to suppress substrate noise produced by other elements and isolate the transistors providing a low impedance path to ground.

Four types of metal have been used to optimise performance interconnection: Metal 1 (M1) and Metal 2 (M2) are used for very short connections; Metal 3 (M3) is used for horizontal connections; and Metal 4 (M4) is used for vertical connections. Directional staggering ensures efficient signal routing since it allows the metal strips to cross on different layers.

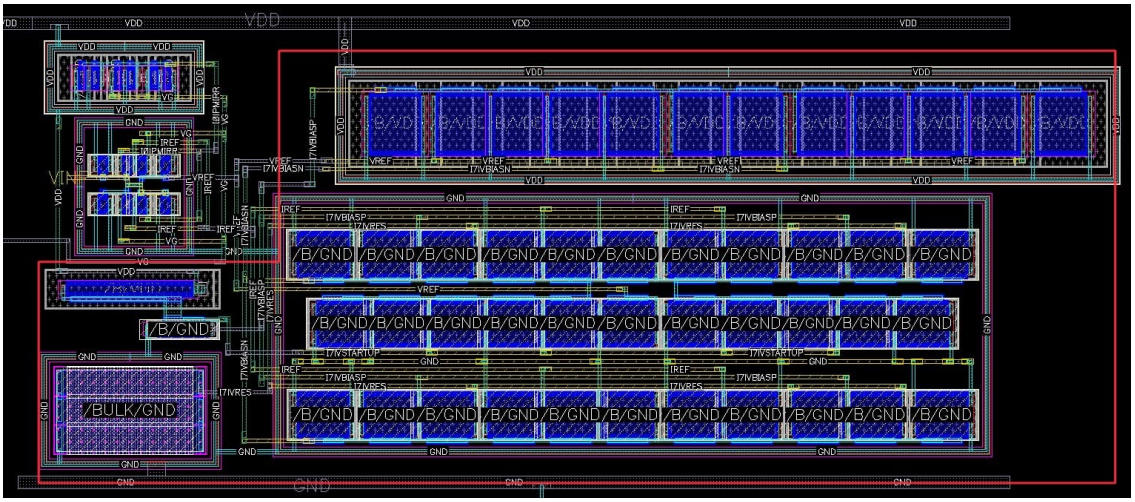


FIGURE 2.12: Layout of beta multiplier reference (red box)

Once the layout has been created, it is mandatory to perform the following verifications to ensure the manifacturability of the integrated circuit:

- **DRC (Design Rule Check)**: verifies compliance with the DRM (Design Rule Manual), which specifies technological rules such as distances and thicknesses
- **LVS (Layout vs Schematic)**: checks the accordance between the layout and the schematic
- **PEX (Parasitic Extraction)**: extracts parasitic capacitances and resistances

2.3.1 Post layout simulations

DC and transient analysis have been performed to assure consistency with the pre-layout results.

DC analysis

Voltage dependence Figures 2.13 and 2.14 show the line regulation for the current and voltage references, respectively. As expected, the parasitic resistances cause the values to differ slightly from the pre-layout simulations: the voltage increases while the current decreases.
From the computed parameters summarized in Table 2.5 it is possible to notice that the line regulation is marginally decreased.

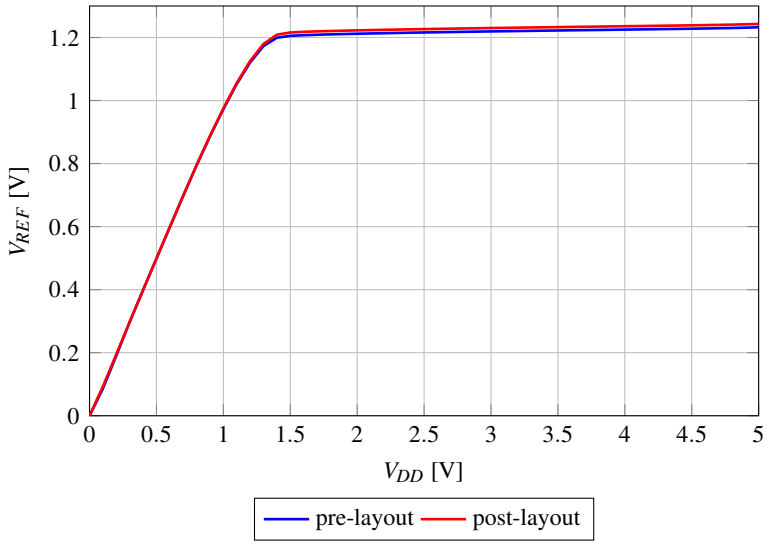


FIGURE 2.13: Comparison of voltage reference line regulation pre and post layout

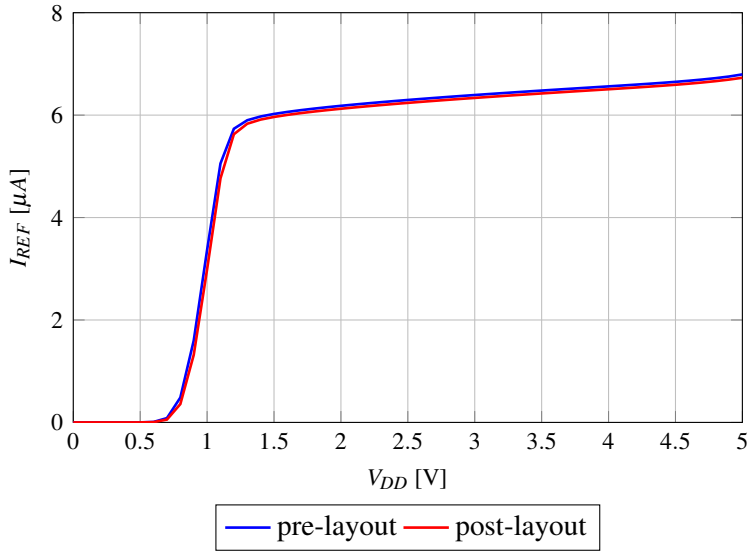


FIGURE 2.14: Comparison of current reference line regulation pre and post layout

Temperature dependence Figures 2.15 and 2.16 show the dependence of voltage and current reference respectively.

Table 2.5 presents the temperature coefficients (TC) obtained from the graphs; the value of the parameter is minimally reduced.

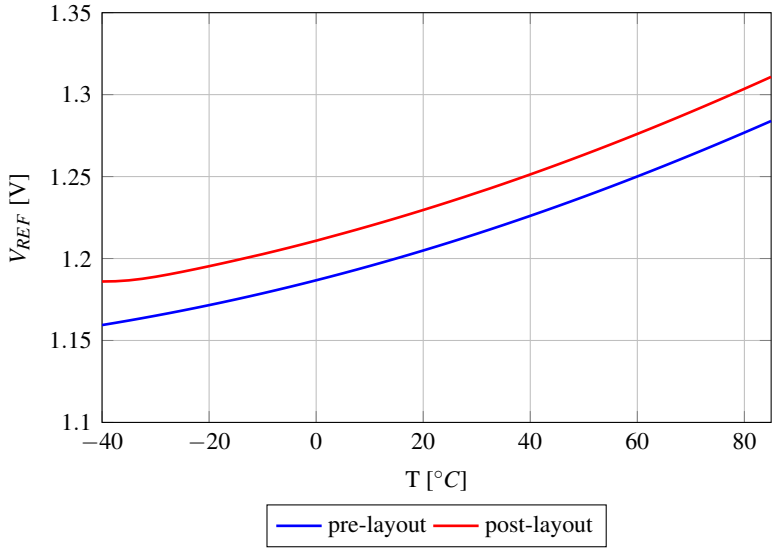


FIGURE 2.15: Comparison of voltage reference dependence on the temperature pre and post layout

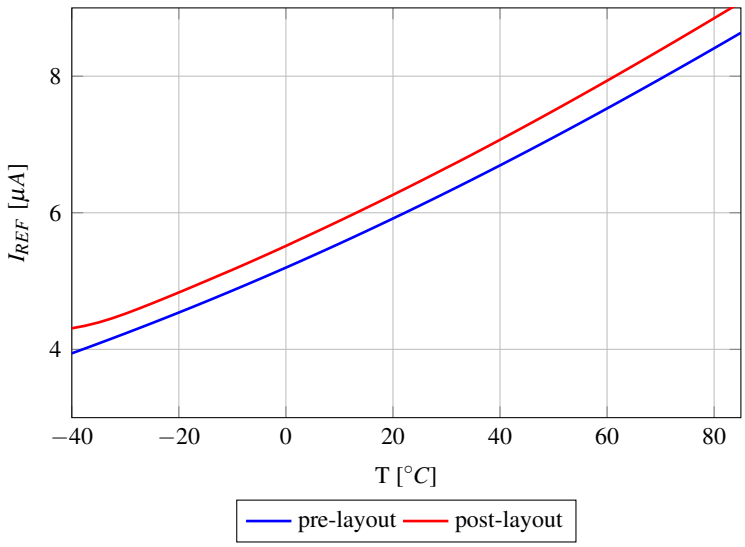
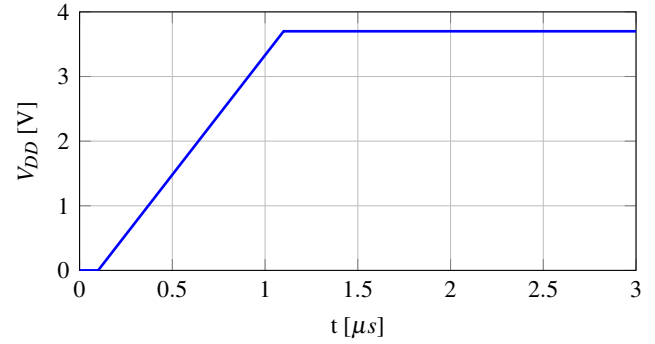


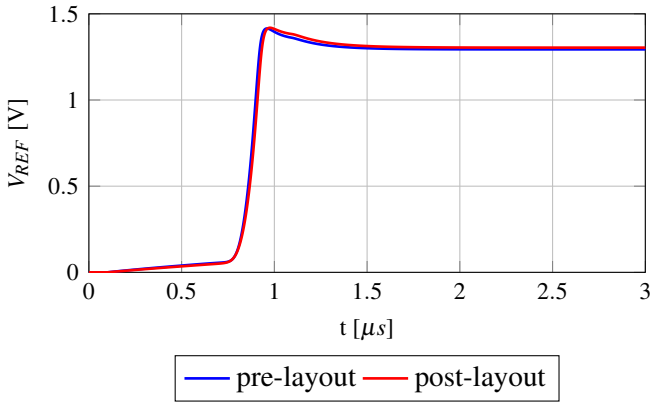
FIGURE 2.16: Comparison of current reference dependence on the temperature pre and post layout

Transient analysis

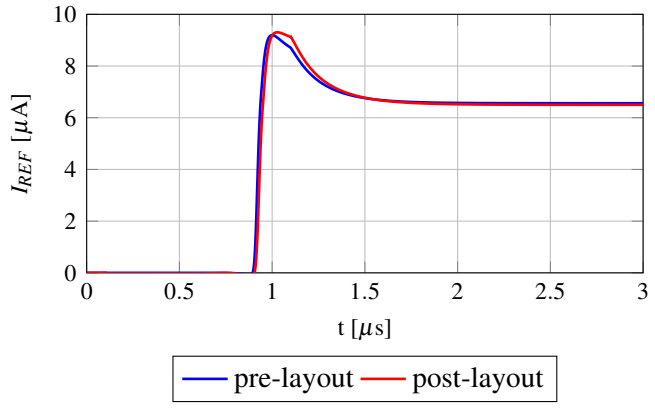
Figure 2.17 shows the behavior resulting from a voltage supply step. The waveform rises from 0 V to 3.7 V in 1 μs. Due to the parasitic capacitances, the start up time increases, as reported in Table 2.5.



(A)



(B)



(C)

FIGURE 2.17: Comparison of transient response at start up pre and post layout: (a) Voltage supply; (b) Voltage reference; (c) Current reference

Parameter	Variable	Pre-layout	Post-layout
Line reg.	V_{REF}	7.8 mV/V	7.7 mV/V
	I_{REF}	220 nA/V	218 nA/V
TC	V_{REF}	815 $ppm/^{\circ}C$	800 $ppm/^{\circ}C$
	I_{REF}	5971 $ppm/^{\circ}C$	5705 $ppm/^{\circ}C$
Start up time	V_{REF}	1.2 μs	1.3 μs
	I_{REF}	1.6 μs	1.7 μs

TABLE 2.5: Comparison of performances of beta multiplier pre and post layout

Montecarlo analysis

Intra die variations can be modelled with statistical distributions to represent their random, spatially correlated nature.[16]

Monte Carlo simulations can be used to verify both global and local variations. With regard to corner analysis, which represents the worst-case scenario, this type of analysis provides a statistical overview of how the circuit behaves, allowing to estimate the yield.

Figures 2.18 and 2.19 depict the current and voltage reference obtained from the Monte Carlo analysis at 3.7 V and using 5000 samples.
The current reference has a mean value of 6.22 μA and a standard deviation of 0.45 μA, while the voltage reference has a mean value of 1.21 V and a standard deviation of 34 mV.

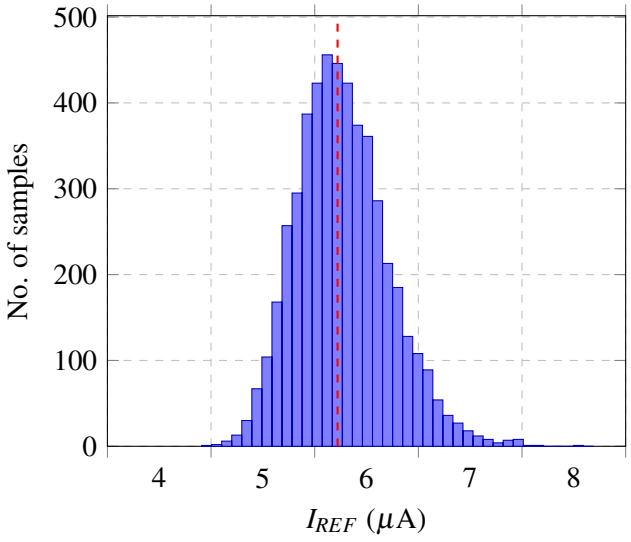


FIGURE 2.18: Monte Carlo analysis of I_{REF}. The standard deviation σ is 0.45μA and the dispersion $3\sigma/\mu$ is equal to 22%.

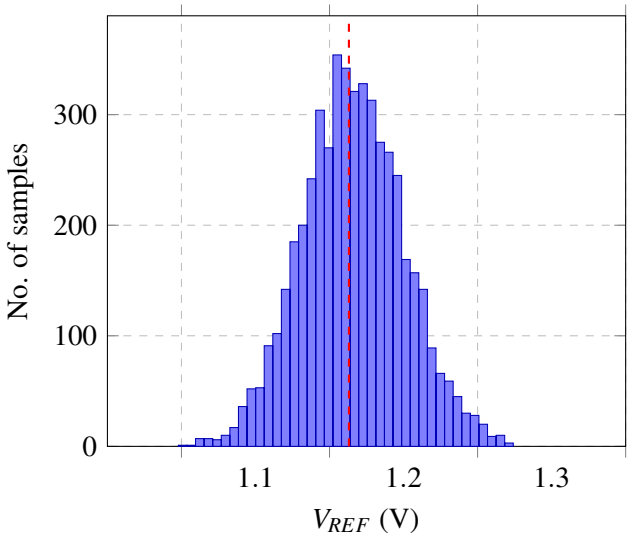


FIGURE 2.19: Monte Carlo analysis of V_{REF}. The standard deviation σ is 34 mV and the dispersion $3\sigma/\mu$ is equal to 8.5%.

2.3.2 Final considerations

The results of the simulations confirm that the design is suitable for the intended application. The component achieves a small footprint and low power consumption, while ensuring optimum voltage and current regulation. Furthermore, the Monte Carlo simulation performed after the layout was finalized validates the robustness of the architecture against global and local process variations.

Chapter 3

Design and analysis of the low dropout (LDO) regulator

3.1 Power management system

Technological advancements have resulted in scaled devices, increasing the density of transistors per die, as predicted by Moore's law. This trend has facilitated the integration of a greater number of features, expanding the range of applications for integrated circuits. Consequently, this has enabled the invention of devices that were not conceivable two decades ago. However, electronic designers have to face new challenges related to scaled devices: power consumption have become an issue of paramount importance. While the dimensions of the transistors are decreasing, the conventional battery technology is not progressing in a similar manner, with no equivalent reduction in size. Therefore, efficient power management is required to heavily limit dynamic and leakage power. [17]

In the domain of wearable devices, which are conventionally powered by a battery, this issue assumes even greater significance. It is evident that, in consideration of the operational mechanisms of these devices, two primary functional modes can be delineated. Firstly, the run mode, where the system performs a measurement and operates with the peak energy consumption. Secondly, a sleep mode characterised by the device's minimal activity and where power consumption is dominated by the leakage and quiescient current.
This suggests the necessity for a power management module that is capable of delivering the requisite power to the system's components, switching between operational modes, and efficiently conditioning the electrical signal when energy harvesting sources are employed.

In order to accomplish the aforementioned tasks, power management integrated circuits (PMICs) offer a wide range of features, including voltage regulators, battery chargers, and power management control algorithms. They also handle failure cases such as overcurrent or overheating with dedicated modules for monitoring and protection.

This variety of components is characterised by its versatility, which enables its deployment across a multitude of applications. Consequently, the modules available on the market are either general-purpose or tailored for a particular field of application. In the context of wearable devices, the implementation of a power management system that executes only the required functions is crucial. This is due to the fact that it prevents energy and area wastage, both of which are aspects of fundamental relevance for this kind of application. It is evident that the utilisation of an ASIC (Application-Specific Integrated Circuit) inevitably incurs a higher manufacturing cost. However, this is a justifiable drawback when considered against the advantages offered by a highly efficient module.

Being a key module in a device, PMICs have to satisfy several requirements:

- **Size, volume, footprint, and weight**: following the trend of miniaturisation, the component should be as small and lightweight as possible
- **Power conversion efficiency**: this parameter can be expressed as:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{in} + P_{loss}} \tag{3.1}$$

  where P_{out} is the power transferred to the load, P_{in} is the input power and P_{loss} is the power dissipated. Ideally, P_{loss} should be equalt to 0; in this case all the input power would be delivered to the load and the efficiency would be maximum ($\eta = 1$). A high power efficiency increases the battery life-time, which implies an extended autonomy for a wearable device.
- **Reliability, no disturbances, and low noise**: these modules must maintain stable operation under various environmental and electrical conditions, including temperature fluctuations and input voltage variations. The power delivery must exhibit high signal integrity to ensure that noise and ripple do not degrade the performance of sensitive circuitry. Furthermore, the circuit must possess an excellent load transient response, maintaining the regulated output voltage constant despite sudden changes in load current.
- **Cost**: this is an important factor to consider when designing a product for the market. Integrated circuits, such as PMICs, play a key role in reducing the overall product costs by minimizing the need for numerous bulky external components.

[18]

Voltage regulators are an essential component of a PMIC. They are used to convert the voltage from the source to the required level at the load.
Voltage regulators can be mainly categorized in:

- **Switching regulators (DC-DC converters)**: these regulators are well-known for their high power efficiency, adjustable output voltage and high driving capability.
  The basic components include two switches that operate in antiphase and must not be on at the same time to avoid energy loss or potential damages. A control module is used to alternate the configuration of the switches to deliver the required voltage to the load. To filter the high frequency harmonics produced by the switching operation, a low pass filter is implemented.
  The conversion ratio is the ratio between the output voltage and the input voltage. It depends on the duty cycle (D) that can be defined as the time the primary switch is on over the total switching period.
  Three main switching regulators can be defined based on the type of conversion (Figure 3.1). The buck regulator performs step down conversions, meaning that V_{out} is lower than V_{in}, while the boost converter performs the opposite operation: from a low V_{in} a high V_{out} is obtained. Buck/Boost converters on the other hand, can behave as either a buck or a boost converter, depending on the value of the parameter D.
  Switching converters provide high power efficiency, normally around 80/90 %, but the drawback is that the voltage supplied to the load is not noise free, due to the ripple voltage caused by the conversion process. For this reason, switching converters alone are not suitable for sensitive circuits. Moreover the components used for the low pass filter (inductors and capacitors) can occupy a significant amount of area.

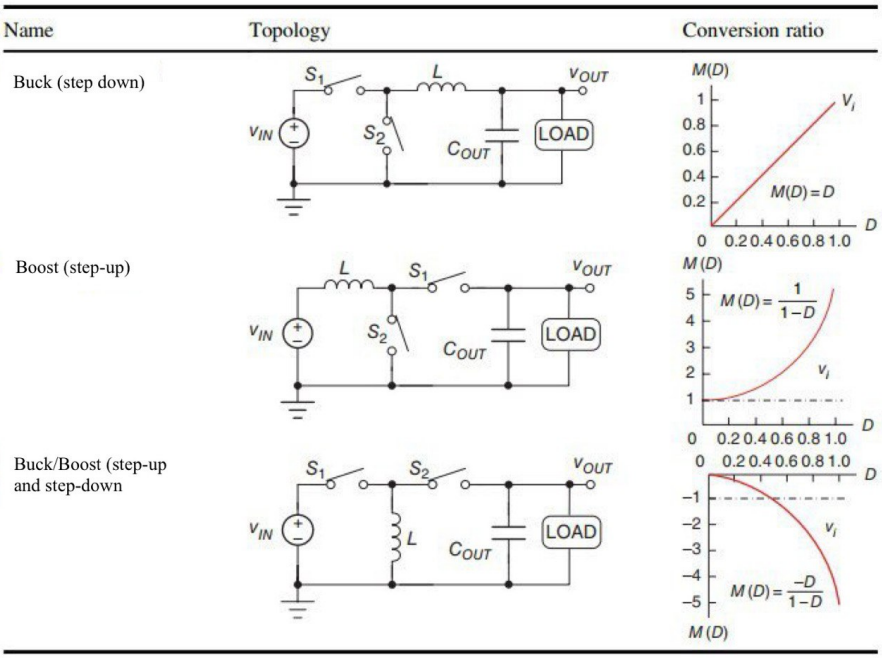


FIGURE 3.1: Summary of the three basic inductor-based SWR topologies [19]

- **Linear Regulators (Low dropout regulators)**: LDO regulators are composed of an error amplifier, a pass transitor and a resistive partition (see Figure 3.2). When the difference between the input and output voltages is high, most of the power is dissipated in the pass transistor, resulting in poor power efficiency. Conversely, the feedback loop enables excellent load and line regulation, ensuring a stable voltage is delivered to the load in different circumstances. Features such as low noise, a fast transient response, low quiescent current and a small footprint make these electronic components a good choice for wearable applications.

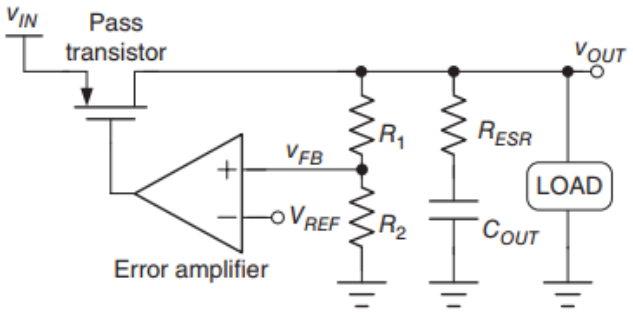


FIGURE 3.2: Structure of basic LDO regulator [19]

When area and power consumption are not stringent requirements, a two-stage regulation architecture can be implemented to exploit the respective advantages of both types of regulators. First, the switching regulator is used to efficiently convert most of the power. Then, the LDO is placed in series to effectively reduce the ripple and switching noise produced by the former while maintaining acceptable overall power efficiency.

3.2 Low Dropout (LDO) regulators

3.2.1 Specifications

When designing an LDO regulator, several specifications have to be taken into account:

- **Steady-state characteristics**:
  - *Dropout voltage*:this parameter is defined as the difference between the supply voltage and the regulated output voltage when the latter is decreased of approximately 2% of its nominal value.
    Figure 3.3 shows the variation of the output voltage V_{OUT} as a function of the supply voltage V_{IN}. Three different regions can be defined. In the regulation region, the LDO provides optimal performance, ensuring a stable output voltage with respect to input voltage variations. In this region, the pass transistor is in saturation and acts as a variable resistor to dissipate the excess voltage. The dropout region is characterized by the pass transistor's entry into the triode region due to an insufficient V_{DS}. In this state, the LDO loses its ability to regulate, and V_{OUT} begins to drop as V_{IN} is further reduced. At a certain point, the value of V_{IN} is insufficient to sustain the required current flow, causing the LDO to enter the off region, where the output voltage drops to zero.

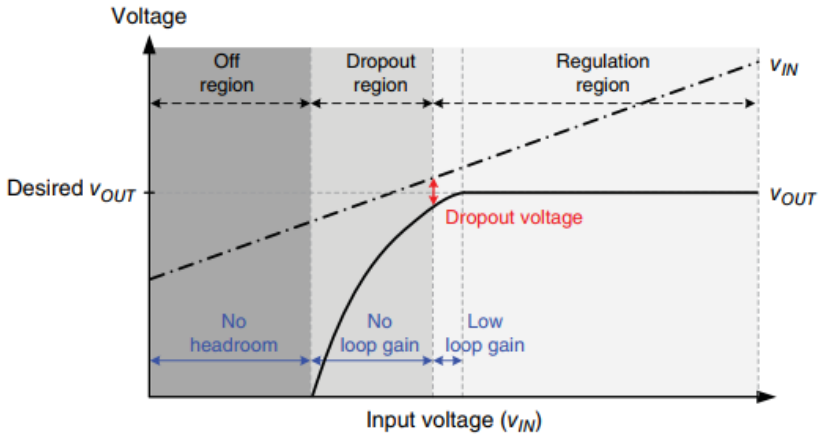


FIGURE 3.3: Characteristic curve of input voltage and output voltage that defines the dropout voltage $V_{dropout}$ [19]

  - *Efficiency*: the power conversion efficiency is defined as the ratio between the output power and the input power:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} I_{LOAD}}{V_{IN} I_{IN}} \tag{3.2}$$

    The current I_{IN} can be expressed as:

$$I_{IN} = I_{LOAD} + I_Q \tag{3.3}$$

    where I_Q is the quiescient current that includes the biasing current of the error amplifier, the bandgap reference and the feedback resistance network.

Therefore the power conversion efficiency can be expressed as

$$\eta = \frac{I_{LOAD}V_{OUT}}{(I_{LOAD}+I_Q)V_{IN}} = \eta_I \cdot \eta_V \tag{3.4}$$

which under heavy loads can be expressed only as η_V because I_q becomes negligible. Under light loads, however, the value of I_q is significant, representing most of the power consumed in sleep mode and influencing battery lifetime.

– *Line regulation*: this parameter is defined as the output voltage variation in case of input voltage variation, computed in the regulation region (Eq. 3.5). Line regulation is deteriorated approaching the dropout region.

$$\text{Line regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \tag{3.5}$$

– *Load regulation*: this parameter is determined by the output voltage variation with respect to the load current variation.

$$\text{Load regulation} = \frac{\Delta V_{OUT}}{\Delta I_{LOAD}} \tag{3.6}$$

Increasing the load current, the gain is reduced. This results in a lower regulation which is evident when comparing the output voltage for light and heavy loads.

– *Temperature coefficient (TC)*: this parameter is defined as the relative change in the output voltage over the temperature variation and is usually expressed in parts per million (ppm):

$$TC = \frac{\Delta V_{OUT}}{V_{OUTmean}\Delta T} \cdot 10^6 \tag{3.7}$$

– *Maximum/minimum load current*: permits to identify the operational window of the LDO. The maximum load current is the highest current that the pass transistor can supply while keeping the component within the regulated range. The minimum load current represents the limit condition for maintaining stability and providing the required performance.

– *Quiescient current*: represented by the bias current of the entire system, this specification is determinant for the power consumption. It also affects the loop gain and bandwidth of the voltage regulator, and consequently its stability.

- **Dynamic characteristics**:

– *Load transient variations*: Figure 3.4 shows the output voltage response in case of an abrupt current load variation. When the latter transitions from a light load to a heavy one, V_{OUT} drops and four different segments can be identified. The first segment, characterized by the voltage variation V_1 is due to the Equivalent Series Inductance (ESL) of the output capacitor (in the case of pole dominant configuration). This value can be expressed as:

$$V_1 = ESL\frac{di}{dt} = ESL\frac{I_{LOAD(heavy)} - I_{LOAD(light)}}{T_{rise}} \tag{3.8}$$

$V2$ is caused by the ESR of the output capacitor and is computed as

$$V_2 = ESR(I_{LOAD(heavy)} - I_{LOAD(light)}) \tag{3.9}$$

The upward voltage peak V_3 is induced by the ESL once the current load has reached the $I_{LOAD(heavy)}$ value. Lastly, $V4$ depends on the slew rate of the power amplifier and on the gate capacitance of the pass transistor. The drop period Δt_1, which is the time needed to reach the maximum negative peak, can be expressed as:

$$\Delta t_1 = \frac{1}{BW_{cl}} + t_{sr} \tag{3.10}$$

where BW_{cl} is the closed loop bandwidth, and $t_{sr} = C_{par}\frac{\Delta V}{I_{sr}}$ where C_{par} is the gate capacitance of the pass transistor and I_{sr} is the bias current of the error amplifier. Δt_3 is determined using the same equation but results in a different value since the bandwith is different in the case of light and heavy load.
The settling time depends on the bandwidth and the phase margin. Furthermore, the value of the output voltage differs at heavy and light load due to the load regulation.
The value for overshoot and undershoot can be calculated as:

$$\Delta V_{tr,max} = \frac{I_{LOAD(heavy)} - I_{LOAD(light)}}{C_{OUT}} \cdot \Delta t_1 (or \Delta t_3) + \Delta V_{ESR} \tag{3.11}$$

In case of light to heavy load variation, the output capacitor supplies the difference before the amplifier's feedback loop has stabilised and controlled the pass transistor in order to provide the required current. Conversely, when the load current transitions from a heavy to light value, the surplus charges can be stored in the capacitor.
The feedback resistive path determines the rate at which the overshoot is discharged.

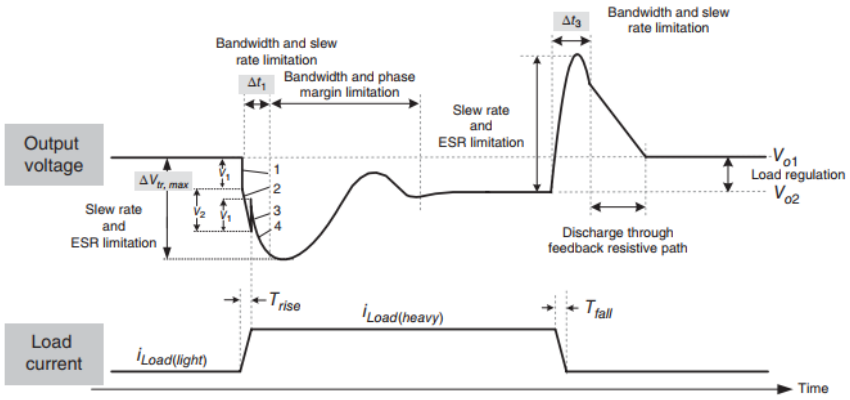


FIGURE 3.4: Load transient response in case of a load current change [19]

– *Line transient variations*: when the supply voltage transitions from a low value to a high value, the output voltage experiences a temporary overshoot. This occurs because the feedback loop reacts with a delay to the sudden change in the supply voltage causing the pass transistor to deliver more current than required. Conversely, when the supply voltage transitions from a high value to a low one, the output voltage experiences a temporary undershoot because the feedback loop is too slow to reduce the resistance of the pass transistor, which momentarily delivers a lower current than necessary to the load.

– *Transient recovery time*: in the case of a transient variation (either load or line), this parameter indicates the time necessary for the output voltage to return and settle within a specified boundary of $\pm 1\%$ of the nominal value.

– *Phase margin (PM)*: this parameter determines the stability of the frequency response and affects the transient recovery time. The phase margin can be computed as:

$$PM = 180^\circ + \phi_{loop} \quad (at\ f = f_c) \tag{3.12}$$

where f_c is the crossover frequency, this is the frequency at which the open loop gain is equal to 0 dB (unity gain). The system is considered unstable if the phase margin is negative and the gain is greater than zero. For an LDO, an acceptable value is tipically PM > 45° even if the system is considered stable for lower values (see Figure 3.5). This higher requirement is necessary because a smaller PM leads to a less damped response. This dynamic behavior results in significant ringing and a longer settling time, which compromises system reliability and can potentially damage the connected load.

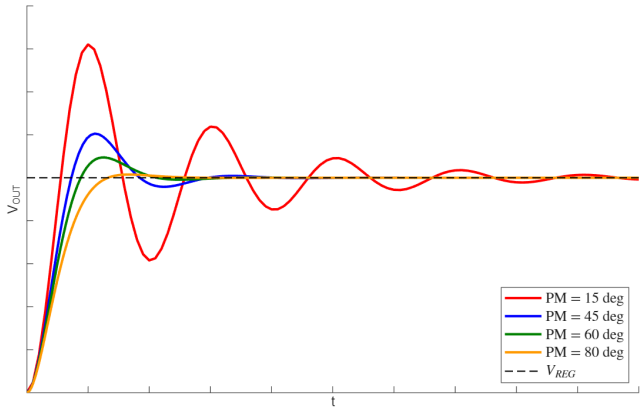


FIGURE 3.5: Transient output voltage for different values of phase margin (PM)

– *Unity Gain Frequency (UGF) and Bandwidth (BW)*: the UGF determines how the system responds to transient variations. A higher value implies a shorter transient recovery time because the feedback loop is faster.
The bandwidth is defined as the frequency at which the gain reduces by 3 dB from its maximum DC value. This parameter represents the frequency range for which the regulator can correct errors with the highest efficiency and accuracy.

– *Power Supply Rejection Ratio (PSRR)*: it measures the efficiency with which the LDO suppresses power supply ripple at different frequencies. It can be calculated by dividing the ripple voltage present at the input by the ripple voltage resulting at the regulated output:

$$PSRR = 20log\left|\frac{1}{A_p}\right| = 20log\left|\frac{v_{in}}{v_{out}}\right| \tag{3.13}$$

3.2.2 LDO operating principle

As mentioned in Section 3.1, the main components of an LDO regulator include the resistive ladder, the error amplifier and the pass transistor. These three elements, adequately connected, ensure output voltage regulation under different environmental and electrical conditions.
The pass transistor is the element that connects the input voltage and the output voltage. A PMOS is usually implemented because this configuration allows for the lowest dropout voltage compared to other topologies like NMOS or Darlington, which could permit higher driving capability.
The lower the dropout voltage, the higher the power conversion efficiency. Still, this voltage must be limited, since to decrease the dropout voltage, the size of the power mos has to be increased. This increase translates to a higher parasitic gate capacitance, which in turn can slow down the transient response or even cause system instability. Besides, this choice also occupies a greater area.
The error amplifier is another fundamental component which determines the velocity of the dynamic transient response. This parameter, in fact, is affected by the loop gain, bandwidth, phase margin and slew rate, which directly depend on the amplifier's characteristics. Once again, these specifications are strictly bound together; while striving to optimize one, one must be careful to avoid the deterioration of another. A high bandwidth is optimal if the target is decreasing the transient recovery time but the stability of the system could be affected.
Finally, the resistive ladder influences the loop gain, and the value of the resistances determines the quiescient current. The latter increases the bandwidth, but at the cost of a higher power consumption. Due to the presence of the feedback loop, these three elements efficiently maintain a stable voltage at the output. If a perturbation is present, it is reflected in the voltage difference $V_{REF} - V_{FB}$ which results in a different output voltage of the error amplifier. The latter drives the power MOS, which in turn delivers the correct current to the load, thereby counteracting the perturbation.

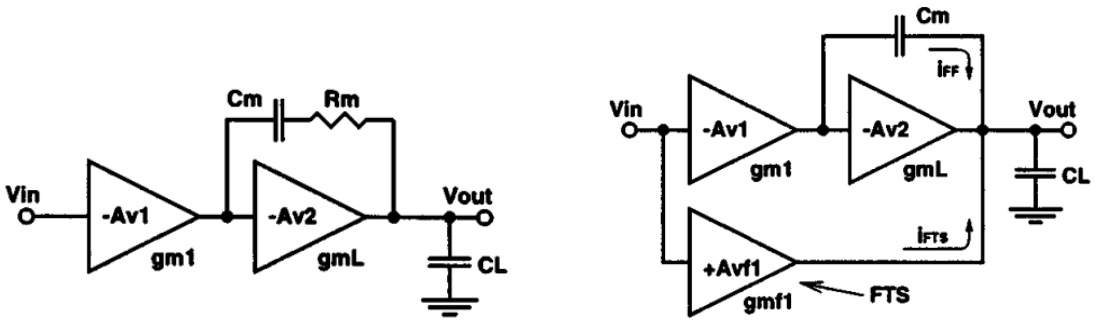
3.2.3 LDO classification

LDO regulators can be divided in two categories according to their controlling method: analog LDO (A-LDO) and digital LDO (D-LDO).
D-LDOs can be easily integrated in SoCs and present high regulation performance. However, their bandwidth is limited by the sampling frequency and clock latency. Conversely, while A-LDOs may have slightly higher operational quiescient current, they offer superior continuous-time response speed.
A-LDOs, in turn, include compensation techniques to accomplish stability and enhance the bandwidth. Based on the method implemented to reach stability, A-LDO can be divided into:

- **Dominant pole compensation LDO**: this technique involves adding an off-chip large capacitor at the output of the voltage regulator. Therefore, the output node becomes the dominant pole of the system. This solution guarantees a high phase margin at the cost of a reduced bandwidth which translates into slow transient response. However, since the large capacitor supplies all the current needed during the transitions, there is no need for a high gain amplifier. Thus the power consumption is limited due to the low quiescient current, though at the expense of a large area occupation.

- **Capacitor free LDO**: in this case, sophisticated internal compensation techniques are applied. Among the most popular solutions figures the insertion of a buffer at the output of the error amplifier, which decouples the output pole and the pole at the input of the power MOS. This pole is at low frequency due to the high gate capacitance of the pass transistor and the high output resistance of the error amplifier. Adding the buffer, two poles at high

frequency are created and the dominant pole of the system becomes the output node. [19]
Other techniques involve the implementation of a capacitor between two nodes (Miller capacitor), to exploit the Miller effect and shift the pole position.
The inclusion of the Miller capacitance could be a source of instability since it adds a feedforward small signal current which originates a right half plane (RHP) zero. To overcome this issue, a nulling resistor could be added in series with the Miller capacitance, thereby eliminating the unwanted zero. However, the choice of the resistor could be not adequately accurate to effectively compensate for the zero. A safer option is using a feedforward transconductance stage which produces a small signal current to cancel the feedforward small signal current.
Several solutions combinations of this methods are available, based also on the numer of stages of the amplifier. When choosing the number of stages one should be careful because a higher number of stages doesn't imply better performances: exceeding the three stages, the circuit becomes more complex due to the added compensation techniques to keep stability and the power consumption increases. Moreover the bandwidth can even be reduced. [20] The capacitorless LDOs are suitable for SoC integration, occupying less area than the dominant pole counterpart. Furthermore, these regulators are characterized by fast transient response, due to the higher bandwidth, which is typically achieved at the expense of a slightly higher quiescent current.



(A) (B)

FIGURE 3.6: Frequency compensation topologies: (a) Single Miller Capacitor with Nulling Resistor (SMCNR); (b) Multipath zero cancellation (MZC) [20]

3.2.4 State of art

Capacitor-less LDO (CL-LDO) implementing local positive feedback tenchnique (LPFB)

Figure 3.7 shows the schematic of the proposed capacitor less LDO (CL-LDO). It adopts a single stage error amplifier and produces a negative resistance that effectively increases the loop gain. The LPFB consists of an input differential amplifier, the folded transistor, an adaptive biasing circuit and a local common mode feedback. [21] The positive feedback loop is formed by the current mirror transistors M_{15} and M_{16} and the local common mode feedback resistors R_1 and R_2. The differential voltage drives the gates of transistors M_3 and M_4, forming a positive feedback path.

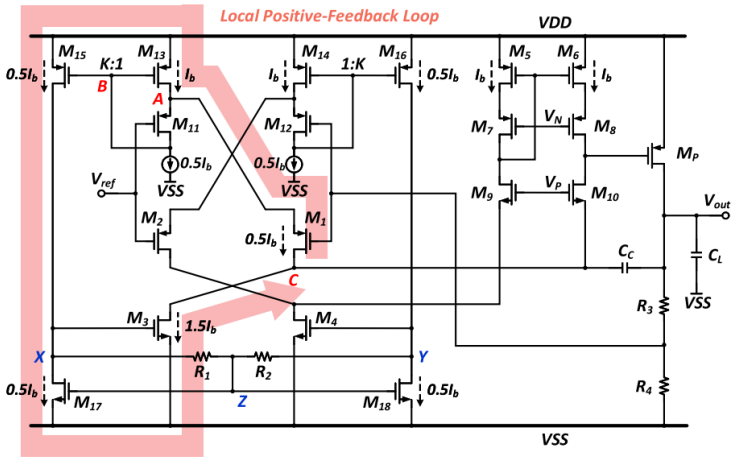


FIGURE 3.7: Schematic of the capacitor-less LDO (CL-LDO) implementing local positive feedback tenchnique (LPFB)[21]

This structure enables the achievement of an improvement in the general performance of the LDO while keeping the area and power consumption limited due to the simplicity of the schematic.

Capacitor less LDO (C-LDO) regulator with an adaptive biased super class AB recycling folded cascode error amplifier

Paper [22] proposes an LDO suited for biomedical implants. The regulator is characterized by an ultra low power consumption and a high and almost constant gain over the load range. The schematic of the circuit, reported in Figure 3.8, employs a two stage super class AB error amplifier, a power MOS as the pass transistors, compensation loops and and adaptive biasing circuit. The passive resistive ladder is substituted by a MOS feedback network. [22]

The area occupation is not mentioned in this paper, but it is reasonable to infer it will be much higher than the previous solution. In this case, low power consumption and high dynamic performances have been traded off for a larger footprint.

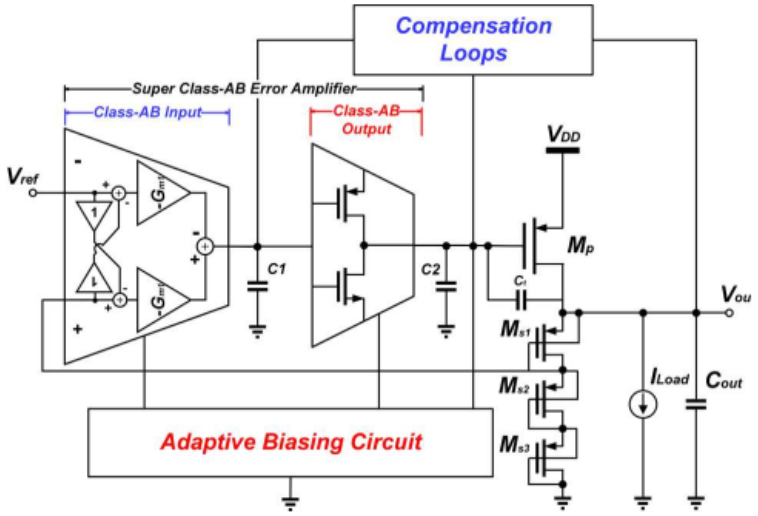


FIGURE 3.8: Schematic of the LDO regulator with an adaptive biased super class AB recycling folded cascode error amplifier[22]

Capacitor-less LDO (C-LDO) with three stage error amplifier and dynamic gain adjusting (DGA) mechanism

Figure 3.9 investigates the performances of an LDO regulator which presents a three stage error amplifier, with a single compensation capacitor and a flying capacitor to enhance the system's stability. The dynamic gain adjusting (DGA) mechanism allows stability for ultra light loads by sensing the the gate voltage of the pass transistor and modulating the R_P resitance which in turn modifies the gain of the first stage.

In the previous solutions, the stability for light loads was primarly guaranteed by the adjusting biasing circuit, which tunes the gain of the amplifier by changing the bias current.

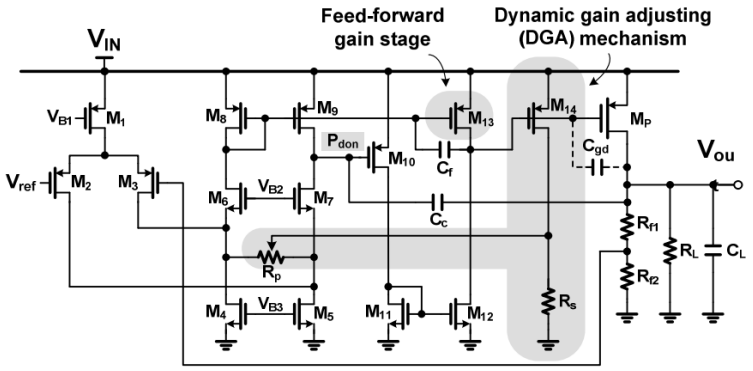


FIGURE 3.9: Schematic of capacitor-less LDO (C-LDO) with three stage error amplifier and dynamic gain adjusting (DGA) mechanism[23]

LDO with hybrid mode operational transconductance amplifier (HM-OTA) as error amplifier and adaptive biasing circuit

Figure 3.10 depicts the schematic of the LDO described in [24]. The voltage regulator present a single stage amplifier. The paper investigates the difference in performance between a DM-OTA, CM-OTA and HM-OTA. The HM-OTA's characteristics are in between the two configurations: the CM-OTA has higher DC gain but exhibits deeper voltage peaks and a slower transient response. Conversely, the DM-OTA is less stable and presents ringing, but it has higher bandwidth, hence a smaller transient recovery time. Moreover, the undershoot and overshoots are reduced.
The adaptive biasing circuit senses the gate voltage of the power pMOS and injects a current proportional to the load into the OTA's tail.

This solution increases the slew rate thereby reducing the undershoot voltage while keeping the quiescent current low.

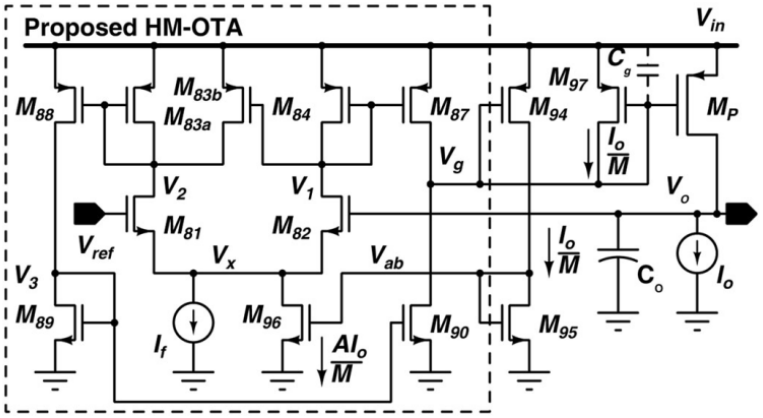


FIGURE 3.10: Schematic of the LDO with hybrid mode operational transconductance amplifier (HM-OTA) as error amplifier and adaptive biasing circuit [24]

Capacitor less LDO with adaptive biased circuit, supply ripple subtraction and pole tracking compensation (PTC)

Paper [25] presents an LDO with a single stage amplifier that includes an adaptive biasing circuit (see Figure 3.11). Moreover pole tracking compensation (PTC) is implemented. This circuit includes a Miller capacitance in series with an adaptive nulling resistor. The latter consists of a resistor in series with a current controlled resistor formed by the transistor M_{C1}. [1]
The PSR of the system is greatly enhanced by implementing a reference buffer with reversed-phase PSR. To understand the working principle, two paths must be analyzed. The first path is from V_{DD} through the error amplifier, and the power mos to V_{OUT}. The second path is from V_{DD} through the buffer to V_{OUT}. The output ripples of the two path have opposite phases. Thus, they are subtracted at the output, resulting in a substantially increased PSR.

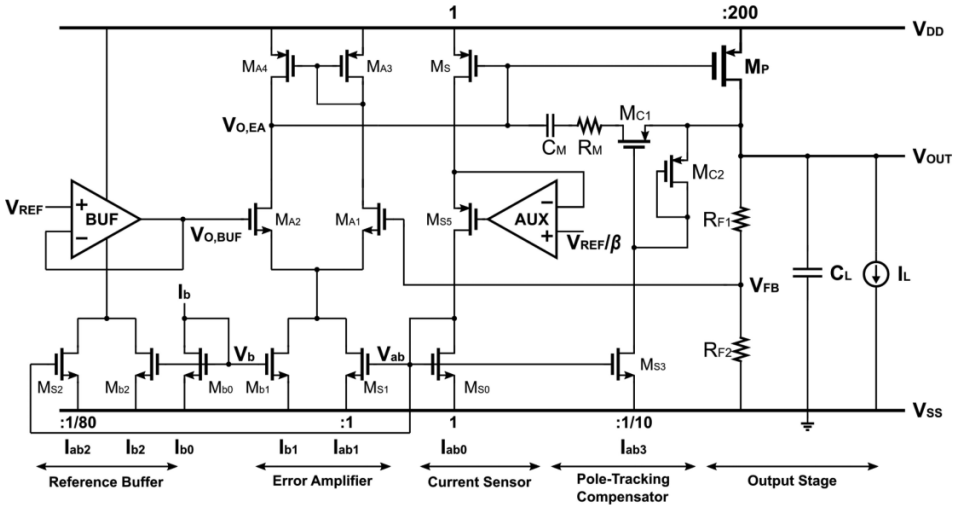


FIGURE 3.11: Schematic of Capacitor less LDO with adaptive biased circuit, supply ripple subtraction and pole tracking compensation (PTC) [25]

Table 3.1 summarizes the key performance metrics of the architectures described above, providing a comprehensive comparison of their respective design trade-offs.

Paper	[21]	[22]	[23]	[24]	[25]
Technology (nm)	180	180	65	180	180
$V_{dropout}$(mV)	290	200	200	200	200
i_L (mA)	0.1-50	0.01-10	0.05-100	0.01-50	0-20
I_q (μA)	138	1.99	-	1.6-200	8.6-241
C_L (pF)	100	10	100	10^6	100
Area (mm^2)	0.0326	-	-	0.0285	0.0113
PSR (dB)	45	66	-	<30 dB	50 dB
@ Hz	10k	100	-	10M	100k
LNR (mV/V)	10.368	3	4.4	0.10	-
LDR ($\mu V/mA$)	476	20	21	100	930
Overshoot (mV)	65.2	200	85	5	88.5
Undershoot (mV)	88	400	52	24	117
@ T_{rising} (ns)	200	500	10^3	10	100
$T_{recovery}$ (μs)	-	1.35	0.6	1.2	0.35
Gain (dB)	99.92	102.13	70	51.6	60
UGF (Hz)	2.543M	123.36k	1.82M	1.65M	4.4M
PM (deg)	63.12	63	62	45	78

TABLE 3.1: Comparison between state of art LDO architectures

3.3 Design

In analog circuit design, the transconductance g_m is a fundamental parameter used to trade-off speed and power consumption. It is defined as the change in the drain current I_D relative to a small change in the gate voltage V_G:

$$g_m = \frac{\Delta I_D}{\Delta V_G} \tag{3.14}$$

This parameter directly influences several figures of merit, such as the intrinsic voltage gain A_V and the maximum operating speed. For example, for a common-source stage, the gain is given by $A_v = g_m r_o$, where r_o is the output resistance. Similarly, the Gain-Bandwidth Product (GBW), which represents the maximum frequency of operation, is linearly dependent on g_m:

$$GBW = A_v BW = \frac{g_m}{2\pi C_L} \tag{3.15}$$

Additionally, the transconductance plays a critical role in noise performance. In summary, this paramer is the key design variable that must be accurately targeted during MOSFET sizing, as it directly governs the essential trade-offs between speed, power consumption, and noise performance.
Traditionally, the square law model which is employed for long-channel defines I_D as:

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2 = \frac{\mu C_{ox}}{2}\frac{W}{L}V_{ov}^2 \tag{3.16}$$

and g_m can be obtained deriving with respect to V_{GS}:

$$g_m = \frac{dI_d}{dV_{GS}} = (\mu C_{ox})\frac{W}{L}(V_{GS} - V_{th}) = (\mu C_{ox})\frac{W}{L}V_{ov} \tag{3.17}$$

The transistor efficiency is then defined by the ratio:

$$\frac{g_m}{I_D} = \frac{2}{V_{ov}} \tag{3.18}$$

Eq. 3.18 embodies the trade-off between g_m (a source of high performance and speed which should be maximixed) and I_D (which is directly connected to power consumption and should be kept as low as possible). However, the model is not reliable for scaled devices due to short channel effects. Figure 3.12 illustrates the different results obtained with the square model and a complex simulator that takes into account all the effects for both a short and long channel device.
Scaled devices are affected by velocity saturation and mobility degradation. Thus, I_D is no longer quadraticaly dependent on V_{GS} because g_m saturates for large overdrive voltages. The relation becomes linear, as can be seen from the graph. Furthermore, the square law model fails to accurately characterize the behavior of the ratio g_m/I_D for low values of V_{GS}. In fact, according to this model, the value should be infinite.
While this model can still be used to get an idea of the trend, it has proven to be inaccurate for compute the sizing. Conversely, circuit simulators implement extremely complex equations. A middle ground is represented by the g_m/I_D methodology which shifts the focus on this ratio rather then the gate overdrive voltage V_{ov}. [27]

3.3.1 The g_m/I_D design methodology

This methodology consists in consulting pre-compiled look up tables or extracting the useful information from specific graphs obtained using a circuit simulator. [27]

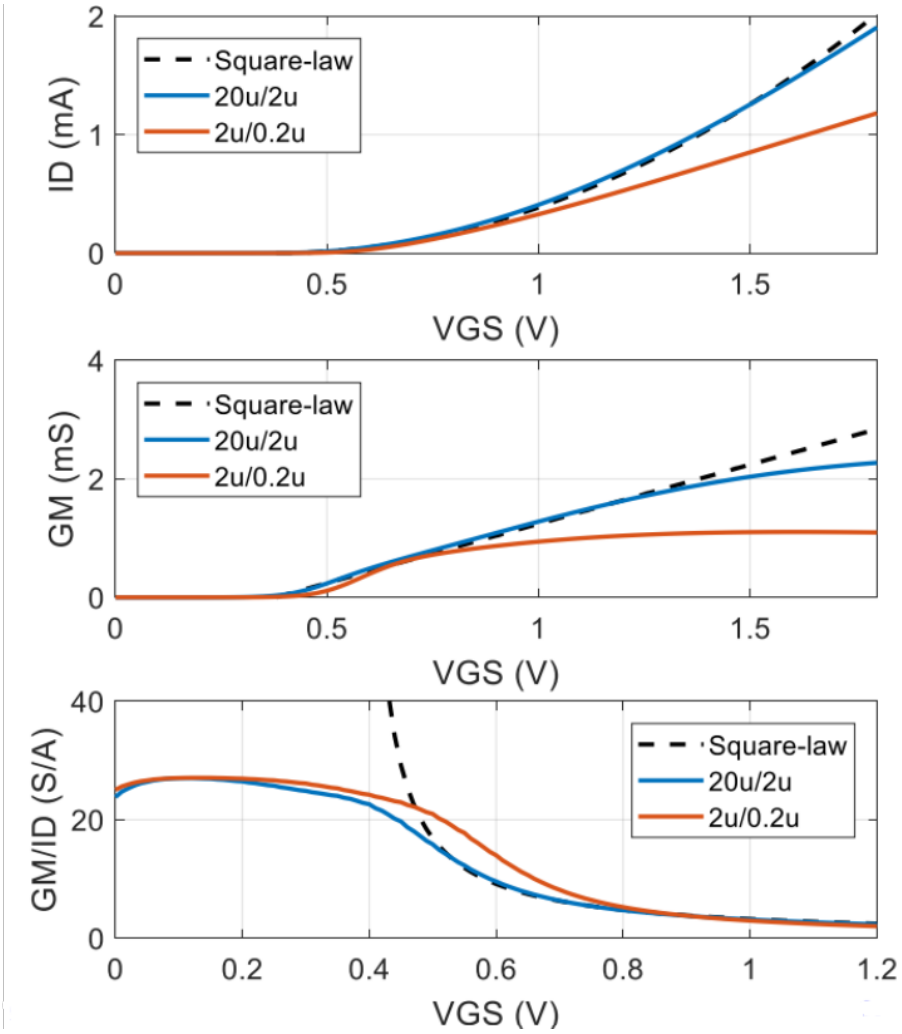


FIGURE 3.12: Comparison between results obtained with square law model and a simulator for long and short channel devices [26]

From the last graph in Figure 3.12 even if there are no strict boundaries, three regions can be roughly identified:

- **Strong inversion (SI)** with $g_m/I_D < 10$
- **Moderate inversion (MI)** with g_m/I_D from 10 to 20
- **Weak inversion (WI)** with g_m/I_D higher than 20

The choice of the operating regions depend on the design requirements, but considering the advantages of each one (reported in Table 3.2) it is possible the understand which is the most suitable.

Use small g_m/I_D if you want	Use large g_m/I_D if you want
- Strong-inversion (SI) biasing	- Moderate inversion (MI) or weak-inversion biasing
- Small gm (for a given ID) • Devices whose gm do NOT contribute to gain (ex: active loads)	- Large gm (for a given ID) • Devices whose gm do not contribute to gain (Ex: input stage and cascode devices)
- Small area	- High efficiency • Low power consumption (low ID) for a given speed or noise spec (gm spec)
- Small capacitance	- Less random mismatch • Large gm/ID implies larger W (large area) (beware of exceptions due to non-uniform doping profile)
- High speed	- Low flicker noise • Large gm/ID implies larger W (larger area)
- Large V_A (large ro) • The gate has better control on channel (VDS effects is less)	- Large input range and/or output swing • Large gm/ID implies small V*

TABLE 3.2: Differences in performance for small and large g_m/I_D [26]

The strength of the g_m/I_D methodology lies in its versatility: the listed ranges aren't greatly affected by the chosen device or technology.[26]

Design flow

Below are listed the steps followed for the design presented in this thesis. It is important to highlight that this approach represents one specific methodology, as the design sequence can vary significantly. Alternative sizing methods include the utilization of pre-compiled look-up tables or the implementation of automated sizing algorithms.

1. **Definition of** g_m: from the project requirements, this parameter is defined. For example, it can be computed starting from the expected velocity of the system, represented by the gain bandwidth product (GBW):
$$g_m = 2\pi GBW C_L \tag{3.19}$$

2. **Definition of** g_m/I_D: once g_m is fixed, based on the g_m/I_D range of choice, the current parameter can be selected computing the maximum and minimum range of values for the determined region. Finally, the exact value of g_m/I_D is computed

3. **Definition of L**: considering that:
$$A_V = \frac{g_m}{g_{ds}} \tag{3.20}$$
a sweep a parametric analysis is performed plotting A_v vs g_m/I_D for different values of L (see Figure 3.13). In this simulation V_{DS}, V_{BS} and W are fixed. When selecting the value of L, one must be aware of the performance that this parameter influences (see Table 3.3).

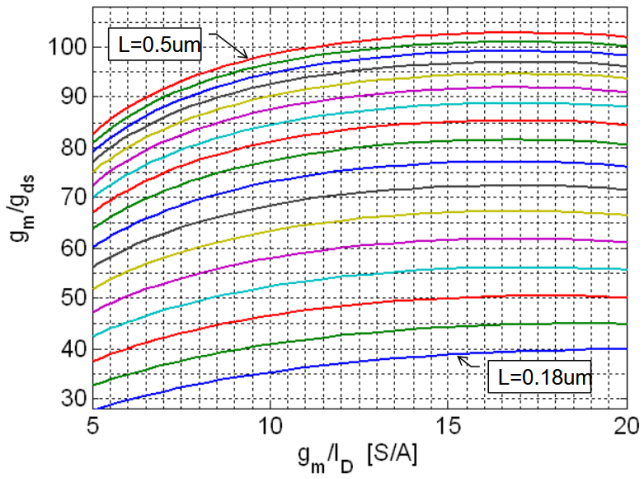


FIGURE 3.13: Example of graph obtained through a simulation of A_v vs g_m/I_D for different channel length values [28]

Use shorter L if you want	Use longer L if you want
- Smaller area	- High gain (high V_A) • Must have large VDsat_margin to be effective (beware of exceptions due to feedback)
- Smaller capacitance	- Less random mismatch • Longer L implies larger area (beware of exceptions due to non-uniform doping profile)
- High speed (high $f_t = \frac{g_m}{2\pi C_{gg}}$)	- Low flicker noise • Longer L implies larger area

TABLE 3.3: Differences in performance for small and large channel length value L [26]

4. **Definition of W**: since the current is directly proportional to the width, the following relation can be written:

$$W_x = I_{D_x} \frac{1}{\frac{I_D}{W}} \tag{3.21}$$

and the final width can be determined.
By performing a simulation and plotting I_D/W vs g_m/I_D with the other found parameteres fixed, the required value of W can be accurately determined.

It is important to note that the process is not always linear, since optimising one parameter can affect other specifications. Therefore, trade-offs are applied, and it may be necessary to iteratively review some steps before proceeding in order to achieve the desired balance and meet the requirements.

3.3.2 LDO design

Figure 3.15 represents the schematic of the LDO voltage regulator designed for this thesis. The implemented error amplifier is a 5T operational transconductance amplifier (OTA), consisting of

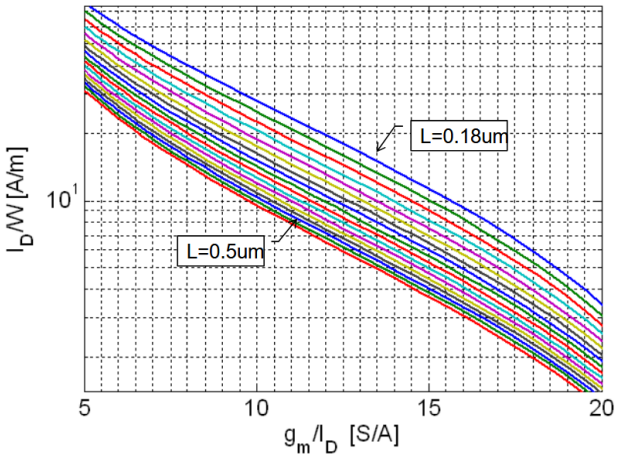


FIGURE 3.14: Example of graph obtained through a simulation of I_D/W vs g_m/I_D [28]

a differential pair and a current mirror that is used as an active load. The fifth transistor is used for biasing.

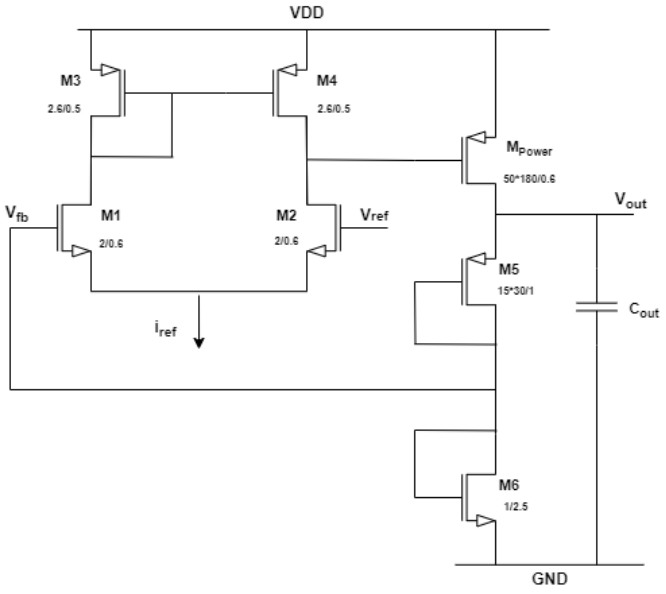


FIGURE 3.15: Schematic of the LDO voltage regulator designed

The working principle is based on the differential pair. When the gate voltages of the input transistors are equal, the tail current is shared equally between the two branches due to transistor symmetry. However, when a difference in the gate voltages is introduced, the transistors of the differential pair drive different currents proportional to the input voltage difference. The load, implemented as a current mirror, converts the differential current into a single ended output current trying to force the same currents on the two branches. This mechanism ensures that the resulting current difference flows into the amplifier's load, achieving voltage to current conversion.

The principal figures of merit that describe the characteristics and performance of the amplifier are:

$$A_v = \frac{v_{out}}{v_{id}} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} \tag{3.22}$$

$$\omega_{-3dB} = \frac{1}{(g_{ds2} + g_{ds4})C_L} \tag{3.23}$$

$$SR = \frac{I_{SS}}{C_L} \tag{3.24}$$

$$P_{diss} = V_{DD} I_{SS} \tag{3.25}$$

The channel length (L) is shorter with respect to the current reference value to limit the parasitic capacitance and achieve a high bandwidth. The tail current (I_{SS}) is set to $6\mu A$, which represents a compromise between the requirements of high slew rate and low power consumption.

The final sizing is reported in Table 3.4. Finally, the dimension of the power pMOS is chosen

MOS	W (μm)	L (μm)
M1,M2	2·1	0.6
M3, M4	2·1.3	0.5
M_{POWER}	180·50	0.6
M5	15·30	1
M6	1	2.5

TABLE 3.4: Transistor dimensions for the LDO regulator

large enough to reduce the dropout voltage and to be able to drive the maximum current of $10mA$. However, the size is limited to avoiding slowing down the transient response, save area and assure an optimum driving capability.
In place of the passive resistances are used a pMOS and an nMOS for the resistive ladder. The transistors are sized such that the quiescient current is maintained low.
The circuit is powered by a Lithium battery with a nominal voltage of 3.7V, the output voltage is 1.8V and the load of the LDO is considered to be 100 pF.

3.4 Pre-layout simulations

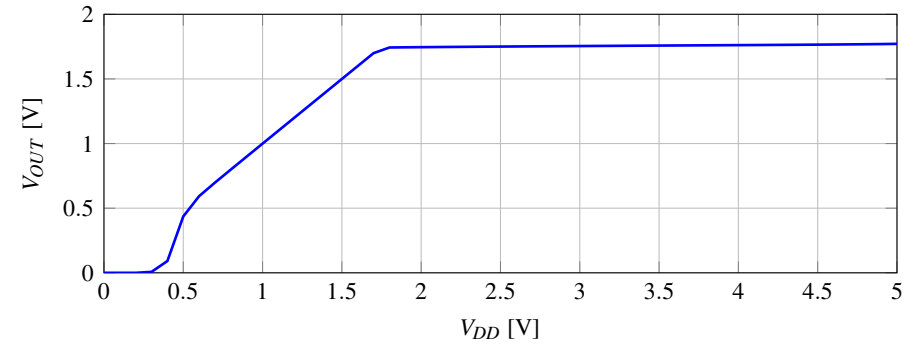
Following the sizing step, DC, AC and transient simulations were performed to measure the the actual performance of the LDO regulator.

3.4.1 DC analysis

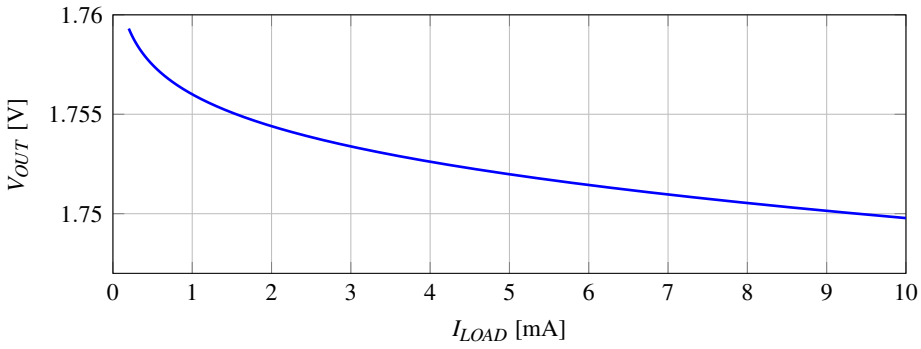
Figure 3.24b represents the results of the DC analysis. In particular, Figure 3.24a shows the line regulation. The value of the parameter is 8.7 mV/V and the LDO enters the regulating region at 1.8V. The measured dropout voltage is 100 mV.
The load regulation is reported in Figure 3.16b. The sweep is performed from 200 μA to 10 mA. The reason for the lower bound will be explained in the next section. The value of load regulation is equal to 0.97 mV/mA.
Figure 3.24c shows the output voltage variation as a function of temperature. For the sweep, the industrial range has been considered: from -40 °C to 85 °C. However for this application, the temperature coeffcieint doesn't represent a key parameter since the expected variations are only a few degrees. The temperature coefficient obtained by considering the maximum variation is 238 ppm/° C.
The parameters measured from the graphs are summarized in Table 3.5.

Parameter	Value
$V_{dropout}$	100 mV
Line regulation	8.7 mV/V
Load regulation	0.97 mV/mA
TC	238 ppm/°C

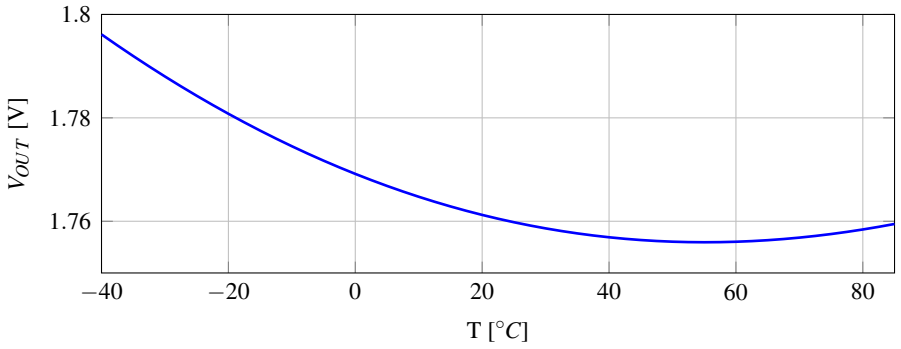
TABLE 3.5: DC parameters for LDO regulator



(A)



(B)



(C)

FIGURE 3.16: Results of DC analysis of LDO regulator: (a) Line regulation; (b) Load regulation; (c) Temperature variation

3.4.2 AC analysis

In this section, the frequency behavior of the component is evaluated. A parametric analysis (see Figure 3.17) was performed to extract the minimum load. Plotting the phase margin as a function of the current load, reveals that for values lower than 200 μA, the phase margin drops below 45°. This indicates that the system no longer maintains the required stability for optimal transient response.

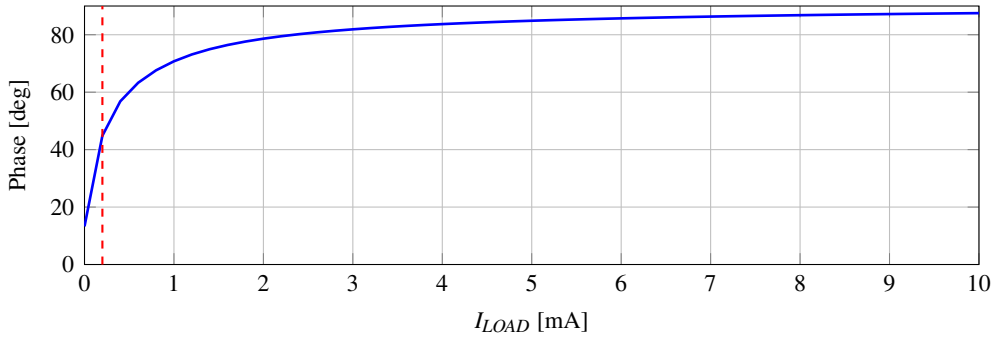
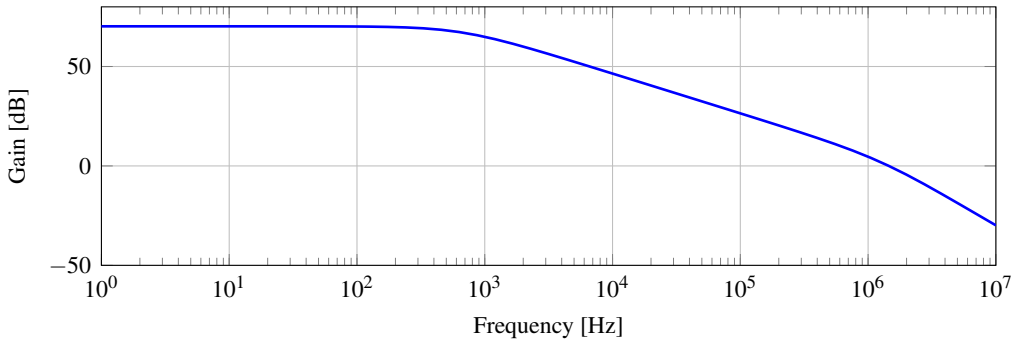


FIGURE 3.17: AC simulation to evaluate the minimum load for the LDO

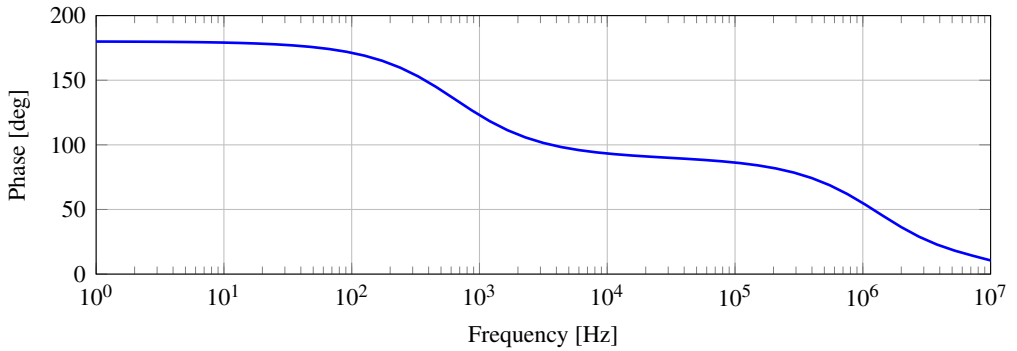
Thus the following simulations are obtained for the worst case represented by the minimum load (see Figure 3.18)
Table 3.6 reports the numeric information obtained from the graphs.

Parameter	Value
BW	648 Hz
Gain	70 dB
UGF	1.45 MHz
PM	45 deg
PSRR	40.9 dB

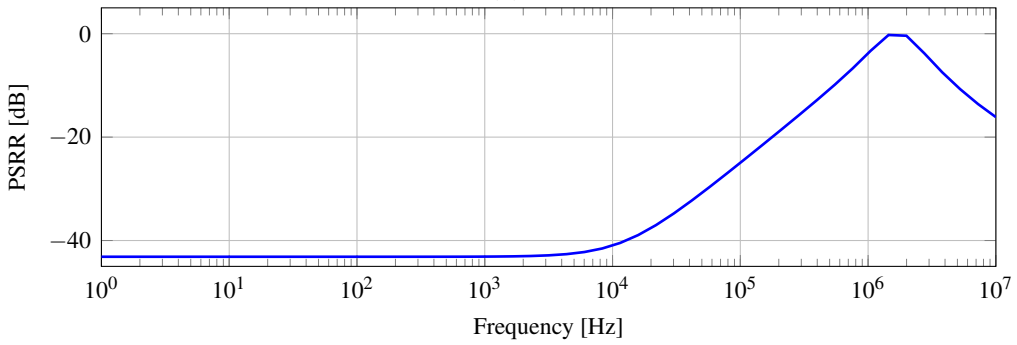
TABLE 3.6: AC performances for LDO regulator



(A)



(B)

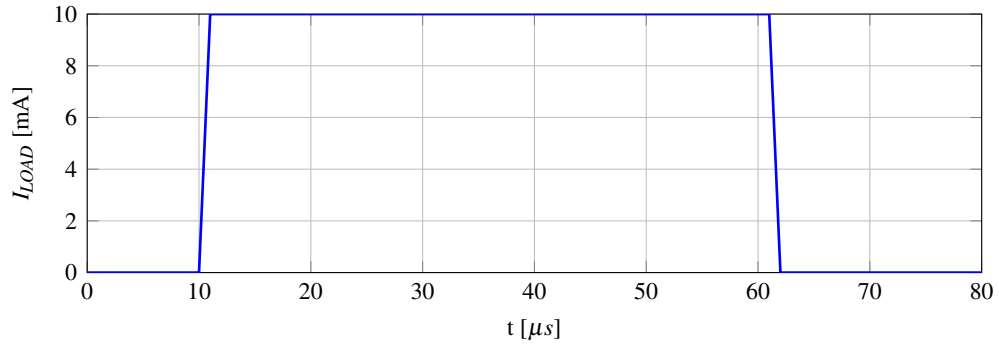


(C)

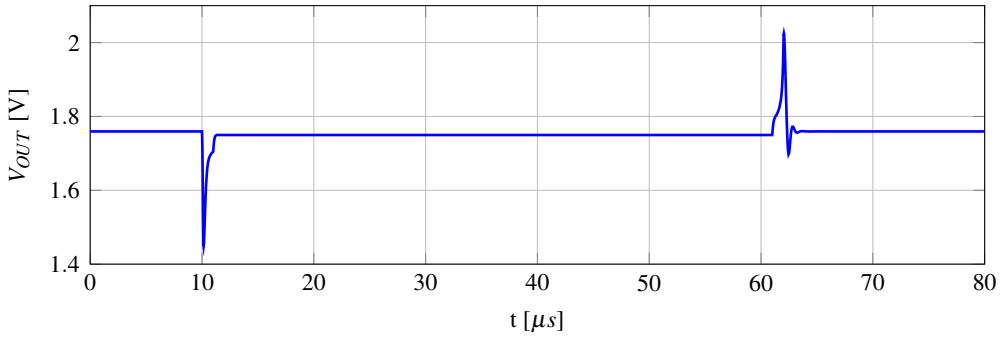
FIGURE 3.18: Results of AC analysis of LDO regulator: (a) Gain; (b) Phase; (c) PSRR

3.4.3 Transient analysis

Figure 3.19 shows the output voltage variation when a current load step is applied. The waveform transients from 200 μA to 10 mA with a rise and fall time of 1 μs. The overshoot measured is of 266 mV while the undershoot reaches 309 mV. The transient recovery time is less than 2 μs for both of the transitions.



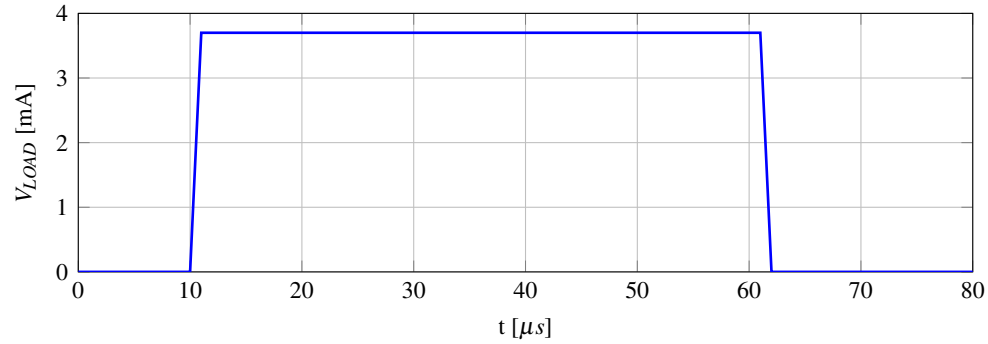
(A)



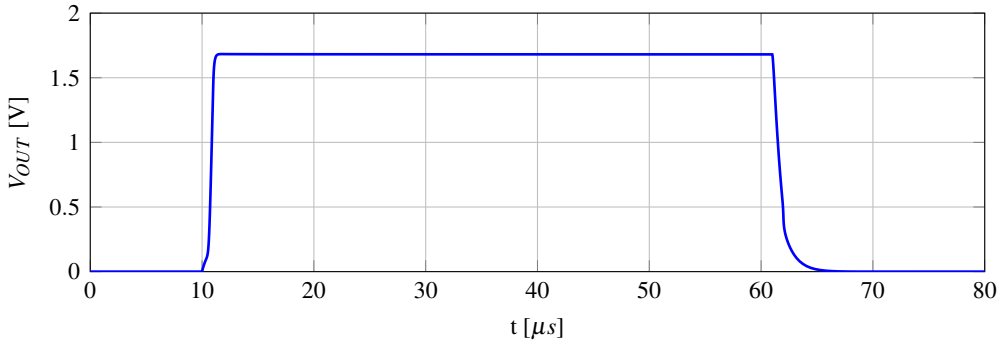
(B)

FIGURE 3.19: Transient analysis results for LDO regulator: (a) Current step from 0 a 10 mA; (b) Output voltage variation

Figure 3.20 illustrates the output voltage variation for an input voltage step from 0 to 3.7V with rising and falling time of 1 μs. In this case no overshoots or undershoots are present. The transient recovery time is longer because it is necessary to wait also for the current reference to reach stability.
Table 3.7 lists the results extracted from the transient analysis.



(A)



(B)

FIGURE 3.20: Transient analysis results for LDO regulator: (a) Voltage step from 0 a 3.7V; (b) Output voltage variation

Parameter	t_r	t_f	Undershoot	Overshoot
ΔV_{DD}	1.3 μs	3.8 μs	-	-
ΔI_{LOAD}	1.1 μs	1.9 μs	309 mV	266 mV

TABLE 3.7: Results obtained with transient analysis for LDO regulator

3.4.4 Corner analysis

For the conrer analysis, a DC simulation has been performed to measure what are the worst cases for line regulation. From Figure 3.21 it can be noted that in the SS corner, the minimum voltage required to obtain regulation is the highest. Furthermore, the regulated voltage at 3.7V is increased by 6% with respect to the nominal value due to the variation of V_{REF} in beta multiplier. Conversely, with FF the threshold voltage required to start regulation is the minimum and the regulated voltage at 3.7V is decreased by 5.7%.

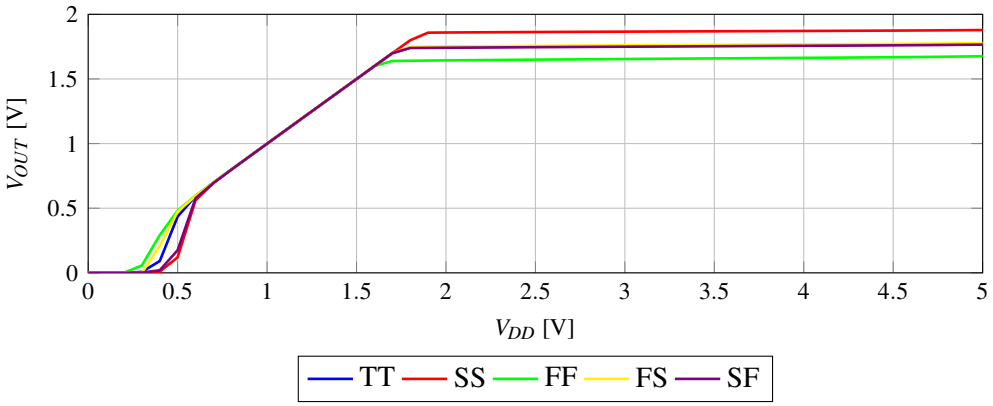
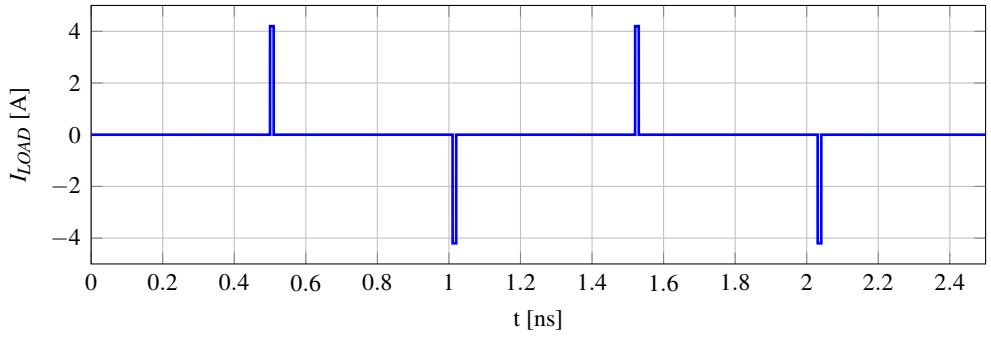


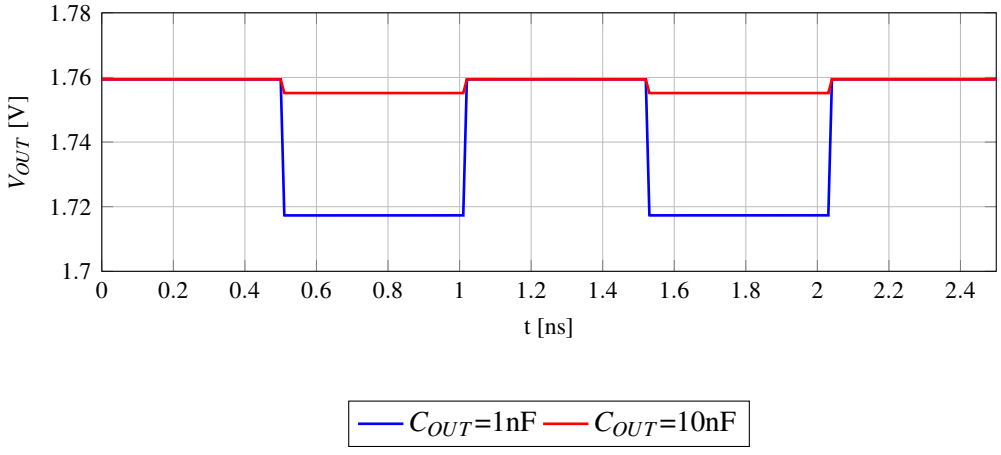
FIGURE 3.21: Corner analysis representing line regulation for LDO regulator

3.4.5 Digital load

Until now, the simulation were perfomed considering an analog load. LDO regulators are typically used for both analog and digital circuits, often employing different LDOs for each to maintain isolation.
Applying a capacitor at the output is necessary to sustain the current demands during the rapid commutations typical of a digital circuit. Compared to analog ones, digital circuits are characterized by high value current peaks during these transitions.
Figure 3.22a simulates a worst case scenario where the current request is characterized by fast transient peaks. The results show that applying a 1nF output capacitor is enough to supply the required charge. Thus, this design could be robustly implemented for digital circuit loads as well.



(A)



(B)

FIGURE 3.22: Digital load simulation: (a) digital load transitions; (b) comparison between two possible output capacitors

3.5 Layout

Figure 3.23 presents the layout of the designed LDO. Considering that the total area is of 0.027 mm^2, the majority of it is occupied by the power MOS. To address reliability issues, the metal lines intended for delivering the highest current are designed to be thicker.The common centroid layout has also been applied to this design, and guard rings have been implemented for sensitive components. Moreover, to avoid mismatches, the orientation is kept the same for all the transistors.

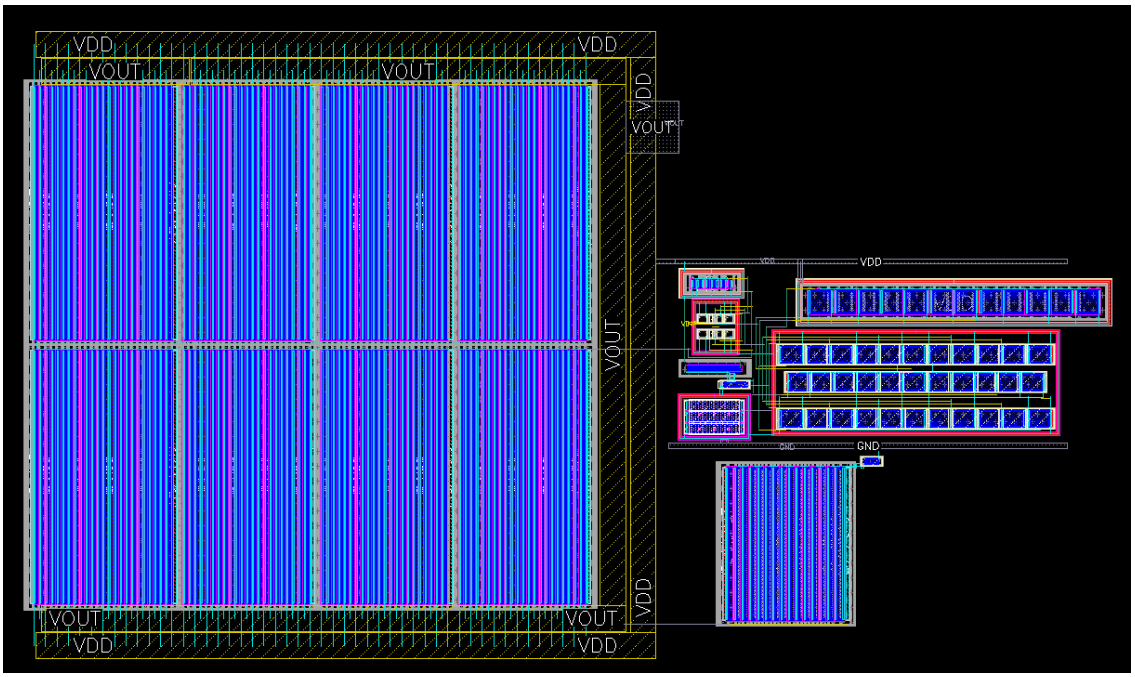


FIGURE 3.23: Layout of designed LDO regulator

3.5.1 Post layout simulations

Post layout simulations are performed to verify the compliance with the pre-layout simulations and how the parasitics have affected the final design.

DC analysis

Figure 3.24 shows the results obtained with DC analysis. All the graphs present an offset with respect to the pre layout case, this is due to the parasitic resistance that has increased.
Both line regulation and load regulation have increased post layout, while the temperature coefficient decreased. The quiescient current measured is of 16.6 . Table 3.8 reports the numerical results obtained from the simulations.

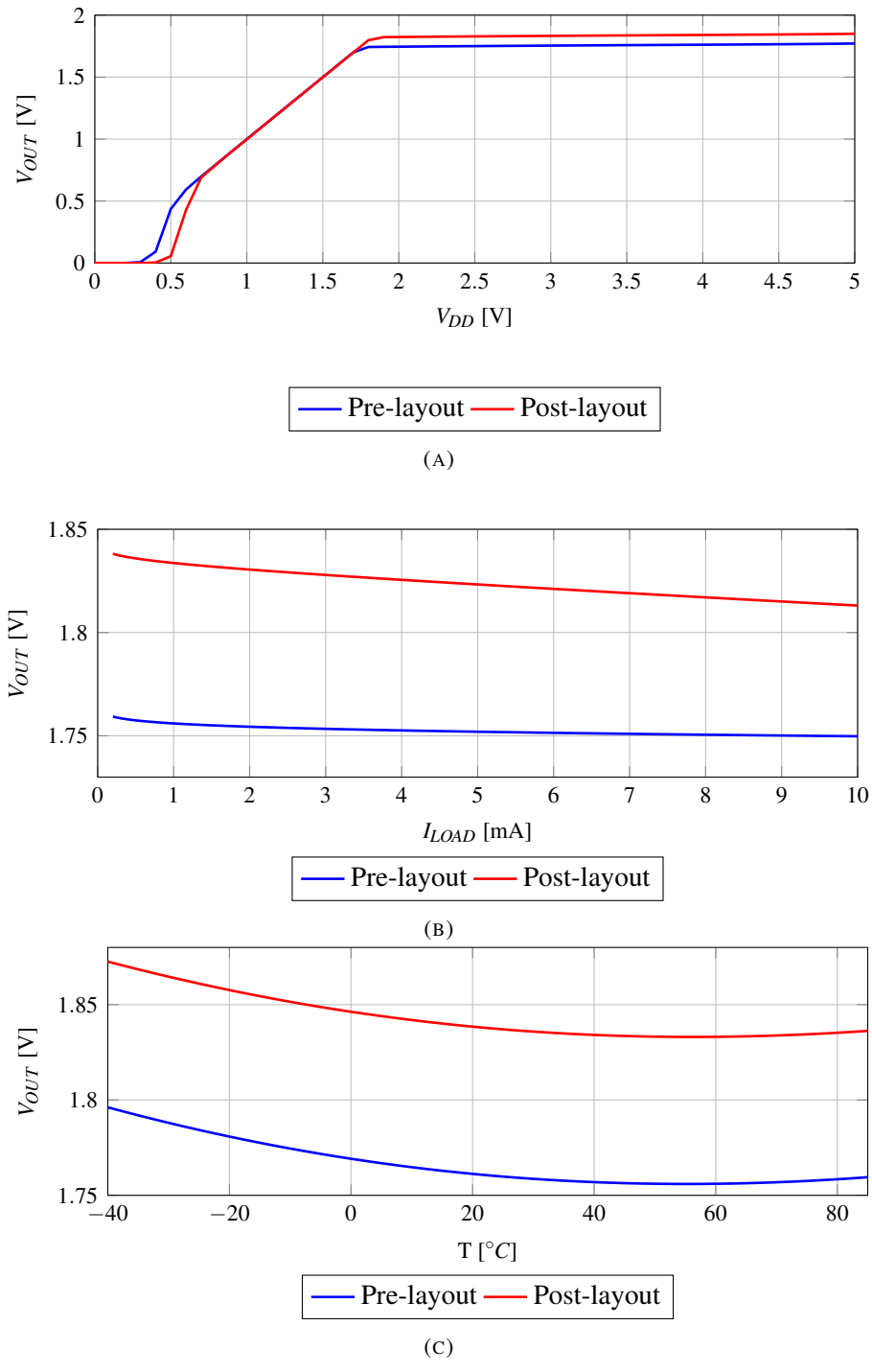


FIGURE 3.24: Results of DC analysis post layout for LDO regulator: (a) Line regulation; (b) Load regulation; (c) Temperature variation

Parameter	Simulation	Value
Line regulation	Pre-layout	8.7 mV/V
	Post-layout	16 mV/V
Load regulation	Pre-layout	0.97 mV/mA
	Post-layout	2.6 mV/mA
TC	Pre-layout	238 ppm/$^{\circ}C$
	Post-layout	171 ppm/$^{\circ}C$

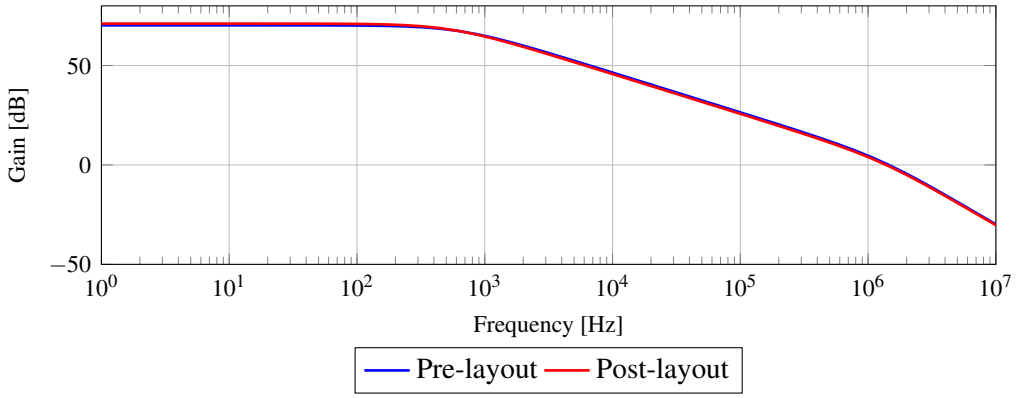
TABLE 3.8: Comparison of performances obtained from DC analysis pre and post layout

AC analysis

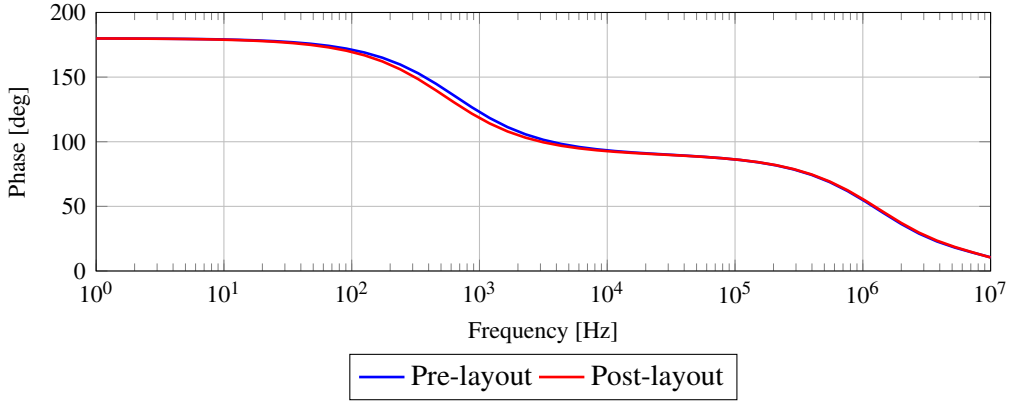
Figure 3.25 depicts the results obtained from the AC simulations. Except for a decreased bandwidth due to the parasitic capacitance, the overall differences in the frequency response remained negligible with respect to the pre layout simulation, suggesting that the layout has been properly performed. Table 3.9 summarizes all the data extracted from the graphs for a easier comparison of the two cases.

Parameter	Simulation	Value
BW	Pre-layout	648 Hz
	Post-layout	539 Hz
Gain	Pre-layout	70 dB
	Post-layout	71 dB
UGF	Pre-layout	1.45 MHz
	Post-layout	1.4 MHz
PM	Pre-layout	45 deg
	Post-layout	47 deg
PSRR	Pre-layout	40.9 dB
	Post-layout	40.2 dB

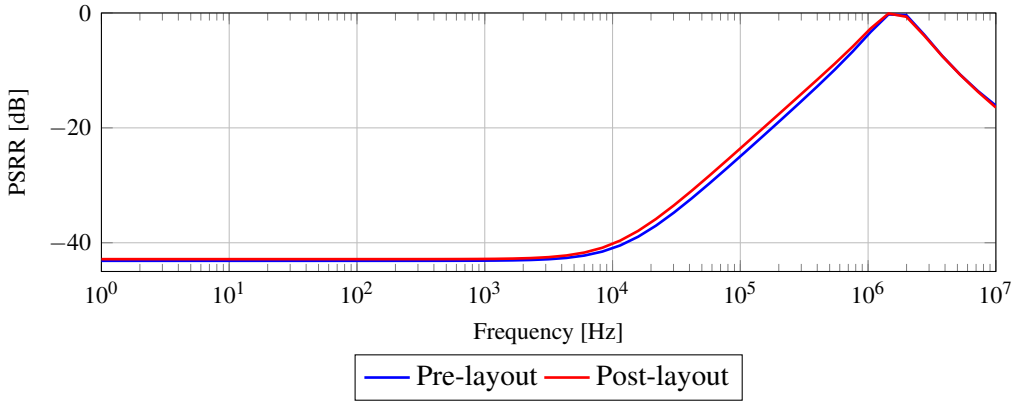
TABLE 3.9: Comparison of performances obtained from AC analysis of LDO regulator pre and post layout



(A)



(B)



(C)

FIGURE 3.25: Results of post layout AC analysis of LDO regulato: (a) Gain; (b) Phase; (c) PSRR

Transient analysis

Figure 3.26 shows the transient response for a current load step. The waveform transits from 200 μA to 10 mA with a rising and falling time of 1μs. The output voltage variation post layout presents an offset due to parasitic resistances. Furthermore the values for overshoot and undershoot along with the transient recovery time have incresed post layout. This effect is due to the parasitic capacitances that have reduced the bandwidth.

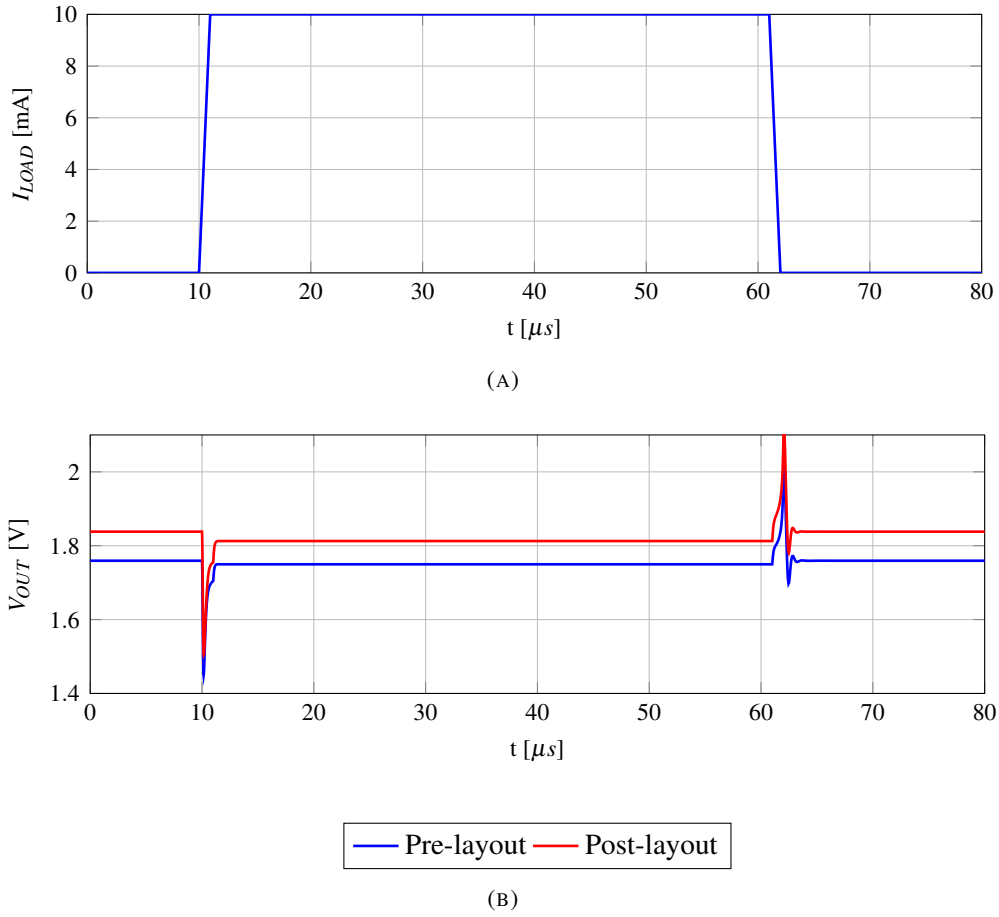


FIGURE 3.26: Results from transient simulation of LDO regulator pre and post layout: (a) Current load step from 0 to 10 mA; (b) Output voltage variation pre and post layout

Figure 3.27 shows the behavior obtained from the transient simulation in case of voltage supply variation from 0 to 3.7V with rising and falling time of 1μs. The start up time has increased post layout, confirming the slowing effect of the parasitic capacitance. Moreover, an overshoot of 39 mV has appeared. Conversely, no undershoot is registered for the high to low transition.
Table 3.10 summarizes the discussed results.

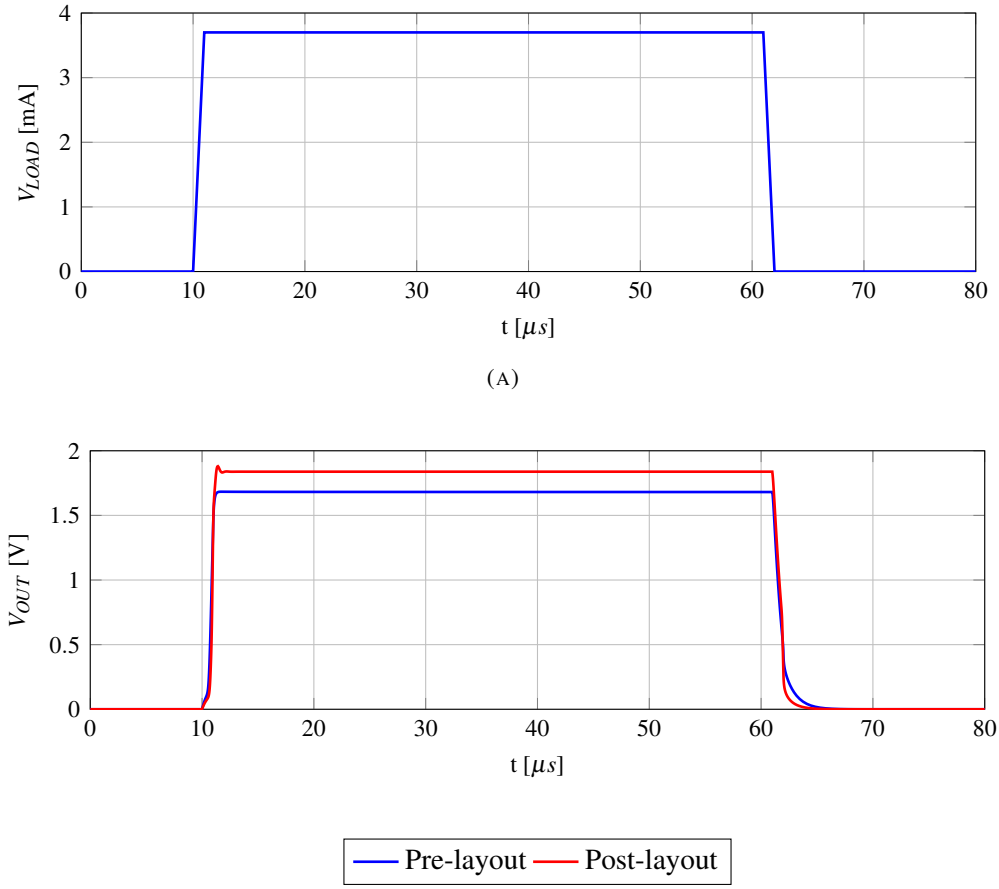


FIGURE 3.27: Results from transient simulation of LDO regulator pre and post layout: (a) Voltage supply step from 0 to 3.7V; (b) Output voltage variation pre and post layout

Parameter	Simulation	t_r	t_f	Undershoot	Overshoot
ΔV_{DD}	Pre-layout	1.3 μs	3.8 μs	-	-
	Post-layout	1.6 μs	2.6 μs	39 mV	-
ΔI_{LOAD}	Pre-layout	1.1 μs	1.9 μs	309 mV	266 mV
	Post-layout	1.1 μs	1.6 μs	310 mV	288 mV

TABLE 3.10: Comparison of performances obtained from transient simulation pre and post layout

Monte Carlo simulation

Figure 3.28 depicts the results obtained from a Monte Carlo simulation performed with 5000 samples. The histogram present a mean value of 1.81 V with a standard deviation of 47 mV. The LDO has been designed taking into account the layout parasitic effects in order to obtain a nominal regulated value of 1.8V. This requirement is succesfully reached.
The robustness of the component could be increased by implementing a trimming circuit.

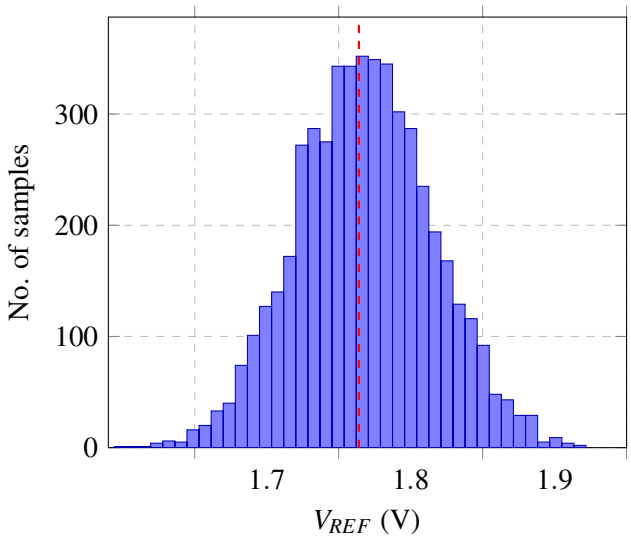


FIGURE 3.28: Monte Carlo analysis of V_{OUT} for LDO regulator. The standard deviation σ is 47 mV and the dispersion $3\sigma/\mu$ is equal to 7.8%.

Chapter 4

Conclusion

The power management integrated circuit (PMIC) is an essential component in the growing field of portable devices. LDO voltage regulators, in particular, are fundamental thanks to their high degree of integration.
These circuits offer high performance, including a fast transient response, high load and line transient regulation, and low power consumption. These characteristics make them ideal for powering wearable sensors.
This thesis focuses on designing a capacitorless low dropout voltage regulator (CL-LDO) as part of the PMIC for an electrochemical wearable sensor for sweat monitoring. The component consists of a single-stage error amplifier to limit the system's power consumption. Specifically, it uses a 5T-OTA (five transistor operational transconductance amplifier). A pMOS pass transistor is used to achieve high power conversion efficiency, due to the minimum voltage drop required between the input and output voltages. Finally, an active resistive ladder is implemented.
After characterising the architecture through DC, AC and transient simulations, the layout was created using all the techniques necessary to avoid mismatches. Post-layout simulations are consistent with pre-layout simulations, showing limited differences with respect to the designed architecture, thus confirming the robustness of the layout choices. The designed voltage regulator is suitable for the intended application thanks to its low power consumption, limited footprint size, and overall performance.

4.1 Future work and improvements

Further improvements could focus on adding a buffer to extend the bandwidth and reduce overshoots and undershoots in the system, as well as adding an adjustable biasing mechanism to reduce the minimum load current. Additionally, a digital trimming mechanism could be incorporated to enhance the post-layout precision of the current reference.
Since bio-Socs spend most of their time in sleep mode, including a load switch could decrease the system's quiescent power consumption.

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