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Fabrication and electrical characterization of ferroelectric Si-doped HfO_2 thin films for cryo-electronic memory devices

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Abstract

The discovery of ferroelectricity in the non-centrosymmetric orthorhombic crystal phase of HfO_2 in 2011 has led to renewed interest in ferroelectric non-volatile memories. In particular, the recent widespread attention for hafnia thin films can be attributed to their remarkable performance in terms of low power consumption, remnant polarization, memory window, retention, endurance and switching speed, combined with their already well-known compatibility with CMOS technology. These qualities meet the growing demand for high-speed computation and high-density data storage, paving the way for technologies such as in-memory computing and neuromorphic computing. These technologies can be implemented using FeFETs (ferroelectric field-effect transistors) and FeCAPs (ferroelectric capacitors).
This project focuses on the fabrication and electrical characterization of two main types of HfO_2-based devices: MFIS gate-stacks and MFM capacitors, where M is the metal electrode, F is Si:HfO_2 (silicon-doped hafnia thin film with Si concentration of 3 %, in order to favour the ferroelectric character) and I is the SiO_2 dielectric layer between F and the p-doped silicon substrate S. In both devices, the hafnia was deposited using ALD (atomic layer deposition) and subsequently crystallized through an RTP (rapid thermal process).
The first part is dedicated to the extraction of important information describing a non-switching MFIS gate, such as flatband voltage, effective work function of the metal and interface trap density. The analysis was carried out mainly by means of the measured capacitance-voltage curves, according to the High-Low frequency method. The parallel conductance peaks were also studied for a more complete understanding of the physics behind the device. The study was conducted on three different thicknesses of the Si:HfO_2 layer, keeping fixed the thickness of the SiO_2. The parameters were extracted for different gate metals, such as W, Ti/Pt, TiN, TiN/W. Then, a further design was tested and discussed in order to increase the voltage drop across the hafnia. This was achieved by reducing the thickness of SiO_2 with respect to Si:HfO_2, thus balancing their capacitances.
The second part is devoted to the study of FeCAPs. These capacitors feature a staggered geometry to prevent the breaking of the hafnia while probing/wire bonding. After performing wake-up cycles by means of applied voltage pulses, different curves were measured, such as charge-voltage, capacitance-voltage, current-voltage and current-time plots. Important figures

of merit were then extracted, including the remnant polarization 2 P_r, the coercive field E_c (thus the memory window 2 V_c), the maximum capacitance and the baseline capacitance.
The measurements were performed at first at room temperature (RT) and then at 77 K using liquid nitrogen cooling. The aim was to highlight the impact of a cryogenic environment on the performance of non-volatile memories. The interest for memories working in such harsh environment has in fact grown in the recent years: in quantum computers, for example, qubits operate at temperatures of few mK and the processors must work at maximum 4 K. This has restricted the choice of memories to those able to work at temperatures matching the one of processors, in order to allow low thermal leakage, scalability and high speed.
A third part of the thesis focuses on the TCAD Sentaurus simulations of the ion implantation for a correct formation of the source and drain regions of the FeFETs. The type of implantation was a PIII (plasma immersion ion implantation) and the implanted substrate was an SOI (silicon on insulator). Phosphorous was used as dopant species and different combinations of dose, energy and thermal oxide mask thickness were tested. The aim of these simulations was to verify the presence of a sufficiently high dopant concentration ($\simeq 10^{20} cm^{-3}$) up to few nm from the top silicon surface and to make sure that no penetration of ions occurred inside the BOX, in order to prevent leakage.

Chapter 1

Introduction

One of the most important discoveries of the past decade was the unexpected excellent performance of HfO_2 at small scale, when crystallized in its ferroelectric non-centrosymmetric orthorhombic crystal phase. In fact, the potential of non-volatile memories was limited by the poor compatibility of perovskites with integrated circuit technologies. But HfO_2 thin films managed to combine their outstanding performances in terms of low power consumption, remnant polarization, memory window, retention, endurance and switching speed with their already renowned compatibility with CMOS technology. The need of high-speed computation and high-density data storage encouraged therefore the rising of exciting technologies such as in-memory computing and neuromorphic computing. Von Neumann architecture has in fact faced a critical bottleneck, arising from the need of constant transfer of information between the CPU and the memory; since this operation is considerably power-demanding and time-consuming, new brain-inspired technologies have emerged to embed memory cells within the same area intended for computation. This project will focus on the fabrication and electrical characterization of two structures that represent the building blocks of non-volatile memories, i.e. MFIS gate-stacks and MFM capacitors, where M is the metal electrode, F is Si:HfO_2 (silicon-doped hafnia thin film with Si concentration of 3 %, in order to favour the ferroelectric character) and I is the SiO_2 dielectric layer between F and the p-doped silicon substrate S. The study was carried out by applying different methods for the electrical characterization, investigating traps and ferroelectric domains. Low temperature measurements were also performed and compared to RT results. Finally, TCAD simulations were performed to predict the outcome of an ion implantation performed on an SOI substrate. The aim of the simulations was to prevent the penetration of Phosphorus ions inside the BOX and to guarantee a sufficiently high dopant concentration ($> 10^{20}\ cm^{-3}$) at few nm from the TopSi surface. This thesis was conducted at Nanolab of prof. Adrian Mihai Ionescu, at EPFL. The fabrication was carried out at the Center of MicroNanoTechnology (CMi), at EPFL. The goals were defined in agreement with NCCR SPIN, which funded this project together with Nanolab.

Chapter 2

Theoretical Overview

2.1 Ferroelectricity

Materials exhibit ferroelectric properties when revealing a spontaneous intrinsic polarization even in absence of an applied electric field, and when this polarization can be reversed by applying an electric field E smaller than $E_{breakdown}$. This peculiar behavior is justified by their non-centrosymmetric crystalline structure when they are kept below the Curie Temperature (T_c): the broken symmetry causes the formation of molecular dipoles, which can align to sufficiently high external electric fields. The result is that, while standard dielectric materials typically show a linear response of the polarization to electric fields, the P-E curve (P ≡ polarization, E ≡ electric field) of ferroelectrics is an hysteresis loop [1], which make them suitable for memory applications (like their ferromagnetic counterparts) since the polarization depends not only on E but also on the history of the sample.

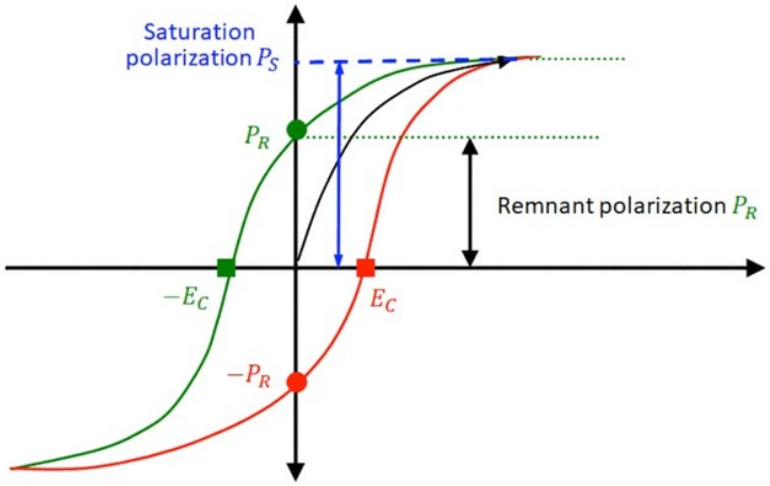

Figure 2.1: Ferroelectric hysteresis [2].

After reaching saturation (P_s), when turning off the electric field the material will exhibit a retained polarization (P_r), which can be eventually fully erased only by applying a reverse coercive field ($-E_c$). Above T_c the material undergoes a phase transition, losing its asymmetry and entering a paraelectric state, where the hysteresis loop shrinks and becomes a single line:

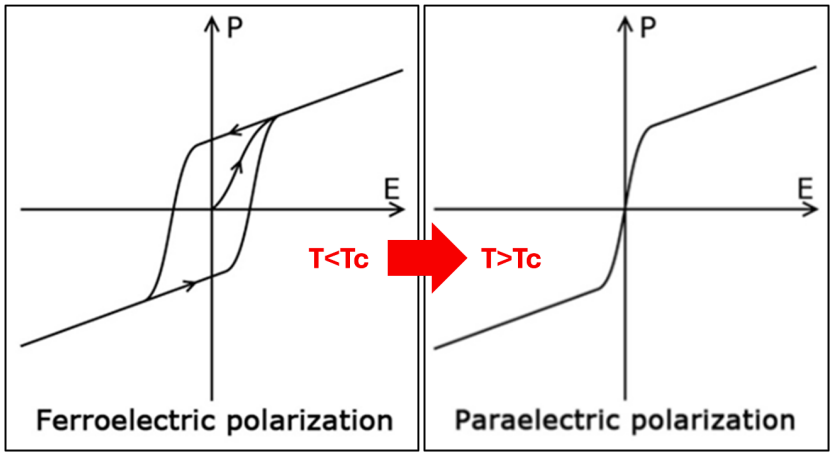

Figure 2.2: Ferroelectric to Paraelectric phase transition [3].

As shown in 2.2, in real devices the polarization typically does not perfectly saturate but has a small slope instead, because of the linear contribution of its dielectric component [4]. In general, we can state that the P-E nonlinear behavior of ferroelectric materials can be attributed to the ϵ_r dependence on E (P-E relation in 2.1.1) and to the *ferroelectric domains* dynamics when subjected to an external electric field. In fact, such materials are made of many homogeneous regions (i.e. ferroelectric domains), each of them made of uniformly aligned dipole moments. Typically, larger grains can contain more than one domain, while fine grains are likely hosting only one domain; since in the latter case the interaction between domains is more significantly obstructed by grain boundaries, we can state, as a rule of thumb, that fine grain materials usually have a smaller dielectric constant than large grain ones [5].

2.1.1 Ferroelectric Capacitors and the Landau Devonshire Theory

By placing a ferroelectric material between two conductive plates we obtain a ferroelectric capacitor, which inherits from ferroelectrics a nonlinear behavior and a high dielectric constant ϵ_r. We can briefly introduce the Landau Devonshire theory in order to understand the origin of hysteresis in such capacitors.
The total stored energy of standard non-ferroelectric capacitors is:

$$G = \frac{Q^2}{2C} - V_0 Q$$

where the first term is the internal energy of the capacitor and the second one corresponds to the work done to build up the charge. At equilibrium we expect that:

$$\frac{dG}{dQ} = 0$$

such that

$$Q_c = CV_0$$

The existence of a stable state for the capacitor requires the presence of a minimum in the G function, therefore:

$$\frac{d^2G}{dQ^2} > 0 \text{ , that is } \quad \frac{1}{C} > 0$$

Let's indicate with G' the energy per unit volume:

$$G' = \frac{G}{A \times tox}$$

and being

$$P = Q' = \frac{Q}{A} \quad \text{and} \quad V_0 = E \times tox$$

The energy density ends up being:

$$G' = \frac{P^2}{2C'tox} - EP$$

where P is the polarization. Unlike conventional dielectrics, it was experimentally observed that ferroelectric materials differ in the relationship between the energy density and the polarization, which resulted being not a simple quadratic one, still remaining an even function of P (at zero fields):

$$G' = G_0 + \frac{1}{2}aP^2 + \frac{1}{4}bP^4 + \frac{1}{6}cP^6 - EP \quad [6]$$

where G_0 is the energy at zero field, while a,b,c are experimental parameters. In particular,

$$a = a_0(T - T_c)$$

a_0 is always greater than zero in ferrorelectrics, thus $a<0$ when $T<T_c$. Finally, $c>0$ in ferroelectrics, while the sign of b determines the discontinuity/continuity (first order/second order phase transition) of the polarization below T_c. This generalized formula introduces 2 stable minima and 1 unstable maximum between them, strengthening the idea of bistability of the ferroelectric polarization:

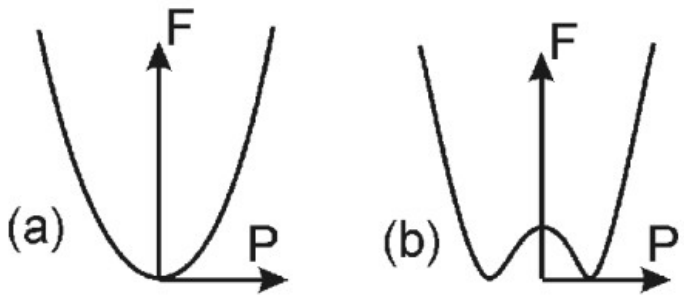

Figure 2.3: Free energy F ($F \equiv G$) vs Polarization in a) paraelectric material, b) ferroelectric material [7].

The energy barrier between the two stable states in 2.3 b) suggests that we need a sufficiently high electric field to switch the polarization (coercive field).
Recalling the Landau-Khalatnikov equation:

$$\frac{dP}{dt} + \Gamma \frac{dG'}{dP} = 0$$

we can state that:

$$\frac{dP}{dt} = -\Gamma(G_0 + aP + bP^3 + cP^5 - E)$$

This expression is able to predict the P-E hysteresis loop. As an example we can derive the spontaneous polarization values: for simplicity we assume static conditions ($\frac{dP}{dt} = 0$), ignore the fifth order term (reasonable when b>0) and take $G_0 = 0$:

$$E = aP + bP^3$$

In real devices the P-E curve in 2.4 b) experiences an abrupt transition from the negative to the positive branch (from one minimum to the other stable minimum) and viceversa, thus showing the typical hysteresis shape. To extract the spontaneous polarization we consider $E = 0$, which leads to the following solutions:

$$P_\mathrm{r} = \pm\sqrt{\frac{a_0(T_\mathrm{c} - T)}{b}}$$

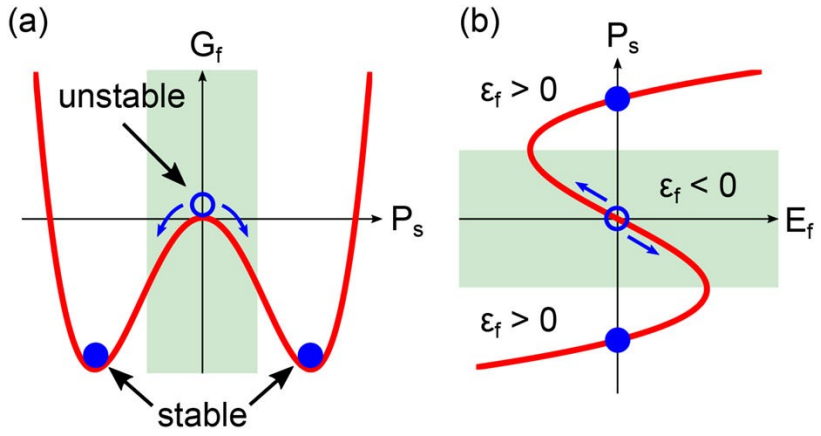

Figure 2.4: a) G-P curve for $E = 0$, b) P-E odd dependence and P_r roots [8].

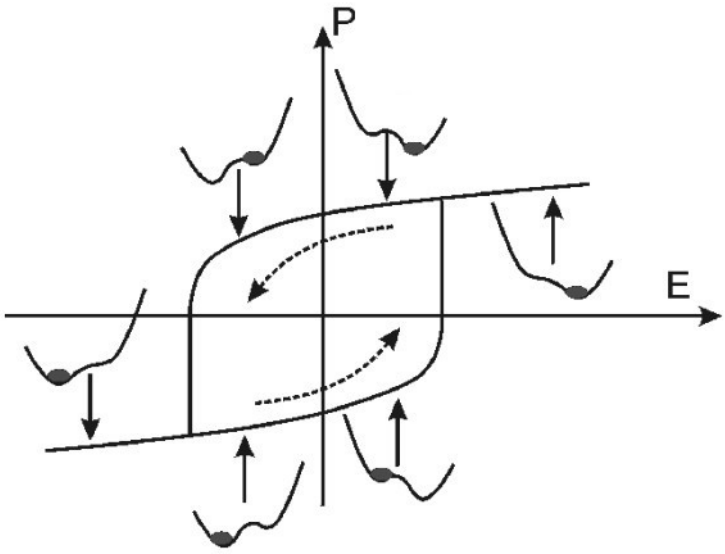

Figure 2.5: Effect of applied E on the polarization state of the ferroelectric [7].

Finally, from the P-E curve we can also calculate the polarization switching current as follows:

$$I(t) = \frac{A}{L} \int_0^{t_{FE}} \frac{\partial P(x,t)}{\partial t} dx \quad [6]$$

being A the area of the sample and t_{FE} its thickness.

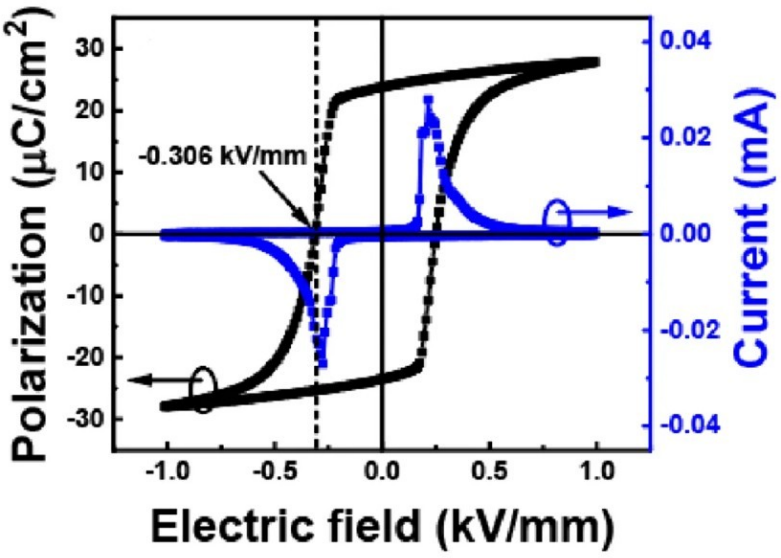

Figure 2.6: Example of polarization switching current response [9]

In figure 2.6 we can clearly notice that switching peaks in the I-V curve occur at the coercive voltage, which represent the contribution of the shifted dipoles to the total current.

2.1.2 From bulk ferroelectric materials to doped HfO_2 thin films

The first evidence of ferroelectricity was found in hydrogen-bonded materials, such as Rochelle salt (1921) and KDP (1935) [10]. However, the studies conducted in the 40s led to the discovery of ferroelectric properties in a simpler structure, that is the one of the perovskite oxide $BaTiO_3$. From that moment on, ferroelectric perovskites became very popular, especially thanks to their bistable nature which led to suggest the idea of FeRAMs (1952, by Dudley Allen Buck) and FeFETs (1963, by Jhon Moll and Yasuo Tarui) [11].
The perovskites (whose name refers to the mineral Perovskite $CaTiO_3$) have a composition ABO_3, being A and B cation elements, and their ideal structure is the one shared among most ferroelectric perovskites when observed at high temperature, that is the high symmetry paraelectric structure with space group $Pm\bar{3}m$ [12].
For example, $\mathbf{BaTiO_3}$ shows this paraelectric phase for $T > 393K$. As T decreases, the material udergoes three phase transitions, starting from the paraelectric cubic one and shifting to three ferroelectric phases: tetragonal, orthorhombic and rhombohedral. The change of phase occurs through slight displacements of the atoms, especially the Ti ones with respect to the position of the oxygen.

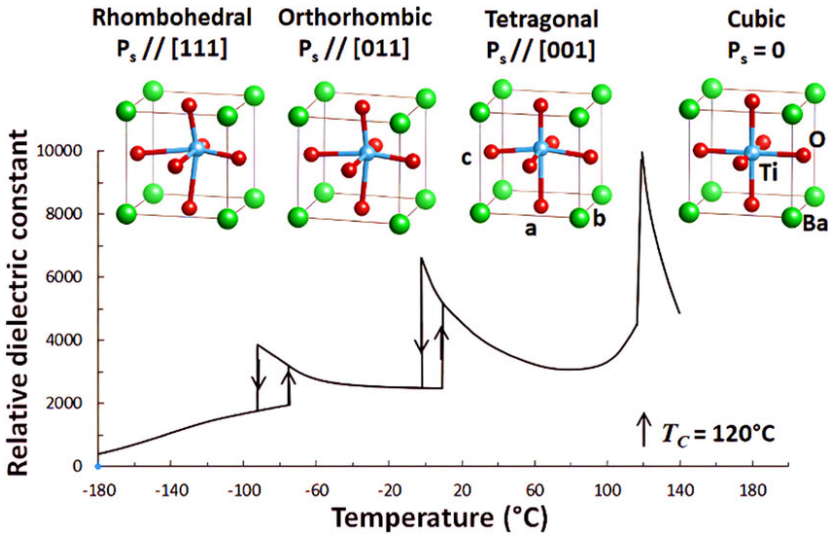

Figure 2.7: $BaTiO_3$ phase transitions [13].

After $BaTiO_3$, many studies focused on **PZT (Lead Zirconate Titanate)** were carried on in the 50s. PZT is a solid solution of Lead Titanate ($PbTiO_3$) and Lead Zirconate ($PbZrO_3$), and it rapidly became extremely popular, especially in sensors and transducers, thanks to its excellent piezoelectric properties. With respect to other perovskites, PZT (in different compositions) can count on: a wide range of dielectric constants (up to 2000), high electromechanical coupling coefficient, high Curie Temperature (~ 350 °C, thus a larger range of fabrication temperatures is accepted), high remnant polarization ($10 - 40\ \mu C/cm^2$) [14]. However, maintaining a stable ferroelectricity becomes very challenging with the increasing need of miniaturization. In fact, as the size of the ferroelectric layer decreases, the material properties start deviating from the ideal bulk ones, since the surface/volume ratio increases; as a result they start being more critically affected by the thickness, the strain, the type of substrate, the type of electrode, etc. The main reasons behind degraded performances lie in many factors (intrinsic and extrinsic) affecting simultaneously the behavior of the material due to size effect:

- each choice made in terms of **synthesis and deposition conditions** (temperature, pressure, environment, time, etc.) can significantly change the grain size, the domain size, the density of defects and impurities, which in turns will affect the ferroelectric stability and the critical thickness [11].

- depending on the substrate, on the electrode and on how the ferroelectric layer is deposited, many types of **strain** can affect the degree of polarization: strain arising from substrate clamping, epitaxial strain (due to lattice mismatch) and strain due to thermal

expansion coefficient difference (here annealing conditions are critical) [11].

- when the ferroelectric material is polarized, it generates surface charges at the interface with the electrode, which are responsible of a depolarization field: in fact, since the charge screening effect in **non-ideal metals** is not perfect (finite screening thickness), the depolarization field is only partially hindered. This has an impact on the level of remnant polarization and of course it becomes more and more critical as the thickness reduces, since the surface charge remains constant with decreasing t and the **depolarization field** rises, threatening the P_r [15].

- another issue may originate from the interaction between the ferroelectric material and the electrode, that can lead to the formation of a so-called **dead layer**. This region has properties that differ from the rest of the ferroelectric film and this may induce a reduction of the effective ferroelectric thickness. The dead layer may be caused by two main types of interaction: interface-induced relaxation (due to a mutual relaxation of the electrode and the FE film, altering the structural properties) and chemical intermixing (due to an interdiffusion between the two layers, altering the chemical properties [15]. For the dead layer, however, a trade off is typically found: as we will see also in this project, the generation of oxides between the ferroelectric layer and the metal may have some benefits. For example, it has been experimentally demonstrated that, in presence of a TiN capping electrode, the TiOx and TiON formation at the interface with ferroelectric Hafnia favour its ferroelectricity. Another example will be given by the Ti/Pt metal gate on top of the Hafnia: we used an intermediate thin Ti layer as adhesive layer between Pt and Hafnia; the formation of a very thin TiOx at the interface with Hafnia is very useful to keep the gate metal stack bonded to the gate oxide, especially when dealing with noble metals like Pt and Au. Moreover, the dielectric constant of the TiOx is extremely high, so it is basically transparent to the total capacitance of the stack. Overall, the thickness of the dead layer is so thin that the aforementioned benefits typically prevail on the drawbacks.

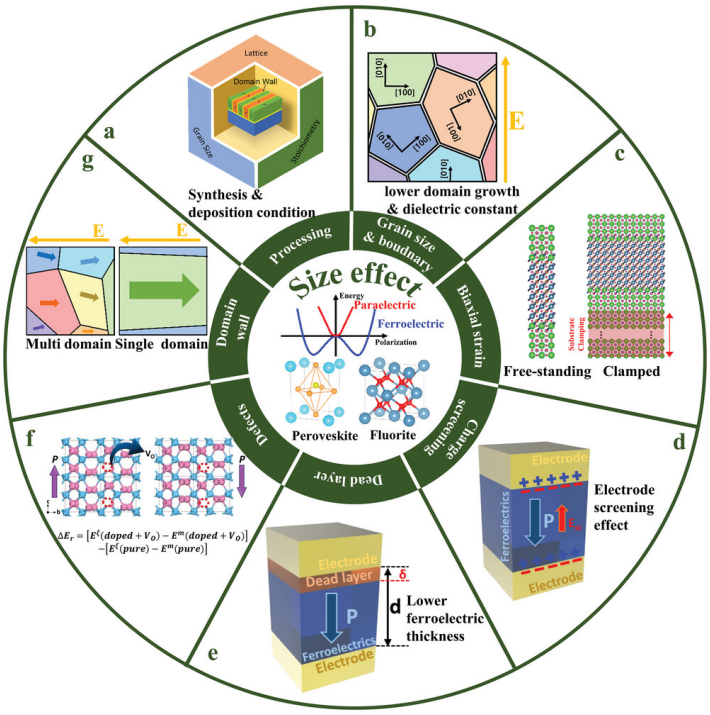

Figure 2.8: Factors affecting ferroelectricity in thin films [15] [16] [17].

These multiple phenomena at small scale negatively affected the compatibility of perovskite structure-based materials with integrated circuit technology. Hence, among all the other ferroelectric materials, the fluorite structure-based ones captured the attention of researchers as potential substitute of perovskites in thin films: in 2011, thin films of doped HfO_2 revealed an unexpected stable ferroelectricity. This discovery holds tremendous potential, as currently Hafnium Oxide is used as high-k material for gate oxides in standard CMOS technology. The reason behind its unpredicted behavior stands in the different way the polarity is formed inside the doped HfO_2: in this case the oxygen atoms are responsible for the broken symmetry, as half of them deviates from their original position in the unit cell, whereas perovskites experienced a dislocation of cations. Along with that, the tighter bondings between cations and anions with respect to the ones of perovskites contribute to maintain a stable level of polarization at small scale. Similar behavior was discovered for other Hf-based materials, such as HZO ($Hf_xZr_{1-x}O_2$) [11]. Figure 2.9 shows how the remnant polarization is preserved in thin films made of fluorite structure-based materials rather than perovskite ones, which undergo an abrupt drop instead [15].

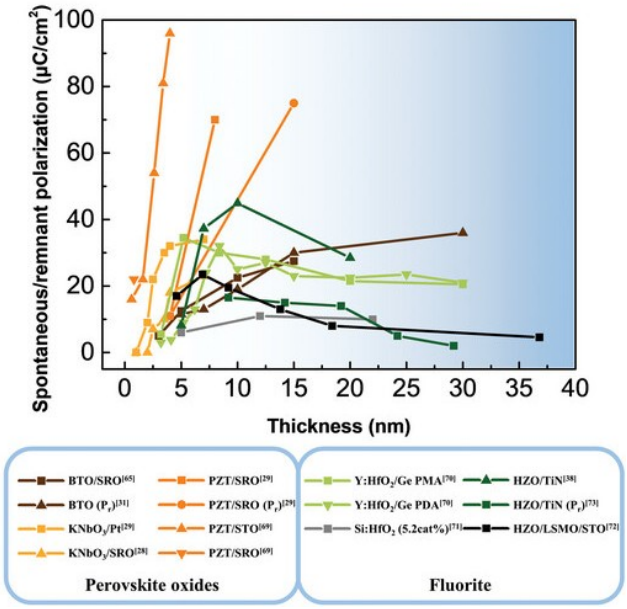

Figure 2.9: P_r values comparison Perovskite vs Fluorite structure-based oxides [15].

At this point, it is crucial to understand the mechanism behind the emergence of ferroelectricity in HfO_2. Bulk Hafnium Oxide at room temperature and ambient pressure has a monoclinic phase. With increasing temperature, it experiences two phase transitions: m-t (t=tetragonal) and t-c (c=cubic, that is the paraelectric phase reached when $T>T_{curie}$). Whereas whith increasing pressure, it goes across the oI (anti-polar) and oII (non-polar) phases (o=orthorhombic).

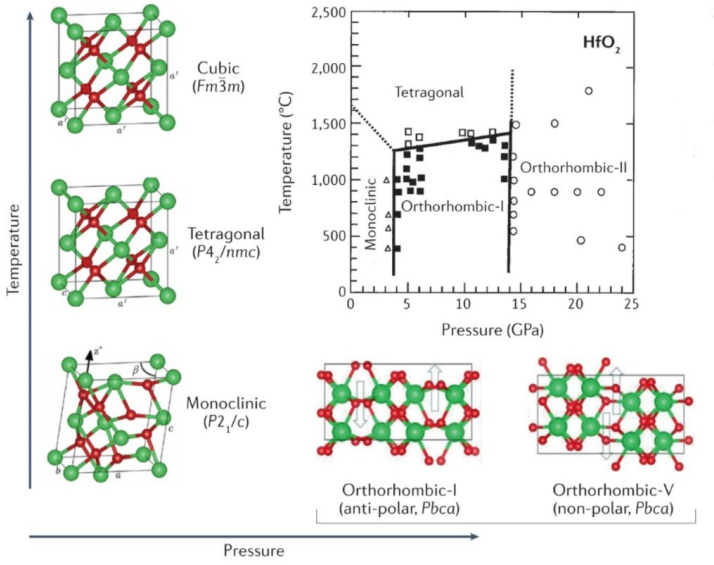

Figure 2.10: Phases of bulk HfO_2 for increasing temperature and pressure [11].

The polar ferroelectric oIII phase we are interested in does not show up in bulk but only in thin films after a proper crystallization process: the formation of oIII is based in fact on a rapid thermal process (RTP) made of two fundamental steps, that are annealing at high temperature and subsequent cooling. Once we deposit HfO_2 by means of ALD in our sample, the grown material is typically amorphous. After that, by rapidly reaching temperatures around 600 °C we can trigger the nucleation of the t phase up to a full crystallization, as the t free energy reduces very quickly with rising temperature with respect to m phase thanks to its much higher entropy [18]; finally, a rapid cooling down to room temperature leads to the t-o transition. This final outcome was not obvious, since it was experimentally demonstrated that the m phase is the most thermodynamically stable phase for all annealing temperatures; but in the end the unexpected occurrence of the metastable oIII phase has been associated to a kinetic suppression of the monoclinic phase: despite the m-phase still being the absolute minimum in free energy, the energy barrier between t and o phases is much smaller than the one separating t and m, thus favouring the t-o transition [19] [20].

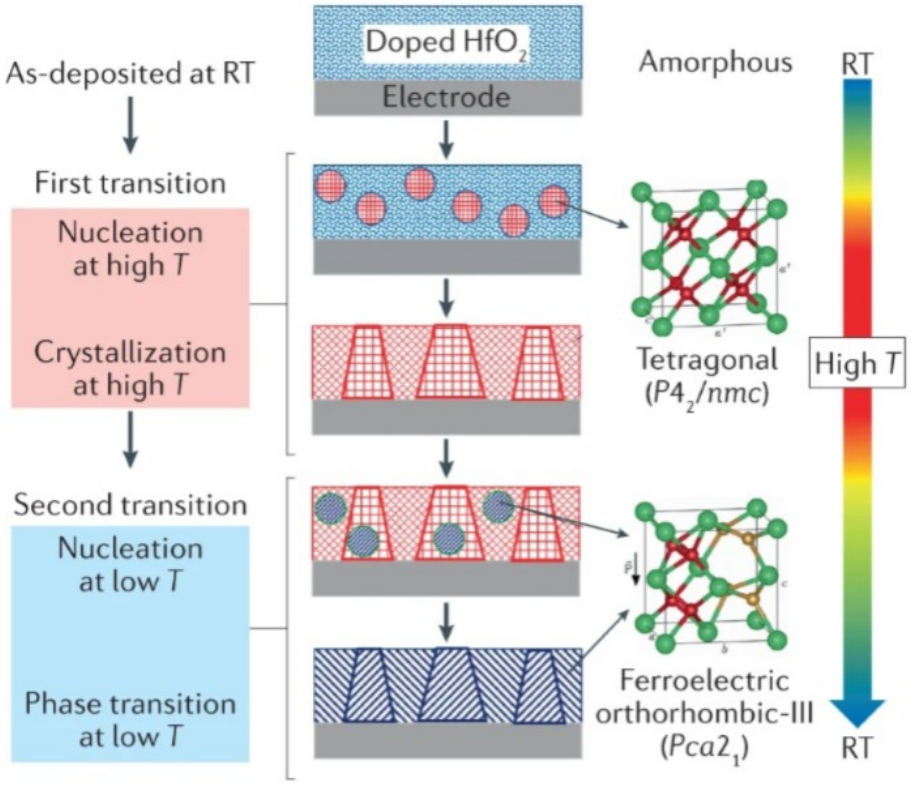

Figure 2.11: Formation of oIII ferroelectric phase during RTP [11]

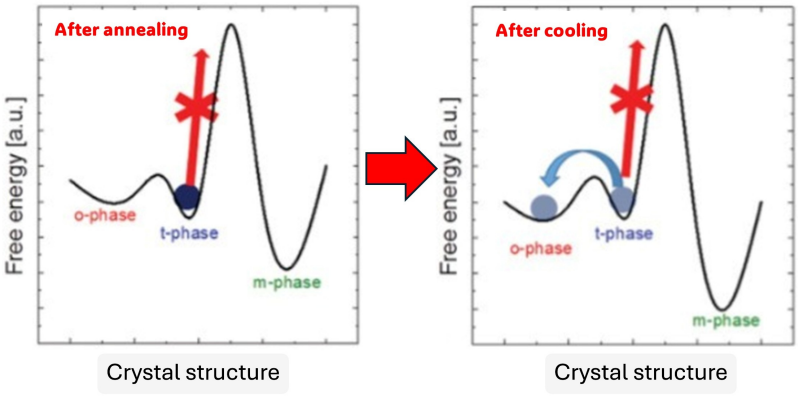

Figure 2.12: Free energy and activation energy of different phases of thin HfO_2 after the crystallization annealing and after the cooling. Adapted from [20]

As shown in figure 2.12, thanks to its higher entropy, the free energy of the t phase increases more rapidly than the o phase while cooling.

The free energies of each phase and the kinetic barrier between them are affected by many factors such as type of dopants, dopants concentration, oxygen vacancies, cooling speed, surface and interfacial energy, mechanical stress and strain:

- it was experimentally verified that using **Silicon as dopant** can induce either a ferroelectric behavior or an antiferroelectric one depending on its concentration [21]. In this project, 3 % of Si concentration will be used, thus we will expect a ferroelectric hysteresis for a crystallization temperature of 600 °C.

- the initial nucleation of the t phase at the beginning of the RTP for **thin films** occurs because the t phase can count on a **lower value of interfacial energy** if compared with the ones of m and o phases [11] [22].

- it was observed that the application of a **tensile stress** (coming both from the substrate and the electrode) favors the formation of the oIII phase, thus increasing the resulting P_r [11]. For example, a TiN capping electrode is able to induce a sufficient tensile strain, which increases with the increasing TiN thickness [22].

- the quenching speed (i.e. the **cooling rate**) should be high in order to maximize the fraction of ferroelectric phase and suppress the monoclinic one; the reason behind this is that the mechanical confinement is kept higher when employing a higher cooling speed [11] [23]. In this project, however, the machine used to perform the RTP was not provided of an active cooling system: the time needed for the heater to turn off was short enough to obtain a sufficient crystallization of the Hafnia.

- **oxygen vacancies** in fluorites favor the precursor t phase to nucleate during the RTP, which in turns enhances the oIII formation and discourages the formation of the stable m phase. For this purpose, TiN electrodes are frequently used since they have a role in aggregate oxygen vacancies inside HfO_2 near the electrode/Hafnia interface. This occurs thanks to the formation of thin TiON and TiOx layers at that interface. Moreover, the redistribution of mobile oxygen vacancies along the HfO_2 bulk may also have a role in affecting the wake up of domains (increase of switchable dipoles by means of pulsed wake up cycles) and the fatigue (degradation of P_r), thus having overall some side effects on the remnant polarization; however this is still matter of discussion [24] [25].

2.2 An example of application: FeFETs working principle

The idea behind FeFETs is to integrate ferroelectric materials in the gate stack of traditional MOSFETs: the ferroelectric behavior has an impact on the device operations and allows to tune the conductivity of the channel by means of polarization switching. A first FeFET based on an n-channel was realized by Shu-Yau We et al. at the Research Laboratory of Westinghouse Electric Company, Pittsburgh in 1974, where two threshold voltages were discovered: after applying a sufficient electric field (E>Ec) the device entered a first operation state (identified by a certain threshold Vth_1 and a certain ON drain current level ID_1) and persisted in that state even after turning off E. By reversing the electric field the device entered a second non-volatile state (identified by Vth_2 and OFF drain current ID_2). After this discovery, FeFETs have been intensively studied especially for their non-volatility, low power consumption, high endurance and high density, which make them suitable for low-power non-volatile memories and a worthy and ambitious alternative to flash memories. [26] [27] [28].
Different configurations for FeFETs are possible. The easiest example is the MFS (Metal-Ferroelectric-Semiconductor) stack, which however ends up having some drawbacks despite its simple layout: the growth of ferroelectric materials directly on Silicon does not guarantee a high interface quality and this leads to several problems, from mobility degradation to high depolarization fields. A more valid alternative to MFS is represented by the MFIS stack, which will be the subject of study for this project. By means of an intermediate thermally grown SiO_2 layer, we are able to improve the interface quality at the cost of introducing a low-dielectric constant non-switching layer, which is the main origin of depolarization field and degraded retention (together with the dead layer which may arise at the top electrode) [26] [27] [28].

2.3 Main oxide defects

In order to better understand the non-idealities affecting the ferroelectric device operation as well as the polarization dynamics, it is important to distinguish the nature of different oxide defects [29]:

- **Fixed bulk charges (ρ_{ox})**:
  they are charges found inside the oxide, typically due to the injection of electrons and holes during the device operations or when radiating the sample. They are not in electrical communication with the channel but can produce a shift of the flatband voltage V_{FB} [29] [30] [31].

- **Fixed Oxide Charges (Q_f)**:
  also called slow states, they occur due to an incomplete thermal oxidation of some Si atoms, which remain inside the gate oxide as the thermal growth proceeds. They do not communicate with the channel but still are responsible of a flatband voltage shift. Other process-induce fixed charges may arise also at the SiO_2/hk-dielectric interface and we will indicate them with $Q_{f,hk}$ [29].

- **Interface traps at the Si/SiO_2 interface (Qit)**:
  also called fast surface states or P_b centers, they are due to structural defects at the Si/SiO_2 interface. During the thermal oxidation, an interface trap is formed when the Si atoms does not bind to oxygen and exhibits a dangling bond [29]. These types of defects introduce energy levels inside the gap, thus becoming G/R centers for electrons and holes. They are responsible for leakage current, low-frequency noise, lower mobility, introduction of a shift in V_{FB} and variation of the capacitance in low frequency [29].Those traps with energy distribution between the Fermi level and the C.B. act as acceptors (neutral when electrons are missing, negatively charged when trapping them) while those between the V.B. and the Fermi level act as donors (neutral when trapping electrons, positively charged when releasing them). Differently from $Q_{f,ox}$, these traps can exchange carriers with the Si substrate; however, since both $Q_{f,ox}$ and Q_{it} can influence the flatband voltage, we will sum them up and treat them in general as interface charges [29].

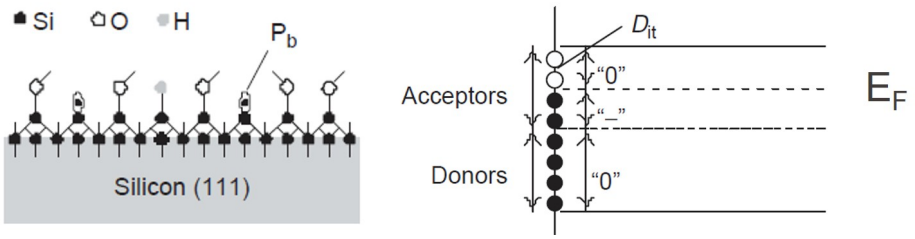

Figure 2.13: Left: interface traps due to dangling bonds of Si atoms. Right: donor and acceptor interface traps

- **Mobile Oxide Charges**:
  they are due to contamination of ionic impurities during fabrication, especially of alkali cations (ex. Na^+, Li^+, K^+). They can diffuse through the gate oxide and may cause an unstable gate biasing. Mobile charges also involve charged oxygen vacancies, that can affect the polarization switching causing the pinning of ferroelectric domains [29] [32].

- **Interface traps at the SiO_2/hk-dielectric interface**:
  they are due to the different conductivities of the insulators. However, their effect is typically implicit in the experimentally determined hk dielectric constant [29].

- **Border traps**:
  they are near interface traps (NIOTs) that can communicate with the channel via tunneling. The most frequent border traps are E' centers, i.e. oxygen vacancies due to a trivalent Si atom. They are located at $2 \div 3$ nm from the channel. Their effect on the capacitance will be presented in a dedicated chapter [29].

Chapter 3

Fabrication

3.1 MFIS

During the project, three different MFIS gate stacks were fabricated and characterized, as three different gate metals were used:

- ~~TiN~~ $\rightarrow$ Ti + Pt
- ~~TiN~~ $\rightarrow W$
- TiN

where, for the first two stacks, the TiN was used only for the crystallization of the hafnia and was subsequently wet etched.

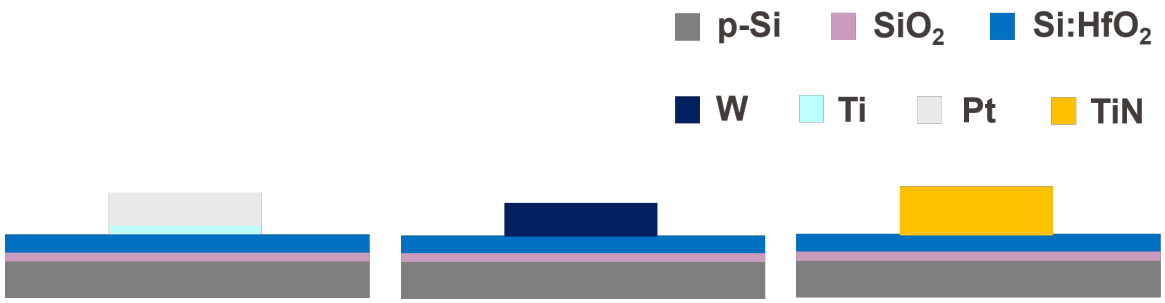

Figure 3.1: MFIS stacks layout. From left to right: Ti+Pt, W and TiN gate metal

For each MFIS structure, six chips were fabricated by changing the deposited Si-doped HfO_2 thickness and by either avoiding or performing the post-metalization annealing :

Si-doped HfO_2 thickness [nm]	Post-metalization annealing	
12	w/o	w/
16	w/o	w/
20	w/o	w/

Table 3.1: MFIS chips with different Si-doped HfO_2 thickness and w/ or w/o post-metalization annealing

Figure 3.2: Chips with MFIS stacks. From left to right: W, Ti+Pt and TiN gate metal. Per each metal: 3 chips with and 3 chips without post-metalization annealing

The thickness of the SiO_2 gate oxide was left unchanged for all the chips ($\simeq 5\,nm$) and the real value of the EOT was precisely extracted from the measured CV curves. The purpose of performing a post-metalization annealing in forming gas (N_2/H_2) is to passivate the dangling bonds at the interfaces of the MFIS stacks by favoring the diffusion and binding of hydrogen atoms, thus potentially reducing the overall number of defects [33] [34]. The fabrication was carried out on a 4" wafer consisting of a p-type Si <100> substrate of 525 μm.

The process flow of the stacks for the three gate metals was very similar. In the following, the fabrication steps for the MFIS with Ti+Pt will be presented at first and the slight changes concerning W and TiN will be specified in the end. All details about the equipment comes from both the CMi (Center of MicroNanoTechnology) website [35] and from what was learnt during these months in cleanroom.

3.1.1 Dry thermal oxide growth

The 5 nm of SiO_2 were grown in the Centrotherm furnace of the Cmi. This is a service of the CMi done under request. The growth is carried out in an atmosphere of 90 % of N_2 and 10 % of O_2 with a pressure of 1 bar. The temperature is gradually increased up to a maximum of

900°C, according to the following ramps:

- 10 °C/min from 20 °C to 880 °C
- 5 °C/min from 880 °C to 890 °C
- 2 °C/min from 890 °C to 895 °C
- 1 °C/min from 895 °C to 900 °C

Once reached 900 °C, the heater is switched off for a passive cooling.

3.1.2 Si:HfO_2 ALD

The atomic layer deposition (ALD) process was used to deposit Si:HfO_2 with a very precise thickness. For this purpose, the machine BENEQ TFS200 was employed. The deposition was performed under vacuum ($4 \div 8$ mbar). The temperature of the chamber was 300 °C. The two precursors for Hf were TEMAH (kept at 80 °C) and H_2O (at RT) while the precursors for Si were BTBAS and O_3 (both at RT). Each deposition cycle consists of four steps:

- Pulsed injection of the first precursor in the reaction chamber, so that it is chemisorbed by the sample surface.
- Purging of the chamber by means of the inert gas N_2 in order to remove the excess of precursor 1
- Pulsed injection of the second precursor in the reaction chamber, so that it reacts with the chemisorbed first precursor at the sample surface. After the reaction, the monolayer is formed and a byproduct is generated as well.
- Purging of the chamber with N_2 in order to remove the excess of precursor 2 and the byproduct of the reaction.

Each cycle is repeated several times in order to reach the desired thickness. In this project, the Si:HfO_2 thin film was obtained by performing 16 deposition cycles of Hf, 1 deposition cycle of Si and again 16 deposition cycles of Hf (Hf:Si:Hf, 16:1:16). This proportion guarantees a 3 % of Si doping. In order to reach 12 nm, 16 nm and 20 nm of Si:HfO2, this sequence of cycles was repeated respectively 5, 7 and 9 times. Together with our wafer, a dummy Si chip was put in the chamber. In this way, the deposited thickness of the Si:HfO2 could be precisely measured by means of the ellipsometer Woollam RC2. The ellipsometer sends a linearly polarized light on the sample and receives a reflected elliptically polarized light. By measuring the reflectivities of the parallel and perpendicular components, the refractive index and the thickness of the thin film are extracted. In our case, the presence of TiN below the hafnia prevented a correct measurement because TiN acts as a metal-like absorber. This is why a Si dummy chip was needed.

3.1.3 TiN sputtering

A layer of 24 nm of TiN was sputtered (only for the crystallization of the hafnia) by means of the machine DP 650. The machine uses a DC source to make Ar ions hit the TiN target (cathode). In this way our target was dislodged and deposited on the sample surface. This process was performed at RT and under vacuum. The deposition rate of TiN is 0.9 Å/s. Hence, 267 s were needed to reach 24 nm.

3.1.4 Protection PR coating and dicing

Before dicing, the wafer was covered with 5 μm of AZ resist in order to protect it from the Nickel blade. The resist was coated by the automatic coater EVG150, after 10 minutes of dehydration. Then the backside of the wafer was glued to a plastic cover, that was useful to carry the chips after the cut. After the dicing, 64 square chips of 10 mm $\times$ 10 mm were obtained. The PR and the glue were then removed using acetone. After that, the chips were cleaned with isopropanol (IPA).

3.1.5 Rapid Thermal Process (RTP)

The RTP is a crucial step since it is responsible of the crystallization of the hafnia, as already discussed previously. The temperature used for the crystallization was 600 °C for 2 minutes in N_2. This process was possible thanks to the machine RTP JETFIRST 200. The chips were positioned on a Si wafer used as a carrier. The samples were heated by means of a furnace made of infrared lamps and their local temperature was measured by a thermocouple in contact with the backside of the wafer. It was important to verify that the thermocouple was actually in contact with the wafer, since the furnace and the thermocouple work as a feedback system (proportional-integral-derivative or PID controller): if the measured temperature is too low with respect to the one indicated in the loaded recipe, the furnace may increase the temperature up to unwanted values to compensate the error. For this reason, a dummy run was performed at first by loading only the carrier wafer. During the dummy run it was verified that the measured temperature followed the desired one. Moreover, the power of the heater was monitored as well: it was expected to experience a sharp increase when switching to 600 °C and then to stabilize at around 25 % for the rest of the process. Details about the recipe loaded on the machine are reported:

RTP			
# step	**duration**	**pumping**	**temperature**
1	50 s	vacuum	RT
2	60 s	purging (N_2)	RT
3	20 s	//	600 °C (rise)
4	120 s	//	600 °C
5	12 s	//	RT (switch off)
6	30 s	purging (N_2)	RT

Table 3.2: RTP recipe for Si:HfO_2 crystallization

At the end of the process, there was a cooling down of 6 minutes before unloading the sample from the chamber.

Figure 3.3: Picture of the RTP JETFIRST200 [35]

3.1.6 TiN wet etching

After the RTP, the TiN was wet etched with a solution consisting of NH_4OH:H_2O_2:H_2O (1:2:50), also called standard clean 1 (SC1) solution, at 50 °C for 5 minutes. The hydrogen peroxide H_2O_2 acts both as oxidant and as complexant of Ti^{4+} (forms complexes which are soluble in water). The role of ammonium hydroxide NH_4OH is to increase the pH (OH^- groups) and favors the generation of HO_2^- peroxyl radicals, which are more reactive and increase the etching rate [36] [37] [38].

3.1.7 Photolithography: PR coating, Direct Laser Writing (DLW) and development

For the patterning of the MFIS stacks, one photolithographic step was sufficient. The chips were prepared with 10 minutes of dehydration at 135 °C. After that, they were coated by means of the manual coater Sawatec SM-200. Two resists were used: LOR 5A (lift-off resist) and AZ 1512 HS. In order to deposit 400 nm of LOR 5A, the chips were coated with 6000 rpm (rounds per minute) and subsequently cured on the hotplate at 180 °C for 4'10". Soon after the LOR 5A, 1.05 μm of AZ 1512 HS were coated using 5000 rpm. Then, a softbake at 100 °C for 1'30" was performed.

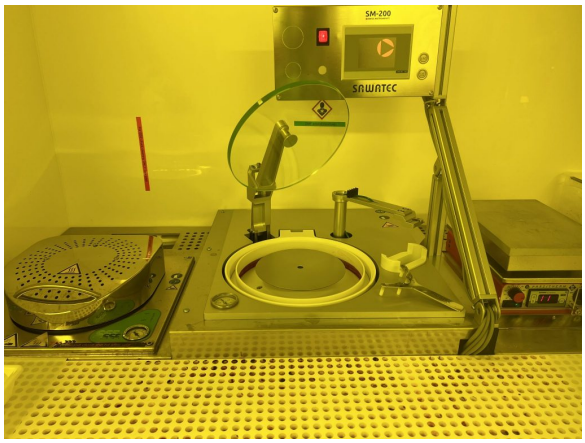

Figure 3.4: Picture of the manual coater Sawatec SM-200 (center), the hotplate used for the dehydration (left) and the hotplate used for the softbake (right) [35]

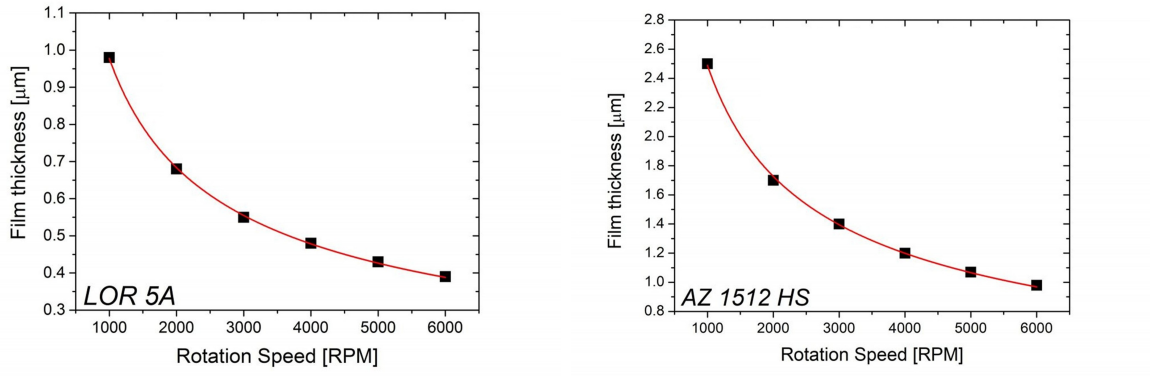

Figure 3.5: Spincurves of LOR 5A (left) and AZ 1512 HS (right) [35]

For the exposure of the chips, the mask-less aligner MLA150 was employed. This machine converts the design prepared on a CAD tool and print the desired patterns directly on the sample (direct laser write DLW). In our case, KLayout was used as CAD tool, which saves the

design on a .gds file. The design consisted of 13 × 15 square patterns. Each row contained 3 sets of 5 squares, having side lengths equal to 200 μm, 150 μm and 100 μm. The chips were exposed with a 405 nm laser diode (h-line). The setting of dose and defocus depended on the type of resist and on its thickness. Moreover they were constantly updated by the staff after each calibration. In our case, the dose was around 40 mJ/cm^2. The defocus was between 0 and -3 (a negative defocus pushes back the focal point from the middle of the resist). Finally, the development of the resist was done in AZ 726 MIF for 75 s, followed by 1 min. in water.

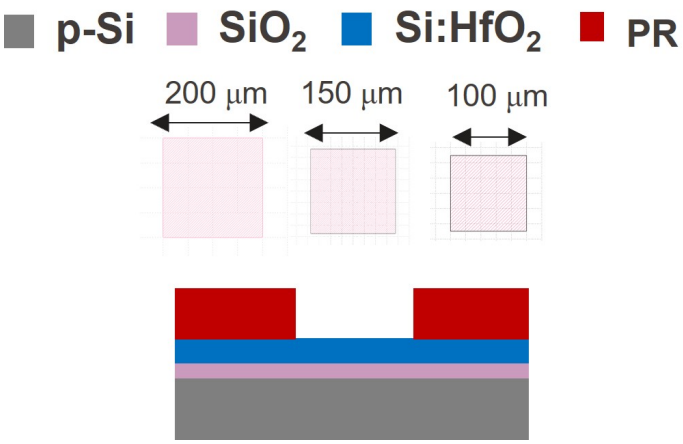

Figure 3.6: Photolithographic pattern for MFIS stacks. Square patterns with the 3 different areas

3.1.8 Resist residue descum

In order to ensure that no resist residues remained stuck within the patterns, a resist descum was performed for 30 s at low power (200 W) using the TeplaGiGAbatch. The chips were positioned on a quartz plate and then loaded in a vacuum chamber. The machine uses O_2 plasma. The use of O_2 was not a problem in MFIS fabrication. However, in the MFM the risk of oxidizing TiN electrodes was too high and this descum was avoided whenever possible.

3.1.9 Ti+Pt evaporation and lift-off

The Ti+Pt gate metal was deposited using the e-beam evaporator Leybold Optics LAB 600H. The chips were mounted on a carrier wafer by means of a Kapton tape. The wafer was then mounted on one of the 4 segments of the evaporator holder placed on the top part of the chamber. In this process, most of the fabrication time is spent in creating the vacuum (1.5×10^{-6} mbar). Among all the processes, this one was the slowest since it lasted around 3 h. Normally, the entire process requires between 2 h and 2 h 30 min., but the creation of the vacuum may need more time if the chamber remains open for too long while loading the sample. The Ti and Pt to deposit are hosted in two crucibles and they can be evaporated in

sequence by rotating the crucible platform without breaking the vacuum. This is very useful since Ti oxidizes very easily when exposed to air. The evaporation occurs by means of an electron beam (emitted by an electron gun) accelerated and deviated towards the material. The final thicknesses of Ti and Pt were respectively 3 nm and 30 nm, deposited with a rate of $4\,\text{Å}/s$.
Afterwards, the chips were immersed in the remover SVC-14 and left for 24 h for the lift-off of the as-deposited metals.

3.1.10 Post-metalization annealing

As already mentioned at the beginning, half of the chips was subject to a post-metalization annealing in forming gas (N_2/H_2) trying to passivate the dangling bonds across the stack with hydrogen. This process was carried out in the RTP JETFIRST200 at a temperature of 300 °C for 15 minutes. Details about the recipe are reported:

Post-metal. annealing			
# step	**duration**	**pumping**	**temperature**
1	40 s	vacuum	RT
2	50 s	purging (N_2)	RT
3	60 s	vacuum	RT
4	90 s	N_2/H_2	RT
5	20 s	N_2/H_2	300 °C (rise)
6	900 s	N_2/H_2	300 °C
7	30 s	N_2/H_2	RT (switch off)
8	600 s	purging (N_2)	RT

Table 3.3: RTP recipe for post-metalization annealing in forming gas

3.1.11 W and TiN process flow variations

Unlike Ti+Pt, W and TiN were not evaporated. Instead, they were sputtered. In particular, concerning the MFIS with W, its gate metal was sputtered for 70 s, to obtain a W layer of 24 nm (dep. rate of 3.4 $\text{Å}/s$). In the MFIS having TiN as gate metal, the initial 24 nm of TiN were not wet etched after the RTP and a second TiN layer of 24 nm was sputtered for 267 s, so to obtain 48 nm of TiN in total. Moreover, this time the deposition processes preceded the photolithography: hence, in order to obtain the square patterns according to the KLayout design already presented in 3.1.7, an inverted design was used. Since no lift-off was performed, only AZ 1512 HS was coated (1.05 μm with 5000 rpm + 1 minute of softbake at 100 °C). The exposure line was again 405 nm. The dose was $\simeq 70\,mJ/cm^2$. Since an inverted design was printed this time, an exposure area larger than the chip area was selected to avoid the presence of resist along the borders of the chip after development. The development was carried out using AZ 726 MIF for 32 s, followed by 1 minute in water.

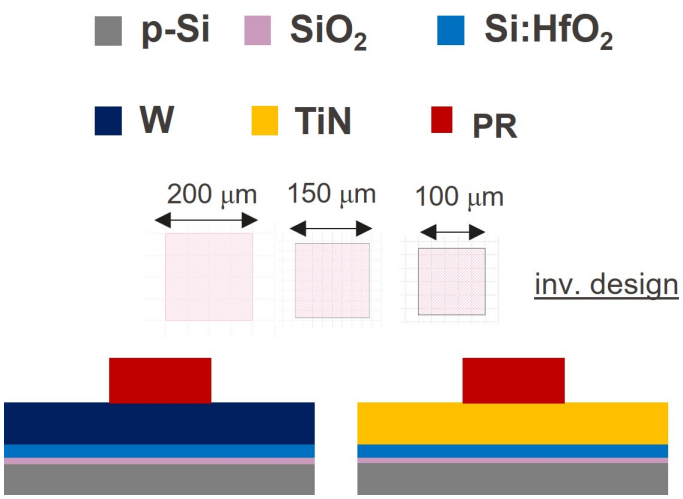

Figure 3.7: Photolithographic pattern for MFIS stacks with W and TiN gate metals (inverted design)

After the photolithography, this time the resist was used to protect the underlying gate metal from dry etching. In particular, the W was etched by SF_6 plasma, while the TiN was etched using a Cl_2/BCl_3 plasma.

3.1.11.1 Dry etching of TiN

The dry etching of TiN was performed by means of the PlasmaPro100 Cobra. This machine is a plasma etcher that uses mainly chlorine chemistry to etch metals under vacuum. In fact, TiN was etched with a Cl_2/BCl_3 plasma. By means of the quickstick, the chips were glued on a carrier wafer made of Si and 200 nm of dry thermal SiO_2. For a better etching, the cleaning of the chamber was done at first, after loading a clean Si wafer. Then, one dummy run was performed to stabilize the plasma before the actual run. The machine uses an endpoit detection based on a spectrometer to monitor when a certain material has been completely etched. In particular, the spectrometer is used to control the change in concentration of a specific material by monitoring the emission wavelength. While etching, the tool provides three plot: the raw signal, the elaborated signal and its derivative. To avoid an overetch of the hafnia, the etching had to be stopped on the fly when the raw signal dropped. In fact, the elaborated signal and its derivative were affected by a delay and relying on them was too risky. In the case of MFIS, an overetch of the hafnia was not a big issue since the hafia surrounding the pattern was not part of the stack (in the MFM, instead, this process was more critical). In the end it was verified that the etch rate of TiN is 2 nm/s (very fast), so that 48 nm were removed after $\simeq$ 24 s.

After the dry etching, a descum of 1 minute at low power was performed in the TeplaGiGA-batch to remove part of the resist that was cooked by the Cobra. Finally, acetone was used to

definitively remove the rest of the resist.

3.2 MFM

In order to verify and study the ferroelectric behavior of the Si:HfO_2 thin film, an MFM capacitor was fabricated. Moreover, a staggered geometry for the electrodes was used to prevent the breaking of the hafnia when probing the capacitor or during the wire bonding of the contacts. To realize this geometry, four photolithographic steps were needed. The fabrication was carried out on a 4" wafer made of 525 μm of a p-type Si <100> and 100 nm of dry thermal SiO_2. The chosen thickness for the hafnia was 12 nm. For the electrodes TiN was used, while the contacts were made using a Ti+Pt stack.

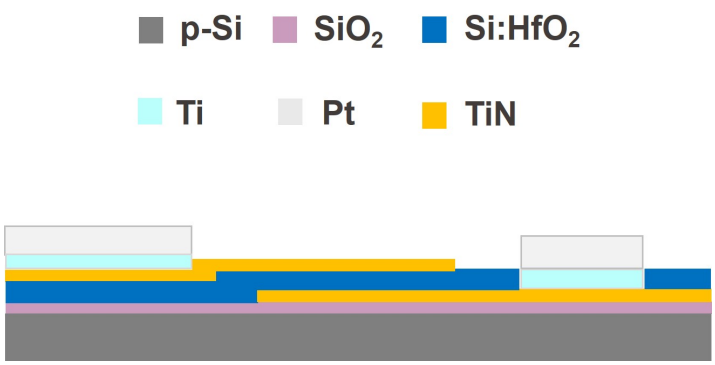

Figure 3.8: MFM layout

Since almost all the processes used in the MFM fabrication were already presented in the MFIS section, the description of the MFM process flow will be more cohesive and seamless, without dedicating chapters to the already introduced equipment.

The first step of the MFM fabrication was the deposition of the TiN bottom electrode. 12 nm of TiN were deposited by sputtering for 133 s. Afterwards, the **first photolithography** was performed: after 10 min. of dehydration, 1 μm of AZ resist was coated by the automatic coater; then, the exposure was carried out in the MLA150, using 405 nm as light source and 70 mJ/cm^2 as dose. An inverted design was selected in order to cover the TiN with rectangular patterns. Moreover, one of the most important differences with respect to the MFIS process was the need of the **alignment**, due to the presence of more than one photolithographic step. For this purpose, one square marker having side length of 10 μm was positioned at each corner of the chip design.

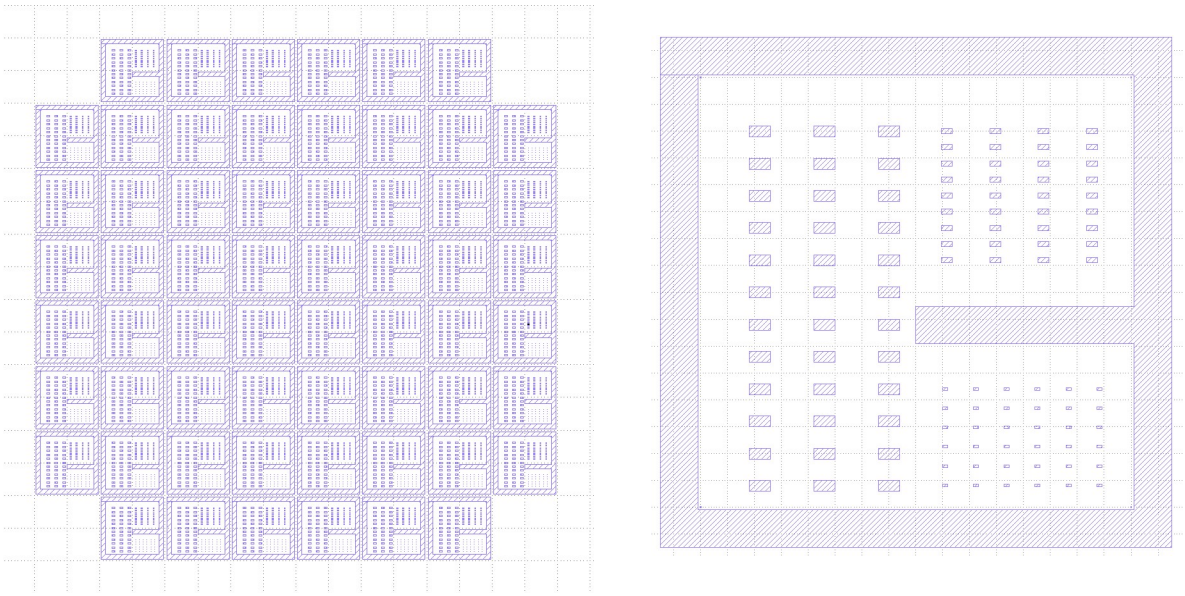

Figure 3.9: MFM first photolithographic layer on KLayout. Left: wafer view (actual printed design). Right: single chip view. The square markers are extremely small and placed at each corner of the chip

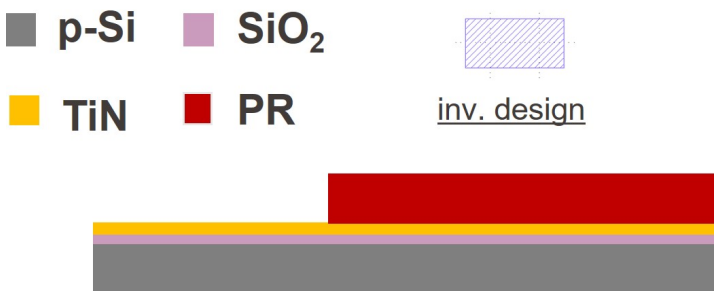

Figure 3.10: First photolithographic pattern for the MFM capacitors

After a resist residues descum for 30 s at low power, the TiN was dry etched with a Cl_2/BCl_3 plasma for 11 s. Since the etching rate is very fast (2 nm/s), 11 s were too much for a TiN layer of 12 nm. This probably caused an overetching of the SiO_2 and affected some choices done in the following steps. Afterwards, the resist was removed first with a descum at low power for 1 min. and finally by dipping the wafer in acetone. IPA was used to clean the wafer in the end. The ALD was then performed to deposit a conformal layer of 12 nm of Si:HfO_2. The process was exactly the same used for the MFIS (Hf:Si:Hf cycles, 16:1:16 $\times$ 5 to reach a thickness of 12 nm). After that, the TiN top electrode was deposited by sputtering. This time, the choice of the thickness to deposit was crucial: the patterning of the bottom electrode introduced a step and the top electrode had to span it to prevent an open circuit. Without overetching of the SiO_2, the step would have been of 12 nm (bottom electrode thickness). To

guarantee the spanning of the step considering the overetching, 36 nm of top electrode were deposited (400 s).

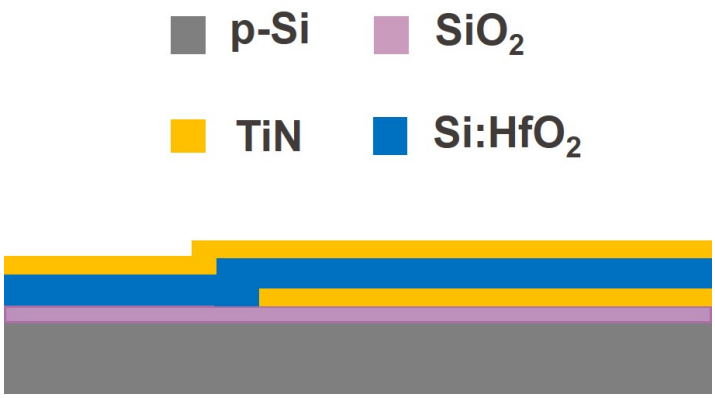

Figure 3.11: Deposition of the TiN top electrode of the MFM capacitor

Then, the dicing of the wafer was carried out after coating it with a protection PR of 5 μm. Square chips having side length of 10 mm were obtained. The PR was subsequently removed with acetone. After that, the RTP was performed to crystallize the hafnia (600 °C for 2 min. in N_2). Next, a **second photolithography** was carried out for the patterning of the top electrode. The process was the same as the one used for the MFIS stacks with W and TiN gate metals (AZ 1512 HS only). The only difference was the alignment procedure that consisted in centering each marker using the high resolution mode. The recognition of 3 markers was sufficient to define the plane of the chip, in case one marker was not visible because covered by non-uniform resist.

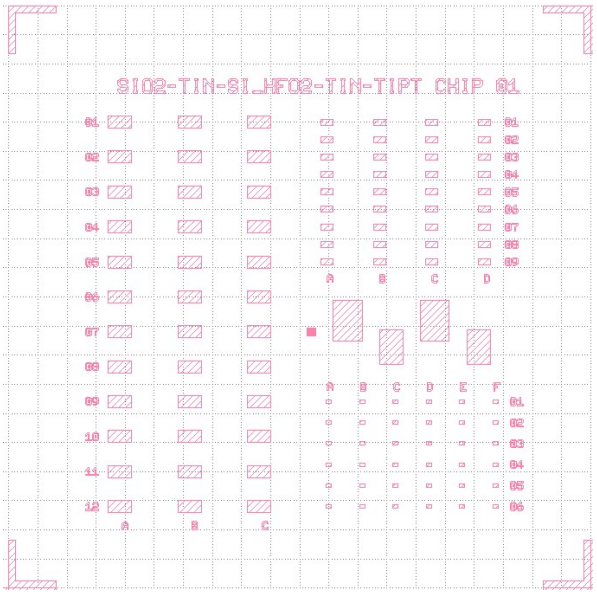

Figure 3.12: MFM second photolithographic layer on KLayout

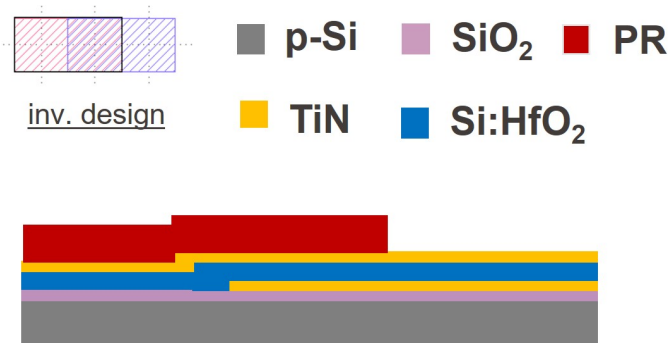

Figure 3.13: Second photolithographic pattern for the MFM capacitor

Then a resist descum at low power for 30 s was performed. Afterwards, the top TiN was dry etched with the usual Cl_2/BCl_3. However, this process required a very precise timing: the plasma was not selective for TiN since the underlying hafnia had an etching rate of 1 nm/s. The 36 nm of top TiN were etched in $\simeq$ 18 s. Finally, the resist was removed with 1 min. at low power in the TeplaGiGAbatch followed by immersion in acetone for few seconds. Next, a **third photolithography** was carried out with the same parameters as the previous one. The aim of this photolithgraphy was to pattern a square opening on the hafnia in order to create the contact for the bottom electrode.

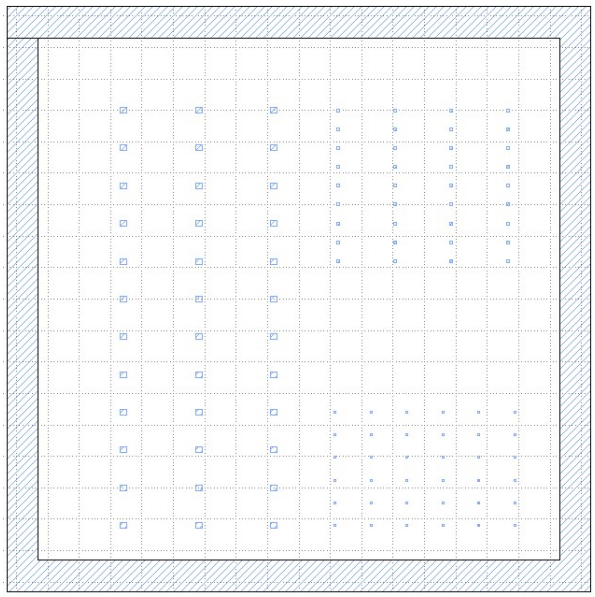

Figure 3.14: MFM third photolithographic layer on KLayout

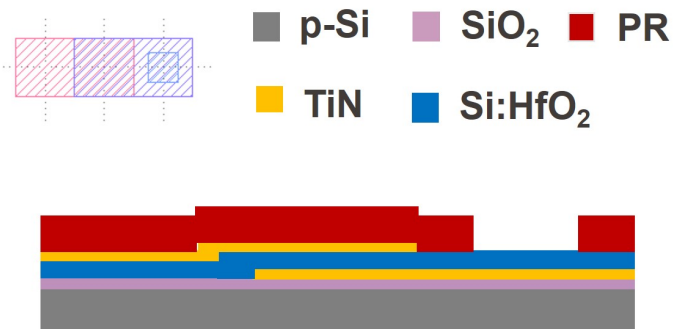

Figure 3.15: Third photolithographic pattern for the MFM capacitor

What followed next was one of the most challenging part. In order to etch the hafnia, two types of processes were tried. First, wet ethcing in BHF (buffered hydrofluoric acid) was performed in two sessions of 10 min. each (between one session and the other, the third photolithographic step was repeated). However, this was not sufficient to etch the hafnia. Hence, dry etching with IBE (ion beam etching) was performed.

3.2.1 Ion beam etching (IBE)

This process was carried out using the Veeco Nexus IBE350. In this case there was a better landing condition than the top electrode etching, since for the IBE the etching rate of the underlying TiN is much smaller with respect to the hafnia. The machine uses a primary beam of accelerated Ar ions. Once the sample is bombarded, the emitted secondary ions

are collected and analyzed by a secondary ions mass spectrometer (SIMS). When monitoring the output signal of the SIMS, a large peak was observed after $\simeq 50s$ on the signal that was associated to a large mass (hafnium is much more massive than the other elements present in the stack). This peak represented the successful etching of Si:HfO_2, thus the run was stopped. The absence of hafnia was subsequently verified by testing the sample with a multimeter at the borders of the chip $\simeq 800\ k\Omega$ were measured, which are compatible with TiN. Moreover, its less bright golden color was a further confirmation of the successful etching of hafnia.

After the IBE, a prolonged immersion in acetone was used to remove the resist. This was not sufficient to eliminate the cooked resist, thus a descum at low power for 1 minute became necessary, despite the risk of TiN oxidation. Finally, a **fourth photolithography** was used to create small square openings for the two contacts. For this step, the LOR 5A + AZ 1512 HS recipe was employed (already discussed in the MFIS with Ti+Pt gate metal).

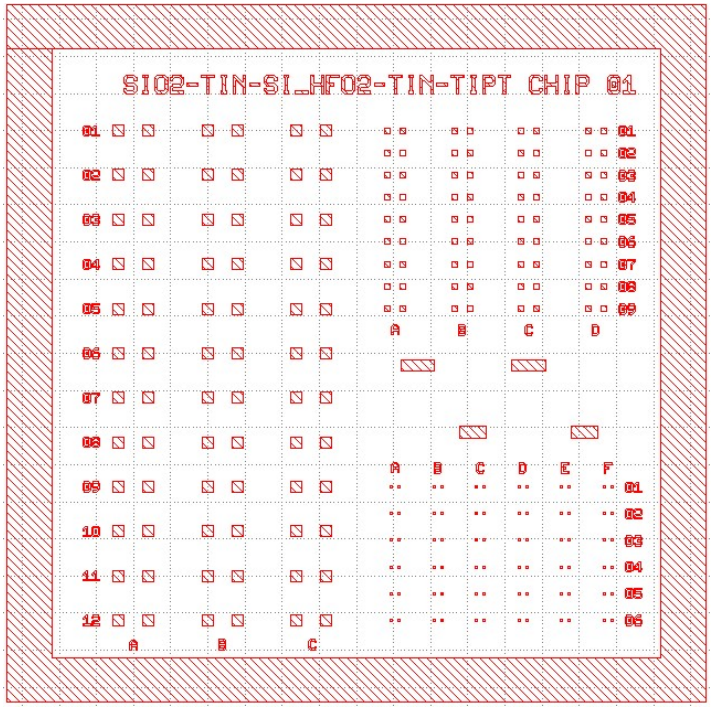

Figure 3.16: MFM fourth photolithographic layer on KLayout

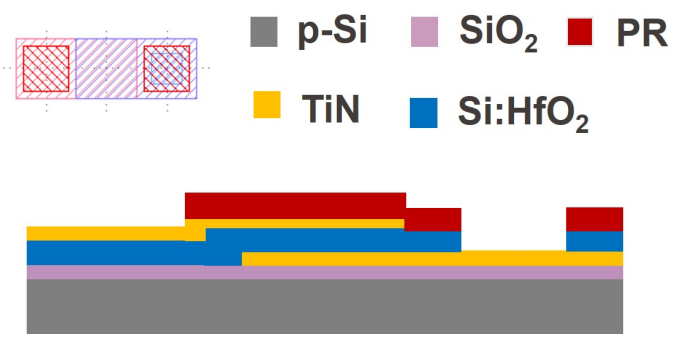

Figure 3.17: Fourth photolithographic pattern for the MFM capacitor

The metallic contacts of Ti+Pt were deposited by sputtering. In particular, 3 nm of Ti and 30 nm of Pt were deposited, with a deposition rate of respectively 3.3 Å/s and 6.7 Å/s. The fabrication ended after the immersion in SVC-14 for $\simeq 24\,h$ for a proper lift-off.

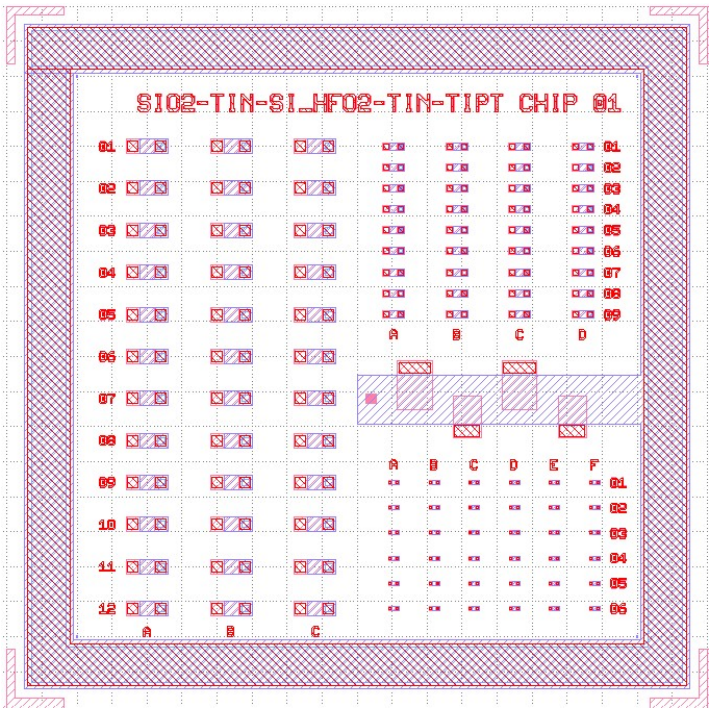

Figure 3.18: MFM design with all photolithographic layers on KLayout

Chapter 4

Electrical testing and data analysis

4.1 Testing of MFIS stacks

4.1.1 CV curves measurement at LF (low frequency) and HF (high frequency)

C-V curves can be really useful to extract important information out of a MOS structure (MFIS, in our case), such as equivalent oxide thickness (EOT), flatband voltage (V_{FB}), threshold voltage (V_{th}), metal work function (Φ_M), doping distribution ($N_{a/d}$), depletion width (W_{dep}), interface trap density (D_{it}) and possibly the bulk charge (ρ) throughout the stack. The measurements were carried out by means of a Cascade Microtech probe station, the multimeter Keithley 4200A-SCS Parameter Analyzer and its software Clarius. Two voltage sources were used: a sweep over DC voltages overlapped with an AC voltage signal. By changing V_{DC} we make the capacitor go through different operation modes, while the V_{AC} sets the frequency at which we stimulate the DUT [39]. The three operation modes for an NMOS (so with p-type Silicon) can be described as follows:

- **Accumulation**
  By applying a negative voltage between the top electrode and Silicon, electrons accumulate at the metal/oxide interface, thus inducing an opposite charge at the oxide/semiconductor interface. Therefore, more holes start to populate the valence band of the p-type semiconductor near the oxide. This buildup of majority carriers is called accumulation. The accumulation mode is typically used to measure the oxide capacitance, since in this region the overall capacitance is almost equal to Cox and the curve remains almost flat in the strong accumulation range.

■ **Depletion**

The depletion condition occurs when the Silicon is depleted of majority carriers (holes, in our sample) at the interface with the oxide in order to balance the positive charges that are formed at the metal/oxide interface once a positive voltage is applied. The depleted region acquires a dielectric character and its capacitance is added in series with the one of the gate oxide, thus reducing the overall capacitance.

■ **Inversion (LF and HF)**

Let's assume a quasi static condition (low frequency AC voltage source). By further increasing the positive voltage beyond a certain threshold, minority carriers (electrons, in our sample) are pushed towards the oxide by the applied electric field and a region populated of electrons is formed at the silicon/oxide interface: this region is called inversion layer, since an inversion of polarity occurred in the p-type semiconductor. If the positive voltage is raised even further, most of charge is now screened by the inversion layer since the electron density increases exponentially with the surface potential. The depletion region expansion is therefore no longer needed and its width saturates to a maximum value: the result is that Cox starts dominating over the depletion capacitance, thus making the overall capacitance raise again. When the electron population in the inversion layer becomes comparable with the p-type doping, the device enters the so-called strong inversion region and Ctot almost reaches Cox (the same value in accumulation). However, depending on the adopted frequency, the response of mobile carriers inside the silicon can change: if the frequency is low enough, net e-h pairs have time to thermally generate inside the silicon and the electrons can continue to populate the surface, as described before. If the frequency is too high, the generation of minority carriers may struggle to follow the AC voltage and the only way to screen the potential is a further increase of the depletion region, since the response time of majority carriers is much shorter compared to that of minority carriers [40][30]. This leads to a progressive reduction of the total capacitance, which saturates at its minimum when the depletion region reaches its maximum extension.

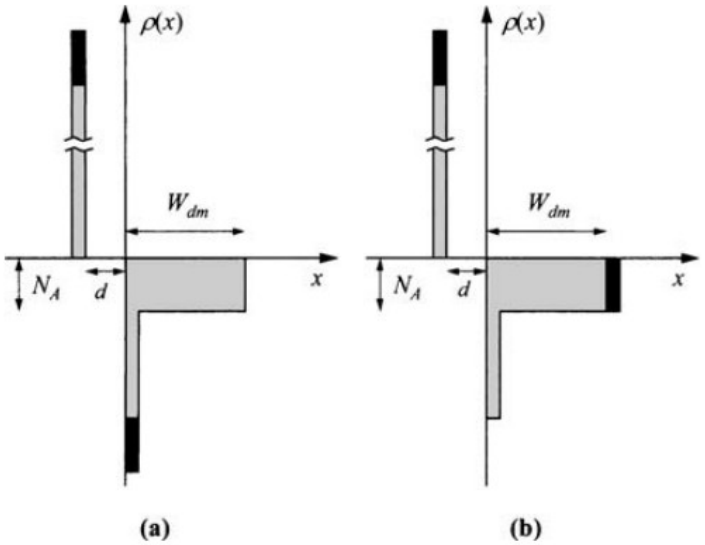

Figure 4.1: Inversion space charge distribution in a) low frequency b) high frequency [40].

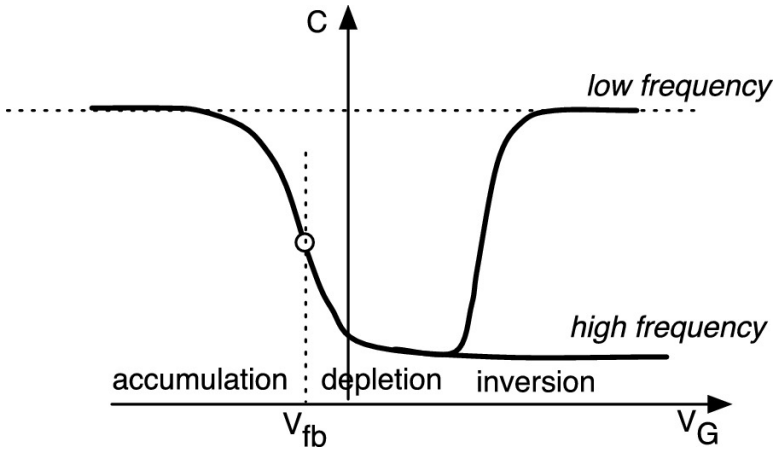

Figure 4.2: Ideal low and high frequency CV curves for a p-type substrate [41].

4.1.2 Connections and measurement setup

In order to switch from HF to LF configurations, a switch matrix was connected between the Keithley and the DUT. One probe was used to contact the gate while the chuck acted as second contact. A 2-wire (coaxial cables for HF measurements, triaxial cables for LF measurements) method was adopted: since the DUT had a resistance in the order of $\sim M\Omega$ that is much larger with respect to the ones of the cables ($\sim \Omega$), the 4 wires were not strictly necessary to compensate for the cable resistance and 2 wires were sufficient. Generally, an open/short circuit compensation is suggested at high frequency to compensate for parasitic

capacitance [42] and avoid an overestimation of the DUT capacitance; however, since the CV curves extracted at 100 kHz without compensation gave almost the same C_{ox} value in accumulation as the 1 Hz curves, the compensation was not considered impactful at that frequency and was therefore avoided.

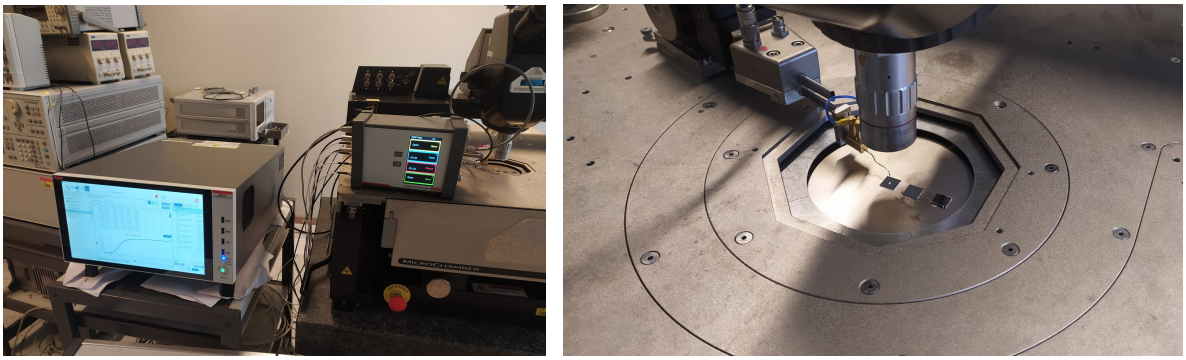

Figure 4.3: Keithley and switch matrix (*left*). MFIS samples being tested on the probe station (*right*).

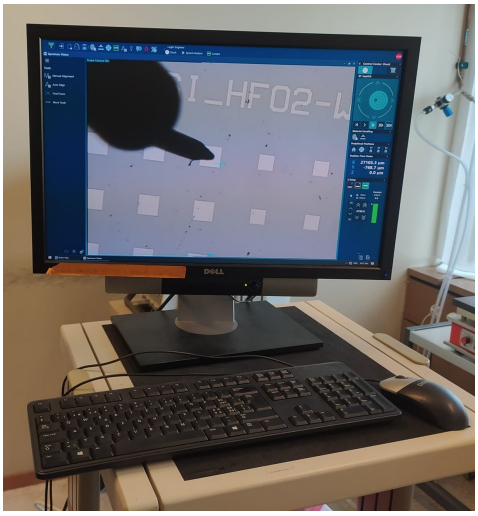

Figure 4.4: Contacting probe on MFIS capacitors.

To perform CV **HF measurements**, the CVU (Capacitance-Voltage Unit) was used: it is able to make impedance measurements by sourcing DC+AC voltages and measuring the output AC voltage and AC current [39]. In this configuration the allowed range of frequencies goes from 1 kHz up to 1 MHz. In our specific case, frequencies between 1 Khz and 10 kHz produced too noisy CV curves, so the 100 kHz was the best choice; an RMS of 30 mV was employed, which is within the range suggested for HF by the Keithley manual [39].

To perform **LF measurements**, the SMU (Source Measure Unit) was used, which allows measuring with great precision very high impedances at specific low frequencies. The use of the preamplifier here is fundamental since we are dealing with high impedance and therefore very small currents. The SMU1 is used to source the DC+AC voltage to the chuck and simultaneously measure the output AC voltage, while the SMU2 measures the AC current on top of the capacitor and sources 0 V. By computing the discrete Fourier Transform of the ratio between the measured AC voltage and AC current, the tool is able to evaluate the impedance in terms of magnitude and phase. From the impedance, the capacitance is easily extracted. For this configuration, the allowed range of frequencies is from 1 mHz up to 10 Hz. In our case, 1 Hz was the selected frequency and an RMS of 300 mV was employed, that is within the acceptable range for LF according to the Keithley manual [39].

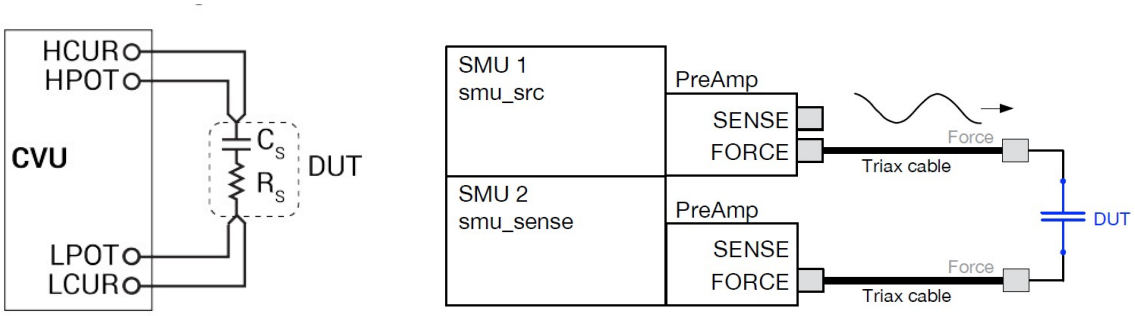

Figure 4.5: a) CVU connections model b) SMU connections model [39]

After applying a certain bias, the MOS capacitor needs time to be completely charged and to reach its quasi-equilibrium condition; this is why the choice of the sweep delay time is important for a proper measurement. A double sweep from accumulation to inversion and then from inversion to accumulation was performed and this was useful to make sure that a right delay time was chosen. In particular, when sweeping from accumulation to inversion, if the delay time is too short we expect the HF capacitance to never reach its equilibrium minimum value and to start dropping below it. The reason behind this phenomenon is that minority carriers do not have enough time to populate the inversion layer and the only way to compensate for the charge is by enlarging the depleted region, thus reducing the overall capacitance. On the other hand, when performing the opposite sweep (from inversion to accumulation) the effect of a short delay time is typically less evident but still present: in general the recombination of minority carriers is pretty fast, but if the delay time is still too short, then they may not recombine in time, producing a larger inversion capacitance than we expect [43]. If the two HF C-V curves for the two reverse sweeps coincide, then a correct sweep delay has been chosen, in our case 0.5 s.

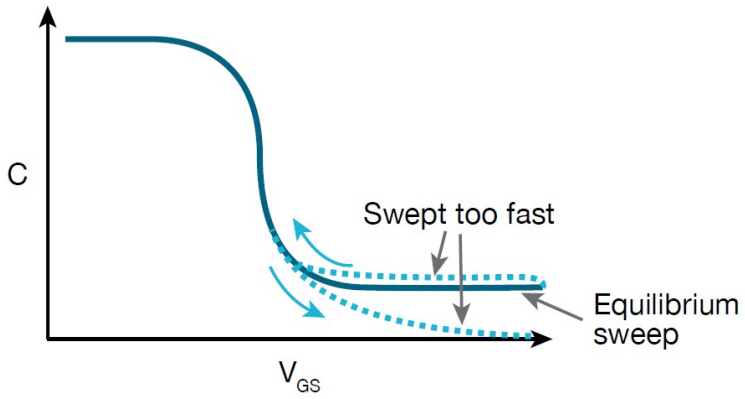

Figure 4.6: Effect of too fast sweep for *accumulation* ⇒ *inversion* and *inversion* ⇒ *accumulation* [39].

Moreover, on the backside of the Si substrate of our sample (used as electrical contact in our case) some process induced thermal SiO_2 may introduce a series resistance R_s that is detrimental especially for the G-V measurement(it may hide the conductance peak) but also for the C-V measurement (we risk to measure a lower and distorted capacitance with respect to the actual one); also the Si substrate itself introduces a resistance (although much lower than the former). We need therefore to adjust the capacitance and the conductance with a series compensation [39] [30] as in the following:

$$C_{\mathrm{ADJ}} = \frac{\left(G^2 + (2\pi f C)^2\right) C}{a_r^2 + (2\pi f C)^2}$$

$$G_{\mathrm{ADJ}} = \frac{\left(G^2 + (2\pi f C)^2\right) a_{\mathrm{r}}}{a_r^2 + (2\pi f C)^2}$$

where:

$$a_r = G - \left(G^2 + (2\pi f C)^2\right) R_s \qquad \text{and} \qquad R_s = \frac{\left(\frac{G_{\mathrm{a}}}{2\pi C_{\mathrm{a}}}\right)^2}{\left[1 + \left(\frac{G_{\mathrm{a}}}{2\pi C_{\mathrm{a}}}\right)^2\right] G_{\mathrm{a}}}$$

being f the test frequency and Rs the series resistance calculated in accumulation. The series resistance is more critical for high frequencies [30]. At low frequency, in fact, R_s is negligible with respect to the impedance $\frac{1}{\omega C}$, while at high frequency R_s and the capacitive impedance risk to become comparable. In our case the effect of the adjustment was equally important for both 1 Hz and 100 kHz CV curves.

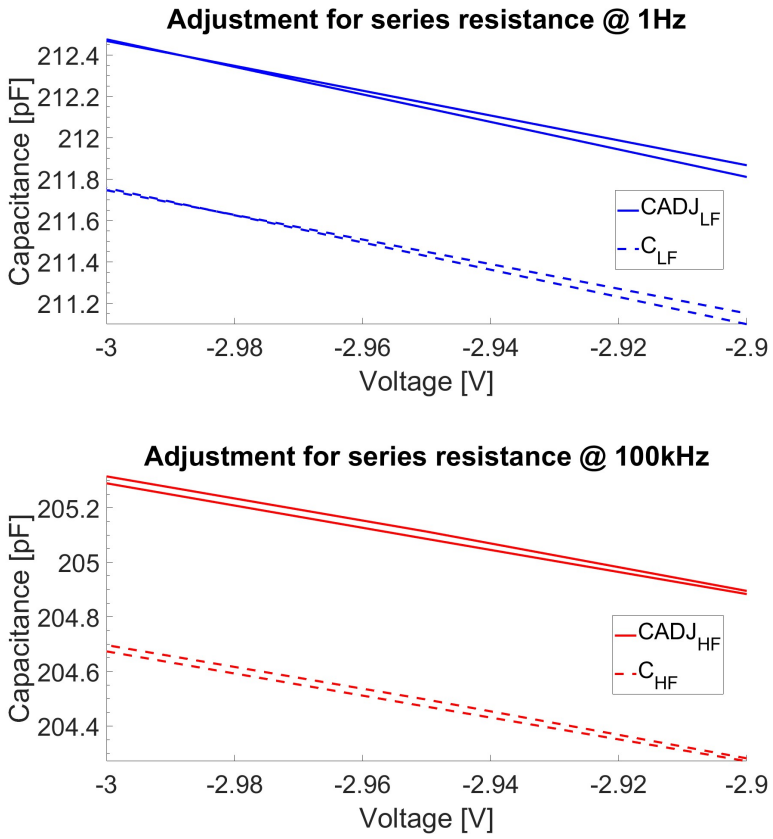

Figure 4.7: Effect of series resistance adjustment on C_{ox} (accumulation value) measured during this project on the MFIS stack with Ti+Pt gate metal at 1 Hz (*top*) and 100 kHz (*bottom*).

4.1.3 Main oxide defects

4.1.4 Circuit model of the gate stack

Starting from the general definition of the capacitance $C = \frac{dQ_G}{dV_G}$ we can derive a circuit model for the MOS system depending on the operation condition. Being the total charge null in the system, we know that Q_G=-(Q_S+Q_{it}). Q_S is the charge found in Silicon, that in the most general case is $Q_S = Q_{p/n} + Q_d$, so the sum of accumulation/inversion and depletion charge respectively. Also, the system behaves as a voltage divider, splitting V_G over the Hafnia, the SiO_2 and the Silicon: $V_G = V_{FB} + V_{hk} + V_{ox} + \psi_s$. We can therefore expand the definition of the total capacitance:

$$C = -\frac{dQ_S + dQ_{it}}{dV_{hk} + dV_{ox} + d\psi_s} = -\frac{1}{\frac{dV_{hk}}{dQ_S+dQ_{it}} + \frac{dV_{ox}}{dQ_S+dQ_{it}} + \frac{d\psi_s}{dQ_S+dQ_{it}}} = \frac{1}{\frac{1}{C_{hk}} + \frac{1}{C_{ox}} + \frac{1}{C_S}} \quad [43]$$

In accumulation, the total capacitance is basically dominated by the series of C_{hk} and C_{ox}, since the holes in Si are so many that C_S is much higher than the oxide capacitance; therefore there's no contribution coming from C_S. In depletion, the behavior depends on the frequency we are using to stimulate our DUT, since C_{it}=$C_{it}(\omega)$: interface traps typically respond to slow AC signals because the inverse of their trapping time constant is matched with low frequencies. Thus at low frequencies C_S is C_d+C_{it}. At high frequencies, the traps are transparent and C_S is dominated by C_d. Finally, in inversion at low frequencies the total capacitance comes back to the series of C_{hk} and C_{ox} while at high frequencies it is a series of C_{hk}, C_{ox} and C_d, for the reasons explained in 4.1.1.

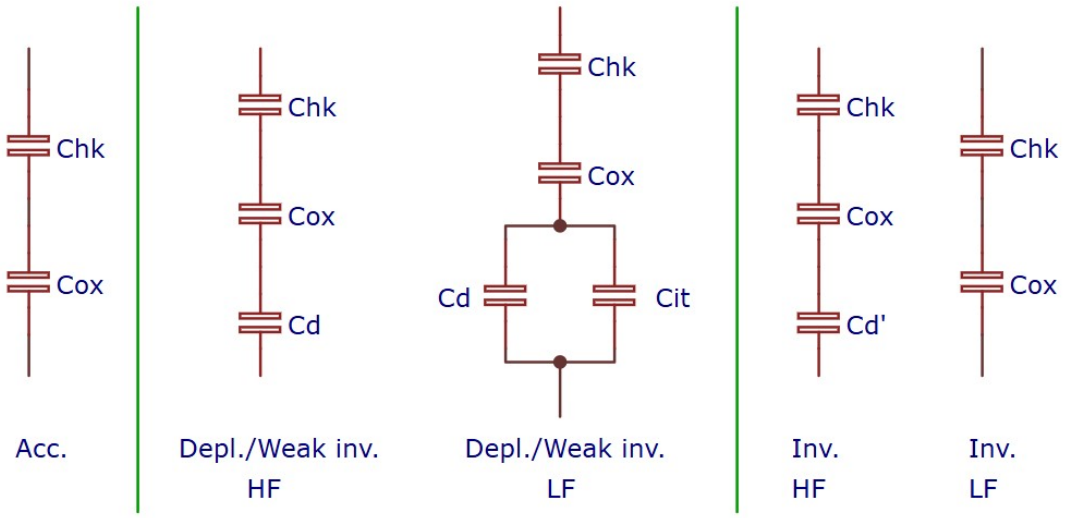

Figure 4.8: Capacitance model throughout the operation modes at HF and LF.
N.B. C_d' is smaller than C_d since the depletion region slighlty enlarges in inversion at HF. Inspired by [44].

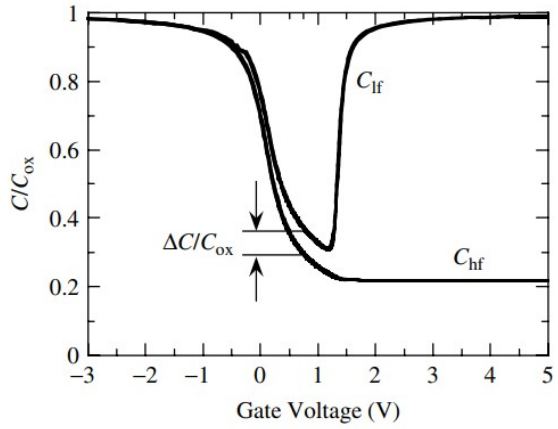

Figure 4.9: Ideal normalized low and high frequency curves in presence of interface traps (p-type substrate) [43] N.B. in this picture C_{ox} is already the series of C_{SiO_2} and C_{hk}.

It is important to highlight that, due to the voltage divider, we are not going to observe a ferroelectric shift in the CV curve for those MFIS having t_{SiO_2}=5 nm and t_{hk}={12,16,20} nm, since the portion of V_G that drops across C_{hk} is smaller than the coercive voltage during our electrical tests. Still, the absence of the ferroelectric shift did not prevent the analysis from obtaining useful information on the stacks. After that, to push for a ferroelectric character of the stack, new recipes were tested and new results were discussed.

4.1.5 How to define and extract the Flatband Voltage V_{FB} and the Effective Metal Work Function $\Phi_{m,eff}$

The flatband voltage is the voltage at which the MOS system shows flat energy bands since Si is neutral in every point (the net space charge ρ is zero, so there's no band bending) [30]. From the surface potential equation we know that:

$$V_G - V_{FB} = -\frac{Q_s}{C_{ox}} + \psi s \quad [45]$$

being Q_s the total charge per unit area in the silicon (depletion charge + accumulation/inversion charge) and ψs the surface potential. Let's set the band bending to zero ($\psi s = 0$): if we assume a uniformly doped silicon, then $Q_s(\psi s = 0) = 0$ [30]. Thus V_G=V_{FB}. V_{FB} is ideally equal to the work function difference between the metal and the semiconductor ($V_{FB} = \Phi_m - \Phi_s$). However, the presence of non-ideal charges inside the MOS stack (bulk charges $\rho_{ox/hk}(x)$, interface charges Q_{it} and fixed charges $Q_{f,ox/hk}$) strongly influences the voltage needed to flatten the energy bands. Therefore, a more correct definition of the flatband voltage is the following:

$$V_{FB} = \phi_{m,eff} - \phi_s - \frac{1}{\varepsilon_{ox}\varepsilon_0}\int_0^{EOT} x\rho(x)\,dx \quad [29]$$

being $\rho(x)$ the charge per unit volume inside the gate oxide and being EOT the equivalent oxide thickness ($EOT = t_{\mathrm{ox}} + EOT_{\mathrm{hk}} = t_{\mathrm{ox}} + \frac{\epsilon_{\mathrm{ox}}}{\epsilon_{\mathrm{hk}}} t_{\mathrm{hk}}$).
$\mathrm{Q_{it}}$ are the interface charges, $\mathrm{Q_{f,ox}}$ and $\mathrm{Q_{f,hk}}$ are the fixed charges we can find respectively near the SiO_2/Si and the Si:HfO_2/SiO_2 interfaces, whereas $\rho_{\mathrm{ox}}(x)$ and $\rho_{\mathrm{hk}}(x)$ are distributed along the bulk of SiO_2 and Si:HfO_2. We are going to treat $\mathrm{Q_{it}}$ + $\mathrm{Q_f}$ together simply as "$\mathrm{Q_{it}}$" interface charges for this calculation, since they are typically indistinguishable unless using more than one technique [29] [31] [46] (for example, a post-metalization annealing in forming gas may help to reduce $\mathrm{Q_{it}}$ and keep $\mathrm{Q_f}$ unperturbed [34]). Finally, $\phi_{m,eff}$ takes into account the influence of the metal-Si:HfO_2 interface on the real value of the metal work function. We can therefore expand $\mathrm{V_{FB}}$ as follows:

$$
\begin{aligned}
V_{FB} &= \phi_{m,\mathrm{eff}} - \phi_s + V_{FB}(\mathrm{SiO_2}) + V_{FB}(\mathrm{hk}) = \\
&= \phi_{m,\mathrm{eff}} - \phi_s - \frac{1}{\epsilon_0 \epsilon_{ox}} \int_0^{EOT} x Q_{it,ox}(x) \delta(EOT)\, dx \\
&\quad - \frac{1}{\epsilon_0 \epsilon_{ox}} \int_{EOT_{hk}}^{EOT} x \rho_{ox}(x)\, dx - \frac{1}{\epsilon_0 \epsilon_{ox}} \int_0^{EOT_{hk}} x Q_{it,hk}(x) \delta(EOT_{hk})\, dx \\
&\quad - \frac{1}{\epsilon_0 \epsilon_{ox}} \int_0^{EOT_{hk}} x \rho_{hk}(x)\, dx \\
&= \phi_{m,\mathrm{eff}} - \phi_s - \frac{Q_{it,\mathrm{ox}}}{\epsilon_0 \epsilon_{ox}} EOT - \frac{\rho_{ox}}{2\epsilon_0 \epsilon_{ox}} EOT^2 \\
&\quad + \frac{\rho_{ox}}{2\epsilon_0 \epsilon_{ox}} EOT_{hk}^2 - \frac{Q_{it,\mathrm{hk}}}{\epsilon_0 \epsilon_{ox}} EOT_{hk} - \frac{\rho_{hk}}{2\epsilon_0 \epsilon_{ox}} EOT_{hk}^2 \quad [29]
\end{aligned}
$$

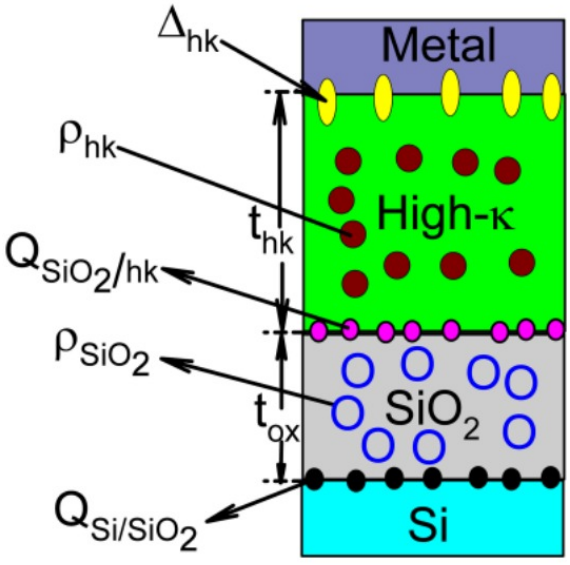

Figure 4.10: Different types of charges along the gate stack affecting $\mathrm{V_{FB}}$ [31].

We can approximate even further by making an a posteriori assumption: based on the experimental results that will be presented later, a linear interpolation provides a better fit for the collected data. We will therefore neglect the bulk charge density contribution to V_{FB} with respect to interface traps. This is a frequently used approximation when a quadratic fit is not possible [47] [48] [49] [50] [51]. This hypothesis is partially supported by the measured peaked parallel conductance curves in HF: when bulk trap losses dominate, the conductance is typically flat since those losses don't depend on V_G; in our G_p-V_G curves, instead, the conductance clearly shows a peak around V_{FB}, which confirms the prevalence of interface trap interacting with the Silicon via generation and recombination mechanisms [30]. However, this represents only a partial proof, since there may be deeper bulk traps that are invisible to the conductance method (no contribution to the losses) but still cause the shift of V_{FB}.
Hence, we end up with a simplified expression of V_{FB}:

$$V_{FB} = \phi_{m,\text{eff}} - \phi_s - \frac{Q_{it,\text{ox}}}{\epsilon_0 \epsilon_{ox}} EOT - \frac{Q_{it,\text{hk}}}{\epsilon_0 \epsilon_{ox}} EOT_{hk}$$

At this point, we may decide to express V_{FB} either as a function of EOT, assuming $Q_{it,\text{hk}} << Q_{it,\text{ox}}$, or as a function of EOT_{hk}, assuming $Q_{it,\text{ox}} << Q_{it,\text{hk}}$. Also in this case, we will base our decision on the collected experimental data: the choice of EOT as variable for V_{FB} did not give realistic values of work function for the different gate metals; whereas, by plotting V_{FB} vs EOT_{hk}, much more reliable values for $\Phi_{\text{m,eff}}$ were obtained. We can therefore give a final expression for V_{FB} assuming $Q_{it,\text{ox}} << Q_{it,\text{hk}}$:

$$\begin{aligned}
V_{FB} &= \phi_{m,\text{eff}} - \phi_s - \frac{Q_{it,\text{ox}}}{\epsilon_0 \epsilon_{ox}} EOT - \frac{Q_{it,\text{hk}}}{\epsilon_0 \epsilon_{ox}} EOT_{hk} = \\
&= \phi_{m,\text{eff}} - \phi_s - \frac{Q_{it,\text{ox}}}{\epsilon_0 \epsilon_{ox}} tox - \frac{Q_{it,\text{ox}}}{\epsilon_0 \epsilon_{ox}} EOT_{hk} - \frac{Q_{it,\text{hk}}}{\epsilon_0 \epsilon_{ox}} EOT_{hk} = \\
&= \phi_{m,\text{eff}} - \phi_s - \cancel{\frac{Q_{it,\text{ox}}}{\epsilon_0 \epsilon_{ox}} tox} - \frac{Q_{it,\text{ox}} + Q_{it,\text{hk}}}{\epsilon_0 \epsilon_{ox}} EOT_{hk} \simeq \\
&\simeq \phi_{m,\text{eff}} - \phi_s - \frac{Q_{eff}}{\epsilon_0 \epsilon_{ox}} EOT_{hk}
\end{aligned}$$

where Q_{eff} represents a mixed contribution of interface and fixed traps found at both the Si-SiO_2 and the Si:HfO_2-SiO_2 interface [31].

Let's bring ϕ_s to the first term of the equation to take into account the variation of the Silicon work function between different wafers:

$$V_{FB} + \phi_s = \phi_{m,eff} - \frac{Q_{eff}}{\epsilon_0 \epsilon_{ox}} EOT_{hk}$$

By knowing V_{FB} for different equivalent thicknesses, we will therefore extract information on the effective metal work function as well as on the amount of effective interface charges, by extracting respectively the y-axis intercept and the slope.

The transition between accumulation and depletion condition occurs exactly at V_{FB}. Thus, we can extract V_{FB} exploiting the linearity of the $\frac{1}{C^2}$ curve around depletion ("$\frac{1}{C^2}$ method" [30] [52] [53]):

$$\frac{1}{\left(\frac{C_{tot}(V_G)}{A}\right)^2} - \frac{1}{\left(\frac{C_{ox}}{A}\right)^2} = m(V_G - V_{FB}) \quad @\ V_G \text{ in depletion}$$

where C_{ox} is the value of the total capacitance in accumulation (series of C_{SiO_2} and C_{hk}), A is the area of the capacitor and $m = \frac{2}{q\, N_a\, \epsilon_0 \epsilon_{ox}}$

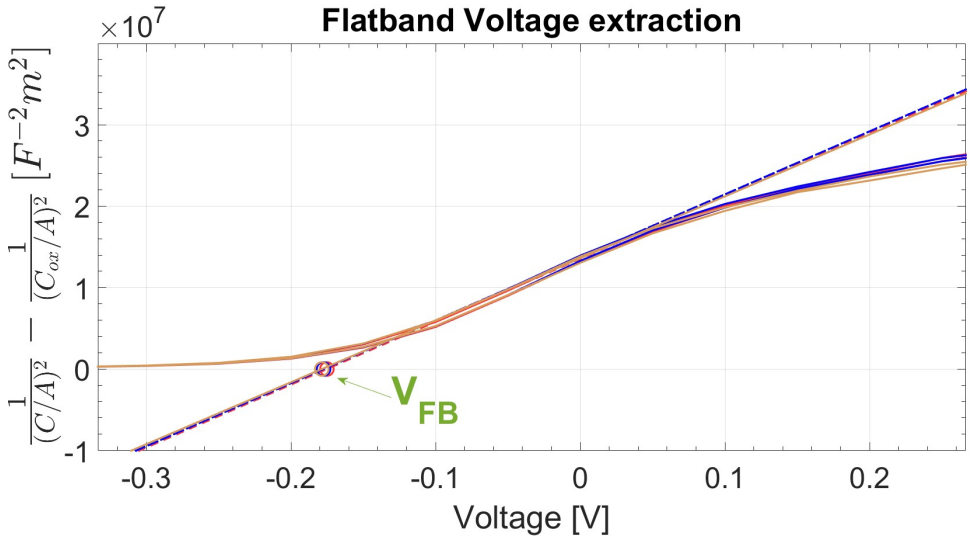

Figure 4.11: Flatband Voltage extraction from an MFIS provided with W gate metal, fabricated during this project. The linear interpolation of $\frac{1}{C^2}$ was done on the CV curve measured for the accumulation ⇒ inversion voltage sweep.

We can also infer the exact doping N_a from the linear coefficient m, assuming Silicon uniformly doped, such that we have a more precise measure of $\phi_s = \chi_s + \frac{E_{g,s}}{2} - \phi_p = \chi_s + \frac{E_{g,s}}{2} - k_b T ln(\frac{N_a}{n_i})$ (around 4.6 eV).
The equivalent oxide thickness is obtained from the total capacitance in accumulation C_{ox}:

$$EOT = \frac{\epsilon_{ox}\epsilon_0 A}{C_{ox}}$$

where $\epsilon_{ox} \equiv \epsilon_{SiO_2} = 3.9$ and A is the area of the capacitor. The accuracy of the thickness of the thermally grown SiO_2 was verified on the ellipsometer, hence the equivalent oxide

thickness of the Hafnia can be calculated:

$$EOT_{hk} = EOT - t_{ox}$$

The thickness of the Hafnia was measured on the ellipsometer as well, soon after the ALD. Therefore, an experimental value of its dielectric constant can also be extracted:

$$\epsilon_{hk} = \frac{\epsilon_{ox} t_{hk}}{EOT_{hk}}$$

At this point, we have all the required data for a linear interpolation of V_{FB} vs EOT_{hk}:

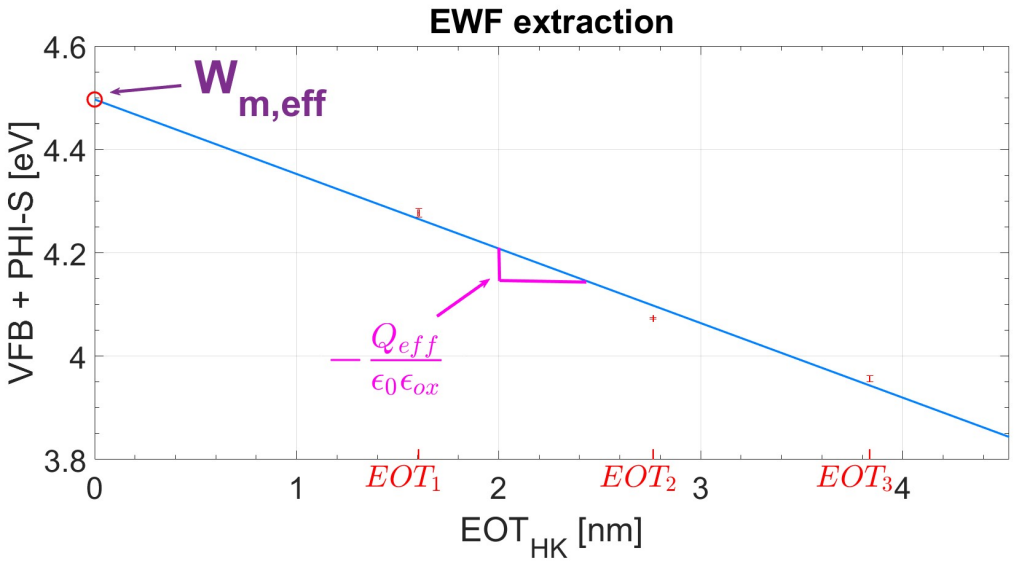

Figure 4.12: Effective metal work function extraction from an MFIS provided with Ti+Pt gate metal, fabricated during this project. Q_{eff} can also be calculated from the slope.

The knowledge of the real metal work function (i.e. the distance between metal Fermi level and the vacuum level) is fundamental for a precise tuning of the threshold voltage; the main causes behind the work function deviation from its value in vacuum are the presence of process-induced stoichiometry variations at the metal-HfO_2 interface (e.g. reduction of the metal with consequent generation of oxygen vacancies inside the Hafnia) and the interplay of HfO_2 interface traps with the metal surface (by trapping charges, these states generate dipoles affecting the potential barrier seen by the carriers) [54]

Concerning the Q_{eff}, a part from its calculated value (which will be discussed later), we can anticipate that all the V_{FB} interpolation lines exhibited a negative slope, that is a

positive Q_{eff}. This may suggest that the majority of interface traps and near-interface fixed traps are donor-like (i.e. neutral when filled and positive when empty) and that they are mostly located in the lower half of the Si bandgap [29] [31] .

4.1.6 How to define and extract the interface trap density Dit

We know that interface traps typically react to AC V_G changes at low frequency. This has an impact on the LF capacitance, which will result as the series of C_{ox} and C_d+C_{it} in depletion. On the other hand, at high frequency the interface charges are not fast enough to follow V_G and the HF capacitance is not affected by them [30]. The only effect of interface traps that is visible in both HF and LF CV curves is the so-called *stretch-out* , that is an horizontal broadening of the curve with respect to its ideal shape. The reason behind this is that part of V_G is consumed by traps to capture electrons, thus inducing a slower band bending. Basically, ψ_s starts changing less with V_G, a wider range of V_G needs to be used and therefore the curve experiences a distortion along the x axis [30] [29] .
In the end we can basically exploit the difference between LF and HF to extract the Dit, i.e. the density of interface charges per unit area and per energy level, by comparing the HF and LF capacitances:

$$\mathrm{Dit} = \frac{1}{q \cdot A}\left[\left(\frac{1}{\frac{1}{\mathrm{CLF}} - \frac{1}{\mathrm{Cox}}}\right) - \left(\frac{1}{\frac{1}{CHF} - \frac{1}{\mathrm{Cox}}}\right)\right] \quad [30][29][55][56]$$

where q is the elementary charge and A is the area of the capacitor. Originally, this theory formulated by Berglund was based on the comparison of C_{LF} with an ideal trap-free CV curve. However, if the frequency is high enough, the effect of traps is negligible and the HF CV curve can be used instead of the ideal one. This method is of course valid only in depletion, where those interface trap levels at few k_BTs from E_F start being active once they cross E_F [30] [56] (see also 4.1.7). The response of interface traps follows the SRH (Shockley-Read-Hall) mechanism [56] [57] and is dictated by the trap time constant of majority carriers τ_e and τ_h defined as follows:

$$\tau_e = \frac{1}{\sigma_n v_{th_n}(n_s + p_1)} \quad \text{and} \quad \tau_h = \frac{1}{\sigma_p v_{th_p}(p_s + n_1)} \quad [56][57]$$

where $\sigma_{n/p}$ is the capture cross section, $v_{th_{n/p}}$ is the average thermal velocity, n_s and p_s are the electrons and holes surface densities, n_1 and p_1 are respectively the electrons and holes concentrations that would exist in case $E_F = E_T$ (i.e. if the Fermi level equals the trap energy level). In particular:

$$n_1 = N_c\, e^{\left(-\frac{E_c - E_T}{k_B T}\right)}$$

$$p_1 = N_v\, e^{\left(-\frac{E_T - E_v}{k_B T}\right)}$$

where N_c and N_v are respectively the effective density of states of electrons and holes, E_c and E_v are the band edges of the conduction and valence bands, k_B is the Boltzmann constant and T is the temperature. It must be clarified that $\tau_{e/h}$ does not refer to a carrier lifetime, that is inversely proportional to the number of traps N_t, but to a trapping time constant of the dominant carriers at the surface (holes in accumulation and electrons in inversion), that is instead decreasing with the carrier density [57]. While n_s and p_1 affect respectively the electron capture probability to the trap and hole emission probability from the trap (when electrons are the majority carriers), vice versa, p_s and n_1 influence the hole capture probability to the trap and electron emission probability from the trap (when holes are majority carriers).

From the definition of $\tau_{e/h}$ we can infer its different behavior depending on the operation condition: in accumulation, p_s prevails at the denominator and makes τ_h very small and almost constant ($\tau_h \simeq \tau_{h_0}$). In strong inversion, n_s prevails and $\tau_e \simeq \tau_{e_0}$. In depletion/weak inversion, n_1 and p_1 start dominating, thus making the trapping rate dependent on the position of the trap with respect to the band edges as well as on the temperature. Assuming σ temperature-independent (acceptable at the cost of some uncertainty [58] [59]), in depletion the time constant depends on T especially because of the Arrhenius behavior of n_1 and p_1 $\propto e^{-\frac{E_a}{k_B T}}$ [60] (prevailing over $v_{th} \propto \sqrt{T}$ [40]), where the activation energy E_a is the distance between E_T and the conduction/valence band edge.

In this project a p-type substrate was used, hence the position of the traps was defined using as reference the valence band edge E_v. The D_{it} was calculated choosing 100 kHz as high frequency and 1 Hz as low frequency. The frequency value of 100 kHz was high enough to neglect the contribution from the traps to the HF CV curve (no rising curve in inversion) and low enough to reduce the range of analyzed traps. In fact, the calculated value of D_{it} is the density of traps responding to a stimulating frequency in the range [1 Hz, 100 kHz], that is with a time constant whose order of magnitude is in the range [10^{-5} s, 1 s].

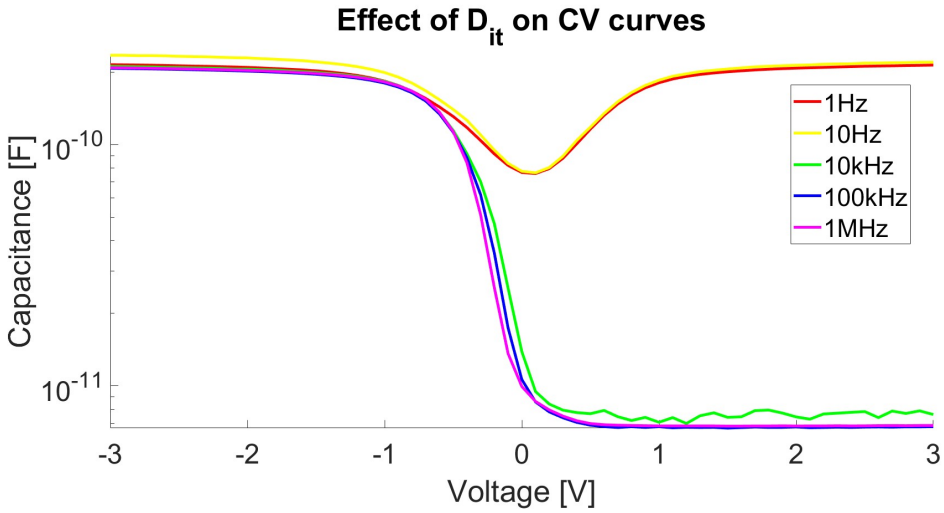

Figure 4.13: Effect of D_{it} on the experimental CV curves measured during this project on an MFIS stack with a W gate metal and 12 nm of Si:HfO_2. The difference between LF and HF CV curves in depletion contains information on D_{it}. Note: the measured 10 kHz curves were too noisy, especially in inversion, and they did not exhibit the same drop observed for higher frequencies. Hence 100 kHz turned out to be the best compromise for the high frequency.

Moreover, it is very important to highlight the difference between $N_{eff} = \frac{Q_{eff}}{q}$ and D_{it}: the former is a mixed contribution of interface traps throughout the whole stack affecting the shift of V_{FB}, the latter is the density of interface traps which are in the immediate vicinity of the Si channel, so that C_{it} can be added in parallel to C_d. Another difference is that the N_{eff} is an average over different gate oxide thicknesses (EOTs) whereas the D_{it} is calculated for a specific stack.
An example of Dit profile obtained during this project is shown in Fig. 4.14. The shape is the typical one also found in literature as well as in different papers [40] [39] [55] [56] [61] [62] [63] [64] [44].

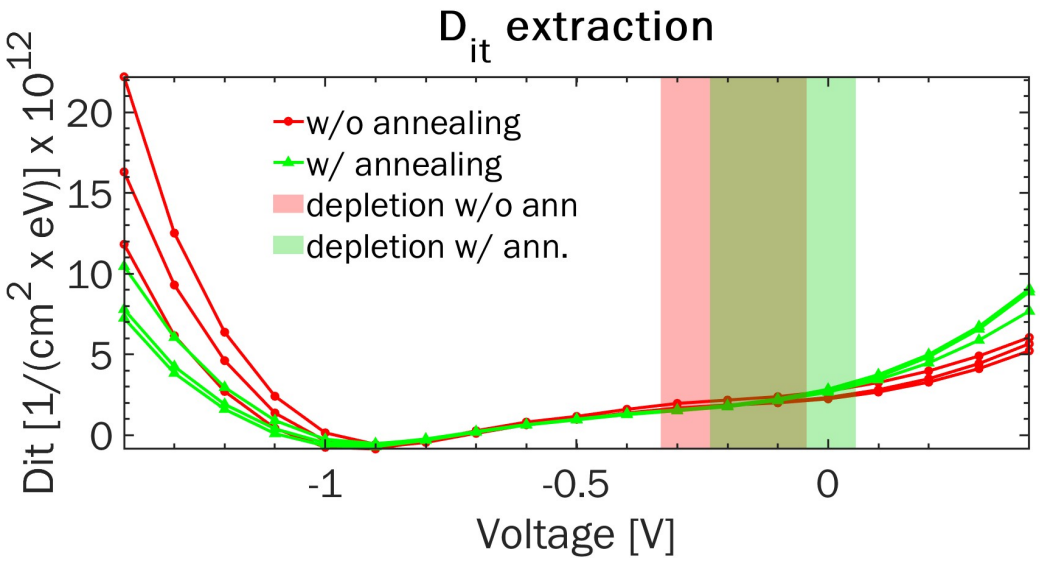

Figure 4.14: D_{it} curve obtained during this project from the MFIS stack provided with a Ti+Pt gate metal and 12 nm of Si:HfO_2 with and without post-metalization annealing. The depletion is highlighted by shaded areas, whose left edge is V_{FB} while the right edge is $V_{FB}+\psi_s(inv)$.

We can notice that part of the curve gets negative for a small range of V_G and this has no physical meaning for a trap density. This occurred very frequently for many D_{it} curves. However, as previously stated, the High-Low frequency method, used to extract D_{it}, gives reliable results only in depletion. For this reason we need to take into account only those trap density values in the range of V_G between V_{FB} (onset of depletion) and $V_{FB}+\psi_s(inv)$ (where $\psi_s(inv)$ is the band bending required for the intrinsic energy level E_i to cross the Fermi level, which approximately represents the onset of weak inversion [30]). In order to find $\psi_s(inv)$, the Fermi level was calculated knowing that

$$E_F - E_i = -k_B T \ln\left(\frac{n_i}{N_A}\right) \quad [40]$$

where n_i is the intrinsic carrier concentration ($\simeq 10^{10}\, cm^{-3}$ in Silicon) and N_A is the acceptor doping density ($\simeq 10^{15}\, cm^{-3}$ in our case). The obtained E_F-E_i distance was $\simeq 0.29$ eV, i.e. $\psi_s(inv) \simeq 0.29$ V. As shown in chapter 5, in depletion the D_{it} curves were not only positive (so physically acceptable) but most of them were also almost constant, similarly to Fig. 4.14.

4.1.7 The parallel conductance G_p and the Conductance method

Along with the capacitance, the Keithley multimeter is able to measure other important data, such as the parallel conductance G_p. Even this quantity is strictly connected to the interface trap density. In fact, the interface traps change their occupancy when sweeping over V_G [30]. In particular, by applying $V_G > V_{FB}$ on a MOS stack with a p-type substrate, the downward band bending at the Si surface causes trap energy levels E_T to progressively cross the Fermi level E_F. The trap energy levels above E_F are initially empty because of the Fermi-Dirac statistics. As soon as a certain E_T bends below E_F, it releases its hole (majority carrier) to the valence band V.B., i.e. it gets filled by an electron (for an n-type substrate, the behavior is symmetrical). This mechanism (extensively described by Nicollian and Brews in their book "MOS (Metal Oxide Semiconductor) Physics and Technology" [30]) is exploited by the so-called Conductance method, which is another technique used to extract D_{it}. The method consists in stimulating the MOS with a small AC signal at a specific frequency. This makes the energy band oscillate upward and downward with respect to the Fermi level at the Si surface, inducing an alternate emission and capture of carriers respectively from and towards those trap states at few k_BTs from E_F. If the stimulation frequency is too high, the traps are not fast enough to respond to the signal; if the frequency is too low, the traps immediately react to the stimulation. Only if the frequency is matched with the inverse of the trapping time constant $\frac{1}{\tau}$, then an energy loss occurs and a resonance in the parallel conductance shows up at that specific frequency. More precisely, in order to provoke an energy loss, the traps need to lag behind the signal, hence their trapping frequency must be slightly smaller than the external stimulus: in a p-type Si, when an empty trap initially above E_F is bent below E_F by the positive half cycle of a matched AC small-signal, that trap will still remain empty because of its slightly smaller trapping speed. This induces a thermal relaxation of electrons (thus a phonon emission) coming from higher energy levels in order to fill the trap. On the other hand, a filled trap originally below E_F will still be filled when brought above E_F by a negative half-cycle of the external AC voltage. Even in this case, the relaxation of the electron from that trap to lower energy levels requires the generation of a phonon. This phenomenon is therefore dissipative and can be modeled by a parallel conductance [30].

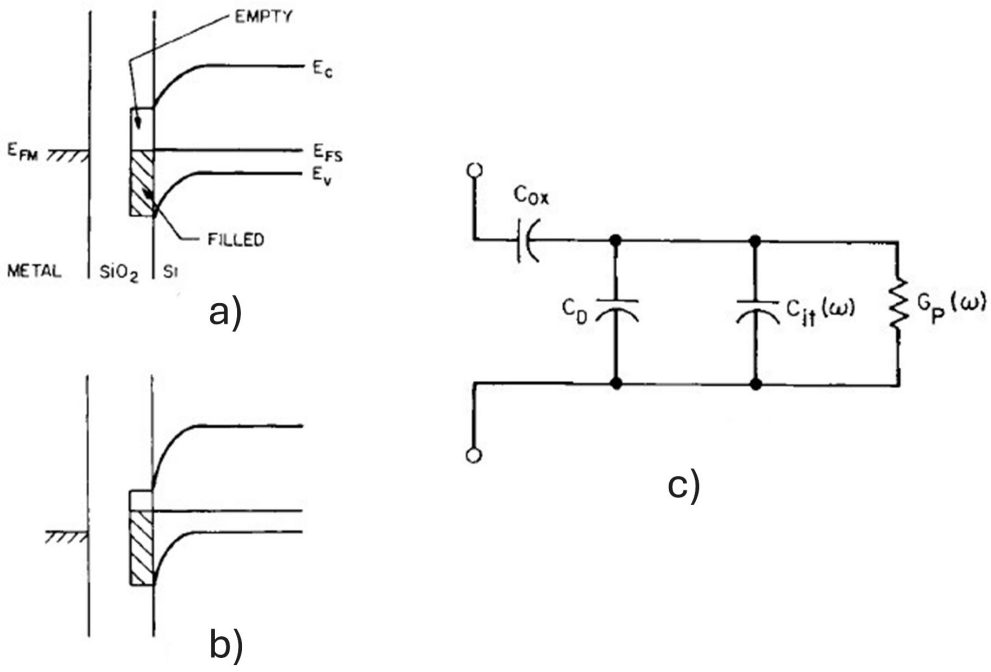

Figure 4.15: Interface traps occupancy in case of a p-type silicon for a) $V_G = 0$ V and b) $V_G > 0$ V [30]. c) Circuit model of a single trap level, including energy losses [30].

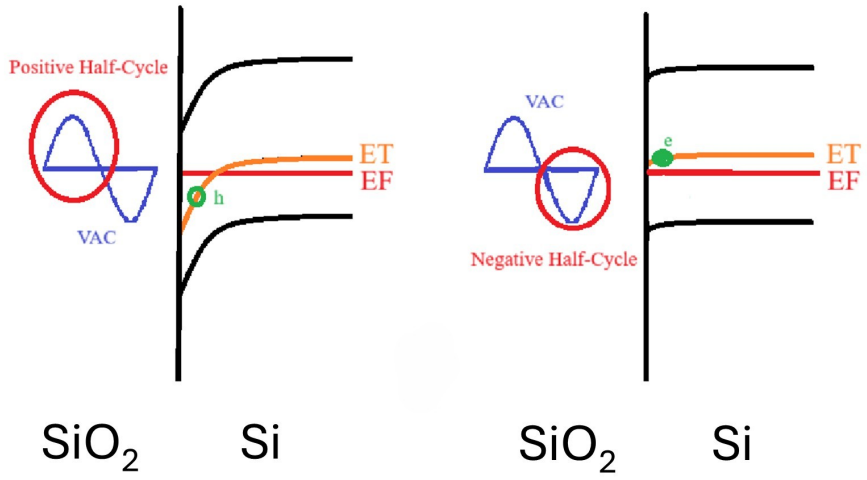

Figure 4.16: Effect of AC small-signal on the traps energy levels at the surface. Traps lagging behind the signal. Left: positive half-cycle, traps still empty below E_F. The thermal relaxation of a more energetic electron will occur to fill the trap. Right: negative half-cycle, traps still filled above E_F. The thermal relaxation of the electron occupying the trap will occur to free the trap. This phenomenon is described in [30]

The value of D_{it} can be extracted from the resonance peak of $\frac{G_p(\omega)}{\omega}$ vs $log(\omega)$. A simplified expression that is frequently used in literature is the following:

$$D_{it} = \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{max} @V_{G_0} \quad [40]\,[30]\,[44]\,[65]\,[66]$$

where V_{G_0} is a fixed gate voltage. The reason why the conductance method is generally considered more accurate is thanks to its direct extraction of D_{it}, differently from the High-Low frequency method, where further calculation steps are needed (thus higher error propagation) [30]. The main drawback, however, is that the resonant frequency is typically low (as suggested by results in chap. 5), which makes the method more difficult to implement.

The parallel conductance not only depends on the frequency but also on the V_G bias. In fact, V_G dictates the position of the traps with respect to E_F, which in turns changes their trapping time constant τ, that is exponentially dependent on ΔE = E_T - E_v. When V_G=V_{FB}, the traps placed just above E_F are activated by the stimulus and are responsible of the resonance peak. If V_G increases and enters weak inversion, the traps close to midgap are bent up to few k_BTs from E_F, thus they contribute to the energy loss this time. In this way we are able to scan over the energy levels between E_i and E_F. When V_G is such that $\frac{1}{\tau}$ matches the small-signal frequency, $G_p(V_G)$ exhibits a resonance peak. This maximum typically occurs in depletion. In accumulation, the capture rate is too high because of the high majority carrier density at the surface (τ is small and approximately constant [30] [67]), resulting in small energy losses. In depletion, instead, the reduction of majority carrier density causes τ to increase, thus making its inverse comparable with the stimulation frequency. Here the energy loss reaches its maximum. Moving deeper in depletion (towards weak inversion) the majority carrier density becomes too small, making the traps too slow to respond, thus reducing the losses. In weak inversion, the SRH model for the calculation of the capture rate $\frac{1}{\tau}$ changes and gets more complex because of the additional interaction of minority carriers. For this reason, sometimes the conductance may exhibit a second resonant peak in this operation condition [68]. Overall, the analysis of G_p in weak inversion is generally not recommended [30] [56]. Furthermore, the G_p vs V_G curve is useful to demonstrate which type of traps dominates between interface and bulk traps at specific frequencies. In fact, while the former are responsible of a resonance peak, the latter do not exhibit any peak because of their bias-independent losses [30].

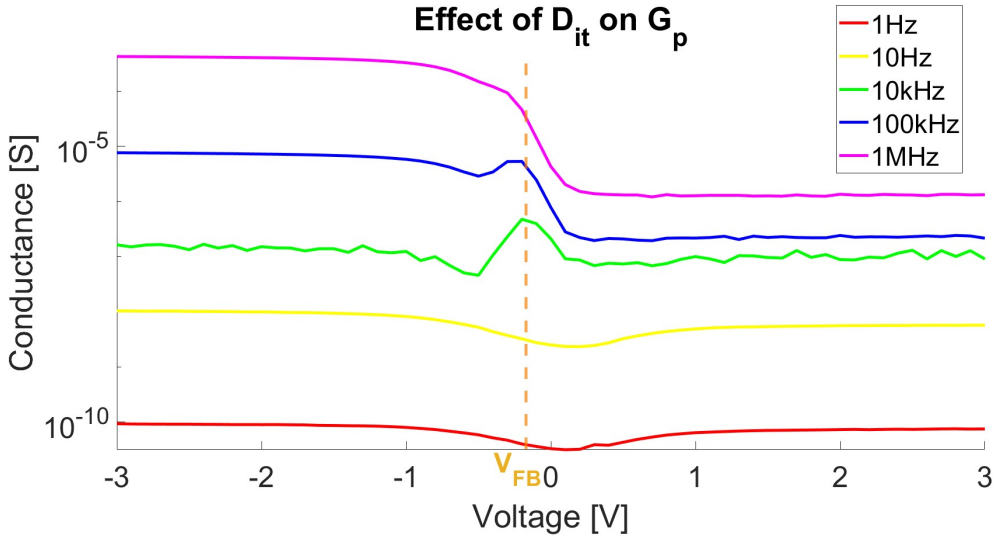

Figure 4.17: Experimental parallel conductance curves measured in this project on an MFIS stack with a W gate metal and 12 nm of Si:HfO_2. The resonance of G_p is confirmed to occur at V_{FB} (calculated with the $\frac{1}{C^2}$ method presented in 4.1.5), i.e. at the onset of depletion. The peak shows up for 100 kHz and 10 kHz. Passing from 100 kHz to 10 kHz, the resonance gets more pronounced: the maximum of $\frac{G_p(\omega)}{\omega}$ is therefore expected to exist between 10 kHz and 10 Hz. At 1 MHz, 10 Hz and 1 Hz the resonance is absent, which may suggest the dominance of bulk traps over D_{it} for very high and very low frequencies.

4.1.8 The effect of border traps

As stated before, CV curves were measured by performing a double sweep in V_G, first from accumulation to inversion ($V_G(\uparrow)$, forward sweep) and then from inversion to accumulation ($V_G(\downarrow)$, reverse sweep). By comparing the forward and reverse curves, an hysteretic behavior was observed. However, since in principle the tested MFIS are non-switching capacitors (para. 4.1.4), this phenomenon has to be attributed to the effect of border traps rather than to ferroelectric domains [57] [69] [70] [71] [72] [73] [74] [75]. The border traps (or near interface oxide traps, NIOTs) are classified as traps present inside the gate oxide very close to the gate oxide/substrate interface (SiO_2/Si in our case) that are able to exchange carriers with the surface of the substrate via tunneling [29] [76]. The nature of these traps is still matter of discussion but most of them belong to the general class of E' centers, i.e. oxygen vacancies due to the presence of trivalent Si defects inside the SiO_2 crystal (including many variants depending on the local properties of the crystal around the defect, such as E'_γ, E'_δ, E'_s, etc.) [72]. These defects are typically caused by high temperature annealing, electrical stress or irradiation [69] [71]. Moreover, it is generally accepted that the maximum distance at

which these traps can interact via tunneling with Silicon is 2÷3 nm [29] [69] [76]. It is also quite common the distinction between fast and slow border traps: the former behave similarly to interface traps but have a slower response, the latter are deeper in the oxide, are slower than fast traps and are considered the main responsible of the hysteresis during the sweep of the bias [70] [72]. In order to model the behavior of border traps, we can modify the cross section in the expression of the trap time constant (para. 4.1.6) by introducing a space-dependence [57] [29]:

$$\sigma_x = \sigma \, \exp\Big(-\frac{x}{\lambda}\Big), \quad \tau_{bt} = \frac{1}{\sigma_x \, v_{th} \, n} = \tau_0 \, \exp\Big(\frac{x}{\lambda}\Big)$$

where x is the distance of the trap from the Si/SiO_2 interface, τ_0 is the trap time constant at the interface and λ is the attenuation length ($\simeq$ 1Å, inversely proportional to the square root of the tunneling effective mass and of the energy barrier height between the semiconductor and the oxide). This implies that deeper traps are also slower traps [29]. At this point, Heimann and Warfield offer a formulation that is very useful to explain the hysteresis caused by border traps [57] [75]. Given T_m as measurement time, one can define the maximum distance of electron capture x_m and the maximum distance of electron emission x_e as follows:

$$x_m = \frac{1}{\lambda} ln[T_m \sigma v_{th}(n_s + p_1)], \quad x_e = \frac{1}{\lambda} ln[T_m \sigma v_{th}(p_s + n_1)]$$

If $x_m > x_e$, some electrons will remain in the traps and will exert an influence on the channel during the reverse sweep, thus provoking the hysteresis.

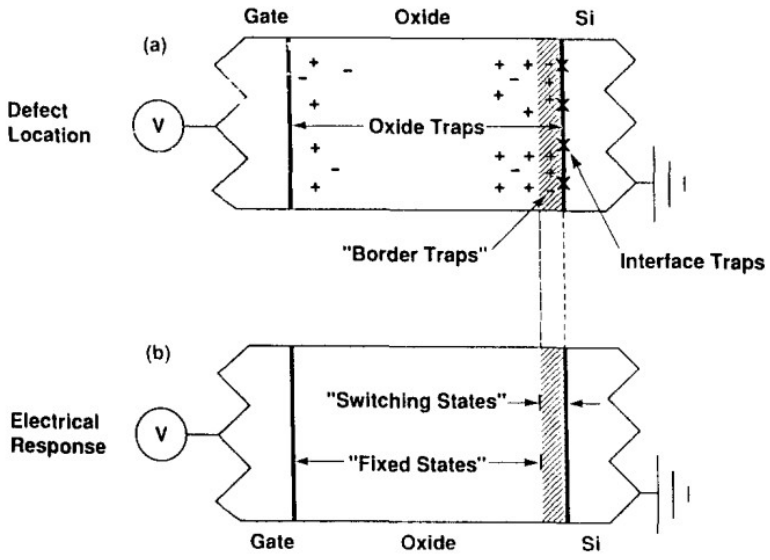

Figure 4.18: Location and electrical behavior of oxide traps, border traps and interface traps. The depth of border traps depends on the time of measurement as well as on the applied bias [70].

Several attempts have been made in order to precisely evaluate the density of border traps. One way is by measuring the voltage shift observed in the CV curves around the midgap voltage after performing a double sweep in V_G [70] [72] [74]. However, it should be specified that several systematic tests are required for a precise evaluation of border trap density N_{bt}, since it could be sensitive to various factors: for example, it has been reported its dependence on the bias ramp rate (that in our case was 50 mV/s) [69] [70]. This is reasonable since border traps are very slow ($\tau_{bt} \simeq 0.01 \div 1s$, i.e. $100 \div 1Hz$ [29]) and therefore only those traps with $\frac{1}{\tau_{bt}}$ larger than the DC-sweep frequency are responsible of the hysteresis and can be characterized. Since the analysis of border traps was not the main focus of the project, an approximated value of N_{bt} was considered sufficient. The expression used to evaluate N_{bt} is the following:

$$N_{bt} = \frac{\Delta V_{bt} C_{ox}}{qA} = \frac{\Delta V_{bt} \epsilon_0 \epsilon_{ox}}{qEOT}$$

In fig. 4.19 an example of hysteresis observed during this project is shown. The effect attributed to border traps is a positive voltage shift and a counter-clock wise loop. The sign of the shift suggests the following behavior: after the accumulation $\Rightarrow$ inversion sweep, border traps are filled with electrons because of the increasing positive

bias. Hence, during the reverse sweep some trapped electrons exert an extra negative bias on the channel. For this reason a less negative external bias is needed to build-up the accumulation.

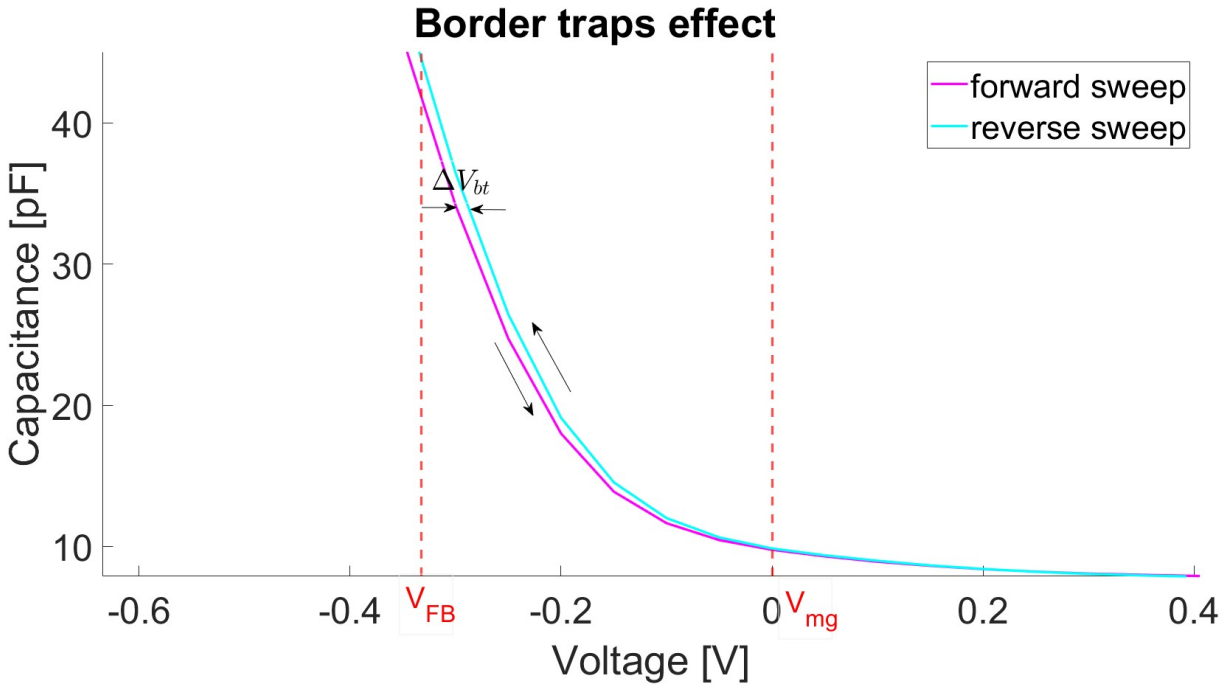

Figure 4.19: Hysteresis attributed to border traps observed on the CV curve extracted in this project from an MFIS stack with Ti+Pt gate metal, 12 nm of Si:HfO_2 and 5 nm of SiO_2. The stretch-out in V_G arises during the reverse sweep starting from midgap ($V_{mg} \simeq 0$ V) and stabilizes at a value of $\Delta V_{bt} \simeq 10$ mV at V_{FB}. The calculated N_{bt} is 3.26 $\times$ 10^{10} cm^{-2}.

4.2 Testing of MFM stacks

4.2.1 FeCAPs properties and the wake-up effect

The performance of ferroelectric capacitors mainly regards their potential for data storage and power efficiency. For this reason, the main figures of merit that characterize FeCAPs are the remnant polarization 2 P_r and the memory window 2 V_c (MW). A high P_r guarantees large and stable data storage. A wide MW on one hand allows a higher data retention, on the other hand may require a too high energy consumption for the polarization switching. A further limitation to a large MW is the endurance. The endurance is the resistance to degradation of the device before fatigue occurs (i.e. the reduction of the polarization after different voltage cycles) and its value is threatened by a large V_c close to $V_{breakdown}$ [77] [78] [79]. A trade-off is therefore needed and a moderate value of the MW is the best compromise. As already stated in para. 2.1.1,

the hysteresis of the polarization-voltage PV (or polarization-field PE) curve is the most important feature of ferroelectric capacitor, since it is what make them suitable for memory applications. However, prior to exhibiting a fully developed hysteretic behavior and a maximum P_r, ferroelectric thin films need to undergo the so-called wake-up effect. The wake-up effect is the widening of an originally pinched hysteresis loop by means of several voltage cycles. P_r progressively increases while cycling [80] [32]. This phenomenon represents a drawback since the material in its pristine phase is not behaving as desired; moreover, because of the wake-up effect the remnant polarization is not stable enough and may induce a misreading of the stored data [80]. The most widely accepted causes behind this phenomenon in HfO_2 thin films are the following: 1) a redistribution of defects (mainly oxygen vacancies) which leads to a depinning of ferroelectric domains and a consequent reduction of the built-in depolarization field, 2) an increase of the fraction of ferroelectric orthorhombic phase over the monoclinic non-ferroelectric one, thanks to the action of oxygen vacancies [78] [80] [32] [32] . In order to characterize the MFM stacks, pulsed voltage wake-up cycles were therefore needed. In particular, four types of measurements were performed:

- **hysteresis test**, used to monitor the hysteretic behavior of the capacitor by means of V-shape voltage pulses
- **DC IV test**, used to isolate the switching current (plus leakage) from the displacement current
- **PUND test**, used to wake-up the domains and check whether the hafnia still acts as an oxide after applying several iterated PUND (Positive, Up, Negative, Down) cycles
- **DC+AC CV test**, used to study the capacitance at different frequencies

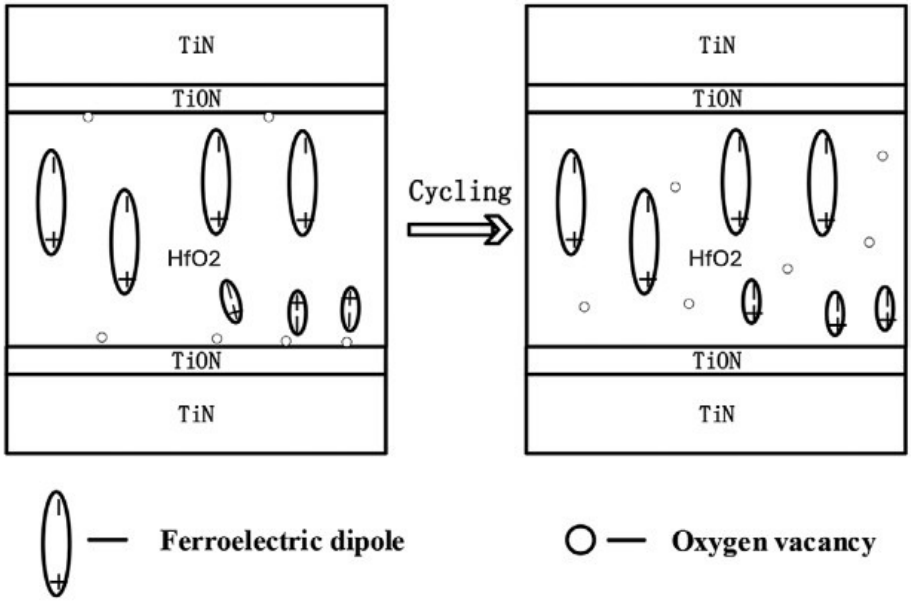

Figure 4.20: Depinning of ferroelectric domains after wake-up cycling. Oxygen vacancies leave the interface between HfO_2 and TiON and approach the center of the HfO_2 film, thus reducing their Coulombic interaction with dipoles at the extremities of the oxide. Adapted from [80].

4.2.2 Connections and measurement setup

The measurements on FeCAPs were performed by means of the already used Keithley multimeter. However, this time two probes were used to contact the two staggered electrodes of the MFM capacitor and three types of modules were needed: the PMU (Pulse Measure Unit), the SMU and the CVU. The last two units (already seen in MFIS measurements) were employed respectively for DC measurements and C-V measurements. Whereas the PMU was used to perform ultra-fast voltage sourcing and simultaneous current and voltage measurements with high resolution [39]. Along with these modules, two single-channel RPMs (Remote Preamplifier/Switch Modules) were employed for different purposes: to switch from PMU to SMU and CVU, to reduce the parasitic effects of cables and to allow low-current measurement ranges [39]. Four triaxial cables were adopted for SMU connections and four coaxial cables for the CVU. Two HDMI cables were used to interface the PMU ports to the RPMs.

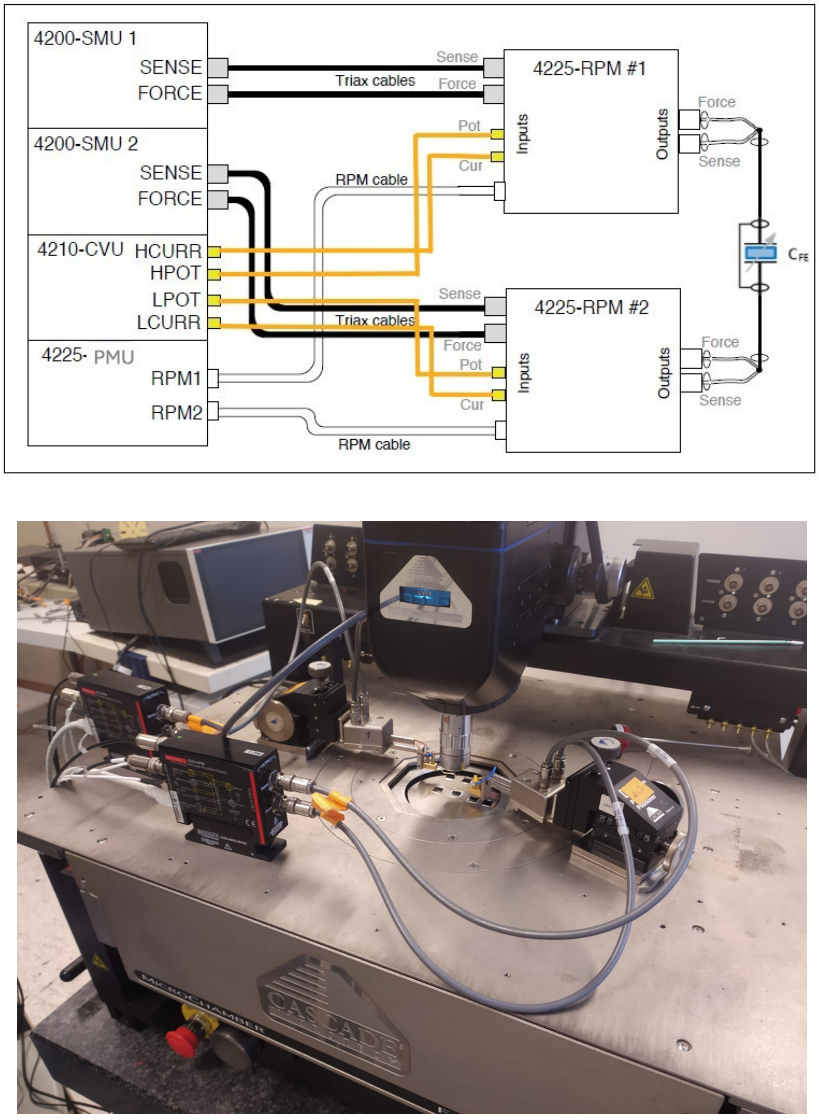

Figure 4.21: MFM measurement setup. Up: design of the setup (adapted from [39]). Down: probe station with the two RPMs and two manipulators used in MFM electrical tests

4.2.3 Hysteresis test: current and charge-voltage curves

In this project, the hysteresis test was a dynamic hysteresis measurement performed by means of an input voltage waveform made of positive and negative V-shape pulses. These tests were performed before and after each wake-up in order to check the opening of the PV loop. Between one wake-up and the other, the amplitudes chosen for the triangular pulses were progressively increased from 1 V to 4 V with a step of 1 V. During each hysteresis test, the current was continuously measured: by integrating the current

over time, the Keithley provided the charge vs voltage curve [39] [81]. From the QV loop, the PV hysteresis is easily extracted dividing by the area of the capacitor. The measured current is the sum of three different components: displacement current, switching current and leakage current. The displacement current is the current generated by the varying electric field applied to the capacitor. Since the ramp of the input voltage has a constant slope $\frac{dV}{dt}$, the displacement current can be considered almost constant in magnitude, i.e. $i_{\mathrm{d}} \simeq C\frac{dV}{dt}$, with a sign that depends on the sweep direction [81]. For what concerns the switching current, this consists of at least two spikes found in correspondence of the positive and the negative coercive voltage. However, the quality factor and the number of these spikes are affected by the wake-up cycles and depend on the distribution of oxygen vacancies, which in turns are responsible of built-in fields. In fact, the presence of two or more peaks around $\mathrm{V_c}$ indicate that different domains switch at slightly different voltage: at a certain $\mathrm{V_{bias}}$ some of them become depinned while some others may remain pinned. After wake-up cycles, oxygen vacancies are redistributed and the spikes tend to merge in one [80] [82] [83]. The switching and leakage current can be separated from the displacement current by means of a DC measurement of the IV curve. Regarding the PV loop, before the wake-up the curve is typically pinched, hence the maximum 2 $\mathrm{P_r}$ was measured after the last wake-up cycle on a well-opened hysteresis.

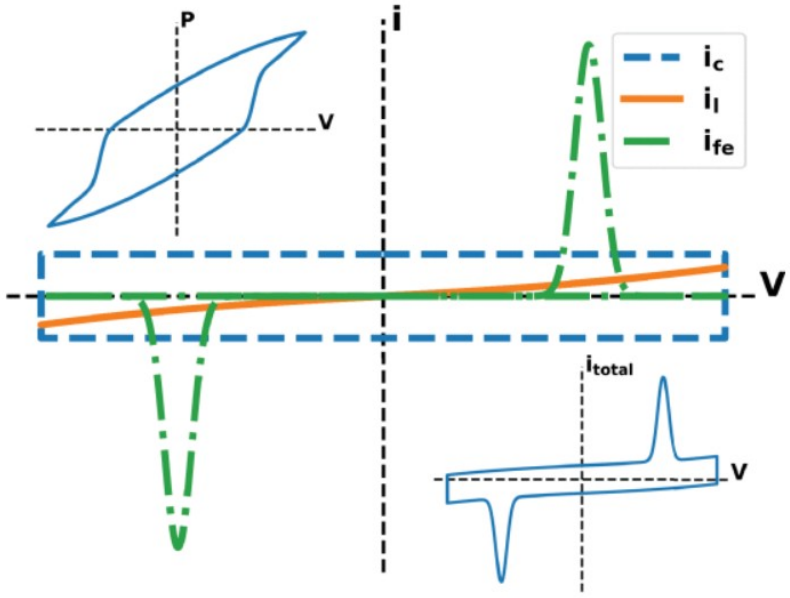

Figure 4.22: PV hysteretic loop (top left) and IV hysteretic loop (bottom right) in MFM capacitors. At the center, the three components of the measured current are shown: $\mathrm{i_c} \equiv \mathrm{i_d}$ is the displacement current, $\mathrm{i_l}$ is the leakage current, $\mathrm{i_{fe}}$ is the switching current [84].

4.2.4 PUND test: wake-up and charge-iterations curves

This test consists in applying several cycles of PUND forming pulses. The PUND waveform is a sequence of four pulses: positive, up, negative, down. The P and N pulses act as switching pulses, hence they are used to measure the total current involving switching, displacement and leakage currents. While the U and D pulses only measure the contribution of leakage and displacement currents, since they have the same polarity of P and N respectively [39] [85]. In this way, by subtracting the P(N) response to the one of U(D), the polarization charge can be extracted. In particular, the Keithley extracts Q_{SW}, i.e. the average of the polarization charge accumulated after the positive and after the negative switch as follows:

$$Q_{SW} = \frac{(P-U)+(N-D)}{2} \quad [39]$$

The endurance test is used to monitor the degradation in terms of P_r vs iterations, where one iteration is a PUND sequence [39] [85] [86] [87]. However, in this project, the PUND pulses were mainly exploited to perform the wake-up of the hafnia (the actual endurance test typically requires 10^6 iterations). These tests were executed alternately with the hysteresis tests. The first PUND test used pulses of 1.5 V. For the next ones, the amplitude increased with a step of 1 V up to 4.5 V. The maximum number of iterations was 1000 and the value of t_p (width of the pulse), t_d (delay time between one pulse and the other) and t_{rf} (rise and fall time) was 2.5×10^{-5} s.

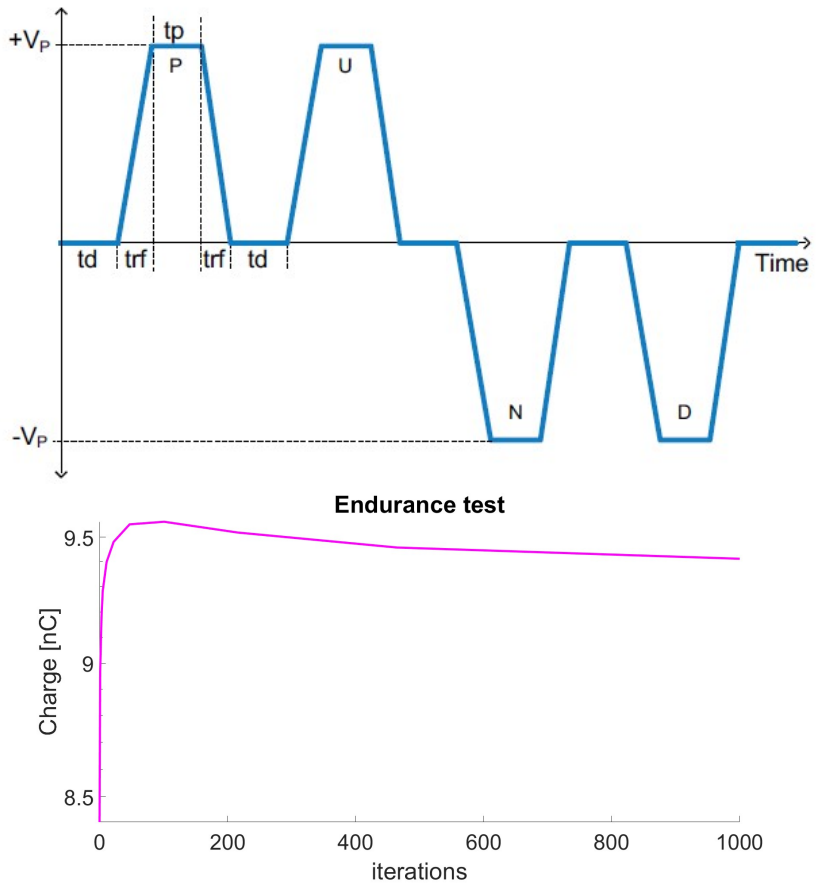

Figure 4.23: Up: input PUND waveform used for the wake-up [39]. Down: endurance test performed in this project with a pulse amplitude of 4.5V. After 1000 iterations, Q_{SW} is slightly reduced.

4.2.5 CV curves

The capacitance-voltage curves were extracted by sourcing the MFM capacitor with a DC voltage superimposed with a small AC signal at 10 kHz and 100 kHz. The measured CV curve show the typical "butterfly" shape [88] [89] [90], that is directly related to the hysteretic behavior of the charge. The ideal capacitance-voltage relationship can be obtained from the expression of the charge according to the Landau-Devonshire theory, by calculating its derivative with respect to the voltage $C = \frac{dQ}{dV}$ [91]. Alternatively, the CV theoretical behavior can be calculated from a modified Johnson formula that describes the dielectric constant as a function of the electric field $\epsilon(E)$ in paraelectric states, by adapting it to ferroelectrics [92]. The ideal curve is expected to have symmetric "wings" with respect to zero bias, whereas in real devices asymmetry arises: this can be attributed mainly to oxygen vacancies that introduce an imbalance between the two

interfaces with the electrodes [89]. As shown in Fig. 4.24, for example, the oxygen vacancies are responsible of the pinning of ferroelectric domains on the positive voltage side, thus inducing a large number of domain walls at zero bias. After passing on the negative voltage side most of domains are correctly switched and domain walls disappear when coming back to zero bias. This causes the existence of two different capacitance states at zero bias, i.e. HCS (high capacitance state) and LCS (low capacitance state), depending on the history of the device [89].

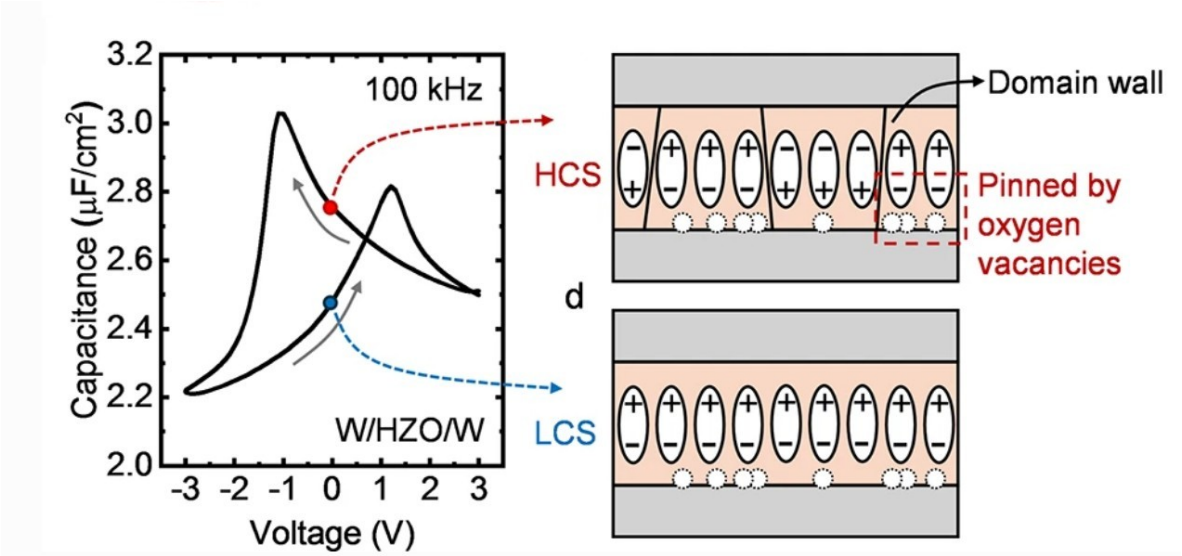

Figure 4.24: CV curve of an MFM capacitor with its typical "butterfly" shape. The asymmetry of the curve is attributed to oxygen vacancies, responsible of a different pinning of ferroelectric domains depending on the sign of the bias. This induces two states at zero bias, i.e. HCS and LCS, which differ in the capacitance value and in the number of domain walls [89]

The most common figure of merit extracted from the CV curves of FeCAPs is the capacitance (or permittivity) tunability [90] [93] defined as:

$$t_{CAP} = \frac{C_{MAX} - C_{MIN}}{C_{MIN}}$$

or

$$t_{EPS} = \frac{\epsilon_{MAX} - \epsilon_{MIN}}{\epsilon_{MIN}}$$

This quantity indicates how much two different states can be distinguished. Typically, the capacitance and the tunability tend to decrease with frequency. This behavior is explained by ferroelectric dipoles lagging behind frequencies that are higher than the inverse of their characteristic time [90].

Chapter 5

Results and discussion

5.1 MFIS results and discussion

5.1.1 Capacitance

In the following, some CV curves extracted from the stacks with 12 nm of Si:HfO_2 w/o annealing are described.
As predicted in chapter 4, the capacitances at LF and HF almost coincide in accumulation. Furthermore, the stacks differing only in the gate metal gave almost the same capacitance in accumulation, which is a reasonable outcome, although some variability was still observed. In particular, for Ti+Pt, TiN and W the $C_{LF,max}$ was respectively $\simeq 214\,pF,\ 222\,pF,\ 205\,pF$ while $C_{HF,\,max} \simeq 205\,pF,\ 214\,pF,\ 210\,pF$ (area capacitor $200\,\mu m \times 200\,\mu m$). When approaching less negative voltages, the C_{LF} crosses the C_{HF} curve: as will be presented later, this crossing point corresponds to the point where the D_{it} curves turn slightly negative. Moreover, as expected, in depletion $C_{LF} > C_{HF}$ and their difference gives us information on the interface traps between 1 Hz and 100 kHz. Finally, in inversion the C_{LF} rises up again to its accumulation value. The C_{HF}, instead, drops because of the dominance of the depletion capacitance. This was predicted as well by the theory presented in chapter 4. The same behavior of CV curves described up to now was observed for the other Si:HfO_2 thicknesses.

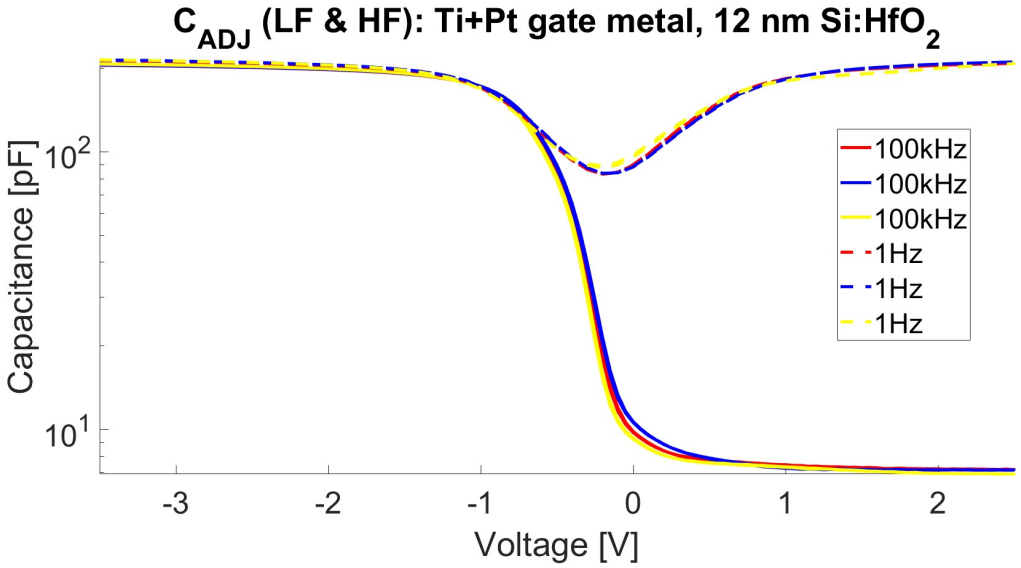

Figure 5.1: C_{ADJ} (LF and HF), Ti+Pt gate metal, 12 nm Si:HfO_2 w/o annealing

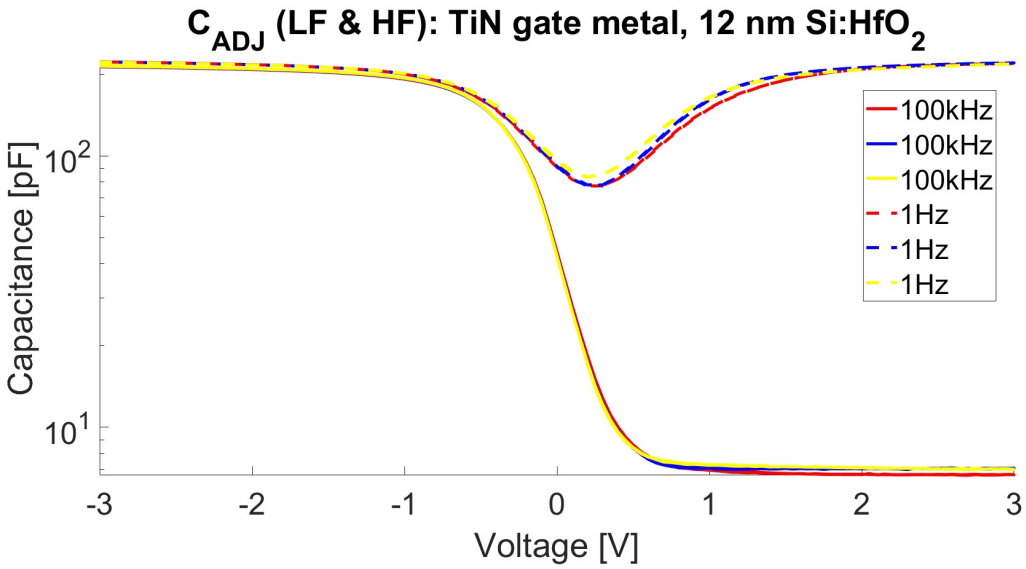

Figure 5.2: C_{ADJ} (LF and HF), TiN gate metal, 12 nm Si:HfO_2 w/o annealing

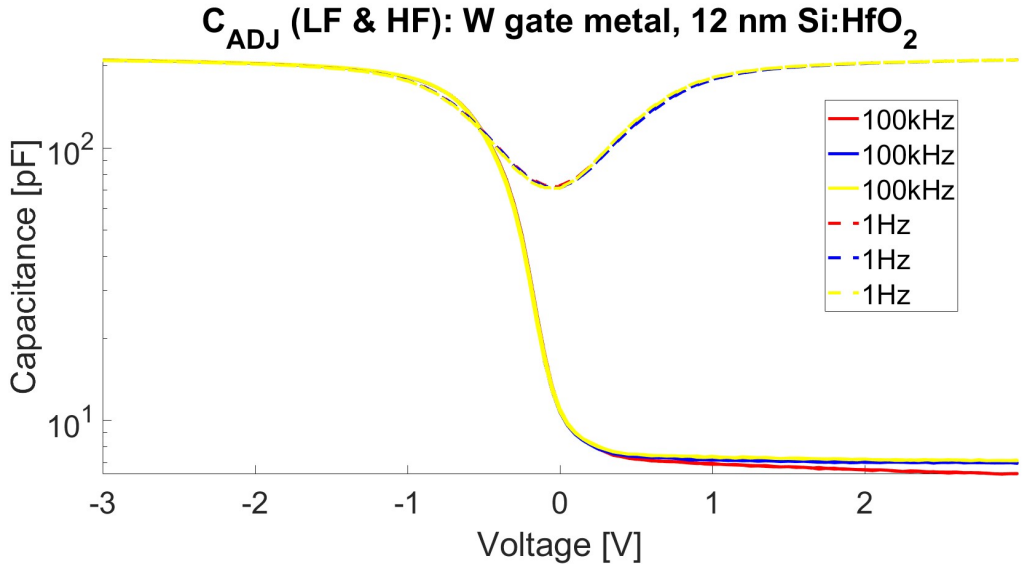

Figure 5.3: C_{ADJ} (LF and HF), W gate metal, 12 nm Si:HfO_2 w/o annealing

In smaller patterns, a smaller capacitance was of course measured. The linearity between C_{ox} and the area was also verified with a linear interpolation across the three capacitance values in accumulation for the three areas (forcing the crossing of the origin). Moreover, the slope was used to extract the EOT.

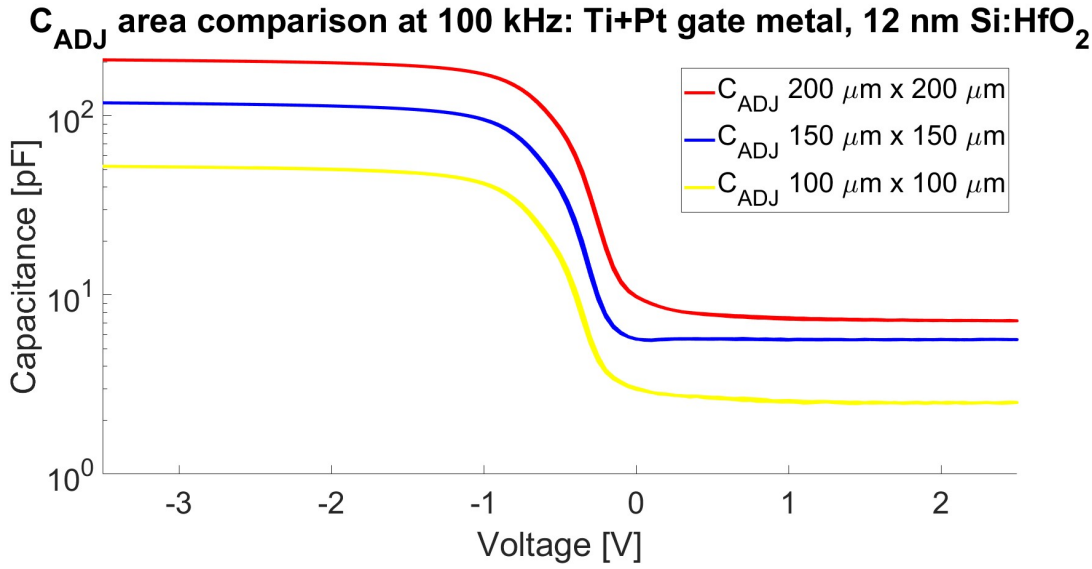

Figure 5.4: Comparison of CV curves measured for the three areas of the capacitors. In this example, only Ti+Pt results are shown, since the gate metal did not influence the values of the capacitance

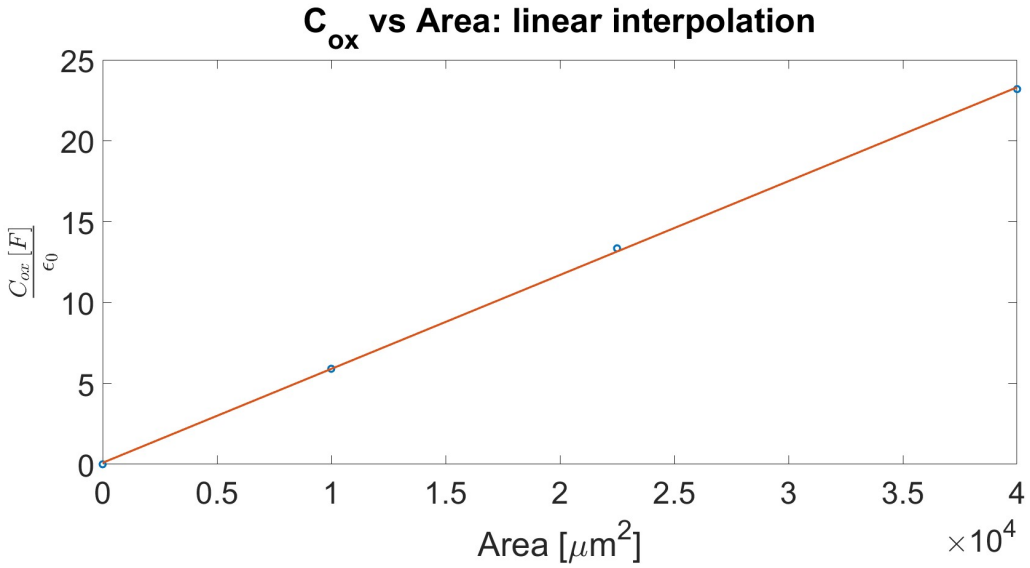

Figure 5.5: Linear interpolation of the capacitance in accumulation for the three areas. The linear relationship is confirmed.

5.1.2 Flatband Voltage

The flatband voltage was extracted with the $\frac{1}{C^2}$ method described in chapter 4. A linear interpolation was performed in the linearity range of the inverse square of the capacitance. In particular, for this purpose 3 replicas per each area were measured and analyzed. In this way, for each type of stack 9 values of V_{FB} were extracted and eventually averaged. An example of extraction from the three areas is reported:

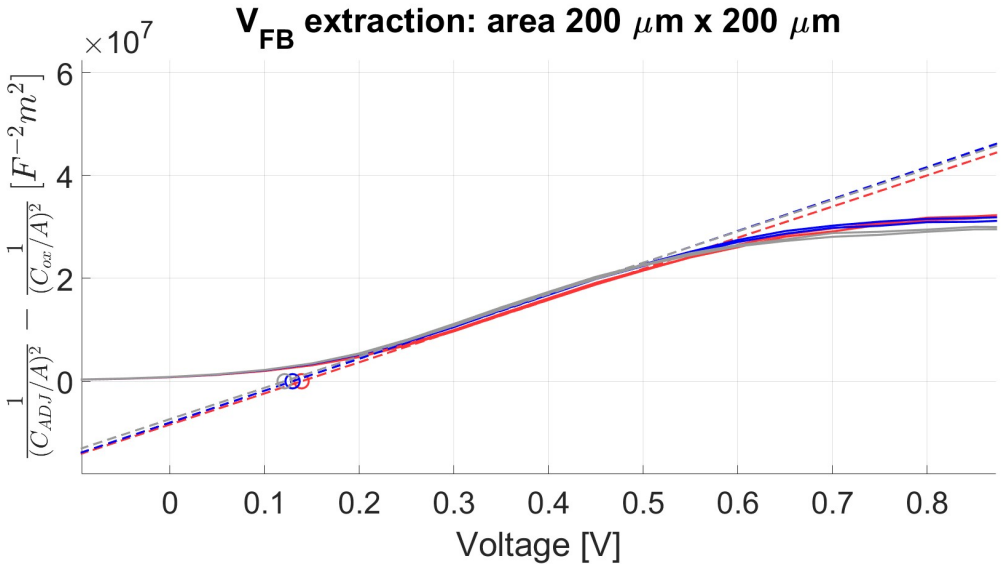

Figure 5.6: V_{FB} extraction from TiN gate metal, 12 nm Si:HfO_2 w/o annealing, area 40000 μm^2

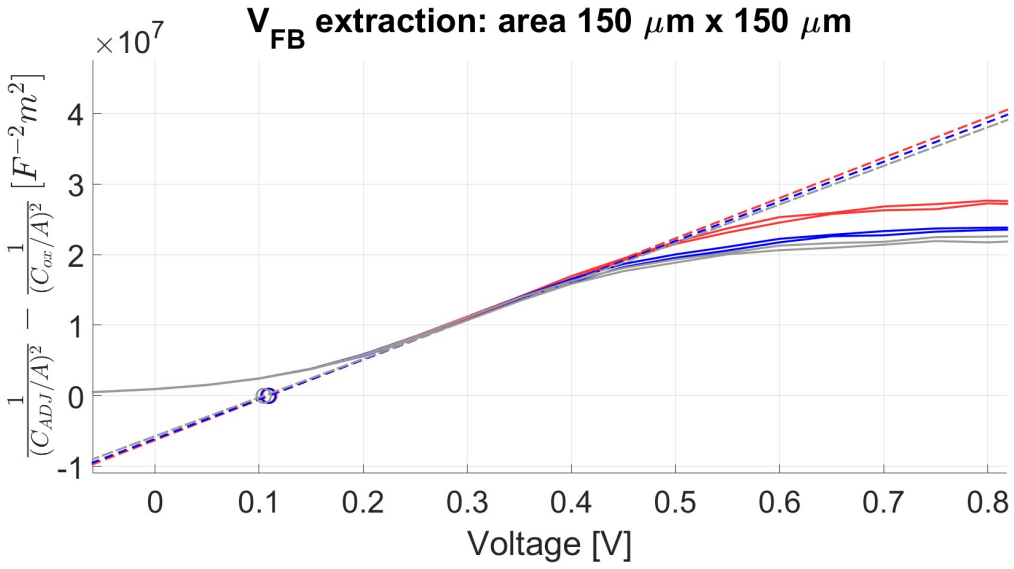

Figure 5.7: V_{FB} extraction from TiN gate metal, 12 nm Si:HfO_2 w/o annealing, area 22500 μm^2

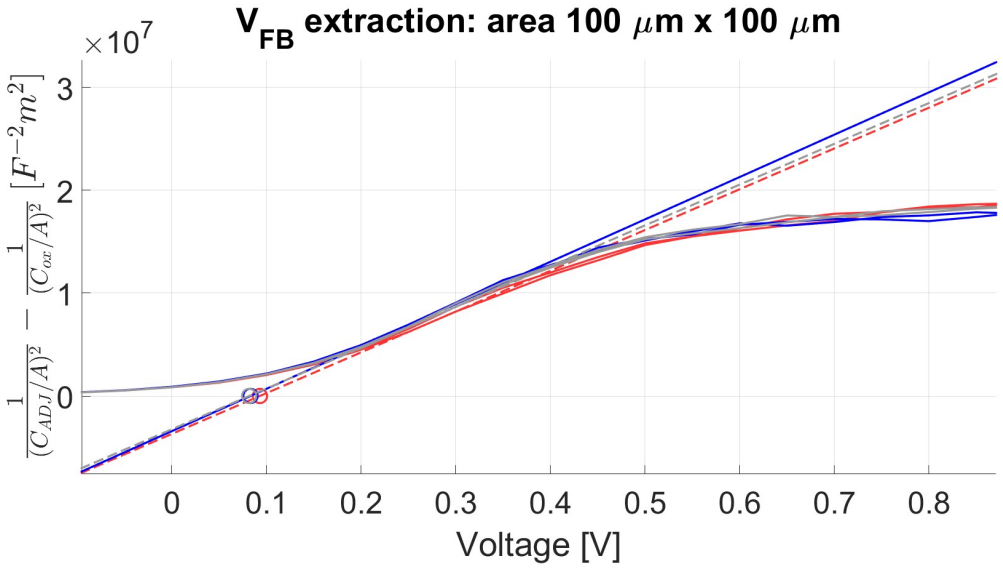

Figure 5.8: V_{FB} extraction from TiN gate metal, 12 nm Si:HfO_2, w/o annealing, area 10000 μm^2

For Ti+Pt and W gate metals stacks, the V_{FB} increased in magnitude and became "more negative" as the thickness of the hafnia increased. Hence, a larger energy consumption is required to reach the flatband condition for thicker gate oxides. Also in the stack with TiN the V_{FB} experienced a shift on the left with the increasing EOT. However, in the case of TiN the values of V_{FB} were always positive or very close to zero.

5.1.3 Work function and effective charge

As presented in chapter 4, the work function and the Q_{eff} were extracted respectively from the y-intercept and from the slope of the linear interpolation of $V_{FB} + \Phi_s$ vs EOT_{HK}. Among the three gate metals, Ti+Pt provided the best fitting. A reasonable value of the work function was extracted for all the three metals [94] [95] [96]. Moreover, in the bimetallic gate having Ti+Pt, the work function can be tuned from the one of Ti (3.9 eV) to the one of Pt (5.3 eV) depending on their thickness [94]. The effect of the annealing was more evident in TiN where the work function was significantly increased. In W, the annealing caused a small increase of the work function, while in Ti+Pt the work function was slightly reduced. Concerning the Q_{eff}, this was always positive since the slope was always negative (see also chapter 4): this may be a confirmation that the actively involved traps were mostly donors, i.e. neutral when occupied and positive when empty, and that they were mostly located in the lower half of the bandgap [29] [31]. The extracted value of $N_{eff} = Q_{eff}/q$ was in the order of 10^{12} cm^{-2} for all stacks.

This order of magnitude was also obtained in the following paper: [31].

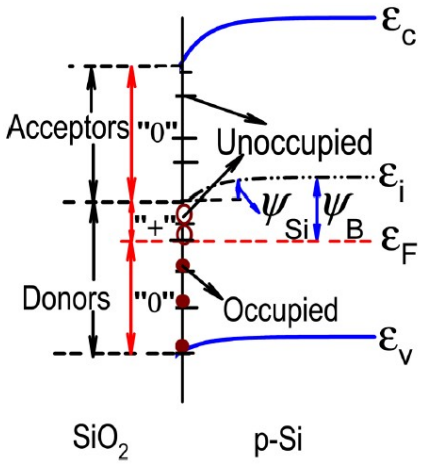

Figure 5.9: Positive donor traps in the p-Si bandgap [31]

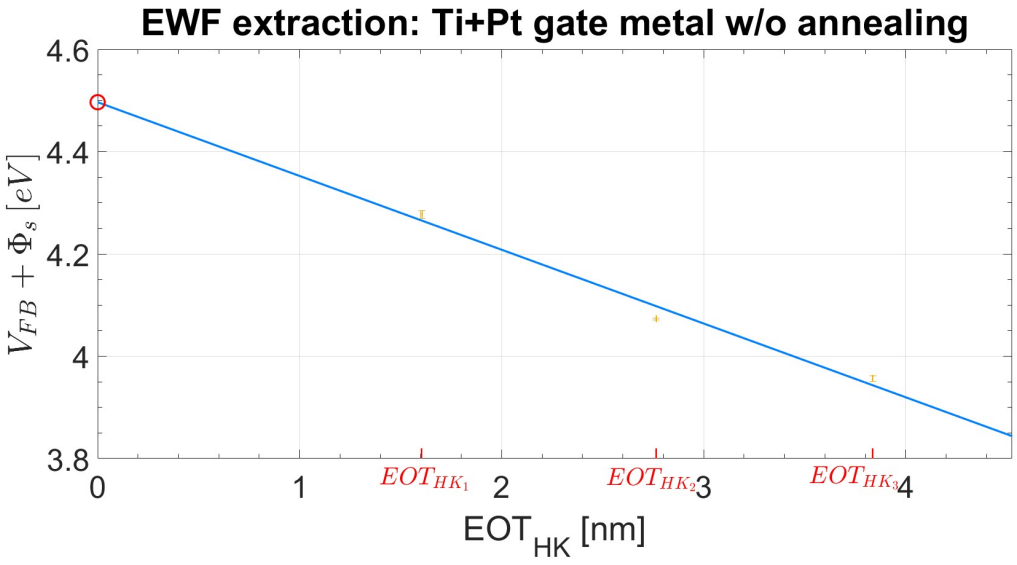

Figure 5.10: Effective Work Function and Q_{eff} extraction from MFIS stack with Ti+Pt gate metal w/o annealing

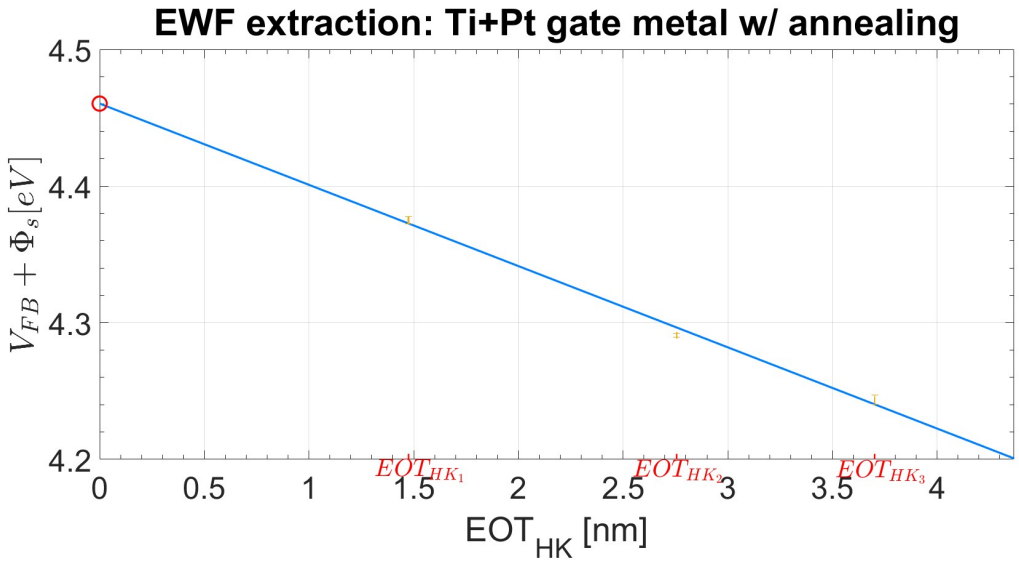

Figure 5.11: Effective Work Function and Q_{eff} extraction from MFIS stack with Ti+Pt gate metal w/ annealing

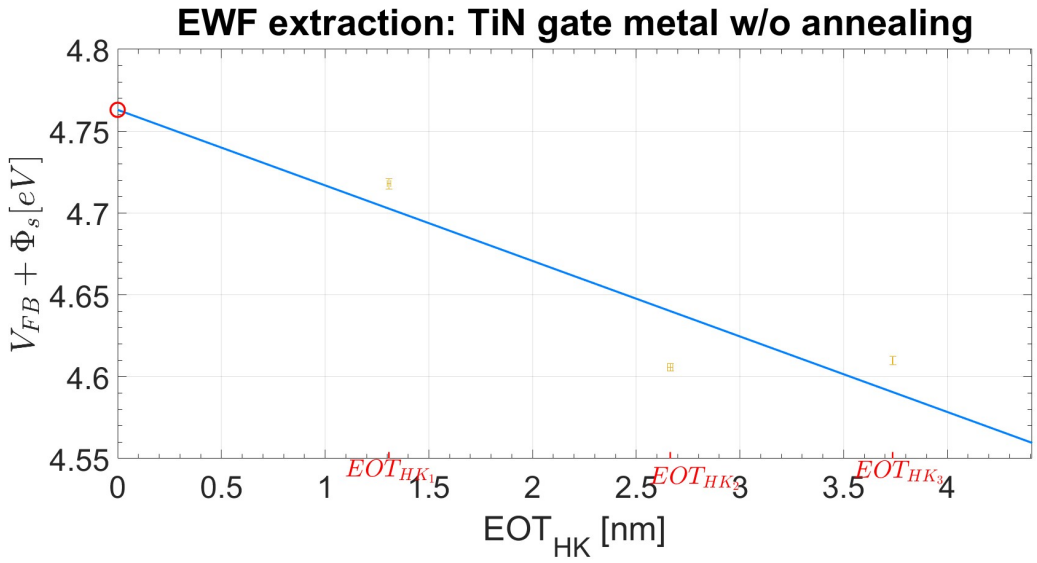

Figure 5.12: Effective Work Function and Q_{eff} extraction from MFIS stack with TiN gate metal w/o annealing

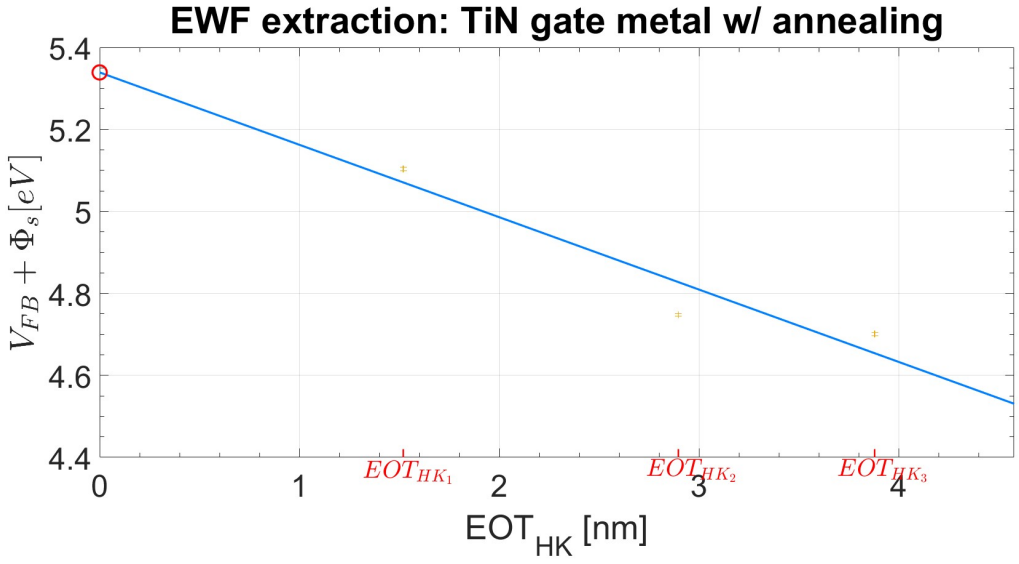

Figure 5.13: Effective Work Function and Q_{eff} extraction from MFIS stack with TiN gate metal w/ annealing

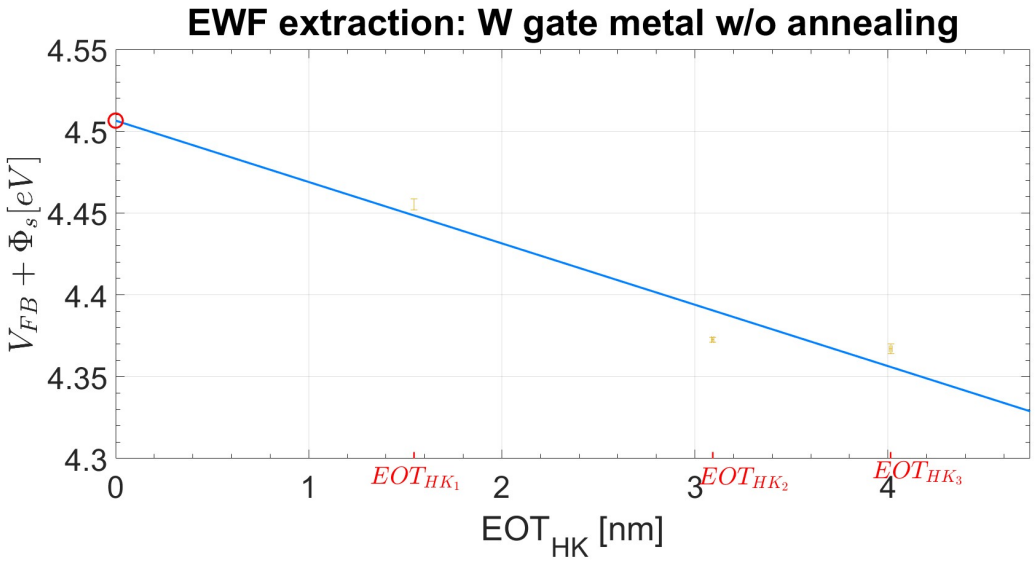

Figure 5.14: Effective Work Function and Q_{eff} extraction from MFIS stack with W gate metal w/o annealing

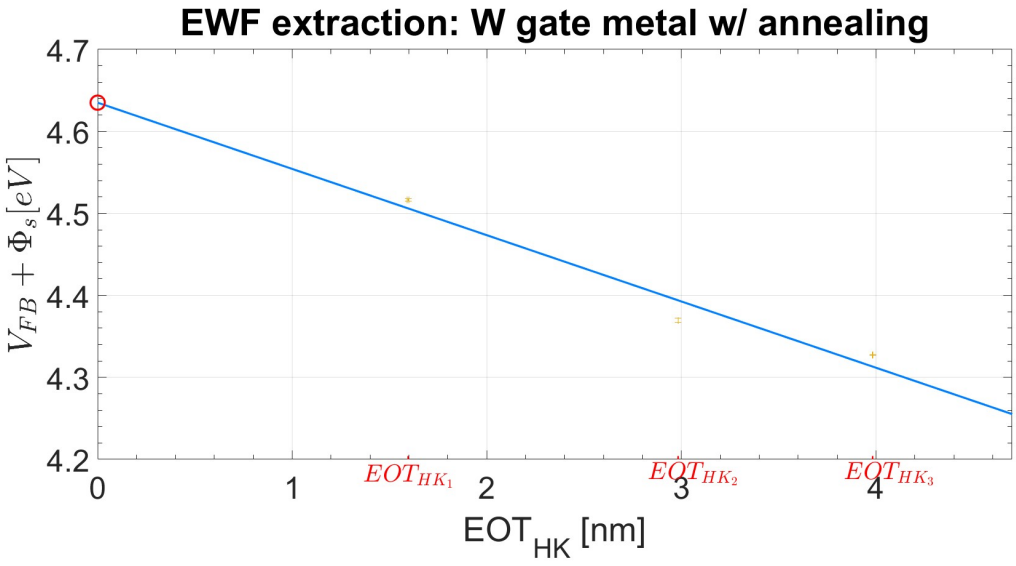

Figure 5.15: Effective Work Function and Q_{eff} extraction from MFIS stack with W gate metal w/ annealing

5.1.4 Interface trap density

The interface trap density curves exhibit the typical shape shown by several books and papers [39] [55] [56] [61] [62] [63] [64] [44]. As previously mentioned, the range of voltages where the curve becomes negative corresponds to a region where $C_{LF} < C_{HF}$. However, the reliable values of the calculated D_{it} are only valid in depletion, i.e. the shaded areas in the plots. The two extremities of these areas are V_{FB} on the left and $V_{midgap} = V_{FB}$ + 0.3 V, where 0.3 V was calculated knowing the position of the Fermi level with respect to the midgap, i.e. knowing the doping density. Almost all the extracted values of D_{it} in depletion are $\simeq 2 \times 10^{12}\ eV^{-1}\ cm^{-2}$, whose order of magnitude is consistent with the one reported in these references: [97] [98]. A part from few exceptions, there is no significant difference between the D_{it} extracted from the samples w/o annealing and w/ annealing, which could suggest that the annealing was not successful in saturating the dangling bonds at the Si/SiO_2 interface.

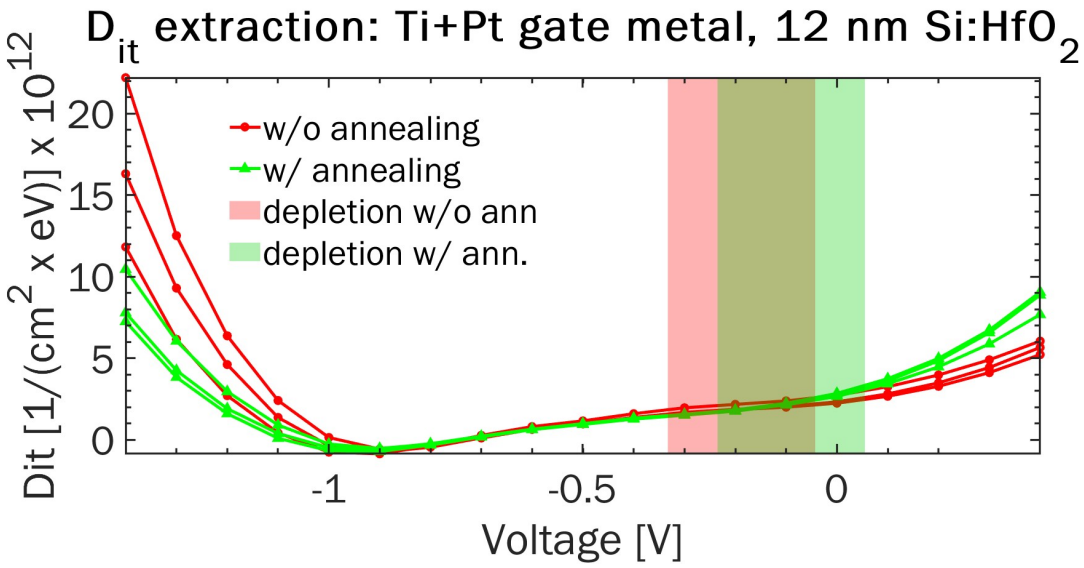

Figure 5.16: D_{it} of MFIS stack with Ti+Pt gate metal and 12 nm Si:HfO_2

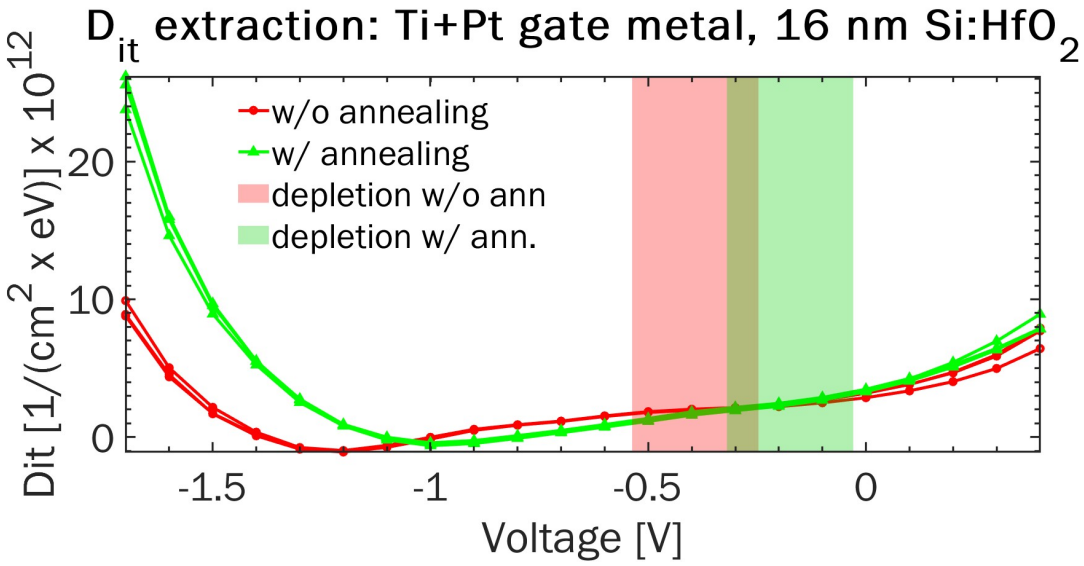

Figure 5.17: D_{it} of MFIS stack with Ti+Pt gate metal and 16 nm Si:HfO_2

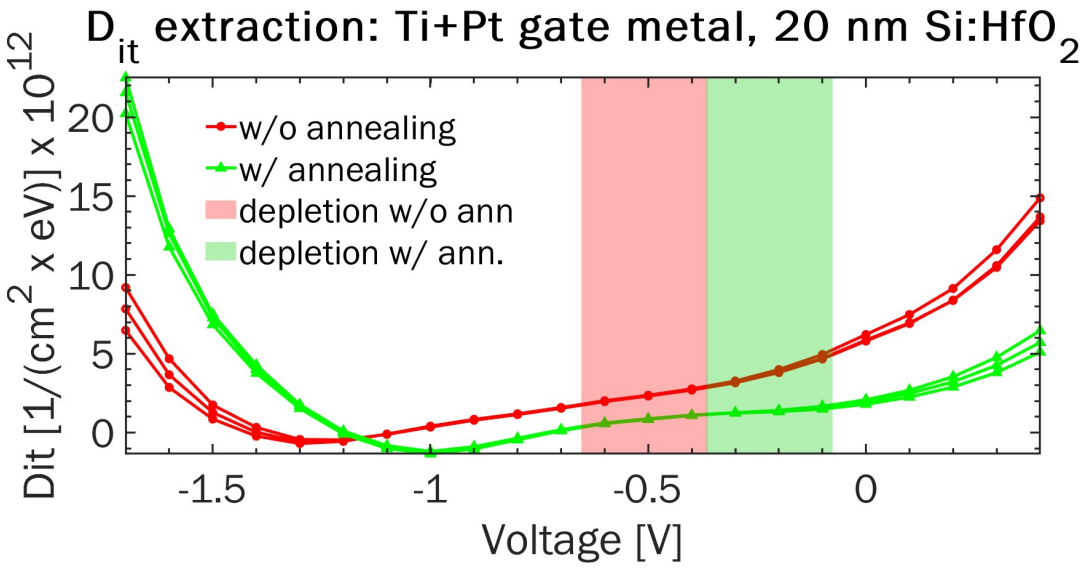

Figure 5.18: D_{it} of MFIS stack with Ti+Pt gate metal and 20 nm Si:HfO_2

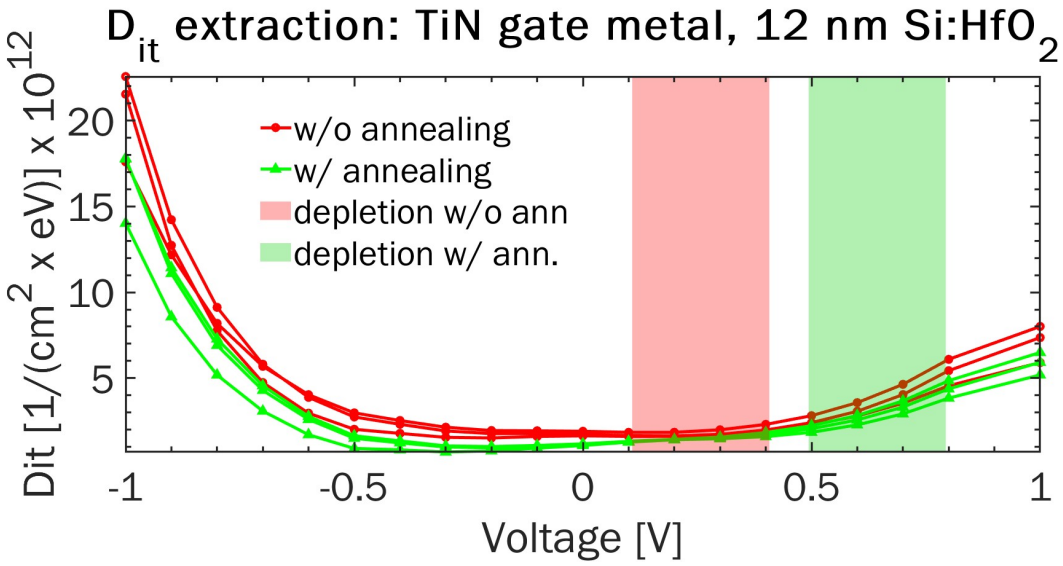

Figure 5.19: D_{it} of MFIS stack with TiN gate metal and 12 nm Si:HfO_2

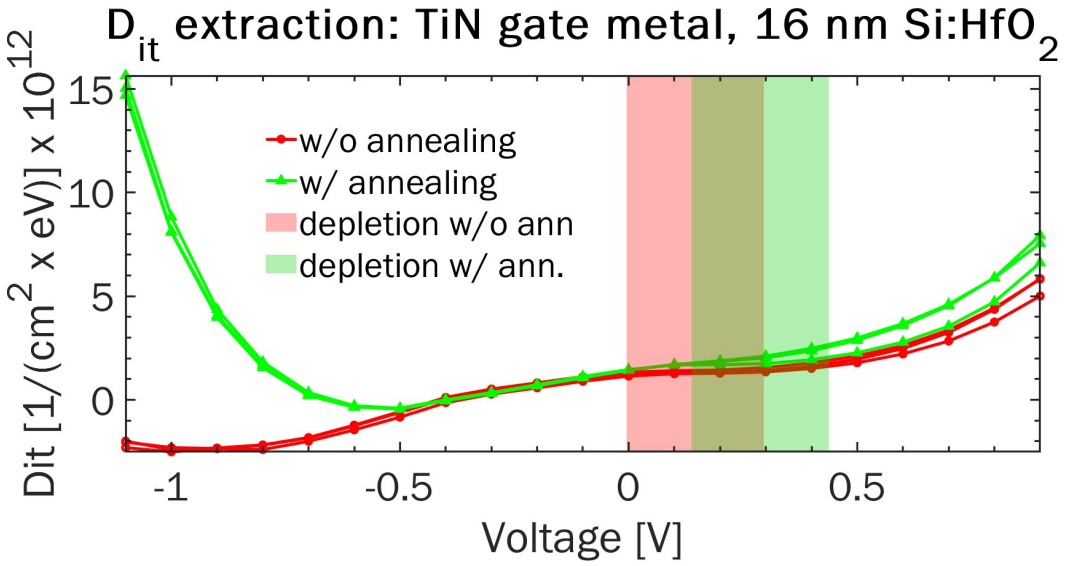

Figure 5.20: D_{it} of MFIS stack with TiN gate metal and 16 nm Si:HfO_2

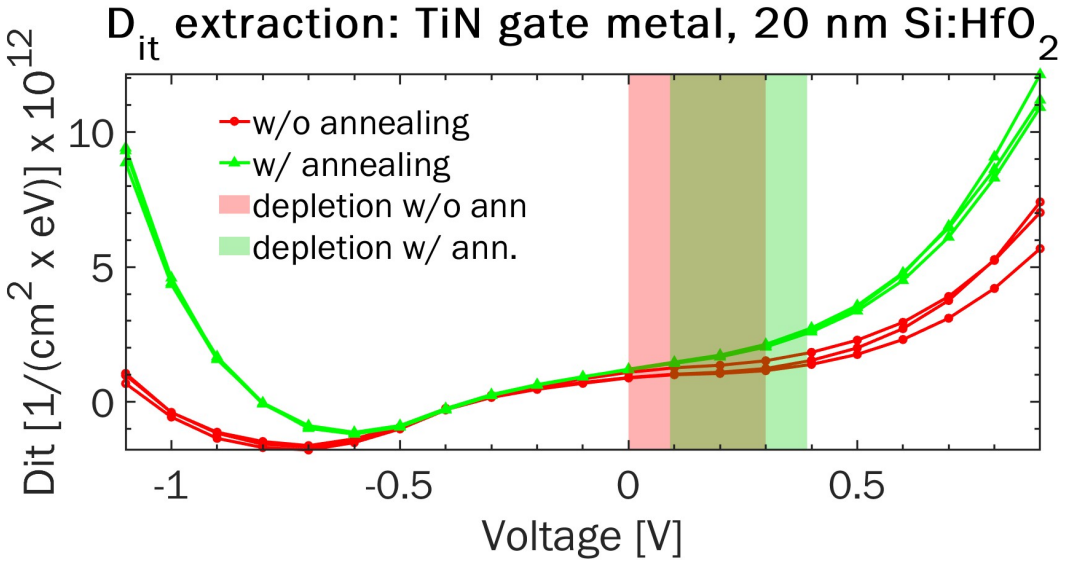

Figure 5.21: D_{it} of MFIS stack with TiN gate metal and 20 nm Si:HfO_2

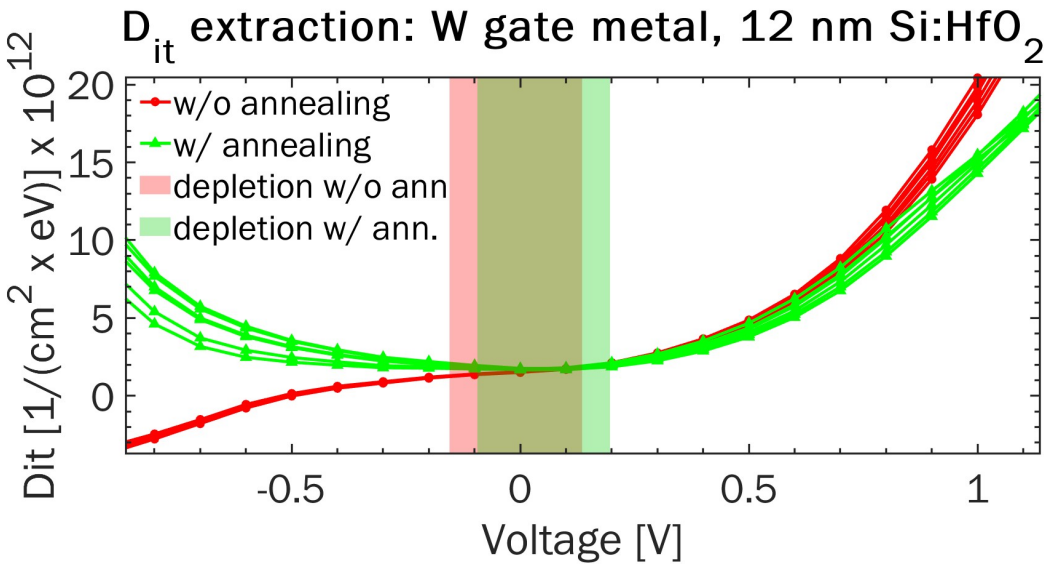

Figure 5.22: D_{it} of MFIS stack with W gate metal and 12 nm Si:HfO_2

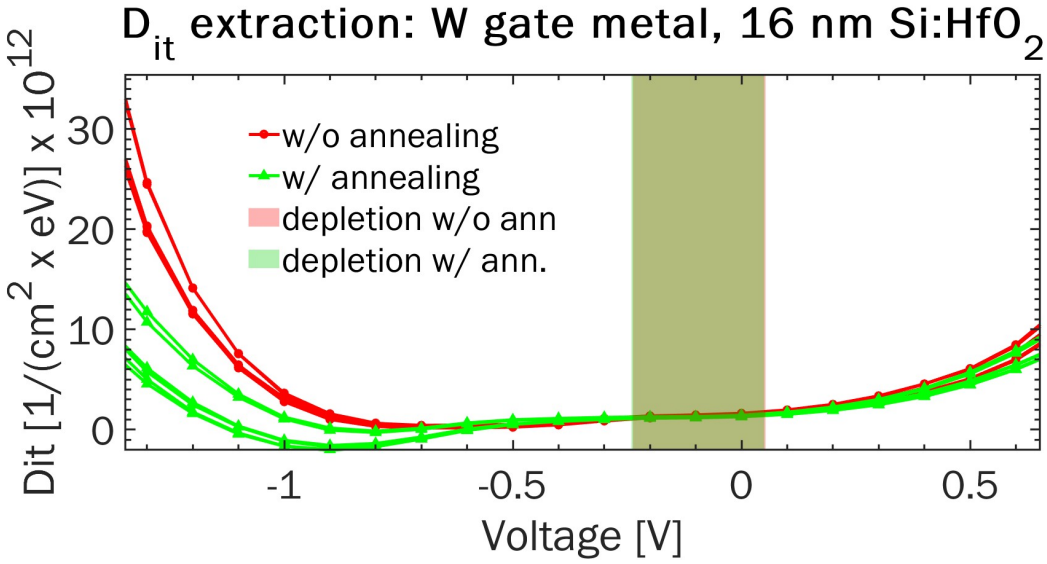

Figure 5.23: D_{it} of MFIS stack with W gate metal and 16 nm Si:HfO_2

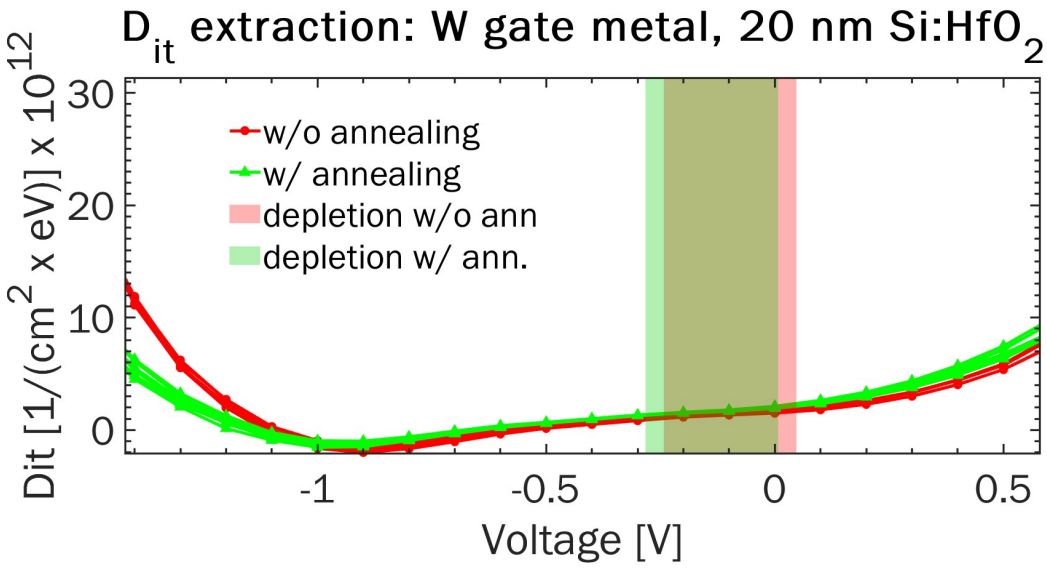

Figure 5.24: D_{it} of MFIS stack with W gate metal and 20 nm Si:HfO_2

5.1.5 Parallel conductance

The G_p vs V_G curves at 100 kHz served two purposes: to verify the dominance of interface traps over bulk traps at 100 kHz and to evaluate the reliability of the V_{FB} extraction method. The resonance occurs around V_{FB} since before and after the flatband τ is too small and its inverse is too large with respect to the small-signal frequency [30] [67]. The Ti+Pt gate metal w/o annealing provided the best resonance peaks exactly in correspondence of the extracted V_{FB}. Moreover, in the TiN w/ annealing curve, a second peak in weak inversion was observed. This can happen because of the interaction with electrons that start populating the channel: in this case the model describing τ gets more complex and can induce a second resonance peak [68].

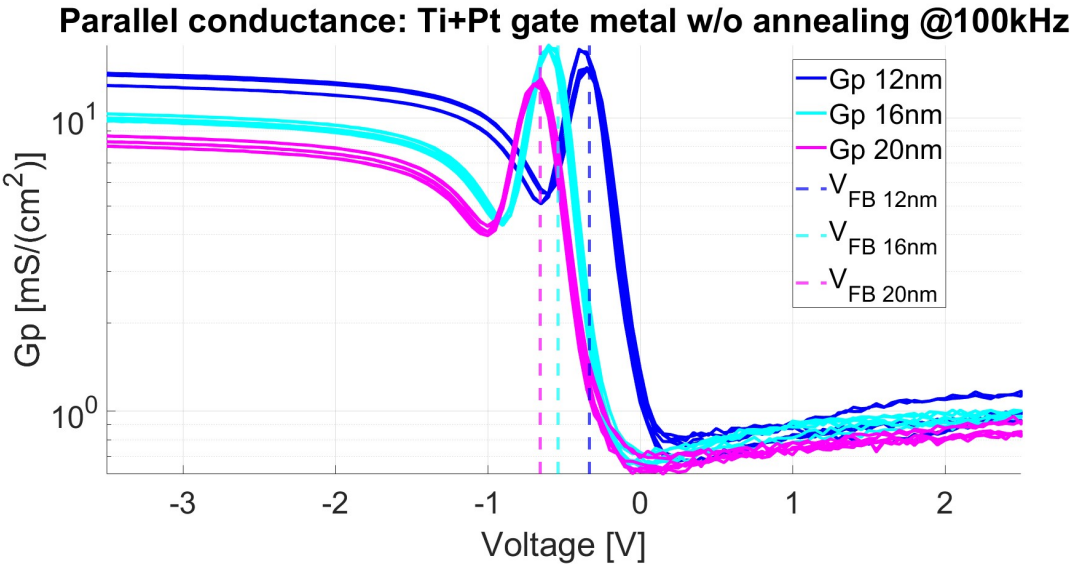

Figure 5.25: G_p of MFIS stack with Ti+Pt gate metal w/o annealing at 100 kHz

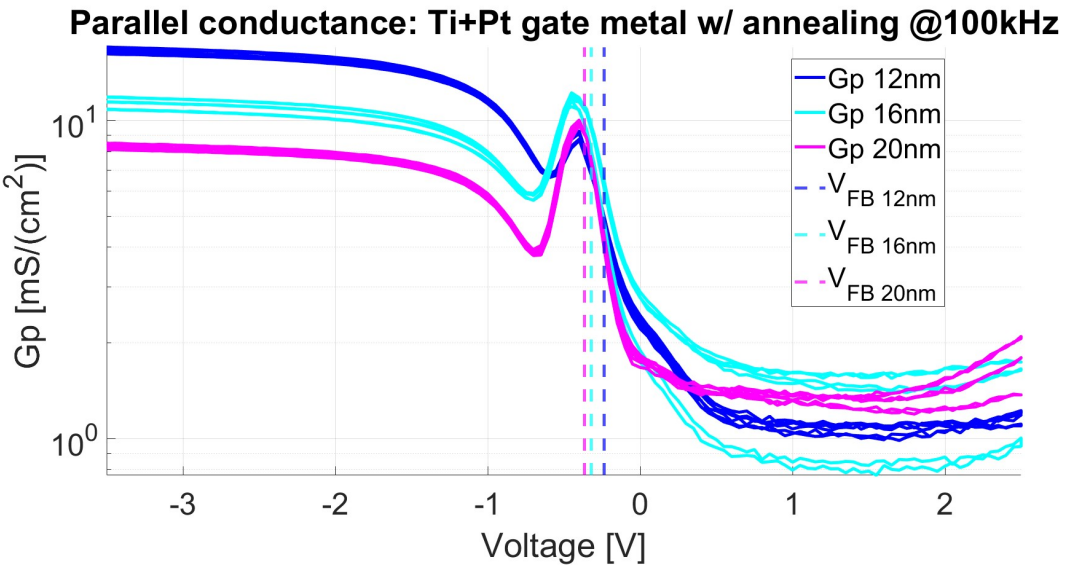

Figure 5.26: G_p of MFIS stack with Ti+Pt gate metal w/ annealing at 100 kHz

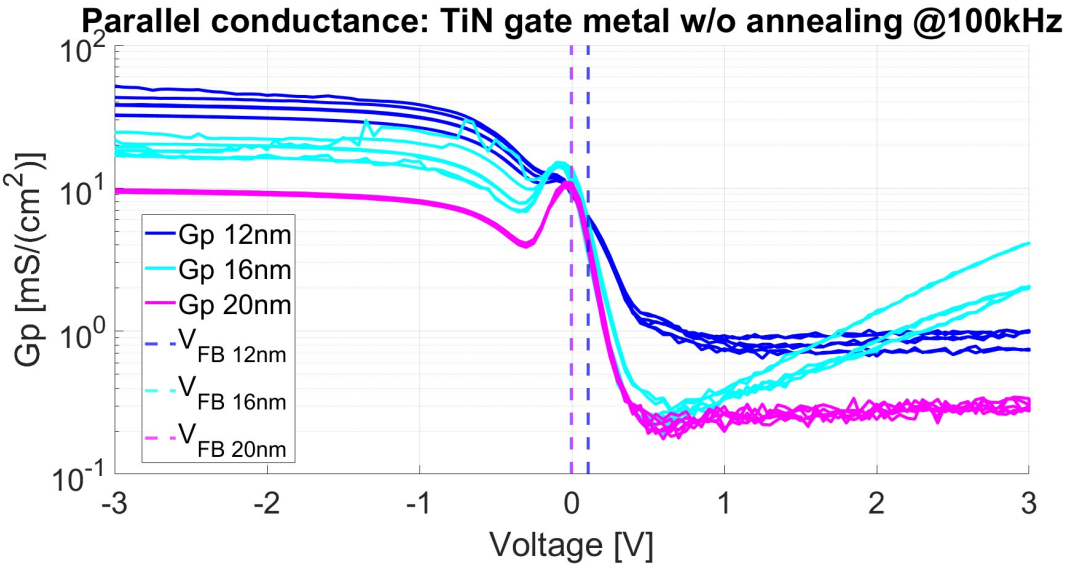

Figure 5.27: G_p of MFIS stack with TiN gate metal w/o annealing at 100 kHz

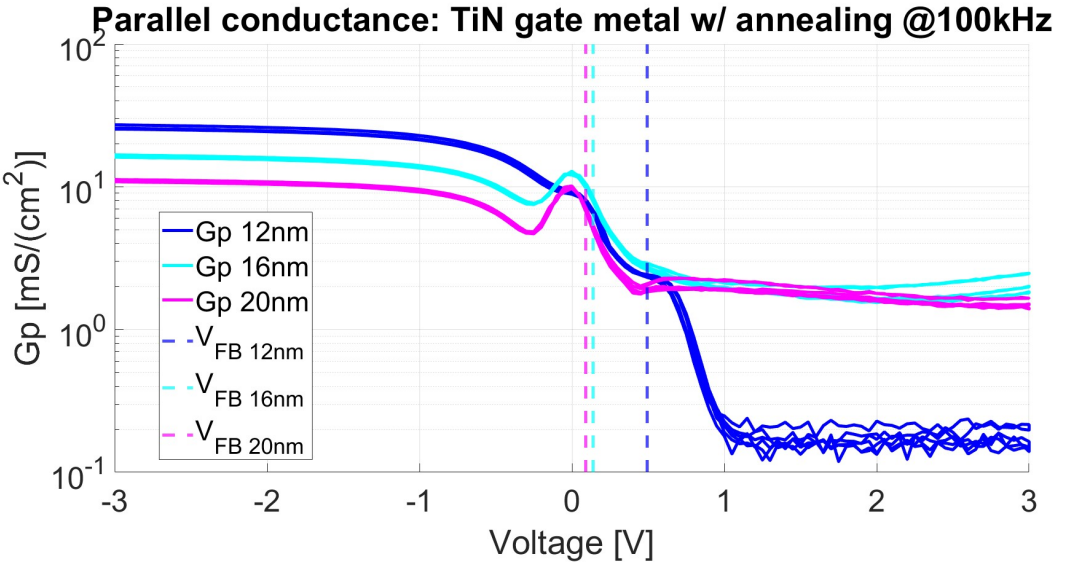

Figure 5.28: G_p of MFIS stack with TiN gate metal w/ annealing at 100 kHz

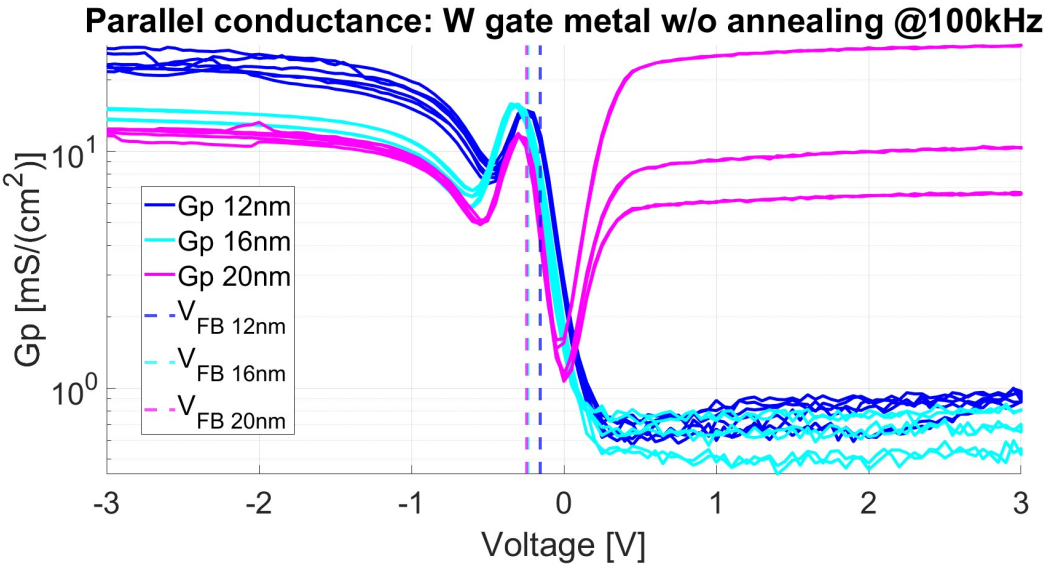

Figure 5.29: G_p of MFIS stack with W gate metal w/o annealing at 100 kHz

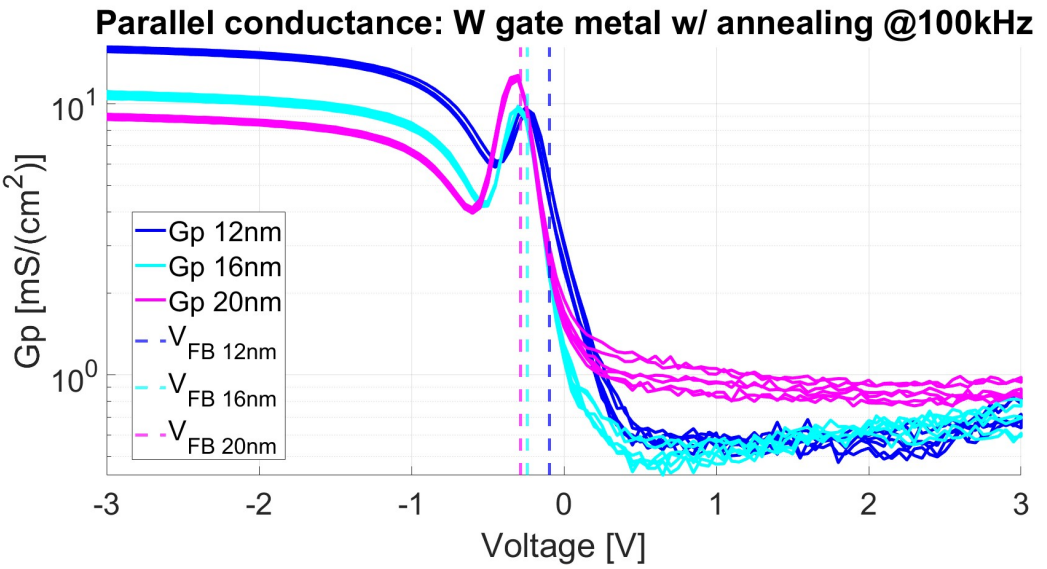

Figure 5.30: G_p of MFIS stack with W gate metal w/ annealing at 100 kHz

5.1.6 Comprehensive tables of findings

Table 5.1: Ti+Pt results

Ti+Pt			
$\Phi_{m,eff}$ [eV]		4.50 A: 4.46	
N_{eff} $\times 10^{12}$ $[cm^{-2}]$		3.10 A: 1.28	
	12 nm	16 nm	20 nm
V_{FB} [V]	-0.33 A: -0.24	-0.54 A: -0.32	-0.65 A: -0.37
V_{th} [V]	0.34 A: 0.48	0.14 A: 0.42	0.06 A: 0.35
EOT [nm]	6.60 A: 6.48	7.76 A: 7.76	8.80 A: 8.70
D_{it} $\times 10^{12}$ $[eV^{-1}\,cm^{-2}]$	$[1.52 \div 2.15]$ A: $[1.76 \div 2.74]$	$[1.84 \div 2]$ A: $[1.14 \div 2]$	$[2.01 \div 2.76]$ A: $[1.25 \div 1.66]$
N_{bt} $\times 10^{10}$ $[cm^{-2}]$	3.26 A: 3.28	2.78 A: 2.78	2.44 A: 2.47

Table 5.2: TiN results

TiN			
$\Phi_{m,eff}$ [eV]		4.76 A: 5.34	
N_{eff} $\times 10^{12}$ $[cm^{-2}]$		0.99 A: 3.8	
	12 nm	16 nm	20 nm
V_{FB} [V]	0.1 A: 0.49	-0.004 A: 0.14	$\simeq 0$ A: 0.09
V_{th} [V]	0.78 A: 1.14	0.67 A: 0.85	0.70 A: 0.78
EOT [nm]	6.30 A: 6.52	7.66 A: 7.90	8.73 A: 8.87
D_{it} $\times 10^{12}$ $[eV^{-1}\,cm^{-2}]$	$[1.84 \div 2.3]$ A: $[2.23 \div 4.85]$	$[1.18 \div 1.40]$ A: $[1.88 \div 2.48]$	$[0.90 \div 1.5]$ A: $[1.47 \div 2.74]$
N_{bt} $\times 10^{10}$ $[cm^{-2}]$	3.42 A: 3.30	2.81 A: 2.73	2.47 A: 2.43

Table 5.3: W results

W			
$\Phi_{m,eff}$ [eV]		4.50 A: 4.63	
N_{eff} $\times 10^{12}$ $[cm^{-2}]$		0.81 A: 1.74	
	12 nm	16 nm	20 nm
V_{FB} [V]	-0.15 A: -0.09	-0.23 A: -0.24	-0.24 A: -0.28
V_{th} [V]	0.48 A: 0.59	0.43 A: 0.45	0.43 A: 0.42
EOT [nm]	6.54 A: 6.59	8.09 A: 7.98	9.01 A: 8.98
D_{it} $\times 10^{12}$ $[eV^{-1}\,cm^{-2}]$	$[1.40 \div 1.89]$ A: $[1.95 \div 2.13]$	$[1.28 \div 1.81]$ A: $[1.25 \div 1.58]$	$[1.23 \div 2.06]$ A: $[1.37 \div 2.15]$
N_{bt} $\times 10^{10}$ $[cm^{-2}]$	3.29 A: 3.27	2.66 A: 2.70	2.39 A: 2.39

5.1.7 Low temperature measurements

The low temperature measurements were carried out inside a vacuum chamber (PMC150) properly connected to a tank filled with liquid nitrogen (LN_2). In this way the temperature inside the chamber could reach $\simeq 77\ K$. For these measurements the MFIS with Ti+Pt gate metal and 12 nm Si:HfO_2 was loaded in the PMC, since this stack had given the best results.

Only C_{HF} was analyzed in this case. Overall, a lower capacitance was observed in all operation conditions. This outcome is reasonable since at low temperature the freeze-out of dopants occur, hence less free charges are available for the charge screening at the interface. This means that the depletion region must increase to guarantee a charge compensation. The increase of the depletion region causes a reduction of the capacitance.

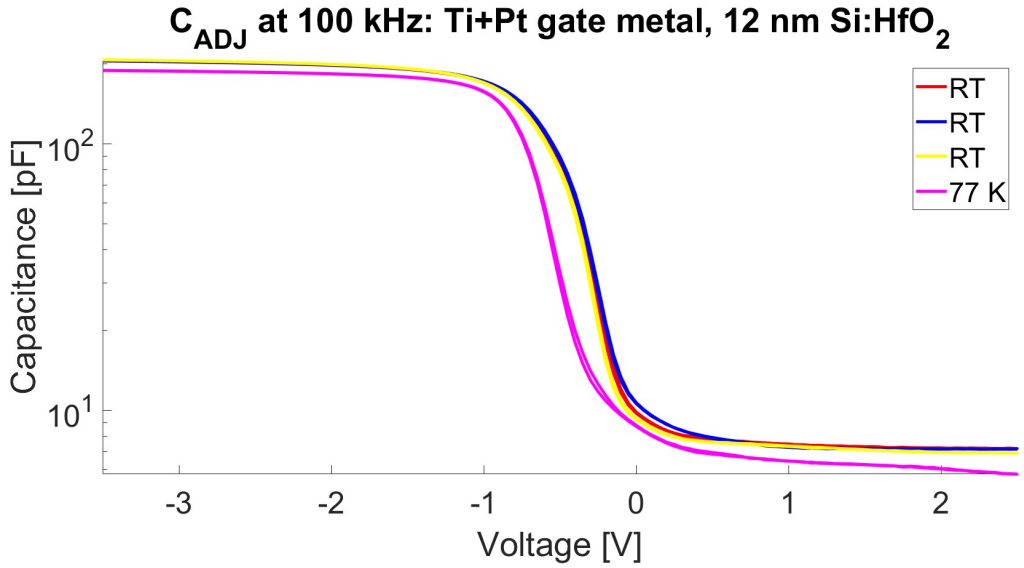

Figure 5.31: C_{HF} RT vs 77 K comparison

Regarding the parallel conductance, a shift on the left was observed as well as an overall reduction of G_p. The reduced parallel conductance can explained by the reduction of thermal vibration, thus the reduction of phonons, which are the main responsible for the resonance in depletion. The shift of the resonance may be justified by the change in the trap time constant: as described in chapter 4, this time constant strongly depends also on the temperature.

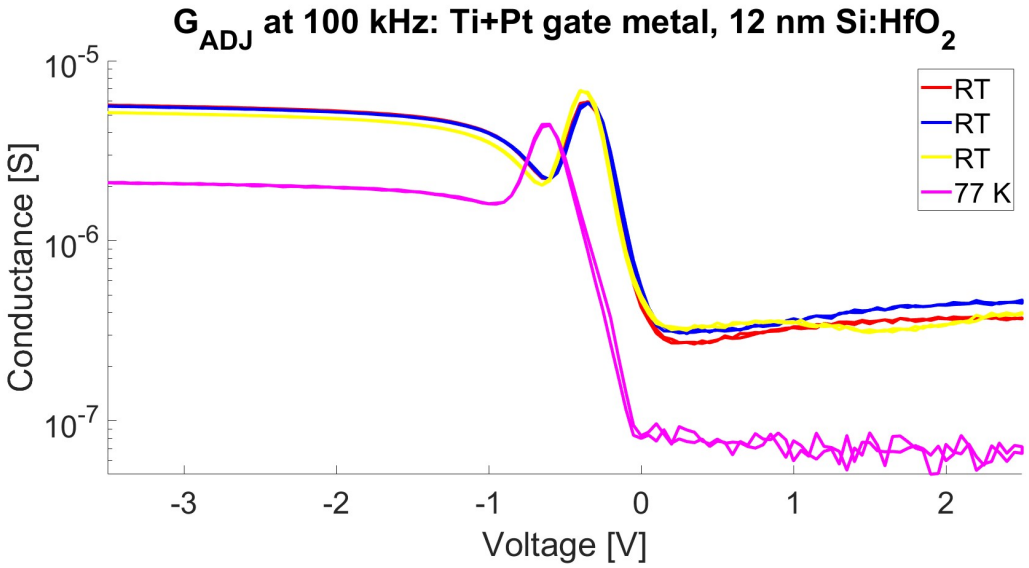

Figure 5.32: G_p RT vs 77 K comparison

5.1.8 New design with thinned SiO_2

In order to favor the ferroelectric character of the MFIS stack, a new design was tested using:

- 1.5 nm of thinned SiO_2 (etched using BHF)
- 12 nm of Si:HfO_2
- 3 nm of Ti+ 30 nm of Pt as gate metal

In this way, an increase of the voltage drop across the hafnia was expected. Moreover, an influence of the $Q_{it,SiO_2/hk}$ interface traps was also hypothesized. A couple of CV curves were extracted at HF (RT and at 77 K) and at LF (only RT).

At HF, the measured capacitance exhibits an evident hysteretic behavior. However, differently from typical ferroelectric loops, the observed hysteresis was clockwise. For this reason, this behavior was associated to the presence of a large amount of traps. At low temperature, the CV curve behaved similarly to the one measured on the standard stack, showing an overall lower capacitance.

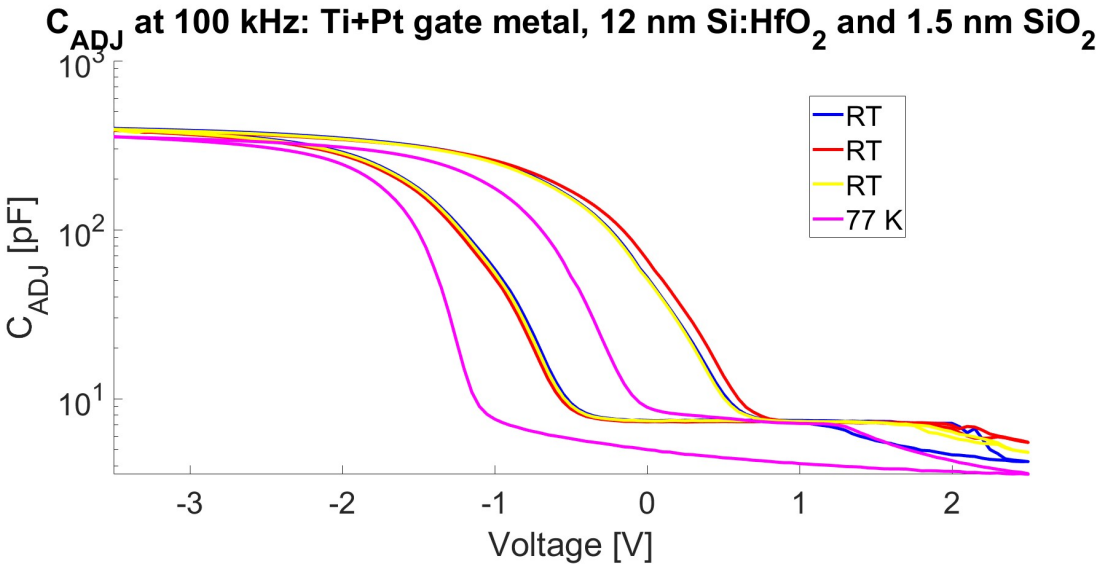

Figure 5.33: C_{HF} of the thinned SiO_2 design

At LF the measured curve exhibit three major differences with respect to the design studied throughout this project:

- in inversion the capacitance does not rise up again to its accumulation value. This means that the electrons were not able to accumulate inside the channel. Three main reasons were hypothesized: 1) formation of a native SiO_2 layer at the Si surface due to a permeation of O_2 across the thinned SiO_2. Native oxide may have trapped electrons preventing the channel population; 2) presence of a leaky path for electrons; 3) trapping of electrons inside border traps (less probable)
- the capacitance exhibits an hysteresis. However the nature of this hysteresis was considered ambiguous and probably still caused by traps rather than ferroelectric domains
- the capacitance in accumulation is $\simeq 550\ pF$, that is higher than the one measured in the previous design. This is of course due to the smaller thickness of the gate oxide

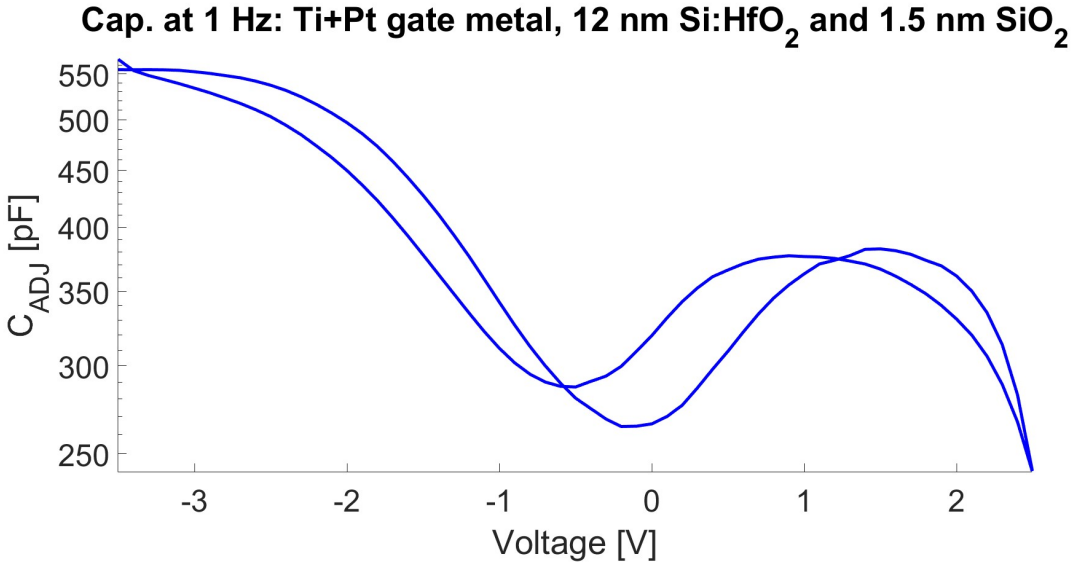

Figure 5.34: C_{LF} of the thinned SiO_2 design

5.2 MFM results and discussion

5.2.1 PE and IV loops

The measurements on the MFM devices provided a charge-voltage loop. In order to obtain a PE curve, the charge was divided by the area of the capacitor ($200\ \mu m \times 200 \mu m$) and the voltage was divided by the thickness of the hafnia (12 nm). From the fully opened PE loops, two figures of merits were extracted: the remnant polarization P_r and

the coercive field E_c. These values were directly read on the PE curve after a proper centering. The P_r was found to be $\simeq$ 12 $\mu C/cm^2$ while the E_c was $\simeq$ 1 MV/cm.

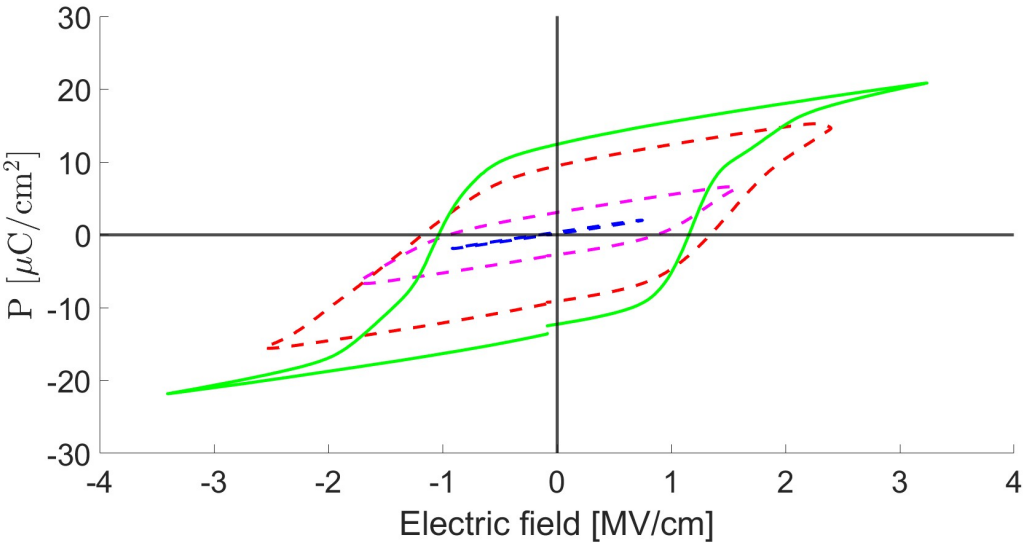

Figure 5.35: PE curve at RT

Regarding the IV curve, this exhibited peaks around E_c due to the contribution of the switching current. The second bump can be associated to other domains switching at higher fields.

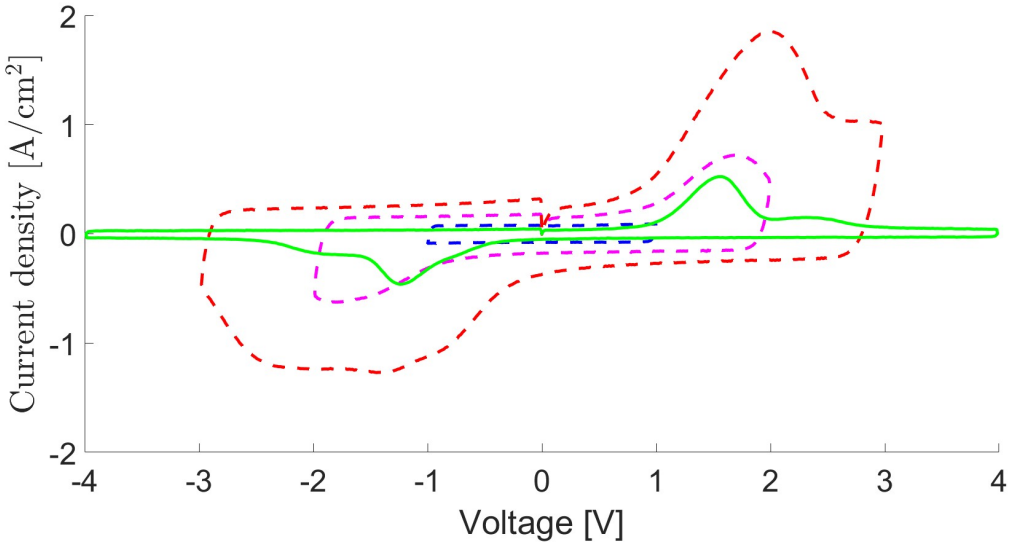

Figure 5.36: IV curve at RT

5.2.2 CV curves

From the CV curves, the baseline and the maximum capacitance were extracted at 10 kHz and 100 kHz. Based on these quantities, the capacitance tunability was calculated. This behavior is confirmed by the following paper [99] and is due to ferroelectric domains responding to lower frequencies.

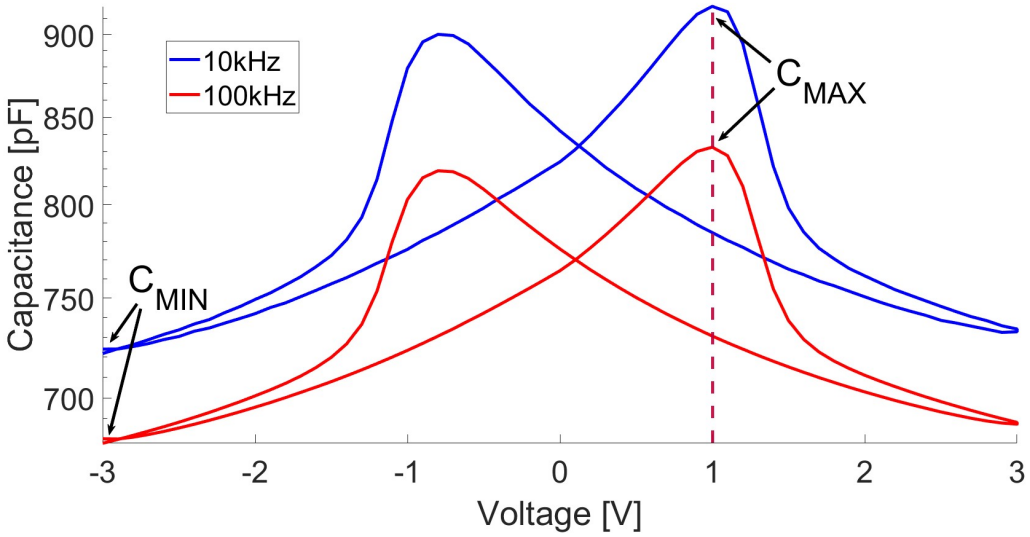

Figure 5.37: CV curve at RT

$$C_{MAX,\,10\,kHz} \simeq 920\ pF$$

$$C_{MIN,\,10\,kHz} \simeq 720\ pF$$

$$tun_{(10kHz)} = \frac{C_{MAX} - C_{MIN}}{C_{MIN}} \simeq 27\%$$

$$C_{MAX,\,100\,kHz} \simeq 830\ pF$$

$$C_{MIN,\,100\,kHz} \simeq 680\ pF$$

$$tun_{(100kHz)} = \frac{C_{MAX} - C_{MIN}}{C_{MIN}} \simeq 22\%$$

5.2.3 Low temperature measurements

Afterwards, the capacitors were tested in the PMC at 77 K. The result was a reduction in terms of P_r and capacitance. The extracted P_r was $\simeq 10\ \mu C/cm^2$ while the coercive

voltage was still $\simeq 1\ MV/cm$. The reduction of capacitance and P_r at low temperature can be explained by the freezing of ferroelectric domains [100].

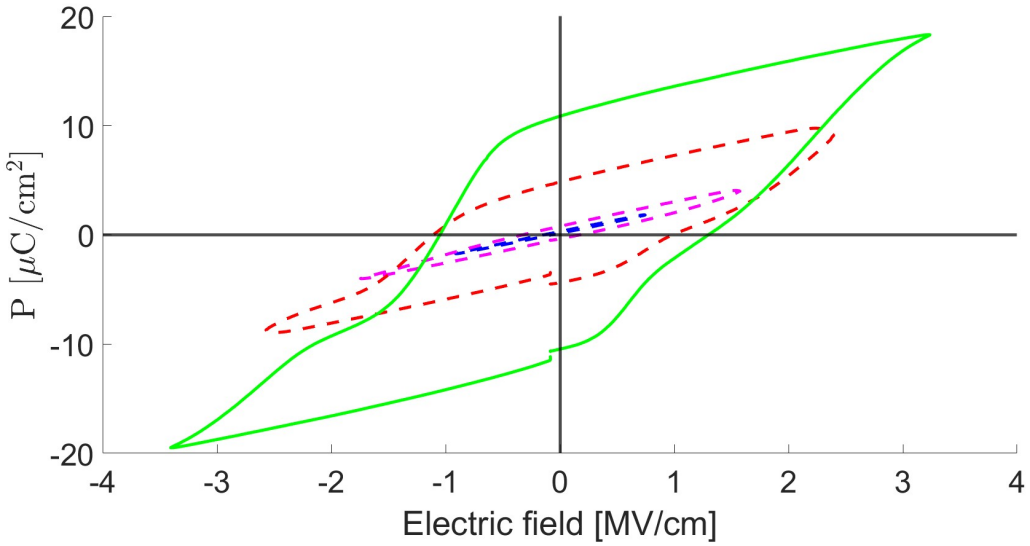

Figure 5.38: PE curve at 77 K

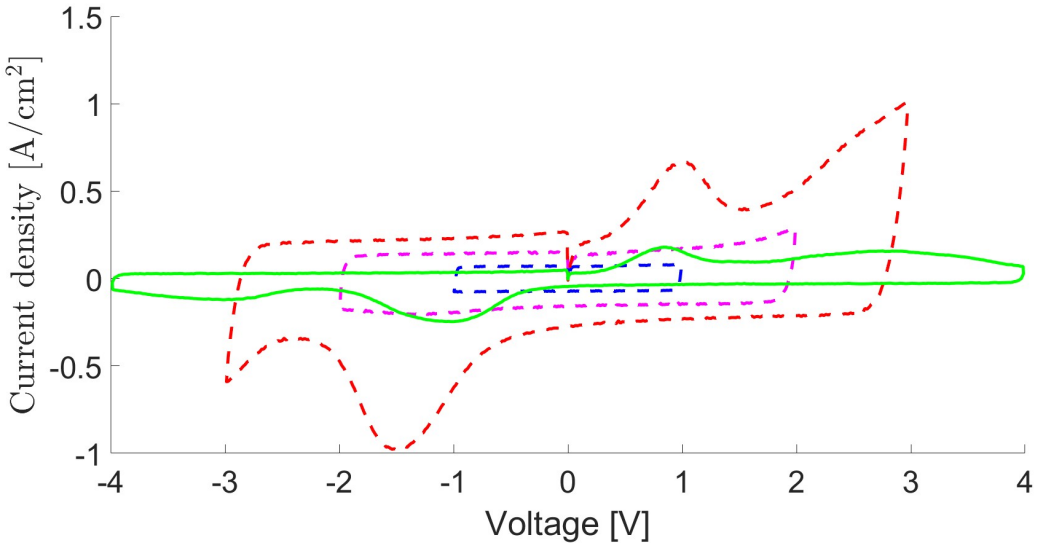

Figure 5.39: IV curve at 77 K

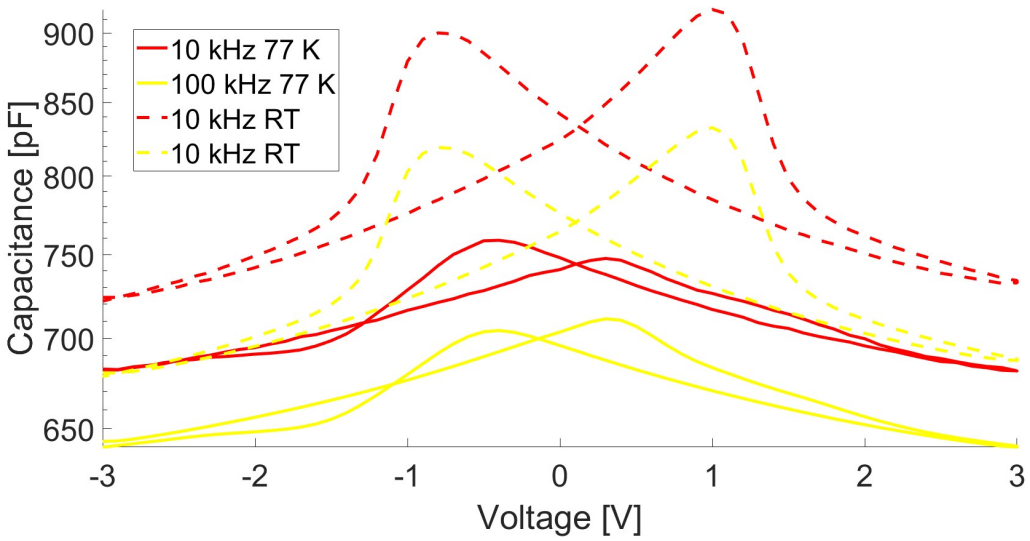

Figure 5.40: CV curve at RT vs 77 K

$$C_{MAX,\,10\,kHz} \simeq 760\ pF$$

$$C_{MIN,\,10\,kHz} \simeq 680\ pF$$

$$tun_{(10kHz)} = \frac{C_{MAX} - C_{MIN}}{C_{MIN}} \simeq 12\%$$

$$C_{MAX,\,100\,kHz} \simeq 710\ pF$$

$$C_{MIN,\,100\,kHz} \simeq 640\ pF$$

$$tun_{(100kHz)} = \frac{C_{MAX} - C_{MIN}}{C_{MIN}} \simeq 11\%$$

Chapter 6

TCAD Sentaurus simulations

The aim of TCAD simulations was to predict the outcome of an implantation process on an SOI substrate. In particular, two main requirements had to be satisfied:

- no penetration of P ions had to occur inside the BOX
- a sufficiently high doping level ($> 10^{20} cm^{-3}$) had to be ensured at few nm from the surface

In order to meet both requirements, many combinations of oxide mask thickness, energy, dose as well as tilting angle were simulated. The structure to implant had the following layout:

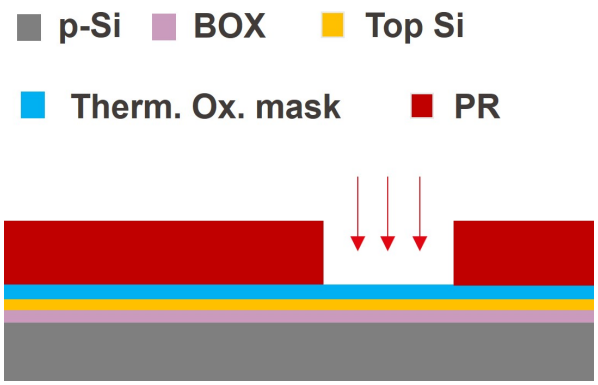

Figure 6.1: Layout of SOI to implant

The fixed parameters were the BOX thickness = 200 nm, the TopSi thickness = 70 nm and the PR thickness = 100 nm. Instead, the variables were the following:

- oxide mask thickness = {5, 10} nm
- energy = {0.9, 1, 1.1, 1.2, 1.3} keV
- dose = $\{10^{15}, 4 \times 10^{15}, 7 \times 10^{15}, 10^{16}\}$ ions/cm^2
- tilting {0, 7}°

Regarding the first variable, the choice of an oxide mask of 10 nm was almost immediately discarded because most of the ions ended trapped inside the thermal oxide. An oxide mask of 5 nm was therefore used for all simulations. Moreover, the tilting angle of 0° and 7° provided very similar results and therefore no tilting was selected.
For an atomistic simulation of the ion implantation a Monte Carlo model was initialized. Moreover, since the real implantation had to be carried out with a PIII (plasma-immersion ion implantation), a specific model for simulating the plasma energy distribution was selected, i.e. the Burenkov model. The mesh and the structure were subsequently defined. In particular, a very fine mesh was adopted at the TopSi surface. The growth of the thermal oxide mask was simulated by depositing SiO_2 (after a proper definition of its density so that it matched that of the thermal oxide i.e. 2.2 g/cm^3) over a TopSi whose thickness value was actually set to 70 $nm - 0.44 \times 5$ nm. After depositing the PR mask and after the Phosphorus implantation, a diffusion was performed. This process consisted of different ramps from 25 °C to 900 °C in N_2 atmosphere.

```
diffuse temperature = 25<C> time = 10.0<s> N2 ramprate = 27<C/s>
diffuse temperature = 300<C> time = 15.0<s> N2
diffuse temperature = 300<C> time = 10.0<s> N2 ramprate = 20<C/s>
diffuse temperature = 500<C> time = 30.0<s> N2
diffuse temperature = 500<C> time = 20<s> N2 ramprate = 20<C/s>
diffuse temperature = 900<C> time = 8.0<s> N2
```

After several tests, the best combination of energy and dose ended up being energy = 1.1 keV and dose = 7×10^{15} ions/cm^2. In this way, $> 10^{20} cm^{-3}$ of P concentration was guaranteed up to 30 nm inside the TopSi.

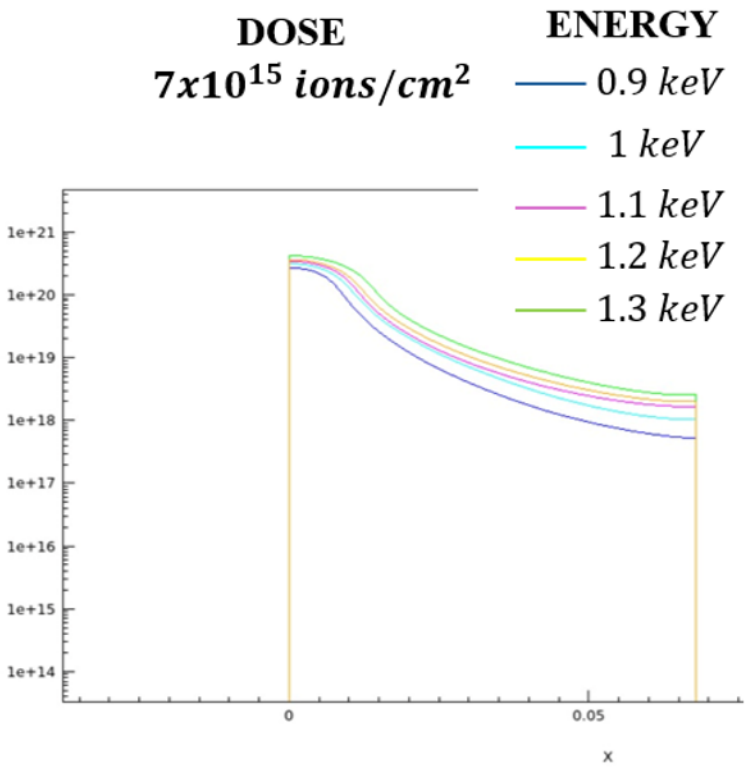

Figure 6.2: Implantation with dose 7×10^{15} ions/cm^2

Chapter 7

Conclusions

The main achievements of this project were: 1) gained practical skills in the use of different machines in the cleanroom through hands-on experience; 2) successful fabrication of two different devices, a simpler MFIS and a more challenging MFM structure; 3) investigation of traps, especially for a deeper understanding of MFIS electrical behavior; 4) study of the ferroelectric nature of the Si-doped hafnia thin films, especially through MFM capacitors; 5) testing of the fabricated structures both at RT and low temperature; 6) active involvement in the hosting laboratory, through the simulations of an ion implantation for an SOI subtrate.
In conclusion, possible optimizations for the MFIS and MFM devices are suggested. In particular, a resistor could be connected to the MFIS with the thinned SiO_2, in order to verify no leakage occurs in inversion. The device could be also subject to pulsed illumination to favor the build-up of electrons in the channel. For the MFM, a different dopant material, such as Zirconium, may be used in order to increase the value of P_r.

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