Politecnico di Torino

Master's Degree Thesis

Design and prototyping of a power amplifier for an optimum trade-off of efficiency and linearity

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Summary

Over the past few decades, with the rapid development of communication technology, the power amplifier, which is the final stage of the transmission chain, has played a crucial role in the wireless communication system. Nowadays, with the fifth-generation (5G) communication standard, the communication system is required to be compact and cost-effective. The use of power amplifiers in high-frequency bands, such as millimeter waves, which allow for wider channel bandwidths, has gained significant attention in both industrial and academic communities. At the same time, research and applications of the power amplifier in low-frequency bands also attract much interest. To achieve higher data rates and minimize losses, the power amplifier operating in the low-frequency regime is typically required to maintain high efficiency and linearity over wide bandwidths.

The proposed thesis presents the design, assembly, and characterization of a single-stage Class-AB microwave power amplifier around 2.6 GHz. The amplifier design strategy focuses on the optimum trade-off of efficiency and linearity at the operating frequency, and it satisfies the requirements of the "High Efficiency Power Amplifier" student competition of the major conference in the Radio Frequency field, the International Microwave Symposium. The design mainly needs to achieve three requirements: gain, output power, and third-order intermodulation products (IMD3). The main challenge is maintaining the trade-off between efficiency and linearity. In terms of linearity, the IMD3 should be below -30 dBc in a two-tone linearity measurement with 20 MHz tone spacing. Besides, the designer needs to boost as much as possible the power-added efficiency, which is the main figure of merit in the competition.

The final design simulation can achieve a power-added efficiency of 57% at maximum power and of 42% at the minimum required linearity. These results have satisfied the requirements of the competition in simulation, but unfortunately, the final prototype could not be manufactured before the competition date. The future work will focus on the measurements, verification, and tuning of the performance of the circuit.

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1 Introduction

1.1 Overview

In recent decades, with the rapid development of communication technology, the power amplifier, which is the final stage of the transmission chain, has played a crucial role in the wireless communication system [1], [2]. The number of devices connected to the Internet has increased significantly due to communication devices, such as smartphones, tablets, and computers, leading to a growing demand for higher data throughput [3]–[5]. The high data rate capabilities of fifth-generation (5G) communication systems offer an effective solution to address the growing demand and challenges posed by the explosive increase in network capacity. In addition to research efforts focused on millimeter wave (FR2) bands, the sub-6 GHz frequency range (FR1) has also attracted substantial interest from both academia and industry due to its favorable characteristics [4], including lower propagation loss, wider coverage, and suitability for large-scale deployment. In the FR1 band, power amplifiers (PAs) are typically required to maintain high efficiency and linearity across wide bandwidths in order to reduce power loss and support higher data rates [6], [7].

1.2 Thesis Goal

In this proposed thesis, the work aims to design a power amplifier targeting the FR1 frequency band, fabricate and characterize its performance through PCB prototyping and measurement, and ultimately submit the design to the High-Efficiency Power Amplifier (HEPA) Student Design Competition (SDC).

The PA must produce an output power of at least 4 watts, but no more than 40 watts at a single-carrier drive with input power not higher than 24 dBm, and maintain the highest inter-modulation product below -30 dBc in a two-tone linearity measurement with 20 MHz tone spacing. In such a framework, the challenges and restrictions of competition design necessitate compromises between efficiency and linearity, while maintaining sufficient output power.

In previous award-winning design cases from the competition, the Doherty power amplifier (DPA) architecture was commonly employed to meet performance requirements and achieve favorable results. Instead, inspired by the 2016 and 2022 competition entries, a single-stage Class-AB amplifier topology was selected [8], [9]. This topology extends the linearity by fully exploiting the ”sweet spots”. The term “sweet spots” as used throughout this article refers to some specific operating condition values

(i.e., class-AB gate bias values) that are found to improve the linearity of the PA's power transfer characteristic. Compared to DPA structures, the Class-AB single-stage design is structurally simpler and easier to implement within the limited time available.

The work of this thesis is to design, fabricate, and assemble a single-stage Class-AB power amplifier, which has a center frequency around 2.6 GHz. The target of the design is to achieve the requirements of the competition.

In the design phase, the strategy first focuses on checking the DC characteristics and stability, then finding the optimum load and source terminations in base-band, fundamental, and 2nd-harmonic frequencies in the Advanced Design System (ADS) CAD simulation software. In the second stage, the main work is designing and optimizing the matching networks and biasing networks based on optimum load and source terminations. Finally, evaluate the circuit in the electromagnetic environment and measure the practical circuit to verify the performance.

The final practical hybrid circuit will be presented on the Printed Circuit Board (PCB). The real-time vector test bench in the laboratory will be adopted to experimentally characterize the manufactured PA demonstrator.

2 Power Amplifier theory

2.1 The Power Amplifier in Wireless Communication Systems

The PA is an essential component, playing a key role in the realization of many microwave and millimeter-wave systems. PA applications span a broad range of areas, including telecommunications, radar, electronic warfare, heating, and medical microwave imaging. However, this thesis primarily focuses on its application in a wireless communication system.

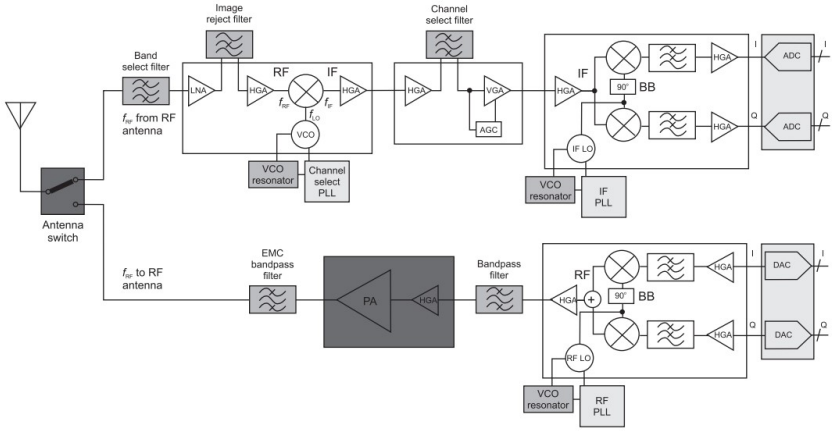

Figure 2.1: Transceiver architecture [1].

In Figure. 2.1, the whole structure of the transceiver, the PA is the final stage in the transmitter chain before the antenna. Its primary function is to amplify the modulated electrical signal, which carries the information, to a sufficient power level for effective radiation through the antenna. Then, the antenna transfers the signal into an electromagnetic waveform towards the receiver [10]. As a critical component, the power amplifier (PA) has a significant impact on overall system power consumption [2]. Consequently, increasing demands are being placed on the power conversion efficiency of PA.

2.2 Main Figures of Merit of Power Amplifier

Figure. 2.2 shows a typical single-stage circuit for a power amplifier, as an active and crucial device in a wireless communication system. Its function is to convert the DC signal

and low-level RF signal into a high-level RF signal. The purpose of RF and microwave power amplifiers is to obtain, rather than the maximum power gain, the maximum output power compatible with a given device, with acceptable efficiency and linearity [1], [2].

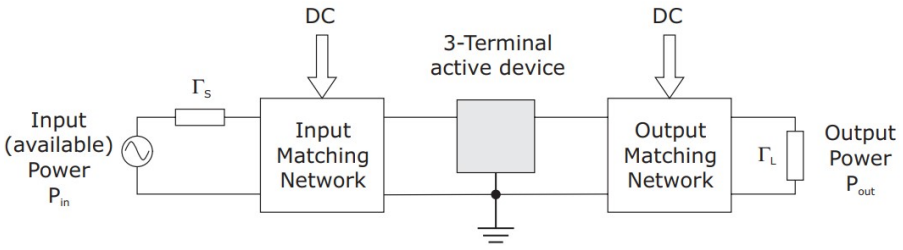

Figure 2.2: Power Amplifier[2].

The main figures of merit of PA are the gain and efficiency, which refers to the continuous wave (CW) single-tone simulation. Other significant merits such as linearity can be evaluated by the two-tone simulation.

The gain of a power amplifier primarily consists of the operational gain G_{op} and the transducer gain G_{tr}.

The transducer gain G_{tr} is defined as,

$$G_{tr} = \frac{P_{out}(f_0)}{P_{in,av}(f_0)}$$

where the $P_{in,av}$ is the input available power, and the P_{out} is the output power on the load. The operational gain G_{op} is defined as,

$$G_{op} = \frac{P_{out}(f_0)}{P_{in}(f_0)}.$$

where P_{in} is the power entering the input port of the active device (i.e., transistor).

The efficiency is the ratio between the output power at fundamental $P_{out}(f_0)$ and the DC power required from the DC power supply P_{DC}:

$$\eta = \frac{P_{out}(f_0)}{P_{DC}}.$$

Another important figures of merit is related to the efficiency of the PA is the power-added-efficiency (PAE), which describes the effective RF power converts from the DC source, where the effective RF power here refers to the difference between $P_{in,f0}$ and

$P_{out,f0}$, the equation is presented following:

$$PAE = \frac{P_{out}(f_0) - P_{in}(f_0)}{P_{DC}} = \eta(1 - \frac{1}{G_{op}}).$$

The PAE and η get close when the G_{op} is high.

In two-tone simulation, the $P_{in} - P_{out}$ characteristic is shown in Figure. 2.3. In the small signal region, only the P_{out} at fundamental is generated by the PA. With the P_{in} increases, the P_{out} at harmonics increases and $P_{out}(f_0)$ comes into saturate region. As the input signal grows, the gain is compressed. From the Figure 2.3: $P_{in} - P_{out}$ characteristics, we can see the third harmonic intercept point, which can be used as a linearity Figure of Merit since it is the result of an extrapolation from the small-signal [1].

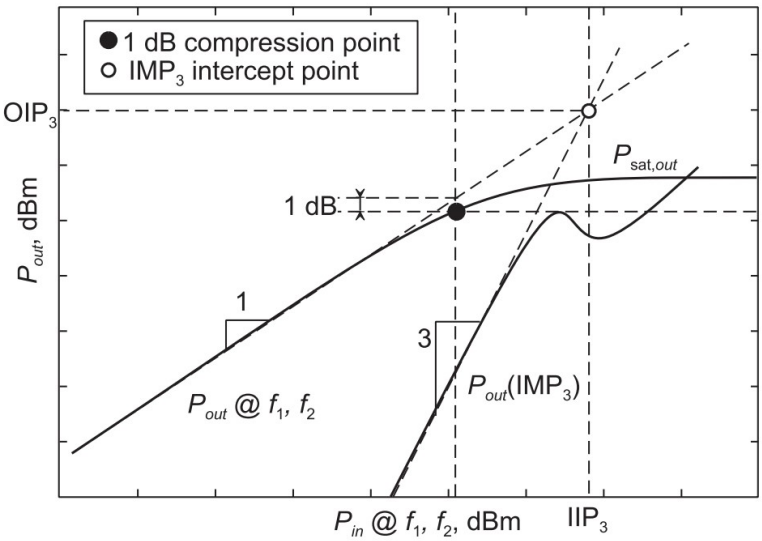

Figure 2.3: Pin-Pout Characteristics[1].

From the power at fundamentals and the IMP_n (with n odd), the n-th-order carrier-to-intermodulation ratio (CIMR_n) is defined as:

$$\mathrm{CIMR}_n = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}}(\mathrm{IMP}_n)}$$

$$\mathrm{CIMR}_n|_{\mathrm{dB}} = P_{\mathrm{out}}|_{\mathrm{dBm}} - P_{\mathrm{out}}(\mathrm{IMP}_n)|_{\mathrm{dBm}},$$

The upper and lower third-order intermodulation products (IMP_3) at frequencies:

$$f_a = 2f_1 - f_2$$

$$f_b = 2f_2 - f_1.$$

Those products are the main cause of distortion.

From Figure. 2.4, we can see the output spectrum of the two-tone simulation and the CIMR merit directly.

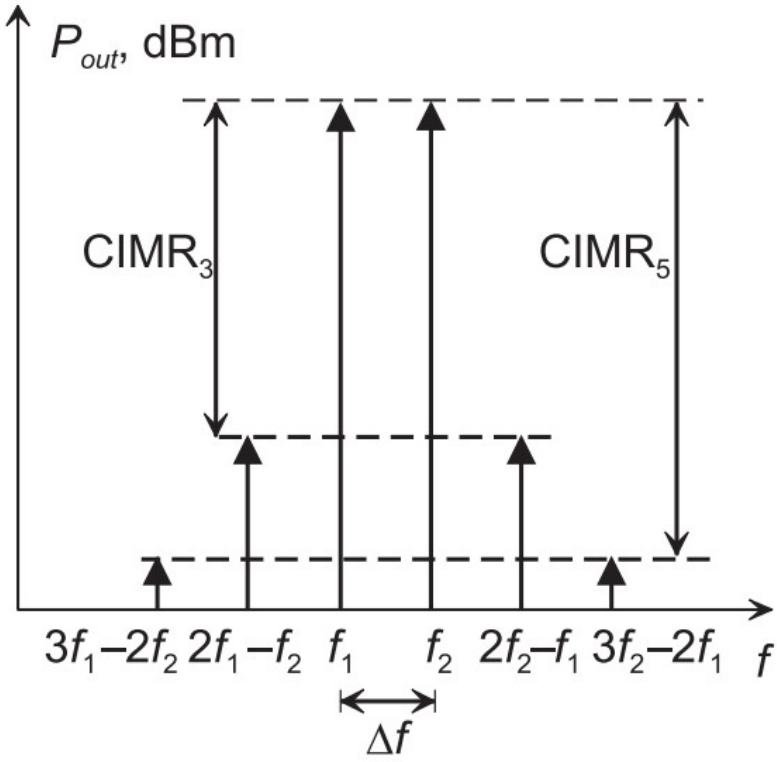

Figure 2.4: Output Spectrum of Two-Tone Simulation[1].

In the modulated signal test, the amplifier input has a continuous spectrum, typically limited to a narrow band around f_0(see Figure. 2.5). The output spectrum will also be continuous, and the generation of odd-order intermodulation products will lead to the so-called spectral regrowth, i.e., the broadening of the input spectrum to the nearby channels, as shown in Figure. 2.5.

Notice that the IMP3 level also affects the main channel and should be regarded as a kind of deterministic noise. The Adjacent Channel Power Ratio (ACPR) is defined as:

$$\mathrm{ACPR}_k = \frac{\int_{\mathrm{MC}} P_{\mathrm{out}}(f)\, df}{\int_{C_k} P_{\mathrm{out}}(f)\, df},$$

where MC is the main channel, C_K the k-th adjacent channel. An example of the shape of the output spectrum is shown in Figure.2.6.

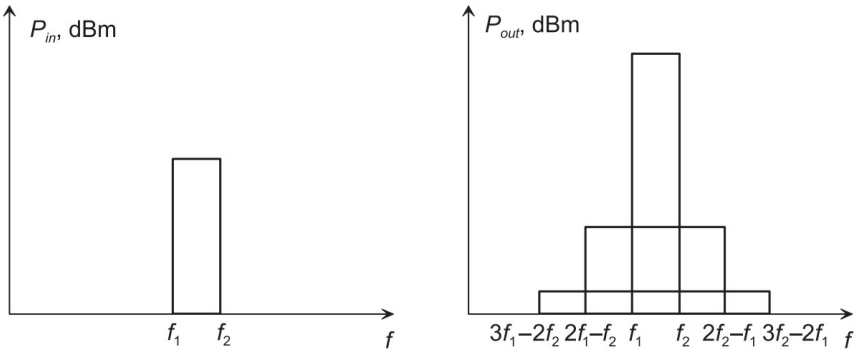

Figure 2.5: Continuous input spectrum(left) and broadening of the input spectrum to the nearby channels(right)[1].

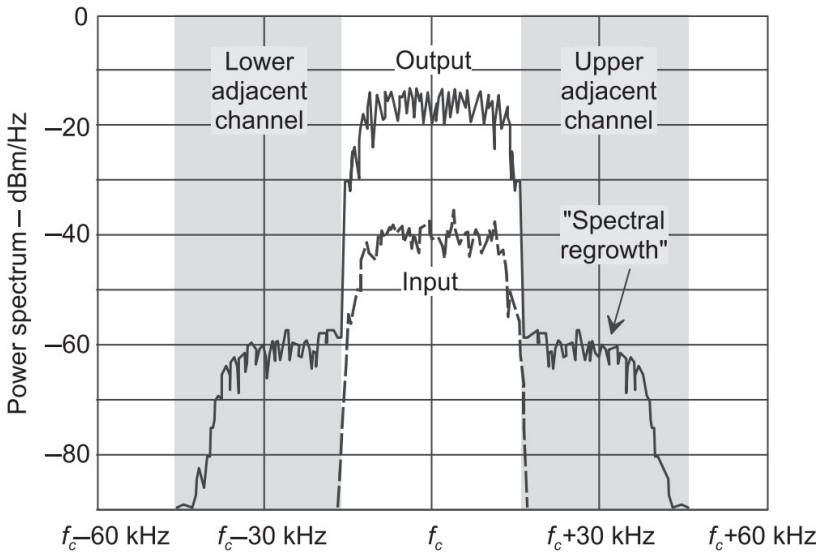

Figure 2.6: Input modulated signal and output power spectrum after amplification, affected by spectral regrowth[1].

2.3 The Classification of Power Amplifiers

PAs are normally classified on the basis of their operating classes. Such a traditional classification, which may seem natural and simple at first glance, may, on the contrary, be ambiguous and misleading. With the term operating class in fact, several different features can be referred to, ranging from the bias point selection (Class A, AB, B or C), to the selection of matching network topologies (Tuned Load, Class F, etc.) or to the operating conditions of the active device (Class E, Class S, etc.) [2].

In order to avoid confusion, in this thesis, the term biasing class (i.e., Class A, AB, B,

or C) will be mainly adopted to define the active device quiescent bias adopted in the design of the PA. Moreover, high-efficiency PAs(i.e., Class E, F) will also be introduced simply.

In fact, the identification of the quiescent bias point may be performed in terms of device output conduction angle (CCA) Φ, i.e., the fraction of the RF signal period where a non-zero current is flowing. Alternatively, it is assumed in terms of the current value as compared to the maximum allowable one, i.e., the ratio between the quiescent output current and its maximum allowable value.

As a consequence, the classification reported in Table 2.1 and graphically depicted in Figure. 2.7 results.

Table 2.1: Classification of PAs in terms of output current conduction angle Φ or biasing point.

Operating Class	Current Conduction Angle CCA (Φ)	Dependence on Drive Level	Bias
A	$\Phi = 2\pi$	No	*Midway between Device Pinch-off and Saturation regions*
AB	$\pi < \Phi < 2\pi$	Yes	*Above Pinch-off*
B	$\Phi = \pi$	No	*Device Pinch-off*
C	$\Phi < \pi$	Yes	*Below Pinch-off*

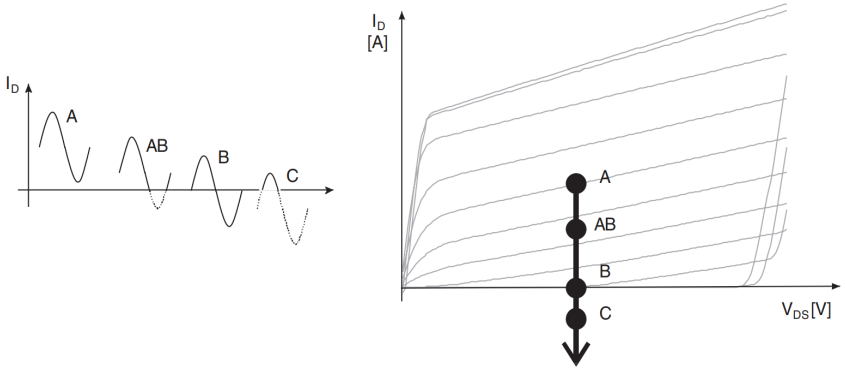

Figure 2.7: Class of operation defined as output current conduction angle (left) or simply by the device quiescent bias point (right)[1].

Figure. 2.8 shows the transcharacteristics and output characteristics of an ideal device. It illustrates the biasing conditions necessary to obtain the different PA classes.

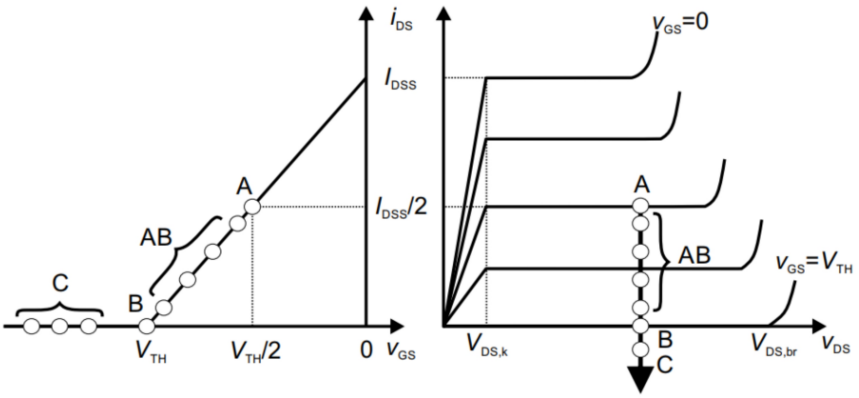

Figure 2.8: Transcharacteristics (left) and output characteristics (right) with bias points of different PA classes [11].

Linear PA: Class-A

In Class-A amplifiers, the minimum total input voltage (including both the input signal and the input voltage DC bias) is always larger than the device threshold voltage. As a consequence, the output current is never zero, and the current waveform is almost sinusoidal. In an n-type compound semiconductor FET, the maximum peak-to-peak input voltage swing is from the (negative) threshold voltage to approximately 0, and the gate bias voltage allowing for the maximum swing is midway between the two extremes. Since the output current is almost sinusoidal, Class-A amplifiers operate with minimal distortion but also with relatively low maximum efficiency. Notice that in a single-tone test, the load voltage is purely sinusoidal, but in a two-tone test, in-band IMPs are also present in the load current.

Nonlinear PAs: Class-AB, B, C

Class-B PA

In Class-B amplifiers, the output voltage is below threshold for exactly half of the period, and the gate bias is at threshold. As a consequence, the output current is (approximately) a half-wave rectified sinusoid. Despite the high nonlinearity of the amplifier, thanks to the tuned load, the load current is almost sinusoidal. Class-B amplifiers exhibit larger distortion and lower gain when compared to class-A, but better efficiency.

Class-AB PA

Class-AB is an intermediate case between Class-A and Class-B, meaning that the

input voltage is below threshold for less than half a period. The load current is a clipped sinusoid and efficiency, gain, and distortion are intermediate between Class-A and B.

Class-C PA

In Class-C amplifiers, the input bias is below threshold, and the output current is different from zero for more than half a period. Class-C exhibits, stronger distortion and lower gain vs. Class-B, but also a larger efficiency. However, 100 percent efficiency is achieved, in the limit, with zero gain; this limits the practical utility of Class-C amplifiers.

Class-E PA

Class-E amplifiers can ideally achieve 100 percent efficiency. It adopts the single-pole switching element and a tuned reactive network is applied between the switch and the load [12], [13]. The high efficiency performance is obtained by only operating the switching device either at points of zero current or zero voltage, which minimizes power lost in the switch. However, to this aim, the zero active device instantaneous dissipation already mentioned is not enough. To maximize efficiency, we also have to deliver to the load no power at the harmonics (remember that only the load fundamental power is relevant for the input-output information transfer) [1], [10].

Class-F PA

Class-F amplifier adopts the harmonic loading technique to boost the efficiency, its biasing condition is the same as that of Class-B amplifier [14], [15]. From the Figure. 2.9, the waveforms of the Class-F power amplifier, the instantaneous power dissipated by the device is zero, and therefore the power from the DC source is completely converted into RF, with 100 percent efficiency.

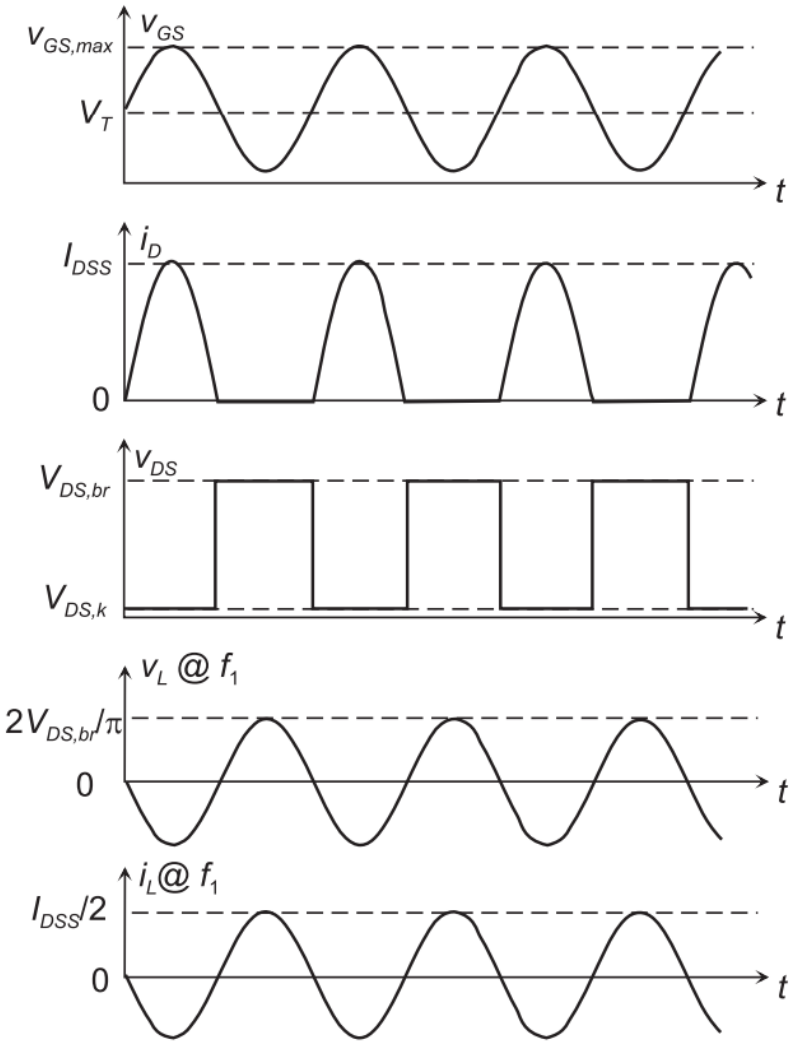

Figure 2.9: Waveforms of Class F PA

3 PA Circuit Design Process

In this design, a high electron mobility transistor (HEMT) of gallium nitride(GaN) is adopted to meet the output power and linearity requirements for achieving high efficiency and relatively linear performance. The selected packaged device is manufactured and commercialized by Wolfspeed Inc[16]. the model code of the device is CG2H40010F.

The DC characteristics and stability of device CG2H40010F are first considered, which are analyzed during the pre-design stage. The following simulations and analyzed chapters are all processed by the CAD tool (Keysight ADS).

3.1 DC Characteristic

In the pre-design stage, it is very important and necessary to evaluate the DC characteristics of the active device–CG2H40010F. Since choosing the biasing point is the first step in designing a power amplifier.

DC characteristics, including output-characteristics and trans-characteristics [1], [2], [17]. The output-characteristics describes the relationship between V_{DS} and I_{DS} for each V_{GS}; the trans-characteristics shows how the I_{DS} curve changes as the V_{GS} varies at a specific V_{DS}.

Figure. 3.1 shows the output-characteristics and trans-characteristics. By sweeping the V_{DS} from 0 V to 160 V and setting the V_{GS} ranges from -4 V to 0.8 V, the output-characteristic(left) is obtained. The trans-characteristics is acquired by sweeping the V_{GS} from -4 V to 0.8 V for each V_{DS} between 0 V to 160 V.

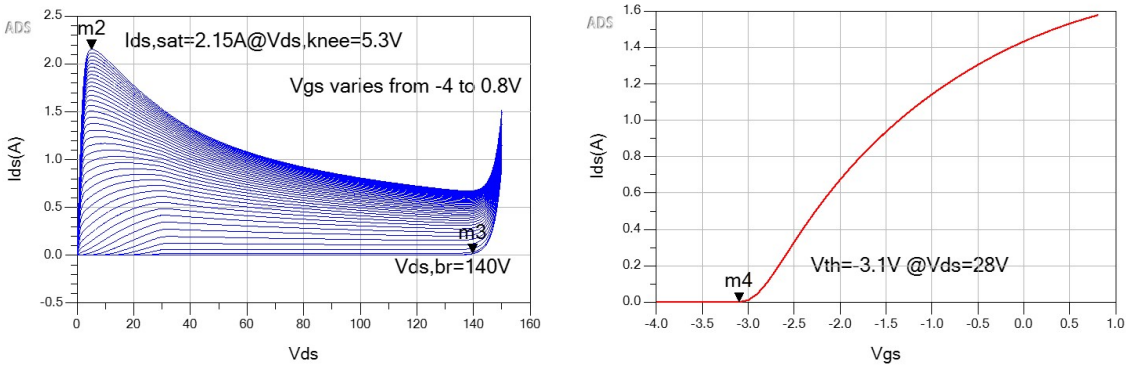

Figure 3.1: DC characteristics of transistor: output-characteristics (left) and trans-characteristics with V_{ds} = 28 V (nominal) (right).

Through the DC characteristics figures, some important design parameters can be obtained. In the output-characteristics, the Knee, breakdown drain-source voltage, and saturated drain-source current of the device could be seen: Knee voltage $V_{DS,knee}$ is 5.3 V,

Breakdown voltage $V_{DS,br}$ is 140 V, Saturated current $I_{DS,sat}$ is 2.15 A. While in the trans-characteristics, the threshold voltage is obtained: Threshold voltage V_{TH} is -3.1 V.

As the plan is to design a Class-AB power amplifier, the biasing point of the device will be chosen according to the DC characteristics figures. So in the end, the chosen V_{GSq} is -2.95 V and V_{DSq} operates at a nominal 28 V by the datasheet of manufacture.

3.2 Stabilization Network

Stabilization of PA is an important design step to avoid in-band and out-band oscillations. If the oscillation exists in the low frequencies, the power amplifier will be saturated [1], [2]. Hence, the stabilization network in the whole PA design is very crucial.

The simulation of stability was processed on the CAD tool ADS, which mainly evaluated the stability condition by the stability factor μ (μ is the one-parameter stability criterion, Edwards and Sinksky proved that a condition on a single parameter is sufficient to assess unconditional stability in 1992 [18]. When μ is greater than 1, which means that the device is in unconditional stability). In simulation, the transistor CG2H40010F was biased in the deep region of Class-AB PA at a frequency of 0 to 20 GHz.

In Figure. 3.2 and Figure. 3.3, the simulation results show the stability analysis in small signal. In low frequencies and above 10 GHz, the device is conditionally stable, while between 3.5 GHz and 10 GHz, the device is unconditionally stable. Maximum Available Gain (MAG) refers to the theoretical maximum gain that a transistor can achieve at a given bias point and frequency, under the condition of unconditional stability.

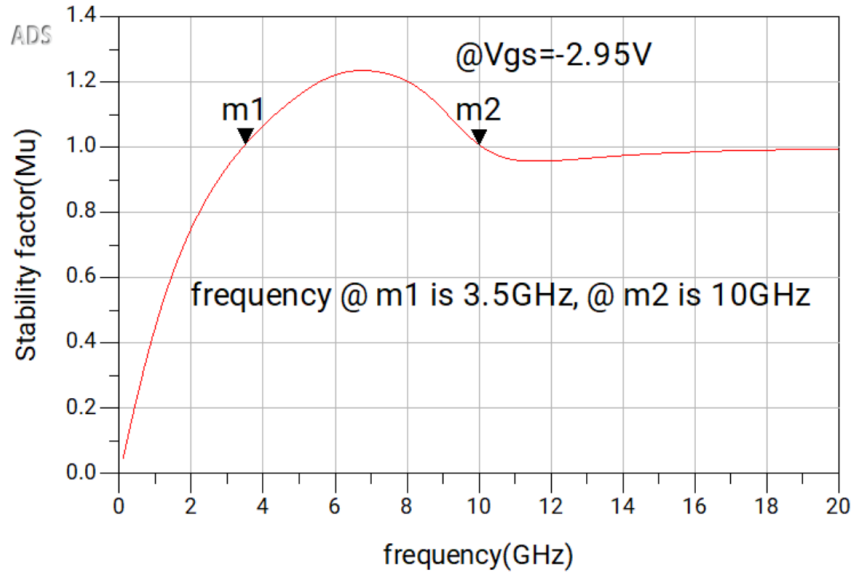

Figure 3.2: Stability factor

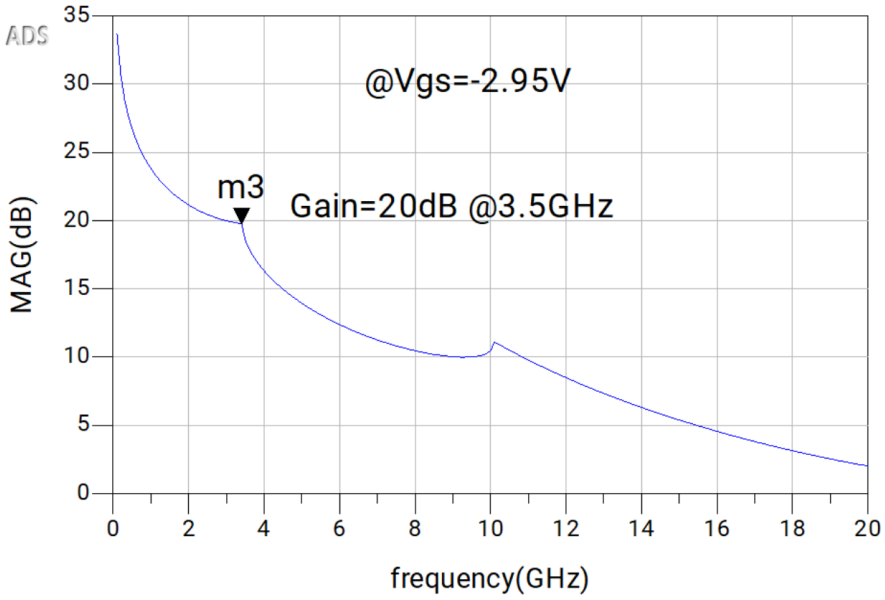

Figure 3.3: Maximum Available Gain(dB)

The classical stabilization network (see Figure. 3.4) is a parallel RC group in series with the gate (RF stabilization) + series and shunt resistors in the biasing lines. The parallel resistance(R_a) provides unconditional stability at low frequency, series resistance (totally or partially resonated out in band by the parallel capacitance) stabilizes the devices in the medium-high frequency range (at low frequency, the value required would

be too high).

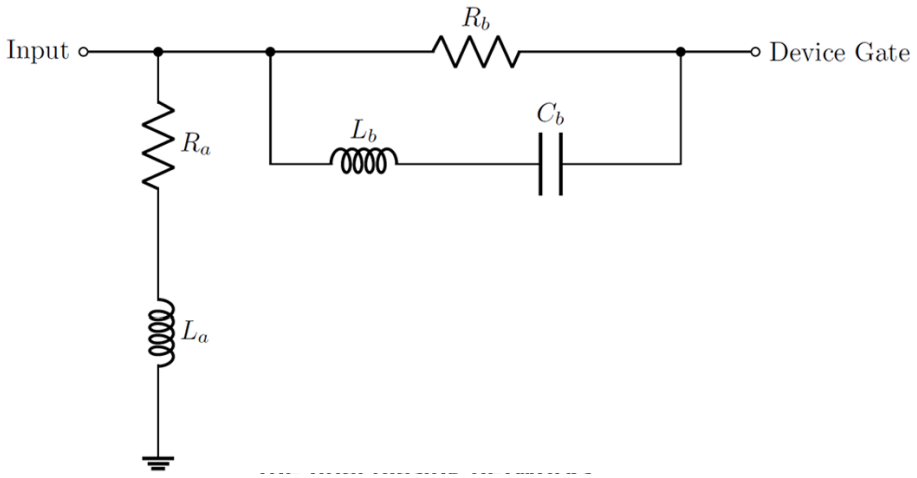

Figure 3.4: Classical stabilization network

The objective is to ensure that the device remains unconditionally stable out-of-band and potentially stable in-band, which in turn enhances the gain of the PA. By adding the stabilization network (see Figure. 3.5) into circuit, the parameters of stabilization network are: Rser = 25 Ω, Cser = 15.5 pF, Rsh = 4 Ω, the Lsh=0.3 nH. And the result is shown in Figure. 3.6.

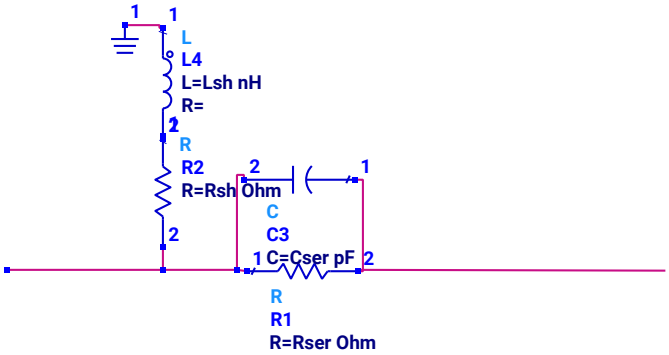

Figure 3.5: Stabilization Network in Circuit

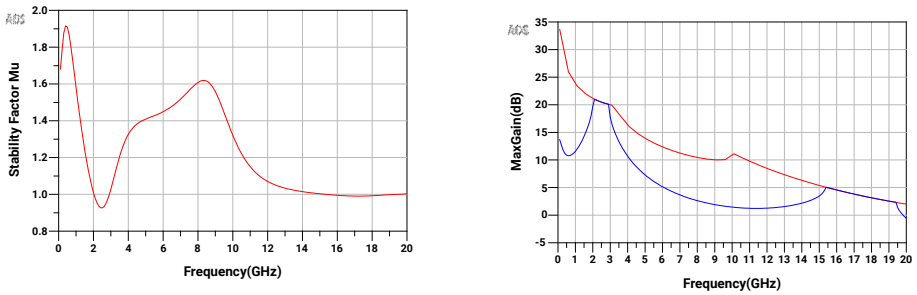

Figure 3.6: Performance with Stabilization Network

In the subsequent section, a practical stabilization network topology is introduced. This topology retains only the RL network, replaces the parallel RC group with microstrip line network, and integrates the biasing and stabilization networks into the matching network. The substitution is motivated by the fact that, although a series RC network is highly effective for stabilization in other designs, it is extremely difficult to reproduce accurately during prototyping. Even small variations can lead to significant differences in input impedance, gain, and efficiency. Therefore, despite acknowledging that stability may become more critical, we take the risk of removing the series RC network in favor of a more reproducible solution.

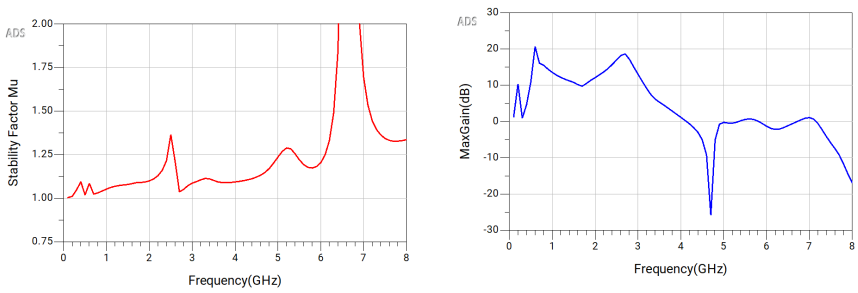

Figure 3.7: Performance with Practical Stabilization Network

From the performance comparison between Figure. 3.6(performance with conventional SN) and Figure. 3.7, it can be observed that after introducing the practical stabilization network, the stability factor μ remains above 1 across the entire frequency range, indicating that the circuit achieves unconditional stability. However, the maximum available gain at the operating frequency of 2.6 GHz decreases from 21 dB to 16 dB.

3.2.1 Practical Biasing Network

In PAs design, the DC biasing network is intentionally engineered to isolate the DC power supply from the RF signal path through appropriate decoupling circuit blocks. This isolation is critical to minimize mutual interference between the DC and RF domains. Such interference primarily manifests in two ways:

- Potential power dissipation or even device damage due to unintended DC current flow into passive components of the RF circuitry
- Unpredictable electrical behavior arising when the RF circuitry is adversely loaded by the DC bias network

Therefore, effective decoupling is essential to ensure both reliable operation and performance integrity of the PA system [1], [19].

The ideal classic biasing network topologies are shown in Figure. 3.8.

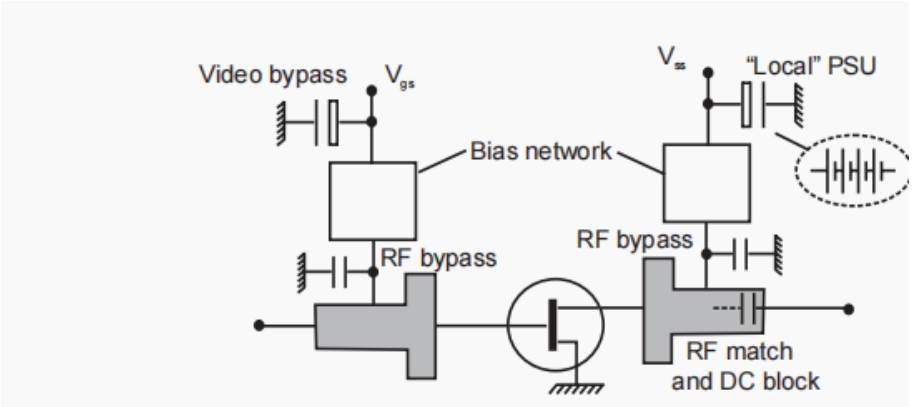

Figure 3.8: PA with Biasing Network

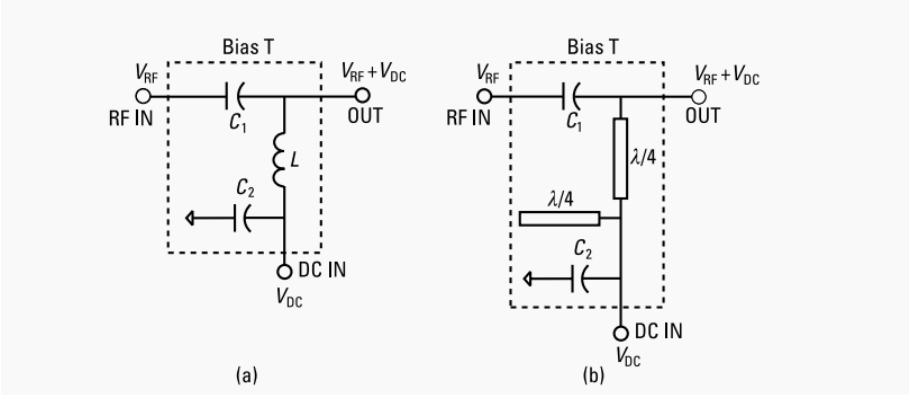

Figure 3.9: Biasing Network Topologies: (a) Lumped elements (b) with transmission line

In practical biasing network design, it is better to embed the bias stubs into the matching networks. The practical applied topology in this design is in Figure. 3.10, which takes the classical stabilization network topology of Figure. 3.9 (b); the biasing circuit functions as a close approximation to an ideal short due to the recursion of numerous pairs of big capacitors and the appropriate length ($\lambda/4$) of microstrip line stub.

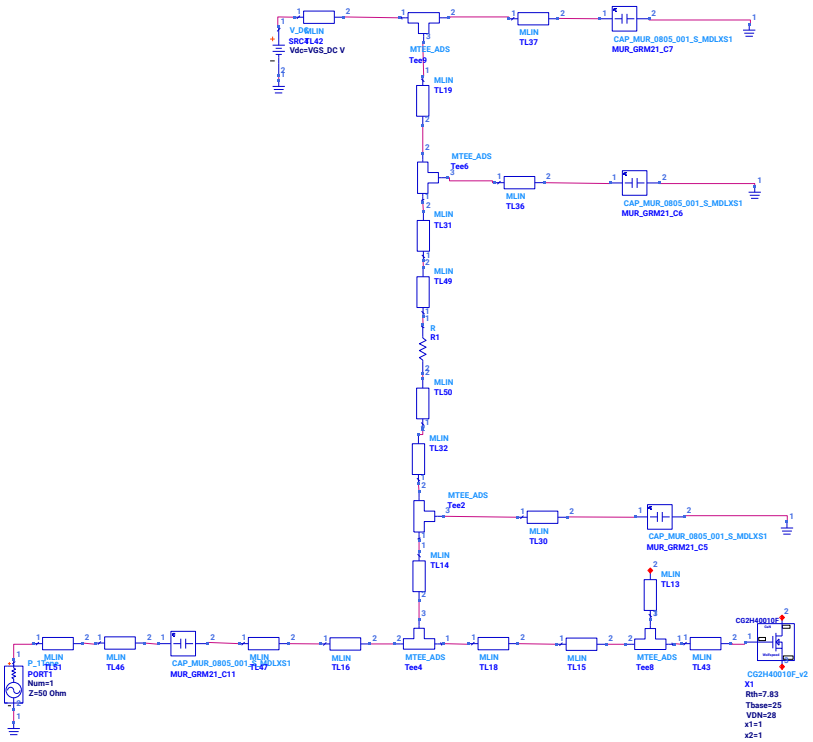

Figure 3.10: Practical Biasing Network

The biasing network is implemented by the microstrip line and fabricated on the material Roger4350B-TanD31. The existing ideal ”short” in the stabilization network is replaced by a biasing block, which presents a high-quality ”short” in practice. Consequently, the stabilization and biasing networks are integrated.

3.3 Optimization for Figures of Merit

In this design section, the work mainly focuses on finding the optimum load and source terminations to satisfy the requirements of the SDC on Keysight ADS. Using the same biasing setting in both CW one-tone and two-tone measurements to achieve the design target.

3.3.1 Optimization for Power and Gain(in one-Tone)

Output power $P_{out,f0}$ and transducer gain G_{tr} are the main figure of merits of PA to evaluate in the one-tone simulation. The optimum source and load terminations will maximize the two figures of merit. Since the output power is closely related to the

transducer gain, finding the source and load terminations that maximize the output power is equivalent to identifying the optimum source and load terminations that yield the maximum transducer gain.

In the PA design, the source/load termination is expressed as the reflection coefficient Γ_S and Γ_L present to the transistor. The design order for the optimization of Γ_S and Γ_L simultaneously is explained by the equation shown below [1], [19],

$$\Gamma_{in} = \frac{S_{11} - \Delta\,\Gamma_L}{1 - S_{22}\,\Gamma_L}$$

as the equation presents, for a two-port network, Γ_L and Γ_{in} are related. Moreover, the maximized P_{out} depends on the match condition between Γ_L and Γ_{in} at the corresponding input power level. Therefore, Γ_L should be primarily determined, enabling the appropriate selection of Γ_G to achieve input matching under specific power conditions.

Load-pull Simulation and Source-pull Simulation

Firstly, considering the load termination, if the source termination is determined prior to considering the load termination, the latter may influence the final outcome of the source termination, thereby affecting the overall circuit performance. Since the parasitic effect exists in the packaged device adopted in this design, the ideal optimum load impedance, which is based on the load-line theory, is not able to compensate for the parasitic parts inside the device, so it would not be selected as the load termination in this design. Instead, the load impedance is searched by the load-pull simulation in Keysight ADS to realize output power maximization.

The load-pull simulation model is introduced to determine which load impedance presents to a device to achieve the power delivered, PAE, IMD3 level and other specifications. Such measurements are available to simulate in Keysight ADS. The intended circuit is measured in the provided load-pull template, with a 50 Ω at source termination under the biasing condition $V_{DSq} = 28V$ and $V_{GSq} = -2.95V$.

The output performance when $P_{in,f0}$ = 24 dBm is shown in Figure. 3.11.

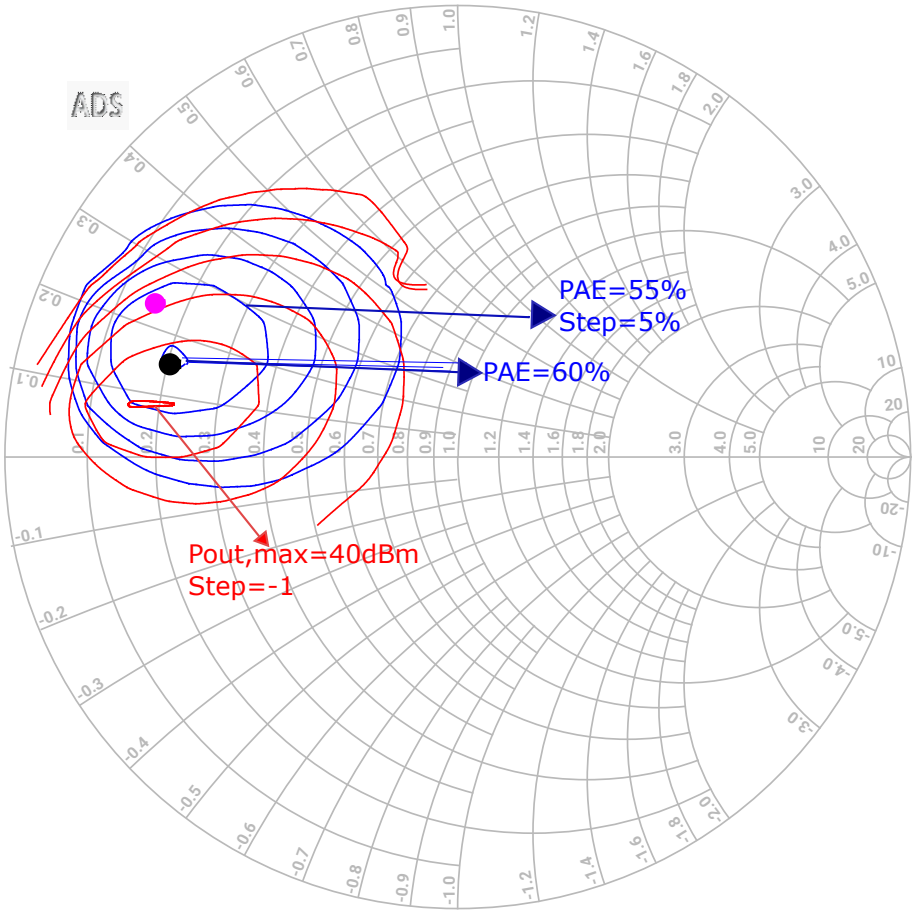

Figure 3.11: Load-pull in 1-tone simulation

Figure. 3.11 shows the contours of the PAE and $P_{out,f0}$ heavily overlap in one part of the Smith Chart, which indicates the PAE would remain at a high level when $P_{out,f0}$ is optimized. In the one-tone simulation, it is anticipated that $P_{out,f0}$ is optimized to 40 dBm, leaving enough margin for P_{out}, the possible loss in a practical PCB. At the same time, the expected PAE result is 55%.

Once the load termination is obtained through load-pull simulation, the temporary result is utilized in a subsequent source-pull simulation to determine the optimum source termination under the corresponding performance condition. The resulting source termination is then fed back into the load-pull simulation again. This iterative process is repeated until the optimal one-tone performance is achieved.

In the final step, $Z_{s,f0}$ is chosen to be (3-0.75*j) Ohm and $Z_{L,f0}$ is selected as (10.8+7.55*j) Ohm in order to maximize $P_{out,f0}$ and PAE. The 1-tone simulation performance is shown in Figure. 3.12, with the single-carrier injection of 24 dBm $P_{in,f0}$, the PAE reaches 64% and obtains the 41 dBm $P_{out,f0}$.

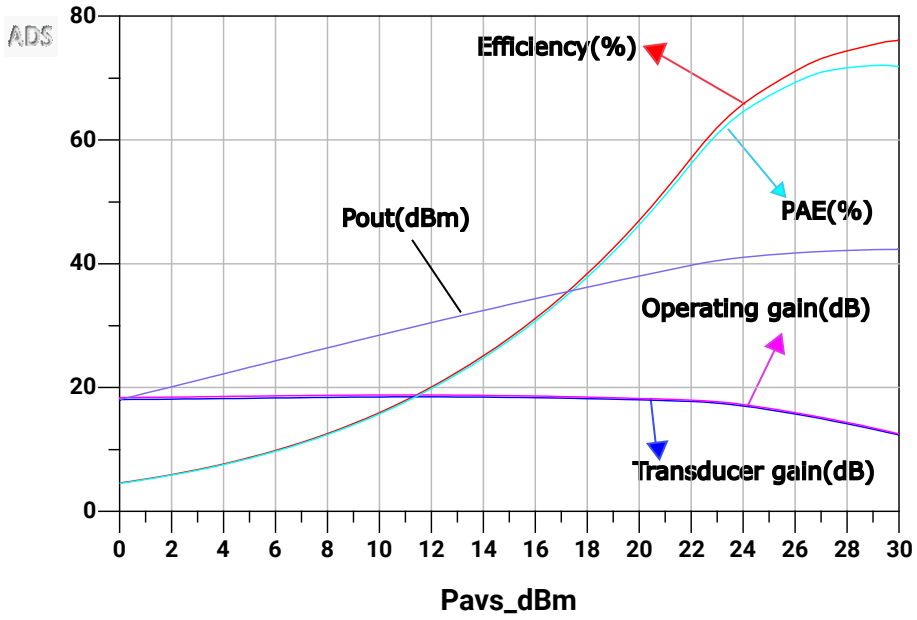

Figure 3.12: one-tone simulation performance after source-pull and load-pull optimization

As the $P_{out,f0}$, PAE, and Gain in one-tone simulation have satisfied the requirements of competition, the next step is to evaluate the IMD3 and PAE in two-tone simulation under the same biasing condition: $V_{DSq} = 28V$ and $V_{GSq} = -2.95V$ as CW simulation setting.

To assess the linearity of PA, IMD3 is an important figure of merit. By using the same source and load terminations, the performance is shown in Figure. 3.13. As the plot presents, the IMD3 is seen to only sustain a high linear level in a restricted and very small signal region. However, it exceeds -30 dBc when the $P_{in,f0}$ starts from 0 dBm and comes to 12 dBm, the PAE reaches 22%.

From the two-tone performance, the IMD3 does not look good and does not satisfy the requirements of SDC. Therefore, the IMD3 should be optimized for maintaining below -30 dBc until the PA is injected with a maximum of 24 dBm $P_{in,f0}$. Meanwhile, the PA should be optimized for trading-off between PAE, IMD3, and $P_{out,f0}$.

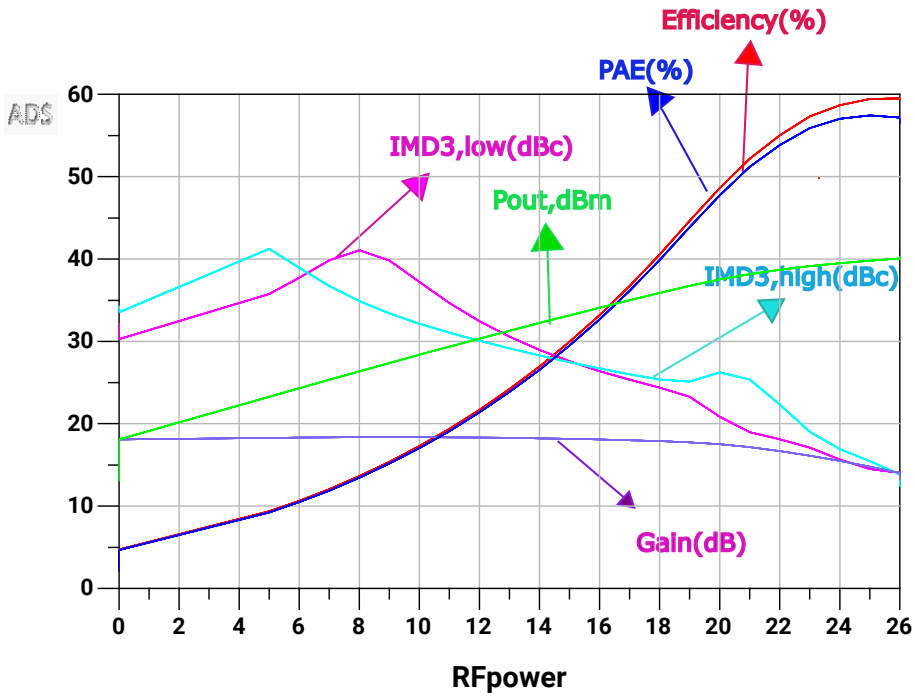

Figure 3.13: two-tone performance of PA after optimization

3.3.2 Optimization for IMD3 in two-tone simulation

There are several approaches to improve IMD3 performance.

- Bias point adjustment represents the most straightforward method. Altering the bias point modifies the transistor's operating region, thereby changing the power amplifier's (PA's) linearity characteristics. [1], [2]

- Modifying the source and load terminations at baseband offers another viable strategy. This technique enables baseband control to influence IMD3 behavior, as suggested in prior studies. [2]

- Adjusting the matching conditions can also affect linearity performance, as impedance mismatches or optimizations directly influence the amplifier's nonlinear response. [20]

At the same time, it is very important and necessary to verify the $P_{out,f0}$ in one-tone simulation again to confirm if it still gives enough margin to the requirement after modification, since each modification will more or less have an impact on the P_{out}.

Adjustment of the Biasing point

Since the $V_{DSq} = 28V$ is specified by the transistor manufacturer and cannot be changed in the design, the only remaining adjustable bias point is V_{GSq}. Linearity FOM changes with V_{GSq} changes from -2.85 to -3.05 V, which is shown in Figure. 3.14. When $V_{GSq} = -3.05V$, the IMD3 tends to flatten out, and as the input power increases, the slope declines more slowly than it did in the previous biasing point. However, IMD3 reaches the -30 dBc earlier when V_{GSq} decreases; in meanwhile, the PAE gets little growth as V_{GSq} increases, but not too much.

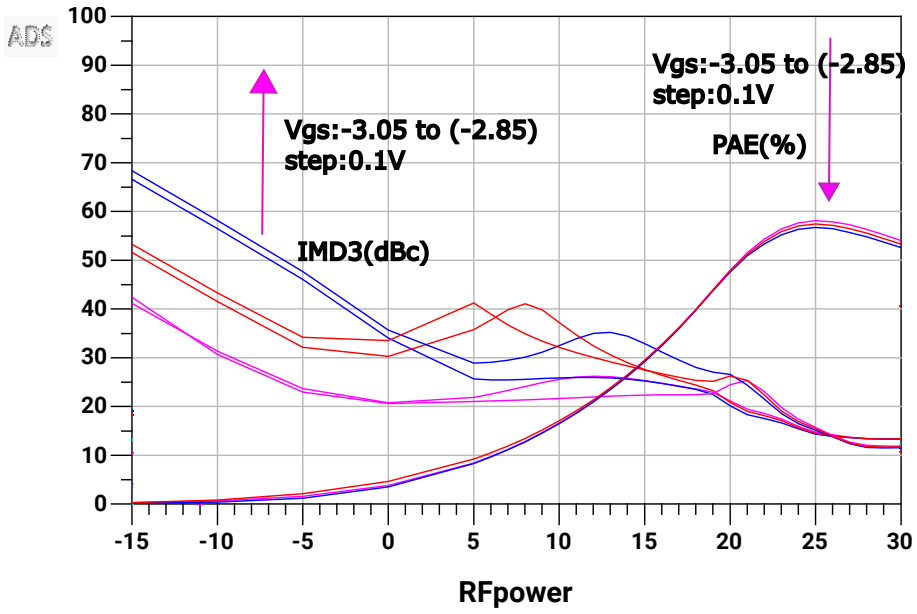

Figure 3.14: Optimize IMD3 by changing biasing point(V_{GSq} ranges from -2.85 to -3.05 V)

Modification of source and load terminations in base-band

IMD3 performance is affected by source and load terminations in base-band frequency. For testing and verifying if they could optimize the IMD3, the modification trial was started. The termination impedance range in this instance is 5 Ω, 50 Ω, and 100 Ω.

As Figure. 3.15 presents, the IMD3 moves toward a higher linearity value throughout the whole input power range when the load impedance at baseband $Z_{L,bb}$ lowers, and IMD3 is not benefited by changing the source impedance at baseband $Z_{S,bb}$. Another important FOM PAE increases as the value gets lower. As a result, the $Z_{L,bb}$ is set to 5Ω, while the $Z_{S,bb}$ keeps the previous value.

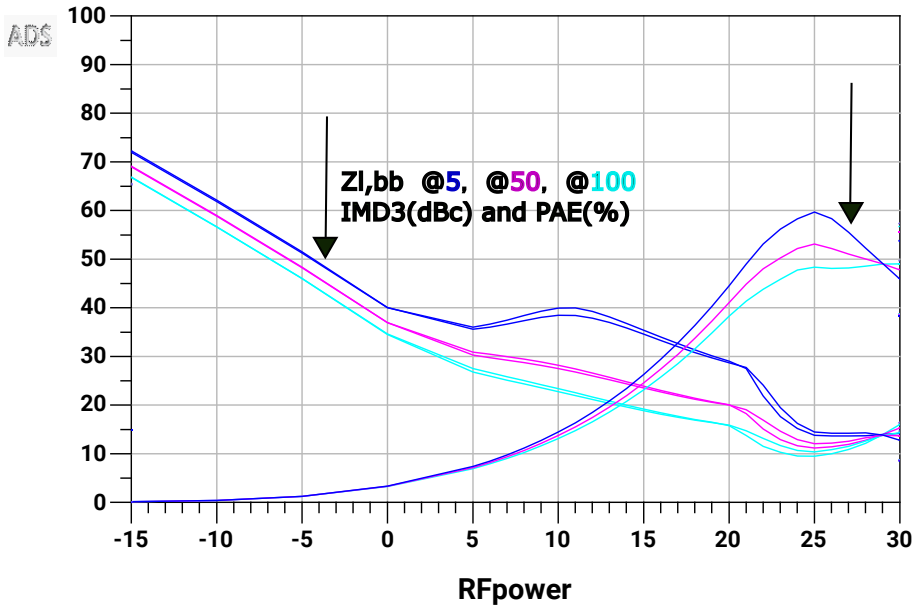

Figure 3.15: Optimize IMD3 by changing load termination in baseband(@$Z_{L,bb}$=5, 50, 100 Ohm)

Mismatching the Load and Source

When the Load and Source are mismatched, the values of the fundamental source and load, baseband source and load, and 2nd-harmonic source and load will be changed manually.

Compared to the performance of Figure. 3.13, the performance of Figure. 3.16 shows that the PAE increases a little when the input power reaches 24 dBm, but boosts a lot when the IMD3 reaches -30dBc. The previous value of PAE is 22% @IMD3=30 dBc, but now it reaches 51.6%.

After optimizing the terminations, IMD maintains below -30 dBc till a further input power level, and it keeps a good margin before reaching the input power level to 24 dBm. In the optimized case, the $Z_{L,bb}$=(5+0.24*j) Ohm, $Z_{L,f0}$=(13.8+21.25*j) Ohm, $Z_{L,2h}$=(2-4*j) Ohm. Source terminations are $Z_{s,f0}$=(4.7+1.4*j) Ohm, $Z_{s,2h}$=(500+20*j) Ohm. When used with these terminations, the IMD3 maintains a value above 30 dBc until the input RF power reaches a value of 21 dBm, with a corresponding PAE of about 51.6%

In the tuning process, the 2-Harmonic load and source tuning have little impact on IMD3, notably not in the region of a strong signal. And it mainly affects the Efficiency and PAE.

In conclusion, tuning the source/load at the base-band, fundamental, and second harmonics is a good way to optimize the performance for satisfying the target of SDC.

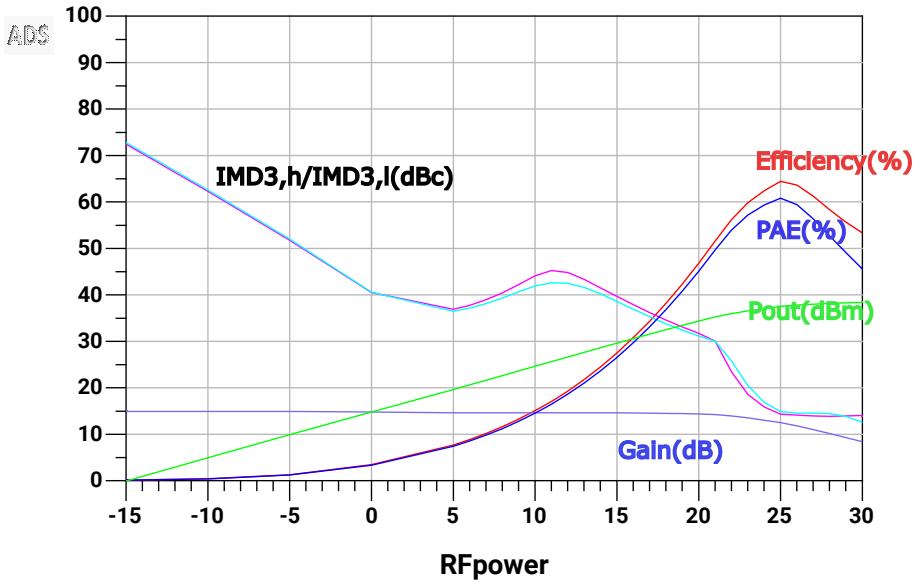

Figure 3.16: Optimize IMD3 by mismatching the load and source termination

3.3.3 Verification of the one-Tone performance

Taking the values of optimized terminations into the one-tone schematic obtains the performance in Figure. 3.17. As presented in the plot, the one-tone simulation performance satisfies the requirements of SDC, leaving enough margin to deal with the loss in PCB manufacturing.

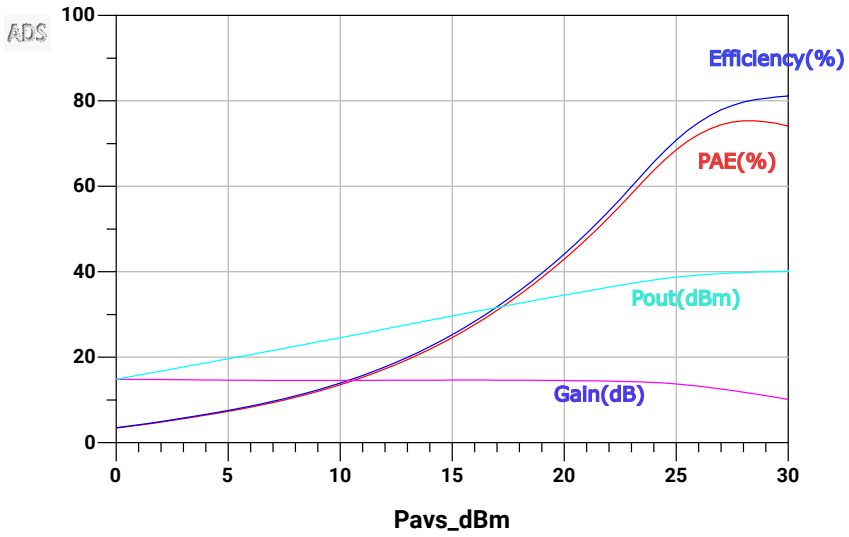

Figure 3.17: Verification of one-tone simulation after optimizing IMD3

3.4 Ideal Matching Network

In the conventional PA design process, the input and output impedance for the PA integrated into the RF front-end are 50 Ω [1], [2], [21], which differs from the optimal values required for maximum power transfer or efficiency, as determined through impedance optimization techniques. To address this mismatch, impedance matching networks are introduced to transform the standard 50 Ω reference to the target optimal impedance. In this work, such ideal matching networks are realized by using ideal transmission lines (TLs). The design approach and implementation details of these networks are discussed in the following sections.

3.4.1 Output Matching Network

According to the sequence of determining the optimum impedance, the output matching network is designed first. Load optimization involves simultaneous control of the baseband, second harmonic, and fundamental frequency components. To achieve the target, matching networks must be designed to provide the target impedances at the respective frequencies where optimization is desired. Each matching sub-network is responsible for independently controlling its designated frequency component, thereby enabling frequency-selective impedance shaping for optimal PA performance.

The design order of the matching network is shown in Figure. 3.18, the place of the fundamental control block follows the 2nd-Harmonic control block to achieve optimal performance in terms of $P_{out,f0}$ and PAE at the fundamental frequency.

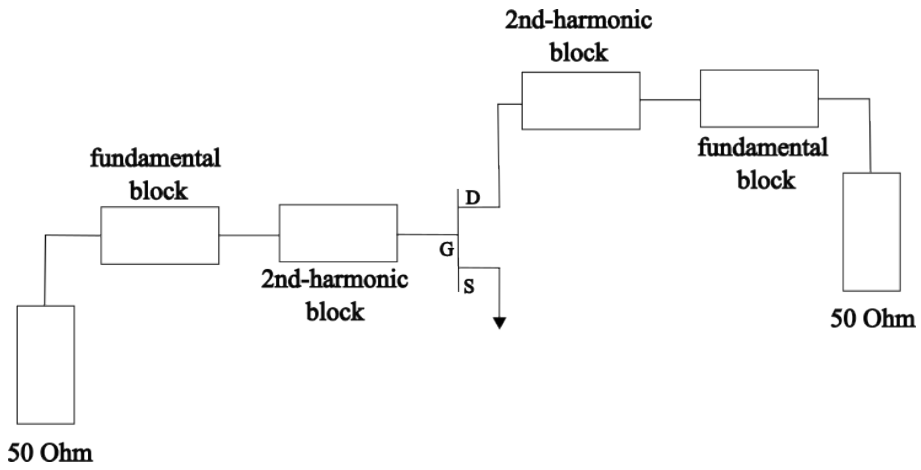

Figure 3.18: Ideal Matching Network Blocks

Second-harmonic Short Block

Theoretically, the harmonic matching network does not cause any power dissipation, as the reflection coefficient at the second harmonic is purely reactive. Based on this principle, an appropriate network topology is introduced to provide the required harmonic termination without incurring power loss.

Topology is presented in Figure. 3.19, a transmission line structure in series is used primarily to modify the phase of $\Gamma_{L,2f0}$, where a shunt is used to "short" the 2nd-harmonic wave in the matching network.

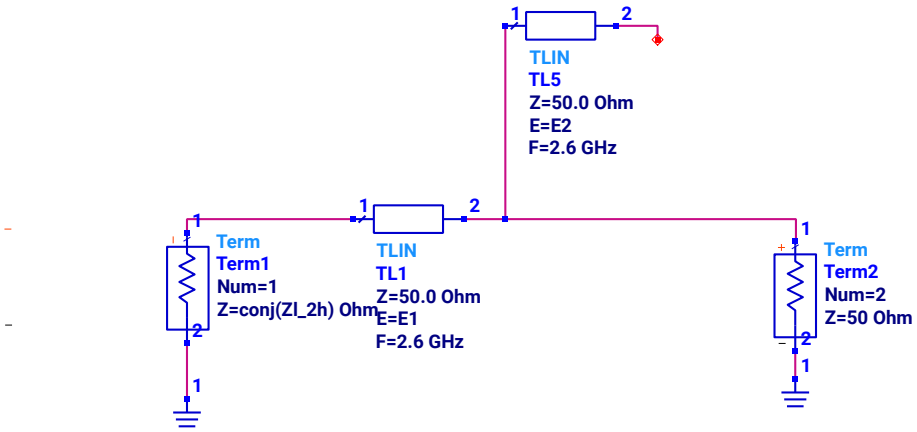

Figure 3.19: Second-harmonic Control Block in Output Matching Network

By presenting a short-circuit termination at the $2f0$ frequency, the 2nd-harmonic current is reflected into the circuit rather than being transmitted to the load, thereby minimizing power dissipation.

The S_{11} will be located in the short point of the Smith Chart by employing this topology with the correct length of the TLs in series (see Figure. 3.20).

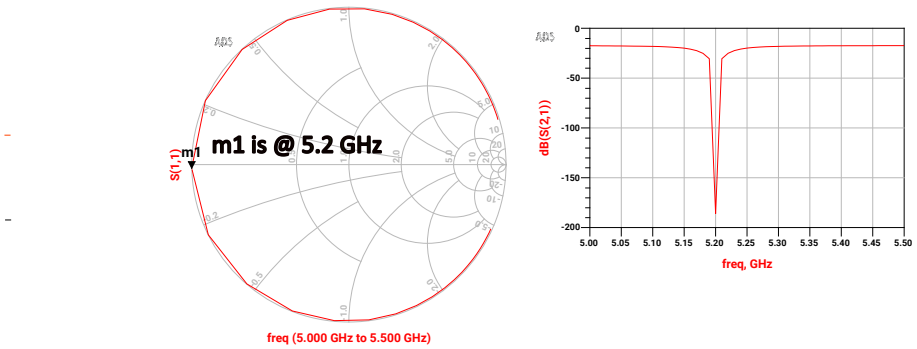

Figure 3.20: Second-harmonic reflection coefficient

Fundamental Control Block

In the fundamental control block design, the target is to make the chosen fundamental load matches the 50 Ω without power dissipation. The topology also uses a tunable transmission line to present the determined $\Gamma_{L,f0}$ at the load. And the topology is similar to the 2nd-harmonic control block. In Figure. 3.21, the S_{11} provides an illustration of the match condition. As a result, the S_{11} reaches almost -50 dB on frequency 2.6 GHz in the plot, demonstrating the network is well-matched to the $\Gamma_{L,f0}$ over the whole band.

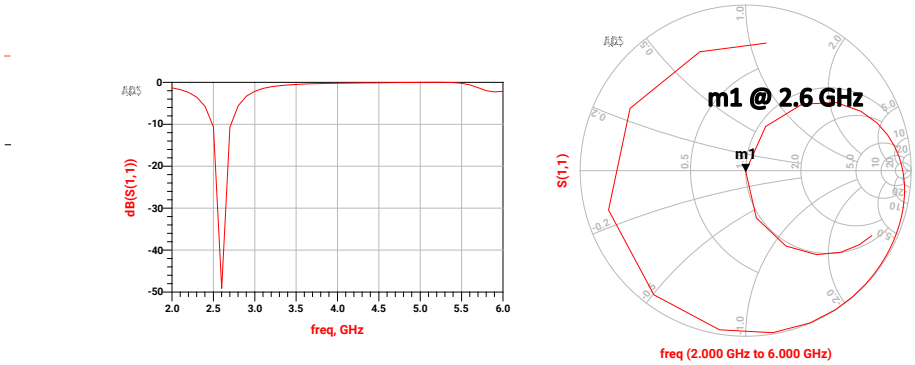

Figure 3.21: Fundamental frequency reflection coefficient

Verification after applying the ideal output matching network

In one-tone simulation and two-tone simulation, the ideal output matching network (OMN), which is designed in a forward process, is applied to the active device, and the source termination setting is determined as the values.

Figure. 3.22 presents the 1-tone performance after using the output matching network. From the plot, it illustrates that the matching network works well as the performance is perfectly similar to the Figure. 3.16 (before using the output matching network).

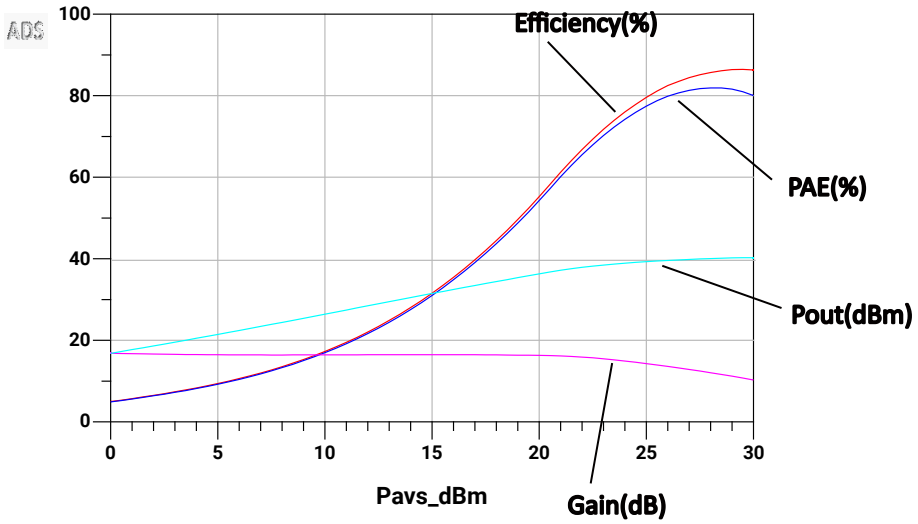

Figure 3.22: 1-tone simulation after introducing output matching network

As for the two-tone simulation, it is shown in Figure. 3.23. Compared with the performance of Figure. 3.16 (without OMN), the performance of applying the OMN looks better. The IMD3 curve becomes smoother and maintains a better margin between 0 dBm and 7 dBm P_{in}.

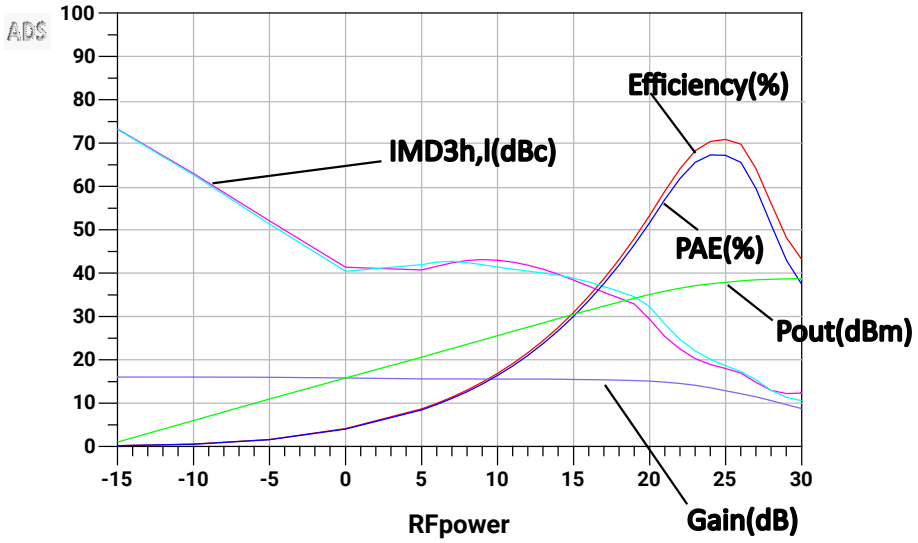

Figure 3.23: 2-tone simulation after introducing output matching network

3.4.2 Input Matching Network

For the input matching network (IMN) design, the steps are the same as OMN design process. Firstly, consider the 2nd-harmonic control block, then design the fundamental control block.

In the chosen topology, which uses the adjustable transmission line to achieve the desired match condition. Consequently, the S_{22} shows the corresponding condition. The S_{11} maintains a good match at center frequency 2.6 GHz and stays below -50 dB over the band.

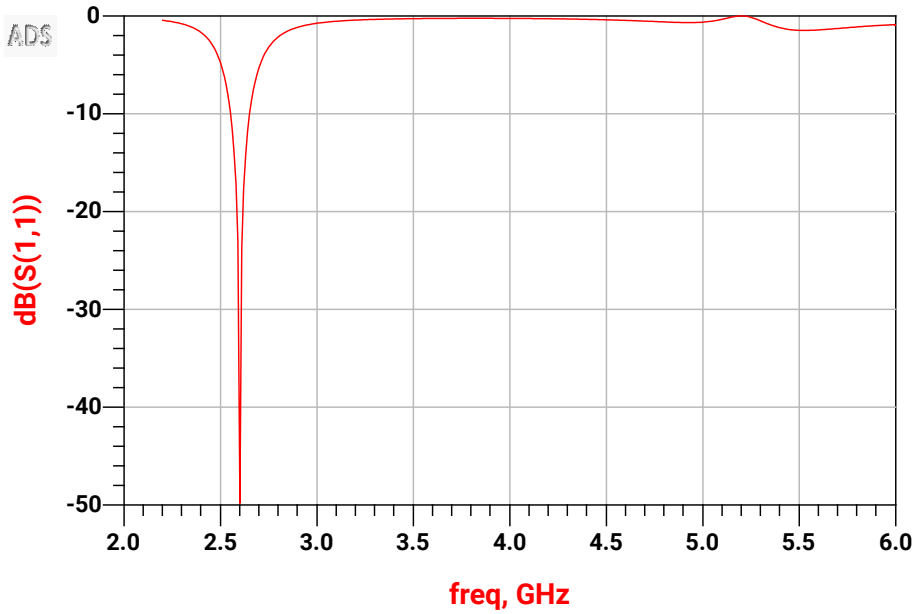

Figure 3.24: Fundamental frequency reflection coefficient

Taking the IMN and OMN into the schematic to verify the one-tone and two-tone performances, which are shown in Figure. 3.25 and Figure. 3.26. The plots show that the performances are similar to schematic without IMN and OMN (only using optimized source and load impedance), which means the matching networks are working well.

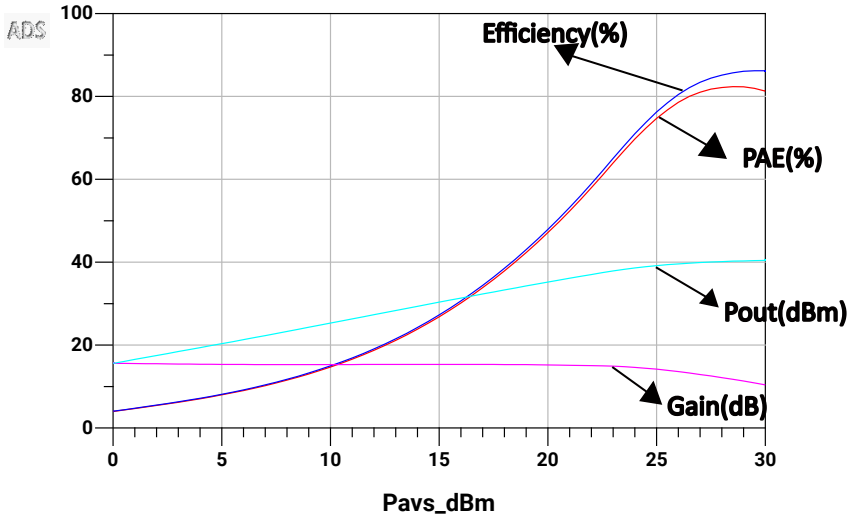

Figure 3.25: 1-tone simulation after introducing matching networks

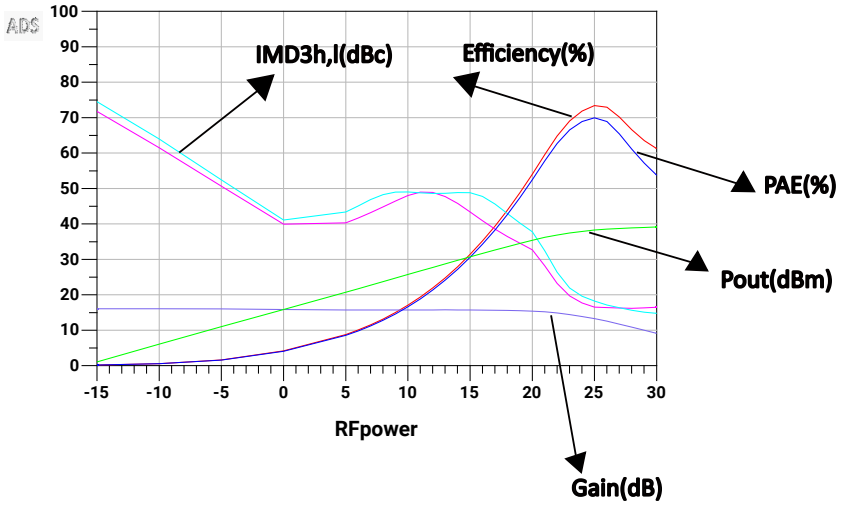

Figure 3.26: 2-tone simulation after introducing matching networks

3.5 Microstrip Line Implementation

After designing the TLs version schematic, the next step is to convert the transmission lines to microstrip lines (MLs). The converted circuit will be built in hybrid technology on a Rogers_4350B_TanD31[22] PCB with a dielectric constant of 3.66. Since introducing the MLs will affect and worsen the performance of the TLs version and MLs version, the primary step is focusing on optimizing the input and output matching network to ensure it is coherent with the ideal one. An EM simulation is set up to evaluate the practical performance.

3.5.1 Microstrip Line in Matching Networks Design

The microstrip is a quasi-TEM transmission line due to the inhomogeneous cross-section. Microstrip line is a form of electrical transmission line comprising a conducting strip, a dielectric substrate, and a ground plane [1]. In this configuration, the conducting strip is positioned above the ground plane and is separated from it by the dielectric substrate. The schematic representation of the microstrip structure is illustrated in Figure. 3.27. All corresponding line parameter is provided in Keysight ADS.

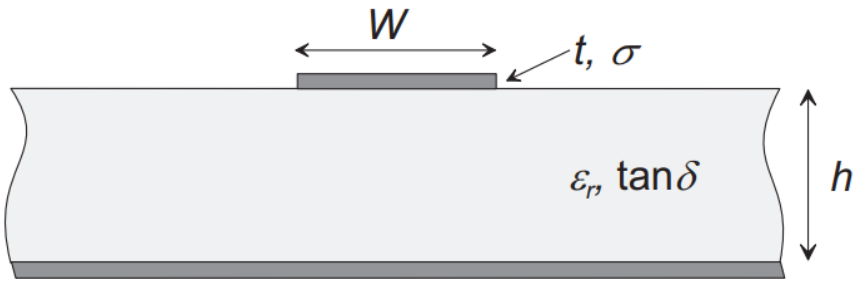

Figure 3.27: Microstrip line model [1]

Microstrip lines, unlike ideal transmission lines, inherently exhibit losses that cannot be entirely eliminated. These losses are primarily categorized into conductor losses and dielectric losses, both of which are closely related to the geometry of the transmission line—particularly its width, which determines the characteristic impedance [1], [2], [19].

Generally, increasing the strip width reduces ohmic losses; thus, narrow, high-impedance lines tend to suffer greater conduction loss. However, high-impedance lines also tend to radiate more electromagnetic energy, which can adversely affect the performance of power amplifiers (PAs). Therefore, in practical design, careful consideration must be given to the transmission line width to balance impedance, minimize radiation, and reduce overall losses. Overly wide lines, while offering reduced resistive loss, may introduce other performance trade-offs and should be avoided.

The matching networks designed using ideal TLs are typically well optimized to achieve the intended terminations and meet the desired performance specifications. Building upon these optimized designs, equivalent matching networks are then implemented using MLs by preserving the same circuit topology (in Figure. 3.28, Figure. 3.29). The physical dimensions of the MLs are subsequently determined based on the electrical characteristics derived from the ideal TLs implementation.

Furthermore, microstrip lines and T-junctions are incorporated into the circuit, introducing parasitic effects that influence the overall performance of the PA. Consequently, the matching networks require careful optimization to mitigate these parasitic influences and ensure optimal performance.

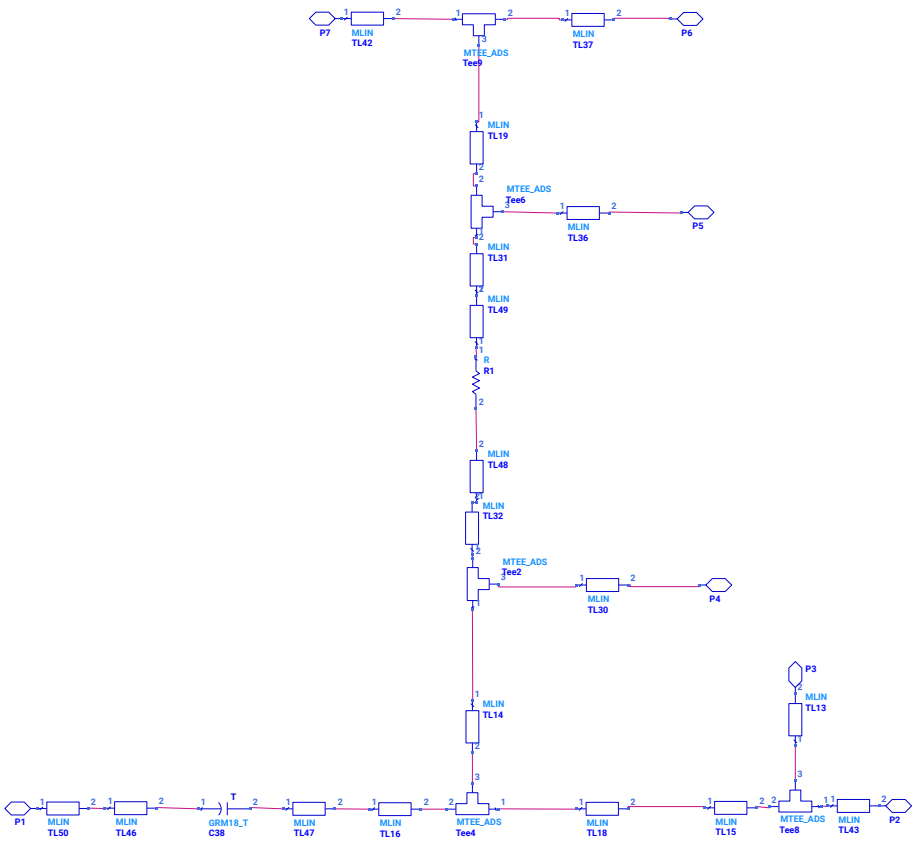

Figure 3.28: Input Matching Network (MLs)

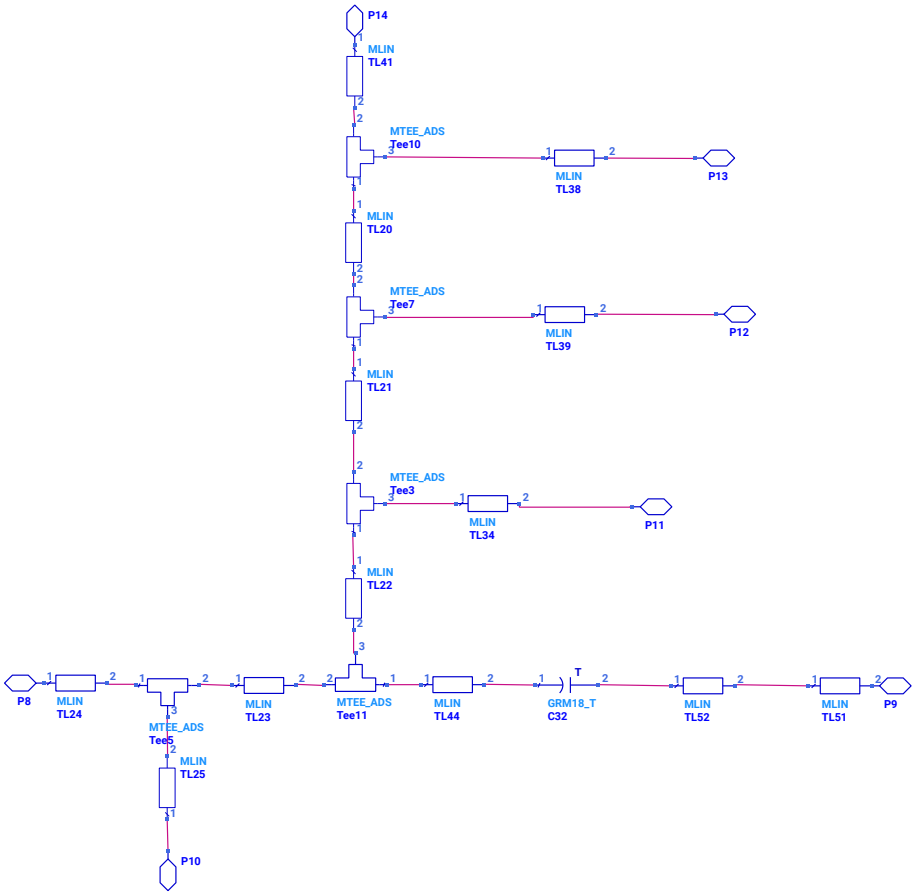

Figure 3.29: Output Matching Network (MLs)

The optimization results of IMN and OMN are shown in Figure. 3.30 and Figure. 3.31 respectively.

From the plots, the S11 of MLs stays below -20 dB in the IMN simulation over the 2.58 GHz to 2.62 GHz band, and reaches below -25 dB in the center frequency. In comparison to the ideal TLs, it is less matched because of the loss and parasitic effect in the microstrip lines. However, overall, the performance of MLs after optimization performs well in that band. In the OMN simulation, the S22 at the center frequency maintains a level of lower than -20 dB.

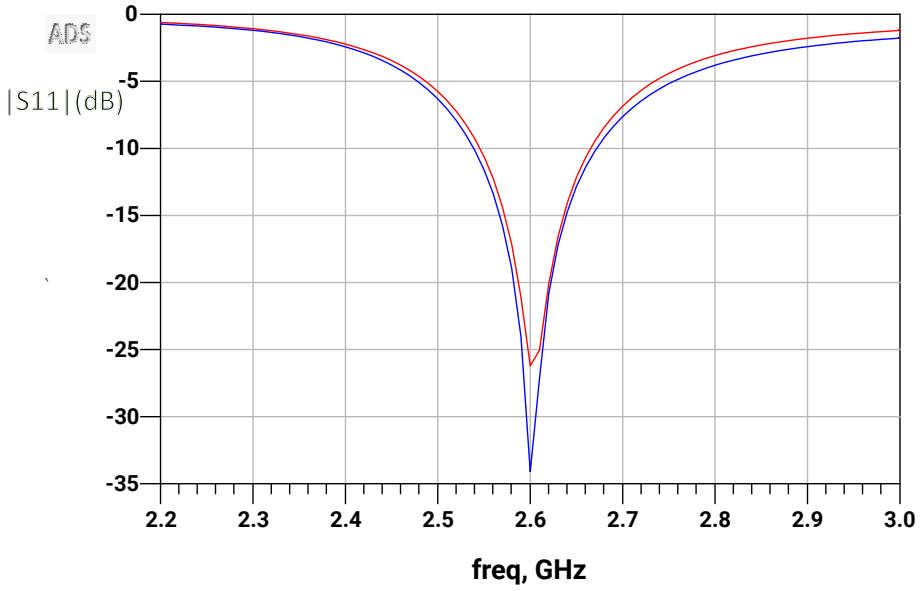

Figure 3.30: Comparison between MLs IMN (red) and ideal TLs IMN (blue).

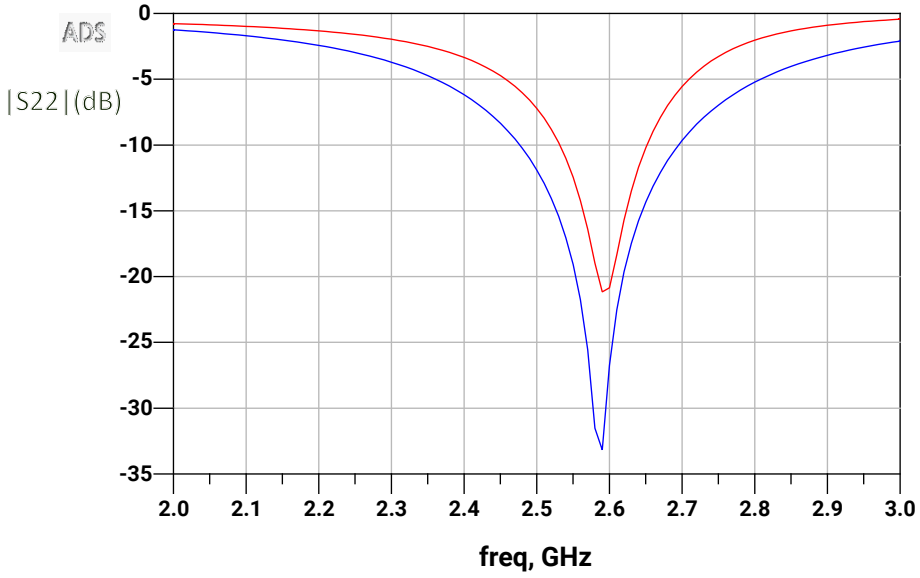

Figure 3.31: Comparison between MLs OMN (red) and ideal TLs OMN (blue).

Taking the optimized matching networks into one-tone and two-tone simulation schematics, the performances of one-tone and two-tone simulations are presented in Figure. 3.32 and Figure. 3.33 respectively. These performances are compared to the PA implemented with ideal TLs. Both of the circuits are biased, with V_{GSq} = -2.95 V and V_{DSq} = 28 V.

Figure. 3.32 and Figure. 3.33 present the one-tone and two-tone performances of the optimized circuit. In the one-tone simulation, the PAE reaches 62% and Pout exceeds 36

dBm, which satisfies the requirements of SDC. In the two-tone simulation performance, the IMD3 keeps a good margin and reaches -30 dBc until 19 dBm, and the PAE of the two-tone simulation (19dBm) is 48%, which is an acceptable value.

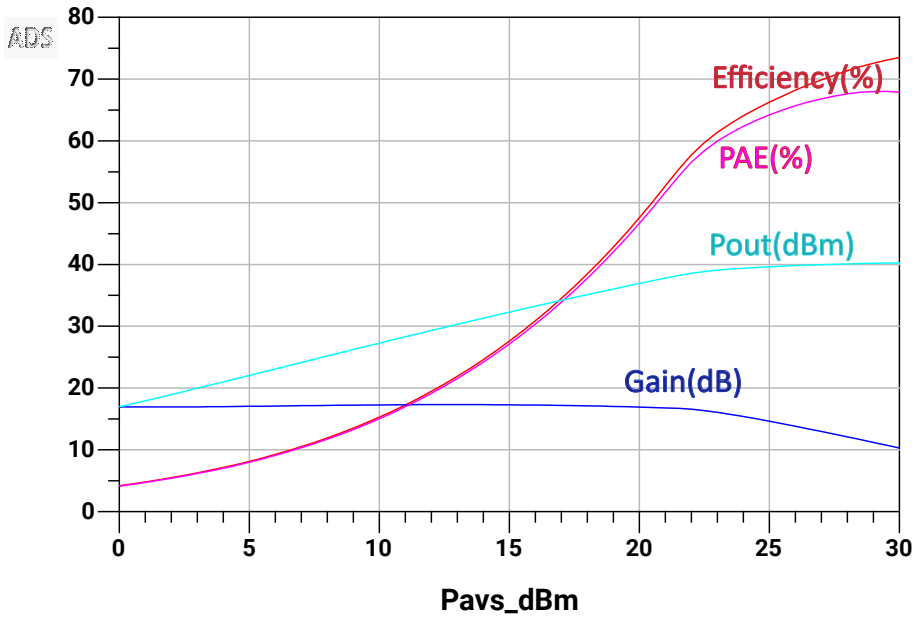

Figure 3.32: 1-tone performance of optimized MLs circuit.

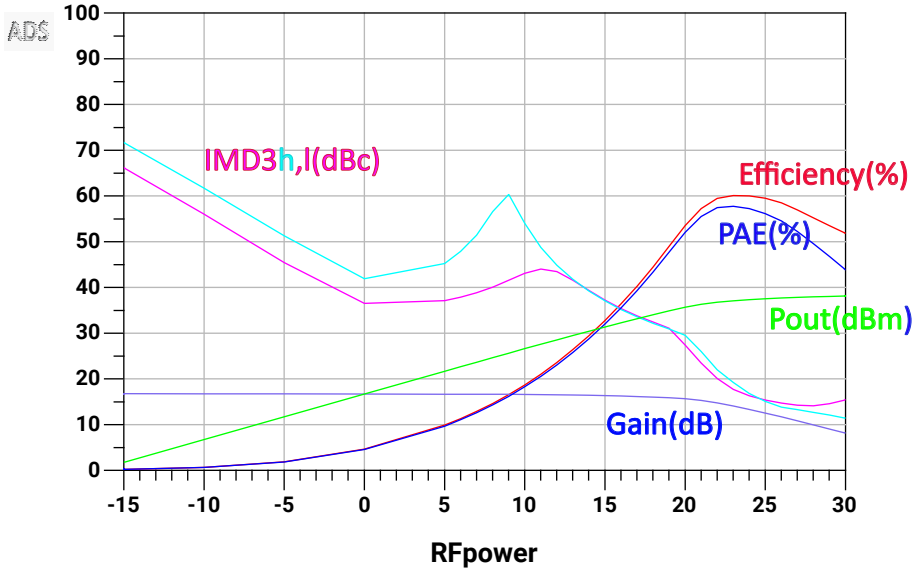

Figure 3.33: 2-tone performance of optimized MLs circuit.

3.5.2 Layout and Electromagnetic Simulations

The following step involves the generation of the circuit layout based on the optimized schematic (see in Figure. 3.34). Following the layout design, an electromagnetic (EM) simulation is performed to achieve a more accurate result of the power amplifier's performance. The EM simulation accounts for the presence of electric and magnetic fields within the circuit, thereby enabling the analysis of interactions among various circuit elements that may alter the expected behavior predicted by schematic-level simulations.

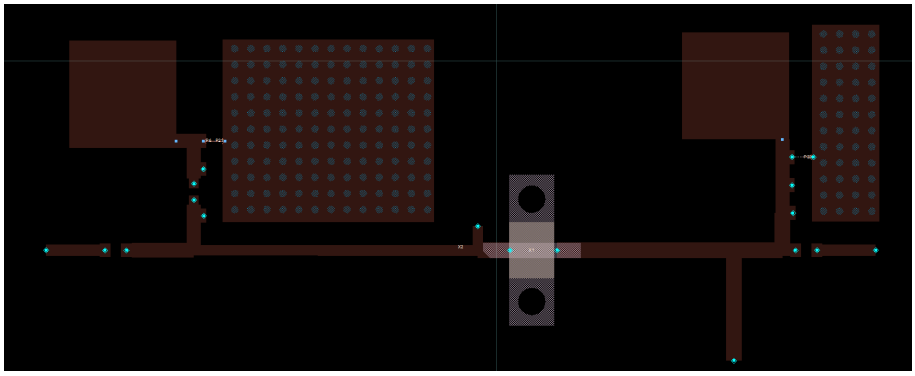

Figure 3.34: EM Layout

An effective approach to addressing potential design issues involves partitioning the circuit into distinct sub-blocks and performing electromagnetic (EM) simulations on each segment individually. This strategy facilitates the identification and correction of localized problems.

The EM simulation yields S-parameters for each sub-circuit, which are subsequently integrated into the nonlinear circuit-level simulation following the inclusion of active devices and lumped elements. Upon completing the EM-based optimization of the power amplifier, a final layout verification is conducted to ensure that the design meets the desired performance specifications. A comparative analysis of the PA's performance, with and without the inclusion of EM effects, is presented in the following section.

The comparison performances between the EM layout level and schematic are shown in Figure. 3.35 and Figure. 3.36, which include both one-tone and two-tone simulations. The one-tone performance shows that the EM layout level satisfies the specification of SDC: the P_{out} in the performance reaches near 36 dBm and the PAE reaches 59% when $P_{in,f0}$ = 24 dBm, which satisfies the target $P_{out,f0}$.

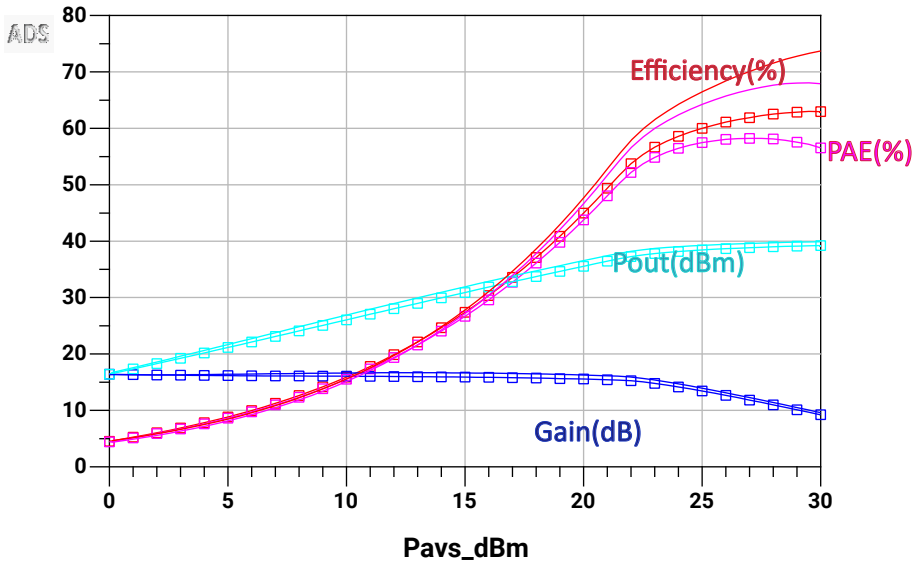

Figure 3.35: Comparison of 1-tone performance between EM layout level (square) and schematic level (line)

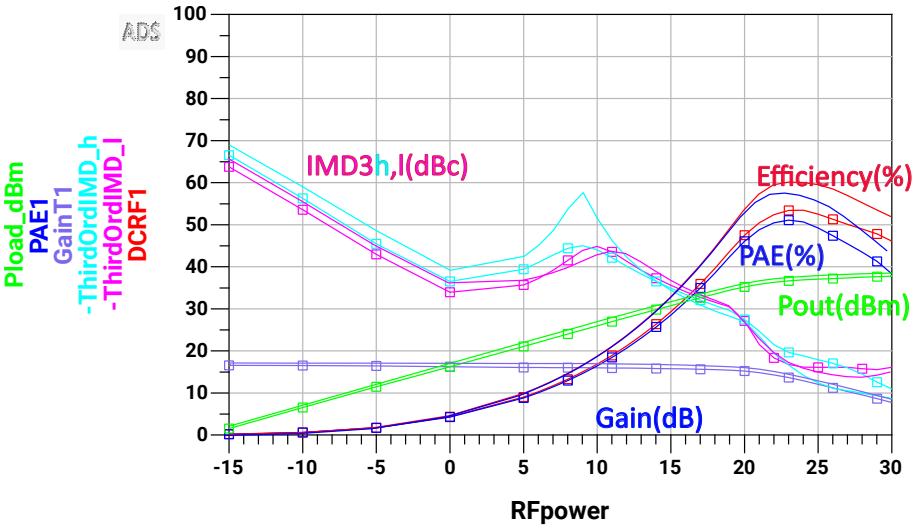

Figure 3.36: Comparison of 2-tone performance between EM layout level (square) and schematic level (line)

For the comparison of two-tone performance between EM layout level and schematic level, the PA of EM simulation presents a bit worse than schematic level performance, the IMD3 margin drops a little but still keeps an enough margin over -30 dBc. The PAE in EM simulation is 46%.

The final layout is shown in the following Figure. 3.37.

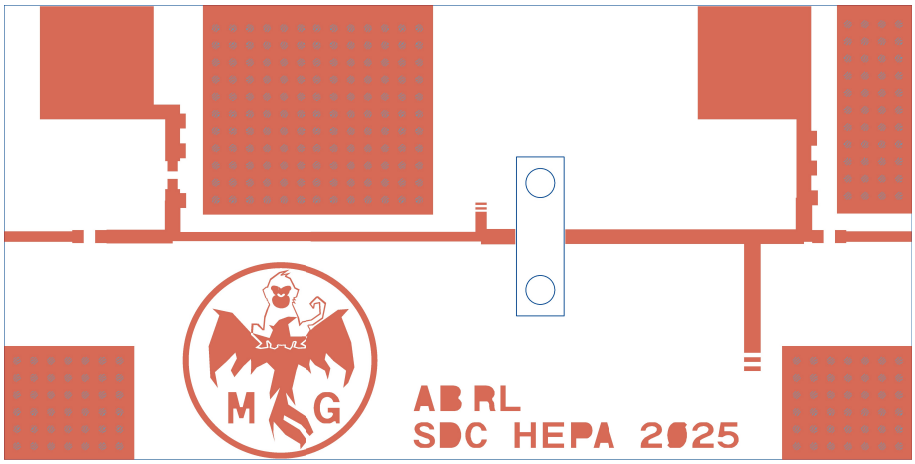

Figure 3.37: Final Layout of PA

4 Prototyping

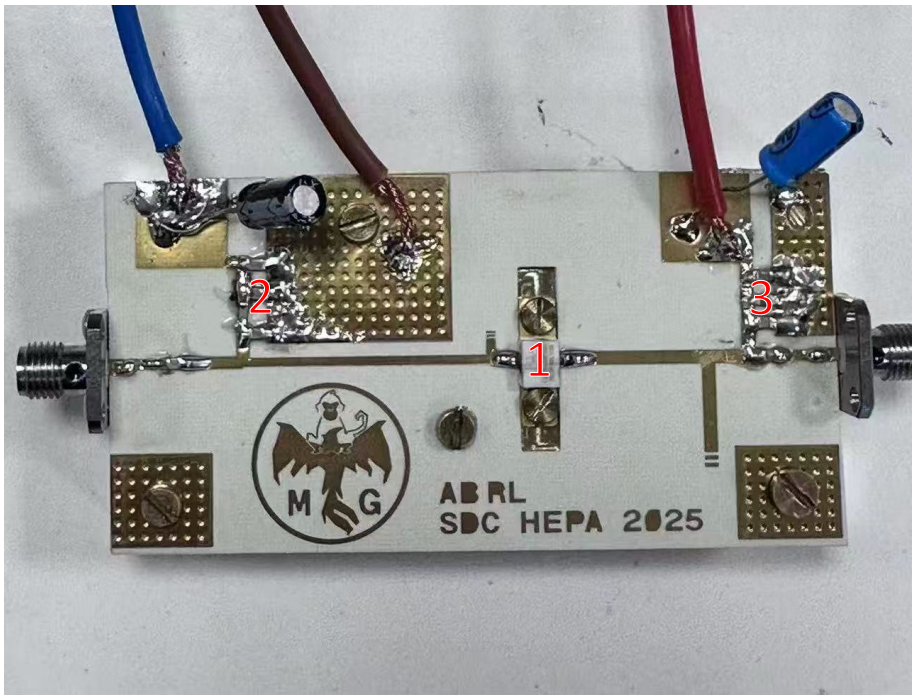

Figure 4.1: Final prototype of PA

Figure. 4.1 presents the final PA prototype, in which the IMN, transistor, and OMN are arranged from left to right. The region with number ”2” indicates the biasing path of the IMN, region ”1” corresponds to the transistor, and region ”3” represents the biasing path of the OMN. The areas with multiple holes serve as ground connections.

In the Design Process of the Stabilization Network section, we discussed the methodology for designing the essential components of PAs and explained why we adopted the rationale for adopting a novel, non-conventional stabilization network in this thesis. However, during laboratory measurements, the prototype exhibited oscillations at a relatively low frequency (approximately 600 MHz). Based on the observed behavior, this oscillation is likely attributed to instability in the system.

To solve the oscillation problem, the following three methods are used in the simulation stage. The first method involves modifying the biasing network on the drain side, and the second method consists of replacing the first decoupling capacitor in the input matching network (IMN) with a higher value capacitor, increasing it from 56 pF to 100 pF, and the third method focuses on redesigning the input matching network (IMN) itself, induced by some resistance from the gate to ground is needed to attenuate the gain.

Figure. 4.2 and Figure. 4.3 shows the original results before using methods to solve the instability problem.

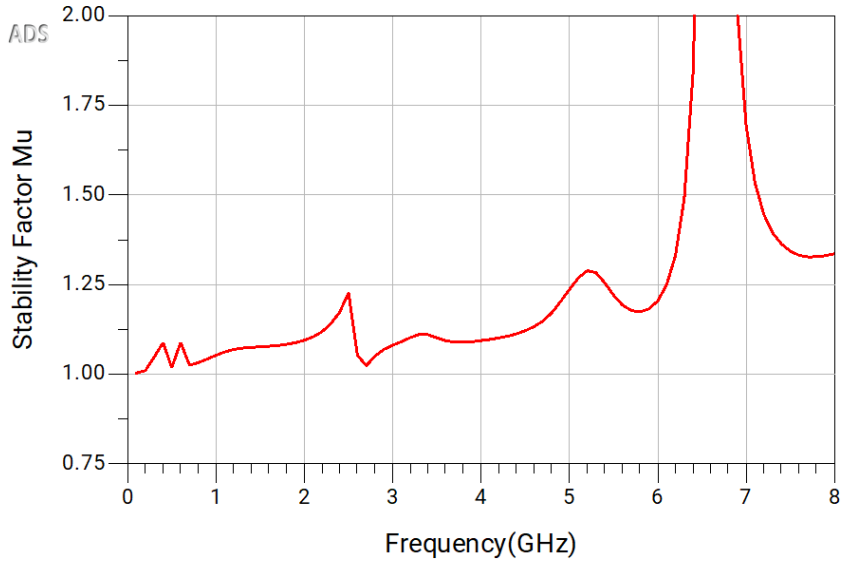

Figure 4.2: Stability factor before using the methods to solve the instability issue

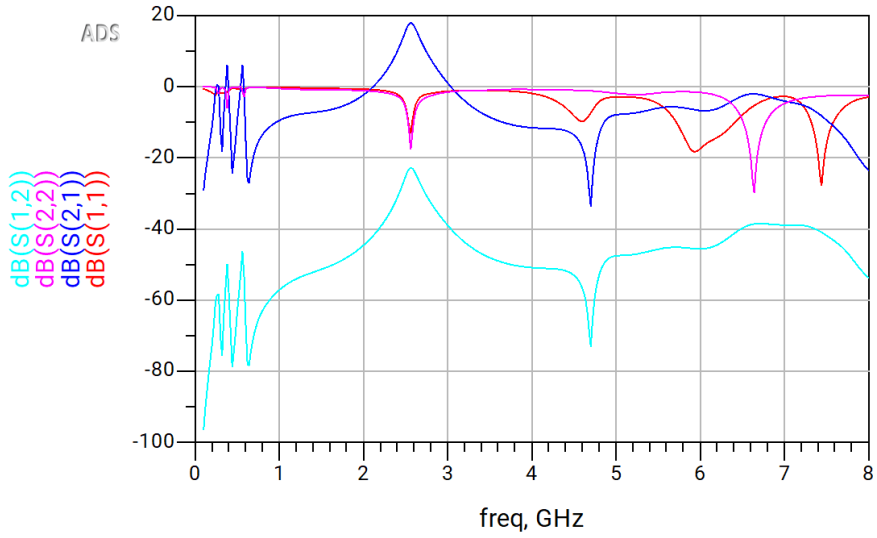

Figure 4.3: S-parameters before using the methods to solve the instability issue

From the two figures, we can see that S_{12} and S_{21} have peaks between 200 and 700 MHz. Mu shows two peaks between 400-600 MHz, which may cause the instability issue.

The First Method is changing the biasing network (drain side). The last 270 pF capacitor (close to the DC feed) can be replaced with a capacitor in the mF range to cancel

the resonance at the kHz level. After that, an additional capacitor in the nF range can also be added. All of these considerations are aimed at ensuring stability in the baseband range. The underlying assumption is that the oscillations observed at 600 MHz(in the Lab) may be caused by baseband instability, so the first step is to address the baseband issue from the drain side. Figure. 4.4 shows the S-parameter performance after using the first method.

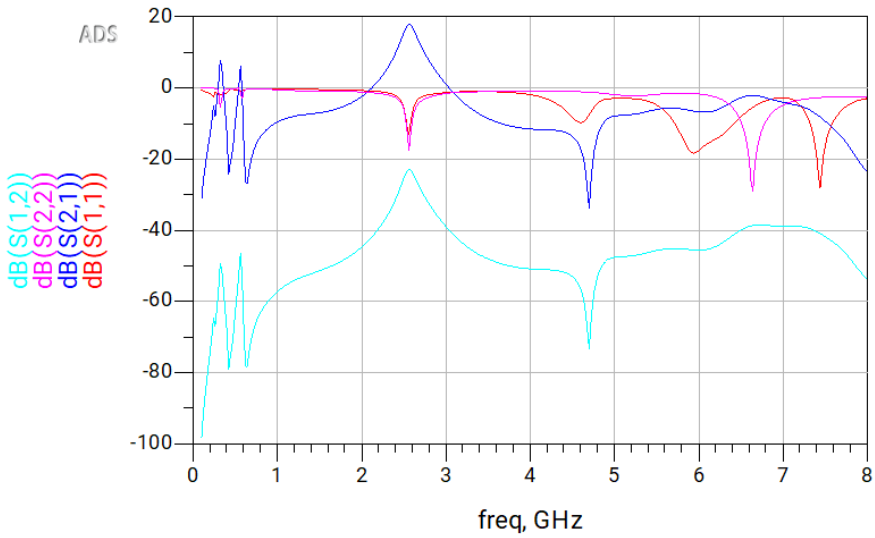

Figure 4.4: S-parameters result after using the first method

The Stability Factor still has two peaks in low frequencies, whose amplitudes are over 0 dB. The S_{21} and S_{12} peaks are above 0 dB in the range of 200-700 MHz, so this method may not be enough to solve the problem in the PCB.

The Second Method is to change the first decouple capacitor in IMN from 56 pF to 100 pF(if the cap value is bigger than 100 pF, the mu will be lower than 1 in 600 MHz). Figure. 4.5 shows the performance of adapting the second method; the amplitudes of peaks are decreasing.

The Third Method is changing the IMN. This approach mainly considers that some resistance from the gate to ground is needed to attenuate the gain, and we don't want to change the original matching condition. The matching condition does not change, and the RF performance will not change. We can connect the resistance on the original biasing path to a nearby ground. Then, cut a section close to the transistor, insert a DC block (an inductor), and in the Lab, use a copper sticker to reconnect it to the original biasing network. The main idea is to separate the DC pass part and the RF path to maintain the original RF path matching condition.

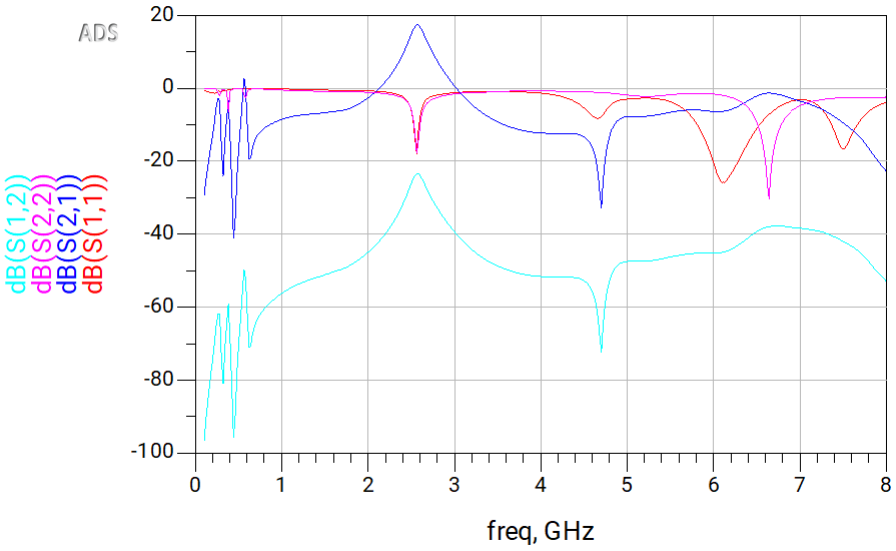

Figure 4.5: S-parameters result after using the second method

Figure. 4.6 shows the performance of S-parameters, and Figure. 4.7 shows the structure of IMN after using the Third Method,

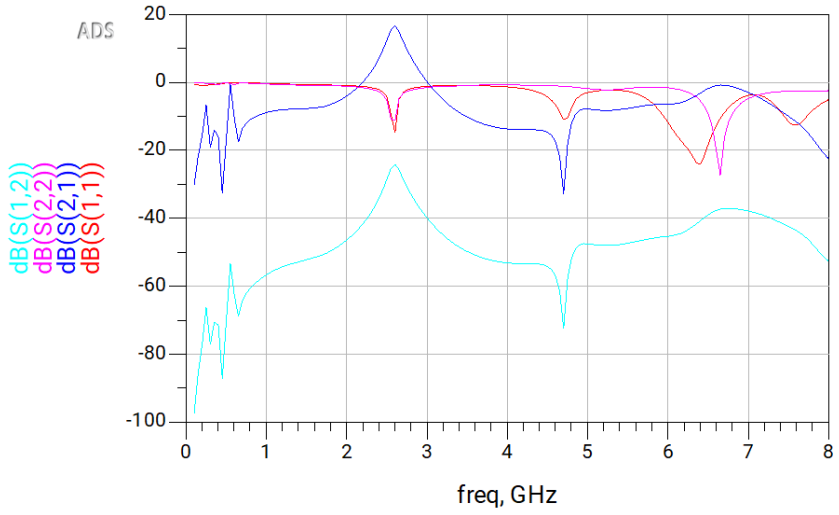

Figure 4.6: S-parameters result after using the third method

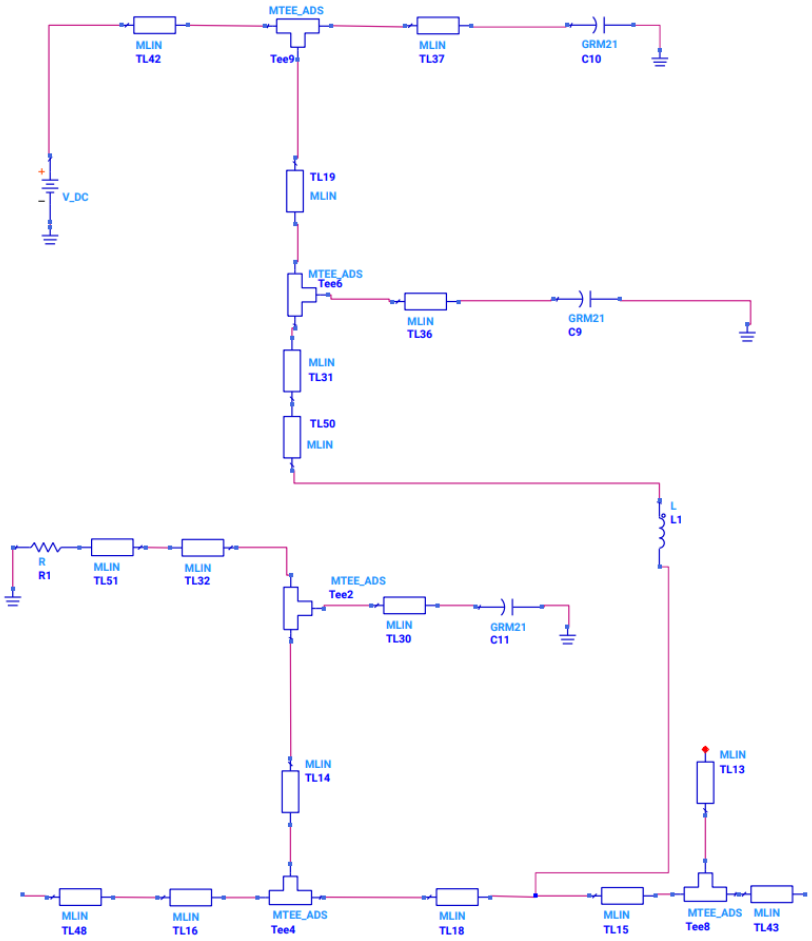

Figure 4.7: IMN structure after using the third method

After changing the IMN part, the performance of S_{21} and S_{12} shows a big difference with the First and Second Methods, the number of peaks is reduced compared to the Second method, and the amplitude of peaks is lower than the First Method and the original performance. Therefore, the third method appears to be the most suitable choice in the three methods for addressing the instability issue. However, this requires the realization of a new prototype, which will be carried out as future work and is outside the scope of this thesis.

5 Conclusion

This thesis presents the design of a Class-AB microwave power amplifier operating at approximately 2.6 GHz, with an optimized trade-off between efficiency and linearity.

The objective of the proposed power amplifier (PA) is to optimize its performance for the HEPA competition at the MTT-S conference. A major challenge in the design process lies in simultaneously satisfying the requirements for minimum output power, gain, and linearity under two-tone testing, while achieving the best trade-off among these parameters. To meet the design goals defined by HEPA, the optimum source and load terminations at the baseband, fundamental, and 2nd-harmonic frequencies are carefully selected. Furthermore, to account for electromagnetic effects that cannot be fully captured at the circuit level, EM simulations are performed on all passive structures to evaluate the expected performance of the PA. Finally, a prototype is implemented using a 10W packaged GaN device.

The final simulations demonstrate that the design fully meets the requirements of the SDC, achieving a PAE of 59% in one-tone test and a PAE of 46% while maintaining the linearity target of better than −30 dBc in two-tone test.

To solve the prototype's oscillation problem in the laboratory, we discussed three methods in the simulation stage, and the third method appears to be the most suitable and useful choice in the three methods for addressing the instability issue. However, this requires the realization of a new prototype, which will be carried out as future work and is outside the scope of this thesis.

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