POLITECNICO DI TORINO
Master Degree in Electronic Engineering

Master Degree Thesis

Design and Implementation of an Embedded Board for Vehicular Connectivity

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Abstract

Vehicular connectivity serves as a cornerstone in the rapid diffusion of intelligent transport systems and smart mobility. By rendering information exchange feasible between vehicles and networked devices, a shift towards more reliable, resource efficient and environmentally conscious traffic interactions is possible. Versatile, reliable hardware platforms supporting various interfaces play a pivotal role in the ongoing deployment of Vehicle-to-Everything (V2X) communication protocols. To provide the physical infrastructure able to integrate different communication standards and allow for interoperability, a compact, custom, open source hardware platform has been tailored for this application.

Starting from a set of initial specifications in terms of interfaces, storage, and physical dimensions, an embedded board has been designed to accommodate off-the-shelf modules and support wireless connectivity between vehicles and networked devices in general. The design revolves around a System-on-Module by Variscite (DART series) which functions as a core processing module equipped with interfaces for a standard V2X On-Board-Unit. The board includes multiple miniPCIe slots supporting Wi-Fi and cellular modules, ports for serial communication, CAN, Gigabit Ethernet and Automotive Ethernet, USB and several GPIOs to grant flexibility, in addition to multiple storage solutions.

This thesis describes the board design process up to component placement. The work covers the specification refinement, schematic design, PCB stack-up and component placement, taking into account automotive environmental constraints such as power supply and thermal management. The electronic design has been implemented using KiCad EDA tools. Completion of signal routing and PCB manufacturing files for final prototype development will be carried out in future work.

Summary

Safe interactions, improved mobility, reduced pollution and energy saving are driving factors for the development of connected vehicles systems. The primary aim is to create a system that goes beyond traditional sensors, laying the foundation for better decision-making and predictive safety insights, as well as improving traffic management with dynamic route adjustment to reduce congestion and minimize emissions associated to fuel consumption.

Consequently, this leads to the necessity of open source embedded hardware for Vehicle-to-Everything (V2X) communication, essential to effortlessly integrate a reliable, powerful, low latency platform in existing vehicles.

Therefore, a solution to lack of customization, limited number of connectors and plug-in slots for connectivity modules on commercial platforms is proposed, while also safeguarding open source compatibility and ensuring interoperability. This thesis outlines the design methodology and implementation of an embedded board for vehicular connectivity, starting from a set of specifications, moving on to hardware components selection and printed circuit board layout up to component placement.

Once the concept was drafted and the initial requirements were refined, the core processing module was selected. The DART-MX8M-PLUS System-on-Module by Variscite based on the NXP i.MX 8M Plus processor was chosen due to its longevity support, small form factor, and most importantly, its capability to operate with Yocto built distributions. The Yocto project is an open source collaboration that provides tools and processes to create custom Linux-based systems in the embedded and IoT sector, regardless of the hardware architecture.

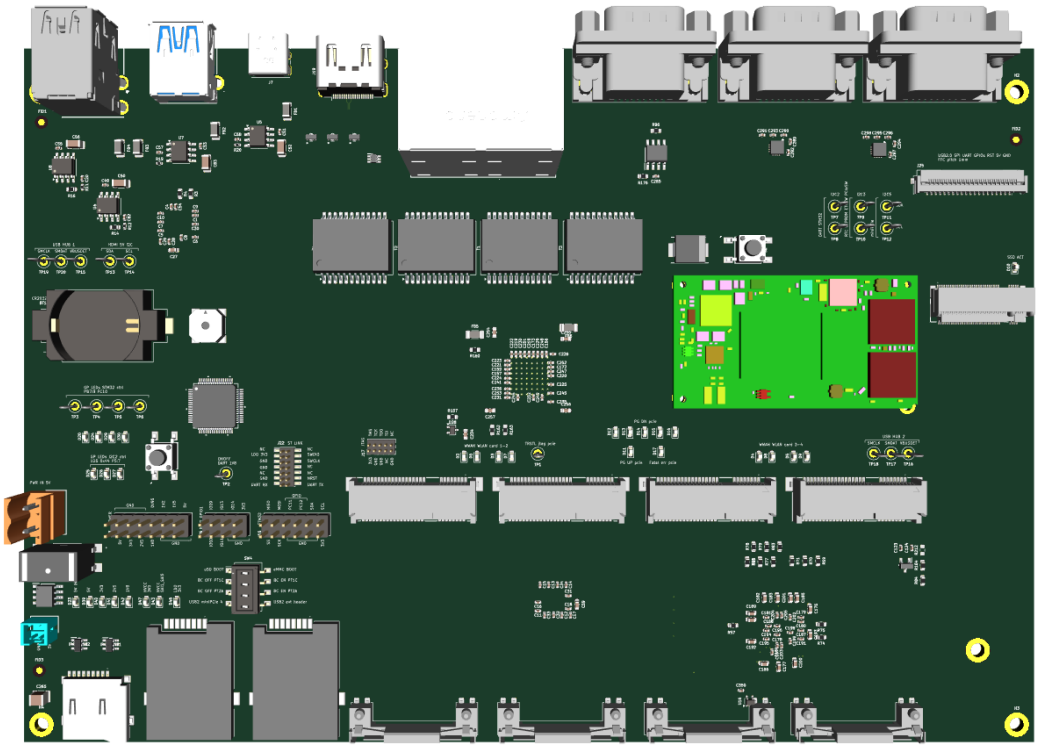
The design process proceeded with the switches and hubs selection, employed to adapt the SoM interfaces to the number of connectors requested by the end user. As for storage solutions, the board features a microSD card slot and an SSD slot compliant with PCIe standard for high speed event logging, in addition to the embedded Multi Media Card (eMMC) integrated on the SoM. Several Gigabit Ethernet ports are incorporated, as well as one Automotive Ethernet port which allows for precise synchronization and timestamp control in high-precision communication. The board is also equipped with multiple USB connectors of different form factors, a couple of serial debug ports and a display output. The Controlled Area Network (CAN) interface is included for robust and low cost data exchange and miniPCIe slots supporting Wi-Fi and cellular modules are incorporated for wireless connectivity.

On board power monitoring, fault detection and recovery is coordinated with the use of a microcontroller which handles the start-up routine and supplies additional interfaces for expandability. Component selection was conducted preferring widely available products with industrial temperature range, to ensure ease of replacement and scalability for future requirements. Board mounted connectors were chosen for enhanced stability due to their resilience to mechanical stress that is caused by frequent attaching and detaching in harsh environments. Furthermore, visual LED signaling for user ease of use and debugging purposes, such as real time monitoring of systems activity and quick fault identification, was incorporated. Integration of additional modules and support for optional peripherals

is ensured via export of interfaces and power lines, granting expandability and flexibility. The thermal management strategy adopted revolves around conductive cooling which, in conjunction with an aluminum case that also grants high grade shielding, help improve system reliability. A power supply with a wide input voltage range is used to step down the voltage and supply the board, facilitating system operation across multiple vehicle types such as passenger vehicles and heavy duty vehicles (trucks, buses, construction machinery).

Finally, the design was implemented using KiCad EDA tools. The schematic meets all the requirements specified by the interface standards integrated on the board in question and the PCB stack-up was chosen with the aim of reducing interference, optimize layer count and reliability. The final step ultimately involved careful component placement to ease routing and trace management, while maintaining functional grouping of components, also taking into account mechanical constraints and accessibility.

Further development of the project is planned as part of future work which will include routing completion, the generation of PCB manufacturing files for prototype fabrication and firmware design.



On Board Unit top view

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Chapter 1
Introduction

Over the past decade a worldwide effort has been invested towards implementing Intelligent Transport Systems (ITS) solutions, primarily addressing safety and traffic congestion concerns. ITS relies on vehicular connectivity and consists in monitoring, evaluating and managing transportation networks.

Many benefits derive from its deployment. Using real-time traffic data, it's possible to provide several services aimed at improving road safety, traffic efficiency and energy saving altogether. To illustrate some, it features hazards warning systems designed to reduce accidents, built upon predictive safety insights that extend beyond traditional sensors, and dynamic route adjustment to optimize course and maintain efficient movement, thereby minimizing the resulting emissions. Being applicable to both passenger and freight transport, a cohesive network for data exchange is formed, leading to smart mobility.

In recent developments, ITS solutions have evolved towards Cooperative Intelligent Transport Systems (C-ITS), focused on direct communication between entities that enables cooperation and lays the foundation for connected automated mobility (CCAM) [1]. Real-time data is exchanged via Vehicle-to-Everything (V2X) communication technology which allows vehicles to connect to each other, to road infrastructure and other users, thus to coordinate their actions.

Concept	Role	Example scenario
C-ITS	System level coordination	Traffic management
CCAM	Automated mobility application	Self driving car
V2X	Communication technology	Shared messages between entities

Table 1.1: Conceptual overview of C-ITS ecosystem

Successful outcome of C-ITS integration strongly depends on the number of vehicles and objects equipped with units featuring interfaces compatible with vehicular communications. To achieve this, organizations adopt cooperative strategies to ensure coherent and coordinated deployment [2]. Different funding programs are currently active in Europe [3], targeting both infrastructure improvements and research breakthroughs.

1.1 Vehicular communications

Vehicular communications refer to information exchange involving vehicles. They include both in-vehicle interactions and external communications enabled by V2X technologies.

Vehicle-to-Everything (V2X) describes a subset of vehicular communications implemented via wireless connection. Its purpose is to allow interactions between the vehicle and the surrounding environment; meaning among any entity that may affect or may be affected by the vehicle. This technology is developed as part of C-ITS and relies on WLAN and cellular networks infrastructure.

As a result, vehicles can interact with other vehicles, infrastructure, people, bicycles and networks, acquiring so the capability to know ahead even without visibility. This implies that means of transport equipped with V2X can see around corners and beyond any obstruction across a one mile radius; it constitutes a significant technological breakthrough.

Applications for connected vehicles consist of data acquisition from sensors, information transfer and processing, as well as end-user interface aspects. Focusing on the information transfer component, different communication modes of V2X exist and are classified according to the target entity participating in the interaction.

Some types of communication involved in V2X applications are listed below:

- Vehicle-to-Vehicle (V2V): vehicles send messages to other vehicles via On-Board-Units (OBUs);
- Vehicle-to-Infrastructure (V2I): vehicles send messages to the infrastructure and vice-versa, specifically to Road-Side-Units (RSUs);
- Vehicle-to-Pedestrian (V2P): vehicles send messages to pedestrians or bicycles, i.e., Vulnerable Road Users (VRUs), and vice-versa;
- Vehicle-to-Network (V2N): vehicles exchange messages with an application server in the network.

Vehicle interactions with road infrastructure are enabled by the use of Road-Side-Units (RSUs), identified as communicating nodes in the connected vehicles environment. The RSU is a transceiver that links vehicles to infrastructure. It is installed in designated areas alongside roads, collects traffic data and transmits information to a local server. Meanwhile, vehicle to vehicle communication is carried out by means of On-Board-Units (OBUs) installed on vehicles. The OBU is a hardware platforms that implements wireless connectivity and handles signaling, providing interfaces and processing power to let the vehicle engage in V2X communications.

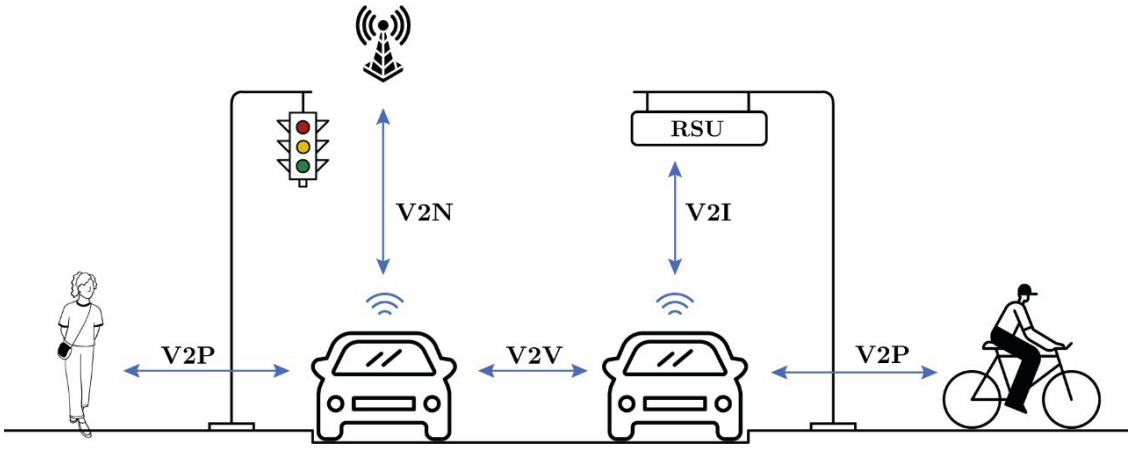


Figure 1.1: Sketch of a V2X system. Adapted from *Phenikaa X Joint Stock Company.*

It follows that V2X sets out to resolve two main problems: safety and mobility. Secure exchange of speed, position, acceleration and travel direction data, provides the

means to create applications, such as collision alert, hazards warning, and to notify the driver of any other danger in the path. Therefore, accidents can be dramatically reduced. Risk associated to heavy machinery use in construction sites is mitigated, motorcyclists are safeguarded with prompt warnings of nearby hazards and off-road drivers rescue operations are facilitated, despite being in rough terrain areas where cellular service is often not available. Furthermore, exploiting V2X to control the vehicle's speed, mobile nodes can coordinate their maneuvers as to avoid traffic jams and synchronize themselves to drive through a green wave. Moreover, V2X is essential for large scale deployment of autonomous vehicles since it extends the limited perception of onboard sensors. It is of utmost importance in poor lighting conditions and rough weather, complementing information coming from line-of-sight sensors.

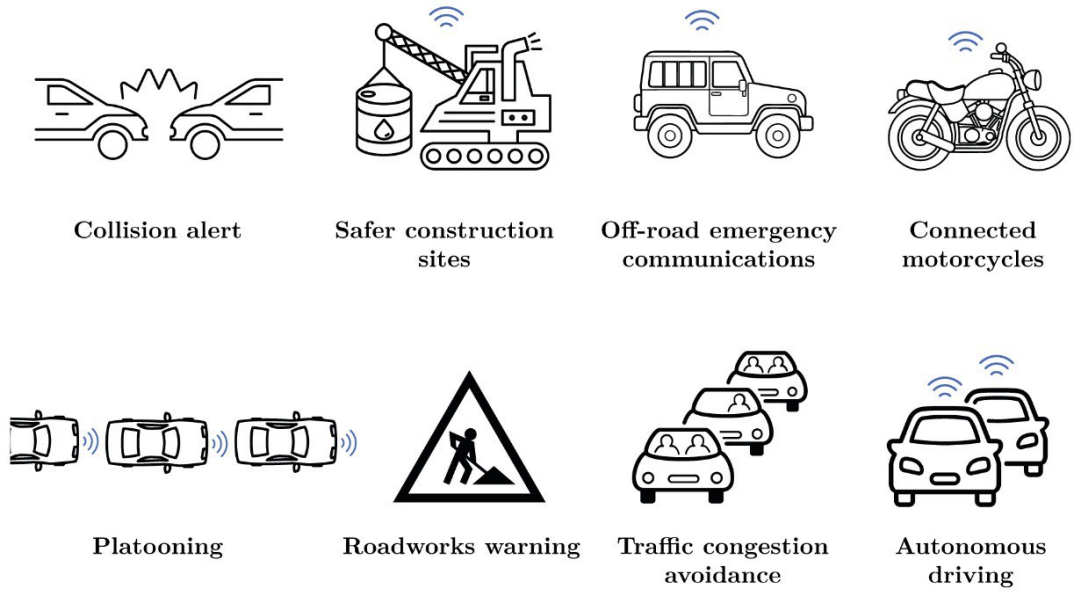


Figure 1.2: Several V2X use cases. Adapted from *Nexus Group*.

1.1.1 Regulatory Bodies, Standards and Protocols

The aforementioned communication types of V2X, rely on standards and protocols developed by international organizations. These include the European Telecommunications Standards Institute (ETSI) [4], the Institute of Electrical and Electronics Engineers (IEEE) and the 3rd Generation Partnership Project (3GPP) [5]. They provide guidelines to implement the underlying technology and define message format in order to support interoperability across devices.

On the other hand, regulatory bodies such as the European Commission and the Federal Communications Commission (FFC) in the United States, hold legal authority and enforce rules related to operational conditions such as defining spectrum allocations.

Dedicated Short Range Communications Early V2X communication used only Wireless Local Area Network (WLAN) technology, forming a vehicular ad hoc network based on V2V and V2I information sharing, once two senders are in range. This ensures communication in remote areas where no platforms other than the vehicles' OBUs and infrastructure RSUs are present. Standardization at the physical level of WLAN based V2X was handled by IEEE who first published 802.11p, an amendment of 802.11 [6] that adapts the wireless standards to vehicular communications. It operates in the licenced ITS band of 5.9GHz, referred to as the Dedicated Short Range Communications (DSRC) band. Higher layers definition differs according to region, resulting in specific stacks built on the same underlying access technology defined by IEEE. In Europe, the ITS protocol stack with ITS-G5 access [7], specified by ETSI, is adopted; meanwhile, Wireless Access in Vehicular Environments (WAVE) is its counterpart in the United States, which incorporates IEEE 802.11p for the physical layer and IEEE 1609.x protocols for higher layers.

Cellular V2X As commitment towards innovation of ITS solutions grew, V2X started evolving into Cellular V2X (C-V2X), a technological branch that leans on the existing cellular infrastructure. It faces the drawbacks encountered in 802.11p commercial deployment since it did not progress as expected. C-V2X is defined by 3GPP in Release 14/15 as LTE-V2X and was later upgraded to 5G-V2X, from Release 16 onward [8]. The second generation version offers higher speed and lower latency, as it is based on 5th generation New Radio (5G NR) technology. It's important to specify that two cellular communications interfaces are defined for C-V2X. Both of them can be employed for communications based on either LTE or 5G technologies. The interfaces in question are the PC5 for direct communications and the Uu for mobile networks communications. The PC5, also known as sidelink, uses device-to-device communications without requiring the presence of a base station. It enables V2V, V2I, V2P communication, and it's ideal for low latency and safety critical applications. On the other hand, the Uu interface relies on the cellular network infrastructure to connect end users and vehicles to base stations, providing V2N services over a wide range. Hence, the two interfaces complement each other and address the trade off between maximum communications range and response time.

The two implementations are not interoperable at the access layer and are used in conjunction to augment V2X capabilities. Aside from this, they have identical application layers and use cases. The standardization efforts and resulting protocol stacks, are summarized in Table 1.2.

Communication type	Region	Protocol Stack	Access Layer	Standardization Body
DSRC	Europe	ITS-G5	802.11p	ETSI / IEEE
	U.S.	1609.x	802.11p	IEEE
Cellular V2X	Global	C-V2X	LTE/5G NR	3GPP

Table 1.2: V2X protocol stacks and access layers

1.2 On Board Units

As mentioned before, V2X communication, on the vehicle side, relies on specific hardware platforms that provide the necessary interfaces and processing power to enable vehicular connectivity. On-Board-Units are developed for this purpose.

These units manage both internal and external vehicle communications: once a message is received through a V2X link, the OBU acts as an actuator and notifies the vehicle's internal Electronic Control Unit (ECU). For instance, upon receiving a collision alert via V2X data exchange, the OBU transmits this information to the ECU which will trigger the braking system and prevent impact.

Hence, they are built for transmitting, collecting and storing data. Additionally, they often rely on external hardware components to enhance connectivity, such as cellular modems (usually connected through a miniPCIe adapter), GPS/GNSS receiver for real time positioning and CAN bus for interfacing various sensors and ECUs.

1.2.1 Commercial OBUs

With the intention of understanding technological and functional challenges of OBU devices, available solutions in the commercial market are briefly analyzed. Table 1.3 displays some V2X products listed by companies. Most of these manufacturers offer multiple solutions in the vehicular communications sector, spanning from chipsets and modules to standalone hardware platforms such as OBUs and RSUs.

The product list showed, is based on a cross reference of the latest technical report of C-V2X devices by 5GAA Automotive Association [9], its marketplace website [10] and online research. The 5GAA Automotive Association is an organization of companies in the automotive and telecommunications industries that contributes to the development of ITS solutions.

For simplicity, the table does not distinguish between products supporting PC5 sidelink and Uu connection types, hence the reader is advised that the classification is more complex than illustrated, since the aim is to give a brief overview of commercial products.

Moreover, only products supporting DSRC 802.11p at the physical layer are marked as DSRC compliant, given that it's important to differentiate between devices able to process direct messages using 802.11p radio and the ones that support only the 1609.x protocol stack for DSRC but use Cellular V2X LTE or 5G as underlying technology. In particular, the MobiQ 5931 OBU features this characteristic.

Although the solutions hereby outlined are commercial products, it is worth mentioning a platform developed for research purposes in this field: the LINKS V2X OBU [11]. It is used for advanced CCAM applications testing and supports both DSRC and C-V2X connectivity.

Table 1.4 presents a hardware comparison of products with accessible documentation listed in table 1.3. Fields are left empty if no information is provided. Available solutions proposed by manufacturers in this sector are rapidly evolving, companies are acquired (Cohda Wireless is now part of Danlaw [12]; Lacroix has been incorporated by the Austrian company Swarco [13]), some products are phased out and replaced by more

profitable solutions (Harman Savari mobiWAVE OBU has been superseded by Ready Connect Telematics Control Unit [14]).

Company	OBU	Market	DSRC	C-V2X LTE	C-V2X 5G
Cohda Wireless	MK5 [15]	Global	✓	✗	✗
	MK6 [16]	Global	✓	✓	✓
Commsignia	ITS-OB4 [17]	EU/US	✓	✓	✓
Chemtronics	Hybrid OBU [18]	US/KOR/CHN	✓	✓	✗
Danlaw	AutoLink [19]	US	✓	✗	✗
			✗	✓	✗
CICTCI	VU4105 [20]	CHN	✗	✓	✓
Cradlepoint	Ericsson R1900 [21]	Global	✗	✓	✓
DENSO	MobiQ [22]	Global	✗	✓	✗
Ettifos	THEUS OBU [23]	Global	✓	✓	✗
RANiX	RXV200 [24]	Global	✓	✓	✗
Askley	5G OBU [25]	EU/US/CHN	✗	✓	✓
CTAG	HMCU-OBU [25]	EU	✓	✓	✗
Company	**Chipset**	**Market**	**DSRC**	**C-V2X LTE**	**C-V2X 5G**
Qualcomm	C-V2X 9150 [26]	Global	✗	✓	✗
Autotalks	CRATON2 [27]	Global	✓	✓	✗
	TEKTON3 [28]	Global	✓	✓	✓
Company	**Module**	**Market**	**DSRC**	**C-V2X LTE**	**C-V2X 5G**
Unex	SOM-301 [29]	Global	✓	✓	✗

Table 1.3: Widely known embedded solutions for V2X applications

Essential hardware features that allow classification of an embedded board as OBU are V2X radio, Global Navigation Satellite System (GNSS) and in-vehicle communications (Controller Area Network and Automotive Ethernet) interfaces. Most of the listed boards come with a rugged enclosure, which is critical in automotive environments where dust, vibrations and extreme temperatures must be withstood. The core processor adopted is common to all cases, manufacturers opt for either a NXP System-on-Chip based on the ARM Cortex or simply a standalone ARM CPU. It is worth noting that platforms which employ the NXP processor use Linux as operating system, while the ARM based systems rely on proprietary software. Storage is often limited to the embedded Multi Media Card (eMMC), though sometimes external storage solutions are supported such as microSD slots or USB flash drives. Ethernet ports are a must, in fact they provide a high speed, reliable connection for both in-vehicle and external communications. Additional interfaces are Wi-Fi, Bluetooth, USB and serial, which complete the connectivity of the

board. Some OBUs are equipped with audio inputs and HDMI video output, as well as additional GPIOs for expansion. Power input to the board always complies with automotive applications, the voltage range is often wide or simply matches the common 12V supply of standard vehicles. Multiple antennas connectors are always present, seeing as they are necessary to reliably send and receive wireless signals for Wi-Fi, Bluetooth, V2X radio and GNSS.

	MK5	**MK6**	**ITS-OB4**	**Hybrid OBU**	**AutoLink**	**R1900**	**MobiQ**	**THEUS**	**RXV200**	**5G OBU**	**HMCU-OBU**
Core	NXP i.MX6	NXP i.MX8	NXP i.MX6	ARM A9	-	ARM v8	ARM	NXP i.MX8 Plus	ARM A7	-	NXP i.MX6
OS	Ubuntu	Debian	Linux	Prop.	Prop.	Prop.	Prop.	Linux	Linux	-	Linux
RAM	1G	1G	2G	1G	1G	1.8G	-	4G	1G	2G	1G
eMMC	4G	16G	4G	8G	8G	6G	-	16G	8G	16G	4G
Storage	4G	uSD	uSD	uSD	-	-	-	-	-	-	-
Ethernet [bps]	100M	1G	1G	1G	✓	1G	✓	✓	1G	1G	1G
Power [V]	7-36	7-36	-	12/24	12/24	9-36	12	7-36	12	-	8-16
GNSS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Wi-Fi	✗	✓	✓	-	✓	✓	-	✓	✓	✓	✓
Bluetooth	✗	✓	✗	-	✓	✓	-	✓	✗	✓	✓
DSRC chip	NXP Road-link	NXP Road-link	-	-	-	-	-	-	-	-	-
C-V2X chip	✗	SA515	-	-	-	-	-	SA515M	CX1860	-	-
USB	✗	✓	✓	✓	✓	✓	✓	✓	✓	✗	✓
CAN	✗	✓	✓	✓	✓	✗	✓	✓	✗	✓	✓
Automotive Ethernet	✗	✓	✗	✗	✗	✗	✗	✗	✗	✗	✗
Serial	✗	✗	✗	✓	✓	✓	✓	✓	✓	✗	✗

Table 1.4: Hardware comparison of commercial OBUs with accessible documentation

Security and certification is a key aspect in OBU design. When handling safety critical data it is essential to certify the board to ensure automotive standards and V2X radio specifications are met. This is quite expensive, since hardware, software and radio interfaces must all be tested for standard conformance.

Adopting standalone pre-certified chips or modules is an important breakthrough for OBU design: it allows seamless integration of security and radio compliant, ready to use devices in the hardware platform. Doing so, time and costs associated with obtaining the

certification are dramatically reduced, focus is shifted on the actual board design neglecting the V2X radio interfaces and lastly, automotive and V2X compliance is guaranteed due to the integration of an already certified module.

These modules are extremely versatile and can be exploited as self contained V2X SoM in OBUs as well as RSUs, Telematics Boxes and Network Access Devices.

An example is the Unex SOM-301 module that integrates the Autotalks CRATON2 communication processor and the PLUTON2 V2X/WLAN transceiver. It is designed to specifically address the rising demand for easy to use V2X units in connected vehicles. The form factor matches the PCI Express Mini Card (miniPCIe) standard and the host interface required is the USB 2.0 interface. The module relies on Linux operating system and requires both 3.3 V and 5 V voltages to function (compliant with the supply defined by miniPCIe standards).

These V2X System on Modules with miniPCIe form factor confer remarkable architectural flexibility and interoperability. They can be easily swapped with other modules to expand the board's functionality or support different communication standards, thus leading to a scalable and future proof final platform.

1.2.2 Challenges and Gaps

A binding disadvantage of commercial V2X hardware solutions proposed by industries, is the non disclosure of information related to both hardware and software employed. As a consequence, customization efforts are vain since proprietary designs defy any modification and must be used as is. In addition to this, high costs are a major factor, especially when taking into account the limited customization options and the rapidly evolving market where a product could be easily discontinued and its software support may be ceased.

Open source platforms, not only allow a high degree of customization, transparency and community support, but also facilitate the adoption of V2X devices improving interoperability . More connected devices across the network grant V2X applications access to larger amounts of real time information, thereby reaching higher success rate, accuracy and efficiency.

Taking this into consideration, the connected vehicle ecosystem demands for a low cost, open source hardware platform, interoperable, reliable, with low latency and multiple interfaces support.

1.3 Thesis objective

This thesis outlines the design methodology and implementation of an embedded board for vehicular connectivity that can easily be installed on non-connected vehicles. The aim is to propose an open source OBU that answers to the lack of customization, limited number of connectors and plug-in slots for connectivity modules on commercial platforms. The board is compatible with Linux-based systems filling the gaps illustrated in the previous section. Radio interfaces are supported arranging multiple miniPCIe slots that will accommodate self contained V2X System on Modules, thus avoiding complex

certification requirements, granting flexibility and adaptability with respect to evolving standards.

1.4 Document structure

A brief overview of the contents discussed in this documents is provided below. The aim is to guide the reader through the understanding of all design choices that were made to accommodate specific needs and how the final platform was implemented, starting from a set of specifications, moving on to hardware components selection and printed circuit board layout up to component placement.

- **Chapter 2:** focuses on pen and paper design which consists in refining the specifications, drafting the system architecture and selecting components;
- **Chapter 3:** schematic implementation is described and main design choices are thoroughly investigated;
- **Chapter 4:** covers the PCB aspects, stack-up and design rules, footprint layout, enclosure selection and details on the complete platform.

Chapter 2
Concept to hardware architecture definition

First and foremost, it is essential to lay out the groundwork for board development using a pen and paper approach. This chapter covers the description of several steps that led from the initial concept to the architecture of the hardware system.

A substantial part of the design process thus includes specification refinement, high level architecture draft and components selection. Ultimately, the components list and final block diagram are obtained, which serve as foundation to set up the schematic design in KiCad.

2.1 Specification Refinement

The initial concept is built on a set of specifications pertaining processor performance, storage, connectivity, power supply and thermal management. Acting as a starting point for drafting the design, these features are not definite at this time, thus they are considered minimum requirements that should be met to attain performance levels demanded by the end user.

Raw specifications are summarized as follows:

- **Processor:** embedded CPU, quad-core 1 GHz equivalent or better, Linux compatible;
- **Memory:** 2 GB minimum, 4,8 GB of RAM is preferred ;
- **Storage:** either SD card or SSD (SATA or PCIe interface);
- **I/O** two USB 3.0 connectors, one DB9 serial port (for debug and installation purposes), optional video output, multiple GPIOs (for additional sensors), three LED (status indicators and debug diagnostics), power on bi-stable switch , optional programmable buzzer;
- **Power supply** 12 V (passenger vehicles) or 24 V (heavy duty vehicles) DC input voltage, coin cell battery and at least two exposed 5 V power pins;
- **Connectivity** minimum two Gigabit Ethernet RJ45 connectors, one Automotive Ethernet 1000BASE-T1, a CAN transceiver, Integrated Wi-Fi chip supporting up to IEEE802.11ac (Wi-Fi 5) or IEEE802.11ax (Wi-Fi 6), three miniPCIe or PCIe slots (for expansion cards: vehicular Wi-Fi - without SIM slot, cellular network - mandatory SIM slot, C-V2X - optional SIM slot);
- **Thermal management and cooling system:** passive cooling strategy (avoid dust, less susceptible to vibrations).

The first task involves polishing these specifications, in particular the ones regarding connector types and their respective interfaces. To illustrate, at this stage Type-A

connectors for USB interfaces and a DB9 connector for the Controlled Area Network transceiver are chosen, while the DB9 debug port is set to support UART communications over RS232 interface. The selected storage solutions include the embedded Multi Media Card, an SD card slot and an M.2 Next Generation Form Factor (NGFF) slot for an SSD with PCIe interface. Featured video output type is the High Definition Multimedia Interface (HDMI), aimed at being mostly used in a lab setup environment. All optional specifications are implemented to grant more flexibility. In addition, a reset pushbutton is included as well as SMA antenna connectors, mounted on the enclosure and connected via cable to the U.FL coaxial connector on miniPCIe radio modules fastened to their dedicated slot.

A sketch is drawn to help visualize the board concept, figure 2.1.

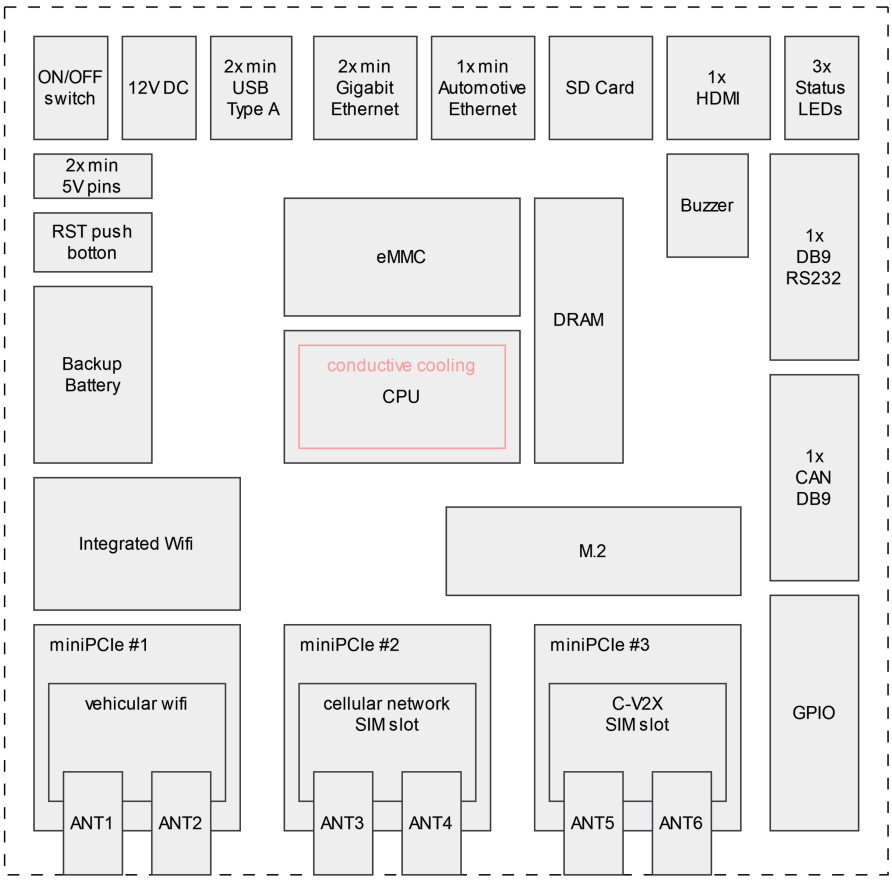


Figure 2.1: Board draft conceptual diagram with minimum requirements

Once this minimum requirements conceptual draft is completed, focus is shifted to the core processing element and memory subsystem.

2.1.1 Core processing module: SoM selection

To simplify the design and maintain high reliability, a System on Module is adopted as embedded processing unit. Doing so, design complexity and error probability are dramatically reduced. Intricate high speed routing for DDR memory and CPU interface is avoided in conjunction with signal integrity challenges. Moreover, System on Modules help minimize development efforts thanks to pre-installed boot loaders and drivers on top of vast OS support resources. Moreover, they often embed components and subsystems such as eMMC, Wi-Fi chipsets and power management circuitry, in addition to CPU and RAM. The compact form factor makes system integration effortless and having an already validated and certified module, stability is already guaranteed under operating conditions.

Considering the previously listed requirements and application conditions, the module selected for this role is the DART-MX8M-PLUS by Variscite [30], which relies on the NXP i.MX 8M Plus System on Chip (SoC). It is worth noting that this specific SoC, as well as others from the same family, are employed in several commercial OBUs as highlighted in table 1.4.

The DART-MX8M-PLUS module is built to provide high performance while maintaining power consumption low. The set of NXP products family is the first with machine learning and artificial intelligent accelerators, making it ideal for security and time critical tasks. Product longevity is guaranteed for a 15 year period until 2036, with continuous software updates and support. Among other OSs, the module can also operate with Yocto built distributions. The Yocto project is an open source collaboration that provides tools and processes to create custom Linux-based systems in the embedded and IoT sector, regardless of the hardware architecture. The module is available in both commercial and industrial temperature range versions and Linux OS support is widely accessible through the dedicated development wiki page [31].

Main Features of the DART-MX8M-PLUS SoM are briefly mentioned in the following:

- **NXP SoC:** i.MX 8M Plus Quad core Cortex-A53 and Real Time 800 MHz Cortex-M7 co-processor;
- **Memory and storage:** configurable up to 8 GB RAM, 128 GB eMMC for high volume orders;
- **Embedded subsystems:** Dual band Wi-Fi 5 and Bluetooth/BLE 5.2 or Wi-Fi 6 and Bluetooth/BLE 5.4 (V2), Ethernet, Audio Codec;
- **Interfaces:** Display (LVDS, HDMI, MIPI DSI), Ethernet, Camera, Audio, PCIe, USB, serial (ECSPI, FlexSPI, I2C, UART, CAN, JTAG), SDIO/MMC, GPIO, PWM, timers;
- **Supply voltage:** 3.4 V - 5 V;
- **Boot loader and OS:** module comes preloaded with Linux U-boot, compatible with Yocto build distributions.

Variscite also offers a specific heat sink [32] tailored for the DART SoM family, which is consistent with the passive cooling strategy adopted in the current design.

Four hardware configuration options are selectable for single unit purchase. These include version 1 or version 2 of the SoM respectively with Wi-Fi 5 and Wi-Fi 6, both available in commercial and industrial temperature range. The configuration chosen for this design is version 2 with industrial temperature range. Table 2.1 shows the selected SoM ready for purchase set up.

DART-MX8M-PLUS V2 SoM	
CPU NXP i.MX 8M Plus	1.6 GHz Quad core Cortex-A53
Real Time co-processor	800 MHz Cortex-M7
RAM	4 GB
Storage	16 GB eMMC
Integrated Wi-Fi and BT	V2: Wi-Fi 6 802.11ax, 5.4 BT (V1: Wi-Fi 5 802.11ac, 5.2 BT)
Boot loader	SoM preloaded with Linux U-Boot
OS support	Yocto, Debian, Boot2Qt; Android; FreeRTOS; QNX
Boot sources	Internal: eMMC; External: SD card
Temperature range	Industrial: $-40°C$ to $85°C$
Dimensions	55.0 × 30.0 mm
Cost	169$

Table 2.1: DART-MX8M-PLUS V2 ready for purchase hardware configuration

2.2 Architecture Draft

Having established the minimum system requirements and chosen the core processing unit, the design is carried out analyzing how to combine the downstream connectors to the upstream SoM interfaces. The aim is to identify any mismatch in number between the upstream SoM interface outputs and downstream ports required by the specifications. When mismatch is found, it is addressed with the insertion of a Hub or switch Integrated Circuit (IC) so as to adapt the number of data interfaces to the number of available connectors on the board.

Furthermore, a DC-DC converter is picked out to step down the 12 V - 24 V input supply to 5 V and, once all the main ICs are selected, the power distribution is drafted and on board buck converters are identified. Final specifications, block diagram, a list of ICs and passive components are ultimately extracted as they define the baseline for schematic design. It should be noted that during the schematic implementation, minor adjustments will be made.

2.2.1 Interfaces

Integrated Circuits selection is described in this section. Only interfaces that do need a PHY or a switch are highlighted, further information will be provided in the next chapter. In Ethernet communications, the physical layer transceiver is often referred to as PHY, it is a dedicated IC that converts data from the Media Access Control (MAC) interface into

electrical signals, matching the transmission requirements that suit the physical medium. MAC and PHY are part of the data link layer and are typical in communications interfaces such as Ethernet. Hence, the MAC is tasked with managing access to the communication medium (frame transmission, addressing and error detection), while the PHY takes care of signal conversion at the electrical level. This terminology is typically used specifically for Ethernet, other communications interfaces still employ a physical transceiver but the second layer in the structure is referred to as a controller.

Some physical transceivers and controllers are already embedded in the SoM, namely one Ethernet PHY, USB and PCIe.

USB

The Universal Serial Bus is serial communication standard [33] that enables data exchange between host controller and peripherals. The latest generation of the standard is the fourth, while the SoM integrates generation 3.0 and 2.0 controllers. Each one supports a different signaling rate, 5 Gbit/s Super Speed for the USB 3.0 controller and 480 Mbit/s High Speed for USB 2.0. The interface signals consist in one bidirectional differential pair of data lines (High Speed), one transmit and one receive unidirectional differential pairs (Super Speed).

The SoM supports only two controllers with PHYs, thus a Hub IC is selected to adapt the host interface to the downstream ports needed. Two USB Hubs are employed to support eight different PHYs for four USB ports and four miniPCIe slots, starting from two host controllers on the SoM, as depicted in figure 2.2.

The four miniPCIe slots provide both USB 2.0 and PCIe buses to the add-in modules, in accordance with the miniPCIe standard [34]. Most Wi-Fi miniPCIe modules require USB 2.0 interface, as they employ Wi-Fi chipsets originally developed for USB dongles. For basic Wi-Fi 5 connectivity, the data rate theoretical speed does not exceed the 480 Mbit/s USB 2.0 speed limit, hence PCIe high speed interface is not necessary. To guarantee flexibility, all four miniPCIe slots on board support both interfaces. In order to accommodate a specific miniPCIe module with non standard pinout, USB 2.0 signals routed to the fourth miniPCIe slot are deviated to a 20-pin header meant for Flat Flexible Cable (FFC) connection, using a multiplexer picked out from a family made especially for this application, thus granting bandwidth compatibility and signal regeneration. Doing so, the integration of a non standard miniPCIe slot is avoided, while having the possibility to operate the module through the use of a dedicated adapter.

As for USB connectors instead, three USB Type A up to 5 Gbit/s and one USB Type C up to 480 Mbit/s ports are included. Battery charging (BC) capability is featured by only two ports, one Type A and one Type C. This functionality can be activated on a single port at the time using a DIP switch, preventing current overload.

The selected USB Hub is the USB5744 [35], High speed 4 ports Hub controller IC by Microchip. It supports both USB 3.0 and 2.0 signaling speeds at the same time, in addition to port power controllers. Customization is possible through bus communications or simply via resistor straps. Industrial temperature range version is available and it comes in a 56-pin Very thin Quad Flat No-lead (VQFN) package. This package type has a low profile and good thermal performance due to the exposed thermal pad underneath the

IC, that allows for direct heat transfer to the printed circuit board. Pin pads are on the bottom side of the package, which results in improved signal integrity on account of lower parasitic resistance and inductance with respect to package types where traces from pins to PCB are longer.

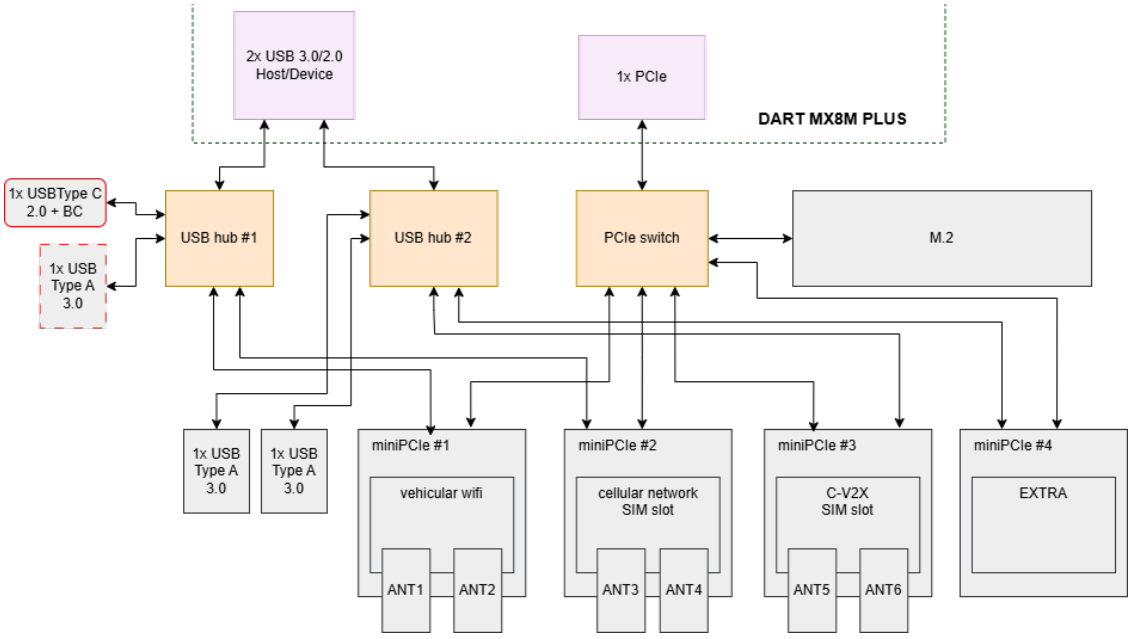


Figure 2.2: Block diagram detail: USB and PCIe interfaces

PCIe

Peripheral Component Interconnect Express (PCIe) is an industrial standard for high speed communication of hardware components inside a computer. It replaces the old PCI bus interface and it's developed by PCI Special Interest Group (PCI-SIG) [36]. Each device has a dedicated connection to the host (point-to-point), data transmission is serial and is implemented with two complementary signals: when the voltage difference between the two crosses zero, data is detected, enabling precise timing even at high speeds. The topology consists of a differential pair interconnect between two devices, with a transmitter on one side and a receiver on the other. Each connection is based on two differential pairs, one intended for transmitting data and the other dedicated to its reception; this couple of differential pairs is identified as lane. Multiple lanes grouped together and connected to a single port are referred to as link, figure 2.3. Links may have different width based on the number of parallel lanes they consist in. Synchronization between transmitter and receiver is enabled by sharing the 100 MHz differential reference clock between devices.

The DART SoM supports a single lane Gen 3.0 8 Gb/s interface, including three differential pairs (transmission, reception and reference clock). The board accommodates 5 connectors supporting PCIe interface, hence a switch is employed to adapt the single

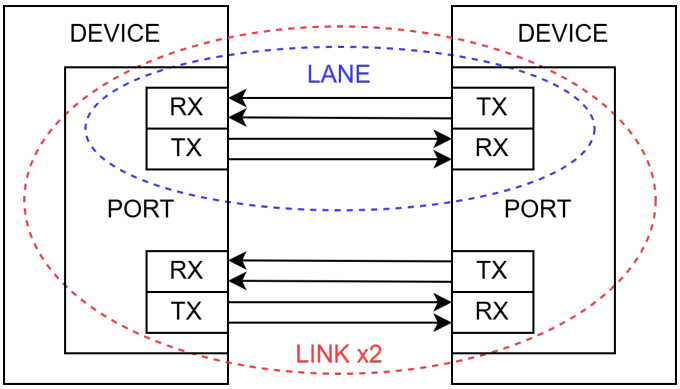


Figure 2.3: PCI Express link concept. Adapted from *Board Design guidelines for PCI Express interconnect, PCI-SIG Developers Conference.*

upstream lane to five downstream ports, each with single lane routing. A 6-port, 6-lane, PCIe 3.0 Packet switch by Diodes Inc. [37] is selected, it manages the reference clock integrating buffers for all downstream ports as well as PHYs. Is is programmable via several interfaces and it comes in a 144-pin Ball Grid Array package (with ball pitch 0.8 mm which allows enough routing clearance).

The system then comprises four miniPCIe slots and one M.2 slot all equipped with single lane routing, all interfacing the same switch figure 2.2. The M.2 slot is reserved for an SSD which will be mostly used for data logging, hence no bandwidth limitations are expected even in the worst case scenario where all links are active. The M.2 card follows a different set of specifications with respect to the miniPCIe modules, though still developed by the same organization [38].

The switch employed does support module hot plugging, but the option has not been enabled. Consequently, the user must restart the board to reestablish the connection once the add-in cards are swapped.

Ethernet

Ethernet is a wired computer networking technology frequently used in Local Area Networks (LAN) and Wide Area Networks (WAN). It is implemented in the data link and physical layers (layer 1 and 2 of the Open Systems Interconnection model [39]) and defined by the IEEE 802.3 specification [40]. With this technology data rates up to the gigabit range can be achieved over a distance of 100 m or even more if fiber optic cables are used as physical medium. Several transmission speeds and physical media interfaces exist, Ethernet families are thus identified according to the following naming convention:

$$< BitRate >< Signaling > - < Medium >< PCSEncoding >< \#Lanes >$$

To illustrate, the 1000BASE-T family name indicates a 1000 Mb/s interface with baseband signaling over twisted pair medium and blocked encoding as bit encoding scheme. This family type requires a 4-pair Category 5 unshielded twisted copper pair cable and is the one implemented in the designed board.

Ethernet PHY is divided into two main domains: Medium Independent Interface (MII) and Medium Dependent Interface (MDI). The MII comes in different variants according to speed and pin count supported, it interfaces directly with the MAC of the host device. On the other hand, the MDI connects two devices over a physical media and it is considered as the analog section of the PHY, in contrast with the MII that works in the digital domain.

The MAC to PHY connections in this design are done exploiting the Reduced Gigabit MII (RGMII) which supports speeds up to 1000 Mb/s and has a low pin count.

The DART SoM supports two controllers capable of simultaneous operation, one of which comes with an integrated PHY. The MAC interface corresponding to the integrated PHY supports both Time Sensitive Networking (TSN) and Energy Efficient Ethernet (EEE), as well as Audio Video Bridging (AVB) and the IEEE 1588 time stamping module for clock synchronization, in addition to Quality of Service (traffic prioritization), after which is labeled. Thus, the ENET_QOS RGMII signals are connected internally on the SoM while magnetics and connectors are implemented on the carrier board. The second MAC, labeled as ENET1 in figure 2.4, is directly exposed on the SoM connectors. The corresponding RGMII signals are routed to a switch equipped with an additional RGMII interface, essential for implementing the Automotive PHY connection. Selecting an appropriate switch for this application, not only allows integration of additional Gigabit Ethernet ports with respect to the ones supported by the SoM, but also simplifies integration of the Automotive PHY.

The KSZ9567 7-Port Gigabit Ethernet Switch [41] by Microchip with five integrated PHYs and two MACs, was chosen for this design. In order to accommodate a second RGMII interface, this 7-Port switch is adopted and additional unused ports are left unconnected. It supports all features previously listed, hence its performance easily matches the one of the SoM integrated PHY.

Automotive Ethernet

Automotive Ethernet is used for in-vehicle communications, specifically to connect different ECUs. It was initially introduced to address the requirements increase both for infotainment and multimedia applications as well as higher data rates of sophisticated sensors and actuators for autonomous driving. Being a subset of Ethernet systems, it's standardized by the same IEEE 802.3 [40] specifications, though anther organization comes into play to promote its widespread adoption in the automotive industry: OPEN Alliance [42], a collaboration of mainly automotive industry that encourages adoption of Ethernet as a standard in networking applications. Automotive Ethernet follows a point-to-point topology approach, hence only two devices can be connected with a single cable. The aim is to keep the vehicle as light as possible, since multiple cables are needed to connect different sensors and ECUs. For this purpose Automotive Ethernet uses only a single twisted pair with respect to the four pairs used in standard Ethernet. They implement the same higher layer protocols but are not interchangeable at the physical level. Moreover, the communication distance is far lower than the one supported by standard Ethernet (around 15 m for passenger vehicles and 40 m for heavy duty ones).

As previously mentioned, the Automotive PHY is connected to the Ethernet switch via

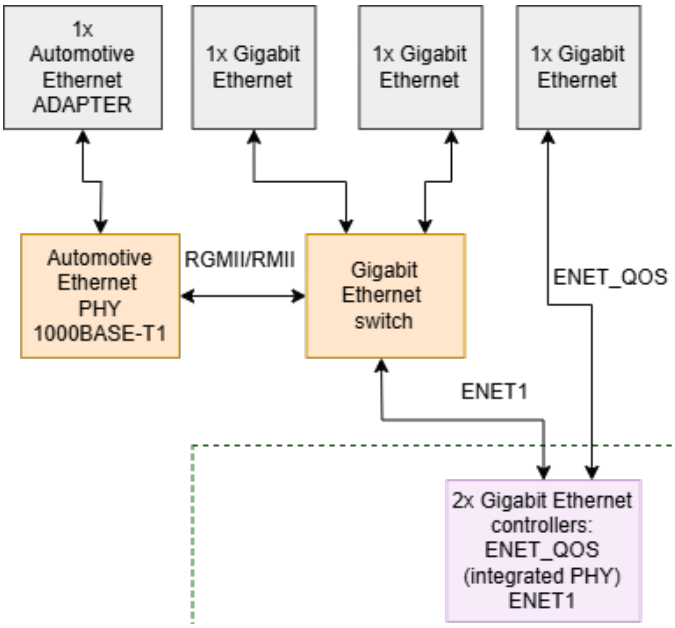


Figure 2.4: Block diagram detail: Ethernet interface

RGMII interface. The selected PHY is the DP83TG721R-Q1 [43] by Texas Instruments. It supports the technology family 1000BASE-T1, requiring only a single twisted pair. Its distinctive features are 802.1AS [44] support and AVB Clock generation. The first is an adaptation of IEEE 1588 Precision Time Protocol (PTP) for real time communications and allows highly precise time synchronization between the connected devices. It is essential for Advanced Driver Assistance Systems (ADAS) and V2X critical applications, since it guarantees deterministic latency and time synchronization. On the contrary, AVB alone is suited for multimedia and infotainment systems as well as basic communications.

Regarding the Automotive Ethernet port, several connectors types can be found in the commercial market; most manufacturers offer their own proprietary solution like the H-MTD by Rosenberger [45] and MATEnet by TE Connectivity [46]. Compatibility between these connectors it not at all guaranteed; as a consequence, designing a board interoperable with devices developed by different vendors is extremely challenging. To address this problem, a common RJ45 connector is used as Automotive Ethernet port, leaving unconnected the pins reserved for the 3 twisted pairs not used by the Automotive standard. Doing so, flexibility is maintained and if a connector is standardized in the future a simple adapter to the RJ45 will grant compatibility.

CAN

The high speed serial communications international standard for using the Controller Area Network bus protocol is the ISO 11898 [47]. Supporting programmable data rates up to 1 Mbps, real time control and multimaster operation, it is well suited for sensors and actuators in rugged electrical environment as the automotive one.

The DART SoM includes a Flexible Controller Area Network (FLEXCAN) supporting

both CAN-FD (flexible data rate) and CAN 2.0B. An external transceiver is integrated on the carrier board, figure 2.5. The SN65HVD232 [48] operates in the common mode range of -2 V - 7 V and common mode transients are withstood up to ±25 V. Signals interfacing with the CAN bus transceiver are only two, one for transmission and the other for reception. The transceiver output is attached to the bus lines CANH and CANL through the DB9 port with the insertion of a 120 Ω termination resistance to comply with the standard and minimize signal reflections.

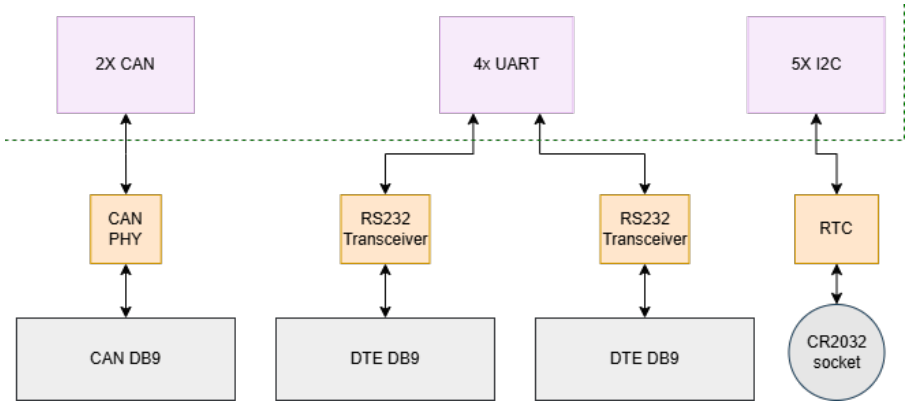


Figure 2.5: Block diagram detail: CAN, RS232 interfaces

RS232

RS232 is a point-to-point communication interface that enables communication between a host and a peripheral. The bus is full duplex, meaning that it receives and transmits data at the same time. The transmitter logic level ranges from -15 V to -5 V for a logic one and from +5 V to +15 V for a logic zero. On the other hand, the receiver sensitivity is ±3 V. The standard defines a Data Terminal Equipment (DTE) and a Data Communication Equipment (DCE). Devices in DTE configuration act as host and controller while in DCE they would be considered as peripherals. The four signals involved in the communication are labeled as TXD (from DTE to DCE) and RXD (from DCE to DTE) for data signals, RTS (Ready to Send) and CTS (Clear to Send) for control signals.

As illustrated in figure 2.5, two DB9 ports are dedicated to RS232 communication, this way one port is always available to engage in serial communications while the other is tasked with debugging. The TRSF3232E [49] is picked out as transceiver converting the UART signals outputted by the SoM into ones compliant with electrical levels specified by the RS232 standard.

2.2.2 DART SoM pinout mapping

Ultimately, the SoM pinout and pinmux table attached to the documentation provided by its manufacturer, are analyzed. In particular, having selected the interfaces required on the carrier board, the corresponding SoM pins that provide these functions are identified. Most controller signals are mapped onto multiple pins and can be selected by a

corresponding alternative function number with proper firmware setup. To reduce the probability of having firmware configuration issues related to signals allocation, assignment priority is given to signals mapped on pins with alternative function 0. If conflicts arise, pins are assigned to signals with higher number alternative functions.

Signal mapping onto pins is a delicate process. Thorough review is essential to avoid mistakes and obtain a balanced and coherent configuration in terms of both functional requirements and hardware constraints, while keeping peripherals configuration and initialization as simple as possible.

2.3 Components selection

Component selection was conducted preferring widely available products with industrial temperature range, to ensure ease of replacement and scalability for future requirements. Board mounted connectors were chosen for enhanced stability due to their resilience to mechanical stress that is caused by frequent attaching and detaching in harsh environments.

2.4 Power distribution and step down converters

Having selected the main ICs, they can now be sorted into categories with respect to the voltage supply range they require, based on the data extracted from their datasheet summarized in table 2.2. The ICs grouping depends on the required maximum tolerance on a specific supply, which is identified during this step and the maximum acceptable tolerance of the several buck converters is thus obtained. To illustrate, the USB Hub, Ethernet switch and Automotive PHY supply voltages intersect in the range 1.14 V - 1.21 V, thus, in order to have a common supply rail to all three of them, the respective step down converter must be very accurate. A DC-DC with 1% output accuracy is indeed chosen. In addition to the modules listed in table 2.2, plug-in cards must also be taken into account. These include four miniPCIe modules, two SIM cards and one M.2 SSD. Their contribution is reported in table 2.3. The SD card voltage is instead provided by the SoM directly, hence its contribution is not relevant in this context.

Once the modules are properly categorized and the final supply voltages that need to be derived on the carrier board are determined, the total current per supply is evaluated. The aim is to extract from this data a rough estimate of the worst case current that a voltage supply must be able to provide during typical operating conditions. Knowing the required current, suitable buck converters can then be picked out; refer to table 2.4. Further ICs and components are added later on during the schematic design stage but since their current draw is minimal, they have negligible impact on the overall current required on a specific voltage rail and are thereby omitted in the calculation.

Power distribution is shown in figure 2.6. The main supply rail is the 5 V, from which all other voltages are derived. This rail feeds all 5 V devices on board, the DART SoM and the buck converters. However, it is important to recall that the input voltage required by the specifications denoted in section 2.1 is 12 V - 24 V. The strategy chosen then involves using an external enclosed DC-DC converter to step down the voltage

SoM	**Voltage supply [V]**	**Current supply [A]**	**Notes**	**Qty**
DART-MX8M-PLUS V2	3.5-5	0.73 @ 3.826 V, 0.56 @ 5 V	2.79 W @ 3.826 V	1
Embedded module	**Voltage supply [V]**	**Current supply [A]**	**Notes**	**Qty**
RTC DS1337U+	1.8-5.5, typical 3.3	150 μ	draws from external battery	1
CAN Transceiver SN65HVD232QDR	3-3.6 (3.3±10%)	maximum 17 m, typ. 10 m @ 3.3 V	x2 driver and receiver	1
I2C Expander PCAL6408APWJ	1.65-5.5	0.75 m	with pullups enabled	2
USB HUB USB5744-I/2G	1.2 ±10% (1.08-1.32), 3.3 ±10% (3-3.6)	93 m @ 3.3 V 688 m @ 1.2 V	4 SS/HS ports. BC supported	2
PCIe Switch PI7C9X3G606GP	VDDC: 0.95±5%; CVDDC: 0.95±5%; VDDR: 1.8±5%; CVDDR: 1.8±5%; VP: 0.95±5%; VPH: 1.8±5%	5 @ VDDC, 0.02 @ CVDDC, 0.02 @ VDDR, 0.07 @ CVDDR, 0.54 @ VP, 0.13 @ VPH	worst case current values, highest temperature, 5.7 W	1
Gigabit Ethernet switch KSZ9567R	VDDIO: 3.3, 2.5, 1.8±5%; AVDDH: 2.5±5%; AVDDL: 1.2±5%; DVDDL: 1.2±5%	I_{DDAH} 330 m, I_{DDIO} 80 m, I_{DDCA} 460 m, I_{DDCD} 750 m, with AVDDH @ 2.5 V, VDDIO @ 3.3 V	full 1 Gbps operation all ports.	1
Automotive Ethernet PHY DP83TG721R-Q1	VDDA3P3V: 3.3±10%; VDDIO: 3.3±5%, 2.5±10%, 1.8±10%; VSLEEP: 3.3±10%; VDD: 1.05-1.21 (1.13±7%)	40 m @ VDDIO 3.3 V, 89 m @ VDDA3P3V, 1.5 m @ VSLEEP, 250 m @ VDD	active mode @ VDDIO 3.3 V. DP83TG720R-Q1 model used as reference	1
RS232 Transceiver TRSF3232E	5, 3.3 ±10%	1 m		2

Table 2.2: SoM and ICs: typical operating voltage and current supply. Operating mode selected is the one that requires higher supply values.

Peripheral/ plug-in card	**Voltage supply [V]**	**Current supply [A]**	**Notes**	**Qty**
USB type A 3.0	5 V	0.9 A HP SS; 150 mA LP SS; 0.5 A USB 2.0, 1.5 A USB 3.0 BC	1 port USB type A USB 3.0 BC considered	4
miniPCIe	3.3±9%, 1.5±5%	1100 mA (2750 mA) normal (peak) @ 3.3 V; 375 mA (500 mA) normal (peak) @1.5 V	latest is 2.1. 7.5 W per slot (manufacturers' limit)	4
SIM	5±10% class A	60 m	asynchronous cards (also class B 3 V, class C 1.8 V)	2
M.2 NVMe SSD	3.3±9%, 3.3Vaux±9%	3 A @ 3.3 V for a 10 W slot estimated: 1 A (3 W)	latest is revision 6. Optional Vaux is needed for wake signal	1

Table 2.3: Peripherals: typical operating voltage and current supply. Operating mode selected is the one that requires higher supply values.

Voltage supply [V]	**Current supply [A]**	**Total power [W]**	**DC-DC converter**	**Specs**
5	4.8	24	RSD-60G-5	2%, 12A
3.3	5.8	19	TPS6286A08	0.7%, 8A
2.5	330m	0.83	TPS62827AD	1%, 4A
1.8	0.22	0.4	TPS62827AD	1%, 4A
1.5	1.5	2.25	TPS62827AD	1%, 4A
1.2	2.8	3.4	TPS62827AD	1%, 4A
0.95	5.56	5.3	TPS6286A08	0.7%, 8A

Table 2.4: Board current drawn per power supply and step down converters

and feed 5 V to the board while providing all the necessary protections for automotive applications. Therefore, a DC jack is mounted on the enclosure and it accepts a voltage in the range defined by the enclosed DC-DC converter input. An anti-vandal pushbutton with integrated LED is used to disconnect the converter from the input power acting as a power on switch for the board. On the other side, the DC-DC output is attached to wires terminated with a connector that mates with the one on the PCB. On the board, a simple two terminal block header able to withstand the needed current is used, thus

providing a secure and easily pluggable interface between the 5 V rail on the PCB and the wiring of the external DC-DC converter.

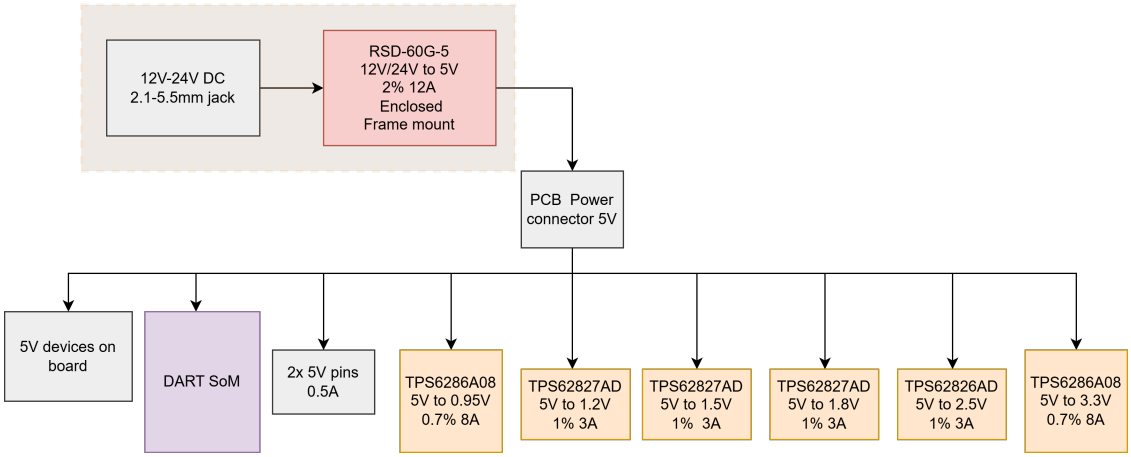


Figure 2.6: Block diagram detail: power distribution

Before focusing on the integrated DC-DC converters, let's discuss the reasons why an external enclosed DC-DC converter was chosen to provide the 5 V power to the board. Most importantly, enclosed converters often include built in protections that in solderable buck converters have to be implemented externally using additional chips or components. Robust and reliable protections are a key aspect in automotive applications in order to prevent the downstream system from being damaged. Common protection mechanisms are Under Voltage Protection (UVP), Over Voltage Protection (OVP), Over Current Protection (OCP), short circuit and reverse polarity protection. Moreover, enclosed converters are thoroughly tested for isolation, electromagnetic interference, mechanical stress and correct operation across the allowed temperature range. On top of these benefits employing an external converter brings additional flexibility to the design: it can be easily swapped in case more power is needed or replaced if damaged.

The railway-grade 60 W enclosed converter used to step down the voltage and supply the board is the RSD-60G-5 by MEAN WELL [50], figure 2.7. It is perfectly suited for this application, being specifically implemented for transportation systems. The 9 V→36 V wide input range facilitates system operation across multiple vehicle types, such as passenger and heavy duty vehicles (trucks, buses, construction machinery). It features reinforced isolation and it can be used in environments subject to dust, vibration and strong temperature gradients thanks to the semi-potted silicone interior.

As for the other DC-DC converters on board, two different modules are used, according to the current required by the rail. One can provide up to 4 A while the other reaches 8 A. They both are synchronous step down converters that can operate in forced PWM mode which allows to reduce the output voltage ripple. The output voltage is set using a resistive divider and it's highly accurate, they also feature excellent load transient performance. Load transient behavior is essential to understand how the converter responds to a sudden change in the output load current which causes a variation in the output voltage that will return to its nominal value after some time. In addition to this, both converters

Figure 2.7: RSD-60G-5 Enclosed DC-DC converter by MEAN WELL

support soft-start to limit inrush current. The term inrush current is used to refer to the current drawn to charge the converter output capacitor during start up. The start up response depends on how large the output capacitance is and on the load resistance. In the case of a large capacitive or small resistive load, the inrush current is consistent and it may even overcome the converter current limit. Soft starting the converter is a precaution taken to avoid high current surges. It consists in limiting the output voltage ramp up speed (slew rate limiting), thereby defining its rise time and reducing inrush current. This feature is very helpful in the current design since multiple converters feed from the same 5 V main rail and the expected current draw at start up is substantial.

Furthermore, the converters are equipped with both enable and power good pins. The power good signal is asserted by the converter internal circuitry to advise the system that the output voltage is stable and ready, it has reached its nominal condition. These are useful for managing power sequencing, as well as for proper monitoring of different supply rails. Requirements for power sequencing are extracted from the datasheet information of all the modules employed. These focus on the minimum and maximum supply voltage rise time allowed and, in the case of ICs with multiple supply rails, the order in which they should be ramped up. For simplicity, but mostly for robustness and error mitigation, a microcontroller is used to manage power sequencing. It senses the power good signal level and drives the enable of each converter.

2.4.1 Microcontroller as power supply supervisor

On board power monitoring, fault detection and recovery is coordinated with the use of a microcontroller which handles the start-up routine and supplies additional interfaces for expandability. STM32G071RB 64-pin microcontroller in Low-profile Quad Flat Package (LQFP) by STMicroelectronics [51] is used. A Low Dropout (LDO) regulator is added to supply the microcontroller with 3.3 V. The LDO is always enabled and it feeds directly

from the 5 V main rail, in this way the microcontroller powers on as soon as possible and can then promptly drive the enable signal of the DC-DC converters, managing their start up sequence.

Below are listed all board features implemented by microcontroller:

- monitors the hall effect current sense IC output voltage and promptly shuts down the board or signals the user if the current limit on the 5 V rail is excedeed;
- monitors all voltage supply levels connected to its ADC inputs;
- drives the enable and senses the power good of DC-DC converters;
- manages sleep, wake up and watchdog signals of the DART SoM as well as its reset;
- shares a multimaster I2C line with the SoM connected to I2C expanders that manage reset signals of ICs on board;
- has a dedicated reset pushbutton separate from the one of the SoM;
- drives four general purpose LEDs;
- SPI, UART, the non shared I2C line and two GPIOs are exported to a header for flexibility;
- is programmed and debugged via Serial Wire Debug (SWD) interface.

2.5 Board I/Os summary and block diagram

A summary of all user accessible hardware interfaces included on the board is reported below in table 2.5, together with the final block diagram sketched at a high level in figure 2.8.

Ports/sockets	**Qty**	**Notes**
SMA antenna connectors on the enclosure	x7	external antennas (2 x3 for miniPCIe, x1 for SoM integrated Wi-Fi)
microSD card	x1	SD/SDIO/MMC standards, up to SDR104 rate, auto-eject
M.2 NVMe M key	x1	PCIe Gen 3, 2280 form factor
USB Type A	x3	USB 3.0 SS, 1x BC 1.5 A active on 1 port at the time, either type A or C, choose via switch
USB Type C	x1	USB 2.0, 1x BC 1.5 A active on 1 port at the time, either type A or C, choose via switch
DB9 RS232	x2	serial ports for debug
DB9 CAN	x1	CAN-FD 5Mb/s, CAN2.0B
HDMI type A	x1	HDMI 2.0
Power status LEDs	x8	main rails, 3.3 V LDO, SoM power outputs
General Purpose LEDs	x7	x4 uCU driven, x3 multimaster I2C line driven
Power on switch	x1	Anti-vandal pushbutton with led
Reset push button	x2	SoM reset, uCU reset (i.e. board reset)
Buzzer	x1	Magnetic Audio Transducer
12 V-24 V input voltage jack	x1	2.1 × 5.5 mm, mounted on the enclosure
5 V input voltage connector	x1	2 positions, 5.08 mm pitch, main board supply
Battery CR2032	x1	Real Time Clock always on supply
5 V pins	x2	current limit set to 0.5 A each
Gigabit Ethernet RJ45	x3	IEEE 1588v2, IEEE 802.1AS/Qav AVB, QoS, 1000BASE-T
Automotive Ethernet RJ45	x1	TSN: IEEE 1588V2/802.1AS, AVB IEEE 1722, SQI, 1000BASE-T1; QoS
miniPCIe full size card 51mm x 30mm	x4	vehicular Wi-Fi cellular network (SIM slot) C-V2X (SIM slot) extra socket with standard pinout
SIM slots	x2	routed to miniPCIe slots, auto-eject
uCU Headers	x2	SPI, UART, I2C, GPIOs
SoM Headers	x2	JTAG, GPIOs
Power Header	x1	one pin per supply (0.95 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V) except for the 5 V that has two
Fan connector	x1	connected to the 5 V rail
DIP switch	x1	Boot mode select, USB BC enable, USB mux select
20-pin connector	x1	FFC-FPC, USB 2.0, ESPI, UART, GPIOs, RST, 5 V supply

Table 2.5: User accessible connectors, controls and status indicators.

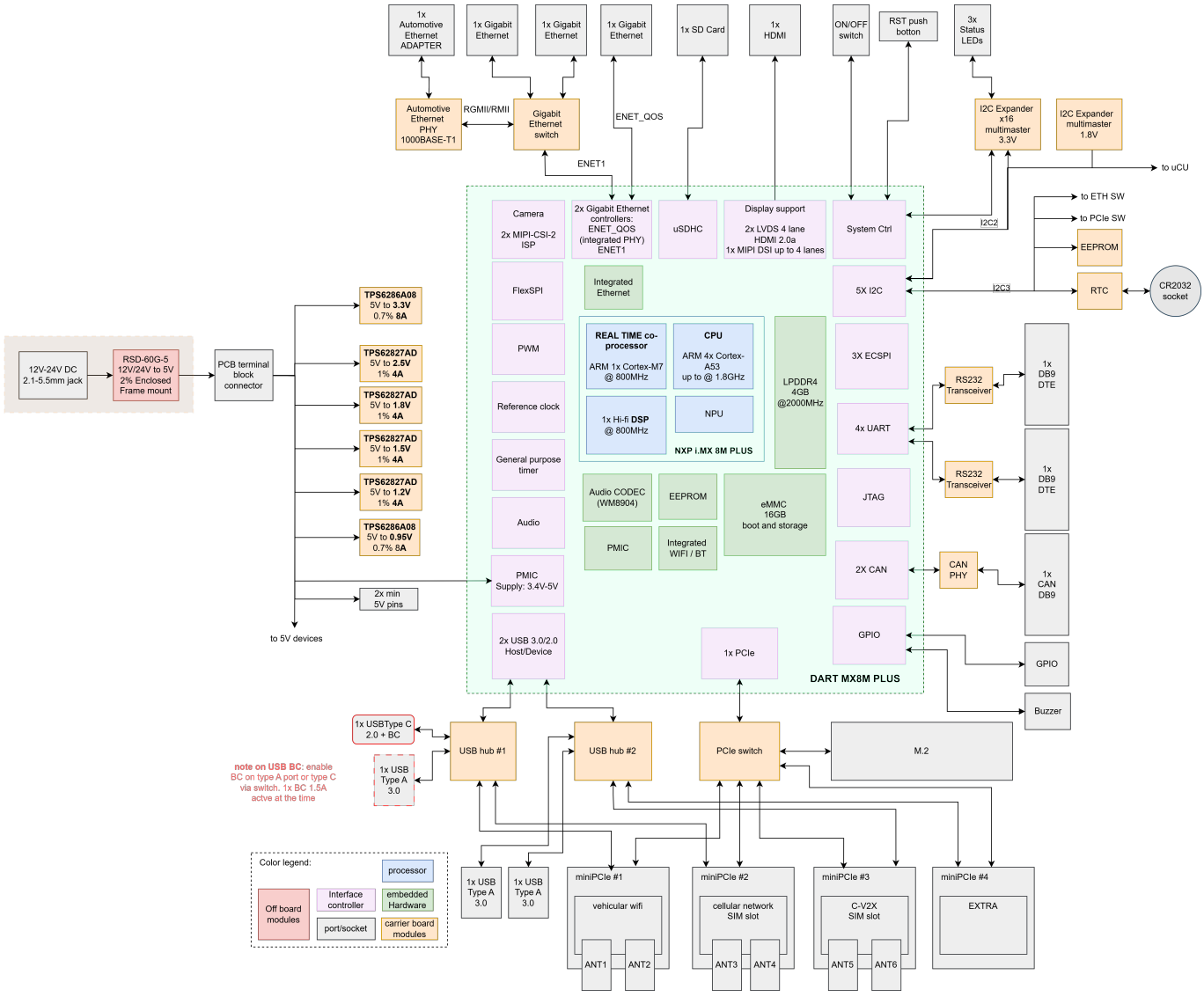


Figure 2.8: High level block diagram of the system

Chapter 3
Schematic design

From this point onward, the design implementation is carried out making use of KiCad Electronic Design Automation (EDA) tools. To start with, the electrical structure is outlined developing the schematic. The latter acts as a logical representation of the board and illustrates all functional connections between components. Its purpose is to guide PCB layout and manufacturing serving as blueprint of the design. The complete schematic is included in appendix A. The first sheet, also called Root sheet, provides an overview of the contents which can be roughly grouped in four categories: DART SoM connections, power distribution, interfaces and mechanics.

3.1 Library setup and symbols adjustment

Components in the schematic are represented by symbols characterized by all the essential attributes of the object they describe. Symbols that are commonly used can be found in standard libraries, while unconventional ones may be provided by their manufacturer and if not, they can be manually created, as was done for the DART SM symbol.

Project libraries are then configured including all the symbols required for the board design. To complete the set up, symbols physical appearance is adjusted for more clarity. In particular, to ease troubleshooting, pins within the symbol are rearranged according to their functionality and the object is divided in multiple units if the IC has a high pin count, such as in the case of Ethernet switch and PCIe switch.

3.2 Highlights of design choices

This section describes all design choices that were made to address a specific issue of compatibility, to accommodate user requests or simply to add value and flexibility to the overall system.

3.2.1 DART-MX8M-PLUS

The DART SoM incorporates three 90-pin connectors referred to as J1, J2 and J3, residing on the top, bottom and left side of the module respectively. Its corresponding symbol is divided up into multiple units where pins are grouped according to the interface belonging to the signals mapped onto them. All alternative functions of each pin are shown and the signals name is coherent with the nomenclature used the its manufacturer in order to minimize errors during the schematic design process.

The voltage supply range in which the module operates is within 3.5 V - 5 V. The 5 V main rail on the board has a 2% tolerance as stated in the RSD-60G-5 datasheet. Hence, to guarantee a more robust system a Schottky diode is inserted between the 5 V rail and the supply pins of the SoM to drop the voltage by 0.4 V. Doing so, reliability

is enhanced ensuring that the module is always powered by a voltage within the allowed operating range.

The reset signal of the module is configured as open drain, thus it can be driven by multiple sources allowing control of the SoM reset in different ways, depending on user needs. Specifically, the line is managed by the microcontroller and a dedicated pushbutton that controls exclusively the SoM reset, giving the user the possibility to initiate the DART restart routine while keeping the carrier board powered on.

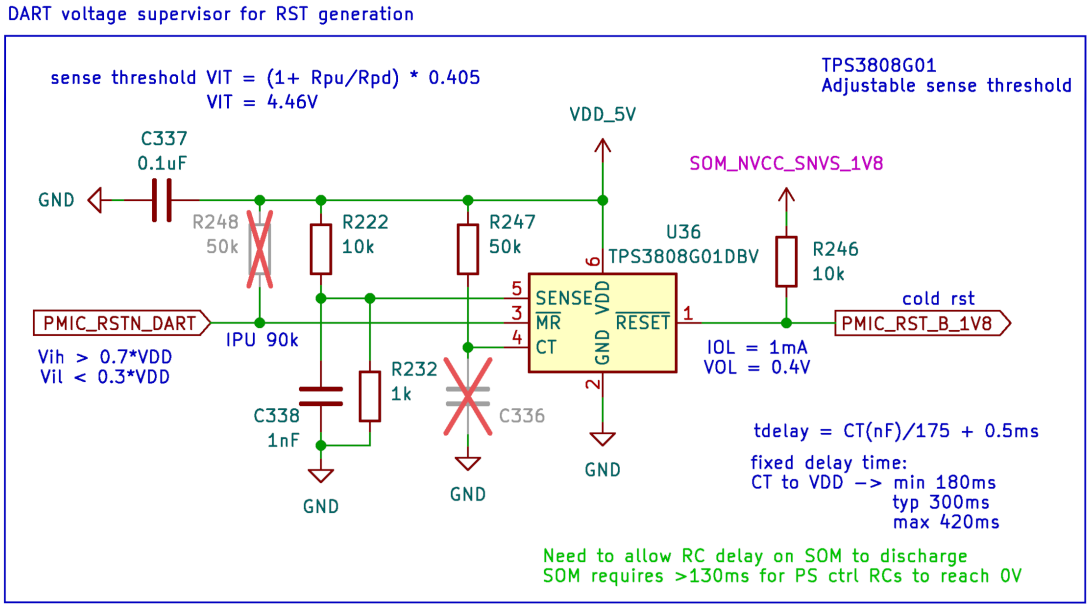


Figure 3.1: Schematic capture: SoM reset circuit

In addition to this, a sense threshold IC is used to ensure the reset signal deassertion during the time interval required by the microcontroller to start up and drive the line low. Implementation of the supervisory circuit for reset generation is illustrated in figure 3.1 and can be found in sheet 12 of the schematic. The selected IC is a programmable delay supervisory circuit, it monitors the voltage level of its input signal, which is connected to both the microcontroller and the pushbutton, and generates a secondary open drain signal tied to the SoM pin associated with the reset function. The programmable delay refers to the delay time that undergoes between the input signal deassertion (i.e. when it returns above the set threshold value) and the one of the output (i.e. reset state exit request). The delay time can either be set to 20 ms by disconnecting the dedicated delay pin (i.e. CT pin), 300 ms by connecting the delay pin to the IC power supply through a resistor or it can be user adjusted between 1.25 ms and 10 s connecting an external capacitor. In the current design, the 20 ms fixed delay time configuration is exploited, however a capacitor placeholder is added on the IC dedicated delay pin. Doing so, a capacitor can be placed later on during prototype testing, facilitating delay adjustment if needed.

3.2.2 Power distribution and current sensing

As previously mentioned in section 2.4, the main board power rail carries 5 V and power from it is distributed to six DC-DC step down converters and one LDO regulator. Board's power is supplied through a 2-position pluggable through-hole terminal header for PCB. Through-hole technology ensures robustness in the design; this way the connector is well soldered onto the board and less susceptible to mechanical stress. The power input connector is followed by a common mode choke that was inserted to reduce impact of external EMI and suppress high frequency noise injection into the rest of the system. While DC power is allowed to pass through the choke, common mode noise is presented with a high impedance path and is thereby blocked. Several bypass capacitors are also placed and, together with the common mode choke, they form an LC filter which contributes to high frequency noise attenuation. Through this approach a clean and stable main power rail is obtained and can be used to safely supply all devices on board.

Given that the external enclosed DC-DC converter has a current rating of 12 A and the board integrates multiple step down converters, devices that operate with 5 V supply, together with various slots and sockets for add-in cards, a current sensing circuit has been implemented, figure 3.2.

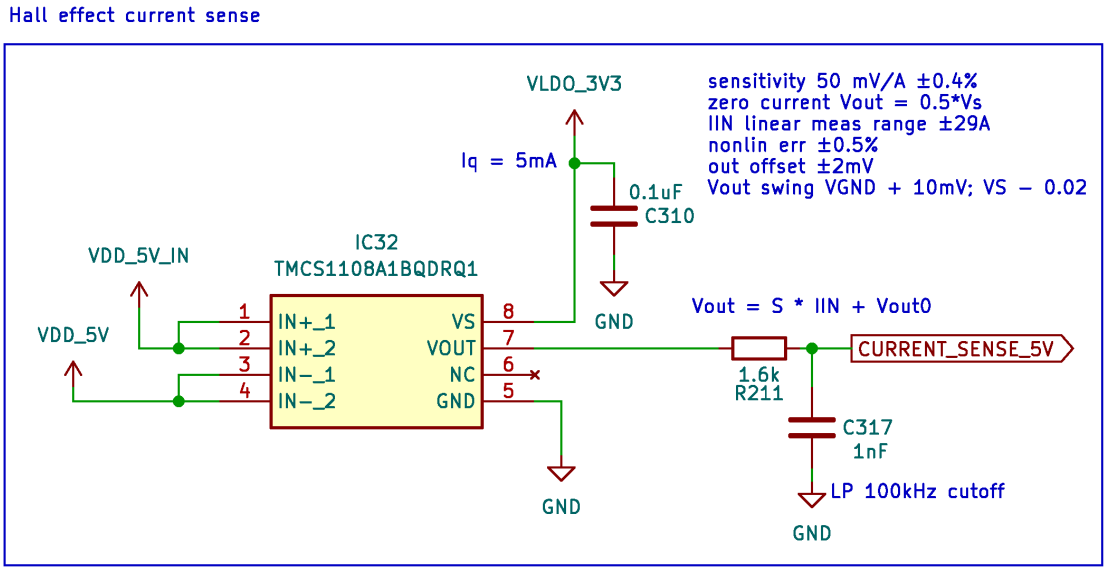


Figure 3.2: Schematic capture: Hall effect sensor for current sensing on the main power rail

An IC tailored for current sensing applications has been used. It is based on the Hall effect and, in addition to providing galvanic isolation, it allows to measure current on the main rail without resorting to intrusive techniques. Input current flows in a resistor of the order of a few mΩ integrated in the sensor, thereby the voltage drop introduced on the rail is negligible and thermal dissipation is minimal. The current measure of the sensor is embedded in its output voltage which is fed to an ADC input of the microcontroller integrated on the board. The sensor is of ratiometric type, meaning that the output

characteristic follows supply voltage variations. It improves immunity to noise and simplifies ADC interfacing. Taking advantage of this characteristic, voltage fluctuations are automatically compensated by using the 3.3 V output of the LDO regulator that powers the microcontroller, to supply the sensor as well.

As for the step down converters, they all feature adjustable output voltage via a resistive divider and are equipped with input EMI filters and output LC low pass filters. Specific capacitors and inductors are selected for the converter design with the help of WEBENCH Power designer tool by TI [52]. Equivalent series resistance of capacitors must be taken into account to minimize the voltage ripple as well as output inductor characteristics since they affect the converter efficiency. They must be able to withstand the maximum load current and store the required energy, which is why larger packages are used instead of basic SMD packages, such as 0402 or 0603, not suited because of their low current rating and limited capacitance. Hence the selection is made based on a trade off between efficiency and area occupied by the external components.

The chosen power distribution strategy follows a tree topology. Here, the main rail is branched out to the step down converters, which contrasts the linear approach where the converters are connected in sequence and each enable pin is tied to the power good of the DC-DC that precedes it. The solution adopted instead relies on the microcontroller to manage the buck converters control signals; this grants more flexibility since the start up sequence can be adjusted via software and converters can be independently disabled which also facilitates the troubleshooting process during prototype testing.

Furthermore, each power rail with a voltage greater than 1.8 V has a green LED for signaling the line status to the user while a red LED is used for the 1.8 V lines instead. Status LEDs are also included for two power outputs of the DART SoM: 3.3 V and 1.8 V. No status LED is included for rails with voltages below 1.8 V but all power rails can be measured since they are accessible via headers, as described in a later section 3.2.9.

3.2.3 USB port power controller and current limit

Every USB device must be supplied with 5 V and its current draw is limited by the port power controller IC. Specifications state that the typical value of drawn current allowed is 0.9 A for USB 3.0 and 0.5 A for USB 2.0. For ports with battery charging capability the current can reach 1.5 A instead. To prevent overload and waste of resources, the user is instructed to enable battery charging in only one port at the time, even if the design allows both port to be simultaneously active in battery charging mode.

The port power controller manages the USB device connection with the 5 V rail and interacts with the USB Hub through the power port control signal, figure 3.3. This flag warns the Hub when the current drawn by the port exceeds the limit imposed. Current limit values are set by placing a certain resistor on the dedicated ILIM pin of the device. Exploiting this, when varying resistor values connected to the ILIM pin, the current limit is modified. To achieve this, a simple switch is used, figure 3.9. When active it lowers the total resistance seen by the ILIM pin of the power controller by adding another resistor in parallel. In this way, battery charging ability can be enabled in the two ports, one Type A connector and Type C connector, by simply toggling the respective DIP switch.

An additional resistor and capacitor in series, are placed on the ILIM pin, allowing

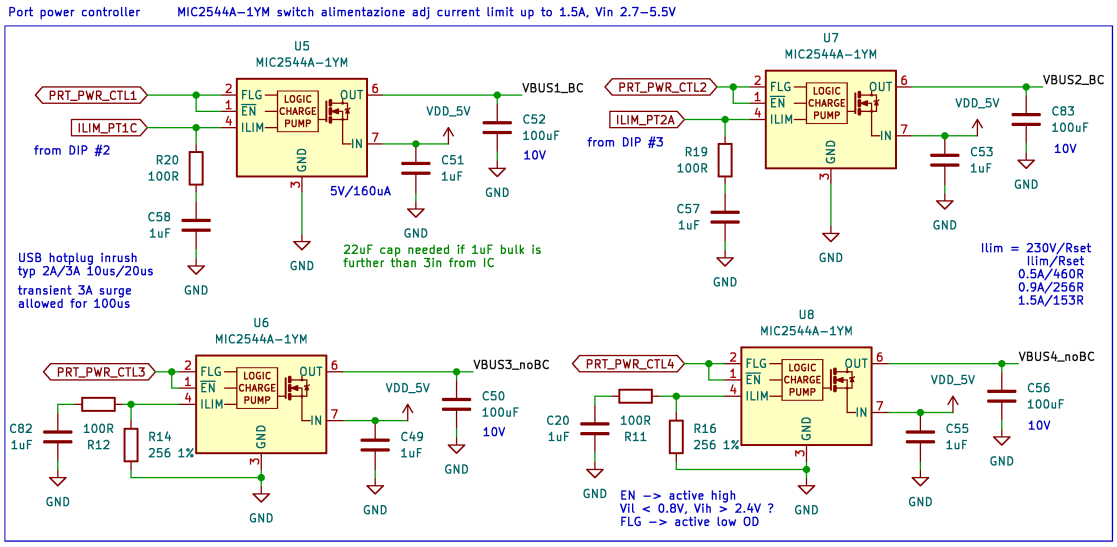


Figure 3.3: Schematic capture: USB Port power controller

the IC to tolerate a 3 A current surge for a time interval lower than 100 *u*s, so the flag signal will remain deasserted. The current surge event is a common condition that may happen every time a device is plugged or unplugged when the system is powered on.

3.2.4 USB 2.0 multiplexer/demultiplexer switch and 20-pin FFC-FPC connector

At a later stage of the design process, the end user asked if it would have been possible to accommodate an additional miniPCIe module with non standard pinout. Two issues arose from this request: lack of free interfaces and proprietary slot limitations. The USB Hubs employed are fully utilized, thus to accommodate the new miniPCIe slot the USB section would've had to be redesigned, starting from the selection of a different Hub with more interfaces available. Moreover, a custom connector dedicated to a specific add-in card leaves no margin for flexibility, restricting its use to a far too limited device type. Besides this, embedding a connector compatible with only vendor specific designs, is inconsistent with the purpose of the board itself which should be open, flexible and highly customizable.

To address both matters while still fulfilling the end user request, a solution was found. The first issue was resolved inserting a USB 2.0 multiplexer and demultiplexer switch which deviates the USB 2.0 signals from the fourth miniPCIe slot to a 20-pin connector meant for Flat Flexible Cables (FFC) or Flat Printed Cables (FPC), figure 3.4. The mux select signal is routed to the DIP switch, figure 3.9, allowing the user to easily choose between the two USB 2.0 differential pair routing options according to the intended use.

Inserting the 20-pin FFC-FPC connector helps overcome limitations that would have arisen with the integration of a miniPCIe slot compatible with only the proprietary module in question. The connector's pin assignment is shown in figure 3.5. Interface signals

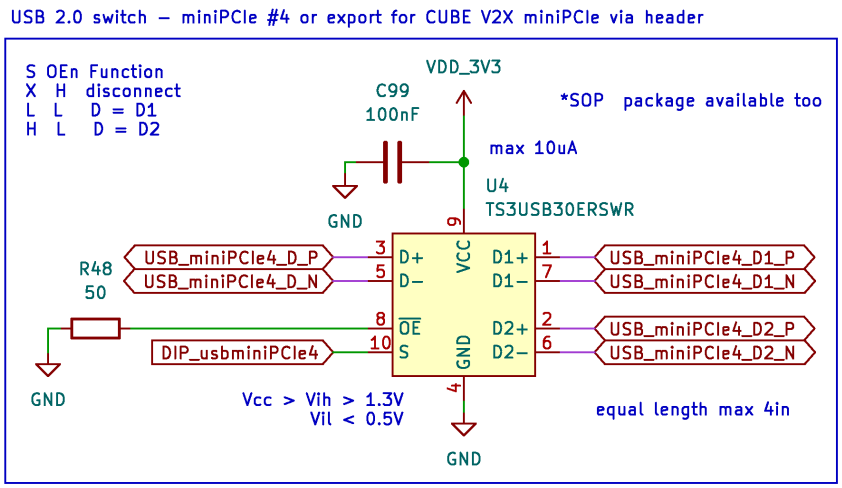


Figure 3.4: Schematic capture: USB 2.0 Mux/Demux switch

routed to the connector correspond to the ones required by the vendor-specific module. The idea is to use this connector to attach via FFC or FPC cable an external miniPCIe adapter that matches the non standard pinout required by the module. This configuration allows the board to preserve interoperability and remain standard compliant.

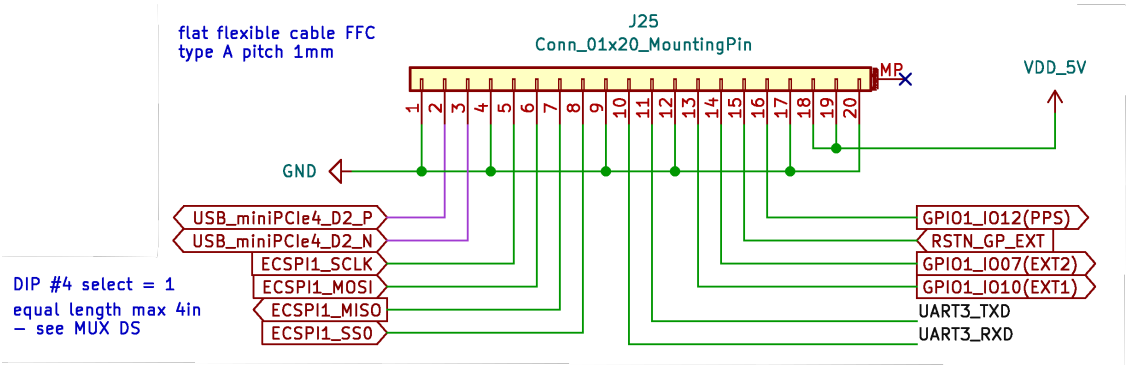


Figure 3.5: Schematic capture: 20-pin FFC-FPC connector for non standard pinout miniPCIe adapter

Ultimately, this proved to be the right choice as, during project development, the proprietary CUBE V2X module by nfiniity [53] was taken off the market, which could've been expected since the V2X sector is rapidly evolving.

3.2.5 EEPROM for Board ID

A small memory has been included to provide board identification and configuration data. It interfaces with the DART SoM via I2C bus. The selected EEPROM offers Write Protect functionality. It features a dedicated pin that defines whether writing on the memory is allowed or not. When pulled high, the memory becomes read-only; on the

other hand, if pulled low, both read and write operations are allowed.

The write protect option can be enabled by assembling a 0 Ω resistor in the respective placeholder inserted and, at the same time, deassembling the 0 Ω resistor that is already placed and pulls the pin low. With this configuration, the EEPROM can be written using the I2C interface during the configuration phase and the write protect function can be disabled later on once board initialization is complete.

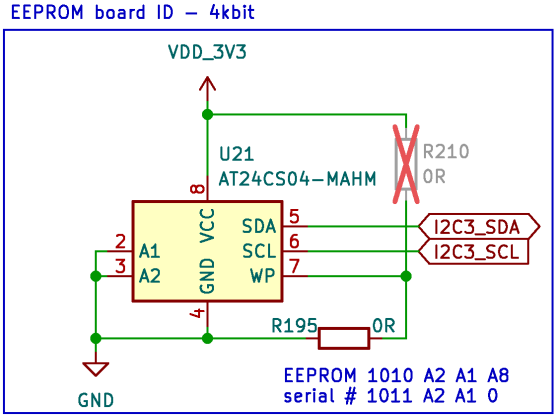


Figure 3.6: Schematic capture: EEPROM

3.2.6 RGMII clock delay

The RGMI Interface is used to implement Ethernet MAC to PHY connections as described in section 2.2.1. It includes four transmit and receives lines, one per bit, two separate signals for transmission and reception control, as well as transmit and receive reference clocks at 125 MHz for a 1000 Mb/s links.

Clock and data at the transmitter side are not skewed, they are dispatched simultaneously, whereas the receiver samples data on both rising and falling clock edges (Double Data Rate clocking). This results in extremely tight set up and hold times at the receiver, which is why RGMII v2.0 specification states that the interface must be designed so as to introduce a 1.5 - 2 ns delay on the clock lines adding some skew between the clock edges and the valid data, thus improving set up and hold time constraints.

Additional delay can be achieved through different approaches. Delay can be introduced on the clock lines with respect to the data lines exploiting propagation delay that arises from a mismatch in distance between the routed signals. The calculation below provides a rough estimate of how much distance mismatch is needed to introduce 1.5 ns and 2 ns delay based on the speed at which the electric field propagates in the PCB FR4 dielectric.

$$v = \frac{c}{\sqrt{\varepsilon_{r,FR4}}} = \frac{3 \cdot 10^8 m/s}{\sqrt{4.5}} = 1.4 \cdot 10^8 m/s \tag{3.1}$$

$$t_{delay} = 1.5ns \rightarrow d_{mismatch} = 21.2cm \tag{3.2}$$

$$t_{delay} = 2ns \rightarrow d_{mismatch} = 28.3cm \tag{3.3}$$

As shown by the results in 3.2 and 3.3, the required distance mismatch is considerably high and routing traces with this much mismatch is not practical: parasitic inductance and capacitance come into play, slowing down edges of the signals, increasing crosstalk and causing reflections. In addition to this, in DDR clocking little jitter, in conjunction with even the smallest distortion introduced by routing such long traces, may cause wrong data sampling. Space constraints are also considered since almost 30 cm of trace routing would take up a lot of area on the board and most importantly, propagation delay is strongly affected by temperatures thus it may drift with time causing timing violations. For this reasons the RGMII clock traces won't be routed with a 21 to 28 cm distance mismatch with respect to the data lines. However, the option of introducing a lower amount of propagation delay via trace length mismatch is still taken into consideration.

Alternatively, the Ethernet switch IC features an internal delay setting which can be configured by writing in a specific configuration register. Then again, this does not constitute a safe solution. Devices connected to the switch via RGMII interface may also introduce internal delay. This devices are the SoM and the Automotive Ethernet PHY. Their behavior in this situation is unknown since there is no mention of it in the DART SoM documentation and the Automotive Ethernet PHY datasheet has not yet passed NDA approval. Moreover, an errata has been issued regarding the employed Ethernet switch, which states that additional delay is required with respect to the one defined by the RGMII specification, reaching a value of minimum 2.2 ns. Given that the internal delay option allows to set a 1.5 ns delay, following the errata dispositions, other solutions to introduce additional delay must be taken into account.

Ultimately, to address all of the illustrated concerns, a 0 Ω resistor and a capacitor placeholder are added on the reference clock connections so as to introduce a propagation delay by assembling components of adequate values during the prototype testing phase.

Refer to sheet 23 of the schematic A for the described implementation.

3.2.7 Ethernet switch management interface

The Ethernet switch can be configured through various interfaces, including I2C and Management Data Input Output (MDIO). Both buses are though mapped onto the same pins of the switch IC. The design choice consists in connecting the management interface pins of the Ethernet switch to the I2C bus of the SoM using 0 Ω resistors, yet prearranging two resistor placeholders for a potential connection between the management interface of the switch and the one of the SoM.

Therefore, if needed, the management interface can be disconnected from the I2C bus and attached to the SoM MDIO pins. The management interface configuration is set via resistor straps, hence when enabling the MDIO interface, the I2C resistor strap must be deassembled and at the same time, a 1 $k\Omega$ resistor should be assembled in its dedicated placeholder. In this way the Ethernet switch and the integrated Ethernet PHY on the SoM would be daisy chained through the management interface.

3.2.8 Automotive Ethernet

The Automotive Ethernet PHY [43] datasheet is not available to the public, the only accessible document is a brief containing the main features supported by the IC. As the signing procedure for the Non Disclosure Agreement is still underway, the corresponding section of the schematic has not yet been implemented. Nonetheless, connections between magnetics and RJ45 have been predisposed, as shown in figure 3.7. Figure illustrates how standard magnetics and RJ45 connector have been adapted for Automotive Ethernet that employs only a single twisted pair instead of four, as previously discussed in section 2.2.1.

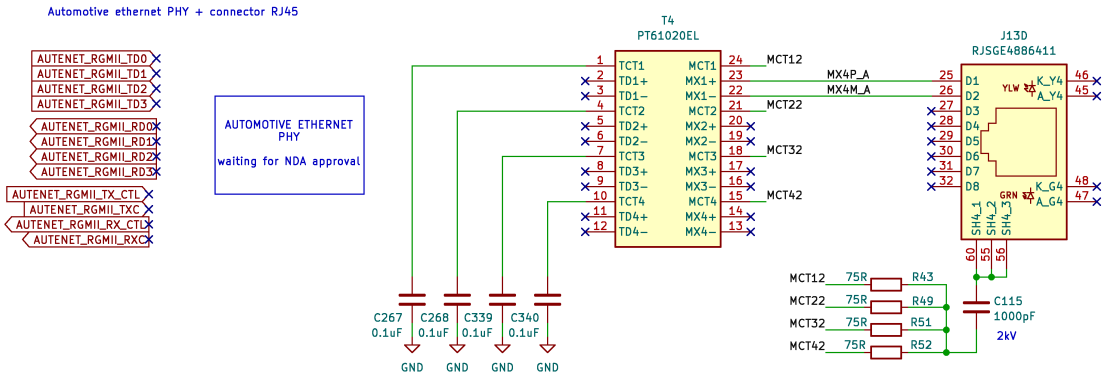


Figure 3.7: Schematic capture: Automotive Ethernet

Moreover, an alternative PHY has been selected in order to avoid stalling the design process due to administrative issues. Though, it should be noted that the substitute PHY is no match to the one selected and would strongly limit the performance of the board, since it does not support precise time stamping capability for real time communications (i.e. 802.1AS support and AVB clock generation) which is an essential feature for Automotive Ethernet connections.

An additional LDO regulator has also been added to generate the 1V power supply needed by the replacement PHY, but will be removed once the NDA is approved.

3.2.9 Polyfuses on voltage supply header

All available power rails on the board are exposed through a dedicated header. Having direct access to the supply lines facilitates testing and debugging, allows expandability and can be useful in case adjustments are needed. Voltages can be measured using an oscilloscope or a multimeter without having to scrape off the solder mask to get to the copper trace, which is helpful for checking the nominal value of the rail as well as the start up sequence and voltage ramp up. The header ensures seamless integration of additional modules, sensors and even ICs, given that also low power rails are exposed.

Polyfuses are added between each rail and the connector, as shown in figure 3.8. The fuse insertion grants protection in case of accidental shorts between the rails, preventing damage from spreading to the rest of the board. They act as current limiters averting excessive current flow that may cause electromigration in the copper trace and overheating

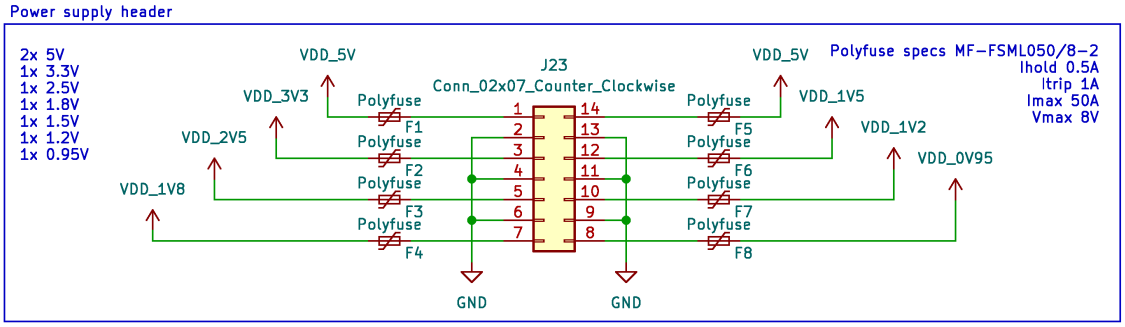


Figure 3.8: Schematic capture: Power supply header

of the system. Besides, they can be easily replaced in case of faults or if a higher or lower current limit is desired.

Employing resettable fuses instead of traditional glass fuses offers many advantages. Glass fuses are expensive, they need to be replaced after a fault occurs since they are one time usage devices and the process can be a bit tedious. Resettable fuses on the other hand, automatically recover after faults, can be reused and are also available in SMD package. They are Polymeric Positive Temperature Coefficient devices and operate increasing their resistance in response to a temperature rise. As most devices, they are characterized by values of maximum voltage and current that define the limit over which the device will be damaged. Specific electrical characteristics are the trip and hold current. The hold current can flow continuously through the fuse without causing it to trip. On the contrary, the trip current corresponds to the current amount needed to activate the fuse. It should be noted that when the polyfuse trips, current does keep flowing even if in just small amounts. This is caused by its inherent properties. Once flowing current exceeds the trip value, the resistance increases dramatically but the electrical connection is still present.

Fuses characterized by a trip current of 1 A have been chosen for this application.

3.2.10 DIP switch

One 4-position DIP switch is included on the board. It eases user interaction with the hardware setup. Functions that can be enabled when altering the switch state are reported in table 3.1. A single device is integrated instead of having four separate slide switches, for practical reasons. This way all configuration options are next to each other and less board area is occupied, which is convenient for both troubleshooting and layout placement.

The first position is dedicated to the DART SoM boot mode option. Switching between a pull down and pull up resistor, either boot from the internal eMMC or the external microSD card can be selected.

As described in section 3.2.3, the second and third position of the DIP switch are used to enable battery charging on a type A USB connector and a type C, respectively. When the switch is on, the total resistance seen by the ILIM pin of the USB port power controller is lowered by adding an additional resistor in parallel, figure 3.9.

The last position is reserved for the select signal of the multiplexer/demultiplexer

used to deviate the USB 2.0 differential pair from the fourth miniPCIe slot to the 20-pin FFC connector. In this case as well, the switch is used to convert a pull up into a pull down.

Switch number	Function	OFF state	ON state
1	Boot mode select	uSD	eMMC
2	BC USB Type A enable	off	on
3	BC USB Type C enable	off	on
4	USB 2.0 mux select	miniPCIe slot	20-pin FFC-FCP connector

Table 3.1: DIP switch functions selection

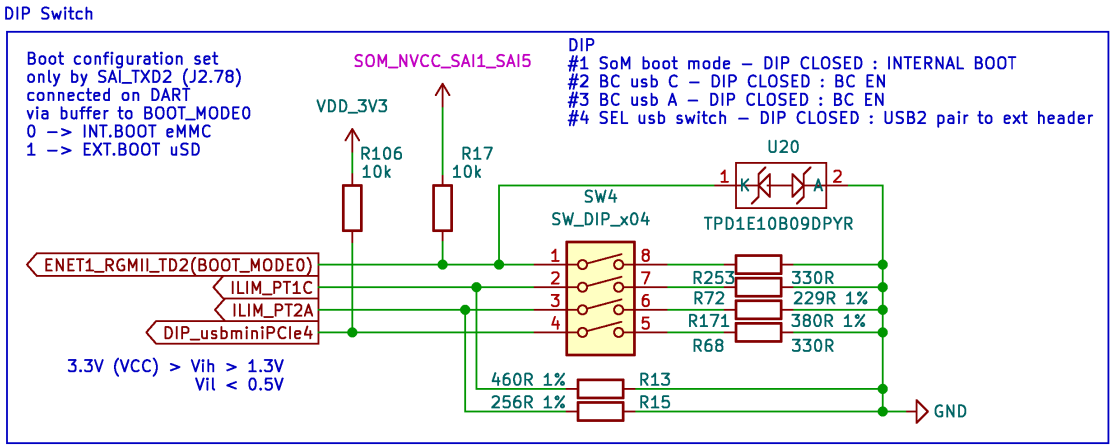


Figure 3.9: Schematic capture: DIP swicth

3.2.11 I2C

The DART SoM exposes five I2C interface peripherals, of which the first and fourth buses are used internally, one for the boot process and Audio coded, the other for Bluetooth. This leaves 3 available buses, assigned as indicated in table 3.2.

The I2C2 bus is connected to the SoM and the microcontroller, as both of them support multimaster operation. The three I2C expanders act as slave devices, hence they can be controlled by either the SoM or the microcontroller. The expanders are used to generate all devices reset and control signals, as well as output enable signals for level shifters. They also sort the fault indicators and interrupt signals from different components and warn both masters using a dedicated interrupt line.

On the other hand, the I2C3 bus is implemented as single master and is shared between the EEPROM, the serial Real Time Clock, Ethernet switch and PCIe switch for configuration and debugging. Both Serial Data line (SDA) and Serial Clock line (SCL) signals of this bus are connected to a 5 kΩ pull up resistor internal to the SoM. Resistor placeholders are though added on the board in case a stronger pull up is needed.

The last bus, I2C5 is only shared between the four miniPCIe slot and is controlled solely by the SoM. This eases the troubleshooting process of potential addressing problems that may surface.

Moreover, all output signals are kept low during board power on, by adding a 10 kΩ pull down resistor. Exceptions are the ICs reset signals which feature their own RC circuit, as described in section 3.2.14. Refer to sheet 29 of the schematic A for the I2C board section.

It should be noted that the PCIe reset signal has a specific ramp up timing constraint that is addressed using a tri-state output CMOS buffer, which guarantees that the minimum slew rate requirements are met. Hence, it does not feature the same RC circuit for reset generation as the other mentioned ICs do.

I2C1	SoM internal usage (EEPROM, Audio codec)
I2C2	to uCU, I2C expanders - multimaster line
	0x40 I2C expander 1.8 V 0x42 I2C expander 3.3 V (Schematic reference designator: U24) 0x44 I2C expander 3.3 V (Schematic reference designator: U25)
I2C3	5 kΩ internal pull up on SoM
	0x50 EEPROM board ID 0x5F ETH switch 0x68 RTC 0x6F PCIe switch
I2C4	SoM internal usage (BT function)
I2C5	4x miniPCIe slots

Table 3.2: DART SoM I2C addressing

3.2.12 JTAG chain

The DART SoM exposes its system JTAG controller which provides access to internal registers for testing and debugging purposes. A second IC on the board also supports JTAG interface, the PCIE switch.

The Joint Task Action Group (JTAG) protocol is based on four signals also known as Test Access Port (TAP) which belong to the IEEE 1149.1 standard [54]. Proper pull up and pull down resistors are added on control, clock and data input lines, to ensure correct operation. Signals voltage level is 3.3 V, compatible with the DART SoM logic; the PCIe switch operates at 1.8 V instead. Thus, JTAG interfaces of the two devices are daisy chained together using appropriate level shifters to adapt the 3.3 V signals of the SoM to the 1.8 V ones of the PCIe switch.

3.2.13 PCIe clock

PCIe interface requires a reference clock to provide precise timing between the host and the endpoint device. A dedicated 100MHz oscillator compliant with PCIe Gen 3 specifications, is used in this application. The output reference clock differential pairs are

connected to the SoM and the PCIe switch, which in turn, outputs a buffered clock for each of its downstream ports. This scheme is described as Common Clock Architecture since the host and endpoint receive the clock from a common source, in contrast with the Separate Clock Architecture were each device has an independent local reference clock. The clock is distributed using High speed Current Steering Logic (HCSL) signaling, a differential logic format designed for low jitter clock transmissions in high speed communications.

To minimize the interference caused by the clock signals with other parts of the system and improve signal integrity, proper termination of PCB traces must be implemented. In this case, 50 Ω resistors to ground are used to terminate the lines and are placed close to the receiver device, that is the SoM and the PCIe switch. A 33 Ω series resistor is also added to avoid debouncing, it lowers the Q factor for ringing caused by the fast switching HCSL drivers.

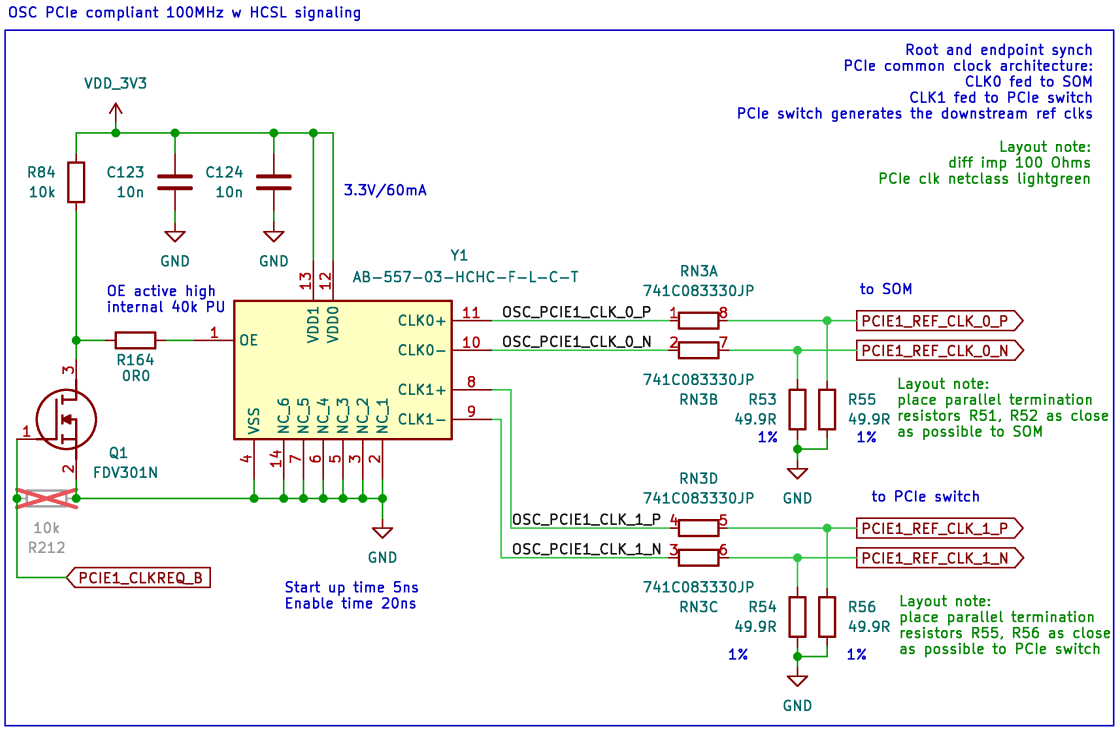


Figure 3.10: Schematic capture: PCIe 100 MHz HCSL oscillator

The PCIe switch supports low power management for the downstream devices. When entering low power mode, the reference clock must be disabled. As a consequence, the module asserts a clock request signal to reactivate the clock and exit low power mode. Hence, the clock request signal is used to drive the output enable pin of the clock oscillator. The request signal is active low, thus a simple mosfet is used to invert logic and obtain a control compatible with the oscillator active high output enable.

To improve robustness and ensure correct operation of the system in all cases, the connection of the control signal to the enable pin is done using a 0 Ω resistor that can

be removed to disable low power functionality. Hence, exploiting the enable internal pull up of the oscillator, the clock will always be in an active state. As an alternative, the mosfet can be disabled forcing its gate to ground by assembling a resistor in the dedicated inserted placeholder.

3.2.14 IC reset circuit

Both USB Hubs and the Ethernet switch reset signals are shaped using an RC net in conjunction with a pair of diodes. Figure 3.11 shows the circuit implementation for the Ethernet switch reset signal, although the reader should be aware that the same circuit is applied for the USB Hub reset generation.

The reset signal is driven by the I2C expander which, in turn, answers to the SoM and microcontroller controls. The signal is then routed to the RC circuit. The input diode prevents current to flow backwards into the I2C expander and, at the same time, provides a discharge path for the capacitor when the voltage rail is powered. Instead, the diode connected to the voltage supply is essential for discharging the capacitor when power is turned off. Omitting this diode is counterproductive since the capacitor would remain charged and the reset signal would be deasserted at the following power on.

Therefore, the circuit works in different scenarios: at power on when the I2C expander has all its pins configured as inputs (Power on Reset) and during normal operation, when the expander can drive the signal line (Warm Reset).

At power on, the capacitor is initially discharged and the voltage supply is still ramping up, thus the reset signal is low which ensures that the devices are in a known state. The rate at which the capacitor charges depends on the RC time constant of the net.

During normal operation, the reset is kept high via the pull up resistor connected to the power rail. Warm reset (i.e. device is reset when the board is powered) can be initiated by asserting the output reset signal of the I2C expander.

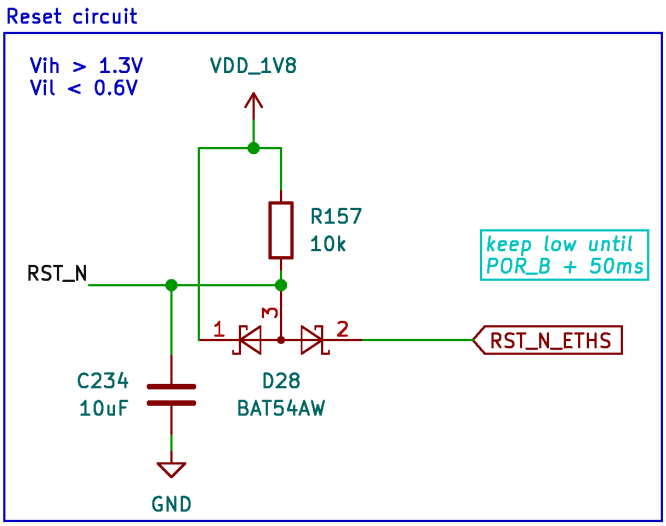


Figure 3.11: Schematic capture: Ethernet switch reset circuit

3.2.15 RTC OR circuit

A serial real time clock IC is included on the board. It functions as a low power clock and calendar, it features two programmable time-of-day alarms and is accessed via I2C interface where it operates as slave. The RTC relies on a 32.768 kHz crystal oscillator and it does not require any other external components since the oscillator circuitry is implemented internally.

Accurate time and date information is granted by always providing power to the IC even when the board is powered off. For this purpose, the RTC is powered by two sources: the 3.3 V board power rail and the CR2032 3 V coin cell battery. Diodes positioned so as to implement an OR circuit, are used to switch between the two power sources. When the board is on, the diode connected to the cell battery is reversed biased and isolates the battery from the IC. On the other hand, when no board power is present, the diode connected to the 3.3 V board power rail is the one in reverse bias, hence current is supplied to the IC through the battery cell. Schottky diodes are used in order to minimize the voltage drop seen by the RTC supply pin with respect to the power rail, caused by the diode insertion.

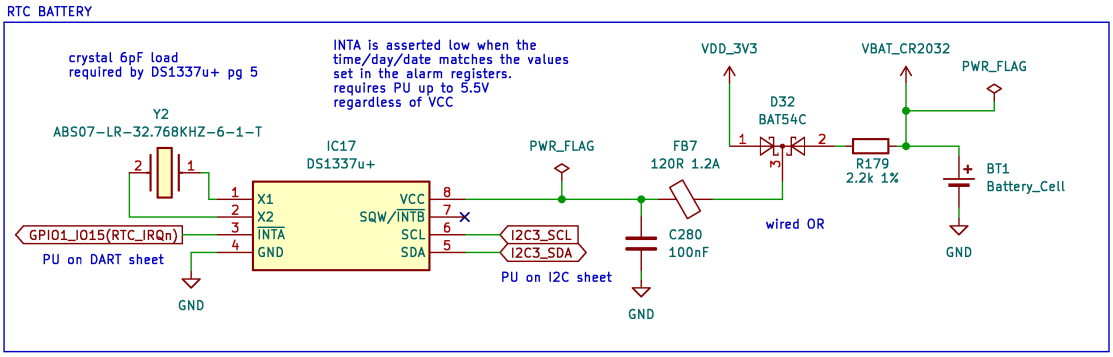


Figure 3.12: Schematic capture: Real Time Clock

3.3 Passive components

The current section contains a brief overview of the main passive components used in the schematic implementation.

3.3.1 Resistors and capacitors

Package types of each resistor and capacitor were chosen based on their function and physical position on the board. The 0603 packages were employed for resistor straps and placeholders, so as to facilitate the assembly and deassembly process in case any changes are needed during prototype testing. On the contrary, 0402 packages were used for terminations and current limiting in order to maintain good signal integrity and avoid wasting board area where it's not needed.

A similar reasoning was applied for capacitor package selection, though taking into account the capacitor nominal value as well. Small 0402 packages have lower parasitic inductance and are exploited for decoupling high frequency noise on the ICs power rails, hence they are placed close to the device power pins. Beside this, 0402 capacitors are also selected for AC coupling on differential lines such as the USB and PCIe differential pairs. The 0402 package is therefore assigned to capacitors with nominal value smaller than or equal to 1 μF, above this value, 0603 packages are used as in the case of bulk decoupling and capacitor placeholders. Moreover, as mentioned in section 3.2.2, buck converters capacitors are of 0603 or 0805 package types which present higher voltage ratings and can handle higher ripple currents. For capacitors with nominal value greater than 10 μF, 1210 packages were used.

All capacitors on the board are Multi Layer Ceramic Capacitors (MLCC) with Class 2 dielectrics X7R or X5R. The first character of the dielectric classification code refers to the minimum temperature the capacitor can handle, which in this case corresponds to -55°C; while the second indicates the maximum temperature, corresponding to 85°C for X5R and 125°C for X7R. Instead, the last character indicates how much the capacitance value can change in the defined temperature range, that is ±15% for X5R and X7R types. MLCC are made of a layered structure where metal plates and ceramic dielectric are alternated. They do not contain electrolytes and are not polarized, which results in improved robustness and better thermal endurance as well as longer life time, with respect to other technologies.Voltage derating is also taken into account when choosing the capacitor for a specific application; in fact, most of the selected capacitors are rated for 10 V and are used at an operating voltage smaller than or equal to 5 V.

3.3.2 ESD

Electrostatic Discharge (ESD) protections have been inserted on USB, HDMI, microSD signal traces to ensure robustness. In particular, for the USB 2.0 and USB 3.0 interfaces, components integrating both ESD protections and common mode chokes have been selected. Although, it should be noted that neither ESD protections and common mode chokes are inserted on the USB 2.0 lines routed to the miniPCIe connectors, since they are well controlled on the PCB and are thus less susceptible to EMI and electrostatic discharge events.

3.3.3 Ferrite Beads

Ferrite beads have been added on power rails in the vicinity of the ICs, specifically near the PCIe switch, Ethernet switch and RTC; they act as noise suppressors exhibiting very high impedance at high frequencies. They have been selected appropriately taking into considerations requirements of the target IC in terms of current rating, impedance and package size. These components are also exploited on the 5 V rails routed to the USB connectors and the fan connector, as protection toward surges, that may occur when connectors are attached and detached, in addition to their noise suppression capability.

3.3.4 Ethernet magnetics

An important aspect behind the implementation of the Ethernet interface is the integration of magnetics. Discrete magnetics were chosen for this application: all four Ethernet ports on the board have their own transformer array, placed between the PHY and the RJ45 connector. Its purpose is to create a high voltage barrier between the cable and the PHY, galvanically isolating the PHY from the transmission medium, as stated in Ethernet specification [40].

Two main reasons justify this requirement. First, according to the Ethernet specification, transmission up to 100 m is supported for twisted copper pairs and is even higher for fiber media. Therefore, the two object engaged in the communication may be very far apart from each other, resulting in a possible ground offset between the devices. The second goal is to prevent any failures from propagating into the board, protecting devices from surges, ESD or shorts on the high voltage rail. It must be ensured that all circuitry residing in or related to the high voltage barrier region, is only referenced to the chassis ground; hence, all LEDs and capacitors connected to the digital ground cannot reside in this region that must remain isolated from the rest of the system.

Furthermore, additional benefits arise from employing transformers to obtain galvanic isolation. They have a high common mode rejection ratio which allows only the differential voltage to get through the barrier. This ensures that any reflection caused by impedance mismatch in the differential pair is suppressed, resulting in a more robust design. In addition to this, each center tap of the transformer is separately terminated to the chassis ground through a 75 Ω resistor to prevent signal reflections, together with a high voltage capacitor (2 kV rating) which constitute additional filtering for common mode noise reduction.

On the PHY side, center taps are terminated to system ground via a capacitor, so as to avoid having leakage current flow between pairs. Refer to sheet 24 and 25 of the schematic A for the implementation described. Mapping of the magnetics outputs to RJ45 pins is shown in table 3.3.

RJ45 Pin	Signal Name	Pair
1	MX1P_A	A
2	MX1M_A	A
3	MX1P_B	B
4	MX1P_C	C
5	MX1M_C	C
6	MX1M_B	B
7	MX1P_D	D
8	MX1M_D	D

Table 3.3: Ethernet magnetics to RJ45 mapping

3.4 Mechanics

Physical features play a major role in board design. Device mounting must be reliable and components should be well aligned to guarantee robust support of add-in cards. For this purpose, miniPCIe card holders are included instead of opting for a basic screw mounting, while an M3 hole is inserted for securing the SSD as required by the PCIe M.2 Electromechanical specifications [38]. In addition to this, four M3 mounting holes electrically connected to the chassis are placed on each corner of the board. Although, they won't be used for securing the board to the enclosure as described later on in section 4.3.

The DART SoM features four mounting holes for carrier board mounting, they are plated and connected to ground. Correct positioning of these holes with respect to the three 90-pin connectors of SoM has been done creating a dedicated footprint for the module, following the information provided by the manufacturer. A mechanical solution for ensuring robustness in harsh vibration environments is suggested by the manufacturer who proposes a set of standoffs by MAC8, identified with the product number TH-1.6-1.5-M2 [55] which require M2 screws with head diameter smaller than 4 mm.

Six fiducials are positioned near three board corners, both on the front side and on the back. They are essentially markers meant for assisting pick-and-place machines during component placement in the PCB assembly phase. Two more are placed in the vicinity of the PCIe switch Ball Grid Array package. Testing the BGA pads after assembly is unfeasible since they are underneath the package and can't be accessed once the component is placed. Which is why, to address this issue, additional local fiducials are placed, ensuring accurate calibration of the assembly machine and avoiding misalignment.

Furthermore, multiple Test Points (TP) are added on specific traces to facilitate troubleshooting, measurements, debugging or simply to toggle a signal manually. They allow access to electrical signals without resorting to intrusive methods. Anticipating that testing will be done almost certainly via probe, looped type test points were chosen. The looped shape test point occupies more area with respect to basic test point pads but ensures a robust contact point. TPs are added on traces routed to the following signals:

- LED_1, LED_2, LED_3, LED_4 mapped on pins 61 to 64 of the microcontroller, aimed at monitoring waveforms when change in the LED behavior cannot be detected by eye;
- ONOFF_1V8 DART SoM on-off control signal, for turning off the module manually and verify that the signal is properly driven by the microcontroller;
- SMDAT, SMCK pins 38 and 39 of the USB Hub, to allow HUB configuration via interface and bypass the strap resistors;
- VBUSDET pin 37 of the USB Hub, to force connection renegotiation;
- TRST_L pin J9 of PCIe switch, to toggle manually during JTAG mode;
- HDMI_CN_SCL, HDMI_CN_SDA for monitoring the connection between SoM and HDMI device;

- I2C2, I2C3, I2C5 SDA and SCL, to observe communication waveforms.

All the described features reinforce the board, extend its lifetime, guarantee correct assembly and simplify testing. The result is a robust and efficient platform resilient to vibrations, mechanical and thermal stress which is often induced by harsh environmental conditions.

Chapter 4
PCB design

Once the schematic is finalized and carefully reviewed, the design is carried out by shifting focus towards the actual Printed Circuit Board.

Similarly to what was done for symbol libraries, as detailed in chapter 3, footprint libraries are thoroughly examined and altered when needed. Each footprint is compared to the mechanical drawing provided in the component datasheet and if any inconsistencies are found, it is adjusted to match it.

To prevent misalignment and spacing errors, three composite footprints were built exclusively for this application, one for the DART SoM and the other two for the miniPCIe and M.2 slots. The DART footprint incorporates three 90-pin connectors and four mounting holes while the one designed for the miniPCIe includes a 52-pin connector and card holder. The M.2 footprint contains only the 67-pin M key connector and mounting hole accurately positioned as indicated by the electromechanical specifications.

The set up continues with the configuration of PCB stack-up and design rules, described in the following section. Afterwards, components are placed and minimum board dimensions are estimated. Finally, the enclosure is picked out and the overall system is adjusted to perfectly fit.

4.1 PCB Stack-up and design rules

A 6-layer stack-up configuration was chosen, where the outer copper layers are dedicated to controlled and differential impedance traces, while the innermost layers are for power distribution and non critical signals, mostly controls and simple logic, nothing high speed or that requires controlled impedance. The two remaining layers serve as ground planes. This stack-up ensures tight coupling between the ground planes and the controlled impedance layers since they are separated by a small distance and exhibit lower inductance. Doing so, interference is reduced, layer count and reliability are optimized.

Thickness data shown in figure 4.1, is obtained from build up information provided by Eurocircuits [56] manufacturer which has been chosen for board fabrication and assembly. The expected PCB total thickness is of 1.6 mm although it may vary by $\pm 10\%$ due to fabrication tolerances.

As for design rules instead, minimum width and clearance, via diameters and other characteristics are set to the values indicated by Eurocircuits PCB Design classification for pattern class 6 and drill class E. Where pattern and drills classes are measures of PCB manufacturability.

4.2 Component Placement

The final step ultimately involves careful component placement to ease routing and trace management, while maintaining functional grouping of components, also taking into account mechanical constraints and accessibility. The resulting silkscreen and footprints

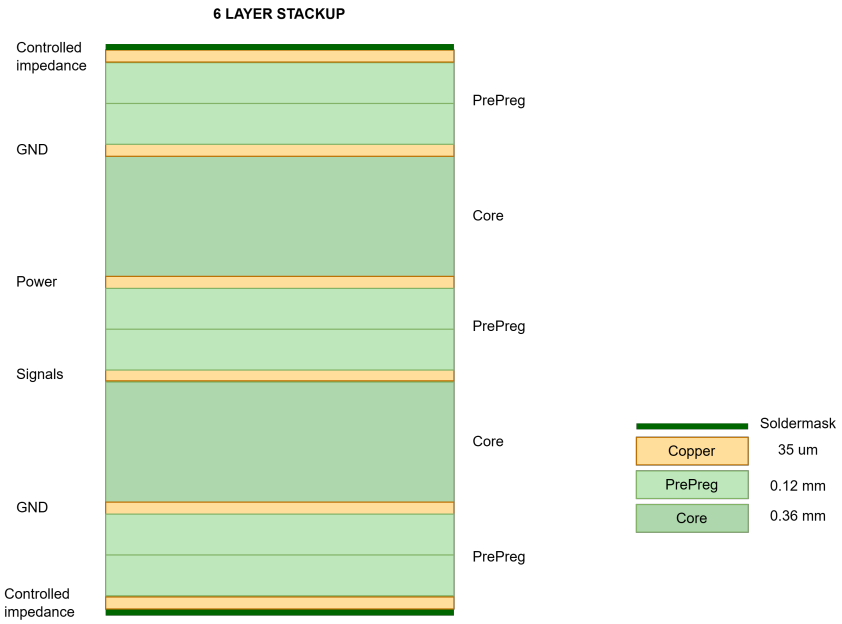


Figure 4.1: PCB Stack-up

layout overview can be found in appendix B.

The placement procedure begins with defining the board outline. After estimating the minimum required dimensions based on the space occupied by the connectors that need to be accessible from the front panel, standard sizes corresponding to the Double Eurocard are chosen. Therefore, a 233 × 160 mm rectangle is outlined on the Edge cuts layer.

Initially, all connectors are placed along the longest edge of the board outline. The aim is to obtain a compact and convenient system were all user accessible objects are placed on one side only, to ease installation and maintenance, figure 4.4. Proper spacing is introduced between the ports, to avoid any connection nuisance that may arise due to additional space taken up by the cable mating connector plastic housing. On top of this, front panel accessible connectors are placed so as to extend beyond the board edge by 4 mm. As a result, cables can be correctly attached when the 2 mm thick front panel is fastened.

Other components are now placed, starting from the largest ones, figure 4.2. The microSD and SIM card slots are placed on the board edge opposite to the front panel, since these cards are occasionally accessed, usually for initial setup or maintenance.

Magnetics are then placed close to the RJ45 connectors, the DART SoM and miniPCIe slots are positioned on the right side, as well as the M.2 slot.

Power input connector is positioned on the bottom left side, where also power status LEDs, the DIP switch and several headers are inserted. Reset pushbuttons are placed in the vicinity of the device they control, namely the microcontroller and the DART SoM. Ultimately, the battery socket and buzzer are situated on the center left side also.

Through-hole test points are arranged where enough vertical clearance is available to

facilitate probe insertion, while avoiding critical areas that are reserved for differential trace routing.

After placement of all connectors, modules and sockets on the top side of the board is completed, small size components are arranged on both top and bottom sides. Positioning starts from devices close to downstream ports and connectors, then follows the connections logical flow until the upstream control interface is reached. Functional arrangement is obtained with the help of the ratsnest tool available in KiCad which highlights all connections implemented in the schematic on the layout view. Most ICs such as the Ethernet switch, PCIe switch and USB Hubs, are placed on the bottom side, figure 4.3, while bypass capacitors and configuration resistors are on the top side, aligned with the corresponding IC.

At last, power section is located close to the input power connector on the bottom side in the lower right corner. All remaining passive components are placed on the bottom side of the board. It should be noted that heavy devices or more precisely, components with small solder footprints, are placed on the top side to avoid component displacement that may happen during assembly if positioned on the bottom side instead. Components with larger solder area (i.e. PCB area where board and device are physically contacted through solder) experience greater surface tension, this helps anchor the device to the board. As consequence, the component remains firmly attached even during reflow for top assembly. Such configuration results in a more reliable and robust platform with high assembly yield.

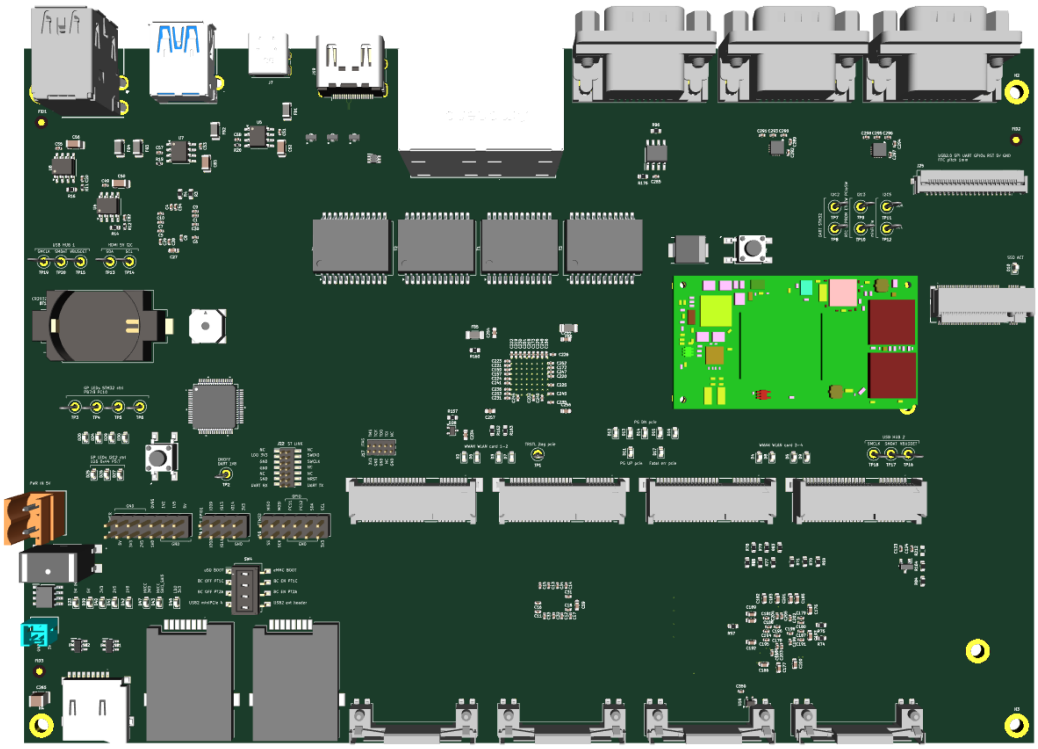


Figure 4.2: Board 3D view: Top

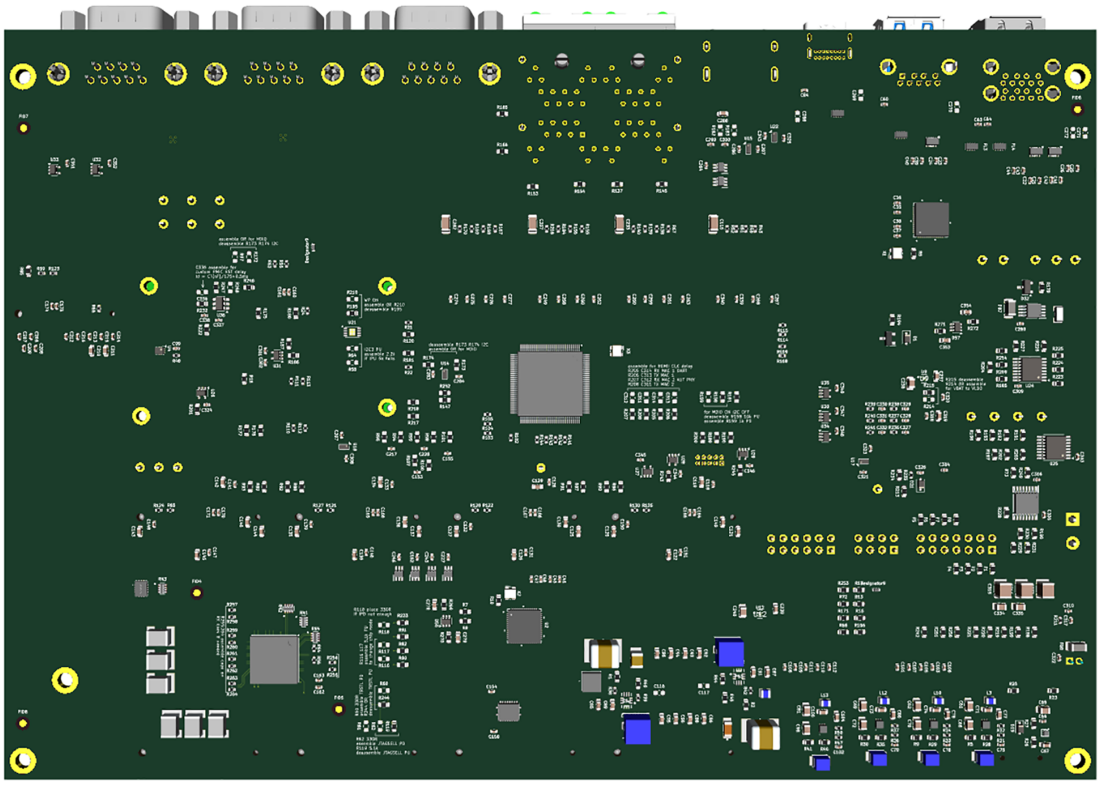


Figure 4.3: Board 3D view: Bottom

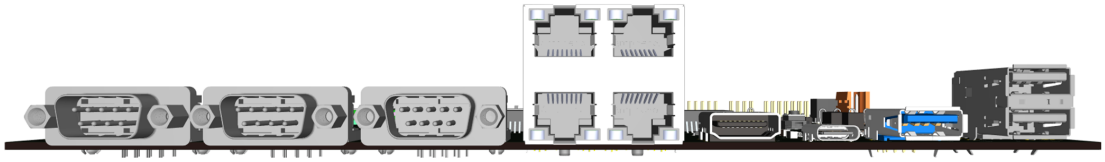


Figure 4.4: Board 3D view: Front panel

4.3 Final dimensions and enclosure: the overall system

Having completed component placement, board dimensions are finalized and, at this point, the enclosure can be picked out.

The selected enclosure is a METTEC Desk case by METCASE [57]. It is entirely made of aluminum, lightweight yet robust, with high thermal conductivity which makes it well suited for the conductive cooling strategy adopted in this design. The case features a removable top panel, shielded internal surfaces and side extrusions for PCB support. Its dimensions are reported in table 4.1.

A slightly bigger enclosure was chosen to allow seamless incorporation of all objects that constitute the overall system. Therefore, PCB dimensions are adapted to perfectly fit the enclosure, exploiting the side extrusion to support the final platform, figure 4.5. The board area is positioned on the right side of the platform, while, on the left, space is reserved for securing the enclosed DC-DC converter, dimensions in table 4.2. Additional room on the remaining side of the platform, opposite to the front panel, is dedicated to the possible insertion of a miniPCIe adapter for non standard pinout add-in cads. The area occupied by the adapter is estimated to be around 40 × 80 mm which corresponds to the rounded footprint dimensions 33.6 × 61 mm comprising both card connector and holder. Front panel screws are also taken into account when defining the PCB outline; for this purpose, a 5 × 10 mm PCB area is removed on both corners of the front side .

The system has been engineered so as to allow the PCB panel holding all external modules to slide through the case's side extrusions. In this way, the platform can be easily pulled out of the enclosure by removing the front panel without having to detach any device first. Board access is thus greatly simplified, and besides this, having a single platform that accommodates all items, also contributes to improve robustness while maintaining a compact system.

	Length [mm]	**Width** [mm]	**Height** [mm]
Internal	306	233	61 (front panel)
External	350	250	85

Table 4.1: Enclosure dimensions

	Length [mm]	**Width** [mm]	**Height** [mm]
RSD-60G-5	60	128	25
Board area	233	160	1.6

Table 4.2: RSD-60G-5 enclosed converter and Double Eurocard dimensions

Moreover, the seven SMA antenna connectors will be mounted on the front panel above the connectors, together with the anti-vandal pushbutton for power on, which features an integrated LED, and a DC jack 2.1 × 5.5 mm designated for the 12 V - 24 V power input. Connection between the enclosed DC-DC converter and the power input is managed by inserting the power on pushbutton inbetween them, thus when the latter is disabled, the power flow is cut off.

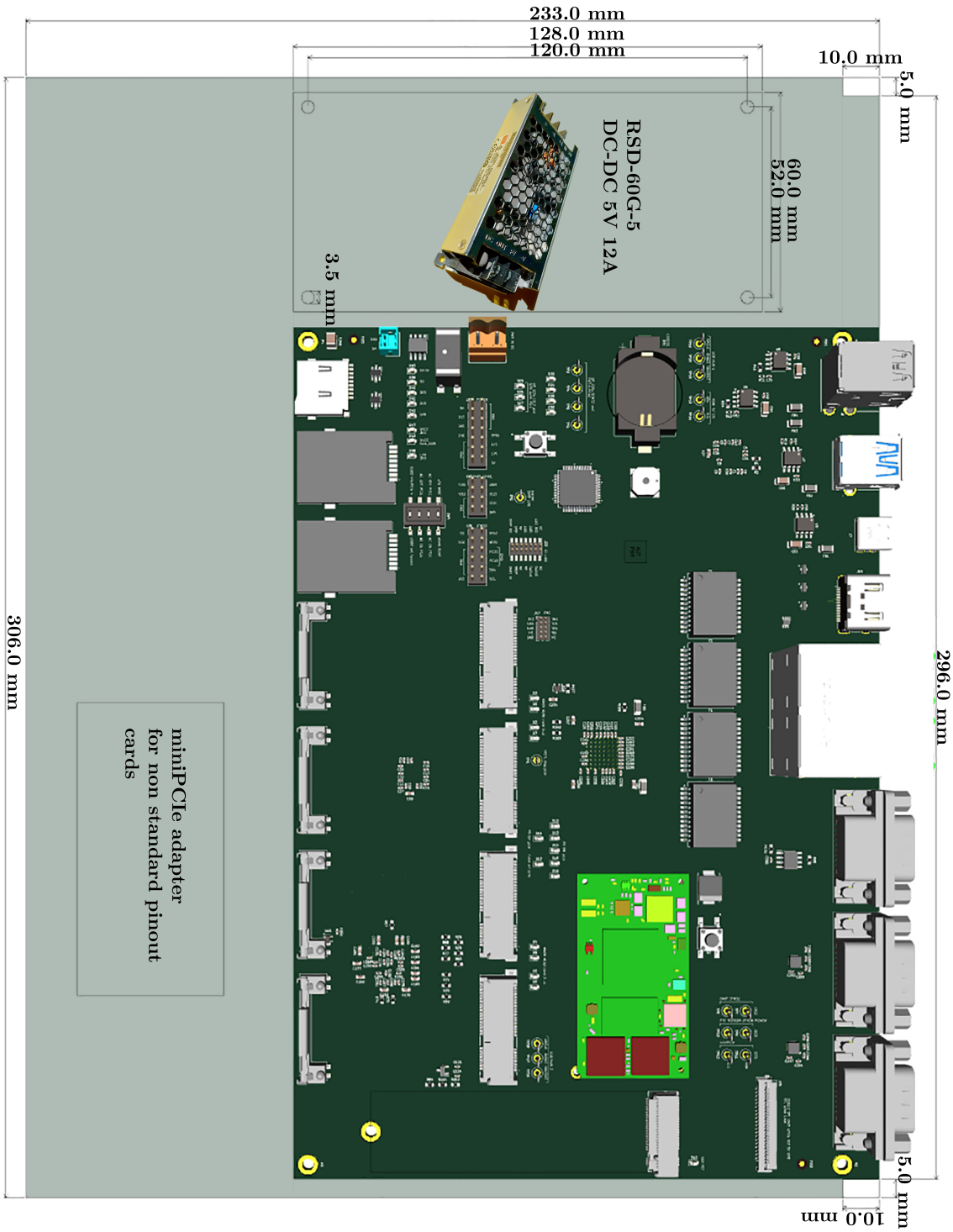


Figure 4.5: PCB top view: dimensions designed to fit the selected enclosure

Chapter 5
Conclusions

This thesis describes the design methodology and implementation of an embedded board for vehicular connectivity, starting from a set of specifications, moving on to hardware components selection and printed circuit board layout up to component placement.

The overall platform designed presents a solution to lack of customization, limited number of connectors and plug-in slots for connectivity modules on commercial platforms. The final result is an open source embedded board designed to accommodate off-the-shelf modules and support wireless connectivity between vehicles and networked devices in general. It addresses the connected vehicle ecosystem's demand for a low cost, open source hardware platform, interoperable, reliable, with low latency and multiple interfaces support.

Specifically designed to equip vehicles with capabilities for engaging in V2X communications, it operates as an On-Board-Unit, built for transmitting, collecting and storing real-time data, that provides the necessary interfaces and processing power to enable vehicular connectivity. It serves as a cornerstone for establishing a system that goes beyond traditional sensors, playing a pivotal role in attaining more reliable, resource efficient and environmentally conscious traffic interactions.

All stages of the design process are thoroughly detailed in this document, which illustrates the chain of thought and decisions that brought to the finalized system starting from the bare concept, also including considerations on physical aspects such as mechanics and enclosure fitting. To summarize, once the concept was drafted and the initial requirements were refined, the DART-MX8M-PLUS System-on-Module by Variscite was selected as core processing module due to its longevity support, small form factor and its capability to operate with Yocto built distributions, namely custom Linux-based systems. Final specifications, block diagram, a list of ICs and passive components are extracted from the preliminary architecture draft, which constitute the baseline for schematic design. Subsequently, the design was implemented using KiCad EDA tools. To start with, the electrical structure was outlined developing the schematic which illustrates all functional connections between components. Afterwards, components were carefully placed according to their functional grouping, to ease routing and trace management, while also taking into account mechanical constraints and accessibility. Ultimately, board dimensions were adjusted to perfectly fit the selected enclosure and integrate all objects that constitute the overall platform.

Further development of the project is planned as part of future work which will include routing completion, the generation of PCB manufacturing files for prototype fabrication and firmware design.

In conclusion, the designed platform meets all the objectives set at the beginning of the project, it's robust, compact, powerful and can be effortlessly integrated in already circulating vehicles. It supports all interfaces required for taking part in V2X communications, which play an essential role in the development of connected vehicle systems whose ultimate intent is to achieve safer interactions, improved mobility, reduced pollution and energy saving.

Appendix A
Schematic

Sheet 1 ROOT
Sheet 2 DART POWER CTRL JTAG
Sheet 3 DART ETHERNET
Sheet 4 DART PCIe SD USB
Sheet 5 DART LVDS DSI HDMI
Sheet 6 DART I2C3 CAN AUDIO GPIO
Sheet 7 DART UART I2C GPIO
Sheet 8 Power distribution 1
Sheet 9 Power distribution 2
Sheet 10 Power distribution 3
Sheet 11 uCU
Sheet 12 uCU 2
Sheet 13 HUB USB type A + C
Sheet 14 USB type A + C
Sheet 15 HUB USB miniPCIe
Sheet 16 miniPCIe 1
Sheet 17 miniPCIe 2
Sheet 18 PCIe OSC M.2
Sheet 19 PCIe switch 1
Sheet 20 PCIe switch 2
Sheet 21 PCIe switch 3
Sheet 22 uSD CAN RTC EEPROM
Sheet 23 ETHERNET switch 1
Sheet 24 ETHERNET switch 2
Sheet 25 Ethernet - SoM integrated PHY
Sheet 26 HDMI
Sheet 27 RS232 Buzzer
Sheet 28 Headers 1
Sheet 29 I2C expander
Sheet 30 Mechanics

J1 J2 J3 DART-MX8M-PLUS SoM

DART POWER CTRL JTAG
File: dart_pow_ctrl.kicad_sch

DART ETHERNET
File: dart_eth.kicad_sch

DART PCIe SD USB
File: dart_pcie_sd_usb.kicad_sch

DART LVDS DSI HDMI
File: dart_display.kicad_sch

DART I2C3 CAN AUDIO GPIO
File: dart_aud_gp.kicad_sch

DART UART I2C GPIO
File: dart_uart_qspi_ecspi.kicad_sch

Power distribution 1
File: pwr_distrib.kicad_sch

Power Distribution 2
File: pwr_distrib_3.kicad_sch

Power distribution 3
File: pwr_distrib_2.kicad_sch

uCU
File: uC_ctrl.kicad_sch

uCU 2
File: uCU_2.kicad_sch

aut eth substitute LDO 1V
not req w NDA aut eth IC

HUB USB type A+C
File: carrier_usbhubAC.kicad_sch

USB type A+C
File: carrier_usbAC.kicad_sch

HUB USB miniPCIe
File: carrier_usbhub_miniPCIe.kicad_sch

HDMI
File: crrier_hdmi_varie.kicad_sch

uSD CAN RTC EEPROM
File: carrier_usd_hdmi.kicad_sch

PCIe switch 1
File: carrier_pcie.kicad_sch

PCIe switch 2
File: carrier_pcie2.kicad_sch

PCIe switch 3
File: carrier_pcie4.kicad_sch

RS232 Buzzer
File: carrier_uart.kicad_sch

Headers 1
File: ext_headers_1.kicad_sch

miniPCIe 1
File: miniPCIe.kicad_sch

miniPCIe 2
File: miniPCIe2.kicad_sch

PCIe OSC M.2
File: carrier_pcie3.kicad_sch

I2C expander
File: i2c_exp.kicad_sch

ETHERNET switch 1
File: carrier_eth2.kicad_sch

ETHERNET switch 2
File: carrier_eth.kicad_sch

Ethernet – SoM integrated PHY
File: carrier_eth3.kicad_sch

Mechanics
File: aut_enet2.kicad_sch

layout note

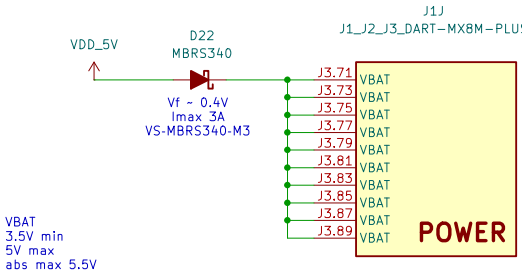
firmware note

Sofia Giannoccaro s314083
Politecnico di Torino

Sheet: /
File: OBU_1.kicad_sch

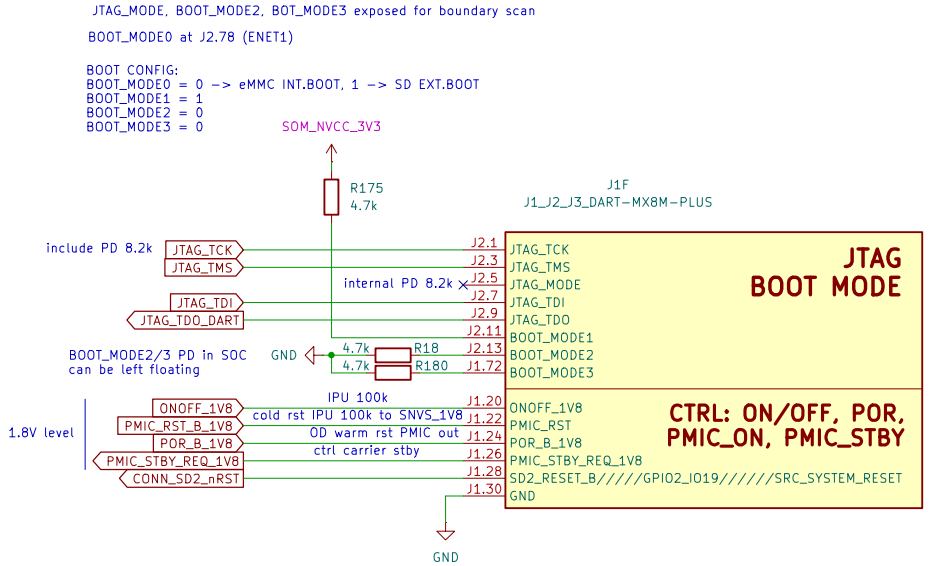
Title: OBU V2X board

Size: A4	Date: 2025-07-18	**Rev: 1**
KiCad E.D.A. 8.0.2		Id: 1/30



VBAT
3.5V min
5V max
abs max 5.5V

DART estimated power consumption:
3W



DART ctrl notes:

ONOFF
In OFF mode: brief connection to GND causes the internal power management state machine to change state to ON.
In ON mode: brief connection to GND generates an interrupt (intended to initiate a software-controllable power-down).
To Force OFF: approximate 5 second or more connection to GND

PMIC_RST_B
Pull low to hold DART internal regulators OFF
Pulse low for cold reboot.
As a PMIC input can be programmed to Cold/Warm/No reset; Default Cold reset;

POR_B
Pull low to hold SOC in reset state
Pulse low for Warm reboot.

PMIC_STB_REQ
Can be used externally to control carrier board power for standby state; Active-high output for going to SUSPEND state;
Transition 0 to 1: Enter Standby
Transition 1 to 0: Wake up from standby

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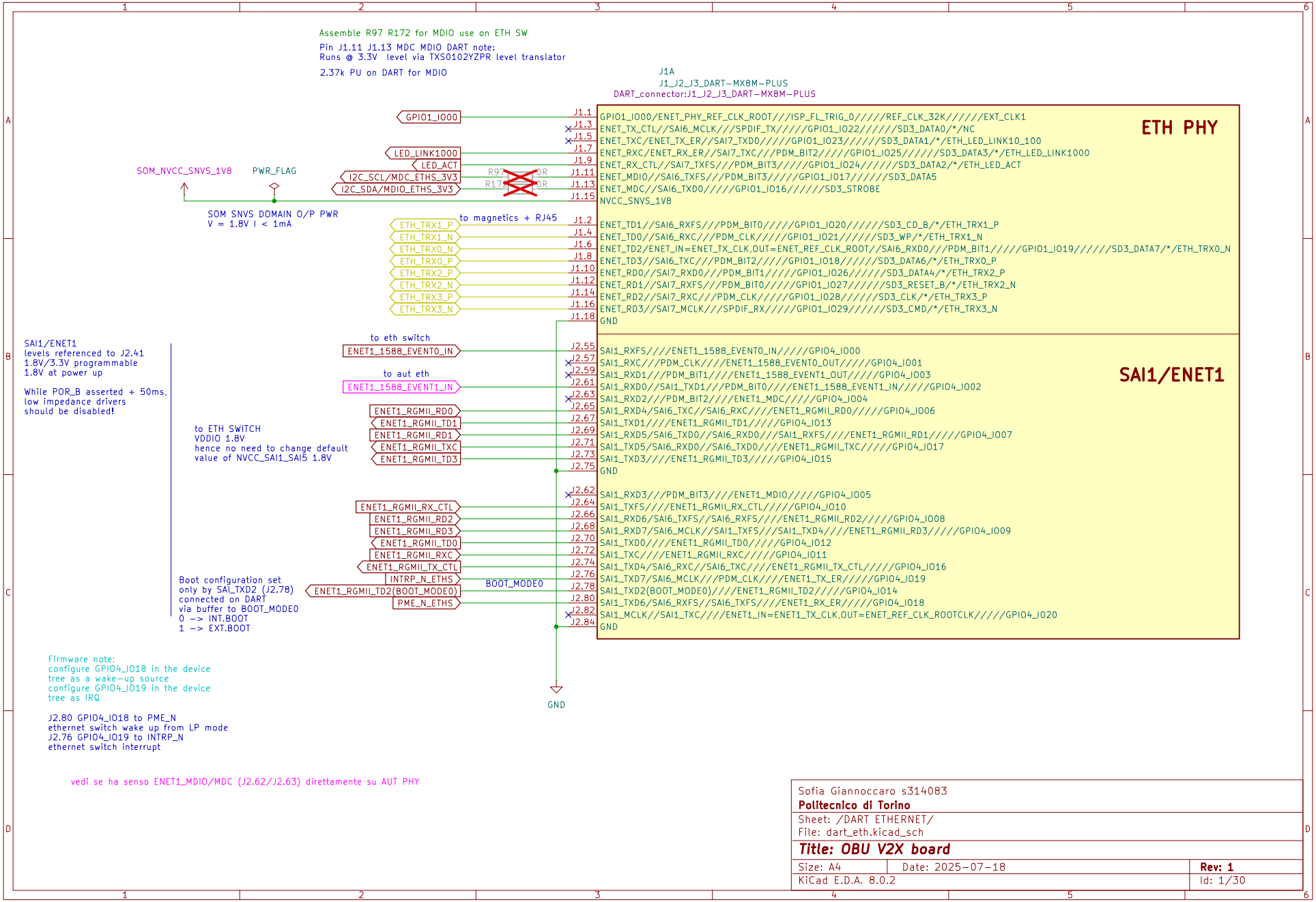
Politecnico di Torino
Sheet: /DART POWER CTRL JTAG/
File: dart_pow_ctrl.kicad_sch

Title: OBU V2X board

Size: A4	Date: 2025-07-18	**Rev: 1**
KiCad E.D.A. 8.0.2		Id: 1/30


Assemble R97 R172 for MDIO use on ETH SW
Pin J1.11 J1.13 MDC MDIO DART note:
Runs @ 3.3V level via TXS0102YZPR level translator
2.37k PU on DART for MDIO
J1A
J1_J2_J3_DART-MX8M-PLUS
DART_connector:J1_J2_J3_DART-MX8M-PLUS
ETH PHY
SAI1/ENET1
GPIO1_IO00/ENET_PHY_REF_CLK_ROOT///ISP_FL_TRIG_0/////REF_CLK_32K//////EXT_CLK1
ENET_TX_CTL//SAI6_MCLK///SPDIF_TX/////GPIO1_IO22//////SD3_DATA0/*/NC
ENET_TXC/ENET_TX_ER//SAI7_TXD0/////GPIO1_IO23//////SD3_DATA1/*/ETH_LED_LINK10_100
ENET_RXC/ENET_RX_ER//SAI7_TXC///PDM_BIT2/////GPIO1_IO25//////SD3_DATA3/*/ETH_LED_LINK1000
ENET_RX_CTL//SAI7_TXFS///PDM_BIT3/////GPIO1_IO24//////SD3_DATA2/*/ETH_LED_ACT
ENET_MDIO//SAI6_TXFS///PDM_BIT3/////GPIO1_IO17//////SD3_DATA5
ENET_MDC//SAI6_TXD0/////GPIO1_IO16//////SD3_STROBE
NVCC_SNVS_1V8
ENET_TD1//SAI6_RXFS///PDM_BIT0/////GPIO1_IO20//////SD3_CD_B/*/ETH_TRX1_P
ENET_TD0//SAI6_RXC///PDM_CLK/////GPIO1_IO21//////SD3_WP/*/ETH_TRX1_N
ENET_TD2/ENET_IN=ENET_TX_CLK,OUT=ENET_REF_CLK_ROOT//SAI6_RXD0///PDM_BIT1/////GPIO1_IO19//////SD3_DATA7/*/ETH_TRX0_N
ENET_TD3//SAI6_TXC///PDM_BIT2/////GPIO1_IO18//////SD3_DATA6/*/ETH_TRX0_P
ENET_RD0//SAI7_RXD0///PDM_BIT1/////GPIO1_IO26//////SD3_DATA4/*/ETH_TRX2_P
ENET_RD1//SAI7_RXFS///PDM_BIT0/////GPIO1_IO27//////SD3_RESET_B/*/ETH_TRX2_N
ENET_RD2//SAI7_RXC///PDM_CLK/////GPIO1_IO28//////SD3_CLK/*/ETH_TRX3_P
ENET_RD3//SAI7_MCLK///SPDIF_RX/////GPIO1_IO29//////SD3_CMD/*/ETH_TRX3_N
GND
SAI1_RXFS////ENET1_1588_EVENT0_IN/////GPIO4_IO00
SAI1_RXC///PDM_CLK////ENET1_1588_EVENT0_OUT/////GPIO4_IO01
SAI1_RXD1///PDM_BIT1////ENET1_1588_EVENT1_OUT/////GPIO4_IO03
SAI1_RXD0//SAI1_TXD1///PDM_BIT0////ENET1_1588_EVENT1_IN/////GPIO4_IO02
SAI1_RXD2///PDM_BIT2////ENET1_MDC/////GPIO4_IO04
SAI1_RXD4/SAI6_TXC//SAI6_RXC////ENET1_RGMII_RD0/////GPIO4_IO06
SAI1_TXD1////ENET1_RGMII_TD1/////GPIO4_IO13
SAI1_RXD5/SAI6_TXD0//SAI6_RXD0///SAI1_RXFS////ENET1_RGMII_RD1/////GPIO4_IO07
SAI1_TXD5/SAI6_RXD0//SAI6_TXD0////ENET1_RGMII_TXC/////GPIO4_IO17
SAI1_TXD3////ENET1_RGMII_TD3/////GPIO4_IO15
GND
SAI1_RXD3///PDM_BIT3////ENET1_MDIO/////GPIO4_IO05
SAI1_TXFS////ENET1_RGMII_RX_CTL/////GPIO4_IO10
SAI1_RXD6/SAI6_TXFS//SAI6_RXFS////ENET1_RGMII_RD2/////GPIO4_IO08
SAI1_RXD7/SAI6_MCLK//SAI1_TXFS///SAI1_TXD4////ENET1_RGMII_RD3/////GPIO4_IO09
SAI1_TXD0////ENET1_RGMII_TD0/////GPIO4_IO12
SAI1_TXC////ENET1_RGMII_RXC/////GPIO4_IO11
SAI1_TXD4/SAI6_RXC//SAI6_TXC////ENET1_RGMII_TX_CTL/////GPIO4_IO16
SAI1_TXD7/SAI6_MCLK///PDM_CLK////ENET1_TX_ER/////GPIO4_IO19
SAI1_TXD2(BOOT_MODE0)////ENET1_RGMII_TD2/////GPIO4_IO14
SAI1_TXD6/SAI6_RXFS//SAI6_TXFS////ENET1_RX_ER/////GPIO4_IO18
SAI1_MCLK//SAI1_TXC////ENET1_IN=ENET1_TX_CLK,OUT=ENET_REF_CLK_ROOTCLK/////GPIO4_IO20
GND
GPIO1_IO00
LED_LINK1000
LED_ACT
I2C_SCL/MDC_ETHS_3V3
I2C_SDA/MDIO_ETHS_3V3
R97 0R
R172 0R
SOM_NVCC_SNVS_1V8
PWR_FLAG
SOM SNVS DOMAIN O/P PWR
V = 1.8V I < 1mA
to magnetics + RJ45
ETH_TRX1_P
ETH_TRX1_N
ETH_TRX0_N
ETH_TRX0_P
ETH_TRX2_P
ETH_TRX2_N
ETH_TRX3_P
ETH_TRX3_N
SAI1/ENET1
levels referenced to J2.41
1.8V/3.3V programmable
1.8V at power up
While POR_B asserted + 50ms,
low impedance drivers
should be disabled!
to eth switch
ENET1_1588_EVENT0_IN
to aut eth
ENET1_1588_EVENT1_IN
ENET1_RGMII_RD0
ENET1_RGMII_TD1
ENET1_RGMII_RD1
ENET1_RGMII_TXC
ENET1_RGMII_TD3
to ETH SWITCH
VDDIO 1.8V
hence no need to change default
value of NVCC_SAI1_SAI5 1.8V
ENET1_RGMII_RX_CTL
ENET1_RGMII_RD2
ENET1_RGMII_RD3
ENET1_RGMII_TD0
ENET1_RGMII_RXC
ENET1_RGMII_TX_CTL
INTRP_N_ETHS
ENET1_RGMII_TD2(BOOT_MODE0)
PME_N_ETHS
BOOT_MODE0
Boot configuration set
only by SAI_TXD2 (J2.78)
connected on DART
via buffer to BOOT_MODE0
0 -> INT.BOOT
1 -> EXT.BOOT
GND
Firmware note:
configure GPIO4_IO18 in the device
tree as a wake-up source
configure GPIO4_IO19 in the device
tree as IRQ
J2.80 GPIO4_IO18 to PME_N
ethernet switch wake up from LP mode
J2.76 GPIO4_IO19 to INTRP_N
ethernet switch interrupt
vedi se ha senso ENET1_MDIO/MDC (J2.62/J2.63) direttamente su AUT PHY
Sofia Giannoccaro s314083
Politecnico di Torino
Sheet: /DART ETHERNET/
File: dart_eth.kicad_sch
Title: OBU V2X board
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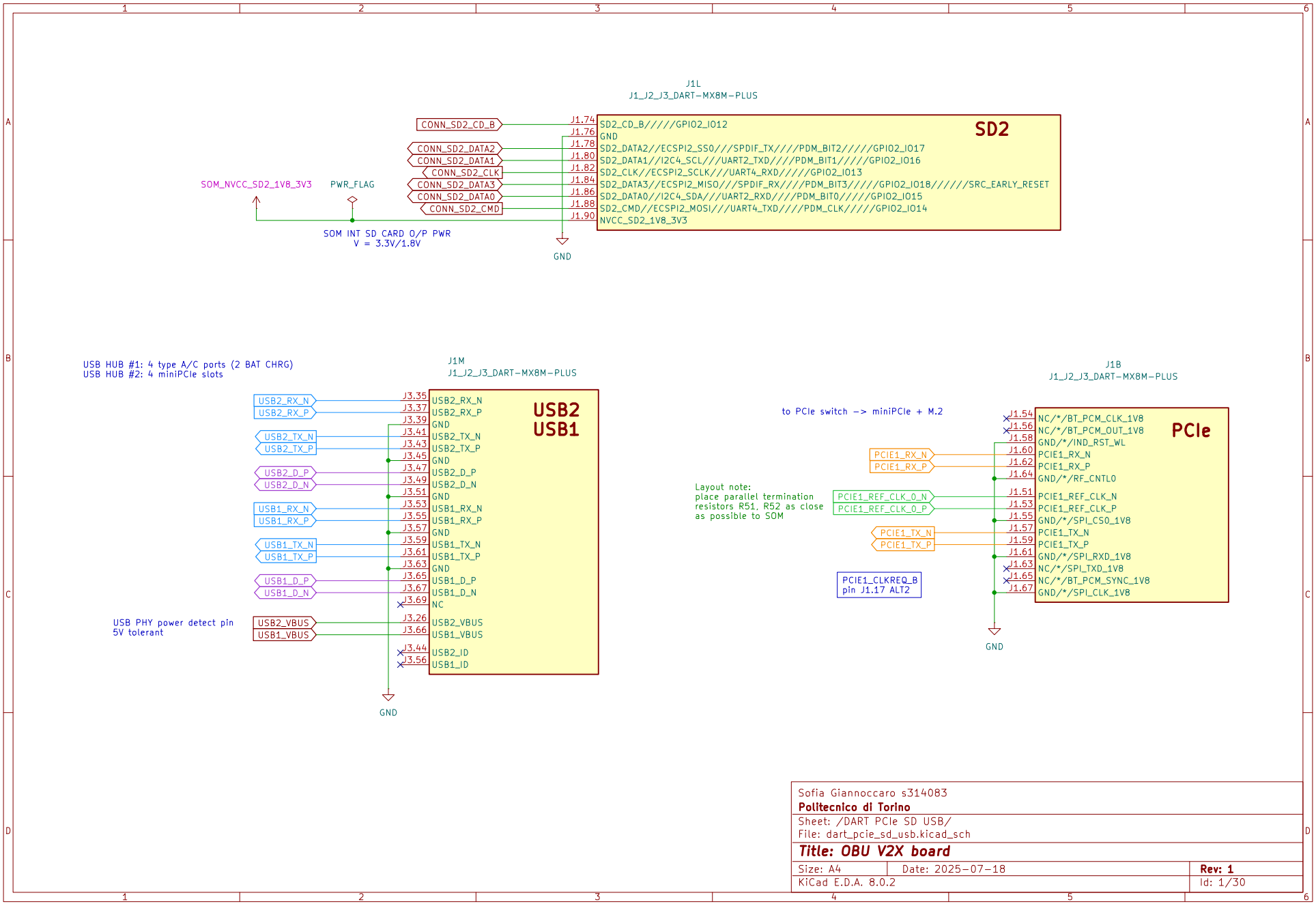
J1L
J1_J2_J3_DART-MX8M-PLUS
SD2
CONN_SD2_CD_B
CONN_SD2_DATA2
CONN_SD2_DATA1
CONN_SD2_CLK
CONN_SD2_DATA3
CONN_SD2_DATA0
CONN_SD2_CMD
J1.74 SD2_CD_B/////GPIO2_IO12
J1.76 GND
J1.78 SD2_DATA2//ECSPI2_SS0///SPDIF_TX////PDM_BIT2/////GPIO2_IO17
J1.80 SD2_DATA1//I2C4_SCL///UART2_TXD////PDM_BIT1/////GPIO2_IO16
J1.82 SD2_CLK//ECSPI2_SCLK///UART4_RXD/////GPIO2_IO13
J1.84 SD2_DATA3//ECSPI2_MISO///SPDIF_RX////PDM_BIT3/////GPIO2_IO18//////SRC_EARLY_RESET
J1.86 SD2_DATA0//I2C4_SDA///UART2_RXD////PDM_BIT0/////GPIO2_IO15
J1.88 SD2_CMD//ECSPI2_MOSI///UART4_TXD////PDM_CLK/////GPIO2_IO14
J1.90 NVCC_SD2_1V8_3V3
SOM_NVCC_SD2_1V8_3V3
PWR_FLAG
SOM INT SD CARD O/P PWR
V = 3.3V/1.8V
GND
USB HUB #1: 4 type A/C ports (2 BAT CHRG)
USB HUB #2: 4 miniPCIe slots
J1M
J1_J2_J3_DART-MX8M-PLUS
USB2
USB1
USB2_RX_N
USB2_RX_P
USB2_TX_N
USB2_TX_P
USB2_D_P
USB2_D_N
USB1_RX_N
USB1_RX_P
USB1_TX_N
USB1_TX_P
USB1_D_P
USB1_D_N
J3.35 USB2_RX_N
J3.37 USB2_RX_P
J3.39 GND
J3.41 USB2_TX_N
J3.43 USB2_TX_P
J3.45 GND
J3.47 USB2_D_P
J3.49 USB2_D_N
J3.51 GND
J3.53 USB1_RX_N
J3.55 USB1_RX_P
J3.57 GND
J3.59 USB1_TX_N
J3.61 USB1_TX_P
J3.63 GND
J3.65 USB1_D_P
J3.67 USB1_D_N
J3.69 NC
USB PHY power detect pin
5V tolerant
USB2_VBUS
USB1_VBUS
J3.26 USB2_VBUS
J3.66 USB1_VBUS
J3.44 USB2_ID
J3.56 USB1_ID
GND
J1B
J1_J2_J3_DART-MX8M-PLUS
to PCIe switch -> miniPCIe + M.2
PCIe
PCIE1_RX_N
PCIE1_RX_P
PCIE1_REF_CLK_0_N
PCIE1_REF_CLK_0_P
PCIE1_TX_N
PCIE1_TX_P
Layout note:
place parallel termination
resistors R51, R52 as close
as possible to SOM
PCIE1_CLKREQ_B
pin J1.17 ALT2
J1.54 NC/*/BT_PCM_CLK_1V8
J1.56 NC/*/BT_PCM_OUT_1V8
J1.58 GND/*/IND_RST_WL
J1.60 PCIE1_RX_N
J1.62 PCIE1_RX_P
J1.64 GND/*/RF_CNTL0
J1.51 PCIE1_REF_CLK_N
J1.53 PCIE1_REF_CLK_P
J1.55 GND/*/SPI_CS0_1V8
J1.57 PCIE1_TX_N
J1.59 PCIE1_TX_P
J1.61 GND/*/SPI_RXD_1V8
J1.63 NC/*/SPI_TXD_1V8
J1.65 NC/*/BT_PCM_SYNC_1V8
J1.67 GND/*/SPI_CLK_1V8
GND
Sofia Giannoccaro s314083
Politecnico di Torino
Sheet: /DART PCIe SD USB/
File: dart_pcie_sd_usb.kicad_sch
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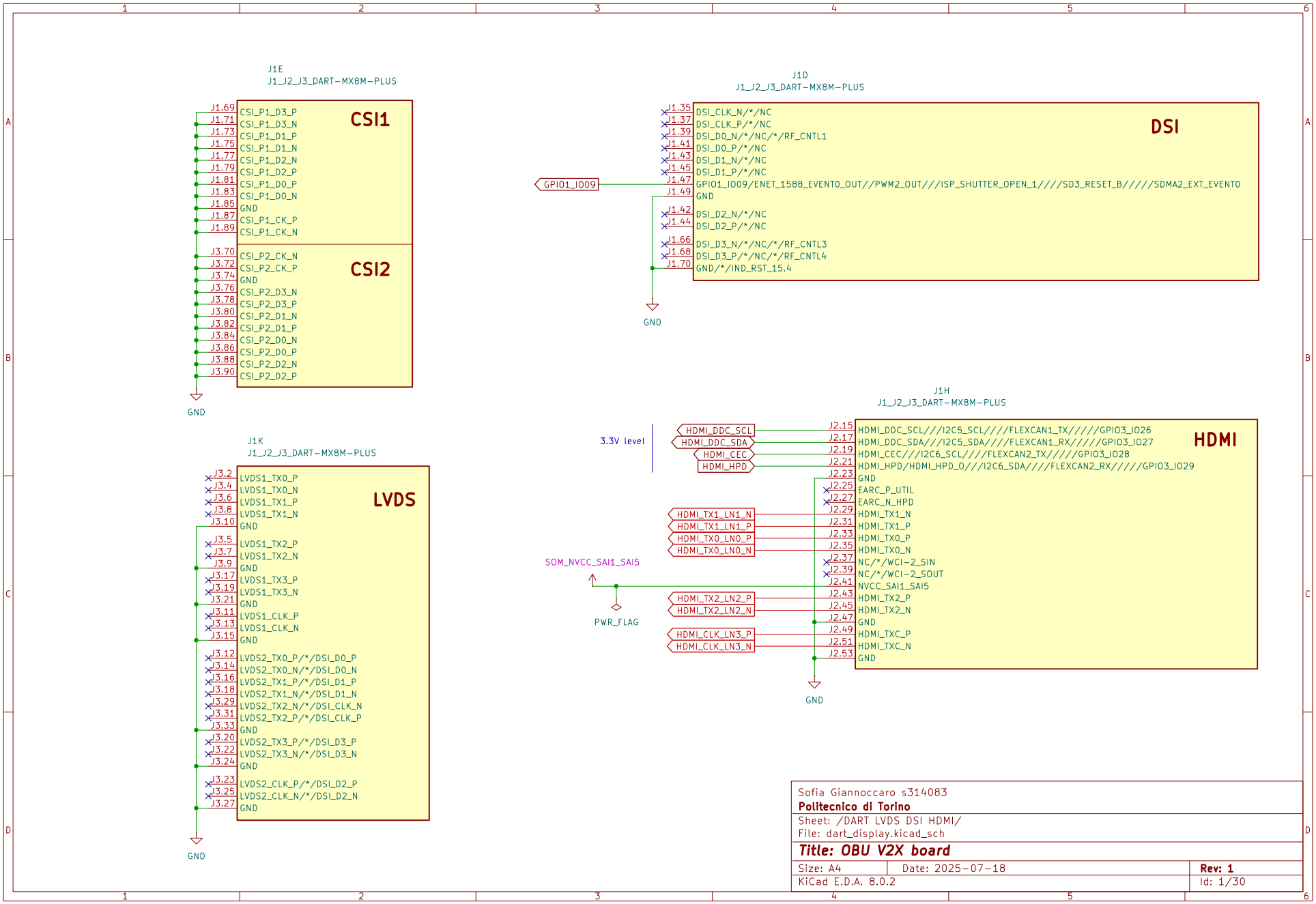
J1E
J1_J2_J3_DART-MX8M-PLUS
CSI1
J1.69 CSI_P1_D3_P
J1.71 CSI_P1_D3_N
J1.73 CSI_P1_D1_P
J1.75 CSI_P1_D1_N
J1.77 CSI_P1_D2_N
J1.79 CSI_P1_D2_P
J1.81 CSI_P1_D0_P
J1.83 CSI_P1_D0_N
J1.85 GND
J1.87 CSI_P1_CK_P
J1.89 CSI_P1_CK_N
CSI2
J3.70 CSI_P2_CK_N
J3.72 CSI_P2_CK_P
J3.74 GND
J3.76 CSI_P2_D3_N
J3.78 CSI_P2_D3_P
J3.80 CSI_P2_D1_N
J3.82 CSI_P2_D1_P
J3.84 CSI_P2_D0_N
J3.86 CSI_P2_D0_P
J3.88 CSI_P2_D2_N
J3.90 CSI_P2_D2_P
GND
J1D
J1_J2_J3_DART-MX8M-PLUS
DSI
J1.35 DSI_CLK_N/*/NC
J1.37 DSI_CLK_P/*/NC
J1.39 DSI_D0_N/*/NC/*/RF_CNTL1
J1.41 DSI_D0_P/*/NC
J1.43 DSI_D1_N/*/NC
J1.45 DSI_D1_P/*/NC
GPIO1_IO09
J1.47 GPIO1_IO09/ENET_1588_EVENT0_OUT//PWM2_OUT///ISP_SHUTTER_OPEN_1////SD3_RESET_B/////SDMA2_EXT_EVENT0
J1.49 GND
J1.42 DSI_D2_N/*/NC
J1.44 DSI_D2_P/*/NC
J1.66 DSI_D3_N/*/NC/*/RF_CNTL3
J1.68 DSI_D3_P/*/NC/*/RF_CNTL4
J1.70 GND/*/IND_RST_15.4
GND
J1K
J1_J2_J3_DART-MX8M-PLUS
LVDS
J3.2 LVDS1_TX0_P
J3.4 LVDS1_TX0_N
J3.6 LVDS1_TX1_P
J3.8 LVDS1_TX1_N
J3.10 GND
J3.5 LVDS1_TX2_P
J3.7 LVDS1_TX2_N
J3.9 GND
J3.17 LVDS1_TX3_P
J3.19 LVDS1_TX3_N
J3.21 GND
J3.11 LVDS1_CLK_P
J3.13 LVDS1_CLK_N
J3.15 GND
J3.12 LVDS2_TX0_P/*/DSI_D0_P
J3.14 LVDS2_TX0_N/*/DSI_D0_N
J3.16 LVDS2_TX1_P/*/DSI_D1_P
J3.18 LVDS2_TX1_N/*/DSI_D1_N
J3.29 LVDS2_TX2_N/*/DSI_CLK_N
J3.31 LVDS2_TX2_P/*/DSI_CLK_P
J3.33 GND
J3.20 LVDS2_TX3_P/*/DSI_D3_P
J3.22 LVDS2_TX3_N/*/DSI_D3_N
J3.24 GND
J3.23 LVDS2_CLK_P/*/DSI_D2_P
J3.25 LVDS2_CLK_N/*/DSI_D2_N
J3.27 GND
GND
J1H
J1_J2_J3_DART-MX8M-PLUS
HDMI
3.3V level
HDMI_DDC_SCL
HDMI_DDC_SDA
HDMI_CEC
HDMI_HPD
J2.15 HDMI_DDC_SCL///I2C5_SCL////FLEXCAN1_TX/////GPIO3_IO26
J2.17 HDMI_DDC_SDA///I2C5_SDA////FLEXCAN1_RX/////GPIO3_IO27
J2.19 HDMI_CEC///I2C6_SCL////FLEXCAN2_TX/////GPIO3_IO28
J2.21 HDMI_HPD/HDMI_HPD_O///I2C6_SDA////FLEXCAN2_RX/////GPIO3_IO29
J2.23 GND
J2.25 EARC_P_UTIL
J2.27 EARC_N_HPD
HDMI_TX1_LN1_N
HDMI_TX1_LN1_P
HDMI_TX0_LN0_P
HDMI_TX0_LN0_N
J2.29 HDMI_TX1_N
J2.31 HDMI_TX1_P
J2.33 HDMI_TX0_P
J2.35 HDMI_TX0_N
SOM_NVCC_SAI1_SAI5
J2.37 NC/*/WCI-2_SIN
J2.39 NC/*/WCI-2_SOUT
J2.41 NVCC_SAI1_SAI5
PWR_FLAG
HDMI_TX2_LN2_P
HDMI_TX2_LN2_N
J2.43 HDMI_TX2_P
J2.45 HDMI_TX2_N
J2.47 GND
HDMI_CLK_LN3_P
HDMI_CLK_LN3_N
J2.49 HDMI_TXC_P
J2.51 HDMI_TXC_N
J2.53 GND
GND
Sofia Giannoccaro s314083
Politecnico di Torino
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File: dart_display.kicad_sch
Title: OBU V2X board
Size: A4
Date: 2025-07-18
Rev: 1
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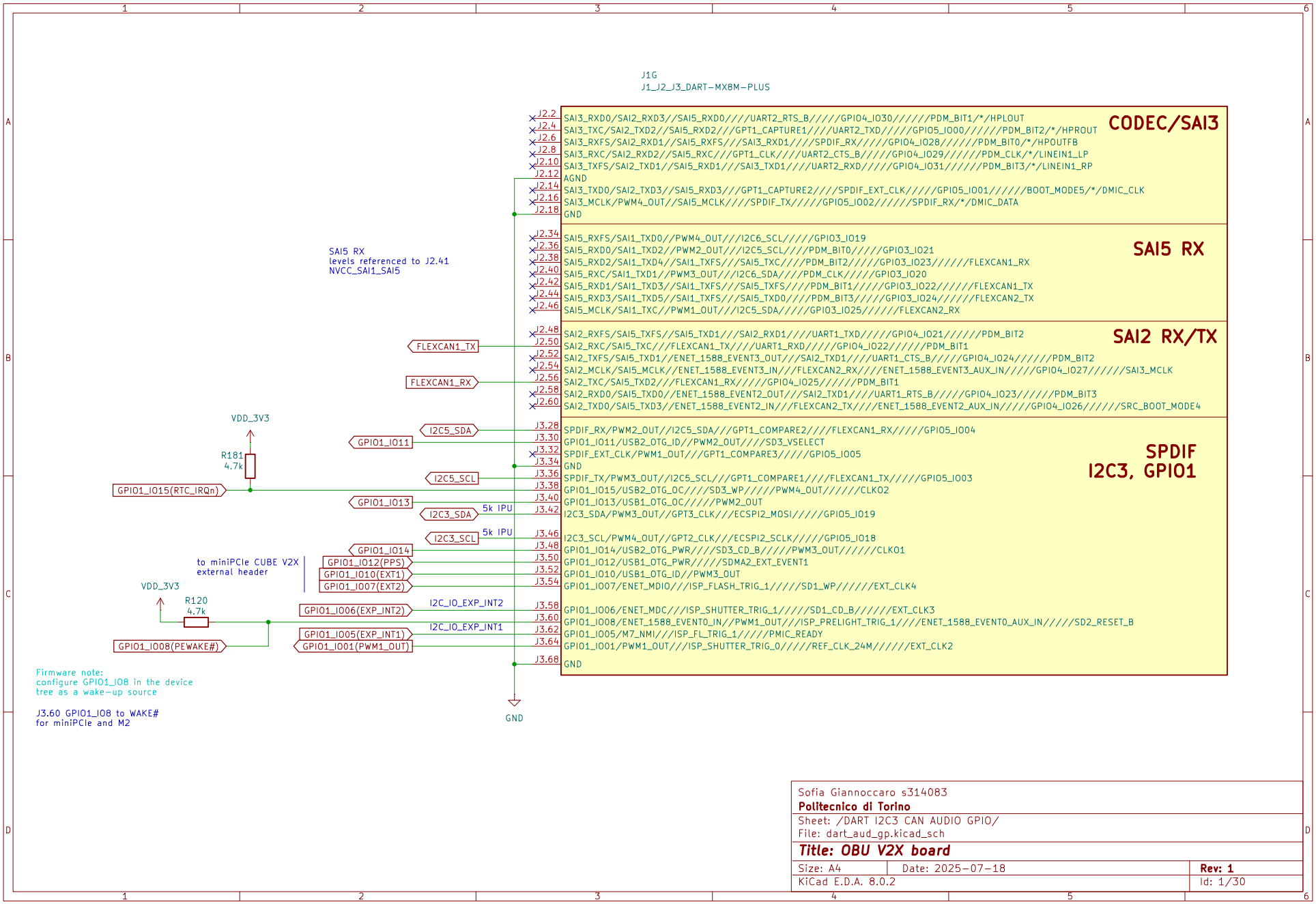
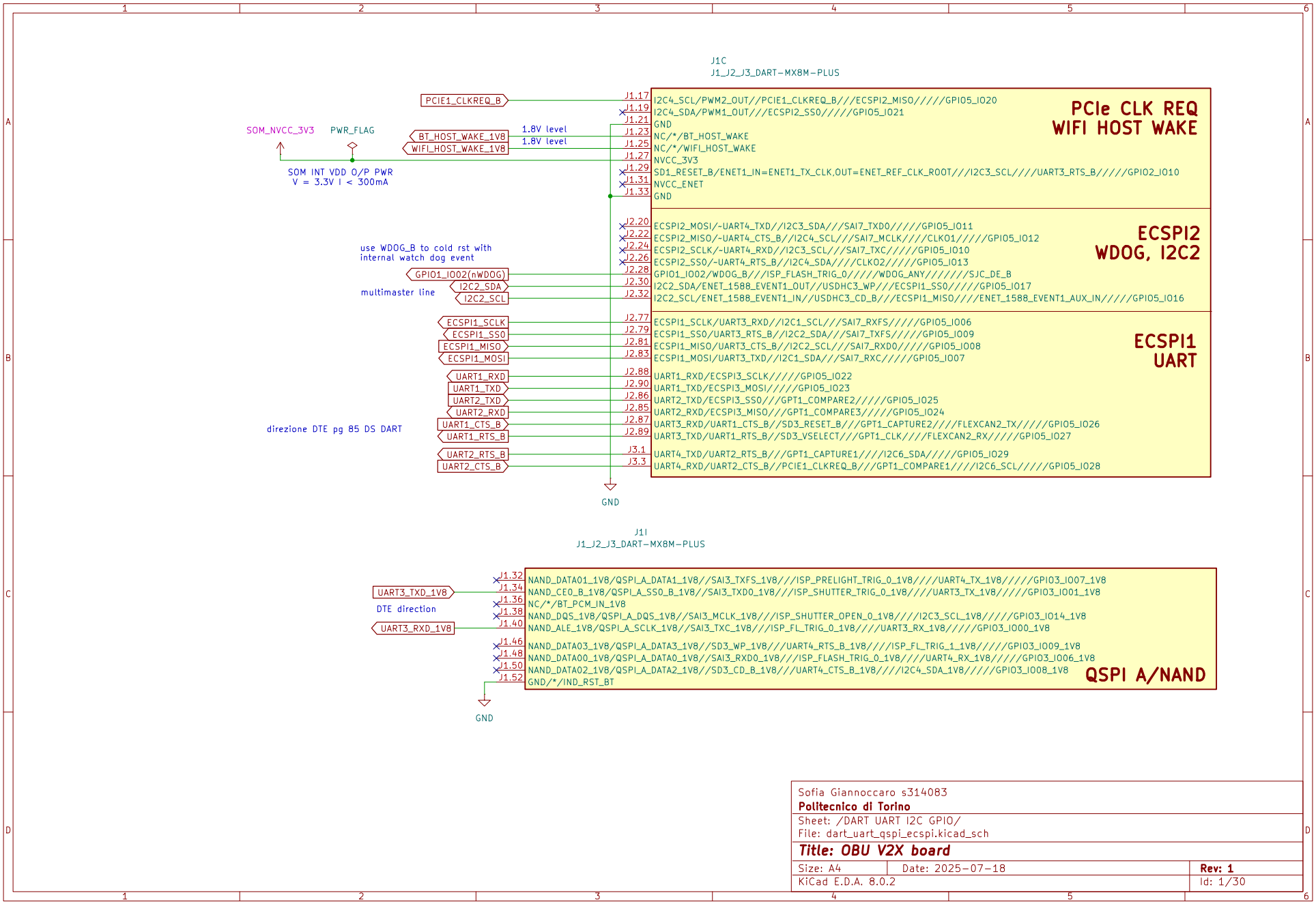

J1G
J1_J2_J3_DART-MX8M-PLUS
CODEC/SAI3
J2.2 SAI3_RXD0/SAI2_RXD3//SAI5_RXD0////UART2_RTS_B/////GPIO4_IO30//////PDM_BIT1/*/HPLOUT
J2.4 SAI3_TXC/SAI2_TXD2//SAI5_RXD2///GPT1_CAPTURE1////UART2_TXD/////GPIO5_IO00//////PDM_BIT2/*/HPROUT
J2.6 SAI3_RXFS/SAI2_RXD1//SAI5_RXFS///SAI3_RXD1////SPDIF_RX/////GPIO4_IO28//////PDM_BIT0/*/HPOUTFB
J2.8 SAI3_RXC/SAI2_RXD2//SAI5_RXC///GPT1_CLK////UART2_CTS_B/////GPIO4_IO29//////PDM_CLK/*/LINEIN1_LP
J2.10 SAI3_TXFS/SAI2_TXD1//SAI5_RXD1///SAI3_TXD1////UART2_RXD/////GPIO4_IO31//////PDM_BIT3/*/LINEIN1_RP
J2.12 AGND
J2.14 SAI3_TXD0/SAI2_TXD3//SAI5_RXD3///GPT1_CAPTURE2////SPDIF_EXT_CLK/////GPIO5_IO01//////BOOT_MODE5/*/DMIC_CLK
J2.16 SAI3_MCLK/PWM4_OUT//SAI5_MCLK////SPDIF_TX/////GPIO5_IO02//////SPDIF_RX/*/DMIC_DATA
J2.18 GND
SAI5 RX
J2.34 SAI5_RXFS/SAI1_TXD0//PWM4_OUT///I2C6_SCL/////GPIO3_IO19
J2.36 SAI5_RXD0/SAI1_TXD2//PWM2_OUT///I2C5_SCL////PDM_BIT0/////GPIO3_IO21
J2.38 SAI5_RXD2/SAI1_TXD4//SAI1_TXFS///SAI5_TXC////PDM_BIT2/////GPIO3_IO23//////FLEXCAN1_RX
J2.40 SAI5_RXC/SAI1_TXD1//PWM3_OUT///I2C6_SDA////PDM_CLK/////GPIO3_IO20
J2.42 SAI5_RXD1/SAI1_TXD3//SAI1_TXFS///SAI5_TXFS////PDM_BIT1/////GPIO3_IO22//////FLEXCAN1_TX
J2.44 SAI5_RXD3/SAI1_TXD5//SAI1_TXFS///SAI5_TXD0////PDM_BIT3/////GPIO3_IO24//////FLEXCAN2_TX
J2.46 SAI5_MCLK/SAI1_TXC//PWM1_OUT///I2C5_SDA/////GPIO3_IO25//////FLEXCAN2_RX
SAI5 RX
levels referenced to J2.41
NVCC_SAI1_SAI5
SAI2 RX/TX
FLEXCAN1_TX
J2.48 SAI2_RXFS/SAI5_TXFS//SAI5_TXD1///SAI2_RXD1////UART1_TXD/////GPIO4_IO21//////PDM_BIT2
J2.50 SAI2_RXC/SAI5_TXC///FLEXCAN1_TX////UART1_RXD/////GPIO4_IO22//////PDM_BIT1
J2.52 SAI2_TXFS/SAI5_TXD1//ENET_1588_EVENT3_OUT///SAI2_TXD1////UART1_CTS_B/////GPIO4_IO24//////PDM_BIT2
J2.54 SAI2_MCLK/SAI5_MCLK//ENET_1588_EVENT3_IN///FLEXCAN2_RX////ENET_1588_EVENT3_AUX_IN/////GPIO4_IO27//////SAI3_MCLK
FLEXCAN1_RX
J2.56 SAI2_TXC/SAI5_TXD2///FLEXCAN1_RX/////GPIO4_IO25//////PDM_BIT1
J2.58 SAI2_RXD0/SAI5_TXD0//ENET_1588_EVENT2_OUT///SAI2_TXD1////UART1_RTS_B/////GPIO4_IO23//////PDM_BIT3
J2.60 SAI2_TXD0/SAI5_TXD3//ENET_1588_EVENT2_IN///FLEXCAN2_TX////ENET_1588_EVENT2_AUX_IN/////GPIO4_IO26//////SRC_BOOT_MODE4
SPDIF
I2C3, GPIO1
VDD_3V3
R181
4.7k
I2C5_SDA
GPIO1_IO11
J3.28 SPDIF_RX/PWM2_OUT//I2C5_SDA///GPT1_COMPARE2////FLEXCAN1_RX/////GPIO5_IO04
J3.30 GPIO1_IO11/USB2_OTG_ID//PWM2_OUT////SD3_VSELECT
J3.32 SPDIF_EXT_CLK/PWM1_OUT///GPT1_COMPARE3/////GPIO5_IO05
J3.34 GND
I2C5_SCL
GPIO1_IO15(RTC_IRQn)
J3.36 SPDIF_TX/PWM3_OUT//I2C5_SCL///GPT1_COMPARE1////FLEXCAN1_TX/////GPIO5_IO03
J3.38 GPIO1_IO15/USB2_OTG_OC////SD3_WP/////PWM4_OUT/////CLKO2
GPIO1_IO13
J3.40 GPIO1_IO13/USB1_OTG_OC/////PWM2_OUT
I2C3_SDA
5k IPU
J3.42 I2C3_SDA/PWM3_OUT//GPT3_CLK///ECSPI2_MOSI/////GPIO5_IO19
I2C3_SCL
5k IPU
J3.46 I2C3_SCL/PWM4_OUT//GPT2_CLK///ECSPI2_SCLK/////GPIO5_IO18
GPIO1_IO14
J3.48 GPIO1_IO14/USB2_OTG_PWR////SD3_CD_B/////PWM3_OUT//////CLKO1
to miniPCIe CUBE V2X
external header
GPIO1_IO12(PPS)
J3.50 GPIO1_IO12/USB1_OTG_PWR/////SDMA2_EXT_EVENT1
GPIO1_IO10(EXT1)
J3.52 GPIO1_IO10/USB1_OTG_ID//PWM3_OUT
GPIO1_IO07(EXT2)
J3.54 GPIO1_IO07/ENET_MDIO///ISP_FLASH_TRIG_1/////SD1_WP//////EXT_CLK4
VDD_3V3
R120
4.7k
I2C_IO_EXP_INT2
GPIO1_IO06(EXP_INT2)
J3.58 GPIO1_IO06/ENET_MDC///ISP_SHUTTER_TRIG_1/////SD1_CD_B//////EXT_CLK3
J3.60 GPIO1_IO08/ENET_1588_EVENT0_IN//PWM1_OUT///ISP_PRELIGHT_TRIG_1////ENET_1588_EVENT0_AUX_IN/////SD2_RESET_B
I2C_IO_EXP_INT1
GPIO1_IO05(EXP_INT1)
J3.62 GPIO1_IO05/M7_NMI///ISP_FL_TRIG_1/////PMIC_READY
GPIO1_IO08(PEWAKE#)
GPIO1_IO01(PWM1_OUT)
J3.64 GPIO1_IO01/PWM1_OUT///ISP_SHUTTER_TRIG_0/////REF_CLK_24M//////EXT_CLK2
J3.68 GND
GND
Firmware note:
configure GPIO1_IO8 in the device
tree as a wake-up source
J3.60 GPIO1_IO8 to WAKE#
for miniPCIe and M2
Sofia Giannoccaro s314083
Politecnico di Torino
Sheet: /DART I2C3 CAN AUDIO GPIO/
File: dart_aud_gp.kicad_sch
Title: OBU V2X board
Size: A4
Date: 2025-07-18
Rev: 1
KiCad E.D.A. 8.0.2
Id: 1/30


J1C
J1_J2_J3_DART-MX8M-PLUS
PCIE1_CLKREQ_B
J1.17
I2C4_SCL/PWM2_OUT//PCIE1_CLKREQ_B///ECSPI2_MISO/////GPIO5_IO20
J1.19
I2C4_SDA/PWM1_OUT///ECSPI2_SS0/////GPIO5_IO21
J1.21
GND
PCIe CLK REQ
WIFI HOST WAKE
SOM_NVCC_3V3
PWR_FLAG
BT_HOST_WAKE_1V8
1.8V level
J1.23
NC/*/BT_HOST_WAKE
WIFI_HOST_WAKE_1V8
1.8V level
J1.25
NC/*/WIFI_HOST_WAKE
J1.27
NVCC_3V3
SOM INT VDD O/P PWR
V = 3.3V I < 300mA
J1.29
SD1_RESET_B/ENET1_IN=ENET1_TX_CLK,OUT=ENET_REF_CLK_ROOT///I2C3_SCL////UART3_RTS_B/////GPIO2_IO10
J1.31
NVCC_ENET
J1.33
GND
J2.20
ECSPI2_MOSI/~UART4_TXD//I2C3_SDA///SAI7_TXD0/////GPIO5_IO11
J2.22
ECSPI2_MISO/~UART4_CTS_B//I2C4_SCL///SAI7_MCLK////CLKO1/////GPIO5_IO12
J2.24
ECSPI2_SCLK/~UART4_RXD//I2C3_SCL///SAI7_TXC/////GPIO5_IO10
J2.26
ECSPI2_SS0/~UART4_RTS_B//I2C4_SDA////CLKO2/////GPIO5_IO13
ECSPI2
WDOG, I2C2
use WDOG_B to cold rst with
internal watch dog event
GPIO1_IO02(nWDOG)
J2.28
GPIO1_IO02/WDOG_B///ISP_FLASH_TRIG_0/////WDOG_ANY///////SJC_DE_B
multimaster line
I2C2_SDA
J2.30
I2C2_SDA/ENET_1588_EVENT1_OUT//USDHC3_WP///ECSPI1_SS0/////GPIO5_IO17
I2C2_SCL
J2.32
I2C2_SCL/ENET_1588_EVENT1_IN//USDHC3_CD_B///ECSPI1_MISO////ENET_1588_EVENT1_AUX_IN/////GPIO5_IO16
ECSPI1_SCLK
J2.77
ECSPI1_SCLK/UART3_RXD//I2C1_SCL///SAI7_RXFS/////GPIO5_IO06
ECSPI1_SS0
J2.79
ECSPI1_SS0/UART3_RTS_B//I2C2_SDA///SAI7_TXFS/////GPIO5_IO09
ECSPI1_MISO
J2.81
ECSPI1_MISO/UART3_CTS_B//I2C2_SCL///SAI7_RXD0/////GPIO5_IO08
ECSPI1_MOSI
J2.83
ECSPI1_MOSI/UART3_TXD//I2C1_SDA///SAI7_RXC/////GPIO5_IO07
ECSPI1
UART
UART1_RXD
J2.88
UART1_RXD/ECSPI3_SCLK/////GPIO5_IO22
UART1_TXD
J2.90
UART1_TXD/ECSPI3_MOSI/////GPIO5_IO23
UART2_TXD
J2.86
UART2_TXD/ECSPI3_SS0///GPT1_COMPARE2/////GPIO5_IO25
UART2_RXD
J2.85
UART2_RXD/ECSPI3_MISO///GPT1_COMPARE3/////GPIO5_IO24
direzione DTE pg 85 DS DART
UART1_CTS_B
J2.87
UART3_RXD/UART1_CTS_B//SD3_RESET_B///GPT1_CAPTURE2////FLEXCAN2_TX/////GPIO5_IO26
UART1_RTS_B
J2.89
UART3_TXD/UART1_RTS_B//SD3_VSELECT///GPT1_CLK////FLEXCAN2_RX/////GPIO5_IO27
UART2_RTS_B
J3.1
UART4_TXD/UART2_RTS_B///GPT1_CAPTURE1////I2C6_SDA/////GPIO5_IO29
UART2_CTS_B
J3.3
UART4_RXD/UART2_CTS_B//PCIE1_CLKREQ_B///GPT1_COMPARE1////I2C6_SCL/////GPIO5_IO28
GND
J1I
J1_J2_J3_DART-MX8M-PLUS
J1.32
NAND_DATA01_1V8/QSPI_A_DATA1_1V8//SAI3_TXFS_1V8///ISP_PRELIGHT_TRIG_0_1V8////UART4_TX_1V8/////GPIO3_IO07_1V8
UART3_TXD_1V8
J1.34
NAND_CE0_B_1V8/QSPI_A_SS0_B_1V8//SAI3_TXD0_1V8///ISP_SHUTTER_TRIG_0_1V8////UART3_TX_1V8/////GPIO3_IO01_1V8
J1.36
NC/*/BT_PCM_IN_1V8
DTE direction
J1.38
NAND_DQS_1V8/QSPI_A_DQS_1V8//SAI3_MCLK_1V8///ISP_SHUTTER_OPEN_0_1V8////I2C3_SCL_1V8/////GPIO3_IO14_1V8
UART3_RXD_1V8
J1.40
NAND_ALE_1V8/QSPI_A_SCLK_1V8//SAI3_TXC_1V8///ISP_FL_TRIG_0_1V8////UART3_RX_1V8/////GPIO3_IO00_1V8
J1.46
NAND_DATA03_1V8/QSPI_A_DATA3_1V8//SD3_WP_1V8///UART4_RTS_B_1V8////ISP_FL_TRIG_1_1V8/////GPIO3_IO09_1V8
J1.48
NAND_DATA00_1V8/QSPI_A_DATA0_1V8//SAI3_RXD0_1V8///ISP_FLASH_TRIG_0_1V8////UART4_RX_1V8/////GPIO3_IO06_1V8
J1.50
NAND_DATA02_1V8/QSPI_A_DATA2_1V8//SD3_CD_B_1V8///UART4_CTS_B_1V8////I2C4_SDA_1V8/////GPIO3_IO08_1V8
QSPI A/NAND
J1.52
GND/*/IND_RST_BT
GND
Sofia Giannoccaro s314083
Politecnico di Torino
Sheet: /DART UART I2C GPIO/
File: dart_uart_qspi_ecspi.kicad_sch
Title: OBU V2X board
Size: A4
Date: 2025-07-18
Rev: 1
KiCad E.D.A. 8.0.2
Id: 1/30

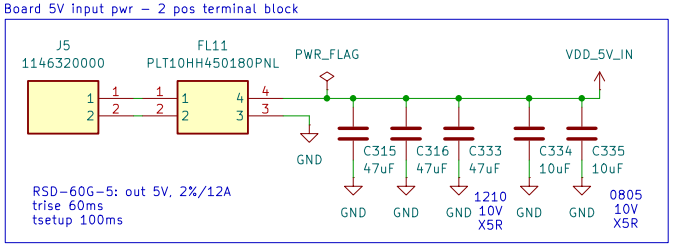
5V board input from RSD-60G-5 feeds:
5V devices on board + DART + 2x 5V/0.5A pins

TPS6286A08VBMR 3.3V /5.8A req /8A max 5%
TPS6286A08VBMR 0.95V/5.6A req /8A max 5%
TPS62827ADMQ 2.5V /0.5A req /4A max 5%
TPS62827ADMQ 1.8V /0.5A req /4A max 5%
TPS62827ADMQ 1.5V /2A req /4A max 5%
TPS62827ADMQ 1.2V /3A req /4A max 1%

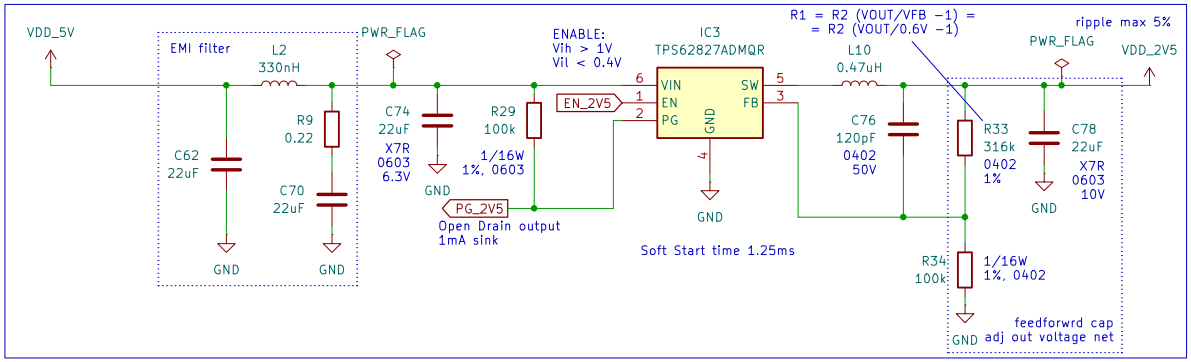
TPS7A20105PDQN (LDO) 1.05V /250mA req/ 300mA max ±1.5%
TPS7A2033PDQN (LDO) 3.3V /100mA req/ 300mA max ±30mV

On/Off Anti-vandalism bistable push button is OFF board
(connects DC jack pwr in to RSD-60G-5)

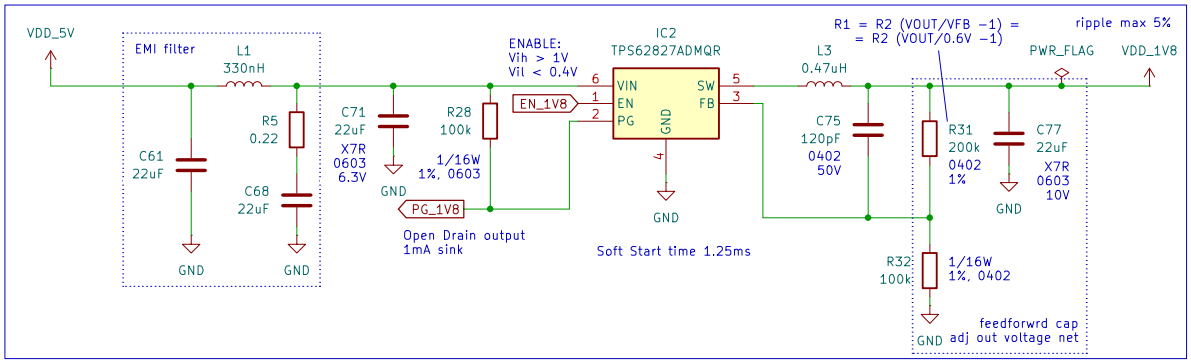
Board 5V input pwr - 2 pos terminal block



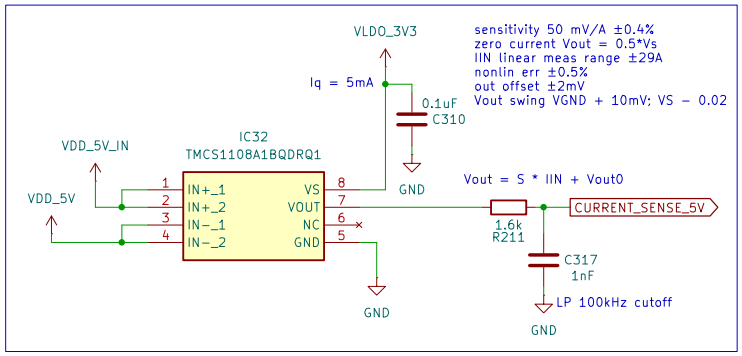
2.5V/4A - Rout_fb = 316k



1.8V/4A - Rout_fb = 200k



Hall effect current sense



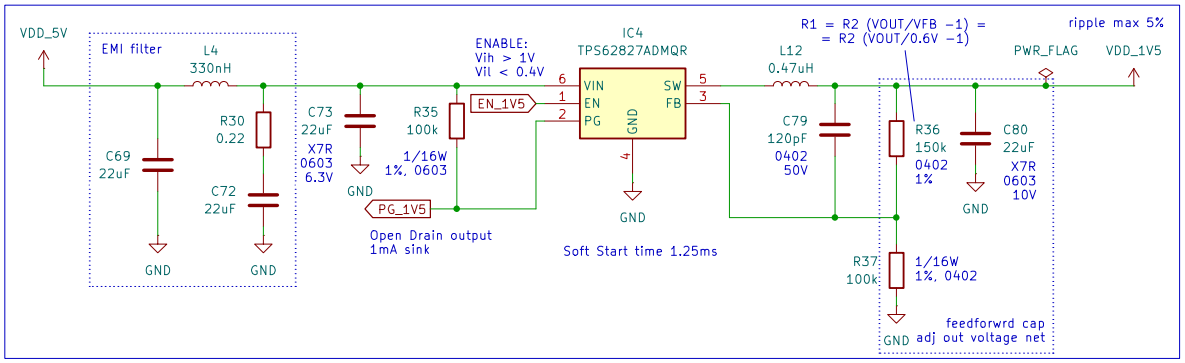
Sofia Giannoccaro s314083
Politecnico di Torino

Sheet: /Power distribution 1/
File: pwr_distrib.kicad_sch

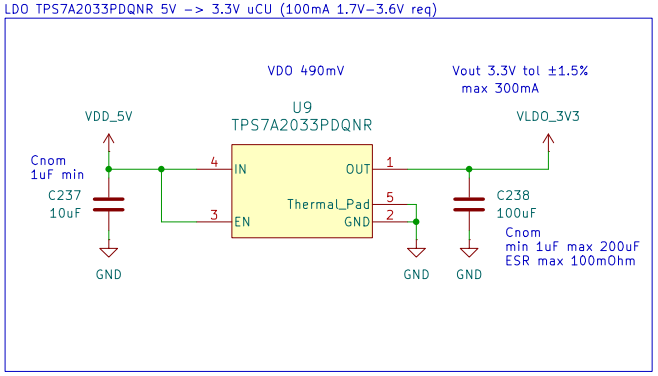
Title: OBU V2X board

Size: A4	Date: 2025-07-18	**Rev: 1**
KiCad E.D.A. 8.0.2		Id: 8/30

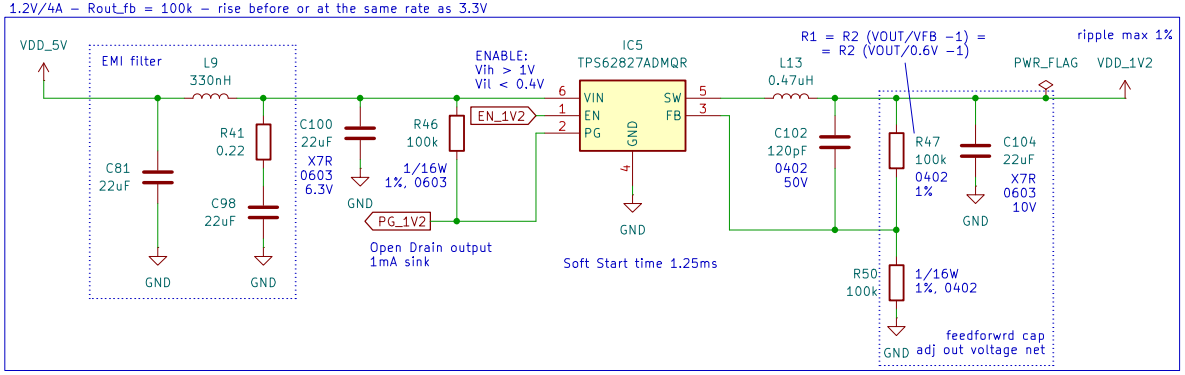
1.5V/4A – Rout_fb = 150k



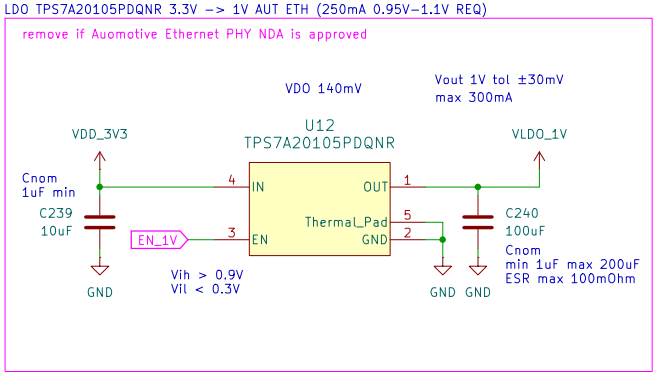
LDO TPS7A2033PDQNR 5V –> 3.3V uCU (100mA 1.7V–3.6V req)

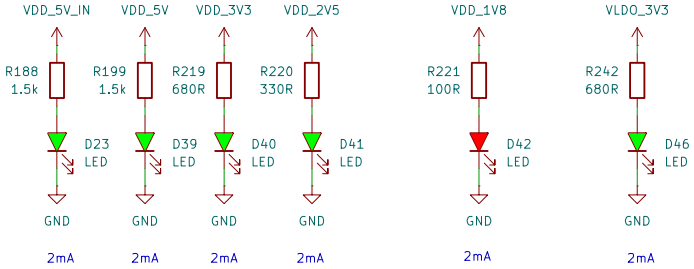


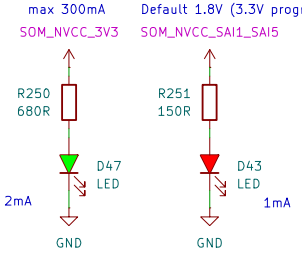
1.2V/4A – Rout_fb = 100k – rise before or at the same rate as 3.3V



LDO TPS7A20105PDQNR 3.3V –> 1V AUT ETH (250mA 0.95V–1.1V REQ)





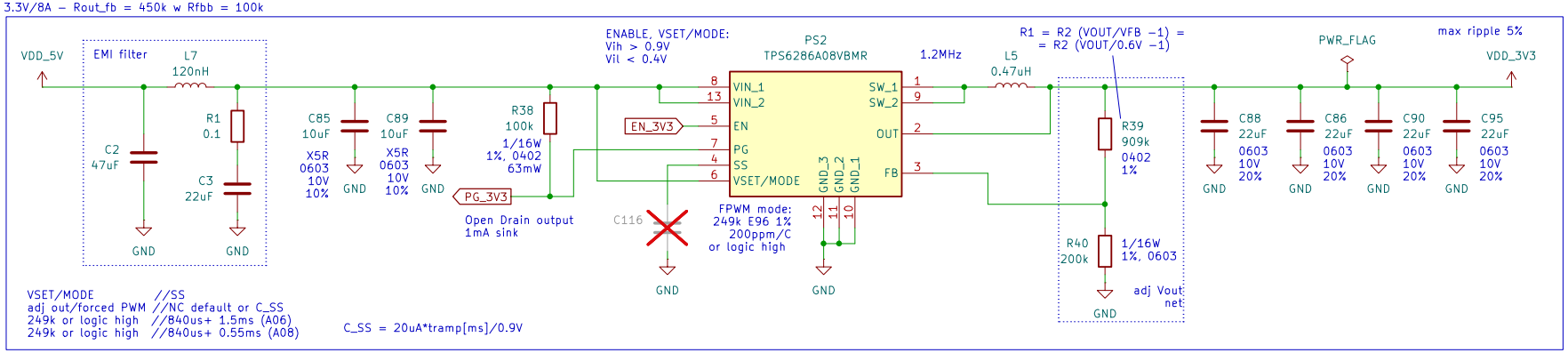


DART SNVS 1.8V max 1mA – to PMIC_RST PU
DART SD2_1V8_3V3 uSD card power – no signaling led

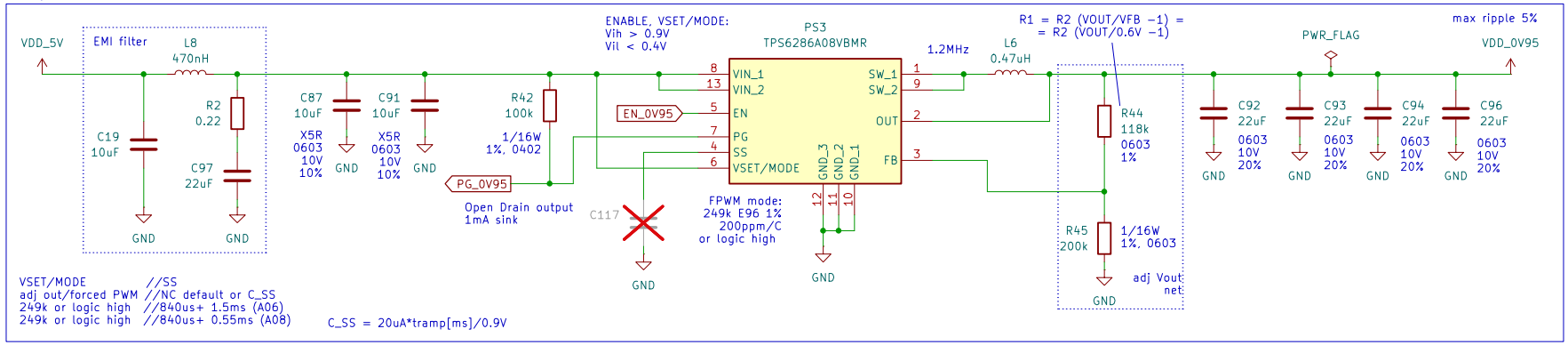
Sofia Giannoccaro s314083		
Politecnico di Torino		
Sheet: /Power Distribution 2/		
File: pwr_distrib_3.kicad_sch		
Title: OBU V2X board		
Size: A4	Date: 2025–07–18	**Rev: 1**
KiCad E.D.A. 8.0.2		Id: 1/30

3.3V/6.6A
0.95V/5.6A

3.3V/8A – Rout_fb = 450k w Rfbb = 100k



0.95V/8A – Rout_fb = 58.3k w Rfbb = 100k

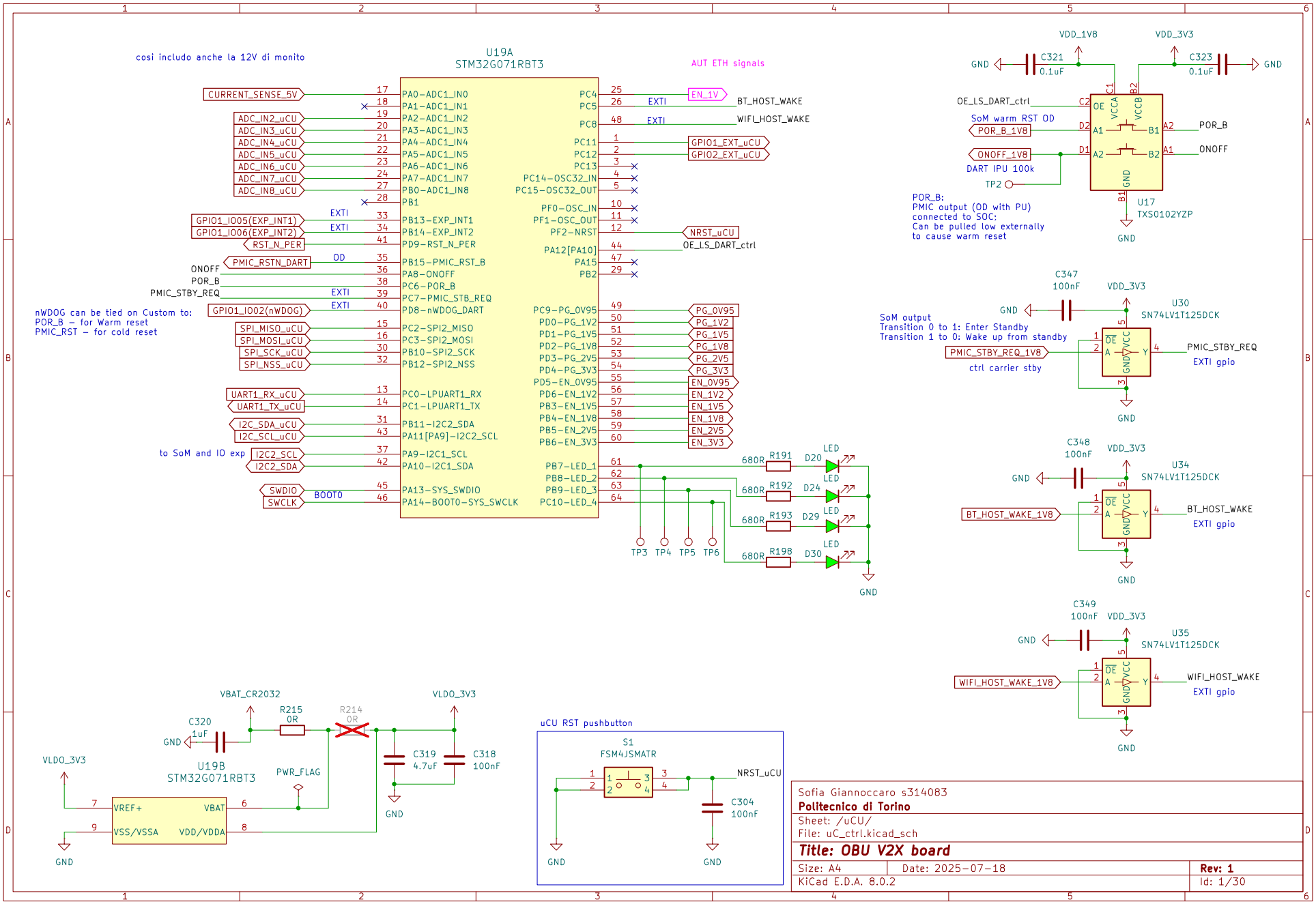


Sofia Giannoccaro s314083
Politecnico di Torino

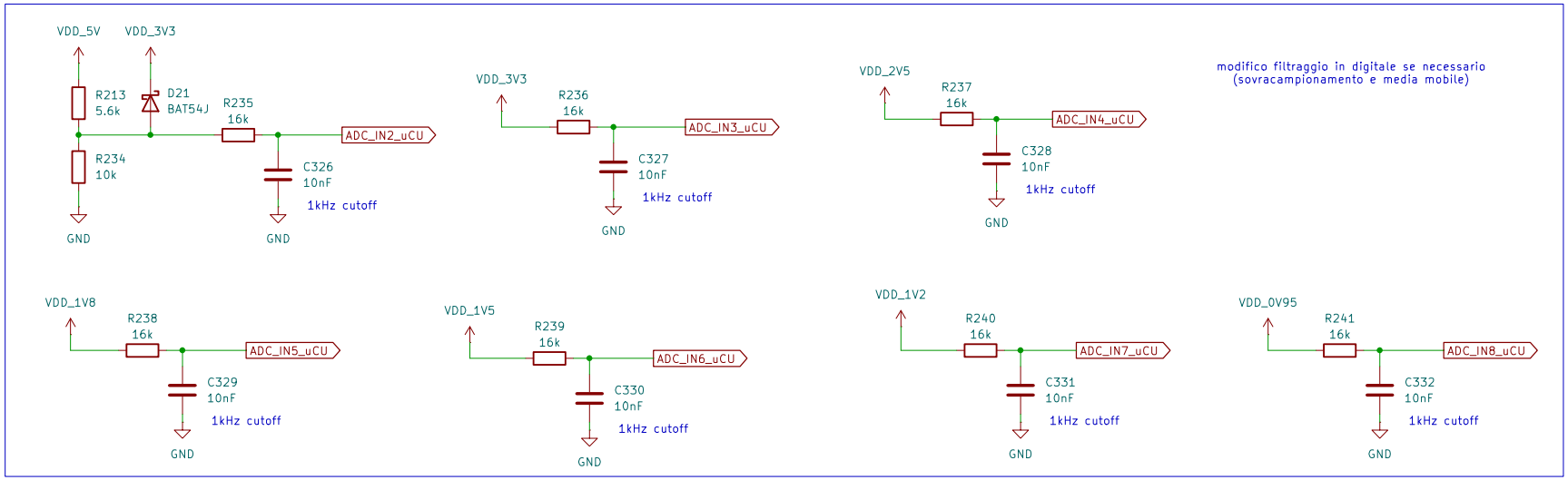
Sheet: /Power distribution 3/
File: pwr_distrib_2.kicad_sch

Title: OBU V2X board

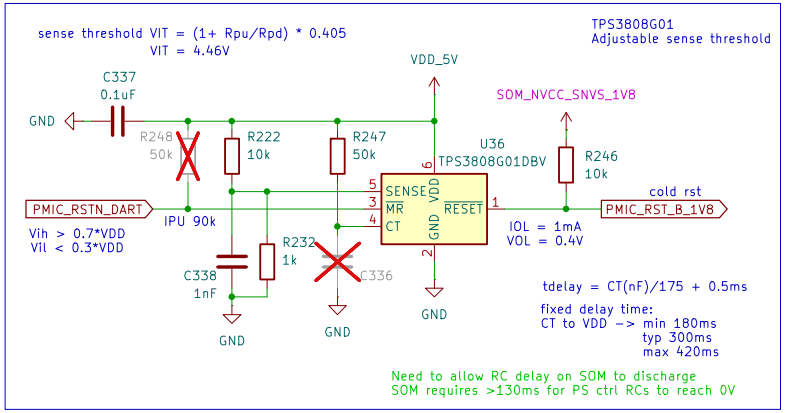
Size: A4	Date: 2025-07-18	**Rev: 1**
KiCad E.D.A. 8.0.2		Id: 10/30


cosi includo anche la 12V di monito
U19A
STM32G071RBT3
AUT ETH signals
CURRENT_SENSE_5V
ADC_IN2_uCU
ADC_IN3_uCU
ADC_IN4_uCU
ADC_IN5_uCU
ADC_IN6_uCU
ADC_IN7_uCU
ADC_IN8_uCU
GPIO1_IO05(EXP_INT1)
GPIO1_IO06(EXP_INT2)
RST_N_PER
PMIC_RSTN_DART
ONOFF
POR_B
PMIC_STBY_REQ
GPIO1_IO02(nWDOG)
SPI_MISO_uCU
SPI_MOSI_uCU
SPI_SCK_uCU
SPI_NSS_uCU
UART1_RX_uCU
UART1_TX_uCU
I2C_SDA_uCU
I2C_SCL_uCU
to SoM and IO exp
I2C2_SCL
I2C2_SDA
SWDIO
SWCLK
BOOT0
EXTI
OD
nWDOG can be tied on Custom to:
POR_B – for Warm reset
PMIC_RST – for cold reset
EN_1V
BT_HOST_WAKE
WIFI_HOST_WAKE
GPIO1_EXT_uCU
GPIO2_EXT_uCU
NRST_uCU
OE_LS_DART_ctrl
PG_0V95
PG_1V2
PG_1V5
PG_1V8
PG_2V5
PG_3V3
EN_0V95
EN_1V2
EN_1V5
EN_1V8
EN_2V5
EN_3V3
680R
R191
R192
R193
R198
D20
D24
D29
D30
LED
TP3
TP4
TP5
TP6
GND
VDD_1V8
VDD_3V3
C321
0.1uF
C323
OE_LS_DART_ctrl
SoM warm RST OD
POR_B_1V8
ONOFF_1V8
DART IPU 100k
TP2
U17
TXS0102YZP
POR_B:
PMIC output (OD with PU)
connected to SOC;
Can be pulled low externally
to cause warm reset
C347
100nF
U30
SN74LV1T125DCK
SoM output
Transition 0 to 1: Enter Standby
Transition 1 to 0: Wake up from standby
PMIC_STBY_REQ_1V8
ctrl carrier stby
C348
U34
BT_HOST_WAKE_1V8
C349
U35
WIFI_HOST_WAKE_1V8
EXTI gpio
VBAT_CR2032
VLDO_3V3
C320
1uF
R215
0R
R214
0R
C319
4.7uF
C318
100nF
U19B
STM32G071RBT3
PWR_FLAG
VREF+
VBAT
VSS/VSSA
VDD/VDDA
uCU RST pushbutton
S1
FSM4JSMATR
C304
100nF
Sofia Giannoccaro s314083
Politecnico di Torino
Sheet: /uCU/
File: uC_ctrl.kicad_sch
Title: OBU V2X board
Size: A4
Date: 2025-07-18
Rev: 1
KiCad E.D.A. 8.0.2
Id: 1/30

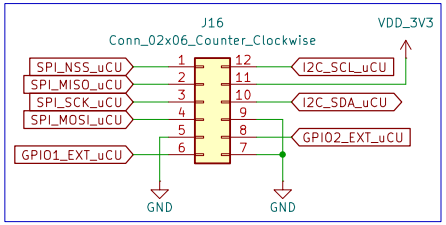
ADC/CMP voltage reduction and input protection



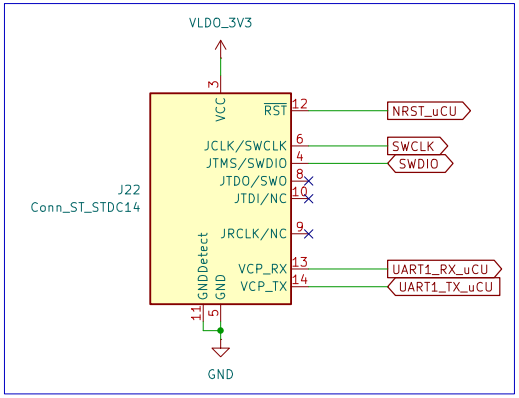
DART voltage supervisor for RST generation



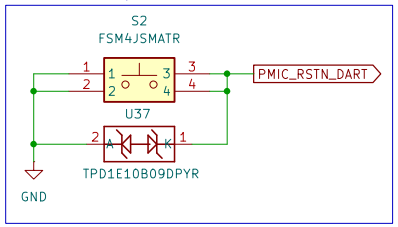
uCU master



ST LINK header from uCU



DART SoM Reset pushbutton

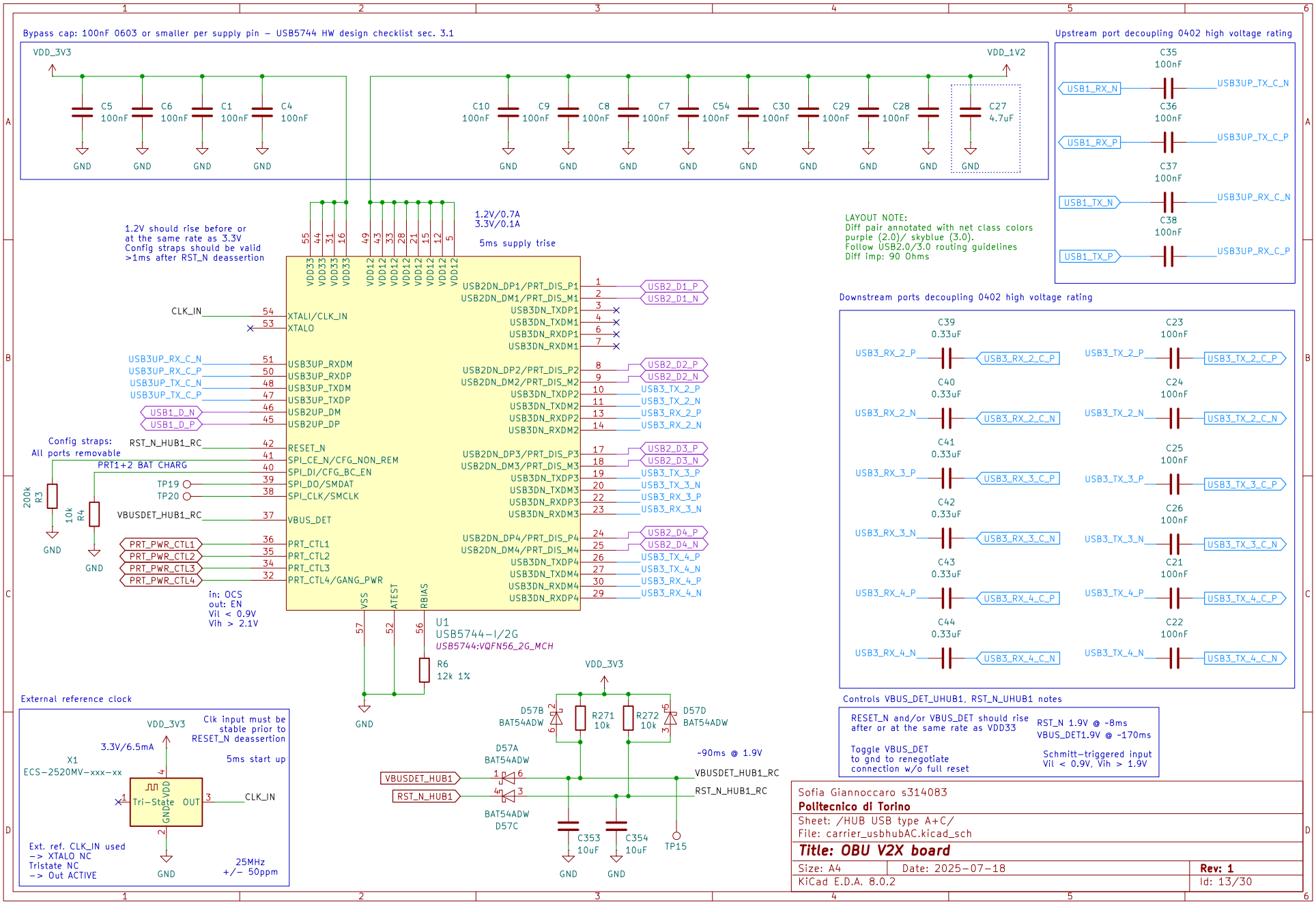


Sofia Giannoccaro s314083
Politecnico di Torino

Sheet: /uCU 2/
File: uCU_2.kicad_sch

Title: OBU V2X board

Size: A4	Date: 2025-07-18	**Rev: 1**
KiCad E.D.A. 8.0.2		Id: 1/30

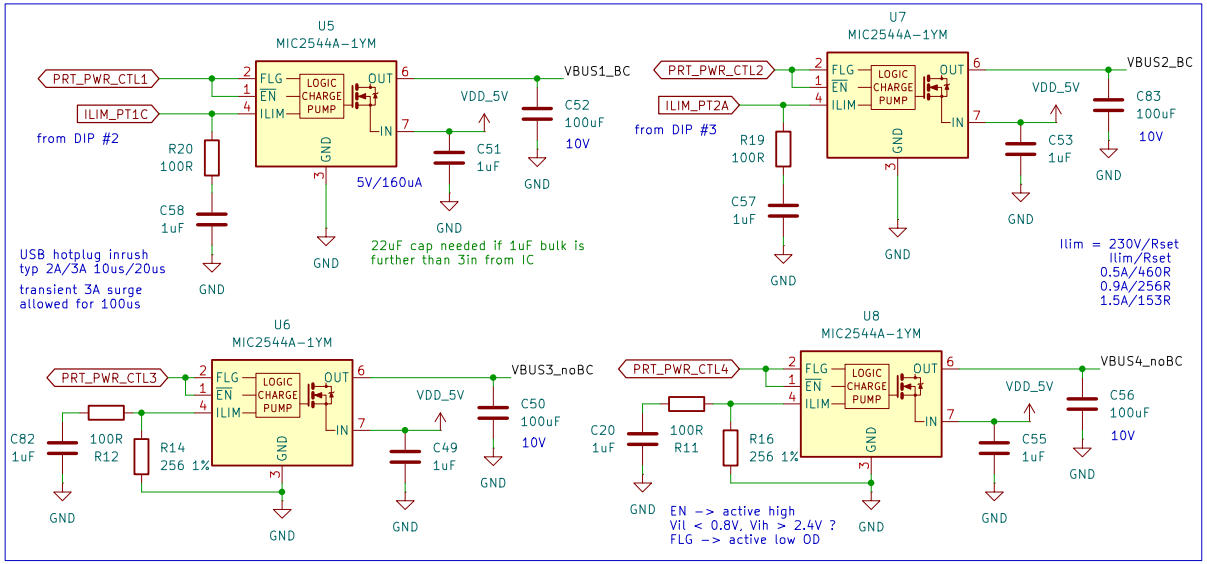


Sofia Giannoccaro s314083
Politecnico di Torino
Sheet: /HUB USB type A+C/
File: carrier_usbhubAC.kicad_sch

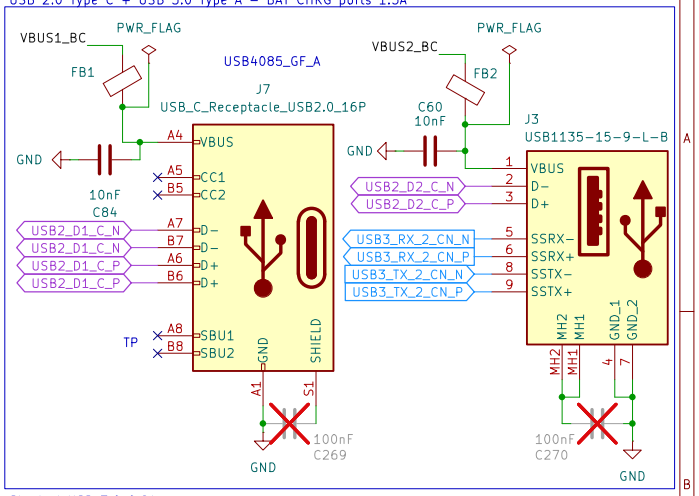
Title: OBU V2X board

Size: A4	Date: 2025-07-18	**Rev: 1**
KiCad E.D.A. 8.0.2		Id: 13/30

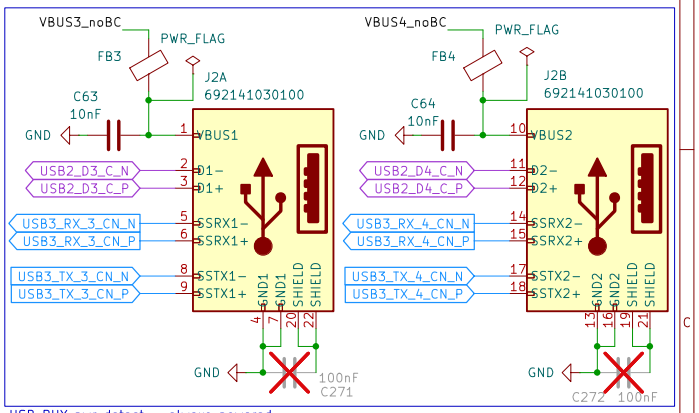
Port power controller — MIC2544A-1YM switch alimentazione adj current limit up to 1.5A, Vin 2.7-5.5V



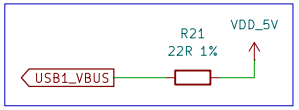
USB 2.0 Type C + USB 3.0 Type A - BAT CHRG ports 1.5A



Stacked USB 3.0 0.9A



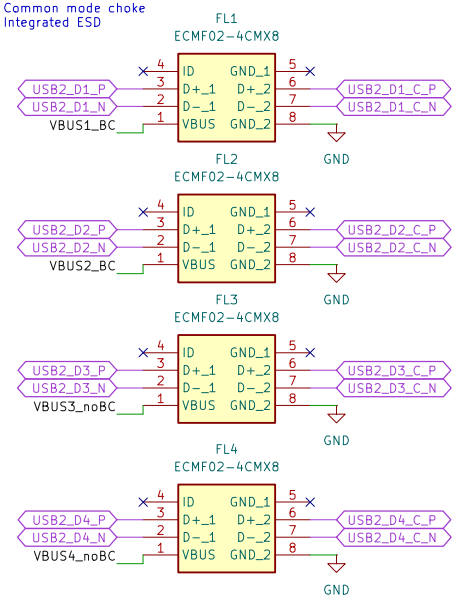
USB PHY pwr detect - always powered



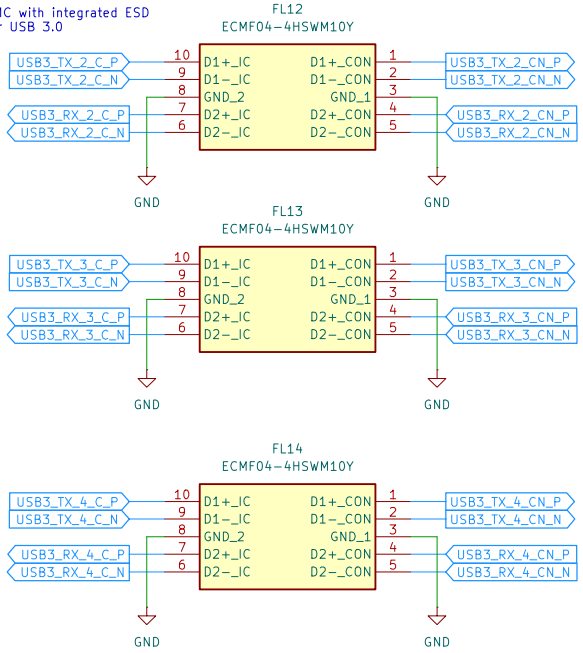
LAYOUT NOTE:
Diff pair annotated with net class colors
purple (2.0)/ skyblue (3.0).
Follow USB2.0/3.0 routing guidelines
Diff imp: 90 Ohms

CMC for USB2.0: ESD protection for USB3.0 - clamp to GND

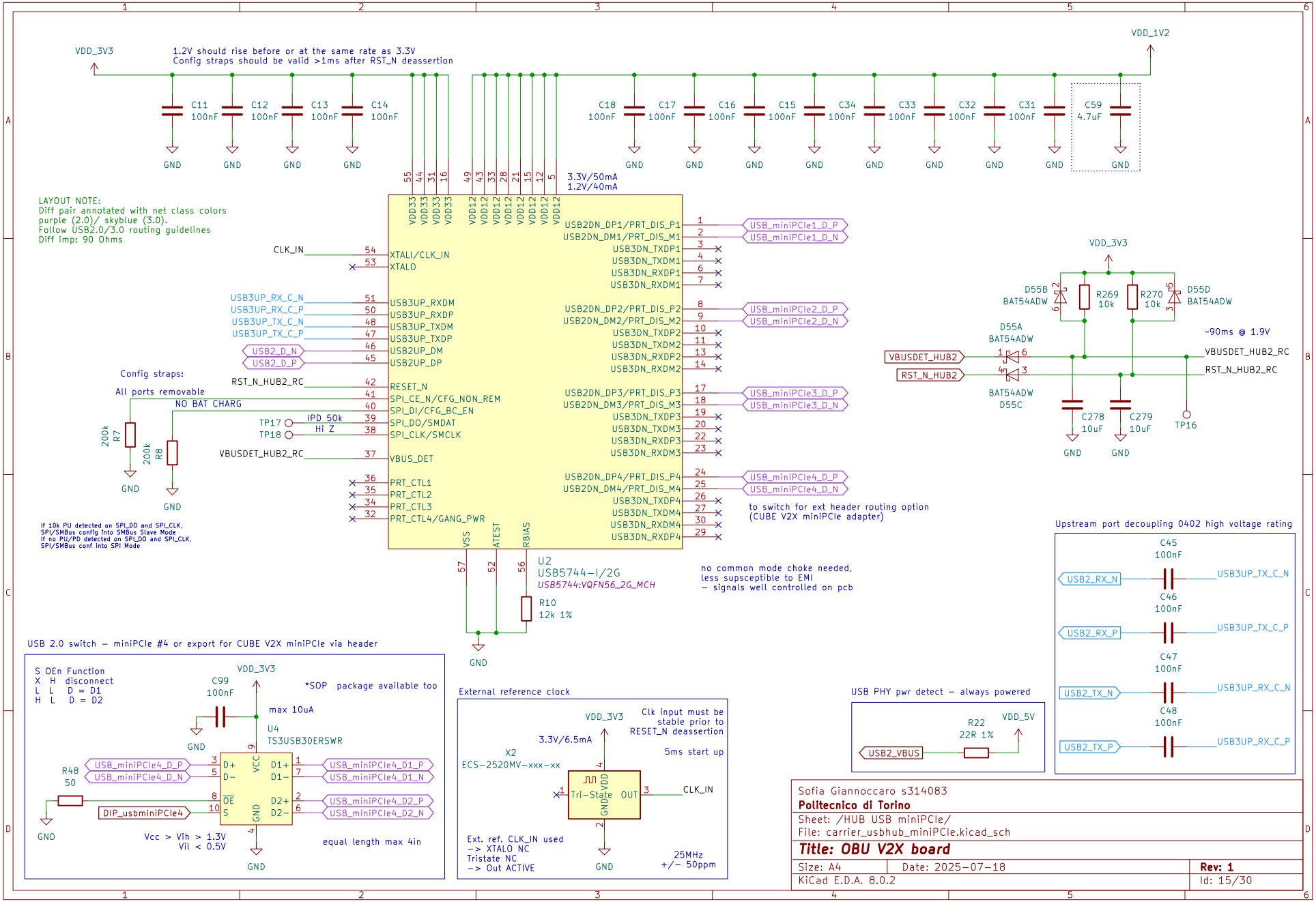
EMI reduction for usb 2.0:
Common mode choke
Integrated ESD

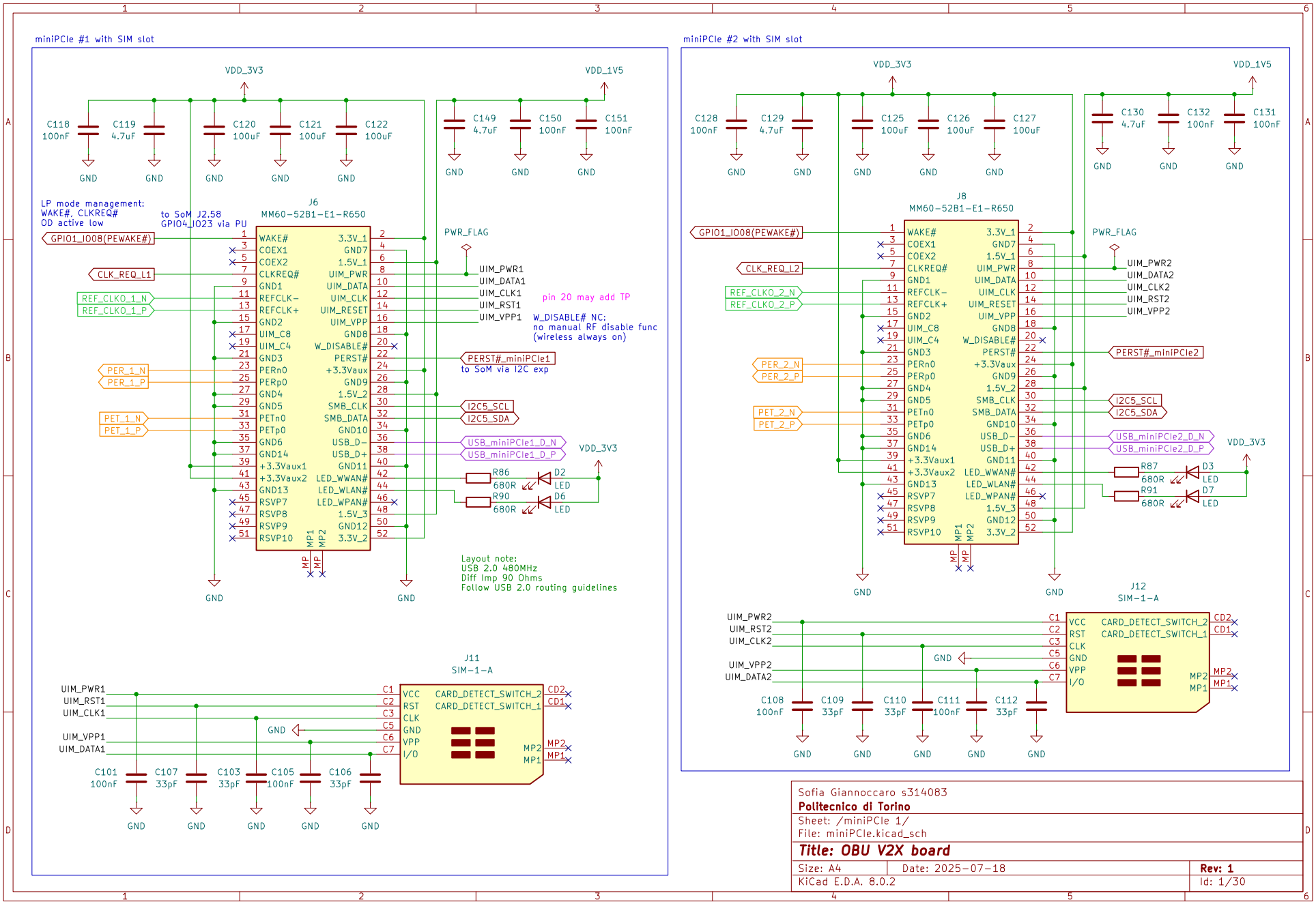


CMC with integrated ESD
for USB 3.0



Sofia Giannoccaro s314083	
Politecnico di Torino	
Sheet: /USB type A+C/	
File: carrier_usbAC.kicad_sch	
Title: OBU V2X board	
Size: A4	Date: 2025-07-18
KiCad E.D.A. 8.0.2	**Rev: 1**
	Id: 14/30


VDD_3V3
1.2V should rise before or at the same rate as 3.3V
Config straps should be valid >1ms after RST_N deassertion
VDD_1V2
C11 100nF
C12 100nF
C13 100nF
C14 100nF
C18 100nF
C17 100nF
C16 100nF
C15 100nF
C34 100nF
C33 100nF
C32 100nF
C31 100nF
C59 4.7uF
GND
3.3V/50mA
1.2V/40mA
LAYOUT NOTE:
Diff pair annotated with net class colors
purple (2.0)/ skyblue (3.0).
Follow USB2.0/3.0 routing guidelines
Diff imp: 90 Ohms
CLK_IN
USB3UP_RX_C_N
USB3UP_RX_C_P
USB3UP_TX_C_N
USB3UP_TX_C_P
USB2_D_N
USB2_D_P
RST_N_HUB2_RC
VBUSDET_HUB2_RC
XTALI/CLK_IN
XTALO
USB3UP_RXDM
USB3UP_RXDP
USB3UP_TXDM
USB3UP_TXDP
USB2UP_DM
USB2UP_DP
RESET_N
SPI_CE_N/CFG_NON_REM
SPI_DI/CFG_BC_EN
SPI_DO/SMDAT
SPI_CLK/SMCLK
VBUS_DET
PRT_CTL1
PRT_CTL2
PRT_CTL3
PRT_CTL4/GANG_PWR
USB2DN_DP1/PRT_DIS_P1
USB2DN_DM1/PRT_DIS_M1
USB3DN_TXDP1
USB3DN_TXDM1
USB3DN_RXDP1
USB3DN_RXDM1
USB2DN_DP2/PRT_DIS_P2
USB2DN_DM2/PRT_DIS_M2
USB3DN_TXDP2
USB3DN_TXDM2
USB3DN_RXDP2
USB3DN_RXDM2
USB2DN_DP3/PRT_DIS_P3
USB2DN_DM3/PRT_DIS_M3
USB3DN_TXDP3
USB3DN_TXDM3
USB3DN_RXDP3
USB3DN_RXDM3
USB2DN_DP4/PRT_DIS_P4
USB2DN_DM4/PRT_DIS_M4
USB3DN_TXDP4
USB3DN_TXDM4
USB3DN_RXDM4
USB3DN_RXDP4
USB_miniPCIe1_D_P
USB_miniPCIe1_D_N
USB_miniPCIe2_D_P
USB_miniPCIe2_D_N
USB_miniPCIe3_D_P
USB_miniPCIe3_D_N
USB_miniPCIe4_D_P
USB_miniPCIe4_D_N
VSS
ATEST
RBIAS
U2
USB5744-I/2G
USB5744:VQFN56_2G_MCH
R10
12k 1%
to switch for ext header routing option
(CUBE V2X miniPCIe adapter)
no common mode choke needed,
less supsceptible to EMI
– signals well controlled on pcb
Config straps:
All ports removable
NO BAT CHARG
IPD 50k
Hi Z
R7 200k
R8 200k
TP17
TP18
If 10k PU detected on SPI_DO and SPI_CLK,
SPI/SMBus config into SMBus Slave Mode
If no PU/PD detected on SPI_DO and SPI_CLK,
SPI/SMBus conf into SPI Mode
D55B BAT54ADW
D55A BAT54ADW
D55C BAT54ADW
D55D BAT54ADW
R269 10k
R270 10k
~90ms @ 1.9V
C278 10uF
C279 10uF
TP16
Upstream port decoupling 0402 high voltage rating
C45 100nF
C46 100nF
C47 100nF
C48 100nF
USB2_RX_N
USB2_RX_P
USB2_TX_N
USB2_TX_P
USB3UP_TX_C_N
USB3UP_TX_C_P
USB3UP_RX_C_N
USB3UP_RX_C_P
USB 2.0 switch – miniPCIe #4 or export for CUBE V2X miniPCIe via header
S OEn Function
X H disconnect
L L D = D1
H L D = D2
C99 100nF
max 10uA
*SOP package available too
U4
TS3USB30ERSWR
R48 50
DIP_usbminiPCIe4
Vcc > Vih > 1.3V
Vil < 0.5V
equal length max 4in
External reference clock
X2
ECS-2520MV-xxx-xx
3.3V/6.5mA
Clk input must be
stable prior to
RESET_N deassertion
5ms start up
Tri-State
OUT
CLK_IN
Ext. ref. CLK_IN used
-> XTALO NC
Tristate NC
-> Out ACTIVE
25MHz
+/- 50ppm
USB PHY pwr detect – always powered
R22 22R 1%
VDD_5V
USB2_VBUS
VBUSDET_HUB2
RST_N_HUB2
Sofia Giannoccaro s314083
Politecnico di Torino
Sheet: /HUB USB miniPCIe/
File: carrier_usbhub_miniPCIe.kicad_sch
Title: OBU V2X board
Size: A4
Date: 2025-07-18
Rev: 1
KiCad E.D.A. 8.0.2
Id: 15/30



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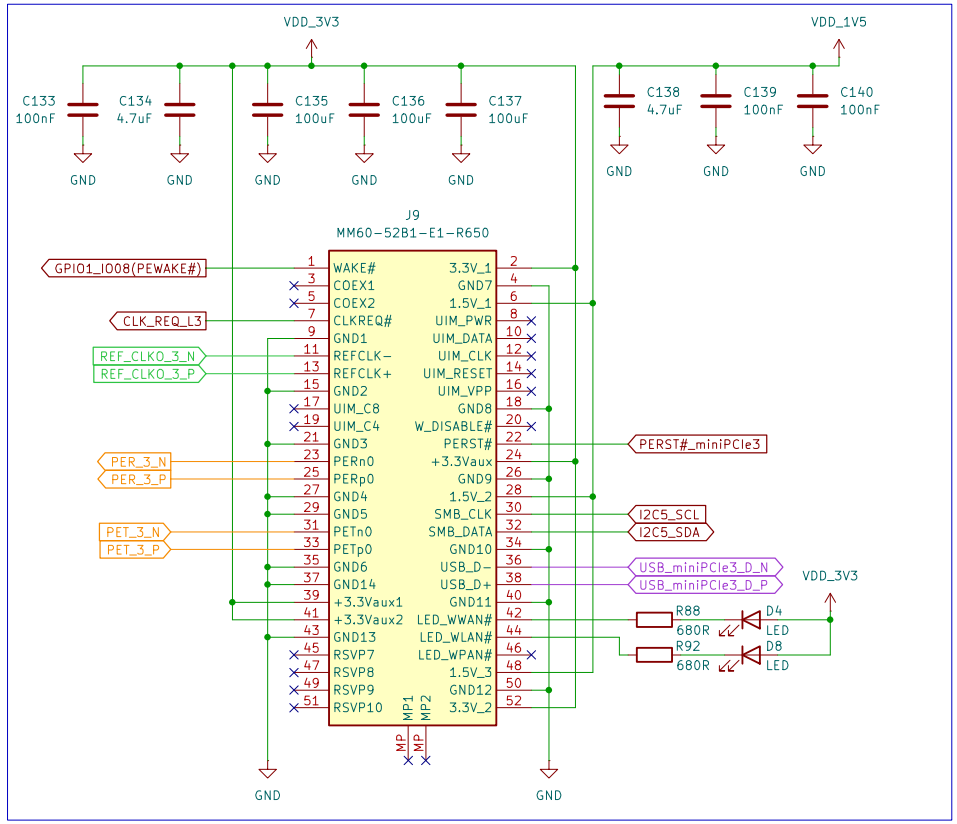
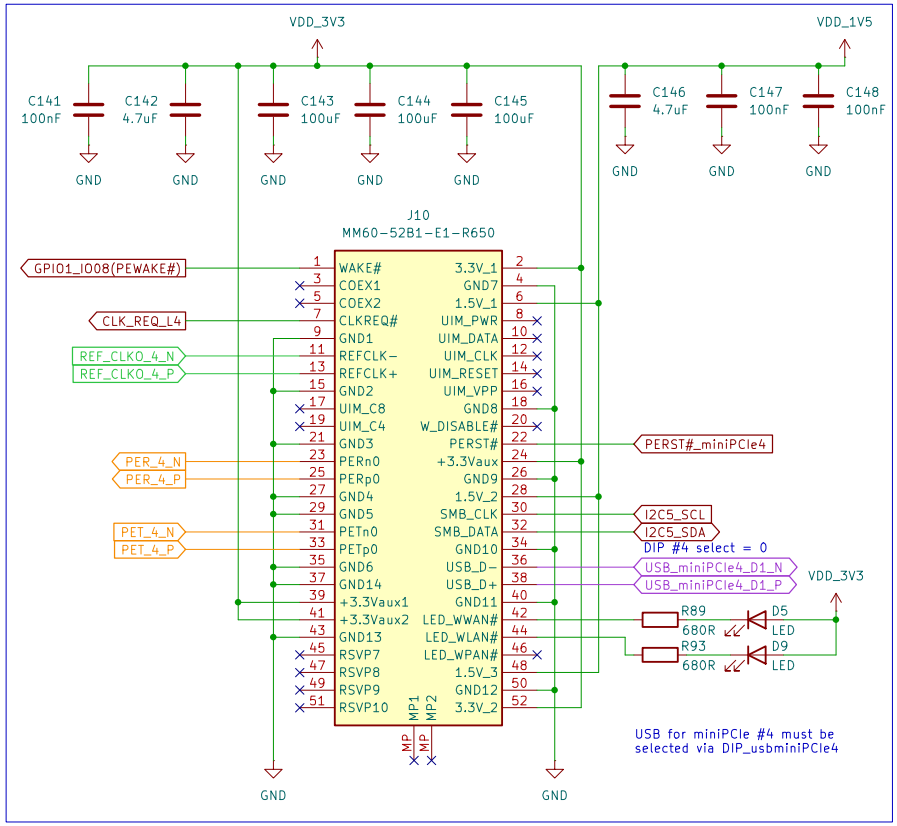
Politecnico di Torino

Sheet: /miniPCIe 1/
File: miniPCIe.kicad_sch

Title: OBU V2X board

Size: A4	Date: 2025-07-18	**Rev: 1**
KiCad E.D.A. 8.0.2		Id: 1/30





Reference Documentation:
PCI Express Mini Card
Electromechanical Specification Revision 1.2, 2007

PCI Express Base Specification Revision 6.0, 2021

PCI Express M.2 Specification Revision 1.1, 2016

PCIe mini card electromechanical specs pg 41:
By default, the PETp0 and PETn0 pins (the transmitter differential pair of the connector) shall be connected to the PCI Express transmitter differential pair on the system board and to the PCI Express receiver differential pair on the PCI Express Mini Card add–in card. Similarly by default, the PERp0 and PERn0 pins (the receiver differential pair of the connector) shall be connected to the PCI Express receiver differential pair on the system board and to the PCI Express transmitter differential pair on the PCI Express Mini Card add–in card.

PCIe M.2 specs pg 106:
By default, the PETp0 and PETn0 pins (the transmitter differential pair of the connector) shall be connected to the PCI Express transmitter differential pair on the system board and to the PCI Express receiver differential pair on the PCI Express M.2 Card add–in card. Similarly by default, the PERp0 and PERn0 pins (the receiver differential pair of the connector) shall be connected to the PCI Express receiver differential pair on the system board and to the PCI Express transmitter differential pair on the PCI Express M.2 Card add–in card

UIM_PWR (Power source for the UIM): Output
UIM_RESET (UIM reset signal): Output
UIM_CLK (UIM clock si gnal): Output
UIM_VPP (Variable supply voltage (e.g.,programming voltage)
for class A devices): Output
UIM_DATA (UIM data si gnal): Input/Output

W_DISABLE# (used by the system to disable radio operation on add–in cards that implement radio frequency applications): Input

CLKREQ# (driven low by the PCI Express Mini Card function to request that the PCI Express reference clock be available (active clock state) in order to allow the PCI Express interface to send/receive data)

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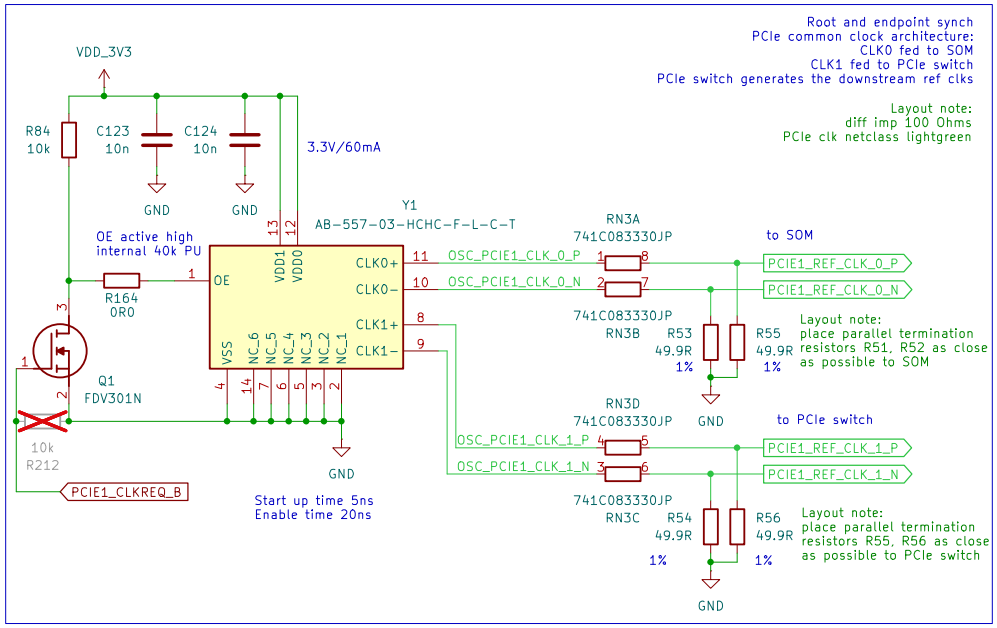
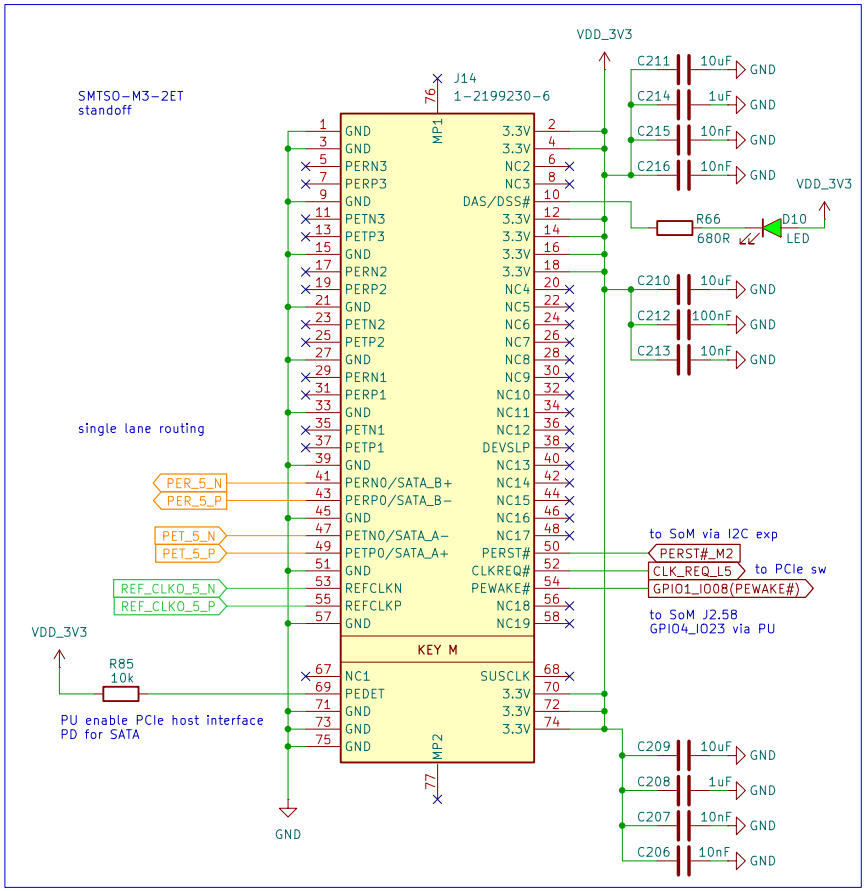
Sheet: /miniPCIe 2/
File: miniPCIe2.kicad_sch
Title: OBU V2X board
Size: A4 | Date: 2025-07-18 | **Rev: 1**
KiCad E.D.A. 8.0.2 | Id: 1/30

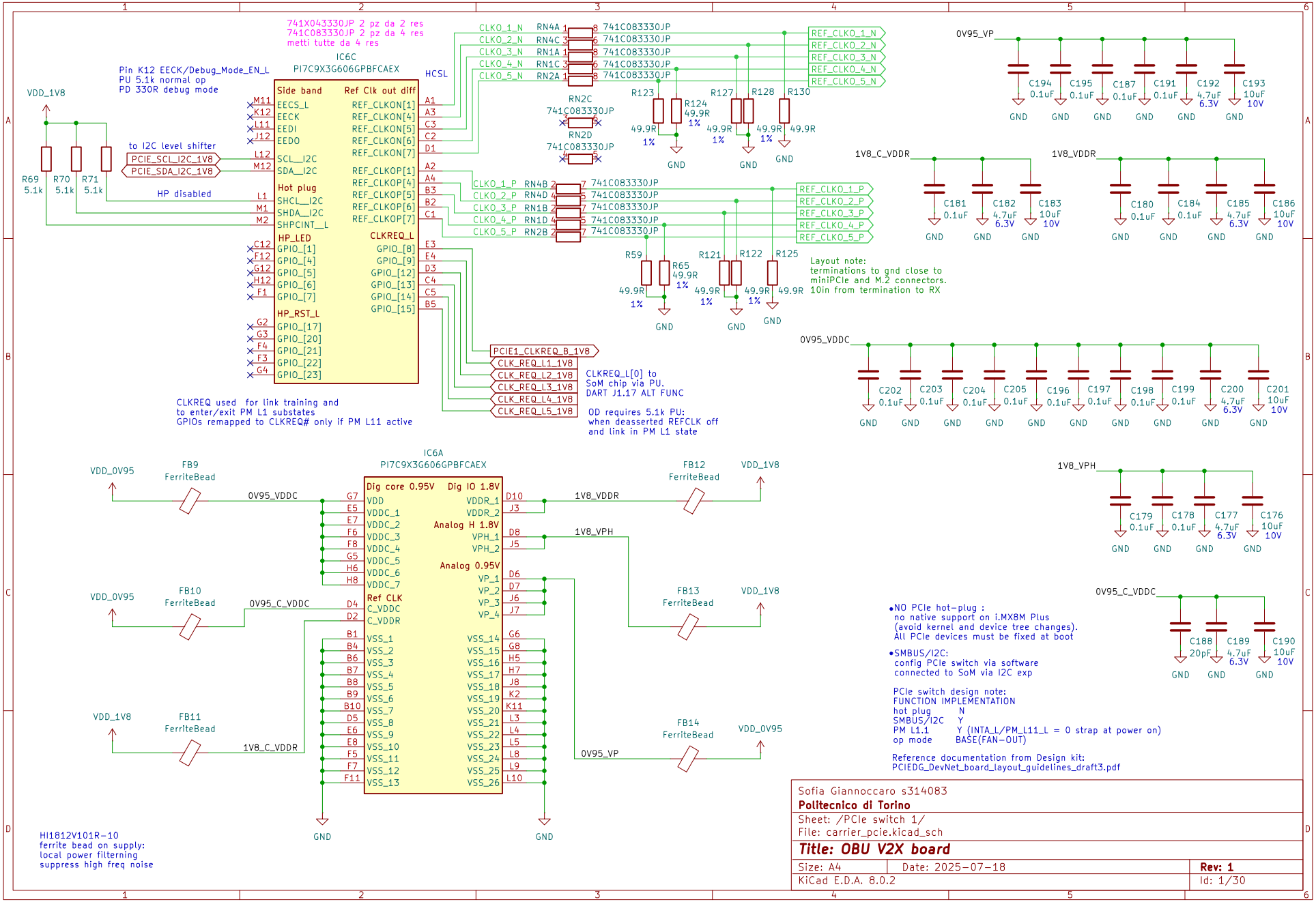
OSC PCIe compliant 100MHz w HCSL signaling

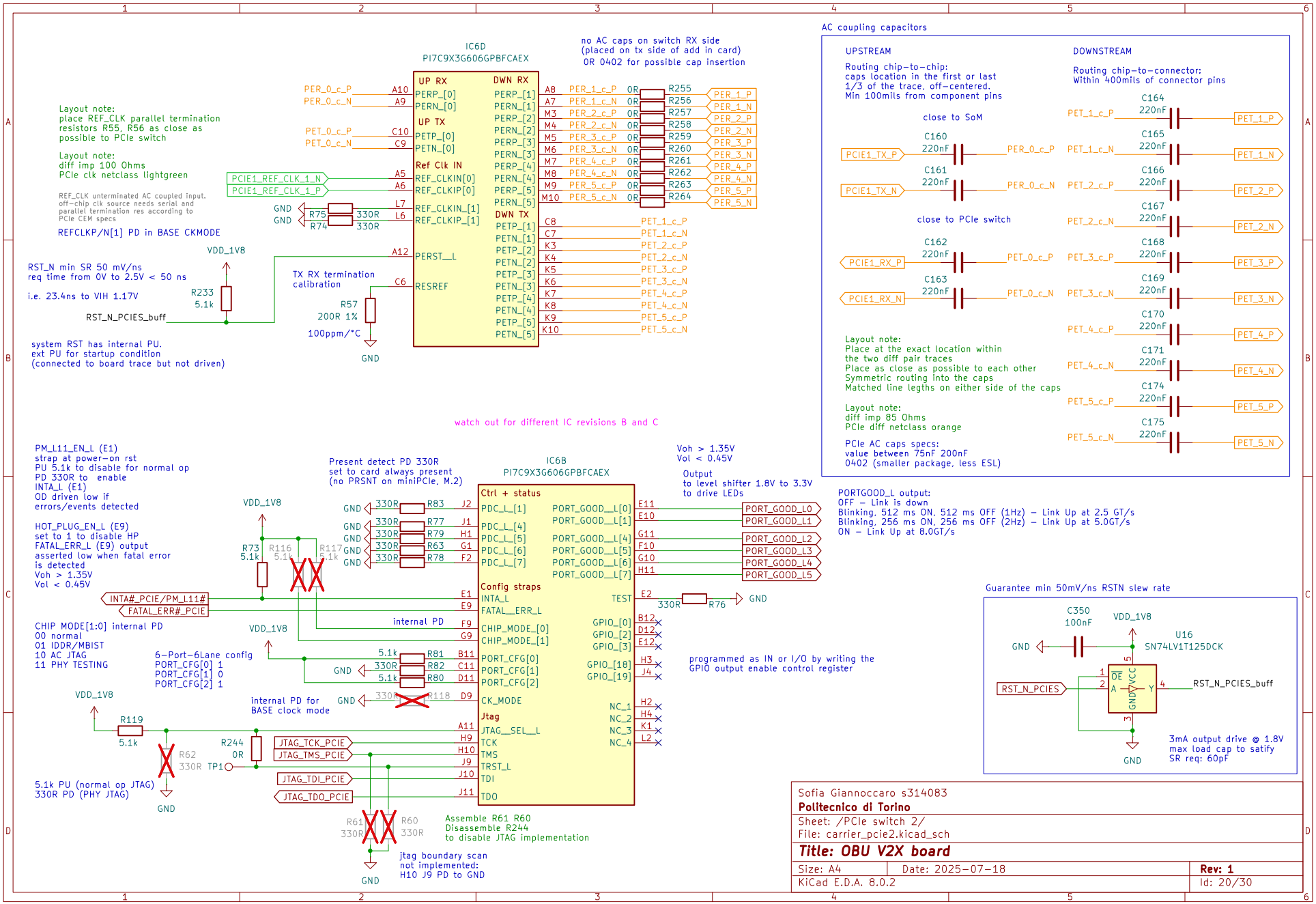


M.2 (M key) SSD NVMe protocol over PCIe interface – 10W slot 3A



Sofia Giannoccaro s314083		
Politecnico di Torino		
Sheet: /PCIe OSC M.2/		
File: carrier_pcie3.kicad_sch		
Title: OBU V2X board		
Size: A4	Date: 2025-07-18	**Rev: 1**
KiCad E.D.A. 8.0.2		Id: 1/30


741X043330JP 2 pz da 2 res
741C083330JP 2 pz da 4 res
metti tutte da 4 res
IC6C
PI7C9X3G606GPBFCAEX
HCSL
Pin K12 EECK/Debug_Mode_EN_L
PU 5.1k normal op
PD 330R debug mode
VDD_1V8
R69 5.1k
R70 5.1k
R71 5.1k
to I2C level shifter
PCIE_SCL_I2C_1V8
PCIE_SDA_I2C_1V8
HP disabled
Side band
EECS_L
EECK
EEDI
EEDO
SCL__I2C
SDA__I2C
Hot plug
SHCL__I2C
SHDA__I2C
SHPCINT__L
HP_LED
GPIO_[1]
GPIO_[4]
GPIO_[5]
GPIO_[6]
GPIO_[7]
HP_RST_L
GPIO_[17]
GPIO_[20]
GPIO_[21]
GPIO_[22]
GPIO_[23]
Ref Clk out diff
REF_CLKON[1]
REF_CLKON[4]
REF_CLKON[5]
REF_CLKON[6]
REF_CLKON[7]
REF_CLKOP[1]
REF_CLKOP[4]
REF_CLKOP[5]
REF_CLKOP[6]
REF_CLKOP[7]
CLKREQ_L
GPIO_[8]
GPIO_[9]
GPIO_[12]
GPIO_[13]
GPIO_[14]
GPIO_[15]
CLKREQ used for link training and
to enter/exit PM L1 substates
GPIOs remapped to CLKREQ# only if PM L11 active
CLKO_1_N
CLKO_2_N
CLKO_3_N
CLKO_4_N
CLKO_5_N
RN4A
RN4C
RN1A
RN1C
RN2A
RN2C
RN2D
741C083330JP
REF_CLKO_1_N
REF_CLKO_2_N
REF_CLKO_3_N
REF_CLKO_4_N
REF_CLKO_5_N
R123
R124
R127
R128
R130
49.9R
1%
GND
CLKO_1_P
CLKO_2_P
CLKO_3_P
CLKO_4_P
CLKO_5_P
RN4B
RN4D
RN1B
RN1D
RN2B
REF_CLKO_1_P
REF_CLKO_2_P
REF_CLKO_3_P
REF_CLKO_4_P
REF_CLKO_5_P
R59
R65
R121
R122
R125
Layout note:
terminations to gnd close to
miniPCIe and M.2 connectors.
10in from termination to RX
PCIE1_CLKREQ_B_1V8
CLK_REQ_L1_1V8
CLK_REQ_L2_1V8
CLK_REQ_L3_1V8
CLK_REQ_L4_1V8
CLK_REQ_L5_1V8
CLKREQ_L[0] to
SoM chip via PU.
DART J1.17 ALT FUNC
OD requires 5.1k PU:
when deasserted REFCLK off
and link in PM L1 state
0V95_VP
C194 0.1uF
C195 0.1uF
C187 0.1uF
C191 0.1uF
C192 4.7uF 6.3V
C193 10uF 10V
1V8_C_VDDR
C181 0.1uF
C182 4.7uF 6.3V
C183 10uF 10V
1V8_VDDR
C180 0.1uF
C184 0.1uF
C185 4.7uF 6.3V
C186 10uF 10V
0V95_VDDC
C202 0.1uF
C203 0.1uF
C204 0.1uF
C205 0.1uF
C196 0.1uF
C197 0.1uF
C198 0.1uF
C199 0.1uF
C200 4.7uF 6.3V
C201 10uF 10V
IC6A
PI7C9X3G606GPBFCAEX
VDD_0V95
FB9
FerriteBead
0V95_VDDC
Dig core 0.95V
VDD
VDDC_1
VDDC_2
VDDC_3
VDDC_4
VDDC_5
VDDC_6
VDDC_7
Ref CLK
C_VDDC
C_VDDR
Dig IO 1.8V
VDDR_1
VDDR_2
Analog H 1.8V
VPH_1
VPH_2
Analog 0.95V
VP_1
VP_2
VP_3
VP_4
VSS_1
VSS_2
VSS_3
VSS_4
VSS_5
VSS_6
VSS_7
VSS_8
VSS_9
VSS_10
VSS_11
VSS_12
VSS_13
VSS_14
VSS_15
VSS_16
VSS_17
VSS_18
VSS_19
VSS_20
VSS_21
VSS_22
VSS_23
VSS_24
VSS_25
VSS_26
FB12
VDD_1V8
1V8_VDDR
1V8_VPH
FB10
0V95_C_VDDC
FB13
FB11
1V8_C_VDDR
FB14
VDD_0V95
0V95_VP
GND
1V8_VPH
C179 0.1uF
C178 0.1uF
C177 4.7uF 6.3V
C176 10uF 10V
0V95_C_VDDC
C188 20pF
C189 4.7uF 6.3V
C190 10uF 10V
•NO PCIe hot-plug :
no native support on i.MX8M Plus
(avoid kernel and device tree changes).
All PCIe devices must be fixed at boot
•SMBUS/I2C:
config PCIe switch via software
connected to SoM via I2C exp
PCIe switch design note:
FUNCTION IMPLEMENTATION
hot plug N
SMBUS/I2C Y
PM L1.1 Y (INTA_L/PM_L11_L = 0 strap at power on)
op mode BASE(FAN-OUT)
Reference documentation from Design kit:
PCIEDG_DevNet_board_layout_guidelines_draft3.pdf
HI1812V101R-10
ferrite bead on supply:
local power filterning
suppress high freq noise
Sofia Giannoccaro s314083
Politecnico di Torino
Sheet: /PCIe switch 1/
File: carrier_pcie.kicad_sch
Title: OBU V2X board
Size: A4
Date: 2025-07-18
Rev: 1
KiCad E.D.A. 8.0.2
Id: 1/30



Sofia Giannoccaro s314083
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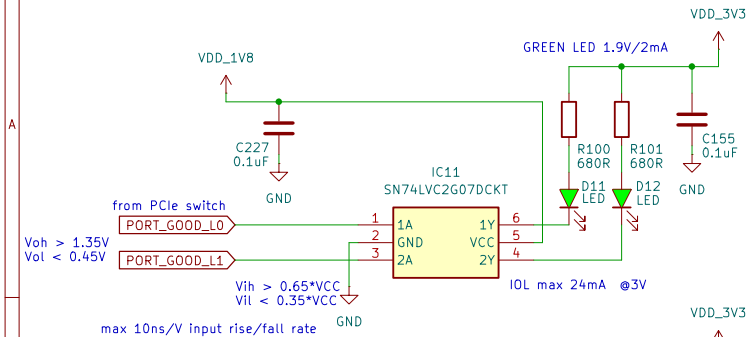
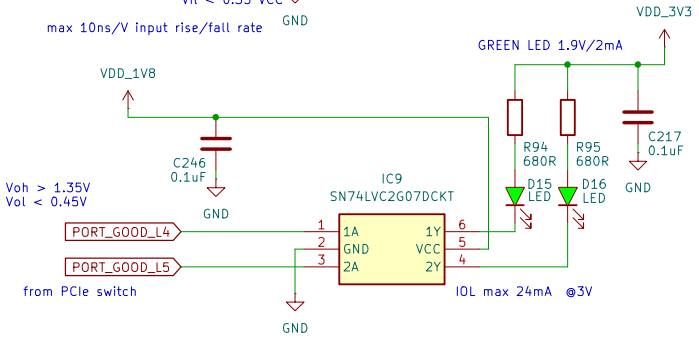
Sheet: /PCIe switch 2/
File: carrier_pcie2.kicad_sch

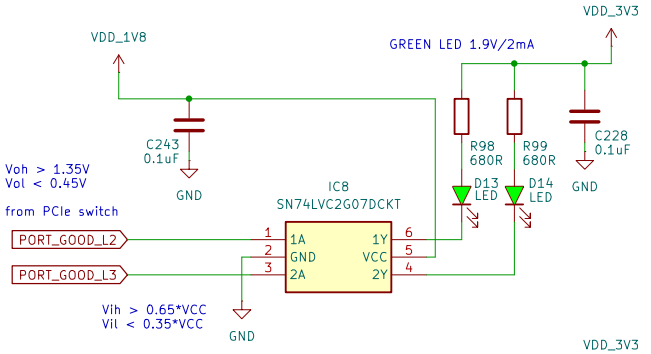
Title: OBU V2X board

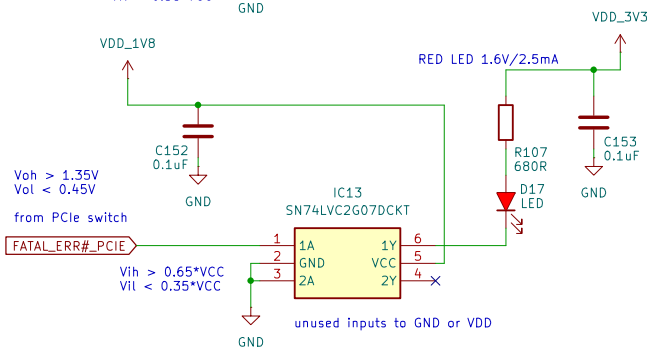
Size: A4	Date: 2025-07-18	**Rev: 1**
KiCad E.D.A. 8.0.2		Id: 20/30

Level shifter for PCIe switch signals 1.8V to carier 3.3V – SN74LVC Dual buffer and driver OD outputs

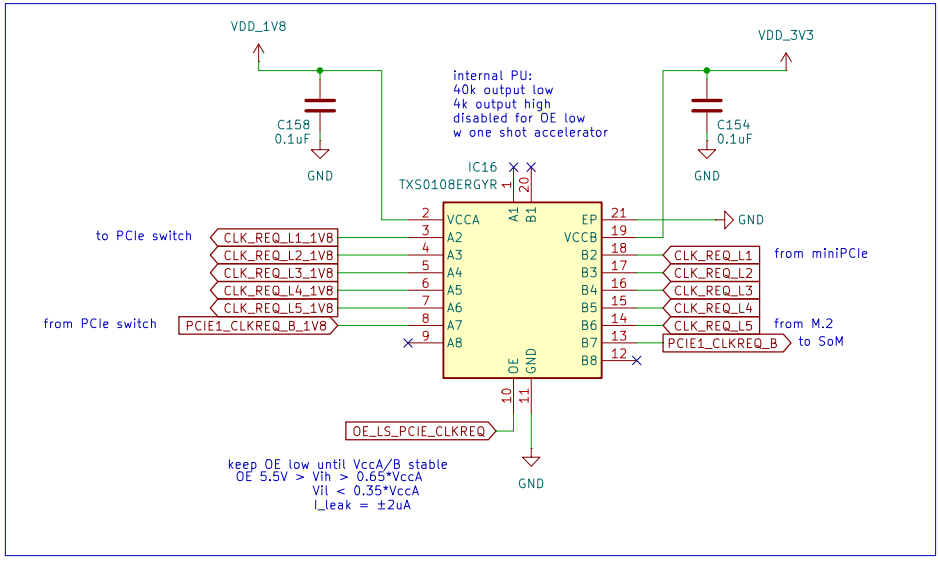








Level shifter for PCIe switch signals 1.8V to carier 3.3V – TXS0108E bidirectional level shifter for OD applications

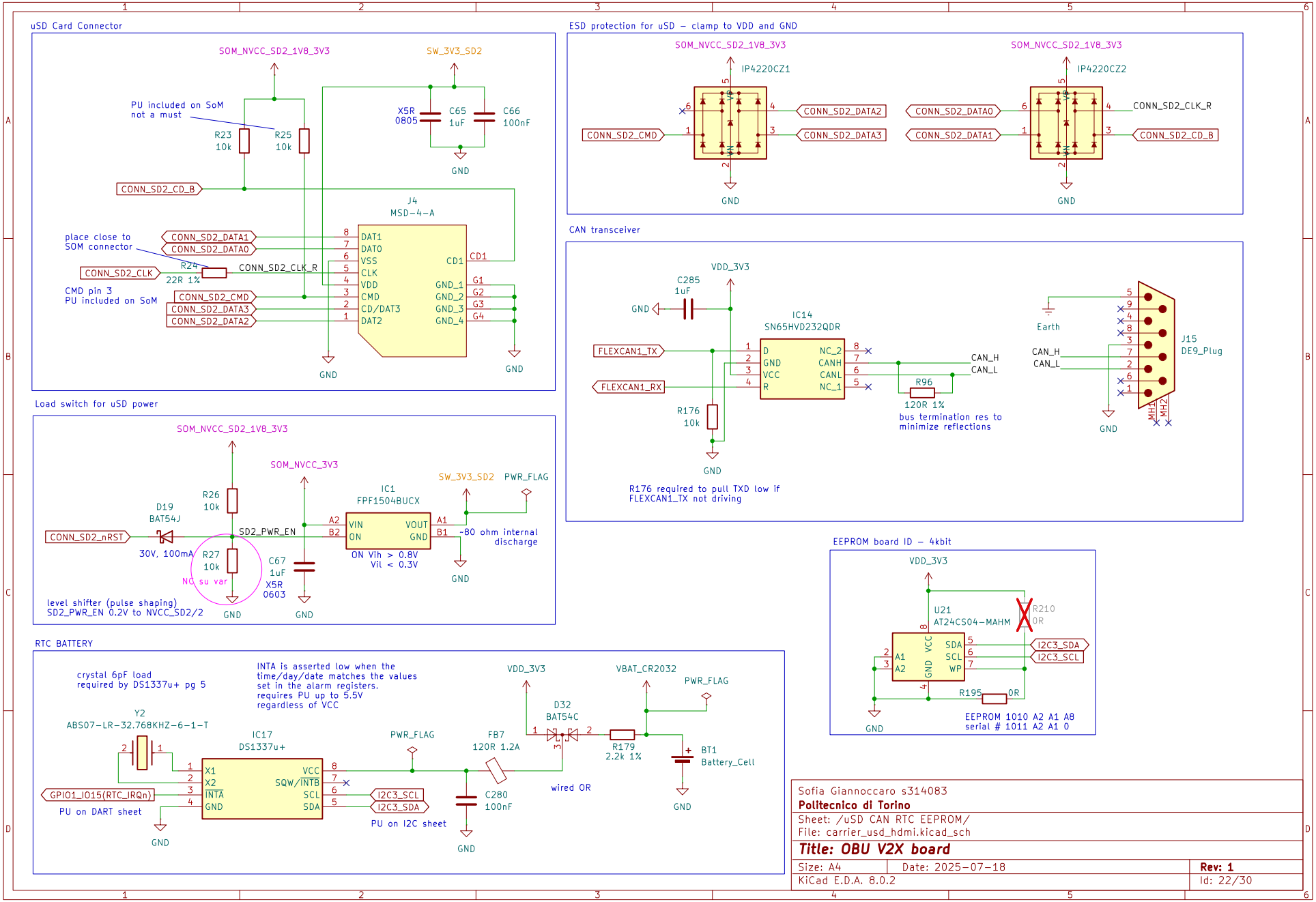


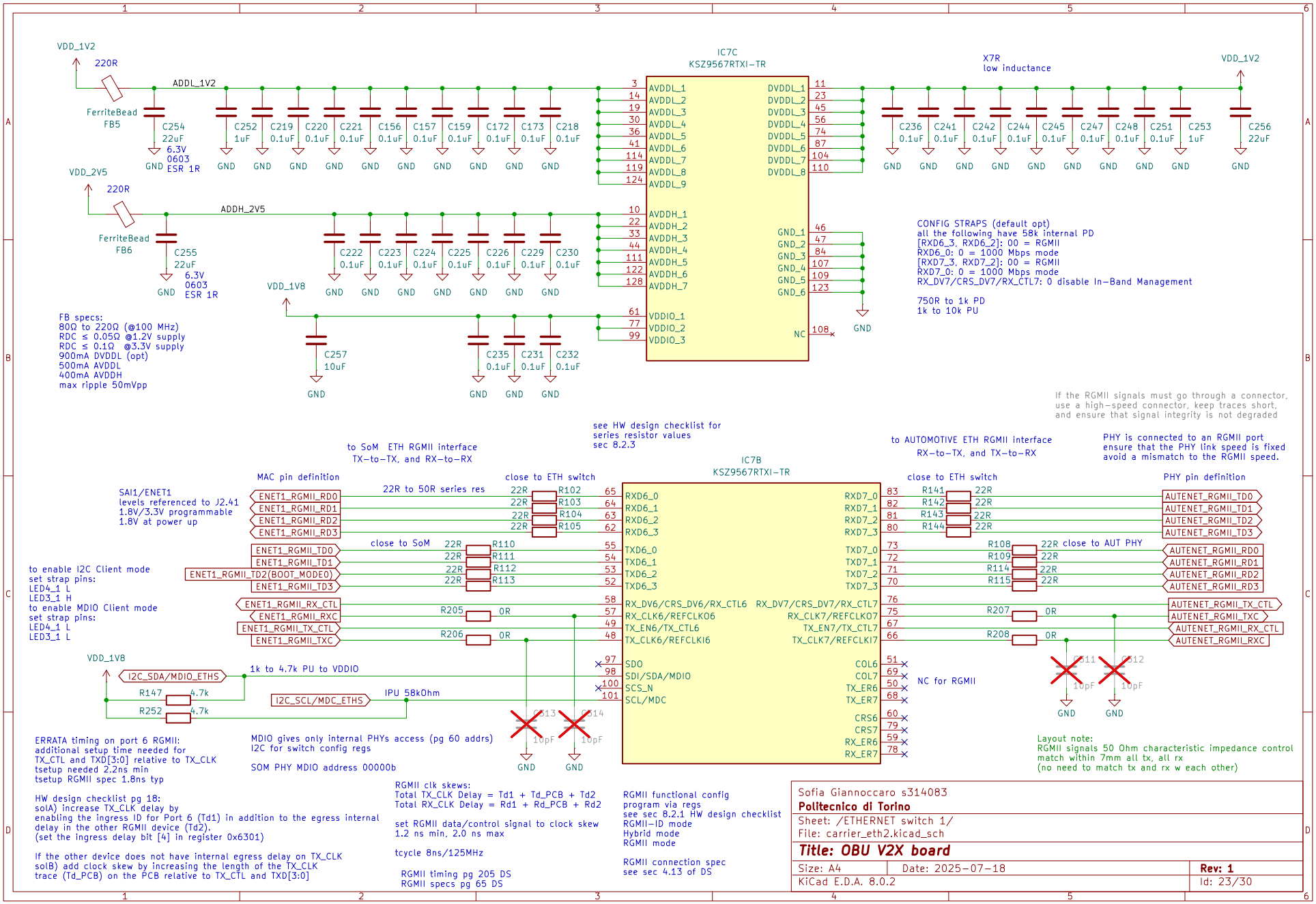
Sofia Giannoccaro s314083
Politecnico di Torino

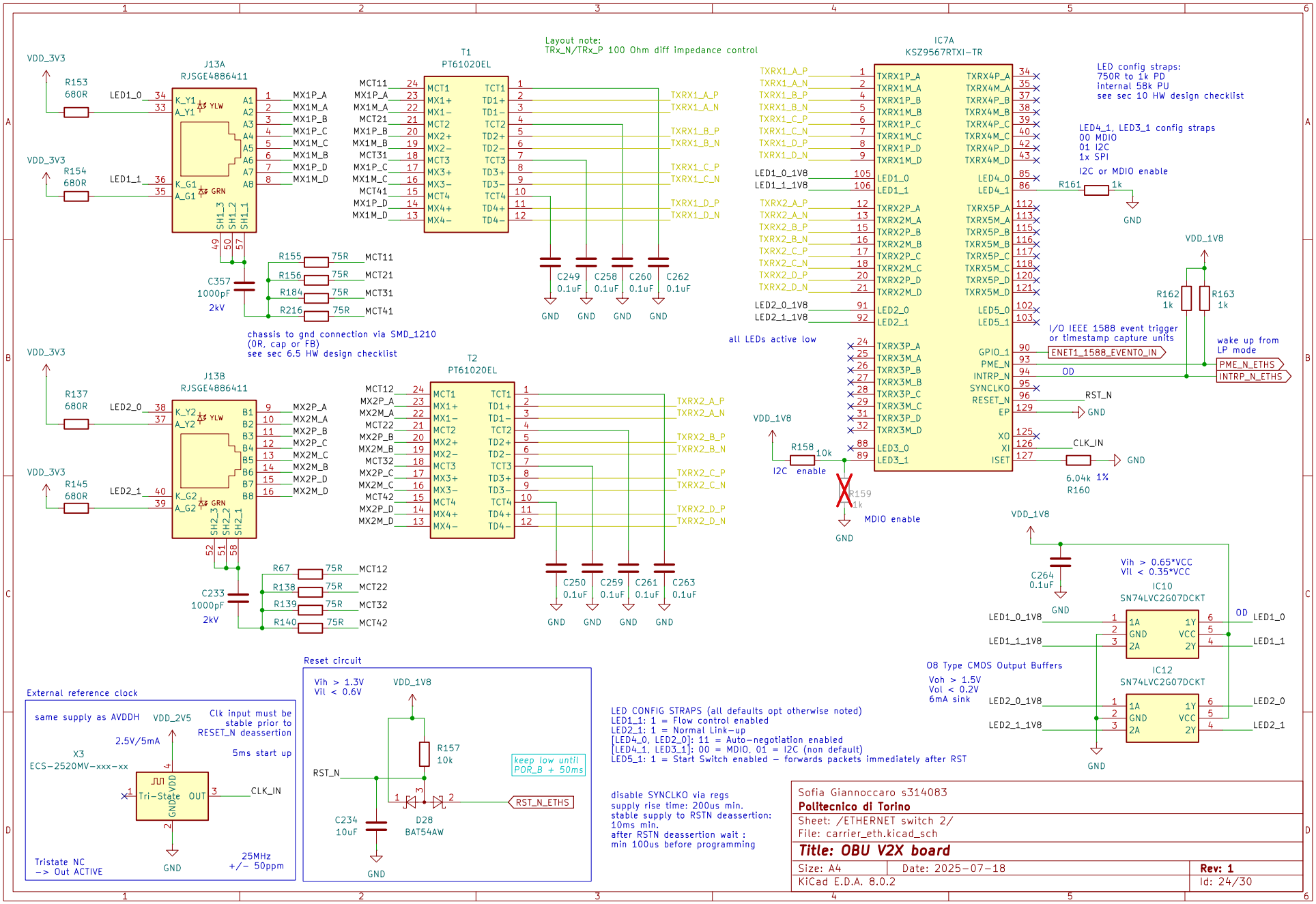
Sheet: /PCIe switch 3/
File: carrier_pcie4.kicad_sch

Title: OBU V2X board

Size: A4	Date: 2025-07-18	**Rev: 1**
KiCad E.D.A. 8.0.2		Id: 1/30

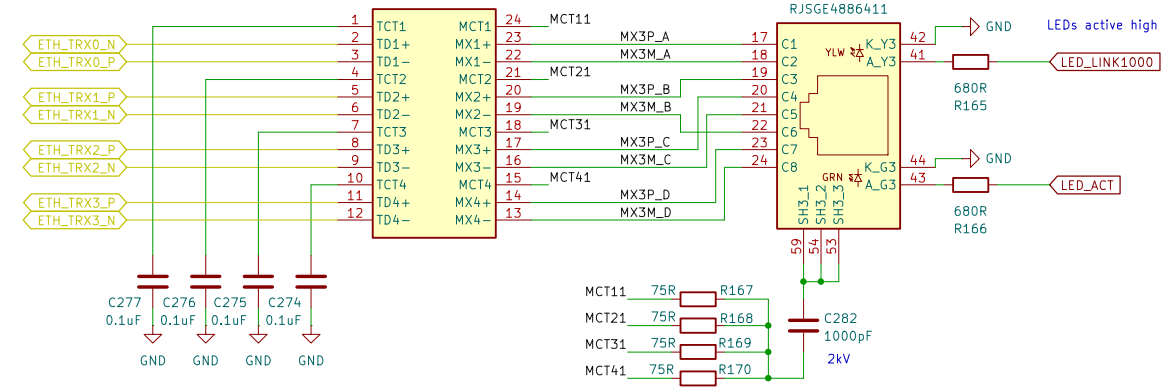

uSD Card Connector
SOM_NVCC_SD2_1V8_3V3
SW_3V3_SD2
PU included on SoM
not a must
R23
10k
R25
10k
X5R
0805
C65
1uF
C66
100nF
GND
CONN_SD2_CD_B
J4
MSD-4-A
place close to
SOM connector
CONN_SD2_DATA1
CONN_SD2_DATA0
CONN_SD2_CLK
R24
22R 1%
CONN_SD2_CLK_R
CMD pin 3
PU included on SoM
CONN_SD2_CMD
CONN_SD2_DATA3
CONN_SD2_DATA2
DAT1
DAT0
VSS
CLK
VDD
CMD
CD/DAT3
DAT2
CD1
GND_1
GND_2
GND_3
GND_4
G1
G2
G3
G4
ESD protection for uSD - clamp to VDD and GND
SOM_NVCC_SD2_1V8_3V3
IP4220CZ1
IP4220CZ2
CONN_SD2_DATA2
CONN_SD2_DATA3
CONN_SD2_DATA0
CONN_SD2_DATA1
CONN_SD2_CLK_R
CONN_SD2_CD_B
CAN transceiver
VDD_3V3
C285
1uF
IC14
SN65HVD232QDR
FLEXCAN1_TX
FLEXCAN1_RX
R176
10k
R96
120R 1%
bus termination res to
minimize reflections
CAN_H
CAN_L
Earth
J15
DE9_Plug
R176 required to pull TXD low if
FLEXCAN1_TX not driving
Load switch for uSD power
SOM_NVCC_SD2_1V8_3V3
SOM_NVCC_3V3
SW_3V3_SD2
PWR_FLAG
R26
10k
D19
BAT54J
IC1
FPF1504BUCX
CONN_SD2_nRST
SD2_PWR_EN
30V, 100mA
R27
10k
NC su var
C67
1uF
X5R
0603
ON Vih > 0.8V
Vil < 0.3V
~80 ohm internal
discharge
level shifter (pulse shaping)
SD2_PWR_EN 0.2V to NVCC_SD2/2
EEPROM board ID - 4kbit
VDD_3V3
U21
AT24CS04-MAHM
R210
0R
I2C3_SDA
I2C3_SCL
R195
0R
EEPROM 1010 A2 A1 A8
serial # 1011 A2 A1 0
RTC BATTERY
crystal 6pF load
required by DS1337u+ pg 5
INTA is asserted low when the
time/day/date matches the values
set in the alarm registers.
requires PU up to 5.5V
regardless of VCC
Y2
ABS07-LR-32.768KHZ-6-1-T
IC17
DS1337u+
GPIO1_IO15(RTC_IRQn)
PU on DART sheet
PU on I2C sheet
FB7
120R 1.2A
D32
BAT54C
VBAT_CR2032
R179
2.2k 1%
BT1
Battery_Cell
C280
100nF
wired OR
Sofia Giannoccaro s314083
Politecnico di Torino
Sheet: /uSD CAN RTC EEPROM/
File: carrier_usd_hdmi.kicad_sch
Title: OBU V2X board
Size: A4
Date: 2025-07-18
Rev: 1
KiCad E.D.A. 8.0.2
Id: 22/30


IC7C
KSZ9567RTXI-TR
VDD_1V2
220R
FerriteBead
FB5
ADDL_1V2
C254 22uF 6.3V 0603 ESR 1R
C252 1uF
C219 0.1uF
C220 0.1uF
C221 0.1uF
C156 0.1uF
C157 0.1uF
C159 0.1uF
C172 0.1uF
C173 0.1uF
C218 0.1uF
AVDDL_1
AVDDL_2
AVDDL_3
AVDDL_4
AVDDL_5
AVDDL_6
AVDDL_7
AVDDL_8
AVDDL_9
DVDDL_1
DVDDL_2
DVDDL_3
DVDDL_4
DVDDL_5
DVDDL_6
DVDDL_7
DVDDL_8
X7R
low inductance
C236 0.1uF
C241 0.1uF
C242 0.1uF
C244 0.1uF
C245 0.1uF
C247 0.1uF
C248 0.1uF
C251 0.1uF
C253 1uF
C256 22uF
VDD_2V5
220R
FerriteBead
FB6
ADDH_2V5
C255 22uF 6.3V 0603 ESR 1R
C222 0.1uF
C223 0.1uF
C224 0.1uF
C225 0.1uF
C226 0.1uF
C229 0.1uF
C230 0.1uF
AVDDH_1
AVDDH_2
AVDDH_3
AVDDH_4
AVDDH_5
AVDDH_6
AVDDH_7
VDD_1V8
C257 10uF
C235 0.1uF
C231 0.1uF
C232 0.1uF
VDDIO_1
VDDIO_2
VDDIO_3
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
NC
FB specs:
80Ω to 220Ω (@100 MHz)
RDC ≤ 0.05Ω @1.2V supply
RDC ≤ 0.1Ω @3.3V supply
900mA DVDDL (opt)
500mA AVDDL
400mA AVDDH
max ripple 50mVpp
CONFIG STRAPS (default opt)
all the following have 58k internal PD
[RXD6_3, RXD6_2]: 00 = RGMII
RXD6_0: 0 = 1000 Mbps mode
[RXD7_3, RXD7_2]: 00 = RGMII
RXD7_0: 0 = 1000 Mbps mode
RX_DV7/CRS_DV7/RX_CTL7: 0 disable In-Band Management
750R to 1k PD
1k to 10k PU
If the RGMII signals must go through a connector,
use a high-speed connector, keep traces short,
and ensure that signal integrity is not degraded
see HW design checklist for
series resistor values
sec 8.2.3
to SoM ETH RGMII interface
TX-to-TX, and RX-to-RX
IC7B
KSZ9567RTXI-TR
to AUTOMOTIVE ETH RGMII interface
RX-to-TX, and TX-to-RX
PHY is connected to an RGMII port
ensure that the PHY link speed is fixed
avoid a mismatch to the RGMII speed.
MAC pin definition
close to ETH switch
PHY pin definition
SAI1/ENET1
levels referenced to J2.41
1.8V/3.3V programmable
1.8V at power up
22R to 50R series res
ENET1_RGMII_RD0
ENET1_RGMII_RD1
ENET1_RGMII_RD2
ENET1_RGMII_RD3
ENET1_RGMII_TD0
ENET1_RGMII_TD1
ENET1_RGMII_TD2(BOOT_MODE0)
ENET1_RGMII_TD3
ENET1_RGMII_RX_CTL
ENET1_RGMII_RXC
ENET1_RGMII_TX_CTL
ENET1_RGMII_TXC
close to SoM
22R R102
22R R103
22R R104
22R R105
22R R110
22R R111
22R R112
22R R113
R205 0R
R206 0R
RXD6_0
RXD6_1
RXD6_2
RXD6_3
TXD6_0
TXD6_1
TXD6_2
TXD6_3
RX_DV6/CRS_DV6/RX_CTL6
RX_CLK6/REFCLKO6
TX_EN6/TX_CTL6
TX_CLK6/REFCLKI6
RXD7_0
RXD7_1
RXD7_2
RXD7_3
TXD7_0
TXD7_1
TXD7_2
TXD7_3
RX_DV7/CRS_DV7/RX_CTL7
RX_CLK7/REFCLKO7
TX_EN7/TX_CTL7
TX_CLK7/REFCLKI7
close to ETH switch
R141 22R
R142 22R
R143 22R
R144 22R
R108 22R close to AUT PHY
R109 22R
R114 22R
R115 22R
R207 0R
R208 0R
AUTENET_RGMII_TD0
AUTENET_RGMII_TD1
AUTENET_RGMII_TD2
AUTENET_RGMII_TD3
AUTENET_RGMII_RD0
AUTENET_RGMII_RD1
AUTENET_RGMII_RD2
AUTENET_RGMII_RD3
AUTENET_RGMII_TX_CTL
AUTENET_RGMII_TXC
AUTENET_RGMII_RX_CTL
AUTENET_RGMII_RXC
C511 10pF
C512 10pF
to enable I2C Client mode
set strap pins:
LED4_1 L
LED3_1 H
to enable MDIO Client mode
set strap pins:
LED4_1 L
LED3_1 L
VDD_1V8
I2C_SDA/MDIO_ETHS
I2C_SCL/MDC_ETHS
1k to 4.7k PU to VDDIO
IPU 58kOhm
R147 4.7k
R252 4.7k
SDO
SDI/SDA/MDIO
SCS_N
SCL/MDC
C513 10pF
C514 10pF
COL6
COL7
TX_ER6
TX_ER7
CRS6
CRS7
RX_ER6
RX_ER7
NC for RGMII
ERRATA timing on port 6 RGMII:
additional setup time needed for
TX_CTL and TXD[3:0] relative to TX_CLK
tsetup needed 2.2ns min
tsetup RGMII spec 1.8ns typ
HW design checklist pg 18:
solA) increase TX_CLK delay by
enabling the ingress ID for Port 6 (Td1) in addition to the egress internal
delay in the other RGMII device (Td2).
(set the ingress delay bit [4] in register 0x6301)
If the other device does not have internal egress delay on TX_CLK
solB) add clock skew by increasing the length of the TX_CLK
trace (Td_PCB) on the PCB relative to TX_CTL and TXD[3:0]
MDIO gives only internal PHYs access (pg 60 addrs)
I2C for switch config regs
SOM PHY MDIO address 00000b
RGMII clk skews:
Total TX_CLK Delay = Td1 + Td_PCB + Td2
Total RX_CLK Delay = Rd1 + Rd_PCB + Rd2
set RGMII data/control signal to clock skew
1.2 ns min, 2.0 ns max
tcycle 8ns/125MHz
RGMII timing pg 205 DS
RGMII specs pg 65 DS
RGMII functional config
program via regs
see sec 8.2.1 HW design checklist
RGMII-ID mode
Hybrid mode
RGMII mode
RGMII connection spec
see sec 4.13 of DS
Layout note:
RGMII signals 50 Ohm characteristic impedance control
match within 7mm all tx, all rx
(no need to match tx and rx w each other)
Sofia Giannoccaro s314083
Politecnico di Torino
Sheet: /ETHERNET switch 1/
File: carrier_eth2.kicad_sch
Title: OBU V2X board
Size: A4
Date: 2025-07-18
Rev: 1
KiCad E.D.A. 8.0.2
Id: 23/30

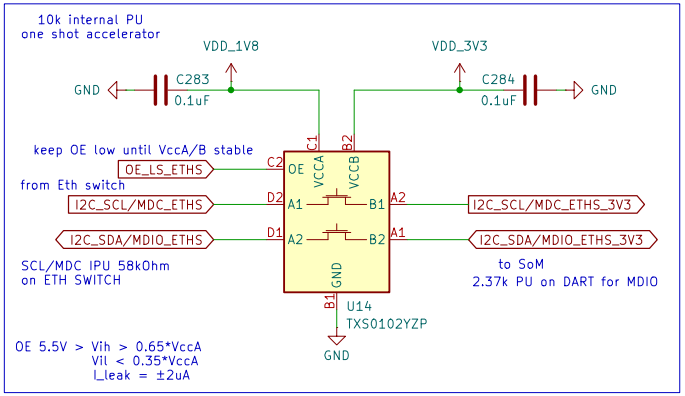

J13A
RJSGE4886411
J13B
RJSGE4886411
T1
PT61020EL
T2
PT61020EL
IC7A
KSZ9567RTXI-TR
Layout note:
TRx_N/TRx_P 100 Ohm diff impedance control
chassis to gnd connection via SMD_1210
(OR, cap or FB)
see sec 6.5 HW design checklist
LED config straps:
750R to 1k PD
internal 58k PU
see sec 10 HW design checklist
LED4_1, LED3_1 config straps
00 MDIO
01 I2C
1x SPI
I2C or MDIO enable
all LEDs active low
I/O IEEE 1588 event trigger
or timestamp capture units
wake up from
LP mode
I2C enable
MDIO enable
Vih > 0.65*VCC
Vil < 0.35*VCC
IC10
SN74LVC2G07DCKT
IC12
SN74LVC2G07DCKT
O8 Type CMOS Output Buffers
Voh > 1.5V
Vol < 0.2V
6mA sink
External reference clock
same supply as AVDDH
Clk input must be
stable prior to
RESET_N deassertion
2.5V/5mA
5ms start up
X3
ECS-2520MV-xxx-xx
Tri-State
Tristate NC
-> Out ACTIVE
25MHz
+/- 50ppm
Reset circuit
Vih > 1.3V
Vil < 0.6V
keep low until
POR_B + 50ms
D28
BAT54AW
LED CONFIG STRAPS (all defaults opt otherwise noted)
LED1_1: 1 = Flow control enabled
LED2_1: 1 = Normal Link-up
[LED4_0, LED2_0]: 11 = Auto-negotiation enabled
[LED4_1, LED3_1]: 00 = MDIO, 01 = I2C (non default)
LED5_1: 1 = Start Switch enabled - forwards packets immediately after RST
disable SYNCLKO via regs
supply rise time: 200us min.
stable supply to RSTN deassertion:
10ms min.
after RSTN deassertion wait :
min 100us before programming
Sofia Giannoccaro s314083
Politecnico di Torino
Sheet: /ETHERNET switch 2/
File: carrier_eth.kicad_sch
Title: OBU V2X board
Size: A4
Date: 2025-07-18
Rev: 1
KiCad E.D.A. 8.0.2
Id: 24/30

Ethernet PHY integrated on SoM

Layout note:
TRx_N/TRx_P 100 Ohm diff impedance control



LEVEL SHIFTER 1.8V to 3.3V for MDIO DART pin J1.11 J1.13 compatibility

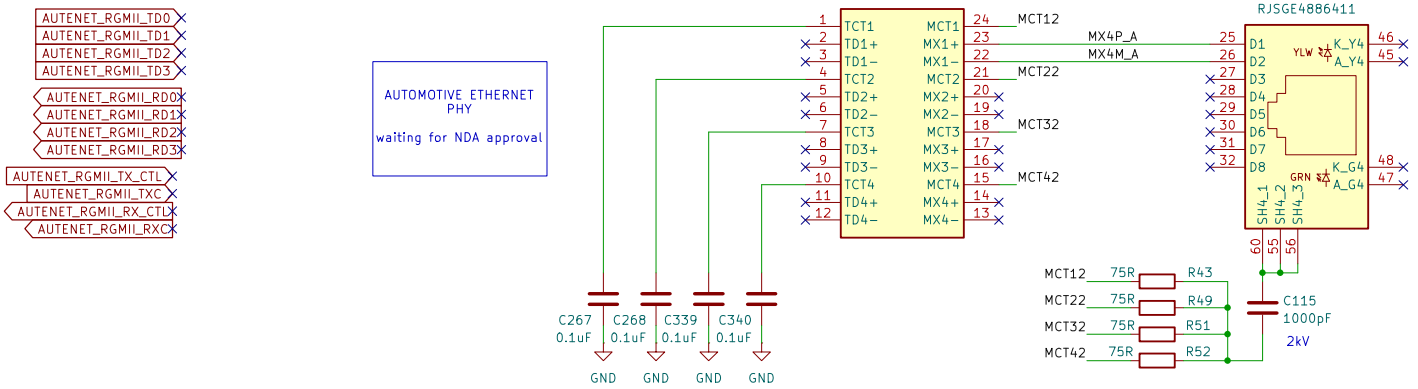


IPU 58k del SCL/MDC del ETH SW
PU 4.7k di SDA/MDIO on board pg 24

IPU 2.37k DART MDIO
on DART both MDC and MDIO are connected to TXS0102

10k IPU TXS0102

Automotive ethernet PHY + connector RJ45



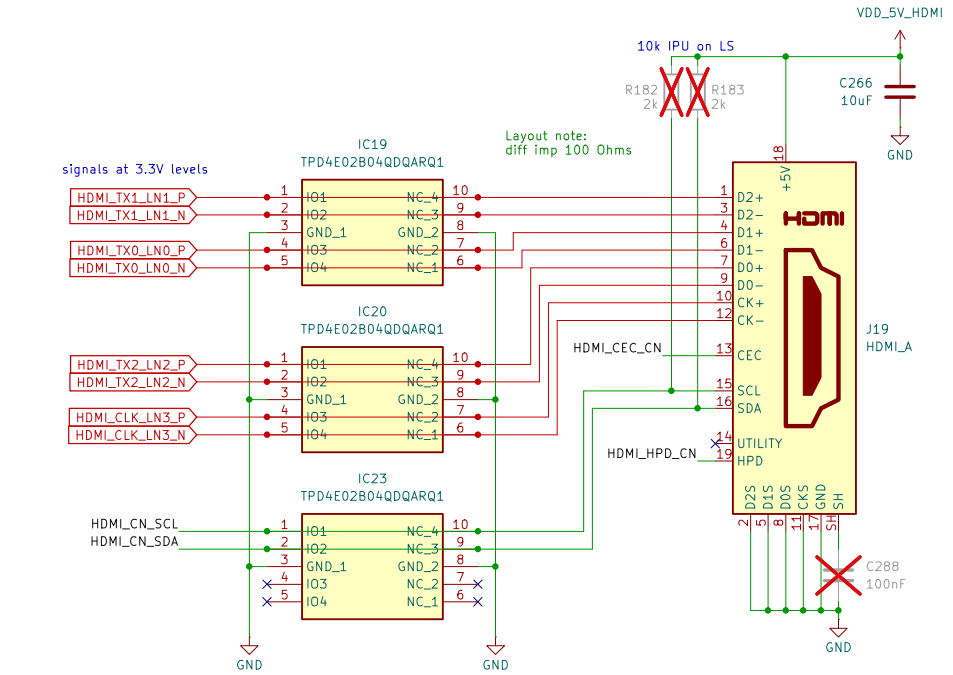
su entrambe le porte RGMII:
- delay interno
- RC fatto con R 0 ohm e C do not place. montiamo 0R default .
C piazzato solo se non riusciamo a settare il ritardo con I2C registri .
(100ohm 10pF)
- lunghezza traccia

ritardo impostabile su tx dello switch fisso solo 1.3ns typ, max 1.5ns XMII Port Control 1 Reg pg 65, 156, 205

vedi bene anche lato dart processore nxp imx8m plus

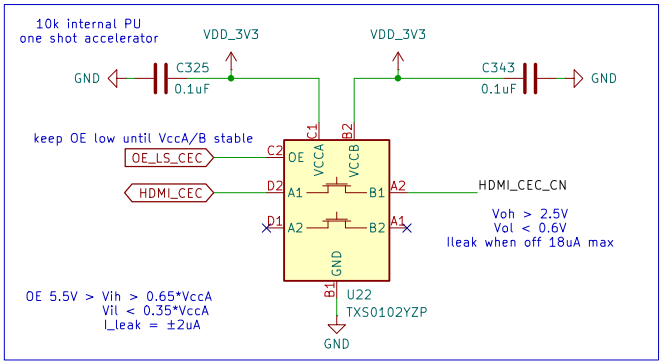
Sofia Giannoccaro s314083
Politecnico di Torino

Sheet: /Ethernet – SoM integrated PHY/
File: carrier_eth3.kicad_sch
Title: OBU V2X board
Size: A4 | Date: 2025-07-18 | **Rev: 1**
KiCad E.D.A. 8.0.2 | Id: 25/30

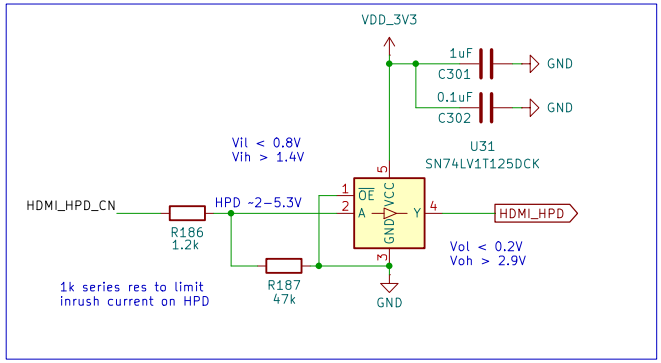


CEC control msgs btw source and sink
one wire bidirectional comm
OD line req PU 3.3V

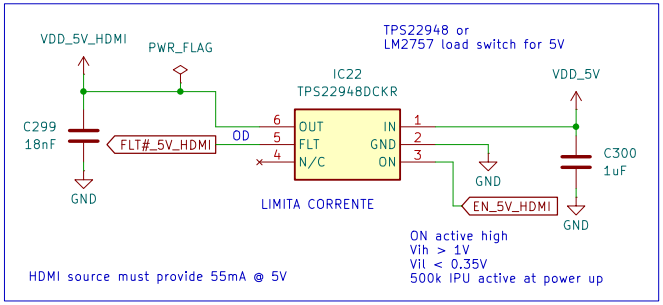
CEC pull ups and protections 3.3V level signal



LS CMOS tri-state output 5V to 3.3V

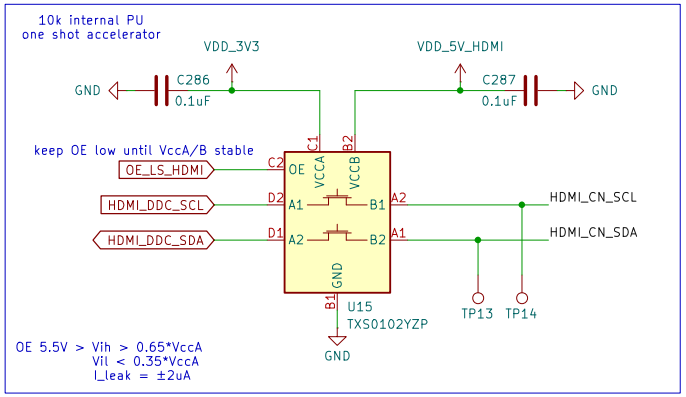


Load switch 5V



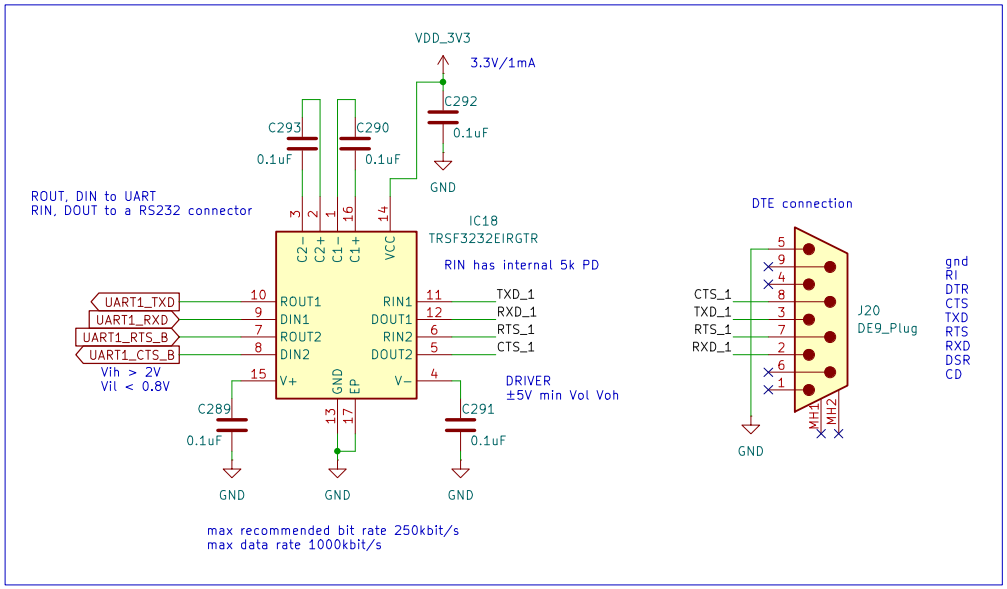
Load switch pros:
short circut protection
reverse current blocking
fast response

LEVEL SHIFTER 3.3V to 5V for HDMI DART vs Connector compatibility

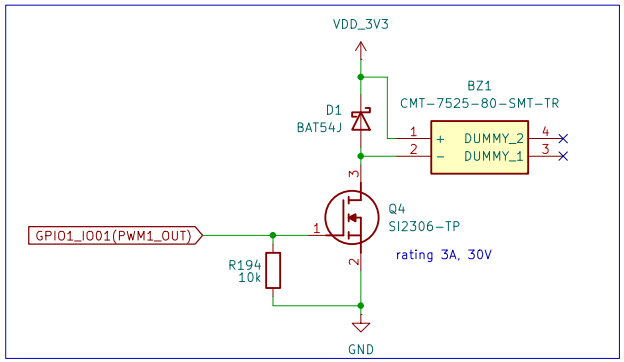


Sofia Giannoccaro s314083
Politecnico di Torino
Sheet: /HDMI/
File: crrier_hdmi_varie.kicad_sch
Title: OBU V2X board
Size: A4 | Date: 2025-07-18 | **Rev: 1**
KiCad E.D.A. 8.0.2 | Id: 1/30

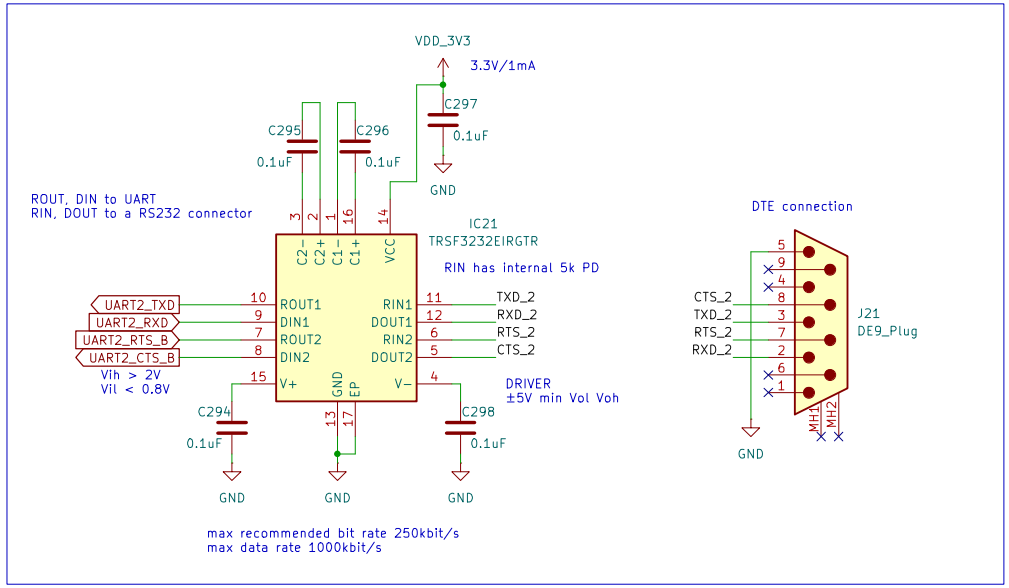
UART RS232 port 1



Buzzer PWM ctrl



UART RS232 port 2



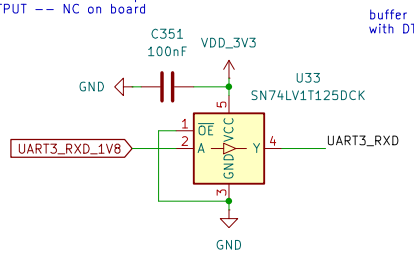
Sofia Giannoccaro s314083
Politecnico di Torino
Sheet: /RS232 Buzzer/
File: carrier_uart.kicad_sch

Title: OBU V2X board

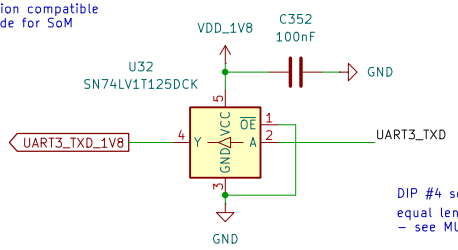
Size: A4	Date: 2025-07-18	**Rev: 1**
KiCad E.D.A. 8.0.2		Id: 27/30

Header compatible with CubeV2X non standard miniPCIe module

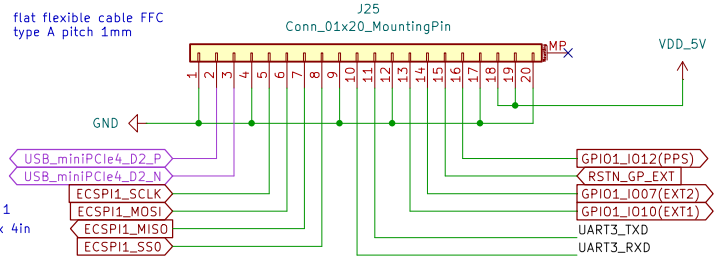
exported for CUBE V2X miniPCIe adapter:
3.3V miniPCIe OUTPUT -- NC on board
UART_TX
UART_RX
GPIO0, GPIO1
SPI_MOSI
SPI_MISO
SPI_CLK
SPI_CS
PPS
USB_DM
USB_DP
RST
5V/1A
GND



buffer direction compatible
with DTE mode for SoM



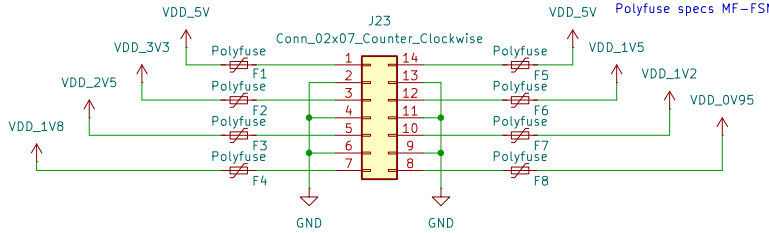
flat flexible cable FFC
type A pitch 1mm



DIP #4 select = 1
equal length max 4in
– see MUX DS

Power supply header

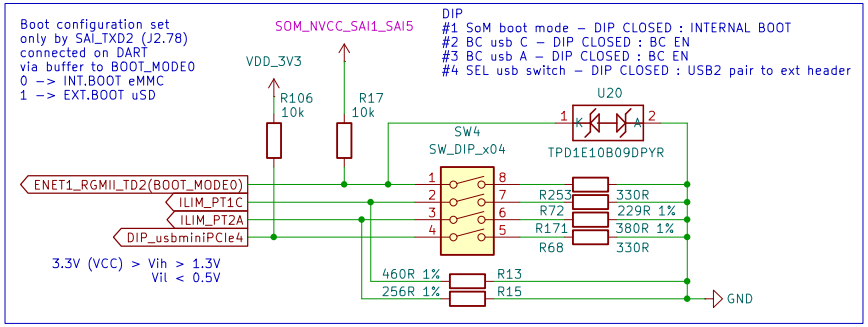
2x 5V
1x 3.3V
1x 2.5V
1x 1.8V
1x 1.5V
1x 1.2V
1x 0.95V



Polyfuse specs MF-FSML050/8-2
Ihold 0.5A
Itrip 1A
Imax 50A
Vmax 8V

DIP Switch

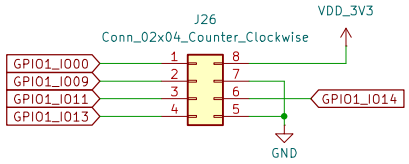
Boot configuration set
only by SAI_TXD2 (J2.78)
connected on DART
via buffer to BOOT_MODE0
0 -> INT.BOOT eMMC
1 -> EXT.BOOT uSD



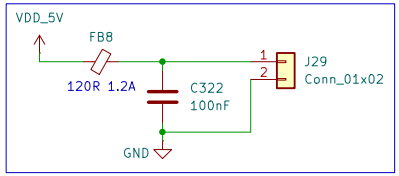
DIP
#1 SoM boot mode – DIP CLOSED : INTERNAL BOOT
#2 BC usb C – DIP CLOSED : BC EN
#3 BC usb A – DIP CLOSED : BC EN
#4 SEL usb switch – DIP CLOSED : USB2 pair to ext header

3.3V (VCC) > Vih > 1.3V
Vil < 0.5V

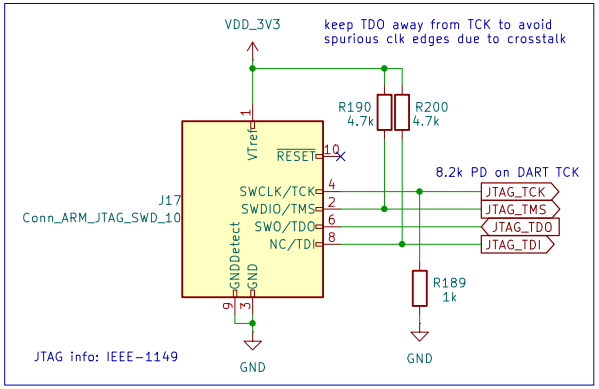
GPIO Header from DART SoM

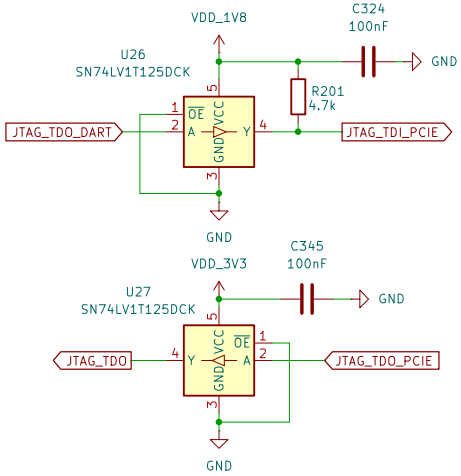


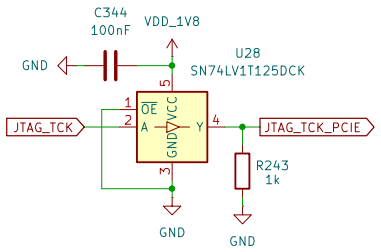
Fan connector

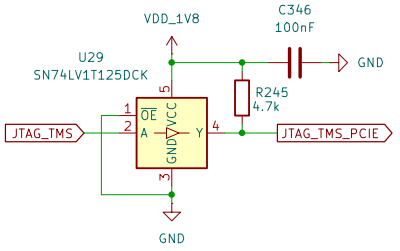


JTAG chain – DART SoM and PCIe switch – 10 pin header







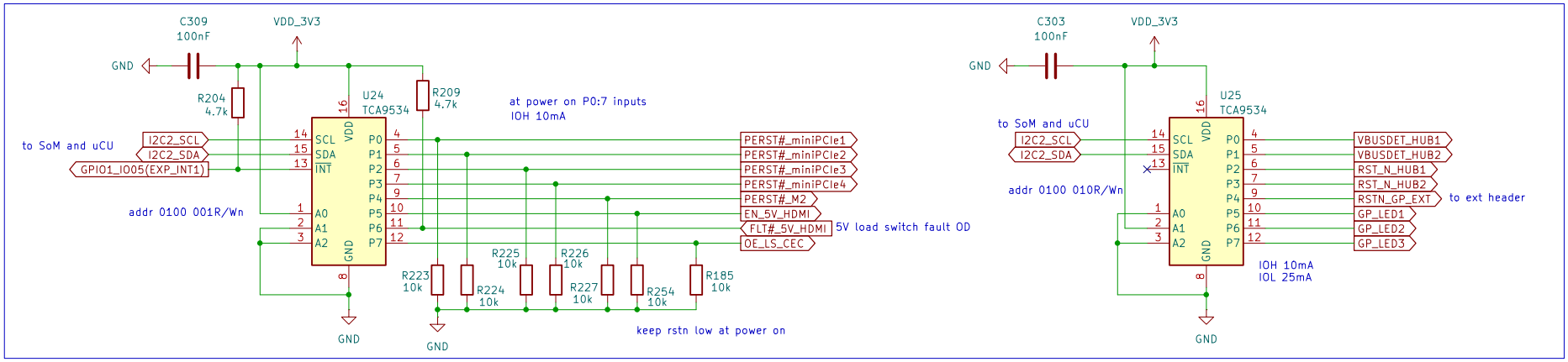


Sofia Giannoccaro s314083
Politecnico di Torino
Sheet: /Headers 1/
File: ext_headers_1.kicad_sch

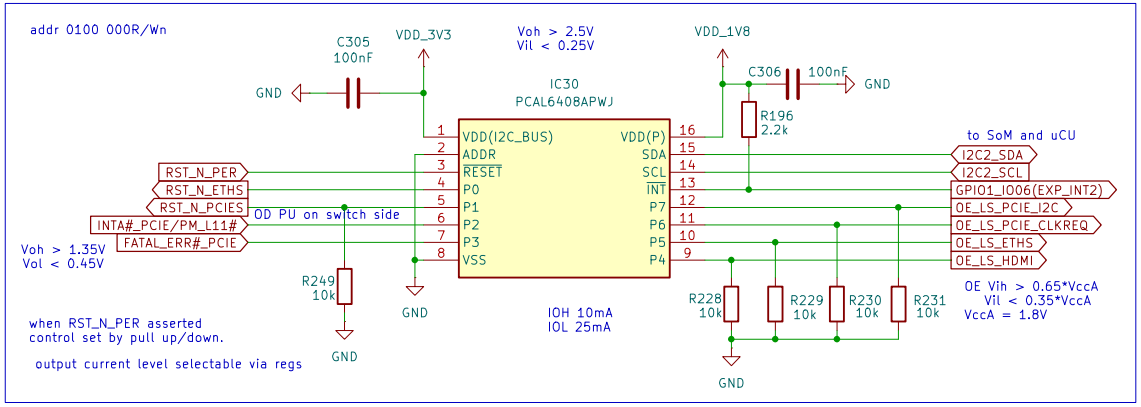
Title: OBU V2X board

Size: A4	Date: 2025-07-18	**Rev: 1**
KiCad E.D.A. 8.0.2		Id: 1/30

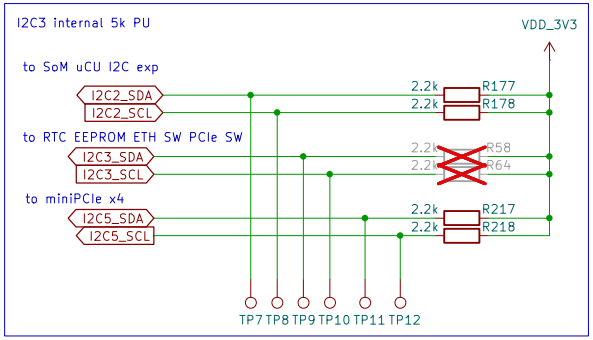
I2C2 IO expander – multimaster uCU SoM



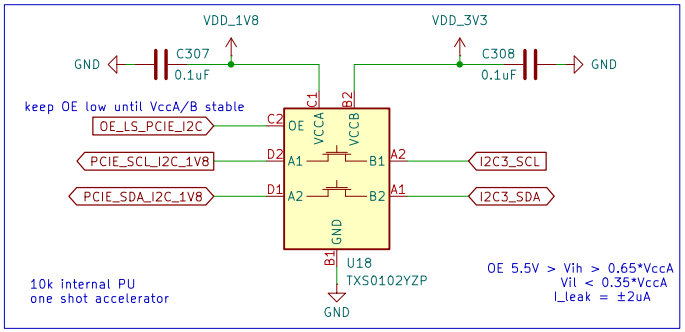
I2C2 IO expander – multimaster uCU SoM – 1.8V IO

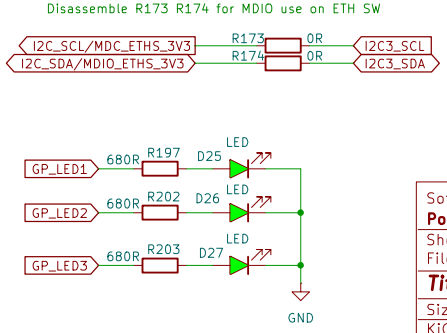


I2C PU



LEVEL SHIFTER 1.8V to 3.3V for I2C PCIe sw





note su SoM I2C interfaces
I2C1 UNUSED interno a SoM non usato su Carrier!!
I2C2 a uCU e I2C exp:
0x40 I2C exp 1.8V
0x42 I2C exp 3.3V
0x44 I2C exp 3.3V
I2C3 (5k internal PU on DART):
0x68 1101000 RTC
0x50 101000A8 (serial# 0x58 1011000) EEPROM board ID
0x5F 1011_111 ETH SW
0x6F 1101111b PCIe SW
I2C4 UNUSED interno a SoM for BT func
I2C5 a miniPCIe x4

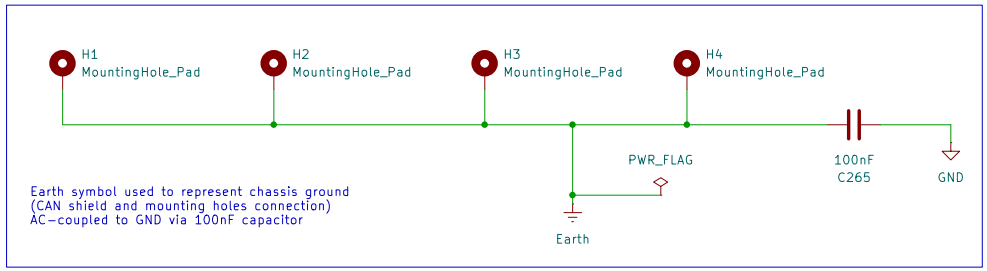
Sofia Giannoccaro s314083
Politecnico di Torino

Sheet: /I2C expander/
File: i2c_exp.kicad_sch

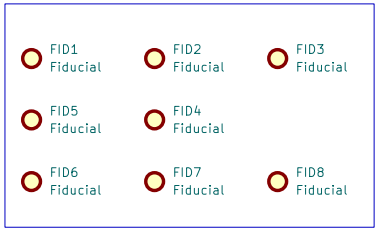
Title: OBU V2X board

Size: A4	Date: 2025-07-18	**Rev: 1**
KiCad E.D.A. 8.0.2		Id: 1/30

Mounting hole M3 3.2mm DIN965



Fiducials 1.5mm 3mm mask
2 su BGA e 3 a L su angoli del PCB



SOM MOUNTING STANDOFFs
TH-1.6-1.5-M2
manufacturer: MAC8
https://www.mac8japan.com/products/258

rst sgn to generate:
VBUS_DET_UHUB1
RST_N_UHUB1
VBUS_DET_UHUB2
RST_N_UHUB2
PERST#_miniPCIe1
PERST#_miniPCIe2
PERST#_miniPCIe3
PERST#_miniPCIe4
PERST#_M2
RST_N_ETHS (occhio che va a 1.8V)
RST_N_PCIES (pcie sw 1.8V)

VBUSDET e RSTHUB Schmiddt triggered input 3.3V
In embedded applications, VBUS_DET may be controlled (toggled)
when the host desires to renegotiate a connection without requiring a
full reset of the device

(list includes I2C signals connected to I2C exp multimaster SoM uCU)

OE_LS_PCIE_CLKREQ
OE_LS_ETHS
OE_LS_HDMI

OE Vih > 0.65*VccA ; VccA = 1.8V
Vil < 0.35*VccA

uCU output enable to generate:
EN_0V95
EN_1V2
EN_1V5
EN_1V8
EN_2V5
EN_3V3
EN_1V (LDO)
EN_5V_HDMI (LOAD SWITCH)

ENABLE:
Vih > 1V
Vil < 0.4V
ENABLE 3.3V 0.95V:
Vih > 0.9V
Vil < 0.4V

EN 1V LDO
Vih > 0.9V
Vil < 0.3V

EN 5V HDMI
Vih > 1V
Vil < 0.35V

start activating EN after PG received, according to power sequencing reqs:
1.2V rise bf or at the same rate of 3.3V

uCU inputs:
PG_0V95
PG_1V2
PG_1V5
PG_1V8
PG_2V5
PG_3V3

Open Drain output
1mA sink
PU on DCDC converter side already placed

exported signals:
20 pins GPIO header (9 GND, 2 PWM, 4 ANALOG, 4 DIGITAL, 1 EVENTOUT)
SPI
I2C master
UART
SWD

Sofia Giannoccaro s314083
Politecnico di Torino
Sheet: /Mechanics/
File: aut_enet2.kicad_sch

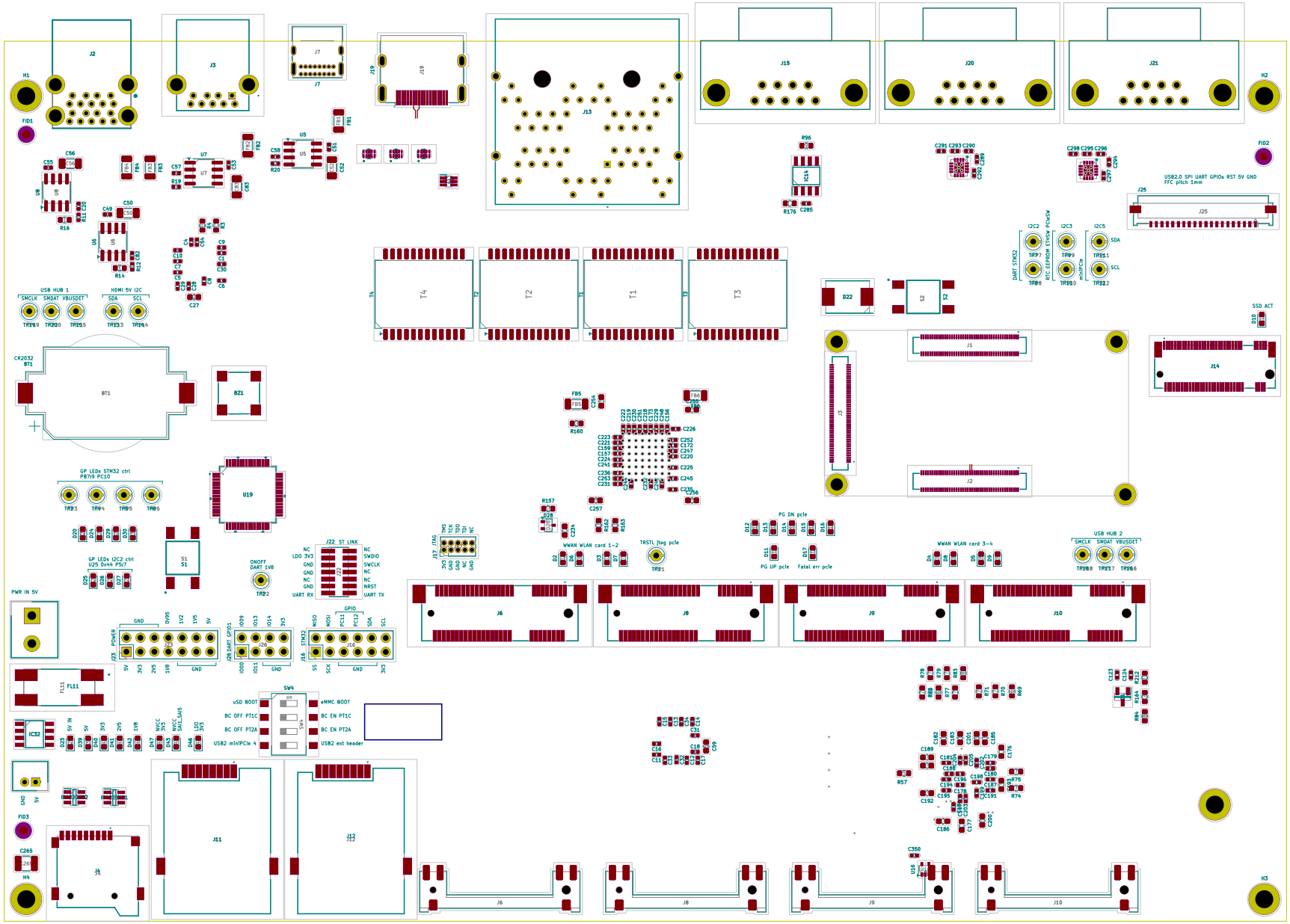
Title: OBU V2X board

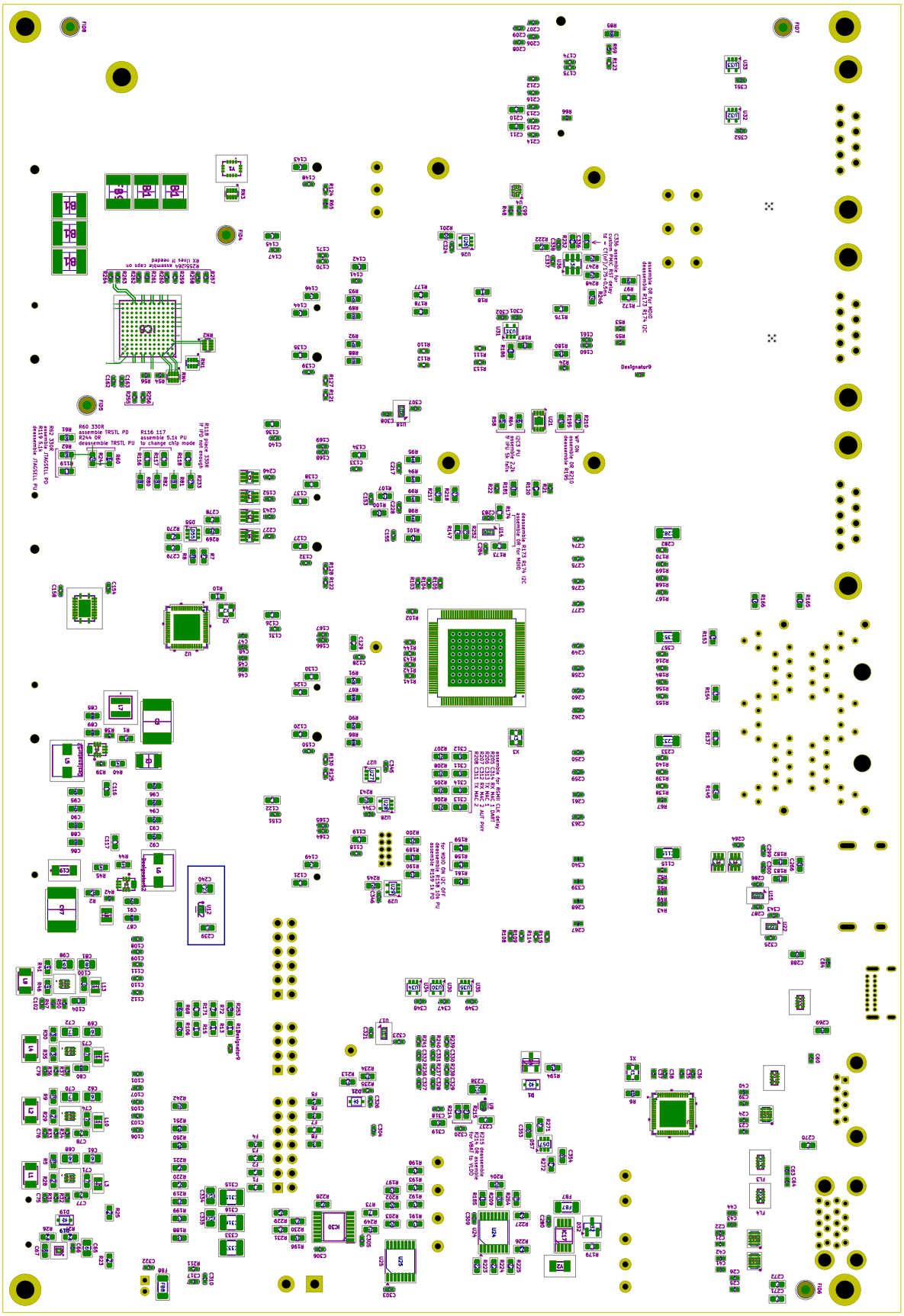
Size: A4	Date: 2025-07-18	**Rev: 1**
KiCad E.D.A. 8.0.2		Id: 1/30

Appendix B
PCB layout view

Sheet 1 Front Footprints and Silkscreen

Sheet 2 Back Footprints and Silkscreen


USB HUB 1
SMCLK SMDAT VBUSDET
HDMI 5V I2C
SDA SCL
GP LEDs STM32 ctrl
P87:9 PC10
GP LEDs I2C2 ctrl
U25 0x44 P5:7
ONOFF
DART LV8
PWR IN 5V
J22 ST LINK
NC
LDO 3V3
GND
SWDIO
SWCLK
NRST
UART RX
UART TX
J17 JTAG
TMS
TCK
TDO
TDI
WWAN WLAN card 1-2
TRSTL Jtag pcie
PG DN pcie
PG UP pcie
Fatal err pcie
WWAN WLAN card 3-4
USB HUB 2
USB2.0 SPI UART GPIOs RST 5V GND
FFC pitch 1mm
I2C2
I2C3
I2C5
DART STM32
RTC EEPROM ETH5V PCIe5V
miniPCIe
SSD ACT
J23 POWER
J26 UART GPIO1
J16 STM32
GPIO
MISO
MOSI
SCK
SW4
uSD BOOT
eMMC BOOT
BC OFF PT1C
BC EN PT1C
BC OFF PT2A
BC EN PT2A
USB2 miniPCIe 4
USB2 ext header
J6
J8
J9
J10
J11
J12
J13
J15
J20
J21
J25
J1
J2
J3
J14
T1
T2
T3
T4
BT1
CR2032
BT1
BZ1
U19
IC32
IC24
H1
H2
H3
H4
FID1
FID2
FID3



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