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# Biodegradable CMOS-based Wireless Power Transfer Device for Remote Sensing Applications

Master's degree in Electronic Engineering

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# Abstract

The growing demand for electronic devices in environmental, healthcare remote sensing and Internet of Things (IoT) applications has raised critical concerns about sustainability, electronic waste (e-waste), and safety in implantable systems. In precision agriculture (PA), dense and real-time field monitoring is still limited by battery-powered nodes that require periodic maintenance and retrieval, by non-biodegradable hardware that accumulates as environmental pollution in soil, and by the cost and complexity that limits sensor density and spatial resolution.

To address these challenges, a promising direction for modern sensing platforms is to become (a) biodegradable to minimize long-term impact, (b) autonomous via wireless power transfer (WPT) to eliminate toxic batteries, and (c) integrated with CMOS technology to ensure efficient energy conversion, robust signal processing, and advanced multi-functionality.

Despite significant progress, today's solutions address these aspects only partially, lacking a fully biodegradable system that combines WPT, sensing, and CMOS integrated circuits (IC) on the same substrate. This thesis tackles this gap by focusing on an intermediate yet crucial goal: the design and fabrication of a biodegradable WPT device for field deployment in precision agriculture, developed through photolithography-based processes as the starting point for future integration with CMOS and sensing components.

The device realized in this work is an LC coil receiving antenna operating at 6.78 MHz, based on Near-Field Communication (NFC), a wireless power transfer technique based on inductive coupling that is well suited for short-distance ($\approx$ 10 cm), low-power (mW) sensing applications. The receiver (Rx) coil harvests power from an external, electrically supplied transmitter (Tx) that can be carried by a drone, a wearable patch, or a rover (as in this project). To support later functions, the design includes two external output pads for interconnection and integration with a CMOS chip.

To ensure biodegradability, polylactic acid (PLA) was used as both substrate and encapsulant, silicon oxide/nitride as insulators, and molybdenum (Mo) for the metal layers. While environmentally compatible, these choices introduce major challenges: (i) PLA's glass-transition temperature ($\approx$ 65 °C) and melting point ($\approx$ 150 °C) impose a strict thermal budget on fabrication and complicate PLA/$SiO_2$/Mo interface engineering; (ii) biodegradable metals such as Mo exhibit higher resistivity than standard conductors (Cu, Au, Ag, Al), reducing the LC coil's quality factor and thereby limiting WPT efficiency, here estimated at $\approx$ 28% compared to >50% in conventional systems.

A cleanroom-compatible process flow was developed at Delft University of Technology (Else Kooi Laboratory and Kavli NanoLab), exploiting advanced photolithography (direct laser writing) to pattern the LC coil on biodegradable substrates. The process was validated through systematic experiments that optimized Mo patterning on different substrates (PLA, Dextran + PLA, Dextran and $SiO_2$). The results demonstrate that adapting biodegradable polymeric substrates to microfabrication is challenging but feasible, establishing a solid foundation for further development.

This work provides the basis for biodegradable WPT devices fabrication and paves the way toward their integration with CMOS ICs and sensors. Future perspectives include using sacrificial layers (e.g. Dextran) in a different process sequence, to facilitate fabrication before final PLA deposition, and the extension of the developed flowchart toward the fabrication of fully integrated biodegradable systems.

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# Introduction on Biodegradable Electronics

Remote sensing and Internet-of-Things (IoT) technologies are increasingly required to be sustainable, autonomous, and efficient, particularly in medical and environmental applications [1]. Within this framework, this thesis explores the fabrication of a biodegradable Wireless Power Transfer (WPT) device integrating a Complementary-Metal-Oxide-Semiconductor (CMOS) chip and sensor.

A promising approach for such systems is to be **1) biodegradable** to reduce long-term impact, **2) energetically autonomous** by wireless power transfer, and **3)** able to ensure efficient energy conversion while enabling new functionalities by **integrating a CMOS chip**.

In this first chapter, each of these aspects will be addressed. The analysis begins by outlining advantages of biodegradability in Section 1.1. Subsequently, current solutions developed for wireless biodegradable systems without CMOS integration are reported in Section 1.2, highlighting their functional limitations. In section 1.3, it then moves on to examine non-biodegradable systems in which WPT, sensors, and CMOS technology are combined. A survey on biodegradable materials for electronics in then presented in Section 1.4. Finally, in Section 1.5 the state-of-the-art in biodegradable system integration is discussed and the purpose of the thesis is stated. This methodical approach will outline the novel contributions of this work and helps to clearly define the state of technology today.

## 1.1 Advantages of Biodegradability

The rapid growth of the electronic industry and the widespread deployment of electronic devices across medical and environmental applications have raised urgent concerns and challenges regarding sustainability, electronic waste (e-waste), and long-term safety in biomedical implants [1] [2]. According to recent estimates, the global volume of e-waste reached 53.6 million tons in 2020 and is projected to increase to 74 million tons by 2030 [1]. Conventional electronics, typically composed of non-degradable materials (e.g. heavy metals) that persist in the environment or within the human body, contribute to environmental pollution and pose significant health risks in medical applications [1] [2] [3].

In response to these challenges, in recent years Biodegradable Electronics - also referred to as Transient or Eco-friendly electronics - has emerged as a promising solution by developing biodegradable devices that safely and naturally decompose after use, either in biological fluids or natural environments, leaving non-toxic degradation by-products. Biodegradable electronics offer a fundamentally different and innovative approach to device design by enabling temporary functionality [3] [4] [5].

Among the many device types being developed, biodegradable sensors have been particularly investigated in recent years. These sensors have been engineered to monitor a wide range of physical, chemical, and biological parameters - including temperature, pressure, strain, hydration levels, and pH - within the body or the environment, over a defined operational period [6] [7] [8].

The applications of biodegradable sensors are diverse and rapidly expanding. These platforms exhibit notable versatility due to their biocompatibility, and hold considerable advantages over their non-biodegradable counterparts [9]. The two main applications of interest for this project are:

- **Medical Applications (Health-Care and Implantable)**
  In the biomedical field, biodegradable devices are used to create implantable or wearable sensors, drug delivery systems, stimulators, neural probes and many other systems (as briefly summarized in Figure 1.3) that operate over a clinically relevant timescale and then dissolve [6] [7]. In this way, especially in case of biomedical implants, they offer significant improvements:

  1. **Elimination of Removal Surgery**
     Biogradable devices eliminate the need for secondary surgeries to remove the implant, reducing both patient risk and healthcare costs [6] [7].
  2. **High biocompatibility**
     They are often integrated into soft, flexible substrates that mechanically

match soft and stretchable tissues, improving biocompatibility and conformality [10] [11].

3. **Safety**
   Clinically, they reduce the risks associated with permanent implants (such as infection, mechanical mismatch, or scarring) by degrading safely after fulfilling their diagnostic or therapeutic roles, minimizing immune responses and chronic inflammation [10] [11].

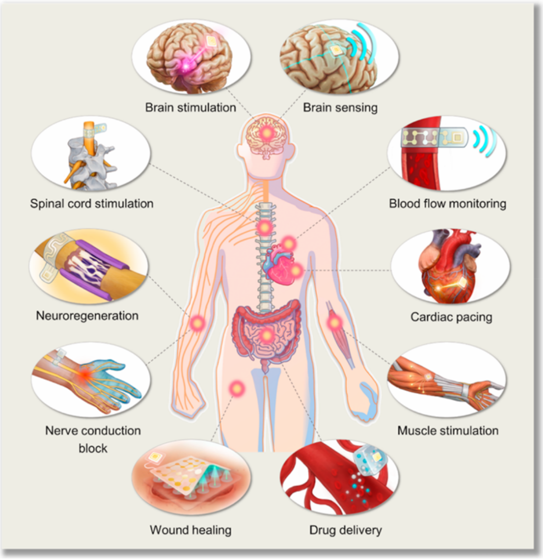


Figure 1.1: Illustration of clinical applications for implantable and bioresorbable electronics [6]

- **Environmental Monitoring and Agricultural Applications (Green IoT, Smart Farming)**
  In environmental monitoring, biodegradable devices serve as disposable sensors for soil moisture, humidity, pH, temperature, plants health assessment or pollutant detection, and eco-friendly antennas, supporting sustainable practices by avoiding the accumulation of electronic waste and long-term pollution in natural ecosystems [3] [8] [12]. By directly mitigating these environmental impacts, biodegradable electronics also advance sustainable agriculture —particularly precision agriculture (PA) — by enabling dense, low-cost, non-persistent deployments that can be safely left in the field.
  Therefore, also in this field, biodegradable devices bring substantial advancements:

  1. **Eco-Friendly Impact and Retrieval-Free Operation**
     Traditional sensors are not designed to operate within natural environments and must be physically removed, further complicating sustainable agriculture practices. On the contrary, biodegradable technologies eliminate re-

trieval needs, allowing devices to remain in the environment and degrade naturally after their operational lifetime [13]. These devices, therefore, prevent sensor buildup in the soil and reduce the need for costly infrastructure. They also minimize the carbon and ecological footprint of deploying and recovering sensing systems, by eliminating the need for end-of-life recycling or incineration [3] [2] [1]. Furthermore, they avoid pollution from toxic materials used in standard electronics, which are especially problematic in sensitive environments like soil [14].

2. **Enabling Dense, Real-Time, and Localized Monitoring**
   In the context of agriculture, current standard electronic systems face additional limitations. The cost and complexity of commercial soil or plant-monitoring devices restrict their use to low spatial densities, often no more than one sensor per field, making it difficult to obtain high-resolution data necessary for precision farming [15]. Biodegradable electronics instead, by being cheaper and disposable, enables high-density sensor networks, allowing in-situ monitoring of critical environmental variables and data-driven farming [13].

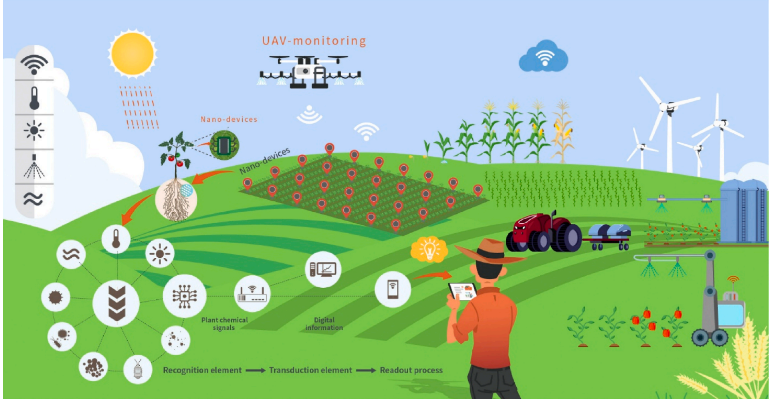


Figure 1.2: Representation of integrated application of nanotechnology and precision agriculture [16]

## 1.2 Need for Sensor Autonomy

For a biodegradable electronic system to truly meet application needs, whether in the biomedical, environmental, or agricultural field, it is essential that the sensor remains autonomous and functional for the entire time necessary to perform its diagnostic or monitoring function. However, the use of conventional batteries is often incompatible with biodegradability and miniaturization requirements, as well as representing a potential source of toxicity in implantable or environmental systems. Moreover, a battery needs to be periodically recharged, limiting system’s autonomy.

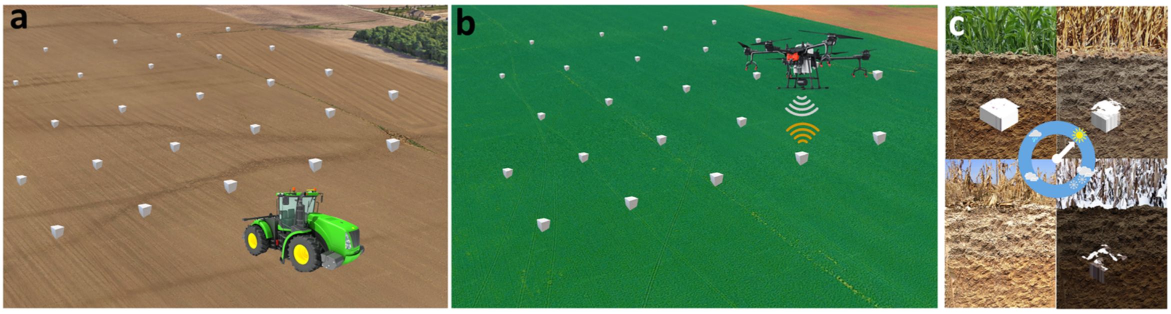


Figure 1.3: Conceptual representation of the timeline and working of the sensor tags (a) Sensor tags are distributed throughout the fields via an automated dispenser or a sower machine at the start of the crop season. (b) During the crop season, a drone equipped with an RF reader reads each of the sensor tags in the network. (c) After the crop season, the sensor tags gradually biodegrade over the following seasons.

For this reason, a promising direction is the integration of wireless power transfer (WPT) and wireless communication technologies, allowing biodegradable devices to operate completely autonomously and non-invasively throughout their active life cycle.

In precision agriculture, as highlighted by Le et al. [17], the use of a wireless system for power and data transmission enables remote monitoring of agricultural conditions (e.g., soil moisture, nutrients) with fully biodegradable devices, avoiding both the use of batteries and the need for post-use recovery. For instance, Sasaki et al. developed an entirely biodegradable wireless pH sensor based on split-ring resonators, demonstrating remote monitoring of soil acidity [18]. More recently, Zaccarin et al. introduced an inductively coupled capacitive soil moisture sensor fabricated on biodegradable substrates, showing stable operation over several weeks with wireless readout [19]. Furthermore, Gopalakrishnan et al. [20] proposed a fully biodegradable chipless resonant tag for monitoring soil volumetric water content, which can be interrogated remotely by drones as depicted in Figure 1.3.

These examples illustrate how biodegradable wireless sensors can enable dense, retrieval-free deployments in agriculture, aligning with the broader vision of precision farming. This is particularly relevant to this thesis, since the project is designed specifically for PA applications, where the designed system is intended to be deployed in the fields and interrogated via a rover.

Finally, as highlighted by several review studies [4] [21], the complete functional autonomy of biodegradable sensors is made possible by the integration of wireless components that ensure both power and data transfer, avoiding device recovery and reducing environmental or biological impact. More comprehensive reviews [22][23] further emphasize the rapid progress of biodegradable wireless systems, but also point out intrinsic limitations: reduced interrogation range due to lossy biodegradable conductors, cross-sensitivity to environmental factors (e.g., temperature, salinity), and lack of on-board calibration or multiplexing without CMOS integration. In the biomedical domain, comprehensive reviews on bioresorbable implants [24] and on wireless power/telemetry techniques [5][25] emphasized that while chipless architectures can achieve safe, temporary monitoring, the absence of active electronics restricts multiplexing, secure communication, and reliable power management. These limitations motivate the exploration of architectures where WPT is combined with active circuitry, while still maintaining biodegradability.

In summary, current wireless biodegradable sensors without CMOS integration offer proof-of-concept validation in both medical and agricultural domains, but share recurring limitations:

- **Restricted readout distance and SNR**, due to low-Q biodegradable conductors and lossy environments
- **Calibration drift and cross-sensitivity**, since chipless resonant tags cannot perform on-board compensation
- **No data processing or secure communication**

## 1.3 Need for CMOS integration: Efficiency and Functionality

To fully exploit the potential of biodegradable sensors and wireless power transfer (WPT) systems, the integration with CMOS technology is a key enabling step. This integration enhances both energy efficiency and the functional capabilities of the overall system, transforming standalone sensing modules into intelligent, compact, and autonomous systems.

From an energy perspective, CMOS integration allows the development of on-chip power management units (PMUs) and rectifiers, which are critical for maximizing wireless power transfer efficiency. For instance, Bai et al. presented a CMOS-based WPT system achieving a peak 77% system efficiency while supporting dynamic power regulation to match varying load conditions in implantable devices, reducing risk of over-heating and energy losses [26]. Similarly, Biswas et al. developed a fully CMOS-integrated WPT receiver with on-chip power regulation and rectification, achieving a power conversion efficiency (PCE) of 52% and a power transfer efficiency (PTE) of 35%, enabling safe and reliable operation in neuromodulation applications [27].

Moving from passive diode bridges to synchronous/active rectification reduces losses and avoids problematic start-up/shut-down behaviors; even simple digitally driven schemes have been shown to cut receiver losses versus Schottky bridges [28]. In parallel, receivers operating in typical sensor bands (e.g. HF/NFC 13.56 MHz, ISM 6.78 MHz) show that CMOS active/synchronous rectification and device-level threshold cancellation consistently raise rectifier and system efficiency over passive bridges. For example, an integrated receiver reached 88% system efficiency with 94% rectifier efficiency (+16% vs passive system), while a CMOS rectifier with internal threshold-cancellation achieved PCE = 86% [29] [28] [30].

Furthermore, CMOS integration facilitates advanced signal processing, analog-to-digital conversion (ADC), data storage, and wireless communication functionalities. These features allow sensors to not only acquire raw data but also their real-time signal conditioning, analysis, and transmission, essential in both biomedical and environmental scenarios. For instance, Seo et al. demonstrate a monolithic integration of a carbon nanotube (CNT) gas sensor with a CMOS chip, embedding an ADC and communication interface to realize a compact, intelligent sensing platform [31].

On the measurment side, CMOS technology enables complex features such as signal multiplexing, feedback loops, and dynamic calibration, which are essential to improve sensor precision and dealing with noise, cross-sensitivity, and environmental variability/drift, especially important in low-power biodegradable systems. The non-biodegradable literature also shows that CMOS co-integration improves readout robustness: fully-digital/PLL-based capacitive interfaces can be inherently immune to supply variation, enabling stable baselines witout an LDO [32]; sensing in the frequency/phase domain (VCO+phase detector) reduces susceptibility to amplitude noise and helps control PVT/temperature-induced drift [33]; and arrays with on-chip multiplexing/ADC improves reproducibility and enable per-channel calibration, a concrete solution against drift and cross-sensitivity at system level [31].

Even 2 x 2.2 $\text{mm}^2$ fully-integrated on-chip coils in standard CMOS have delivered milliwatts at centimeter distances within SAR limits, confirming that single-die WPT+CMOS can remain small, efficient, and viable for sensing [34].

Finally, from a system integration perspective, CMOS technology allows the realization of ultra-compact System-on-Chip (SoC) platforms. This makes the co-integration of sensor, energy management, and communication circuits feasible within a minimal footprint, vital for implantable or miniaturized environmental systems [35].

In summary, integrating CMOS chips with a sensors and WPT modules offers the following benefits:

- **Improves energy conversion efficiency** (via on-chip rectifiers and PMUs).
- **Enables real-time signal processing, data handling, and wireless transmission**.
- **Supports multifunctionality** and adaptive behavior.
- **Improves readout robustness.**
- **Reduces overall device volume and complexity**.
- **Paves the way toward fully autonomous, miniaturized, and smart biodegradable systems**

The goal of this thesis is to transfer these proven architectural benefits into a fully biodegradable platform: use WPT to ensure battery-free autonomy, and use CMOS co-integration to raise efficiency, stabilize the power supply, and embedd calibration/-multiplexing/telemetry so that readout, noise, and drift/cross-sensitivity are controlled in real-world sensing. In order to do this, a deep knowledge about biodegradable materials in essential.

**Research Question**

Which are the biodegradable materials truly compatible with electronic fabrication for building such a fully integrated WPT–CMOS–sensor system?

Transient devices, in contrast to conventional electronic systems, where the engineering focus is on long-term operational and physical stability, take into account the opposite objective by using materials that completely or partially dissolve, resorb, or otherwise disappear through chemical or physical processes at programmed rates or at triggered times after a defined period of operation.

In this section, an overview of biodegradable materials is presented, with the aim of outlining how both natural and synthetic, organic or inorganic materials can be engineered for the design and fabrication of transient electronic devices. An ideal material for a biodegradable electronic system must satisfy three key requirements [10]:

a) **Compatibility with microfabrication processes**

b) **Biocompatibility** with its surroundings (chemically and mechanically, i.e. flexibility and stretchability are important especially in medical applications)

c) **Degradation rate** tailored to the intended operational lifetime of the device.

Since any electronic system is composed of multiple functional elements (conductors, semiconductors, and dielectrics), different classes of biodegradable materials have been explored to address each role. Accordingly, this section is structured as follows: first, the discussion focuses on the main material classes, organized by electronic function; then, the fundamental mechanisms of biodegradation are introduced.

### 1.3.1 Biodegradable Insulators, Semiconductors and Conductors

Biodegradable materials can be classified for their electronic function. Both insulators, semiconductors and conductors are then divided into inorganic and organic [6] [7] [10].

- **Insulators**
  Biodegradable insulating materials, such as oxides, nitrides, and polymers, can serve multiple roles in electronic devices, including supporting substrates, passivation coatings, encapsulation structures, isolation layers between conductive traces or electrodes, and gate dielectric layers in transistors, as illustrated in Tables 1.1, 1.2, and 1.3. [7]

  - **Inorganic insulators**
    Inorganic insulators such as silicon oxide ($SiO_2$), silicon nitride ($Si_3N_4$) and magnesium oxide (MgO), due to their microfabrication compatibility, are widely adopted in biodegradable applications. These materials degrade through hydrolysis, exhibiting dissolution rates of 0.1–10 nm/day for $SiO_2$, 0.85 nm/day for $Si_3N_4$, and 6.3 $\mu$m/day for MgO at pH 7.4 and 37 °C. They are primarily employed as dielectric layers (e.g., in capacitors, transistors, and interlayers) and as encapsulants [6].
  - **Organic insulators**
    Organic (polymeric) insulators play a central role in biodegradable electronics, as they can also be adapted to device design and fabrication. As shown in Figure 1.4, biodegradable polymers are generally classified as naturally derived or synthetic. The main naturally derived materials for transient electronics include plant-based polymers (e.g., cellulose) and animal-derived materials (e.g., collagen, silk, chitosan). While they exhibit excellent biocompatibility, tunable degradation kinetics, eco-friendly production, their extraction and processing are often more complex than those of synthetic materials. Synthetic polymers (such as PLA, PVA, PCL, PGS, PMMA, POMaC) are indeed extensively used for being low-cost, easily fabricated, ideal for flexible/stretchable application, with tunable mechanical and thermal stability. These materials are valuable for encapsulation, where hydrophobicity and impermeability to biofluids are important factors; but also as

supporting material to fabricate other features on. Other crucial factors in the material selection are the transition temperature $T_g$, dissolution rate, and Young's modulus (which describes the material's stiffness). [6] [7] [10]

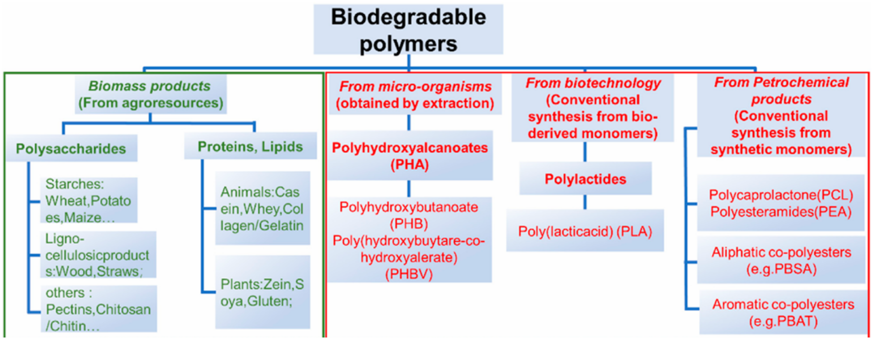


Figure 1.4: Natural and synthetic biodegradable polymers classification, and associated chemical structures.[10]

Table 1.1: Properties of biodegradable substrates [7].

| **Materials** | **Type** | **$T_g$ [°C]** | **Degradation mechanism and rate** | **Young's modulus [GPa]** |
|---|---|---|---|---|
| Cellulose | Natural | 250 | Enzymatic: ≈0.3 $\mathrm{nm\,min^{-1}}$ | 135 |
| Chitosan | Natural | 140-150 | Enzymatic: 80% weight loss in 20 days | 65 |
| Peptides | Natural | - | Enzymatic: 90% weight loss in 20 h | 20 |
| Chitin | Natural | 236 | Enzymatic: 60% weight loss in 25 h | 41 |
| Silk | Natural | 200-240 | Enzymatic: (40% weight loss in 25 days) | 23 |
| Dextran hydrogel | Natural | 172.5 | Hydrolysis: 90% weight loss in 9 days | ≈0.000015 |
| PLGA | Synthetic | 37 | Hydrolysis: ≈100% weight loss in 50 days | 0.092 |
| PVA | Synthetic | 77 | Hydrolysis: - | 0.00032 |
| PGA | Synthetic | 34-40 | Hydrolysis: 40% weight loss in 20 days | 7 |
| PHBV | Synthetic | 5 | Hydrolysis: 2.5% weight loss in 250 days | 0.2315 |
| DTE carbonate | Synthetic | 90 | Hydrolysis: 70% weight loss in 20 weeks | 1.471 |
| PEO | Synthetic | −56 | Hydrolysis: 90% weight loss in 8 weeks | 0.65 |
| POC | Synthetic | - | Hydrolysis: ≈100% weight loss in 35 days | 0.00014 |
| PPS | Synthetic | 80 | Hydrolysis: 8% weight loss in 10 days | 3.7 |

Table 1.2: Properties of biodegradable dielectrics [7].

| **Materials** | **Type** | **Degradation mechanism and rate** | **Dielectric constant** |
|---|---|---|---|
| $SiO_2$ | Inorganic | Hydrolysis: $SiO_2 + H_2O \rightarrow Si(OH)_4$;<br>0.1-10 nm day$^{-1}$ | $\approx 4$ |
| $Si_3N_4$ | Inorganic | Hydrolysis: $Si_3N_4 + 6H_2O \rightarrow 3SiO_2 + 4NH_3$;<br>0.85 nm day$^{-1}$ | $\approx 7$ |
| Cellulose | Natural polymers | Enzymatic: $\approx$ 0.3 nm min$^{-1}$ | $\approx 8.4$ |
| Shellac | Natural polyester | Hydrolysis: 1% weight loss after 2 h | $\approx 3$ |
| PBS | Synthetic polyester | Enzymatic: 70% weight loss after 72 h | $\approx 5$ |
| PGS | Synthetic elastomer | Enzymatic: 10% weight loss after 35 days | - |
| PBS / natural graphite | Composite | - | $\approx 40$<br>(0.05 graphite) |
| PBS / PANI | Composite | - | $\approx 40$<br>(0.15 PANI) |

Table 1.3: Properties of biodegradable encapsulants [7].

| **Materials** | **Type** | **$T_g$[°C]** | **Degradation mechanism and rate** | **Young's modulus [GPa]** |
|---|---|---|---|---|
| $SiO_2$ | Inorganic | - | Hydrolysis: $SiO_2 + H_2O \rightarrow Si(OH)_4$;<br>0.1-10 nm day$^{-1}$ | 74 |
| $Si_3N_4$ | Inorganic | - | Hydrolysis: $Si_3N_4 + 6H_2O \rightarrow 3SiO_2 + 4NH_3$;<br>0.85 nm day$^{-1}$ | 149 |
| Collagen | Natural polymer | - | Hydrolysis: 60% weight loss in 5 weeks | $\approx 10$ |
| PLLA | Synthetic polymer | 63 | Hydrolysis: 20% weight loss in 154 days | 3.4 |
| POMaC | Synthetic polymer | - | Hydrolysis: 80% weight loss in 10 weeks | 0.00029 |
| PCL | Synthetic polymer | $-60$ | Hydrolysis: 40% weight loss in 10 days | 24.6 |
| Polyanhydrides | Synthetic polymer | 92 | Hydrolysis: 100% weight loss in 14 days | 1.28 |
| PMMA | Synthetic polymer | $\approx 116$ | Enzymatic: 0.05 mg cm$^{-2}$ weight loss in 70 h | $\approx$3 |
| PU | Synthetic polymer | $-41$ | Enzymatic: 100% weight loss in 100 h | 0.016 |

- **Semiconductors**

  - **Inorganic semiconductors**

    Silicon (Si) is still nowadays the main character in electronic microfabrication. As recently discovered, especially under a certain thickness (approximately 10 $\mu$m) monocrystalline silicon (mono-Si) can be considered biodegradable. This represents a pivotal achievement in the progress of bioresorbable electronic technologies and the realization of a class of biodegradable devices. Indeed, this is significantly important for this thesis, as it implies that if properly thinned, a CMOS chip can be biodegradable.[6]
    Mono-Si can indeed biodegrade reacting by surrounding water ($Si + 4H_2O \rightarrow$

$Si(OH)_4 + 2H_2$) with a rate of 2-5 nm/day in pH 7.4 at 37°C. This can be tuned (generally reduced) by varying the p/n-type doping level. Finally, polycristalline Si (0.14 nm/day) and amorphous Si (0.2 nm/day) are biodegradable as well, but the rates of biodegradability is affected by crystal morphology. Table 1.4 reports the most commonly used biodegradable semiconductors, which are all inorganic. [6]

- **Organic semiconductors**
  Even if inorganic semiconductors offer better electronic properties and performances, polymeric organic semiconductors can also be employed for transient electronics because of their simple synthesis, soft/flexible mechanical qualities, and chemically controlled rate of biodegradation. Most bioresorbable semiconductors investigated so far originate from natural pigments and dyes such as $\beta$-carotene, indigo, perylenediimide, and chlorophyll, since many synthetic semiconducting polymers exhibit limited biodegradability. The performance of semiconductors is typically assessed in terms of charge carrier mobility, which quantifies the velocity of charge transport under an applied electric field. In organic systems, charge conduction relies on interactions within and between $\pi$-conjugated molecular backbones, enabling efficient charge transfer. These properties make organic semiconductors appealing candidates for transient electronic applications, including CMOS logic circuits. Nevertheless, despite significant progress, further development is still needed to achieve reliable integration of organic semiconductors into bioresorbable implantable medical devices. [7] [10]

- **Conductors**

When considering biodegradable conductors, it is important to recognize that their electrical performance remains significantly below that of conventional interconnect and contact materials used in standard microelectronics, such as copper, silver, gold, or aluminum. These metals indeed exhibit very high electrical conductivities (Cu, $\approx 5.96 \times 10^7$ $\mathrm{S\,m^{-1}}$; Ag, $\approx 6.30 \times 10^7$ $\mathrm{S\,m^{-1}}$; Au, $\approx 4.10 \times 10^7$ $\mathrm{S\,m^{-1}}$; Al, $\approx 3.77 \times 10^7$ $\mathrm{S\,m^{-1}}$), values that set the benchmark for reliable and low-loss operation in standard devices.

Despite this gap, research has identified and developed a variety of biodegradable metals and conductive materials that combine sufficient conductivity for transient electronics with the crucial advantage of being environmentally friendly and non-toxic in biomedical implants.

- **Inorganic conductors**
  Materials such as magnesium, zinc, iron, molybdenum, tungsten, or their alloys are valid candidate to replace non-degradable conductors. Indeed,

they can degrade in water/biofluids by hydrolysis. Such materials are very attractive as electrodes or interconnects, thanks to their acceptable electrical conductivity (Mg, $\approx 2.3 \times 10^7\ \mathrm{S\,m^{-1}}$; Zn, $\approx 1.7 \times 10^7\ \mathrm{S\,m^{-1}}$; Mo, $\approx 2.0 \times 10^7\ \mathrm{S\,m^{-1}}$; W, $\approx 2.0 \times 10^7\ \mathrm{S\,m^{-1}}$; Fe, $\approx 1.0 \times 10^7\ \mathrm{S\,m^{-1}}$) and compatibility to deposition processes and microfabrication. Table 1.5 summarizes the degradation rates and mechanisms of the main inorganic conductive metals, reporting also other important parameters such as melting temperature, Young's modulus and conductivity. [7] [6]

- **Organic conductors**
  Conducting polymers (CPs) represent an interesting alternative to conventional metals due to their simple processing and favorable mechanical properties. Researchers are currently exploring ways to make materials like polypyrrole (PPy) or PEDOT biodegradable. CPs are typically synthesized by doping conjugated polymers with delocalized $\pi$-electrons along the backbone. A common approach to render them more suitable for transient systems involves blending CPs with biodegradable insulating polymers [6]. However, the conductive component itself cannot be completely degraded into its monomeric units, which limits the true bioresorbability of these materials. Furthermore, their relatively low electrical conductivity, combined with the difficulty of designing polymers that simultaneously preserve conductivity and undergo controlled biodegradation, remains a significant challenge for their application in bioresorbable electronics [7].

Table 1.4: Properties of biodegradable inorganic semiconductors [6] [7]

| **Material** | **Type** | **Biodegradation Rate**<br>100 nm thickness and evaluated in PBS (pH 7.4 at 37 °C) [6] [7] | **Melting Temperature** | **Young's Modulus** | **Degradation Mechanism** [7] |
|---|---|---|---|---|---|
| Monocrystalline Si | Inorganic | 2-5 nm/day | ∼1414 °C | 130–190 GPa | Hydrolysis |
| n-doped Si ($10^{17}$-$10^{19}$ cm$^{-3}$) | Inorganic | 3.1 nm/day | ∼1414 °C | 130-190 GPa | Hydrolysis |
| n-doped Si ($10^{20}$ cm$^{-3}$) | Inorganic | 0.4 nm/day | ∼1414 °C | 130-190 GPa | Hydrolysis |
| p-doped Si ($10^{17}$–$10^{19}$ cm$^{-3}$) | Inorganic | 2.9 nm/day | ∼1414 °C | 130–190 GPa | Hydrolysis |
| p-doped Si ($10^{20}$ cm$^{-3}$) | Inorganic | 0.2 nm/day | ∼1414 °C | 130-190 GPa | Hydrolysis |
| Polycrystalline Si | Inorganic | 0.14 nm/day | ∼1414 °C | ∼130 GPa | Hydrolysis |
| Amorphous Si | Inorganic | 0.2 nm/day | ∼600–800 °C | 70-90 GPa | Hydrolysis |
| Ge | Inorganic | 0.15 nm/day | ∼938 °C | 70-110 GPa | Hydrolysis |
| Si-Ge | Inorganic | 0.1 nm/day | ∼936-1414 °C | 70-170 GPa | Hydrolysis |
| ZnO | Inorganic | 4 nm/day | ∼1975 °C | 120-160 GPa | Hydrolysis |
| $MoS_2$ | Inorganic | 1.4-2.8 nm/day | ∼1185 °C | 0.3-0.5 GPa | Hydrolysis |
| $WS_2$ | Inorganic | 0.7-1.1 nm/day | ∼1200 °C | 0.5-0.7 GPa | Hydrolysis |

Table 1.5: Properties of biodegradable conductive materials [6] [7]

| **Material** | **Type** | **Biodegradation Rate** (pH 7.4 at 37 °C) [6] [7] | **Melting Temp.** | **Young's Modulus** | **Conductivity** ($S\ m^{-1}$) at 20 °C [6] | **Degradation Mechanism** [7] |
|---|---|---|---|---|---|---|
| Magnesium [Mg] | Inorganic | 480 nm/day in HBSS | 650 °C | ~45 GPa | $2.3 \times 10^7$ | Hydrolysis |
| Zinc [Zn] | Inorganic | 300 nm/day in HBSS | 419.5 °C | ~108 GPa | $1.7 \times 10^7$ | Hydrolysis |
| Molybdenum [Mo] | Inorganic | 0.7 nm/day in HBSS | 2623 °C | ~329 GPa | $2.0 \times 10^7$ | Hydrolysis |
| Tungsten [W] | Inorganic | 20 nm/day in HBSS | 3422 °C | ~411 GPa | $2.0 \times 10^7$ | Hydrolysis |
| Iron [Fe] | Inorganic | 7 nm/day in HBSS | 1538 °C | ~200 GPa | $1.0 \times 10^7$ | Hydrolysis |
| PDPP-PD | Synthetic | 40 days in PBS | - | 1–5 GPa | $10^{-2}$–$1.0 \times 10^3$ | Hydrolysis |
| PPy/PLA | Composite | 15 days in PBS | ~150–160 °C | 0.5–2 GPa | $10^{-4}$–1 | Hydrolysis |

### 1.3.2 Mechanisms of Biodegradation

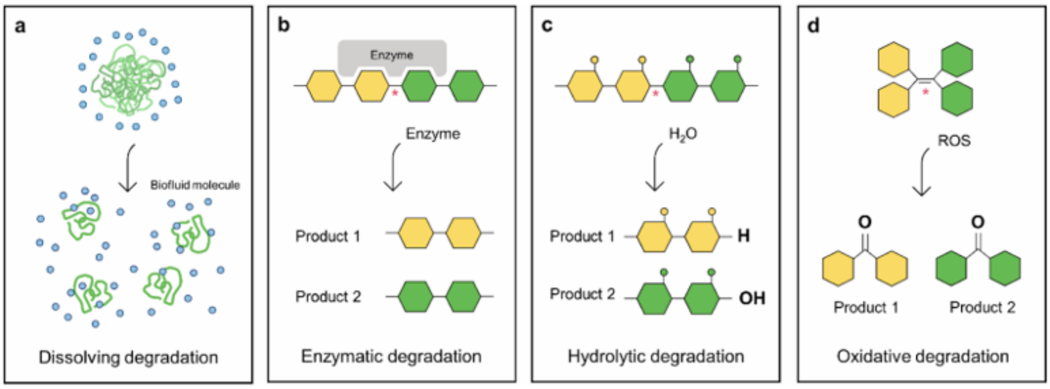


Figure 1.5: Mechanisms of biodegradation of bioresorbable polymers [6]

Biodegradable materials can physically or chemically dissolve after a predetermined period of time, without harming living organisms or the environment. Specifically considering bioresorbable polymers, there are four main mechanisms of biodegradation: dissolution, enzymatic, hydrolysis, oxidation. Most commonly, the degradation takes place as a two steps process, starting with dissolution in water, then going on with a combination of the other three mechanisms [6].

- **Dissolution**
  Water molecules or biofluids diffuse into a solid polymer. The polymer chains desorption takes place, leading to swelling and loss of mechanical integrity. This is often the first stage before other reactions take over.

- **Enzymatic biodegradation**
  Chemical bond cleavage in a polymer chain occurs as a result of a reaction with enzymes in the surrounding biofluids, after the adsorbtion of enzymes on the polymer's surface. This is particularly typical of natural polymers (e.g., silk, collagen, cellulose, chitosan).

- **Hydrolysis**
  A polymer chain's bonds are chemically cleaved as a result of an interaction with nearby water molecules. Hydrolysis is main degradation mechanisms for synthetic polymers (such as PLA, PGA, PCL, PA) but it is also the most common degradation reaction which takes place for the majority of the inorganic biodegradable materials introduced before, both insulators, semiconductors and conductors, as reported in Tables 1.1, 1.2, 1.3, 1.4 and 1.5. In Figure 1.6, the hydrolysis reactions of the main inorganic materials are reported.

$$\begin{aligned}
&\mathrm{SiO_2 + 2H_2O \;\rightarrow\; Si(OH)_4}\\
&\mathrm{Si_3N_4 + 6H_2O \;\rightarrow\; 3SiO_2 + 4NH_3}\\
&\mathrm{MgO + H_2O \;\rightarrow\; Mg(OH)_2}
\end{aligned}$$

$$\mathrm{Si + 4H_2O \;\rightarrow\; Si(OH)_4 + 2H_2}$$

$$\begin{aligned}
&\mathrm{Mg + 2H_2O \;\rightarrow\; Mg(OH)_2 + H_2}\\
&\mathrm{Zn + 2H_2O \;\rightarrow\; Zn(OH)_2 + H_2}\\
&\mathrm{2W + 2H_2O + 3O_2 \;\rightarrow\; 2H_2WO_4}\\
&\mathrm{2Mo + 2H_2O + 3O_2 \;\rightarrow\; 2H_2MoO_4}\\
&\mathrm{4Fe + 3O_2 + 6H_2O \;\rightarrow\; 4Fe(OH)_3}
\end{aligned}$$

Figure 1.6: Hydrolysis biodegradation reactions of the most common biodegradable inorganic insulators, semiconductors and conductors [6].

- **Oxidative degradation**
  Reactive oxygen or nitrogen species (ROS) released by inflammatory cells, together with free radicals, attack susceptible chemical groups (ethers, alcohols, aldehydes, amines), leading to depolymerization. This mechanism is especially relevant in vivo, as seen in polymers like poly(vinyl alcohol), which undergo swelling and oxidative chain scission leading to soluble byproducts such as acetic acid.

## 1.4 Fully-biodegradable systems integrating WPT and CMOS technology

Research Question

What are the current technological solutions for combining a sensor, wireless energy transmission, and CMOS-level functionality in a single fully-biodegradable system?

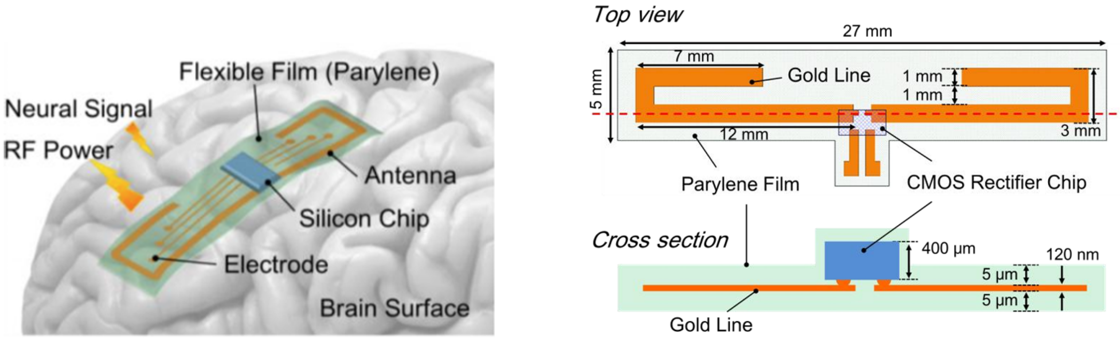
In the previous sections, it was stated the importance for a remote sensing system (especially in the medical and environmental sectors) to be:

1. **Biodegradable**
2. **Autonomous and Battery-free** (by Wireless Power Transfer)
3. **Integrated with a CMOS chip**

Current literature demonstrates partial solutions, either biodegradability without CMOS integration, or CMOS-enhanced systems without biodegradability. The challenge, and novelty of this thesis, lies in bridging these domains to investigate a fully biodegradable system that combines WPT, CMOS-level functionality, and sensing capabilities, integrated on the same biodegradable substrate.

For instance, a chipless fully degradable intelligent radio transmitting sensor (DIRTS), enabling drone-assisted wireless monitoring of soil volumetric water content through a biodegradable resonant antenna was recently developed [20]. This work proves the viability of wireless biodegradable sensors, but it does not include CMOS integration or active circuitry, thus limiting functionalities.
On the other hand, a CMOS-integrated organic neuromorphic imager with dual-modal operation was lately designed, but the device relies on stable CMOS and organic materials not intended to degrade [36]. Likewise, Lakshminarayana et al. reviewed emerging CMOS sensing SoCs, emphasizing multimodal integration, energy harvesting, and on-chip AI, but the technologies described are entirely based on conventional non-biodegradable platforms [37].

In addition, Okabe et al. [38] demonstrated the importance of co-integrating an antenna with a CMOS rectifier IC through a wafer-level packaging approach for wireless-powered neural interface systems. The fabricated rectenna, based on an ultra-thin parylene film (which is not biodegradable), successfully integrated passive and active components. The same architectural concept — flexible substrate, integrated rectifier, and wafer-level assembly — resonates with the goals of this work, which aims to adapt such strategies into a biodegradable framework. The obtained device is reported in the Figure 1.7 below.



(a) (b)

Figure 1.7: (a) Flexible wireless-powered neural interface. (b) Antenna and CMOS rectifier IC integrated on flexible parylene thin film by wafer-level packaging [38].

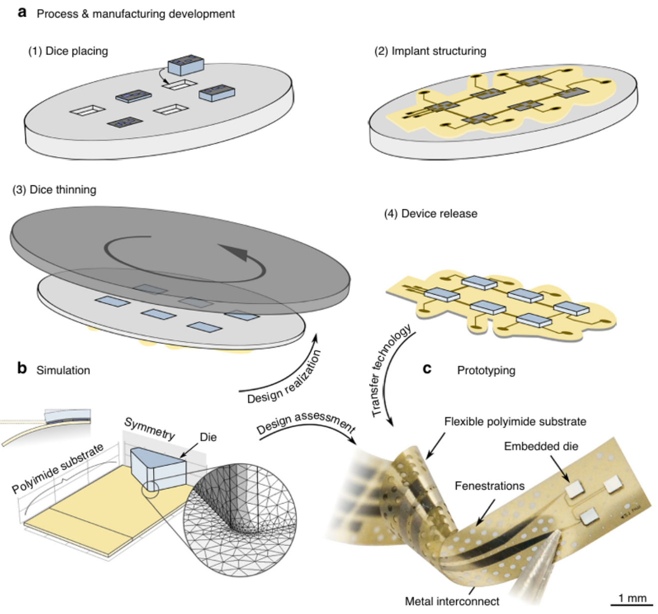


Figure 1.8: Transfer technology and design of a chip-in-foil implant. The basic idea behind the batch transfer of several silicon-based IC into flexible polyimide (PI) substrate is shown: (1) the die are placed into a carrier substrate; (2) the flexible PI substrate, metal interconnect lines, contact pads, and electrode sites are structured; (3) the die backside is thinned to the appropriate thickness; and (4) the devices are released. An image of a flexible PI-based device prototype showing three Si-based die (each measuring 390 x 390 $\mu m^2$ and 24 $\mu m$ thin) connected by metal interconnects. [39]

In this scientific landscape, a novel and very interesting approach for the integration of CMOS die into a flexible substrate was proposed by Stieglitz at al. [39], who developed a chip-on-foil neural implant as shown in Figure 1.8.

Although this system is also based on non-biodegradable materials such as polyimide, the design method followed suggests some key ideas of considerable interest for this thesis. Indeed, the system is based on transferring multiple CMOS chips onto a single flexible substrate, which are then interconnected, all according to the fabrication method shown in figure 1.9. Once interconnected, the backside of the chips is thinned and the overall design is finally released, resulting in a flexible chip-on-foil system. This suggests the possibility of interconnecting not only multiple CMOS die, but also integrating devices with different functions such as a sensor and a WPT device.

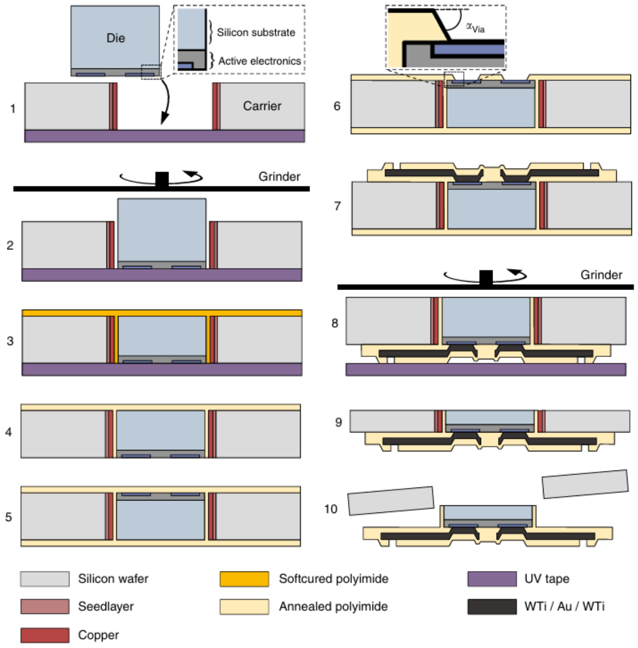


Figure 1.9: Fabrication process sequence for silicon-based die transfer into flexible polyimide (PI) based neural implants. 1) A CMOS chip is placed in the carrier. 2) The backside is levelled. 3) PI is deposited on the backside and the grinding tape is removed. 4) PI is annealed in nitrogen. 5) PI substrate is deposited on frontside. 6) PI is opned over die contact pads by reactive ion etching (RIE). 7) Metallizations are realized by sputtering, PI topside substrate is applied, and contact pads are opened. 8) Die and carriers backside are thinned. 9) Grinding tape is removed. 10) PI-based structures are released by dissolving the sacrificial layer.

### 1.4.1 Research Gap

Build on these considerations, the ultimate goal of this thesis is to develop a feasible fabrication method for a fully biodegradable system in which WPT, CMOS technology, and a sensor are co-integrated on the same substrate. Inspired by the chip-in-foil concept [39], the idea is to adapt such an integration scheme into a biodegradable framework, and, most importantly, using photolithography-based processes compatible with standard cleanroom facilities, representing a completely new approach.

However, before tackling the full integration of the system, an intermediate step has been defined. The work first focuses on the design and fabrication of the biodegradable wireless power transfer (WPT) device alone. This simplification allows concentrating on the key challenge of achieving efficient energy transfer with biodegradable materials and processes, while establishing a reliable fabrication method. Once this intermediate goal is achieved, the methodology can be extended toward the final objective: the fabrication of a fully integrated, fully biodegradable system combining WPT, CMOS, and sensing functionalities.

**Sub-research Question**

How can a photolithography-based process enable the fabrication of an efficient biodegradable wireless power transfer device as the first step toward a fully integrated WPT–CMOS–sensor biodegradable system?

# Wireless Power Transfer Theory and Design

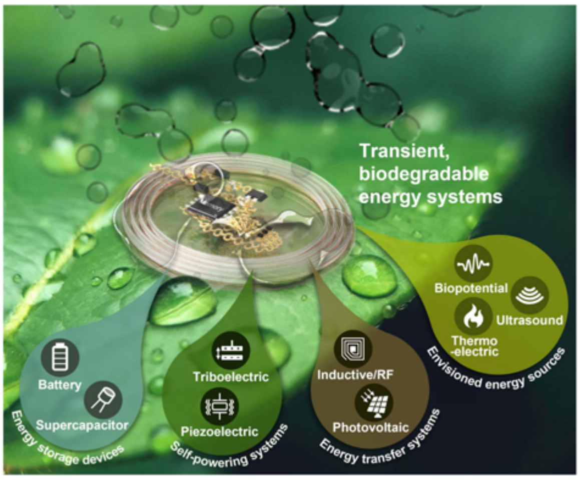


Figure 2.1: Overview of the main type of biodegradable energy devices [40].

Energy and power can be supplied to biodegradable sensors in four main ways, as shown in Figure 2.1: a) stored energy in transient batteries or supercapacitors; b) self-powered harvesters that transduce mechanical or chemical energy (triboelectric, piezoelectric, galvanic/biofuel); c) wireless power transfer (WPT) (radiofrequency/inductive coupling, near-infrared photovoltaic links, or ultrasound); and d) envisioned sources such as thermoelectrics and biopotentials. Each technique involves distinct trade-offs in output, performances, lifetime, and biodegradability. For instance, while batteries offer high energy density, they introduce safety and end-of-life concerns; supercapacitors deliver high power but suffer from self-discharge; most harvesters provide only nW–$\mu$W-level or intermittent output [40].

On the contrary, wireless power transfer (WPT) can deliver milliwatt-level power with higher power-transfer efficiency (PTE) and greater design flexibility than many energy harvesters, at the cost of high sensitivity to Tx–Rx misalignment. WPT also enables smaller, softer, and safer devices by eliminating bulky batteries that would otherwise require periodic recharging or replacement, thereby improving operational autonomy [5] [40]. For these reasons, WPT has been selected as the most suitable technique to investigate to eventually supply power to a sensor.

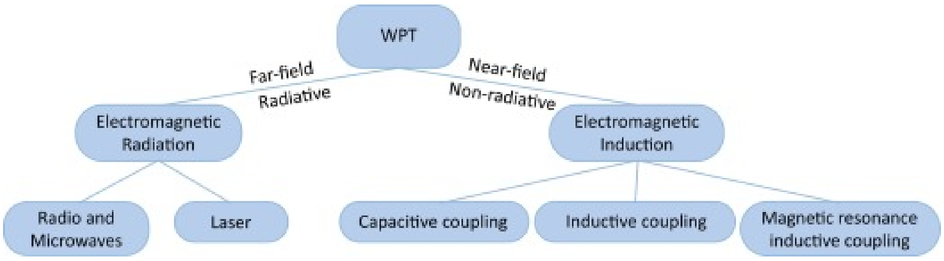


Figure 2.2: Wireless power transfer techniques [41].

Therefore, this section reviews the essential theoretical background of WPT. Among the several techniques available as reported in Figure 2.2, the focus will be on **Near-Field Communication (NFC)**, the WPT modality chosen for this project because, according to [20], it is well suited to:

- **Low-power** sensing applications (typical power delivered to the load is in the range of 1–50 mW);
- **Short distances** ($\approx$ 10 cm);
- **13.56 MHz or 6.78 MHz working frequency**, standard ISM/NFC bands widely used for sensor communications;
- **High power transfer efficiency** in strongly coupled, short-range links.

## 2.1 Near-Field Communication (NFC)

In near-field or non-radiative methods, inductive coupling between wire coils uses magnetic fields to transfer power over a short distance.

The basic principle of inductive coupling is electromagnetic induction. When an alternating current flows through a transmitting coil, electrically powered, it generates a magnetic field. The alternating voltage at the Tx side induces a magnetic flux change through the receiving coil, generating electromotive force (i.e. a voltage), according to the Faraday's law of induction, enabling wireless transferring of energy and power, as shown in Figure 2.3. [4] [42]

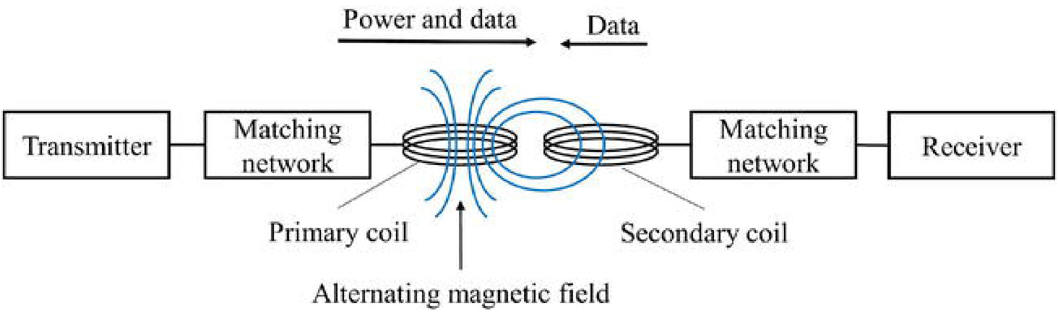


Figure 2.3: Inductive coupling between Tx and Rx coils [42].

Considering a single turn coil, the inductance is defined by Eq. 2.1:

$$L_0 = \mu_0 \, r \, \ln\left(\frac{2r}{d}\right) \tag{2.1}$$

where $\mu_0$ is the permeability of free space, $r$ is the radius of the coil and $d$ is the diameter of the metallic wire.

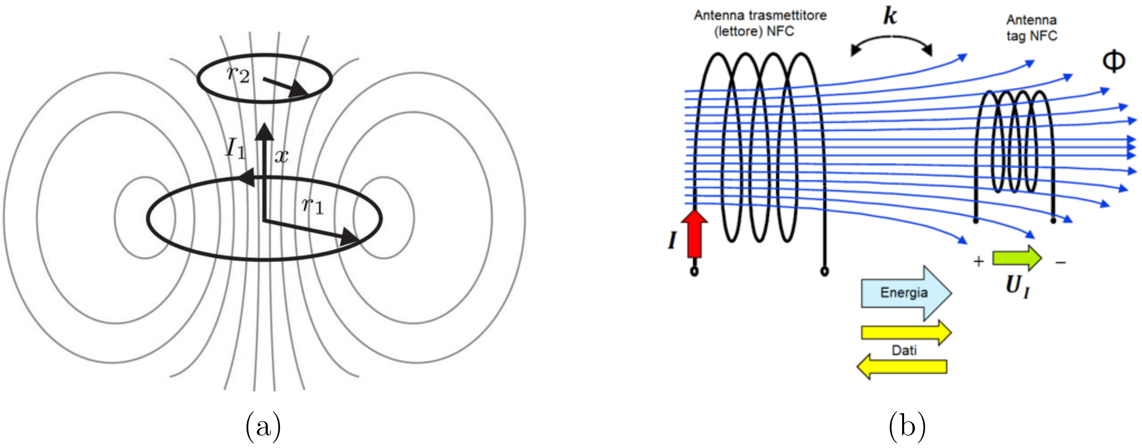
Essential figures of merit, indicative of how strong is the inductive coupling between the Tx and Rx coils, are the mutual inductance $M$ and the coupling factor $k$:

$$M = \frac{\mu \pi N_1 N_2 r_1^2 r_2^2}{2\sqrt{(r_1^2 + x^2)^3}} \tag{2.2}$$

$$k = \frac{M}{\sqrt{L_1 L_2}} \tag{2.3}$$

where $N_1$ and $N_2$ are the number of turns of the Tx and Rx coils, $r_1$ and $r_2$ the respective radius, $x$ is the axial separation and $\mu$ is the permeability, $L_1$ and $L_2$ are the Tx and Rx inductances. Mutual inductance and coupling factor are both strongly affected by the distance $x$, but also by lateral and angular misalignment between primary and secondary coil. [42]
The coupling factor $k$ ranges from 0 to 1. The entire magnetic flux produced by the transmitter coil couples with the receiver coil without any leakage when $k = 1$, indicating a perfect coupling. The coupling is null for $k = 0$. [43] Both $M$ and $k$ are directly affecting wireless power transfer efficiency [42].

Once an alternating current flows through the primary wire, it generates a time-varying magnetic field, as in Fig 2.4(a), which can couple to a secondary coil at an axial distance $x$.



(a) (b)

Figure 2.4: (a) Alternated magnetic field pattern [42]. (b) Magnetic coupling between primary and secondary coils [44].

Figure 2.4(b) highlights that, to maximize mutual coupling and the power induced in the Rx coil, the Tx and Rx coils should be closely spaced and of comparable diameter. To better intercept the Tx magnetic flux, and to retain some tolerance to lateral misalignment, the Rx coil is often made slightly smaller than the Tx coil. [42]

### 2.1.1 Wireless Power Transfer Efficiency (PTE)

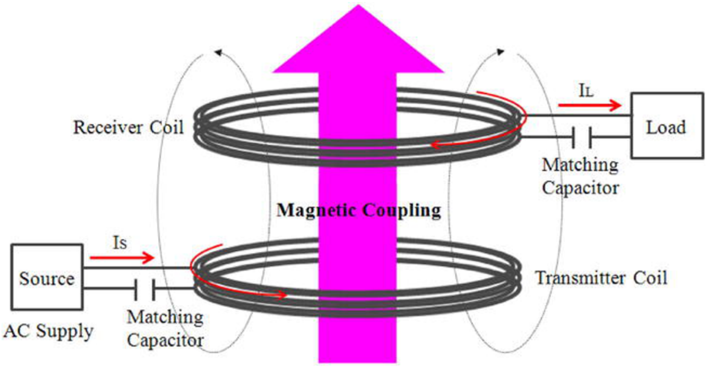


Figure 2.5: Mutual magnetic coupled coils for a WPT systems [42].

Power transfer efficiency (PTE) between two coils antennas is a crucial parameter for NFC communications, that directly depends on inductive coupling. When both the Tx and Rx antennas resonate at the same resonant frequency $f_0$, the maximum power transfer is achieved. The presence of an airgap causes weak magnetic coupling, therefore the performance of a NFC system are good only if the Tx and Rx coils are close to each other. [43]

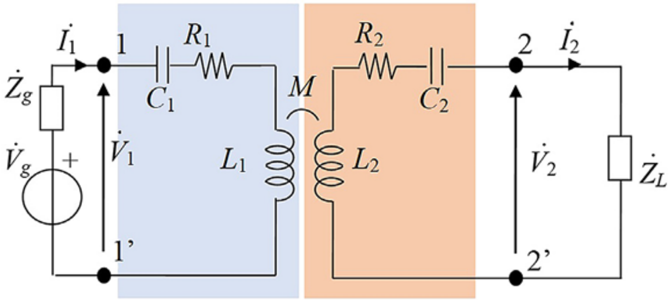


Figure 2.6: Equivalent circuit of an NFC system [43].

The equivalent circuit of an NFC systems made of two coupled coil antennas is reported in Figure 2.6, and is represented by two self-inductances $L_1$ and $L_2$, their mutual inductance $M$, two series resistances $R_1$ and $R_2$ that model power losses, and two matching series capacitors $C_1$ and $C_2$ both at the Tx and Rx. The Tx is powered by an AC voltage generator $V_g$ with an internal impedance $Z_g$. On the other hand, $Z_L$ is the load impedance. [43]

To maximize PTE, a matching capacitor is required on both Tx and Rx antennas, in order to achieve the resonance condition and tune the resonant frequency $f_0$, which is indeed a function of both the inductance $L$ and this matching capacitor $C$, as reported in Eq. 2.7. [42] [43]

Overall, the coil impedance is:

$$Z = R + j(X_L - X_C) = R + j(\omega L - \frac{1}{\omega C}) \tag{2.4}$$

The resonance condition occurs when, thanks to the matching capacitor, there is a complete compansation of the inductor reactance and minimization of the impedance in Eq. 2.4. Indeed, by minimizing the impedance $Z$ the coil current and the generated magnetic field are maximized and, consequently, the magnetic flux, therefore maximizing the power transfer. [43]

This compensation is described by the following equation.

$$X = X_L - X_C = \omega L - \frac{1}{\omega C} = 0 \tag{2.5}$$

At the resonant frequency $f_0$, the **resonance condition** is achieved.

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2.6}$$

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{2.7}$$

Consequently, the values of the matching capacitors to obtain the resonance are:

$$C_1 = \frac{1}{\omega_0^2 L_1} \tag{2.8}$$

$$C_2 = \frac{1}{\omega_0^2 L_2} \tag{2.9}$$

Considering the electrical scheme in Figure 2.6, the real input power $P_1$ and output power $P_2$ at the resonance are reported, respectively, in Eq. 2.10 and Eq. 2.11:

$$P_1(\omega_0) = (R_1 + \frac{\omega_0^2 M^2}{R_L + R_2}) \frac{(R_L + R_2)^2 V_g^2}{[(R_g + R_1)(R_L + R_2) + \omega_0^2 M^2]^2} \tag{2.10}$$

$$P_2(\omega_0) = R_L \frac{\omega_0^2 M^2 V_g^2}{[(R_g + R_1)(R_L + R_2) + \omega_0^2 M^2]^2} \tag{2.11}$$

where the assumption of $Z_g = R_g$ and $Z_L = R_L$ was made. [43]

The power transfer efficiency $\eta$ is defined as:

$$\eta(\omega_0) = \frac{P_2(\omega_0)}{P_1(\omega_0)} = \frac{1}{1 + \frac{R_2}{R_L} + \frac{R_1(R_L+R_2)^2}{R_L \omega_0^2 M^2}} \tag{2.12}$$

Considering the Eq. 2.13 of the optimum load $R_{L,\mathrm{opt}}$ that maximizes the power transfer, the maximum efficiency $\eta_{\max}$ is derived by Eq. 2.14. [43]

$$R_{L,\mathrm{opt}} = R_2 \sqrt{1 + \frac{\omega_0^2 M^2}{R_1 R_2}} \tag{2.13}$$

$$\eta_{\max} = \frac{\dfrac{\omega_0^2 M^2}{R_1 R_2}}{\left(1 + \sqrt{1 + \dfrac{\omega_0^2 M^2}{R_1 R_2}}\right)^2} \tag{2.14}$$

Finally, introducing the definition of quality factor $Q$ as:

$$Q = \frac{\text{reactive power}}{\text{active power}} = \frac{X_L I^2}{R I^2} = \frac{X_L}{R} = \frac{\omega L}{R} \tag{2.15}$$

$$Q_1 = \frac{\omega L_1}{R_1}, \qquad Q_2 = \frac{\omega L_2}{R_2} \tag{2.16}$$

Substituting Eq. 2.16 in Eq. 2.14, and considering $\mathrm{M}^2 = \mathrm{k}^2 \mathrm{L}_1 \mathrm{L}_2$ as derived by Eq. 2.2 and 2.3, the **maximum wireless power transfer efficiency $\boldsymbol{\eta_{\max}}$** is finally given by Eq. 2.17. [43]

$$\boxed{\eta_{\max} = \frac{k^2 Q_1 Q_2}{\left(1 + \sqrt{1 + k^2 Q_1 Q_2}\right)^2}} \tag{2.17}$$

and the optimum load $R_{L,\text{opt}}$ is re-arranged as follows.

$$R_{L,\text{opt}} = R_2 \sqrt{1 + k^2 Q_1 Q_2} \tag{2.18}$$

The efficiency $\eta$ is maximized by maximizing $\mathrm{k}^2 \mathrm{Q}_1 \mathrm{Q}_2$, therefore increasing the coupling factor $k$, the frequency $\omega$, and increasing the self-inductances $L_1$ and $L_2$ while reducing the losses, i.e. the resistances $R_1$ and $R_2$. [43] The resistance $R$ of a metallic wire is defined as:

$$R = \rho \frac{l}{A} \tag{2.19}$$

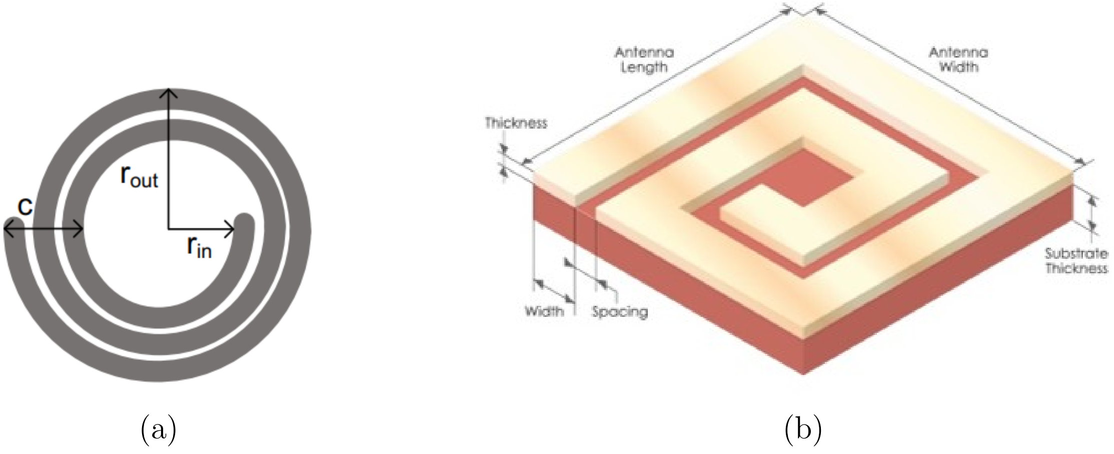
where $\rho$ is the electrical resistivity of the metallic wire, $l$ is the length of the wire/coil and $A$ is the wire section area. As a consequence, the losses reduction has to deal with material selection and geometric design.

### 2.1.2 NFC Antenna

As mentioned in [45], an NFC antenna is basically a metallic wire coil schematically represented by:

- An **inductance $L$**, which determines the resonant frequency $f_0$, as reported in Eq. 2.7;
- A **resistance $R$**, contributing to ohmic losses ($\mathrm{R} \cdot \mathrm{I}^2$). Higher $R$, higher losses;
- An **external matching capacitor $C$**, interconnected in series or in parallel to properly tune the resonant frequency;
- A **parasitic capacitance $C_{par}$**, mainly between turns.

Several expressions can be found in literature for the inductance $L$, depending on the shape. In the specific case of this thesis, where a planar thin film antenna was designed, the possible choices were a circular, spiral or squared antenna. In the end, a spiral NFC antenna was designed as in Figure 2.7 (a), since this shape is one of the most common. [46]



(a)

(b)

Figure 2.7: (a) Spiral NFC antenna [46]. (b) Geometric parameters of a NFC antenna [46].

The essential design parameters of a spiral NFC antenna according to [46] are:

- **Geometry**
  - Number of turns $\boldsymbol{N}$
  - Outer radius $\mathbf{r_{out}}$ and outer diameter $\boldsymbol{D}$
  - Inner radius $\mathbf{r_{in}}$ and inner diameter $\boldsymbol{d}$
- **Conductor**
  - Width $\boldsymbol{w}$
  - Spacing $\boldsymbol{s}$
  - Thickness $\boldsymbol{t}$
- **Substrate**
  - Substrate thickness $\mathbf{t_s}$
  - Relative permittivity $\boldsymbol{\epsilon_r}$

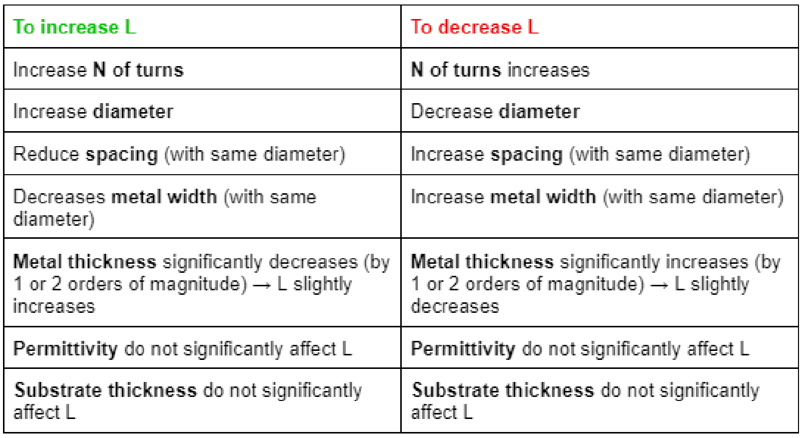
The definition of the inductance $L$ (measured in Henry H) as a function of the geometric parameters of the coil is reported in Eq. 2.20. [46]

$$\boxed{L = 31.33\,\mu_0\,N^2\,\frac{\left(\dfrac{D+d}{4}\right)^2}{8\left(\dfrac{D+d}{4}\right)+11\left(\frac{D-d}{2}\right)} = 31.33\,\mu_0\,N^2\,\frac{a^2}{8a+11c}} \tag{2.20}$$

where:

a = $(D+d)/4$ (m)
c = $\frac{D-d}{2}$ (m)
N = number of turns
$\mu_0 = 4\pi 10^{-7}$ (H/m)

The variation of each geometric parameter affects the value of the inductance $L$, as summarized in Figure 2.8.



| To increase L | To decrease L |
|---|---|
| Increase **N of turns** | **N of turns** increases |
| Increase **diameter** | Decrease **diameter** |
| Reduce **spacing** (with same diameter) | Increase **spacing** (with same diameter) |
| Decreases **metal width** (with same diameter) | Increase **metal width** (with same diameter) |
| **Metal thickness** significantly decreases (by 1 or 2 orders of magnitude) → L slightly increases | **Metal thickness** significantly increases (by 1 or 2 orders of magnitude) → L slightly decreases |
| **Permittivity** do not significantly affect L | **Permittivity** do not significantly affect L |
| **Substrate thickness** do not significantly affect L | **Substrate thickness** do not significantly affect L |

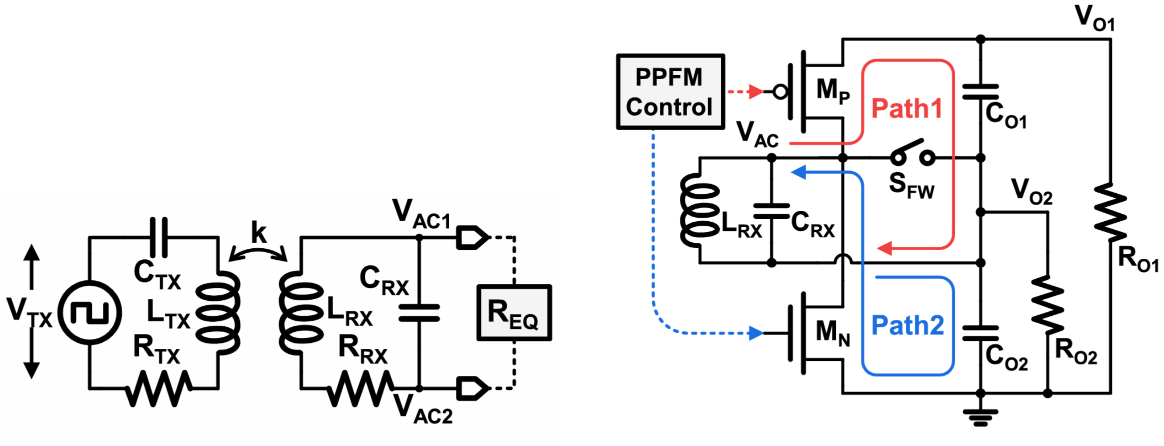
Figure 2.8: Summary of the effect of geometric parameters on the $L$ [46].

## 2.2 Design

This section outlines the design process of the wireless power transfer device, central to this thesis. First, the operation and key parameters of the CMOS rectifier underpinning the design are introduced. Next, the design flow is presented. Finally, the device is detailed, including its layout and the photolithography masks generated in KLayout.

### 2.2.1 AC-to-DC Rectification

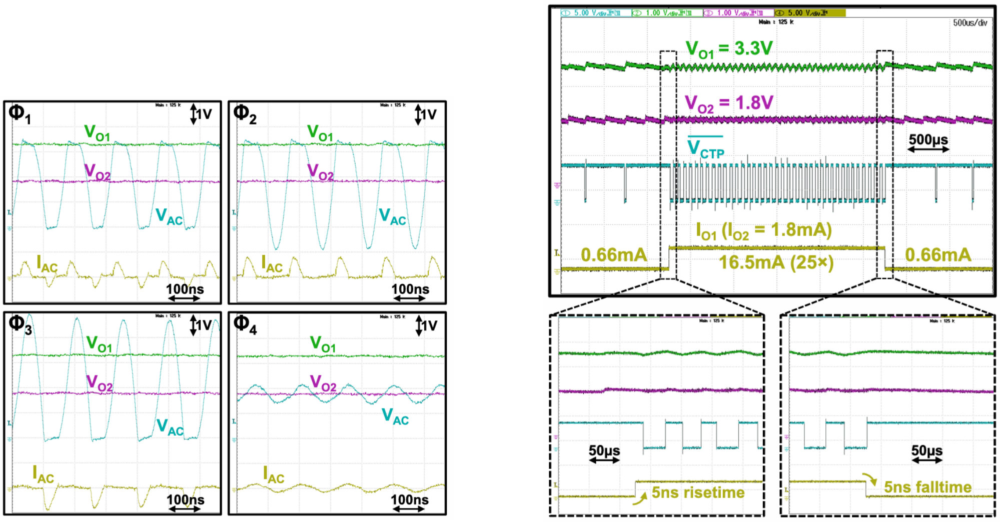
Typically, most sensors require a regulated DC supply. Consequently, the AC power harvested by a WPT receiver must be rectified and then regulated [47]. A standard power-conditioning chain comprises (a) an AC–DC rectifier - e.g. a full-bridge topology - and (b) a DC–DC converter that generates a stable output voltage. As discussed in Section 1.3, this functionality is efficiently realized in CMOS technology. In this work, the design of the WPT device is based on the CMOS rectifier integrated circuit by Lu et al. [47], developed in the Electronic Instrumentation section of the Faculty of Microelectronics, Delft University of Technology. A schematic of the IC is shown in Figure 2.9.



(a) (b)

Figure 2.9: (a) WPT system [47]. (b) Schematic the CMOS IC, a single-stage dual-output regulating voltage doubler rectifier (DOVD) [47].

Lu et al. [47] designed a single-stage dual-output regulating voltage doubler (DOVD), made of two power transistors $M_P$ and $M_N$, two output capacitors $C_{O1}$ and $C_{O2}$ and two resistances $R_{O1}$ and $R_{O2}$ mimicking the load, i.e. the sensor. Such IC is able to provide two stable DC supply voltages $V_{O1}$ and $V_{O2}$, respectively 1.8 V and 3.3 V, typical values for sensor supplies, even during a load-transient of both $R_{O1}$ and $R_{O2}$ between 5 kΩ and 200 Ω, with just a 4% ripple, as shown in Figure 2.10.



(a) (b)

Figure 2.10: (a) Four-phases operation of the DOVD to provide steady-state output voltage waveforms [47]. (b) Negligible variations of $V_{O1}$ during load-transient and $I_{O1}$ changes between 0.66 mA ($R_{O1}$=5 kΩ) and 16.5 mA ($R_{O1}$=200 Ω), while $I_{O2}$ remains fixed at 1.8 mA ($R_{O2}$=1 kΩ) [47].

Considering Figure 2.9(a), an external transmitter delivers a certain power. This AC power is then harvested by wireless power transfer by the receiver, ensuring a PTE $\eta_{\text{wpt}}$ as described by Eq. 2.17, that depends on coupling. This induces an alternating voltage $V_{AC}$ at the receiver coil, which in this case is the input voltage for the rectifier.

Therefore, by analyzing the power relationship at the Rx side [47]:

$$P_{O1} + P_{O2} = \frac{V_{O1}^2}{R_{O1}} + \frac{V_{O2}^2}{R_{O2}} = \eta_{rect} \frac{V_{AC}^2}{2R_{EQ}} \tag{2.21}$$

where $P_{O1}$ and $P_{O2}$ are the DC output powers of the CMOS rectifier, $R_{EQ}$ is the equivalent input resistance of the DOVD. Furthermore, $\boldsymbol{\eta_{rect}}$ is the **power conversion efficiency (PCE)** of the circuit, an important figure of merit defined as the ratio between the DC output power and the AC input power of the rectifier, as in Eq. 2.22. [47]

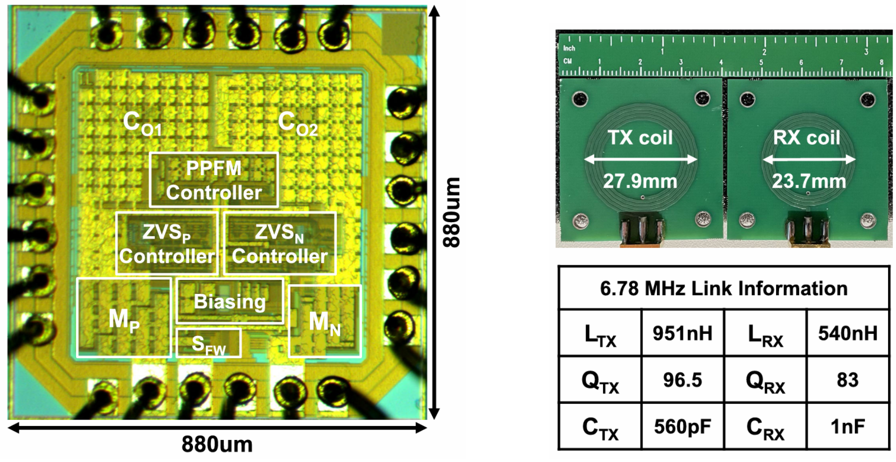
$$PCE = \eta_{rect} = <\frac{\frac{V_{O1}^2}{R_{O1}} + \frac{V_{O2}^2}{R_{O2}}}{(V_{AC} - V_{O2}) \cdot I_{AC}}> \tag{2.22}$$

where "<>" represents the average.

Besides PCE, another important figure of merit qualifying the AC-DC conversion in terms of voltage is the **voltage conversion ratio (VCR)**, which is instead defined as the ratio between the DC output voltage and the AC input voltage of the rectifier. In particular, the VCR at $V_{O1}$ can be derived as in Eq. 2.23. [47]

$$VCR = \frac{2V_{O1}}{(V_{AC} - V_{02})_{PP}} \tag{2.23}$$

Figure 2.11(a) shows the die layout. The chip footprint is 880x880 $\mu\text{m}^2$ ($\approx 0.77$ mm$^2$), with 0.34 mm$^2$ of active silicon. Figure 2.11(b) summarizes key parameters of the 6.78 MHz WPT system used in the schematic in Figure 2.9, such as Tx/Rx inductance $L$, tuning capacitance $C$ and quality factor $Q$. In [47], both coils are non biodegradable. In this project, the biodegradable Rx LC coil is designed to match these parameters, as a possible replacement of the original Rx in the future. The Rx coil is derived from the Tx design, and since they must resonate at the same operating frequency, the $LC$ product must be the same. [47]



| 6.78 MHz Link Information | | | |
|---|---|---|---|
| $L_{TX}$ | 951nH | $L_{RX}$ | 540nH |
| $Q_{TX}$ | 96.5 | $Q_{RX}$ | 83 |
| $C_{TX}$ | 560pF | $C_{RX}$ | 1nF |

(a) (b)

Figure 2.11: (a) CMOS rectifier die layout [47]. (b) 6.78 MHz WPT link parameters.

Finally, a summary of all the main parameters regarding the CMOS rectifier, including input voltage range, maximum PCE and VCR achieved for specific values of $R_{O1}$ and $R_{O2}$, and output power range is reported in Table 2.1. [47]

Table 2.1: Rectifying Chip Parameters. [47]

| **Rectifying Chip Parameters** | |
|---|---|
| **Input voltage range** $V_{\mathrm{AC}}$ | $-1.5$ V to 5.5 V |
| **Operating frequency** | 6.78 MHz |
| **Dual regulated outputs** | 1.8 V and 3.3 V (approx. 4% ripple) |
| **Voltage conversion ratio (VCR)** | 1.875 |
| **AC/DC power conversion efficiency (PCE)** | 92.95% |
| **Output power range** | 2.6−90.5 mW |
| **Maximum output power** | 90.5 mW |
| **Chip area** | 0.77 $\mathrm{mm}^2$ |
| **Silicon active area** | 0.34 $\mathrm{mm}^2$ |

### 2.2.2 Design Flow

In this subsection, the design process of a **spiral thin-film LC coil antenna** is presented. Specifically, the inductance $L$ is represented by the coil itself, while the matching capacitance $C$ is a circular parallel plate capacitance, placed outside the coil and interconnected in parallel to the inductance by planar photo-lithographic technology. The fabrication process will be thoroughly described in Chapter 3 and 4. For the moment, Figure 2.12 shows a planar squared LC circuit, just to give a reference.

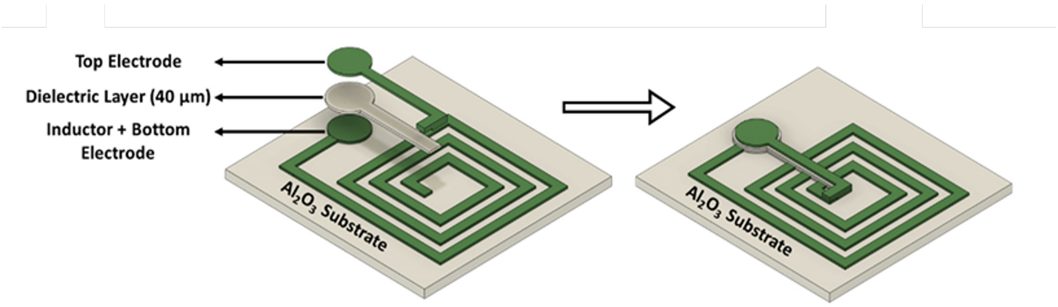


Figure 2.12: Parallel LC circuit Rx antenna [48].

Let's start the description of the design process with the overall **design flow**.

1. **Collection of parameters from Tx** and rectifier chip provider;
2. **Target definition**;
3. **Material selection**;
4. **Design LC coil geometry** using inductance formulas;
5. **Calculate Rx inductance $\mathbf{L_{RX}}$** to match Tx resonance;
6. **Calculate Rx matching capacitance $\mathbf{C_{RX}}$** to match Tx LC product;
7. **Calculate quality factor $\boldsymbol{Q}$ and PTE $\boldsymbol{\eta_{\mathrm{wpt}}}$**.

In more detail: first, the target is outlined, then component sizing and choices are discussed, and finally the physical implementation, layout, and key parameters are presented.

1. **Collection of parameters from Tx**

   The Rx coil is designed based on the Tx coil provided by Tianqi Lu (TU Delft) [47], illustrated in Figure 2.11(b), whose parameters are summarized in Table 2.2.

Table 2.2: Tx LC Coil Parameters.

| **Tx LC Coil Parameters** | |
|---|---|
| **Frequency $\boldsymbol{f_0}$** | 6.78 MHz |
| $\boldsymbol{L_{\mathrm{TX}}}$ | 951 nH |
| $\boldsymbol{Q_{\mathrm{TX}}}$ | 96.5 |
| $\boldsymbol{C_{\mathrm{TX}}}$ | 560 pF |
| $\boldsymbol{R_{\mathrm{TX}}}$ | 0.45 Ω |
| **Tx diameter** $D$ | 27.9 mm |

2. **Target definition**

   The geometry selection criterion for the Rx LC coil is to maximize the Rx quality factor $Q_{\mathrm{RX}}$ in Eq. 2.24 and the overall power transfer efficiency $\eta_{\mathrm{wpt}}$ in Eq. 2.25.

$$Q_{Rx} = \omega \frac{L_{Rx}}{R_{Rx}} \tag{2.24}$$

$$\eta_{wpt} = \frac{k^2 \cdot Q_{Tx} \cdot Q_{Rx}}{\left(1 + \sqrt{1 + k^2 \cdot Q_{Tx} \cdot Q_{Rx}}\right)^2} \tag{2.25}$$

   To calculate the PTE, the coupling factor $k$ was first estimated. The value of $k$ depends on the distance and relative dimensions of the inductors, as well as on the coils' shape and the angle between them. The coupling factor $k$ decreases with lateral (or radial) misalignment even when the coil-to-coil distance is small; conversely, for perfectly aligned coils, $k$ decreases as the axial distance increases. This behavior is illustrated in Figure 2.13, which shows the measured coupling factor for two parallel planar coils with 30 mm diameters as a function of horizontal misalignment, for different axial distances.

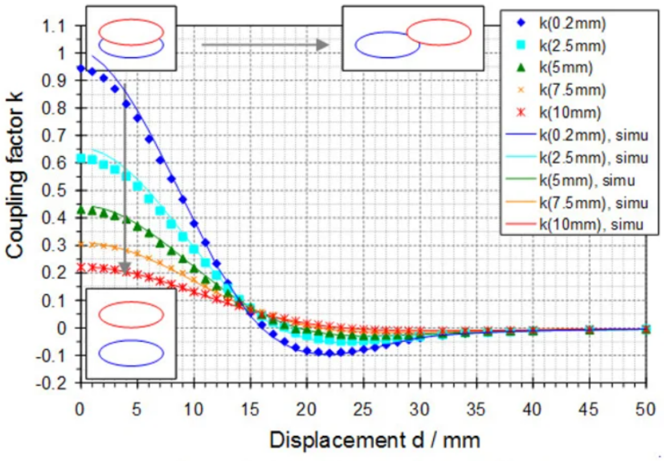


Figure 2.13: Coupling factor $k$ for two planar coils with 30 mm diameters as a function of horizontal misalignment, for different axial distances. [49]

   In this work, the device is intended for precision agriculture applications and is deployed in the soil, where an average separation of approximately 10 cm between the Tx and Rx coils is assumed. Under these conditions, and assuming perfect alignment, a coupling factor of $\boldsymbol{k = 0.2}$ is adopted, considering that $k = 1$ corresponds to very closely spaced coils. All subsequent PTE estimations are based on this coupling factor

3. **Material selection**

To ensure biodegradability, polylactic acid (PLA) was selected as both substrate and encapsulant, silicon oxide/nitride as dielectrics and insulators, and molybdenum (Mo) as the LC coil conductor. This material selection will be properly justified in Chapter 3. For the design developed here, the relevant quantities are the materials electrical properties - namely electrical resistivity $\rho$ of Mo and the relative permittivity $\epsilon_r$ of PLA, $SiO_2$ and $Si_3N_4$.
In particular, Table 2.3 summarizes the thin-film resistivity of Mo deposited at different temperatures. For this design, a value of $\rho$=120 nm Ω is adopted [50], corresponding to Mo sputtered at room temperature (RT) during fabrication. Indeed, deposition of Mo at low T is required to not affect PLA (who's glass temperature $T_g \approx 65$°C). This resistivity is about seven times higher than that of conventional conductors such as Cu (16.8 nm Ω), and negatively impacts device performance.

Table 2.3: Material Properties @ 6.78 MHz.

| **Material** | **Resistivity [nm Ω]** | **Relative Permittivity @ 6.78 MHz** | **Loss Factor tg $\delta$ @ 6.78 MHz** | **Ref.** |
|---|---|---|---|---|
| **Mo** (Bulk) | 53.4 | | | [50] |
| **Mo** (Thin Film - Sputtering @350°C) | 85 | | | [50] |
| **Mo** (Thin Film - Sputtering @RT) | $\sim$ 120 | | | [50] |
| **Cu** | 16.8 | | | [51] |
| **PLA** | | $\sim$ 3.1 | $\sim$ 0.51 | [52] |
| **$SiO_2$** (Thin Film - PECVD TEOS @300°C) | | $\sim$ 4 | | [53] |
| **$SiO_2$** (Thin Film - PECVD TEOS @RT) | | $\sim$ 8.5 | | [53] |
| **$Si_3N_4$** (Thin Film - PECVD @400°C) | | $\sim$ 7.5 | | [54] |

4. **Design LC coil geometry**

   Based on the Tx parameters in Table 2.2, the $L_{Tx}C_{Tx}$ product can be easily derived. The geometric coil design started taking into account some essential **constraints**:

   (a) The acceptable inductance $\boldsymbol{L_{Rx}}$ has an estimated range of **[520, 550] nH** to maintain enough coupling [47];

   (b) The capacitance $\boldsymbol{C_{Rx}}$ is derived by **matching $\mathbf{L_{Tx}C_{Tx}}$** product;

   (c) The **Rx coil diameter** $D \leq$ **28** cm to be **comparable to the Tx's one**, or slightly smaller;

   (d) The maximum **Mo trace** thickness was initially estimated at **500 nm**, to avoid delamination issues during the fabrication.

   In order to maximize quality factor $Q$, according to Eq. 2.24, the resistance of the LC coil $R_{Rx}$ must be minimized. Since:

   $$R_{Rx} = \rho \frac{l}{w \cdot t} \tag{2.26}$$

   where the resistivity of thin-film @RT Mo is $\rho_{Mo}$= 120 nm Ω and the estimated maximum trace thickness $t$= 500 nm, as already mentioned. To reduce $R_{Rx}$ therefore, the length $l$ of the coil should be decreased and the trace width $w$ should be increased, to enlarge the section area.

   For an $N$-turns spiral coil, of outer diameter $D$ and inner diameter $d$, the length $l$ is defined as:

   $$l = \pi N \frac{D+d}{2} \tag{2.27}$$

   where the inner diameter $d$ could also be derived as a function of the outer diameter $D$, the number of turns $N$, the trace width $w$ and the spacing $s$ between turns by the following equation.

   $$d = D - 2N(w+s) \tag{2.28}$$

   Once $D$ and $t$ are fixed as **design choices** to respect the constraints described above, the only **free variables** to play with to maximize $Q$ and PTE and, at the same time, obtaining an inductance $L_{Rx}$ in the acceptable range [520,550] nH, are basically the **number of turns $\boldsymbol{N}$**, the **trace width $\boldsymbol{w}$** and the **spacing $\boldsymbol{s}$**. Indeed, all the other important quantities like the length $l$ of the coil and the inner diameter $d$ depend on them.

Since several parameters are involved, the first step toward the final design was to express $Q$ as a function of the number of turns $N$, while treating the remaining variables ($w$, $s$, $D$, $t$) as fixed parameters. Parametric analyses were then carried out in Matlab with respect to $w$, $s$, $D$, and $t$ in order to identify the **optimal number of turns** $N_{opt}$ that maximizes $Q$ and, consequently, the power transfer efficiency (PTE).

By re-arranging Eq. 2.1 of the spiral coil inductance, the following equation can be derived.

$$L = 1.96 \cdot \mu_0 \cdot N^2 \cdot \frac{(D+d)^2}{7.5D - 3.5d} \tag{2.29}$$

Considering Eq. 2.27 and 2.28, both the inductance $L$ and the quality factor $Q$ could be re-written as a function of $l$.

$$L(l) \approx \frac{l^2}{7.5D - 3.5d} \times 10^{-6} \tag{2.30}$$

$$Q(l) \approx \frac{2\pi f_0 \times 10^{-6}}{\rho} \cdot \frac{l \cdot w \cdot t}{7.5D - 3.5d} \tag{2.31}$$

Finally, considering that the length $l$ is a function of the number of turns $N$ (Eq. 2.27), one unique expression for the quality factor $Q$ as a function of $N$ (Eq. 2.32) can be derived, using $D$, $w$, $s$ and $t$ as parameters.

$$\boxed{Q(N) = \frac{2\pi^2 f_0 \times 10^{-6}}{\rho} \cdot \frac{N[D - N(w+s)]wt}{4D + 7N(w+s)}} \tag{2.32}$$

The quality factor $Q$ vs $N$ is then analyzed by varying respectively the trace width $w$ in Figure 2.14, the spacing $s$ in Figure 2.15, the outer diameter $D$ in Figure 2.16 and the trace thickness $t$ in Figure 2.17, fixing each time the other values. In all these cases, the quality factor $Q(N)$ has always a maximum for a given set of parameters. Therefore, an **optimum number of turns** $\boldsymbol{N_{opt}}$ as a function of *D*, $w$, $s$ and $t$ to maximize $Q_{Rx}$ can be found.

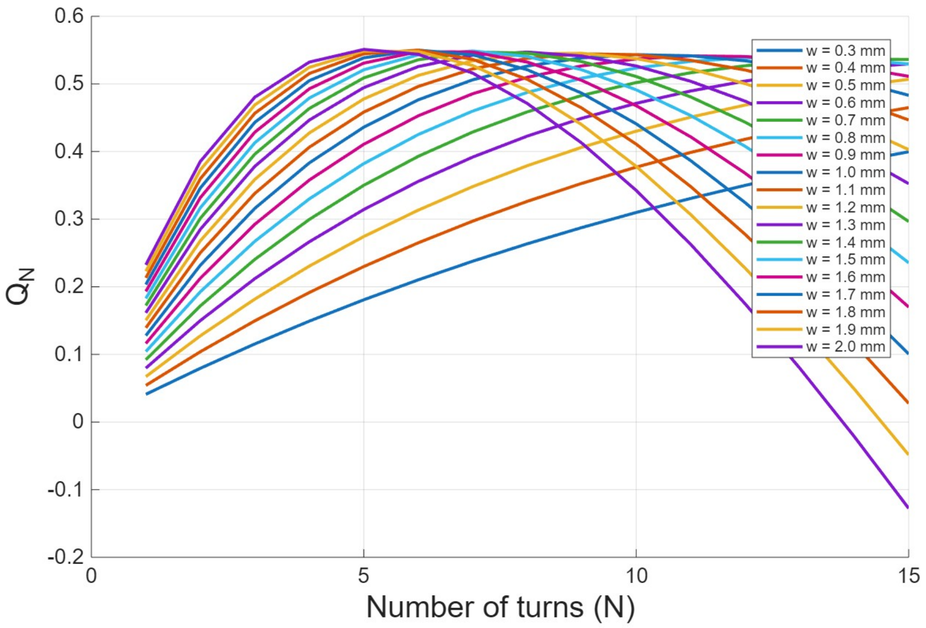


Figure 2.14: $Q_{Rx}$ vs N for different values of w (D=28 mm, t=500 nm, s=30 $\mu$m).

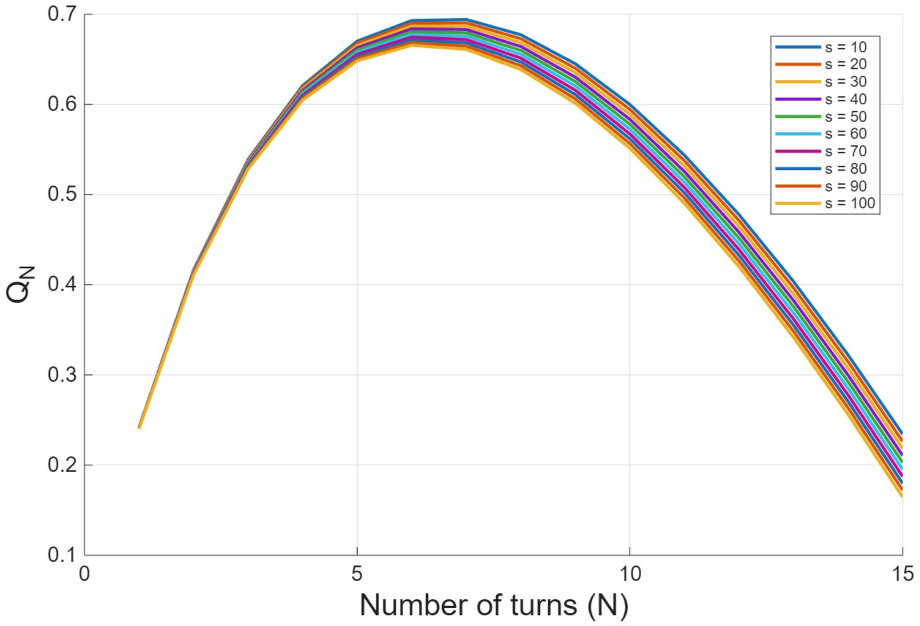


Figure 2.15: $Q_{Rx}$ vs N for different values of s (D=28 mm, t=500 nm, w=1.8 mm).

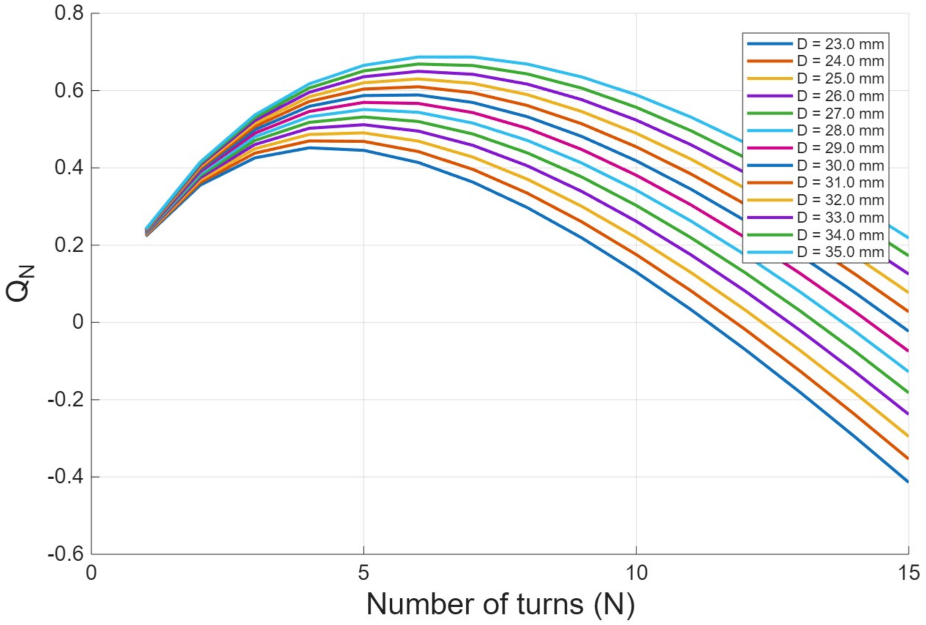


Figure 2.16: $Q_{Rx}$ vs N for different values of D (s=30 $\mu$m, t=500 nm, w=1.8 mm).

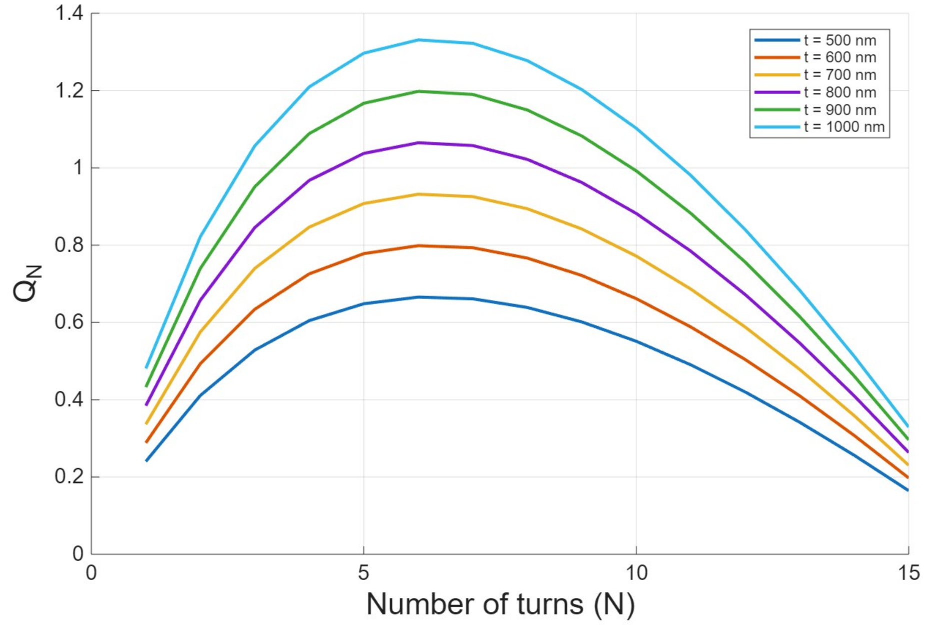


Figure 2.17: $Q_{Rx}$ vs N for different values of t (D=28 mm, s=30 $\mu$m, w=1.8 mm).

Overall, varying the trace width $w$ between 0.3 mm and 2 mm (Figure 2.14) shows that increasing $w$ allows for a reduction in the number of turns $N$ while keeping $Q$ unchanged. However, this variation does not raise the quality factor above 0.55, which remains well below the initial target ($Q_{Rx} = 2$). Similarly, varying the spacing $s$ from 10 $\mu$m to 100 $\mu$m does not lead to any improvement in $Q$ (Figure 2.15).

By contrast, Figure 2.16 indicates that increasing the diameter $D$ can enhance the quality factor. Nevertheless, as stated at the beginning of this subsection, the outer diameter must remain $\leq$ 28 mm to stay comparable to, or smaller than, the Tx coil.

The most significant improvement is obtained by increasing the metal trace thickness $t$ (Figure 2.17). Raising $t$ from 500 nm to 1 $\mu$m would substantially reduce the wire resistance and thus maximize $Q_{Rx}$. Unfortunately, this option cannot be assumed feasible without first demonstrating in the cleanroom the deposition, by sputtering, of a 1 $\mu$m Mo layer. For this reason, throughout this design, the thickness $t$ is fixed at 500 nm, which was assumed as a more reasonable value.

Finally, based on the parametric analysis in Figures 2.14, 2.15, 2.16 and 2.17 above, a trade-off has been found and an optimum number of turns $N_{opt}$=6 was selected. Furthermore, these are the other key geometric parameters: $D$=28 mm, $t$=500 nm, $w$=1.8 mm and $s$=30 $\mu$m. Consequently, an inner diameter $d$=6 mm, a trace length $l$= 321 mm and a total area $A$=6.16 cm$^2$ were derived. All these geometric values will be summarized in Table 2.5.

5. **Calculate Rx inductance $\mathbf{L_{Rx}}$**

   Considering the above mentioned geometric parameters, the Rx inductance $L_{Rx}$=543 nH is finally calculated by Eq. 2.1, respecting the initial constraint of $L_{Rx} \in$ [520, 550] nH.

6. **Calculate Rx matching capacitance $\mathbf{C_{Rx}}$**

   Given $L_{Rx}$=543 nH, and the $L_{Tx}C_{Tx}$, the value of the matching capacitor at the receiver $C_{RX}$ can be derived by respecting the condition in Eq. 2.33, which guarantee that both the transmitter and the receiver resonate at the same resonant frequency (Eq. 2.7), and that the power transfer is maximized.

$$L_{Tx}C_{Tx} = L_{Rx}C_{Tx} \tag{2.33}$$

   Consequently, $C_{Rx}$ is equal to 988 pF.

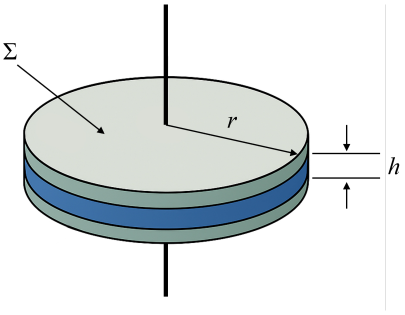


Figure 2.18: Parallel plate capacitor [55].

In this design, it was decided to realize the capacitor in planar technology as a parallel plate capacitor of circular shape, interconnected in parallel to the inductance, i.e. the coil, as done in the reference circuit developed by Lu et al. [47]. The radius $r_{cap}$ of the capacitance $C_{Rx}$ can be calculated using the definition of a parallel plate capacitance in Eq. 2.34.

$$C_{Rx} = \epsilon_0 \epsilon_r \frac{\Sigma}{h} = \epsilon_0 \epsilon_r \frac{\pi r_{cap}^2}{h} \tag{2.34}$$

$$r_{cap} = \sqrt{\frac{hC_{Rx}}{\epsilon_0 \epsilon_r \pi}} \tag{2.35}$$

where $h$ is the thickness of the dielectric in the capacitance and is here estimated as 30 nm, $\epsilon_0$=8.854×$10^{-12}$ F/m is the vacuum permittivity, and $\epsilon_r$=7.5 is the relative permittivity of $Si_3N_4$, which is the material chosen as dielectric. All the parameter related to the capacitance's design are reported in Table 2.6.

7. **Calculate quality factor $Q_{Rx}$ and PTE $\eta_{\mathrm{wpt}}$**

   After geometry definition, the $R_{Rx}$=42.8 Ω of the LC coil can be estimated by Eq. 2.26 (resulting as predicted much higher then the transmitter's resistance $R_{Tx}$=0.45 Ω), together with the quality factor $Q_{Rx}$=0.55 (Eq. 2.15) and the PTE $\eta_{wpt}$=28 % (Eq. 2.17).

### 2.2.3 Final Design: Layout and geometric Parameters

Finally, after recalling the Tx parameters in Table 2.4, a summary of the geometric parameters of the LC coil is reported in Tables 2.5 and 2.6, which present the inductor and capacitor design. Two different geometric designs are shown, one starting from an outer diameter $D$=28 mm (as the Tx one) and one from $D$=24 mm (slightly smaller). In both cases, all parameters were selected to try to maximize PTE.

Table 2.4: Tx LC Coil Parameters.

| **Tx LC Coil Parameters** | |
|---|---|
| **Frequency $\boldsymbol{f_0}$** | 6.78 MHz |
| $\boldsymbol{L}_{\mathbf{Tx}}$ | 951 nH |
| $\boldsymbol{Q}_{\mathbf{Tx}}$ | 96.5 |
| $\boldsymbol{C}_{\mathbf{Tx}}$ | 560 pF |
| $\boldsymbol{R}_{\mathbf{Tx}}$ | 0.45 Ω |
| **Tx diameter** $D$ | 27.9 mm |

Table 2.5: Rx coil geometric parameters.

| **Rx coil geometric parameters** | | |
|---|---|---|
| **Parameters** | **Design 1** | **Design 2** |
| **Outer diameter** $D$ | 28 mm | 24 mm |
| **Inner diameter** $d$ | 6 mm | 7 mm |
| **Number of turns** $N$ | 6 | 6 |
| **Trace thickness** $t$ | 500 nm | 500 nm |
| **Trace width** $w$ | 1.8 mm | 1.4 mm |
| **Spacing** $s$ | 30 $\mu$m | 50 $\mu$m |
| **Trace length** $l$ | 321 mm | 288 mm |
| **Total area** $A_{\mathrm{tot}}$ | 6.16 cm$^2$ | 4.52 cm$^2$ |

Table 2.6: Parallel plate C design.

| **Parallel plate C geometric parameters** | | |
|---|---|---|
| **Parameters** | **Design 1** | **Design 2** |
| **Capacitance** $\boldsymbol{C}$ | 988 pF | 1015 pF |
| **Vacuum Permittivity** $\varepsilon_0$ | $8.854 \times 10^{-12}$ F/m | $8.854 \times 10^{-12}$ F/m |
| **Dielectric Material** | SiN | SiN |
| **Relative Permittivity of SiN** | $\sim 7.5$ | $\sim 7.5$ |
| **Distance between plates** $h$ | 30 nm | 30 nm |
| **Capacitor Radius** $r$ | 377 $\mu$m | 382 $\mu$m |
| **Capacitor Area** $A$ | 0.446 mm$^2$ | 0.459 mm$^2$ |

Table 2.7: Rx coil electrical parameters.

| **Rx coil electrical parameters** | | |
|---|---|---|
| **Parameters** | **Design 1** | **Design 2** |
| **Operating frequency $f$** | 6.78 MHz | 6.78 MHz |
| **Inductance $L$** | 543 nH | 529 nH |
| **Capacitance $C$** | 988 pF | 1015 pF |
| **Molybdenum resistivity $\rho$** | 120 nm Ω | 120 nm Ω |
| **resistance $R$** | 42.8 Ω | 49.4 Ω |
| **Quality factor $Q_{Rx}$** | 0.55 | 0.46 |
| **PTE $\eta_{wpt}$** | **28%** | **25%** |

Table 2.7 shows the quality factor and the PTE calculated for these designs. This efficiency is limited mainly by:

1. **High resistivity of molybdenum** (120 nm Ω, approximately x7 with respect to copper), which compromises the overall resistance and quality factor;
2. **Nanometric thickness of the metal traces** ($t$=500 nm), leading to a strong increase of $R$;
3. **The operating frequency $f_0$=6.78 MHz**, which limits the quality factor $Q$ according to Eq. 2.24. Considering a 13.56 MHz transmitter, the quality factor would double, and the PTE would increase approximately by 50%, reaching 42%.

However, considering the first design with a power transfer efficiency $\eta_{wpt}$=28%, this is still a good result for the low-power target of this thesis. Specifically, the WPT device is intended to power a biodegradable sensor with an estimated demand of about 1-50 mW. Indeed, it is sufficient for the transmitter to deliver an input power of $P_{in,AC}$ = 200 mW to achieve a final DC output power available to the sensor of approximately 50 mW, considering a power transfer efficiency (PTE) of 28% and a rectifier power conversion efficiency (PCE) of 92% (as reported in Table 2.1).

$$\boldsymbol{P_{out,DC}} \approx PTE \cdot PCE \cdot P_{in,AC} = 0.28 \cdot 0.92 \cdot 200 \text{ mW} \approx \mathbf{50\ mW} \tag{2.36}$$

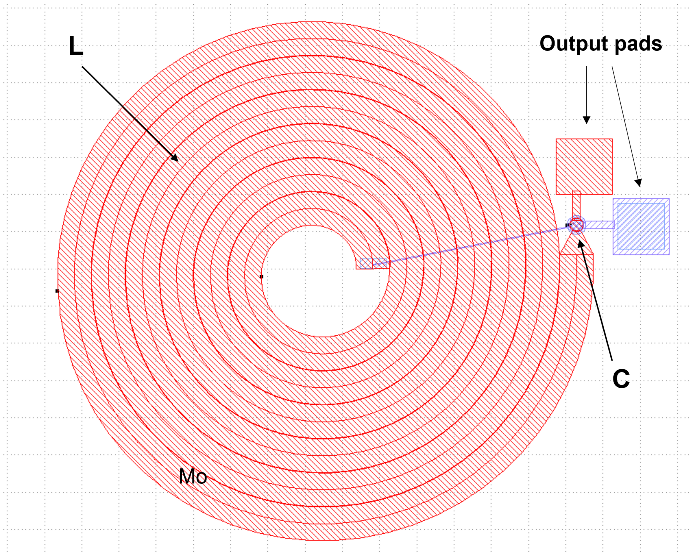


Figure 2.19: LC coil Rx antenna final layout.

Finally, the **device layout** is illustrated in an overview image (Figure 2.19) based on **design 1** (according to Table 2.5). A full description of the fabrication process is deferred to Chapter 3, where the mask set designed in KLayout for the MLA150 direct-writing photolithography tool is described. In this chapter, only the **bottom metal layer** is shown in details in Figure 2.20, in order to discuss the device's parasitic capacitance $C_{par}$, which has influenced the overall design.

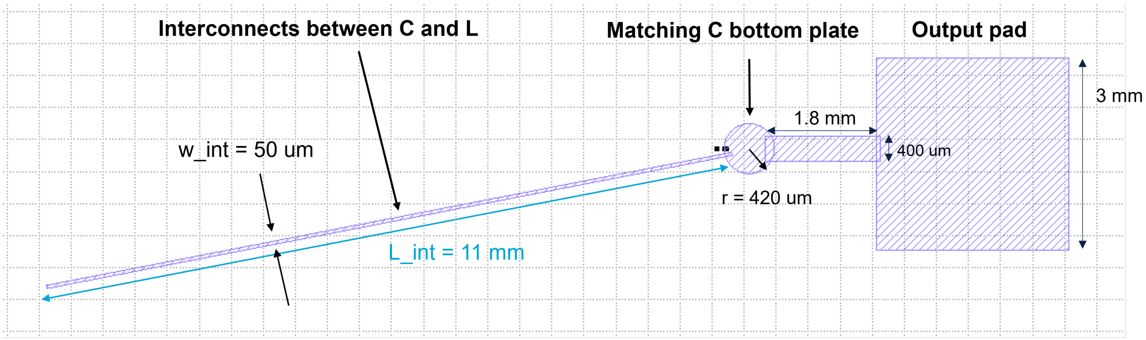


Figure 2.20: **Mask 1:** Output pad + Bottom Plate C + Interconnects.

The first Mo metal layer is depicted in Figure 2.20, and is made up of a first output pad, the bottom plate of the matching parallel plate C, and some interconnects (output pad-C and C-L).

The second metal layer (red), shown in Figure 2.19, overlaps the interconnects (purple) with width $w_{\text{int}} = 50\ \mu\text{m}$. A dielectric spacer of thickness $t_{sp}$ is inserted between them to prevent short circuits.

This metal-dielectric-metal overlap introduces a parasitic capacitance $C_{par}$. The choice of $w_{\text{int}}$ therefore reflects a trade-off between:

- **Low interconnect resistance $\boldsymbol{R}_{\text{int}}$**, which is reduced by increasing $w_{\text{int}}$;
- **Low parasitic capacitance $\boldsymbol{C_{par}}$**, which is reduced by decreasing $w_{\text{int}}$ (thereby shrinking the overlap between the first and second metal layers) and by increasing the dielectric interlayer thickness $t_{sp}$.

Assuming $w_{\text{int}}$=50 $\mu$m, $R_{\text{int}}$ and $C_{par}$ can be estimated as:

$$R_{\text{int}} = \rho \frac{L_{\text{int}}}{w_{\textbf{int}} \cdot t} = 120 \text{ nm } \Omega \cdot \frac{11 \text{ mm}}{50 \ \mu\text{m} \cdot 500 \text{ nm}} = 52.8 \ \Omega \tag{2.37}$$

$$C_{par} = \epsilon_0 \cdot \epsilon_r \frac{A}{t_{sp}} = \epsilon_0 \cdot \epsilon_r \frac{N \cdot w \cdot w_{\text{int}}}{t_{sp}} = 8.854 \times 10^{-12} \text{ F/m} \cdot 4 \cdot \frac{6 \cdot 1.8 \text{ mm} \cdot 50 \ \mu\text{m}}{700 \text{ nm}} = 27 \text{ pF} \tag{2.38}$$

These are rough estimates obtained by assuming a 700 nm $SiO_2$ dielectric interlayer with $\epsilon_r = 4$. The overlap area $A$ is computed as $N \cdot w \cdot w_{\text{int}}$, where $N$ is the number of turns, $w$ is the coil trace width, and $w_{\text{int}}$ is the interconnect width.

According to Eq. 2.38, $C_{par} = 27\,\text{pF}$, which is a non-negligible value. Since $C_{par}$ is in parallel with the nominal matching capacitor $C = 988\,\text{pF}$, it may shift the resonant frequency. However, a precise assessment of this effect will be possible only once fabrication is completed and the device is tested.

More generally, the interconnect dimensions in this mask and the ones illustrated in Chapter 3 were chosen primarily to reduce series resistance $R$: where routing permits, the metal width $w$ is maximized, while the thickness is fixed at $t = 500$ nm. At 6.78 MHz the effective wavelength (considering a PLA substrate with $\varepsilon_r \approx 3.1$) is $\lambda_{eff} \approx 25$ m according to Eq. 2.39, so these interconnects are electrically short and reflections/transmission-line effects are negligible.

$$\lambda_{eff} = \frac{\lambda_0}{\sqrt{\epsilon_{r,PLA}}} = \frac{c_0}{f_0\sqrt{\epsilon_{r,PLA}}} = \frac{3.0 \times 10^8}{6.78 \text{ MHz} \cdot \sqrt{3.1}} \approx 25 \text{ m} \tag{2.39}$$

where $c_0$ is the speed of light in vacuum, $\epsilon_{r,PLA}$= 3.1 is the relative permittivity of PLA and $f_0$ is the working frequency.

# Materials and Methods

The literature offers several fabrication routes for biodegradable devices. Transfer printing can accurately align and place components with features down to tens of nanometers, but it relies on customized stamps and specialized equipment, limiting its widespread implementation. Laser ablation provides mask-free metal patterning on polymer substrates; however, the local generated heat often drives the polymer above its glass-transition temperature, leading to softening, distortion, or crack initiation of the substrate. Inkjet printing is another maskless option, but its limitations about the minimum printable feature size and its variability in line width and film uniformity hinders repeatable, wafer-scale batch production. [21]

For these reasons, a central aim of this thesis is to develop a fabrication method that is **compatible with standard photolithography-based microfabrication** and cleanroom practice, yet remaining innovative and capable of adapting biodegradable materials to the fabrication of a wireless power transfer (WPT) device. The broader goal is to establish a process that can be extended to the complete realization of an integrated system combining WPT, a sensor, and a CMOS integrated circuit.

A microfabrication process usually consists of alternating 3 main processes: 1) thin-film deposition of uniform layers, 2) patterning of that layer via photolithography, and 3) selective removal of excess material via etching or lift-off.

Specifically, **photolithography** defines features on a wafer by transferring a pattern from a photomask into a photosensitive resist film (photoresist). After UV exposure and development, the patterned resist serves as a temporary ”stencil” that protects selected regions during etching or guides material deposition, thereby imprinting the circuit layout into the underlying layers. Basically, lithography converts the designed layout into physical patterns on the substrate.

Given a mask with some features, like the ones presented in Subsection 2.2.3, it is possible to directly transfer those features onto the substrate using a positive resist (which becomes soluble when exposed to UV light) or its complementary in case of negative resist (which photo-polymerizes and hardens under UV light). A classic UV proximity photolithography process is illustrated in Figure 3.1. The main steps are: 1) Spin coating of resist on the wafer; 2) Alignment and UV light exposure, using a lithographic mask; 3) Development of resist mask.

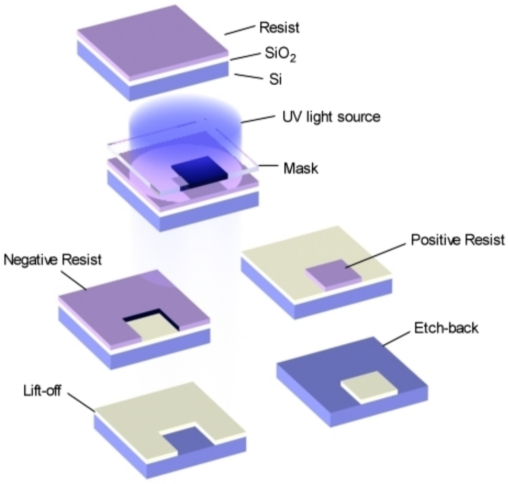


Figure 3.1: Photolithography process with positive and negative photoresist. [56]

In this work, the fabrication process was designed around the toolsets available at the Else Kooi Laboratory (EKL) and the Kavli Nanolab at Delft University of Technology (TU Delft). Accordingly, this chapter presents the selected materials and the detailed microfabrication process flow (flowchart) used to implement the device.

## 3.1 Microfabrication

In general, microfabrication refers to the suite of cleanroom processes used to build structures with feature sizes from the sub-micrometre to the hundreds-of-micrometres scale. Starting from a silicon wafer (usually 4-inch wafers at lab scale), a typical process flow comprises the following sequence of processes.

1. **Substrate preparation**
    (a) **Cleaning:** Remove organics/particles/oxides (e.g. solvent cleans, piranha).
    (b) **Dehydration and adhesion:** Dehydration bake, then apply an adhesion promoter (e.g. HMDS) before resist or polymer coatings.
    (c) **Surface activation:** Short $O_2$ plasma to raise surface energy and improve adhesion and hydrophilicity of the silicon wafer.

   (d) **Alignment infrastructure:** Define/verify alignment marks early for subsequent lithography steps.

2. **Thin-film formation (uniform layers)**
   Choose the method by material, step coverage needs, temperature (thermal budget), and compatibility with other steps.

   (a) **Physical Vapour Deposition (PVD):** thermal/e-beam evaporation and sputtering for metals (e.g., Ti, Au, Al, Cu, W, Mo) and some dielectrics. PVD gives good purity but limited step coverage.

   (b) **Chemical Vapour Deposition (CVD):** Low Pressure CVD (LPCVD), Plasma Enhanced CVD (PECVD), Inductively Coupled CVD (ICP-PECVD) for $SiO_2$, $Si_3O_4$, a-Si; highly conformal, but usually requires high temperature (150°C-750°C, exception for ICP-PECVD which can reach 75°C).

   (c) **Atomic Layer Deposition (ALD):** ultra-conformal, angstrom-level control for thin film thicknesses at relatively low temperature.

   (d) **Spin coating:** photoresists; spin-on dielectrics; polymer/biodegradable layers. Thickness is set by viscosity and spin speed; edge-bead removal improves uniformity.

   (e) **Electroplating:** metal deposition (after a PVD “seed”).

3. **Patterning (define geometries)**

   (a) **Photolithography:** spin coat resist → soft bake → exposure (contact/proximity/stepper) → post-exposure bake → development → hard bake. Choose positive (clear features where exposed) or negative (cross-link on exposure) resist by resolution and thickness needs. For thick structures, use thick resists (e.g. SU-8) and consider undercut for lift-off.

   (b) **Alternatives:** laser direct writing and electron-beam lithography (very high resolution, slower).

4. **Material transfer (turn patterns into structures)**

   (a) **Etching:**

      i. **Wet etch** (e.g. KOH/TMAH for Si, HF for SiO): high selectivity, often isotropic; use etch-stops (e.g. buried oxide in SOI).

      ii. **Dry etch** (RIE/ICP-RIE/DRIE): anisotropic profiles, finer control; DRIE (Bosch) for deep, high-aspect Si trenches. Manage selectivity, anisotropy, and mask durability.

   (b) **Lift-off:** pattern sacrificial resist, deposit film (often metals), then dissolve resist to remove unwanted areas. Lift-off is ideal for delicate substrates or when etching is risky. Ensure that the resist is thicker than the film (rule-of-thumb ≥ 3×) and promote sidewall undercut for clean edges.

5. **Doping and material modification (if required)**
   Ion implantation or diffusion followed by activation annealing for semiconductor regions. Relevant for integrated CMOS or on-chip sensors.
6. **Planarization, interconnects, and stacking**
7. **Encapsulation and packaging**

### 3.1.1 Practical notes for biodegradable materials

Conventional microfabrication is designed around standard materials (silicon, metals, and insulating dielectrics) whose thermal and chemical robustness supports aggressive process conditions. Biodegradable materials, particularly polymers, have different thermal, chemical, and mechanical responses and are generally more delicate. Introducing them into a cleanroom flow therefore requires specific precautions: lower temperature budgets, accurate solvent selection, gentler plasmas. Here are some important aspects to take into account [11] [21]:

- **Temperature budget:** many biodegradable polymers soften or degrade at modest temperatures, therefore a **low-T** flow (e.g. ≤100°C unless the chosen polymer allows more). Prefer ICP-PECVD at reduced temperature or sputtering; avoid high-T LPCVD/oxidation. the sequence of steps must be carefully designed to avoid high T processes once the biodegradable polymer is deposited.
- **Solvent compatibility:** select photoresists/developers and strippers that **do not swell or dissolve** the biodegradable layer; where possible, use lift-off to avoid aggressive etches.
- **Adhesion:** brief $O_2$ plasma or adhesion promoters compatible with the polymer.

## 3.2 Material selection

As already mentioned in Subsection 2.2.2, the biodegradable materials selected for the fabrication of the LC coil antenna are:

- **Polylactic Acid (PLA)** as both substrate and encapsulant;
- **Silicon nitride ($Si_3O_4$)** as dielectric layer of the capacitor;
- **Silicon oxide ($SiO_2$)** as insulator between metal layers;

- **Molybdenum (Mo)** as the LC coil metal traces;
- **Dextran** as sacrificial layer.

Among the biodegradable polymers introduced in Section 1.4, PLA was selected as the substrate because it is widely used in organic electronics, wearable systems, implantable platforms, and agricultural sensing, and it offers low cost, intrinsic hydrophobicity, and good moisture resistance [11, 20]. PLA is also easy to synthesize and is compatible with standard microfabrication. In particular, it can be spin-coated into uniform films [21]. In addition, its glass-transition temperature ($T_g \approx 65$–$70\,^{\circ}\mathrm{C}$) is higher than that of most polymers listed in Tables 1.3 and 1.1, providing better thermal stability and, consequently, greater compatibility with processing steps [7].

Silicon oxide ($SiO_2$) and silicon nitride ($Si_3O_4$) were chosen for their long-standing, well-established use in microfabrication. Molybdenum (Mo), among the biodegradable metals listed in Table 1.5, was chosen for its conductivity $\sigma = 2.0 \times 10^{-7}$ S m$^{-1}$ (comparable to that of W, Zn, and Mg) and its compatibility with the sputter-deposition toolsets available at the Else Kooi Laboratory (EKL) and the Kavli Nanolab at TU Delft.

Furthermore, Bathei et al. [21] recently demonstrated a photolithography-based process for patterning Mo on PLA for biodegradable sensors. This work was of particular interest and inspiration for this thesis and contributed to the final decision to fabricate the LC coil by photolithographic patterning of Mo on PLA.

Finally, dextran was selected as a sacrificial layer for its straightforward synthesis, water solubility and compatibility to microfabrication.

## 3.3 Fabrication Flowchart

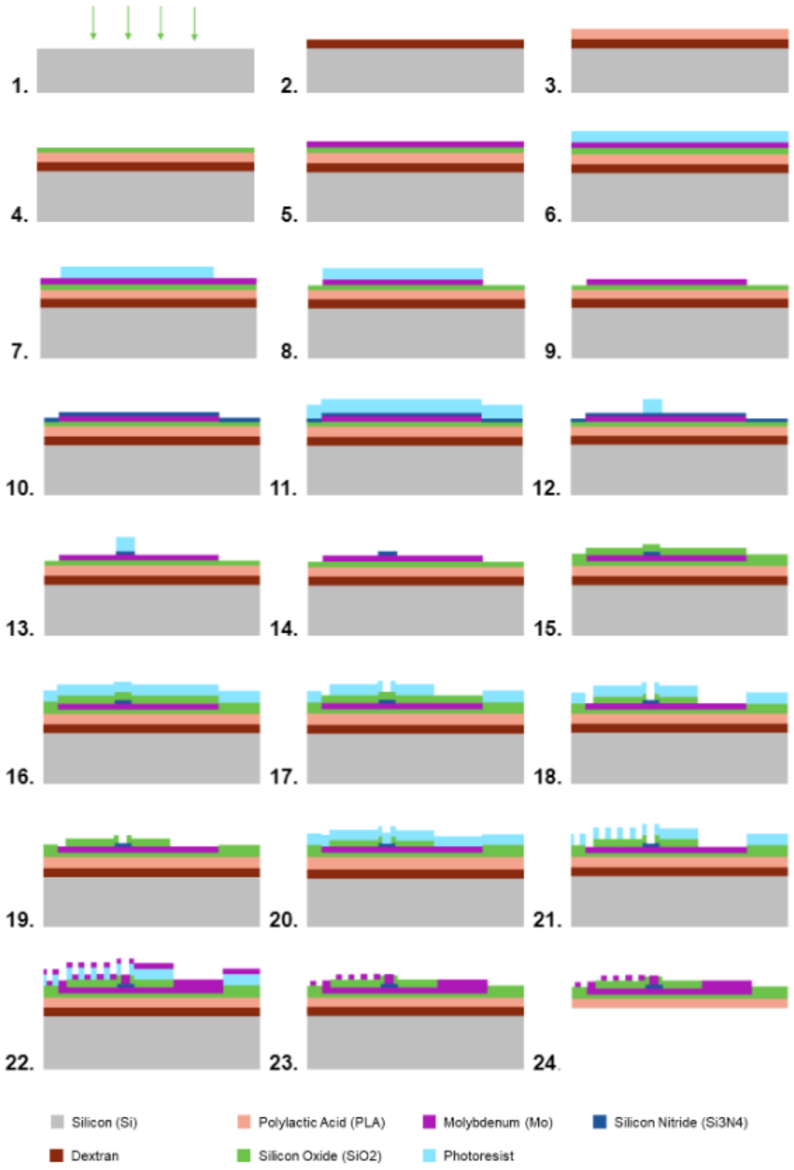


Figure 3.2: Fabrication process steps. (1) $O_2$ plasma surface treatment. (2) Spin coating of Dextran (sacrificial layer). (3) Spin coating of PLA. (4) Deposition of $SiO_2$ by ICP-PECVD. (5) Sputtering of Mo. (6) Spin coating of photoresist (PR). (7) Exposure and development of PR. (8) Reactive ion etching (RIE) of Mo. (9) Stripping of PR. (10) Deposition of $Si_3O_4$ by ICP-PECVD. (11) Spin coating of PR. (12) Exposure and development of PR. (13) RIE of $Si_3O_4$. (14) Stripping of PR. (15) Deposition of $SiO_2$ by ICP-PECVD. (16) Spin coating of PR. (17) Exposure and development of PR. (18) Wet etching of $SiO_2$. (19) Stripping of PR. (20) Spin coating of PR. (21) Exposure and development of PR. (22) Sputtering of Mo. (23) Lift-off of Mo. (24) Device release.

The complete LC coil process flow is illustrated in Figure 3.2 above. It could be summarized as follows:

1. **Substrate formation:** Starting with a silicon carrier wafer, a sacrificial Dextran layer was spin-coated, followed by a polylactic acid (PLA) layer serving as biodegradable substrate. To protect PLA and enhance adhesion between the PLA and the subsequently deposited molybdenum (Mo) metal film, a thin silicon oxide layer was deposited by ICP-PECVD. [Figure 3.2 (steps 1-4)]
2. **Etching of first Mo metal layer:** A uniform Mo layer is sputtered onto the $SiO_2$ surface and subsequently patterned by photolithography using **Mask 1** (Figure 3.13). A positive photoresist and etching process define the structures: the output pad, the bottom plate of the capacitor, and the LC interconnection. [Figure 3.2 (steps 5-9)]
3. **Silicon nitride dielectric layer for the capacitor C:** A layer of $Si_3N_4$ is deposited by ICP-PECVD and it is then patterned using **Mask 2** (Figure 3.19) to create a dielectric circle for the matching capacitor of the LC coil. [Figure 3.2 (steps 10-14)]
4. **Silicon oxide insulating layer:** $SiO_2$ is again deposited by ICP-PECVD for both insulation and reduction of the parasitic capacitance between the two Mo metal layers. $SiO_2$ is then patterned by lithography and wet etching using **Mask 3** (3.25) to: open a via for the parallel interconnect between the inductance L and the capacitance C, leave the pad opened, to create the second plate of the capacitor. [Figure 3.2 (steps 14-19)]
5. **Lift-off of second Mo metal layer:** Using **Mask 4** (3.32), a photoresist layer is spin coated and patterned performing a lift-off process of the subsequently sputtered Mo layer. In this way, the inductive spiral coil L is realized, and interconnected in parallel with the C. Finally, the device is released. Figure 3.2 (steps 20-24)]

1. **Substrate formation**

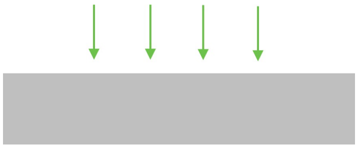


Figure 3.3: **Step 1** - $O_2$ plasma surface activation treatment.

Starting from a clean n-type 4 inches silicon carrier wafer, 525 $\mu$m thick, a short **oxygen plasma treatment** ($O_2$ gas at 50 sccm, 200 W for 2 min) is performed using Diener Atto Plasma Reactor in polymer Lab in EKL, to increase the surface energy of the silicon wafer and enhance its adhesion and hydrophilic properties.

Figure 3.4: **Step 2** - Spin coating of Dextran (sacrificial layer).

A 2 $\mu$m dextran sacrificial layer is deposited by spin-coating of a 10 wt% solution of dextran and water, at 1200 rpm for 30 s, followed by a 15 min soft baking at 165°C in an oven. The process was carried out in the BioMEMS Lab of EKL. **Spin coating** is a widely used technique for depositing thin and uniform films onto flat substrates. In this process, a liquid solution is dispensed onto the surface and spread evenly by rapid rotation as shown in Figure 3.5, with film thickness controlled by factors such as spin speed, time, and solution viscosity. By performing a soft bake, the solvent evaporates, forming a thin film.

In particular, a sacrificial layer was first deposited to enable the device release at the end of fabrication. Since dextran is water-soluble, this step can be achieved by simply immersing the device in water for 5–10 minutes.

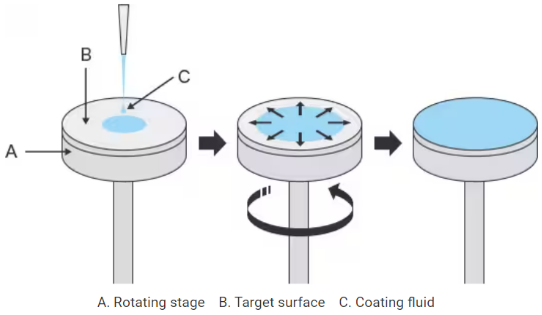


Figure 3.5: Spin coating process. [57]

Figure 3.6: **Step 3** - Spin coating of polylactic acid (PLA).

After dextran, a 1.5 $\mu$m PLA substrate is deposited by spin coating of a 4 wt% solution of PLA and chloroform, at 3000 rpm for 1 min, followed by 10 min soft baking at 70°C on a hotplate. A thickness of 1.5 $\mu$m was deemed sufficient to provide adequate mechanical support and device flexibility, while also facilitating biodegradation. The preparation of both dextran and PLA solutions and the optimization of these spin coating steps will be thoroughly described in next Chapter.

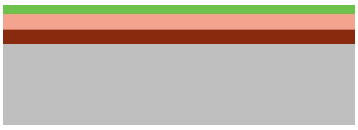


Figure 3.7: **Step 4** - Deposition of silicon oxide ($SiO_2$) by ICP-PECVD.

A 100–200 nm layer of $SiO_2$ was deposited in steps of 50 nm at 75°C, 1300 W and 8 mTorr by **inductively coupled plasma enhanced CVD (ICP-PECVD)** using Oxford Instruments PlasmaPro100 system at Kavli Nanolab, using a gas mixture of silane $SiH_4$ (16 sccm), oxygen $O_2$ (60 sccm), and argon (10 sccm). The deposition rate is 60 nm/min.

A silicon oxide layer was necessary to promote adhesion between PLA and Mo and, crucially, to protect the PLA during subsequent Mo sputtering and etching. For these reasons, a high quality silicon oxide is required. At the same time, the PLA must be kept below its glass-transition temperature ($T_g \approx 65°C$). Low quality room-temperature (RT) PVD depositions, like sputtering, cannot be adopted. Therefore, the oxide was deposited by ICP-PECVD), which yields dense, high-quality dielectrics at relatively low temperatures ($\leq 150°C$, compared to "standard" CVD temperatures like 300-750°C). In this work, deposition was performed at 75°C.

In ICP-PECVD (Figure 3.8), an RF inductive coil generates a high-density plasma that efficiently dissociates precursors, providing abundant reactive radicals for low-temperature film growth. The formation of $SiO_2$ by ICP-PECVD typically proceeds through plasma-enhanced reactions between silane ($SiH_4$) and an oxidizing gas. The overall reaction is often written as:

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2 \tag{3.1}$$

In the plasma, the reactant gases are dissociated into radicals which recombine at the substrate surface to form a dense $SiO_2$ film, while byproducts such as $H_2$ are pumped away. Usually, Plasma density is set by the coil power, while ion energy is independently controlled by a separate RF substrate bias—enabling high reactivity with minimal ion damage and heating. This enables the formation of films with low porosity and hydrogen content, high conformality and step coverage, good stoichiometry, smooth morphology, and strong adhesion.

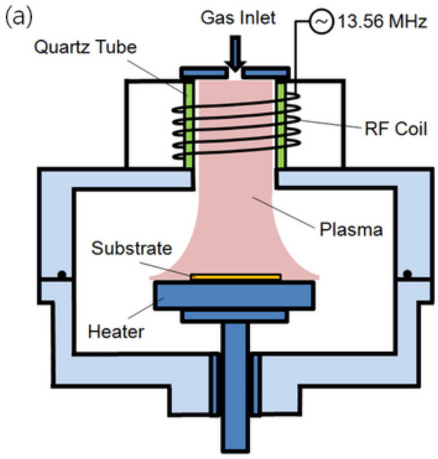


Figure 3.8: ICPCVD deposition chamber [58].

2. **Etching of Mo first metal layer**

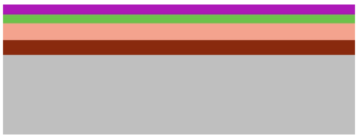


Figure 3.9: **Step 5** - Sputtering of molybdenum (Mo).

A uniform molybdenum (Mo) layer was deposited by **sputtering** at room temperature by Alliance Concept (AC) Metal 1 in Kavli Nanolab, using 100 W power, 3.4 $\mu$bar pressure, and a deposition rate of 0.6 nm/s.

Sputtering technique relies on ion bombardment of a target (here, a Mo disk) using an $Ar^+$ plasma sustained under an applied DC or AC voltage. The target is mounted on the cathode, while the wafer substrate sits on the anode (Figure 3.10). Argon gas introduced into the chamber is ionized; the resulting positive ions accelerate toward the target, ejecting Mo atoms that travel and condense on the wafer surface to form a thin, uniform film.

Because energetic ion bombardment can damage the underlying substrate, a protective silicon oxide layer was first deposited to shield the PLA. Sputtering has the advantage of being able to be performed at room temperature, ensuring that the PLA remains unaffected. However, because of the ion bombardment, the wafer surface can heat up considerably. Compared to other PVD methods, sputtering generally provides better step coverage, though its directionality leads to shadowing effects and much lower conformality than CVD techniques.

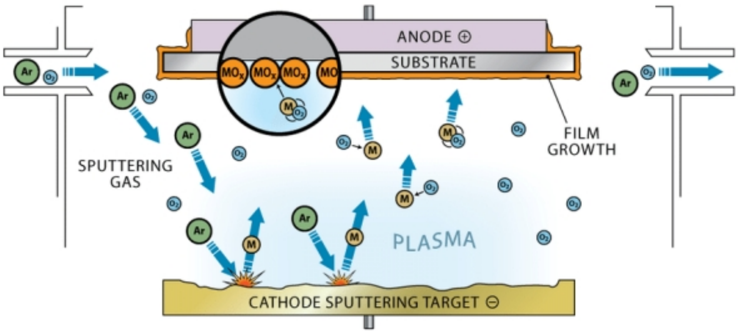


Figure 3.10: Sputtering deposition chamber.

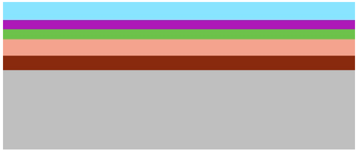


Figure 3.11: **Step 6** - Spin coating of photoresist (PR).

The first photolithography process starts with spin coating of a 1.5 $\mu$m AZ ECI 3012 positive resist onto Mo film, at 2500 rpm for 1 min + 90 s soft baking at 90°C holding the wafer at 1 cm above a hotplate (proximity mode) to let the solvent evaporate.

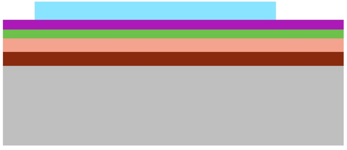


Figure 3.12: **Step 7** - Exposure and development of PR.

A 1.5 $\mu$m photoresist layer is then exposed (exposure dose = 200 mJ/cm$^2$, defoc = 0) using **mask 1** (reported again in Figure 3.13 below) by **laser direct writing**, using Heidelberg Instruments MLA150 maskless laser writer in the Kavli Nanolab. While standard UV lithography, as introduced before, relies on projecting light through a mask to define features in parallel across the whole wafer, direct laser writing is based on focusing a laser beam to locally expose and modify a photosensitive resist, so that patterns are written directly on the substrate without the need for a physical mask. As a result, the process is slower than standard lithography but offers much greater design flexibility, which is the reason it was chosen for this work.

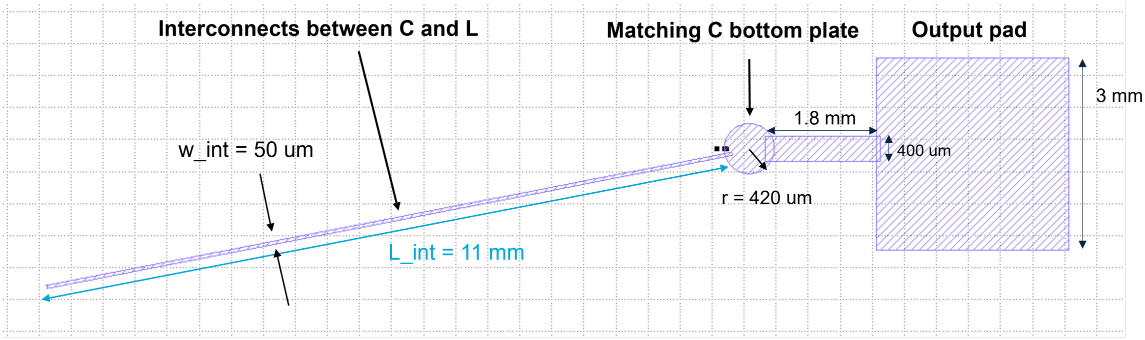


Figure 3.13: **Mask 1:** Output pad + Bottom Plate C + Interconnects.

After the exposure, a 90 s post-exposure baking is performed at 110°C in proximity mode, and the PR mask is finally developed by dipping the wafer into AZ 726 MIF for 1 min + 30 s rinsing by water gun.

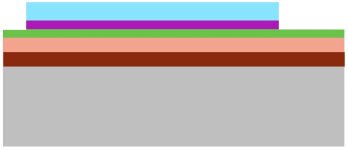


Figure 3.14: **Step 8** - Reactive Ion Etching (RIE) of Mo.

Once the PR mask is formed (light blue in step 7), it serves as a stencil for patterning the Mo layer by **reactive ion etching (RIE)**. In this dry etching process, reactive gases are introduced (in this case $SF_6$ for Mo removal) and a plasma is generated under high voltage. Energetic ions are accelerated toward the substrate, where Mo is selectively removed through a combination of physical ion bombardment and chemical surface reactions. RIE is highly directional and anisotropic, with good selectivity, allowing accurate transfer of the photoresist pattern into the underlying Mo. The etching chamber is similar in design to the sputtering system, but instead of depositing material, reactive species are introduced to precisely remove it and define the desired structures. Since the RIE process can also etch the photoresist mask, it must be sufficiently thick to ensure proper protection of the underlying Mo layer. In this work, a resist thickness of 1.5 $\mu$m was selected.

The 500 nm Mo film is etched in steps of 1-2 min by RIE of $SF_6$ at 650 sccm, at 2000 W power, and a pressure of $1.0 \times 10^{-1}$ mbar, using the ALCATEL AMS110 ICP-RIE tool in EKL.

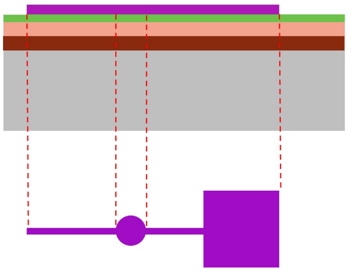


Figure 3.15: **Step 9** - Stripping of PR.

Photoresist is finally removed by dipping the wafer in methanol for at least 30 min. Usually, stripping of PR is performed in acetone, but it would dissolve PLA too. For this reason, methanol was selected as an alternative. Therefore, the first pattern of Mo layer on PLA is shown in Figure 3.15.

3. **Silicon nitride dielectric layer for the capacitor C**

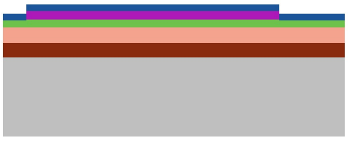


Figure 3.16: **Step 10** - Deposition of silicon nitride ($Si_3O_4$) by ICP-PECVD.

A uniform layer 30 nm layer of silicon nitride is deposited by ICP-PECVD using the Oxford Instruments PlasmaPro100 at the Kavli Nanolab, to create the dielectric layer of the parallel plate matching capacitor. Silicon nitride was selected here because of its high resistance to subsequent silicon oxide wet etching by BHF. The deposition is performed at 75 °C with a gas mixture of silane $SiH_4$ (26 sccm) and nitrogen $N_2$ (25 sccm), at 500 W and 2 mTorr (deposition rate of 44.6 nm/min).

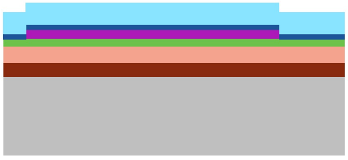


Figure 3.17: **Step 11** - Spin coating of PR.

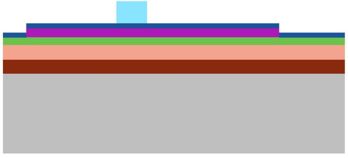


Figure 3.18: **Step 12** - Exposure and development of PR.

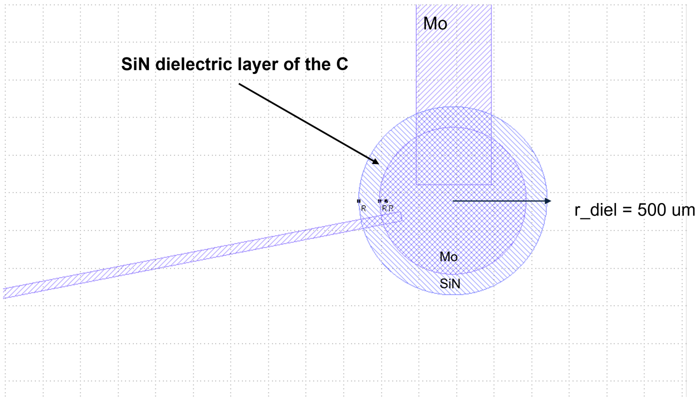


Figure 3.19: **Mask 2:** $Si_3O_4$ layer.

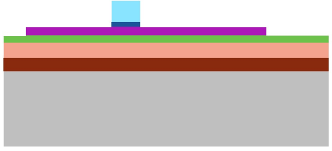


Figure 3.20: **Step 13** - RIE of $Si_3O_4$.

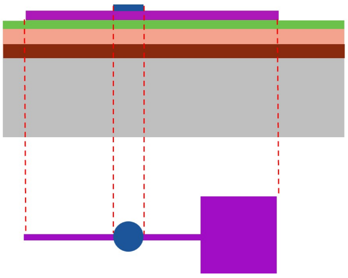


Figure 3.21: **Step 14** - Stripping of PR.

To leave only a $Si_3N_4$ circle as in Figure 3.21, the $Si_3N_4$ film is then patterned by a second lithography process, identical to the first one, using **mask 2** (Figure 3.19) and RIE of $Si_3N_4$ for 8 s using $C_4F_8$ (17 sccm), $CH_4$ (18 sccm), and He (150 sccm) at 2800 W. A 30-45 min stripping in methanol is then carried out. **Mask 2** shows the shape of the SiN dielectric layer of the matching $C_{RX}$. This is larger than both the bottom and top metal plates to avoid misalignment during photolithography and eventual short circuits between metal layers.

4. **Silicon oxide insulating layer**

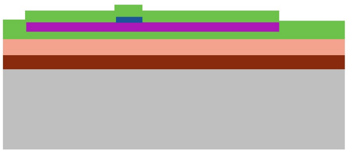


Figure 3.22: **Step 15** - Deposition of $SiO_2$ by ICP-PECVD.

A 500–700 nm layer of $SiO_2$ is deposited by ICP-CVD (75°C, 1300 W, 8 mTorr $SiH_4$ at 11.3 sccm, $O_2$ at 15 sccm, Ar at 13.8 sccm) to provide insulation between metal layers and, most importantly, to reduce parasitic capacitance $C_{par}$ arising from the overlap between the bottom Mo layer and the turns of the inductive coil, as previously discussed. In this case, $SiO_2$ was selected rather then $Si_3N_4$ because of its lower relative permittivity, mitigating therefore the parasitic capacitance.

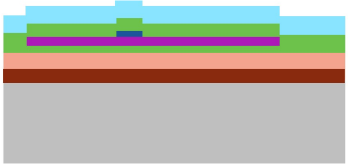


Figure 3.23: **Step 16** - Spin coating of PR.

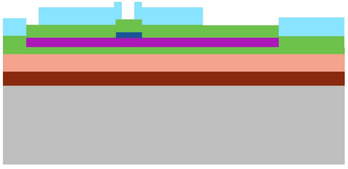


Figure 3.24: **Step 17** - Exposure and development of PR.

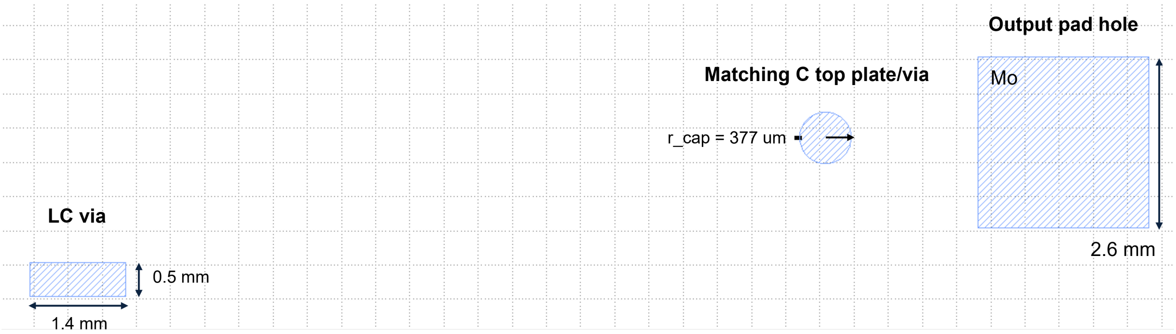


Figure 3.25: **Mask 3:** LC via + Matching C top plate via.

A third equal lithography is performed using **mask 3** (Figure 3.25), in order to create the pattern for the output pads, the LC interconnection vias, and the top plate of the matching capacitor.

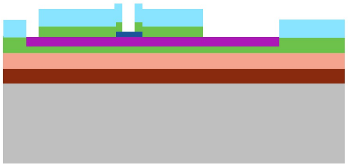


Figure 3.26: **Step 18** - Wet etching of $SiO_2$.

After the PR mask is defined, the $SiO_2$ layer is selectively removed by **wet etching**. Unlike RIE, this process is performed by immersing the wafer in a chemical solution—in this case, buffered hydrofluoric acid (BHF). Wet etching is highly selective toward $SiO_2$ but completely isotropic, proceeding uniformly in all directions. Consequently, undercutting of about 1 $\mu$m usually occurs laterally beneath the resist mask, resulting in slightly enlarged openings. In this work, however, since the feature dimensions are on the order of millimeters or hundreds of micrometers, such undercutting does not pose a significant issue.

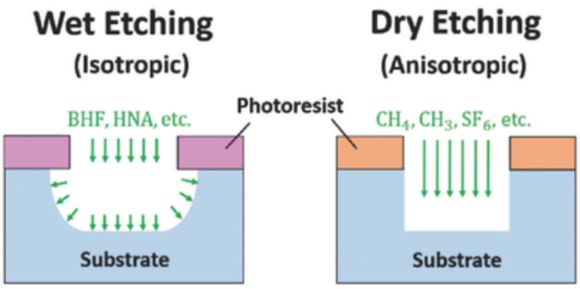


Figure 3.27: Wet etching VS Dry etching [59].

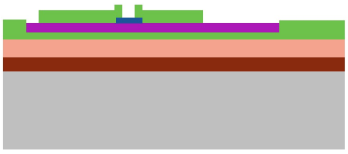


Figure 3.28: **Step 19** - Stripping of PR.

Finally, PR is again stripped by methanol.

5. **Lift-off of Mo second metal layer**

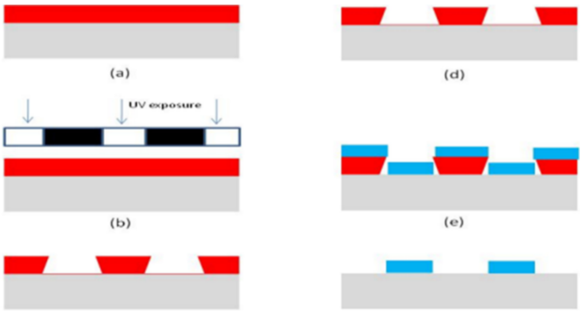


Figure 3.29: Lift-off process. (a) spin coating. (b) UV exposure. (c) Development. (d) descum. (e) PVD. (f) Lift-off by removal of PR. [60]

The second Mo layer was defined by **lift-off** (Figure 3.29). In this approach, the photoresist is patterned with openings where Mo is intended to remain - the inverse of an etch process. A retrograde/undercut resist profile (using a thick negative resist) ensures that, after PVD deposition (e.g. sputtering), the metal on top of the resist is discontinuous from the metal in the openings. The wafer is then immersed in a solvent; the resist dissolves and the unwanted metal lifts off, leaving the Mo features. For clean results, the resist should be several times thicker than the metal and the deposition kept relatively directional to minimize sidewall coating.

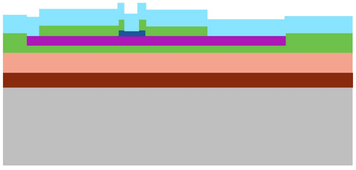


Figure 3.30: **Step 20** - Spin coating of PR.

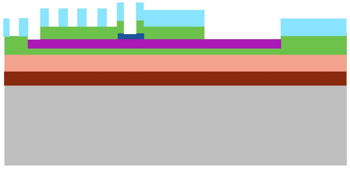


Figure 3.31: **Step 21** - Exposure and development of PR.

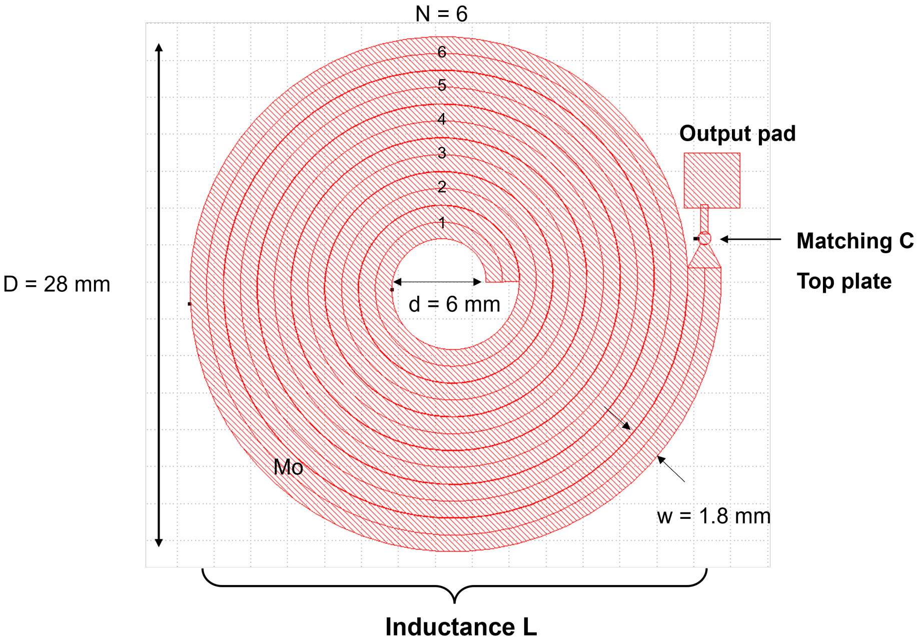


Figure 3.32: **Mask 4:** Spiral inductor + Top plate C + Interconnects.

Therefore, the lift off process starts with spin coating of PR, exposure and patterning based on **mask 4** (Figure 3.32). The top metal is shown in Figure 3.32, represented by the inductive coil $L$, the matching $C$ top plate and the second output pad. A more detailed view of all these features and how they are interconnected is reported in Figure 3.33.

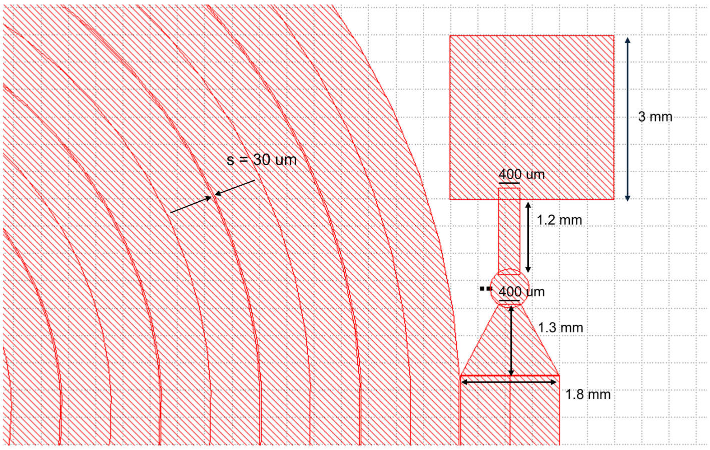


Figure 3.33: **Mask 4:** zoomed view of top metal layer.

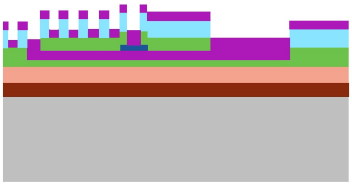


Figure 3.34: **Step 22** - Sputtering of Mo.

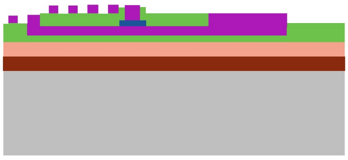


Figure 3.35: **Step 23** - Lift-off of Mo.

Mo is then sputtered on the wafer and lifted off by dissolution of the PR.

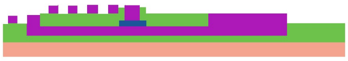


Figure 3.36: **Step 24** - Device release by dissolution of dextran in water.

Finally, the dextran sacrificial layer is dissolved in water for 10-15 min, and the device is released.

The **final device** at the end of the fabrication is illustrated in Figure 3.37:

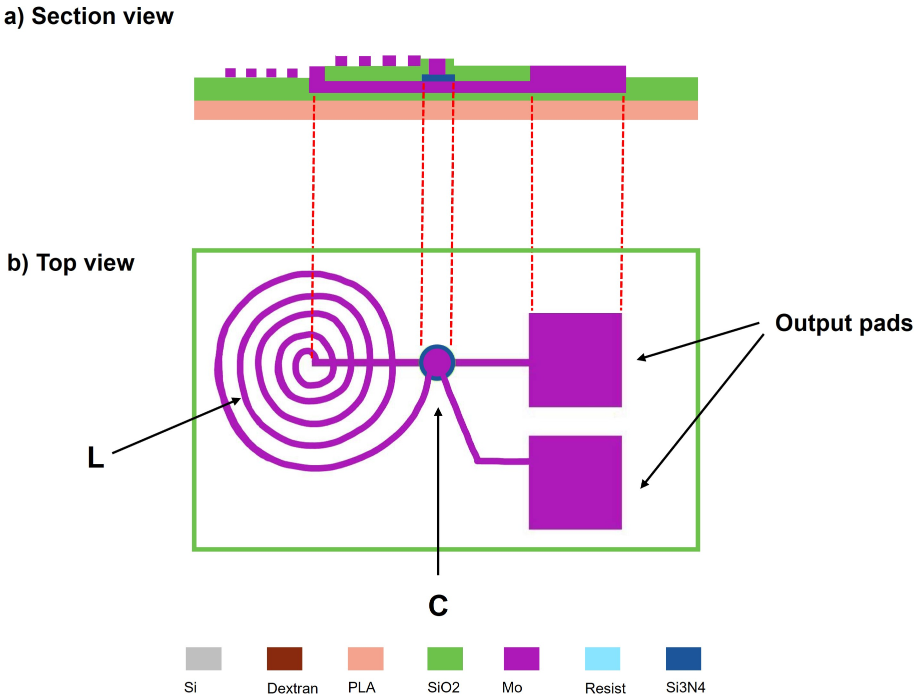


Figure 3.37: Representation of the final device fabricated. (a) Section view. (b) Top view.

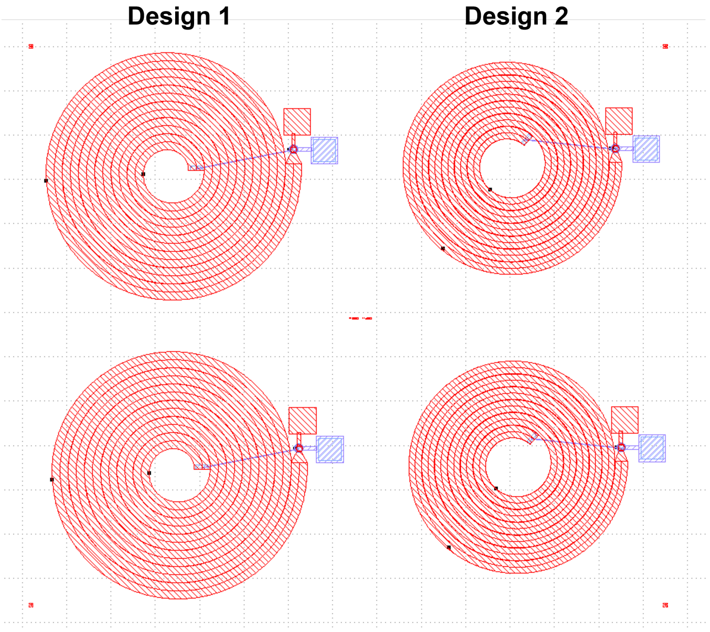


Figure 3.38: **Full mask:** array for LC coils.

Finally, the final mask used during the photolithography is presented, comprised of both designs and all the reticles for each layer to expose, showing how the devices should look on wafer-scale at the end of fabrication.

# Results and Discussion

This chapter describes in detail the practical work carried out in the Else Kooi Laboratory (EKL) and Kavli Nanolab at Delft University of Technology in order to optimize the fabrication process of a biodegradable wireless power transfer device presented in Chapter 3. The fabrication steps will then be retraced, focusing on the problems encountered, the solutions thought up, and therefore the results obtained.

The laboratory work was initially organized considering a Dextran + PLA substrate, and then, a series of experiments with different substrates (Dextran + PLA, only PLA, only Dextran, only $SiO_2$) were carried out.

## 4.1 Solutions preparation

The process begins with the preparation of dextran and PLA solutions in BioMEMS Lab at EKL for subsequent spin coating. Since these solutions remain stable for only 3–4 days, batches of about 10-50 mL were typically prepared as needed in small glass jars. In both cases, a magnetic stirrer was employed to ensure thorough mixing of solute and solvent.

To calculate the solution recipe, the weight/weight percentage formula for solution preparation was adopted, as reported in Eq. 4.1.

$$\%w/w = \frac{\text{mass of solute}}{\text{total mass of solution}} \times 100 = \frac{m_{solute}}{m_{solute} + m_{solvent}} \times 100 \tag{4.1}$$

where the mass of the solvent is $m_{solvent}= V_{solvent} \cdot \rho$, $V_{solvent}$ is the volume of the solvent (usually fixed at the beginning of the preparation) and $\rho$ [g/mL] is the density of the solvent.

- **Dextran solution**

  A 10 wt% dextran solution in deionized water ($H_2O$) was prepared by dissolving 5 g of dextran in 45 mL of DI water. The mixture was placed on a magnetic stirrer at 350 rpm and kept at room temperature (RT) for at least 30 minutes. The solution results very waterish.

- **PLA solution**

  A PLA solution in chloroform ($CHCl_3$) was prepared. Different concentrations of PLA were tested to determine the most suitable conditions for spin coating and to achieve a target substrate thickness of 1.5 $\mu$m.

  - **10 wt% PLA**
    1.65 g of PLA + 10 mL of $CHCl_3$, 250 rpm at T=50°C for ≈ 1 h (until PLA grain are fully dissolved);

  - **5 wt% PLA**
    0.78 g of PLA + 10 mL of $CHCl_3$, 250 rpm at T=50°C for ≈ 1 h;

  - **4 wt% PLA**
    0.62 g of PLA + 10 mL of $CHCl_3$, 250 rpm at T=50°C for ≈ 1 h;

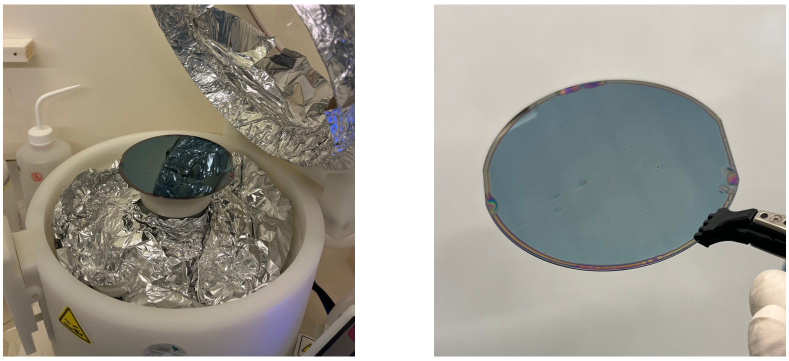
  - **2 wt% PLA**
    0.30 g of PLA + 10 mL of $CHCl_3$, 250 rpm at T=50°C for ≈ 1 h;

  - **1 wt% PLA**
    0.15 g of PLA + 10 mL of $CHCl_3$, 250 rpm at T=50°C for ≈ 1 h.

## 4.2 Spin Coating of dextran and PLA

Starting from a cleaned n-type silicon carrier wafer, an oxygen plasma treatment is performed for surface activation ($O_2$ gas at 50 sccm, 200 W for 2 min) using Diener Atto Plasma Reactor in polymer Lab in EKL.

### 4.2.1 Dextran



(a) (b)

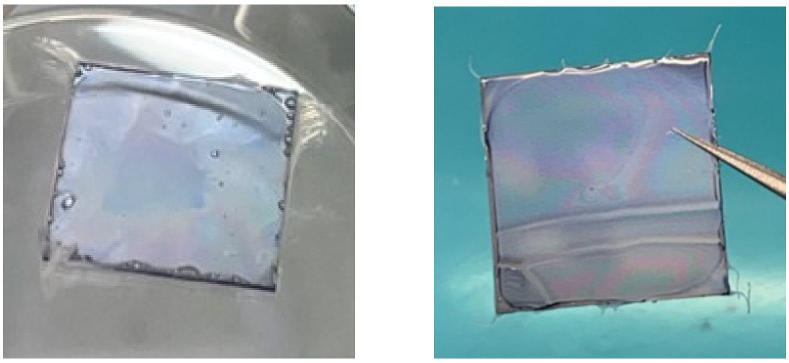
Figure 4.1: (a) Silicon wafer in the spin coater. (b) Dextran thin-film after spin coating.

The spin-coating process was carried out in the BioMEMS Lab. The wafer was mounted on the spin coater chuck and secured under vacuum (Figure 4.1(a)). The dextran solution was dispensed to fully cover the wafer surface (approximately 8-10 mL per wafer). A $\approx 2\ \mu$m dextran film was obtained by spin coating at 1200 rpm for 30 s, followed by baking at 165°C for 15 min in an oven. After this step, the wafer appeared as shown in Figure 4.1(b): the dextran layer was uniform and bluish, yet highly transparent, with the reflective surface of the silicon wafer still visible.

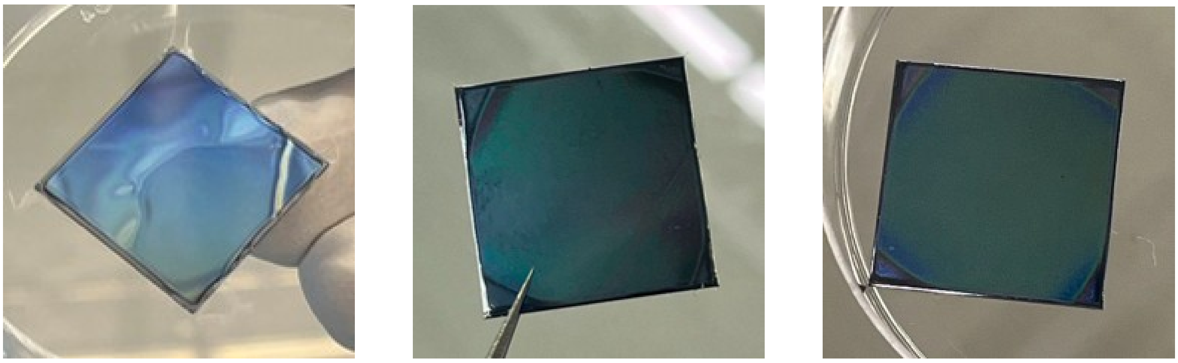
### 4.2.2 PLA

After depositing dextran, the PLA layer was spin coated. The initial objective was to achieve a thickness of 1.5 $\mu$m, so preliminary trials were carried out on 2 × 2 cm samples using PLA solutions of different concentrations (Figure 4.2). As expected, higher PLA concentrations yielded more viscous solutions and consequently thicker films at the same spin speed.

Specifically, PLA solutions of 10 wt%, 5 wt%, 4 wt%, 2 wt%, and 1 wt% were spin coated at 3000 rpm using a three-step program (ramp from 0 to 3000 rpm in 15 s, hold at 3000 rpm for 1 min, ramp down to 0 rpm in 15 s). Following spin coating, the samples were baked at 70 °C for 10 min on a hotplate. It is critical that this bake is performed precisely at 70 °C, and not at higher temperatures above the PLA glass transition ($\approx$ 65 °C) which could compromise subsequent steps, such as silicon oxide deposition. Moreover, due to the high volatility of chloroform, the solution jar must be closed immediately after dispensing a small portion onto the sample.



10 wt% 5 wt%



4 wt% 2 wt% 1 wt%

Figure 4.2: Spin coating of PLA at 3000 rpm (three-step process).

The 10 wt% PLA solution was highly viscous and difficult to dispense onto the wafer, resulting in a non-uniform layer with numerous bubbles. In contrast, the 5 wt% and 4 wt% solutions were easily handled with a pipette and well suited for spin coating, producing uniform, whitish, and opaque films. The 2 wt% and 1 wt% solutions, being very dilute, yielded non-uniform coatings; under the microscope, the films appeared fragmented into PLA islands, likely due to the high chloroform content and its rapid evaporation.

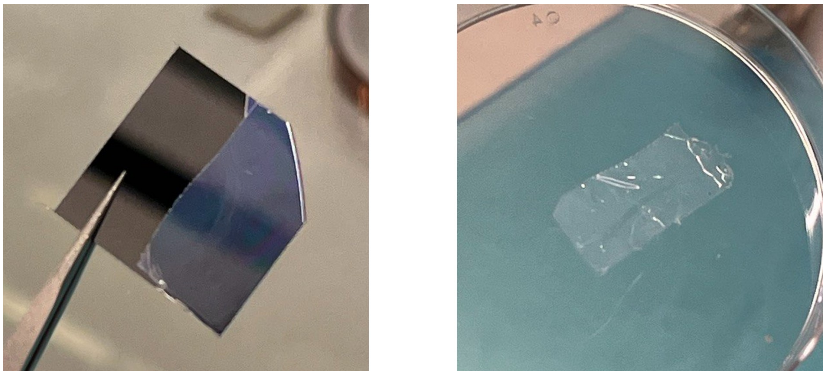


Figure 4.3: Peeling of 5 wt% PLA layer.

In particular, 5 wt% and 4 wt% PLA layers were easy to peel off, as shown in Figure 4.3.

The thickness of the PLA layer for different concentrations at 3000 rpm was then measured by the Bruker Dektak XT profilometer in Kavli Nanolab, after creating a step by peeling off a portion of the PLA layer. The results are summarized in Table 4.1 and Figure 4.4.

Table 4.1: Measured PLA thickness at 3000 rpm (15 s ramp-up time) for different concentrations.

| **PLA concentration (wt%)** | **Thickness ($\mu$m)** |
|---|---|
| 10 | 16.0 |
| 5 | 4.2 |
| 4 | 2.7 |
| 2 | 1.0 |
| 1 | 0.3 |

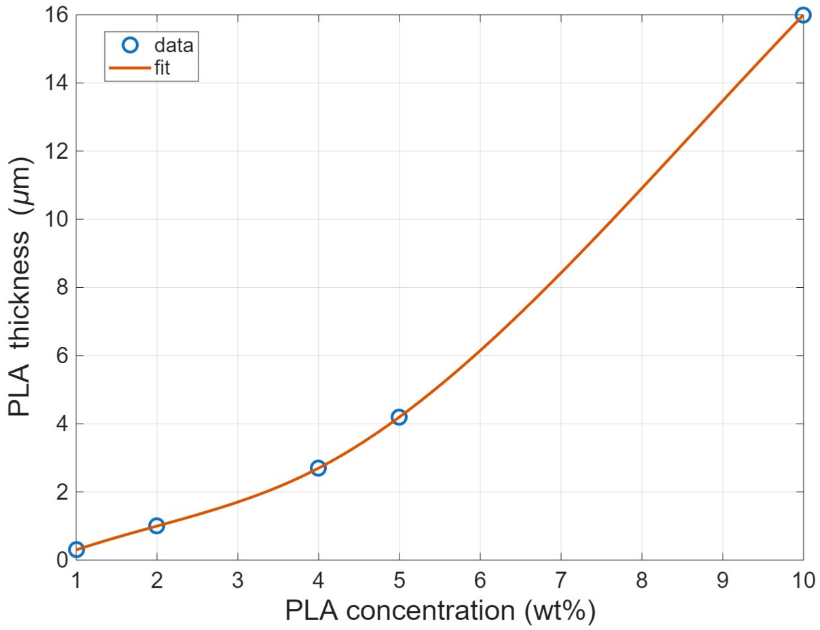


Figure 4.4: PLA thickness vs PLA concentration at 3000 rpm with 15 s ramp-up time.

Since the 5 wt% and 4 wt% solutions proved to be the most suitable, the spin-coating parameters were optimized to achieve the target PLA thickness of 1.5 $\mu$m. Specifically, the ramp-up time was minimized (2 s) to limit chloroform evaporation during acceleration (which was preventing the reduction of the thickness), while the spin duration at maximum speed was kept at 1 minute. The resulting film thickness was then measured at different spin speeds (3000, 5000, and 6000 rpm).

Table 4.2: Measured PLA thickness at different spin speeds for 4 wt% and 5 wt% solutions with 2 s ramp-up time.

| **Spin speed (rpm)** | **Thickness 5 wt% ($\mu$m)** | **Thickness 4 wt% ($\mu$m)** |
|---|---|---|
| 3000 | 2.50 | 1.50 |
| 5000 | 2.12 | 1.38 |
| 6000 | 1.90 | 1.32 |

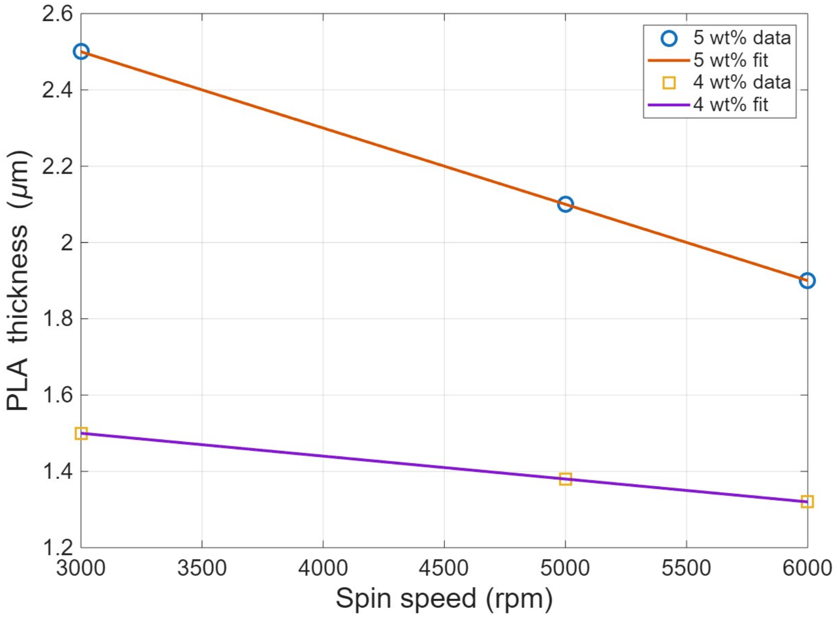


Figure 4.5: PLA thickness vs. spin speed (4 wt% vs 5 wt%) with 2 s ramp-up time.

**Optimization**

- A 2 $\mu$m **dextran** sacrificial layer is deposited by spin-coating of a 10 wt% solution of dextran and water, at 1200 rpm for 30 s, followed by a 15 min soft baking at 165°C in an oven.
- A 1.5 $\mu$m **PLA** layer is achieved using a 4 wt% solution spin coated at 3000 rpm (2 s ramp-up) for 1 min. Then, a 10 min soft baking at 70°C is performed on a hotplate. Stability critically depends on baking at 70°C. The same parameters were then used for wafer-scale deposition on dextran.

## 4.3 Silicon oxide deposition by ICP-PECVD

A 200 nm protective $SiO_2$ layer was deposited by ICP-PECVD using an Oxford Instruments PlasmaPro100 system at Kavli Nanolab. The deposition was performed at the lowest available temperature, 75°C, with 1300 W RF power and 8 mTorr pressure, using a standard precursor mixture of silane $SiH_4$ (16 sccm), oxygen $O_2$ (60 sccm), and argon (10 sccm). The deposition rate is approximately 70.1 nm/min. This step is particularly critical, as the process temperature is close to the glass transition of PLA ($T_g \approx 65$ °C). At this point, PLA begins to soften, and when it cools down after the deposition of an overlying rigid and glassy silicon oxide film, it leads to crack formation both at the 2×2 cm sample scale and across full wafers (Figure 4.7). Actually, cracks take place also in the PLA layer, as showed in Figure 4.6, where a 100 nm $SiO_2$ film was deposited on PLA, and a $\approx$ 440 nm (average value) crack depth was measured.

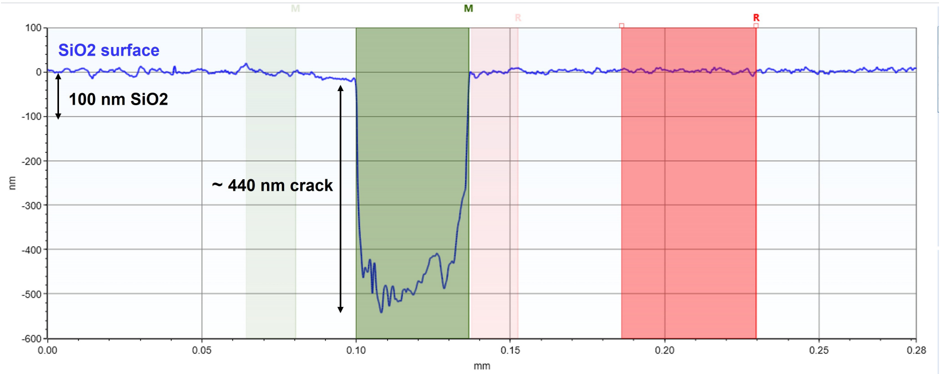


Figure 4.6: $\approx$ 440 nm crack depth (average value) measured in a 100 nm $SiO_2$ film on PLA.

The problem is due to three main reasons:

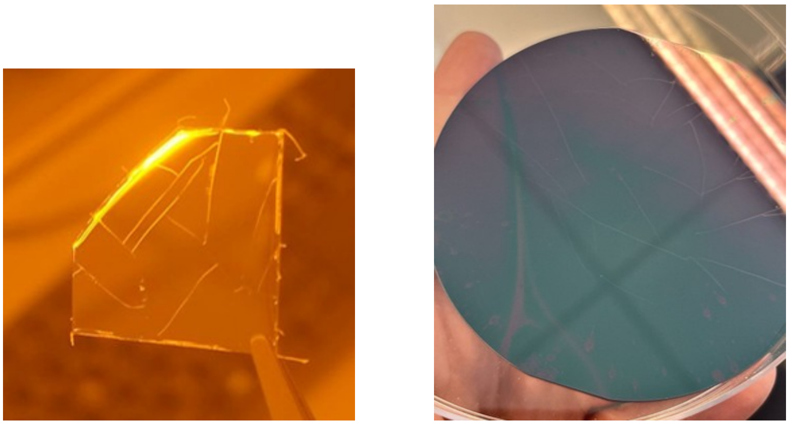
1. The **thermal expansion coefficient (CTE) mismatch** between PLA and $SiO_2$ induces stresses. PLA's CTE can vary significantly depending on its crystallinity, processing, temperature range, but it could be estimated in the order of $40–80 \times 10^{-6}$ $K^{-1}$ [61] [62], while $SiO_2$'s CTE is $\approx 0.5 \times 10^{-6}$ $K^{-1}$ [63]. During heating and cooling cycles, PLA tends to expand and contract much more than the oxide layer, which is instead very stiff, generating significant interfacial stresses. [64]

2. **Intrinsic stresses in low-temperature PECVD-grown $SiO_2$** (which can be either tensile or compressive depending on plasma power, pressure, and gas ratios) add to the mechanical load at the interface. [65]

3. **Polymer residual stress.** Spin-coated polymers often trap residual stress from rapid solvent loss and vitrification; stress relaxes only slowly and can nucleate

microcracks that subsequently propagate through the oxide during/after deposition, leading to cracking, especially near $T_g$. Baking at 70°C can help, but residual stress can remain and interact with the oxide's intrinsic/thermal stress to trigger cracking. [66]

The combined effect of thermal mismatch stress and intrinsic film stresses increases the likelihood of crack formation, causing an overall low yield of this fabrication step $\leq 50\%$.



(a) (b)

Figure 4.7: (a) Silicon oxide cracks on PLA (2x2 sample). (b) Silicon oxide cracks on PLA (full wafer).

In principle, the failure mechanisms and cracking probability of a thin $SiO_2$ film on a compliant PLA substrate should decrease either by increasing the substrate thickness (at constant film thickness) or by reducing the film thickness (at constant substrate thickness). [67] However, in practice, cracks still appeared after depositing 200 nm of silicon oxide on a thicker 4 $\mu$m PLA layer, compared to the original 1.5 $\mu$m substrate.

Nevertheless, after several attempts and ensuring that the PLA layer was properly baked at 70 °C after spin coating, a reliable process was finally established for the efficient deposition of $SiO_2$ on PLA by ICP-CVD at 75°C.

**Optimization**

Crack formation was significantly reduced by:

1. **Reducing the oxide's effective thickness per step** (e.g., 50 nm steps followed by 10 min cool-down between each deposition) and targeting a **lower final thickness** (100 nm);
2. **Selecting a proper ICP-PECVD recipe** for lower intrinsic stress. In particular, $SiO_2$ was deposited 75°C, with 1300 W RF power and 8 mTorr pressure, using a different gas ratio of silane $SiH_4$ (11.3 sccm), oxygen $O_2$ (15 sccm), and argon (13.8 sccm). The deposition rate was estimated as $\approx$ 60 nm/min. Due to much lower oxygen flow, it results in a less brittle and balanced hydrogenated $SiO_2$.

Further ideas still to explore to improve the yield are: a) stabilizing the PLA before oxide deposition by extending the post-spin baking time, holding near but not above $T_g$ to allow stress relaxation, then cool slowly; b) consider adhesion/stress-buffer interlayers. [68]

## 4.4 Molybdenum sputtering

A 500 nm molybdenum thin film was sputtered onto the $SiO_2$ layer at room temperature by Alliance Concept (AC) Metal 1 in Kavli Nanolab, using 100 W power, 3.4 $\mu$bar pressure, and a deposition rate of 0.6 nm/s. This step proved particularly challenging too, as depositing the entire 500 nm in a single run consistently led to substrate cracking. The failure can be attributed not only to the intrinsic stresses that develop in thick sputtered Mo films, but also to localized substrate heating caused by energetic ion bombardment during the process. Both effects combine to increase the overall stress in the PLA/$SiO_2$/Mo stack, reducing its mechanical stability and making cracking more likely.

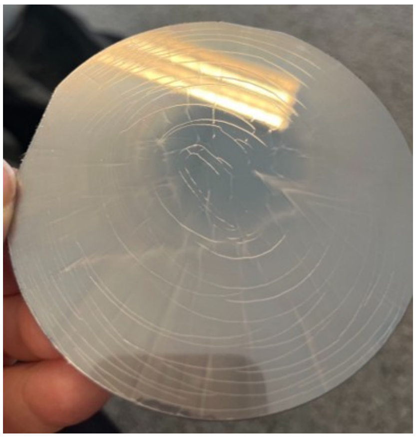


Figure 4.8: Cracks in Mo sputtered film on silicon oxide/PLA substrate.

It is well known that sputtering parameters strongly affect thin-film stress. Higher sputtering power increases ion energy and bombardment, which typically induces compressive stress due to atomic peening, while also enhancing substrate heating. Conversely, higher chamber pressure promotes more scattering of sputtered atoms, leading to a more porous, lower-density microstructure that is often associated with tensile stress. By tuning power and pressure, it is therefore possible to partially mitigate intrinsic stress and reduce the likelihood of cracking in the Mo layer.
Among the available recipes in AC Metal 1, the most suitable was identified and adopted.

**Optimization**

A 500 nm **Mo** film is **sputtered** on $SiO_2$/PLA substrate was performed at RT (100 W, 3.4 $\mu$bar, rate 0.6 nm/s) in steps of 100 nm. This increased the deposition time but eliminated cracking in the Mo film.

## 4.5 Photolithography

The first photolithography step was performed to define a photoresist mask for etching/patterning the Mo film, thereby forming the first metallic layer of the device.

### 4.5.1 Photoresist selection and spin coating

The spin coating of photoresist was performed in the Wet Bench Area inside the Kavli Nanolab cleanroom at TU Delft.

The photoresist was selected, among those available in the Kavli Nanolab cleanroom, based on the soft-bake and post-exposure bake temperatures required, in order to prevent further cracking in the already delicate Dextran/PLA/$SiO_2$/Mo stack. Among the low-temperature options, AZ ECI 3012 positive resist was chosen, as it provides a thickness of about 1.5 $\mu$m at 2500 rpm for 1 min, with a soft bake of 60 s at 90°C (directly on a hotplate). A thickness of 1.5 $\mu$m was considered appropriate for this photolithography step.

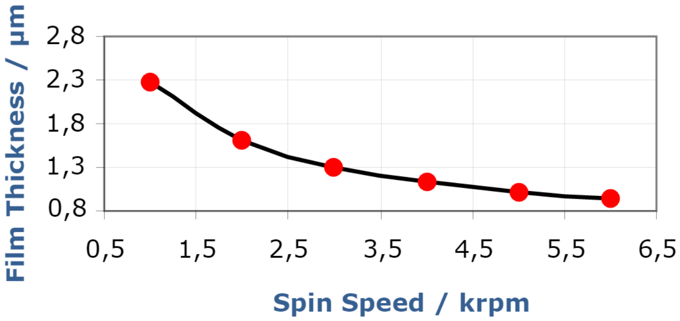


Figure 4.9: AZ ECI 3012 resist film thickness vs spin speed. [69]

From a theoretical perspective, the choice of resist thickness is a trade-off. A resist that is too thin may not provide sufficient protection during subsequent etching, leading to premature mask failure. Conversely, a resist that is too thick can reduce resolution due to light scattering and absorption within the resist, making it difficult to reproduce fine features accurately. Thus, an intermediate thickness of $\approx$ 1.5 $\mu$m ensures both adequate pattern fidelity and sufficient etch resistance for this process.

Normally, before spin coating the resist on a wafer, a treatment with HMDS (hexamethyldisilazane) is performed to improve adhesion. HMDS reacts with hydroxyl groups on the wafer surface, replacing them with hydrophobic $-Si(CH_3)_3$ terminations that promote better resist adhesion. This process is typically carried out in a dedicated station, which also dries the surface at 150°C. In this case, however, when the treatment was attempted, the high temperature (as expected) led to substrate failure.

Similarly, the standard soft bake at 90°C for 60 s after spin coating resulted in substrate cracking. In both situations, the outcome is attributed to PLA softening, followed by contraction during cooling.

After several unsuccessful attempts, it was observed that the cracking issue during soft baking could be mitigated by using a 90°C bake for 90 s **in proximity mode** (holding the wafer by a tweezer at $\approx$ 1 cm above the hotplate) rather than by direct contact with a hotplate.

### 4.5.2 Exposure

The photolithographic exposure was performed with a Heidelberg Instruments MLA150 maskless laser writer in the Kavli Nanolab cleanroom. Unlike conventional steppers, the MLA150 projects a virtual mask directly from a digital layout (e.g. GDSII designed in software such as KLayout) onto the photoresist, using a spatial light modulator while the XY stage scans the substrate. This maskless approach eliminates the time and cost of fabricating physical photomasks and greatly increases flexibility for rapid prototyping and design iterations.

Two parameters are critical and must be optimized for each resist type and thickness, and substrate: 1) exposure dose (mJ/cm$^2$), the effective energy delivered to the resist, which controls underexposure versus overexposure, and thus feature size and profile; 2) defocus (focus offset), the distance of the focal plane from the resist surface, which governs spot size and sidewall verticality. Proper tuning of dose and defocus is essential to achieve the intended critical dimensions, clean openings.

In this work, this tuning was performed by starting exposing a test structure (Figure 4.10) on a 1.5 $\mu$m resist layer by MLA150 setting 200 mJ/cm$^2$ and defoc = 0, considering previous MLA150 users tests. The results of this exposure are reported in Figure 4.11.

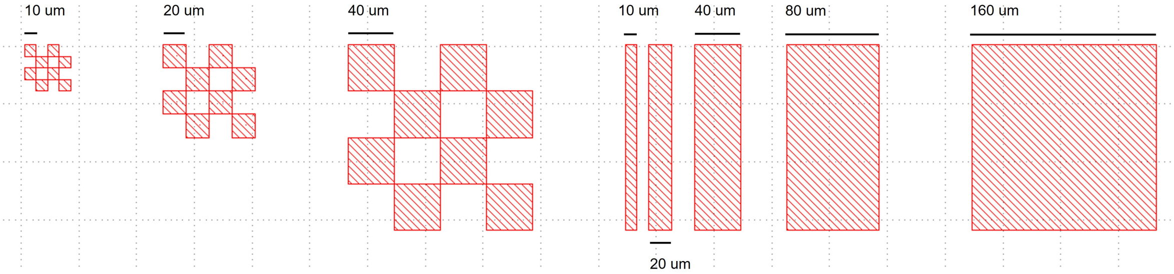
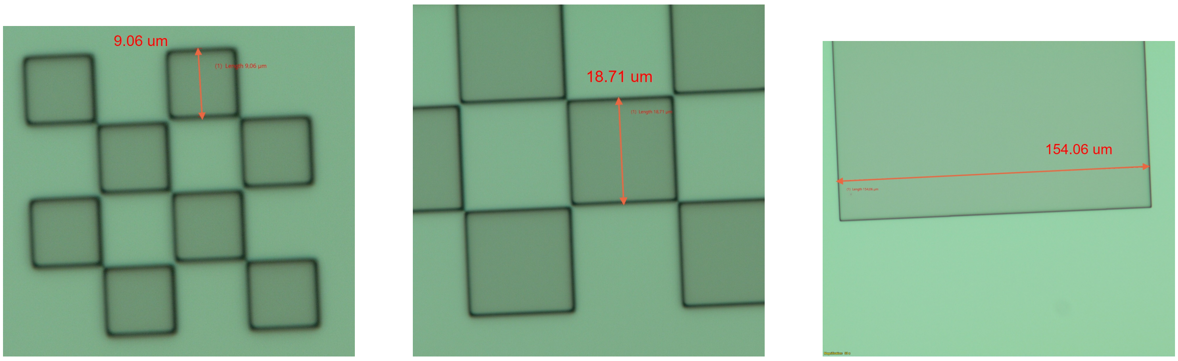


Figure 4.10: Test structures to tune exposure dose and defoc for a 1.5 $\mu$m AZ3012 layer on dextran/PLA/SiO$_2$/Mo stack by MLA150.



(a) (b) (c)

Figure 4.11: Exposure test performed with MLA150 at 200 mJ/cm$^2$ and defocus = 0 on a 1.5 $\mu$m AZ3012 layer deposited on the dextran/PLA/SiO$_2$/Mo stack. Measured feature sizes: (a) 9.06 $\mu$m vs 10 $\mu$m nominal. (b) 18.71 $\mu$m vs 20 $\mu$m nominal. (c) 154 $\mu$m vs 160 $\mu$m nominal.

This result was considered acceptable, as the average relative error was 6.5%. Given that the minimum feature size of the LC coil is the 30 $\mu$m spiral spacing, a deviation of ± 2 $\mu$m does not significantly affect device performance.

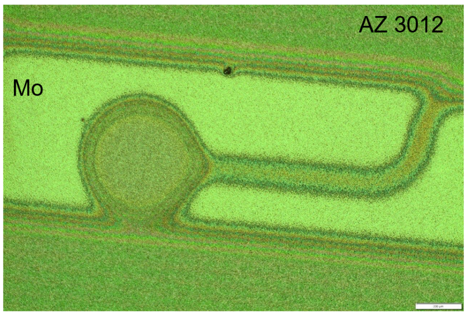


Figure 4.12: Underexposure of AZ 3012 1.5 $\mu$m film on Mo (Dose = 130 mJ/cm$^2$, defocus = 0).

Actually, a previous wrong exposure was performed at dose = 130 mJ/cm$^2$ and defocus = 0, and the result is reported in Figure 4.12 to show the actual effect of underexposure.

Once selected the correct parameters, the exposure can be carried out considering the design in mask 1 (3.13) to pattern the first metal layer (one output pad + bottom plate of the capacitor + LC interconnection). In general, considering the masks designed with KLayout and reported in Subsection 2.2.3, the drawn features correspond to the areas exposed by the MLA150. Since a positive resist was selected, in which the exposed regions are dissolved, it is necessary to invert the mask within the MLA software and expose the complementary pattern of the one previously designed.

It is crucial to include alignment markers in the same position on each mask used in the first and successive lithography steps, to ensure proper alignment with the first developed layer. Typically, four cross-shaped structures are employed on each corner (also two are enough), as illustrated in Figure 4.13.

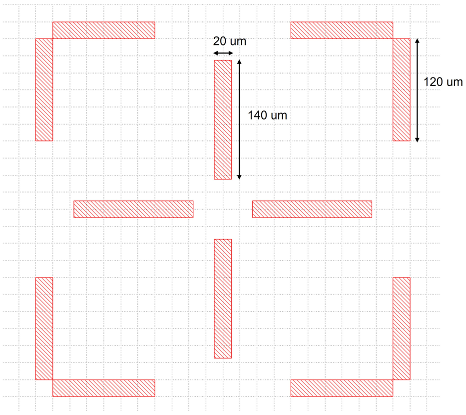


Figure 4.13: Alignment marker.

### 4.5.3 Development

Finally, a 90 s post-exposure bake was performed at 110°C in proximity mode in the wet bench area of Kavli Nanolab. The wafer was then developed by immersion in an AZ 726 MIF developer for 1 min, followed by rinsing with a water gun for 30 s, taking care not to excessively affect the dextran layer, which is water-soluble. This developer is fully compatible with the AZ3012 photoresist and, in this case, does not appear to affect the underlying dextran/PLA substrate. After this step, the photoresist mask is finally developed on the Mo thin film.

After development, the photoresist mask thickness was measured by a Dektak XT profilometer as $\approx$ 1.4-1.5 $\mu$m, as reported in Figure 4.14.

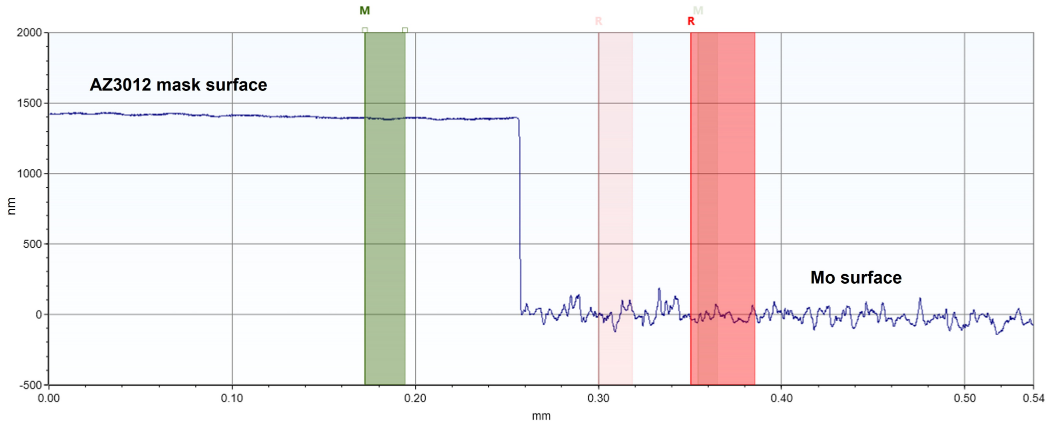


Figure 4.14: ≈ 1.5 photoresist mask thickness.

The entire optimized photolithography process is summarized here:

**Optimization**

**Photolithography process:**

- **Spin coating** of ≈ 1.5 $\mu$m AZ ECI 3012 positive resist film at 2500 rpm for 1 min + 90 s soft baking at 90°C **in proximity mode**;
- **Exposure by MLA150** with dose = 200 mJ/cm$^2$ and defoc = 0 + post-exposure baking at 110°C for 90 s **in proximity mode**;
- **Development** in AZ 726 MIF for 1 min + 30 s rinsing by water gun.

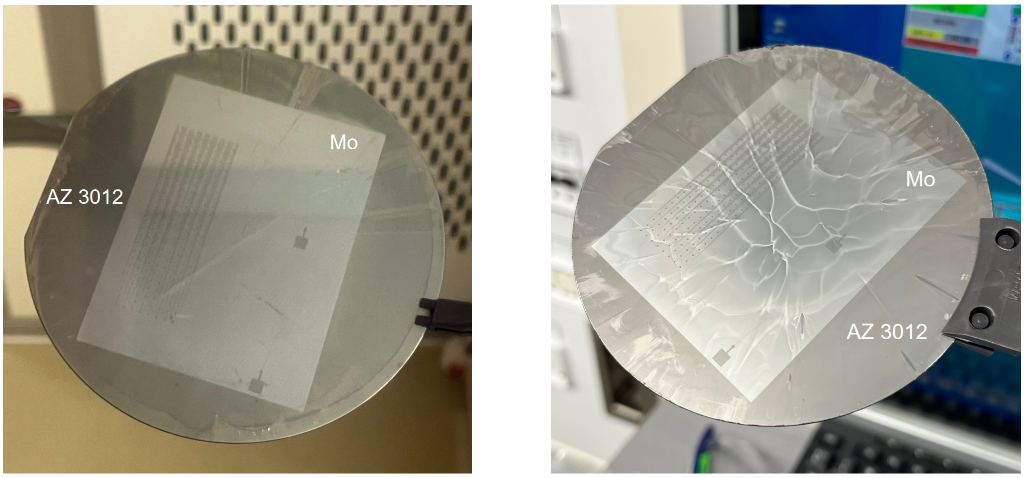
## 4.6 RIE of molybdenum

Molybdenum patterning was carried out in the EKL cleanroom using the ALCATEL AMS110 ICP-RIE tool, with SF$_6$ at 650 sccm, 2000 W, and a pressure of $1.0 \times 10^{-1}$ mbar. The etching rate for Mo is 50 nm/min. At this stage, the work was organized into a series of experiments to investigate Mo etching on different substrates:

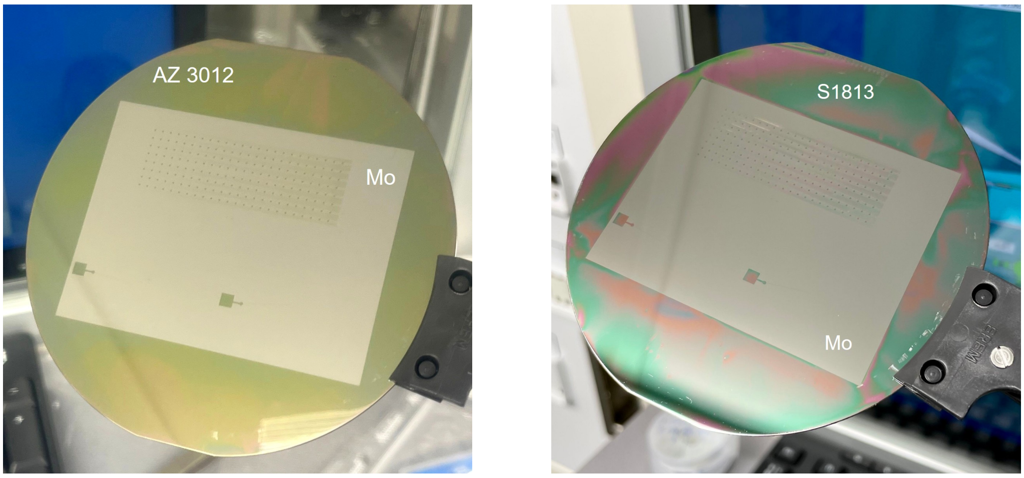
1. **Dextran + PLA** (the complete stack for which the process flow was designed);
2. **PLA alone**;
3. **Dextran alone**;
4. **Silicon oxide SiO$_2$** alone (already used as a protective interlayer between substrate and Mo) to have a safe sample.

This section presents the results of these tests. The Mo etching rate for the selected recipe is 50 nm/min. Since dry etching is particularly critical for polymeric substrates, due to ion bombardment and localized surface heating, the process was performed in small steps of 1, 2 or 2.5 min to limit damage, for an overall etching time of ≈ 10 min, since the Mo film thickness is 500 nm.

Figure 4.15 shows the samples processed by photolithography, where a 1.5 $\mu$m resist mask was developed according to a co-designed mask (Figure 4.16), on four different substrates. The wafer contains two distinct designs: the bottom metal layer of the LC coil developed in this work, and additional features belonging to a separate design by Friso Kahler, a PhD student in my same research group at TU Delft.



(a) Dextran + PLA (b) PLA



(c) Dextran (d) $SiO_2$

Figure 4.15: Four samples after photolithography using Mask 1 with different substrates before etching: (a) Dextran + PLA, (b) PLA, (c) Dextran and (d) Silicon oxide.

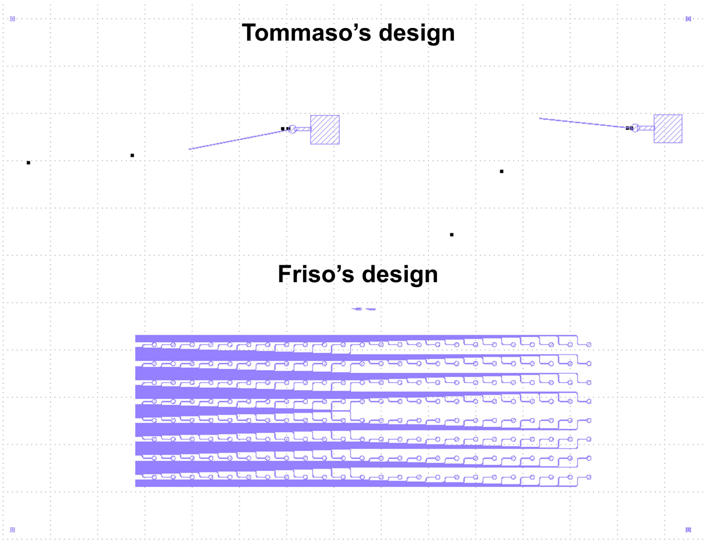


Figure 4.16: Co-designed mask.

1. **Dextran + PLA substrate**

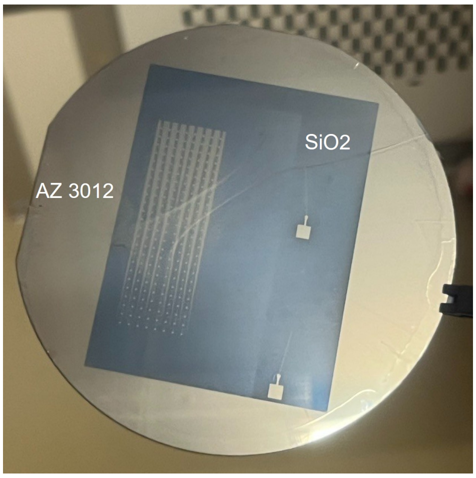
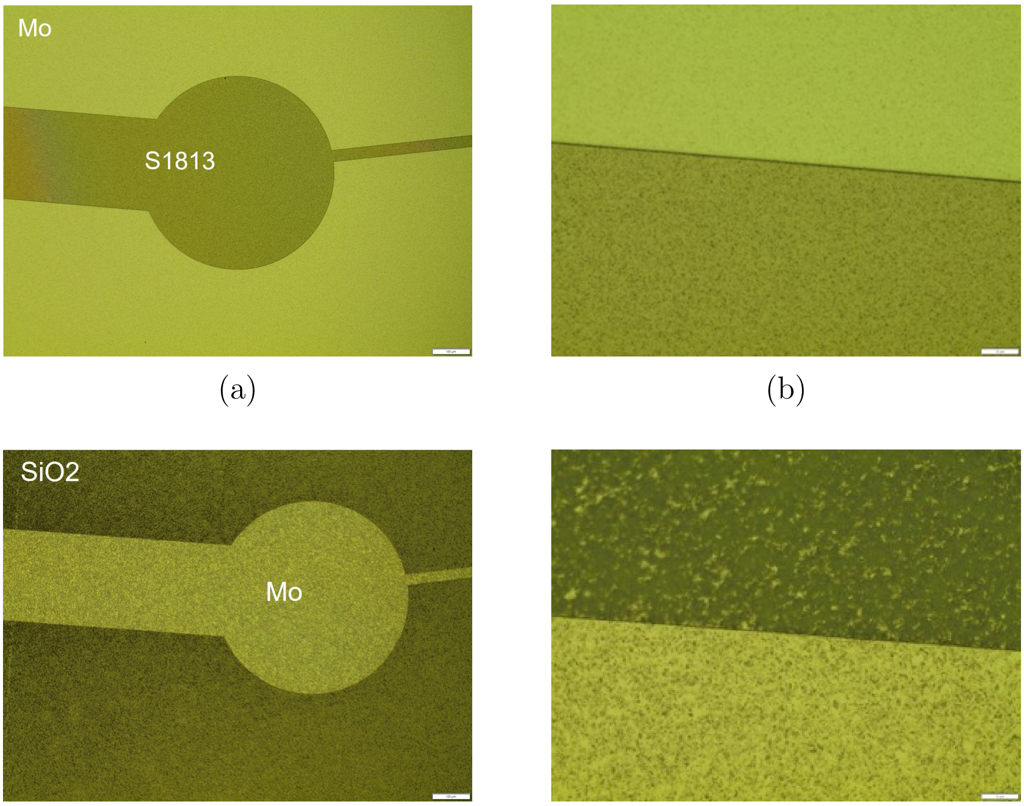


Figure 4.17: Mo etching (10 min in four steps of 2.5 min) by RIE using $SF_6$ on dextran+PLA substrate.

Starting from the wafer shown in Figure 4.15(a), the dextran+PLA sample was etched by RIE in four steps of 2.5 min, for a total etching time of 10 min. After each step, the wafer was inspected to monitor the progressive removal of the Mo layer, which gradually revealed the underlying $SiO_2$ film, exhibiting an expected bluish color. This demonstrated the feasibility of patterning of Mo on dextran + PLA layer.



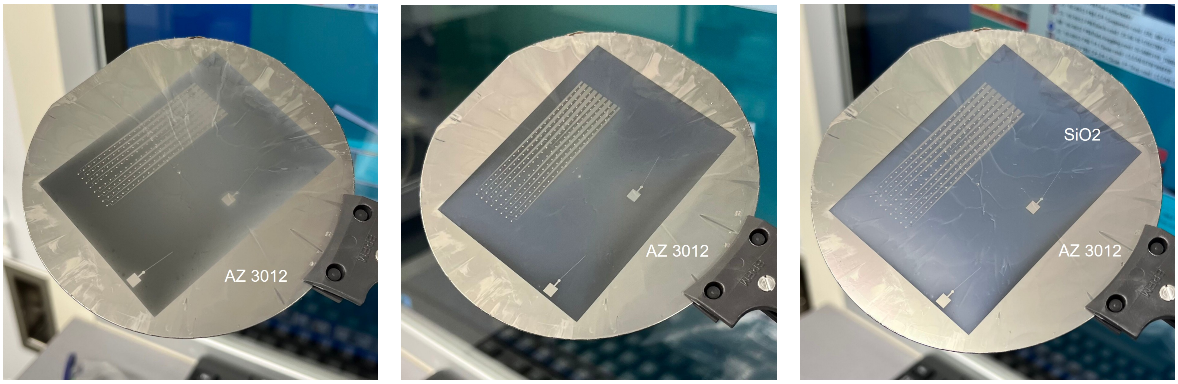
(a) (b)

(c) (d)

Figure 4.18: Microscope inspection of dextran + PLA sample. (a) Before etching (x5). (b) Before etching (x50). (c) After etching (x5). (d) After etching (x50).

The dextran+PLA sample was inspected under a microscope before and after the etching process. As shown in Figure 4.18, the wafer surface appears significantly rougher after RIE. This behavior can be explained by the limited thermal and mechanical stability of polymer-based substrates, which are more susceptible to ion bombardment and plasma-induced heating. As a result, even when the metal layer is effectively removed, the underlying stack experiences localized damage and surface irregularities, leading to an overall rougher morphology compared to more rigid and stable substrates (as will be demonstrated in following Figure 4.23).

2. **PLA-only substrate**



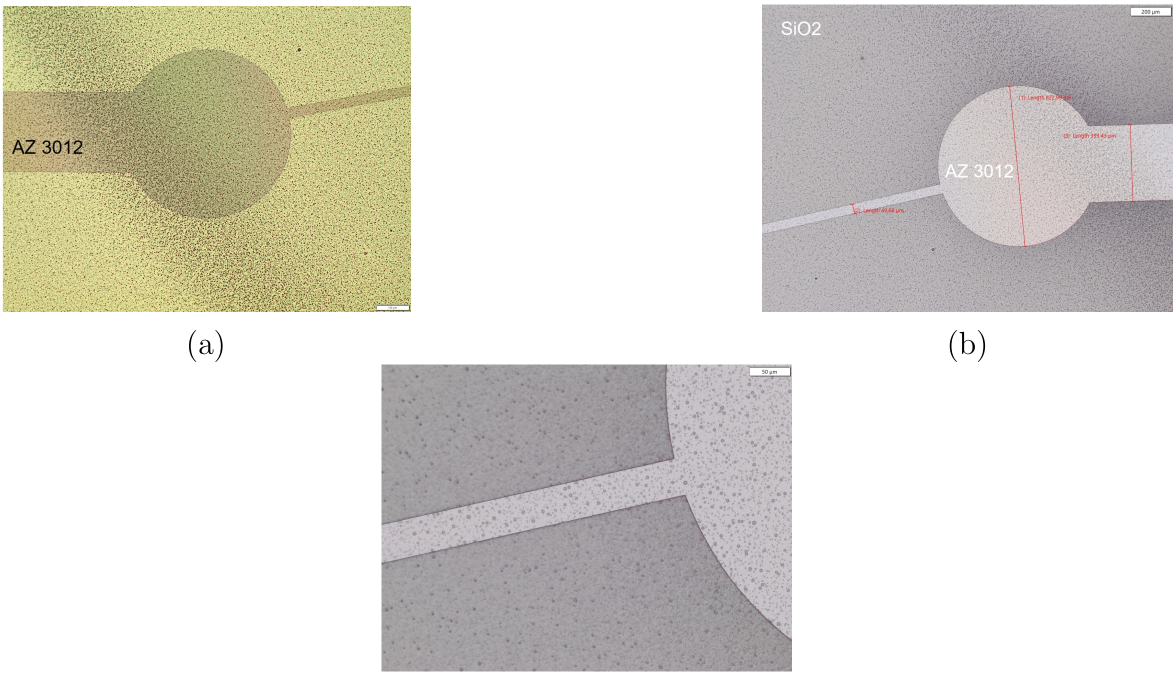
2 min etching

6 min etching

9 min etching

Figure 4.19: Mo etching (9 min in five steps of 1-2 min) by RIE using $SF_6$ on PLA substrate.

In this case as well, the etching process was stopped once the characteristic bluish color was observed, while ensuring under microscope inspection that all features were sharp and well defined, as shown in the examples of Figure 4.20. These results confirm that Mo patterning was successfully achieved also on the PLA-only substrate.



(a)

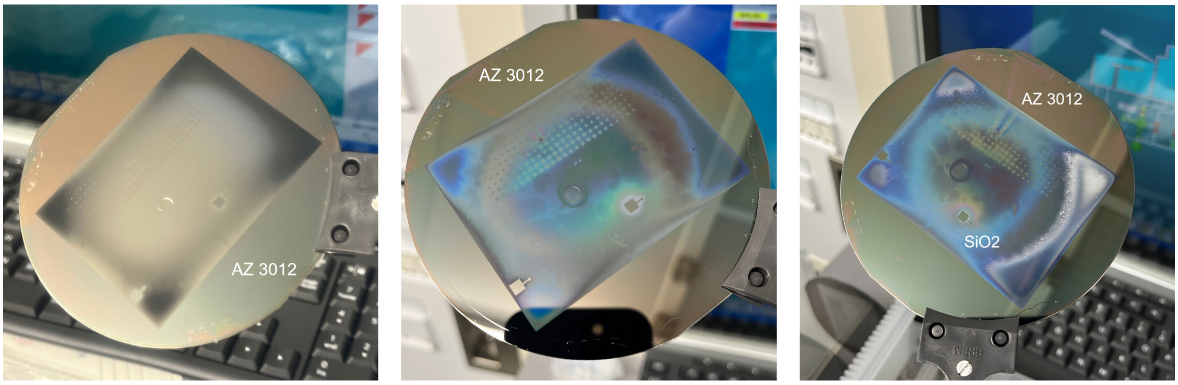
(b)

(c)

Figure 4.20: Microscope inspection of PLA-only sample. (a) Before etching (x5). (b) After etching (x5). (c) After etching (x20).

A comparison between Figure 4.18(a), corresponding to the dextran+PLA substrate, and Figure 4.20(a), corresponding to the PLA-only substrate, shows that the PLA-only sample exhibits a much rougher surface even before etching, and becomes even rougher after RIE. This behavior may be related to the intrinsic surface morphology of spin-coated PLA, which is less uniform than multilayer stacks, and to its lower resistance to plasma exposure, making it more prone to surface degradation during the etching process.

3. **Dextran-only substrate**

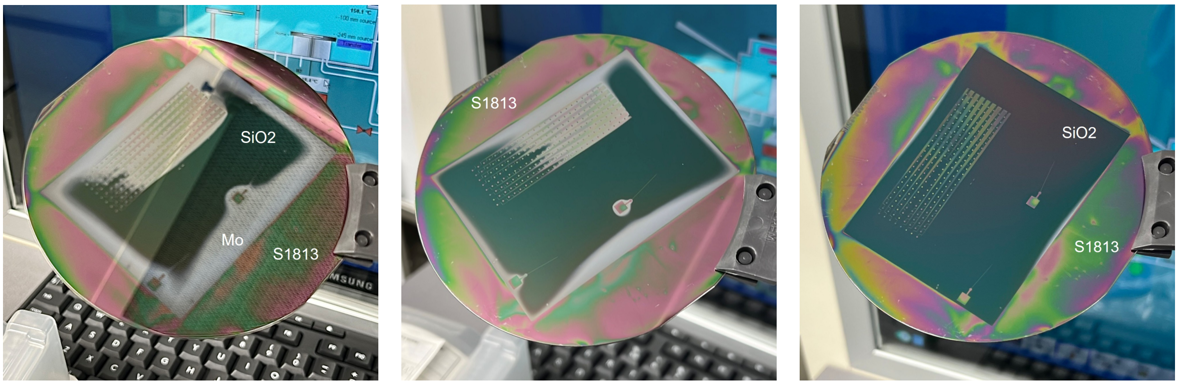


2.5 min etching 5 min etching 10 min etching

Figure 4.21: Mo etching (10 min in four steps of 2.5 min) by RIE using $SF_6$ on dextran-only substrate.

Mo etching was also demonstrated on a dextran-only sample. However, this wafer already had several surface defects prior to etching and was the only remaining dextran-only sample that had successfully withstood the previous process steps. As a result, no further investigations could be carried out on this substrate type.

### 4. Silicon oxide substrate

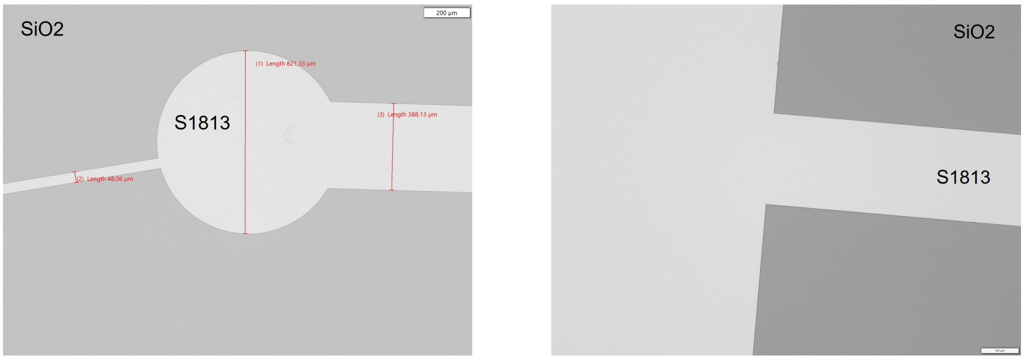


2.5 min etching   5 min etching   11 min etching

Figure 4.22: Mo etching (11 min in four steps of 1-2.5 min) by RIE using $SF_6$ on $SiO_2$-only substrate.

Finally, a standard silicon wafer with 2 $\mu$m of thermally grown oxide was used as a stable substrate to perform Mo RIE, ensuring the availability of a reliable sample for the optimization of subsequent fabrication steps. Due to the thermal growth process, the oxide film has a different color compared to ICP-CVD $SiO_2$, although still bluish. As expected, the RIE step proceeded without issues and complete Mo removal was achieved in approximately 10–11 minutes.

In this case a different photoresist was selected (as can be seen by the different color) just to practice: 1.4 $\mu$m of S1813 spin coated at 4000 rpm + 1 min soft baking at 115° C, exposed with an exposure dose = 145 mJ/cm$^2$ and defoc = 0, without any post exposure baking, and developed for 1 min in MF322 + 30 s in $H_2O$ to stop the development.



(a)   (b)

Figure 4.23: Microscope inspection of $SiO_2$-only sample. (a) After etching (x5). (b) After etching (x20).

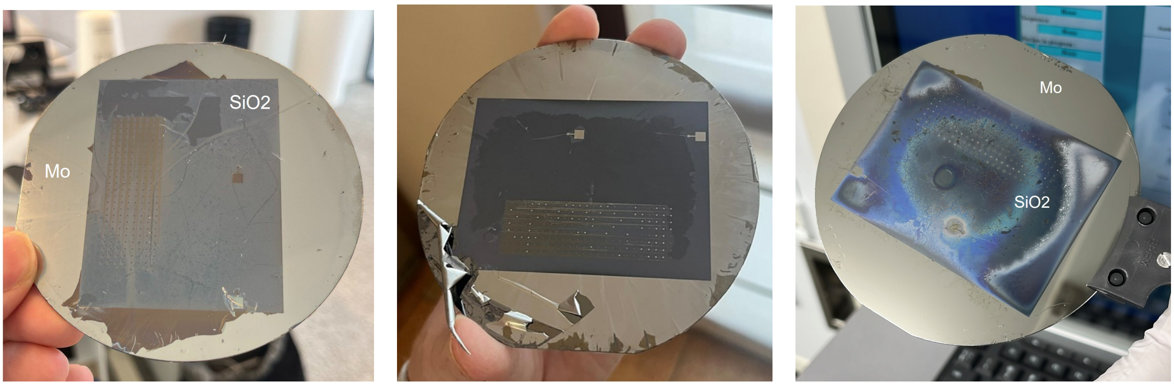
As shown in Figure 4.23, the $SiO_2$-only substrate shows a nearly flat surface after RIE, with no evident roughness, confirming the much higher stability of inorganic substrates compared to polymer-based stacks.

Independently on the substrate, the RIE of Mo was optimized as follows:

**Optimization**

The 500 nm Mo film was **etched by RIE** using $SF_6$ (650 sccm), 2000 W, and $1.0 \times 10^{-1}$ mbar. With an etch rate of 50 nm/min, the process required about 10 min, divided into short steps of 1–2.5 min to limit substrate damage. Etching was stopped once the characteristic bluish color of the underlying $SiO_2$ appeared, and samples were periodically inspected under a microscope to verify proper feature definition.

## 4.7 Stripping of photoresist



(a) Dextran + PLA (b) PLA (c) Dextran

Figure 4.24: Stripping process in methanol. (a) Dextran + PLA sample. (b) PLA. (c) Dextran.

After Mo etching, the photoresist mask was removed in a stripping step. In standard microfabrication, this is typically achieved using acetone; however, since PLA is soluble in acetone, methanol was used instead in order to dissolve the photoresist without damaging the underlying biodegradable polymer layers. In practice, this step proved particularly problematic. Wafer (a) was immersed in methanol for 30–40 min, in intervals of approximately 15–20 min, but the result was unsatisfactory, most likely because a final rinse with fresh methanol was required to completely remove the photoresist residues. Wafer (b) was initially kept in methanol for 40 min, leaving visible photoresist residues; extending the immersion time led to the situation shown in Figure 4.24(b), where delamination of the PLA substrate occurred. Wafer (c) was again treated with methanol for 30–40 min and subsequently rinsed with fresh methanol, but the sample was already in poor condition, preventing any reliable evaluation of the stripping process.

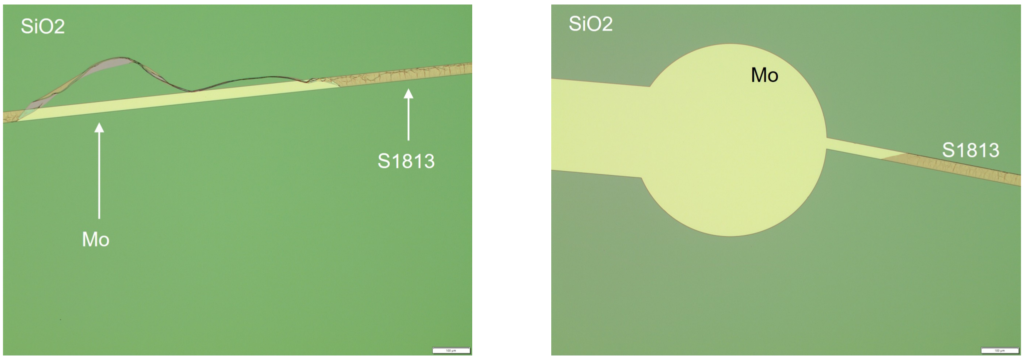
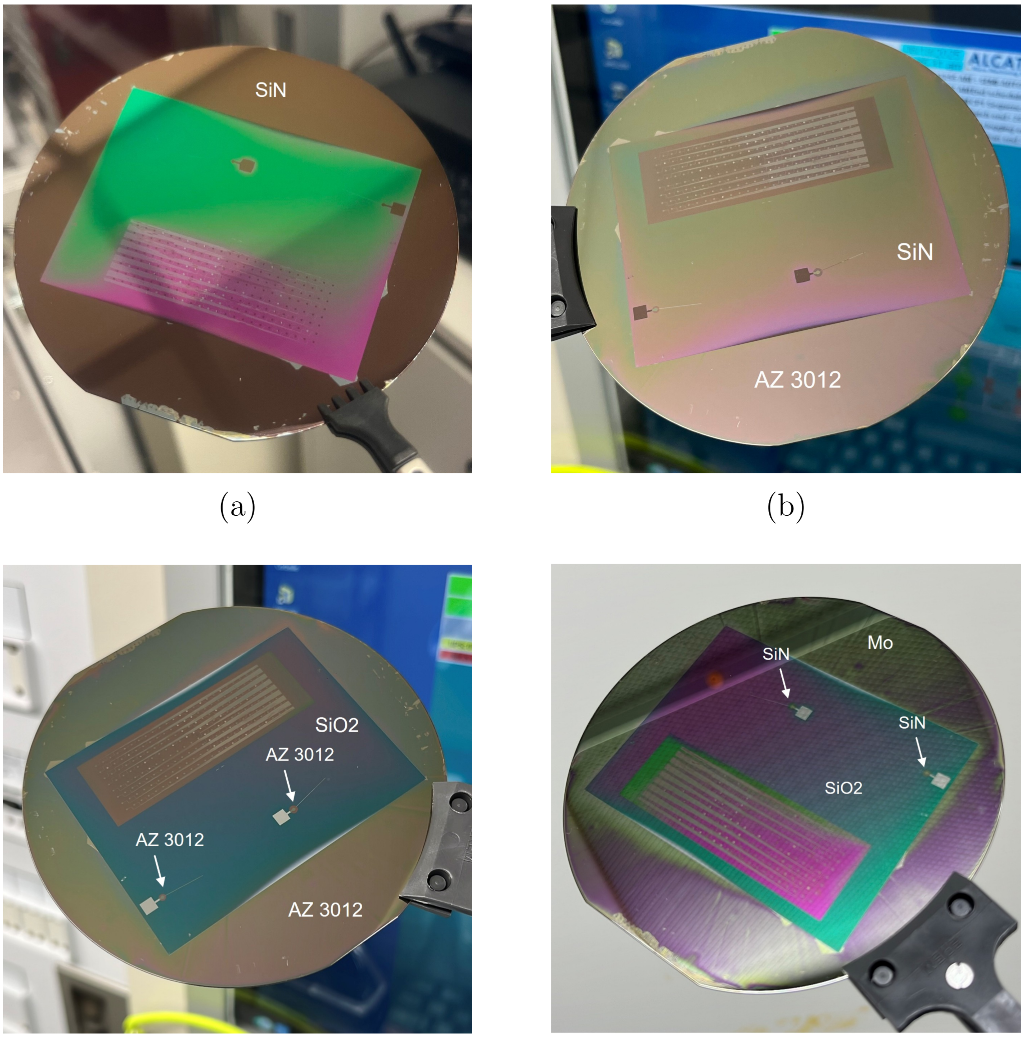


Figure 4.25: Microscope inspection of $SiO_2$-only sample after stripping (x5 view).

The photoresist on the $SiO_2$-only sample was stripped by acetone for 1 h, followed by a careful rinsing by fresh acetone. Despite this long treatment, some photoresist residuals were still visible under microscope.

Overall, regardless of the substrate, this investigation showed that simple immersion in a solvent such as methanol or acetone at room temperature, even for extended times, is not sufficient to completely remove the photoresist film. Future improvements could involve the use of an ultrasonic bath, applied for shorter durations and at slightly elevated temperatures.

## 4.8 Deposition of SiN + Patterning



(a) (b) (c) (d)

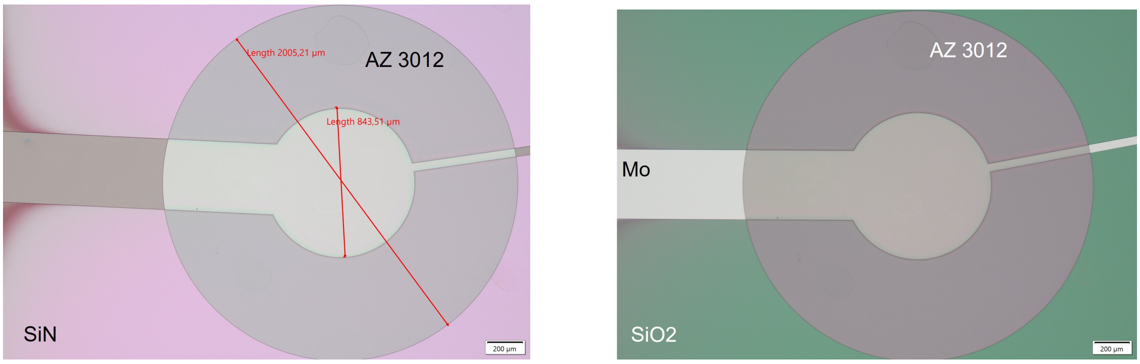
Figure 4.26: SiN deposition and patterning process. (a) Deposition of 30 nm of SiN by ICP-PECVD at 75°C. (b) Photolithography process (spin coating of AZ 3012, exposure, development) according to Mask 2 (Figure 3.19). (c) Etching of SiN by 8 s of RIE using $C_4F_8$ and $CH_4$. (d) Stripping of PR in acetone for 45 min.

Although the photoresist was not completely removed, as shown in Figure 4.25, the $SiO_2$-only sample was still used to continue the fabrication process, focusing on the optimization of SiN deposition and patterning.

As shown in Figure 4.26(a), 30 nm of SiN were deposited by ICP-PECVD using the Oxford Instruments PlasmaPro100 at the Kavli Nanolab. The deposition was performed at 75 °C with a gas mixture of silane $SiH_4$ (26 sccm) and nitrogen $N_2$ (25 sccm), at 500 W and 2 mTorr. With a deposition rate of 44.6 nm/min, only 40 s were required to achieve the target thickness.

A second lithography step was then carried out to pattern the SiN film (Figure 4.26(b)) according to Mask 2 (Figure 3.19), leaving only a circular area to define the dielectric interlayer of the parallel-plate matching capacitor. This process followed the same procedure described in Section 4.5, using AZ 3012 photoresist.

The thin SiN film was subsequently etched by RIE for 8 s in the Alcatel AMS110 at EKL, as shown in Figure 4.26(c). The selected recipe employed $C_4F_8$ (17 sccm), $CH_4$ (18 sccm), and He (150 sccm) at 2800 W. This short etch step immediately revealed the underlying bluish $SiO_2$.



(a)

(b)

Figure 4.27: Microscope inspection of SiN processing. (a) After photoresist mask fabrication. (b) After 8 s RIE of SiN.

Finally, the figure above, shown at 5x magnification, highlights the resist mask used to pattern SiN (Figure 4.27(a)) and the resulting structure after 8 s of SiN RIE (Figure 4.27(b)). This step concludes the practical fabrication and optimization work that could be carried out in the laboratory during the research period at TU Delft.

Although the complete fabrication of the biodegradable WPT LC coil could not be finalized within the available laboratory time, the work established a reliable pathway for building and patterning a biodegradable thin-film stack of dextran/PLA/$SiO_2$/Mo, on which the final device can realistically be completed. The process flow enabled reproducible deposition of each layer under low-thermal-budget conditions and demonstrated clean Mo pattern transfer across the different substrates investigated, despite the constraints imposed by biodegradable polymers. Once the stack's compatibility is established, the development bottleneck moves from materials validation to process integration, thereby reducing the risk associated with completing the LC coil fabrication.

Beyond the immediate fabrication results, the cleanroom activities clarified two key enduring lessons. First, mechanical and thermal stress management is essential when combining rigid inorganic materials with soft biodegradable polymers; staged depositions and controlled cooling proved more effective than single, high-throughput runs. Second, chemistry and temperature choices must be optimized for the entire stack, favoring gentler bakes, alternative solvents, and low-damage patterning to preserve film integrity. Collectively, these results deliver a practical recipe set for transient electronics stacks and provide a solid foundation for future work.

# Conclusion and Future Perspectives

Sustainability and end-of-life management have emerged as key requirements in modern remote sensing and Internet-of-Things (IoT) devices, especially in precision agriculture (PA), where today's battery-powered, non-biodegradable systems limit sensor density, require retrieval, and accumulate as electronic waste. A CMOS-compatible, fully biodegradable platform powered through wireless power transfer (WPT) can remove batteries, improve autonomy, and enable dense, disposable deployments. The thesis objective is therefore to establish a photolithography-based method to fabricate a biodegradable WPT device that is compatible with standard microfabrication for future CMOS integration.

Based on a comparative review of suitable biodegradable materials for thin film processing, polylactic acid (PLA) was selected as substrate, silicon oxide ($SiO_2$) and silicon nitride ($Si_3N_4$) as insulators/dielectrics, and molybdenum (Mo) for conductors, with dextran as the initial sacrificial layer. This choice balances biodegradability with processability, acknowledging the low thermal budget of biodegradable polymers and the higher resistivity of biodegradable metals such as Mo.

The WPT device is a thin-film receiving antenna - a spiral LC coil for NFC operation at 6.78 MHz - with an overall footprint of $\approx$ 2.8 x 2.8 cm. The Rx coil was designed to match the resonant frequency of a transmitter developed by Tianqi Lu (EI section, Delft University of Technology). The rover-mounted transmitter scans agricultural fields and inductively powers the Rx LC coil, which then provides the supply voltage to the biodegradable sensor nodes deployed in the soil, at an average distance of $\approx$ 10 cm. The link is designed to harvest sufficient power with an estimated $\approx 28\%$ power transfer efficiency (PTE), good for low-power sensing (1-50 mW). Main design limitations arise from Mo's high resistivity (120 nm $\Omega$) and the low metal thickness (500 nm) compared with conventional non-biodegradable implementations ($\geq$ 10 $\mu$m).

A complete LC-coil process flow was defined around standard cleanroom steps - spin coating, Inductively Coupled Plasma-PECVD, sputtering, photolithography, Reactive Ion Etching (RIE), and lift-off - to be carried out in Else Kooi Laboratory and Kavli Nanolab at TU Delft, constrained by biodegradable substrates: low-temperature processes near PLA's glass temperature $T_g \approx 65$ °C, solvent compatibility, adhesion management, and stress control across the polymer/inorganic interfaces. These factors influenced the mask and layer sequencing.

Cleanroom work partially optimized the flow and demonstrated a feasible dextran/ PLA/$SiO_2$/Mo stack with reliable Mo pattern transfer on multiple substrates (PLA, dextran+PLA, dextran, $SiO_2$). Key optimizations included staged, low-stress $SiO_2$ deposition and stress-aware Mo sputtering to mitigate cracking on PLA near $T_g$, alongside a validated photolithography/RIE process for Mo. This process represents a reproducible foundation on which to complete the WPT device fabrication, and subsequently integrate it with a CMOS rectifier IC.

Immediate future work should finalize the LC coil on the validated stack and integrate a CMOS front-end for AC-to-DC conversion (and, potentially, communication and data transfer), yielding a fully functional biodegradable system. Furthermore, to alleviate PLA-related limitations, the process flow can be re-sequenced by depositing PLA last, preserving the device while maintaining the rest of the process unchanged, with an initial dextran sacrificial layer to then release the device. Process flowcharts for both improvements are provided in the Appendix. These developments enable the fabrication a fully biodegradable CMOS-based WPT platform for dense, retrieval-free deployments in precision agriculture.

# List of Abbreviations

**IoT** Internet of Things.

**PA** Precision Agriculture.

**WPT** Wireless Power Transfer.

**CMOS** Complementary Metal-Oxide-Semiconductor.

**NFC** Near-Field Communication.

**Rx** Receiver.

**Tx** Transmitter.

**PLA** Polylactic Acid.

**Mo** Molybdenum.

**$SiO_2$** Silicon Dioxide.

**$Si_3N_4$** Silicon Nitride.

**LC** Inductor-Capacitor.

**PTE** Power Transfer Efficiency.

**PCE** Power Conversion Efficiency.

**VCR** Voltage Conversion Ratio.

**IC** Integrated Circuit.

**DOVD** Dual-Output Regulating Voltage Doubler.

**EKL** Else Kooi Laboratory.

**PR** Photoresist.

**RIE** Reactive Ion Etching.

**DRIE** Deep Reactive Ion Etching.

**PVD** Chemical Vapor Deposition.

**ICP-PECVD** Inductively Coupled Plasma - Plasma-Enhanced CVD.

**RIE** Reactive Ion Etching.

**PVD** Physical Vapor Deposition.

**HMDS** Hexamethyldisilazane.

**BHF** Buffered Hydrofluoric Acid.

**CTE** Coefficient of Thermal Expansion.

**HBSS** Hanks' Balanced Salt Solution.

**PBS** Phosphate-Buffered Saline.

**Sccm** Standard Cubic Centimeters per Minute.

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A.2 Process flow of a biodegradable LC coil with PLA at the end. (1) $O_2$ plasma surface treatment. (2) Spin coating of Dextran (sacrificial layer). (3) Deposition of $SiO_2$ by ICP-PECVD. (4) Sputtering of Mo. (5) Spin coating of photoresist (PR). (6) Exposure and development of PR. (7) Reactive ion etching (RIE) of Mo. (8) Stripping of PR. (9) Deposition of $Si_3O_4$ by ICP-PECVD. (10) Spin coating of PR. (11) Exposure and development of PR. (12) RIE of $Si_3O_4$. (13) Stripping of PR. (14) Deposition of $SiO_2$ by ICP-PECVD. (15) Spin coating of PR. (16) Exposure and development of PR. (17) Wet etching of $SiO_2$. (18) Stripping of PR. (19) Spin coating of PR. (20) Exposure and development of PR. (21) Sputtering of Mo. (22) Lift-off of Mo. (23) Spin coating of PLA. (24) Deposition of $SiO_2$ by ICP-PECVD. (25) Spin coating of PR. (26) Exposure and development of PR. (27) RIE of $SiO_2$. (28) Stripping of PR. (29) RIE of PLA. (30) Removal of $SiO_2$. (31) Device release by dissolving dextran in water. . . . . . . . . . . . . . . . . . . . . . . . . . 110

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# Appendix

This appendix illustrates the two flowcharts mentioned in the conclusion as possible future developments for this project. First, the full flowchart for the fabrication of a fully biodegradable system integrating a WPT device and a CMOS IC rectifier is proposed in Figure A.1. It is basically divided into:

1. **CMOS IC transfer** into a Si carrier wafer. Figure A.1 (step 1-8)
2. **PLA substrate spin coating** to fix the CMOS IC. Figure A.1 (step 9-16)
3. **Bottom metal layer** by sputtering and patterning of Mo. Figure A.1 (step 17-21)
4. **Silicon nitride dielectric film formation** by ICP-PECVD deposition and patterning. Figure A.1 (step 22-26)
5. **Silicon oxide insulating layer formation** by ICP-PECVE deposition and patterning. Figure A.1 (step 27-31)
6. **Top metal layer** by lift-off of Mo + **Backside thinning**. Figure A.1 (step 32-36)

In addition, a second alternative flowchart is shown in Figure A.2, where PLA is deposited as the final step. The sequence mirrors the process in Chapter 3, except that only dextran is spin-coated initially as a sacrificial layer. Microfabrication proceeds to define the LC coil; PLA is then spin-coated as the encapsulant and patterned using a silicon-oxide hard mask with oxygen plasma to open windows over the output pads for sensor interconnection. Finally, the device is released by dissolving the dextran in water.

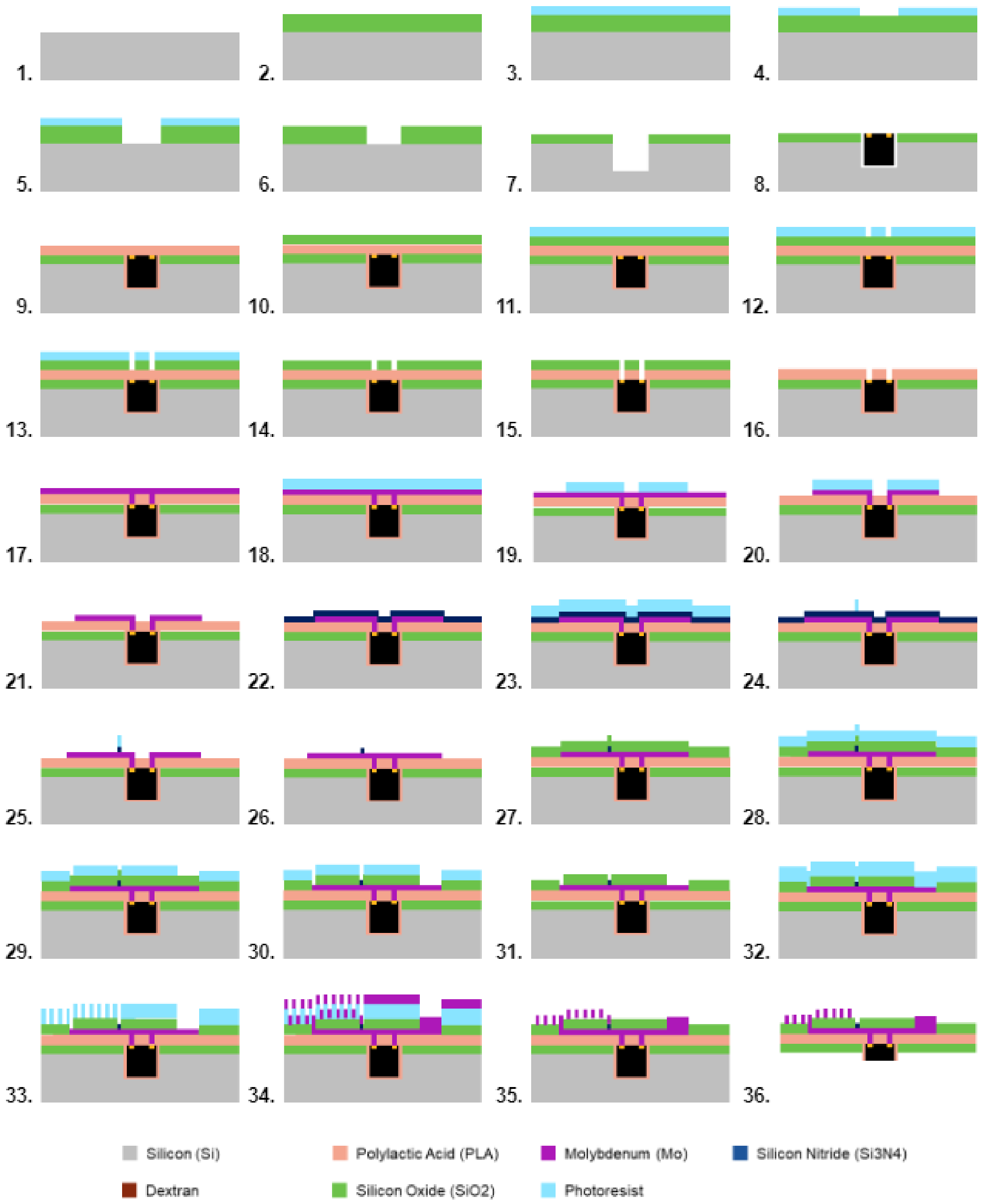
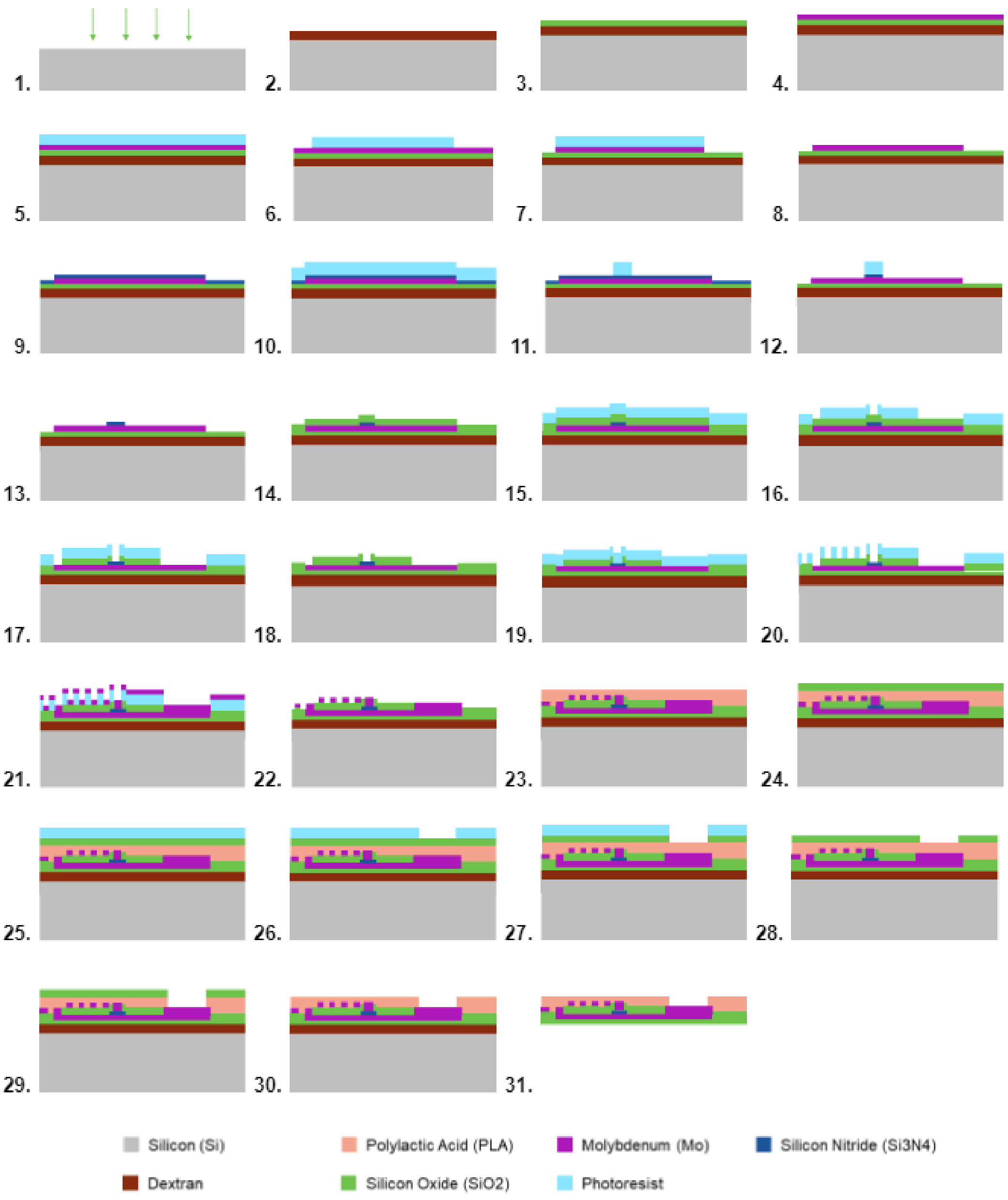


Figure A.1: Process flow of a biodegradable LC coil integrated with a CMOS rectifier. (1) Si carrier wafer. (2) $SiO_2$ deposition. (3) Spin coating of PR. (4) Patterning of PR. (5) RIE of $SiO_2$. (6) Stripping of PR. (7) DRIE of Si. (8) Placement of CMOS IC. (9) Spin coating of PLA. (10) $SiO_2$ ICP-PECVD. (11) Spin coating of PR. (12) Patterning of PR. (13) RIE of $SiO_2$. (14) Stripping of PR. (15) RIE of PLA. (16) Removal of $SiO_2$. (17) Sputtering of Mo. (18) Spin coating of PR. (19) Patterning of PR. (20) RIE of Mo. (21) Stripping of PR. (22) $Si_3N_4$ ICP-PECVD. (23) Spin coating of PR. (24) Patterning of PR. (25) RIE of $Si_3N_4$. (26) Stripping of PR. (27) $SiO_2$ ICP-PECVD. (28) Spin coating of PR. (29) Patterning of PR. (30) Wet etching of $SiO_2$. (31) Stripping of PR. (32) Spin coating of PR. (33) Patterning of PR. (34) Sputtering of Mo. (35) Lift-off. (36) Backside thinning.



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# References

[1] JinKi Min, Yeongju Jung, Jiyong Ahn, Jae Gun Lee, Jinwoo Lee, and Seung Hwan Ko. “Recent advances in biodegradable green electronic materials and sensor applications”. In: *Advanced Materials* 35.52 (2023), p. 2211273. DOI: `10.1002/adma.202211273`.

[2] Wenhui Li, Qian Liu, Yuniu Zhang, Chang’an Li, Zhenfei He, Wallace CH Choy, Paul J Low, Prashant Sonar, and Aung Ko Ko Kyaw. “Biodegradable materials and green processing for green electronics”. In: *Advanced materials* 32.33 (2020), p. 2001591. DOI: `10.1002/adma.202001591`.

[3] Amir Zahedi, Ranjith Liyanapathirana, and Karthick Thiyagarajan. “Biodegradable and Renewable Antennas for Green IoT Sensors: A Review”. In: *IEEE Access* (2024). DOI: `10.1109/ACCESS.2024.3515274`.

[4] Michele De Santis and Ilaria Cacciotti. “Wireless implantable and biodegradable sensors for postsurgery monitoring: current status and future perspectives”. In: *Nanotechnology* 31.25 (2020), p. 252001. DOI: `10.1088/1361-6528/ab7a2d`.

[5] Seungwon Yoo, Jonghun Lee, Hyunwoo Joo, Sung-Hyuk Sunwoo, Sanghoek Kim, and Dae-Hyeong Kim. “Wireless power transfer and telemetry for implantable bioelectronics”. In: *Advanced healthcare materials* 10.17 (2021), p. 2100614. DOI: `10.1002/adhm.202100614`.

[6] Yamin Zhang, Geumbee Lee, Shuo Li, Ziying Hu, Kaiyu Zhao, and John A Rogers. “Advances in bioresorbable materials and electronics”. In: *Chemical Reviews* 123.19 (2023), pp. 11722–11773. DOI: `10.1021/acs.chemrev.2c00923`.

[7] Rahul Singh, Mohammad Javad Bathaei, Emin Istif, and Levent Beker. “A review of bioresorbable implantable medical devices: Materials, fabrication, and implementation”. In: *Advanced Healthcare Materials* 9.18 (2020), p. 2000790. DOI: `10.1002/adhm.202000790`.

[8] Minh Thuy Le, Chi Dat Pham, Thi Phuong Thao Nguyen, Thanh Long Nguyen, Quoc Cuong Nguyen, Ngoc Bich Hoang, and Long D Nghiem. “Wireless powered moisture sensors for smart agriculture and pollution prevention: Opportunities, challenges, and future outlook”. In: *Current Pollution Reports* 9.4 (2023), pp. 646–659. DOI: `10.1007/s40726-023-00276-8`.

[9] Rongfeng Li, Liu Wang, Deying Kong, and Lan Yin. "Recent progress on biodegradable materials and transient electronics". In: *Bioactive materials* 3.3 (2018), pp. 322–333. DOI: `10.1016/j.bioactmat.2017.12.001`.

[10] Zhiqiang Zhai, Xiaosong Du, Yin Long, and Heng Zheng. "Biodegradable polymeric materials for flexible and degradable electronics". In: *Frontiers in Electronics* 3 (2022), p. 985681. DOI: `10.3389/felec.2022.985681`.

[11] Wei-Chen Huang, Wan-Lou Lei, and Chih-Wei Peng. "Fabrication of Biodegradable Soft Tissue-Mimicked Microelectrode Arrays for Implanted Neural Interfacing". In: *2023 IEEE 36th International Conference on Micro Electro Mechanical Systems (MEMS)*. IEEE. 2023, pp. 392–395. DOI: `10.1109/MEMS48254.2023.10044329`.

[12] Rakiba Rayhana, Gaozhi George Xiao, and Zheng Liu. "Printed sensor technologies for monitoring applications in smart farming: A review". In: *IEEE Transactions on Instrumentation and Measurement* 70 (2021), pp. 1–19. DOI: `10.1109/TIM.2020.3038795`.

[13] Steffen Kurth, Sven Voigt, Ralf Zichner, Frank Roscher, Perez Weigel, and Toni Großmann. "Technologies for biodegradable wireless plant monitoring sensors". In: *2021 Smart Systems Integration (SSI)*. IEEE. 2021, pp. 1–4. DOI: `10.1109/SSI52265.2021.9424240`.

[14] Bill Yen and Zerina Kapetanovic. "Towards Designing Self-Powered Biodegradable Sensors For Agricultural Applications". In: *Proceedings of the 2nd Workshop on Advances in Environmental Sensing Systems for Smart Cities*. 2024, pp. 19–24. DOI: `10.1145/3661813.3661818`.

[15] Yongkun Sui, Madhur Atreya, Subash Dahal, Anupam Gopalakrishnan, Rajiv Khosla, and Gregory L Whiting. "Controlled biodegradation of an additively fabricated capacitive soil moisture sensor". In: *ACS Sustainable Chemistry & Engineering* 9.6 (2021), pp. 2486–2495. DOI: `10.1021/acssuschemeng.0c08357`.

[16] Muhammad Zain, Haijiao Ma, Shafeeq Ur Rahman, Md Nuruzzaman, Sadaf Chaudhary, Imran Azeem, Faisal Mehmood, Aiwang Duan, and Chengming Sun. "Nanotechnology in precision agriculture: advancing towards sustainable crop production". In: *Plant Physiology and Biochemistry* 206 (2024), p. 108244. DOI: `10.1016/j.plaphy.2024.108244`.

[17] Takaaki Kasuga, Ami Mizui, Hirotaka Koga, and Masaya Nogi. "Wirelessly Powered Sensing Fertilizer for Precision and Sustainable Agriculture". In: *Advanced Sustainable Systems* 8.1 (2024), p. 2300314. DOI: `10.1002/adsu.202300314`.

[18] Ken Sakabe, Tetsuo Kan, and Hiroaki Onoe. "Entirely Biodegradable Wireless pH Sensor with Split-Ring Resonators for Soil pH Monitoring". In: *Advanced Materials Technologies* 9.13 (2024), p. 2400038. DOI: `10.1002/admt.202400038`.

[19] Anne-Marie Zaccarin, Naimisha Peddada, Michael Machold, Kevin T Turner, and Roy H Olsson III. “Inductively Coupled Capacitive Soil Moisture Sensors Printed on a Biodegradable Substrate: Characterization and Long-term Testing”. In: *Smart Agricultural Technology* (2025), p. 101052. DOI: `10.1016/j.atech.2025.101052`.

[20] Sarath Gopalakrishnan, Jose Waimin, Amin Zareei, Sotoudeh Sedaghat, Nithin Raghunathan, Ali Shakouri, and Rahim Rahimi. “A biodegradable chipless sensor for wireless subsoil health monitoring”. In: *Scientific reports* 12.1 (2022), p. 8011. DOI: `10.1038/s41598-022-12018-0`.

[21] Mohammad Javad Bathaei, Rahul Singh, Hadi Mirzajani, Emin Istif, Muhammad Junaid Akhtar, Taher Abbasiasl, and Levent Beker. “Photolithography-based microfabrication of biodegradable flexible and stretchable sensors”. In: *Advanced Materials* 35.6 (2023), p. 2207081. DOI: `10.1002/adma.202207081`.

[22] S Sreejith, LMI Leo Joseph, Sreedhar Kollem, VT Vijumon, and J Ajayan. “Biodegradable sensors: A comprehensive review”. In: *Measurement* 219 (2023), p. 113261. DOI: `10.1016/j.measurement.2023.113261`.

[23] SM Meshram, Soham Adla, Ludovic Jourdin, and Saket Pande. “Review of low-cost, off-grid, biodegradable in situ autonomous soil moisture sensing systems”. In: *Computers and Electronics in Agriculture* 225 (2024), p. 109289. DOI: `10.1016/j.compag.2024.109289`.

[24] Bo Xia, Yan Liu, Yangkun Xing, Zhewei Shi, and Xiaocheng Pang. “Biodegradable Medical Implants: Reshaping Future Medical Practice”. In: *Advanced Science* (2025), e08014. DOI: `10.1002/advs.202408014`.

[25] Hamed Rahmani, Darshan Shetty, Mahmoud Wagih, Yasaman Ghasempour, Valentina Palazzi, Nuno B Carvalho, Ricardo Correia, Alessandra Costanzo, Dieff Vital, Federico Alimenti, et al. “Next-generation IoT devices: Sustainable eco-friendly manufacturing, energy harvesting, and wireless connectivity”. In: *IEEE Journal of Microwaves* 3.1 (2023), pp. 237–255. DOI: `10.1109/JMW.2022.3228353`.

[26] Xianglong Bai, Yan Lu, Chenchang Zhan, and Rui P Martins. “A 6.78-MHz wireless power transfer system with inherent wireless phase shift control without feedback data sensing coil”. In: *IEEE Journal of Solid-State Circuits* 58.6 (2022), pp. 1746–1757. DOI: `10.1109/JSSC.2022.3228101`.

[27] Dipon K Biswas, Nabanita Saha, Arnav Kaul, and Ifana Mahbub. “Semi-implantable wireless power transfer (WPT) system integrated with on-chip power management unit (PMU) for neuromodulation application”. In: *IEEE Journal of Electromagnetics, RF and Microwaves in Medicine and Biology* 7.2 (2023), pp. 193–200. DOI: `10.1109/JERM.2022.3193976`.

[28] Dominik Huwig and Peter Wambsganß. "Digitally controlled synchronous bridge-rectifier for wireless power receivers". In: *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE. 2013, pp. 2598–2603. DOI: `10.1109/APEC.2013.6520672`.

[29] Andreas Berger, Matteo Agostinelli, Christoph Sandner, Sanna Vesti, and Mario Huemer. "High efficient integrated power receiver for a Qi compliant wireless power transfer system". In: *2016 ieee wireless power transfer conference (wptc)*. IEEE. 2016, pp. 1–4. DOI: `10.1109/WPT.2016.7498816`.

[30] Byeongseol Kim and Joonsung Bae. "A 86%-efficiency CMOS rectifier with an internal threshold voltage cancellation (IVC) scheme". In: *Electronics Letters* 58.11 (2022), pp. 417–419. DOI: `10.1049/ell2.12481`.

[31] Sung Min Seo, Jun Ho Cheon, Seok Hyang Kim, Tae June Kang, Jung Woo Ko, In-Young Chung, Yong Hyup Kim, and Young June Park. "Carbon nanotube-based CMOS gas sensor IC: Monolithic integration of pd decorated carbon nanotube network on a CMOS chip and its hydrogen sensing". In: *IEEE transactions on electron devices* 58.10 (2011), pp. 3604–3608. DOI: `10.1109/TED.2011.2164249`.

[32] Fangming Deng, Yigang He, Bing Li, Lei Zuo, Xiang Wu, and Zhihui Fu. "A CMOS pressure sensor tag chip for passive wireless applications". In: *Sensors* 15.3 (2015), pp. 6872–6884. DOI: `10.3390/s150306872`.

[33] Nasir A Quadir, Mansour Taghadosi, Lutfi Albasha, and Nasser Qaddoumi. "Design of self powered chip integrated humidity sensor". In: *2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS)*. IEEE. 2016, pp. 1–4. DOI: `10.1109/MWSCAS.2016.7870132`.

[34] Meysam Zargham and P Glenn Gulak. "Fully Integrated On-Chip Coil in 0.13 um CMOS for Wireless Power Transfer Through Biological Media". In: *IEEE transactions on biomedical circuits and systems* 9.2 (2014), pp. 259–271. DOI: `10.1109/TBCAS.2014.2328318`.

[35] Shanthala Lakshminarayana, Hyusim Park, and Sungyong Jung. "Emerging Technologies in CMOS Integrated Sensing System-On-Chip: A Review". In: *IEEE Sensors Reviews* (2025). DOI: `10.1109/SR.2025.3498705`.

[36] Salihuojia Talanti, Kerui Fu, Xiaolong Zheng, Youzhi Shi, Yimei Tan, Chenxi Liu, Yanfei Liu, Ge Mu, Qun Hao, Kangkang Weng, and Xin Tang. "CMOS-integrated organic neuromorphic imagers for high-resolution dual-modal imaging". In: *Nature Communications* 16.4311 (2025). DOI: `10.1038/s41467-025-59446-2`.

[37] Shanthala Lakshminarayana, Hyusim Park, and Sungyong Jung. "Emerging technologies in CMOS integrated sensing system-on-chip: A review". In: *IEEE Sensors Reports* 2 (2025), pp. 397–413. DOI: `10.1109/SR.2025.3592654`.

[38] Kenji Okabe, Horagodage Prabhath Jeewan, Shota Yamagiwa, Takeshi Kawano, Makoto Ishida, and Ippei Akita. "Co-design method and wafer-level packaging technique of thin-film flexible antenna and silicon CMOS rectifier chips for wireless-powered neural interface systems". In: *Sensors* 15.12 (2015), pp. 31821–31832. DOI: `10.3390/s151229866`.

[39] Thomas Stieglitz, Calogero Gueli, Julien Martens, Niklas Floto, Max Eickenscheidt, Markus Sporer, and Maurits Ortmanns. "Highly conformable chip-in-foil implants for neural applications". In: *Microsystems & Nanoengineering* 9.54 (2023). DOI: `10.1038/s41378-023-00527-x`.

[40] Kaveti Rajaram, Seung Min Yang, and Suk-Won Hwang. "Transient, biodegradable energy systems as a promising power solution for ecofriendly and implantable electronics". In: *Advanced Energy and Sustainability Research* 3.9 (2022), p. 2100223. DOI: `10.1002/aesr.202100223`.

[41] Stephen Beeby, Sasikumar Arumugam, Nicholas Hillier, Yi Li, Junjie Shi, Yixuan Sun, Mahmoud Wagih, and Sheng Yong. "Power supply sources for smart textiles". In: *Smart clothes and wearable technology.* Elsevier, 2023, pp. 211–236. DOI: `10.1016/B978-0-12-819780-1.00010-4`.

[42] Poonam Lathiya and Jing Wang. "Near-Field Communications (NFC) for Wireless Power Transfer (WPT): An Overview". In: *Wireless Power Transfer.* Ed. by Mohamed Zellagui. Rijeka: IntechOpen, 2021. Chap. 6. DOI: `10.5772/intechopen.96345`. URL: `https://doi.org/10.5772/intechopen.96345`.

[43] Mauro Feliziani, Tommaso Campi, Silvano Cruciani, and Francesca Maradei. *Wireless Power Transfer for e-Mobility: Fundamentals and Design Guidelines for Wireless Charging of Electric Vehicles.* Cambridge, MA: Academic Press, 2023. ISBN: 978-0-323-99523-8. DOI: `10.1016/C2021-0-01579-0`. URL: `https://doi.org/10.1016/C2021-0-01579-0`.

[44] Stefano Lovati. *Considerazioni di design per un'antenna NFC.* `https://it.emcelettronica.com/considerazioni-di-design-per-unantenna-nfc`. Elettronica Open Source. Apr. 2020.

[45] *PN7160 Antenna Design and Matching Guide.* Application note AN13219. Version Rev. 1.5. NXP Semiconductors. URL: `https://www.nxp.com/docs/en/application-note/AN13219.pdf`.

[46] *How to design a 13.56 MHz customized antenna for ST25 NFC / RFID Tags.* Application Note AN2866. Rev. 5. [Online]. Available: `https://www.st.com/resource/en/application_note/an2866-how-to-design-a-1356-mhz-customized-antenna-for-st25-nfc--rfid-tags-stmicroelectronics.pdf`. STMicroelectronics, Aug. 2021.

[47] Tianqi Lu, Kofi AA Makinwa, and Sijun Du. "A single-stage dual-output regulating voltage doubler for wireless power transfer". In: *IEEE Journal of Solid-State Circuits* 59.9 (2024), pp. 2922–2933. DOI: `10.1109/JSSC.2024.3378675`.

[48] Kavin Sivaneri Varadharajan Idhaiam, Joshua A Caswell, Peter D Pozo, Katarzyna Sabolsky, Konstantinos A Sierros, Daryl S Reynolds, and Edward M Sabolsky. "All-ceramic passive wireless temperature sensor realized by tin-doped indium oxide (ITO) electrodes for harsh environment applications". In: *Sensors* 22.6 (2022), p. 2165. DOI: `10.3390/s22062165`.

[49] Wireless Power Consortium. *Coupling Factor — Knowledge Base.* `https://www.wirelesspowerconsortium.com/knowledge-base/magnetic-induction/coupling-factor/`.

[50] T. Havinga. "Characterization of DC-Sputtered Thin Molybdenum Films". Work carried out at Else Kooi Lab (EKL), Delft University of Technology. Bachelor's thesis. The Hague, The Netherlands: The Hague University of Applied Sciences, 2023.

[51] ThoughtCo. *Table of Electrical Resistivity & Conductivity.* `https://www.thoughtco.com/table-of-electrical-resistivity-conductivity-608499`.

[52] Tomas Picha, Stanislava Papezova, and Stepan Picha. "Evaluation of relative permittivity and loss factor of 3D printing materials for use in RF electronic applications". In: *Processes* 10.9 (2022), p. 1881. DOI: `10.3390/pr10091881`.

[53] O. F. Rocha, R. B. Torres, N. Peco, and J. A. de Souza. "Electrical characteristics of PECVD silicon oxide deposited with low TEOS contents at low temperatures". In: *Proceedings of the Electrochemical Society.* Vol. 3. 2004, pp. 295–300. DOI: `10.1149/200406.0295PV`.

[54] Hamood Ur Rahman, Angus Gentle, Eric Gauja, and Rodica Ramer. "Characterisation of dielectric properties of PECVD Silicon Nitride for RF MEMS applications". In: *2008 IEEE International Multitopic Conference.* IEEE. 2008, pp. 91–96. DOI: `10.1109/INMIC.2008.4777704`.

[55] inductiveload. *Parallel Plate Capacitor.* Graphic image (SVG). Public domain. File: Parallel_plate_capacitor.svg, Wikimedia Commons. 2006. URL: `https://commons.wikimedia.org/wiki/File:Parallel_plate_capacitor.svg`.

[56] Carl Hepburn. *Semiconductor Fabrication: Photolithography.* `https://britneyspears.ac/physics/fabrication/photolithography.htm`.

[57] Keyence Corporation. *Spin Coating — Coating & Dispensing Methods — Keyence.* `https://www.keyence.com/ss/products/measure/sealing/coater-type/spin.jsp`. n.d.

[58] Yong Seung Kim, Jae Hong Lee, Sahng-Kyoon Jerng, Eunho Kim, Sunae Seo, J Jung, SH Chun, Y Seung, and J Hong. “H 2-free synthesis of monolayer graphene with controllable grain size by plasma enhanced chemical vapor deposition”. In: *Nanoscale* 5.1221 (2013), pp. 10–1039. DOI: `10.1039/C3NR05214G`.

[59] Alice Lee. *Wet Etching vs. Dry Etching: Key Differences Explained.* `https://www.globalwellpcba.com/wet-etching-vs-dry-etching/`. 2025.

[60] Daniel Berkoh and Sarang Kulkarni. “Challenges in lift-off process using CAMP negative photoresist in III–V IC fabrication”. In: *IEEE Transactions on Semiconductor Manufacturing* 32.4 (2019), pp. 513–517. DOI: `10.1109/TSM.2019.2930746`.

[61] Stanisław Kuciel, Karolina Mazur, and Marek Hebda. “The influence of wood and basalt fibres on mechanical, thermal and hydrothermal properties of PLA composites”. In: *Journal of Polymers and the Environment* 28.4 (2020), pp. 1204–1215. DOI: `10.1007/s10924-020-01674-w`.

[62] Seas3D. *PLA Technical Data Sheet (Polylactic Acid).* `https://www.seas3d.com/MaterialTDS-PLA.pdf`. n.d.

[63] Shih-Shian Ho, Srihari Rajgopal, and Mehran Mehregany. “Thick PECVD silicon dioxide films for MEMS devices”. In: *Sensors and Actuators A: Physical* 240 (2016), pp. 1–9. DOI: `10.1016/j.sna.2016.01.004`.

[64] T Ye, Z Suo, and AG Evans. “Thin film cracking and the roles of substrate and interface”. In: *International Journal of Solids and Structures* 29.21 (1992), pp. 2639–2648. DOI: `10.1016/0020-7683(92)90159-J`.

[65] Neal Wostbrock and Tito Busani. “Stress and refractive index control of SiO2 thin films for suspended waveguides”. In: *Nanomaterials* 10.11 (2020), p. 2105. DOI: `10.3390/nano10112105`.

[66] Günter Reiter, Farzad Ramezani, and Jörg Baschnagel. “The memory of thin polymer films generated by spin coating”. In: *The European Physical Journal E* 45.5 (2022), p. 51. DOI: `10.1140/epje/s10189-022-00188-6`.

[67] Joost J Vlassak. “Channel cracking in thin films on substrates of finite thickness”. In: *International Journal of Fracture* 119.4 (2003), pp. 299–323. DOI: `10.1023/A:1026020425748`.

[68] Gregory Abadias, E Chason, J Keckes, M Sebastiani, GB Thompson, E Barthel, GL Doll, CE Murray, CH Stoessel, and L Martinu. “Review Article: Stress in Thin Film s and Coatings: Current Status”. In: *Challenges, and Prospects* (2018). DOI: `10.1116/1.5011790`.

[69] Merck Performance Materials GmbH. *AZ ECI 3012 Photoresist Technical Data Sheet.* `https://www.microchemicals.com/dokumente/datenblaetter/tds/merck/en/tds_az_eci_3012_photoresist.pdf`. n.d.

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