POLITECNICO DI TORINO

MASTER's Degree in Electronic Engineering

MASTER's Degree Thesis

Characterization of Digital Control Strategies for a 50W Capacitively Isolated DC-DC Converter

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Abstract

This thesis focuses on the characterization of a capacitively isolated DC-DC converter with a control loop for output voltage regulation. Previous research on this technology developed a converter using two interface capacitors for galvanic isolation with a single inductor as compensation network. The Multi Period Damped Resonant (MDPR) mode is exploited [2], where the frequency range is selected, below the resonant frequency, to avoid the complete damping of the resonant current. This is a necessary condition to achieve the ZVS of the half-bridge transistors. Further study was carried out to find an optimum solution for voltage regulation in this technology. The study proposed four control strategies namely - Frequency Modulation (FM), Pulse Width Modulation (PWM), Bang-bang (BB) control and Dyadic Digital Pulse Modulation (DDPM) which were modelled and simulated.

This work focuses on the practical implementation of the previously analyzed and developed control strategies using an ST Microelectronic development board. Each control strategy is implemented using the development board user interface. The converter prototype board behavior is analyzed and characterized in open loop for the range of operation confirming the saturation limits of the system. Later, the prototype board is verified for closed loop operations to draw a comparison between the effects of different control strategies on the converter in terms of efficiency, soft switching and voltage ripple.

Acknowledgement

To my sister, Ananya - my constant.

To my parents, my love and gratitude go out to you for supporting my dreams and aspirations unconditionally. To Naveen, I am always grateful that you are in my life.

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Chapter 1

Introduction

The continuous demand for compact, efficient, and high efficiency power supplies have driven the evolution of DC–DC converter topologies. These converters play an important role in modern power electronics, enabling voltage adaptation, isolation, and energy optimization for a variety of applications, like consumer electronics, renewable systems and electric vehicles. The demand for a more compact, high efficiency, high power density power adapters with a large voltage gain has thus emerged in recent times.

In a typical grid adapter, the complete power conversion chain involves both AC-DC and DC-DC stages. The input from the utility grid, an AC voltage (230VAC or 110VAC) is first rectified to produce a high-voltage DC bus, which then serves as the input for the isolated DC-DC converter stage. This rectification can be implemented using a diode bridge rectifier for low-power applications, or more efficiently through an active Power Factor Correction (PFC) stage, which shapes the input current to follow the mains voltage and ensures compliance with international harmonic standards such as IEC 61000-3-2 [2], [4], [5]. The DC bus voltage after rectification typically ranges from 325V to 400V, depending on the grid voltage and PFC topology [6], [7].

Several converter topologies, advanced from the traditional non-isolated and isolated topologies have been proposed to meet these requirements but they lack in either simplicity of the control circuit or have to compromise the voltage gain achieved leading to poor efficiency. Conventional isolated flyback-derived solutions can meet the requirement, but they pay for it with high device stress and hard switching, often needing auxiliary snubbers or clamp networks that dilute efficiency and increase part count. Classical isolation topologies tend to rely on dual-sided compensation networks in which the resulting resonant frequency is sensitive to component tolerances which complicates control and makes reproducibility difficult. The Capacitive galvanic isolation has emerged as a credible solution in compact converters. This enables a lighter and more compact design while inherently reducing Electromagnetic Interference (EMI).

Building on the resonant converters, a previous work has introduced a step-down capacitively isolated grid adapter that achieves isolation with two interface capacitors and uses a single compensation inductor, reducing the passive component count while safeguarding power density. This proposed converter architecture operates in the Multi-

Period Damped Resonant (MPDR) mode, which exploits damped resonant cycles to achieve Zero Voltage Switching resulting in smaller passive components and limited switching losses. Building on this hardware, a research on closed-loop control strategies tailored to MPDR behavior was developed and analyzed, comparing them for efficiency, soft-switching windows, and output ripple in simulation. By implementing the controllers and validating experimentally their performances, this thesis goes one step further. The control architecture for the voltage regulation uses four control strategies, Frequency Modulation (FM), Pulse-Width Modulation (PWM), Bang-Bang (BB), and Dyadic Digital Pulse Modulation (DDPM), that are implemented using the STM32 development board.

1.1 Scope and Thesis Objectives

The scope of this thesis is centered on the implementation, control, and experimental validation of an isolated DC-DC converter employing capacitive isolation. The converter operates in Multi-Period Damped Resonant (MPDR) mode, a topology designed to minimize passive component count while maintaining galvanic isolation through capacitive coupling.

The main objective of this thesis is to study the grid adapter converter topology and validate the operation of the control strategies that were designed in the previous work. The work proceeds in two phases, starting with the characterization of the prototype board specification in comparison to the design values. This involves the calibration of the sensing chain to establish an end-to-end gain and offset with uncertainty bounds. In the second phase, the four different control strategies are implemented and the system behavior is characterized in open loop and closed loop condition. During this phase, each controller is brought up, stabilized, and tested for saturation behavior in open-loop, efficiency and transient observation due load steps in closed-loop conditions. To complete the work, a conclusion is drawn by comparing the values obtained in the previous study and the values found during the experimental phase.

The tasks performed are:

a. The prototype board characterization- in order to read the output voltage value with accuracy. A gain is applied to the output voltage, which scales the output voltage to be in the range that is compliant to the acceptable range of the microcontroller. The gain provided by this section is characterized initially.
b. STM32 development board peripherals: ADC is configured to precisely read the output voltage, and the high resolution timer to produce accurate high and low gate signals to the GaN transistors.

c. Each control strategy is implemented using the STM32 C/C++ development platform (STM32Cube IDE).
d. Open loop characterization of the control strategies for low and high input voltages to understand the saturation load limits of the system for different control strategies.
e. Closed loop experiments to evaluate the system behavior in a load step condition based on the load range for each control strategy.

Chapter 2

State of the Art and Topology

The DC-DC power conversion state involves various converter topologies like buck, boost, buck-boost classified in the non-isolated type of converters and active clamp flyback, asymmetrical half-bridge, or resonant converters [1], [16]-[18] classified into the isolated type of converters. This stage is responsible for providing galvanic isolation and stepping down this high DC link to the required low-voltage output (20V) while maintaining regulation and efficiency. This modular structure, combining rectification and high-frequency isolated conversion, forms the basis of most modern AC-DC adapters for consumer electronics, industrial supplies, and wireless charging systems [4], [8].

Converters such as buck, boost, and buck-boost classified in the non-isolated topologies, are compact and efficient for low-voltage applications but lack galvanic isolation, limiting their use in grid-connected or safety-critical systems [1]. On the other hand, the isolated architectures such as flyback, forward, and half-bridge converters have long been the foundation of switched-mode power conversion, offering reliable galvanic isolation and flexible voltage regulation [3], [17]. These converters integrate a transformer or capacitive interface to provide electrical isolation between input and output stages. They are indispensable in power adapters, industrial drives, and wireless chargers [8], [9].

As modern electronic systems push for higher power density, faster transient response, and stricter efficiency targets, these conventional designs face increasing challenges related to switching losses, magnetic component size, and thermal management. The advent of Wide Bandgap (WBG) semiconductor devices particularly Gallium Nitride (GaN) and Silicon Carbide (SiC) transistors, has significantly reshaped this landscape [19], [21], [22]. Their superior electrical characteristics, including lower on-resistance, reduced output capacitance, and fast switching capability, enable converters to operate efficiently at megahertz-range frequencies. This advancement allows for substantial reduction in passive component size, paving the way for high-frequency, high-efficiency, and miniaturized power converters. To maximize the leverage of these benefits, research has shifted toward resonant and quasi-resonant topologies, which inherently support soft-switching conditions like Zero Voltage Switching (ZVS), thereby mitigating switching losses and electromagnetic interference [10]-[13].

This chapter reviews the evolution of converter topologies, focusing on the transition from hard-switched PWM converters to high-frequency resonant and capacitive-isolated architectures, highlighting their design principles, operational advantages, and relevance to modern high-density applications

2.1 The Isolated DC-DC Converters

The conventional isolated converter topologies such as flyback, forward, and half-bridge converters have evolved substantially due to the demand for higher power density and efficiency. The introduction of Wide Bandgap (WBG) devices like GaN transistors has enabled operation at higher switching frequencies, reducing passive component sizes while improving conversion efficiency.

2.1.1 Zero Voltage Switching (ZVS)

Zero Voltage Switching (ZVS) is a critical design objective in modern high-frequency power converters, as it directly influences conversion efficiency and thermal performance. In conventional hard-switched converters, device turn-on occurs while significant voltage remains across the switch, leading to large switching losses and elevated electromagnetic interference (EMI) due to high di/dt and dv/dt transitions [3]. To mitigate these drawbacks, resonant and soft-switching techniques such as ZVS are employed, in which the parasitic capacitances of the switching devices are charged or discharged through the resonant current before conduction begins. As a result, switching transitions occur at nearly zero voltage, minimizing overlap losses and stress on the semiconductor devices [12], [13].

In grid-connected AC-DC adapters, where the rectified bus voltage can exceed 325 V, the ability to achieve ZVS becomes particularly advantageous, reducing switching losses at high frequency and allowing the use of wide-bandgap (WBG) transistors such as GaN and SiC [19]. These devices, characterized by low output capacitance and fast transition speeds, further extend the ZVS operating range and enable operation well into the hundreds of kilohertz [21], [22]. The prototype converter studied in this thesis exploits ZVS through resonant operation in the Multi-Period Damped Resonant (MPDR) mode [10], where controlled energy oscillations between the compensation inductor and the interface capacitors ensure that the switching nodes naturally discharge before device turn-on. This approach enables high-density, soft-switching operation with reduced EMI and improved overall efficiency compared to conventional hard-switched flyback-derived topologies [1], [11].

2.1.2 Topologies

Flyback converter power adapters of around 50 W offer simplicity, inherent current limiting, and a low component count, making them a preferred choice for low- to medium-power isolated applications [1], [16]. However, their hard-switching operation leads to high voltage stress on the primary switch and considerable switching losses, particularly at high frequencies. To overcome these drawbacks, advanced topologies such as the Active Clamp Flyback (ACF) and Asymmetrical Half-Bridge Flyback (AHBF) converters have been introduced [17], [18], [20]-[23].

a. Active Clamp Flyback Converters

The Active Clamp Flyback (ACF) converter has emerged as an enhanced alternative to the traditional flyback topology, addressing the inherent limitations of hard-switching, high-voltage stress, and inefficient leakage energy dissipation. In a conventional flyback, the transformer leakage inductance causes high voltage spikes across the main switch during turn-off, necessitating passive snubber networks that dissipate energy and reduce efficiency. The ACF topology replaces the lossy snubber with an auxiliary active switch and a clamp capacitor, forming a resonant circuit that enables energy recovery and soft-switching operation.

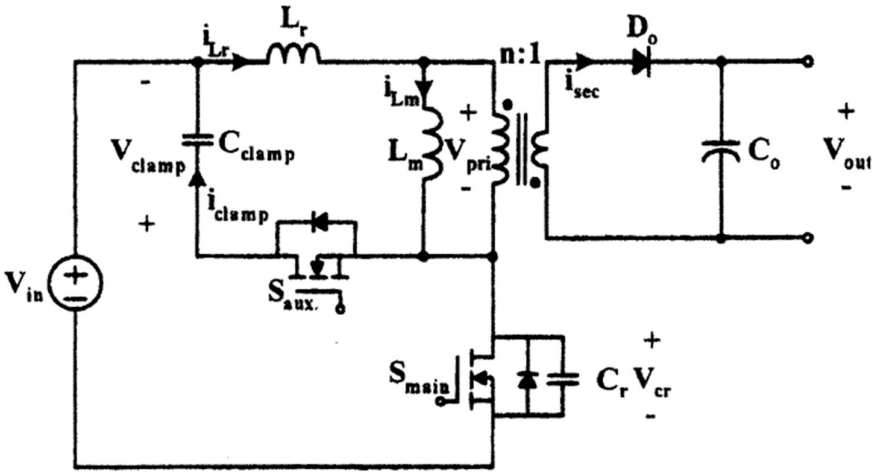


Figure 2.1: Active Clamp Flyback circuit topology. Source:[18]

The steady-state operation of the ACF topology can be divided into two primary modes:

Energy Storage Mode: When the main switch (S_{main}) is turned ON, the transformer magnetizing inductance stores energy, and the secondary diode (D_o) remains reverse-biased. During this period, no energy is transferred to the load, and the magnetizing current increases linearly. The clamp circuit remains inactive.

Resonant Power Delivery Mode: When S_{main} is turned OFF, the primary current continues to flow through the leakage inductance and begins charging the switch's output capacitance while discharging the clamp capacitor. Once the switch-node voltage exceeds the clamp voltage, the auxiliary switch (S_{aux}) conducts, initiating a resonant exchange between the leakage inductance (Lr) and the clamp capacitor (Cclamp). This resonance allows the main switch to achieve ZVS turn-on in the following cycle.

The resonant frequency of this interaction is expressed as:

$$Fres = \frac{1}{2\pi \times \sqrt{Lr \times Cclamp}} \tag{2.1}$$

During resonance, the magnetizing current ensures uninterrupted transformer excitation, preventing core reset issues. For ZVS to be maintained, the energy stored in Lr must exceed that in the combined output capacitances of the primary switches [17].

b. Asymmetrical half bridge Converters

The Asymmetrical Half-Bridge Flyback (AHBF) converter combines the benefits of the flyback and resonant half-bridge topologies, enabling soft-switching operation with high efficiency and power density [16], [17]. The topology of AHBF, as shown in the Figure2.2, consists of two active switches forming a half-bridge, a resonant capacitor (C_r), a resonant inductor (L_r) and the magnetizing inductance (L_m). The inductor which acts as the transformer leakage inductance is the resonant inductor. The secondary employs a synchronous rectifier switch (SR) to minimize conduction losses. The output capacitor C_o filters out the output voltage ripple and the resistance R_o is the equivalent load resistance seen at the output.

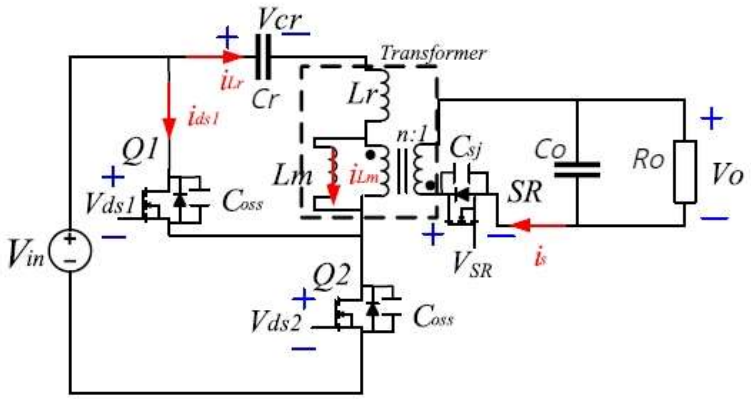


Figure 2.2: Topology of the Grid Adapter. Source:[16]

The operation of the AHBF can be described by dividing the switching time interval into two parts. The first part is the charging period (T_{ON}). In this interval the low-side

switch (Q2) is ON and the high side switch (Q1) on the primary side along with the secondary side switch are OFF. During this period, the magnetizing inductance (L_m) is charged, while no energy transfer is seen from the primary to secondary side. The second is the discharge period (T_{OFF}). The Q2 is OFF and the Q1 along with SR is ON. This interval sees a transfer of power from the primary to secondary side while the magnetizing inductance (L_m) discharges [17], [18].

Unlike the conventional flyback topology, where the magnetizing inductance is responsible for the total energy storage, the AHBF topology includes a resonance capacitor which shares the total energy storage with the magnetizing inductor. Assuming $L_r << L_m$, energy transfer occurs simultaneously from the transformer and the resonant capacitor, resulting in reduced magnetic energy storage and thus a smaller transformer core size [18]. This contributes to improved power density and efficiency, as validated in analytical and experimental studies demonstrating efficiencies exceeding 90% in high-frequency GaN based implementations [19], [21].

However, the AHBF topology presents notable design challenges. Achieving the ZVS condition at each cycle requires a good balance between the magnetizing current and leakage inductance energy [18], [19]. To ensure the ZVS operation, the magnetizing current must remain high, even when output power is low making it difficult to design a converter of this type for a wide load range. Furthermore, the transformer design becomes critical and sensitive to parasitic variations due to the energy transfer and ZVS resonance [17], [18].

Due to these constraints, the AHBF is not adopted in this study. Instead, the focus shifts to the Multi-Period Damped Resonant (MPDR) converter, which achieves capacitive isolation and ZVS without the complexity of coupled magnetics. The MPDR topology operates with a single compensation inductor and a pair of coupling capacitors, eliminating magnetic-core limitations while maintaining soft-switching across a wide load range [9], [10], [11]. This simplification enables higher power density, improved reproducibility, and reduced component stress compared to the magnetically coupled AHBF structure, making it better suited for compact, low-power grid adapter applications.

2.2 Resonant Converters and the Multi-Period Damped Resonant Topology

Resonant converters, on the other hand, overcome the inherent limitations of hard-switched PWM architectures by shaping the voltage and current waveforms through a resonant tank composed of inductors and capacitors. This approach enables soft-

switching, particularly Zero Voltage Switching (ZVS), which significantly reduces switching losses, minimizes electromagnetic interference (EMI), and alleviates thermal stress on semiconductor devices [12], [13]. Common resonant families include the Series Resonant Converter (SRC), Parallel Resonant Converter (PRC), and LLC converter, each optimized for specific load conditions and voltage gain characteristics. Among these, the LLC converter has become one of the most widely used soft-switching topologies due to its ability to maintain ZVS over a wide load range, high efficiency, and natural short-circuit protection [12], [13].

While inductive isolation using magnetic transformers has been the foundation of traditional isolated converter design, capacitive isolation has recently emerged as a promising alternative for achieving galvanic isolation in compact, lightweight, and EMI-sensitive applications [11]. Capacitive coupling provides intrinsic advantages such as reduced electromagnetic emission, elimination of magnetic core losses, and mechanical tolerance to misalignment, all of which make it particularly attractive for miniaturized power adapters and portable devices. However, the conventional implementation of capacitively isolated converters typically requires dual-sided compensation networks inductive-capacitive (LC) filters on both primary and secondary sides to counteract coupling impedance and frequency sensitivity. This not only increases the component count and system complexity but also makes the design highly sensitive to component tolerances, reducing performance reproducibility [9], [11].

As the foundation of the design used in this thesis, previous research has simplified these architectures by introducing single-sided compensation networks and leveraging a new operational regime known as the Multi-Period Damped Resonant (MPDR) mode [9], [10].

The MPDR converter integrates two interface capacitors to provide isolation and a single compensation inductor on the secondary side, effectively minimizing the passive component count while maintaining efficient energy transfer. Unlike traditional resonant converters that operate near or above their resonant frequency, the MPDR topology operates at a switching frequency below the natural resonance ($Fsw < Fres$), where both the inductor current and capacitor voltage exhibit damped oscillations extending across multiple sub-resonant periods. These oscillations naturally discharge the switch node voltage before each commutation, achieving ZVS without additional auxiliary circuits [10]. This operational principle allows the MPDR converter to sustain soft-switching across a broad load range while significantly reducing switching losses. The topology also enables a compact and magnetics-free design, improving reproducibility and simplifying fabrication compared to magnetic transformer-based

systems. The MPDR structure provides a compelling balance between simplicity and performance, making it particularly well-suited for medium-power, high-frequency isolated applications.

The topology for the grid adapter consists of four key functional stages: the half-bridge inverter at the input, the capacitive interface made of discrete capacitors, the secondary-side single inductor compensation network, and the full-bridge rectifier at the output.

a. Half-Bridge Inverter:
   The primary stage consists of two GaN transistors, driven complementarily to generate a high-frequency AC excitation. The switching frequency range determined according to the resonant sub-period, typically lies between 120kHz & 140kHz.
b. Capacitive Interface:
   Two discrete high-voltage capacitors (C1 and C2) form the coupling interface between primary and secondary sides, providing galvanic isolation while transferring displacement current.
c. Compensation Network:
   A single inductor on the secondary side compensates the high reactive impedance introduced by the coupling capacitors.

$$Fres = \frac{1}{2\pi\sqrt{L \times Ceq}} \tag{2.2}$$

   Here, Ceq is the equivalent value of the interface capacitors.

d. Rectifier Stage:
   A full-bridge Schottky rectifier converts the high-frequency AC into DC, supplying the load through a coupling capacitor.

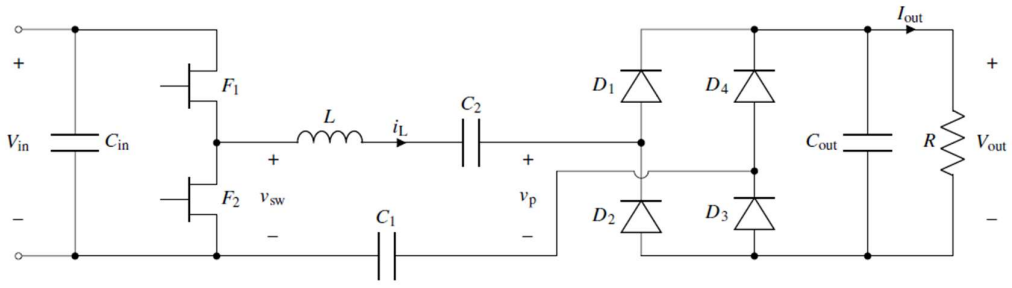


Figure 2.3: Schematic of the Grid Adapter topology [7]

To conclude the study of the state-of-the-art isolated converter topologies, it's evident that the progression from hard-switched converters toward soft-switching and resonant

architectures has culminated in the development of hybrid topologies such as the Active Clamp Flyback (ACF), Asymmetrical Half-Bridge (AHBF), and Resonant converters [16]-[21]. Each represents a distinct balance between complexity, efficiency, and integration level. Developing on these, the study of MPDR-SRC design with its capacitive isolation and reduced passive count, provides an effective trade-off between simplicity and performance for medium-power grid adapters.

The following chapter details the design and implementation of the prototype used to validate the proposed control strategies on this topology.

Chapter 3

The Prototype Board

This chapter presents the design of the prototype board developed for experimental validation of the control strategies described in this work. The converter implements the Multi-Period Damped Resonant (MPDR) topology introduced in Chapter 2, which achieves Zero Voltage Switching (ZVS) operation and high efficiency through capacitive isolation and resonant energy transfer [10], [11], [29].

3.1 The Prototype

The prototype used for this work was designed for the specifications summarized in Table 3.1.

Input Voltage	330V - Grid voltage AC
Output Voltage	20V - DC
Maximum output power	50W

Table 3.1: Prototype specification

The primary goal of this design is to achieve maximum efficiency and power density at the maximum output power. This design achieves ZVS of the input FETs at the rated operation resulting in reduced switching losses [20], [21]. The isolating capacitor values are chosen in the 10nF to 50nF range and the inductor value is chosen in the 10µH to 50µH range to achieve a resonant frequency (fres) of approximately 320kHz, ensuring proper operation in the MPDR region [10], [29].

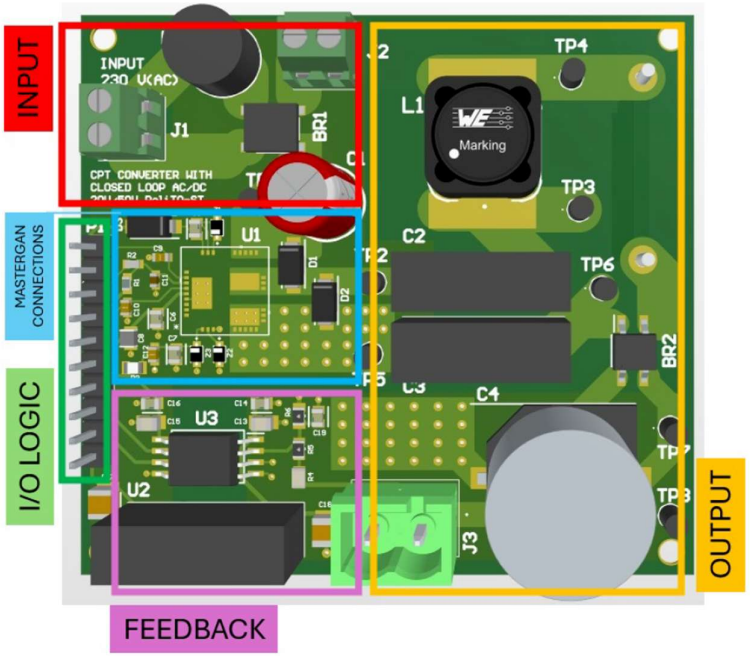


Figure 3.1: Top view of the prototype board Source:[1]

3.1.1 Schematic & Selected Components

The complete schematic of the prototype converter is shown in Figure 3.2. The circuit implements the MPDR–SRC topology introduced earlier, combining a high-frequency half-bridge inverter, two interface capacitors for galvanic isolation, a single secondary compensation inductor, and a full-bridge rectifier for DC output conversion [10], [11]. Each component plays a key role in shaping the resonant response, ensuring Zero-Voltage Switching (ZVS), and preserving the converter's high power density.

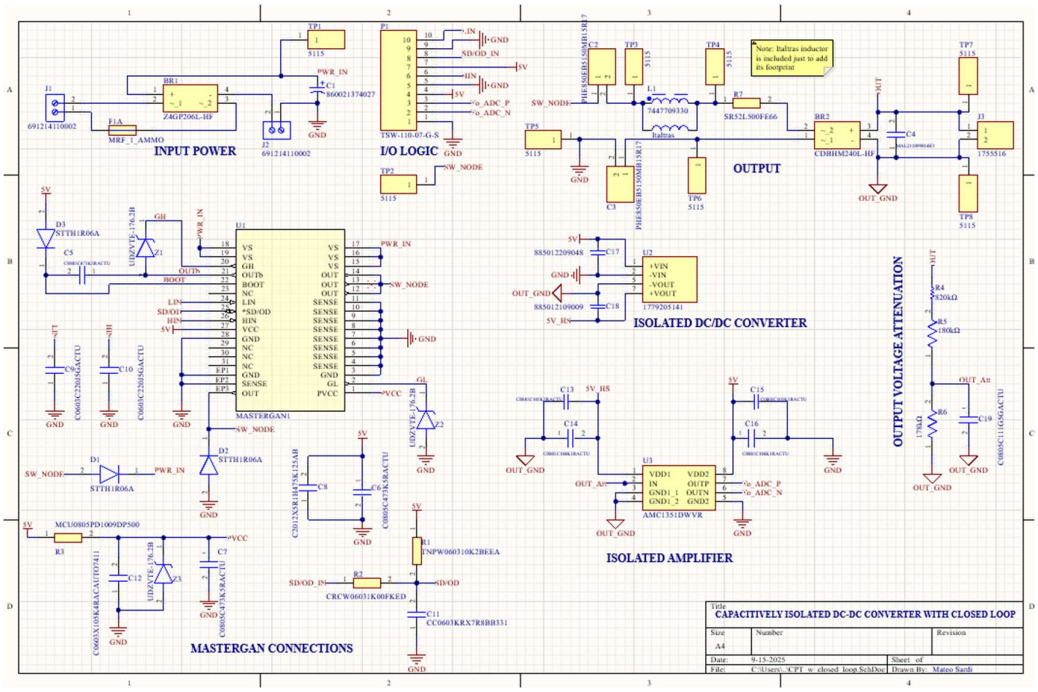


Figure 3.2: Complete Schematic of the Prototype board

The schematic design uses the half-bridge stage employing the MASTERGAN from STMicroelectronics. It combines electrical symmetry, reduced voltage stress, and ease of control, making it a robust choice for modern isolated power conversion systems. The MASTERGAN is a 600 V integrated GaN half-bridge driver with two enhancement mode transistors [29]. The device architecture ensures balanced voltage sharing between the high and low side transistors, reducing transient stress and promoting soft-switching during transitions. The compact layout of this device minimizes parasitic inductance, improves switching edge control, and reduces propagation mismatch between the high and low-side drivers. The key absolute maximum ratings are shown in Fig. 2.5, confirming its suitability for the intended Voltage and current levels.

Symbol	Parameter	Test Condition	Value	Unit
V_{DS}	GaN Drain-to-Source Voltage	T_J = 25 °C	620	V
VCC	Logic supply voltage		-0.3 to 11	V
PVCC-PGND	Low-side driver supply voltage (1)		-0.3 to 7	V
VCC-PGND	Logic supply vs. Low-side driver ground		-0.3 to 18.3	V
PVCC	Low-side driver supply vs. logic ground		-0.3 to 18.3	V
PGND	Low-side driver ground vs. logic ground		-7.3 to 11.3	V
V_{BO}	BOOT to OUTb voltage (2)		-0.3 to 7	V
BOOT	Bootstrap voltage		-0.3 to 620	V
CGL, CGH	Maximum external capacitance between GL and PGND and between GH and OUTb	F_{sw} = 2 MHz(3)	680	pF
RGL, RGH	Minimum external pull-down resistance between GL and PGND and GH and OUTb		6.8	kΩ
I_D	Drain current (per GaN transistor)	DC @ T_{CB} = 25°C (4), (5)	9.7	A
		DC @ T_{CB} = 100°C(4)), (5)	6.4	A
		Peak @ T_{CB} = 25°C(4), (5), (6)	17	A
S_{Rout}	Half-bridge outputs slew rate (10% - 90%)		100	V/ns
V_i	Logic inputs voltage range		-0.3 to 21	V
T_J	Junction temperature		-40 to 150	°C
T_s	Storage temperature		-40 to 150	°C

Figure 3.3: Absolute Maximum ratings for MASTERGAN1 [29]

The displacement current generated by the half-bridge stage flows through the interface capacitors, which form the galvanic isolation barrier between the primary and secondary sides. For the isolating capacitors, PHE850EB5150MB15R17 Y-type capacitor from Kemet is used. Typically, this capacitor is intended to be used are as interference suppressors in Y2 (line-to-earth) applications. This specific capacitor has a capacitance of 15nF [10], [29].

The compensation inductor is the most critical component, as its value directly defines the resonant frequency and affects ZVS range and current stress. The Italtras S.r.l custom designed the inductor used in this thesis. It exhibits a measured inductance of 37.4 µH at 100 kHz and low series resistance, ensuring efficient energy transfer and stable resonance. The resulting resonance frequency from the inductor and the interface capacitors is the design reference for selecting the switching frequency range ensuring ZVS operation in the multi-period damped resonance region [10], [29].

The output stage uses a CDBHM240L-HF Schottky bridge rectifier from Comchip. With a peak reverse voltage of 40 V, forward current of 2 A, and forward voltage drop of only 0.55 V (at 2 A), it provides efficient AC-DC conversion and limits thermal losses in the secondary stage. The fast recovery and low junction capacitance of this rectifier minimizes commutation losses, preserving the converter's high efficiency even

under dynamic load transitions. The rectifier output is filtered by a low-ESR capacitor, providing a smooth DC voltage to the load [29].

The AMC1351 precision isolation amplifier from Texas Instruments is employed to achieve accurate sensing of the output voltage and galvanic isolation between the control circuitry and the high-voltage stage. It accepts a single-ended analog input and outputs a differential signal compatible with the STM32 ADC. The output voltage is scaled using a resistor divider network (Fig. 2.7) with a gain of 0.152, ensuring that a maximum expected converter output of 33 V corresponds to an amplifier input of 5 V, well within the AMC1351's linear range [28], [30].

This isolated feedback path enables closed-loop regulation through the digital controller, forming the interface between the hardware and the control algorithms implemented on the STM32 microcontroller.

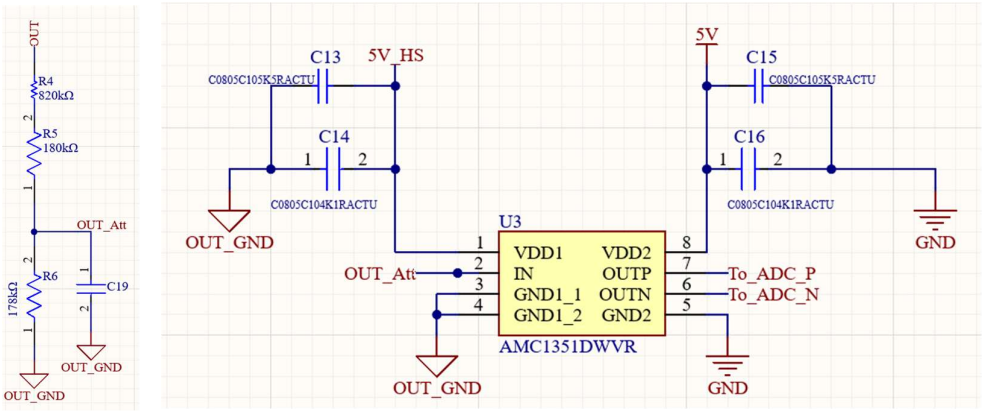


Figure 3.4: Resistor Divider (left) & Isolated amplifier (right) circuit [30]

3.1.2 Layout

The layout of the prototype board was designed with particular attention to minimizing parasitic coupling, ensuring galvanic isolation, and optimizing current return paths. Since the converter operates at high switching frequencies and with significant voltage gradients, the physical arrangement of the power and control sections critically influences overall performance, electromagnetic compatibility (EMC), and measurement accuracy [29], [31].

A clear separation was maintained between the high-frequency power stage and the low-level sensing and control circuitry. The half-bridge node, which experiences the highest voltage slew rate, was kept as compact as possible to reduce parasitic inductance and ringing. Short, wide copper traces were used in the high-current paths between the MASTERGAN package, the interface capacitors, and the compensation inductor to minimize loop area and stray impedance. Thermal dissipation for the

MASTERGAN device was managed through large copper pours on both top and bottom layers, connected by multiple thermal vias to ensure even heat spreading during high-load operation [29], [31].

The galvanic isolation boundary, formed by the interface capacitors, divides the primary and secondary sides of the layout. On the bottom copper layer, the capacitive interface is distinctly visible, providing a physical and electrical separation between the grid-referenced and low-voltage domains. The placement of these capacitors was optimized to minimize parasitic capacitance to ground while maintaining symmetrical field distribution across the plates, ensuring consistent coupling behavior.

Sensitive analog nodes, such as the feedback sense lines connected to the AMC1351 isolation amplifier, were routed away from the switching traces and shielded by a grounded guard plane to suppress common-mode interference. Decoupling capacitors were placed as close as possible to the supply pins of the amplifier and the STM32 microcontroller to stabilize local voltage rails and limit noise propagation [28], [31].

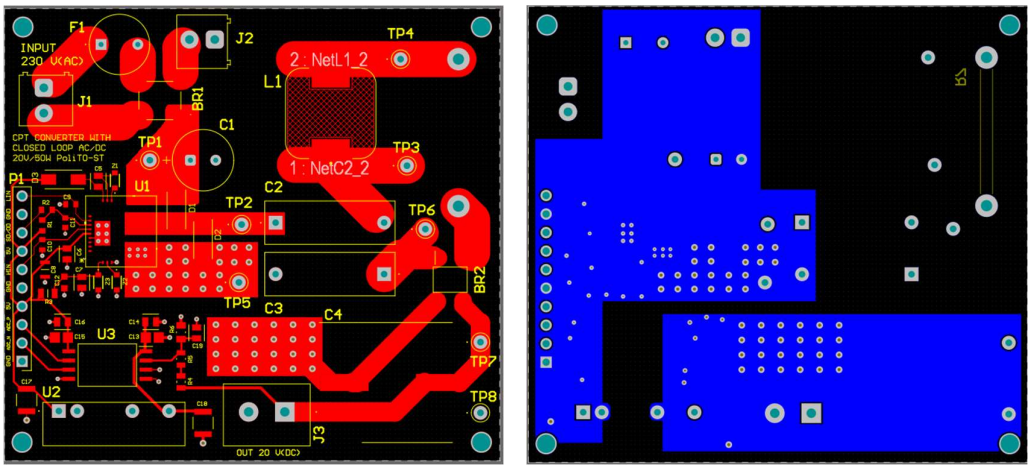


Figure 3.5: Layout top (left) & bottom (right) layers of the prototype board

Overall, the final PCB layout achieves a balanced compromise between electrical isolation, low parasitic interference, and compactness, which is crucial for maintaining reliable operation of the MPDR converter at high frequencies and grid-level voltages.

Chapter 4

Introduction to Control Strategies

In DC–DC converters control strategies determine the dynamic response, efficiency, and stability of the system. The primary goal of any control technique is to maintain a regulated output voltage under varying input and load conditions, while minimizing losses and ensuring reliable operation.

This chapter introduces the control strategies implemented to regulate the output voltage of the isolated DC-DC converter based on the multi-period damped resonant (MPDR) topology. Four distinct control techniques were analyzed and implemented: Frequency Modulation (FM), Pulse Width Modulation (PWM), Bang-Bang (BB) Control, and Dyadic Digital Pulse Modulation (DDPM). All strategies, except the bang bang control, employ the same feedback framework using a proportional–integral (PI) compensator, which adjusts the control signal based on the instantaneous error between the measured output voltage and the desired reference. The modulation scheme determines how this control variable is translated into gate-drive behavior for the half-bridge inverter.

4.1 Frequency Modulation Control

The Frequency Modulation (FM) control strategy regulates the converter output by varying the switching frequency of the half-bridge inverter while maintaining a constant duty cycle, typically 50%. In the context of a capacitively isolated converter operating in Multi-Period Damped Resonant (MPDR) mode, the output voltage is highly sensitive to the excitation frequency. This characteristic makes frequency modulation a natural and effective method for closed-loop voltage regulation [25], [26]. When the frequency is close to resonance, the converter exhibits higher gain and, consequently, a higher output voltage. Conversely, as the switching frequency moves away from the resonant point, the gain decreases and the output voltage falls. However, the MDPR system exploits the local voltage gain peaks which are found in correspondence to the odd sub-harmonics of the resonance frequency [22]. Previous simulations identified this range to be between 120 kHz and 140 kHz. By dynamically adjusting the switching frequency within this defined range, the controller compensates for variations in load resistance and input ripple to maintain the desired output voltage.

A Proportional–Integral (PI) controller is used to eliminate steady-state error and ensure stable regulation. The controller generates a control action u(t) from the voltage error, e(t).

$$e(t) = Vref - Vout \tag{4.1}$$

where, Vref is the desired output voltage (20V) and Vout is the actual output voltage.

The PI controller responsible to generate the control action is defined by the equation:

$$u(t) = kp * e(t) + ki\left(\int_0^t e(t)dt\right) \tag{4.2}$$

The control action is used to calculate the switching frequency to regulate the output voltage by using

$$Fsw = \frac{fmin + fmax}{2} - \left(u(t) * \left(\frac{fmax - fmin}{2}\right)\right) \tag{4.3}$$

The above formula has the following effect on the output voltage:

a. When e(t)<0, the controller action, u(t), reduces the switching frequency to increase power transfer.
b. When e(t)>0, the controller action, u(t), increases the switching frequency, reducing the power transfer.

A key advantage of frequency modulation is its ability to maintain soft-switching (ZVS) over a wide operating range, minimizing switching losses and electromagnetic noise. This makes it highly suitable for high-efficiency operation in medium-power conditions. However, the achievable output voltage range is limited by the resonant characteristic; for very light loads, the converter gain becomes insufficient even at the lowest safe frequency, restricting the control authority.

4.2 Pulse Width Modulation Control

The Pulse Width Modulation (PWM) control method regulates the converter output by varying the duty cycle of the inverter switching signal while maintaining a fixed switching frequency [25], [26]. The sequence of equations are:

$$e(t) = Vref - Vout \tag{4.4}$$

This equation calculates the error value which is provided as input to the PI controller.

$$u(t) = kp * e(t) + ki\left(\int_0^t e(t)dt\right) \tag{4.5}$$

The PI controller is used to generate a control action u(t) as a function of the voltage error e(t), which is limited between [-1, 1] and is linearly mapped to the duty-cycle range used for modulation.

The value of the control action is used to calculate the new duty cycle. The range of duty cycle is considered depending on the converter design and ZVS conditions. The two operating regions that can be chosen symmetrically around 50 % duty are

a. Low-duty region: $d \in [0,17]$ %
b. High-duty region: $d \in [83,100]$ %

Both regions are equivalent in terms of attainable output voltage due to waveform symmetry, but they differ in switch stress and current direction during switching transitions. In practice, the region ensuring soft-switching for both transistors is preferred to minimize losses and ensure balanced thermal operation. Therefore, the low-duty region is chosen. The formula to select the duty cycle (DCycle) is given by:

$$DCycle = \frac{Dutymin + Dutymax}{2} + \left(u(t) * \left(\frac{Dutymax - Dutymin}{2}\right)\right) \tag{4.6}$$

Here, Dutymin and Dutymax are lower and upper limit, respectively, of the low-duty region.

PWM control offers several practical advantages. It is simple to implement using standard timer peripherals, requires only one control variable (duty cycle), and provides fast transient response. Since the switching frequency remains fixed, the sampling and timing loops of the controller are easily synchronized, simplifying firmware design and EMI filtering. However, PWM control also presents limitations when applied to resonant systems. Because the switching frequency is constant, the converter may lose Zero Voltage Switching (ZVS) during large load variations or input ripple conditions. This leads to increased switching losses and potentially reduced efficiency compared with frequency-based control [12], [13], [25].

4.3 Bang Bang Control

The Bang–Bang (BB), or hysteretic control, is one of the simplest yet most responsive regulation techniques used in power converters [26]. Unlike modulation-based methods such as FM or PWM, which compute a continuous control action, Bang–Bang control operates purely on discrete events. The converter switches between two operating states depending on whether the output voltage is above or below the predefined thresholds.

Two voltage boundaries are defined around the desired output voltage Vref, an upper threshold Vmax and a lower threshold Vmin. When the measured output Vout exceeds Vmax, the controller disables the switching stage, forcing the system into an OFF state, where energy transfer temporarily stops and Vout starts to fall. Once Vout falls below Vmin, the converter returns to the ON state, re-enabling power transfer to the load. This cyclic process continues indefinitely, causing the output voltage to oscillate within the defined hysteresis band [9],[26].

The resulting output ripple amplitude is approximately:

$$Vripple = Vmax - Vmin \tag{4.7}$$

By adjusting this window, a direct trade off of output precision against switching frequency can be achieved. A smaller hysteresis band reduces voltage ripple but increases switching frequency and losses and a wider band lowers the switching frequency but results in larger ripple [3], [22].

The bang bang controller's main advantage is its inherent robustness. Because it relies solely on direct feedback of the output voltage, it automatically adapts to parameter variations, load transients, and nonlinearities in the converter. The control logic contains no compensator parameters to tune, making it extremely stable in practice. However, this simplicity comes with drawbacks. The switching frequency is variable, depending on the instantaneous load and input voltage. This variability can cause spectral spreading of the switching noise, complicating electromagnetic interference (EMI) filtering. The abrupt ON–OFF transitions can result in large inrush currents at the switching node and transient stress on the resonant components [9], [22].

4.4 Dyadic Digital Pulse Modulation Control

The Dyadic Digital Pulse Modulation (DDPM) is a fully digital modulation technique that encodes an analog quantity into a deterministic binary bitstream whose pulse density is proportional to the input code. Unlike stochastic dithering or pulse-width modulation, DDPM produces a deterministic, periodic, and spectrally well-defined sequence. Its core property is that most of the spectral energy is shifted toward higher

harmonics, allowing simple low-order filtering for analog reconstruction or power regulation [27].

As defined by [ref], a DDPM associates each N-bit integer code n with a binary sequence obtained by the superposition of dyadic basis functions, each active for 2^i cycles within a fundamental period of $(2^N)*T$sw. The resulting stream is high for exactly n of those cycles, providing a duty ratio of$\left({}^{n}/_{2^N} \right)$. This deterministic relation between the input code and the number of active pulses gives the DDPM its precise density-to-value mapping. Mathematically, the modulated stream $\sigma(t)$ can be expressed as given in [27].

$$\sigma(\mathrm{t}) = \sum_{i=0}^{N-1} bi \times Si(t) \tag{4.8}$$

where bi are the bits of the binary representation of n, and Si(t) are the non-overlapping dyadic basis functions. Because each function occupies a distinct temporal slot, the overall bitstream exhibits a high-frequency harmonic spectrum, making it advantageous for digitally controlled converters, D/A conversion, and amplitude modulation [27].

Implementing the DDPM control of the prototype board, the converter output voltage is regulated by selectively skipping or inserting switching pulses according to a binary-weighted sequence within a fixed macro-period. Instead of continuously adjusting frequency or duty cycle, the controller modulates the average power transfer by distributing a calculated number of active pulses over a predefined set of switching intervals [27].

A macro-period consists of 2^{N} equal time slots, where N represents the number of digital bits defining the modulation resolution. The control variable is an integer $n \in [0 , 2^{N-1}]$ that determines how many pulses are skipped within each macro-period [27].

The mapping b etween the continuous control output u(t) and the integer n(t) is expressed as:

$$n(t) = round\left(\left(\frac{1-u(t)}{2}\right) \times (2^N - 1)\right) \tag{4.9}$$

Here, u(t) is the output of a PI compensator that processes the instantaneous voltage error e(t).

a. When $u(t)$ is positive (indicating Vout less than the reference), the number of skipped pulses is small, leading to higher power delivery.

b. When $u(t)$ is negative (indicating Vout more than the reference), more pulses are skipped, effectively reducing the average power until the output voltage returns to its nominal value.

The pulse distribution within each macro-period follows a dyadic (bitwise operation) pattern, ensuring that skipped pulses are spaced uniformly rather than clustered.

The DDPM technique thus offers a fully digital, resource-efficient, and deterministic approach to closed-loop control. The dyadic pulse distribution inherently minimizes low-frequency harmonic components, improving voltage ripple performance and reducing the need for complex filtering on the power stage. It combines the advantages of precise digital control, predictable spectral behavior, and the high power, and efficiency, making it particularly suited for high-frequency, isolated DC-DC converters such as the capacitively isolated prototype presented in this work. However, due to the effective switching activity which varies within each macro-period (dependant on N), the dynamic response of the system is expected to be slightly slower compared to the continuously modulated strategies like PWM, especially under rapid load transitions [27].

Chapter 5

STM32 Configuration and Control Strategy Implementation

The STM32 development board with the STM32G4 Series microcontroller is used to generate the gate signal input to the MASTERGAN1 and to read the output voltage and perform the control action. The connection between the prototype and the development board is established using the P1 connector in the prototype. The connector pinout of the development board as provided in the user manual is shown below.

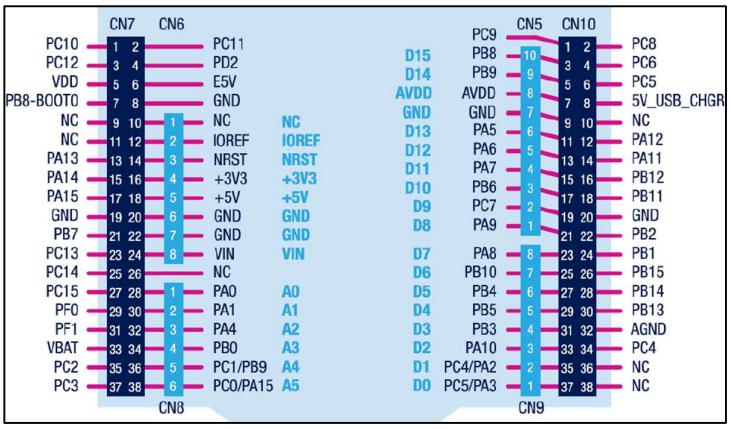


Figure 5.1: Pinout of the development board

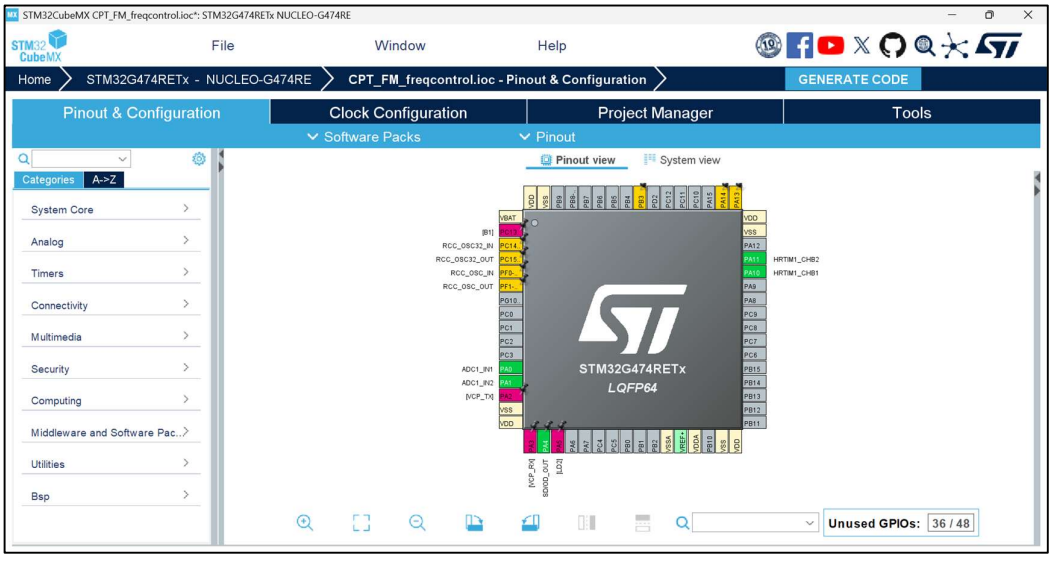


Figure 5.2: STM32CubeMX user interface

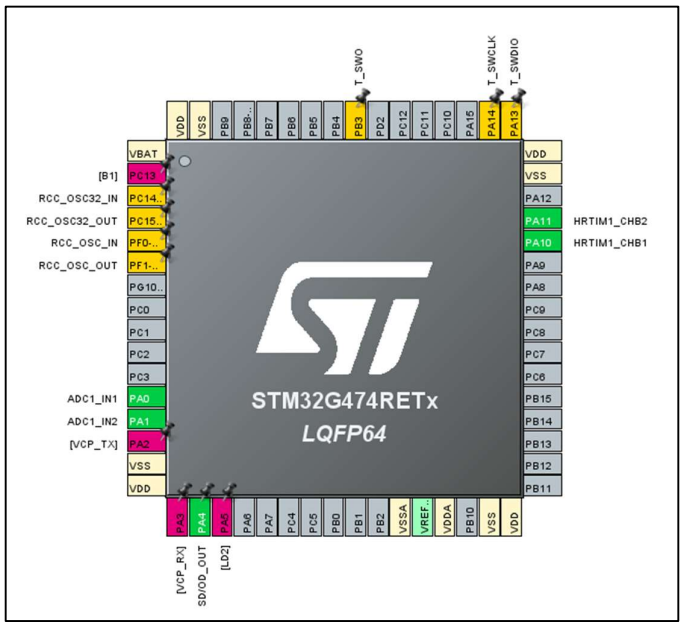


Figure 5.3: Configuration of peripherals in NUCLEO-G474RE

A visual description of the development board's user interface can be found in Figure 5.2 and Figure 5.3. In addition to generating a main.c script and the built-in STM32 library, this user interface enables the user to configure peripherals according to the application. Clicking the blue "GENERATE CODE" button in the STM32CubeMX interface initiates this operation. The control strategy algorithms used in this thesis are based on this script. The STM32Cube IDE is the code editing interface, and the Figure 5.4 below shows the user interface of the development environment.

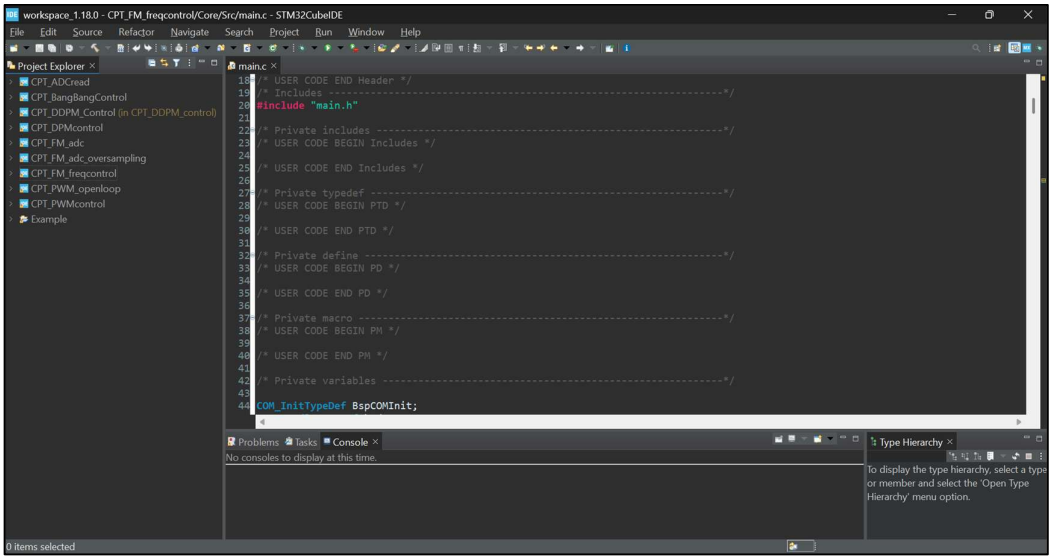


Figure 5.4: STM32Cube IDE interface

5.1 General Configuration

5.1.1 HRTIM

As a general configuration, the high and low side gate signals are configured for a switching frequency of 115kHz with 50% duty cycle. The high-resolution timer (HRTIM) in the STM32 microcontroller is used to generate these gate pulses.

The TB1 and TB2 timers in the HRTIMB is configured along with its compare registers (COM1, COM2, COM3 and COM4) to accurately provide the low and high side gate signals based on the frequency/duty cycle. These compare registers play a crucial role by introducing accurate switching with dead time between the high and low side switch pulses.

The high resolution timer is easily configured with the help of STM32CubeMX, which is the generic graphic use interface (GUI) for all ST Microelectronics development boards. The image shows the window where the HRTIMB is configure:

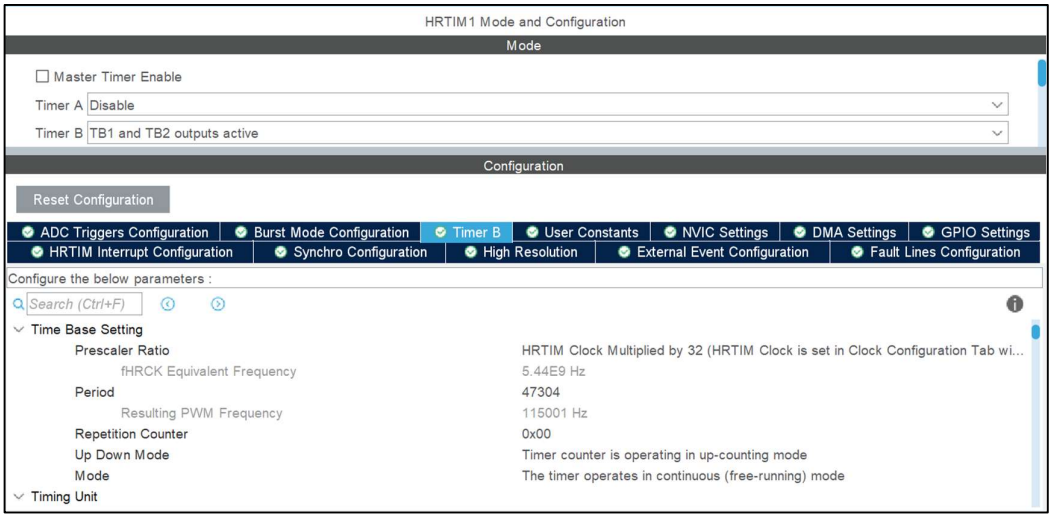


Figure 5.5: HRTIM1 configuration window in STM32CubeMX user interface

As an initial configuration, the switching frequency is set to 115kHz with the following setting:

Parameter	Value	Comment
Pre-scaler ratio	HRTIM clock multiplied by 32	This sets the fHRCK equivalent frequency to 5.44GHz

Period	47304	This sets the switching period for 115kHz. The end of period is where the high side FET switches ON
Compare unit 1	23108	Event at which High side FET switches OFF
Compare unit 2	23652	Event at which the Low side FET switches ON
Compare unit 3	46760	Event at which the Low side FET switches OFF
Compare unit 4 (Used in Bang Bang and DDPM control strategies)	47304	Event at which the high side FET switches ON (Intersects with the period value)

Table 5.1: HRTIMB configuration setting

The values for the Period & Compare unit is calculated as:

$$Period = \frac{fHRTIM}{fsw} \tag{5.1}$$

$$COM1 = \frac{Period}{2} - Period(dt) \tag{5.2}$$

$$COM2 = \frac{Period}{2} \tag{5.3}$$

$$COM3 = Period - Period(dt) \tag{5.4}$$

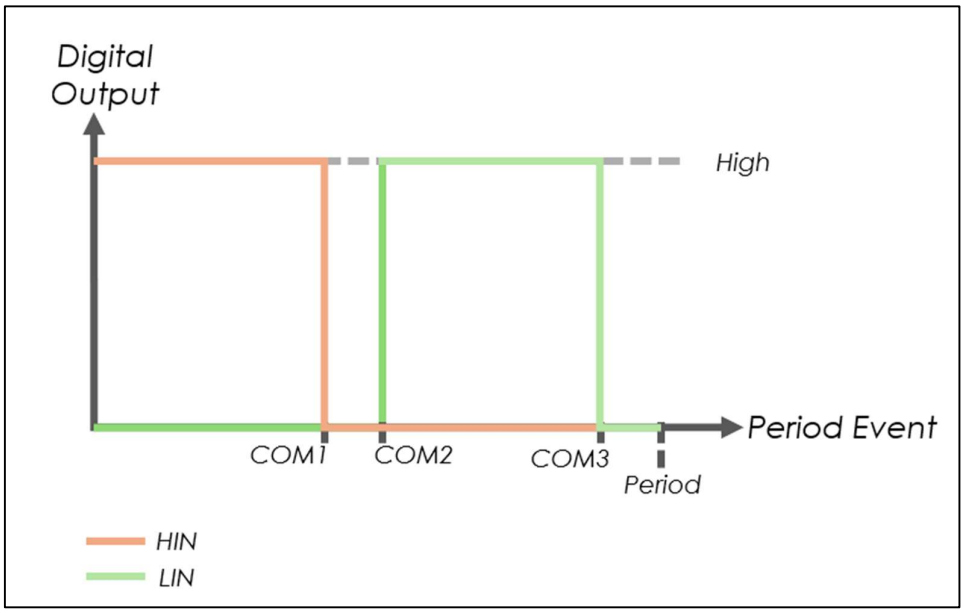
Here,

fHRTIM is the pre-scaler ratio value for the high resolution timer, which is 5.44GHz

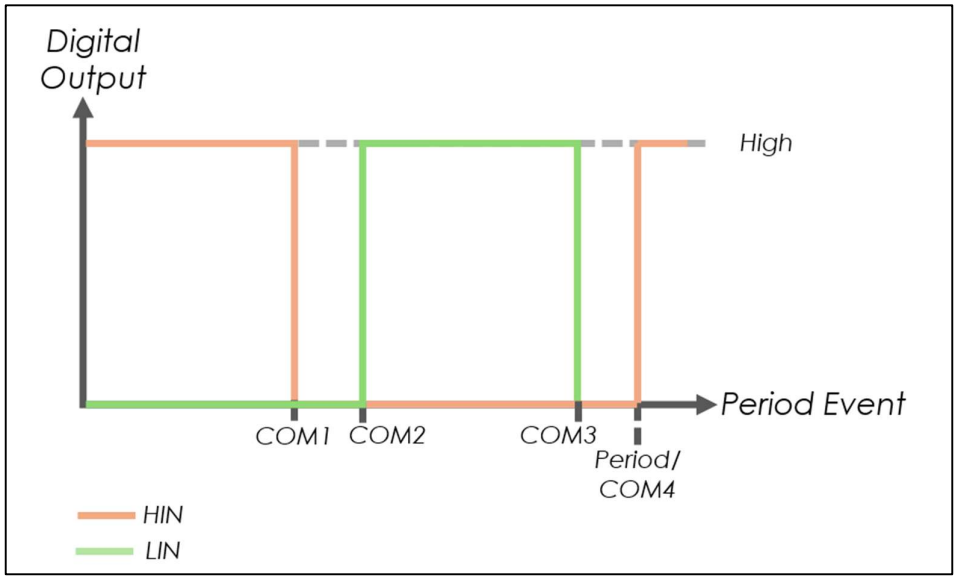
fsw is the switching frequency of the converter, here it is set to 115kHz.

Period(dt) is the dead time period, set to 544 for a dead time of 100ns.

**The ADC trigger event using a compare register of the high resolution timer (HRTIMA/HRTIMB) for the ADC operation will be explained in the ADC Section 5.1.2*.



(a)



(b)

Figure 5.6: Logic diagram of the gate signal generation for (a) FM and PWM (b)Bang bang and DDPM

Figure 5.6(a) and Figure 5.6(b) represents the gate signal generated using the compare registers of the HRTIMB. HIN and LIN represent the high side and low side gate signals respectively.

5.1.2 ADC Calibration and Configuration

The differential IN1 ADC is used to read the output voltage from the prototype board. The parameters are set are given in the table bellow

Parameter	**Value**
Clock Prescaler	Synchronous mode divided by 4
Resolution	12-bit
Sampling time	24.5 cycles
Oversampling Ratio	4x
Oversampling Shift	2

Table 5.2: ADC configuration setting

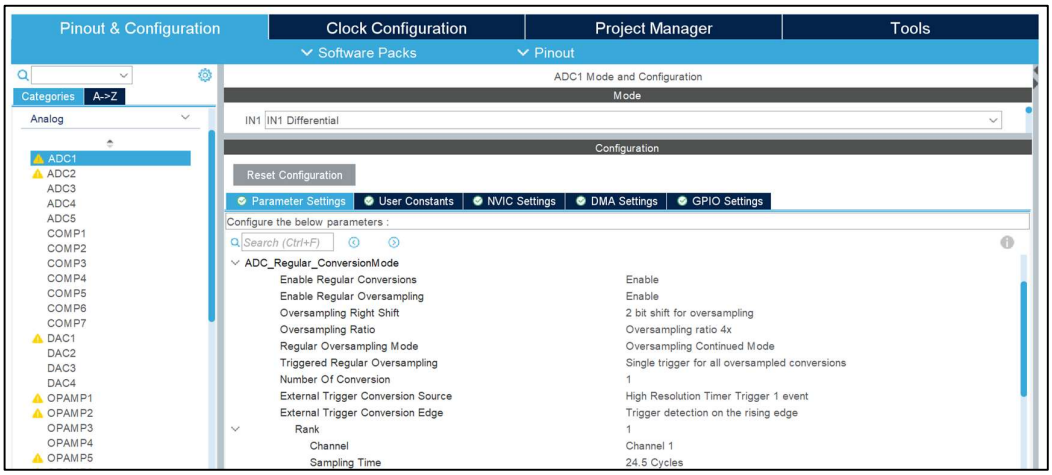


Figure 5.7: ADC configuration window in STM32CubeMX user interface

The sampling time and oversampling ratio is selected as the optimum solution to accurately read the voltage. From the STM32 microcontroller datasheet, the time taken for reading ADC can be calculated:

The ADC clock is derived from the internal AHB clock frequency of 170MHz, calculated to be 42.7MHz

$$fadc = \frac{Fahb}{Clock\ prescaler} = 42.7MHz \tag{5.5}$$

$$tadc = \frac{1}{Fadc} = 23.529ns \tag{5.6}$$

By default, the ADC takes 12.5 such cycles for the conversion. This is called the conversion cycle. However, the ST Microelectronics GUI allows to set the number of cycles to be used for sampling, called the sampling time.

The oversampling feature, detailed in STMicroelectronics Application Notes [] [], allows the converter to accumulate multiple conversion results internally and average them before the final data is presented to the user register. Unlike software averaging, the oversampling process is executed entirely by the ADC peripheral, ensuring deterministic timing and negligible CPU overhead.

During each trigger event, the ADC performs N consecutive conversions of the same analog input. These results are summed within an internal 16-bit accumulator, and the final average is obtained by applying a right bit shift of M bits, as defined by the OVSR (Oversampling Ratio) and OVSS (Oversampling Shift) fields in the ADC_CFGR2 register.

The ADC resolution can be affected is the Oversampling shift value is not set correctly. The resulting resolution for the oversampling ratio and shift value used can be given by,

$$ADCnew_resolution = ADCresolution + \left(\frac{\ln(OVSR)}{\ln(2)}\right) - OVSS \quad (5.7)$$

The averaged result is then written to the ADC data register, producing a single high-resolution output sample for every N raw conversions. It is necessary to keep the total time for this process to be limited within the switching period to enable the controller to actively regulate the output before the new period commences. From ethe above table, oversampling ratio is configured at 4. The total time taken for the entire ADC operation is given by:

$$Tadc = \{tadc * (Conversion\ Cycles + Sampling\ Cycles)\} * 4 = 3.4824\mu s \quad (5.8)$$

In addition, a trigger is set using one of the HRTIM compare register at 25% duty cycle of 140kHz for the ADC to read from the register. For the FM and PWM control strategies, COM4 value of HRTIMB is chosen as the ADC trigger event. For the bang bang and DDPM control strategies, this trigger event is set by the COM3 value of the HRTIMA.

This value is chosen to be able to avoid any anomalies that can be present in the ADC line during switching. This

$$TotalTadc = Ttrigger + Tadc = 5.2681\mu s \quad (5.9)$$

Based on the operating range used in this technology, between 115kHz and 140kHz, the least time period for a switching cycle is for the 140kHz which is 7.149μs. From the above calculation, the ADC computation time is well withing this range.

The value obtained by the ADC is then converted, using the formula given below, which is used in the four different control strategy to provide appropriate control actions.

$$ConvertedValue = \frac{\left(\left(\left(\frac{ADC\ Value}{4095}\right) * 2\right) - 1\right) * Vref}{Total\ gain} \tag{5.10}$$

Here, Vref = 3.2751V represents the reference voltage for the ADC pins in the STM32 development board. This value is measured on the STM32 development board using the digital multimeter listed in Chapter 6.

5.2 Gain Calibration

In Chapter 3, the prototype design discusses the gain introduced to the output voltage. This gain is introduced in two parts,

a. Voltage divider network designed to introduce a gain of 0.152V/V to the output voltage (Vout).
b. Isolation amplifier – the stepped down output voltage from the voltage divider network is fed to the isolation transformer which introduces a linear gain of 0.4V/V for the input range between -0.25V to 5V.

It is essential to read the exact output voltage as the initial step in the control process. In order to verify that the design and device are consistent, the prototype board's gain is calibrated in two stages and for a nominal output voltage of 20V. The calibrated values and calculations are presented below:

a. Voltage measured at the output of voltage divider is 2.6475.

$$Gainofvoltagedivider = \frac{2.6475}{20} = 0.132 \tag{5.11}$$

b. Differential voltage measured across the ADCn and ADCp lines of the isolation amplifier is 1.080.

$$GainoftheIsolationamplifier = \frac{1.080}{2.6475} = 0.4079 \tag{5.12}$$

Therefore, the total gain introduced by the system to the output voltage is

$$TotalGain = 0.132 * 0.4079 = 0.054 \quad (5.13)$$

5.3 The PI Controller Implementation

The Proportional–Integral (PI) controller is one of the most widely used feedback control mechanisms in power electronic converters, offering a balance between simplicity, stability, and steady-state accuracy.

The proportional term provides an immediate response to voltage or current error, while the integral term accumulates past errors to eliminate steady-state offset, ensuring precise output regulation under varying load or input conditions [24], [26]. However, during large transients or at the saturation operation region of the system, the integral term may continue to accumulate error even when the control output is clamped by physical or software-imposed limits, this phenomenon is known as the integral windup. This leads to overshoot and delayed recovery once the error returns within range. To mitigate this, anti-windup mechanisms are implemented, typically by halting integration or back-calculating the integral term when the output reaches a saturation limit. Properly tuned PI controllers with anti-windup protection ensure fast transient response and stable operation, particularly in digitally implemented control loops such as those used in DC-DC converters and AC-DC adapters [24], [25], [26].

The flowchart (Figurex.x) illustrates the implementation of the digital Proportional-Integral (PI) control algorithm used in the prototype board for closed-loop voltage regulation. The control sequence begins by reading the instantaneous error value e(t), computed as the difference between the reference voltage and the measured output voltage. The reference values are set as Vref=3V (as described in Chapter 6) and Vref=20V, for low voltage inputs and for the grid voltage inputs respectively. The output voltage is measured using the differential ADC lines as explained in the previous section. The PI controller calculates the proportional term (P) and the integral term (I),

$$\mathrm{P} = \mathrm{kp} \times \mathrm{e(t)} \quad (5.14)$$

$$I = I\_old + (ki \times e(t) \times Tsw) \quad (5.15)$$

and then computes the total control output u(t).

$$u(t) = P + I \quad (5.16)$$

Evidently, from Eq.5.15, the integral term accumulates over time to eliminate steady state offset.

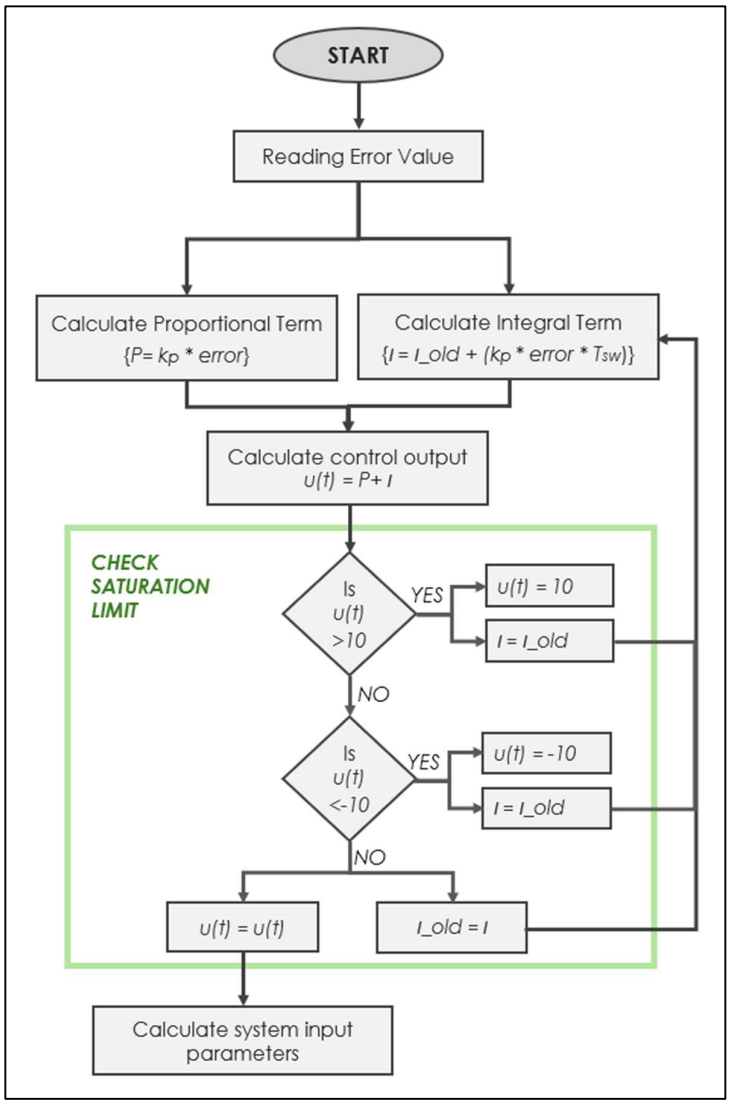


Figure 5.8: PI controller flowchart

The output u(t) is subjected to a saturation check to ensure that the control parameters remain within the allowable operating limits of the system (±10 in this case).

If u(t) exceeds these limits, it is clamped to the boundary value. *The boundary limits for each control strategy are specified in the specific sections below*. At the limit, the integral term is clamped at I=I_old; to ensure the system does not accumulate any values and avoid the system wind-up. This is the anti-windup implementation which prevents integral windup explained above, preventing large overshoots, instability of the system in saturation. If the output remains within the saturation limits, the computed control signal is accepted, and the integral term is updated normally. Finally, the validated control output u(t) is applied to the system to compute the next input parameters (e.g., duty ratio or switching frequency).

In Chapter 4, the control output saturation limits were initially defined as ±1. However, during the experimental phase, it was observed that these limits were frequently reached under nominal load conditions within the acceptable operating range of the control strategies. To ensure adequate controller headroom and prevent premature saturation, the limits were therefore scaled by a factor of 10. This adjustment provided greater flexibility for the controller to respond effectively to dynamic load variations while maintaining stable closed-loop operation.

This PI controller implementation ensures robust closed-loop operation by maintaining a balance between fast transient response (due to the proportional term) and steady-state accuracy (due to the integral term), while the anti-windup mechanism enhances overall stability and responsiveness under varying load and input conditions.

The three control strategies (FM, PWM and DDPM) using the PI controller to generate the required control variables use the controller parameters [24] given in Table 5.x.

Control Strategy	**Control Variable**	**Frequency/ Duty cycle**	**Controller type**	**Controller Parameters**
Frequency Modulation	Switching Frequency (Fsw)	Variable/ Fixed	PI	k_p=3.3 k_i=390
Pulse Width Modulation	Duty cycle (d)	Fixed/ Variable	PI	k_p=6 k_i=320
DDPM	Number of skipped Pulses (n)	Fixed/ Fixed	PI	k_p=1.5 k_i=200

Table 5.3: PI controller parameters used for the control strategy experiments

5.4 Frequency Modulation

Initial values of the high and low side gate signals are configured for a switching frequency of 115kHz with 50% duty cycle.

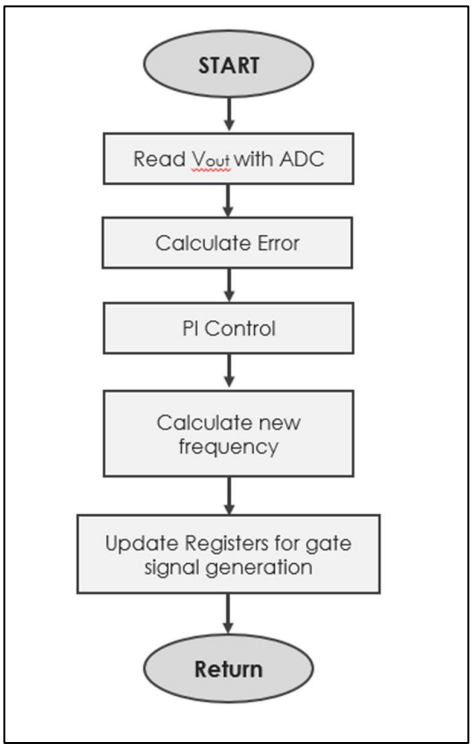


Figure 5.9: Frequency modulation flowchart

The flowchart in the Figure 5.9, depicts the frequency modulation control operation. At each ADC trigger event, the microcontroller reads the Vout values along the differential ADC lines. The ADC values are then converted as explained in section 5.1.2. This value is compared with the nominal output value (Section 5.6).

The control variable is used to determine the switching frequency () to be used in the next period. The main goal is to generated the gate pulses by computing the new compare register values. The code implementation is shown in Appendix C. This will ensure that the new switching frequency is implemented in the system. The values for the Period & Compare registers are calculated using equations 5.1-5.4.

5.5 Pulse Width Modulation

At start-up, the high and low side gate signals are configured for a switching frequency of 115kHz with 20% duty cycle.

Similar to the frequency modulation control, the PWM control process begins with the measurement of the output voltage Vout using the differential ADC integrated within the STM32 microcontroller, followed by the calculation of the error term (e(t)). This error is processed through a Proportional Integral (PI) controller, which determines the

corrective action required to minimize the steady-state error and maintain the output voltage at its nominal level.

The control algorithm can be represented as given in the following flowchart:

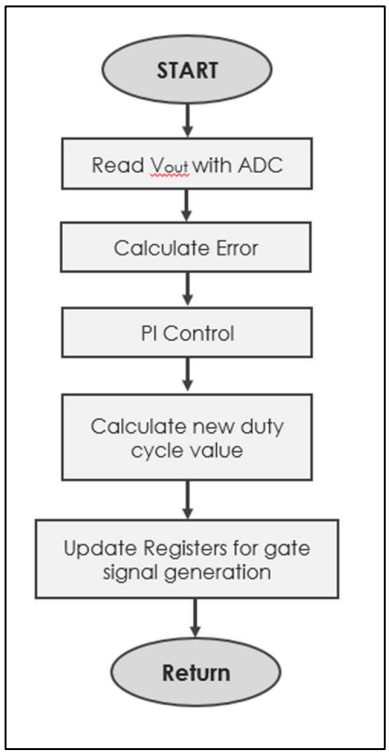


Figure 5.10: Pulse width modulation control flowchart

Since the frequency of the gate pulses is fixed at 115kHz, the duty cycle varies with any changes in the COM1 and COM2 register values. The logic diagram of the gate signals as shown in the Figure 5.6 (a). The code implementation is shown in Appendix D.

The values of COM1 and COM2 is calculated as:

$$COM1 = (Dcycle \times Period) - Period(dt) \tag{5.17}$$

$$COM2 = (Dcycle \times Period) \tag{5.18}$$

5.6 Bang Bang Control

At system initialization, the high- and low-side gate signals are configured for a switching frequency of 115 kHz with a 50% duty cycle. The Bang–Bang (BB) or hysteretic control strategy operates by comparing the real-time output voltage Vout with two predefined thresholds Vmax and Vmin around the nominal reference voltage Vref

The control algorithm can be represented as given in the following flowchart:

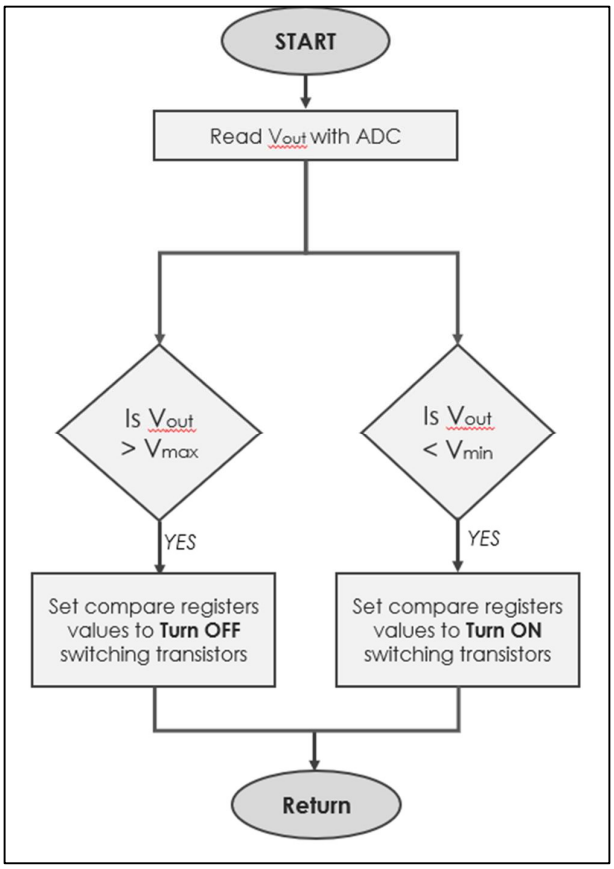


Figure 5.11: Bang bang control flowchart

The microcontroller continuously samples Vout through the ADC at every trigger event. The ADC values are converted and compared with the reference thresholds as explained in the previous chapter. When Vout exceeds the upper threshold, both gate signals are turned OFF, halting energy transfer. Conversely, when Vout drops below the lower threshold, the microcontroller reactivates the gate signals, resuming power delivery to the load.

The action of switching the converter to OFF and ON state is carried out by updating the values of the COM1 and COM4 registers of the timer HRTIMB [Appendix E]. The Table 5.2 and Figure 5.6(b) explains the gate signal generation for the the bang bang control.

To ensure converter is in its OFF state, COM1 and COM4 values are set greater than the Period Event value. This ensures that the high side switch never turns OFF whereas the low side switch never turn ON. This ensures the safe operation of the converter while preventing the transfer of power from the input to output side of the converter.

To switch the converter to its ON state, the initial configuration of the HRTIMB is restored by updating the COM1 and COM4 values.

5.7 Dyadic Digital Pulse Modulation

In the DDPM control mode, the high side and low side gate signals are initially configured for a 115 kHz switching frequency and 50% duty cycle.

In the STM32 implementation, the DDPM control was realized through bitwise operations and conditional toggling of gate drive signals within the HRTIM peripheral. The algorithm follows a deterministic dyadic pattern, ensuring uniform pulse distribution across each macro-period and maintaining predictable spectral characteristics. Figure 5.12 illustrates the flow of the DDPM algorithm as implemented in the STM32CubeIDE environment [Appendix F].

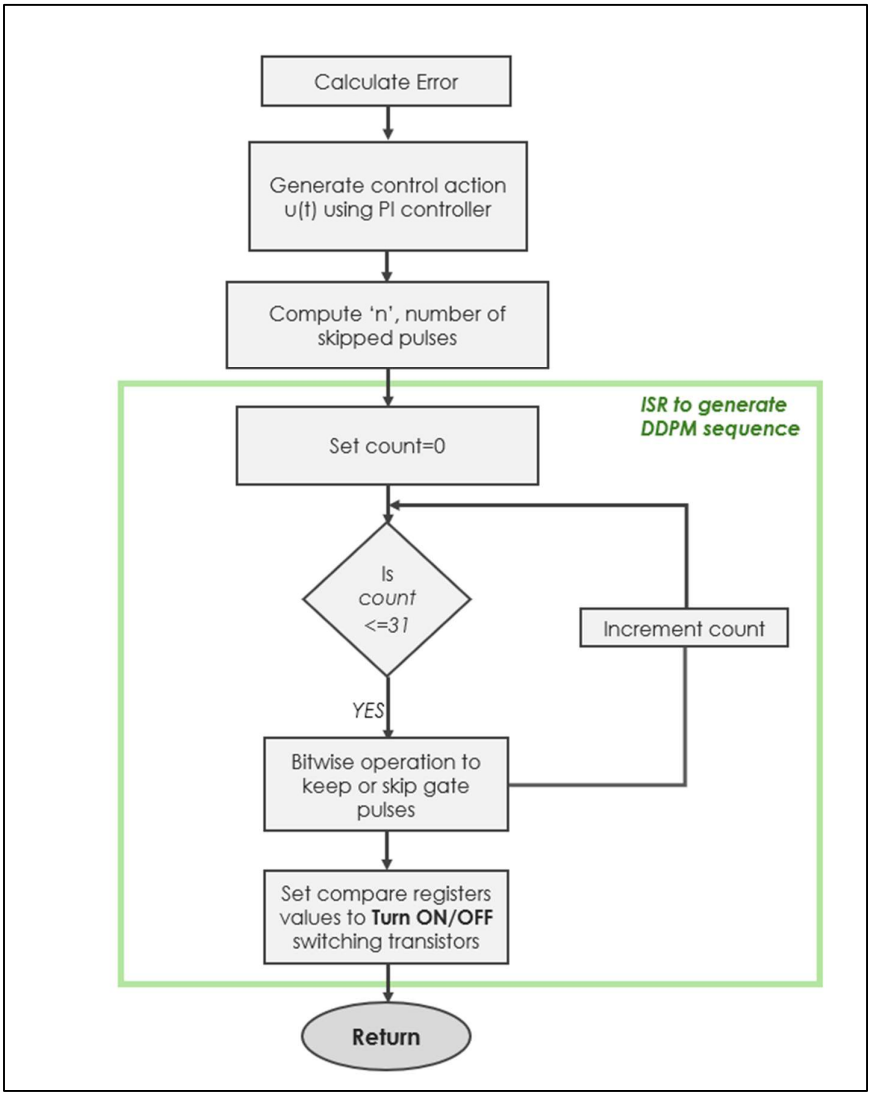


Figure 5.12: DDPM flowchart

The STM32 firmware implementation uses three main computational blocks:

a. Bit Reversal Loop: Reverses the binary representation of n to obtain a temporally balanced sequence, ensuring uniform spacing between active pulses.
b. Dyadic XOR and Masking Operation – Computes the bitwise logic necessary to determine whether each switching interval should be active or skipped, using the relationship:

$$count\_xor\_rightshift = ((cnt \oplus (cnt + 1)) >> 1) + 1$$

$$count\_and = count\_xor\_rightshift \,\&\, nrev\_final$$

   where cnt is the cycle counter, and n_rev_final is the bit-reversed representation of the control variable n.
c. Pulse Output Update: At each switching cycle, the HRTIM registers are updated based on count_and. If the result is non-zero, the converter enters ON state; otherwise, the pulse is skipped where the converter is in its OFF state.

To ensure converter is in its OFF state, COM1 and COM4 values are set greater than the Period Event value. This ensures that the high side switch never turns OFF whereas the low side switch never turn ON. This ensures the safe operation of the converter while preventing the transfer of power from the input to output side of the converter. To switch the converter to its ON state, the initial configuration of the HRTIMB is restored by updating the COM1 and COM4 values.

Chapter 6

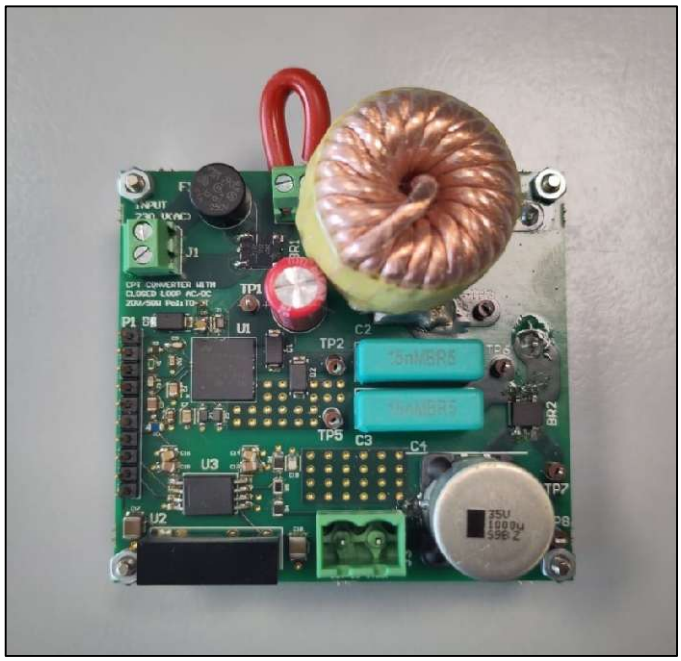
Simulation and Experimental results

This chapter presents the simulation and experimental validation of the control strategies implemented on the capacitively isolated DC–DC converter prototype. The experimental activities were conducted to evaluate the behavior of four different control techniques—Frequency Modulation (FM), Pulse Width Modulation (PWM), Bang–Bang (BB), and Dyadic Digital Pulse Modulation (DDPM)—applied to the Multi-Period Damped Resonant (MPDR) converter.

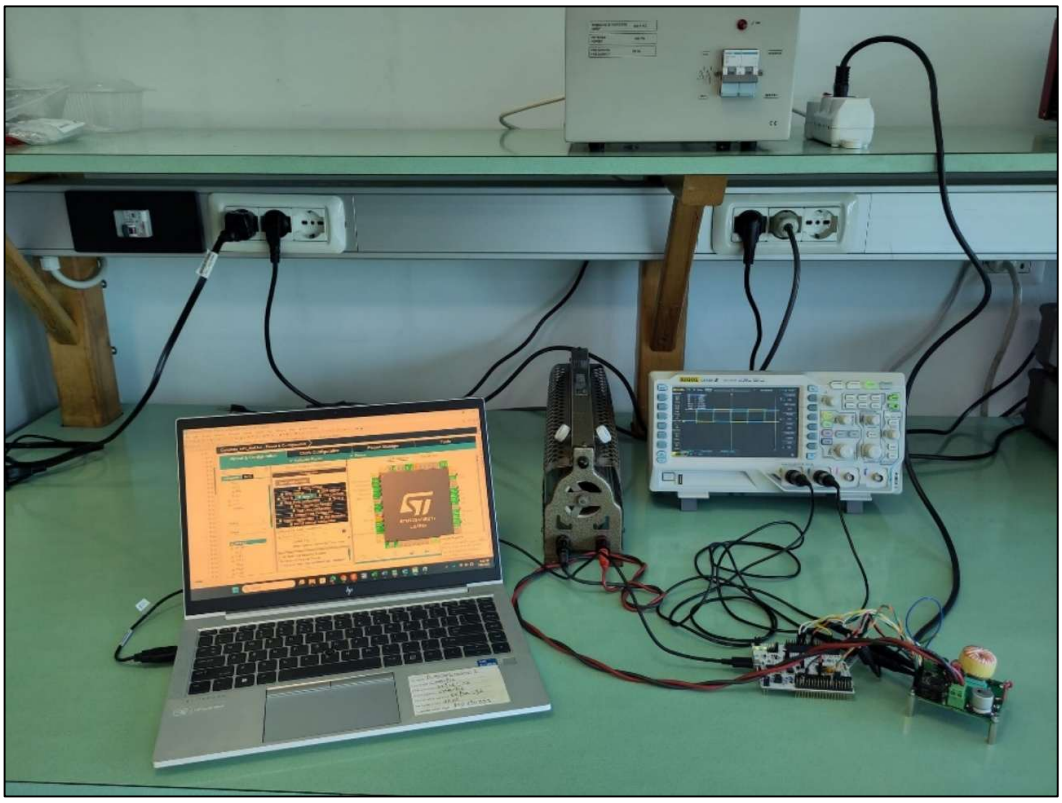
The list of equipment used during the experimental phase of this thesis is listed in the Table 6.1.

Equipment	Description
Microset TSR1000	High insulation Transformer with electrostatic shield: IN-OUT 230VAC-50Hz
RIGOL DP832	Programmable DC supply
RIGOL DL3021	DC Electronic load 150V/40A 200W
Rheostat	100Ω, 2A
RIGOL DM3058	Digital Multimeter $5\frac{1}{2}$ digits
TEKTRONIX P6021	60 MHz AC Current Probe
STM32CubeMX	STM32CubeMX is a graphical tool that allows a very easy configuration of STM32 microcontrollers.
STM32Cube IDE	An all-in-one multi-OS development tool, which is part of the STM32Cube software ecosystem.
The Prototype board	The Device under test (DUT)

Table 6.1: List of the equipment used for experiments



(a)



(b)

Figure 6.2: (a)The Prototype Board (b)Example setup used for open loop testing

6.1 Open Loop Characterization

The open loop analysis and characterization primarily aim to determine the operating range of the prototype board and verify the response of the system to different load conditions.

Preliminary open-loop simulations were carried out in LTSpice using the ideal component parameters derived from the prototype schematic (Figure 6.1). The main purpose of these simulations was to identify the operational limits of the converter and validate the expected range of behavior for the Frequency Modulation (FM) and Pulse Width Modulation (PWM) control strategies. The simulation results provided a theoretical reference to compare with experimental measurements obtained from the hardware setup.

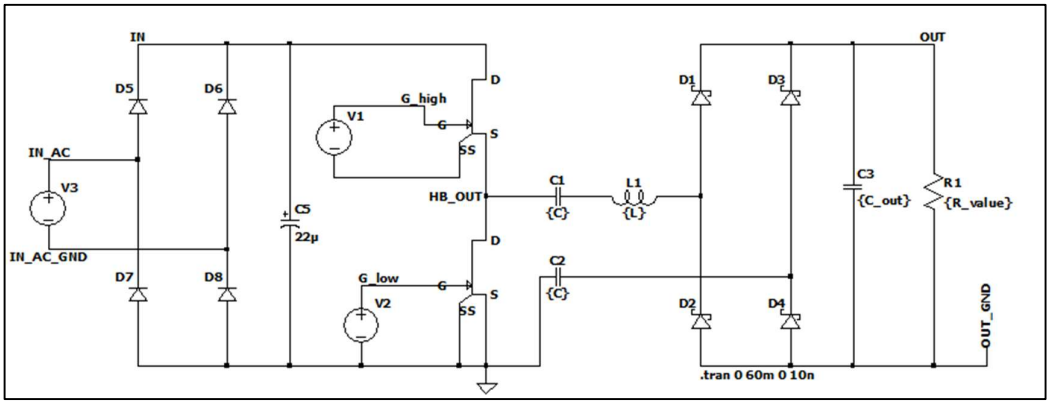
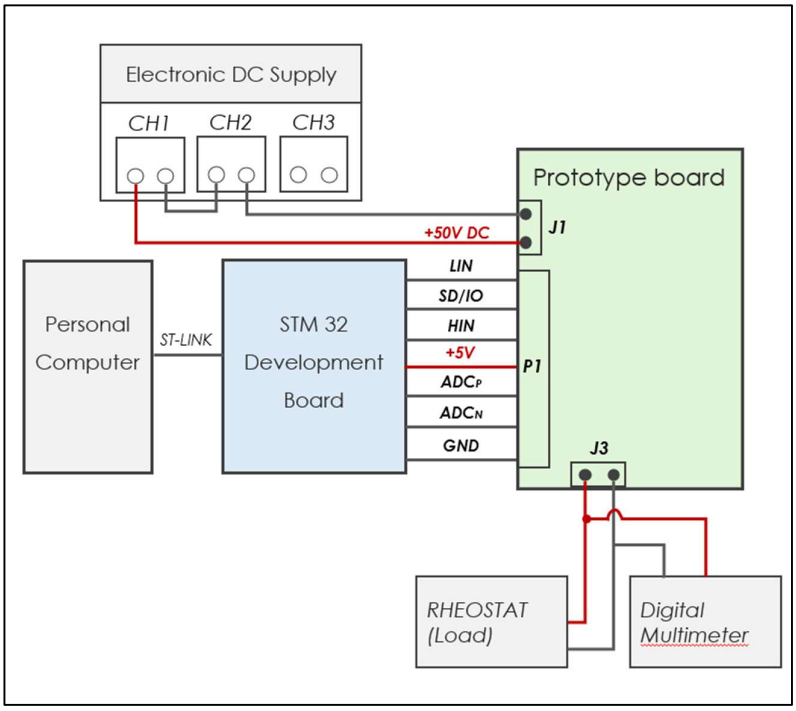
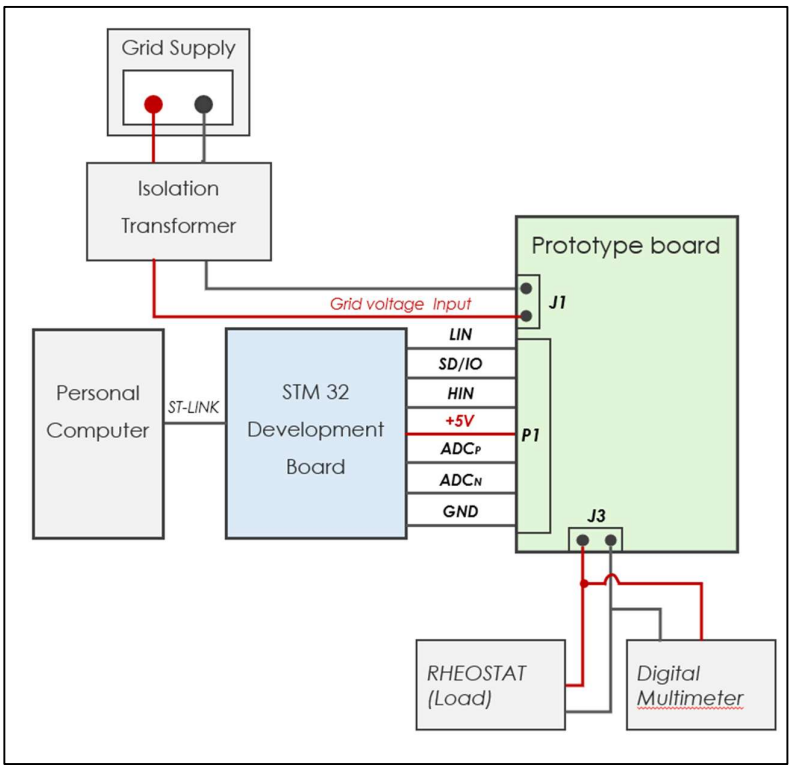


Figure 6.1: Simulation schematic used in LTspice

The open-loop experimental tests were performed using both low voltage (50V DC) and grid input (230VAC) conditions. The primary purpose was to validate the converter's steady-state behavior and identify the nominal operating voltage across the load range. The prototype board was powered with the input voltage, and the STM32 microcontroller generated the gate signals for the MASTERGAN1-based half-bridge stage.



(a)



(b)

Figure 6.3: Setup of the Open loop characterization (a)50V DC input (b)Grid voltage input

6.1.1 Low Voltage Input

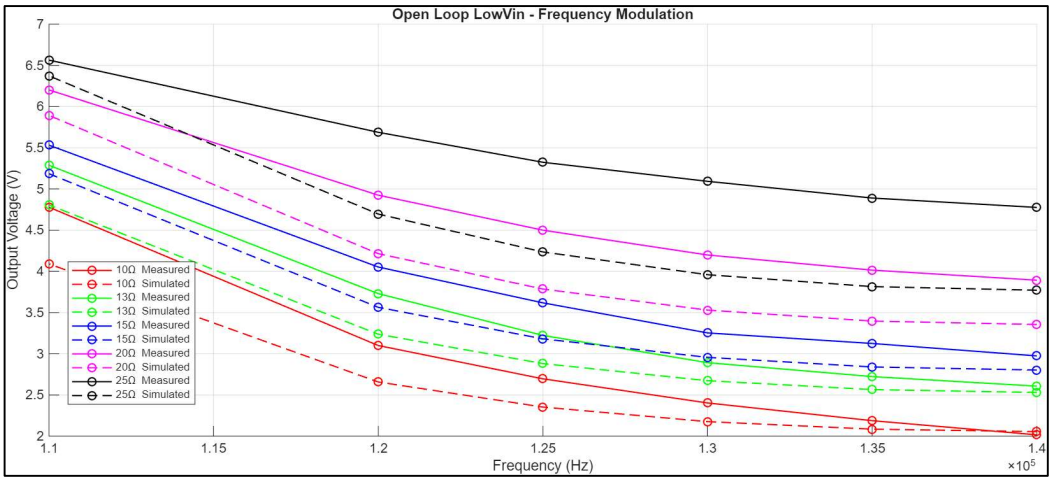


Figure 6.4: 50V input voltage - Open loop Output voltage vs switching frequency

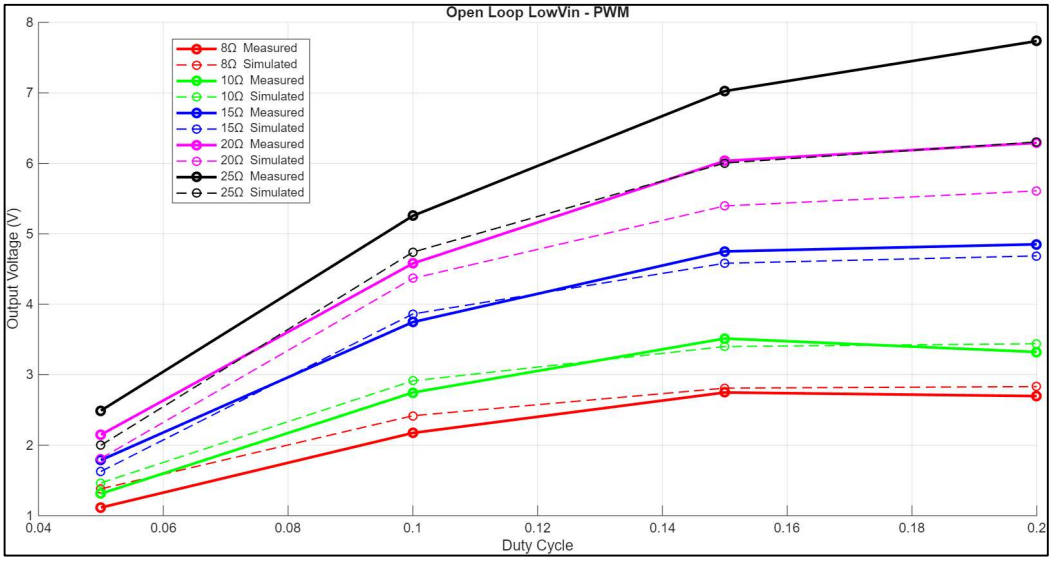


Figure 6.5: 50V input voltage - Open loop Output voltage vs duty cycle

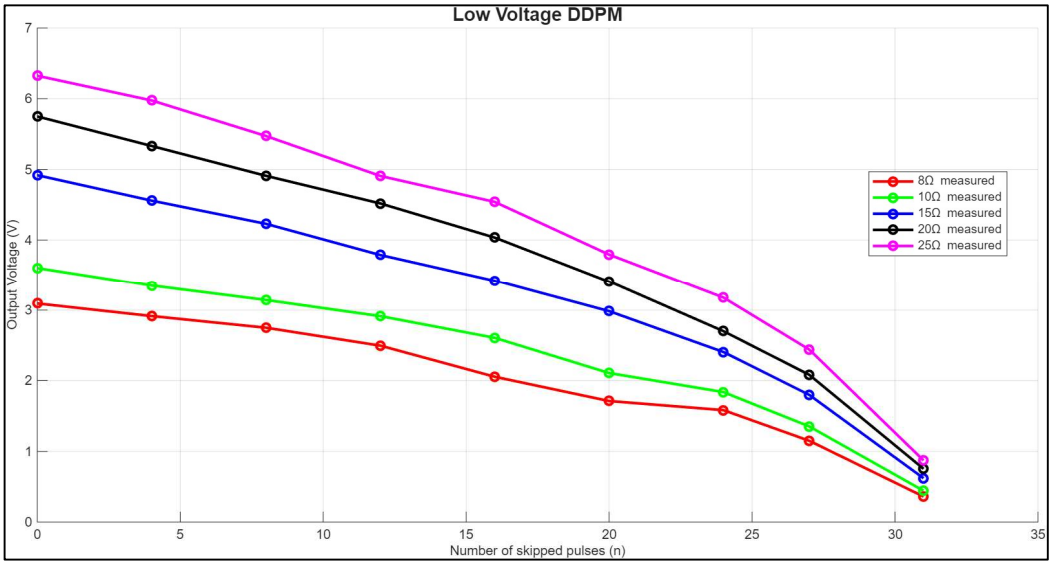


Figure 6.6: 50V input voltage - Open loop Output voltage vs No. of skipper pulses (n)

6.1.2 High voltage Input

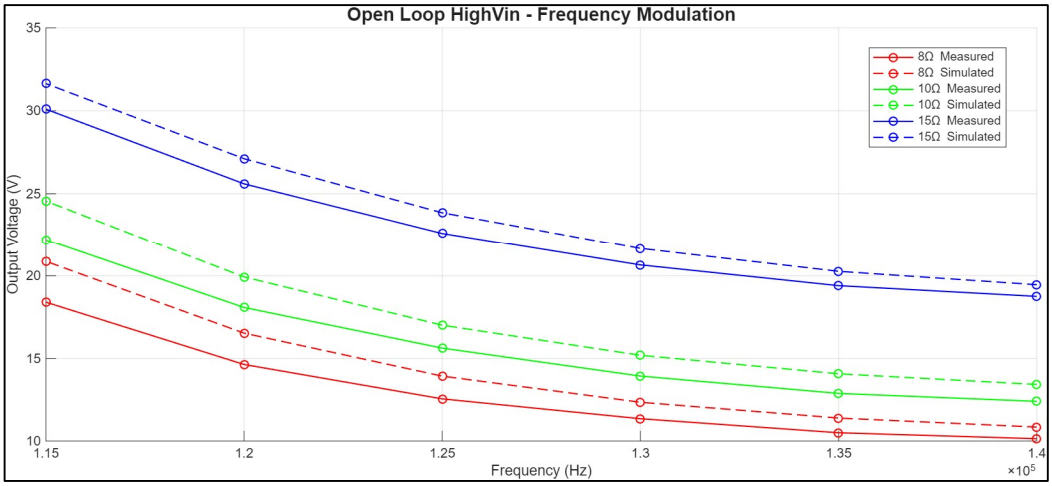


Figure 6.7: Grid input - Open loop Output voltage vs switching frequency

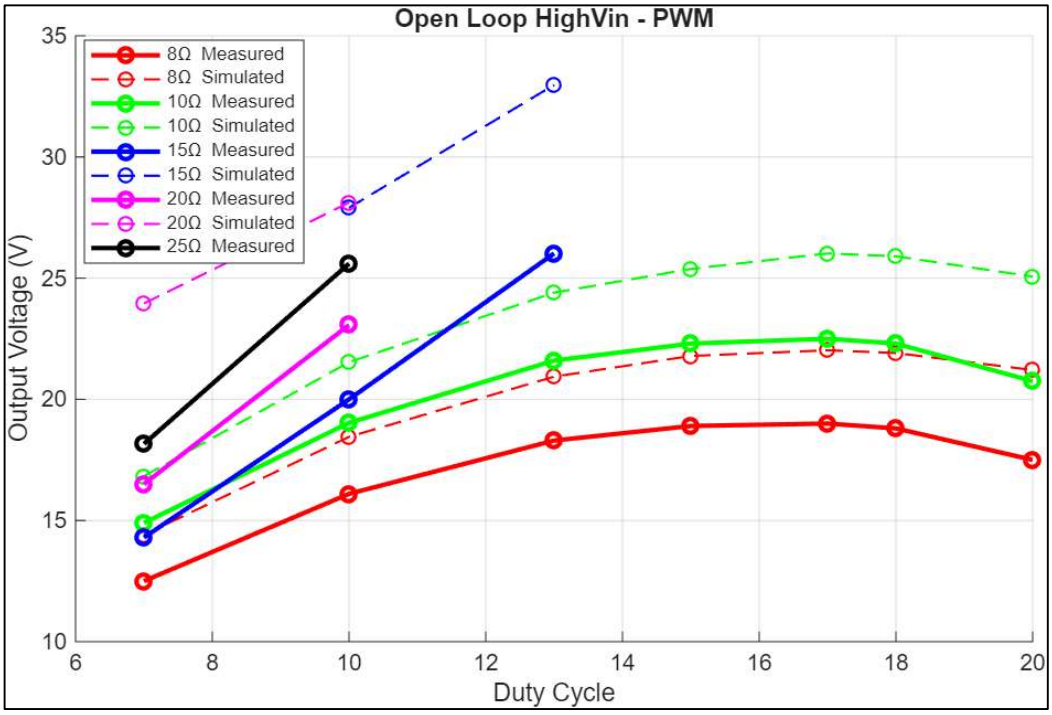


Fig 6.8: Grid input - Open loop Output voltage vs duty cycle

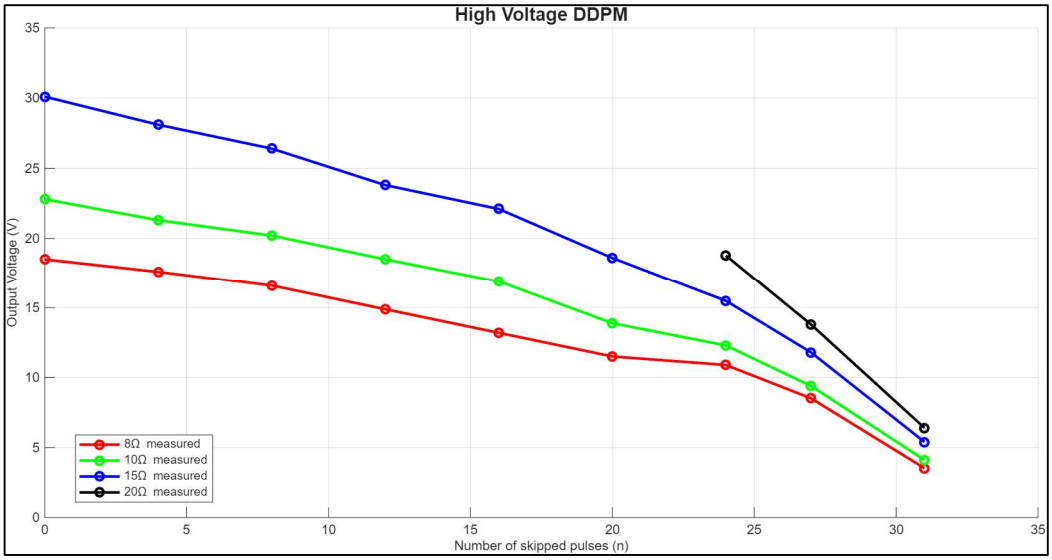


Figure 6.9: Grid input - Open loop Output voltage vs no. of skipped pulses (n)

6.1.3 Observations of Open loop experiments

As observed in Figure 6.7 and Figure 6.8, across all the test cases, the measured output voltages were consistently lower than the simulated results, primarily due to the absence of parasitic elements in the simulation models, such as stray inductance and equivalent series resistance (ESR), which slightly reduce the effective voltage transfer in the

practical setup. The primary scope of this test is to identify the nominal voltage in the low voltage condition. As observed in each control strategy, an output voltage of 3V is seen for load range of each control strategy. This validates the selection of Vref=3V for the closed loop experiments with low input voltage.

It is also interesting to note that the output voltage decreases with the increase in the switching frequency, but with increase in the duty cycle the output voltage increases. This explains the equations 4.3 and 4.6.

The open-loop simulations and experimental measurements with grid-level input voltage provide critical insights into the converter's dynamic response to variations in excitation frequency, duty ratio, and modulation pattern, allowing for the identification of the effective control range for each strategy. By observing how the output voltage responds to modulation changes, the study establishes the safe operating region for the hardware, ensuring that all subsequent closed-loop control experiments remain within the converter's thermal, voltage, and current limits. This established operating range for each control strategy is:

1. For the FM, load range is identified to be between 8Ω and 15Ω, where the switching frequency varied between 115kHz and 140 kHz.
2. For the PWM, load range is identified to be between 8Ω and 25Ω, the duty cycle ranged between 5%–20%.
3. For the DDPM, load range is identified to be between 8Ω and 20Ω, while the number of skipped pulses vary between 1 and 31 (for N=5)

This characterization thus serves as a benchmark for evaluating the stability, controllability, and efficiency of the implemented control strategies under grid-representative operating conditions.

6.2 Closed Loop Characterization

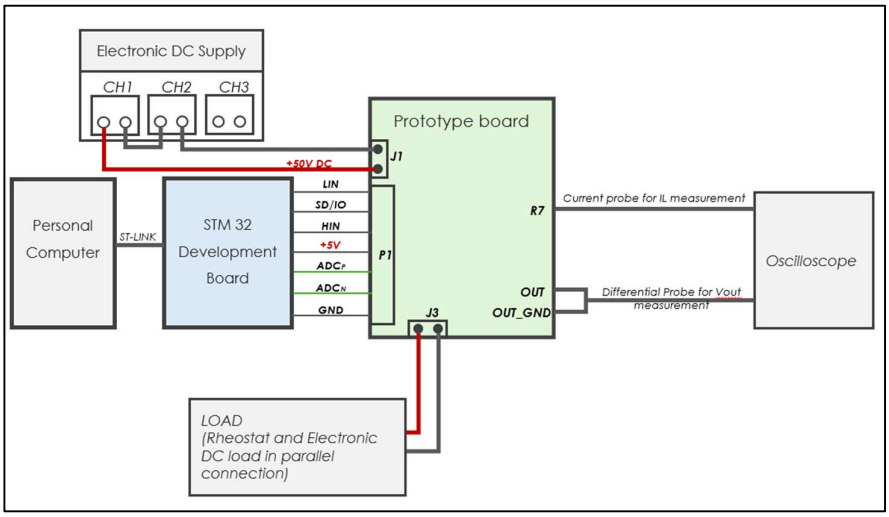
These experiments were conducted in the closed loop condition, to verify the dynamic behavior of the applied control methods under load-step conditions. An initial steady-state load is applied to the converter at the start of each experiment (R1), followed by a step change in load resistance (Rstep) and a subsequent return to the starting value (R1). The controller response is observed in terms of the output inductor current behavior and the output voltage regulation.

Control Strategy	Rheostat (R1) (at t=t0)	Electronic Load (R2) (at t=tstep)	Total Load (Rstep) (at t=tstep)
FM	15Ω	40Ω	11Ω
PWM	17Ω	25Ω	10Ω
Bang Bang	20Ω	25Ω	11Ω
DDPM	20Ω	25Ω	11Ω

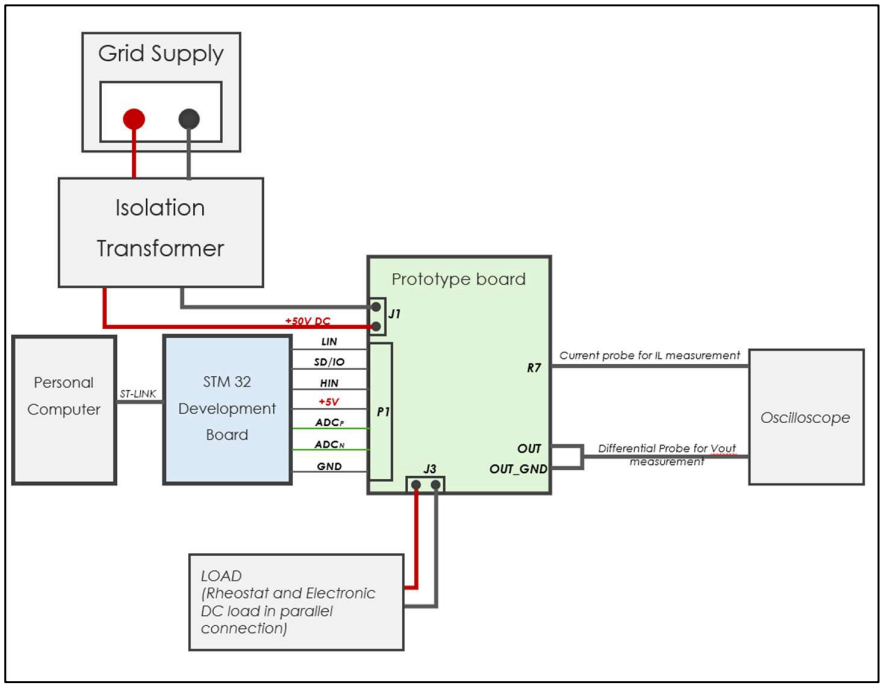
Table 6.2: Load step applied to the system

As shown in the Figure 6.10, the setup uses a parallel combination to for load stepping.

During the experiments, an unusual system behavior was observed when simply using a DC electronic load at the output. The reason for this can be anticipated to be that the electronic load introduces some non-linearities while imposing the load to the system. For example, during the frequency modulation open loop testing using the DC Electronic load, the saturation limit of control strategy was achieved for an R=11Ω and R=19Ω for the lower and upper limit of switching frequency. However, the saturation characterization, which was carried out by using the rheostat as the load, clearly shows the limits are achieved at R=11Ω and R=19Ω for the lower and upper limit of the switching frequency. And using the rheostat and electronic load in a parallel combination reduces the non-linear effect introduced by the electronic load.



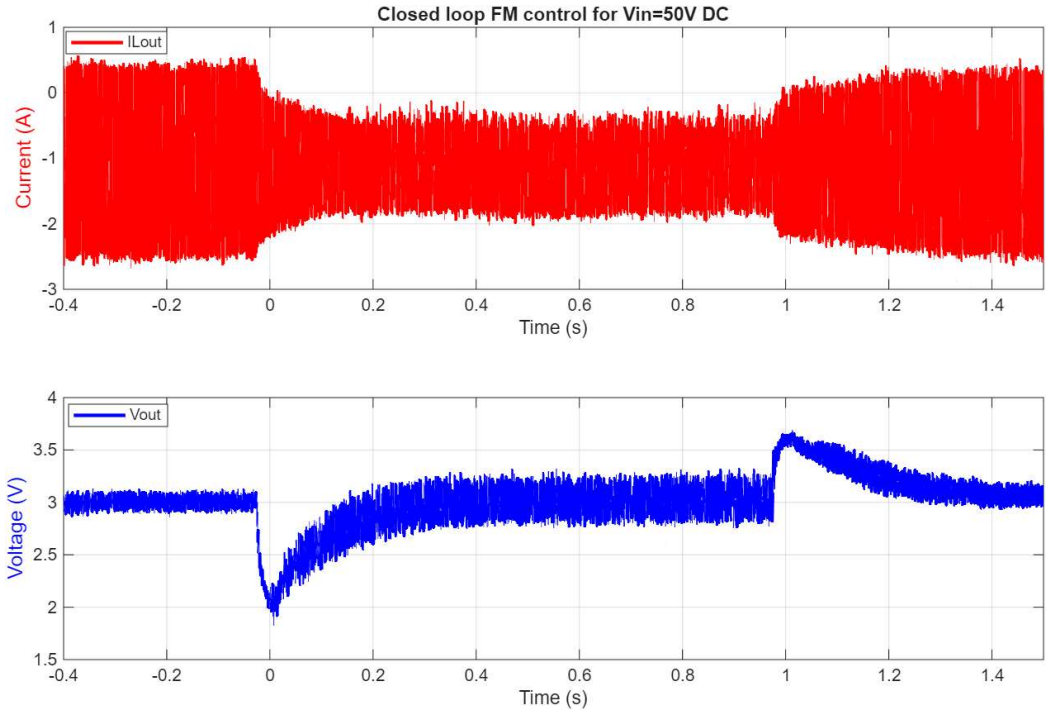
(a)



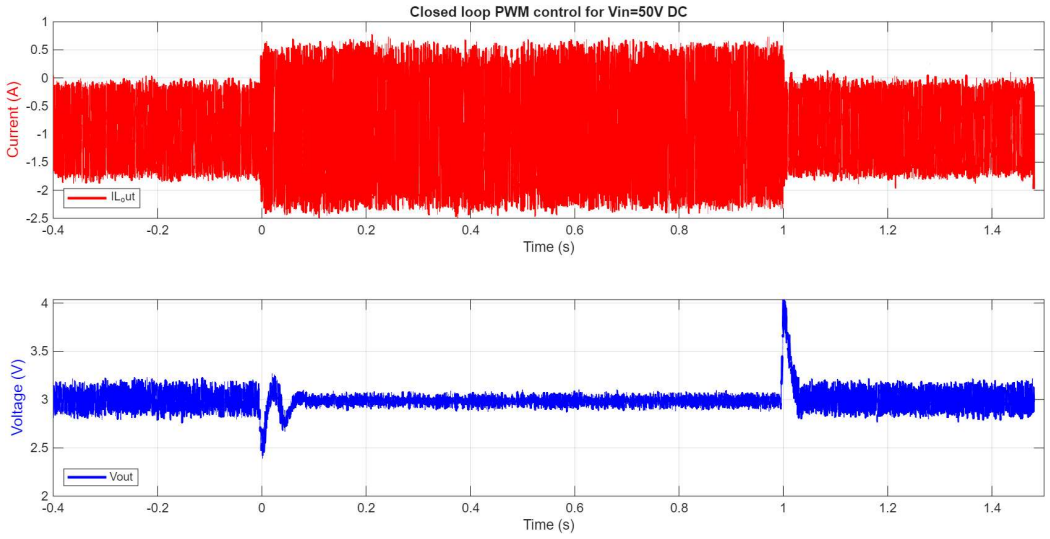
(b)

Figure 6.10: Setup of the Closed loop characterization (a)50V DC input (b)Grid voltage input

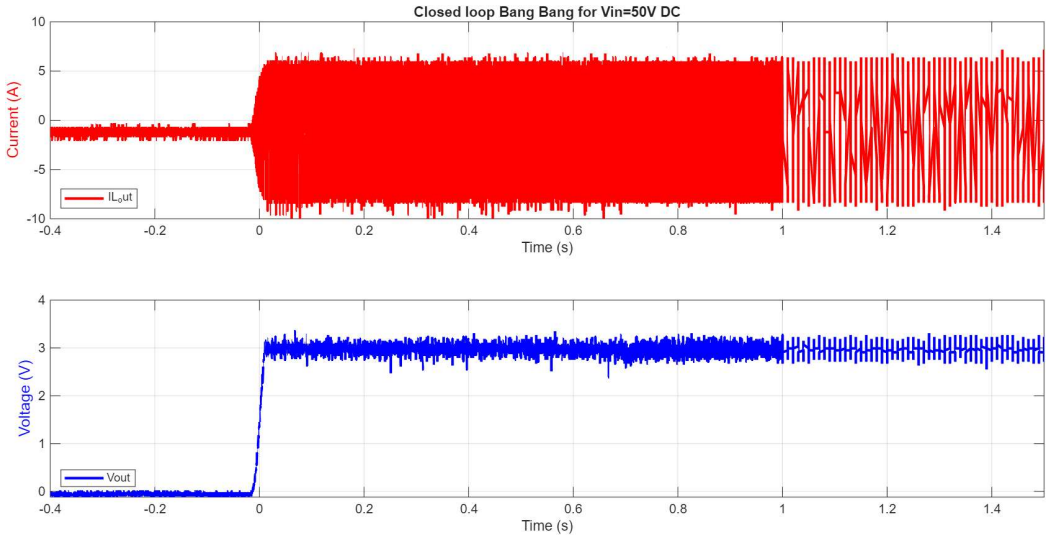
6.2.1 Low Voltage Input



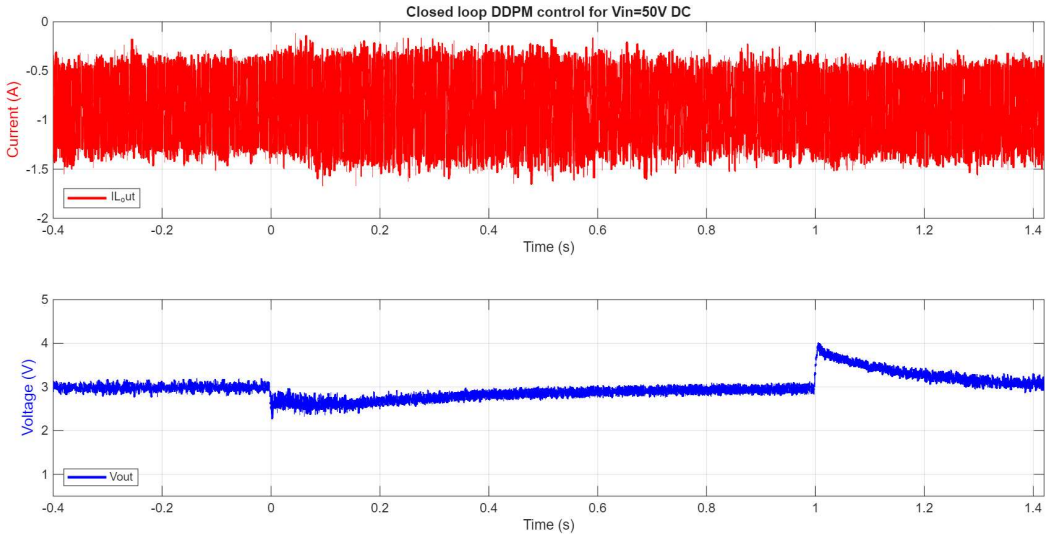
(a)


Closed loop PWM control for Vin=50V DC
Current (A)
Time (s)
Voltage (V)
Time (s)
Vout

(b)


Closed loop Bang Bang for Vin=50V DC
Current (A)
Time (s)
Voltage (V)
Time (s)
Vout

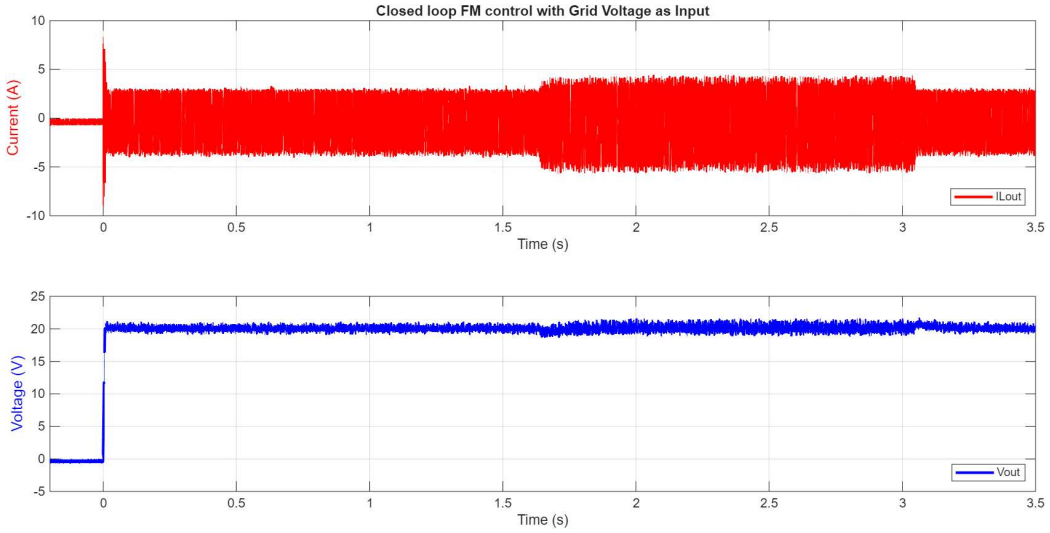
(c)



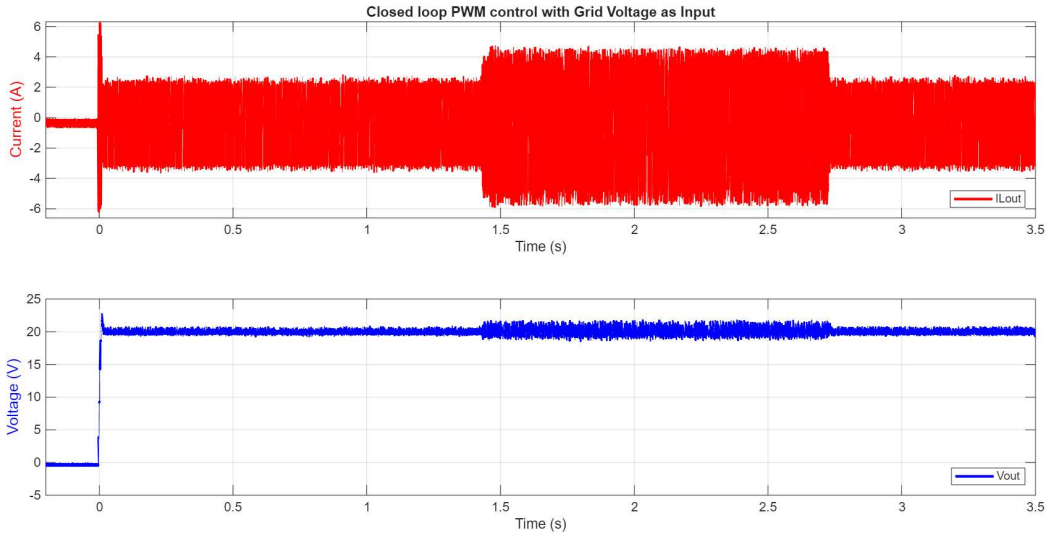
(d)

Fig 6.11: 50V DC input voltage – (a)Frequency Modulation control, (b) Pulse Width Modulation control, (c) Bang Bang Control, (d) DDPM control

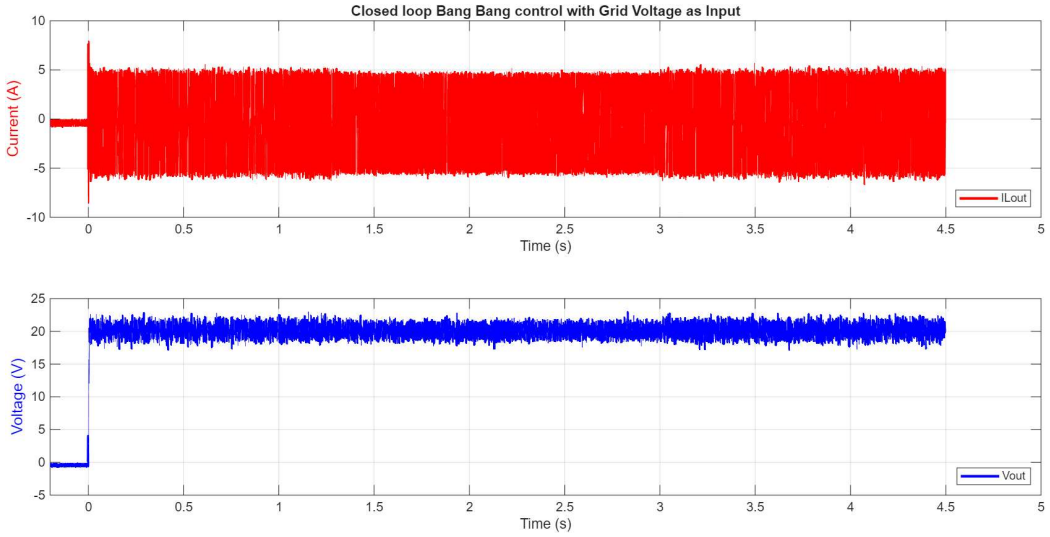
6.2.2 Grid voltage Input



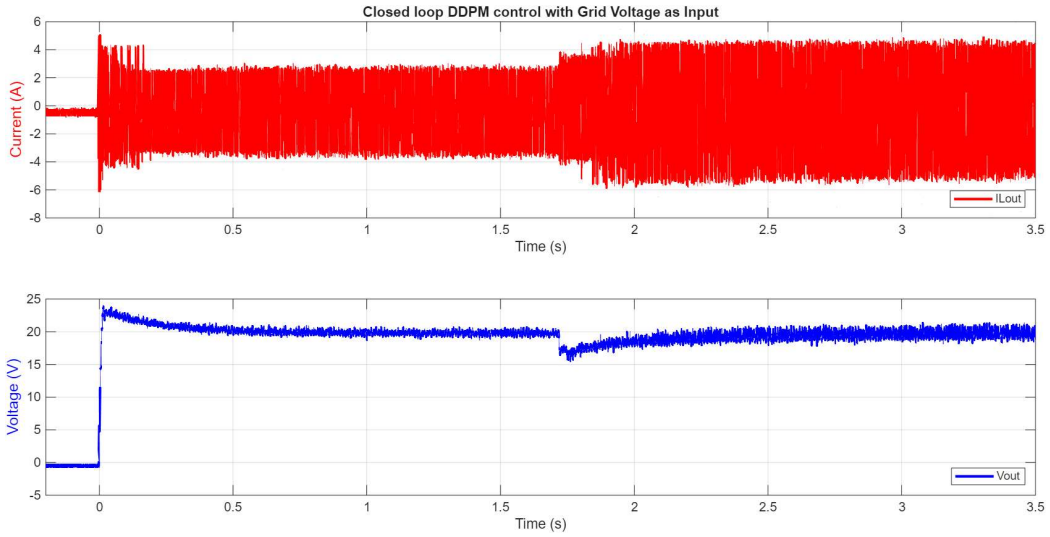
(a)


Closed loop PWM control with Grid Voltage as Input
Current (A)
Time (s)
ILout
Voltage (V)
Time (s)
Vout

(b)


Closed loop Bang Bang control with Grid Voltage as Input
Current (A)
Time (s)
ILout
Voltage (V)
Time (s)
Vout

(c)



(d)

Fig 6.12: Grid input – (a)Frequency Modulation control, (b)Pulse Width Modulation control, (c)Bang Bang Control, (d)Dyadic Digital Pulse Modulation control

6.2.3 Observations of Closed loop experiments

The closed-loop operation of the converter under frequency modulation (FM) control was evaluated for both low and grid input voltage conditions to examine its steady-state and transient performance.

For low input voltage, the FM shows the highest peak-to-peak ripple (approximately 500mV) with a significant transient peak at load variations. While the PWM shows much worse transient peak than the FM, the recovery to steady state is quicker with a lesser steady state ripple voltage. The bang bang observes smoother load transitions while producing a constant ripple that most likely the effect of the constant ON/OFF state of the converter. Whereas, the DDPM observes the longest recovery time and high peaks during load transition. Although different control strategies exhibit varying behaviour, they maintain the nominal 3V under all the load transitions.

With grid input, the control loops maintained a nominal 20 V output under all load transitions. The transient dynamics closely matched the low-voltage results for the bang bang and DDPM, confirming that control performance was largely load-dependent rather than input-dependent, for these strategies. The PWM however, exhibits a highly stable behavior during load transients with minimal transient peaks and nominal voltage ripples. The FM shows a reduced ripple behavior while the recovery to steady state after a load transient remain smooth like in the low voltage conditions.

Comparison of efficiency and power based on different control strategies

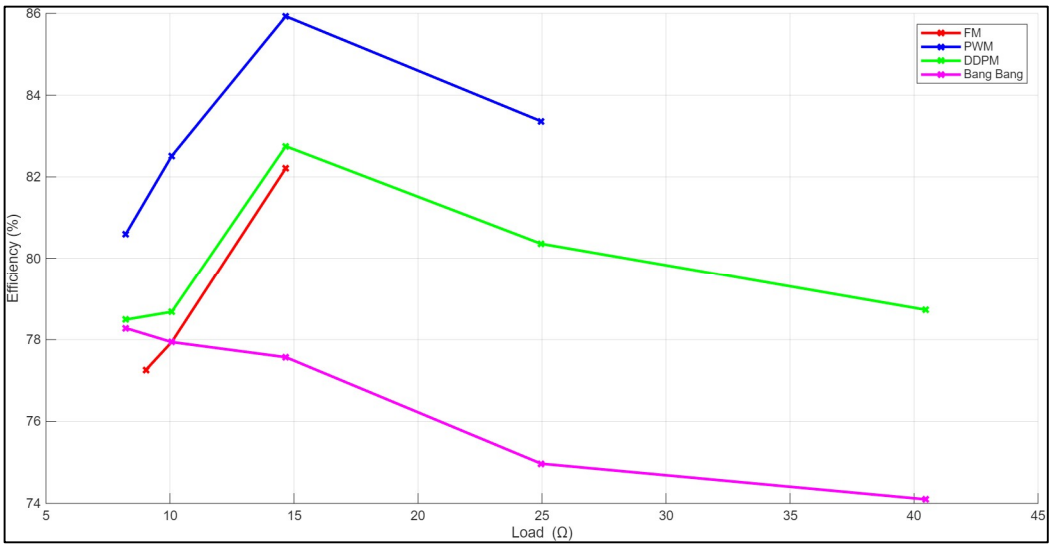


Figure 6.13: Efficiency (%) vs Load (Ω)

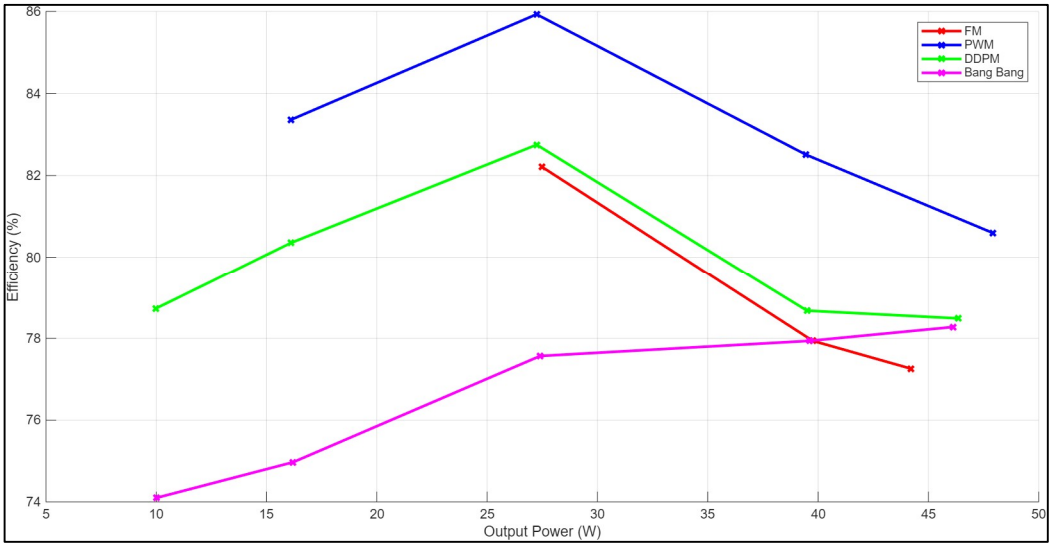


Figure 6.14: Efficiency (%) vs Output Power (W)

The peak efficiency for all control strategies employing a PI-based control loop (FM, PWM, and DDPM) occurs consistently at R = 15 Ω, corresponding approximately to rated power operation near 27W. This indicates that the controllers and the converter hardware are optimally tuned for this operating point, achieving ideal ZVS conditions and minimum switching losses. In contrast, the Bang Bang control achieves its highest efficiency at R = 8 Ω, after which efficiency steadily decreases due to higher switching frequency and current stress caused by the narrow hysteresis window.

PWM exhibits the highest peak efficiency of 86% owing to stable switching frequency and reduced circulating current losses. DDPM follows closely, with slightly lower efficiency attributed to its variable pulse density that introduces minor switching overhead across macro-periods. FM demonstrates comparable performance at medium and light loads but shows a steeper efficiency drop at higher load resistances, likely due to limited frequency tuning range and deviation from the optimal ZVS point at reduced load currents. The bang bang controller, though inherently simple and fast, shows the lowest overall efficiency trend. Its variable switching frequency leads to inconsistent ZVS maintenance and increased switching losses, particularly under lighter load conditions. The DDPM and bang bang controller shows a broader load operating range from R = 8Ω to R = 40Ω.

Chapter 7

Conclusion and Future work

This thesis successfully implemented and characterized four distinct digital control strategies: Frequency Modulation (FM) control, Pulse Width Modulation (PWM) control, Bang Bang (BB) control, and Dyadic Digital Pulse Modulation (DDPM) control, on a 50 W capacitively isolated MPDR DC-DC converter. Using the STM32 development board, both open-loop and closed-loop experiments were conducted under low-voltage (50V DC) and grid-input (230V AC) conditions.

The following key observations are derived from the closed loop experimental tests:

a. PWM and Bang Bang control exhibited the fastest recovery following load transitions. In contrast, FM and DDPM demonstrated smoother but slower recovery to the steady state condition. Despite the difference in recovery time, the output voltage is successfully regulated within the desired range of each control strategy.
b. The Bang Bang controller produced higher ripple owing to its hysteretic behavior, whereas the DDPM achieved the smoothest output with lower harmonic content.
c. As anticipated, the bang bang control which is inherently the simplest control methods, introduces higher voltage ripple due to the continuous regulation its imposes on the system.
d. The PI-based controllers (FM, PWM, DDPM) showed peak efficiency at the same load (R =15 Ω), achieving optimal ZVS and minimal switching loss. PWM achieved the best efficiency at 86%, while BB, though simple and fast, suffered from increased switching losses.

In conclusion, all four control methods successfully maintained voltage regulation within the desired output range, confirming stable closed-loop behavior. However, this work can be further extended to explore alternative control approaches and improve the converter's efficiency, scalability, and robustness under practical operating conditions. Several aspects remain open for development and optimization:

a. The design of the board limits the experimental validation is a 50 W output power. High-power scaling, thermal performance evaluation, and converter miniaturization aspects are beyond the present scope. The prototype PCB design was inherited from previous work and not optimized for parasitic minimization or EMI performance. Further modifications on the board design could implement high output power and the optimization of the PCB layout and components.

b. The PI controller co-efficients (ki and kp) can be further tuned to reduce the transient peak and the steady-state recovery time. The control strategies that were implemented focused on voltage mode control. Many other control technologies based on current-mode control or adaptive tuning can be explored as a future scope of the study of control strategies.
c. The experiments were conducted under controlled laboratory conditions. Environmental factors such as temperature variation, long-term drift, and real-grid disturbances were not evaluated. Future studies could integrate thermal cycling and noise-perturbed grid simulations to assess the long-term reliability and electromagnetic immunity of the system.

Appendix

Appendix A:

```
/* read and compute output voltage using ADC*/
if (isADCFinished==1)
isADCFinished=0;
ADC_Value=HAL_ADC_GetValue(&hadc1);
ADC_fraction= (float) ADC_Value/4095*2;//3970
ADC_Diff_value=(ADC_fraction-1)*3.2751;
Vout=ADC_Diff_value/Gain_conv;
```

Appendix B:

```
/* PI control */
error=Vref-Vout; //compute error
proportional=kp*error;
tentative_integral=ki*error*T_switching;
integral=old_integral+tentative_integral;
PI_out=proportional+integral; //compute pi output
/* Integral anti-windup & saturation limit*/
if (PI_out<-10)
        {
         PI_out=-10;
         integral=old_integral;
        }
else if (PI_out>10)
        {
         PI_out=10;
         integral=old_integral;
        }
old_integral=integral;
```

Appendix C: Frequency modulation

```
/* compute and set frequency & period values from PI_out */
new_Fsw=((f_max+f_min)/2)-(PI_out*(f_max-f_min)/20);
new_PERIOD=5.44e9/new_Fsw; //new period corresponding to new frequency
```

```
newCOMP1=(new_PERIOD*0.5)-dT_PERIOD; //recalculate comp values
newCOMP2= new_PERIOD*0.5;
newCOMP3=new_PERIOD-dT_PERIOD;
Period_switching=new_PERIOD; //new period is stored for next computation cycle
__HAL_HRTIM_SETPERIOD(&hhrtim1, 0x0, new_PERIOD);
__HAL_HRTIM_SETCOMPARE(&hhrtim1,0x1,HRTIM_COMPAREUNIT_1,newCOMP1);
__HAL_HRTIM_SETCOMPARE(&hhrtim1,0x1,HRTIM_COMPAREUNIT_3,newCOMP3);
__HAL_HRTIM_SETCOMPARE(&hhrtim1,0x1,HRTIM_COMPAREUNIT_2,newCOMP2);
```

Appendix D: PWM

```
/*compute duty-cycle*/
dutycycle=((duty_max+duty_min)/2)+PI_out*((duty_max-duty_min)/20);
Ton_period=dutycycle*Period_switching;
newCOMP1=Ton_period-dT_PERIOD;
newCOMP2=Ton_period;
/*set the new compare values*/
__HAL_HRTIM_SETCOMPARE(&hhrtim1,0x1HRTIM_COMPAREUNIT_1, newCOMP1);
__HAL_HRTIM_SETCOMPARE(&hhrtim1,0x1,HRTIM_COMPAREUNIT_2,newCOMP2);
```

Appendix E: Bang Bang

```
/* bangbang control logic */
if (Vout>V_upperlimit)
{
__HAL_HRTIM_SETCOMPARE(&hhrtim1, 0x1, HRTIM_COMPAREUNIT_1, 55100);
__HAL_HRTIM_SETCOMPARE(&hhrtim1, 0x1, HRTIM_COMPAREUNIT_4, 55333);
}
else if (Vout<V_lowerlimit)
{
__HAL_HRTIM_SETCOMPARE(&hhrtim1, 0x1, HRTIM_COMPAREUNIT_4, 47304);
__HAL_HRTIM_SETCOMPARE(&hhrtim1, 0x1, HRTIM_COMPAREUNIT_1, 544);
}
```

Appendix F: DDPM

```
/* calculate number of skipped pulses from the control action PI_out */
n=((10-PI_out)/20)*((pow(2,N))-1);
```

```
/* Implementing the calculated number of skipped pulses */
if (hhrtim->Instance == HRTIM1 && TimerIdx == HRTIM_TIMERINDEX_TIMER_B)
{
cnt = cnt+1;
if (cnt > 31)
{
  cnt = 0;
}
n_reversed=0;
for (int i = 0; i < N; i++)
{
 bit = (n >> i) & 0x01;
 n_reversed |= (bit << ((N-1) - i));
}
n_rev_final=n_reversed;
count_xor_rightshift=(((cnt ^ (cnt+1)) >> 1) + 1);
count_and= count_xor_rightshift & n_rev_final;
if(cnt<31)
{
 if (count_and)
 {
  /*Skip the pulse*/
  __HAL_HRTIM_SETCOMPARE(&hhrtim1, 0x1, HRTIM_COMPAREUNIT_1, 55100);
  __HAL_HRTIM_SETCOMPARE(&hhrtim1, 0x1, HRTIM_COMPAREUNIT_4, 55333);
 }
 else
 {
 /*Keep the pulse*/
  __HAL_HRTIM_SETCOMPARE(&hhrtim1, 0x1, HRTIM_COMPAREUNIT_4, 47260);
  __HAL_HRTIM_SETCOMPARE(&hhrtim1, 0x1, HRTIM_COMPAREUNIT_1, 500);
 }
}
else if (cnt==31)
```

```
{
 if (count_and)
 {
  /*Skip the pulse*/
  __HAL_HRTIM_SETCOMPARE(&hhrtim1, 0x1, HRTIM_COMPAREUNIT_1, 55100);
  __HAL_HRTIM_SETCOMPARE(&hhrtim1, 0x1, HRTIM_COMPAREUNIT_4, 55333);
 }
 else
 {
 /*Keep the pulse*/
   __HAL_HRTIM_SETCOMPARE(&hhrtim1, 0x1, HRTIM_COMPAREUNIT_4, 47260);
   __HAL_HRTIM_SETCOMPARE(&hhrtim1, 0x1, HRTIM_COMPAREUNIT_1, 500);
 }
}
```

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