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Master's degree in Electrical Engineering

Design, Characterization, and Comparison of V_{DS} Conditioning Circuits for Silicon-Carbide Power MOSFETs

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Abstract

In recent years, rapid technological progress coupled with the necessity to concentrate large amounts of energy in increasingly constrained space, and hence in high power density devices, has rendered thermal management and subsequent heat dissipation in electronic systems critical. In particular, the junction temperature of SiC semiconductors has become a fundamental parameter for proper design, ensuring both safety and long-term operational reliability in power applications. Conventional monitoring methods, such as infrared systems, provide an accurate estimate of the MOSFET case temperature but fall short in enabling real-time monitoring of the actual temperature of the individual internal junctions. This limitation is critical, as the true junction temperature represents the genuine indicator of the device's thermal state and, consequently, its reliability.

The study proposed in this thesis focuses on the realization and comparison of dedicated online monitoring circuits based on Temperature-Sensitive Electrical Parameters (TSEP); more specifically, it investigates the use of the on-state voltage, $V_{DS(on)}$, of the device under test (DUT). The underlying concept is based on the possibility of utilizing $V_{DS(on)}$, a parameter that is inherently sensitive to thermal variations, to monitor the DUT's junction temperature through its parametrization with respect to temperature. It is important to note that, although this approach originates from a thermal phenomenon, the present work focuses exclusively on the initial phase: a detailed comparison of different online monitoring circuits for $V_{DS(on)}$.

The objective is to evaluate and compare various circuit configurations, both in the ideal case (using generic components available in LTSpice) and in the realistic case (through the employment of realistic component models based on the original schematics), with the aim of highlighting the advantages and disadvantages of one configuration over another. In particular, the comparison targets the search for the optimal trade-off among measurement precision, voltage waveform volatility, bandwidth, and dynamic performance. For the experimental analysis, the DUT is modeled in LTSpice as a square-wave voltage source that faithfully emulates the switching behavior of an NMOSFET.

Through extensive simulations in LTSpice and subsequent comparative analyses of the ideal and real implementations, this thesis aims to establish an optimal balance between monitoring accuracy and dynamic performance, thereby identifying technical criteria that can guide the practical adoption of such circuits in real operational environments.

Contents

Chapter 1

Introduction

1.1 Fundamentals and Importance of Temperature in Electronic Devices

In electronic systems, which involve not only power semiconductor devices but also a wide range of active and passive components, the management of energy dissipation is a cornerstone for overall performance and long-term reliability. Energy is lost during both conduction and switching operations. In particular, conduction losses are expressed by the relation

$$P_{\text{cond}} = I^2 \cdot R_{\text{DS(on)}},$$

where $R_{\text{DS(on)}}$ represents the device's on-state resistance. During switching, additional losses occur due to the transient overlap of voltage and current, and these switching losses can be approximated by

$$P_{\text{sw}} = \frac{1}{2} V_{\text{DS}} I_{\text{D}} \left(t_{\text{rise}} + t_{\text{fall}}\right) f_{\text{sw}},$$

where V_{DS} is the applied voltage, I_{D} is the conduction current, t_{rise} and t_{fall} denote the rise and fall times respectively, and f_{sw} is the switching frequency. It is also important to note that overvoltage conditions may trigger avalanche phenomena, leading to uncontrolled energy release.

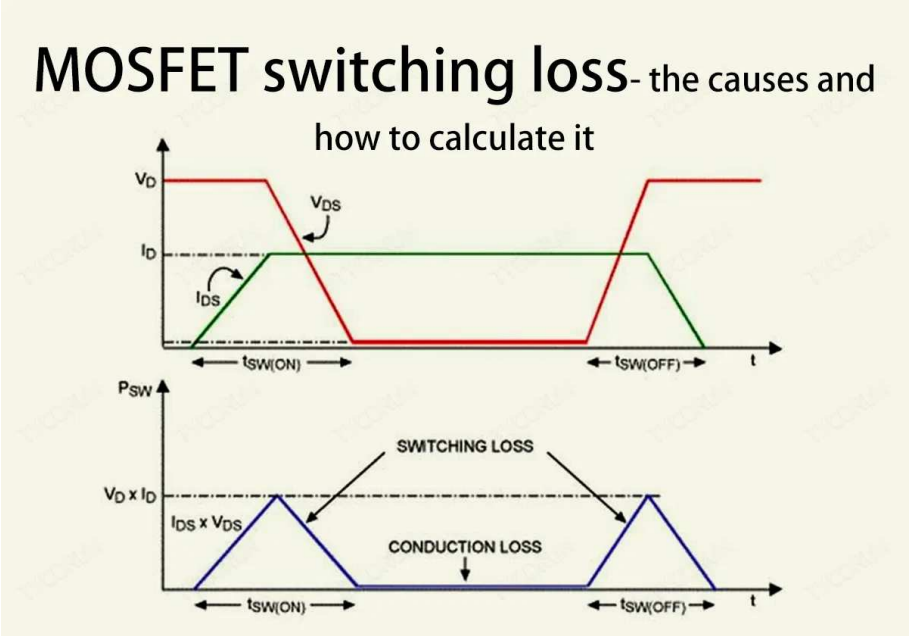


Figure 1.1: Graphic explanation of the switchinglosses.

1.1.1 Thermal Transfer Modeling

Efficient removal of the generated heat is essential to maintain safe operating conditions. The thermal path is commonly modeled by analogy with an electrical circuit, where the temperature difference acts as a "thermal voltage" and the heat flow as a "thermal current." In this context, thermal resistance—expressed in Kelvin per Watt (K/W)—quantifies the temperature rise per unit of power dissipated.

Typically, the thermal path from the active die to the ambient environment is divided into two fundamental segments:

1. **From the Junction to the Case:**
   Heat is transferred from the semiconductor die to the device case. This temperature drop is characterized by the junction-to-case thermal resistance, denoted as $R_{\text{th(jc)}}$. In this context, the junction temperature, Θ_j, represents the point of maximum thermal stress.

2. **From the Case to the Ambient:**
   Subsequently, heat is dissipated from the device case to the surrounding ambient. This stage is described by the case-to-ambient thermal resistance, $R_{\text{th(ca)}}$, where the case temperature is denoted by Θ_c and the ambient temperature by Θ_a.

Therefore, the overall thermal resistance from the junction to the ambient is given by:

$$R_{\text{th(ja)}} = R_{\text{th(jc)}} + R_{\text{th(ca)}}.$$

It is important to note that when a heatsink is employed to enhance heat dissipation, the transfer path is modified. In such a configuration, the case-to-ambient resistance $R_{\text{th(ca)}}$ is replaced by the sum of the resistances from the case

to the heatsink, $R_{\text{th(ch)}}$, and from the heatsink to the ambient, $R_{\text{th(ha)}}$. The overall thermal resistance then becomes:

$$R_{\text{th(ja)}} = R_{\text{th(jc)}} + R_{\text{th(ch)}} + R_{\text{th(ha)}}.$$

To capture the dynamic behavior of the thermal response, the thermal capacitance C_{th} (in J/K) is introduced. This parameter quantifies the ability of the device to store heat. The combination of $R_{\text{th(ja)}}$ and C_{th} yields the thermal time constant:

$$\tau_{\text{th}} = R_{\text{th(ja)}} \cdot C_{\text{th}},$$

which represents the time required for the system to reach a steady state after a change in power dissipation. Manufacturers also provide normalized thermal impedance curves, $Z_{\text{th}}(t)$, which elegantly integrate both the resistive and capacitive aspects of the thermal path.

Dynamic Thermal Impedance $\boldsymbol{Z_{\text{th}}(t)}$

The function $Z_{\text{th}}(t)$ represents the dynamic thermal response of the system and is obtained by combining the overall thermal resistance $R_{\text{th(ja)}}$ and the thermal capacitance C_{th} according to an RC circuit model. For a single-pole system, the thermal impedance as a function of time can be expressed as:

$$Z_{\text{th}}(t) = R_{\text{th(ja)}} \left(1 - e^{-\frac{t}{\tau_{\text{th}}}}\right),$$

where $\tau_{\text{th}} = R_{\text{th(ja)}} \cdot C_{\text{th}}$ is the thermal time constant. This expression shows that at $t = 0$ the thermal impedance is zero, while as $t \to \infty$ it converges to the static value $R_{\text{th(ja)}}$. In this way, $Z_{\text{th}}(t)$ provides a comprehensive picture of the transient response following a sudden change in dissipated power, integrating both resistive and capacitive effects.

1.1.2 Summary of Key Thermal Parameters

The table summarizes the parameters required to move efficiently from theoretical analysis to practical temperature calculations across operating conditions, indicating units and the practical role of each term in the thermal path.

1. A rapid comparison between steady-state contributions (thermal resistances) and dynamic contributions (thermal impedance $Z_{\text{th}}(t)$ and thermal capacitance C_{th}), useful for heatsink sizing and transient management.

2. The compilation of analytical data serves as a reference for constructing a generic thermal simulation, enabling estimation of the thermal-circuit time constants and the determination of $Z_{\text{th}}(t)$ and τ_{th}.

Parameter (Unit) :	**Description**
P_{cond} (W)	Conduction losses, proportional to the square of the current and $R_{\text{DS(on)}}$.
$R_{\text{DS(on)}}$ (Ω)	On-state resistance of the device, determining conduction losses.
$R_{\text{th(jc)}}$ (K/W)	Thermal resistance from the junction to the case, defining the internal temperature drop.
$R_{\text{th(ca)}}$ (K/W)	Thermal resistance from the case to ambient in the absence of a heatsink.
$R_{\text{th(ch)}}$ (K/W)	Thermal resistance from the case to the heatsink (applicable when using a heatsink).
$R_{\text{th(ha)}}$ (K/W)	Thermal resistance from the heatsink to the ambient.
$R_{\text{th(ja)}}$ (K/W)	Total thermal resistance from the junction to the ambient, the sum of the resistances along the thermal path.
$Z_{\text{th}}(t)$ (K/W)	Dynamic thermal impedance, describing the transient response that integrates the effects of $R_{\text{th(ja)}}$ and C_{th}.
C_{th} (J/K)	Thermal capacitance of the device, indicative of its ability to store heat.
τ_{th} (s)	Thermal time constant, given by $R_{\text{th(ja)}} \cdot C_{\text{th}}$, representing the dynamic response time.
Θ_j (°C or K)	Junction temperature, the point of maximum thermal stress within the device.
Θ_c (°C or K)	Case temperature of the device.
Θ_a (°C or K)	Ambient temperature surrounding the device.

Table 1.1: Summary of Key Thermal Parameters

1.2 Importance of Junction Temperature

Junction temperature (T_j) of a power semiconductor device represents the temperature at the point of maximum thermal stress, located precisely on the die where active regions and metallurgical junctions are formed. This parameter is crucial not only for the immediate electrical performance of the device but also for its long-term operational reliability. In high-power applications, effective control of T_j is fundamental, as even minor thermal deviations can lead to performance variations, increased losses, or even premature failure.

Accurate knowledge and strict control of the junction temperature are essential for several reasons:

- **Drift in Electrical Parameters:**
  Electrical characteristics such as on-state resistance ($R_{\mathrm{DS(on)}}$), threshold voltage (V_th), and carrier mobility (μ) are inherently temperature-dependent. As T_j increases, carrier scattering becomes more pronounced, resulting in a reduction of mobility and an increase in $R_{\mathrm{DS(on)}}$. For example, a typical increase of 2–4% in $R_{\mathrm{DS(on)}}$ per 10 °C rise in T_j not only compromises conduction efficiency but also reduces the thermal margin, thereby pushing the device closer to critical operating conditions and potential instability.

- **Switching and Conduction Losses:**
  Elevated T_j enhances conduction losses due to the increased $R_{\mathrm{DS(on)}}$ and may adversely affect switching dynamics by altering rise and fall times, charge injection, and parasitic capacitance behaviors. These effects not only degrade conversion efficiency but also promote the accumulation of heat during switching transitions, thereby necessitating a redesign of the thermal budget and protection schemes.

- **Device Reliability and Lifetime:**
  The operational lifetime of semiconductor devices is strongly influenced by T_j and is commonly modeled using the Arrhenius equation:

  $$\mathrm{MTTF} \propto \exp\left(-\frac{E_a}{k\,T_\mathrm{j}}\right),$$

  where E_a is the activation energy and k is Boltzmann's constant. According to this relationship, an increase of 10 °C in T_j can approximately halve the Mean Time To Failure (MTTF), which signifies the average lifetime of the device. In other words, higher junction temperatures accelerate degradation processes—such as bond wire fatigue, die-attach delamination, and metal migration—thereby shortening the device's lifespan. The activation energy E_a serves as an indicator of thermal stability: higher values imply greater resistance to degradation, whereas lower values render the device more susceptible to failure.

- **Prevention of Thermal Runaway:**
  Thermal runaway is a self-reinforcing phenomenon that occurs in devices with

positive temperature coefficients. An initial increase in T_j causes higher power dissipation (for example, by increasing $R_{\mathrm{DS(on)}}$ and leakage currents), which in turn leads to further temperature rises. This positive feedback loop can drive T_j beyond safe operational limits, ultimately resulting in device failure. Real-time monitoring of T_j is essential to trigger protective measures—such as derating, active cooling, or automatic shutdown mechanisms—that can interrupt the runaway process before catastrophic damage occurs.

- **Packaging and System Design:**
  The thermal path from the die to the ambient environment comprises several interfaces, typically modeled by thermal resistances, such as junction-to-case resistance ($R_{\mathrm{th(j-c)}}$) and case-to-ambient resistance ($R_{\mathrm{th(c-a)}}$). These parameters determine how efficiently heat is transferred away from the device. Accurate estimation of T_j enables engineers to properly size heatsinks, select suitable thermal interface materials, and ensure compliance with international standards such as JEDEC JESD51. Underestimating the thermal resistances can lead to component oversizing or, worse, insufficient cooling.

- **Advanced Thermal Management Techniques and Usage of TSEP:**
  A rigorous thermal model supports the implementation of sophisticated management strategies that integrate both passive and active solutions. Among these, the use of dynamic thermal impedance $Z_{\mathrm{th}}(t)$ and real-time junction temperature estimation via Temperature-Sensitive Electrical Parameters (TSEP) are prominent. In particular, this thesis will focus on the development and comparison of online monitoring circuits based on $V_{\mathrm{DS(on)}}$—the TSEP of interest—to achieve an accurate and dynamic estimation of T_j in power devices, thereby enhancing system performance in high-density applications such as automotive traction inverters and aerospace converters.

In summary, the junction temperature is a key variable that links the electrical behavior of power devices to their thermal environment. Its monitoring and control are not merely desirable but are essential for ensuring system safety, extending component lifetime, and optimizing energy conversion efficiency across a wide range of operating conditions.

1.3 Objectives and Structure of the Work

The overall objective of this thesis is the identification and optimization of online measurement circuits for the voltage $V_{DS(on)}$ of a conducting MOSFET, which is recognized as a temperature-sensitive electrical parameter (TSEP). Although the study originates from a thermal challenge—the need to indirectly assess the junction temperature through variations in $V_{DS(on)}$—the core focus of this work is exclusively on the design, evaluation, and comparative analysis of the measurement circuits themselves. These circuits are considered the fundamental building blocks for obtaining reliable, repeatable, and embedded-system–compatible readings.

In contrast to traditional approaches that concentrate on the direct analysis of the device under test (DUT), this thesis focuses on the measurement circuitry with the aim of identifying the best compromise between measurement accuracy, circuit complexity, and robustness under realistic conditions. Moreover, if a full voltage–temperature calibration were performed that correlated $V_{DS(on)}$ to junction temperature, this could represent an interesting direction for future work.

The specific objectives of the thesis are structured as follows:

1. **Modeling and comparison of circuits under ideal conditions**
   In the first phase, several measurement circuits are designed and modeled. Each circuit features a distinct topology yet shares key elements such as a square-wave voltage generator (to simulate the dynamic behavior of the load) and a logic-level driving stage (essential for interfacing with digital signals produced by microcontrollers or programmable logic). The circuits are simulated under *ideal conditions* by assuming perfect components (i.e., without parasitic effects, losses, or delays) in order to highlight the theoretical performance of each architecture and compare their intrinsic capabilities.

2. **Realistic simulations and comparison with ideal cases**
   Subsequently, the same circuits are analyzed under *realistic conditions*. In this phase, non-idealities such as parasitic impedances, contact resistances, distributed capacitances, and realistic rise/fall times are introduced. This enables a rigorous comparison between the ideal and actual behavior of each circuit, quantifying sensitivity to non-ideal effects and identifying critical aspects of each solution.

3. **Cross-comparison of real circuits**
   After establishing the real-world performance of the individual circuits, a cross-comparative analysis is conducted. Each solution is evaluated in terms of:

   - **Accuracy** in measuring the actual $V_{DS(on)}$ of the MOSFET;
   - **Stability** and insensitivity to environmental and load variations;
   - **Frequency response** for each circuit;
   - **Compatibility** with digital logic and microcontroller-based data acquisition.

4. **Parametric optimization and trade-off analysis**
   The final phase involves deliberate modification of the circuits to improve their performance by:

   - varying the parameters of passive components (resistors, capacitors);
   - replacing active components with more suitable alternatives;
   - introducing topological changes to reduce parasitic effects or enhance signal margins.

   In addition to the above, in several cases some circuit components were substituted with model representations of existing commercial components, integrating characteristic parameters of real devices into the simulation models to obtain more realistic assessments. Through this optimization process the goal is to identify the best trade-off between measurement accuracy, circuit complexity, and robustness under realistic scenarios.

Final Objectives

- A systematic methodology for the evaluation and optimization of $V_{DS(on)}$ measurement circuits.
- A rigorous comparative analysis of different solutions under both ideal and realistic conditions.
- Identification of the best trade-off among measurement accuracy, circuit complexity, and cost, yielding an economically advantageous solution that is easily integrable into electronic circuits.
- Development of online monitoring systems aimed at correctly estimating and measuring the parameter $V_{DS(on)}$, which may, optionally (but not within the scope of the present work), be subjected to subsequent thermal parametrization to obtain a voltage–temperature calibration curve.

1.4 Thesis Structure

The thesis is organized into eight chapters as follows:

Chapter 1: Introduction Presents the motivation for real-time junction temperature monitoring, highlights thermal challenges in power semiconductors, and defines the scope and objectives of the work.

Chapter 2: Theoretical Background Reviews heat dissipation mechanisms (conduction, convection, radiation), thermal modeling (Θ_{JC}, Θ_{CA}, $Z_{\mathrm{th}}(t)$), and the concept of Temperature Sensitive Electrical Parameters, with particular attention to $V_{\mathrm{DS(on)}}$.

Chapter 3: Methodology Describes four conditioning circuits in ideal cases, the simulation parameters, the calibration strategy, and the different solutions for implementing real component models in LTspice.

Chapter 4: Simulations and Results — Ideal Circuits Details the configuration and performance results for each ideal circuit topology, followed by a comparative discussion of estimation accuracy and dynamic behavior.

Chapter 5: Selection and Placement of Real Components and Model Analysis Describes the selection and placement of real components in the adopted configurations and provides circuit-level analysis of the models, highlighting the differences with the previous ideal approach.

Chapter 6: Frequency Analyses of the Circuits Presents the frequency analyses of each circuit with the aim of determining their cutoff frequencies and bandwidths.

Chapter 7: Comparative Analysis of Real Circuits Compares all real-component implementations in order to evaluate the best trade-off between measurement accuracy and circuit complexity.

Chapter 8: Conclusions and Future Work Summarizes the main results, draws conclusions on circuit performance, and proposes possible directions for further research and industrial application.

Bibliography Collects all references cited throughout the thesis in a single consolidated list to ensure traceability and completeness of the literature survey.

Chapter 2

Theoretical Background

2.1 Heat Dissipation and Thermal Modeling

Heat dissipation is a critical aspect of thermal management in electronic and electrical systems. As components and devices operate, they generate heat, and if this heat is not effectively managed, it can lead to performance degradation, reduced lifespan, or even failure. Efficient heat dissipation ensures that devices remain within their optimal temperature ranges, maintaining reliability and performance. Heat dissipation can occur through several mechanisms:

Conduction: The transfer of heat through direct contact with a material. It occurs when two objects at different temperatures are in contact, and heat flows from the hotter to the cooler object.

Convection: The transfer of heat through a fluid (liquid or gas) in motion. As air or liquid moves over a surface, it carries away heat, cooling the surface in the process. This process is heavily used in systems with fans or heat sinks.

Radiation: The emission of heat energy in the form of electromagnetic waves. All objects emit radiation depending on their temperature, with hotter objects radiating more heat.

Effective heat dissipation is vital in preventing thermal runaway and ensuring optimal performance in electronic devices. This leads to the concept of thermal modeling, which provides a detailed approach to understanding and managing heat flow within electronic systems. By using thermal models, it is possible to predict temperature distribution, identify hot spots, and design systems that effectively manage thermal loads. Include an example thermal equivalent circuit:

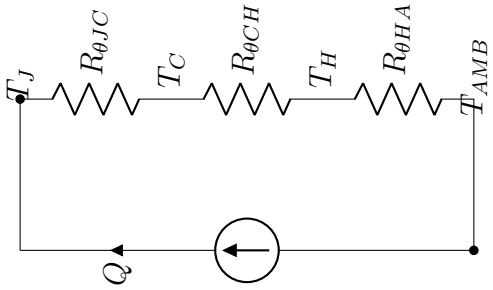


Figure 2.1: Simplified thermal model of a power semiconductor. The thermal current source Q represents the heat generated by power losses in the device. The resistances $R_{\theta JC}$, $R_{\theta CH}$, and $R_{\theta HA}$ model the thermal impedances between junction and case, case and heatsink, and heatsink and ambient, respectively. The temperature nodes T_J, T_C, T_H, and T_{AMB} represent the thermal potentials at each interface.

Although a more accurate model would include thermal capacitances in parallel with each resistance to capture transient thermal behavior, they are omitted here because the focus of this study is not on long-term heat dissipation dynamics but on junction temperature estimation during switching operations, but the goal is to estimate the $V_{\mathrm{DS(on)}}$ as TSEP through a dedicated measurement circuit equipped with a driver to interface at the logical level with the microcontroller.

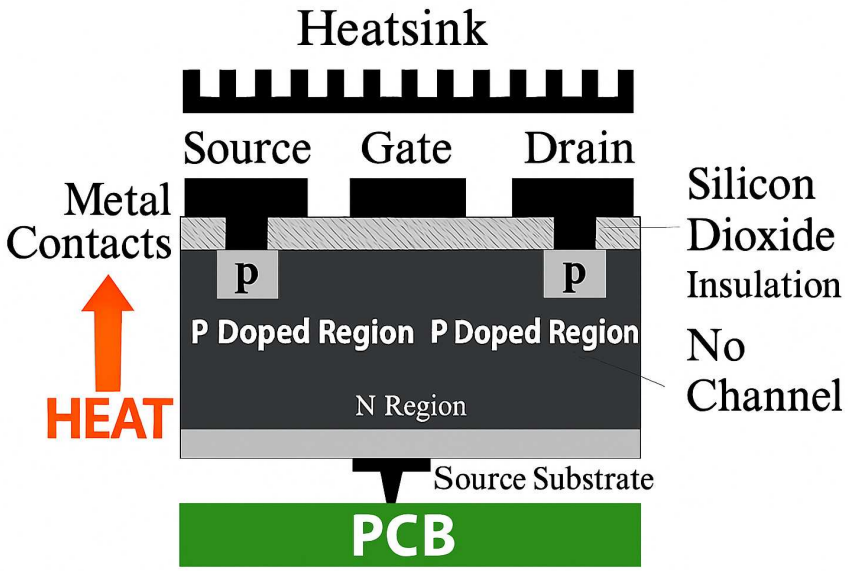


Figure 2.2: How heat flow is dissipated through a heatsink

In power semiconductor devices, such as transistors, heat dissipation occurs predominantly through internal conduction, followed by convective and radiative mechanisms toward the external environment. However, within the device package, the extremely limited space and high power density render convective flow highly ineffective. The absence of natural or forced airflow within the enclosure drastically restricts thermal exchange, forcing the heat transfer process to rely solely on conduc-

tion across the thermal interfaces, following the sequence: junction → package → heatsink → ambient.

Under such constrained operating conditions, an inaccurate estimation of the junction temperature can result in the undersizing of thermal management solutions. In this context, "undersizing" refers to the implementation of cooling devices (for example, heatsinks or active cooling systems) that are insufficient to effectively evacuate the thermal energy generated during operation. This inadequacy leads to an insufficient attenuation of thermal gradients, thereby causing elevated operating temperatures. Such conditions not only compromise the intrinsic performance of the semiconductor—potentially leading to undesirable parametric deviations and increased noise—but also accelerate the aging process of the semiconductor materials, ultimately reducing both operational reliability and the overall lifespan of the device. More critically, the failure to appropriately size the thermal management system exposes the device to the risk of thermal runaway, wherein an increase in temperature induces further, uncontrolled heat generation. This self-reinforcing cycle eventually culminates in irreversible and catastrophic failures, making it imperative to achieve highly accurate modeling and precise estimation of the internal temperature in order to design effective and reliable thermal control systems.

2.2 Temperature Sensitive Electrical Parameter (TSEP)

2.2.1 Introduction to Thermal Sensitive Electrical Parameters (TSEP)

Thermal Sensitive Electrical Parameters (TSEPs) are inherent electrical characteristics of semiconductor materials and devices whose values exhibit a predictable dependence on temperature. Such variations arise from fundamental physical phenomena, including changes in charge carrier mobility, scattering mechanisms, and shifts in the semiconductor band structure.

For instance, parameters such as the on-state resistance $R_{\mathrm{DS(on)}}$ of a MOSFET, the forward voltage drop V_{F} of a diode, and the on-state voltage $V_{\mathrm{DS(on)}}$ of a MOSFET serve as typical examples of TSEPs. As temperature increases, charge carrier mobility generally decreases due to enhanced phonon scattering, resulting in an elevated on-state resistance. Concurrently, alterations in potential barriers and the diffusion processes of carriers yield predictable changes in conduction voltages.

A pivotal advantage of TSEPs lies in their capacity to facilitate monitoring of the device's internal junction temperature solely via electrical measurements. This method enables continuous, real-time determination of the intrinsic operating temperature, surpassing conventional measurement techniques. Traditional methods, such as infrared thermography, typically provide an estimation of the external temperature on the device's case; however, such measurements do not capture the intrinsic thermal gradients present between internal junctions.

By calibrating a given TSEP against established temperature benchmarks, it is possible to derive a continuous temperature estimate during normal operation. This approach effectively supplants traditional external thermal measurement methods, offering a more accurate characterization of the internal thermal state within power semiconductor devices.

Accurate characterization of TSEPs is therefore indispensable for the design of robust thermal management systems, ensuring that effective cooling strategies are implemented to mitigate the risks of overheating and to maintain reliable device operation.[1, 2].

2.2.2 Key Thermal Sensitive Electrical Parameters

$R_{\mathrm{DS(on)}}$ **(MOSFET On-Resistance)** The on-resistance $R_{\mathrm{DS(on)}}$ increases with rising junction temperature due to decreased charge carrier mobility and enhanced phonon scattering. In SiC MOSFETs, the typical temperature coefficient ranges between +0.5% and +1.5% per 10 °C change in temperature [1]. This implies that for every 10 °C increase, the on-resistance rises by an amount between 0.5% and 1.5% of its nominal value, underscoring the necessity for effective thermal management to minimize power losses and ensure proper device operation.

$V_{\mathrm{DS(on)}}$ **(MOSFET On-State Voltage)** The voltage drop across the conducting channel of a MOSFET is given by

$$V_{\mathrm{DS(on)}} = I_{\mathrm{D}}\, R_{\mathrm{DS(on)}},$$

where any temperature-induced change in $R_{\mathrm{DS(on)}}$ directly affects the on-state voltage. In SiC devices, a sensitivity of approximately $1.0\,\mathrm{mV/°C}$ is typically observed [3]. This parameter is valuable for real-time junction temperature estimation during normal operation.

V_{F} **(Diode Forward Voltage)** In SiC Schottky diodes, the forward voltage V_{F} typically decreases with increasing temperature at a rate of about $-2\,\mathrm{mV/°C}$ [2]. This inverse relationship renders V_{F} an effective TSEP for temperature sensing, particularly in hybrid modules where precise thermal control is critical. The temperature-dependent modulation of V_{F} facilitates prompt identification of thermal variations, enabling appropriate compensatory measures.

Leakage Current (I_{leak}) The leakage current I_{leak} exhibits an exponential increase with temperature. Although its variation is less linear compared to other TSEPs, the high sensitivity of I_{leak} to thermal changes makes it extremely useful for high-accuracy, point temperature measurements, particularly under conditions of significant thermal confinement [3].

V_{BE} **(Bipolar Transistor Base-Emitter Voltage)** In bipolar transistors, the base-emitter voltage V_{BE} decreases by approximately $2\,\mathrm{mV/°C}$ with rising temperature. This negative temperature coefficient renders V_{BE} a reliable parameter for thermal compensation applications and provides direct insight into internal temperature variations within the device.

Additional Note: The application of TSEPs offers a distinct advantage over traditional temperature measurement methods, such as infrared thermography, which typically provide an estimate of only the external case temperature. By leveraging TSEPs, it is possible to acquire a direct, continuous measurement of the internal temperature — that is, the temperature present between the various internal junctions — during regular operation. This enhanced approach results in improved diagnostic accuracy and facilitates the design of more effective thermal management strategies, ultimately reducing the risks associated with overheating and consequent device degradation or failure.

2.2.3 Temperature Calibration of $V_{\mathrm{DS(on)}}$ in MOSFETs and Considerations on Non-linearities

Thermal Sensitive Electrical Parameters (TSEPs) are intrinsic characteristics of semiconductor devices whose values vary in a predictable manner with temperature. In particular, the MOSFET on-state voltage, $V_{\mathrm{DS(on)}}$, which is directly correlated with the on-resistance $R_{\mathrm{DS(on)}}$, exhibits a marked temperature dependence. This dependence can be quantified by the temperature coefficient α_{TSEP}, defined as:

$$\alpha_{\mathrm{TSEP}} = \frac{1}{P_0}\,\frac{\mathrm{d}P}{\mathrm{d}T} \quad \left[^{\circ}\mathrm{C}^{-1}\right],$$

where P_0 denotes the value of the parameter at the reference temperature T_0.

For SiC MOSFETs, the temperature coefficient for the on-resistance may be approximated by:

$$\alpha_R \approx \frac{\Delta R_{\mathrm{DS(on)}}}{R_{\mathrm{DS(on)},0}\,\Delta T} \approx \frac{0.015}{10\,^{\circ}\mathrm{C}} = 1.5 \times 10^{-3}\,^{\circ}\mathrm{C}^{-1},$$

as reported in [1]. Since the on-state voltage is given by:

$$V_{\mathrm{DS(on)}}(T) = I_{\mathrm{D}}\, R_{\mathrm{DS(on)}}(T),$$

any temperature-induced variation in $R_{\mathrm{DS(on)}}$ will directly be reflected in $V_{\mathrm{DS(on)}}$. Assuming a linear temperature dependence for $R_{\mathrm{DS(on)}}$, we express:

$$R_{\mathrm{DS(on)}}(T) = R_{\mathrm{DS(on)}}(T_0) + K_R\,(T - T_0),$$

where K_R is the resistance temperature coefficient (in $\Omega/^{\circ}\mathrm{C}$). Consequently, the temperature dependence of $V_{\mathrm{DS(on)}}$ becomes:

$$V_{\mathrm{DS(on)}}(T) = V_{\mathrm{DS(on)}}(T_0) + I_{\mathrm{D}}\, K_R\,(T - T_0).$$

By defining the calibration coefficient K for $V_{\mathrm{DS(on)}}$ as:

$$K = I_{\mathrm{D}}\, K_R \quad [\mathrm{mV}/^{\circ}\mathrm{C}]\,,$$

we quantify the variation of $V_{\mathrm{DS(on)}}$ per unit temperature.

The following systematic procedure outlines the experimental steps for determining K:

1. **Controlled Thermal Environment:**
   Place the MOSFET under test in a temperature-controlled chamber, where the ambient temperature can be varied over the desired range. It is essential that the device reaches thermal equilibrium at each temperature set-point to ensure that measured values reflect a steady-state condition.

2. **Constant Operating Conditions:**
   Maintain a constant drain current I_{D} during the experiment so that any variation in $V_{\mathrm{DS(on)}}$ is solely attributable to temperature changes, eliminating the impact of operational current fluctuations.

3. **Measurement of $V_{\mathrm{DS(on)}}$:**
   Record the value of $V_{\mathrm{DS(on)}}$ at incremental temperature steps (e.g., from T_0 to $T_0 + \Delta T$). The acquired data should cover a sufficiently wide temperature range to accurately capture the temperature dependence.

4. **Validation and Uncertainty Analysis:**
   Perform repeated measurements and apply statistical analysis to validate the linear model. An uncertainty analysis is essential to quantify the confidence in the calibration coefficient K, ensuring its robustness under normal operating conditions.

5. **Considerations on Non-linearities:**
   Although a linear model is often adequate over limited temperature ranges, at extreme temperatures or due to complex physical phenomena (e.g., non-uniform variations in charge carrier mobility or changes in contact resistance), the behavior of $R_{\mathrm{DS(on)}}$ and consequently $V_{\mathrm{DS(on)}}$ may become nonlinear. In such cases, a higher-order polynomial or piecewise-linear model may be required to more accurately describe the temperature dependence. Residual analysis and statistical verification help determine whether the linear model is sufficient or if a nonlinear representation is warranted.

By calibrating $V_{\mathrm{DS(on)}}$ in this manner, the parameter can be used as an *in situ* thermal sensor, providing real-time estimates of the MOSFET's junction temperature. This approach offers significant advantages over traditional external temperature measurement techniques, such as infrared thermography, which capture only the surface temperature of the device's case. Direct electrical parameter measurement enables the accurate assessment of internal thermal gradients, thereby enhancing the effectiveness of thermal management strategies [3].

2.2.4 Effects of Temperature Variation on Circuit Performance

Temperature-induced variations in Thermal Sensitive Electrical Parameters (TSEPs) can significantly affect circuit performance. Key impacts include:

- **Accuracy:** Linear TSEPs (e.g., $R_{\mathrm{DS(on)}}$) provide a straightforward calibration process but exhibit a limited dynamic range. In contrast, nonlinear TSEPs, such as leakage current, yield higher sensitivity over a broader temperature span; however, they require more sophisticated compensation techniques to achieve accurate temperature estimation [3].

- **Noise and Offset:** Transient switching can introduce measurement noise in $V_{\mathrm{DS(on)}}$, degrading the resolution of temperature sensing. Employing advanced filtering methods and synchronous sampling can mitigate these offset errors, ensuring that the temperature readings remain precise [2].

- **Self-Heating:** The measurement process itself—be it through the sensing current or the associated voltage drop—may lead to local self-heating of the junction. This effect can distort the apparent temperature if not properly managed. Low-power sensing circuits, together with duty-cycle control strategies, are essential to minimize self-heating errors and maintain measurement integrity [1].

In summary, understanding and compensating for these effects is critical in designing temperature-sensitive circuits. Careful circuit design and appropriate signal conditioning ensure that the intrinsic TSEP behavior is accurately harnessed for reliable temperature monitoring.

2.2.5 Thermal Management and Compensation Techniques

Robust temperature estimation in semiconductor devices requires the implementation of advanced thermal management and compensation strategies to mitigate deviations in Temperature Sensitive Electrical Parameters (TSEPs). The following techniques, which may be applied individually or in combination, are critical for ensuring precise and reliable temperature measurements in challenging operational environments:

- **Digital Compensation:**
  Nonlinearities in TSEP responses can be effectively corrected by employing digital compensation methods. Polynomial-based correction algorithms and lookup table (LUT) approaches are commonly used to linearize the sensor output. Moreover, adaptive digital compensation schemes, which update correction parameters in real time to accommodate component aging, process variations, and dynamic operating conditions, further enhance measurement accuracy [3].

- **Hardware Filtering:**
  High-frequency noise and offset errors introduced by switching transients can significantly degrade the quality of the $V_{\mathrm{DS(on)}}$ signal. Implementing RC filtering networks in conjunction with differential measurement techniques helps suppress these disturbances. Critical to this approach is the careful selection of resistor and capacitor values as well as meticulous circuit layout design, which collectively improve signal integrity and mitigate measurement errors [2].

- **Self-Heating Correction:**
  The measurement process can itself induce self-heating in the semiconductor junction, causing discrepancies between the intrinsic temperature and the measured value. Techniques such as time-multiplexed sensing, pulsed (or reduced amplitude) excitation, and duty-cycle control are employed to minimize power dissipation during the measurement interval. These approaches reduce self-heating effects, thereby ensuring that the TSEP accurately reflects the true junction temperature [1].

- **Adaptive Compensation:**
  Unlike static correction methods, adaptive compensation strategies continuously adjust calibration parameters in response to real-time sensor data. By comparing the measured TSEP (e.g., $V_{\mathrm{DS(on)}}$) with a predefined reference model, digital signal processing algorithms – sometimes incorporating machine learning techniques – automatically update the corrective coefficients. This dynamic adjustment is particularly advantageous in environments with rapid thermal fluctuations, significant aging effects, or inherent sensor nonlinearities. For further insights into these methodologies, refer to the technical resources provided by Texas Instruments [38].

In summary, the integration of digital compensation, hardware filtering, self-heating correction, and adaptive compensation provides a robust framework for accurate temperature sensing. This comprehensive strategy is essential for mitigating

the dynamic and nonlinear effects that adversely affect TSEP performance in high-precision applications.

2.2.6 Advanced Topics and Future Directions

Emerging developments in wide-bandgap materials, particularly gallium nitride (GaN) and silicon carbide (SiC), are leading to steeper TSEP curves. Owing to their high thermal sensitivity, these materials enable the design of high-resolution thermal monitoring systems in compact converters, thereby enhancing both power density and overall system efficiency [3].

Simultaneously, the integration of on-chip temperature sensors that leverage TSEP principles is becoming increasingly significant. These integrated solutions, driven by advances in microfabrication and the incorporation of calibration circuits, substantially reduce system complexity while improving the accuracy of thermal measurements. Such technologies facilitate real-time temperature management through the deployment of advanced digital compensation and filtering algorithms, ultimately optimizing thermal control in high-performance devices.

Looking toward the future, the convergence of wide-bandgap technologies and integrated sensor solutions is expected to play a fundamental role in the next generation of power electronics. Current research is focused on optimizing sensor integration, reducing power consumption, and developing robust calibration methods that can adapt to dynamic operating conditions and nonlinear variations. These advancements promise to deliver precise thermal management in increasingly compact and high-performance applications.

2.3 Modeling $V_{DS_{on}}$ as a Thermal Sensitive Electrical Parameter (TSEP)

The drain-source voltage in the on-state ($V_{DS_{on}}$) is a key parameter in MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors). It represents the voltage drop between the drain and the source terminals when the MOSFET is fully conducting, meaning it is in the on-state. $V_{DS_{on}}$ is influenced by several factors, including the operating conditions, the MOSFET's channel resistance, and notably, the temperature.

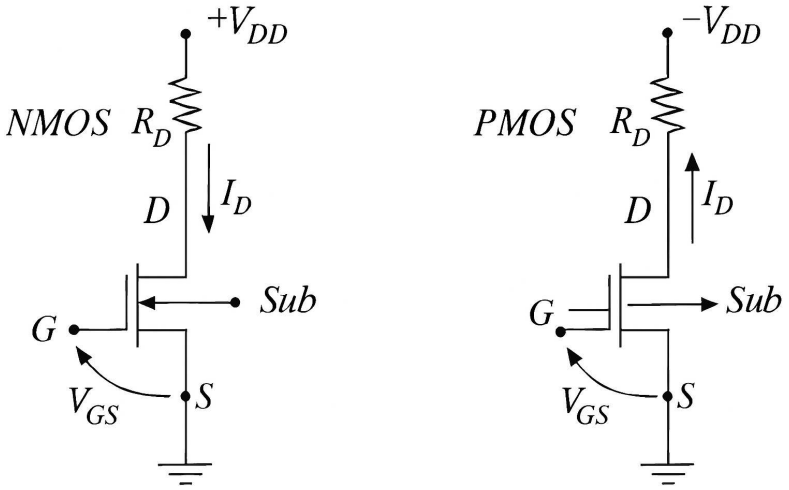


Figure 2.3: The image shows a simplified circuit diagram of two fundamental types of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs): the NMOS (N-channel MOSFET) and the PMOS (P-channel MOSFET).

Symbol	Description	Unit
$V_{DS_{on}}$	Drain-source voltage in on-state	V
$I_{D_{on}}$	Drain current in on-state	A
$R_{DS_{on}}(T)$	Channel resistance vs. temperature	Ω
$R_{DS_{on},0}$	Channel resistance at reference T_0	Ω
α	Temperature coefficient of resistance	1/°C
$\mu(T)$	Carrier mobility vs. temperature	cm^2/Vs
W	Channel width	m
L	Channel length	m
V_{GS}	Gate-source voltage	V
$V_{th}(T)$	Threshold voltage vs. temperature	V
T	Operating temperature	°C or K
T_0	Reference temperature	°C or K

Table 2.1: Parameters used in the modeling of $V_{DS_{on}}$ and TSEP.

2.3.1 Understanding $V_{DS_{on}}$

In the on-state, a MOSFET behaves as a resistive element between the drain and the source. The voltage $V_{DS_{on}}$ is the result of the current flowing through the channel, and it depends on the resistance of the MOSFET channel.

The resistance of the channel $R_{DS_{on}}$ is not constant and varies with factors such as temperature, channel length, and the gate-source voltage (V_{GS}). Temperature is a particularly significant factor because it affects the carrier mobility, the threshold voltage, and the channel resistance, all of which influence the value of $V_{DS_{on}}$.

Thus, $V_{DS_{on}}$ is directly related to the channel resistance $R_{DS_{on}}$ and the drain current $I_{D_{on}}$, which can be modeled as follows:

$$V_{DS_{on}} = I_{D_{on}} \cdot R_{DS_{on}}(T)$$

where:

- $I_{D_{on}}$ is the drain current in the on-state.
- $R_{DS_{on}}(T)$ is the channel resistance as a function of temperature T.

2.3.2 Temperature Dependence of $R_{DS_{on}}$

The channel resistance $R_{DS_{on}}$ increases with temperature due to the decrease in carrier mobility and the variation in the material properties of the MOSFET. The temperature dependence of the channel resistance can be expressed as:

$$R_{DS_{on}}(T) = R_{DS_{on,0}} \cdot (1 + \alpha(T - T_0))$$

where:

- $R_{DS_{on,0}}$ is the channel resistance at a reference temperature T_0.
- α is the temperature coefficient of resistance (TCR) of the MOSFET channel material.
- T is the operating temperature.
- T_0 is the reference temperature.

This equation describes the linear increase in resistance as the temperature rises. As the temperature increases, the resistance of the MOSFET channel increases, leading to an increase in $V_{DS_{on}}$ for a given drain current.

2.3.3 Drain Current $I_{D_{on}}$ and Its Temperature Dependence

The drain current in the on-state ($I_{D_{on}}$) depends on several factors, including the gate-source voltage (V_{GS}), the channel length L, and the channel width W. It is given by the following expression:

$$I_{D_{on}} = \mu(T) \cdot \frac{W}{L} \cdot (V_{GS} - V_{th}(T)) \cdot V_{DS}$$

where:

- $\mu(T)$ is the temperature-dependent mobility of the charge carriers in the MOSFET channel.
- W is the width of the MOSFET channel.
- L is the length of the MOSFET channel.
- V_{GS} is the gate-source voltage.
- $V_{th}(T)$ is the threshold voltage, which decreases with temperature.
- V_{DS} is the drain-source voltage.

The mobility $\mu(T)$ typically decreases with increasing temperature due to increased scattering of charge carriers, while the threshold voltage $V_{th}(T)$ decreases with temperature. As a result, for a given V_{GS}, the drain current $I_{D_{on}}$ increases with temperature. However, the increase in $R_{DS_{on}}$ with temperature leads to a higher $V_{DS_{on}}$.

2.3.4 Modeling Sensitivity of $V_{\mathrm{DS(on)}}$ as a TSEP

The on-state drain–source voltage $V_{\mathrm{DS(on)}}$ is a highly effective Temperature-Sensitive Electrical Parameter (TSEP) for online junction-temperature monitoring in SiC MOSFETs. Its sensitivity arises from two principal dependencies:

1. CHANNEL CONDUCTION PHYSICs: In the linear (ohmic) region, the MOSFET channel behaves as a temperature-dependent resistor. An analytical expression derived from charge-sheet modeling gives

$$V_{\mathrm{DS(on)}} = \frac{J\, p\, L_{\mathrm{CH}}}{\mu(T)\, C_{\mathrm{ox}}\Big(V_{\mathrm{G}} - V_{\mathrm{TH}}(T)\Big)},$$

where J is the current density, p the cell pitch, L_{CH} the channel length, $\mu(T)$ the carrier mobility (decreasing with T), C_{ox} the gate-oxide capacitance, V_{G} the applied gate voltage, and $V_{\mathrm{TH}}(T)$ the threshold voltage (also temperature-dependent) :contentReference[oaicite:0]index=0.

2. SIMPLIFIED RESISTOR MODEL: Equivalently, one can view $V_{\mathrm{DS(on)}}$ as the product of the on-state current and an effective channel resistance:

$$V_{\mathrm{DS(on)}}(T) = I_{D_{\mathrm{on}}}\Big[R_{\mathrm{DS(on)},0}\,(1 + \alpha\,(T - T_0))\Big],$$

where $I_{D_{\mathrm{on}}}$ is the drain current in conduction, $R_{\mathrm{DS(on)},0}$ the resistance at reference temperature T_0, and α the temperature coefficient of resistance :contentReference[oaicite:1]index=1.

Combining these perspectives highlights that $V_{\mathrm{DS(on)}}$ inherits its temperature sensitivity both from the mobility-limited channel conduction and from the linear increase of channel resistance with temperature. In practice, the simplified resistor model is often preferred for calibration and real-time estimation, since it directly relates measured voltage to temperature via a single coefficient α.

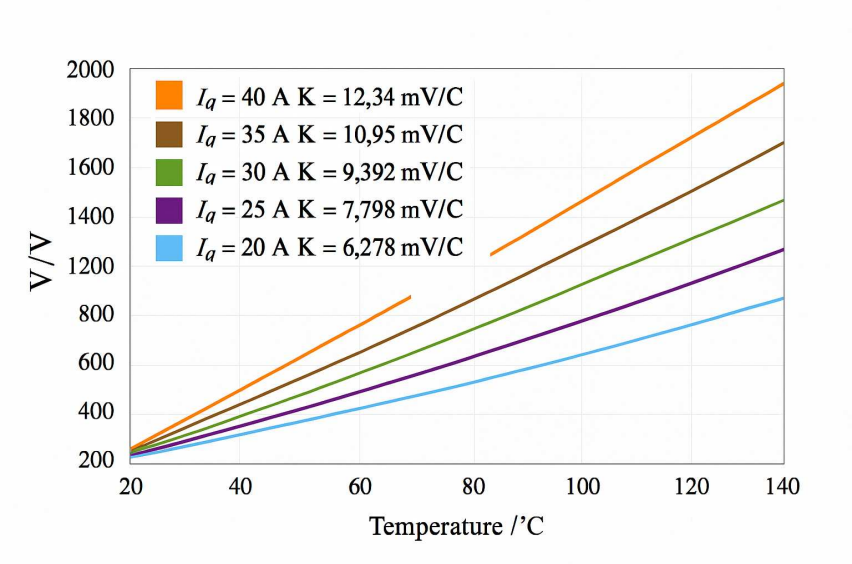


Figure 2.4: Calibration curve of $V_{\mathrm{DS(on)}}$ versus junction temperature under different drain-current levels. The nearly linear slope defines the TSEP coefficient α.

2.3.5 Thermal Sensitivity Coefficient (TSEP)

The thermal sensitivity coefficient (TSEP) quantifies how much $V_{DS_{on}}$ changes with respect to temperature. It is defined as:

$$\mathrm{TSEP} = \frac{dV_{DS_{on}}}{dT}$$

Taking the derivative of $V_{DS_{on}}(T)$ with respect to temperature:

$$\frac{dV_{DS_{on}}}{dT} = I_{D_{on}} \cdot R_{DS_{on,0}} \cdot \alpha$$

This coefficient represents the rate of change of $V_{DS_{on}}$ with temperature and is critical for understanding how temperature variations affect the MOSFET's performance in real-world applications. A higher TSEP indicates that the MOSFET's $V_{DS_{on}}$ is more sensitive to temperature variations, which can impact the overall performance of the circuit. Finally, the modeling of $V_{DS_{on}}$ as a thermal sensitive electrical parameter allows for a better understanding of how temperature affects the operation of the MOSFET. By considering both the temperature-dependent channel resistance and the drain current, we can accurately predict the behavior of the MOSFET under varying thermal conditions. This model is essential for designing reliable electronic systems, where thermal effects play a significant role in the performance and longevity of devices.

2.4 Thermal Estimation Method via $V_{\mathrm{DS(on)}}$

2.4.1 Calibration Strategy for $V_{\mathrm{DS(on)}}$

A critical component in junction temperature estimation using $V_{\mathrm{DS(on)}}$ is the calibration phase, which establishes a repeatable mapping between the on-state voltage and the junction temperature. This process generally consists of the following stages:

1. **Preconditioning and Thermal Stabilization:** The MOSFET is operated under known thermal boundary conditions (e.g., constant ambient or heatsink temperature). To avoid self-heating artifacts, measurements are often taken under pulsed current conditions, or low duty cycles, where thermal equilibrium is preserved.

2. **Controlled Self-Heating Procedure:** A power pulse is applied to heat the junction while keeping the external case temperature monitored. During this transient, $V_{\mathrm{DS(on)}}$ and the applied drain current I_{D} are synchronously sampled.

3. **Reference Temperature Acquisition:** Junction temperature reference points are determined either via infrared thermography, finite element simulation, or indirect thermal models $T_{\mathrm{j}}(T_{\mathrm{c}}, R_{\theta})$ relating case and junction temperatures:contentReference[oaicite:1]index=1.

4. **Fitting and Curve Extraction:** The collected data are fitted to linear or second-order polynomial models:

$$V_{\mathrm{DS(on)}}(T) = aT^2 + bT + c$$

   or, in the linear region:

$$V_{\mathrm{DS(on)}}(T) = V_0 + \alpha(T - T_0)$$

   where α is the temperature sensitivity coefficient extracted from the calibration slope.

5. **Lookup Table or Model Implementation:** The resulting calibration map is embedded into a lookup table or fitted into firmware/FPGA-based control logic for real-time use.

It is essential that the calibration uses the same measurement circuit as the one intended for in-application monitoring to eliminate offset or gain inconsistencies from the analog front-end. Moreover, calibration at both low and high current densities ensures wide-range linearity compensation, as α can vary depending on I_{D} and V_{G}.

2.4.2 Challenges and Compensations

Various nonidealities impact the accuracy of this estimation:

- **BTI Drift of V_{TH}:** Bias Temperature Instability (BTI) leads to a drift in threshold voltage, which translates to a minor but cumulative offset in $V_{\mathrm{DS(on)}}$. However, in SiC MOSFETs this drift is typically within 100 mV, inducing a temperature error of less than 2°C:contentReference[oaicite:3]index=3.
- **Switching Noise and Sampling Timing:** Because $V_{\mathrm{DS(on)}}$ must be sampled during the conduction period, synchronization with gate signals and filtering circuits are essential to mitigate voltage spikes and noise-induced error.
- **Aging Effects:** $R_{\mathrm{DS(on)}}$ increases over time due to degradation, potentially resulting in overestimation of T_{j} if the calibration curve is not updated periodically:contentReference[oaicite:4]index=4.

In conclusion, $V_{\mathrm{DS(on)}}$-based temperature estimation, when supported by rigorous modeling and meticulous calibration, provides a highly practical, non-invasive and accurate solution for real-time thermal monitoring in SiC MOSFET applications.

Chapter 3

Methodology

3.1 Custom Model Development and LTSpice Simulation for Non-Library Components

3.1.1 Introduction to LTSpice

LTspice is a circuit-simulation software built on the SPICE (Simulation Program with Integrated Circuit Emphasis) language. Utilizing advanced mathematical models, it offers a comprehensive framework for describing and analyzing the electrical behavior of both passive and active components. Through SPICE simulation, circuit performance is evaluated under a range of operating conditions, allowing for the verification and optimization of behavior before any physical implementation. This process effectively reduces development time and cost.

The simulation capabilities of LTspice encompass DC, AC, transient, and noise analyses, facilitating the identification of potential issues such as parasitic effects and thermal anomalies at an early stage. Moreover, in addition to its extensive built-in libraries, LTspice permits the integration of custom models—enabling the representation of devices not available in the standard library. In this way, a high level of fidelity in simulation results is achieved, which supports robust design outcomes and a more efficient development cycle.

3.1.2 Custom component Integration Strategies in LTspice

In many advanced circuit simulation projects, especially when non-standard devices are involved, it becomes necessary to integrate custom components whose models are not provided by the default LTspice library. This subsection outlines several robust techniques to achieve this integration.

One straightforward method is to use the .MODEL directive. By employing this directive, simple devices can be defined directly within the schematic or in an included text file. In this approach, it is sufficient to add the corresponding .model text file for a given component and to rename the generic component with the same name as the .model file, so that SPICE assigns that model to the generic component. Essential parameters—such as threshold voltage, on-state resistance, capacitances, and other characteristics—can then be specified to accurately emulate the behavior

of various semiconductor devices. This approach is particularly useful when the device's behavior can be captured with a concise mathematical model.

Another powerful strategy is leveraging external .LIB files. These files allow for storing a collection of SPICE models that can be reused across different projects. By referencing a .LIB file from within the schematic, one can easily incorporate a complex device model without cluttering the main simulation file. This modular approach not only simplifies model maintenance but also enhances the reproducibility of simulations across multiple design iterations.

For devices requiring a higher level of customization—often due to unique characteristics or packaging constraints—a combination of custom symbol (.ASY) and subcircuit (.SUB) files is recommended. The .ASY file defines the visual representation of the component within the schematic, ensuring clarity in circuit diagrams, while the .SUB file contains the detailed SPICE netlist that models the internal electrical behavior of the component. This method offers the greatest flexibility and precision, making it indispensable for pioneering designs where conventional models fail to capture the necessary level of detail.

Despite LTspice's extensive built-in library, the ability to introduce custom components via these methods is crucial. Depending on the complexity of the device and the specific requirements of a simulation, one may choose between using the .MODEL directive for simpler approximations or the combined use of .LIB files and custom subcircuits for more detailed representations.

In summary, these techniques provide a comprehensive framework for adding custom components in LTspice, thereby bridging the gap between simulated models and their real-world counterparts. The proper implementation of these methods is essential for achieving high-fidelity simulations, which in turn supports more accurate circuit analysis and design validation. To explain it better, has given an example below:

For example, let's take a specific component, more precisely a MOSFET RUM001L02 to make a more illustrative example. We use this mosfet that we will then go into more detail in the following chapter of real models.

Using the `.MODEL` Directive

When device parameters (from datasheets) are available, the SPICE model can be defined directly in the schematic:

1. **Place the component:** Press `F2`, select "NMOS," and drop it into the schematic.

2. **Assign the model name:** Right-click the symbol, enter the desired model name (e.g. `RUM001L02`) in the `Mosfet` field.

3. **Add the directive:** Select `Edit → Add SPICE Directive` (or press `S`) and enter, for example:

```
.MODEL RUM001L02 VDMOS(
  Rg=10
  Vto=1.2
  Rd=6m
  Rs=5m
  Rb=15m
  Kp=5
  Lambda=10m
  Cgdmin=3p
  Cgdmax=7p
  A=0.9
  Cgso=10p
  Is=100p
  N=1.2
  Cjo=50p
  M=200m
  Vj=750m
  TT=20n
  ksubthres=0.1
  mfg=Rohm
  Vds=20
  Ron=6m
  Qg=1.2n
)
```

4. **Position directive:**Insert this instruction into an empty area of the schema as we like by using Spice directives.

Using a `.LIB` File

When the manufacturer provides a library file:

1. Download the `.lib` file (e.g. from Rohm semiconductors).
2. Copy it into LTspice's `lib\sub` directory.
3. In the schematic, add:

   ```
   .INCLUDE "filename.lib"
   ```

4. Ensure the symbol's model name matches that in the library.

Creating Custom Components (`.ASY` and `.SUB` Files)

If no standard model exists:

1. **Custom symbol (`.ASY`):** Use the "New Symbol" tool, define pins and graphics.

2. **Subcircuit file (`.SUB`):** Write the SPICE subcircuit, for example:

```
.SUBCKT RUM001L02 D G S
M1 D G S 0 RUM001L02
.ENDS
```

3. Associate the `.SUB` with the `.ASY` symbol.

3.1.3 Comparison between RUM001L02 and RUL035N02

To replicate a MOSFET that was not available in the library, the manufacturer's website was examined; however, it did not provide a corresponding .lib file for the desired component. Instead, an analogous component—already present in the standard SPICE libraries—was identified on the same site. This allowed the .MODEL statement of the similar MOSFET to be copied. Subsequently, the retrieved .MODEL file was retained and its key parameters were modified to emulate a device analogous to the target MOSFET, which was not available in the library. A reference model (RUL035N02) from LTspice's library was therefore adapted to create RUM001L02. Table 3.1 summarizes the main parameters of both models.

Parameter	**RUM001L02**	**RUL035N02**
Type	N-channel MOSFET	N-channel MOSFET
$V_{\mathrm{DS,max}}$	20 V	20 V
$I_{\mathrm{D,max}}$	100 mA	3.5 A
$R_{\mathrm{DS(on)}}$	6 Ω @ $V_{\mathrm{GS}} = 1.2$ V	31 mΩ
$V_{\mathrm{GS(th)}}$	1.2 V	0.9 V
P_{D}	150 mW	2.5 W
Q_{g}	1.2 nC	5.7 nC
$C_{\mathrm{gd,min}}$	3 pF	40 pF
$C_{\mathrm{gd,max}}$	7 pF	350 pF
C_{gs}	10 pF	400 pF
I_{S}	100 pA	756.7 pA
λ	10 m	50 m
R_{b}	15 mΩ	20 mΩ
R_{g}	10 mΩ	23 mΩ

Table 3.1: Main parameters comparison

Explanation of Key Parameters

- R_{g} **(Gate Resistance):** Limits the current during gate switching and affects the response speed.
- V_{th} **(Threshold Voltage):** The minimum V_{GS} required to turn on the MOSFET.

- $R_{\mathrm{d}}, R_{\mathrm{s}}, R_{\mathrm{b}}$ **(Internal Resistances):** Model the intrinsic losses, influencing conduction efficiency.

- K_{p} **(Transconductance):** The ratio of the change in V_{GS} to the change in I_{D}.

- λ: Channel length modulation in the saturation region.

- $C_{\mathrm{gd,min}}, C_{\mathrm{gd,max}}, C_{\mathrm{gs}}$: Parasitic capacitances, which are critical for switching times.

- I_{S}: The junction's saturation current.

- $C_{\mathrm{jo}}, M, V_{\mathrm{j}}$: Parameters of the PN junction under reverse bias.

- TT (Transit Time): The time required for the device to switch states.

- R_{on}: On-state resistance; typically higher in low-current applications.

- Q_{g}: Gate charge; affects switching times and power consumption.

3.1.4 Transitioning from Simulation to Practice

Moving from simulation to physical implementation is a critical phase that bridges the design process with real-world performance. This stage is structured into three distinct steps.

Schematic Construction

- **Component Placement:** Prior to placing symbols, confirm that all component models are properly defined using commands like `.MODEL` or `.INCLUDE`. Emphasis should be placed on organizing the schematic with clearly labeled nodes to eliminate wiring errors and simplify later verifications.

- **Node Connections:** Use clear and consistent node names to minimize connection errors.

Model Integration

- **LTspice Directives:** Include the necessary LTspice directives (e.g., `.MODEL` and `.LIB` references) so that every component is correctly associated with its model.

- **Custom Parts:** When standard components are insufficient, develop custom parts using `.ASY` and `.SUB` files, ensuring they are properly integrated within the simulation environment.

Simulation Execution

- **Verification:** Perform comprehensive checks to identify syntax and connection errors before commencing simulations.
- **Analysis:** Execute DC, transient, and AC analyses to validate circuit performance and confirm that the design meets the anticipated criteria, ensuring readiness for practical realization.

3.2 Description of the Four Ideal Circuits

To establish a baseline for $V_{\mathrm{DS(on)}}$ as a Temperature-Sensitive Electrical Parameter (TSEP), four "ideal" test circuits were created in LTspice using only the standard lossless library components (no parasitics, no dielectric losses, no device degradation). Common modeling choices include:

- Emulation of the MOSFET drain–source path by a square-wave voltage source toggling between 1-2 V and V_{DC}.
- A dedicated branch (current source or resistor network) that imposes a known drain current I_D when the DUT is On-state.
- Logic-level drive circuitry to replicate microcontroller gate signals with the objective to not introducing delay or noise.
- Three circuits derived by modifying an initial reference topology; the fourth designed from first principles to explore alternative measurement arrangements.

3.3 Dynamic Analysis, Clamping Circuit Evaluation, and Temperature Parametrization of $V_{\mathrm{DS(on)}}$ in ideal circuits.

In each of the ideal circuits, an AC frequency analysis is performed to assess the dynamic performance. This analysis is aimed at determining the cutoff frequency and the effective passband, thereby characterizing the circuit's behavior under high-frequency conditions. Furthermore, the analysis evaluates the circuit's efficiency in responding to input manipulations, ensuring that sudden variations in the input are promptly and accurately translated into the corresponding output response, morover the rising and falling edges of $V_{\mathrm{DS(on)}}$ during the transitions are evaluated with the aim of not having an underdamped system to avoid overshoot.

Subsequently, the operation of the clamping circuit is examined in detail. Particular attention is paid to the currents and voltages that develop across both the clamping diode—which is designed to protect against voltage transients—and the compensation diode. The compensation diode offsets the voltage drop introduced by the clamping diode so that the operational amplifier receives solely the voltage of the device under test (DUT). This configuration effectively eliminates any measurement offset, thereby ensuring a precise determination of $V_{\mathrm{DS(on)}}$.

Finally, once the final (and stable) measurement of $V_{\mathrm{DS(on)}}$ is obtained, a comprehensive parametric characterization is carried out as a function of temperature. This procedure is crucial for correlating the temperature variation of the DUT with the corresponding changes in $V_{\mathrm{DS(on)}}$, thus enabling accurate temperature monitoring and reliable prediction of device behavior under varying thermal conditions.

3.4 Strategy for Replacing Ideal with Real Components

To assess the impact of non-idealities, each ideal schematic is converted as follows:

- Preserve nominal values of passive components (resistors, capacitors).
- Substitute ideal voltage/current sources and switches with real components models (SiC MOSFETs, Schottky diodes).
- Use actual gate-driver and logic-level amplifier macromodels in place of ideal logic elements.
- Add representative layout parasitics (series resistance and inductance) to critical nodes if is necessary.

3.5 Real Circuit Simulations: Comparison with Ideal Baselines and Trade-Off Analysis

Having established the objectives and methodologies for simulations on ideal circuits, the next phase targets the evaluation of real circuits—which are derived from their ideal counterparts by substituting ideal components with real device models. In these real circuit simulations, the same performance criteria are pursued; however, several differences emerge due to non-idealities and practical implementation factors.

In particular, this section focuses on:

- **Electrical Characteristics:** Analyzing the voltage and current waveforms in the protection circuits. The behavior of the clamping diode (which guards against voltage transients) and the compensation diode (which offsets the voltage drop to ensure that only the DUT voltage is amplified) is compared with the ideal expectations.
- **Frequency Response:** Evaluating how the bandwidth of the response differs from the ideal case. While ideal circuits exhibit a defined cutoff frequency and passband, real circuits may show variations—such as shifts in cutoff frequency or reduced bandwidth—due to layout parasitics and inherent device non-idealities.
- **Dynamic Performance:** Verifying that the transient response of the real circuit aligns with that of the ideal model, albeit with some deviations induced by practical component behavior.

Finally, a comprehensive comparative analysis among the real circuits will be presented with the aim of identifying the best trade-off topology. The optimal circuit will be the one that guarantees the most reliable and precise measurement of $V_{\mathrm{DS(on)}}$, while balancing any disadvantages (such as increased noise or reduced dynamic range) against potential advantages (like improved stability or simplified circuitry).

Chapter 4

Simulations and Results – Ideal Circuits

4.1 Circuit 1: Configuration and Results

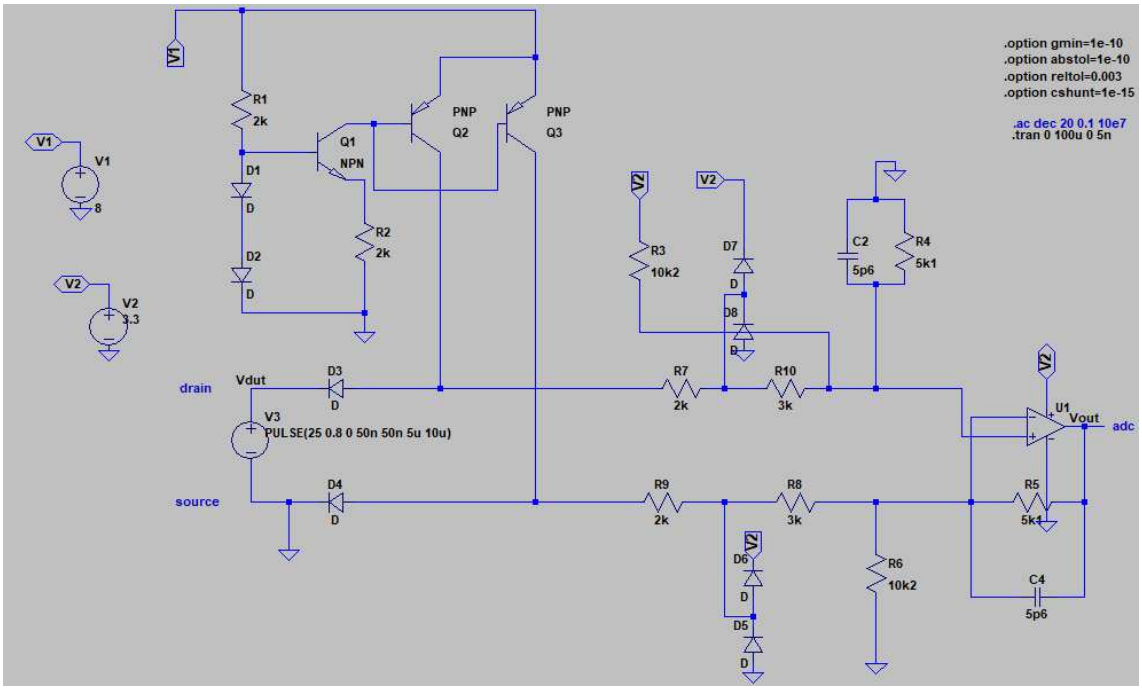


Figure 4.1: Schematic of the ideal circuit 1 on LTSpice.

4.1.1 Frequency Response Analysis of Circuit 1 (Ideal Model)

Bandwidth Limitations and Phase Wrapping

Phase Wrapping in Bode Diagrams

In the frequency response analysis of dynamic systems, phase discontinuities of $\pm 360°$ may appear in the Bode diagram of the output signal. This phenomenon, known as

phase wrapping, is a graphical convention adopted by simulation environments to constrain the phase within a fixed range for readability.

Although mathematically consistent, phase wrapping can obscure the qualitative interpretation of system behavior, particularly in configurations involving multiple poles, zeros, or cumulative phase shifts. These artificial jumps in the phase plot do not represent physical discontinuities but are instead the result of visualization limits.

- `MATLAB`: The default `bode` function displays phase within the range $[-180°, +180°]$. For continuous phase visualization, the `unwrap` function is recommended.
- `LTspice`: The phase is typically shown within the range $[-360°, +360°]$, and similar wrapping behavior may occur when the cumulative phase exceeds these bounds.

To enhance interpretability, especially in systems with complex dynamics, an *unwrapped phase view* is advised. This representation preserves the continuity of the phase response and facilitates a clearer understanding of the system's behavior across the frequency spectrum.

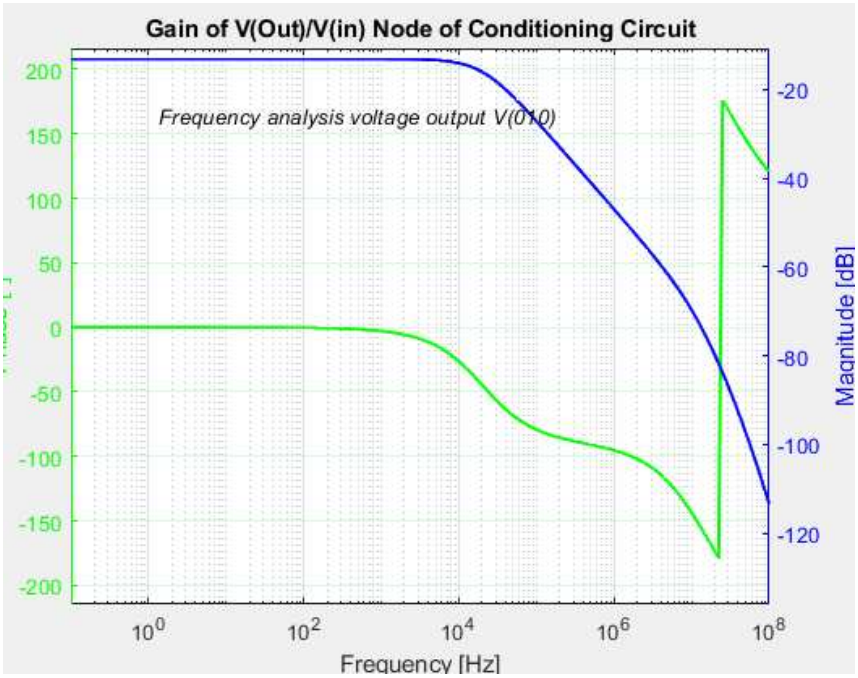


Figure 4.2: Phase discontinuity due to wrapping in the Bode diagram of `V(out)`

The AC analysis revealed a cutoff frequency of approximately $f_c \approx 22\,\text{kHz}$, indicating a severely limited bandwidth. The circuit employed the `Universalpamp2` component, a generic behavioral model available in LTspice which, if not manually configured, adopts rather conservative default parameters for gain and gain-bandwidth product (GBW). These settings can negatively affect the system's frequency response.

- The default gain is typically low, limiting amplification capabilities.

- The gain-bandwidth product (GBW) is set conservatively, restricting high-frequency performance.

- These limitations may result in a frequency response that does not reflect the expected behavior of high-speed systems.

Since such a narrow bandwidth is incompatible with the operational characteristics of SiC-based devices—designed to operate at high voltage and frequency—a revision of the simulation parameters and some nodal connections was necessary. This intervention enabled a response more consistent with the expected real-world behavior of the system.

Revised Frequency Response and Circuit Optimization

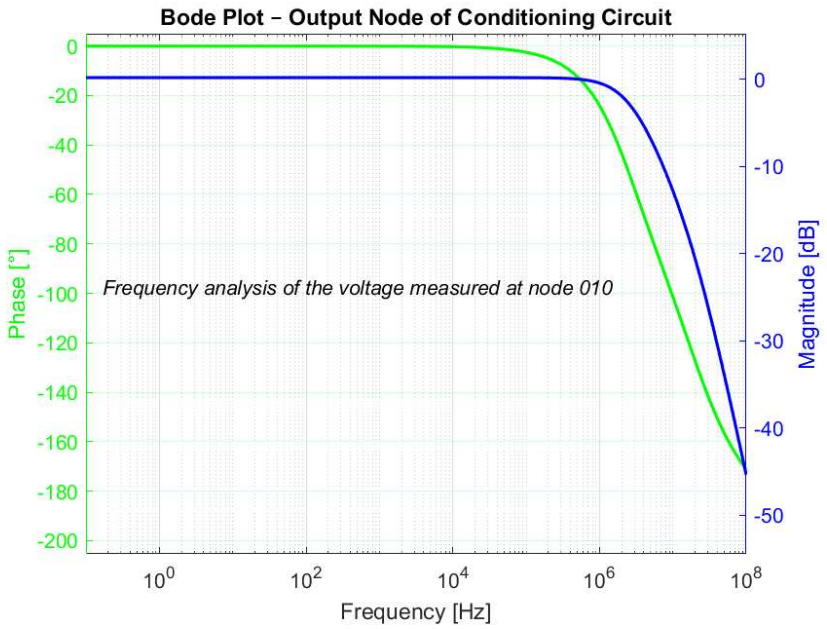


Figure 4.3: Magnitude response of the revised conditioning circuit showing the expected bandwidth for SiC-based high-speed applications.

Following the revision of experimental parameters and nodal configurations, a new frequency analysis was conducted to evaluate the dynamic behavior of the conditioning circuit under more representative conditions. The updated simulation revealed a significantly improved bandwidth, with the magnitude response exhibiting a $-3\,\mathrm{dB}$ drop at approximately $f_c = 2.818\,\mathrm{MHz}$.

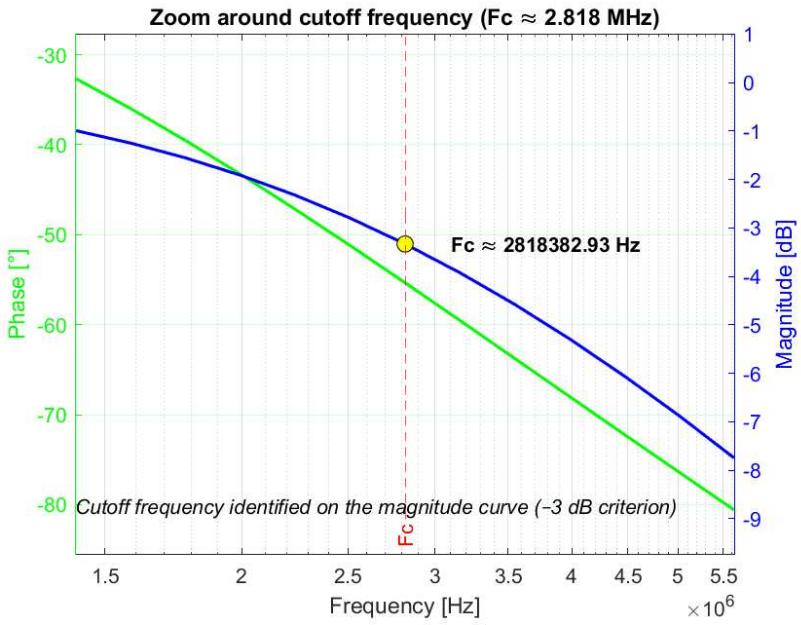


Figure 4.4: Zoomed view showing the $-3\,\mathrm{dB}$ cutoff at $f_c = 2.818\,\mathrm{MHz}$

This cutoff frequency was determined by identifying the point at which the maximum gain falls 3 dB below its peak value, in accordance with standard AC analysis methodology. The result aligns far more closely with the expected performance of SiC-based DUTs, which are engineered for high-voltage, high-frequency operation. The enhanced bandwidth confirms that the revised configuration better captures the dynamic characteristics of the target system.

To achieve this improvement, specific resistive components within the circuit were adjusted. In particular, the resistors `R3` and `R6`—originally set to high values—were reduced to better align with the desired input and feedback characteristics of the operational amplifier.

Table 4.1: Updated resistor values

Component	**Original Value**	**Revised Value**
R3	$130\,\mathrm{k\Omega}$	$10.2\,\mathrm{k\Omega}$
R6	$130\,\mathrm{k\Omega}$	$10.2\,\mathrm{k\Omega}$

In addition to numerical adjustments, the nodal connections of `R3` and `R6` were reconfigured. The original topology inadvertently altered the intended input and feedback resistance values of the operational amplifier, thereby distorting its gain and bandwidth characteristics. The revised layout ensures that the resistive network accurately reflects the theoretical design, restoring proper signal conditioning and dynamic response.

Transient Analysis of Output Signal Behavior

Following the frequency-domain evaluation, a time-domain (transient) analysis was performed to investigate the output signal behavior of the operational amplifier in response to input variations. The objective of this simulation was to assess the amplifier's ability to track fast transitions and to characterize its dynamic response under realistic operating conditions.

The simulation presents both the input and output waveforms, allowing for a direct comparison of their temporal profiles and highlighting any delay or distortion introduced by the circuit.

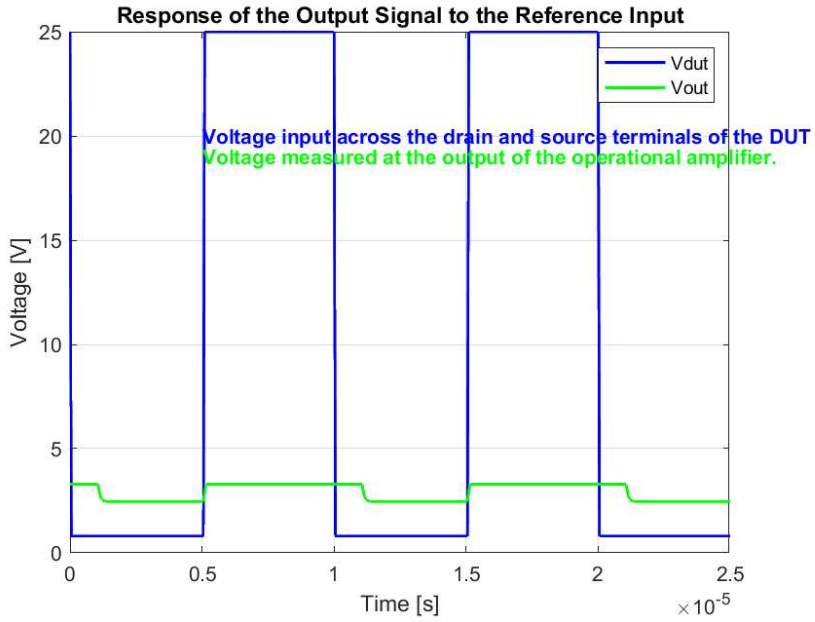


Figure 4.5: Transient simulation showing input and output signals of the conditioning circuit

A zoomed view of the waveform edges was extracted to examine the transition regions in greater detail. This analysis was conducted to highlight the delay of the output signal in tracking the input signal, quantified at approximately 0.10×10^{-5} seconds (i.e., 1 microsecond). The visualization provides information on the slope and timing of the output signal during rapid transitions, offering a clearer understanding of the amplifier's tracking performance.

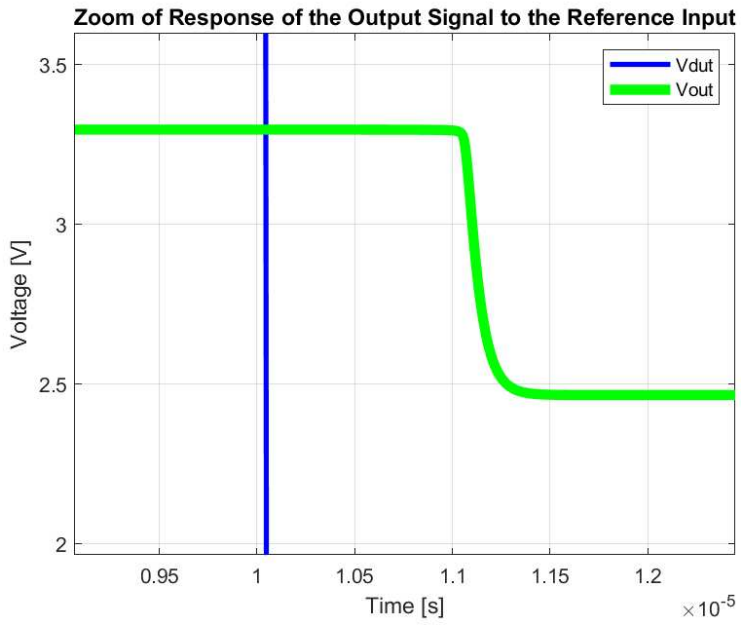


Figure 4.6: Zoomed view of waveform edges highlighting the output response during fast transitions

Temporal Dynamics and Slew Rate Constraints in Operational Amplifiers

In practical applications, operational amplifiers often exhibit a finite temporal response to abrupt input transitions, primarily governed by their limited *slew rate*—the maximum rate at which the output voltage can vary, typically expressed in volts per microsecond (V/μs).

Ideally, the output should mirror input variations instantaneously. However, due to intrinsic capacitances, current limitations, and architectural constraints, the output evolves with a bounded slope:

$$\left|\frac{dV_{\text{out}}}{dt}\right| \leq \text{SR}$$

Consider an input transition from 25 V to 0.8 V over 50 ns. For an amplifier with SR = 25 V/μs, the output requires:

$$t_{\text{slew}} = \frac{24.2\,\text{V}}{25\,\text{V}/\mu\text{s}} \approx 0.968\,\mu\text{s}$$

This 1 µs delay visible in the zoom of the waveform edges is not caused by the slew rate—instead, the slew rate only defines the maximum output-voltage gradient, and the earlier example assumed an SR of 25 V/µs, whereas our actual SR (and corresponding GBW) is significantly higher

Intrinsic Latency and Internal Delay Mechanisms

Beyond slew rate limitations, operational amplifiers may incur additional latency due to internal propagation delays, compensation networks, and parasitic capacitances.

These effects typically introduce delays ranging from several tens to hundreds of nanoseconds.

Such internal dynamics are particularly consequential in timing-sensitive applications, where sub-microsecond discrepancies can impair phase alignment or transient fidelity. Accurate modeling thus necessitates consideration of these non-idealities.

The cumulative delay between input transition and output settling can be approximated as:

$$t_{\text{total}} \approx t_{\text{input}} + t_{\text{slew}} + t$$

where:

- t_{input} denotes the duration of the input transition,
- t_{slew} reflects the slew rate-limited response time,
- t

Group Delay in Operational Amplifiers

Group delay time is the time interval between the arrival of a signal edge at the input and the emergence of its dominant frequency component at the output. In modern closed-loop operational amplifiers, this delay does not depend on the slew rate but rather on the phase dynamics introduced by passive elements, both internal and external.

- Internal Miller capacitance
  Each amplification stage incorporates a compensation capacitor (Miller capacitance) between the input and output. This capacitor creates a dominant low-frequency pole that slows the phase transition during a step, causing a measurable delay before the output begins to respond.

- External or feedback RC filters
  Feedback networks often include resistors and capacitors to ensure stability or to shape the frequency response. Each R–C pair produces a time constant

  $$\tau = R \cdot C$$

  which adds further delay to the propagation of the edge through the signal path.

These sources of group delay accumulate within the operational amplifier, defining an overall hesitation before the output response is delivered. Accurate evaluation of this delay is critical in high-speed systems, since even fractions of a microsecond can compromise signal fidelity and phase alignment.

4.1.2 Average Current Level

The Circuit 1 employs a current mirror to supply the bias current to the conditioning network. In an ideal scenario, both diodes would deliver identical average currents: the measured value is approximately 15.57 mA.

However, offsets of about 0.2 mA may arise due to process variations, intrinsic mismatches between the diodes, and parasitic effects within the bias network. These slight deviations are clearly observable in the i_{D4} trace, whereas in the i_{D3} trace large transient spikes render the steady-state level less apparent.

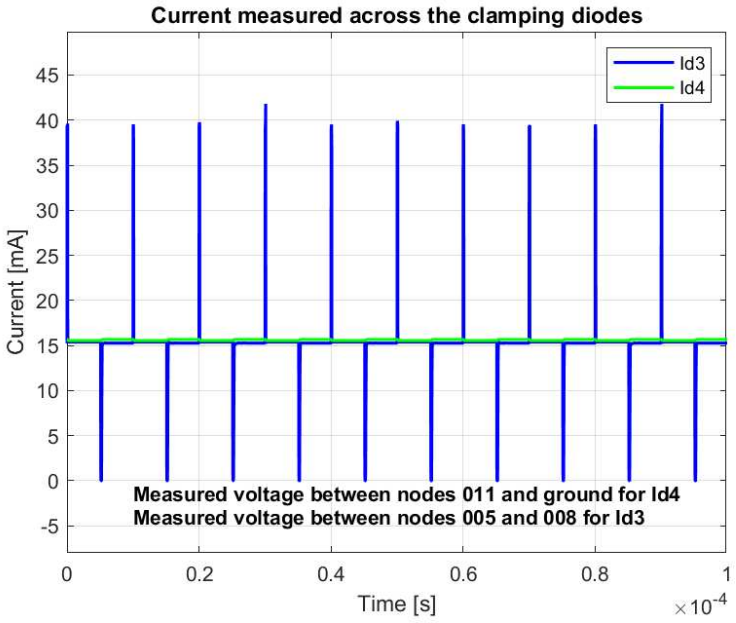


Figure 4.7: Comparison of current traces i_{D3} (blue) and i_{D4} (green) measured on the same scale.

4.1.3 Transient Spikes in i_{D3}

The trace corresponding to i_{D3} (blue) exhibits distinct transient spikes that significantly exceed the average current level. These spikes arise primarily due to:

1. **Clamping Action:** Diode D3 is employed to clamp excessive voltage during rapid switching transitions of the MOSFET. When the MOSFET switches from conduction to a non-conductive state, D6 is forced to conduct abruptly to limit the voltage, resulting in a sudden transient increase in current. This swift response produces pronounced overshoots in the i_{D3} branch.

2. **Dynamic and Parasitic Effects:** The rapid variations in voltage, combined with the non-ideal behavior of the current mirror and the influence of parasitic capacitances and inductances, contribute to temporary overshoots. These dynamic phenomena result in transient spikes that are superimposed on the steady bias current.

4.1.4 Stable Operation in i_{D4}

In contrast, the trace associated with i_{D4} (green) exhibits a flat, well-defined square-wave profile without any observable transient spikes. This stability is due to:

1. **Static Compensation Role:** Diode D4 is configured to compensate for the forward voltage drop incurred by D3 in a predominantly static manner. This ensures that the current remains uniformly constant at approximately 15.57 mA.

2. **Reduced Impact of Switching Transients:** Since D4 is not directly involved in the clamping function, it is not subjected to the rapid switching transients that affect D3. Consequently, the parasitic-induced overshoot phenomena that create spikes in i_{D3} are absent in the i_{D4} branch.

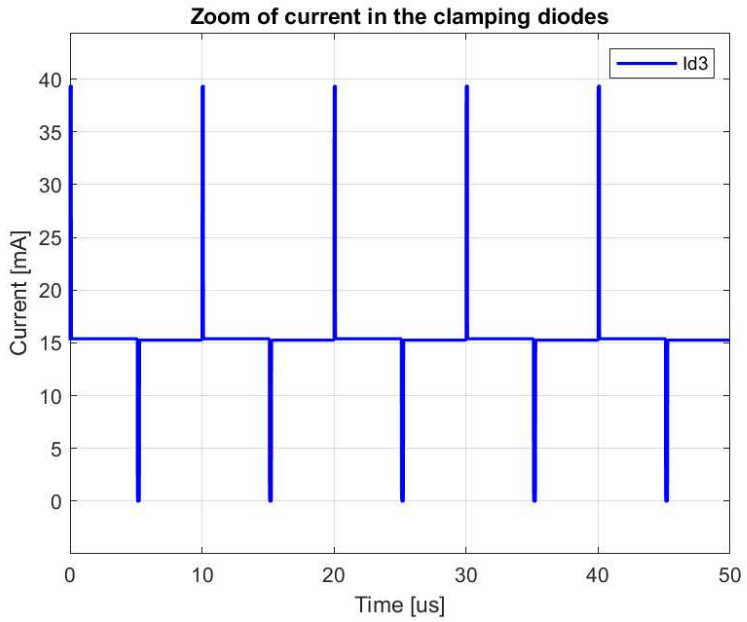


Figure 4.8: Zoomed view of the i_{D3} trace, illustrating its spikes on flat average current profile.

In summary, both branches achieve an average current level of approximately 15.57 mA with a slight offset of about 0.2 mA due to component tolerances and parasitic effects. Specifically:

- The i_{D3} branch exhibits significant transient spikes during fast switching events as a result of D6's clamping action and the associated dynamic parasitic effects.

- The i_{D4} branch, operating in a static compensation mode, maintains a perfectly flat square-wave profile free of transient distortions.

These observations confirm the effectiveness of the current mirror in ensuring identical average current values across both branches, while underlining the distinct roles of diodes D3 and D4 within the compensation circuit.

4.1.5 Voltage Behavior of the Diodes

The compensation diode (D4) reliably maintains a nearly constant voltage of approximately 0.7 V, which is consistent with the typical forward voltage drop of a silicon diode under normal conduction conditions [42]. Conversely, although the clamping diode (D3) exhibits an average forward voltage close to 0.7 V, transient current spikes—exceeding 50 mA—are accompanied by negative voltage excursions that dip to around -0.5 V.

Compensation Diode (D4)

The compensation diode is tasked with stabilizing the voltage in critical regions of the circuit. Measurements confirm that under normal operating conditions, the voltage across D4 remains constant at approximately 0.7 V. Figure 4.9 illustrates a comparison of the voltage across D4, confirming its stable behavior.

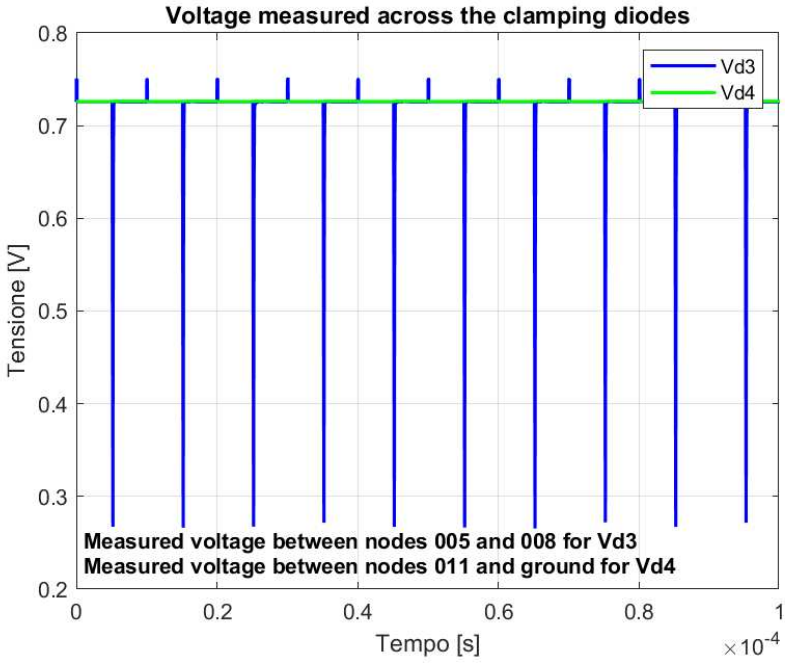


Figure 4.9: Voltage comparison across the compensation diode (D4). The voltage remains stable at approximately 0.7 V under normal conditions.

Clamping Diode (D3)

The clamping diode is designed to limit the voltage by quickly transitioning to conduction when the voltage exceeds a certain threshold. Although the mean voltage across D3 is also about 0.7 V, transient events—specifically, current spikes that can exceed 50 mA—result in voltage excursions. Notably, during these transients, the voltage waveform across D3 exhibits negative spikes reaching values near -0.5 V.

Mechanisms for Negative Voltage Spikes

Several phenomena contribute to these negative voltage spikes:

- **Transient Response and High $\frac{di}{dt}$:** The rapid change in current during clamping events induces significant voltage drops across parasitic inductances in the circuit. Given by $V_L = L\frac{di}{dt}$, these inductive voltage drops can oppose the abrupt change in current, causing a temporary negative excursion.

- **Parasitic Capacitance and LC Resonance:** The diode's junction capacitance, together with parasitic inductances from the PCB traces and packaging, forms an LC circuit. Under fast switching, this LC network may resonate and produce overshoot/undershoot phenomena—where the undershoot drives the voltage momentarily negative.

- **Reverse Recovery Effects:** During the transition from conduction to blocking, reverse recovery effects can occur. In this brief period, the diode's stored charge and the energy in the parasitic elements lead to a negative voltage spike. This negative overshoot is a hallmark of reverse recovery phenomena in fast, clamping operations [43].

Reverse Recovery Analysis of D3

Figure 4.10 shows the comparison of voltage and current waveforms for the clamping diode (D3) during reverse recovery. The graph clearly illustrates that the current spike, which exceeds 50 mA, is followed by a transient negative voltage spike (down to approximately -0.5 V). This behavior confirms that the negative voltage spikes are a consequence of the rapid transient induced by high $\frac{di}{dt}$, further accentuated by reverse recovery and parasitic effects.

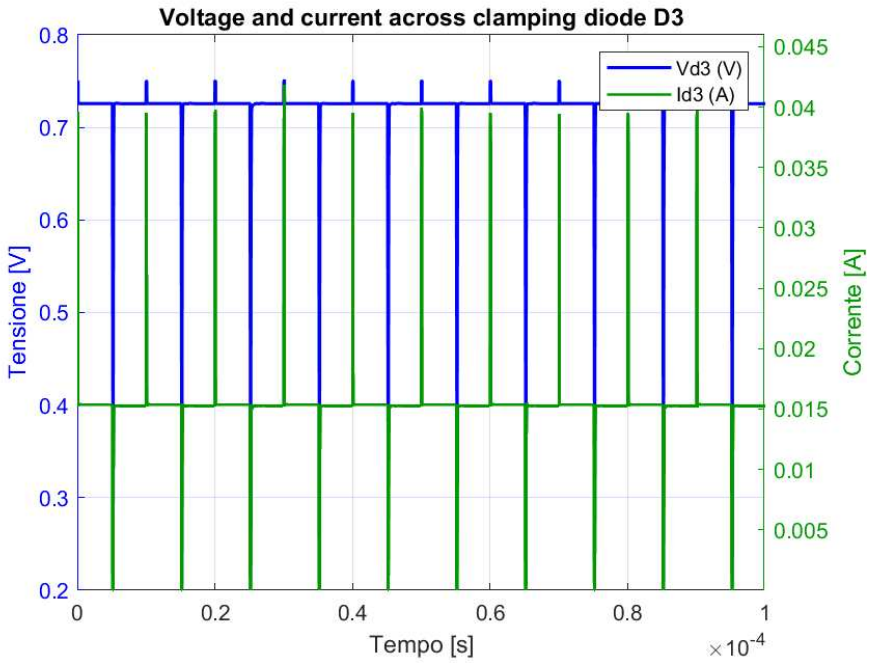


Figure 4.10: Comparison of voltage and current waveforms for the clamping diode (D3) during reverse recovery. The negative voltage spike (approximately -0.5 V) corresponds to the high current transient.

Resume of the diodes behavior

In summary, while the compensation diode (D4) consistently maintains around 0.7 V as expected, the clamping diode (D3) shows significant negative voltage spikes (approximately -0.5 V) during transient high current events. These negative excursions are primarily caused by:

- Inductive voltage drops due to high $\frac{di}{dt}$ across parasitic inductances.
- LC resonance resulting from the interplay of the diode's junction capacitance and parasitic inductances.
- Reverse recovery phenomena that contribute to an undershoot in the voltage during rapid switching.

These findings provide vital insights for the optimization of clamping circuits, emphasizing the need to account for parasitic effects and the dynamic behavior of diodes in high-speed applications.

4.2 Circuit 2: Configuration and Results

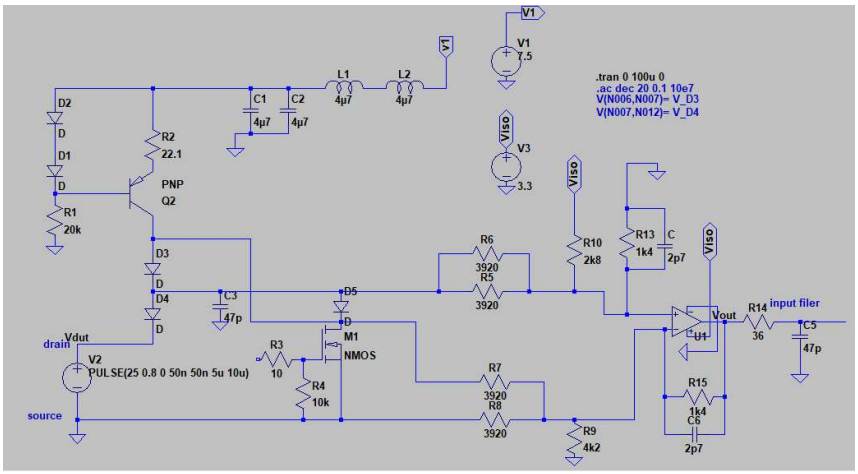


Figure 4.11: Ideal configuration of circuit 2, before the components replacement, as shown above.

4.2.1 Frequency Response Analysis of Circuit 2 (Ideal Model)

As a continuation of the methodology described in the previous subsection, a frequency-domain analysis was performed on Circuit 2 to evaluate its dynamic behavior. The Bode diagram below illustrates the magnitude response, highlighting the system's bandwidth characteristics under its default configuration.

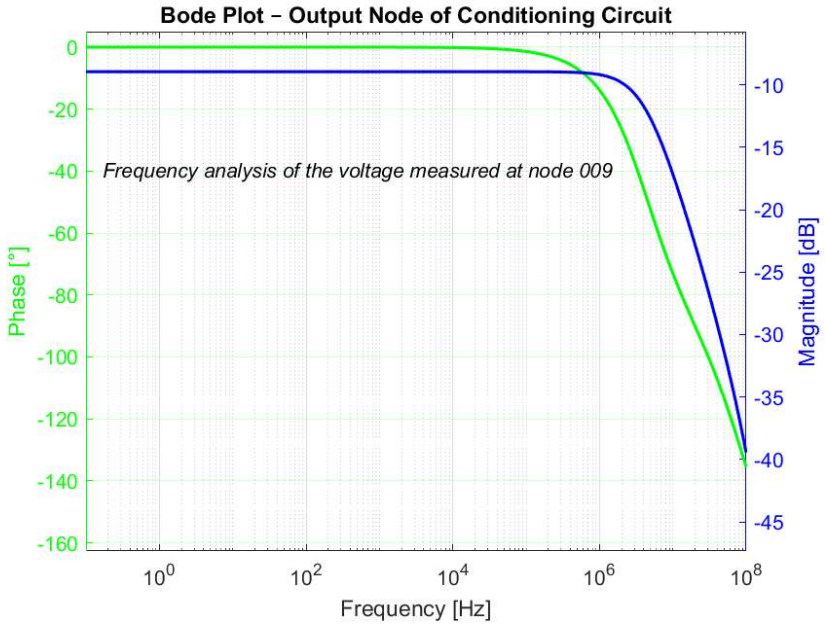


Figure 4.12: Magnitude response of Circuit 2 without parameter modifications

To better visualize the cutoff point, a zoomed view of the frequency region around the $-3\,\mathrm{dB}$ threshold was extracted. The maximum gain observed in the

simulation was $-10.365\,\mathrm{dB}$; accordingly, the cutoff frequency was identified at the point where the gain drops to $-13.365\,\mathrm{dB}$. This corresponds to a cutoff frequency of approximately $4.467\,\mathrm{MHz}$, confirming the circuit's ability to operate effectively within high-frequency domains.

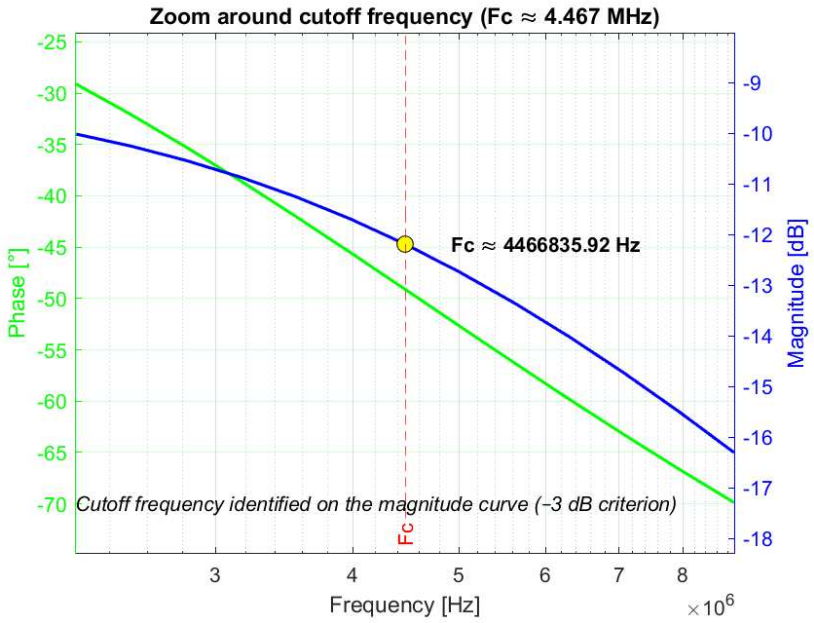


Figure 4.13: Zoomed view of the cutoff region showing the $-3\,\mathrm{dB}$ drop in Circuit 2

4.2.2 Detailed Analysis of the Clamping Circuit Behavior

Clamping Diodes in the Conditioning Circuit

To connect the current mirror to the conditioning circuit based on the operational amplifier U1 (OPA354AIDBVR), two clamping diodes, denoted D3 and D4, were inserted. These components primarily serve to protect the drain–source voltage measurement stage (v_{DS}) from potential transient excursions generated during MOSFET switching. Their inclusion ensures that the operational amplifier receives a reliable signal devoid of undesired spikes, thus preserving the accuracy of the measurement chain.

Operation During MOSFET Conduction

When the MOSFET is in conduction, the drain–source voltage ($v_{DS,ON}$) assumes values on the order of a few hundred millivolts. In this condition, diodes D3 and D4 remain reverse-biased, and the op amp U1 receives at its inputs a differential

$$v_{\mathrm{in,U1}} = v_{DS} + v_{D4} - v_{D3}.$$

Since the diodes do not conduct, the voltage drops v_{D3} and v_{D4} can be neglected. Consequently,

$$v_{\text{in}} = v_{DS},$$

isolating the drain–source voltage v_{DS} from any offset due to the clamping diodes.

Operation During Switching Transients

During switching transitions, the high voltage gradient (dV/dt) across the MOSFET can generate very fast spikes, often exceeding the direct withstand capability of the op amp. In this context, the clamping diodes intervene through two distinct mechanisms:

1. *Parasitic capacitance*: Even without conduction, the diodes act as junction capacitors, providing a low-impedance path for the high-frequency components of the transient. This reduces both the amplitude and the slew rate of the spikes applied to the measurement input.

2. *Direct conduction*: If the transient exceeds the diodes' forward threshold, they switch on, clamping the protected node within a voltage window compatible with the op amp's input specifications.

Effects of Reverse Recovery

When a diode switches from forward conduction to reverse bias, reverse recovery occurs. During this phase, the charge carriers accumulated in the junction must be removed, causing a transient reverse current that may momentarily distort the waveform. To minimize this effect, the selected diodes (S1N-13-F) are ultrafast types characterized by an extremely short reverse recovery time. The limited recovery charge and the rapid extinction of the reverse current render the reverse recovery impact on the measured signal negligible, thereby preserving the conditioning chain's accuracy.
In summary, diodes D3 and D4 do not directly "absorb" the voltage derivative but mitigate it via their junction capacitance and, in extreme cases, through direct conduction followed by reverse recovery. The overall effect is a significant attenuation of high-frequency transients that, without protection, would be applied directly to the operational amplifier. This strategy ensures that the conditioning stage receives only the useful conduction-voltage component, enabling reliable measurements even under extreme electrical stress.

Expected Function Operation and Graph Observations

The design anticipates that a constant bias current is supplied uniformly to both branches. Owing to the exponential characteristic of the diode current–voltage (I-V) relationship, even a minute deviation in the bias current will produce a significantly different forward voltage drop. Hence, any slight dissimilarity in the bias currents in the two branches translates immediately into a voltage discrepancy.

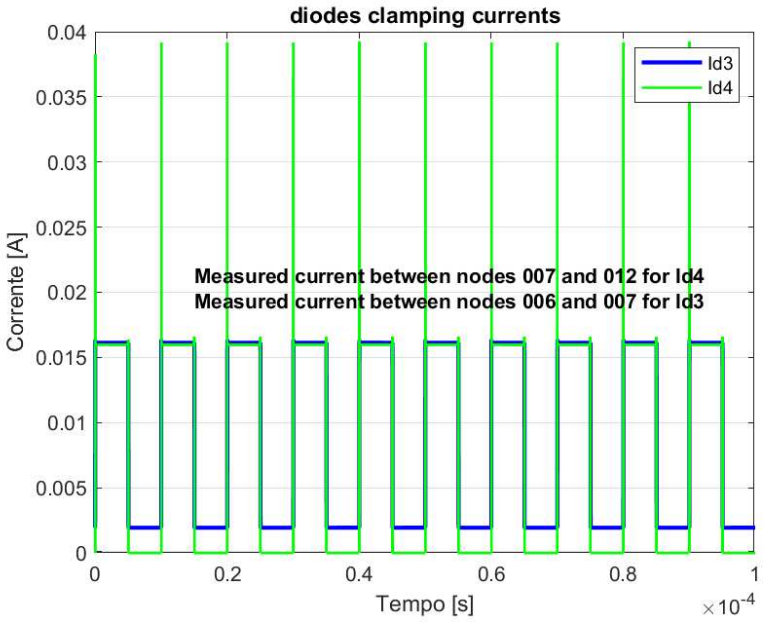


Figure 4.14: Ideal current comparison between the two diode

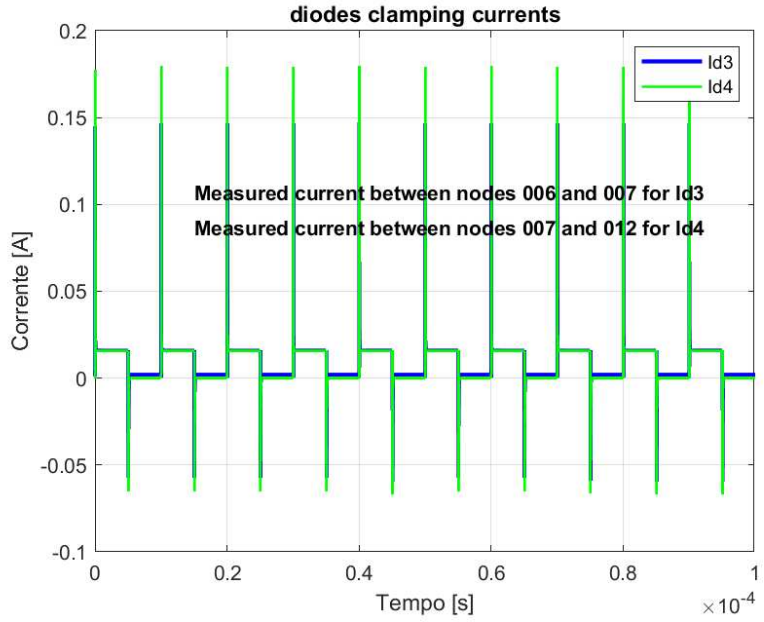


Figure 4.15: Real current comparison between the two diode

Measured Waveform Characteristics

In practice, the measured waveforms indicate that:

- In the *ideal* implementation (experimental), the blue trace (`id3`) varies between approximately 2 mA and 16 mA, whereas the green trace (`id4`) varies between 0 mA and 16 mA.

- In the *real* implementation (experimental), the diode currents exhibit values analogous to those in the ideal model.

These observations establish a current difference ΔI, which produces a corresponding voltage difference

$$\Delta V = V_{d4} - V_{d3} \neq 0.$$

Consequently, from Equation above, the operational-amplifier input becomes

$$V_{\text{in}} = V_{DS} + \Delta V.$$

The bias network is designed to equalize the diode drops and thus eliminate the difference $V_{d4} - V_{d3}$, although in practice V_{d3} remains slightly different from V_{d4}.

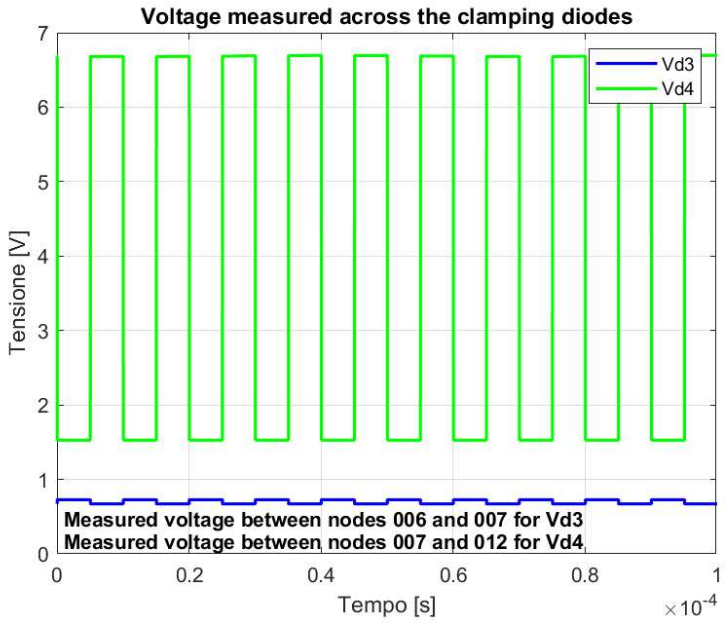


Figure 4.16: Ideal voltage comparison between the two diode

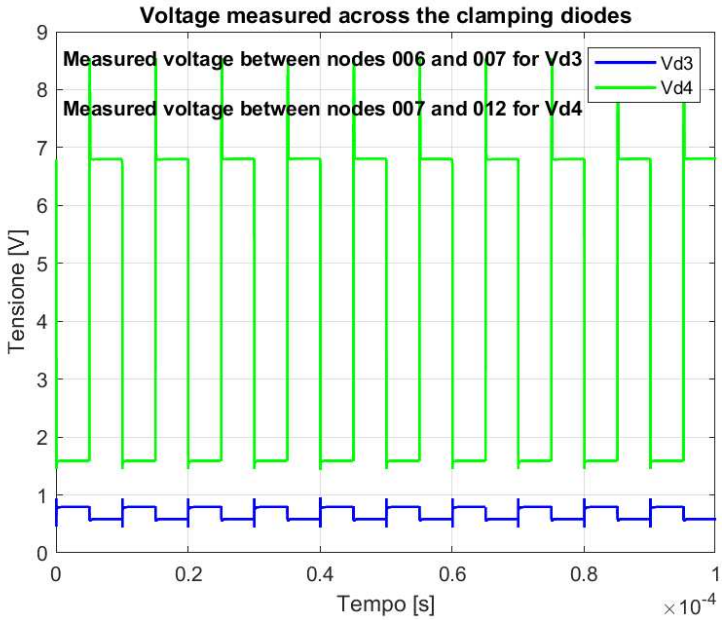


Figure 4.17: Real voltage comparison between the two diode

For proper operation of the conditioning circuit, the non-inverting and inverting inputs must be driven by signals of nearly identical amplitude. This close matching minimizes the differential input voltage, allowing the amplifier to operate in its linear region and accurately amplify only the intended small voltage difference. The outcome is a clean, low-noise conditioned waveform, ideally suited for 14-bit sampling by the downstream ADC.

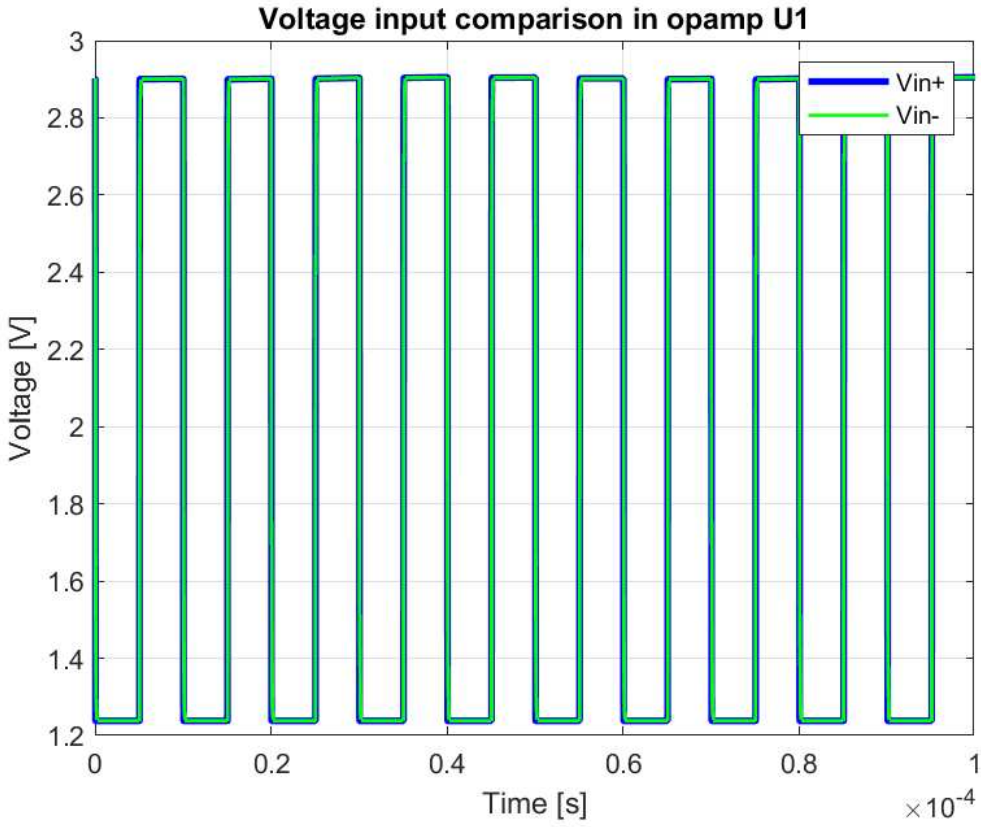


Figure 4.18: Comparison of the signals applied to the non-inverting (+) and inverting (–) inputs of the operational amplifier.

Effects of Commutation, Non-Idealities, and Duty Cycle Influences

The circuit operates under a pulse-width modulation (PWM) regime (e.g., at 20 kHz), whereby rapid transitions between on and off states occur within each cycle. These rapid transients yield two important effects:

1. **Switching Transients:** The very short switching intervals produce non-negligible di/dt effects; transient currents, along with parasitic capacitances and finite recovery times (of both the diodes and the op-amp circuitry), mean that the sampling instants (denoted as SP1 and SP2 in the literature) may not fall in a fully stabilized portion of the conduction period. This results in momentary differences between the two branches.

2. **Exponential I–V Dependency:** Because the diode I-V law is exponential, even a small difference in the instantaneous current (on the order of a few mA) leads to a disproportionately larger difference in the forward voltage drop, preventing perfect cancellation.

Furthermore, variations in the PWM duty cycle can influence the effective instant of sampling:

- **Increased Duty Cycle:** A higher duty cycle prolongs the on-state interval. This extended conduction time promotes greater stabilization of the bias current, so that the sampling occurs when the current has fully settled.
- **Decreased Duty Cycle:** Conversely, a reduced duty cycle shortens the on-state interval and increases the likelihood that the sampling instant occurs during a transient phase, thereby exacerbating the measured discrepancy.

Thus, changes in the duty cycle directly affect the sampling instant and consequently the measured bias current values, although the overall voltage offset ΔV remains nearly constant between simulation and experimental settings.
In summary, the clamping circuit is designed to deliver a constant bias current through two communicating diode branches such that the forward voltage drops V_{d6} and V_{d4} are equal, ensuring that

$$V_{\text{in}} = V_{\text{ds}} + (V_{d4} - V_{d3}) \quad \text{with} \quad V_{d4} - V_{d3} = 0.$$

However, both simulation and experimental measurements demonstrate that the currents settle at two distinct levels, resulting in a constant offset

$$\Delta V = V_{d4} - V_{d3} \neq 0,$$

so that the actual signal at the op-amp input is

$$V_{\text{in}} = V_{\text{ds}} + \Delta V.$$

This outcome arises from the dynamic effects associated with PWM commutation, parasitic element non-idealities, and the exponential behavior of the diode I-V relationship. Modifications to the duty cycle will affect the sampling timing—yielding more stable current readings at higher duty cycles and more pronounced transient effects at lower duty cycles—but the inherent offset remains effectively the same in both ideal and real cases. As a result, the overall waveform ("solfa") observed at the op-amp input is essentially invariant across simulation and real implementations.

4.3 Circuit 3: Configuration and Results

4.3.1 Purpose and Necessity of a Dedicated Current-Source Circuit

In the analogue conditioning network presented by Stella *et al.* (2020) , the current-source stage implemented with Q1 fulfils several critical functions, to understand the crucial role of Q1, the image of the circuit in question is attached below.

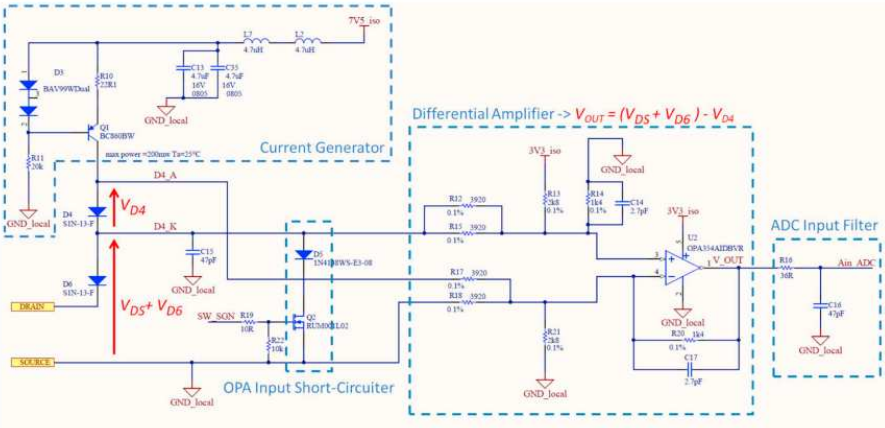


Figure 4.19: The general porpouse of current-source circuit.

First, it provides a constant bias current to diode D6 so that, immediately upon MOSFET turn on, D6 is forward biased and its forward voltage V_F can be used as a reproducible proxy for $V_{\mathrm{DS(on)}}$. Without this presaturation bias, D6 would remain non-conducting until $V_{\mathrm{DS(on)}}$ exceeds the diode threshold ($\approx 0.7\,\mathrm{V}$) , introducing measurement discontinuities.

Second, by placing a matched diode D4 in series, the differential amplifier only senses the small voltage difference $V_F(D6) - V_F(D4)$, typically a few millivolts that depend predominantly on device temperature. This arrangement effectively isolates the amplifier input from the high bus voltage (e.g. 600 V in the OFF-state), ensuring safe operation and preserving the linearity of the thermal-sensitive measurement [**?**].

Third, the constant-current bias improves signal-to-noise ratio by stabilising the diode conduction, while disabling Q2 allows the stage to maintain a bandwidth up to 40 MHz, sufficient to follow rapid switching transients without amplifier saturation.

Circuit 3: Modeling

The dedicated current-source circuit is therefore indispensable to:

- Ensure *immediate* and *continuous* forward conduction of D6 upon MOSFET activation, eliminating clamping delay;
- Provide robust *electrical isolation* of the measurement amplifier from high bus voltages;

- Enhance *measurement linearity* and *signal integrity* by generating a stable, temperature-dependent voltage signal.

The implementation of Circuit 3 retains the fundamental blocks of signal conditioning. In particular, the non-inverting operational amplifier stage—responsible for ensuring logical communication and proper microcontroller control—remains unaltered, as do the ADC filtering systems and the op-amp input short-circuit protection. Concurrently, a significant modification has been applied to the bias current generation branch. Initiated by substituting the bipolar transistor Q1, this branch has been completely redesigned to achieve controlled clamping of the two diodes. Consequently, when the MOSFET is turned off, the op-amp is not subjected to the device's nominal 800 V, but rather it observes only the differential voltage between node V_{d6} and node V_{d4}.

In this context, the differential voltage is defined as

$$\Delta V = V_{d6} - V_{d4},$$

and is purposely sized to be on the order of a hundreds millivolts . This design choice ensures exceptional sensitivity and high precision in measurement, allowing the signal conditioning circuit and the subsequent analog-to-digital conversion stage to operate within an optimized measurement domain. As a result, even minute variations in the signal are captured without interference from excessive voltage levels that would otherwise occur in the absence of controlled clamping.

4.3.2 Proposed i_{BIAS} Generator for Circuit 3

To keep D6 continuously forward-biased while leaving unchanged all other measurement blocks (ADC interface, OPA "short-input" protection network, and main op-amp), we replace the simple transistor-only bias with a precise, op-amp-controlled current source. The schematic in Figure **??** shows the new i_{BIAS} stage.

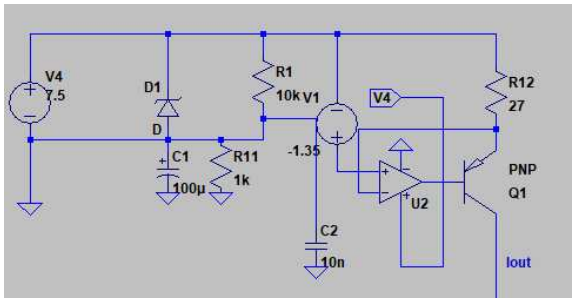


Figure 4.20: first draft of circuit 3's current mirror, it's shown how it should work if the non inverting pin of opamp recieve [7.5 V + (-1.35)V]

4.3.3 Voltage Divider Calculation for Improved Current Mirror in Circuit 3

The goal is to improve the current mirror configuration in order to not use a second voltage generator that lowers the input voltage to the non-inverting pin, so we

use a voltage divider. In this revised design, an op amp in combination with a bipolar transistor was chosen to achieve a superior current waveform compared to the previous current mirror. To properly condition the non-inverting input of the op amp, a voltage divider is used to adjust the available input voltage of 7.5 V down by 1.35 V, resulting in an effective bias voltage of 6.15 V.

The voltage divider is defined by the expression:

$$V_{\text{out}} = V_{\text{in}} \cdot \frac{R_2}{R_1 + R_2}$$

where:

- $V_{\text{in}} = 7.5\,\text{V}$ is the supply voltage,
- $V_{\text{out}} = 6.15\,\text{V}$ is the desired voltage at the non-inverting op amp input.

Substituting the values:

$$\frac{R_2}{R_1 + R_2} = \frac{6.15}{7.5} \approx 0.82.$$

This means R_2 must be about 82% of the total resistance, while R_1 constitutes the remaining 18%. Expressing R_1 in terms of R_2:

$$R_1 = \left(\frac{1 - 0.82}{0.82}\right) R_2 \approx 0.22\, R_2.$$

For example, if we choose $R_2 = 10\,\text{k}\Omega$, then:

$$R_1 \approx 0.22 \times 10\,\text{k}\Omega \approx 2.2\,\text{k}\Omega.$$

Thus, the voltage divider provides:

$$V_{\text{out}} \approx 7.5\,\text{V} \times \frac{10\,\text{k}\Omega}{2.2\,\text{k}\Omega + 10\,\text{k}\Omega} \approx 6.15\,\text{V},$$

which is appropriate for biasing the non-inverting input of the op amp in our modified current mirror circuit, as shown below.

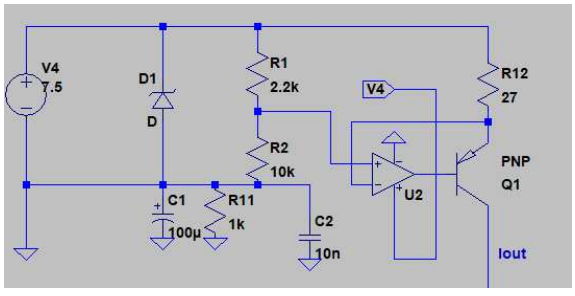


Figure 4.21: last model of circuit 3's current mirror

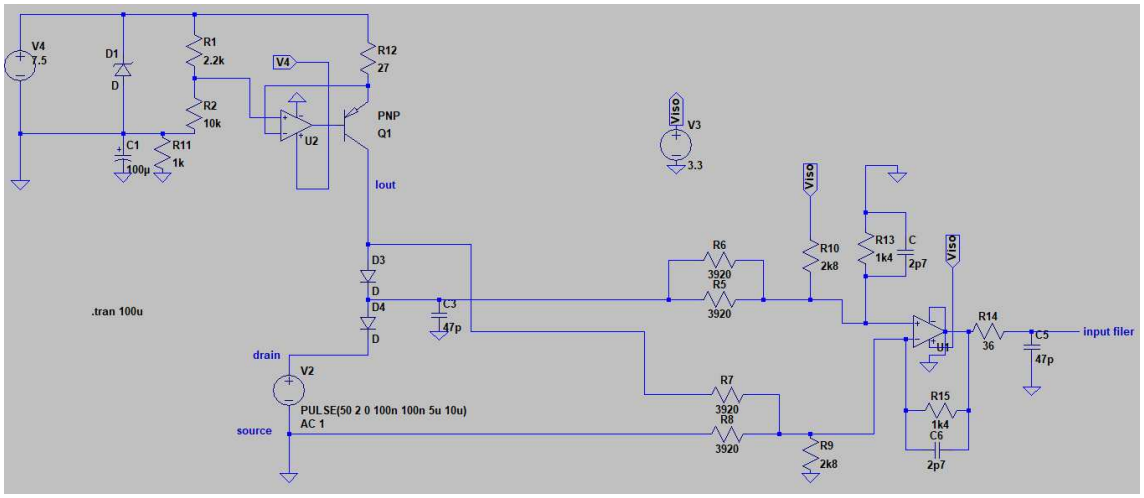


Figure 4.22: last model of circuit 3

4.3.4 Frequency Response Analysis of Circuit 3 (Ideal Model)

Like as the others chapter, the frequency response of Circuit 3 was analyzed, underlining the critical role of frequency domain analysis in verifying signal transfer and filter performance. The focus is directed toward the analysis of Circuit 3, implemented exclusively with ideal components. In this ideal model, losses and parasitic effects are neglected in order to establish a theoretical benchmark for the expected filter behavior.

AC Analysis and Bandwidth Determination

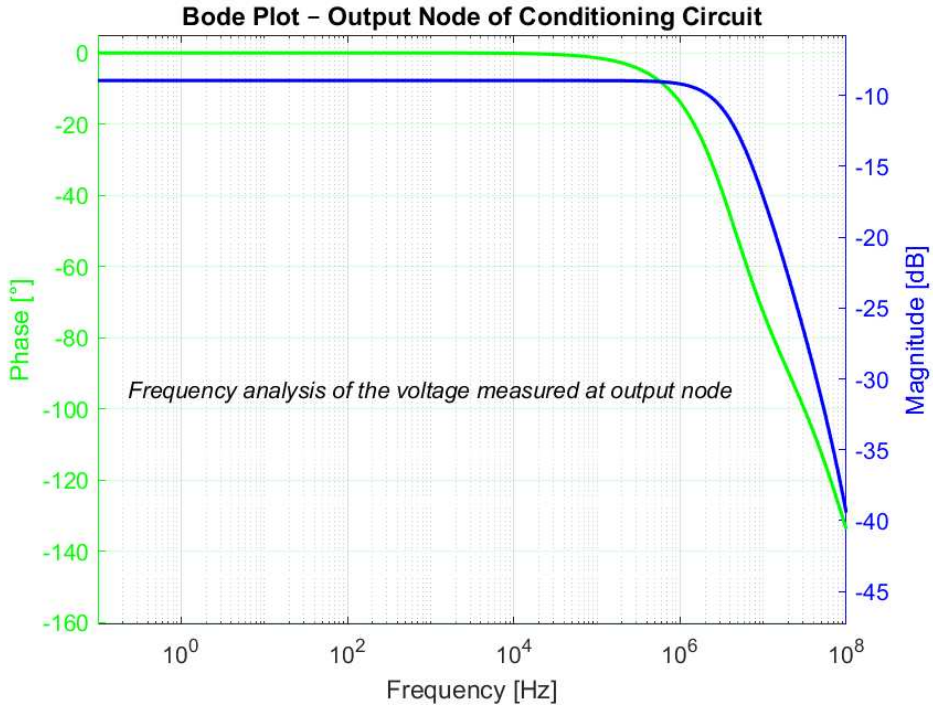


Figure 4.23: Frequency response of Circuit 3 over the range 1 Hz – 100 MHz.

The frequency response of Circuit 3 was investigated in LTspice through AC analysis in the range from 1 Hz to 100 MHz. The maximum gain was found to be $-8.94\,\text{dB}$. According to the $-3\,\text{dB}$ rule, the cutoff frequency was identified at $4.467\,\text{MHz}$. This value represents the bandwidth of the system, beyond which the gain decreases at the expected slope of approximately $-20\,\text{dB/decade}$, confirming the low-pass behavior of the circuit.

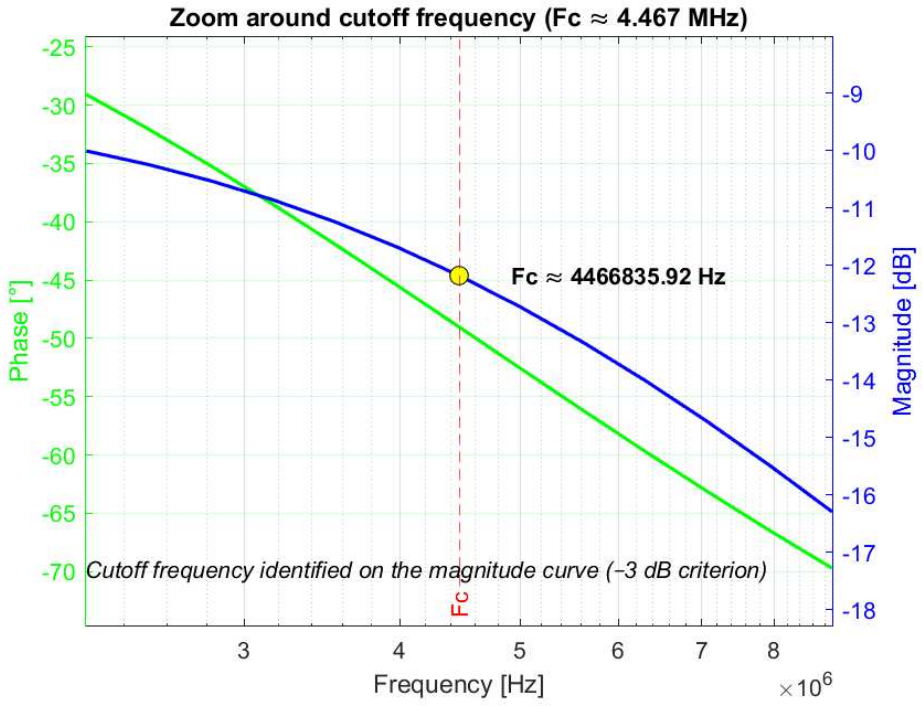


Figure 4.24: Zoomed view of the cutoff frequency at $f_c = 4.467\,\text{MHz}$.

A wide bandwidth is advantageous as it enables a faster dynamic response and reduces signal distortion, thereby improving measurement fidelity. Simulations also showed that variations in the input square-wave amplitude do not affect the cutoff frequency, although they may lead to saturation in the conditioning circuit associated with the DUT when the applied voltage is particularly high.

4.3.5 Detailed Analysis of the Clamping Circuit Behavior

The performance of the current mirror, which characterizes the ideal circuit 3, was evaluated to investigate the propagation of the generated bias current, I_{bias}, throughout the system in terms of its average value. In the implemented configuration, an inverting operational amplifier is employed together with a bipolar transistor. This arrangement yields a highly precise current mirror. The biasing network was carefully dimensioned using a tailored voltage divider to ensure that the I_{bias} generation circuit produces an intended current of 50 mA. Experimental measurements confirm that the average bias current closely approximates the 50 mA target, aside from minor transient spikes that are negligible on a global time scale [**?**].

At first, these transient spikes were not evident. However, by zooming into the waveform, it became apparent that the spikes occur simultaneously with the off-to-on and on-to-off transitions of the device under test (DUT). Detailed inspection of the voltage waveform across resistor R_{12} shows that the transient spikes in the bias current are mirrored by corresponding perturbations in the voltage drop across R_{12}. Such behavior is inherently due to the switching transitions of the DUT, which are accompanied by transient responses caused by parasitic capacitances and by the abrupt redistribution of charge during state changes [**?**].

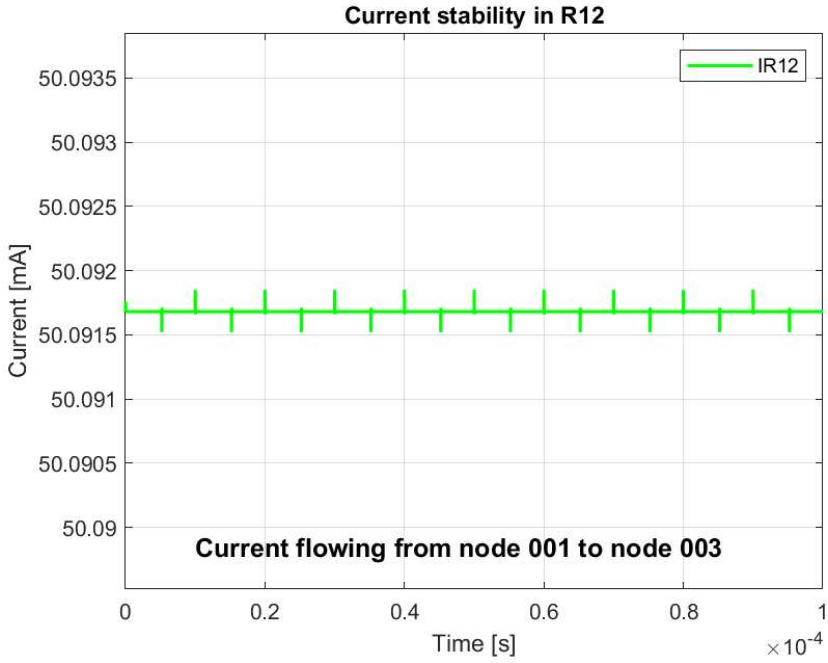


Figure 4.25: Current waveform measured across resistor R_{12}.

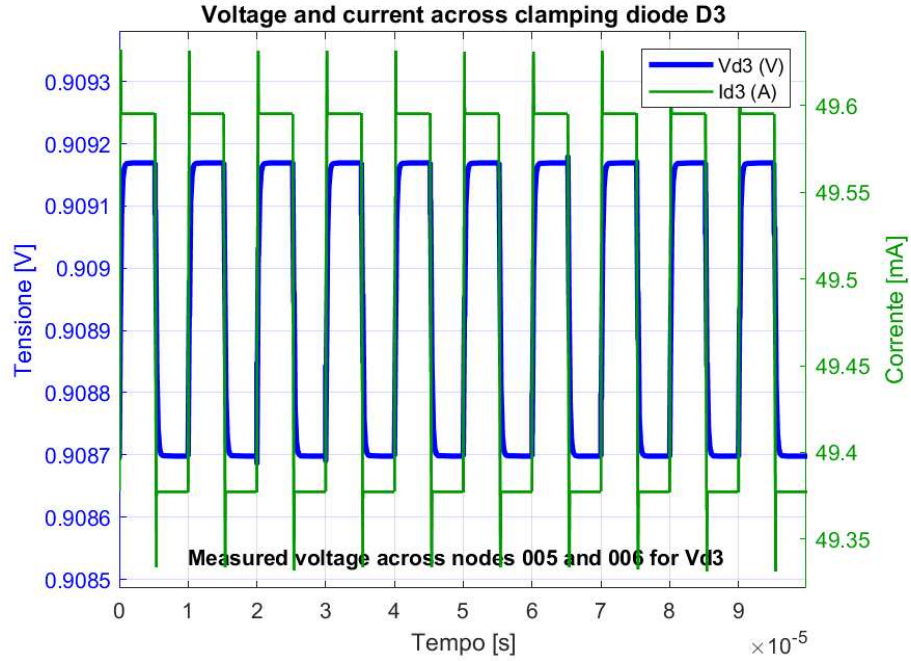


Figure 4.26: Comparative analysis of the current ($I_{R_{12}}$) and voltage ($V_{R_{12}}$) measured across resistor R_{12}.It's possible to see the transient spike shows above

A similar comparative analysis was performed on the voltage drops across the clamping diodes and the compensation diode. The results indicate that the transient events observed in the diode voltage and current waveforms occur at the same instants as those seen across R_{12}. This synchronization confirms that the observed

disturbances stem directly from the DUT switching events and are thus a natural consequence of the circuit's transient behavior during switching.

Clamping diode considerations

In the ideal circuit, the clamping diode exhibits a nearly constant current, oscillating around a mean value of

$$I_{D,\text{ideal}} = 49\,\text{mA} \quad \text{with a peak-to-peak variation } \Delta I_{pp,\text{ideal}} = 0.3\,\text{mA},$$

when the device under test (DUT) is powered with voltages ranging from 0 to 2 V. Similarly, the voltage across the diode oscillates about a mean value of

$$V_{D,\text{ideal}} = 755.66\,\text{mV} \quad \text{with } \Delta V_{pp,\text{ideal}} = 0.2\,\text{mV}.$$

These small variations are negligible with respect to the measurement precision.

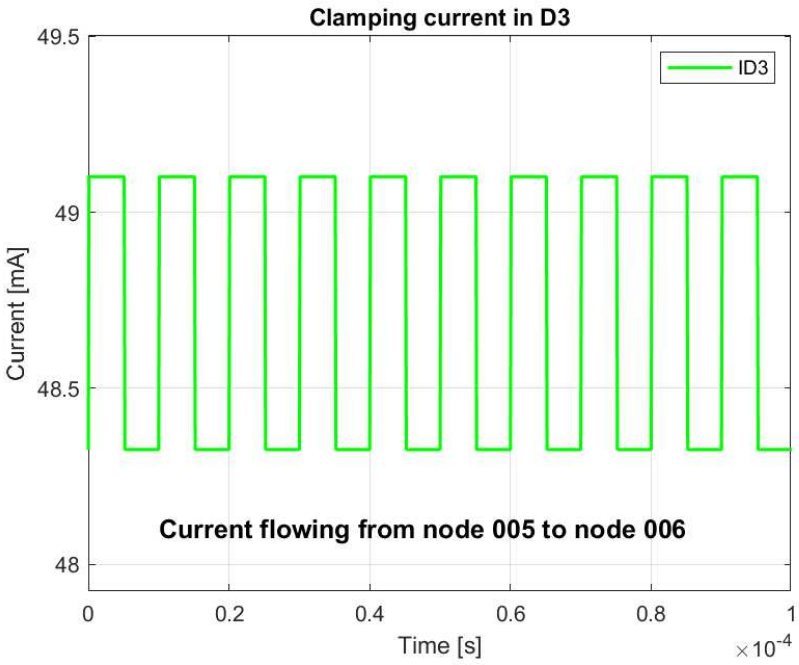


Figure 4.27: Clamping current of ideal circuit 3.

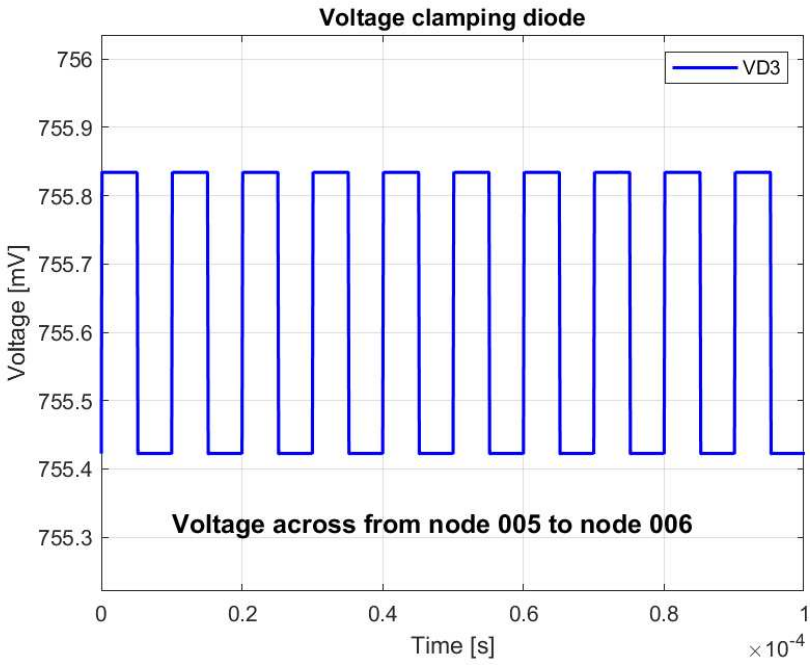


Figure 4.28: Voltage waveforms measured for the clamping diode D3 of the ideal circuit. as can see the voltage is a square wawe.

Conversely, in the real circuit the diode current remains approximately the same ($I_{D,\text{real}} \approx 49\,\text{mA}$); however, the diode voltage exhibits a noticeable increase of about 150 mV in its mean level. Consequently, the voltage oscillates around

$$V_{D,\text{real}} \approx 909\,\text{mV} \quad \text{with } \Delta V_{pp,\text{real}} \approx 2\,\text{mV},$$

due to parasitic effects introduced by the use of real components.

Furthermore, a zoomed analysis of the voltage waveform reveals changes in the rising and falling edges; the waveform loses its ideal square shape during transitions. Despite this, the overall dynamic performance remains highly competitive and the measurement precision acceptable.

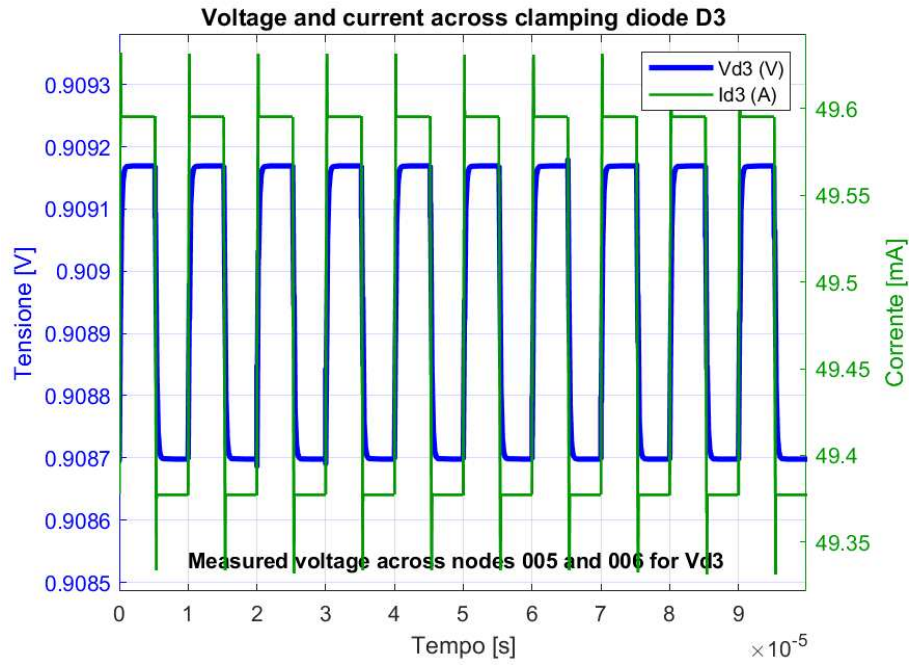


Figure 4.29: voltage and current comparison of clamping diode D3.

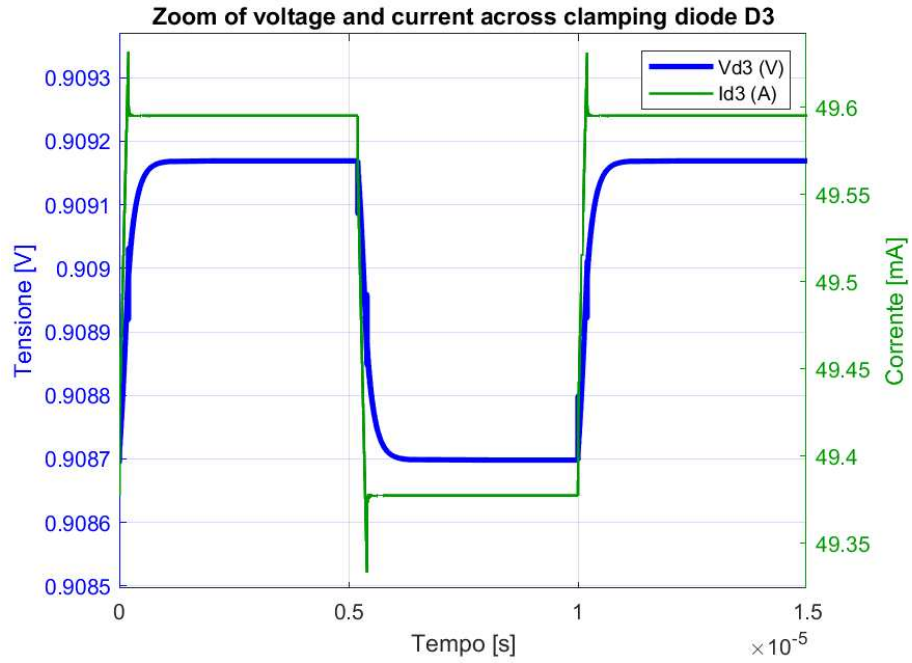


Figure 4.30: Zoom on the rising and falling edges of the voltage on the clamping diode.

4.4 Circuit 4: Configuration and Results

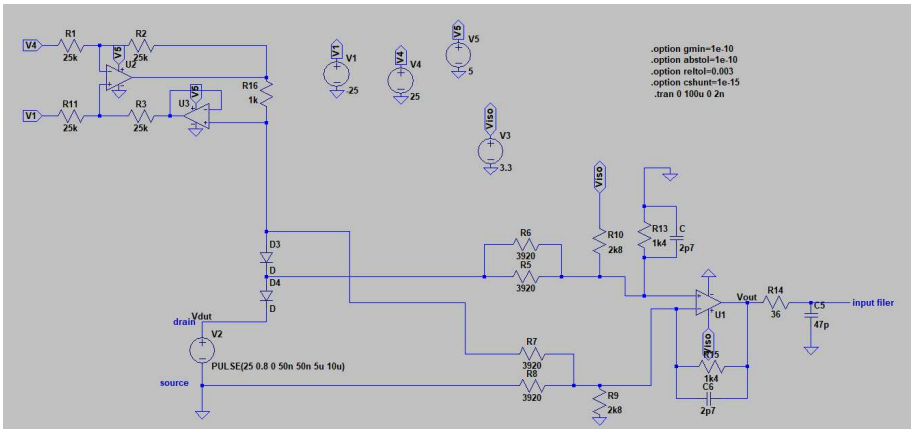


Figure 4.31: Schematic of circuit 4 in the ideal case

4.4.1 Modified Power Supply Configuration

In the updated version of Circuit 2, the conditioning circuit for the Device Under Test (DUT) and the ADC remains unchanged. The original input block, referred to as the "OPA short circuiter," is removed and replaced by a current mirror implemented using two operational amplifiers (op-amps), as illustrated below.

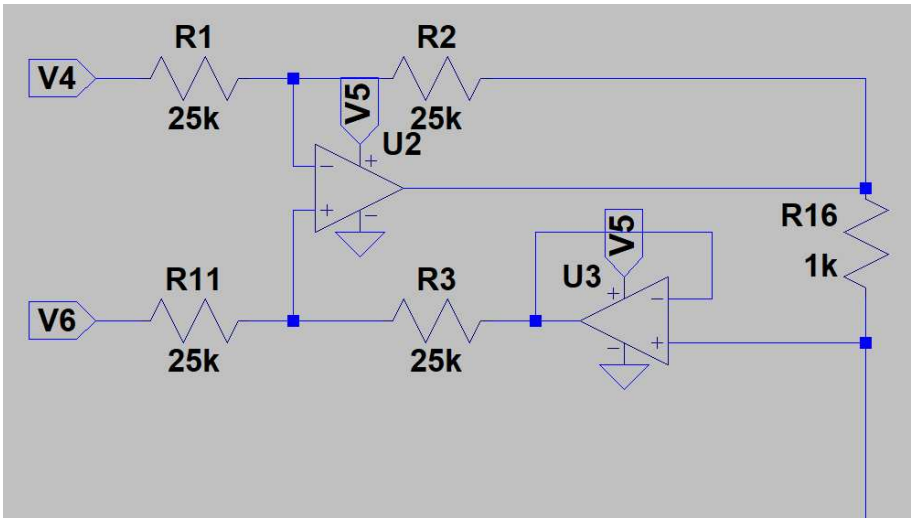


Figure 4.32: Zoom of circuit 4's current mirror

In this configuration, the power supply is provided by two voltage sources, denoted as V_4 and V_6, which deliver $+75\,\mathrm{V}$ and $+25\,\mathrm{V}$, respectively. The positive terminal of V_4 is connected to the node previously labeled V_1, while the negative terminal of V_6 is connected to the node formerly designated as V_2. This dual-supply arrangement ensures a symmetric voltage swing around ground.

The primary objective of the circuit is to establish a constant current through the resistor R_{16}, which has a resistance of $1\,\mathrm{k}\Omega$. The resulting current is:

$$I = \frac{V_4 - V_6}{R_{16}} = \frac{75\,\text{V} - (25\,\text{V})}{1\,\text{k}\Omega} = \frac{50\,\text{V}}{1000\,\Omega} = 50\,\text{mA}$$

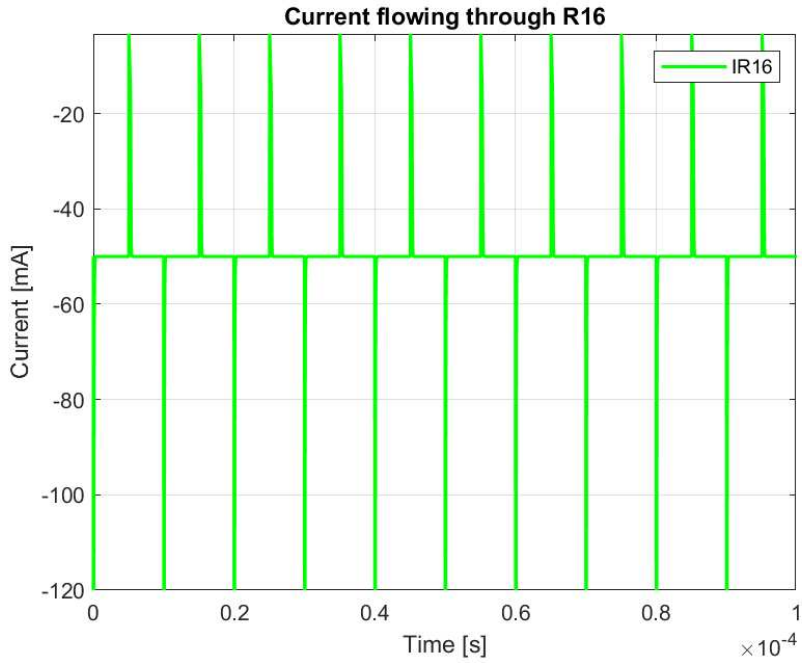


Figure 4.33: Current flowing through resistor R16 in the current mirror.

4.4.2 Operation of the Dual-Op Amp Current Mirror

The current mirror is designed to maintain a reference current of 50 mA through R_{16}. Its operation is divided into two stages:

Reference Stage

The first op-amp monitors the voltage drop across a current-sensing resistor (associated with the 50 mA reference current) and compares it with a fixed internal reference. By stabilizing this voltage drop, the stage sets the correct operating point corresponding to the desired current.

Replication Stage

The second op-amp, configured in a buffer or servo arrangement, receives the error signal from the reference stage and adjusts the output branch accordingly. Through active feedback, it drives the current in the output such that the current through R_{16} precisely replicates the 50 mA reference. Consequently, variations in load are immediately compensated, ensuring that the desired current remains constant. With a dual ± 25 V supply, the circuit operates within a wide voltage range while maintaining accurate current regulation.

4.4.3 Characteristics of Dual-Supply Op-Amps

The op-amps employed in this design are powered by a symmetric dual supply: +75 V and +25 V. This configuration allows for full-range input and output swing, improving linearity and dynamic response. Modern op-amps designed for dual-supply operation can handle wide voltage excursions and are well suited for precision analog applications.

4.4.4 Advantages and Disadvantages

Advantages

- **Precision and Stability:** The dual-op amp feedback loop ensures accurate replication of the reference current, effectively compensating for load variations.
- **Wide Voltage Operation:** The 50 V supply enables high dynamic range and compatibility with various analog subsystems.
- **Enhanced Control:** The two-stage configuration improves linearity and maintains the output current at a constant 50 mA.

Disadvantages

- **Increased Complexity:** The use of two op-amps and additional biasing components results in a more complex circuit compared to simpler alternatives.
- **Higher Power Consumption:** The active feedback mechanism may lead to slightly higher power consumption than solutions based on bipolar transistors coupled with an inverting op-amp.
- **Frequency Response Limitations:** The slew rate and bandwidth of the dual-op amp configuration may be less favorable in high-frequency applications compared to those employing bipolar devices.

In summary, the modified current mirror, employing two op-amps powered by a ±25 V dual supply, is capable of delivering a stable 50 mA through resistor R_{16} while keeping the ADC conditioning circuit unchanged. Although this approach introduces greater complexity and marginally higher power consumption compared to a current mirror based on bipolar transistors with an inverting op-amp, it provides superior precision, stability, and wide-voltage performance. These attributes make it a suitable solution for high-performance analog systems.

4.4.5 AC Analysis and Bandwidth Determination

An AC sweep of Circuit 4 was performed in LTspice over the frequency range 1 Hz–100 MHz. The primary objective was to determine the peak small-signal gain, −8.94 dB, and to identify the cutoff frequency, defined as the frequency at which the gain decreases by 3 dB to −11.94 dB.

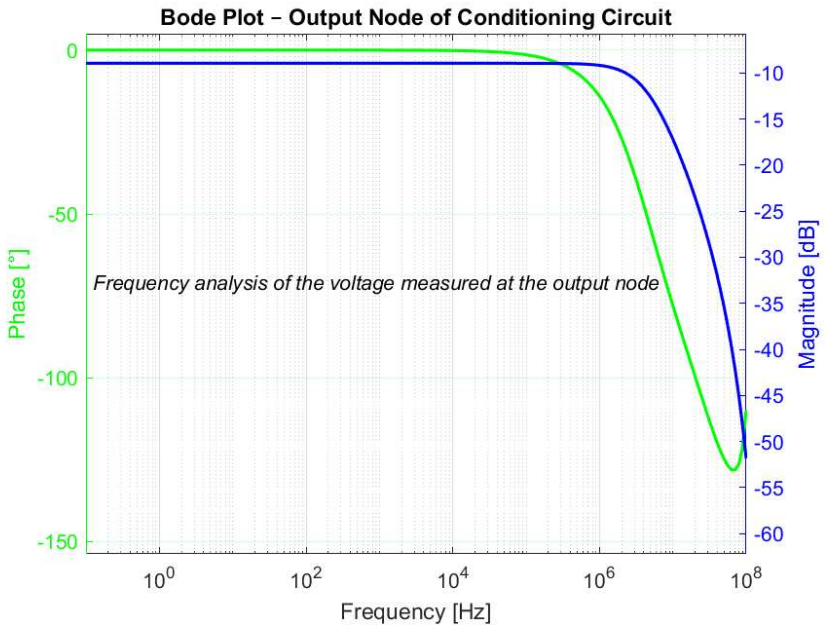


Figure 4.34: Magnitude response of Circuit 4 without parameter modifications

For clarity, the magnitude plot's vertical axis was limited to the interval between $-8.94\,\text{dB}$ and $-11.94\,\text{dB}$. The cutoff frequency was observed at approximately $4.667\,\text{MHz}$. Since the circuit behaves as a single-pole low-pass filter, this cutoff frequency directly corresponds to the system bandwidth; beyond it, the gain rolls off at $-20\,\text{dB/decade}$.

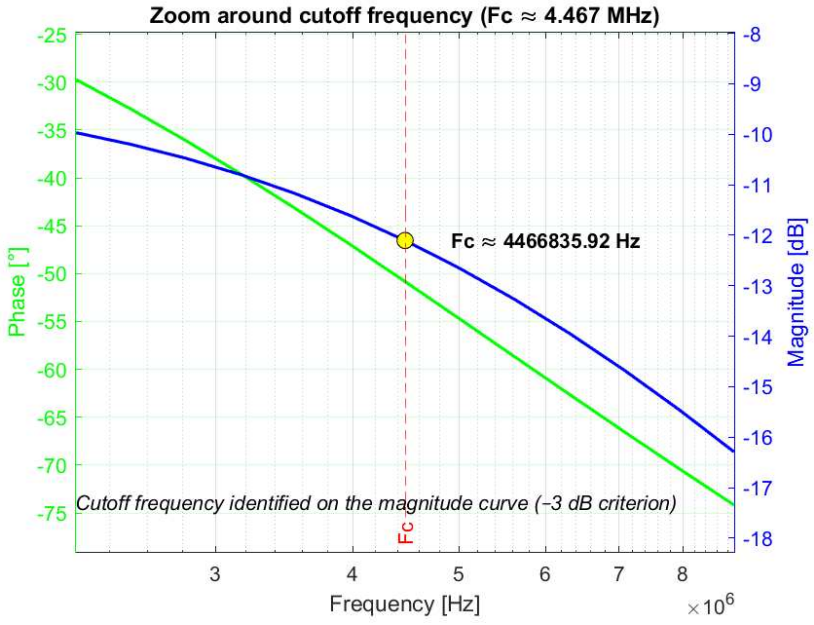


Figure 4.35: Zoomed view of the cutoff region showing the $-3\,\text{dB}$ drop in Circuit 4

A high bandwidth ensures a rapid dynamic response, which is essential for accurate capture and processing of high-frequency components, minimizes signal

distortion, and preserves measurement fidelity in RF and high-precision applications.

The amplitude of the square-wave source emulating the device-under-test (an N-MOSFET) was varied to assess its impact on the frequency response. The analysis confirmed that variations in the input amplitude do not shift the cutoff frequency. Furthermore, the observed bandwidth matches that obtained in Circuit 2, which employed the same conditioning network but a different current mirror for generating the bias current of the two clamping diodes.

4.4.6 Average Current Level in Circuit 4

Circuit 4 retains the current-mirror topology to bias the two clamping diodes $D3$ and $D4$. The measured diode currents exhibit periodic oscillations synchronous with the MOSFET switching, superimposed on large transient spikes at each on/off transition. Specifically: - i_{D3} swings between approximately 33mA (off-state) and 50 mA (on-state), excluding transient spikes. - i_{D4} varies between approximately 44mA and 50mA, likewise apart from switching spikes.

The average currents, computed over several switching cycles and neglecting the transient peaks, are about 41.5 mA for $D3$ and 47 mA for $D4$.

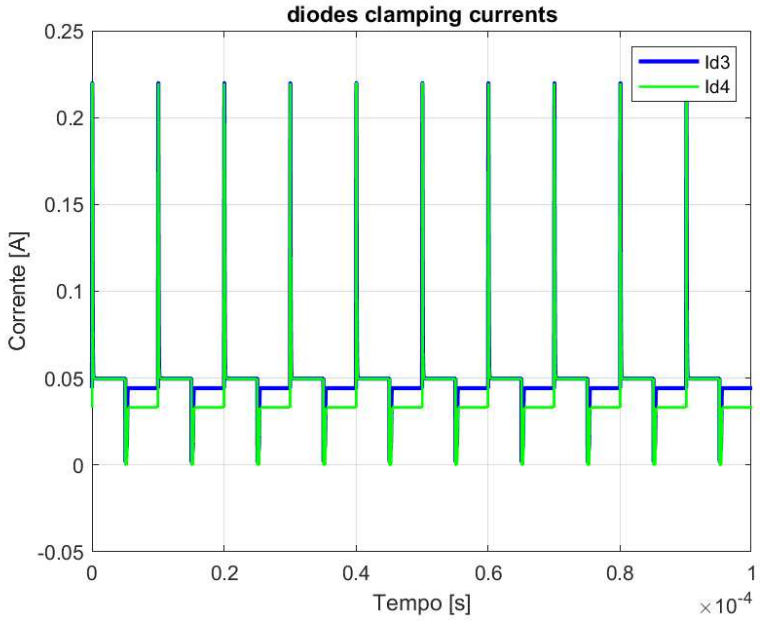


Figure 4.36: Comparison of current traces i_{D3} (blue) and i_{D4} (green) in Circuit 4, plotted on the same scale.

4.4.7 Voltage Behavior of the Diodes

With respect to the voltage drops across the diodes, an analysis was conducted to verify whether they reflect the observed current behavior.

In Circuit 4, the compensation diode (D4) maintains a nearly constant forward voltage of approximately 756 mV, except for substantial negative spikes down to -16 V in proximity to switching events. Conversely, the clamping diode (D3)

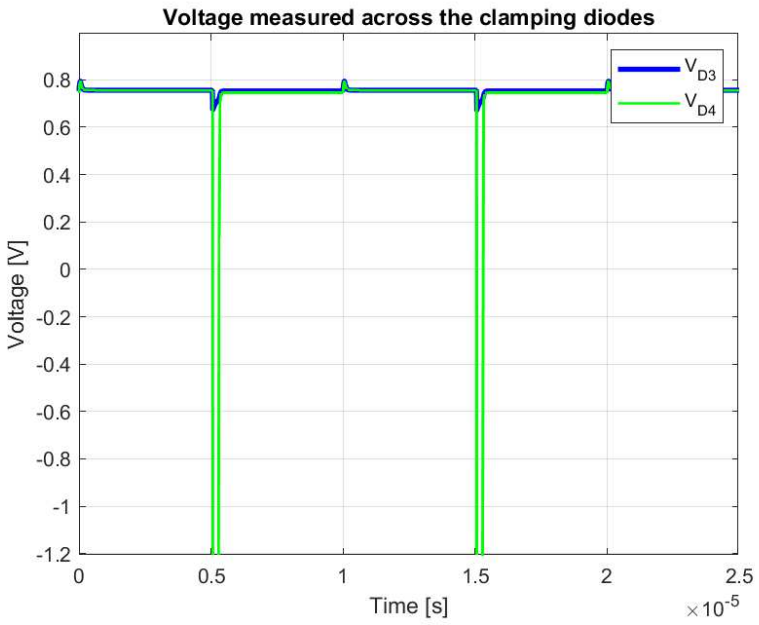


Figure 4.37: Comparison of diode currents v_{D3} (blue trace) and v_{D4} (green trace).

exhibits a forward voltage oscillating around an average of 754 mV, with a ripple of approximately 2 mV (4 mV peak-to-peak) and transient spikes of about 100 mV, mirroring the current behavior of the diode.

4.4.8 Analysis of Amplifier Saturation Behavior and Reference Tracking

As in the previous circuits, the saturation behavior of the operational-amplifier channel and the manner in which the output signal follows the input reference were examined. A brief note on input–output behavior:

Given the inverting (blue) and non-inverting (red) input signals applied to the operational amplifier (Figure 4.38), the resulting output voltage is somewhat noisy yet clearly demonstrates the correct operation of the conditioning circuit.

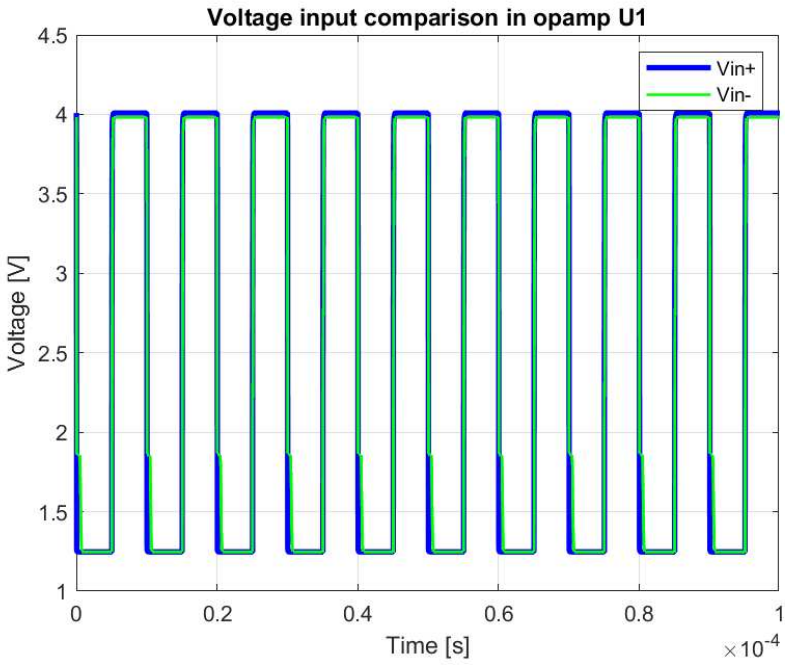


Figure 4.38: Inverting input signal (green) and non-inverting input signal (blue) applied to the operational amplifier.

The output is shown in the following graphics

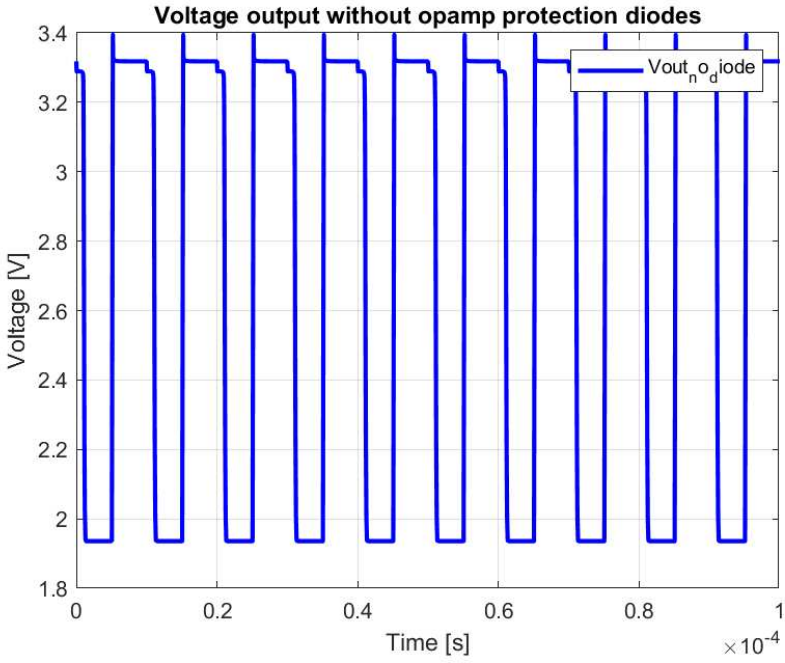


Figure 4.39: Clean output signal achieved with no protection diodes in the branch input.

4.4.9 Why is the signal cleaner in practice?

In Circuit 4, as in the previous circuits, diodes were placed in parallel with both the inverting and non-inverting inputs to emulate a real-world implementation.

The parallel arrangement of diodes at the inputs introduces a parasitic junction capacitance C_j. These capacitances, in conjunction with the op-amp's intrinsic input capacitance and the source resistance, form a low-pass filter at the input that lowers the cutoff frequency slightly. The net effect is the attenuation of high-frequency components, noise, and fast transients before they can be amplified, yielding a cleaner output signal free from transient distortions.

In a practical implementation this non-ideal diode behavior—stemming from parasitic capacitance—is generally undesirable, yet the diodes remain necessary to fulfill their protective role and prevent permanent damage to the op-amp. From a physical standpoint, however, this capacitive effect provides the secondary benefit of improving output signal cleanliness.

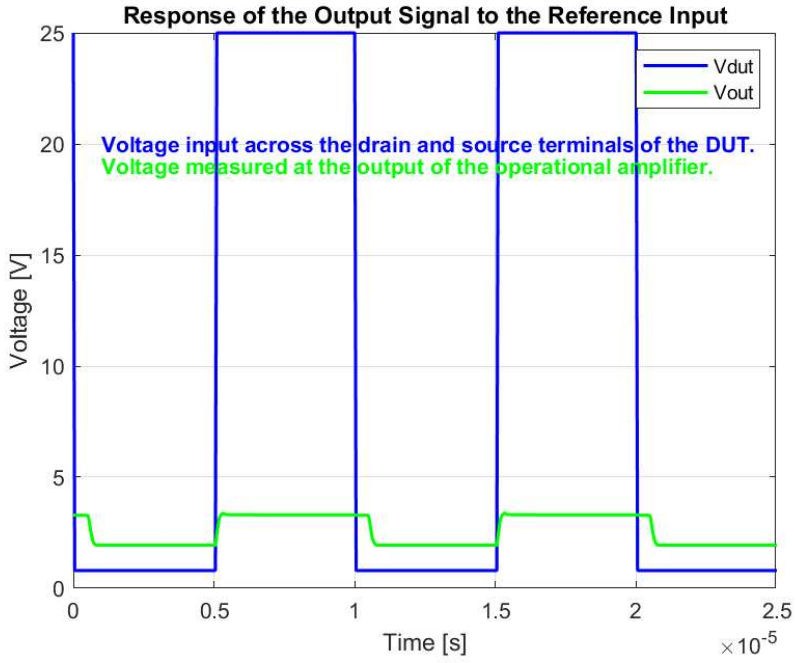


Figure 4.40: Comparison of the input signal (blue) and the output signal (red) of the operational amplifier in Circuit 4.

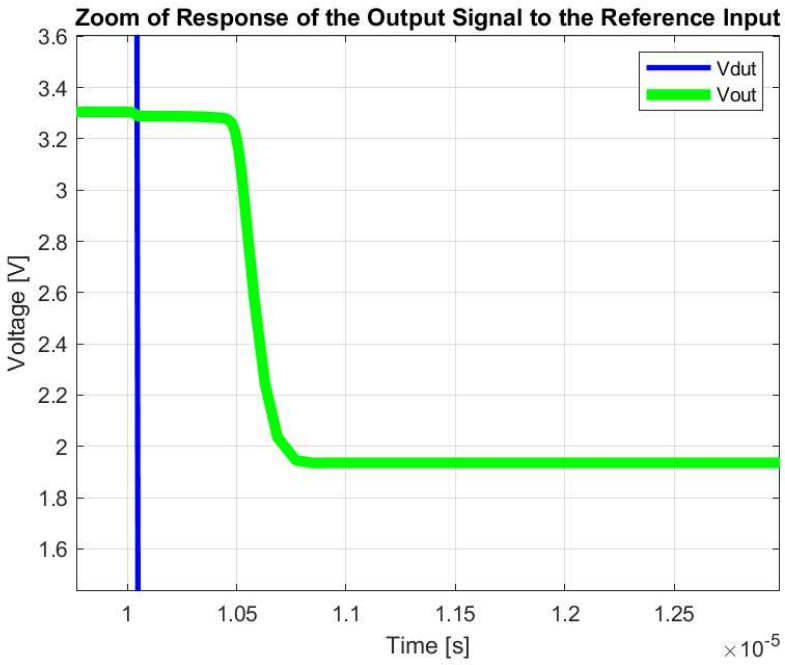


Figure 4.41: Zoom on the rising and falling edges of the input (blue) and output (red) signals.

4.5 Detailed Comparison of the Four Conditioning Circuits in a ideal approach

In the ideal-component simulations, all four circuits were assessed against two key metrics:

- **Group delay:** approximately 1 µs for each topology.
- **–3 dB cutoff frequency (f_c):**
  - Circuit 1: $f_c \approx 2.818\,\text{MHz}$
  - Circuits 2–4: $f_c \approx 4.467\,\text{MHz}$

4.5.1 Strengths of Circuit 1

Circuit 1, despite its narrower bandwidth, offers several advantages:

- **High intrinsic gain:** ideal for interfacing with ADCs having limited dynamic range.
- **Natural HF filtering:** early roll-off suppresses high-frequency noise and switching spikes without extra components.
- **Maximum stability and simplicity:** fewer high-dV/dt nodes reduce risk of parasitic oscillations.
- **Low complexity and power consumption:** suited for compact or battery-powered designs.
- **Relaxed offset calibration:** high gain attenuates the impact of small DC offsets and thermal drifts.

Adding real protection diodes at the amplifier inputs creates a supplementary low-pass effect, further cleaning the output at the cost of a slight reduction in f_c.

4.5.2 4.5.2 Roll-off Characteristics and Strengths of Circuits 2–4

Circuits 2, 3 and 4 employ a different RC network and operational amplifier than Circuit 1, shifting the –3dB point to $f_c \approx 4.467\,\text{MHz}$ while preserving a $\approx$1 µs group delay. Key benefits include:

- **Ultra-fast dynamic response:** sharper rise/fall edges for tracking rapid $\text{V}_{DS(\text{on})}$ transients.
- **Extended spectral fidelity:** minimal attenuation up to several MHz with a –20dB/decade roll-off beyond f_c.
- **Consistent latency:** same group delay as Circuit 1 but with 58% wider bandwidth.

Topology-specific strengths

- **Circuit 2:** balanced trade-off between HF performance and design simplicity, with low distortion on a compact layout.
- **Circuit 3:** dedicated current-source bias yields highly stable diode currents, minimal offset error and excellent linearity.
- **Circuit 4:** dual-op amp current mirror in split supplies ensures precise bias current, wide dynamic range and HV isolation, while retaining broad bandwidth.

HF filtering considerations The larger bandwidth increases sensitivity to high-frequency disturbances; in practice, a second-order or tailored low-pass stage is typically added to restore signal purity before ADC conversion.

Summary: Circuit 1 excels when high gain, minimal HF noise and maximal stability are paramount. Circuits 2–4, with their enhanced RC stages and high-speed amplifiers, deliver superior bandwidth and rapid transient tracking, making them the preferred choice for high-frequency, fast-sampling applications.

4.5.3 Summary

- **Circuit 1**
  - High intrinsic gain, ideal for interfacing with limited-dynamic-range ADCs.
  - Early roll-off ($f_c \approx 2.818\,\text{MHz}$) naturally filters HF noise and spikes.
  - Group delay $\approx 1\,\mu\text{s}$, offering maximum stability and implementation simplicity.
  - Low complexity and power consumption; relaxed offset calibration requirements.
- **Circuits 2–4**
  - RC network and operational amplifier optimized relative to Circuit 1.
  - Only the current mirror is modified; the RC stage and op-amp remain identical across these three circuits.
  - Uniform cutoff frequency $f_c \approx 4.467\,\text{MHz}$ ($\approx 58\%$ wider than Circuit 1).
  - Group delay $\approx 1\,\mu\text{s}$ and equivalent tracking of the reference input regardless of square-wave amplitude.
  - Ultra-fast dynamic response and spectral fidelity up to several MHz, ideal for high-frequency applications.
  - Increased sensitivity to HF disturbances, typically mitigated with dedicated low-pass filtering.

This comparison confirms that Circuit 1 is preferable when high gain, natural HF filtering, and maximum stability are paramount, whereas Circuits 2–4 are optimal for high-frequency systems demanding extended bandwidth and rapid acquisition.

Chapter 5

Simulations and Results – Real Components

5.1 Circuit 1: Ideal vs Real Component replacement

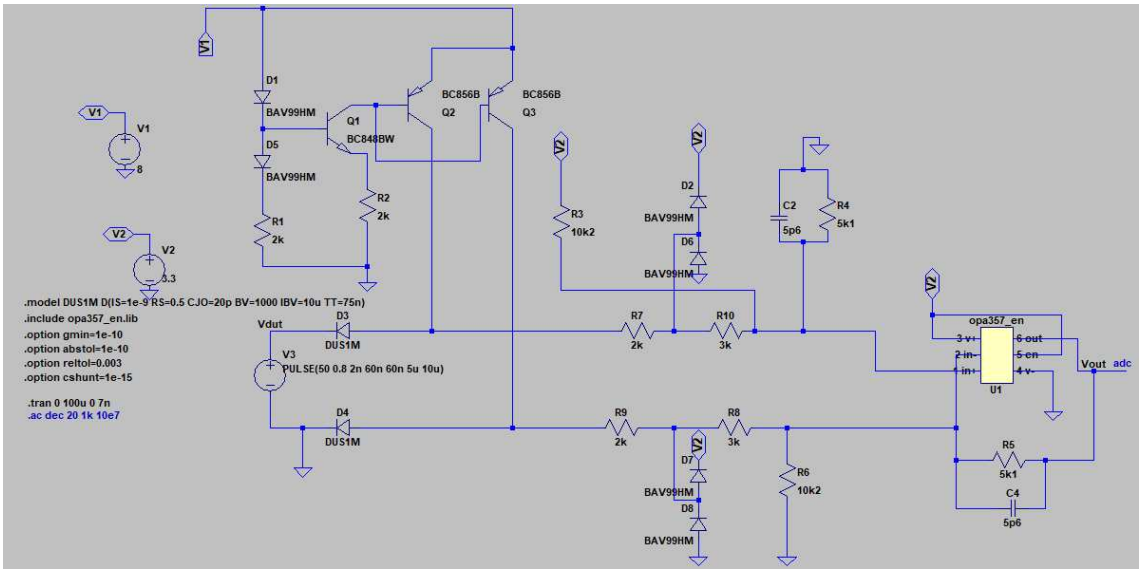
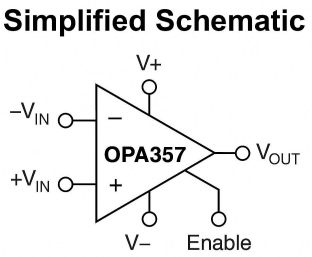


Figure 5.1: Real model of Gran Torino converter, Circuit 1 elaborated in LTspice. This schematic shows the full implementation using SiC MOSFETs with gate-driver stages, a logic-level interface, and the dedicated current–voltage measurement branch for $V_{\mathrm{DS(on)}}$ monitoring, and then, as explained in the previous chapters, it can see how the DUT is modeled as a square wave voltage generator

The following subchapter reports the configuration of circuit 1, visible in the image below, and discusses the substitution of ideal components with real ones.

(a) OPA357 like a phisical component



(b) pinout with Enable

Figure 5.2: non-inverting opamp OPA357_sot23

5.1.1 OPA357

The OPA357 is a high-speed, rail-to-rail CMOS operational amplifier manufactured by Texas Instruments. Housed in a compact SOT-23 package featuring a six-pin configuration, the device includes an integrated enable pin that facilitates controlled activation or power-down. This configuration is particularly advantageous in applications with limited board space and where dynamic circuit operation is required.

Key Electrical Parameters and Characteristics

The principal electrical parameters of the OPA357, as specified in the Texas Instruments datasheet, include:

- **Gain-Bandwidth Product (GBW):** approximately 250 MHz, ensuring high-frequency performance.
- **Rail-to-Rail Input and Output:** allows the device to achieve output swings within 100 mV of the supply rails.
- **Input Offset Voltage:** very low, which is critical for precision amplification.
- **Input Bias Current:** on the order of picoamperes, resulting in minimal loading on the preceding stages.
- **Slew Rate:** sufficiently high to support fast transient response.
- **Supply Voltage Range:** typically from 2.5 V to 5.5 V, accommodating both single- and dual-supply configurations.
- **Integrated Enable Pin:** permits enhanced power management without additional external circuitry.

Custom Modeling Process in LTspice

Due to the absence of a dedicated OPA357_SOT23 model in the standard LTspice library, a custom model was developed through the following process:

1. **Acquisition of the SPICE Model:** A SPICE model file (with a `.sub` extension) was obtained directly from the Texas Instruments website. This file provides a comprehensive set of device equations and empirical parameters that accurately describe the operation of the OPA357_SOT23 [36, 37].

2. **Custom Symbol Creation:** A custom symbol file (`.asy` file) was created to represent the six-pin SOT-23 package. The creation process involved a meticulous assignment of the individual pins—including the enable pin, non-inverting input, inverting input, output, and power-supply pins—based on the geometrical layout described in the datasheet.

3. **Integration into the Project:** Both the `.sub` file (containing the SPICE model) and the `.asy` file (defining the schematic symbol) were saved in the same directory as the Circuit 1 project. This ensures seamless integration and referencing within LTspice.

4. **Utilization and Verification:** The custom model was instantiated in the circuit schematic and thoroughly simulated. The simulation results confirmed that the model accurately portrays the real-world performance in accordance with the datasheet specifications.

In summary, the OPA357 operational amplifier offers high performance by combining a 250 MHz gain-bandwidth product, rail-to-rail input/output capability, and an integrated enable function within a compact six-pin SOT-23 package. The custom modeling approach—encompassing the acquisition of a SPICE model from Texas Instruments, the creation of a corresponding schematic symbol, and the integration of both files into the LTspice project—ensures that the simulated behavior closely mirrors the actual performance of the component.

5.1.2 BC856BDW1T1G

As regards the choice of the Mosfet, **BC856BDW1T1G** is a dual PNP bipolar transistor designed for low-power amplification and switching applications. It is housed in a **SOT-363/SC-88** package, making it particularly suitable for high-density surface-mount circuits [18].

Component Analysis: BC856BDW1T1G

The **BC856BDW1T1G** operates as a dual PNP transistor, facilitating efficient current control within circuit branches [19]. Its key electrical characteristics include:

- **Transistor Type**: PNP dual
- **Collector-Emitter Voltage (V_{CEO})**: -65V
- **Collector Current (I_C)**: -100mA (continuous), -200mA (peak)
- **Power Dissipation (P_D)**: 380mW
- **Transition Frequency (f_T)**: 100MHz

- **DC Current Gain (h_{FE})**: Minimum 220 @ 2mA, 5V

These characteristics make the **BC856BDW1T1G** highly effective in circuits requiring **precise current control and signal amplification**

Utility in Circuitry

In the examined circuit, two **BC856BDW1T1G** transistors are utilized to regulate **drain and source currents**, which are subsequently fed into a **non-inverting operational amplifier** [20]. The operational amplifier is responsible for signal amplification and conditioning, ensuring proper communication with a **microcontroller** [**?**].

Measurement Accuracy: Offset and Filtering

To ensure optimal signal integrity, two primary refinements are necessary:

1. **Reduction of operational amplifier offset** [21]
2. **Implementation of a low-pass filter** for noise attenuation [22]

Recommended Offset Values

Since **drain and source voltages** range between **0.1V and 800V**, selecting a low-offset operational amplifier is essential. The recommended values are:

- **Input Offset Voltage**: Below 50 μV, preferably under 10 μV for high precision
- **Offset Drift**: Below 1 μV/°C for thermal stability.
- **Open-loop Gain**: Above 120 dB to minimize offset impact.

Chopper-stabilized or digitally compensated operational amplifiers are ideal for this application.

Function of the Low-Pass Filter

The implementation of a low-pass filter following the operational amplifier enhances signal quality by:

- **Eliminating high-frequency noise**, improving signal integrity
- **Stabilizing output**, reducing undesirable fluctuations.
- **Protecting the microcontroller** from transient disturbances.
- **Improving dynamic response**, minimizing distortion and overshoot.

A **RC or active filter** may be used depending on precision requirements.

Characteristic	BC856BDW1T1G	BC856B
Type	PNP dual	PNP single
Package	SOT-363/SC-88	SOT-23
V_{CEO} (Max Voltage)	-65V	-65V
I_C (Max Current)	-100mA	-100mA
DC Gain (h_{FE})	220 min	200 min
Transition Frequency (f_T)	100MHz	80MHz
Applications	Amplification, switching	General use
LTspice Availability	No	Yes

Table 5.1: Comparison Between **BC856BDW1T1G** and **BC856B**

Comparative Analysis Between BC856BDW1T1G and BC856B

The **BC856B**, available in the LTspice component library, serves as a viable alternative to the **BC856BDW1T1G**, with notable distinctions [23].

This analysis highlights the **BC856BDW1T1G's characteristics**, its **role in current control**, and optimizations required for **precise signal conditioning**. Comparing it with the **BC856B** validates its suitability in LTspice simulations while discussing alternative solutions for enhanced circuit performance.

Selection of BC856B

The **BC856B** was selected for LTspice simulations due to its presence in the built-in component library, eliminating the need for manual SPICE model definitions. It closely resembles the **BC856BDW1T1G**, ensuring reliable circuit behavior in simulations.

Alternative Options

Other potential substitutes include:

- **BC857B**: Similar but with lower maximum voltage (-45V).
- **BC858B**: Optimized for amplification applications.
- **FMMTA56, KST56, MMBTA56**: Comparable PNP transistors.

5.1.3 BAV99 Diode

The **BAV99** is a high-speed switching diode integrating **two diodes in series** within a single **SOT-23** package. This configuration is particularly useful for applications requiring protection, rectification, and rapid switching [26].

Key Electrical Parameters of the BAV99

The **BAV99** exhibits the following principal electrical characteristics [27]:

- **Maximum Reverse Voltage (VR)**: 100V
- **Maximum Forward Current (IF)**: 215mA
- **Repetitive Peak Forward Current (IFRM)**: 450mA
- **Reverse Recovery Time (trr)**: 4ns
- **Junction Capacitance (Cd)**: 1.5pF
- **Package**: SOT-23

Comparison Between BAV99, BAV99HM, and BAW56

The following table provides a comparative analysis of the key parameters of the **BAV99**, the **BAV99HM** (selected for LTspice simulations), and the **BAW56**, a similar diode [28].

Parameter	BAV99	BAV99HM	BAW56
Maximum Reverse Voltage (VR)	100V	80V	85V
Maximum Forward Current (IF)	215mA	215mA	250mA
Repetitive Peak Forward Current (IFRM)	450mA	500mA	500mA
Reverse Recovery Time (trr)	4ns	4ns	6ns
Junction Capacitance (Cd)	1.5pF	1.5pF	2pF
Package	SOT-23	SOT-23	SOT-23

Table 5.2: Comparison Between **BAV99**, **BAV99HM**, and **BAW56**

Comparative Analysis and Selection of BAV99HM

The comparison among the three diodes highlights several key considerations [29]:

- The **BAV99** offers a higher maximum reverse voltage (100V), while the **BAV99HM** provides a slightly higher repetitive peak forward current capability (500mA).
- The **BAW56** has a larger junction capacitance (2pF), which may negatively affect performance in high-frequency applications.
- The reverse recovery time (**trr**) is identical for the **BAV99** and **BAV99HM** (4ns), whereas the **BAW56** is slightly slower (6ns).

Considering these factors, the **selection favors the **BAV99HM****, as it is readily available in the LTspice library and offers performance closely matching that of the **BAV99**, with enhanced repetitive peak forward current capabilities [30].

5.1.4 BC849C

This section presents a detailed technical analysis of the **BC849C** transistor. The **BC849C** is an NPN general-purpose transistor housed in a small SOT-23 package, optimized for low-power switching and amplification operations [31]. Its design and electrical performance render it suitable for applications where low voltage and moderate current capabilities are required.

Following the introduction, the internal structure and essential characteristics of the component are discussed. In particular, note that while the **BC849C** exhibits robust performance, a comparative evaluation with alternative devices is essential. For our simulations, we have selected the **BC848C** (which is already available in our simulation library) and we also consider the **BC847** as a comparable candidate.

Figure 5.3: **BC849C Transistor Component in SOT-23 Package**

Component Analysis: BC849C

The **BC849C** is designed for general-purpose applications and exhibits the following principal electrical parameters [31]:

- **Collector-Emitter Voltage (V_{CEO})**: Up to 30 V
- **Collector Current (I_C)**: 100 mA (maximum)
- **DC Current Gain (h_{FE})**: Typically ranging from 420 to 800
- **Transition Frequency (f_T)**: Approximately 100 MHz
- **Power Dissipation (P_{tot})**: Typically 250 mW
- **Package**: SOT-23

Such characteristics render the **BC849C** suitable for low-voltage, moderate-current applications in high-speed switching and signal amplification domains.

Parametric Comparison

For a thorough evaluation, the **BC849C** is compared against the **BC848C** and the **BC847**. The **BC848C** has been selected for detailed simulation work, while the **BC847** serves as an additional comparative benchmark.

Parameter	BC849C	BC848C	BC847
$\mathbf{V_{CEO}}$ **(Max Voltage)**	30 V	30 V	40 V
$\mathbf{I_C}$ **(Max Collector Current)**	100 mA	100 mA	150 mA
DC Current Gain ($\mathbf{h_{FE}}$)	420–800	400–750	350–600
Transition Frequency ($\mathbf{f_T}$)	∼100 MHz	∼90 MHz	∼80 MHz
Power Dissipation ($\mathbf{P_{tot}}$)	250 mW	250 mW	300 mW
Package	SOT-23	SOT-23	SOT-23

Table 5.3: Parametric Comparison Between **BC849C**, **BC848C**, and **BC847**

Comparative Analysis and Selection Rationale

A detailed analysis of the three transistors reveals several advantages and disadvantages:

- **Voltage and Current Ratings**: All three devices are designed for low-voltage applications. However, the **BC847** offers a higher maximum collector current (150 mA) but at the expense of a lower current gain.
- **Gain and Frequency Response**: The **BC849C** offers a very high DC gain (up to 800), rendering it ideal for applications requiring high amplification. The **BC848C** provides a similar performance profile with a slightly lower gain range but is already integrated within the simulation library, thus facilitating immediate deployment.
- **Power Dissipation**: The power dissipation ratings are comparable; however, the **BC848C** is preferred as it provides a good balance between performance and thermal behavior.

In summary, despite the robust characteristics of the **BC849C** and the higher current capability of the **BC847**, the **BC848C** has been selected for simulation purposes. Its electrical parameters and frequency response closely match the design requirements without necessitating extensive modifications to the simulation environment [32, 33].

Selecting the appropriate device simplifies simulation and improves accuracy. This analysis has underlined the **BC849C's characteristics, its role in signal amplification, and its limitations** when compared to alternative devices. Ultimately, a careful evaluation led to the selection of the **BC848C** for our simulations owing to its optimized performance and integration convenience within the LTspice library.

Note: Additional simulation and experimental validation are recommended to further refine component selection based on specific circuit demands.

5.1.5 US1M Diode Analysis and Modeling

The US1M diode is a 1.0 A surface-mount ultra-fast rectifier designed for high-speed switching and power management applications. This device is characterized by its high reverse voltage rating and extremely fast recovery properties—attributes that render it ideal for high-frequency rectification in modern power supplies and switching circuits [34].

Key electrical parameters of the US1M diode

- **Maximum Repetitive Reverse Voltage (VRRM):** 1000 V,
- **Maximum Forward Current (IF):** 1.0 A,
- **Forward Voltage Drop (VF):** approximately 1.7 V at 1.0 A,
- **Reverse Recovery Time (trr):** 75 ns,
- **Peak Surge Current:** 30 A,
- **Package:** SMA.

Due to the absence of a dedicated US1M component in the LTspice library, the diode has been modeled using the **.model** instruction. This customized approach ensures that the simulated component accurately reflects the diode's real-world behavior while allowing flexibility for design optimization.

To enhance the precision of the model, advanced parameter extraction techniques—specifically, the Qyello algorithm—were applied. Qyello performs an in-depth analysis by fitting the model parameters directly to the datasheet specifications, meticulously capturing the ultra-fast recovery dynamics and other key characteristics. This results in a highly accurate simulation model that mirrors the intrinsic semiconductor behavior of the US1M diode [35].

Parametric Comparison:

The table below presents a comparative analysis between the US1M diode and two analogous ultra-fast rectifiers, namely the US1A and US1B diodes, which share similar applications and operating characteristics.

In summary, the US1M diode exhibits superior reverse voltage capability and robust ultra-fast recovery, making it a prime candidate for demanding high-frequency rectification tasks. The use of the **.model** it was done by taking the key parameters from the .model instruction of a general fast recovery diode already present in the LTspice library, after which the parameters of interest were replaced by consulting the US1M datasheet.

Parameter	US1M	US1A	US1B
VRRM (Max Reverse Voltage)	1000 V	1000 V	1000 V
IF (Forward Current)	1.0 A	1.0 A	1.0 A
VF (Forward Voltage Drop)	1.7 V	1.0 V	1.3 V
trr (Recovery Time)	75 ns	50 ns	75 ns
Peak Surge Current	30 A	30 A	30 A
Package	SMA	SMA	SMA

Table 5.4: **Parametric Comparison Between US1M, US1A, and US1B Diodes**

5.2 Circuit 2: Ideal vs Real Component replacement

5.2.1 RUM001L02

The **RUM001L02** is optimized for low-power applications (100 mA, 6 Ω). Its low gate charge and reduced parasitic capacitances ensure fast switching and high energy efficiency.

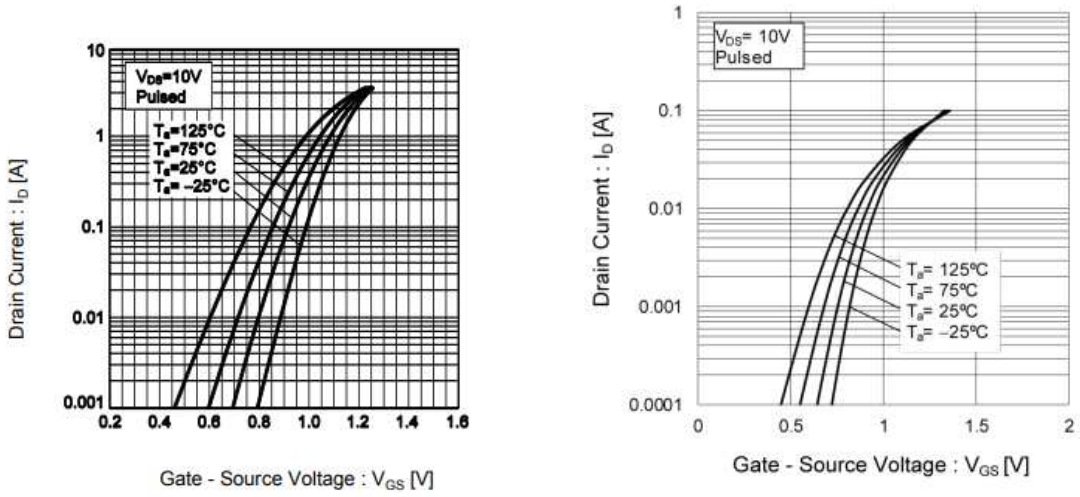


Figure 5.4: **treshold voltage comparison between the two mosfet**

Simulations (transfer, frequency, and transient) confirm a reliable reproduction of its behavior. Regarding the **real model of circuit 2**, the MOSFET has been modeled using the LTspice `.model` directive, referring to the MOSFET **RUL035N02**, which is already present in the LTspice component library, and modifying its physical conduction parameters.

Characteristic	RUM001L02	RUL035N02	Comparison
Nominal Current	100 mA	3.5 A	Variable, configurable
On-Resistance (Rds)	6 Ω	35 mΩ	Lower, optimized for power
Gate Charge	Low	9 nC	Standard
Parasitic Capacitance	Reduced	450 pF (Ciss)	Higher than RUM001L02

Table 5.5: Comparison between MOSFETs RUM001L02 and RUL035N02

5.2.2 OPA357

This subsection provides an in-depth analysis of high-performance operational amplifiers, with a particular focus on the OPA357. We present its specifications, compare it parametrically with analogous devices (OPA354AIDBWR, OPA454, OPA350), and justify the choice of the OPA357 for this project. Emphasis is placed on precision, DC stability, frequency response, noise performance and thermal behavior—critical factors for the signal-conditioning stage of this thesis. Moreover, a validated SPICE model for the OPA357 already exists in our framework, ensuring methodological consistency and simplifying both simulation and experimental verification.

Technical Analysis and Parametric Comparison

Overview of the OPA354AIDBWR The OPA354AIDBWR is optimized for high-speed, moderate-voltage applications. Its key specifications are:

- **Supply voltage range:** $V_{\text{supply}} = 4.5\,\text{V}$ to $36\,\text{V}$.
- **Gain–Bandwidth Product (GBW):** $\approx 40\,\text{MHz}$.
- **Slew rate (SR):** $\approx 50\,\text{V}\,\mu\text{s}^{-1}$.
- **Offset voltage (V_{OS}):** $\approx 2\,\text{mV}$.
- **Peak output current:** $\approx 35\,\text{mA}$.
- **Distortion and linearity:** very low THD, high linearity.
- **Package:** AIDBWR SMD with optimized thermal dissipation.

Comparative Analysis with Other Amplifiers Table 5.6 summarizes the main parameters of four devices:

Rationale for Selecting the OPA357

Based on the comparison above, the OPA357 was chosen for this project because:

- **Superior precision and DC stability:** Typical offset $\approx 1\,\text{mV}$ minimizes systematic errors in high-gain configurations.
- **Balanced performance:** GBW $\approx 18\,\text{MHz}$ and SR $\approx 14\,\text{V}\,\mu\text{s}^{-1}$ suffice for precision conditioning without unnecessary high-speed overhead.

Parameter	OPA354AIDBWR	OPA454	OPA350	OPA357
Supply voltage (V)	4.5–36	15–180	2.7–36	4.5–36
GBW (MHz)	40	3	55	18
Slew rate ($\mathrm{V\,\mu s^{-1}}$)	50	10	220	14
Offset voltage (mV)	2	2	0.5	1
Peak output current (mA)	35	35	60	35

Table 5.6: Parametric comparison of OPA354AIDBWR, OPA454, OPA350 and OPA357.

- **Pre-existing SPICE model:** Ensures consistency and reduces calibration effort.
- **Application-oriented trade-off:** Prioritizes DC accuracy over extreme dynamic speed, aligning with thesis goals.

Conclusions

In summary:

- The OPA357 delivers an optimal compromise between DC accuracy and dynamic performance.
- Its low offset and robust thermal management meet the stringent requirements of the signal-conditioning stage.
- Reuse of an existing validated SPICE model streamlines simulation and experimental validation.

5.2.3 VS-E7MH0112

The S1N-13-F is a silicon rectifier diode characterized as a standard recovery device. It is designed for high-voltage applications where robust reverse-voltage blocking and transient handling are required. However, being a standard-recovery diode, its reverse recovery time is comparatively longer. In contrast, the VS-E7MH0112 is engineered with fast-recovery technology. Although both devices typically handle similar voltage ratings (around 1,200 V) and average forward currents (approximately 1 A), the VS-E7MH0112 offers a significantly shorter reverse recovery time, making it better suited for high-frequency applications.

Electrical Parameter Analysis

Repetitive Peak Reverse Voltage V_{RRM}

- **S1N-13-F:** rated for $V_{\mathrm{RRM}} \approx 1{,}200\,\mathrm{V}$, ensuring wide safety margins under repetitive spikes.
- **VS-E7MH0112:** similarly rated at 1,200 V, providing equivalent reverse-blocking capability.

Average Rectified Forward Current $I_{F(\mathrm{av})}$

- **S1N-13-F:** $I_{F(\mathrm{av})} \approx 1\,\mathrm{A}$, suitable for moderate-power forward conduction.
- **VS-E7MH0112:** also $I_{F(\mathrm{av})} \approx 1\,\mathrm{A}$, matching conduction capability.

Forward Voltage Drop V_F

$$P_{\mathrm{loss}} = I_F \times V_F$$

- **S1N-13-F:** $V_F \approx 0.94\,\mathrm{V}$ at $I_F = 1\,\mathrm{A}$.
- **VS-E7MH0112:** $V_F \approx 0.9\,\mathrm{V}$–$0.94\,\mathrm{V}$, indicating similar conduction losses.

Reverse Recovery Time t_{rr}

- **S1N-13-F:** standard recovery, $t_{rr} \approx 100$–$200\,\mathrm{ns}$.
- **VS-E7MH0112:** fast recovery, $t_{rr} \approx 30$–$50\,\mathrm{ns}$, minimizing switching losses.

Surge Current I_{FSM}

- **S1N-13-F:** $I_{\mathrm{FSM}} \approx 30\,\mathrm{A}$ (8.3 ms pulse).
- **VS-E7MH0112:** $I_{\mathrm{FSM}} \approx 30\,\mathrm{A}$ (8.3 ms pulse).

Junction Capacitance C_j

$$X_C = \frac{1}{2\pi f C_j}$$

- **S1N-13-F:** $C_j \approx 6\,\mathrm{pF}$ at 4 V, 1 MHz.
- **VS-E7MH0112:** slightly higher C_j, offset by faster recovery for high-frequency performance.

Comparative Summary

Parameter	S1N-13-F	VS-E7MH0112
V_{RRM} (V)	1200	1200
$I_{F(\mathrm{av})}$ (A)	1	1
V_F @ 1 A (V)	0.94	0.9–0.94
t_{rr} (ns)	100–200	30–50
I_{FSM} (A)	30	30
C_j (pF)	6	slightly higher

Table 5.7: Parametric comparison of S1N-13-F and VS-E7MH0112 diodes.

Conclusion and Selection Rationale

The VS-E7MH0112 has been selected due to:

- **Fast recovery** ($t_{rr} \approx 30$–$50\,\text{ns}$), ideal for high-frequency switching.
- **Equivalent voltage and current ratings** (1,200 V, 1 A).
- **Availability in LTspice libraries**, simplifying simulation and ensuring model consistency.

Thus, the VS-E7MH0112 provides the best combination of fast switching performance and comparable conduction/blocking capabilities.

5.2.4 BC856B

The BC860BW is a high-voltage PNP bipolar junction transistor (BJT) typically used in amplifier stages and switching circuits. It is engineered for reliability in applications demanding high collector–emitter voltages and moderate currents. However, when circuit performance requires increased speed and higher operating frequencies, devices with superior high-frequency characteristics become desirable. The BC856B, a related PNP transistor, shares similar high-voltage handling but features a significantly higher transition frequency. In this subsection, we analyze the BC860BW's key parameters, compare it with the BC856B, and justify the selection of the BC856B for high-speed applications.

Detailed Analysis of BC860BW Parameters

Collector–Emitter Voltage V_{CEO}

$$V_{\text{CEO}} = \max V_{CE} \quad \text{(open-base)}$$

Datasheet: $V_{\text{CEO}} \approx 300\,\text{V}$. High V_{CEO} provides a large safety margin against voltage spikes in power amplifiers and switching converters.

Collector Current and Current Gain $I_{C(\text{max})}$, h_{FE}

- $I_{C(\text{max})} \approx 50\,\text{mA}$
- $h_{FE} = \frac{I_C}{I_B} \approx 30$–$100$

A broad gain range benefits low-power amplification, while current rating ensures safe operation without saturation.

Transition Frequency f_T

$$f_T = \text{frequency where } h_{FE} = 1$$

Datasheet: $f_T \approx 50\,\text{MHz}$. Adequate for many linear and power applications, but limited for RF or very high-speed switching.

Noise, Stability and Junction Capacitance

- Low noise figure, good thermal stability over -55 to $+150\,^{\circ}\mathrm{C}$.
- Junction capacitance $C_j \approx 6\,\mathrm{pF}$ (4 V, 1 MHz), minimizing parasitic effects in moderate-frequency designs.

Comparison with BC856B

Table 5.8 contrasts BC860BW and BC856B:

Parameter	**BC860BW**	**BC856B**
V_{CEO} (V)	300	300
$I_{C(\max)}$ (mA)	50	40
h_{FE} (DC gain)	30–100	30–80
f_T (MHz)	50	80
Noise/Stability	Low noise, wide $\mathrm{T_{amb}}$	Similar, improved HF linearity
C_j (pF)	6	≈ 6

Table 5.8: Comparison of BC860BW and BC856B PNP transistors.

The BC856B's $f_T \approx 80\,\mathrm{MHz}$ offers faster response and lower phase distortion, making it preferable for high-frequency and RF circuits.

Selection Rationale

Although both transistors share a V_{CEO} of 300 V and similar capacitance, the BC856B's higher transition frequency (80 MHz vs. 50 MHz) and availability in LTspice libraries make it the optimal choice for designs requiring rapid switching and minimal signal distortion. Its use ensures methodological consistency and simplifies simulation and experimental validation in high-speed applications.

5.3 Circuit 3: Ideal vs Real Component replacement

5.4 BC558B

In the design of our modified current mirror circuit (referred to as Circuit 3), we began with the previously analyzed Circuit 2 and reconfigured its current mirror. In this improved design, an operational amplifier in combination with a bipolar transistor has been employed to achieve a superior current waveform relative to the earlier configuration.

5.4.1 Characteristics of the BC558B

The **BC558B** is a PNP bipolar junction transistor (BJT) in the BC55x family manufactured with silicon planar technology. It is principally designed for low-power switching and small-signal amplification applications. Its salient features are as follows:

- **Transistor Type:** PNP BJT (BC55x family) fabricated using silicon planar processes.
- **Collector–Emitter Breakdown Voltage (V_{CEO}):** Approximately $-30\,\mathrm{V}$, which provides adequate protection against supply overvoltage in many switching circuits.
- **Emitter–Base Breakdown Voltage (V_{EBO}):** Around $-5\,\mathrm{V}$, ensuring safe operation under reverse bias conditions.
- **Collector Current (I_C):** Rated for continuous currents up to approximately $100\,\mathrm{mA}$, suitable for low-power circuitry.
- **DC Current Gain (h_{FE}):** Typically ranges from 200 to 450, thereby offering moderate amplification that is well balanced for many applications.
- **Power Dissipation (P_D):** Approximately $625\,\mathrm{mW}$ ensures the device operates reliably within moderate power levels.
- **Transition Frequency (f_T):** Around $100\,\mathrm{MHz}$, making it appropriate for circuits where extremely high frequency is not required.
- **Package:** Commonly available in a TO-92 package, which facilitates rapid prototyping and economical design.

The BC558B's moderate gain and reliable performance in low-power applications make it a strong candidate in circuits where precise current control is critical. However, its relatively low breakdown voltage (approximately $-30\,\mathrm{V}$) can impose restrictions in high-voltage designs.

5.4.2 Comparative Analysis

Table 5.9 presents a comparative assessment of the BC558B, the BC557C, and the 2N3906. The comparison is based on key performance specifications relevant to current mirror applications.

Table 5.9: Comparative Analysis of Selected PNP Transistors

Parameter	**BC558B**	**BC557C**	**2N3906**
Type	PNP (BC55x family)	PNP (BC55x family)	PNP
V_{CEO} (Collector–Emitter Breakdown)	$-30\,\mathrm{V}$	$-45\,\mathrm{V}$	$-40\,\mathrm{V}$
V_{EBO} (Emitter–Base Breakdown)	$-5\,\mathrm{V}$	$-5\,\mathrm{V}$	$-6\,\mathrm{V}$ (typical)
I_C (Collector Current)	$\sim 100\,\mathrm{mA}$	$\sim 100\,\mathrm{mA}$	$\sim 200\,\mathrm{mA}$
h_{FE} (DC Current Gain)	200–450 (moderate)	420–800 (high)	100–300 (lower)
P_D (Power Dissipation)	$\sim 625\,\mathrm{mW}$	$\sim 625\,\mathrm{mW}$	$\sim 625\,\mathrm{mW}$
f_T (Transition Frequency)	$\sim 100\,\mathrm{MHz}$	$\sim 100\,\mathrm{MHz}$	$\sim 250\,\mathrm{MHz}$
Package	TO-92	TO-92	TO-92

5.4.3 Advantages and Disadvantages

BC558B:

- **Advantages:** It demonstrates reliable performance in low-power amplification and switching circuits. Its moderate current gain and satisfactory thermal stability render it suitable for many standard applications.

- **Disadvantages:** Its relatively low collector–emitter breakdown voltage (V_{CEO}) of approximately $-30\,\mathrm{V}$ may restrict its usage in circuits designed for higher voltage operations. Furthermore, the moderate gain might be insufficient in scenarios where higher amplification is required.

BC557C:

- **Advantages:** The BC557C provides a significantly higher DC current gain (approximately 420–800), making it advantageous for applications requiring substantial signal amplification. It also features a higher V_{CEO} (approximately $-45\,\mathrm{V}$), affording a greater margin in high-voltage scenarios. Moreover, its ready availability in LTSpice libraries greatly eases the simulation and design verification process.

- **Disadvantages:** In some operating conditions, its dynamic response may exhibit slight nonlinearity when compared to lower-gain alternatives; however, the benefits gained in amplification typically outweigh this potential drawback.

2N3906:

- **Advantages:** With a transition frequency of about $250\,\mathrm{MHz}$, the 2N3906 is well suited for high-frequency applications. Additionally, it can handle collector currents up to approximately $200\,\mathrm{mA}$, offering greater current handling capability.

- **Disadvantages:** Its lower current gain (ranging from 100 to 300) makes it less suitable for applications where high amplification is a strict requirement.

5.4.4 Final Assessment and Selection of the BC557C

Based on the detailed analysis and the comparative evaluation provided in Table 5.9, the **BC557C** emerges as the optimal transistor for our current mirror circuit requirements. The key factors influencing this decision include:

- The BC557C's superior DC current gain makes it highly effective for applications where robust amplification is imperative.
- Its higher collector–emitter breakdown voltage ($-45\,\mathrm{V}$) offers enhanced operational margin, thereby accommodating higher voltage swings and ensuring circuit resilience.
- The transistor's widespread presence in LTSpice libraries facilitates efficient simulation, design validation, and ultimately a more straightforward transition from design to prototype.

In conclusion, although both the BC558B and the 2N3906 have merits in specific contexts, the BC557C is deemed the most appropriate choice for our modified current mirror circuit. Its enhanced amplification capabilities, better voltage handling, and practical ease of simulation make it the ideal candidate to meet the rigorous demands of our application.

5.5 OPA284EP

The **OPA284EP** is a precision, rail-to-rail operational amplifier engineered for applications that demand high accuracy and low noise in moderate-frequency regimes. It is designed to operate over a wide supply voltage range ($5\,\mathrm{V}$ to $36\,\mathrm{V}$) and exhibits the following key parameters:

- **Bandwidth:** Approximately $4.25\,\mathrm{MHz}$, which is sufficient for many precision signal-conditioning circuits.
- **Slew Rate:** On the order of $4\,\mathrm{V}/\mu\mathrm{s}$, ensuring acceptable performance for moderate-speed applications.
- **Input Offset Voltage:** Typically around $65\mu\mathrm{V}$, a critical specification for high-accuracy measurements.
- **Noise Density:** Approximately $3.9\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, contributing to its low-noise operation.
- **Rail-to-Rail Operation:** Both the input and output stages are rail-to-rail, maximizing the available dynamic range in single-supply configurations.
- **Unity-Gain Stability:** The device is stable at unity gain, which is advantageous for buffer or follower configurations.

These features render the OPA284EP particularly attractive in applications where precision and low distortion are paramount, even though its dynamic performance (in terms of slew rate and frequency response) is not optimized for ultrahigh-speed conditions.

5.5.1 Comparison with OPA2846 and OPA2846IDR

For a better understanding, Table 5.10 provides a comparative overview of the OPA284EP alongside the OPA2846 and OPA2846IDR. While the OPA284EP emphasizes low offset and low noise characteristics, the OPA2846 and OPA2846IDR represent devices from the same family with enhanced speed and bandwidth attributes.

Table 5.10: Comparison of Key Parameters for OPA284EP, OPA2846, and OPA2846IDR

Parameter	**OPA284EP**	**OPA2846**	**OPA2846IDR**
Supply Voltage Range	5 V – 36 V	5 V – 36 V	5 V – 36 V
Bandwidth (GBW)	∼4.25 MHz	∼1.65 GHz	∼1.65 GHz
Slew Rate	∼4 V/μs	∼600 V/μs	∼600 V/μs
Input Offset Voltage	∼65μV	∼150μV	∼150μV
Noise Density	∼3.9 nV/$\sqrt{\text{Hz}}$	∼4 nV/$\sqrt{\text{Hz}}$	∼4 nV/$\sqrt{\text{Hz}}$
Rail-to-Rail I/O	Yes	Yes	Yes
Unity-Gain Stability	Yes	Yes	Yes
Packaging	Single (e.g., TO-92)	Dual (SOIC 8-pin)	Dual (SOIC 8-pin, industrial variant)

5.5.2 Advantages and Disadvantages of the Devices

OPA284EP:

- **Advantages:**
  - Exceptionally low input offset voltage and low noise density, making it highly suitable for high-precision applications.
  - Rail-to-rail operation maximizes the dynamic range, which is beneficial for single-supply designs.
  - Unity-gain stability simplifies its use as a buffer or in voltage-following circuits.
- **Disadvantages:**
  - The moderate bandwidth and slew rate limit its performance in scenarios requiring rapid transient response.
  - Not optimized for high-speed signal processing, which may be a constraint in applications demanding very high dynamic response.

OPA2846 and OPA2846IDR:

- **Advantages:**
  - Very high gain-bandwidth product (approximately 1.65 GHz) and high slew rate (around 600 V/μs), which make them suitable for high-frequency and high-speed applications.
  - Dual channel versions facilitate multi-channel designs in a single package.

- **Disadvantages:**
  - Higher input offset voltage (approximately 150μV) and marginally increased noise levels relative to the OPA284EP may affect precision in low-level signal conditions.
  - Their performance enhancements in speed come at the cost of increased complexity in design and potentially higher power consumption.

Based on the application requirements, where high precision, low offset, and low noise are prioritized over ultrahigh-speed performance, the **OPA284EP** was selected. To accurately capture its behavior in circuit simulations, the OPA284EP has been modeled by creating a dedicated subcircuit file (`OPA284EP.sub`). This file contains a detailed `.model` representing the OPA284EP parameters and behavior. The model is then integrated into the circuit schematic by using the `.include` directive, ensuring that all simulations reflect the intended performance of the device.

Integration Example: In your LTspice schematic, you can include the model as follows:

```
.include OPA284EP.sub
```

This approach allows for a precise simulation of the OPA284EP within the design, supporting detailed analysis of both DC and AC performance as well as transient response within the application context.

5.6 Diodo Zener:Function and Role in Reverse Conduction Control

The Zener diode is a specialized semiconductor device primarily employed for voltage regulation and circuit protection. Unlike standard diodes, which are designed to block reverse current until a destructive breakdown is reached, a Zener diode is engineered to operate reliably in the reverse-breakdown region. This is achieved through heavy doping of the p–n junction, which allows the diode to maintain a nearly constant voltage—known as the Zener voltage (V_Z)—across its terminals even when a significant reverse current flows.

In many applications the principal function of the Zener diode is not to provide high power conduction but rather to serve as a control element. It accomplishes this by initiating conduction when the reverse voltage exceeds V_Z; in doing so, it "clamps" the voltage at a predetermined level. This behavior is essential in several contexts:

- **Voltage Regulation:** Maintaining a stable voltage reference despite variations in supply voltage or load conditions.
- **Transient Protection:** Limiting voltage spikes that could otherwise damage sensitive circuit components.
- **Signal Conditioning:** Defining a precise voltage threshold for triggering or biasing purposes.

In circuit designs, the Zener diode is often implemented in a manner that focuses solely on controlling reverse conduction rather than delivering substantial power. For this reason, an idealized Zener diode model—characterized by its specified breakdown voltage, low dynamic resistance, and minimal leakage current—is typically sufficient to replicate its essential function in simulations. The device acts primarily as a voltage reference and clamp, ensuring that any reverse-biased conduction is controlled and does not lead to potentially damaging conditions.

It is therefore unnecessary to substitute the simulated or idealized Zener diode with a "real" high-power component when its role is limited to reverse conduction control. The key requirement is to guarantee that the voltage is clamped at V_Z under reverse-bias conditions, providing a straightforward and effective means of protecting sensitive circuitry. This approach simplifies both the design and the simulation process, as the idealized model captures all the necessary characteristics without introducing the additional complexities associated with a full-power component.

5.7 Circuit 4: Ideal vs Real Component Replacement

5.7.1 Component Replacement

In Circuit 4 we replaced only the current mirror with real-world components, while leaving the rest of the topology identical to the other two real model. For the INA105 instrumentation amplifier we downloaded the official TI ".sub" file and used LTspice's `auto-generated symbol` feature to import the `.subckt` definition directly into our schematic. The OPA602 model was already available in the LTspice library and required no additional import steps.

INA105

The INA105 model was created by placing a generic `.asy` symbol and pointing its `prefix` to the TI-supplied `.sub` file. LTspice then automatically linked the pin mapping and netlist entries, enabling a drop-in component that exactly matches the manufacturer's SPICE definition.

Table 5.11: Key parameters of the INA105 instrumentation amplifier

Parameter	Value
Supply voltage range	$\pm 2.5\,\mathrm{V}$ to $\pm 12\,\mathrm{V}$
Input offset voltage (typ)	$25\,\mu\mathrm{V}$
Gain–bandwidth product	$2.5\,\mathrm{MHz}$
Input noise (0.1–10 Hz)	$0.5\,\mu\mathrm{V_{RMS}}$
Common-mode rejection ratio (CMRR)	$120\,\mathrm{dB}$
Power-supply rejection ratio (PSRR)	$135\,\mathrm{dB}$

OPA602

The OPA602 was instantiated directly from the LTspice built-in library. No external files were needed, since the vendor-provided .subckt and symbol were preloaded in the standard distribution.

Table 5.12: Key parameters of the OPA602 op amp

Parameter	Value
Supply voltage range	$\pm 2.5\,\mathrm{V}$ to $\pm 16\,\mathrm{V}$
Input offset voltage (typ)	$100\,\mu\mathrm{V}$
Gain–bandwidth product	$50\,\mathrm{MHz}$
Slew rate	$145\,\mathrm{V}/\mu\mathrm{s}$
Input noise density	$2.1\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$
Input bias current (typ)	$0.5\,\mathrm{pA}$

siunitx

5.8 Transient Analysis: Comparison Between Circuit Solutions

In the analysis of the rising and falling edges at each circuit's output, reference was made to the group delay or, where more pertinent, the time interval between the maximum and minimum output values.

- **Circuit 1**
  - Group delay of $0.10\,\mu\mathrm{s}$, yielding very fast and clean rising and falling edges.
  - Maximum gain of $-0.16\,\mathrm{dB}$.
- **Circuit 2**
  - Transition from the saturated level ($3.3\,\mathrm{V}$) to the steady-state value in $0.04\,\mu\mathrm{s}$.
  - This performance reflects an effective balance between response speed and signal fidelity, achieved through a configuration optimized for both gain and stability.
- **Circuit 3**
  - Transition time between extreme output values of $0.03\,\mu\mathrm{s}$ ($30\,\mathrm{ns}$), confirming the superior dynamic reactivity of this topology.
- **Circuit 4**

– Despite a slightly higher gain compared to Circuits 2 and 3 ($-8.73\,\mathrm{dB}$), convergence issues and simulation uncertainties lead to longer delays and reduced overall efficiency.

These results highlight that, for equal bandwidth, both the gain value and the quality of signal conditioning decisively influence how quickly and accurately each circuit tracks rapid variations in $V_{ds(on)}$. In any practical PCB implementation, careful control of parasitic effects from solder joints and trace layout will be essential to preserve edge integrity.

Chapter 6

Circuit 's frequency analysis

The simulations performed in LTSpice are aimed at obtaining Bode diagrams, which will be detailed in the following sections. These diagrams illustrate the frequency response of the circuit across all analyzed configurations. The investigation includes the definition of simulation parameters, the identification of the cut-off frequency, and a comparative discussion on the advantages and disadvantages associated with low and high bandwidth systems.

6.1 Explanation of the Bode Diagram

The Bode diagram is a fundamental graphical tool used to analyze the frequency response of electrical and electronic systems. It consists of two plots:

- **Magnitude plot:** Displays the gain of the system, expressed in decibels (dB), as a function of frequency on a logarithmic scale.
- **Phase plot:** Shows the phase shift between input and output signals, expressed in degrees, also as a function of logarithmic frequency.

These plots provide a clear visualization of system behavior across different frequency ranges, allowing engineers to identify the cut-off frequency, evaluate filter performance, and assess system stability. Specifically, the Bode diagram is instrumental in:

- Determining the *cut-off frequency*, defined as the point where the gain drops by 3 dB from its maximum value.
- Assessing the *stability* of control systems by analyzing gain and phase margins.
- Designing and optimizing *active and passive filters*, tailoring the frequency response to meet application-specific requirements.
- Understanding the influence of *reactive components* (capacitors and inductors) on circuit behavior.

In simulation environments such as LTSpice, the Bode diagram is generated through AC analysis by applying a sinusoidal input across a wide frequency range. This enables precise characterization of the system's frequency-dependent behavior and supports both design validation and performance tuning [47].

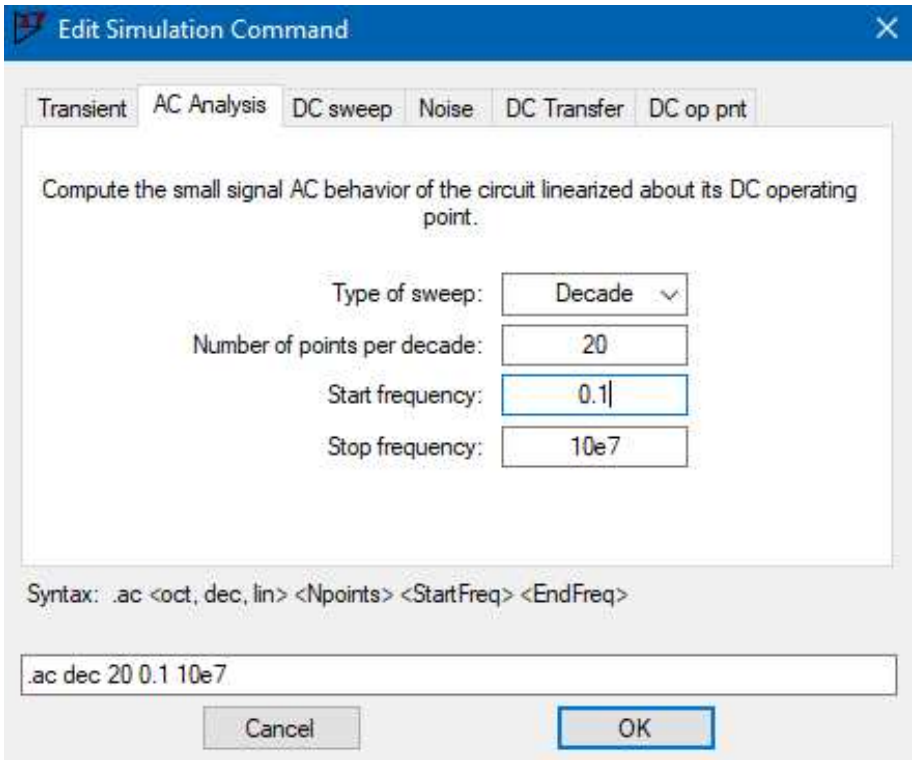


Figure 6.1: Frequency simulation parameters configured in LTSpice. The image shows the AC sweep settings from 0.1 Hz to 100 MHz using 20 points per decade.

6.2 Bandwidth Considerations: Advantages and Disadvantages

The selection of system bandwidth is a critical design decision that must be evaluated based on specific application requirements. Bandwidth affects signal transmission capability, dynamic response, noise susceptibility, and design complexity.

6.2.1 Narrow Bandwidth

Advantages:

- *High selectivity:* Precisely isolates the frequency range of interest, enhancing filtering effectiveness.
- *Reduced noise susceptibility:* Limits the admission of unwanted signals and external disturbances.
- *Improved system stability:* Systems with narrow bandwidth tend to exhibit more stable and predictable responses.

- *Simplified design:* Analog circuits with limited bandwidth are generally easier to design and less prone to layout issues.

Disadvantages:

- *Limited information transmission:* May exclude relevant high-frequency components, resulting in loss of detail.
- *Slower dynamic response:* Reacts more slowly to input signal variations.
- *Restricted applicability:* Unsuitable for processing complex or high-frequency signals, such as RF communications or transient measurements.

6.2.2 Wide Bandwidth

Advantages:

- *High-frequency signal transmission:* Enables handling of signals with elevated spectral components, essential in RF and high-speed digital applications.
- *Fast dynamic response:* Enhances temporal fidelity of the system.
- *Greater information capacity:* Supports transmission of a broader data spectrum.

Disadvantages:

- *Increased noise sensitivity:* Allows entry of unwanted signals and disturbances.
- *Design complexity:* Requires careful attention to layout, parasitic effects which will be explained in the next subsection, and compensation strategies.
- *PCB layout challenges:* Parasitic elements (capacitance, inductance, coupling) become significant and may alter circuit behavior.

6.3 Parasitic Effects and Resonances

At high frequencies, parasitic elements become dominant. Distributed capacitances between PCB traces, inductive loops formed by component leads, and coupling between adjacent nodes can generate unintended resonant circuits. These parasitic networks may produce localized gain peaks that do not reflect the intended design behavior. LTSpice, like other SPICE-based simulators, relies on numerical discretization of circuit equations. At elevated frequencies, time-step resolution and solver precision may introduce spurious oscillations or gain anomalies. Additionally, the SPICE models used—particularly for power components such as SiC MOSFETs—are typically validated only up to a few tens of MHz. Beyond this range, simulation accuracy deteriorates and results must be interpreted cautiously.

Operational Limits of SiC MOSFETs

Although SiC MOSFETs offer superior switching performance compared to conventional silicon-based devices, their effective operating bandwidth remains limited. According to Infineon datasheets and application notes, these devices are optimized for switching applications up to several tens of megahertz. At higher frequencies, several physical constraints emerge:

- **Gate charge and capacitance:** The gate-drain and gate-source capacitances (C_{gd}, C_{gs}) perturb the system's time constant, adversely affecting its dynamic response. Moreover, they introduce non-negligible energy losses that compromise the overall efficiency of the circuit.
- **Parasitic inductance:** Bonding wires and PCB traces contribute to inductive reactance, degrading signal integrity and potentially inducing unwanted oscillations.
- **Thermal and stability constraints:** High-frequency operation increases switching losses and thermal stress, which may lead to instability or long-term degradation of the device.
- **Model validity:** Manufacturer-provided SPICE models are typically validated only up to 100 MHz,beyond which it can no longer be considered reliable

6.4 Frequency behavior of circuit 1

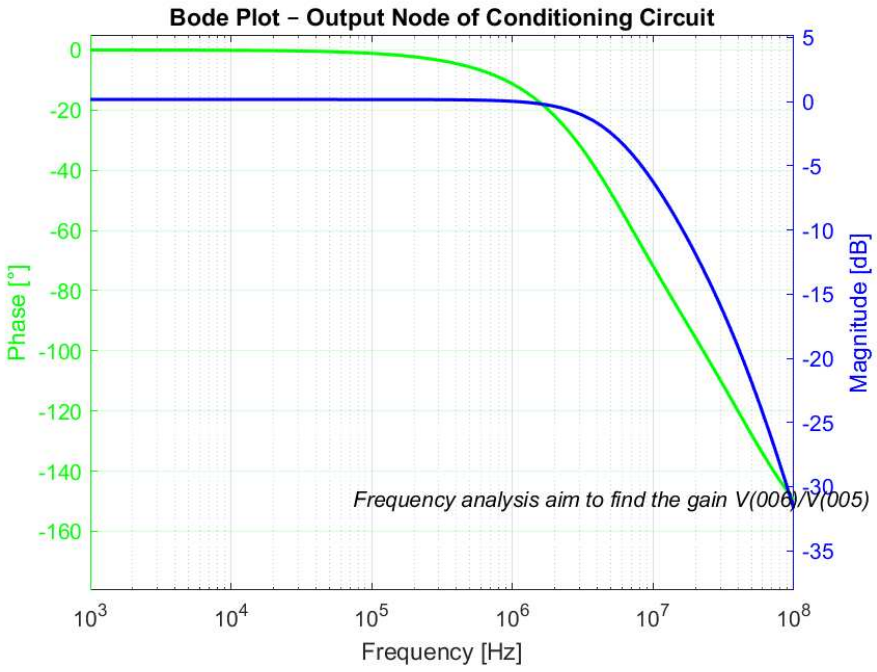


Figure 6.2: Bode diagram of Circuit 1 in a real approach.

6.4.1 Extended Frequency Analysis and Physical Interpretation

With regard to Circuit 1, modeled using real-world components, the frequency analysis yielded significant results, particularly highlighting the circuit's behavior near its cutoff frequency. The extended AC simulation, performed up to 100 MHz, enabled observation of the system's response over a wide frequency range. This investigation provided a more realistic understanding of the circuit's operation, taking into account the non-idealities introduced by physical components and PCB layout constraints.

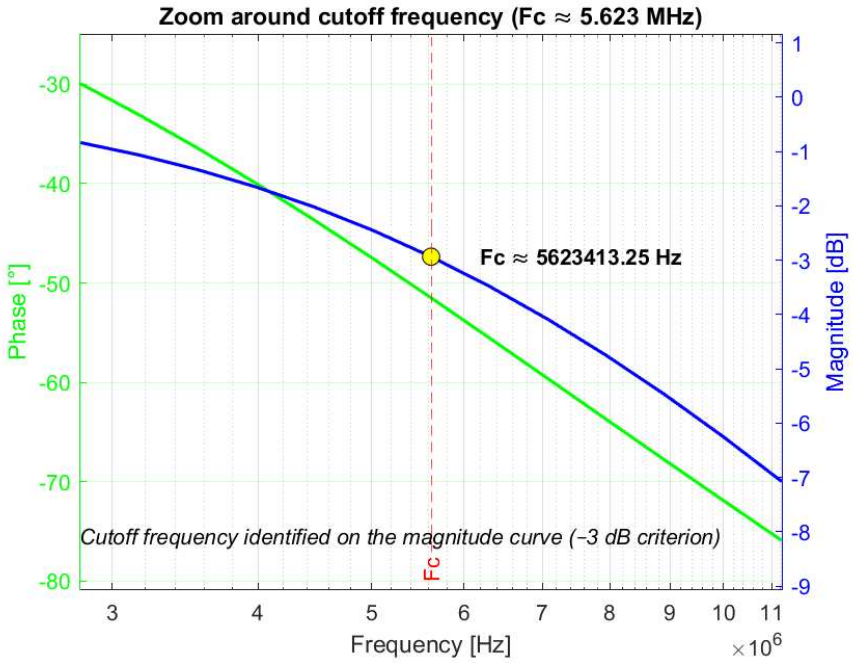


Figure 6.3: The image above shows a zoom of Cut-Off frequency.

Comparison with the Ideal Cutoff Frequency

In the case of Circuit 1, the ideal model predicted a cutoff frequency of approximately 2.818 MHz, whereas the simulation using real components revealed a higher value of 5.623 MHz. Although the discrepancy is not extreme, it remains relevant and warrants further analysis.

This deviation can be attributed to several non-ideal factors inherent in the physical implementation of the circuit:

- **Parasitic capacitances and inductances:** These elements alter the system's time constant, thereby affecting its dynamic response compared to the theoretical model.
- **Packaging-related imperfections:** The physical packaging of components introduces parasitic parameters that can influence the effective impedance of the system. This effect occurs independently of whether the PCB itself is

considered, and extends to the layout and contact traces. The observed shift in cutoff frequency can be interpreted as a direct consequence of this impedance modification.

This comparison underscores the importance of accounting for non-idealities in the design and simulation of real-world circuits.

6.5 Frequency behavior of circuit 2

For Circuit 2, the analysis of ideal model returned a cutoff frequency of approximately 4.467 MHz, whereas the simulation using real components yielded a substantially higher value of 39.811 MHz using the same AC parametres in simultation This order-of-magnitude discrepancy raises important considerations regarding the physical implementation and the choice of components.

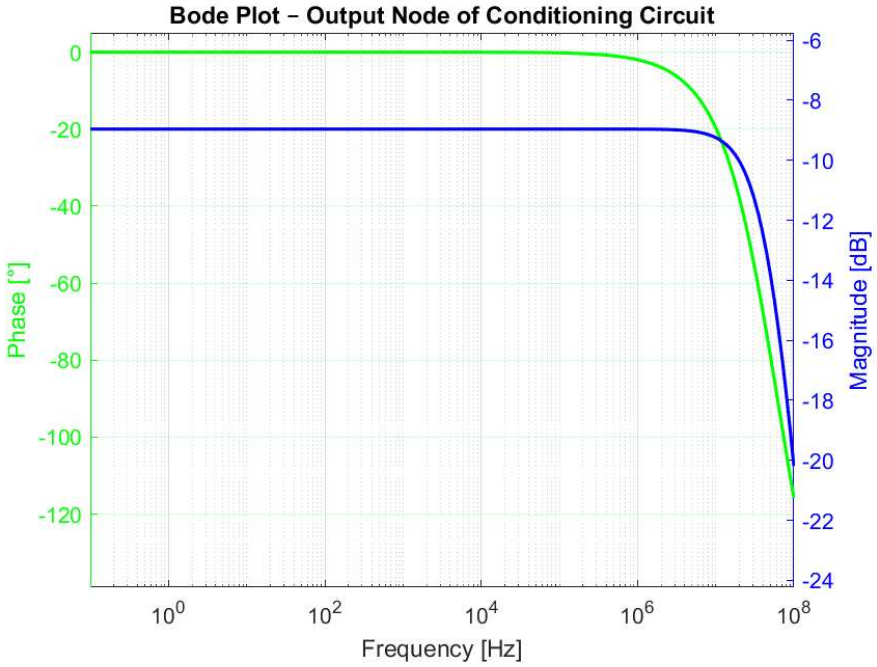


Figure 6.4: Bode diagram of Circuit 2 in a real approach

To provide a clearer representation of the cutoff point in Circuit 2, a focused view of the frequency region near the -3 dB threshold was extracted. The highest gain recorded during simulation was -9.005 dB, and the cutoff frequency was determined at the point where the gain drops to -12.005 dB. This condition corresponds to a cutoff frequency of approximately 39.811 MHz, confirming the circuit's ability to operate effectively in high-frequency environments and to reliably follow the reference signal dynamics.

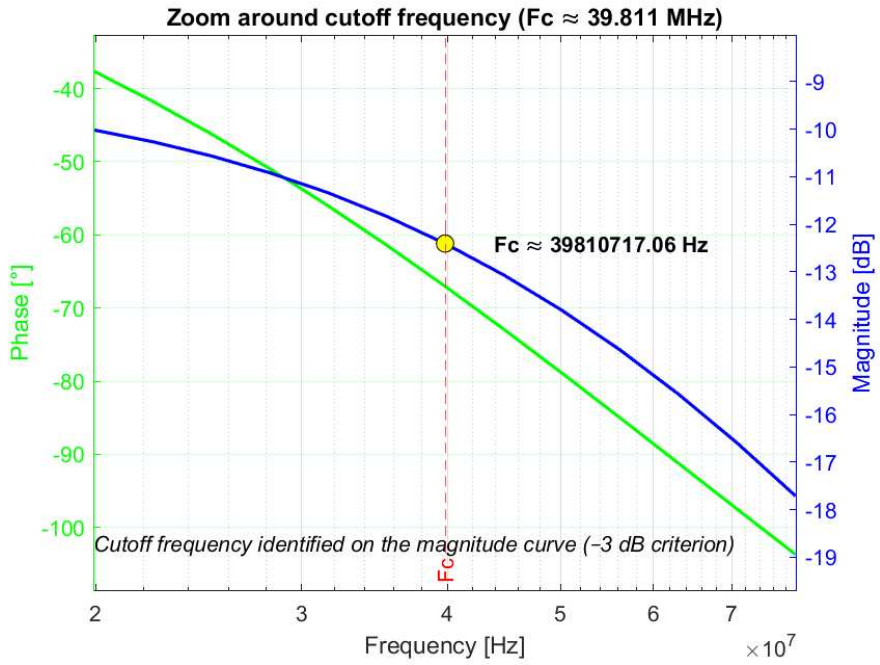


Figure 6.5: The image above shows a zoom of Cut-Off frequency.

The conditioning stage of the circuit employs an OPA357 operational amplifier with enable functionality, known for its high-speed performance and wide bandwidth. While such characteristics are advantageous in terms of fast transient response and minimal signal delay, they also contribute to the propagation of high-frequency components—including noise and unwanted disturbances—that may not be present in the idealized model.

Several factors may explain the observed shift in cutoff frequency:

- **High-bandwidth behavior of the OPA357:** The wide gain-bandwidth product of the op-amp allows the circuit to respond to higher frequency inputs, effectively extending the frequency range beyond the theoretical expectation.
- **Parasitic and layout-induced effects:** As in Circuit 1, parasitic capacitances and inductances alter the effective impedance of the system.
- **Noise and disturbance propagation:** The extended bandwidth, while beneficial for signal fidelity, increases susceptibility to high-frequency noise. If such components are not part of the intended signal, they must be attenuated through appropriate AC filtering strategies to preserve signal integrity.

This observation, emerging from my analysis of Circuit 2, underscores the dual nature of high-bandwidth design encountered throughout the study. On one hand, the elevated cutoff frequency—enabled by the use of a high-speed operational amplifier such as the OPA357—offers clear advantages in terms of signal responsiveness and reduced latency. On the other hand, it also introduces challenges related to the propagation of high-frequency components, including noise and unintended disturbances. These effects, if not properly managed, may compromise signal integrity and must therefore be addressed through careful filtering strategies.

6.5.1 Extended Frequency Analysis and Physical Interpretation

High-Frequency Resonances and Bandwidth Suitability

At elevated frequencies, circuits are more likely to exhibit resonant behaviors due to parasitic effects and then these phenomena can lead to localized gain anomalies that deviate from the intended design response.

Nevertheless, for the specific application of real-time $V_{ds(on)}$ measurement in a TSEP system, the bandwidth achieved is highly suitable. It enables the circuit to accurately track the reference signal with minimal delay, ensuring fast and reliable dynamic response. While high-frequency disturbances may arise, the overall bandwidth represents a well-balanced compromise between speed and signal fidelity.

6.6 Frequency behavior of circuit 3

Bandwidth Evaluation of Circuit 3

In the ideal case, Circuit 3 exhibited a cutoff frequency of approximately 39.818 MHz—a slightly ambiguous value, considering that it was obtained using the generic Universal Opamp2 model, which is unlikely to achieve such wide operational bandwidths in real-world conditions.

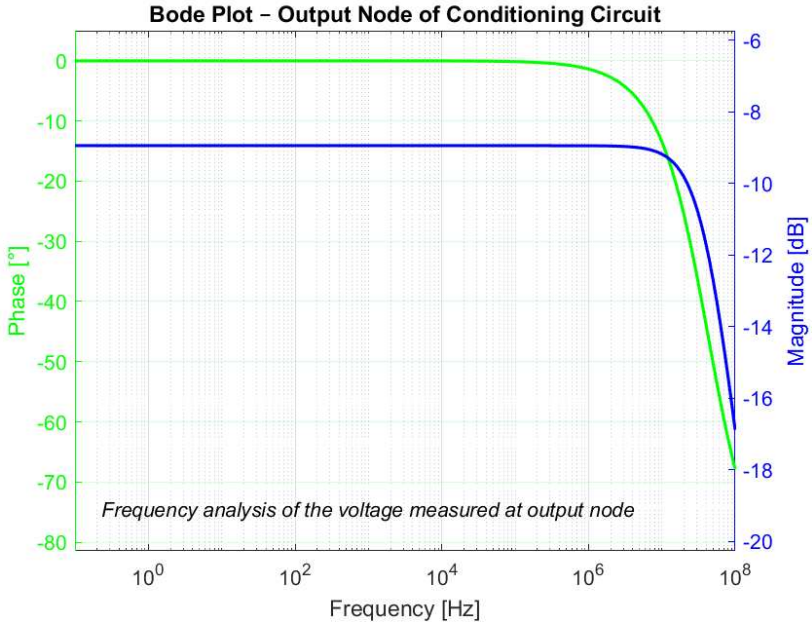


Figure 6.6: Bode diagram of Circuit 3 in a real approach

To better visualize the cutoff point, a zoomed view of the frequency region around the $-3\,\mathrm{dB}$ threshold was extracted. The maximum gain observed in the simulation was $-8.9986\,\mathrm{dB}$; accordingly, the cutoff frequency was identified at the point where the gain drops to $-11.9986\,\mathrm{dB}$. This corresponds to a cutoff frequency of approximately 44.668 MHz, confirming the circuit's ability to operate effectively within high-frequency domains.

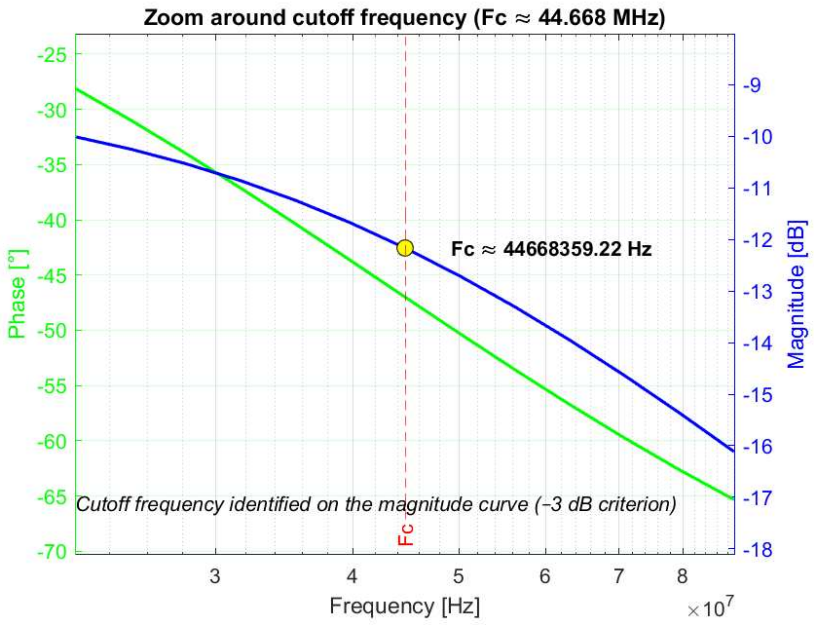


Figure 6.7: Zoomed view of the cutoff region showing the -3 dB drop in Circuit 3

In contrast, the physical implementation yielded a cutoff frequency of 44.667 MHz as shown above, indicating a more responsive configuration well-suited for real-time sampling of $V_{ds(on)}$. This result enables effective tracking of the reference signal, but also necessitates the integration of filtering systems to suppress potential high-frequency disturbances and ensure measurement reliability.

As with the simulations conducted for the previous circuits, the AC sweep parameters used here were identical, ensuring consistency in the evaluation process and allowing for a meaningful comparison across designs.

As previously noted for Circuit 2, the achieved bandwidth represents a solid compromise between speed and precision, yet demands careful design to maintain signal stability and robustness under high-frequency conditions.

6.7 Frequency behavior of circuit 4

Frequency Analysis of Circuit 4

As with the previous circuits, a frequency-domain analysis was also performed for Circuit 4 to validate its dynamic response and investigate the presence of significant components beyond the identified cutoff frequency. To this end, an extended AC sweep simulation was conducted up to 100 MHz.

The Bode diagram below illustrates the magnitude response of the circuit in its default configuration, highlighting its bandwidth characteristics and behavior at high frequencies.

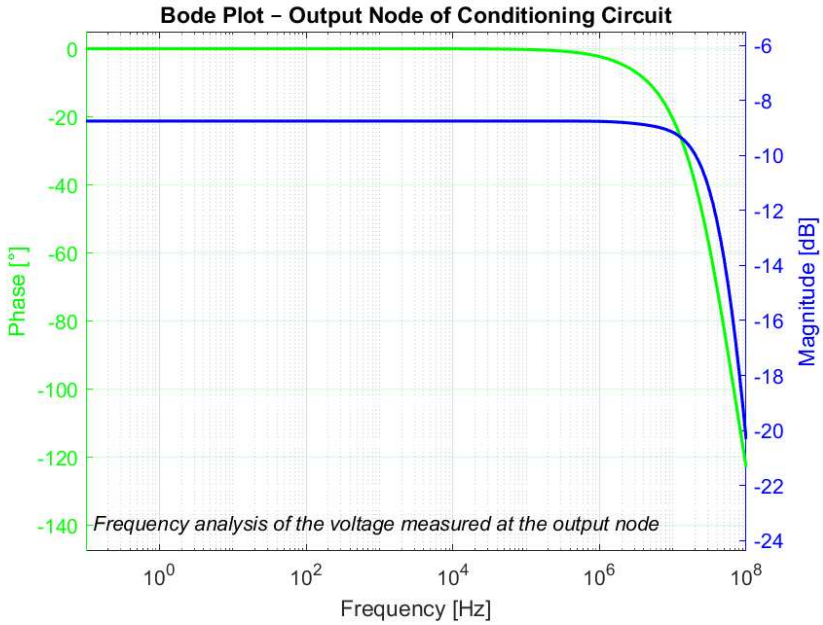


Figure 6.8: Magnitude response of Circuit 4 with real parameter modifications

To ensure consistency with the analysis performed on the other circuits, a detailed examination of the frequency response was also conducted for Circuit 4. A focused view around the -3 dB reference level was used to accurately determine the cutoff point. The peak gain observed during simulation was -8.73 dB, and the cutoff frequency was identified where the gain dropped to -11.73 dB. This corresponds to a cutoff frequency of approximately 35.481 MHz, indicating that the circuit delivers adequate performance for high-frequency applications and supports real-time tracking of $V_{ds(on)}$ with reliable fidelity.

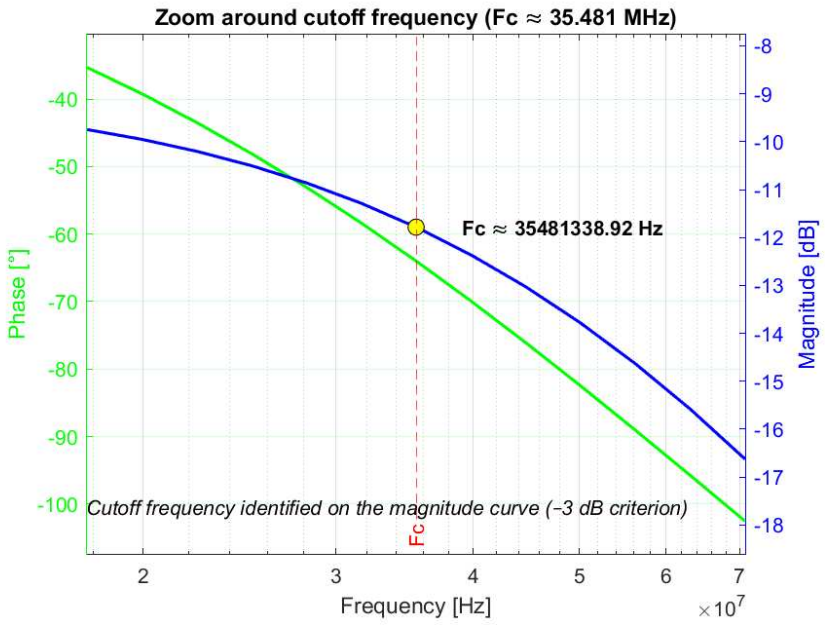


Figure 6.9: Zoomed view of the cutoff region showing the $-3\,\mathrm{dB}$ drop in Circuit 4

Compared to the ideal simulation of Circuit 4, which yielded a lower cutoff frequency due to the limitations of the generic op-amp model, the real-world implementation demonstrates a clear improvement in bandwidth. This confirms the enhanced dynamic response of the physical circuit and its greater suitability for high-frequency signal acquisition.

Chapter 7

Comparative Analysis

7.1 Comparison Between Different Real Circuits

After evaluating the real-world behavior of Circuits 1 through 4, several practical differences emerge. Each configuration offers distinct advantages depending on the intended application, especially in terms of bandwidth, gain, and signal stability.

tabularx

Circuit	**Bandwidth**	**Max Gain**	**Advantages**	**Disadvantages**
1	5.623 MHz	-0.163984 dB	Very stable, high gain, less prone to high-frequency noise	Bandwidth too limited for fast signal tracking
2	39.811 MHz	-9.005 dB	Balanced frequency response, decent compromise between speed and clarity	Sensitive to noise, requires filtering
3	44.667 MHz	-8.9986 dB	Wide bandwidth, ideal for fast sampling and dynamic signals	More exposed to disturbances, needs careful filtering
4	35.481 MHz	-8.73 dB	Higher gain, cleaner output, good fidelity	Slightly narrower bandwidth, less reactive to rapid changes

Table 7.1: Summary of real circuit performance characteristics

7.2 Accuracy, Limitations and Practical Considerations

The results obtained from the online simulations are generally consistent and reliable, but certain practical constraints typical of a real implementation must be taken into account. The AC–sweep parameters were kept identical across all circuits to ensure a

homogeneous comparison, yet in a physical environment exceeding 100 MHz because it would push the device beyond its operational limits, leading to high-frequency artifacts that are neither representative of actual behavior nor physically meaningful.

Although no measurement bench was assembled—since the entire analysis was conducted in simulation—it is useful to anticipate that, upon fabrication of a real board, solder joints, PCB traces, and component packaging would introduce small parasitic capacitances and inductances. These instrumental elements would cause measurement inaccuracies, especially at the band edges, with potential reflections or attenuations that the ideal simulation cannot replicate.

The op-amps used in the simulated models exhibit ideal theoretical performance, whereas real op-amps present internal limitations such as finite slew rate, finite input/output impedance, and limited bandwidth. These constraints result in discrepancies between simulated and experimental responses: in wide-bandwidth circuits, even marginal variations in the frequency response can produce signal distortion or unexpected gain drops.

Finally, it should be emphasized that the primary goal of this analysis is not absolute precision but rather a qualitative understanding of how each topology behaves under realistic conditions. This approach enables the identification of the optimal configuration in terms of response speed, stability, and signal clarity, while maintaining a degree of flexibility in data interpretation.

Chapter 8

Conclusions and Future Work

8.1 Summary of Findings

Throughout this work, several conditioning circuits were analyzed with the aim of evaluating both their frequency response and dynamic behavior under transient simulation. Particular attention was given to how each circuit handles the output signal from the operational amplifier, especially during rapid transitions of the reference signal $V_{ds(on)}$.

By observing the rising and falling edges, it was possible to assess how quickly and accurately each circuit follows the reference profile. This helped distinguish between configurations that are more reactive and those that, while offering a cleaner output, are less dynamic. The results obtained so far show that circuit performance depends not only on bandwidth, but also on how the output signal is conditioned and how well the circuit replicates the reference under realistic conditions.

8.2 Conclusions

Regarding the frequency behavior, preliminary results suggest that Circuit 3, thanks to its wide bandwidth, appears particularly promising for applications requiring fast and accurate tracking of the $V_{ds(on)}$ signal. This early observation indicates that configurations with greater bandwidth may offer significant advantages in terms of responsiveness, although further investigation is needed to assess potential trade-offs in stability and noise.

Regarding the transient analysis, the Topology 2 provides the highest dynamic responsiveness, as does Topology 3; both ensure the most accurate tracking of rapid changes in Vds(on), and Topology 3 emerges as the optimal solution among those examined.

8.3 Suggested Future Extensions

A natural extension of this work involves the physical implementation of the selected conditioning circuit, integrating real-time measurements of $V_{ds(on)}$ into a voltage–temperature calibration system. The idea is to use the measured value of

$V_{ds(on)}$ as a temperature-sensitive electrical parameter (TSEP), allowing the construction of a reference curve for thermal monitoring of the device. This approach would enable direct exploitation of the component's electrical behavior to extract thermal information, reducing the need for external sensors and simplifying the overall system architecture.

Chapter 9

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