POLITECNICO DI TORINO

Master's Degree in Electronics Engineering

Master's Degree Thesis

GaAs MMIC technology evaluation and Doherty power amplifier design

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Acronyms

BO	back-off
DPA	Doherty Power Amplifier
EM	electromagnetic
MAG	maximum available gain
OBO	Output Power Back-off
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	peak-to-average power ratio
RF	Radio Frequency

Chapter 1

Theoretical Fundamentals

1.1 Power Amplifiers

The Power Amplifier (PA) is one of the fundamental blocks of the transceiver chain. As shown in Fig.1.1, PAs are usually the last element before the antenna and are used to boost the signal to higher power levels so that it can be transmitted over long distances.

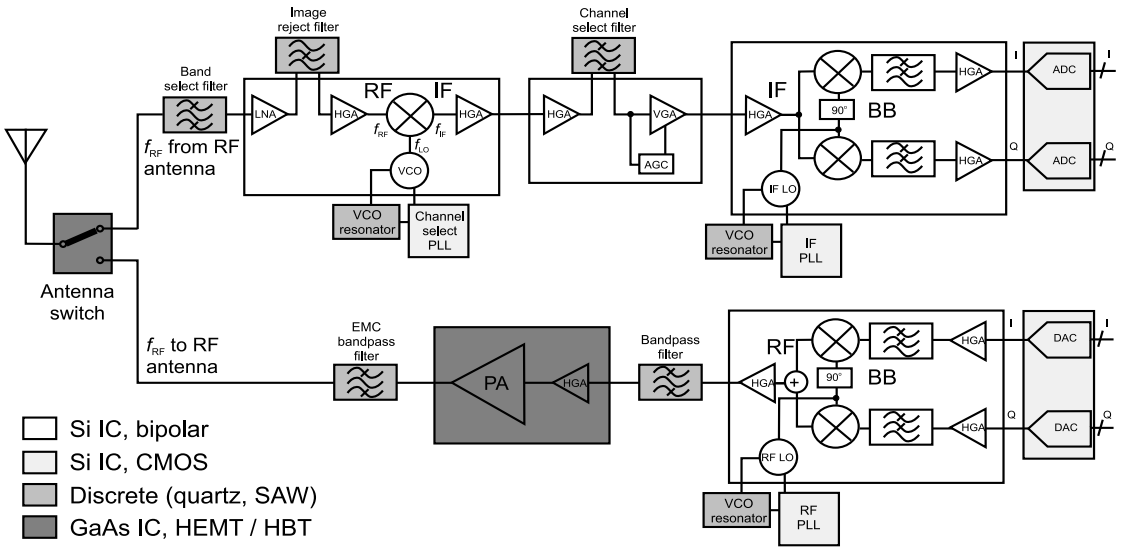

Figure 1.1: Building blocks of a transceiver[1]

The PA converts the DC power supplied into RF power at the load with a certain efficiency.
The goal is to obtain the desired output power while keeping gain and efficiency as high as possible.

1.1.1 Figures of Merit

In an amplifier, figures of merit are the parameters or measurements that characterize its behavior and performance.

Saturated Output Power

It is the maximum power that the device can deliver to the load.
The maximum value of the power is related to the characteristics of the device.
By increasing the size of the device's periphery, it is possible to increase the output power.

Power Gain

The gain is defined as the ratio between output power and input power.
There are multiple definitions of power gain, but the most commonly used ones are:

$$G_{\text{op}} = \frac{P_{\text{out}}(f)}{P_{\text{in}}(f)} \tag{1.1}$$

$$G_{\text{t}} = \frac{P_{\text{out}}(f)}{P_{\text{in,av}}(f)} \tag{1.2}$$

Efficiency

Efficiency is the ratio between the output RF power and the DC power delivered by the supply.

$$\eta = \frac{P_{\text{out}}(f)}{P_{\text{DC}}} \tag{1.3}$$

This definition does not take into account the power delivered to the amplifier input.
The Power Added Efficiency (PAE) also considers the input power and is defined as:

$$PAE = \frac{P_{\text{out}}(f) - P_{\text{in}}(f)}{P_{\text{DC}}} = \eta \left(1 - \frac{1}{G_{\text{op}}}\right) \tag{1.4}$$

Output Power Back-off (OBO)

OBO is defined as the distance in dB between the saturated output power and the output power level corresponding to the input signal.
When the amplifier works in back-off (BO), the efficiency is much lower compared to the level reached at saturation.

1.1.2 PA classes

PAs are usually divided into classes.
In this section, only classes A, B, C, and AB are described, although many other classes exist.
The class of operation of an amplifier is determined by the bias point, as shown in Fig. 1.2.

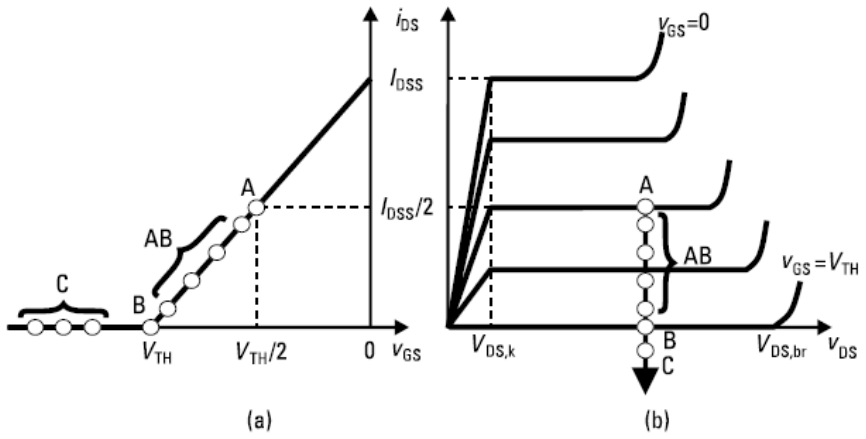

Figure 1.2: Transcharacteristics (a) and output characteristics (b) of an ideal FET device; different bias point correspond to a different class[2]

Class A

In class A, the device is biased with $V_g = \frac{V_{th}}{2}$ so that the device conducts for the whole cycle (Fig.1.3).
Class A offers the best linearity and can also achieve the highest gain compared to other classes.
The drawback of this class is the low efficiency, which can reach at best 50%.

Class B

The gate voltage in class B is $V_g = V_{th}$ (Fig.1.4).
The device is ON only for half the cycle, which means that when there is no input, the device is OFF and does not waste power like in class A, therefore the maximum efficiency is higher (78%). Compared to class A, there is a gain penalty of 6 dB.

Class AB

In class AB, the gate bias is higher than in class B but lower than in class A.
The conduction angle of the device can range between π and 2π (Fig.1.5).

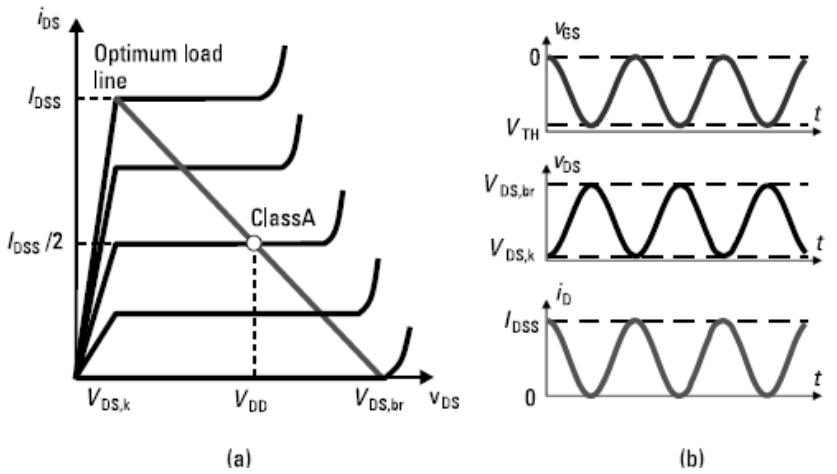

Figure 1.3: Load line (a) and time domain waveforms (b) for class A[2]

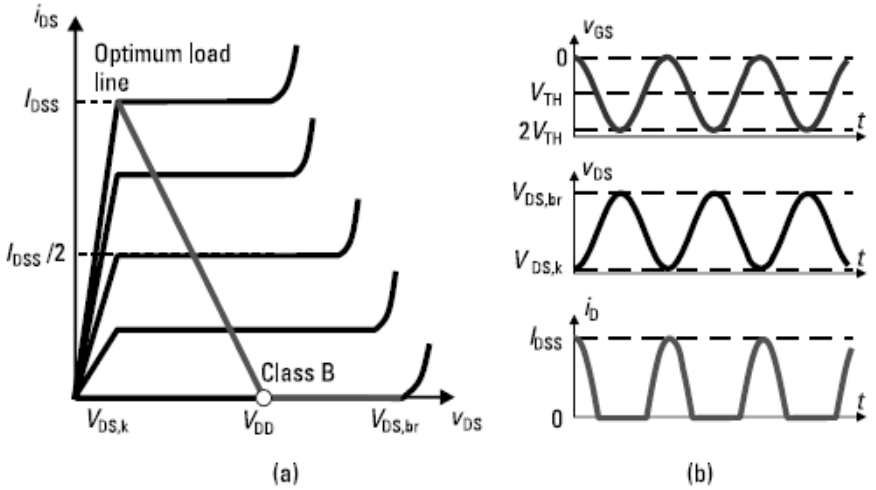

Figure 1.4: Load line (a) and time domain waveforms (b) for class B[2]

The performance in terms of efficiency, gain, and linearity are in between those of classes A and B, making this class a compromise between the two.

Class C

In class C, the gate bias is lower than the threshold voltage, so the device is ON for less than half the cycle.
It is theoretically possible to achieve very high efficiency with this class, up to 100%.

However, class C also presents very high distortion and a lower gain compared to the previous classes.

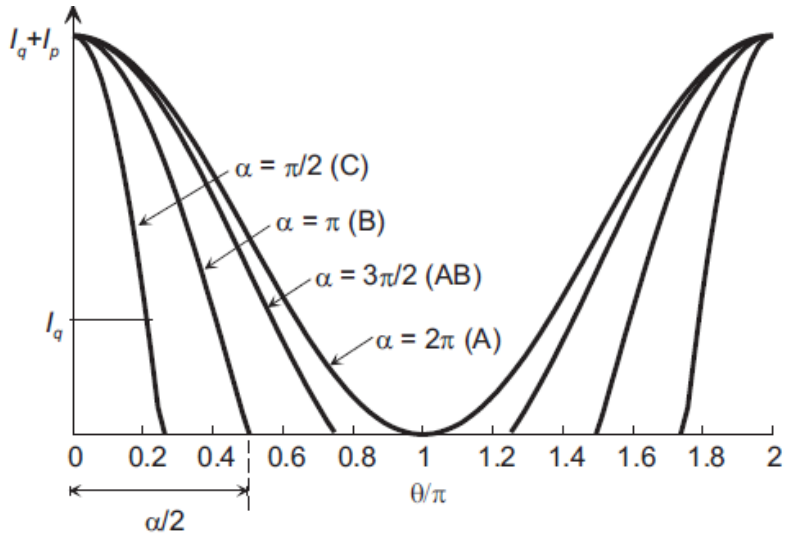

Figure 1.5: Drain current vs conduction angle[1]

1.2 Doherty Amplifier

Nowadays, wireless communication systems often employ complex modulation schemes.
This kind of modulation often involves high peak-to-average power ratio (PAPR) signals, meaning that the working power levels of the PA are not constant and are often far from saturation, where the PA has the best efficiency.
Standard PAs, analyzed in Section 1.1.2, are not optimal for this kind of situation because, regardless of the class, when the PA operates in BO its efficiency degrades.
Doherty Power Amplifiers (DPAs) are one of the architectures proposed over the years as a solution to avoid efficiency drops when operating in BO.
To obtain high efficiency also in BO (e.g. when $V_{\text{in}} = \frac{V_{\text{in,max}}}{2}$), the load must be changed to twice the optimum value computed for saturation.
Therefore, a circuit capable of modulating the load based on the variations of the input signal is needed.[3]

1.2.1 Load Modulation

To achieve this load modulation effect, the schematic shown in Fig.1.6 is used.

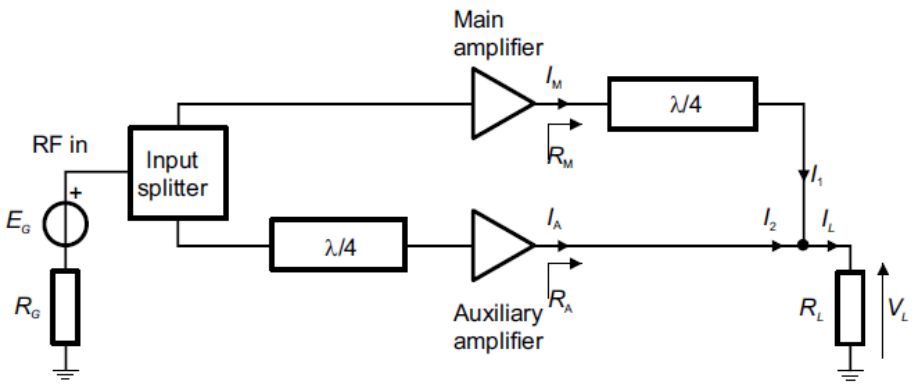

Figure 1.6: Schematic of an ideal Doherty amplifier[1]

When the input signal is low, the auxiliary amplifier is off and only the main amplifier is working.
If the signal increases past a certain value, the auxiliary turns on and changes the value of the load seen by the main amplifier.
To understand how the presence of the auxiliary changes the load, we can look at Fig.1.7.

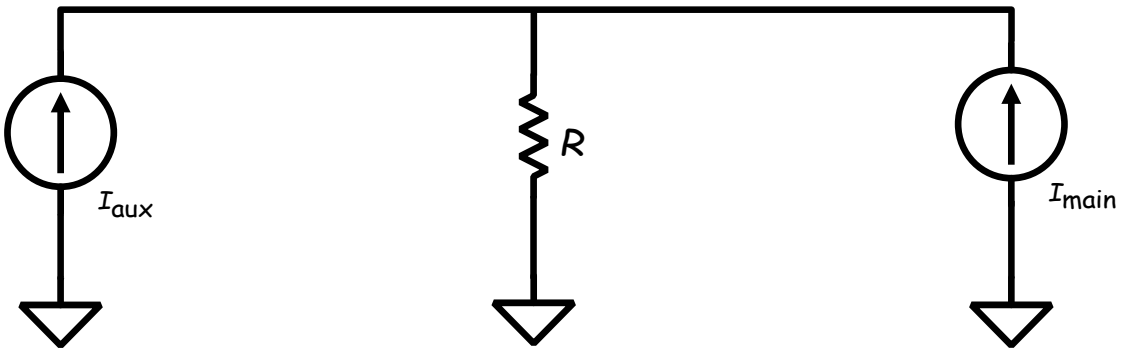

Figure 1.7: Basic scheme for active load pull

The impedance seen from the main is:

$$Z_{\text{main}} = R\left(\frac{I_{\text{main}} + I_{\text{aux}}}{I_{\text{main}}}\right) \tag{1.5}$$

If $I_{\text{aux}} = 0 \longrightarrow Z_{\text{main}} = R$
If $I_{\text{aux}} = I_{\text{main}} \longrightarrow Z_{\text{main}} = 2R$

With this topology, the impedance seen from the main increases going towards the saturation region. Since the load must decrease instead of increasing, a quarter-wavelength transformer is added, as shown in Fig.1.6. As a consequence, the formula in (1.5) changes to:

$$Z_{\text{main}} = \frac{R^2}{R\left(\frac{I_{\text{main}}+I_{\text{aux}}}{I_{\text{main}}}\right)} = R\left(1 - \frac{I_{\text{aux}}}{I_{\text{main}}} + I_{\text{aux}}\right) \tag{1.6}$$

Now, when the auxiliary turns on, I_{aux} increases and Z_{main} decreases accordingly. If $I_{\text{aux}} = I_{\text{main}} \rightarrow Z_{\text{main}} = \frac{R}{2}$, therefore choosing $R = 2R_{\text{opt}}$ the results obtained are the desired ones as shown in Fig.1.8.

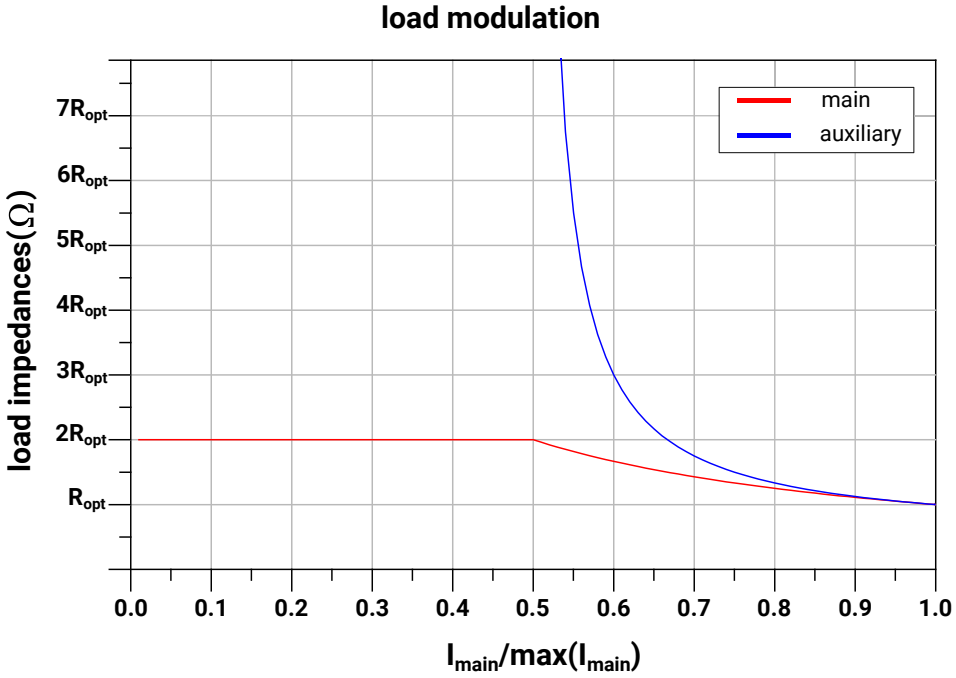

Figure 1.8: Load modulation obtained with the ideal combiner topology

To obtain this behavior, we must ensure that the auxiliary turns on after the main when the input signal starts to increase.
To achieve this, two different bias voltages are used for the gate of the 2 devices. The main is biased in class AB or B while the auxiliary is usually biased in class C. Thanks to this strategy, at 6dB OBO, the Doherty should ideally have the same efficiency value that is reached at saturation, as shown in fig.1.9.
The final element that needs to be added is a 90°phase delay before the auxiliary to compensate for the quarter-wavelength transformer added in the combiner (Fig.1.6). This compensation is needed to make sure that the main and auxiliary currents are in phase at the output node, otherwise the load modulation would not be correct.

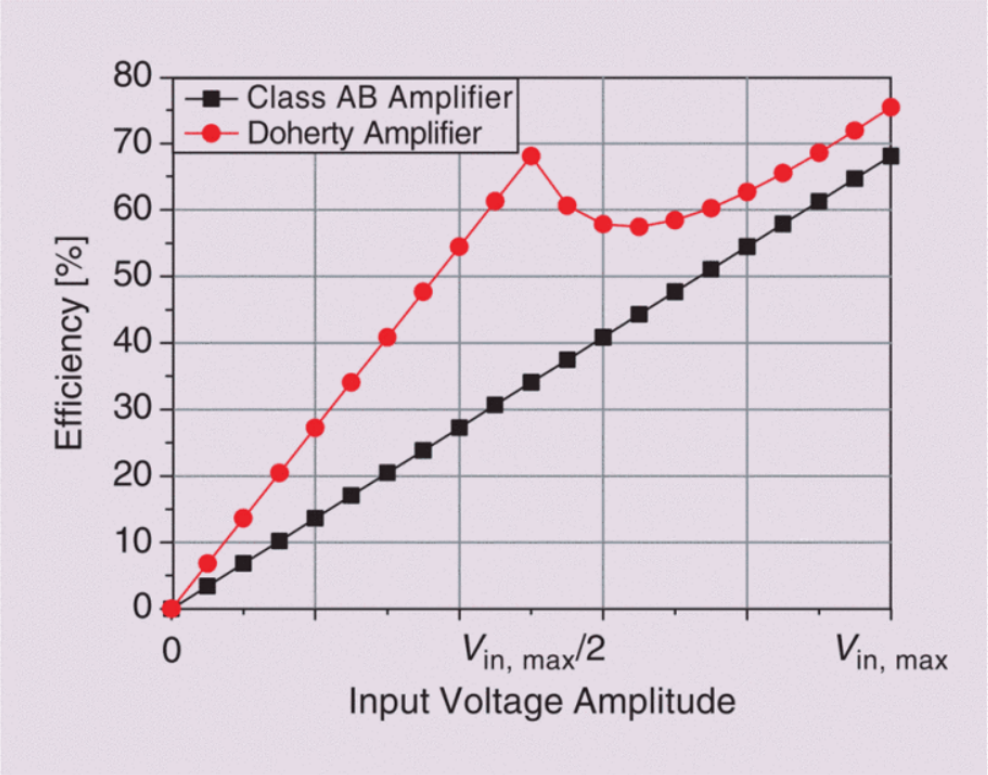

Figure 1.9: Efficiency Doherty vs Class AB[4]

In summary, until $V_{\text{in}} < \frac{V_{\text{in,max}}}{2}$ only the main amplifier is working with a load equal to $2R_{\text{opt}}$.
After this threshold, the auxiliary turns on and the load seen by the main changes from $2R_{\text{opt}}$ to R_{opt} to keep the efficiency high until saturation.

Chapter 2

Comparison of the Two Selected Technologies

The two technologies under investigation are Win PQG3 and UMS PPH15X-20.
For the first technology, the device used is the D-mode transistor because the datasheet indicates that it should have better performance than the E-mode in terms of power density.
For the second technology, the device is the NHF2P as it is the most suitable for power applications and has been validated for a wider range of device sizes compared to the other available options.
Both devices are biased in Class AB.
For PQG3: $V_{\mathrm{d}} = 4\,\mathrm{V}$, $V_{\mathrm{g}} = -0.4\,\mathrm{V}$ and $I_{\mathrm{d}} = 115\,\mathrm{mA}$.
For PPH15X-20: $V_{\mathrm{d}} = 6\,\mathrm{V}$, $V_{\mathrm{g}} = -0.7\,\mathrm{V}$ and $I_{\mathrm{d}} = 130\,\mathrm{mA}$.

2.1 MAG Comparison

In the first comparison, different peripheries of the same technology are analyzed to compare the MAG in the 8-12 GHz frequency band. The results are reported in Fig.2.1 and Fig.2.2.
For both technologies, the gain at 12 GHz is around 2 dB lower than the value at 8 GHz. Ideally, after adding a stabilization network, this drop should be reduced to achieve a more uniform gain across the bandwidth.
The periphery with the highest gain is the 4x150 µm for both technologies but the UMS version performs better.

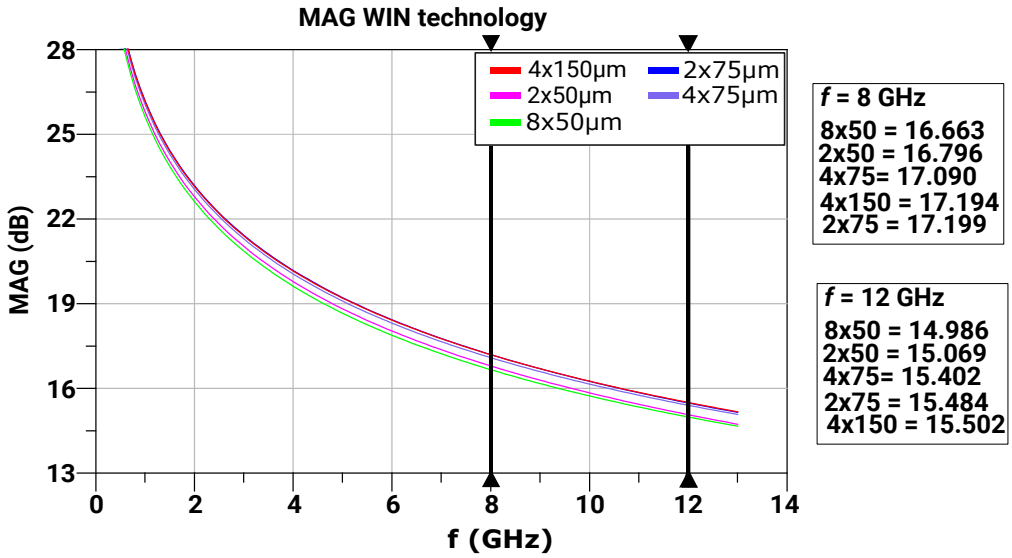

Figure 2.1: MAG comparison among WIN peripheries

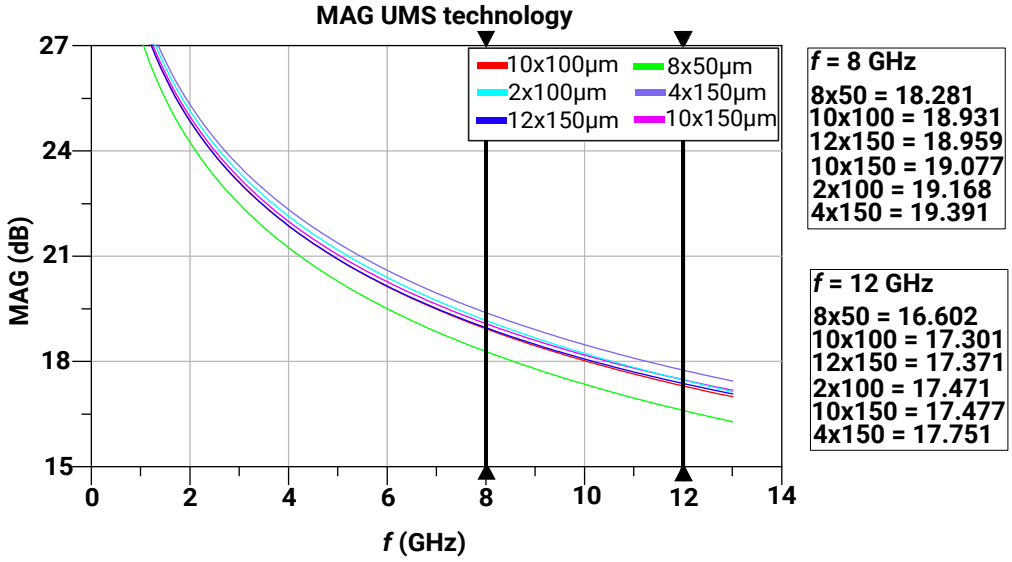

Figure 2.2: MAG comparison among UMS peripheries

A stabilization network, shown in Fig.2.3 is added to check how much gain is lost for each device.

In Fig.2.4 and Fig.2.5 is shown how the MAG changes after stabilization. UMS is still better after this step, not only because of the higher gain but also because it was easier to achieve a flat gain across the desired bandwidth.

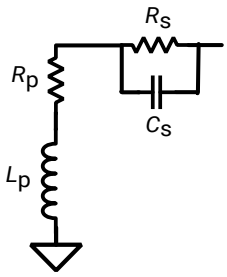

Figure 2.3: Stabilization network

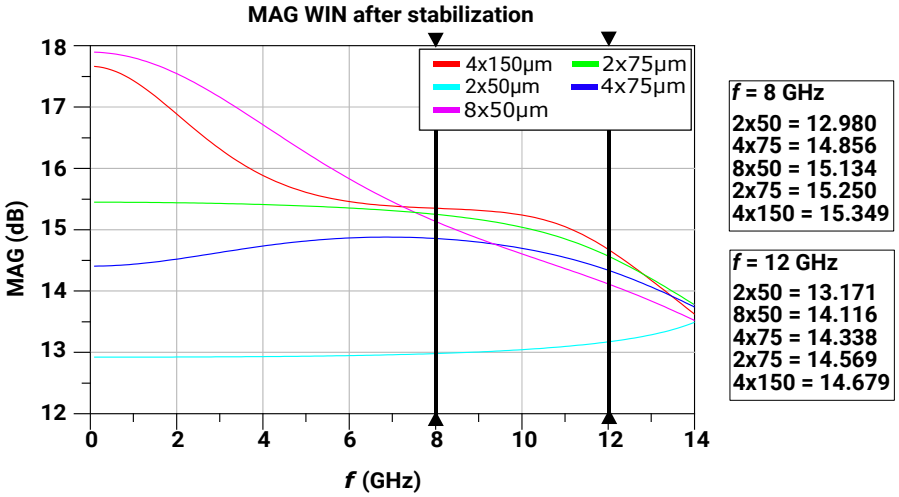

Figure 2.4: MAG after stabilization WIN

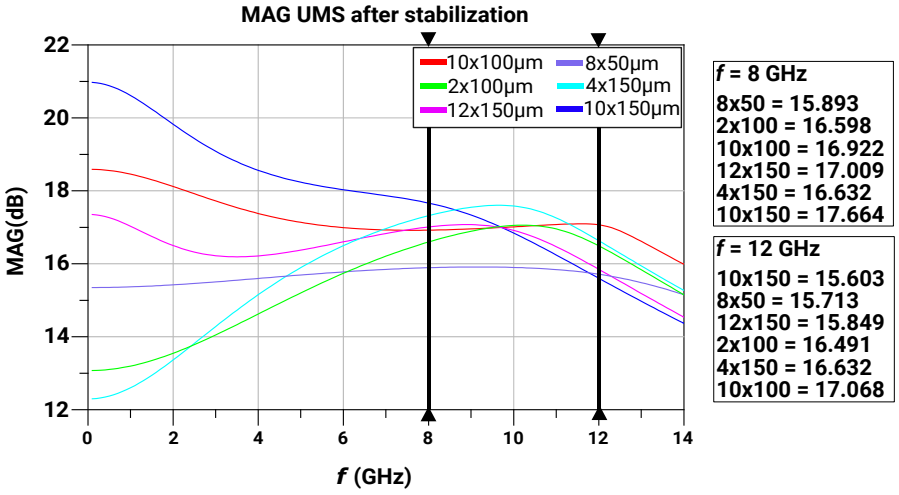

Figure 2.5: MAG after stabilization UMS

2.2 Output Power and Efficiency Comparison

Gain is not the only important parameter to take into account when comparing two technologies.
Since for this design the Doherty should be able to deliver 1 W as output power, we need to identify the best peripheries for this target power. The main and auxiliary amplifiers deliver 0.5 W each, which corresponds to 27 dBm.
Fig.2.6 shows how the output power varies with different peripheries for each technology.

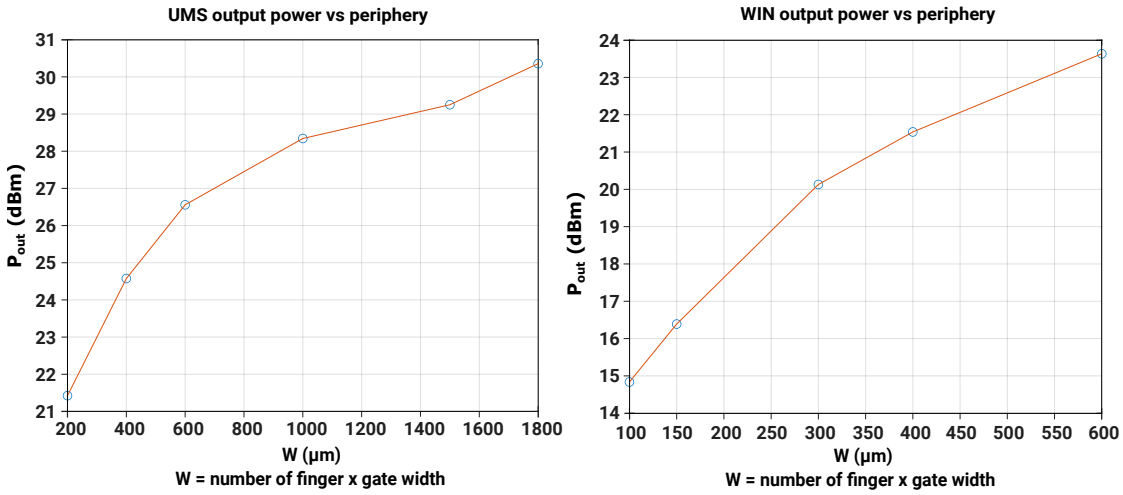

Figure 2.6: Output power comparison

These curves were obtained using linear interpolations starting from the points marked with circles, which come from simulation results.
The power levels represented in the pictures correspond to the 1 dB compression point. UMS achieves higher output power compared to WIN, given the same periphery. Moreover, UMS offers larger peripheries that can easily reach the target power, on the other hand, none of the WIN options reach the 27 dBm level.
It is still possible to use WIN devices by combining them in parallel to obtain the desired power.
The peripheries considered for the following comparisons are:

- 4x150 µm as it is available for both technologies and is the only WIN option that approximately reaches 27 dBm without combining more than two devices
- UMS 10x100 µm and 12x150 µm since these peripheries can reach the target power without combining multiple devices (these sizes are not available in WIN)

The optimum loads, listed in Table 2.1, were selected after performing a load pull simulation at 12 GHz since the highest frequency is the most critical.

Technology	Z_S	Z_L
4x150 µm WIN	$15.123 + j12.959\ \Omega$	$23.042 + j11.115\ \Omega$
4x150 µm UMS	$17.519 + j18.733\ \Omega$	$26.602 + j9.963\ \Omega$
10x100 µm UMS	$4.777 + j12.099\ \Omega$	$17.521 + j12.276\ \Omega$
12x150 µm UMS	$2.161 + j5.657\ \Omega$	$11.220 + j4.682\ \Omega$

Table 2.1: Values of input and output loads

The results obtained are shown in the following figures, where markers indicate the 1 dB compression point.

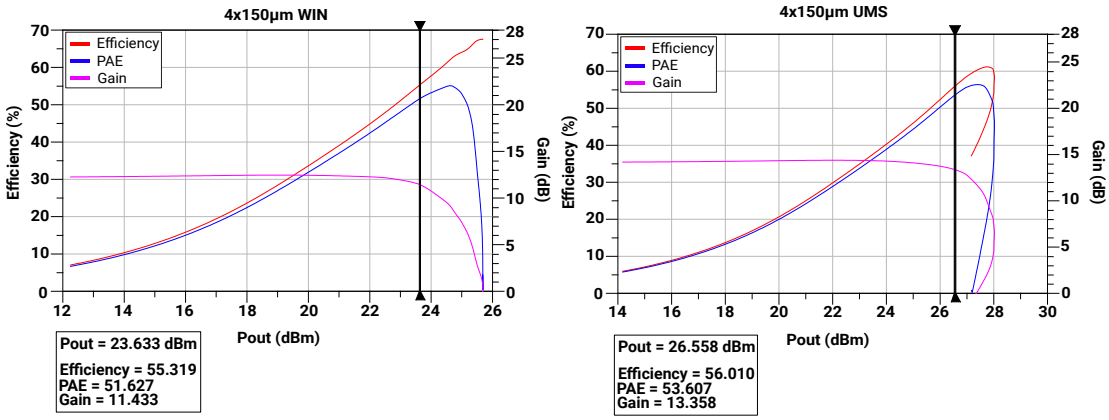

Figure 2.7: 4x150 µm comparison (WIN vs UMS)

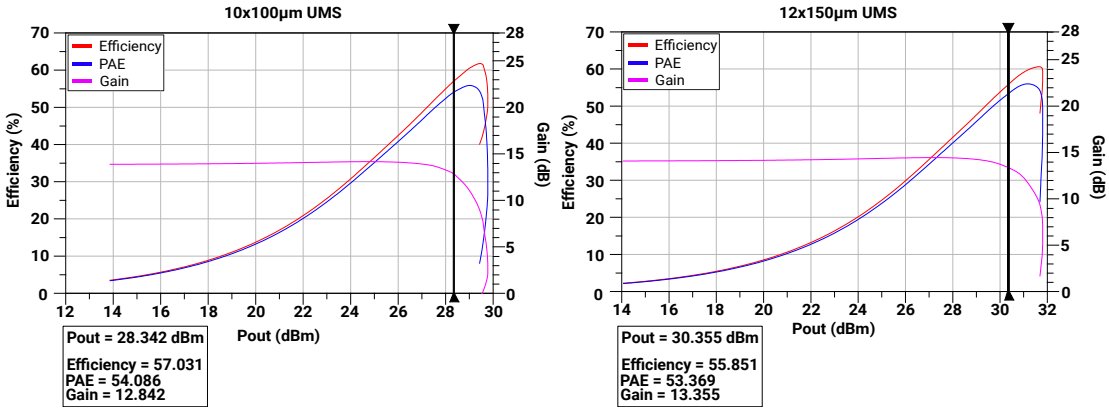

Figure 2.8: 10x100 µm vs 12x150 µm (UMS)

UMS devices exhibit better gain, efficiency and output power compared to WIN devices.
The best WIN solution is the 4x150 µm but it has a 2 dB gain penalty compared to the same periphery in UMS. The output power of the WIN device is much lower (around half) and also efficiency is lower.
With this solution, for both technologies, more than one device must be used in parallel to reach 27 dBm.
UMS also provides larger peripheries that can reach the target power as shown in Fig.2.8.
The 12x150 µm configuration delivers an output saturated power which is more than double compared to the needed one, so it is not a good choice even though it has higher gain.
The 10x100 µm seems to be the best compromise among UMS peripheries.
The devices analyzed in this section will be used in Chapter 3 for the design of the DPA. Two designs will be carried out in parallel using the two technologies under investigation and the final results will be compared.
The peripheries selected are:

- Two 4x150 µm devices in parallel for WIN technology
- A single 10x100 µm device for UMS technology

Chapter 3

Ideal Circuit design

This chapter describes all the details of the design flow of a DPA. As mentioned in Chapter 2 the devices considered are the WIN PQG30C D-mode transistor and the UMS PPH15X 20 NHF2P.

3.1 Active Device Characteristics

3.1.1 Bias Point Selection

The first step in PA design is the selection of the bias point. By analyzing the DC characteristic of the devices it is possible to find the appropriate values.

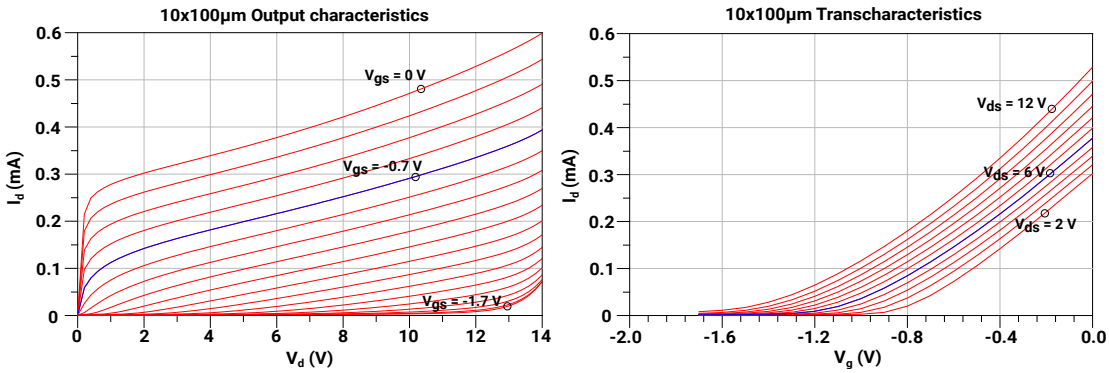

Figure 3.1: 10x100 µm UMS output characteristic (left) and transcharacteristic (right)

The main is biased in class AB and the auxiliary in class C. From Fig.3.1 we can observe that the breakdown voltage is around 13 V, so the drain voltage is set to 6 V (as suggested in the design manual). The gate bias is selected by looking at the transcharacteristic and at the $I_{\mathrm{d,sat}}$. In class A, the drain current should be half of

the saturation value so for class AB in this case the gate voltage selected is -0.7 V, which corresponds to 30% of $I_{\mathrm{d,sat}}$. For the auxiliary, the gate voltage should be selected in the range where Id=0 so Vg = -1.9 V is selected.

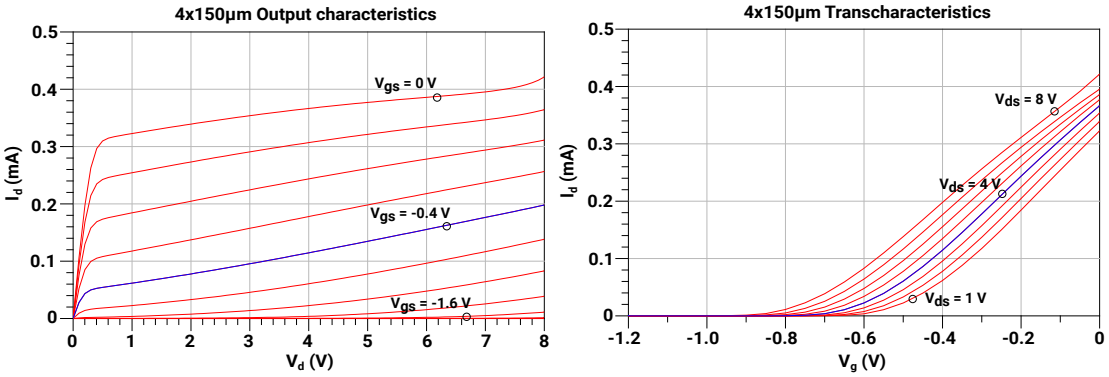

Figure 3.2: 4x150 µm WIN output characteristic (left) and transcharacteristic (right)

It is possible to perform a similar analysis using Fig.3.2 to determine the bias voltages for WIN. The final values selected are listed in Table 3.1.

Technology	V_{d}	V_{g} main	V_{g} auxiliary
WIN	4 V	−0.4 V	−1.5 V
UMS	6 V	−0.7 V	−1.9 V

Table 3.1: bias voltages

3.1.2 Stabilization Network

Stability is one of the key aspects in the design of PAs not only inside the band but also outside it, especially at low frequency. To ensure unconditional stability, as demonstrated in [1], two conditions must be satisfied:

- "the input impedance must have a positive real part for any value of the load impedance"

- "the output impedance must have a positive real part for any value of the generator impedance."

Therefore, to stabilize the devices, dissipative elements, such as resistors, are needed. If the input impedance is negative at some frequencies, it can be compensated by adding a resistor in series or in parallel. The addition of these elements strongly

impacts the MAG; therefore reactive components are also introduced to reduce the impact of resistors within the band of interest while keeping the device stable also outside the bandwidth, especially at lower frequencies. The topology used for the stabilization network is shown in Fig.2.3.
To verify if the devices are unconditionally stable it is possible to use the one-parameter stability criterion. As explained in [5] it is sufficient to check when the parameter $\mu > 1$

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \Delta| + |S_{12} S_{21}|} \tag{3.1}$$

Fig.3.3 and Fig.3.4 show that the two devices are stable in the range (0-14) GHz. The stabilization network was designed to make the gain as flat as possible within the band of interest. The UMS device has a gain of 17 dB which is 2 dB higher than that of WIN and the gain is also flatter.

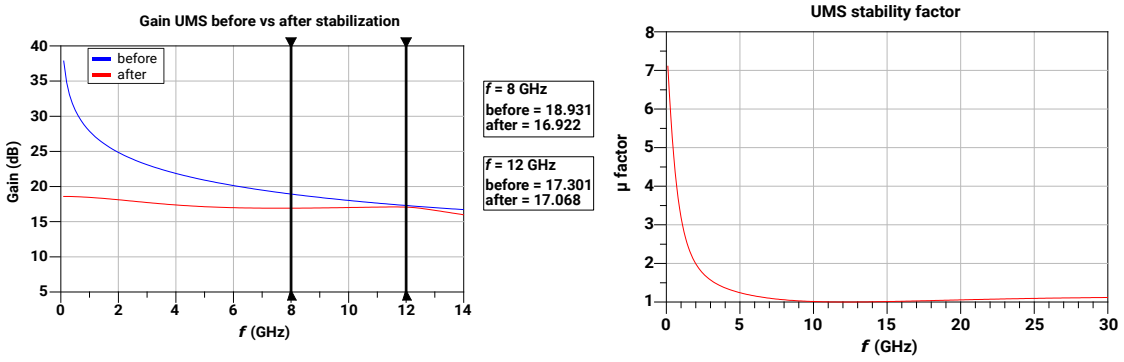

Figure 3.3: Gain and μ factor UMS

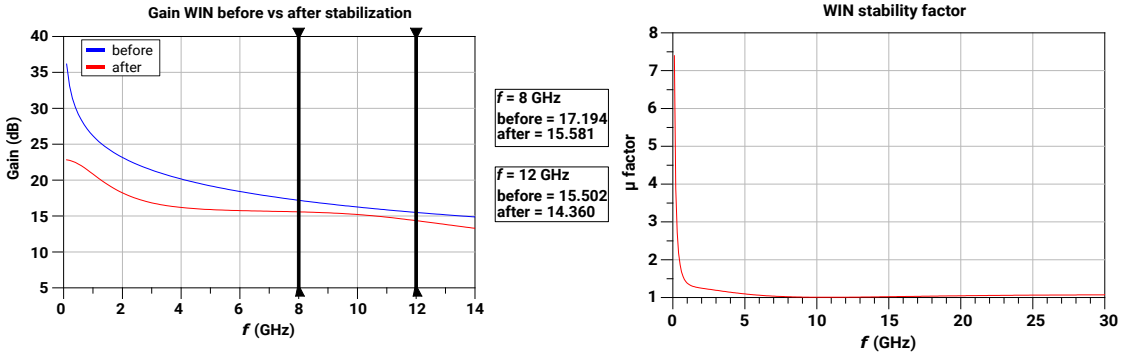

Figure 3.4: Gain and μ factor WIN

3.1.3 Optimum Input and Output Terminations

The next step is to determine the input and output impedances needed to reach the target power without losing too much efficiency. The following load-pull simulations are performed at 10 GHz, which is the center frequency. The circles in Fig.3.5 represent groups of loads that give the same output power (red lines) or the same efficiency (blue lines).

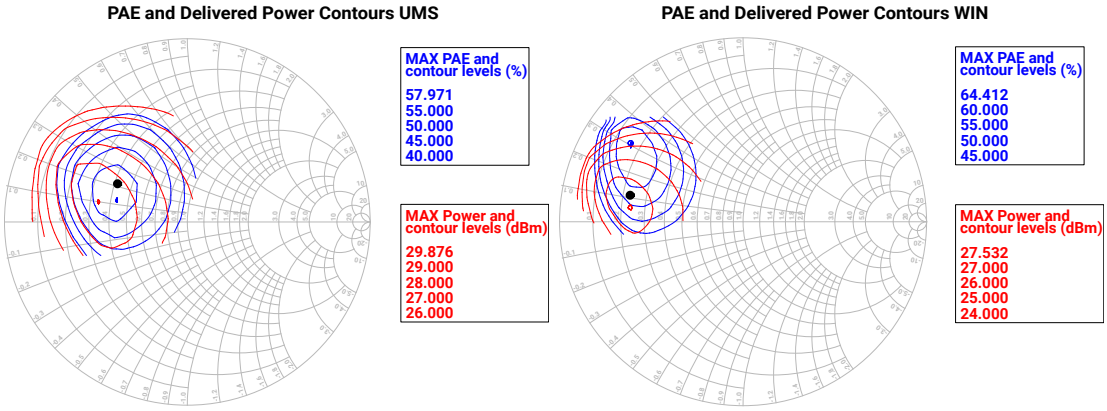

Figure 3.5: Load pull simulations

WIN

For WIN two devices in parallel are used as shown in Fig.3.6.

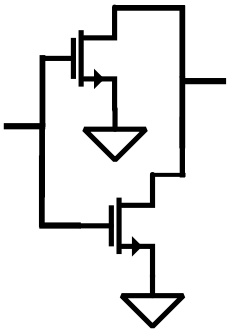

Figure 3.6: WIN devices in parallel

Even with this topology, the load was selected for maximum output power because the maximum is barely enough to achieve the desired 27 dBm. The chosen load and the corresponding optimum input impedances are listed in table 3.2.
With these impedances, the load seen at the intrinsic drain node is real for both the main and the auxiliary (14 Ω). The main amplifier should also be optimized in

	Z_S	Z_L
main	$7.159 + j16.146\,\Omega$	$11.176 + j5.253\,\Omega$
auxiliary	$6.189 + j15.949\,\Omega$	$11.45 + j3.3\,\Omega$

Table 3.2: Optimum load WIN

the back-off region since the amplifier is used for a Doherty configuration.
The optimum value found is:
$Z_{load} = 17.1 + j12.75\,\Omega$
This load gives a real impedance of 27 Ω at the intrinsic node, which is twice the value obtained in the saturation region. Since the input power is split evenly between the main and the auxiliary and the periphery is the same, the combiner will synthesize a load that is twice the one at saturation.

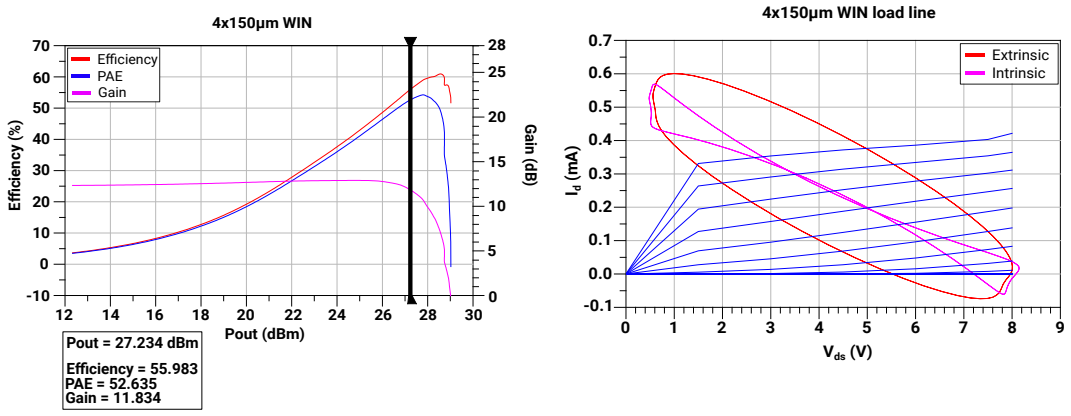

Figure 3.7: Main amplifier gain and efficiency vs Pout (right); Load lines (left)

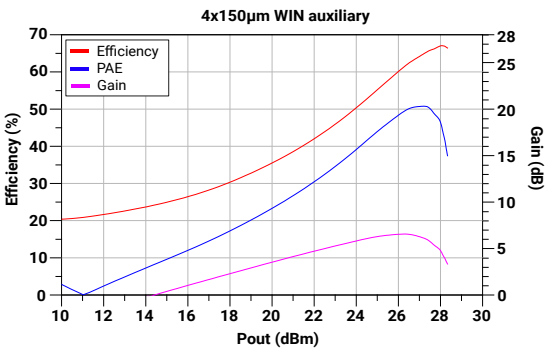

Figure 3.8: Auxiliary gain and efficiency vs Pout

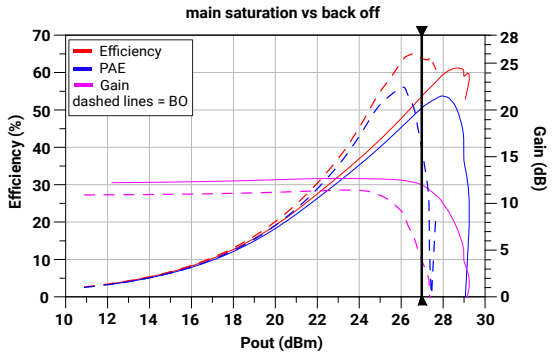

Figure 3.9: Main amplifier back-off vs saturation

The delivered output power is 27.2 dBm which is the minimum requested. This means that in a practical implementation, losses may cause the power to drop below the target value.
In Fig.3.9 it is shown that the amplifier maintains more or less the same performance when working in BO.

UMS

For UMS, since the technology offers higher power density, it is possible to select the load to maximize efficiency. The output power delivered is 28.2 dBm which is more than enough even when considering losses. The values of the input and output loads are in table 3.3.

	Z_S	Z_L
main	$6.394 + j15.855\,\Omega$	$20.247 + j8.34\,\Omega$
auxiliary	$10.403 + j12.078\,\Omega$	$17.521 + j12.276\,\Omega$

Table 3.3: Optimum load UMS

The load seen at the intrinsic drain is real for both the main and the auxiliary ($28\,\Omega$).
The optimum load for the main in BO is:
$Z_{load} = 27.35 + j22\,\Omega$
With this load the main maintains its performance also in BO as shown in Fig.3.12.

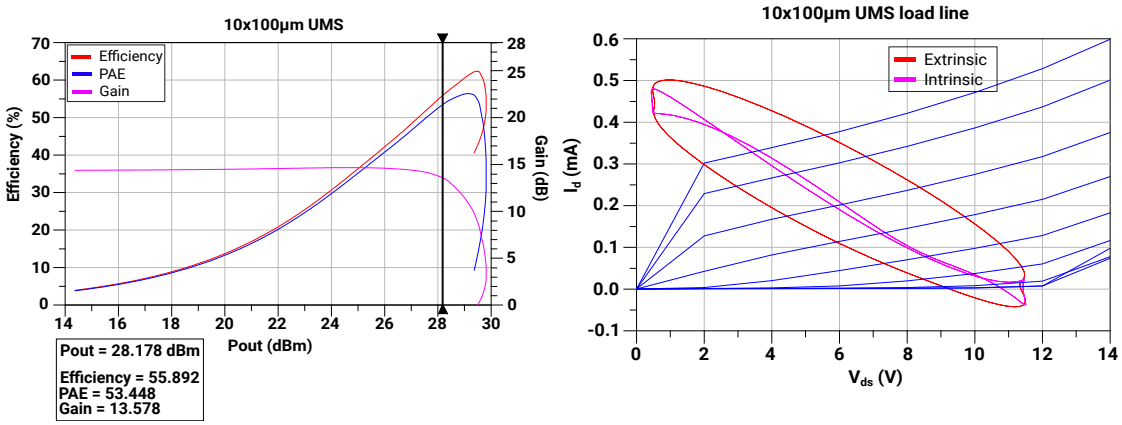

Figure 3.10: Main amplifier gain and efficiency vs Pout (right); Load lines (left)

With the UMS device the gain is 13.57 dB which is almost 2 dB higher than WIN. Efficiency values are comparable between the two technologies but UMS reaches higher output power. So far the results obtained are in line with the previous analysis in Chapter 2.

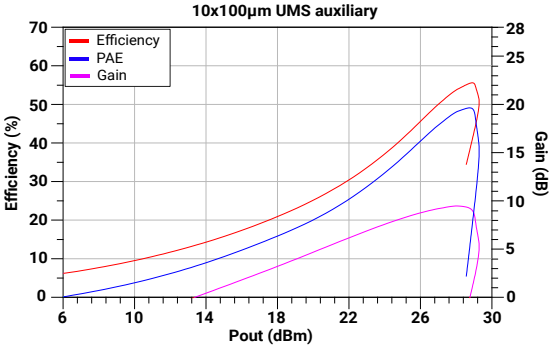

Figure 3.11: Auxiliary gain and efficiency vs Pout

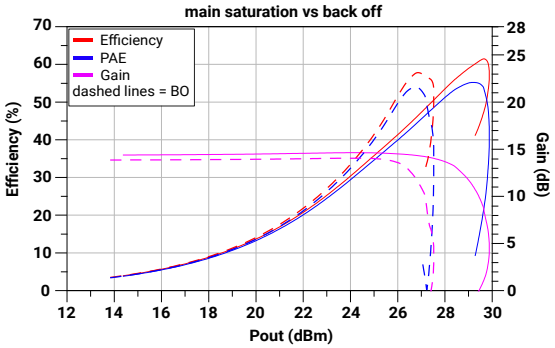

Figure 3.12: Main amplifier back-off vs saturation

3.2 Parasitic Compensation

After choosing the optimum loads the next step is to compensate for the parasitic effects of the transistor. This ensure that the impedance at the drain is real so that the combiner can modulate the load from $2R_{\text{opt}}$ to R_{opt}. The parasitics of the transistor are modeled as a series inductance L_{s} and a shunt capacitor C_{p} and resistor R_{p} as shown in Fig.3.13.

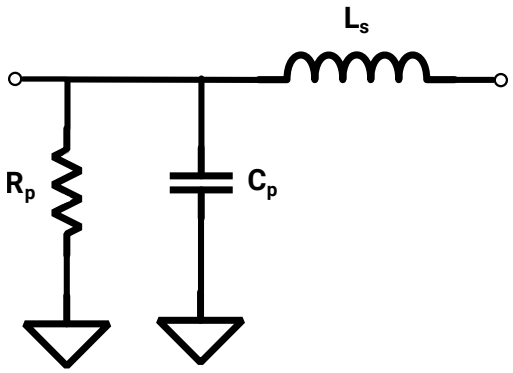

Figure 3.13: Parasitics model

To determine the values of the elements it is sufficient to run an S-parameter simulation when the transistor is off so that the results are influenced only by the device's parasitics. After this step, the values of the model elements can be optimized to replicate the parasitic behavior of the transistor, at least within the (8–12)GHz band. In Fig.3.14 is shown that the model is quite close to the actual parasitics.
Since the goal is to compensate for these parasitics, it is then possible to repeat the S-parameter simulation using a model in which the parasitics found are replaced by

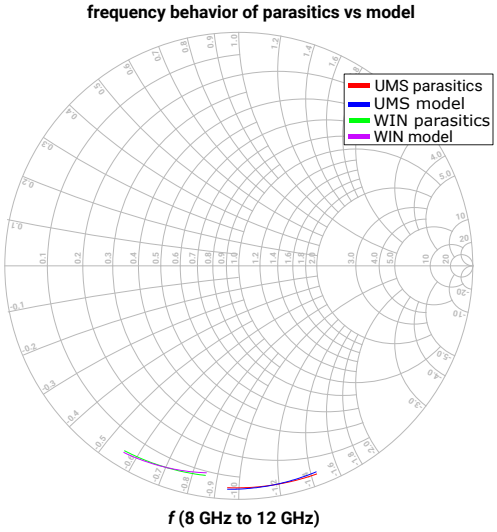

Figure 3.14: Frequency behavior of parasitics vs model

their negated values. The goal is to find a real component, in this case an inductor, that has the same behavior of the negated parasitics in order to compensate for them in the actual circuit. This inductor is placed after the transistor between drain and ground. Fig.3.15 shows that the compensating inductor well reproduces the behavior of the negated parasitics.

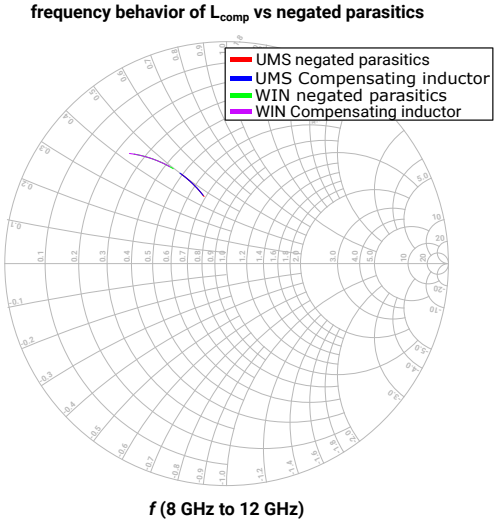

Figure 3.15: Frequency behavior of L_{comp} vs negated parasitics

The values found for the parasitics model and for the compensating inductor are reported in Table 3.4.

	R_p	C_p	L_s	L_{comp}
WIN	405.652 Ω	0.454391 pF	0.014602 nH	0.564135 nH
UMS	1156.38 Ω	0.273213 pF	0.012283 nH	0.965809 nH

Table 3.4: Values of parasitics

3.3 Combiner

As mentioned in Chapter 1, the goal of the combiner is to modulate the load so that the device always sees the optimum load for different levels of input power in order to keep the efficiency high and constant also in BO.
The implemented topology is the simplest combiner with the $\lambda/4$ impedance inverter. With (1.6) it is possible to compute the characteristic impedance of the $\lambda/4$ which is 14 Ω for WIN and 23 Ω for UMS.

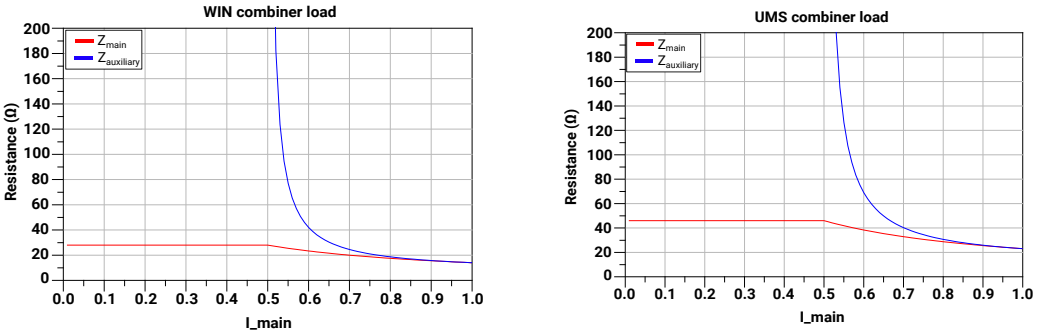

Figure 3.16: Load modulation WIN (left) UMS (right)

At this point it is possible to perform the first simulations of the Doherty using a dual input topology (Fig.3.17) since the splitter has not been designed yet at this stage.

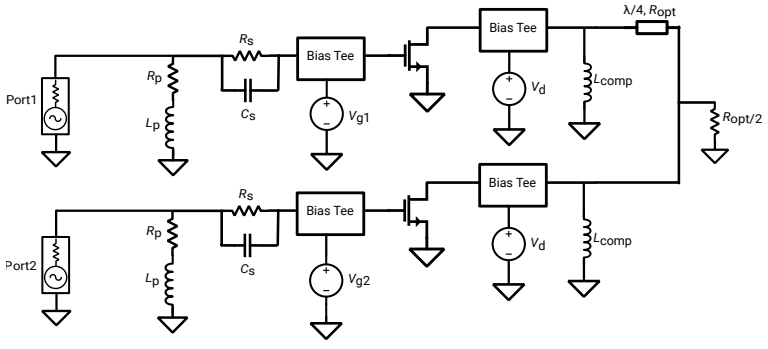

Figure 3.17: Doherty with dual input schematic

To ensure proper operation the signal that comes from the input port of the auxiliary branch needs to be shifted by 90° to compensate for the phase shift introduced in the main branch with the $\lambda/4$. The simulation was performed at 10 GHz.

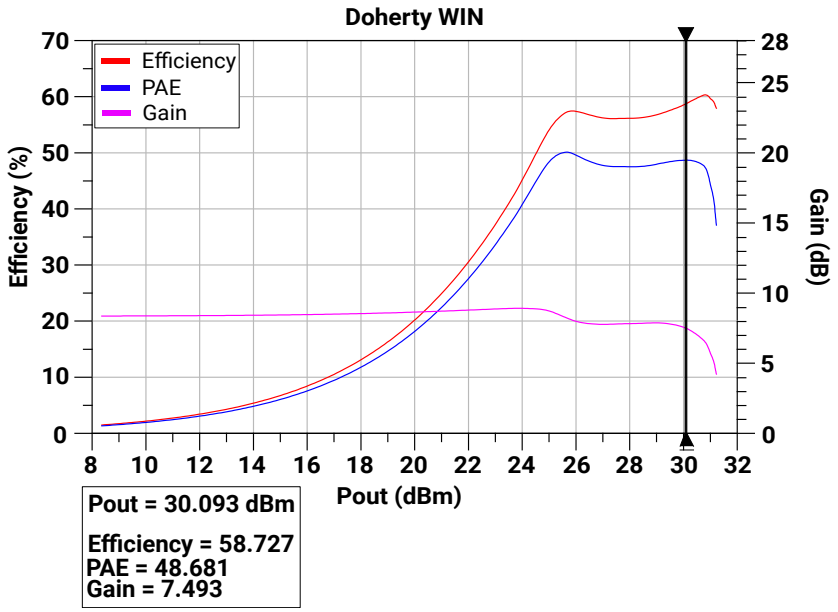

Figure 3.18: WIN Doherty at 10 GHz

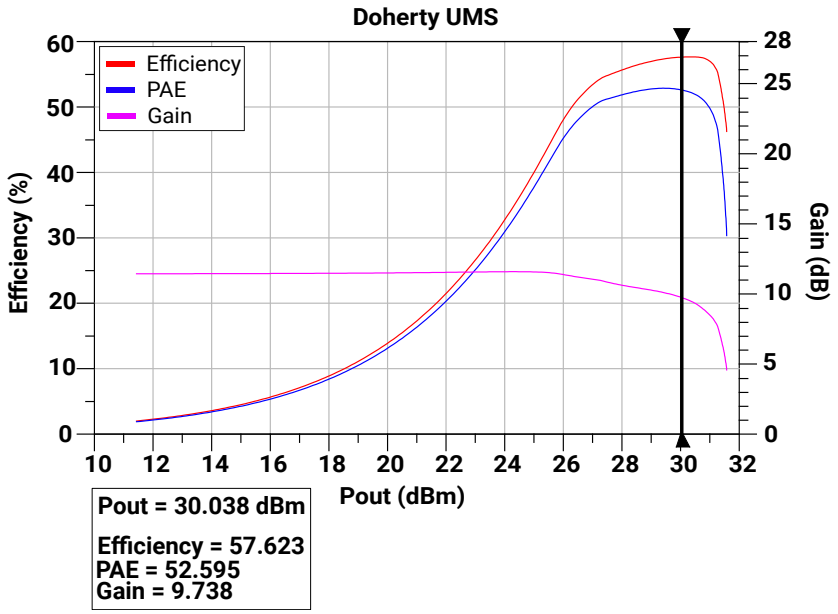

Figure 3.19: UMS Doherty at 10 GHz

Fig.3.18 and Fig.3.19 show the performance of the two DPAs. Both amplifiers work in the target 30 dBm region but UMS demonstrates a slightly higher output power, making it more suitable for applications where maximizing output power is critical. The gain is also higher in the UMS case (9.7 dB vs 7.4 dB) as expected after the analysis in Chapter 2. The WIN DPA, on the other hand, is better in back-off because the Doherty region where efficiency and PAE remain high is a bit wider compared to the UMS amplifier. This advantage can be beneficial in modern applications with high PAPR signals.
To be sure that the DPAs are working as intended we can check the load modulation and the currents of the two branches.

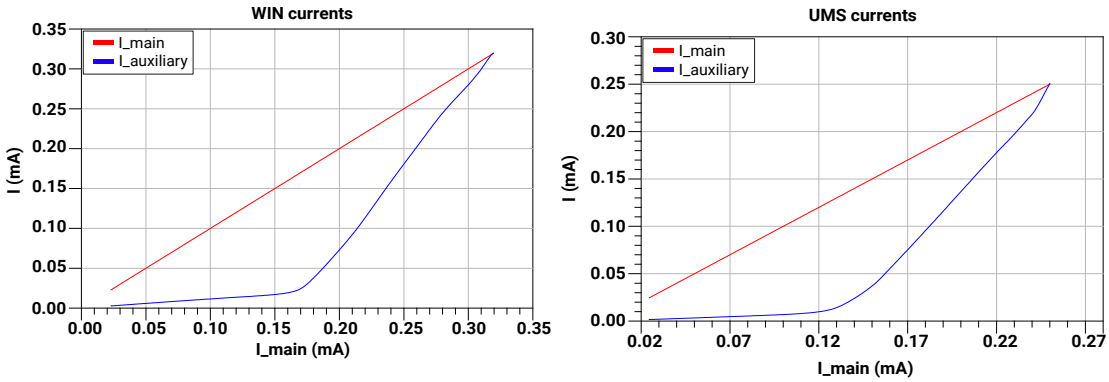

Figure 3.20: Main and auxiliary currents

At the beginning of operation the auxiliary should be off but in WIN case a small current is still present for low levels of the input signal (Fig.3.20). This behavior is likely due to technology-related factors such as leakage current or an imperfect off state. As shown in Fig.3.21 the main impedances are real and have the correct values. The impedance seen by the auxiliary should ideally be an open before saturation. In UMS case this impedance is very high, while in WIN case it is low and not comparable to an open circuit. This is probably the reason why the device is not completely turned off at the start.

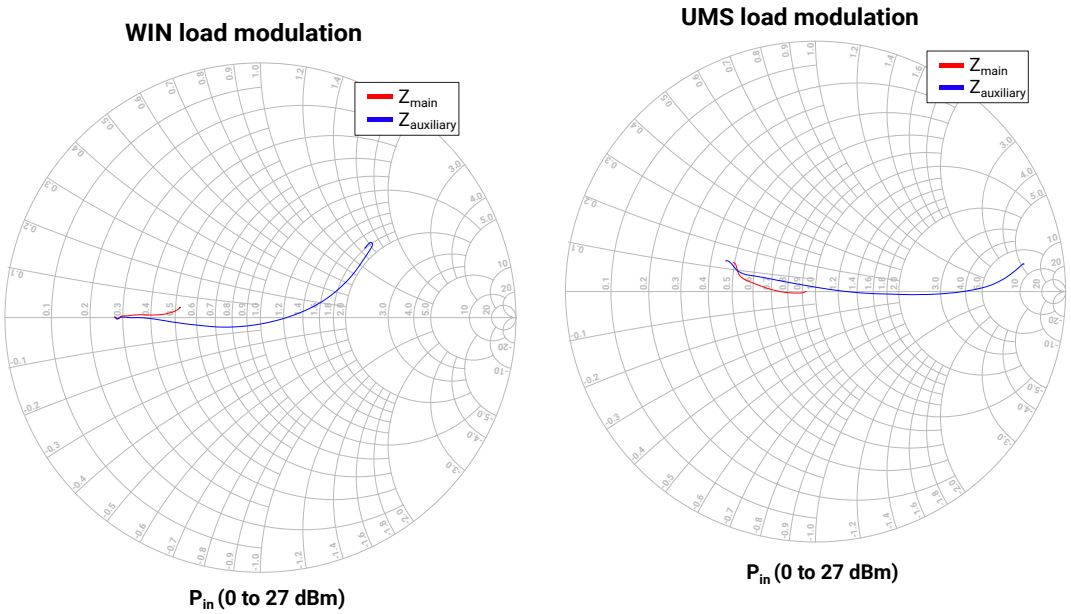

Figure 3.21: Load modulation WIN (left) UMS (right) at the intrinsic drain node

3.4 Splitter

In a DPA configuration the input power must be split between the main and auxiliary amplifiers. In this case a 3 dB branchline coupler is used as a splitter (Fig.3.22).

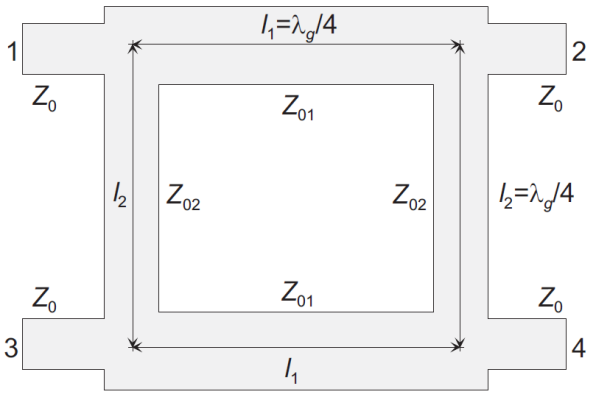

Figure 3.22: Branchline coupler[1]

This splitter also ensures a 90° phase difference between the output ports that compensates for the shift introduced by the $\lambda/4$ in the main branch.
The input signal is connected to port 1 while ports 2 and 4 deliver equal amplitude signal to the main and auxiliary branches. Port 3 is ideally isolated and terminated with 50 Ω.
All transmission lines used are $\lambda/4$ and the characteristic impedances can be computed with the following formulas. For a 3 dB coupler the values are:

$$Z_{02} = Z_0 \tag{3.2}$$

$$Z_{01} = \frac{Z_0}{\sqrt{(2)}} \tag{3.3}$$

Z_0 is the reference impedance that in this case is 50 Ω. To be sure that the splitter is working as intended it is necessary to terminate all the ports with 50 Ω so input matching networks are required to match ports 2 and 4. Fig.3.23 shows the transmission coefficients S_{21} and S_{41} and the phase shift between the ports.

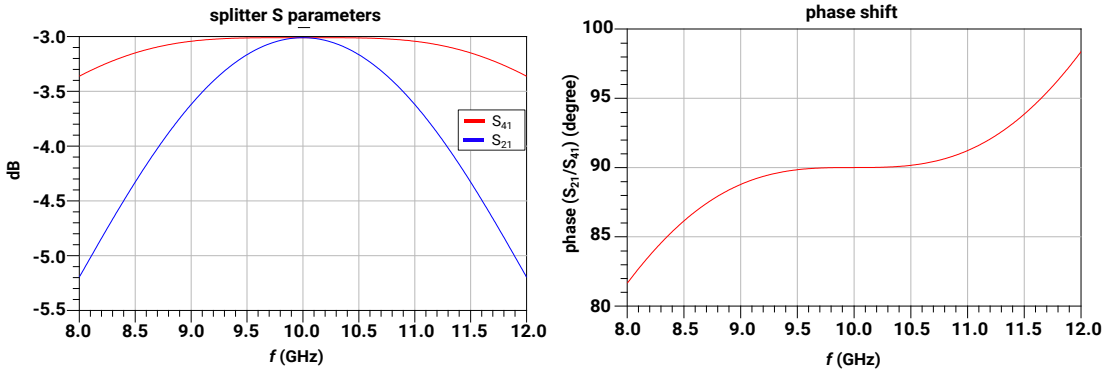

Figure 3.23: Split ratio and phase shift

The bandwidth of this coupler is narrow, so the split ratio is accurate only around the center frequency. To address this limitation in Chapter 4 another splitter topology will be analyzed.

3.5 Matching Networks

3.5.1 Input Matching Section

The input matching network is placed after the splitter but before the amplifier. The goal is to transform the optimum input impedance of the transistor into 50 Ω,

which is the reference impedance of the splitter. A section of the matching network is shown in Fig.3.24.

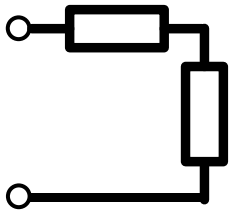

Figure 3.24: Matching section

A single section is not enough to cover a 4 GHz bandwidth so four sections are used. The goal is to achieve a −20 dB matching within the band of interest and also to maintain the correct phase shift between the main and auxiliary branches. An additional line is added in the auxiliary branch in case it is necessary to compensate for the phase shift introduced by the two matching networks.

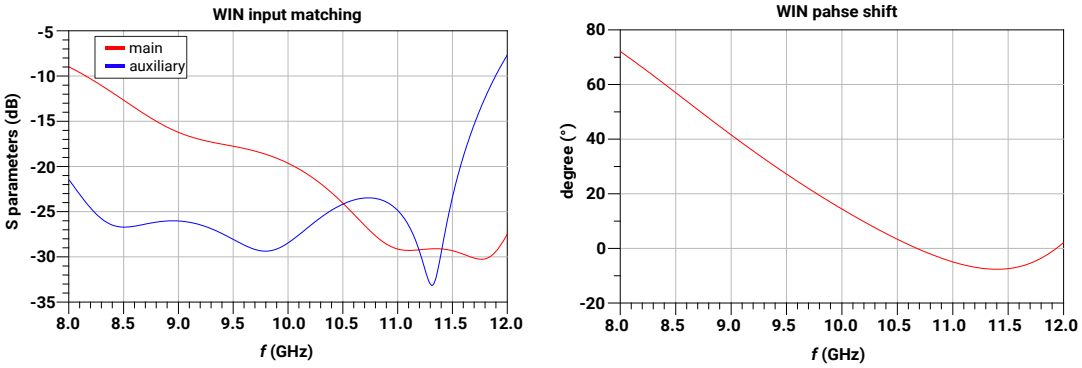

Figure 3.25: WIN matching and phase shift between main and auxiliary networks

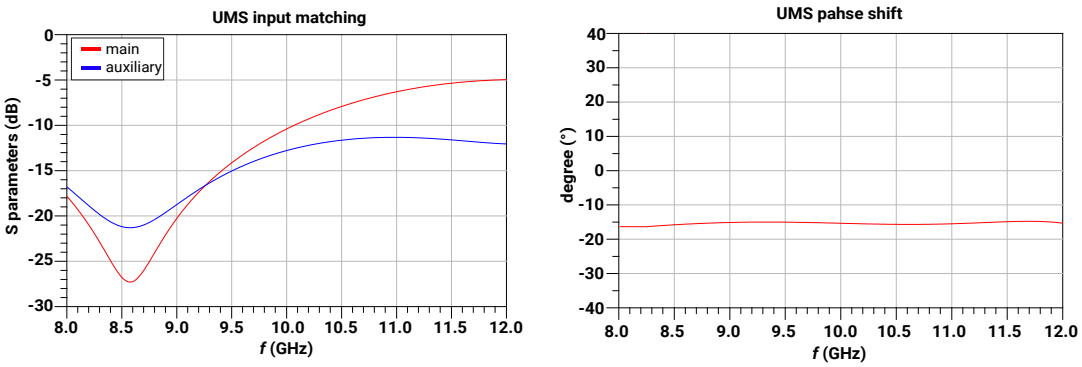

Figure 3.26: UMS matching and phase shift between main and auxiliary networks

Fig.3.25 and Fig.3.26 show the input matching in the 4 GHz bandwidth. The phase shift between the main and the auxiliary networks is close to zero in UMS case while in WIN case this is true only in the higher part of the band. As a consequence, a performance loss is expected at lower frequencies.
It was not possible to achieve a constant −20 dB matching across the band while also trying to minimize the phase difference.

3.5.2 Output Matching Section

The output matching is placed after the combiner and it is necessary to match the amplifier to the 50 Ω output port. Since the load after the combiner is already real, a simple $\lambda/4$ transformer can be used to match it to 50 Ω. However, to achieve broadband matching, three sections are implemented. Instead of optimizing the network to achieve the best matching, it was optimized together with the combiner to ensure that the load modulation is correct in the whole frequency band.

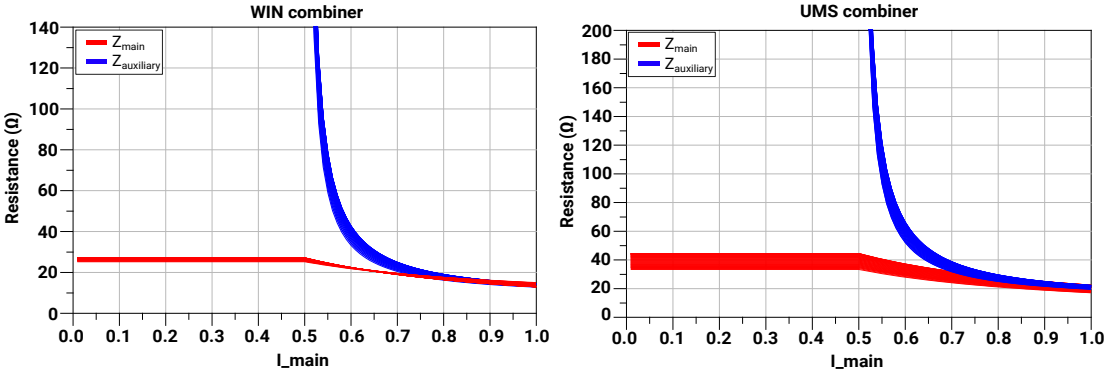

Figure 3.27: Load modulation (8-12) GHz

The values obtained in saturation are around 24 Ω for UMS and around 13 Ω for WIN, which are very close to the desired values. Even though these values slightly change with frequency, the overall load modulation results are quite satisfactory especially if we consider the large bandwidth.

3.6 Performances of the Final Ideal Circuit

Now that all the different building blocks have been designed, it is possible to simulate the complete circuit (Fig.3.28).

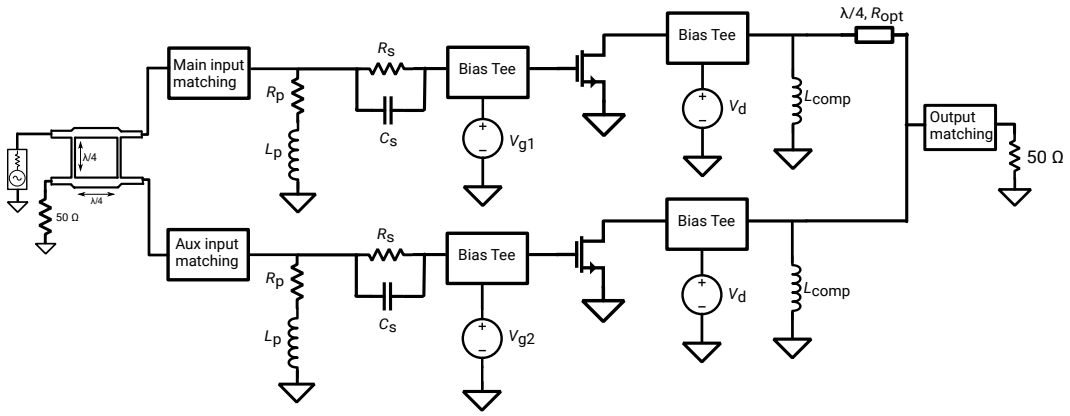

Figure 3.28: Complete schematic of the ideal circuit

The first simulation is at 10 GHz which is the center frequency. In Fig.3.29 is shown the comparison between the two DPAs.

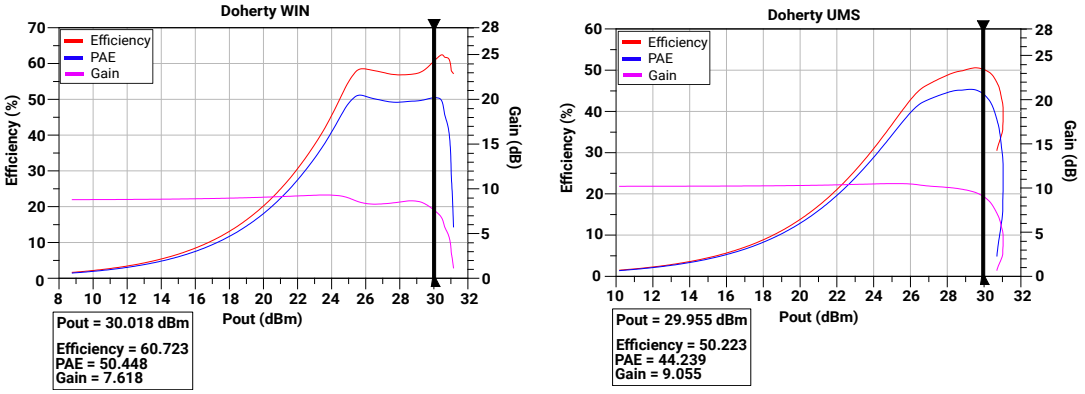

Figure 3.29: Performance of the ideal Doherty

As already underlined by the simulations in section 3.3 the UMS Doherty has higher gain (9 dB vs 7.6 dB). The Doherty region is wider for the WIN process and its efficiency is also higher.
To understand if the two amplifiers are actually able to cover the (8-12) GHz band, we can look at Fig.3.30 where the previous simulation is repeated adding also a frequency sweep.

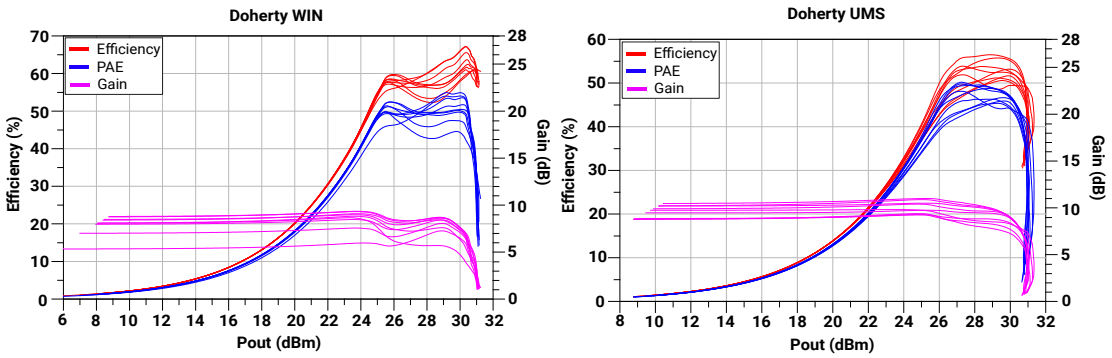

Figure 3.30: Performance of the two Doherty in the (8-12) GHz band

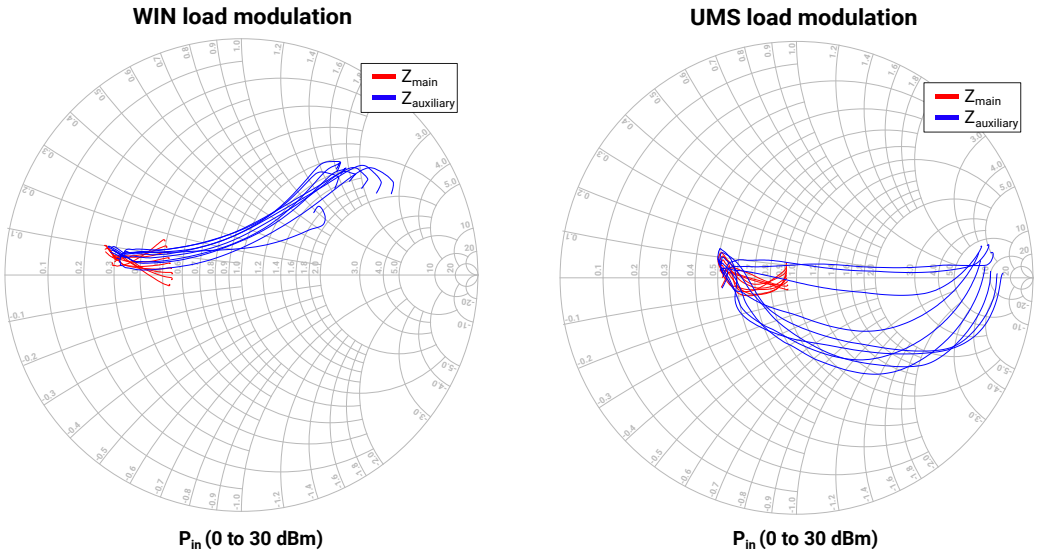

Figure 3.31: Load modulation at the intrinsic node vs frequency

The simulations show that the two amplifiers can operate within the entire band while maintaining good performances.
The WIN amplifier shows some gain issues after 11 GHz, probably due to a not perfect input matching. The input network was designed to synthesize the optimum input impedance at 10 GHz, which is different to the optimum at different frequencies. The splitter is also not working in its best condition at the edges of the frequency interval.
It is also important to remember that all components used so far are ideal, so the performances will deteriorate when switching to real ones. In the next chapter, the changes made to achieve a good broadband design and to address the chip's space limitations will be discussed. Some blocks will be entirely redesigned to deal with these space constraints.

Chapter 4

Real Circuit Implementation

4.1 Real Bias Network

Up to this point, the bias circuit used was ideal and consisted of a series capacitor and a shunt inductor. The purpose of this network is to separate the DC from the RF. The capacitor acts as an open circuit for DC, so it is used to block the DC from reaching the output of the circuit or the input ports. The inductor, on the other hand, behaves as an open circuit at RF so it blocks the RF signals from reaching the bias section.
In a real implementation the behavior of the inductor is affected by parasitic effects so it can no longer block the RF signals effectively.

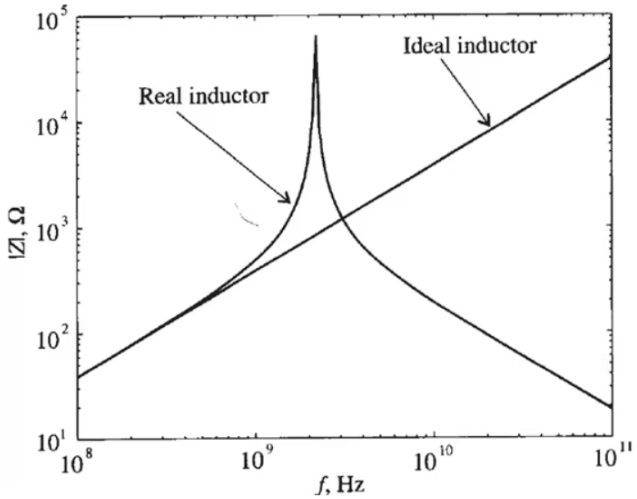

Figure 4.1: Frequency response of the impedance of a real inductor[6]

This occurs because the inductor acts like a parallel LC circuit, which presents maximum impedance at resonance but behaves like a capacitor at frequencies above

the resonance frequency. To overcome this problem, it is possible to add a capacitor, as shown in Fig.4.2, to provide the RF signal with a path to ground.

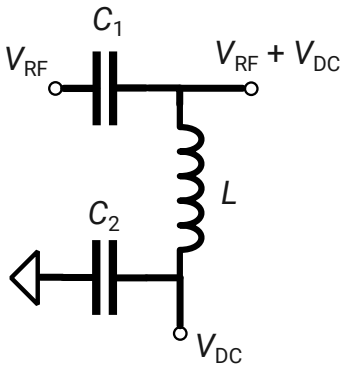

Figure 4.2: Schematic of the bias tee

The dimensions of the capacitor C_2 are 67 µm x 67 µm. In Fig.4.4 is shown that with these dimensions the capacitor acts as a short in the (8-12) GHz range.

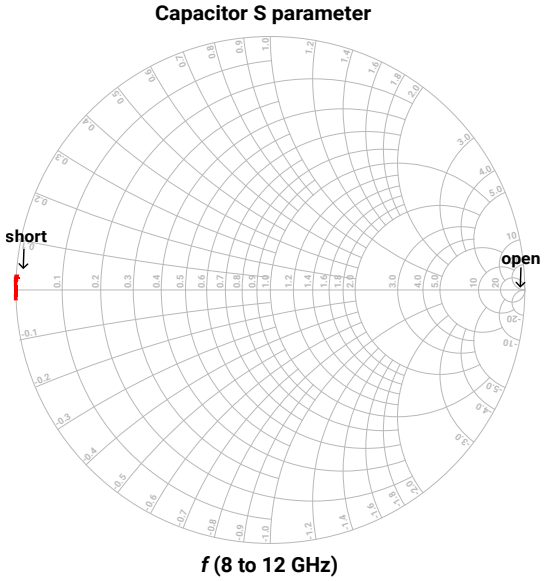

Figure 4.3: S parameters of the capacitor used as RF block

Since the two capacitors already block the DC and RF, it is possible to integrate the inductor used to compensate for parasitics directly into the drain bias circuit. When designing the inductor, the DC current that flows through it must be considered. The maximum DC current is 300 µA that corresponds to a minimum width of 30 µm with WIN technology. Table 4.1 reports all the dimensions used for the elements in the drain bias circuit.

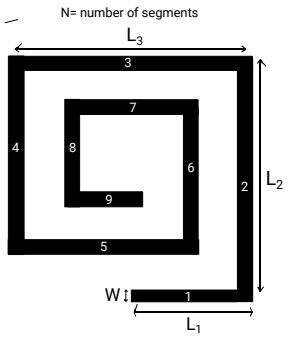

Figure 4.4: Inductor geometry in WIN technology

	W	L_1	L_2	L_3	N
C_1	67 µm	67 µm			
C_2	67 µm	67 µm			
L	35 µm	20 µm	190.11 µm	474.64 µm	6

Table 4.1: Values for the drain bias circuit

4.2 Real Stabilization Network

The input bias is integrated into the stabilization network. As stated in section 4.1, the inductor is no longer used to block the RF and can instead be optimized as part of the stabilization network. In Fig.4.5 is shown how the stabilization network changes with the addition of the gate bias.

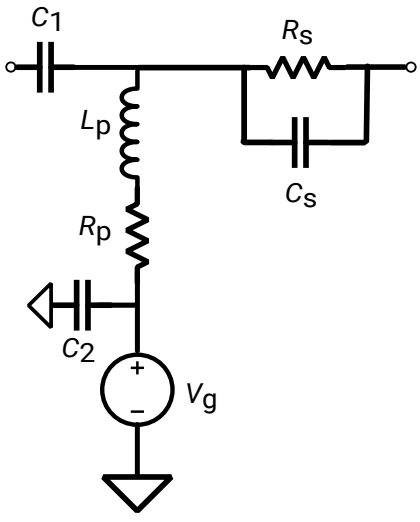

Figure 4.5: Schematic of the bias tee

The initial approach was to use real components with the exact values of the ideal counterparts. However, this resulted in instability in the (8-12) GHz frequency band due to the non idealities of real components. Therefore, all components were manually tuned to ensure stability and the final values are reported in Table 4.2

	W	L_1	L_2	L_3	N
R_p	349.901 µm	6.35713 µm			
R_s	500 µm	73.5093 µm			
C_s	7 µm	86.082 µm			
L_p	35 µm	20 µm	250 µm	250 µm	6
C_1	67 µm	67 µm			
C_2	67 µm	67 µm			

Table 4.2: Values for the drain bias circuit

The amplifier should also be stabilized outside the bandwidth especially at lower frequencies. Analyzing the μ parameter in Fig.4.6 we can see that the device remains stable from 0 GHz to 13 GHz. The gain after stabilization is (12 $\pm$ 0.7) dB, therefore the final circuit maintains a stable gain across the entire bandwidth.

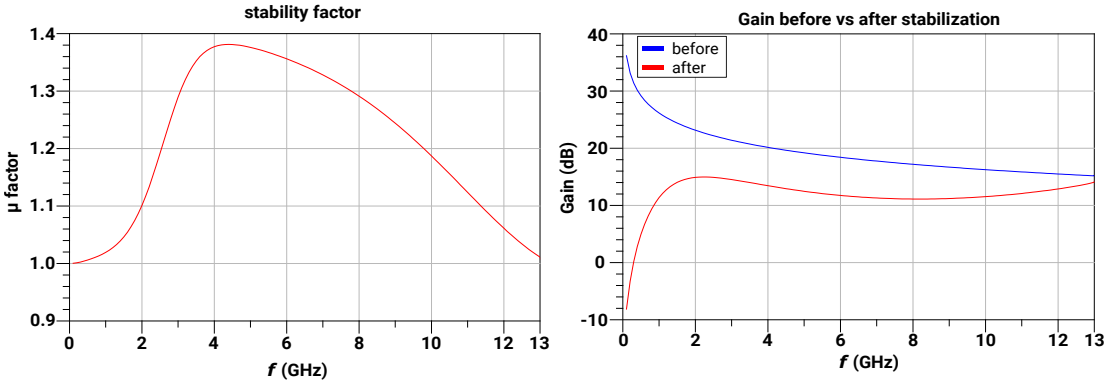

Figure 4.6: μ factor and maximum gain after the stabilization

4.3 Real Combiner

The combiner is one of the parts that changed the most after the real implementation since the ideal topology used in Chapter 3 can modulate the load only in a small

range of frequency around 10 GHz and now a new topology is needed to have the correct modulation in a 4 GHz bandwidth.

The ideal version of the combiner uses four $\lambda/4$ sections, one for the main branch and three to match the 50 Ω output port.
All lines in the ideal topology has lengths of approximately 2.3 mm, which in a (3.5 x 3.5) mm^2 chip means that the lines need to be bent to fit. Moreover, the characteristic impedances of the lines are small, resulting in wide lines that are difficult to bend in a limited space. For these reasons, the combiner topology was replaced with a more suitable one, as shown in Fig.4.7.

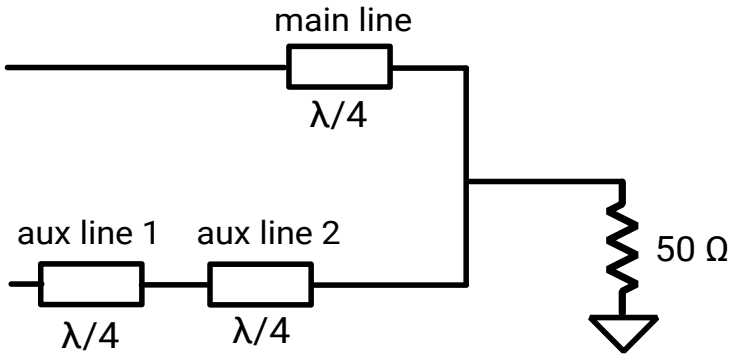

Figure 4.7: Schematic of the combiner

All the theory, design details and equations for the new combiner can be found in [7].
The advantages of this topology include:

- Only three lines are used instead of four

- Higher characteristic impedances (ex. 27 Ω vs 10 Ω for the main line), resulting in narrower lines

The results obtained with this combiner in terms of load modulation are shown in Fig.4.8.
Even with this new configuration, the modulation is not perfect since the impedance values at the edges of the frequency range deviate from the reference values, which are 20 Ω in back-off and 10 Ω at saturation.
To obtain a feasible design a maximum line width of 170 µm was imposed, which made it more difficult to achieve good load modulation across the 4 GHz bandwidth.

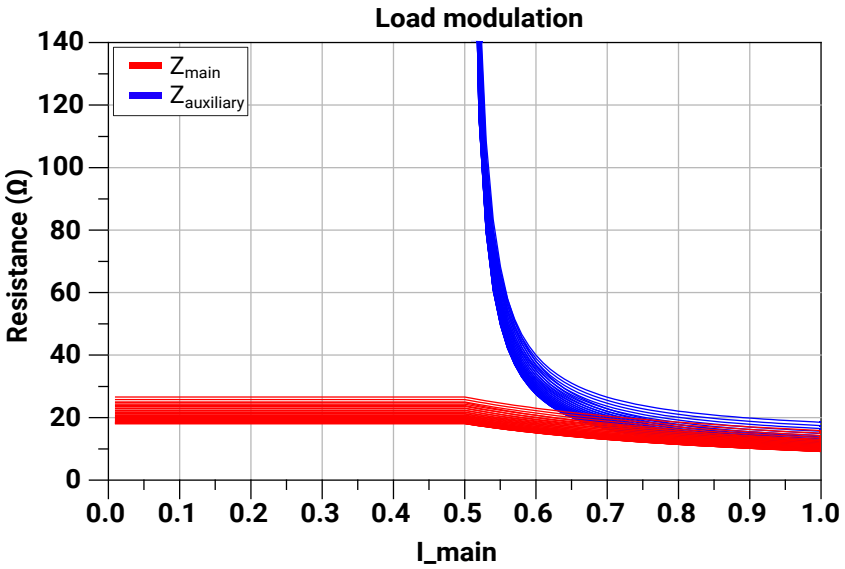

Figure 4.8: Load modulation with real combiner at the intrinsic node (8-12) GHz

By narrowing the frequency range to (8.5-11.5)GHz the impedance values are closer to the desired ones.

In Fig.4.9 is shown the new simulation with the restricted frequency range and it can be observed that there is less fluctuation of the impedances when frequency changes.

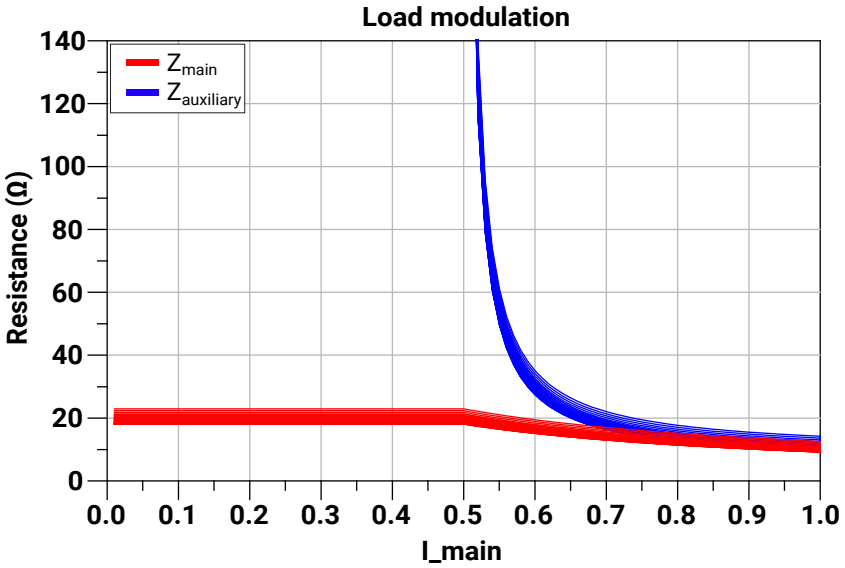

Figure 4.9: Load modulation with real combiner at the intrinsic node (8.5-11.5) GHz

In Table 4.3 are listed the dimensions of the combiner lines.

	W	L
main line	170 µm	2200.9 µm
auxiliary line 1	170 µm	2248.61 µm
auxiliary line 2	6.1 µm	2747.62 µm

Table 4.3: Dimensions of the combiner lines

4.4 Splitter

The branchline coupler used in Chapter 3 was unable to equally divide the input power between the main and the auxiliary branches in the entire frequency range of interest. To overcome this problem a new coupler topology was adopted.

4.4.1 Lange Coupler

The Lange coupler, presented for the first time in 1969 by Julius Lange [8], is the topology implemented in this work (structure shown in Fig.4.10).

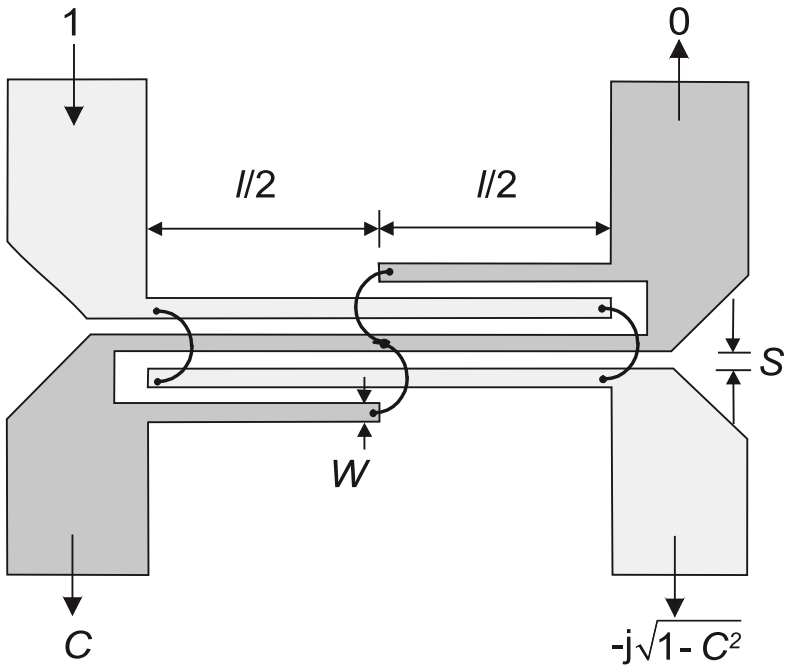

Figure 4.10: Structure of a folded Lange coupler

The main advantages over branchline couplers are:

- Reduced losses
- Wider bandwidth
- More compact layout, making it a good solution when space limitations are important

This coupler also provides a 90° phase shift just like the branchline coupler. The design formulas can be found in [1] but in this case a Lange coupler was already present in the design kit provided by WIN.
The component provided was optimized to achieve a −3 dB coupling factor in the (8-12)GHz frequency band. Table 4.4 reports the coupler parameters.

Parameter	Dimension
W	8.6 µm
S	10 µm
L	2479.78 µm
BW	59.2 µm

Table 4.4: Values for the splitter parameters

In Fig.4.11 and Fig.4.12 is shown the comparison between the Lange coupler and branchline topologies.

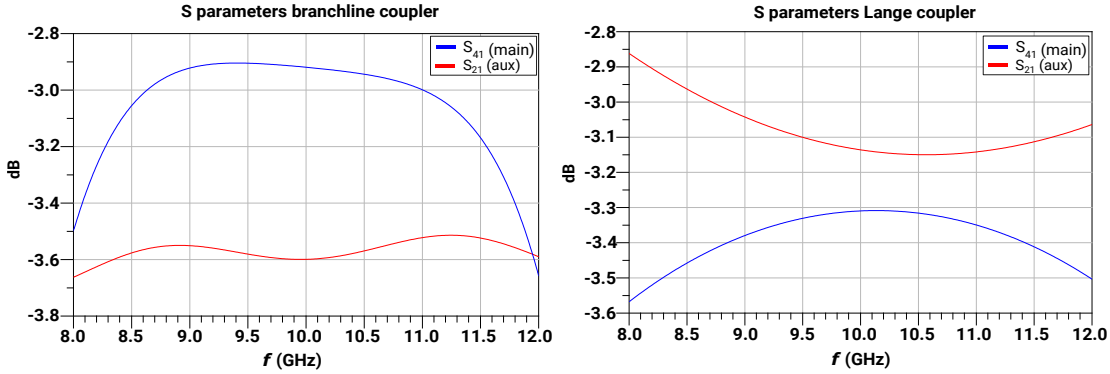

Figure 4.11: Split ratio Branchline(left), Lange(right)

In the new version, the split ratio is closer to −3 dB and also shows less fluctuation inside the bandwidth.
The phase shift between the two branches is also more constant with a maximum deviations of 1° respect to the desired 90°.
Furthermore, the dimensions of the coupler are compatible with the space constraints, unlike in the previous case where the coupler required wider lines.

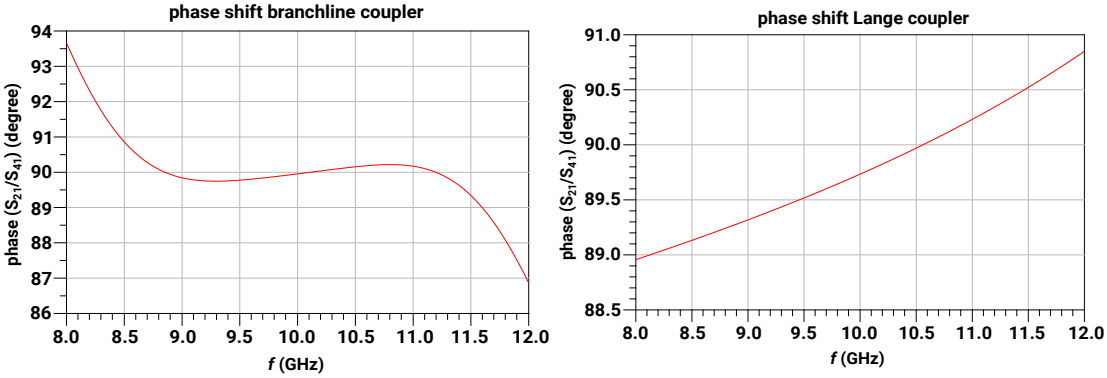

Figure 4.12: Phase shift Branchline(left), Lange(right)

4.5 Input Matching Network

The structure of the input matching network is the same of the one described in 3.5.1.
To reduce the occupied space, in this case only two sections are used for both the main and auxiliary branches instead of four.
The goal is to achieve a matching of at least $-10\,\text{dB}$ in the (8-12) GHz bandwidth while keeping the amplifier gain as flat as possible. Since the frequency range is wide, it is not possible to obtain good results if the matching network is designed to synthesize the optimum impedance at the center frequency. The input impedance is frequency dependent, so to improve the matching, three different frequencies were selected with the respective optimum input impedances.
The matching network was optimized to synthesize the correct impedance for different frequency intervals.
Table 4.5 summarizes the frequencies chosen for the optimization and their corresponding impedances.

	Frequency point (GHz)	Frequency interval (GHz)	Optimum input impedance (Ω)
Main	8.5	(8-9.5)	$16.855 - j23.918$
	10	(9.5-10.5)	$7.741 - j17.129$
	11.5	(10.5-12)	$4.677 - j11.854$
Auxiliary	8.5	(8-9.5)	$22.97 - j30.958$
	10	(9.5-10.5)	$9.675 - j22.737$
	11.5	(10.5-12)	$5.720 - j15.654$

Table 4.5: Values for the optimum input impedances at different frequencies

Fig.4.13 shows that the matching networks achieve a minimum matching of −8 dB.

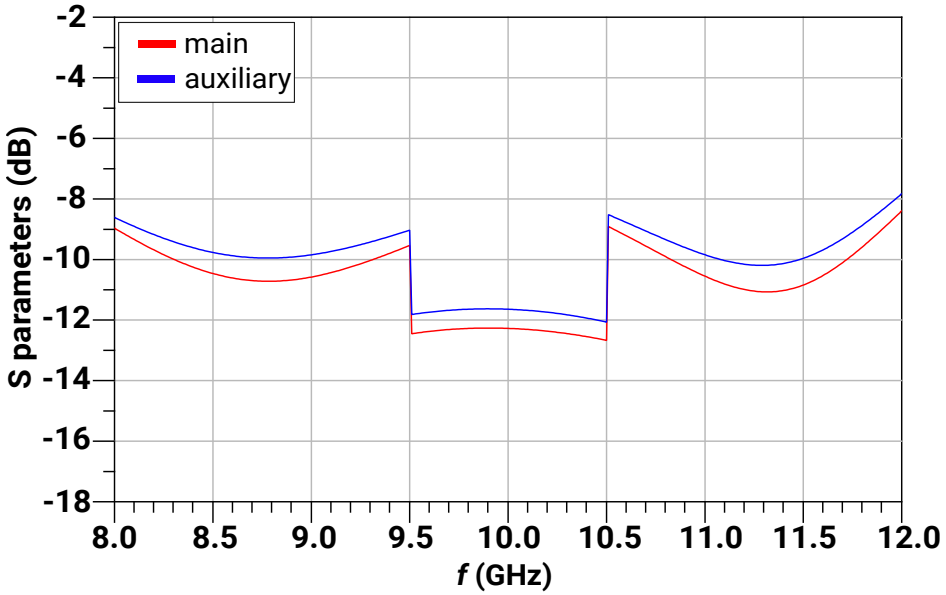

Figure 4.13: Input matching with network designed considering different target impedances at different frequencies

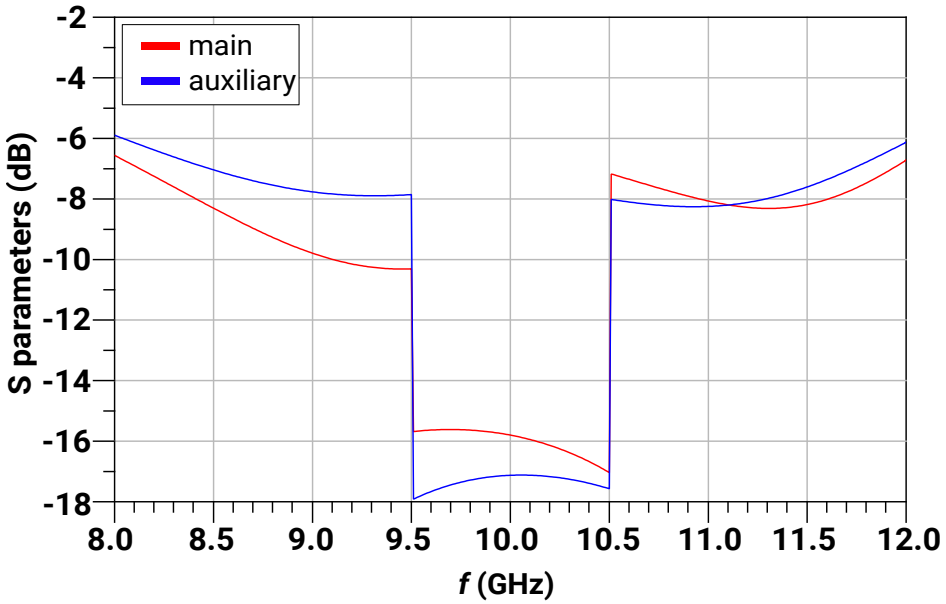

Figure 4.14: Input matching with network designed considering just the 10 GHz impedance

To understand how the matching improves using this approach, it is possible to look at Fig.4.14 where the matching networks are designed considering just the optimum input impedances at 10 GHz. The matching is better around the center frequency (−18 dB) but worse at the edges of the frequency intervals (−6 dB). Since the critical points are the edges of the frequency band, the results in Fig.4.13 are preferable even if there is a small performance deterioration at 10 GHz. The matching networks were also optimized to minimize the phase shift between the main and auxiliary branches. Fig.4.15 shows that the phase shift is close to 0°, which means that there is no need to add lines to compensate for the phase shift like it was done in Chapter 3.

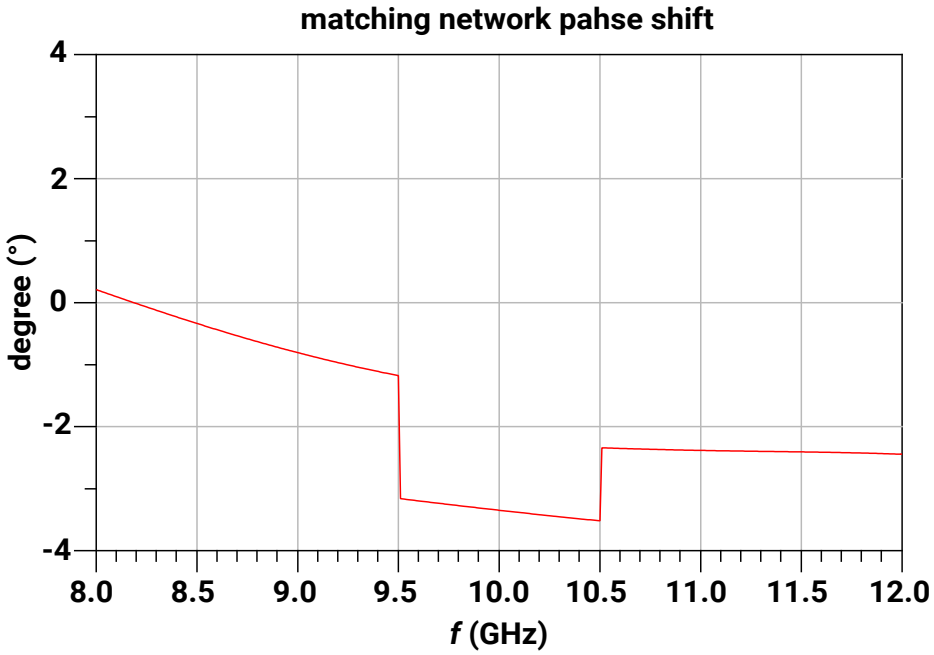

Figure 4.15: Phase shift between the main and auxiliary matching network

Table 4.6 and 4.7 list the widths and lengths of the matching network lines.

	W1	L1	W2	L2
main	190 µm	479.39 µm	190 µm	2999.9 µm
aux	190 µm	330.63 µm	190 µm	2999.9 µm

Table 4.6: Dimensions of the first section of the matching network

	W3	L3	W4	L4
main	33.51 µm	970.51 µm	21.63 µm	703.4 µm
aux	15.2 µm	937.44 µm	13.71 µm	886.9 µm

Table 4.7: Dimensions of the second section of the matching network

4.6 Final circuit simulations

In this section is analyzed the final performance of the circuit with only real components. Fig.4.16 compares the performance at 10 GHz between the ideal and the real circuit.

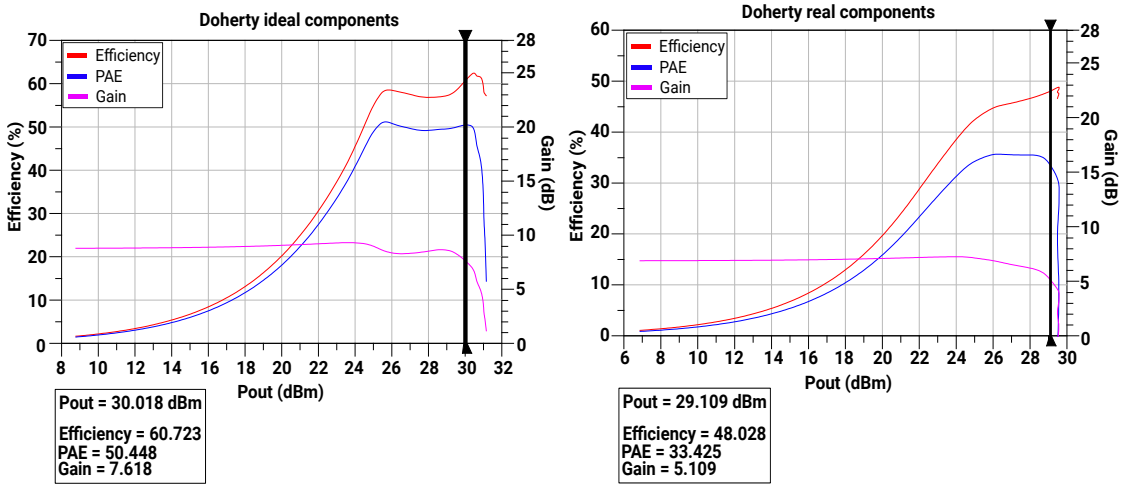

Figure 4.16: Simulation at 10 GHz; ideal circuit(left), real circuit(right)

In the real implementation, the maximum output power is 29.5 dBm, which is 1 dB lower respect to the ideal circuit. This output power drop is reasonable since now we are considering real microstrip lines with their losses instead of ideal transmission lines. The PAE and the gain also decrease like the output power but we still have a 5 dB OBO region where the PAE remains constant above 32%.
The performance are worse when considering the full (8-12) GHz bandwidth mainly due to the fact that the combiner is not able to modulate the load correctly in the whole frequency band.
Therefore the frequency range considered in the following simulations is limited to (8.5-11.5) GHz. The small signal gain (Fig.4.17) is around 6 dB with a variation of 1 dB over the bandwidth. To boost the gain, which is currently very low, a driver stage could be added in the future. The PAE is not constant over the bandwidth but it is still higher than 20%.

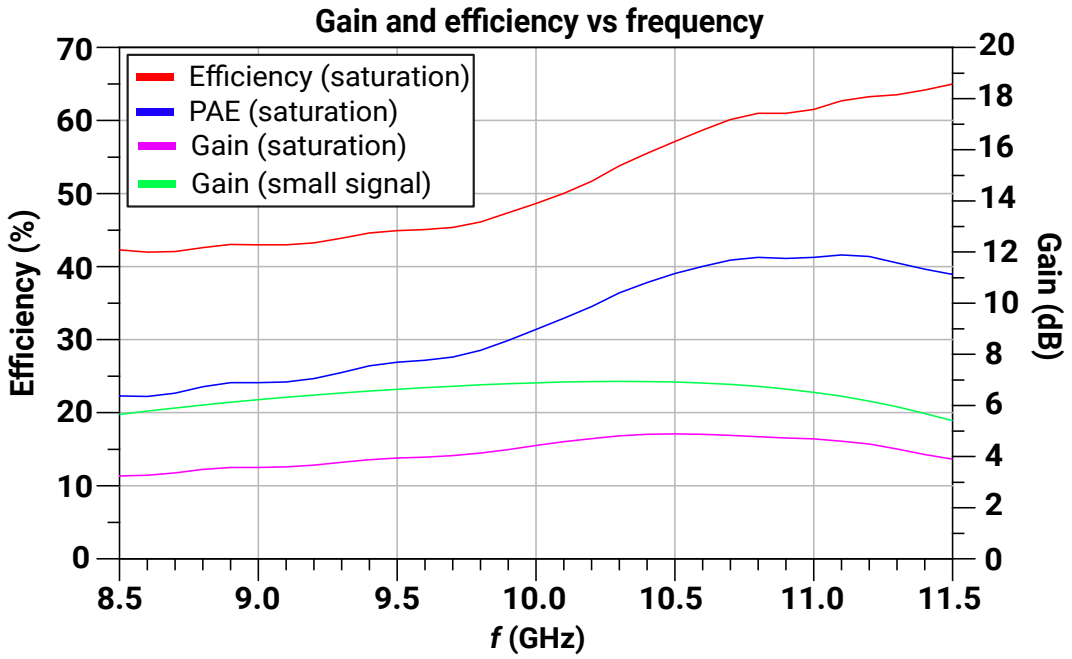

Figure 4.17: Gain, PAE and drain efficiency changes versus frequency

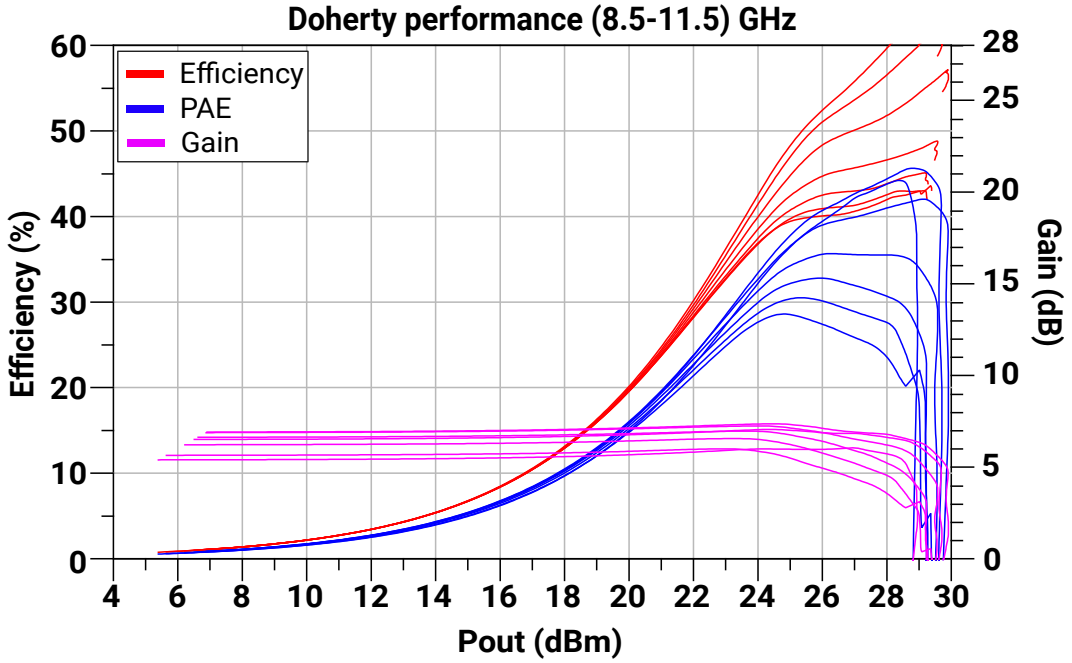

Figure 4.18: Simulation of the real Doherty in the (8.5-11.5) GHz frequency range

In summary the goal was to design a 1 W DPA that could cover the frequency band (8-12) GHz.
This work did not have precise specifications in terms of gain or efficiency since it was an exploratory study to evaluate the best achievable performance using the selected technology. Table 4.8 reports the overall performance of the designed DPA.

frequency band covered	OBO region	drain efficiency	PAE	gain(small signal)	gain(sat)
(8.5-11.5) GHz	5 dB (24-29) dBm	$> 40\%$	$> 20\%$	6 dB	4 dB

Table 4.8: Overall performance of the Doherty

Chapter 5

Final Considerations and future work

The final step is to translate the designed DPA into a layout that can be manufactured. Currently the final layout is still incomplete but in Fig.5.1 is shown the layout of the output part with the combiner.

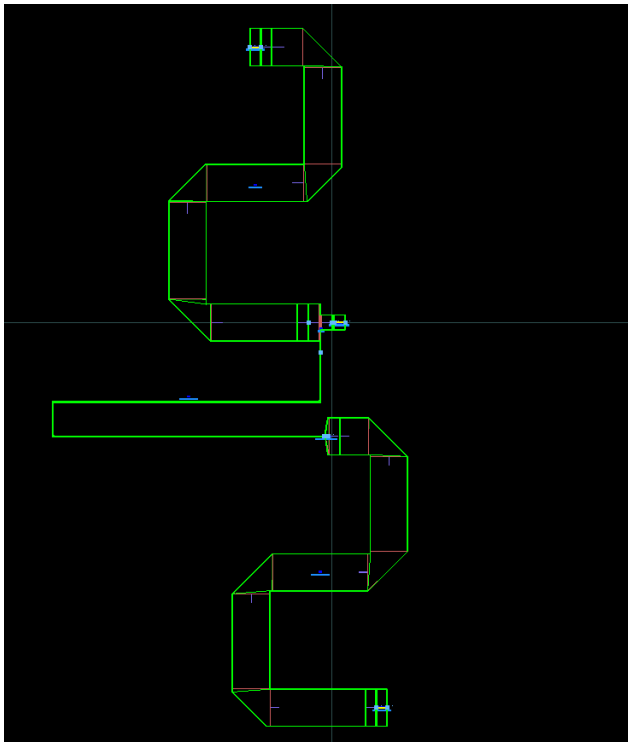

Figure 5.1: Layout of the combiner

The combiner lines are bent to fit in the chip area and MTEE components are used when three lines with different widths need to be connected. The initial auto-generated layout was optimized to match the performance of the previous schematic simulations. Since the lines differ significantly in width, the most problematic element was the junction between them.
In Fig.5.2 is shown the comparison between the S parameters obtained with the electromagnetic (EM) simulations of the combiner and the ones from the schematic simulations.
The layout S parameters match quite well the schematic in the whole frequency band.

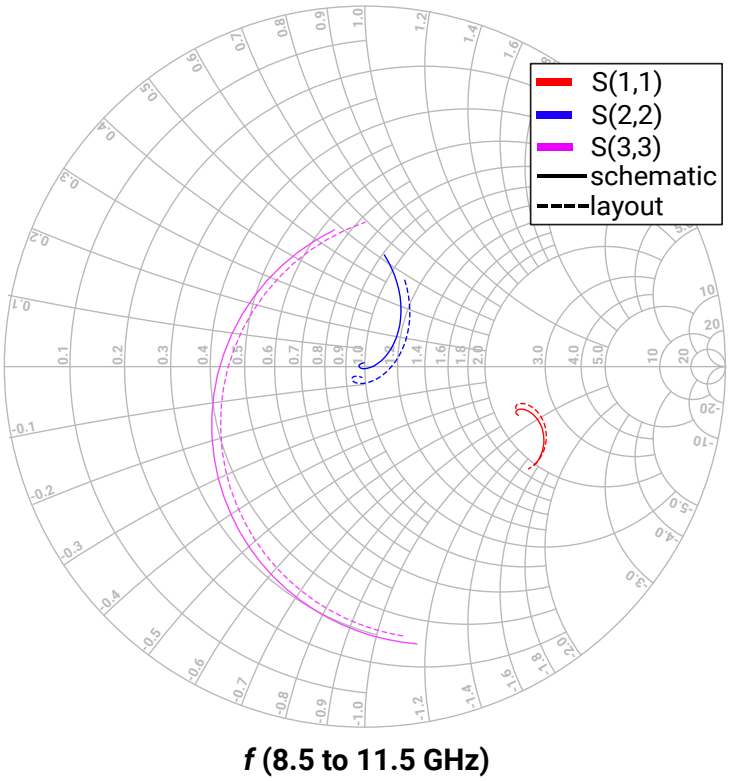

Figure 5.2: S parameters of the combiner (layout vs schematic)

It is now possible to replace the combiner in the Doherty schematic with the layout block that was simulated to verify if there are any changes in the performance of the final circuit.
Fig.5.3 shows the final simulation and comparing the result with Fig.4.18 we can notice that there are no significant changes in the performance.
The layout will be completed in the future when probably also two drivers will be added (one for each branch) to improve the gain, that is currently very low.

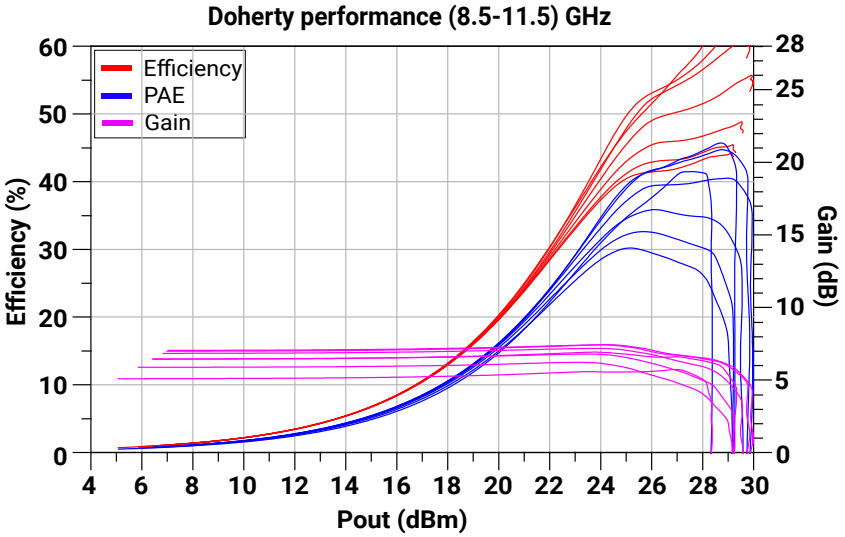

Figure 5.3: Simulation of the Doherty with the EM combiner block

Article [9] provides an explanation of how to design driver stages for DPAs and also discusses the pros and cons of using two drivers instead of a single driver before the splitter.

5.1 Conclusion

The results obtained in this thesis will be analyzed comparing them to other works found in the literature.
There are very few examples of amplifiers designed to operate in the X-band and this number decreases even further when considering only those implemented in GaAs technology.
Table 5.1 summarizes the performance of other DPAs that operate in the frequency band we are interested in.
Although this thesis work does not cover the entire 4 GHz of the X-band, it still achieves a wider bandwidth coverage than the other design reported in the table. The results in terms of efficiency seem to be in line with those of the other designs considered.
Since the gain of the single device available in WIN technology was already not so high, it is expected that the overall gain of the wideband DPA would be limited. The other amplifiers considered also seem to have the same issue, with the exception of [9] where a driver stage was implemented to boost the gain.

article	center frequency	% BW	gain(sat)	efficiency	output power	configuration
[10]	9.5 GHz	14.7%	5.5 dB	$> 27\%$	30 dBm	GaAs single stage
[11]	9.6 GHz	10%	5 dB	$> 30\%$	31 dBm	GaAs single stage
[9]	10 GHz	20%	16 dB	$> 35\%$ (PAE)	27 dBm	GaAs two stages with a single driver
this work	10 GHz	30%	4 db	$> 40\%$	29 dBm	single stage

Table 5.1: Summary of X band Doherty found in literature

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