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Analysis and Design of a Digital-Based Operational Transconductance Amplifier for Neural Signal Acquisition

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Abstract

The thesis activity is in the framework of the European research project CEREBRO, which aims to develop a new non-invasive brain imaging technique with higher spatial resolution than conventional EEG, which is limited by signal attenuation through the skull. To overcome this limitation, the project proposes acquiring neural signals directly at the brain interface and transmitting them at higher frequencies, reducing the effect of signal loss through skull. This approach requires the design of tens-of-micrometer scale, remotely-powered CMOS circuits capable of detecting very low-amplitude brain signals and enabling wireless transmission.

This thesis addresses one of the main challenges of the CEREBRO system by exploring and adapting the concept of the Digital-Based Operational Transconductance Amplifier (DIGOTA) as a neural-interface amplifier. This architecture provides a promising solution to reduce both power consumption and silicon area while maintaining adequate performance for neural signal acquisition.

A key innovation of this work is also the use of the intrinsic resistive and capacitive properties of the electrodes, usually considered parasitic, as functional elements in the circuit. Instead of implementing dedicated resistors and capacitors on silicon, the characteristics of the electrode–solution interface and the coupling between electrodes are exploited as part of the circuit design. This strategy allows for a significant reduction of area.

A differential-output, fully passive-free version of DIGOTA was designed and implemented using Cadence Virtuoso. The circuit was first simulated with a simplified electrode model and later with a more detailed one, including frequency-dependent elements, to better represent real-world conditions. Simulation results show that the circuit output is a train of pulses whose amplitude depends on the input signal. This behavior allows the same circuit to be used for both signal acquisition and direct high-frequency data transmission, eliminating the need for a VCO block and thus saving additional area and power. To better control the pulse frequency and further reduce power consumption, an additional capacitance was introduced in the compensation stage.

One of the challenges was the lack of a accurate model for the electrodes to be used in the simulation. To overcome this, parameters from existing studies were

adapted, and simulations were performed across a wide range of values to ensure robustness.

The final circuit layout was designed to meet strict area constraints. Post-layout simulations, including Corner Analysis and Monte Carlo analysis, were performed and compared with schematic-level results to evaluate the effects of parasitics and process variations.

As a final step, a MATLAB script that calculates the conductance between all electrode pairs was used to explore various electrode geometries and arrangements, including both actual and floating dummy electrodes. The configuration that best matched the circuit model assumptions was selected and implemented in the final layout.

The circuit has now been sent for fabrication, and the next step is to conduct test both on the standalone amplifier and in a test setup reproducing the characteristics of the operating environment. These tests will also provide the opportunity to further refine the electrode models, improving the design and making necessary adjustments based on the measured performance.

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Chapter 1

Introduction

Electroencephalography (EEG) is one of the main techniques used to study brain activity in both scientific research and medical diagnostics. It is a non-invasive method that measures the electrical potentials generated by neurons using electrodes placed on the scalp. However, these signals are significantly attenuated by the human skull, which limits the spatial resolution.

To overcome this limitation, more precise but invasive techniques such as electrocorticography (ECoG) and stereo-EEG (sEEG) can be used, but these require skull trepanation to implant electrodes under the skull or directly into the brain cortex, respectively, and these can only image restricted regions of the brain.

The EIC Pathfinder EU project CEREBRO [1] (an electric Contrast medium for computationally intensive Electroencephalographies for high REsolution BRain imaging withOut skull trepanation) aims to address this gap by developing the first EEG contrast medium, enabling non-invasive imaging of the entire brain. The long-term goal is to achieve the spatial resolution of invasive methods without the need for surgery.

The idea of this project is to create micro-scale circuits capable of detecting neuronal signals close to neurons and transmitting them to external electrodes. By shifting the frequency of the signal to higher frequencies before transmission, attenuation due to skull can be reduced, leading to more accurate readings of neural activity.

To be suitable for such applications, these circuits must be extremely compact and capable of self-powering through energy harvesting. While future versions will need to meet strict constraints in terms of power consumption and area, the prototype explored in this thesis assumes relaxed conditions: the circuit is externally powered via wires, and its shape is designed to be narrow and long, allowing manual placement near the target neuron.

In conventional designs, a typical approach would involve an analog front-end amplifier that senses the potential generated by the neuron through input electrodes. This signal is then amplified and sent to a voltage-controlled oscillator (VCO), which modulates it into a frequency signal. The resulting signal is passed to a digital buffer and finally transmitted to external electrodes for further processing.

However, this thesis investigates an alternative and more innovative approach based on a Digital-Based Operational Transconductance Amplifier (DIGOTA). Previous studies have already highlighted DIGOTA's advantages in terms of lower area and power consumption, making it a candidate for this type of application.

What makes the use of DIGOTA in this work even more innovative and challenging is the use of the parasitic properties of the electrodes as functional circuit elements. The electrodes and their mutual coupling are modeled using resistances and capacitances. Instead of being considered unwanted effects, these parasitic elements are intentionally integrated into the feedback and summing network, replacing traditional passive components usually implemented on silicon. This approach allows for a further reduction in circuit area and simplifies the overall layout.

Another significant advantage of this configuration is that it removes the need for a VCO block. In fact, the DIGOTA circuit naturally produces an output train of pulses whose amplitude is directly modulated by the input signal. This modulation allows the neural signal to be transmitted at a much higher frequency than its original frequency, without requiring an additional frequency-shifting stage. As a result, the system benefits from lower area and power consumption.

This thesis presents the design, simulation, and layout of such a DIGOTA-based circuit, developed with custom-shaped electrodes and integrated in the framework of the CEREBRO project.

The work includes a brief review of existing literature on electrode modeling, with particular attention to the electrical equivalent circuits of electrodes in organic solutions, in order to approximate their behavior for CMOS-compatible simulations.

In addiction, the concept of digitally based analog amplifiers is explored, with analysis and comparison of different DIGOTA topologies.
Behavioral simulations using MATLAB and Simulink are also performed to better understand the operating principles of the architecture and to evaluate its theoretical performance before schematic-level implementation.

Chapter 2

Electrode Models

Recent technological progress have enabled significant miniaturization of both electrodes, such as penetrating microelectrodes that are now preferred over planar ones for higher specificity, and electronic front-end circuits. CMOS technology is the predominant choice for electronic front-ends that are integrated with electrodes, especially for the development of the next generation of miniaturized, wireless, and ultra-low-power biosensors. These integrated devices play a crucial role in monitoring chemical and biological processes, enabling real-time acquisition and processing of vital data. Their applications are broad and include monitoring neural activity, electrochemical biosensing, and the detection of specific analytes such as dopamine. They can be used in a wide range of critical applications, with particular emphasis on medical diagnostics, continuous health monitoring, personalized medicine, and monitoring and addressing neurodegenerative diseases.

However, to ensure reliable CMOS circuit behavior and maintain system performance, the robust and effective design of these integrated devices critically depends on the availability of accurate equivalent electrical models of the interface between the electrode and the biological environment or electrolyte solution.

In the design of CMOS readouts for electrochemical sensors and biosensors, the initial step involves integrating an appropriate electrical equivalent circuit for the sensors into the CAD design tool.

Several equivalent circuits have been proposed to represent sensor behavior. The use of inaccurate models can in fact lead to fatal design errors, improper sensor operation, significant differences between simulations and actual measurements, and, consequently, severely compromise the accuracy of diagnoses.

Typically, Randles models (i.e., R-RC circuits) are used to characterize electrode impedance. The parameters of these models are calculated by solving equations, by fitting experimental data, or even estimated using numerical analysis approaches.

However, this conventional model has substantial limitations and is often considered too simple, failing to accurately represent the complex electrochemical phenomena occurring at the electrode interface.

Following are some models that go to realize a more accurate model that considers phenomena more suitable to modern microelectrodes.

2.1 Neural Electrode Model

The aim of this study [2] is to monitor the impedance changes occurring on Pt/Ir penetrating microelectrodes inserted in ex-vivo porcine brains to derive an opportune electrode/brain model describing the system and its evolution in time. In particular, impedance spectroscopy measurements have been performed for 144 hours to characterise the evolution of the electrochemical behaviour. The experiments were performed using 2-inch monopolar microelectrodes coated with a 3 µm layer of Parylene-C and with a 25 µm exposed tip. The diameter of the microelectrode is 81 µm at the shaft and 3 µm at the tip, which has a taper ratio of about 25:1 and an area of 275 μm^2.

The electrode/brain interfacial impedance varies simultaneously in frequency and in time after implantation.

From the experimental results, shown in Figure 2.1, two equivalent electrical circuit (EEC) models were derived to describe the impedance variation of the microelectrode in different phase of the experiment.

1. For measurements acquired up to 48 hours after electrode insertion, the system was modeled using a Single Time Constant (TC) circuit. This model is illustated in Figure 2.2a and consists of:
   - a series resistance (R_s), representing the resistance of the electrolyte (the artificial cerebrospinal fluid).
   - a charge transfer resistance ($R1$),
   - a capacitance (CPE), which represent the double-layer capacitance at the interface. It modeled as Constant Phase Elements (CPE) instead of ideal capacitors, to account for surface roughness and heterogeneity of biological samples, so that:
   $$Z_{CPE} = \frac{1}{(j\omega)^{\alpha} Q} \tag{2.1}$$
   where j is the imaginary number, ω is the angular frequency, and Q and α are the CPE parameters.

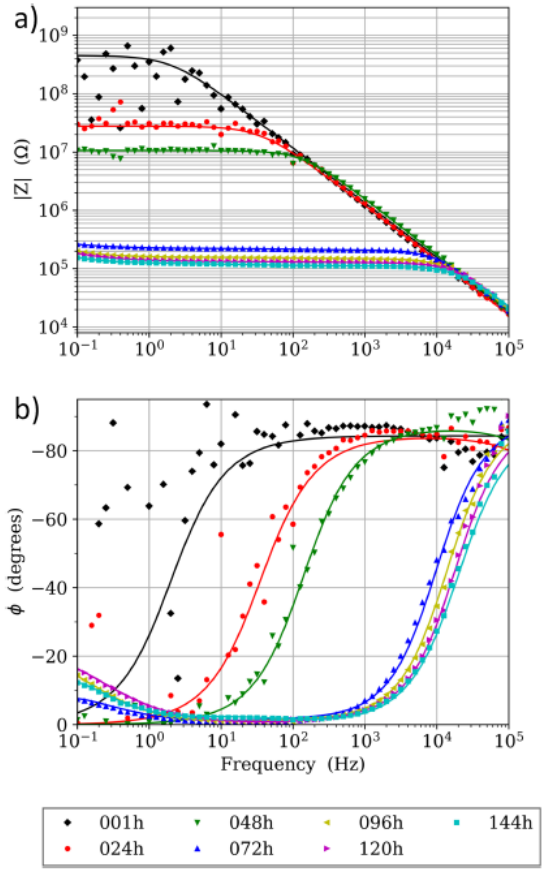


Figure 2.1: Impedance spectra acquired in the experiment (a) modulus and (b) phase [2].

2. After 48 hours, a more complex model is needed because two additional time constants appear in the spectra. This is related to the biological material attached to the surface of the microelectrode, that is not homogeneous and it has a variable thickness. This biofilm alters the transport phenomena close to the electrode and, promotes charge transfer from the solution to the metal. To model this heterogeneous layer covering the miocrolectrode, two time constants (TCs) are added at this model, as shown in Figure 2.2b:

   - the branch $R2 \parallel CPE2$ describes an internal layer of biological material, closer to the electrode surface.
   - the branch $R3 \parallel CPE3$ describes an external layer covering the first one.

The parameters of these EEC models (resistances $R1$, $R2$, $R3$ and parameters Q and α of CPEs ($Q1$, $Q2$, $Q3$) vary considerably over time, Unlike the stationary

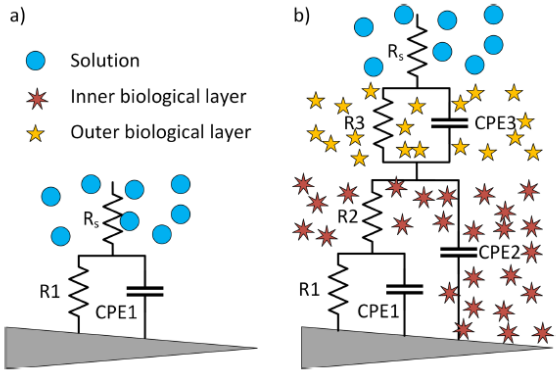


Figure 2.2: EEC of the electrode. a) Model for spectra acquired up to 48 hours. b) Model for spectra acquired in the second part of the experiment [2].

Randles model, Figure 2.3 shows the trend of these parameters, highlighting in particular a significant decrease of the charge transfer resistance ($R1$) in the first 72 hours, attributed to the attachment of the biofilm that improves the charge transfer mechanism.

2.2 Electrochemical Electrode Model

Another approach to consider and model the layering phenomena occurring at the electrode-solution interface is presented in the paper [3], which analyses Pt/Ir planar microelectrodes used in a digital potentiostat.

One of the main problems with traditional models for electrochemical sensors, such as the Passive Model (Figure 2.4a) and the Active Model (Figure 2.4b), is how they represent the capacitance at the interface between the electrode and the electrolyte.

These models use fixed values for this equivalent capacitance. However, in reality, because of the layering phenomema that happen at this interface, the capacitance of a metal electrode changes with the frequency of the input signal. So, it cannot be accurately described with a constant value.

Moreover, the Passive Model does not correctly model the faradaic current (the current linked to redox reactions at the electrode interface, which depends on the analyte concentration). While the Active Model adds a current source to represent the faradaic current, but it only considers the expected current range for a given analyte concentration. It does not take into account changes in the faradaic current caused by variations in the bias voltage (for example, due to CMOS process variations or thermal drift).

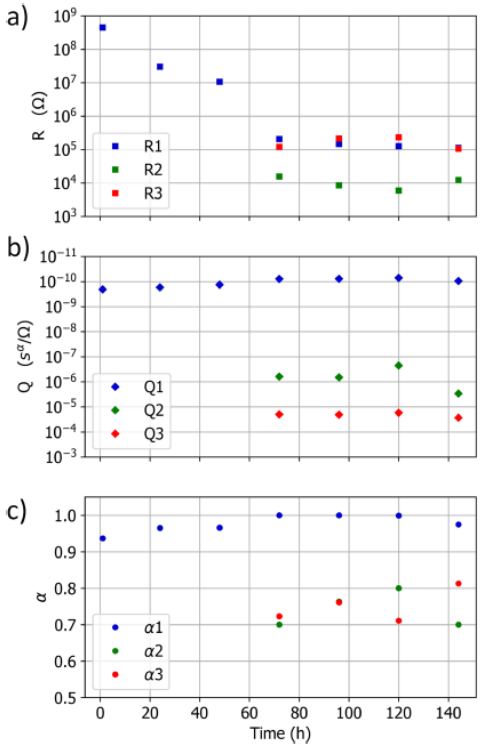


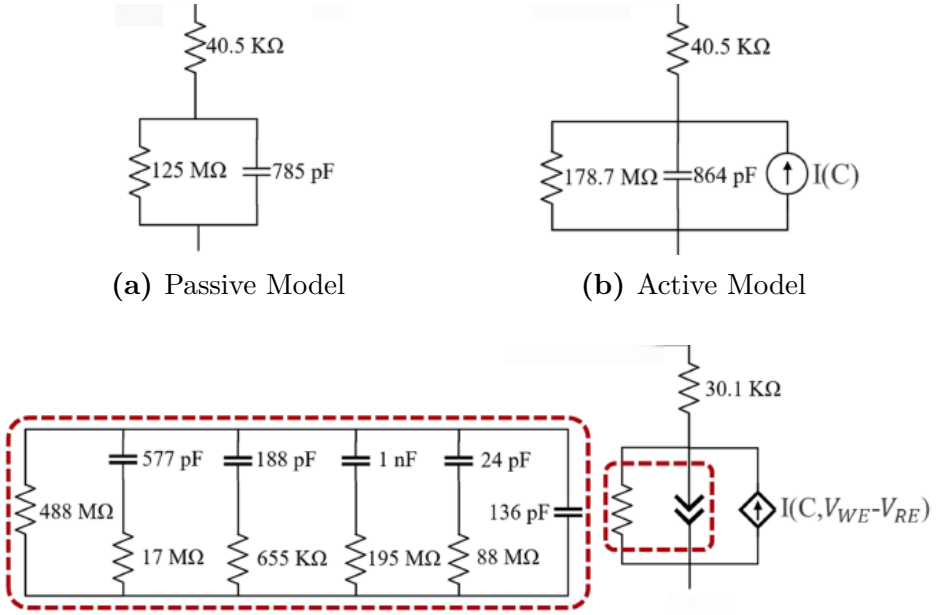
Figure 2.3: Trend of the different fitting parameters derived from EEC modeling of spectra [2].

As a result, these models do not correctly represent how the sensor interface behaves at different frequencies and conditions. In particular, they either fail to predict or wrongly predict when the potentiostat reaches saturation. This can lead to unrealistic CMOS simulation results and possibly critical design mistakes.

This paper introduces a new model called the Full Active Model (Figure 2.4c), which is a more accurate, robust, and complete equivalent circuit for electrochemical sensors than traditional models. In particular:

- It includes Constant Phase Elements (CPEs) to model the frequency-dependent capacitance at the electrode interface caused by layering phenomena. It uses multiple RC branches (the number depends on the sensor's complexity) to accurately match the behaviour of a CPE, as seen in experimental impedance measurements. This makes the model reliable for a wide range of applications.

- It models the faradaic current using a voltage-controlled current source, which reflects its (often nonlinear) dependence on the potential difference between two electrodes.



(a) Passive Model **(b)** Active Model

(c) Full Active Model

Figure 2.4: Different models for the equivalent circuit of an electrode of the electrochemical cell [3].

By comparing different models with experimental data, it is demonstrated that the new model provides the best match. As seen in Figure 2.6, which presents electrochemical impedance spectroscopy (EIS) measurements, the "full active model" closely fits both the magnitude and phase of the measured impedance across a wide frequency range. Figure 2.5 further confirms that the new model accurately predicts the risk of potentiostat saturation.

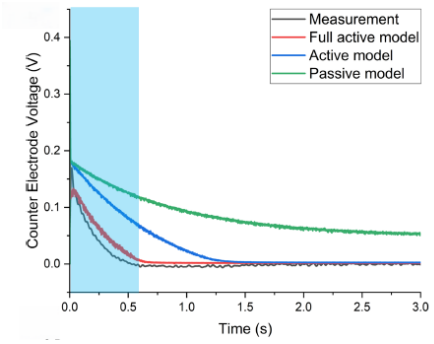


Figure 2.5: The risk of saturation on the voltage measured at the electrode and simulated by the different models. The highlighted time interval shows the operation of the potentiostat before saturation [3].

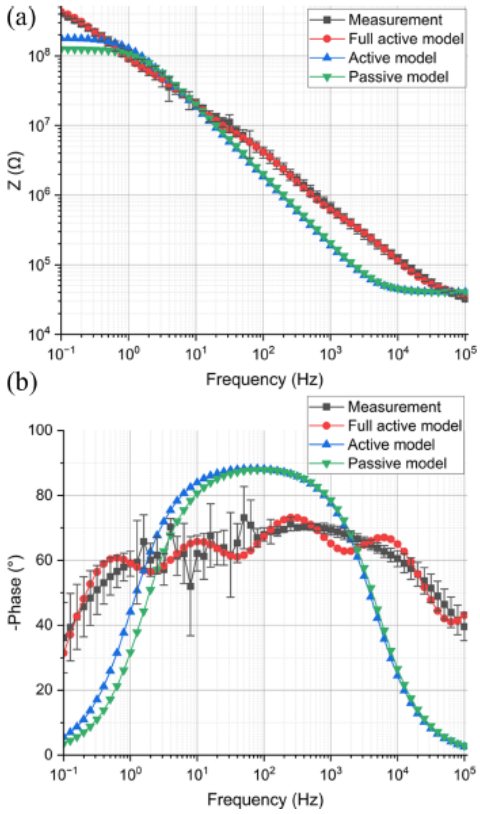


Figure 2.6: Electrochemical impedance spectroscopy of planar Pt/Ir microelectrode and the fitted electrical models [3].

Chapter 3

Digital-Based OpAmp

3.1 Introduction and Context

Roadmap

Moore's Law, formulated by Gordon Moore in the 1965, described an empirical observation: the number of transistors integrated on a chip tended to double every 1.5 to 2 years, leading to increased performance and reduced costs. For nearly fifty years, this exponential trend was a fundamental reference for the development of the semiconductor industry.

To support and guide this technological evolution, global roadmapping efforts were established, initially through the International Technology Roadmap for Semiconductors (ITRS) and currently through the International Roadmap for Devices and Systems (IRDS).

The IRDS aims to identify key directions for the future of microelectronics and *More Moore* and *More-than-Moore* are two of the strategies that continue and extend Moore's law [4].

- *More Moore* refers to continued shrinking of physical feature sizes of digital functionalities (logic and memory storage) in order to improve density (reducing cost per function) and performance (in terms of speed and power consumption) [5].
- *More-than-Moore* refers to the integration of functionalities into devices that do not necessarily scale according to Moore's Law but provide added value in other ways. The *More-than-Moore* approach enables non-digital functionalities (e.g., RF communication, power management, passive components, sensors, actuators) to move from the system board level into the package (System-in-Package, SiP) or directly onto the chip (System-on-Chip, SoC) [6].

This evolution of semiconductor technology, due to scaling, is visually represented in Figure 3.1.

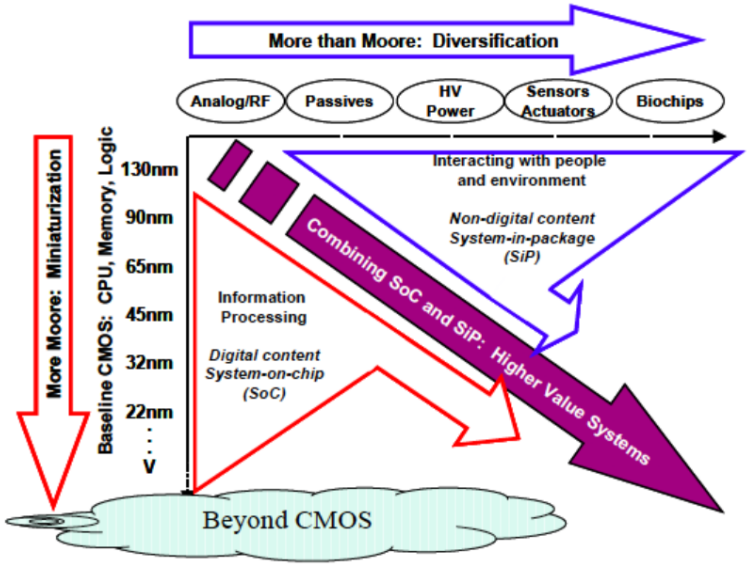


Figure 3.1: IRDS Roadmap

Advancements in fabrication technologies now allow the co-integration of analog components on the same chip with scaled digital logic, enabling the realization of complex mixed-signal systems. However, the aggressive scaling of digital logic associated with *More Moore* imposes significant limitations and challenges on analog/mixed-signal circuit design and integration, such as reliability and matching issues introduced by improved process variability due to scaling [6].

Re-Thinking Analog Integrated Circuits in Digital Terms

As explained above, while modern CMOS technologies have significantly improved the performance of digital integrated circuits thanks to geometric and supply voltage scalability, analog ICs benefit less from these advances. In fact, reduced power levels, short-channel effects, and increased process variability make the integration of analog blocks into System-on-a-Chip designs increasingly difficult [7].

The limitations of analog circuits fabricated in today's digital processes have been addressed through new topologies and design techniques. Many of these solutions mitigate specific technological drawbacks at the cost of increased design complexity and/or degraded performance. State-of-the-art analog circuits typically operate above 1V, have power consumption limited by bias currents, and occupy significant silicon area. Sub-0.5V approaches using analog techniques often exhibit

degraded energy efficiency, larger area, and increased complexity [8].

An alternative approach is to rethink analog functions in digital terms. This allows them to be implemented using circuits and design methodologies that are as close as possible to the digital domain. This approach aims to overcome the limitations of traditional analog circuits in modern low-voltage digital technologies by exploiting the strengths of the digital domain implemented for analog functions [9], [10].

For this reason the DB-OTA circuit has been proposed as a digital-based implementation of an analog differential circuit to fill this gap. The idea is to implement the function of a standard differential circuit (such as a CMOS differential pair) by describing it in digital terms [7], [11].

The main advantages of these digital-based OpAmps are:

- **Ultra-Low Power Consumption:** They can operate with ultra-low supply voltages, even below 0.5 V (down to 0.25/0.3 V), enabling direct powering from energy harvesters or micro-batteries—ideal for energy-autonomous systems. Unlike analog sub-systems, which suffer from degraded transistor performance, reduction in signal swing and reduced SNR at low voltages, digital-based architectures eliminate bias currents and can function deep in the sub-threshold regime.

  As a consequence power consumption is reduced to the nanoWatt range, overcoming the inherent power limitations of conventional analog designs [12], [8].

- **High Area Efficiency:** They are very compact. The implementation based on standard digital cells allows area scaling similar to that of digital circuits and significantly reduces area compared to traditional analog solutions (up to 2–85 times smaller [8]).

- **Reduced Design and Integration Effort:** These circuits take advantage of standard digital design tools, such as computer-aided design (CAD), verification, and testing techniques. Their behavior can be described using hardware description languages (HDLs), allowing for fully automated implementation through digital design flows. This significantly simplifies both the design and integration processes [7], [8].

These features make them particularly suitable for energy- and area-constrained systems, such as sensor nodes for the Internet of Things (IoT) [13] or "Body Dust" [14] applications, which require low-frequency analog interfaces powered directly from energy harvesting.

3.2 Digital-Based OTA Behavior

The Digital-Based Operational Transconductance Amplifier (DB-GOTA) is a mixed-signal circuit that uses standard digital logic elements to replicate the functionality of a differential amplifier, typically implemented with analog circuitry. Its core operation is based on detecting the polarity of a differential input and encoding it into a digital signal, which is subsequently integrated to generate an analog-like output current.

A differential stage produces an output that depends on the difference between two input signals, i.e., the differential-mode signal $v_D = v^+ - v^-$, and ideally rejects any signal common to both inputs, i.e., the common-mode signal $v_{CM} = \frac{v^+ + v^-}{2}$.

In analog CMOS implementations, this function is typically realized by a differential pair (Figure 3.2) composed of two MOS transistors biased in saturation and sharing a common source node. In such configurations, the source node voltage ideally tracks the common-mode input and is subtracted from the gate voltages. This ensures that the gate-source voltages of the transistors depend only on the differential input, enabling effective common-mode rejection. However, in modern digital CMOS technologies, this approach presents several limitations, including a narrow input common-mode range, a relatively high minimum supply voltage, and a limited output swing.

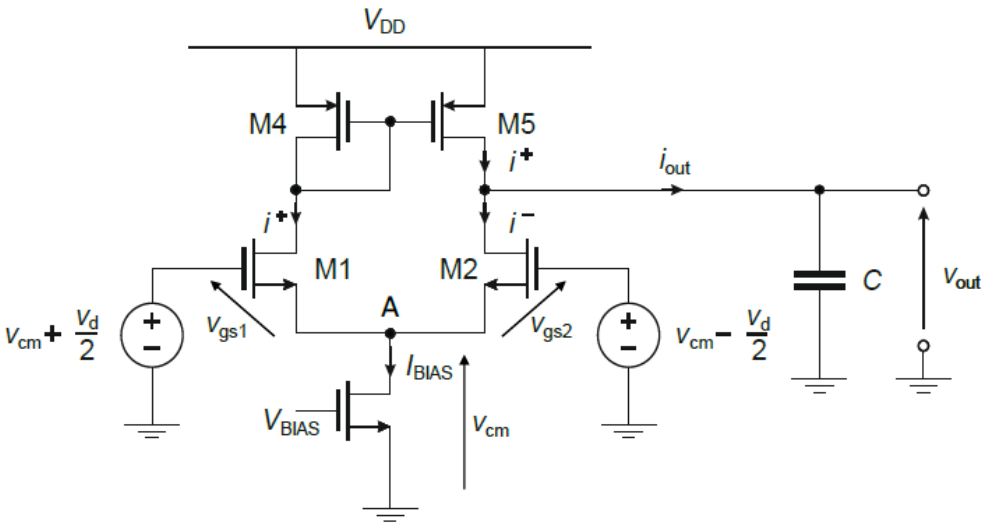


Figure 3.2: Analog differential pair.

DB-OTA addresses these limitations by using digital circuits to sense the differential input. In particular, it employs a pair of non-inverting digital buffers, as shown in Figure 3.3. Each buffer operates as a comparator with a switching threshold V_T:

- When $v_{\text{IN}} > V_T \Rightarrow v_{\text{OUT}} = V_{OH} > V_T \Rightarrow \text{OUT} = \texttt{1}$
- When $v_{\text{IN}} < V_T \Rightarrow v_{\text{OUT}} = V_{OL} < V_T \Rightarrow \text{OUT} = \texttt{0}$

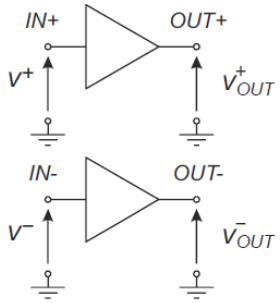


Figure 3.3: Digital buffer pair.

By applying this logic to both inputs, two key conditions can be identified:

- When $v^+ > V_T$ and $v^- < V_T$, the output becomes $(\text{OUT}^+, \text{OUT}^-) = (1, 0)$, which implies a positive differential voltage, i.e., $v_D > 0$.
- Conversely, when $v^+ < V_T$ and $v^- > V_T$, the output is $(\text{OUT}^+, \text{OUT}^-) = (0, 1)$, indicating a negative differential voltage, i.e., $v_D < 0$.

In these cases, the differential voltage is correctly detected, and its polarity is captured by the digital outputs.

However, when both the inputs are on the same side of the threshold (i.e., either $v^+ > V_T$ and $v^- > V_T$, or $v^+ < V_T$ and $v^- < V_T$), the outputs are (1, 1) or (0, 0), respectively. In these situations, the digital outputs do not reflect the differential input but instead indicate the common-mode level:

- If $v^+ > V_T$ and $v^- > V_T$, then $(\text{OUT}^+, \text{OUT}^-) = (1, 1)$. This implies that the average of the two signals exceeds the threshold, i.e., $v^+ + v^- > 2V_T$, which means $v_{CM} > V_T$.
- If $v^+ < V_T$ and $v^- < V_T$, then $(\text{OUT}^+, \text{OUT}^-) = (0, 0)$. In this case, both signals are below the threshold, so $v^+ + v^- < 2V_T$, which implies $v_{CM} < V_T$.

To transform a simple pair of digital buffers into a true differential structure, it is necessary to implement a compensation feedback, as illustrated in Figure 3.5, that rejects the common-mode component of the input. This compensation is performed in real time and ensures that the effective inputs to the buffers are always driven toward a (1, 0) or (0, 1) configuration, independently of the actual common-mode voltage applied at the inputs. As a result, the output of the buffer pair remains exclusively sensitive to the differential input voltage.

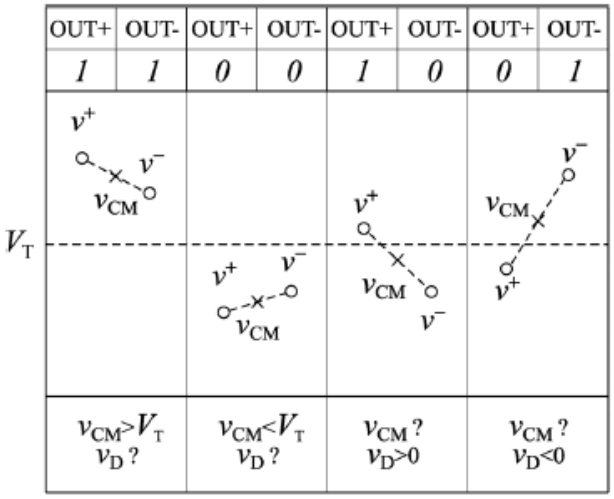


Figure 3.4: Digital output configurations and implications on DM and CM input signals.

Figure 3.4 summarizes the output logic states of the digital buffers for all input combinations relative to the threshold V_T. When the outputs are (OUT^+, OUT^-) = (1,0) or (0,1), the differential input voltage v_D can be clearly determined. This situation corresponds to the condition

$$|v_{CM} - V_T| > \left|\frac{v_D}{2}\right|. \tag{3.1}$$

Conversely, when both buffer outputs are equal, i.e., (1,1) or (0,0), the differential input cannot be resolved, but the common-mode level v_{CM} relative to V_T can be inferred. This is the case when

$$|v_{CM} - V_T| < \left|\frac{v_D}{2}\right| \tag{3.2}$$

. These ambiguous cases activate the compensation mechanism, which dynamically adjusts the internal nodes to restore a valid differential interpretation.

3.3 DB-OTA circuit

The complete digital-based OTA (DB-OTA) circuit proposed in Fig. 3.5 is describer in [7] and it consists of the following main blocks:

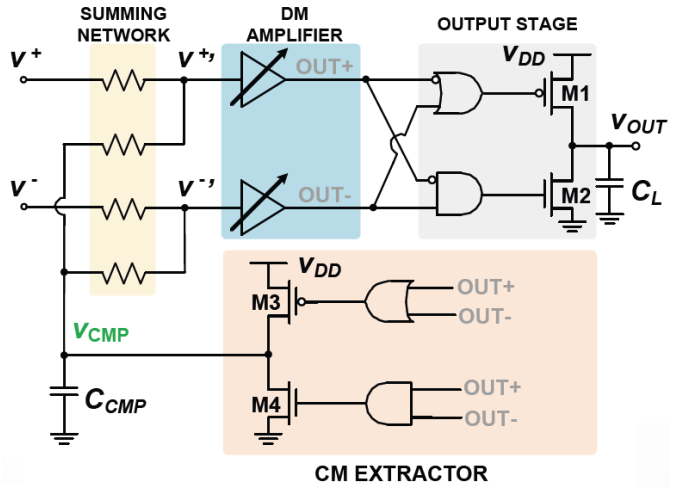


Figure 3.5: DB-OTA schematic [7].

1. **Digital Buffers (DM amplifier):** A pair of single-ended non-inverting digital buffers receives the internal input signals v'^{+} and v'^{-} (which are not directly the external inputs) and generate the digital output signals. These buffers are implemented as cascades of an even number of CMOS inverters.

   It is essential that the two buffers have the same V_T, to ensure correct operation. To address this issue and improve robustness against process variations and mismatch, a calibration network can be introduced [12].

2. **Summing Network:** This block adds a "compensation" signal (v_{cmp}) to the external inputs v^{+} and v^{-} to generate the effective input signals v'^{+} and v'^{-} for the digital buffers:

$$v'^{+} = \frac{v^{+} + v_{cmp}}{2}, \qquad v'^{-} = \frac{v^{-} + v_{cmp}}{2}. \tag{3.3}$$

   It can be implemented using a resistive network or, more conveniently in CMOS technology, using quasi-floating gate (QFG) techniques.

3. **CM Extractor:** This stage controls the common-mode (CM) level. It receives the digital outputs (OUT^{+} and OUT^{-}) of the buffers and generates the compensation signal v_{cmp}. It includes a tri-state inverter (transistors

M1–M2 driven by logic AND and OR gates) loaded by a capacitor (C_{cmp}). Its goal is to keep the internal CM voltage (v_{CM}) close to the threshold voltage of the digital buffers, regardless of the external CM voltage, therefore:

- when (OUT^+, OUT^-) = (0, 0), the pMOS transistor M1 is active, injecting current into the capacitor to increase v_{cmp} (to correct CM);
- when (OUT^+, OUT^-) = (1, 1),the nMOS transistor M2 is active, discharging the capacitor to decrease v_{comp}.
- in the (1,0) or (0,1) configurations, both M1 and M2 are turned off, and v_{comp} is held constant.

4. **Output Stage:** This block receives the digital outputs (OUT^+ and OUT^-) of the buffers and generates the single-ended analog output signal v_{out}. It includes another tri-state inverter (transistors M3–M4) loaded by an output capacitor (C_{out}).

   - If the buffer output is (0,1), M4 is active to decrease v_{out}.
   - If the output is (1,0), M3 is active to increase v_{out}.
   - When the output configuration is (1,1) or (0,0) (i.e., when CM control is active), both M3 and M4 are turned off, and the output is held constant.

3.4 Digital OTA (DIGOTA) circuit

In the paper [8], the previous DB-OTA topology has been modified replacing the resistive summing network used for CM compensation with two Muller C-elements, as presented in Figure 3.6.

In prior digital-based OTAs, the common-mode compensation signal was added to the primary inputs via a passive summing network based on on-chip resistors, pseudo-resistors, or quasi-floating gate transistors, at the cost of substantial area overhead and voltage gain degradation. By eliminating the resistive summing network, this technique results in a fully-synthesizable design that is compatible with a digital standard cell flow. Furthermore, it exhibits reduced input-referred noise and improved resilience against mismatch and process variations, while maintaining a low power consumption in the nW range and a supply voltage of 300 mV.

In this circuit, the inputs of the Muller C-elements are connected both to the external inputs of the OTA and to the output of the common-mode compensation network. The outputs of the Muller C-elements, $v_{\text{MUL}+}$ and $v_{\text{MUL}-}$, drive a pair of digital inverters similar to the digital buffers in the DB-OTA.

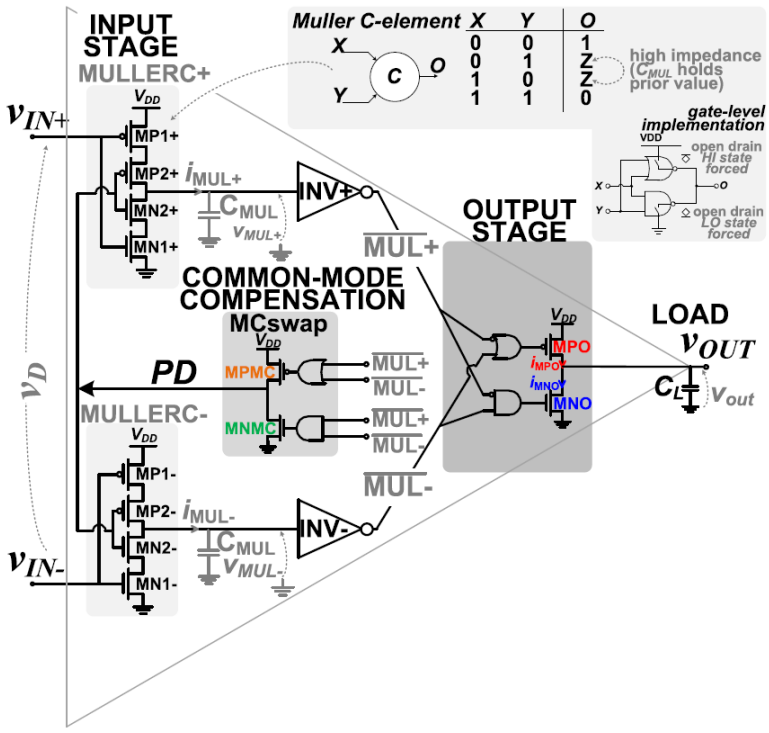


Figure 3.6: DIGOTA schematic [8].

The CM compensation and output stages, as in the DB-OTA, work based on the digital outputs of the inverters, $\overline{\text{MUL}+}$ and $\overline{\text{MUL}-}$, and apply negative-feedback compensation to enforce the condition $v_{CM} = V_T$.

so that when $v_{CM} < V_T$ or $v_{CM} > V_T$, the condition $v_{CM} = V_T$ is enforced with a negative-feedback compensation. The compensation circuit implements a passive-less, self-oscillating loop dynamically tracking the effect of the common-mode input on $v_{\text{MUL}+}$ and $v_{\text{MUL}-}$, as needed by INV+ and INV- to sense the differential input.

The overall DIGOTA state transition graph is summarized in Figure 3.7 and it can be described as follow:

- **State A:** When both voltages v_{MUL+} and v_{MUL-} are lower than the threshold V_T, we have $(\overline{\text{MUL}+}, \overline{\text{MUL}-}) = (1,1)$. As a result, the output stage is turned OFF, while the nMOS of the CM stage is ON, leading to $PD = 0$. Consequently, the pull-up networks of the Muller C-elements are enabled, allowing the capacitor C_{MUL} to charge. This causes both v_{MUL+} and v_{MUL-} to increase until the common-mode voltage v_{CM} approaches V_T, as shown in Figure 3.8a.

  - If $v_D > 0$ (i.e., $v_{IN+} > v_{IN-}$), then $i_{MUL+} < i_{MUL-}$, leading to State B+.

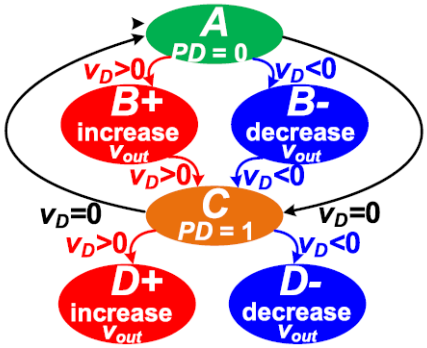


Figure 3.7: Logic states graph [8].

  - If $v_D < 0$ (i.e., $v_{IN+} < v_{IN-}$), then $i_{MUL+} > i_{MUL-}$, leading to State B-.
  - If $v_D = 0$ (i.e., $v_{IN+} = v_{IN-}$), then $i_{MUL+} = i_{MUL-}$, leading to State C.

- **State B+:** When $v_{MUL+} < V_T$ and $v_{MUL-} > V_T$, the logic outputs are $(\overline{\text{MUL+}}, \overline{\text{MUL-}}) = (1,0)$, therefore the common-mode compensation stage is OFF, and output stage pMOS is ON. As a result, the output capacitor C_{OUT} is charged, causing v_{OUT} to increase, as can be observed in Figure 3.8b.

- **State B-:** When $v_{MUL+} > V_T$ and $v_{MUL-} < V_T$, we obtain $(\overline{\text{MUL+}}, \overline{\text{MUL-}}) = (0,1)$ and so the CM stage is OFF andoutput stage pMOS is ON. This leads to the discharge of C_{OUT}, causing v_{OUT} to decrease.

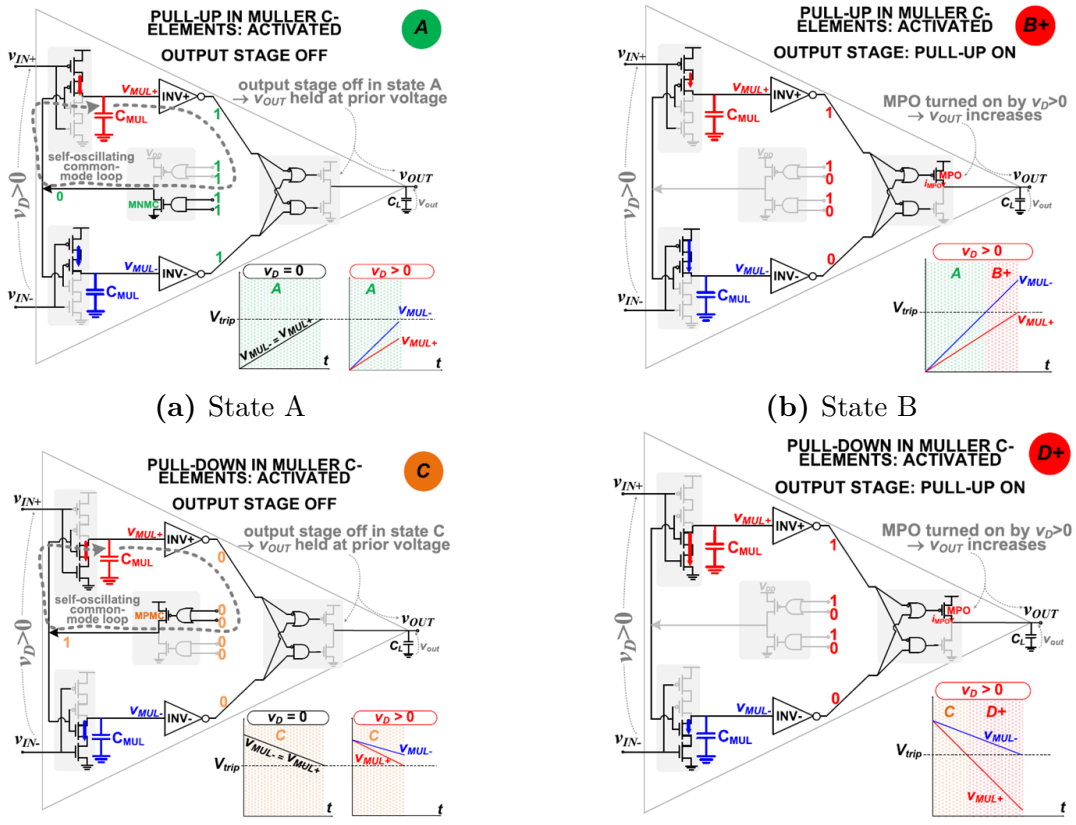
- **State C:** When both v_{MUL+} and v_{MUL-} are higher than V_T, then $(\overline{\text{MUL+}}, \overline{\text{MUL-}}) = (0,0)$. As a result, the output stage is OFF, and the CM stage nMOS is ON, which implies $PD = 1$. The pull-down networks of the Muller C-elements are now activated, discharging C_{MUL}. Consequently, v_{MUL+} and v_{MUL-} decrease, and the common-mode voltage v_{CM} approaches V_T, as illustrated in Figure 3.8c.

  - If $v_D > 0$ (i.e., $v_{IN+} > v_{IN-}$), then $i_{MUL+} > i_{MUL-}$, leading to State D+.
  - If $v_D < 0$ (i.e., $v_{IN+} < v_{IN-}$), then $i_{MUL+} < i_{MUL-}$, leading to State D-.
  - If $v_D = 0$ (i.e., $v_{IN+} = v_{IN-}$), then $i_{MUL+} = i_{MUL-}$, returning to State A.

- **State D+:** When $v_{MUL+} < V_T$ and $v_{MUL-} > V_T$, the condition becomes $(\overline{\text{MUL+}}, \overline{\text{MUL-}}) = (1,0)$. In this state, the CM stage is OFF and output stage pMOS is ON. Therefore, C_{OUT} is charged and v_{OUT} increases, as can be noticed in Figure 3.8d.

- **State D-:** When $v_{MUL+} > V_T$ and $v_{MUL-} < V_T$, the system is in the condition $(\overline{\text{MUL+}}, \overline{\text{MUL-}}) = (0,1)$. Here, the common-mode compensation stage is OFF

and output stage nMOS is ON. As a result, C_{OUT} is discharged, and v_{OUT} decreases.



(a) State A **(b)** State B

(c) State C **(d)** State D

Figure 3.8: DIGOTA circuit operations throughout its digital states when $v_D \geq 0$ [8].

3.5 Time-Multiplexed Digital Differential Amplification (TMD^{2}A)

The TMD^{2}A (Time-Multiplexed Digital Differential Amplifier), presented in [15], uses a single buffer operating in a time-multiplexed way, unlike the DB-OTA architecture, which employs two matched digital buffers to compare the non-inverting and inverting input voltages. This approach eliminates the need for buffer matching by sequentially comparing both input voltages against a shared trip point.

It has been proposed to design a low frequency, nW power Digital-based Acquisition Front-End (DAFE).

The operation of the circuit is schematically illustrated in Figure 3.9.

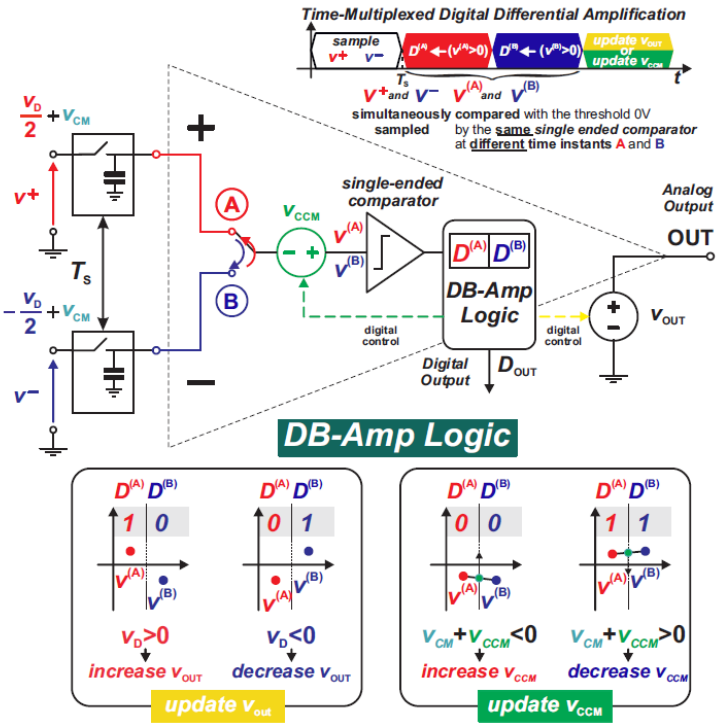


Figure 3.9: Concept diagram of the Time-Multiplexed Digital Differential Amplification principle [15].

The the non-inverting (v^+) and inverting (v^-) input voltages are sampled simultaneously and stored on their respective input capacitors. Then the single-ended comparator is used to process both inputs sequentially (time-multiplexing):

- In phase A, the sampled v^+ is connected in series with the common-mode compensating voltage v_{CCM} at the input of the buffer:

$$v^{(A)} = v^+ + v_{CCM} = \frac{v_D}{2} + v_{CM} + v_{CCM} \tag{3.4}$$

  The buffer output is stored in a D flip-flop $D^{(A)}$:

$$\begin{cases} v^{(A)} > 0 \Rightarrow D^{(A)} = 1 \\ v^{(A)} < 0 \Rightarrow D^{(A)} = 0 \end{cases}$$

- In phase B, similarly, v^- is now connected in series with v_{CCM}:

$$v^{(B)} = v^- + v_{CCM} = -\frac{v_D}{2} + v_{CM} + v_{CCM} \tag{3.5}$$

The result is stored in $D^{(B)}$:

$$\begin{cases} v^{(B)} > 0 \Rightarrow D^{(B)} = 1 \\ v^{(B)} < 0 \Rightarrow D^{(B)} = 0 \end{cases}$$

Depending on the digital outputs $(D^{(A)}, D^{(B)})$, either the output voltage v_{OUT} or the common-mode compensation voltage v_{CCM} is updated as detailed below:

- If $(D^{(A)}, D^{(B)}) = (1,0)$, meaning that $v_D > 0$, the output voltage v_{OUT} is increased, while v_{CCM} remains unchanged.
- If $(D^{(A)}, D^{(B)}) = (0,1)$, corresponding to $v_D < 0$, the output voltage v_{OUT} is decreased, with v_{CCM} again kept constant.
- If $(D^{(A)}, D^{(B)}) = (1,1)$, the compensation voltage v_{CCM} is decreased in order to satisfy the condition $|v_{CM} + v_{CCM}| < \left|\frac{v_D}{2}\right|$. In this case, v_{OUT} is held.
- If $(D^{(A)}, D^{(B)}) = (0,0)$, the compensation voltage v_{CCM} is increased to meet the same condition as above, while v_{OUT} remains unchanged.

The circuit schematic is presented in Figure 3.10. Its operation is governed by the finite state machine (FSM) in Figure 3.11, and the corresponding switch configurations are illustrated in Figure 3.12. The main steps of the operating sequence are described below:

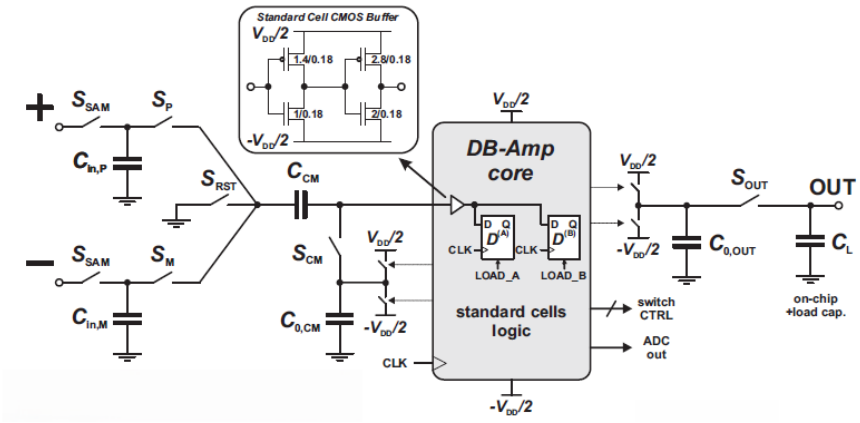


Figure 3.10: Schematic of TMD2A DAFE [15].

- In states A and B, the input capacitors $C_{in,P}$ and $C_{in,M}$, previously charged with v^+ and v^- respectively, are sequentially connected in series with C_{CM} at

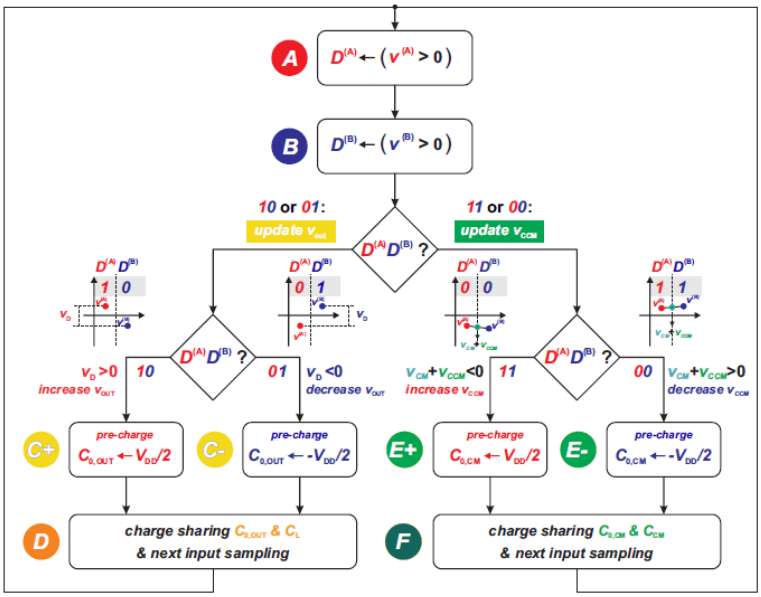


Figure 3.11: State transition graph of the DB-Amp control unit [15].

the buffer input. The corresponding digital outputs are stored in the D-Flip Flops D(A) and D(B) at the next clock edge. Based on their values, the FSM transitions to either states C+/C- (to update the output voltage) or E+/E- (to adjust the common-mode voltage v_{CM}), as shown in Figure **??**.

- In states C+ and C-, the capacitor $C_{0,OUT}$ is respectively charged or discharge to $\pm\frac{V_{DD}}{2}$.
- In state D, $C_{0,OUT}$ is connected in parallel with C_L, resulting in:

$$\Delta v_{OUT} = \frac{C_{0,OUT}}{C_L + C_{0,OUT}} \left(\pm \frac{V_{DD}}{2} - v_{OUT} \right) \tag{3.6}$$

  Therefore depending on whether the condition is (0,1) or (1,0), the output voltage is respectively increased or decreased. At the same time, both v^+ and v^- are sampled and stored again on $C_{in,P}$ and $C_{in,M}$.

- In states E+ and E-, the capacitor $C_{0,CM}$ is pre-charged to $\pm\frac{V_{DD}}{2}$, similarly to state C+/C-.
- In state F, $C_{0,CM}$ is connected to C_{CM} to update v_{CM}, thus compensating for common-mode variations. Input voltages are sampled in the same way as in state D.

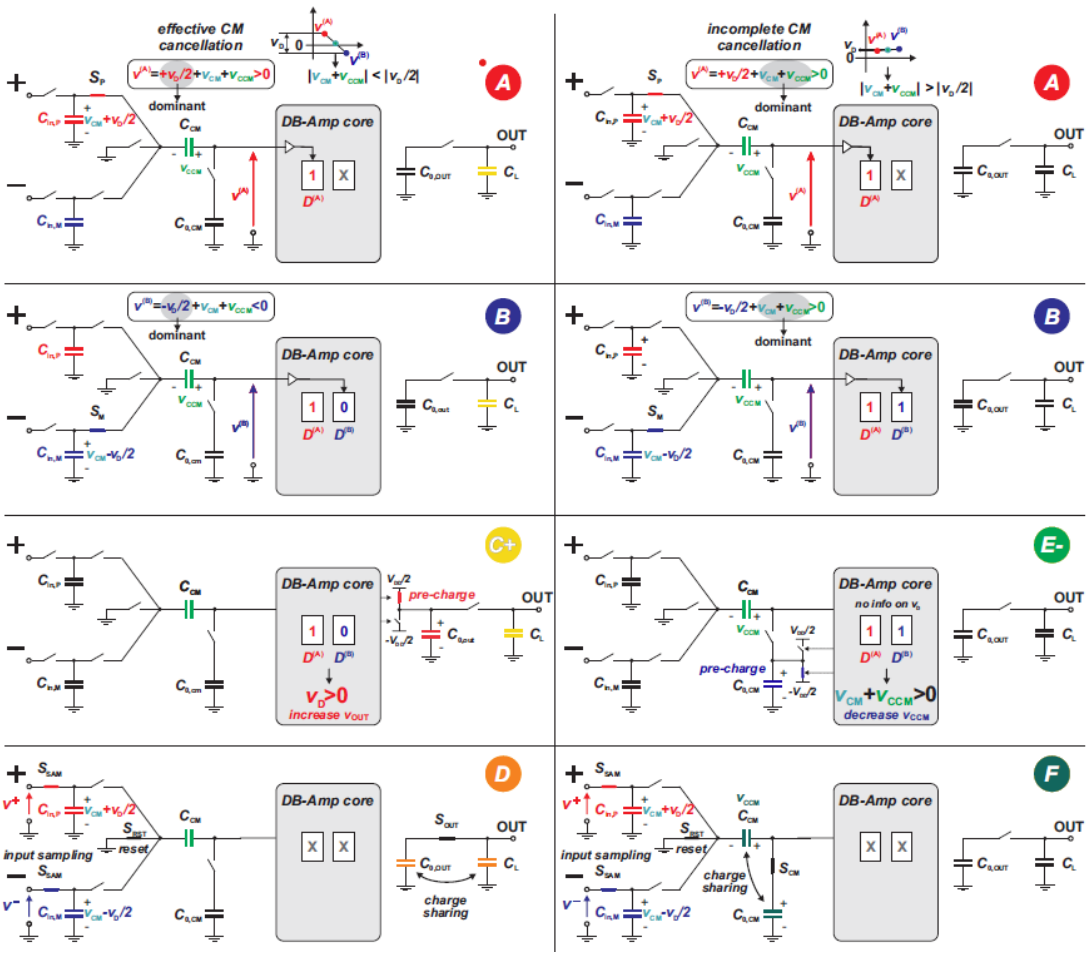


Figure 3.12: Sequence of switch configurations corresponding to the states in Fig.3.11 [15].

3.6 Comparison

Table 3.1 reports the performance of several DB-OTA-based amplifiers.

These implementations show good performance, especially in terms of area and power consumption. This demonstrates that DB-OTA-based amplifiers can meet the energy self-sufficiency requirements of IoT sensor nodes and emerging biosensing applications [11].

	DB-OTA [12]		**DIGOTA** [8]		**TMT2A** [16]
	Min	Max	< 500mV	> 500mV	
Technology (nm)	180		180		180
V_{DD} [V]	0.3		0.3		0.4
Area [μm^2]	1426		982		9450
Cap Load C_L [pF]	80		150		-
Power [nW]	0.407	0.591	2.4	107.5	4.5
DC Gain [dB]	31	29	30	73	39.6
GBW [kHz]	0.229	0.518	0.250	57.5	-
Slew Rate [V/ms]	0.097	0.264	0.085	0.019	-
In-band Input Noise [μV$_{rms}$]	-	-	21	122	11.3
THD [%]	1.26	2.82	2.0	1.0	1.3
CMRR [dB]	-	-	41	65	63.8

Table 3.1: Comparison between different Digital-Based OTA Implementations

Chapter 4

Ideal Behavioral Modeling of DIGOTA

To gain deeper insight into the operation of the proposed DB-OTA circuit and validate the expected behavior of its functional blocks, an ideal behavioral model has been implemented using MATLAB and Simulink. This model, based on the architecture described in the previous section, allows for controlled simulation and analysis under idealized conditions, thus isolating the fundamental mechanisms of operation from non-idealities such as noise, parasitics, and mismatches.

4.1 Simulink Model

To analyze the ideal behavior of the Digital-Based OTA (DIGOTA), the architecture shown in Figure 3.5 has been implemented in Simulink, as illustrated in Figure 4.1. The model includes all key functional blocks and two registers to synchronize the circuit with the clock.

The circuit is composed of the following main components:

- **Summing Network:** Modeled using sum and product blocks. It combines the external differential inputs (v^+ and v^-) with the compensation voltage (v_{cmp}), producing the actual inputs to the digital buffers:

$$v'^{+} = \frac{v^+ + v_{cmp}}{2}, \qquad v'^{-} = \frac{v^- + v_{cmp}}{2}.$$

- **Non-inverting Digital Buffers:** Modeled using comparator and delay blocks to include the propagation delay t_D. It generate the digital output signals

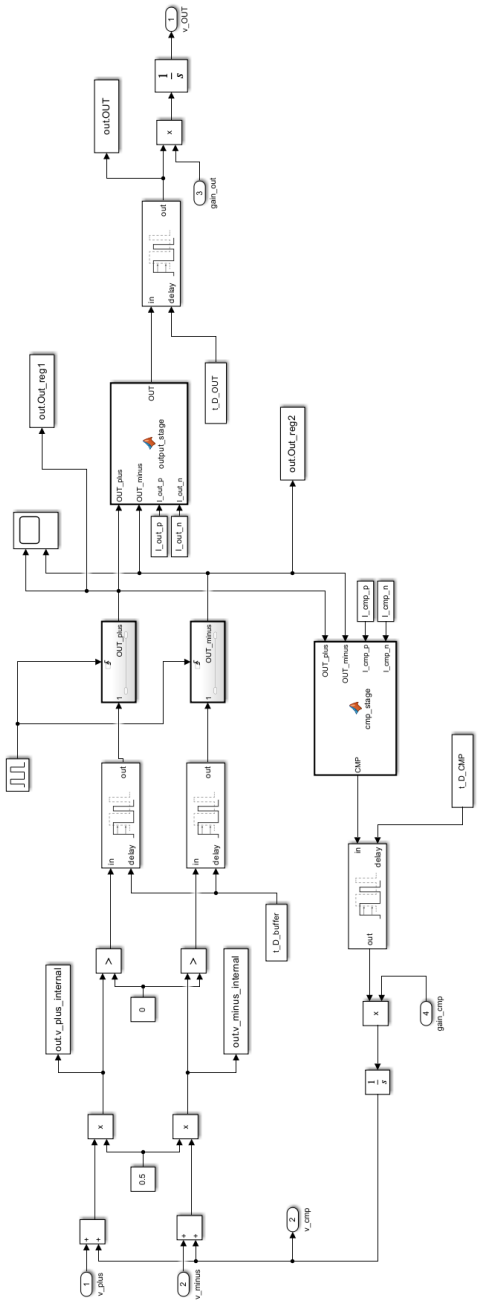


Figure 4.1: Simulink model of the Digital-Based OTA (DIGOTA).

according to the following relations:

$$OUT^{+} = \begin{cases} 1 & \text{if } v'^{+} > 0, \\ 0 & \text{if } v'^{+} \leq 0, \end{cases} \qquad OUT^{-} = \begin{cases} 1 & \text{if } v'^{-} > 0, \\ 0 & \text{if } v'^{-} \leq 0. \end{cases}$$

- **Registers:** They synchronize the circuit with the clock frequency f_{clk}.
- **Compensation Stage:** Controls the common-mode level via a tri-state inverter that charges or discharges a capacitor C_{cmp} based on the digital outputs. The current is modeled using a MATLAB Function block that implements the following equation:

$$I_{cmp} = \begin{cases} |I_{cmp,p}| & \text{if } (\text{OUT}^+, \text{OUT}^-) = (0,0) \\ -|I_{cmp,n}| & \text{if } (\text{OUT}^+, \text{OUT}^-) = (1,1) \\ 0 & \text{otherwise.} \end{cases}$$

  The capacitor behavior is simulated using a gain block $1/C_{cmp}$ followed by an integrator, so that the compensation voltage v_{cmp} is described by the capacitor equation:

$$\frac{dv_{cmp}}{dt} = \frac{I_{cmp}}{C_{cmp}}.$$

- **Output Stage:** Converts the differential digital signals into an analog output v_{out} via a tri-state inverter charging a capacitor C_{out}:

$$I_{out} = \begin{cases} |I_{out,p}| & \text{if } (\text{OUT}^+, \text{OUT}^-) = (1,0) \\ -|I_{out,n}| & \text{if } (\text{OUT}^+, \text{OUT}^-) = (0,1) \\ 0 & \text{otherwise.} \end{cases}$$

  Again, the capacitor is simulated using a gain block $1/C_{out}$ followed by an integrator, and the output voltage is described by the equation:

$$\frac{dv_{out}}{dt} = \frac{I_{out}}{C_{out}}.$$

4.2 Closed-Loop Simulations

4.2.1 Closed-Loop Circuit Configuration

The digital-based differential circuit can be configured in negative feedback to operate as an operational amplifier. In this configuration, the output of the circuit (v_{out}) is connected to the inverting input (v'^-) through a voltage divider, represented by the factor β, while the input signal is applied to the non-inverting input (v'^+). This leads to:

$$v^+ = v_{in}, \qquad v^- = \beta v_{out}.$$

Negative feedback forces the differential input v_d to zero, which implies:

$$v_d = v^+ - v^- = v_{in} - \beta v_{out} = 0 \Rightarrow v_{out} = \frac{1}{\beta} v_{in}.$$

This relationship shows that the circuit provides amplification with a gain determined by the feedback network ($1/\beta$).

The Simulink model of this configuration is illustrated in Figure 4.2.

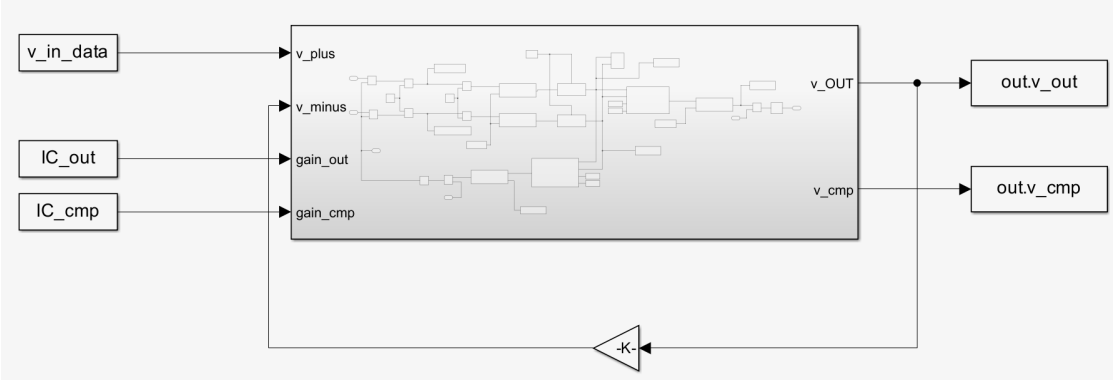


Figure 4.2: Simulink model of a feedback-configured DB-OTA.

4.2.2 Parameters and Inputs

To study the behavior of the circuit in the feedback configuration, simulations were carried out by varying certain parameters to analyze how these changes affect the properties and performance of the circuit.

The main parameters and signals defined in MATLAB are:

- **Feedback gain β:** Often set to $\beta = 1$ for simplicity.
- **Clock period:** $T_{clk} = 1$.
- **Logic gate delay:** $t_D = 0.1 \cdot T_{clk}$.
- **Input signal:** Unit-amplitude sine wave with frequency $f_{in} \gg f_{clk}$:

$$v_{in} = \sin(2\pi f_{in} t).$$

- **Parameters $\frac{I_{out}}{C_{out}}$ and $\frac{I_{cmp}}{C_{cmp}}$:** Some assumptions were made regarding the transistor currents:
  - The pMOS and nMOS transistor currents have equal magnitude.
  - The currents are identical for both the compensation and output stages, i.e.:

$$I_{out,p} = I_{cmp,p}, \quad I_{out,n} = I_{cmp,n}, \quad |I_{out,p}| = |I_{out,n}|, \quad |I_{cmp,p}| = |I_{cmp,n}|.$$

To explore the effect of varying $\frac{I_{out}}{C_{out}}$ and $\frac{I_{cmp}}{C_{cmp}}$, the parameter α was defined to relate these two terms:

$$\alpha = \frac{\frac{I_{out}}{C_{out}}}{\frac{I_{cmp}}{C_{cmp}}} = \frac{I_{out}}{C_{out}} \cdot \frac{C_{cmp}}{I_{cmp}}.$$

4.2.3 Output v_{out}

The circuit was simulated for different values of β. The results for $\beta = 1$ (voltage follower configuration) and $\beta = 0.2$ are shown in Figure 4.3 and 4.4, respectively.

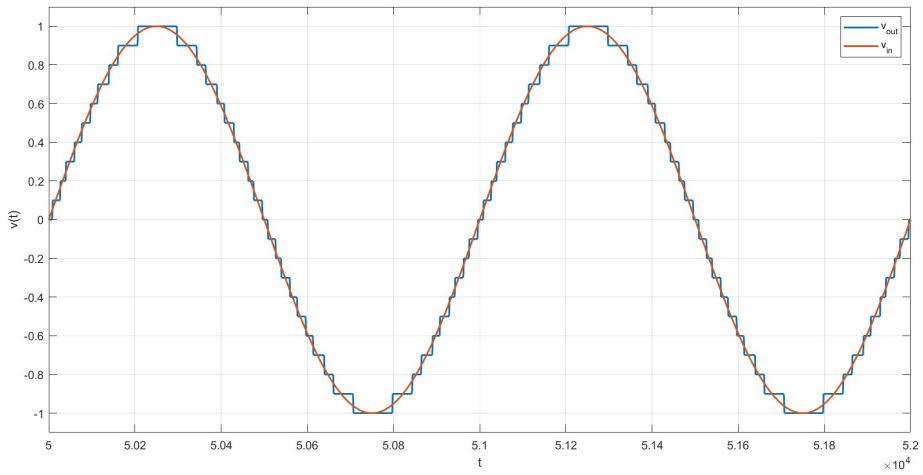


Figure 4.3: Behavior of v_{in} and v_{out} with $f_{in} = 10^{-3}$, $\beta = 1$, $I/C_{out} = 0.1$, $I/C_{cmp} = 0.2$.

In both configurations, the circuit is able to reconstruct the input sinewave with a gain equal to $1/\beta$, showing that the differential voltage $v_d = v^+ - v^- = v_{in} - \beta v_{out}$ is kept close to zero, as expected in a negative feedback system.

4.2.4 Compensation signal v_{cmp}

The compensation signal v_{cmp} is generated to maintain the internal common-mode voltage $v'_{CM} = \frac{v'^+ + v'^-}{2}$ close to the threshold voltage $V_T = 0$, regardless of the external input signal. Figure 4.5 shows the behavior of v_{cmp}.

It can be observed that the output and compensation stages operate alternately: when v_{out} changes, v_{cmp} remains constant, and vice versa.
The variations of v_{out} and v_{cmp} at each clock cycle depend on the parameters I/C_{out} and I/C_{cmp}. Specifically, for each clock pulse, the capacitors C_{out} and C_{cmp} can be

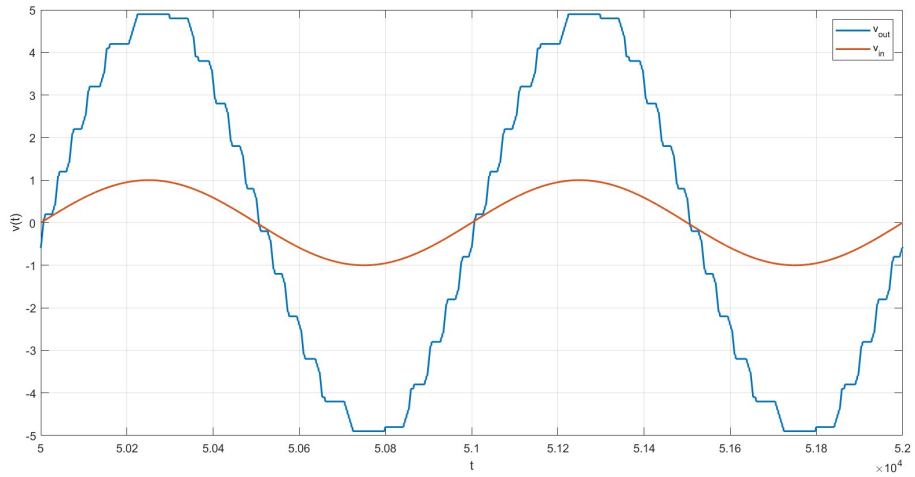


Figure 4.4: Behavior of v_{in} and v_{out} with $f_{in} = 10^{-3}$, $\beta = 0.2$, $I/C_{out} = 0.1$, $I/C_{cmp} = 0.2$.

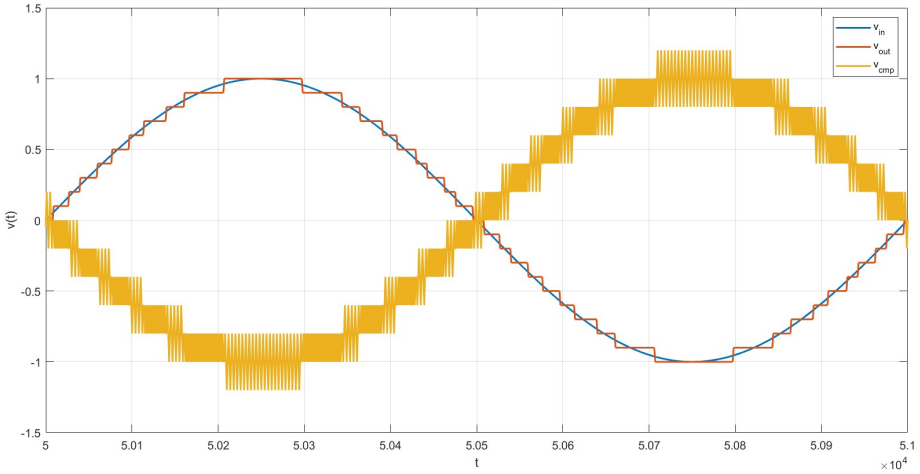


Figure 4.5: Behavior of v_{in}, v_{out} and v_{cmp} with $f_{in} = 10^{-3}$, $\beta = 1$, $I/C_{out} = 0.1$, $I/C_{cmp} = 0.2$.

charged or discharged with a current $I_{out} = I_{cmp}$. Consequently, the voltage across the capacitors may vary as follows:

$$\pm\Delta v_{out} = \frac{I_{out}}{C_{out}} T_{clk}, \qquad \pm\Delta v_{cmp} = \frac{I_{cmp}}{C_{cmp}} T_{clk}.$$

4.2.5 Internal signals

Further insights into the circuit's operation can be obtained by analyzing the waveforms of internal signals on a magnified time scale.

For example, Figure 4.6 shows the behavior of both digital and analog signals in relation to the circuit states.

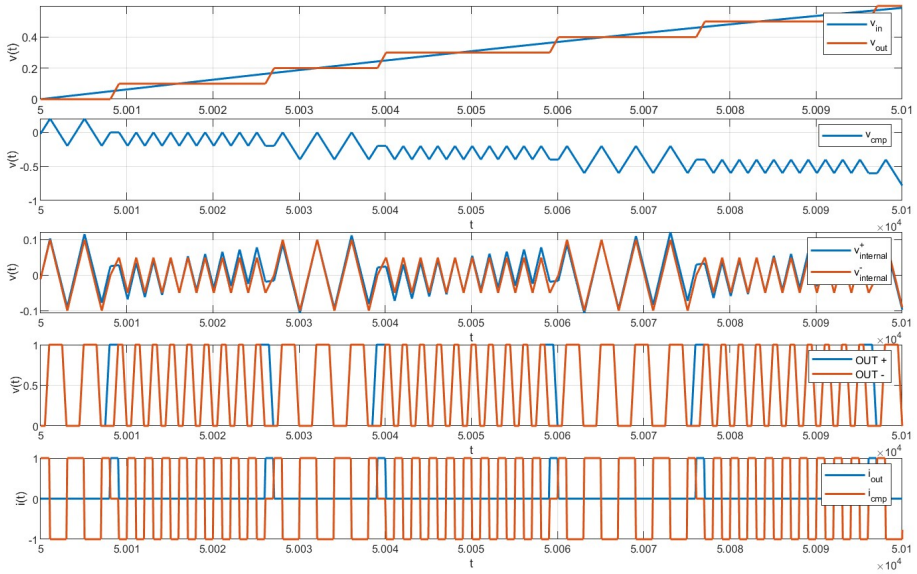


Figure 4.6: Behavior of internal signals with $f_{in} = 10^{-3}$, $\beta = 1$, $I/C_{out} = 0.1$, $I/C_{cmp} = 0.2$.

In particular:

- When $(OUT^+, OUT^-) = (1, 0)$, the output stage is active ($I_{out} = 1$) and the compensation stage is off ($I_{cmp} = 0$).
- When $(OUT^+, OUT^-) = (0, 1)$, the output stage is active ($I_{out} = -1$) and the compensation stage is off ($I_{cmp} = 0$).
- When $(OUT^+, OUT^-) = (1, 1)$, the compensation stage is active ($I_{cmp} = -1$) and the output stage is off ($I_{out} = 0$).
- When $(OUT^+, OUT^-) = (0, 0)$, the compensation stage is active ($I_{cmp} = 1$) and the output stage is off ($I_{out} = 0$).

4.2.6 Frequency analysis

Frequency analysis was performed to verify that the circuit correctly transmits the information contained in the input signal and to study the impact of spurious harmonics.
For the FFT computation, the signal was analyzed only after removing the initial transient, ensuring that the system was in steady-state.

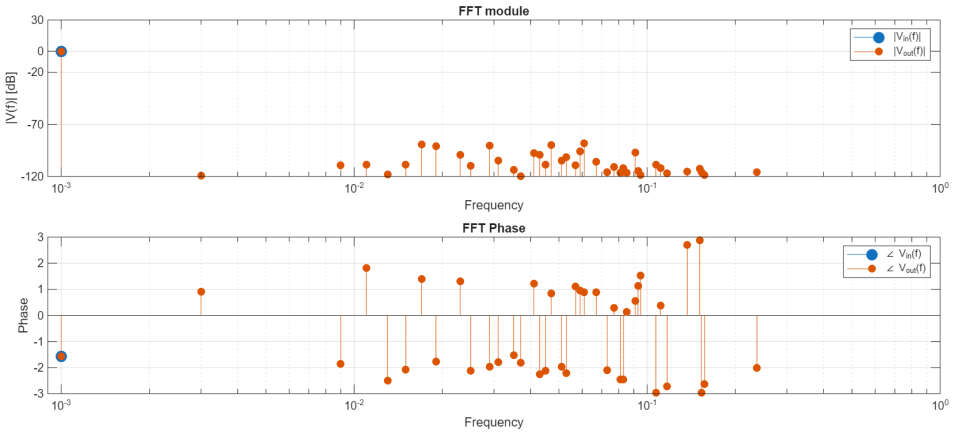


Figure 4.7: FFT of v_{in} and v_{out} with $f_{in} = 10^{-3}$, $\beta = 1$, $I/C_{out} = 0.1$, $I/C_{cmp} = 0.2$.

Figure 4.7 shows the spectra of v_{in} and v_{out}. The fundamental frequency, equal to f_{in}, is preserved in v_{out}, but the output signal exhibits a significant number of spurious harmonics compared to the input. Their presence directly indicates the distortion introduced by the circuit.

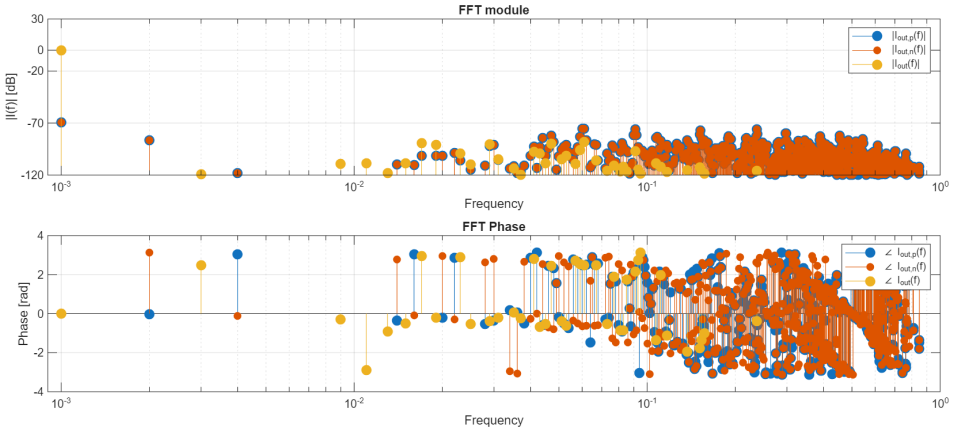


Figure 4.8: FFT of I_{out}, $I_{out,p}$ and $I_{out,n}$ with $f_{in} = 10^{-3}$, $\beta = 1$, $I/C_{out} = 0.1$, $I/C_{cmp} = 0.2$.

Figure 4.8 shows the spectrum of the output current I_{out}, together with the individual transistor currents: that of the pMOS ($|I_{out,p}|$) and the nMOS ($|I_{out,n}|$). It is observed that the fundamental frequency f_{in} is preserved in all currents. Some of the spurious harmonics of $|I_{out,p}|$ and $|I_{out,n}|$ are partially compensated in the total current $I_{out} = |I_{out,p}| - |I_{out,n}|$.

The frequency analysis confirms that the circuit is capable of transmitting the information at the fundamental frequency f_{in}, but the presence of spurious harmonics in the output signals is a critical aspect. Optimizing the circuit parameters, particularly the ratios I/C_{out} and I/C_{cmp}, and choosing an appropriate operating bandwidth, is essential to reduce distortion and improve system performance.

4.3 Bode Diagram

Calculation Method

To compute the Bode diagram of this nonlinear circuit, the following steps are performed:

1. Simulation of the nonlinear circuit using a sinusoidal input signal with variable frequency f_{in} ($v_{\text{in}} = \sin(2\pi f_{\text{in}} t)$) to obtain the corresponding output v_{out}.

2. FFT of v_{in} and v_{out} is computed, considering only their steady-state behavior after removing the transient.

3. The gain is calculated as the ratio between the amplitude of the FFT of v_{out} and that of v_{in} at the fundamental frequency f_{in}:

$$|H(f_{\text{in}})| = \frac{|V_{\text{out}}(f_{\text{in}})|}{|V_{\text{in}}(f_{\text{in}})|}.$$

4. The phase is computed as the difference between the phase of the output and the input signals at the fundamental frequency:

$$\angle H(f_{\text{in}}) = \angle V_{\text{out}}(f_{\text{in}}) - \angle V_{\text{in}}(f_{\text{in}}).$$

5. These steps are repeated for several input frequencies, covering the desired frequency range.

Circuit Behavior

When $f_{\text{in}} > f_t$, the output signal v_{out} is no longer able to follow the input signal v_{in} due to the slew rate limitation. As a result, the amplitude of the fundamental

harmonic in the FFT of v_{out} is lower than that of v_{in}.

It should be noted that the Bode diagram calculated this way considers only the fundamental harmonic and completely neglects higher frequency components that may arise from signal distortion.

Effects of Parameter Variation

- **Variation of $\frac{I_{\text{out}}}{C_{\text{out}}}$ with constant α**
  Increasing $\frac{I_{\text{out}}}{C_{\text{out}}}$ while keeping α constant results in an increase of f_t. This is due to the increased slew rate limit, as shown in the following figures:

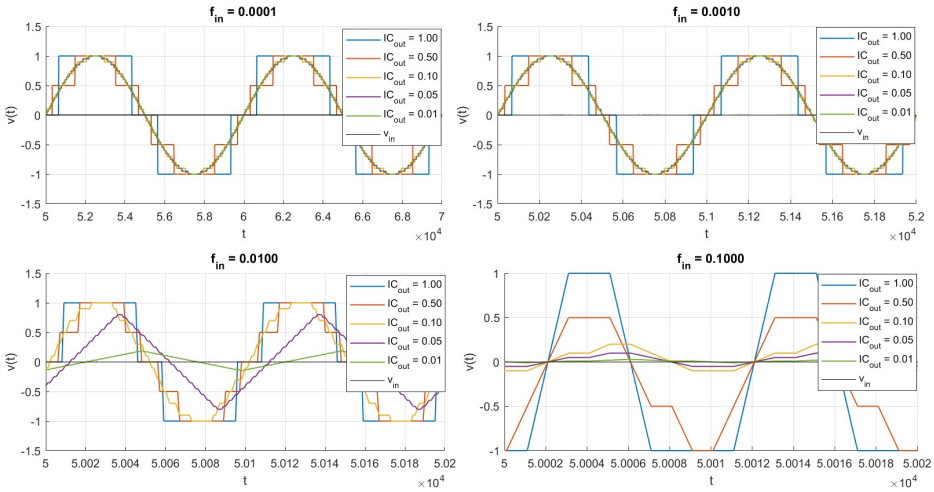


Figure 4.9: Behavior of v_{out} for different values of $\frac{I_{\text{out}}}{C_{\text{out}}}$ with $\beta = 1$, $\alpha = 0.5$.

- **Variation of α with constant $\frac{I_{\text{out}}}{C_{\text{out}}}$**

  Keeping $\frac{I_{\text{out}}}{C_{\text{out}}}$ constant, increasing α results in a decrease of $\frac{I_{\text{cmp}}}{C_{\text{cmp}}}$, and consequently, a decrease of f_t. This behavior is illustrated in the following figures:

- **Influence of Input Signal Amplitude**

  For input signals with smaller amplitude, f_t increases since the slew rate limitation has less effect on the signal. This behavior is illustrated in the following figures:

The computed Bode diagram does not account for the distortion of the v_{out} signal, which becomes particularly significant for high values of $\frac{I_{\text{out}}}{C_{\text{out}}}$ relative to the

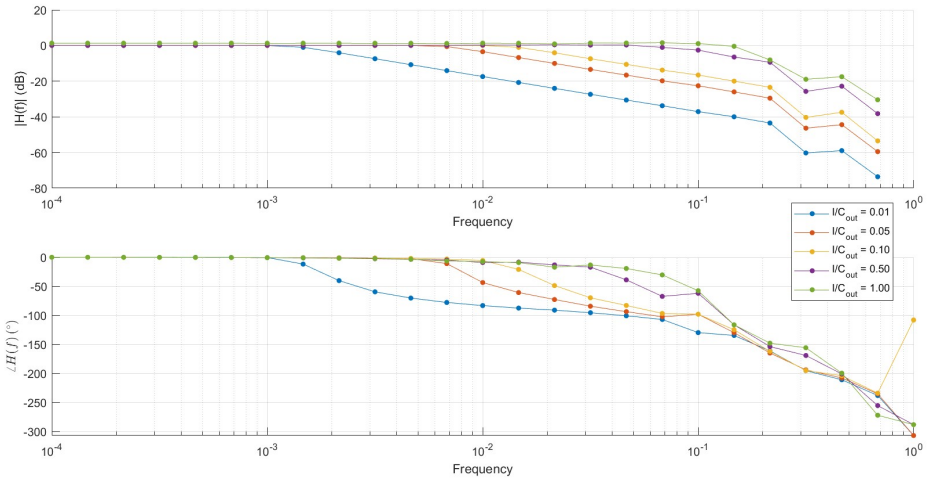


Figure 4.10: Bode diagram for different values of $\frac{I_{\text{out}}}{C_{\text{out}}}$ with $\beta = 1$, $\alpha = 0.5$.

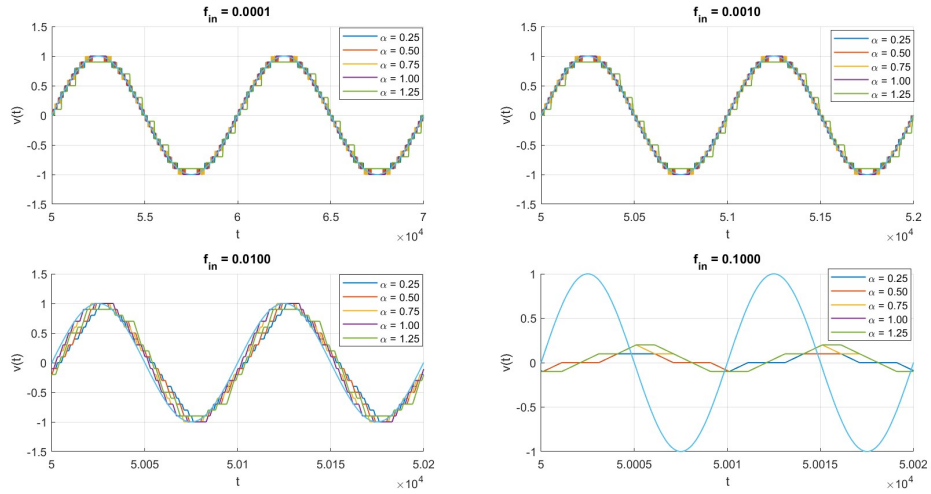


Figure 4.11: Behavior of v_{out} for different values of α with $\beta = 1$, and constant $\frac{I_{\text{out}}}{C_{\text{out}}}$.

input signal amplitude. Specifically:

$$\text{If } \frac{I_{\text{out}}}{C_{\text{out}}} > |A_{\text{in}}| \implies v_{\text{out}} \text{ is amplified and distorted.}$$

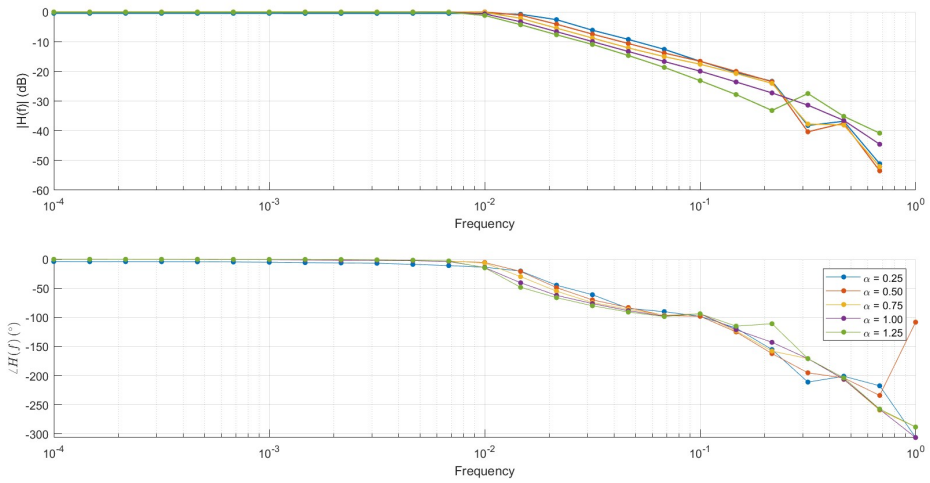


Figure 4.12: Bode diagram for different values of α with $\beta = 1$, and constant $\frac{I_{\text{out}}}{C_{\text{out}}}$.

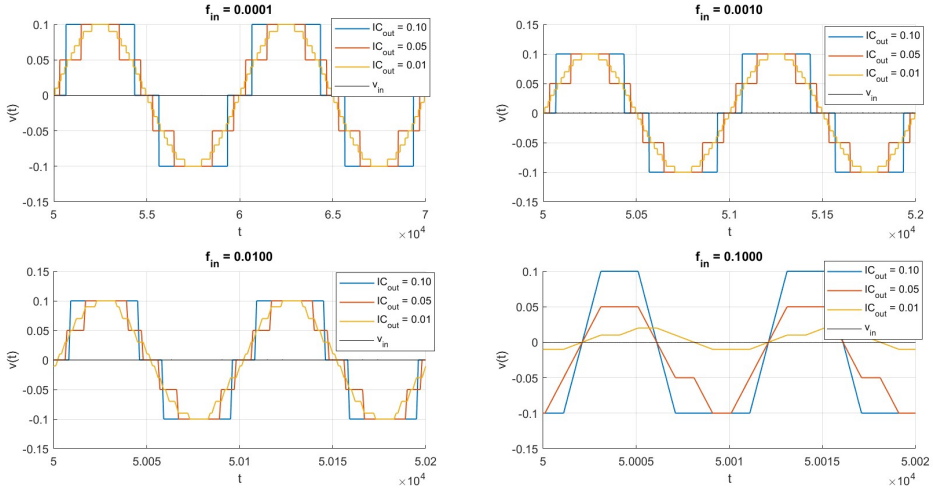
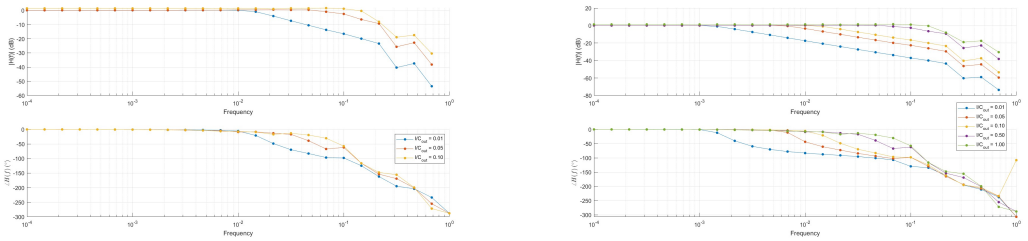


Figure 4.13: Behavior of v_{out} for input signals with reduced amplitude ($v_{\text{in}} = 0.1 \cdot \sin(2\pi f t)$) and $\beta = 1$, $\alpha = 0.5$.

4.4 Differential Gain

The differential gain has been calculated using the same method as for the Bode diagram, but considering $v_d = v_{\text{in}} - \beta v_{\text{out}}$ instead of v_{in}. Therefore, the formulas



(a) $v_{\text{in}} = 0.1 \cdot \sin(2\pi f t)$. **(b)** $v_{\text{in}} = 1 \cdot \sin(2\pi f t)$.

Figure 4.14: Comparison of Bode diagrams for input signals with different amplitudes, $\beta = 1$, $\alpha = 0.5$.

used are the following:

$$|A_d(f_{\text{in}})| = \frac{|V_{\text{out}}(f_{\text{in}})|}{|V_{\text{d}}(f_{\text{in}})|}.$$

$$\angle A_d(f_{\text{in}}) = \angle V_{\text{out}}(f_{\text{in}}) - \angle V_{\text{d}}(f_{\text{in}})$$

It is observed that the differential gain A_d follows a characteristic behavior:

- For low frequencies ($f_{\text{in}} \ll f_t$), A_d decreases with a slope of $-20\,\text{dB/decade}$. In this region, v_{out} is able to correctly reconstruct the input sine wave.
- Near the cutoff frequency f_t, there is a rapid decrease in the differential gain, due to the inability of the v_{out} signal to follow the input signal faithfully due to the limit imposed by the slew rate.
- For higher frequencies ($f_{\text{in}} \gg f_t$), A_d continues to decrease with a slope of $-20\,\text{dB/decade}$. In this region, v_{out} takes on an approximately triangular waveform, caused by the slew rate limitation of the circuit.

4.5 SNDR

To evaluate the distortion of the circuit, the Signal-to-Noise and Distortion Ratio (SNDR) has been calculated for different frequency bands.
The calculation was performed following these steps:

1. **FFT Calculation:** The Fourier transform (FFT) of the output signal v_{out} is calculated after removing the transient part, to consider only the steady-state portion.

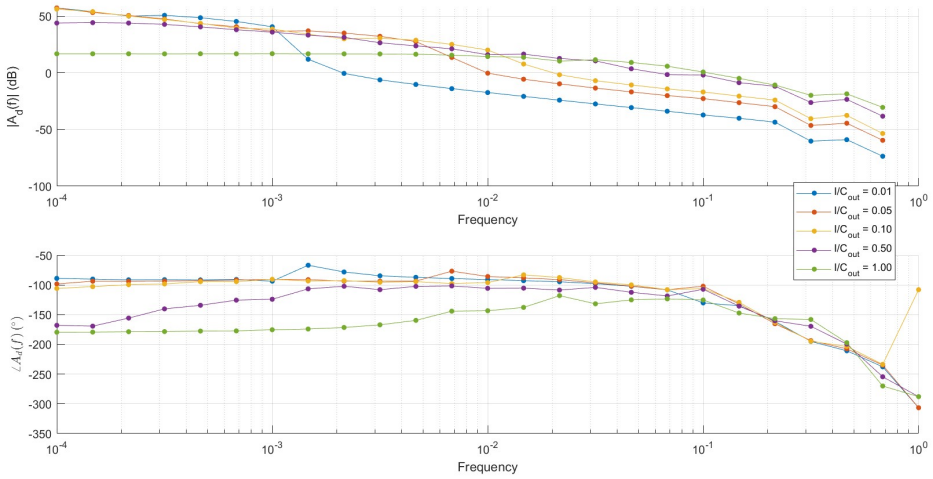


Figure 4.15: Differential gain $A_d(f_{\text{in}})$ for different values of $\frac{I_{\text{out}}}{C_{\text{out}}}$ with $\beta = 1$ and $\alpha = 0.5$.

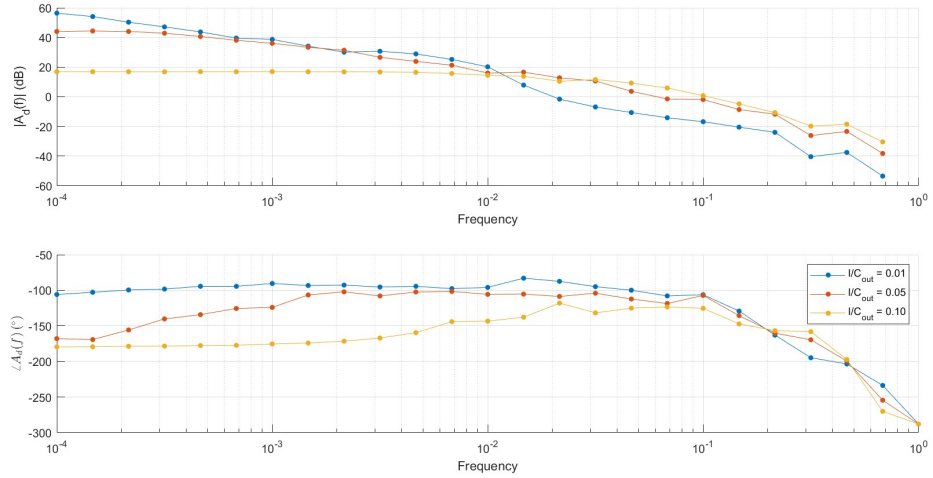


Figure 4.16: Differential gain $A_d(f_{\text{in}})$ for different values of $\frac{I_{\text{out}}}{C_{\text{out}}}$ with $\beta = 1$ and $\alpha = 0.5$.

2. **Signal Power Calculation:** The power of the fundamental signal is calculated, which corresponds to the FFT value at the position of f_{in}:

$$P_{\text{signal}} = |\text{FFT}(v_{\text{out}})(f_{\text{in}})|^2$$

3. **Noise and Distortion Power Calculation:** All spectral components of the FFT within a frequency band B, excluding the fundamental, are considered.

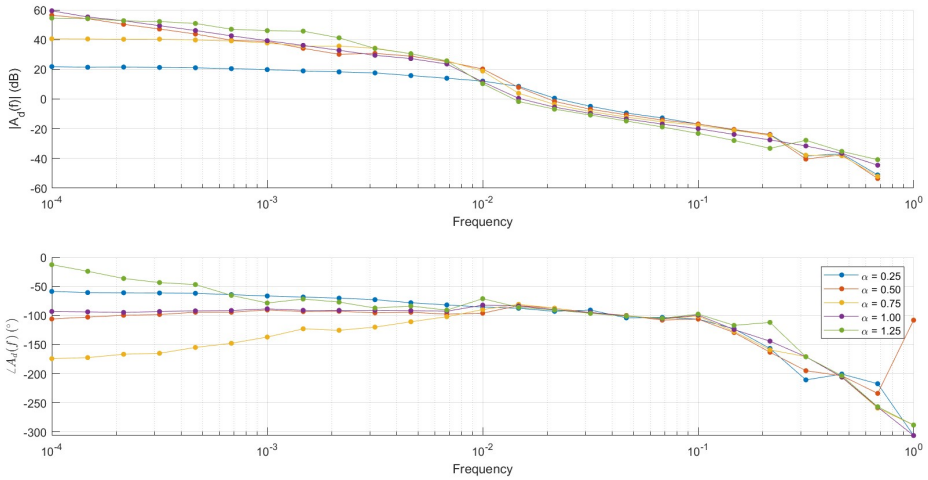


Figure 4.17: Differential gain $A_d(f_{\text{in}})$ for different values of α with $\beta = 1$ and $\frac{I_{\text{out}}}{C_{\text{out}}} = 0.1$.

The power of the residual components is given by:

$$P_{\text{noise and distortion}} = \sum_{f \in B, f \neq f_{\text{in}}} |\text{FFT}(v_{\text{out}})(f)|^2$$

4. **SNDR Calculation:** Using the calculated values of P_{signal} and $P_{\text{noise and distortion}}$, the SNDR is determined as:

$$\text{SNDR} = 10 \cdot \log_{10}\left(\frac{P_{\text{signal}}}{P_{\text{noise and distortion}}}\right)$$

4.5.1 Effects of Parameter Variation

Effects of varying $\frac{I_{\text{out}}}{C_{\text{out}}}$

Considering a range of values where the slew-rate limit does not occur, it was observed that for lower values of the ratio $\frac{I_{\text{out}}}{C_{\text{out}}}$, the SNDR tends to be higher. This is shown in the following figure:

This trend is consistent with the FFT of v_{out}, where it can be seen that for lower values of $I_{\text{out}}/C_{\text{out}}$, the amplitude of the secondary harmonics is smaller:

Effects of varying α

Varying the parameter α, it is observed that the optimal value to maximize SNDR depends on the considered band. Generally, the optimal α lies between 0.5 and 1.

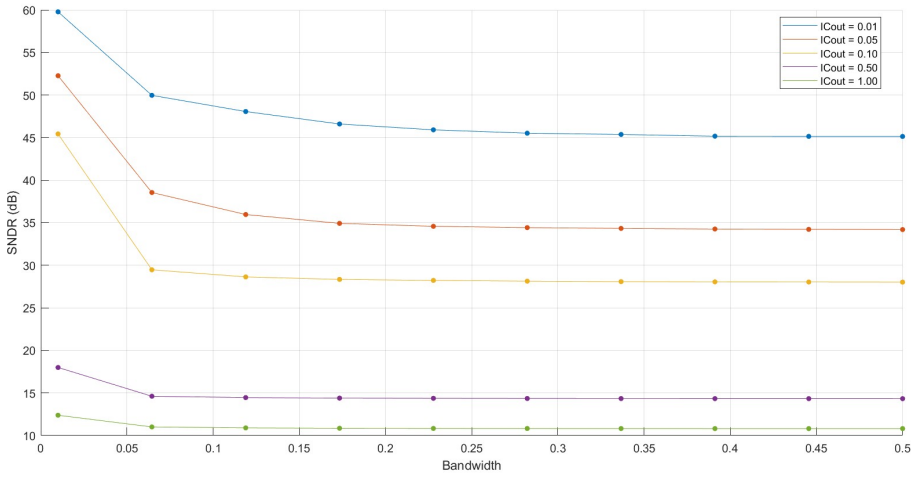


Figure 4.18: SNDR for $\alpha = 0.5$, $\beta = 1$.

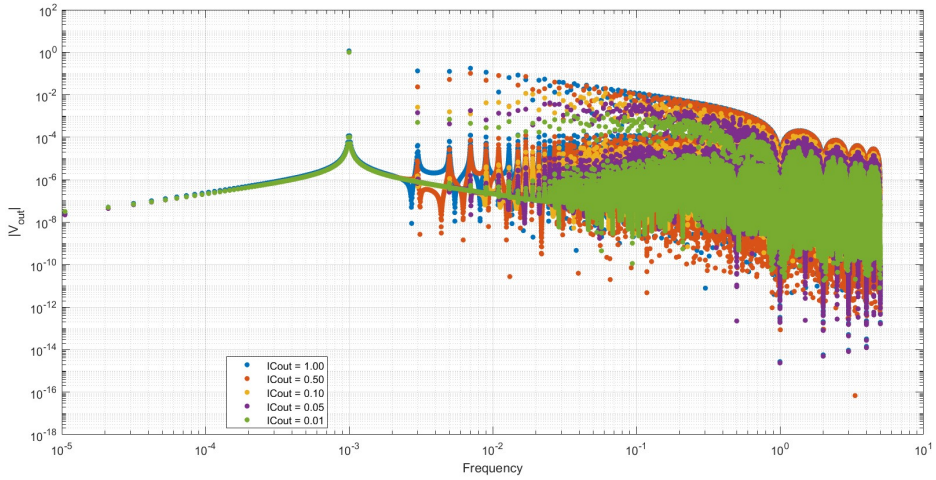


Figure 4.19: FFT of v_{out} for $\alpha = 0.5$, $\beta = 1$.

However, as can be seen in Figure 4.21, for some values of α, the SNDR experiences a sharp drop as the band varies. This behavior is associated with the presence of a peak in the FFT of v_{out} at the normalized frequency $f = 0.25$, as observed in Figure 4.22. This peak is caused by oscillations with a constant period $T = 4T_{clk}$ in the signal v_{out}, as highlighted in the time zoom shown in Figure 4.24.

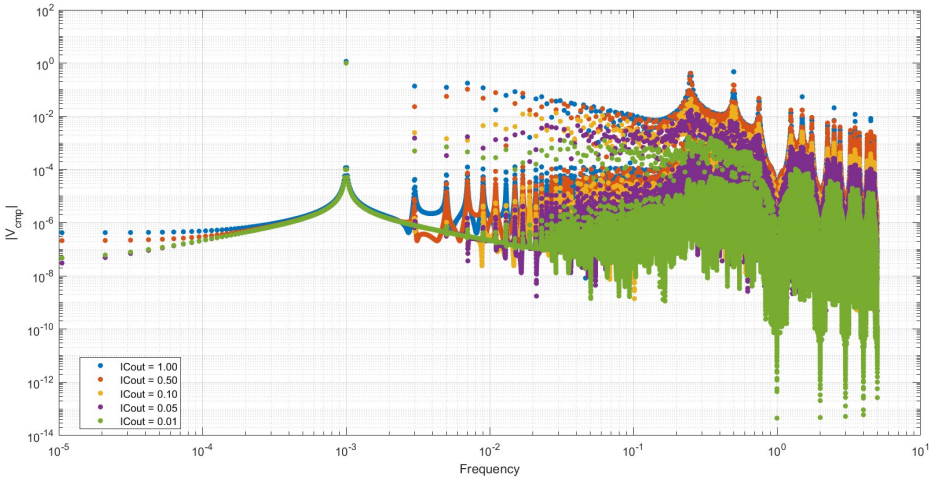


Figure 4.20: FFT of v_{cmp} for $\alpha = 0.5$, $\beta = 1$.

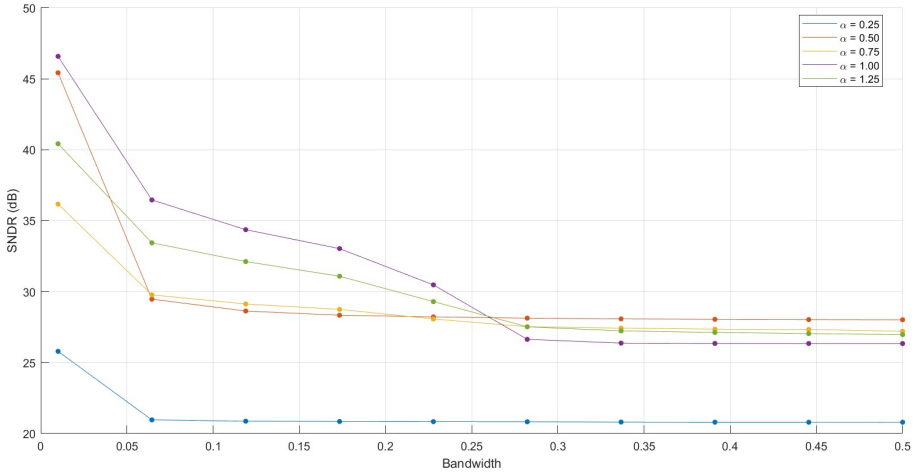


Figure 4.21: SNDR for $\frac{I_{\text{out}}}{C_{\text{out}}} = 0.1$, $\beta = 1$.

4.6 Parameter Dependence

Parameter $\frac{I_{\text{out}}}{C_{\text{out}}}$

The parameter $\frac{I_{\text{out}}}{C_{\text{out}}}$ plays a crucial role in the circuit's behavior. We analyze its effects in two extreme cases:

- Low values of $\frac{I_{\text{out}}}{C_{\text{out}}}$:

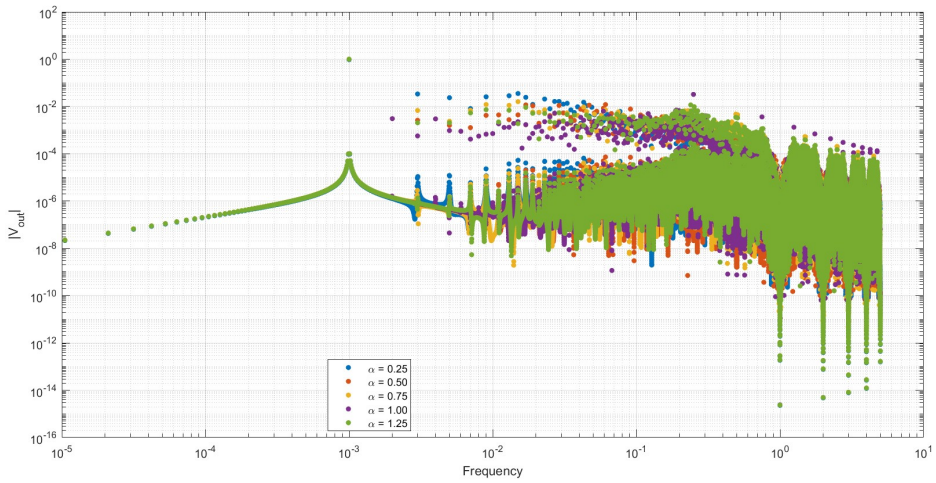


Figure 4.22: FFT of v_{out} for $\frac{I_{\text{out}}}{C_{\text{out}}} = 0.1$, $\beta = 1$.

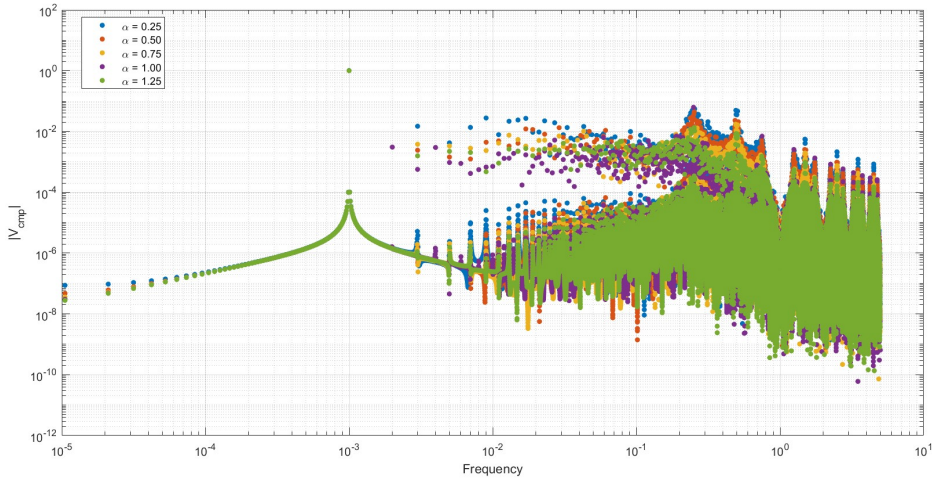


Figure 4.23: FFT of v_{cmp} for $\frac{I_{\text{out}}}{C_{\text{out}}} = 0.1$, $\beta = 1$.

  - Higher SNDR values are observed, indicating lower harmonic distortion.
  - The cutoff frequency f_t is lower, resulting in a narrower passband.

- High values of $\frac{I_{\text{out}}}{C_{\text{out}}}$:
  - The cutoff frequency f_t increases, improving the slew rate limit.
  - Lower SNDR values are observed, due to a greater contribution from unwanted harmonics, leading to increased distortion.

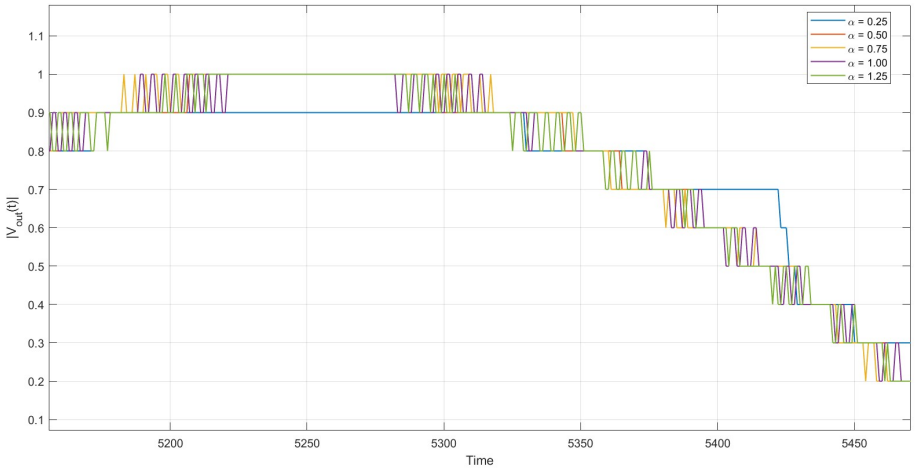


Figure 4.24: Zoom of $v_{\text{out}}(t)$ for $\frac{I_{\text{out}}}{C_{\text{out}}} = 0.1$, $\beta = 1$.

Effects of the α parameter

To study the effect of the parameter α, and hence $\frac{I_{\text{cmp}}}{C_{\text{cmp}}}$, we compared the DB-OTA circuit with a simplified circuit containing only an ideal comparator (without the compensation block).

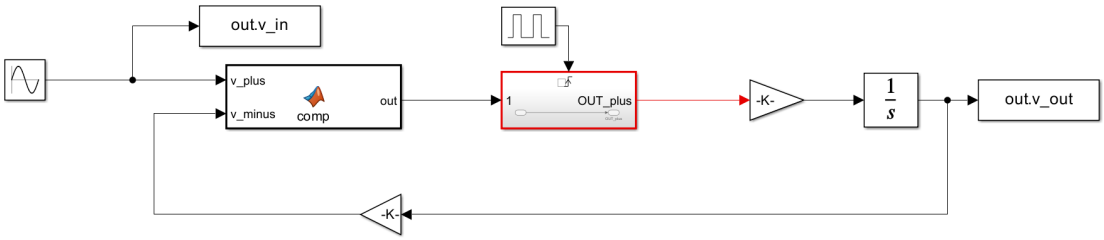


Figure 4.25: Circuit diagram implemented with an ideal comparator.

By calculating the FFT of v_{out} for the circuit with the ideal comparator (Figure 4.26), a significant peak is observed at frequency $f = 0.5$. This occurs because, in the absence of the compensation block, the output stage remains constantly active, generating oscillations with a period equal to $2T_{\text{clk}}$. On the other hand, in the circuit with the compensation block, the oscillations can have shorter periods since the output stage turns off when the compensation block is active, and consequently, the FFT of v_{out} may show peaks at lower frequencies.

The circuit's behavior was also compared in terms of Bode plot, differential gain,

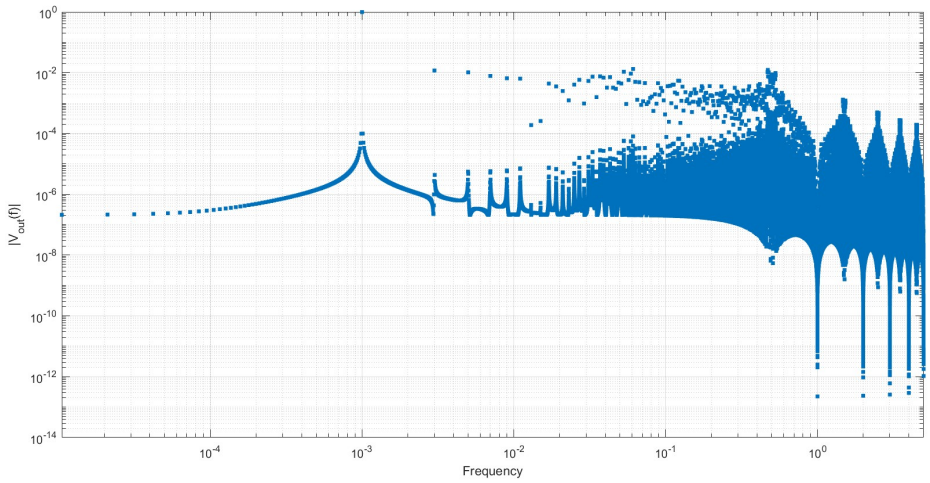


Figure 4.26: FFT of $v_{\text{out}}(t)$ calculated with an ideal comparator for $\frac{I_{\text{out}}}{C_{\text{out}}} = 0.1$, $\beta = 1$.

and SNDR, as shown in Figures 4.27, 4.28, and 4.29. From these simulations, the following observations emerge:

- For the Bode plot (Figure 4.27), the gain is constant up to the cutoff frequency f_t, after which it decreases at -20 dB/decade. However, in the case of the ideal comparator, f_t is higher, as the slew rate limit occurs at higher frequencies.
- The differential gain (Figure 4.28) also shows a similar trend between the DB-OTA and the ideal comparator, changing near the cutoff frequency f_t, where a shift in the trend occurs.
- For the SNDR (Figure 4.29), a relatively constant behavior is observed with some differences in narrow bands and in the band $B = 0.5 f_{\text{clk}}$, due to the peak present at that frequency. It is interesting to note that, for certain DB-OTA configurations (specific values of α) and for certain bands, SNDR values can exceed those of the ideal comparator.

To analyze the effect of α in the DB-OTA, we compared the amplitude and frequency of the main harmonic following the fundamental in the FFTs of v_{out}. The results are shown in Figures 4.30 and 4.31.

From the previous plots, calculated respectively for $\frac{I_{\text{out}}}{C_{\text{out}}} = 0.1$ and $\frac{I_{\text{out}}}{C_{\text{out}}} = 0.05$, it is evident that:

- For $\alpha = 1$, the main harmonic following the fundamental is at a high frequency, but its amplitude is not negligible.

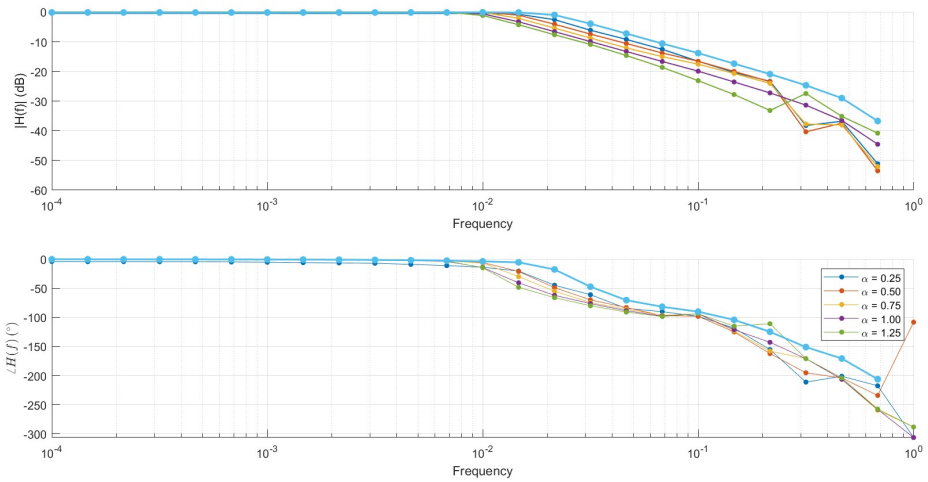


Figure 4.27: Bode plot comparison for DB-OTA and ideal comparator for $\frac{I_{\text{out}}}{C_{\text{out}}} = 0.1$, $\beta = 1$.

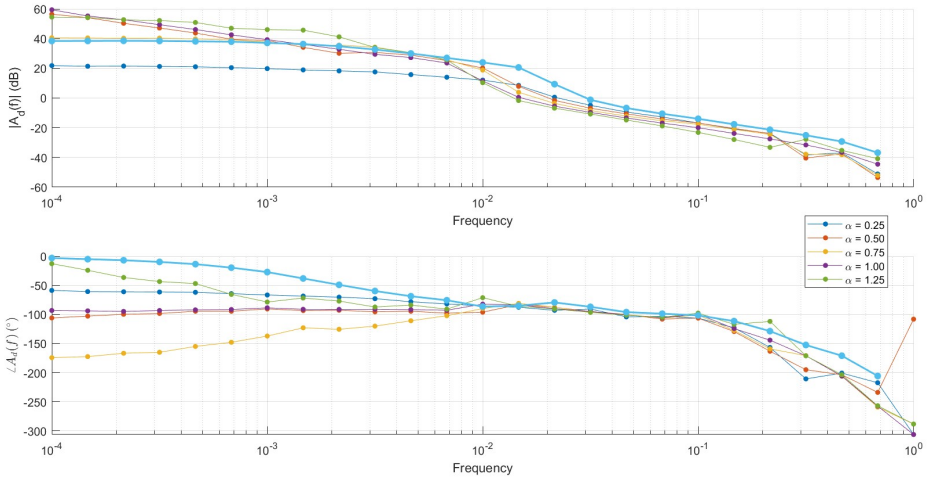


Figure 4.28: Comparison of A_d for DB-OTA and ideal comparator for $\frac{I_{\text{out}}}{C_{\text{out}}} = 0.1$, $\beta = 1$.

- For $\alpha = 0.5$, the main harmonic following the fundamental is at a lower frequency, but its amplitude is not necessarily smaller than the one obtained with the ideal comparator.

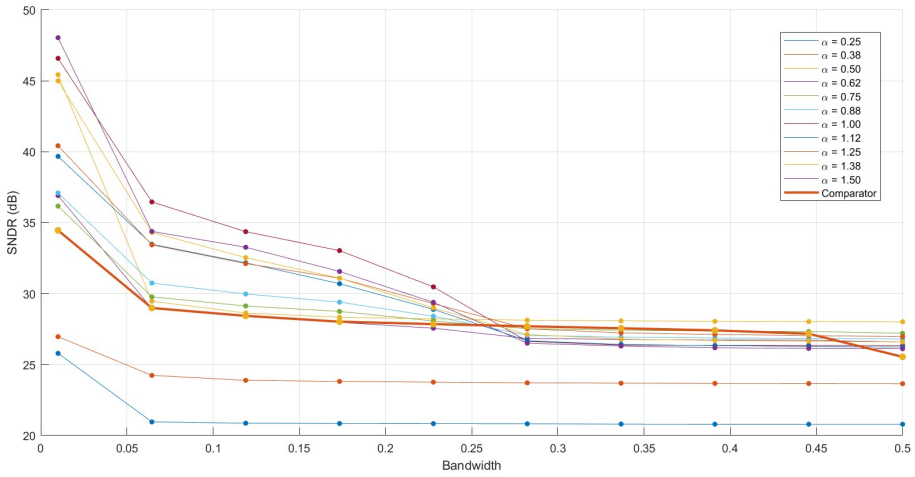


Figure 4.29: SNDR comparison for DB-OTA and ideal comparator for $\frac{I_{\text{out}}}{C_{\text{out}}} = 0.1$, $\beta = 1$.

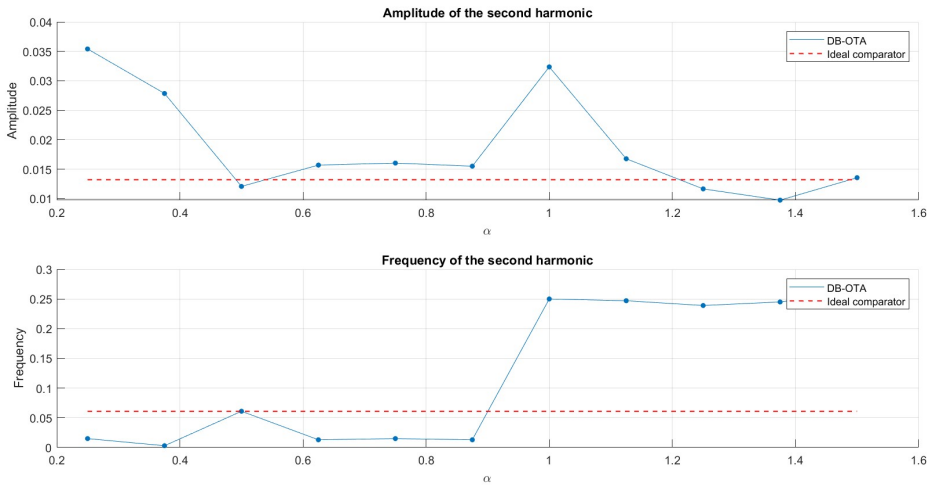


Figure 4.30: Amplitude and frequency of the main harmonic following the fundamental for DB-OTA and ideal comparator with $\frac{I_{\text{out}}}{C_{\text{out}}} = 0.1$, $\beta = 1$.

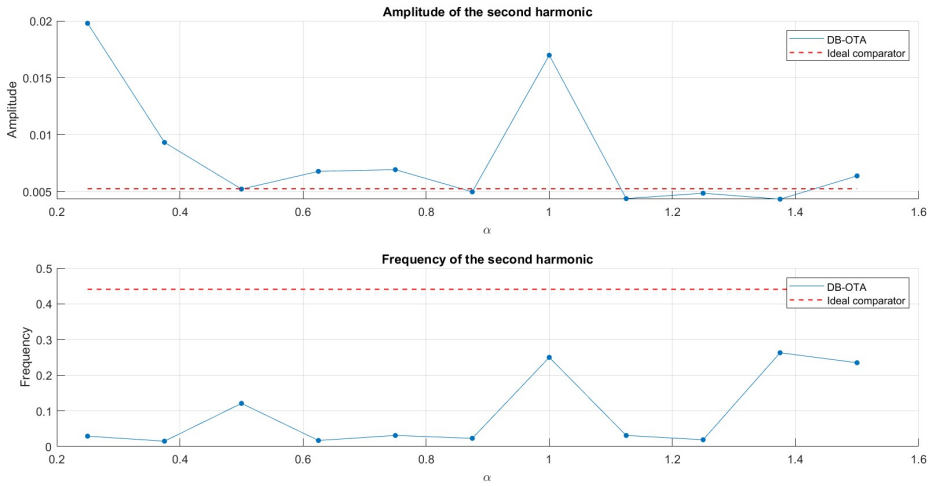


Figure 4.31: Amplitude and frequency of the main harmonic following the fundamental for DB-OTA and ideal comparator with $\frac{I_{\text{out}}}{C_{\text{out}}} = 0.05$, $\beta = 1$.

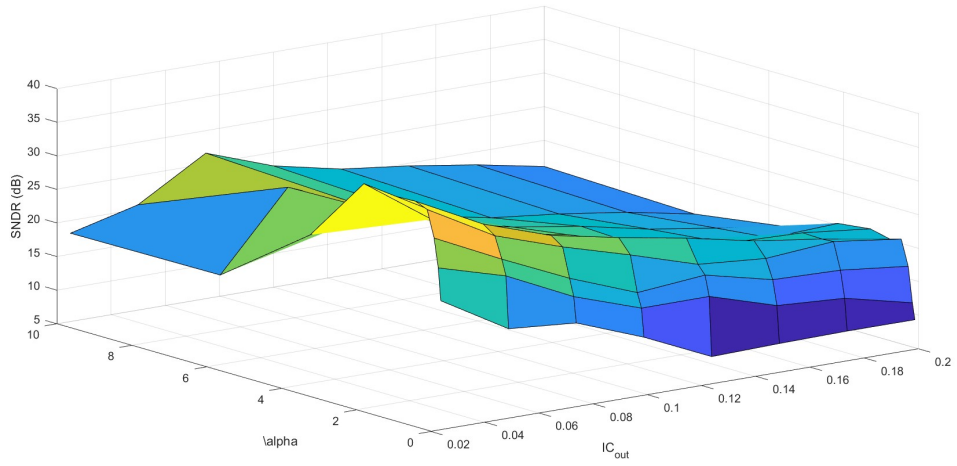


Figure 4.32: Higher SNDR $SNDR = 38$ for $\frac{I_{\text{out}}}{C_{\text{out}}} = 0.025$ and $\alpha = 2$.

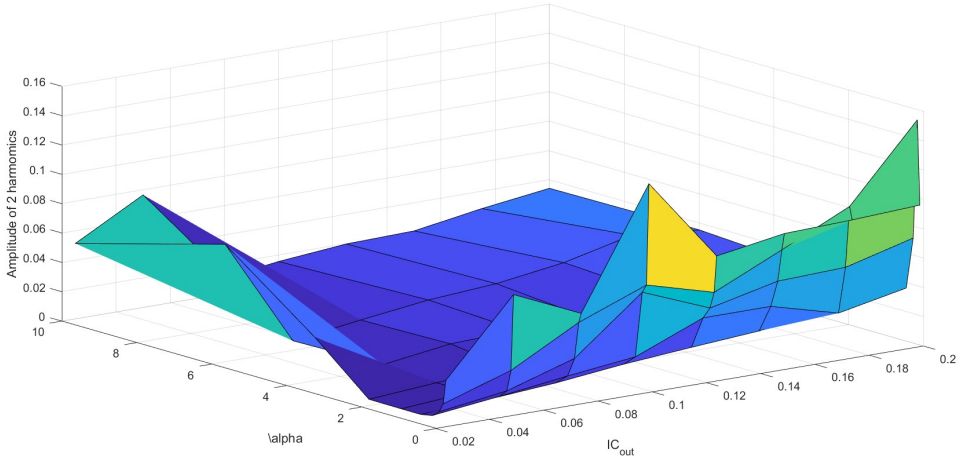


Figure 4.33: Lower amplitude of the second harmonic for $\frac{I_{\text{out}}}{C_{\text{out}}} = 0.025$ and $\alpha = 0.75$.

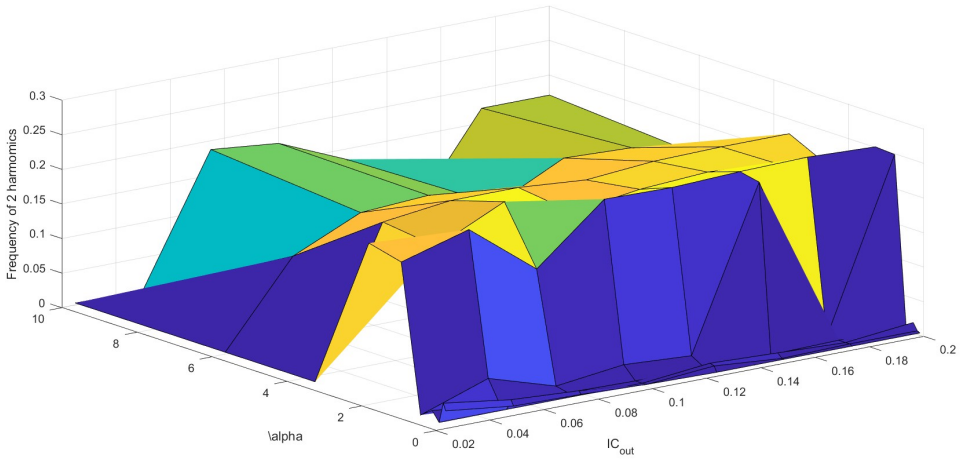


Figure 4.34: Highest frequency of the second harmonic for $\frac{I_{\text{out}}}{C_{\text{out}}} = 0.17$ and $\alpha = 1.3$.

Chapter 5

Circuit Design

5.1 CEREBRO project

The EU-funded CEREBRO project aims to develop the first EEG contrast medium capable of enabling non-invasive, full-brain imaging with higher spatial resolution than conventional techniques.

The core idea is to measure neuron-induced electrical potentials through electrodes placed in close proximity to neurons, and then transmit this information to external electrodes at higher frequencies, as illustrated in Figure 5.1. By shifting the signal to a higher frequency range, this approach reduce the attenuation typically introduced by the skull.

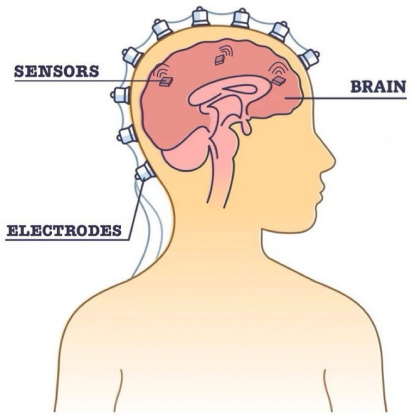


Figure 5.1: Overview of the CEREBRO system.

Due to the target application, the circuit must meet strict constraints in terms of

silicon area and power consumption. In the final implementation, it is expected to be extremely miniaturized (approximately 10x10 µm) to avoid clogging within brain tissue, and to operate at ultra-low power (in the sub-nanowatt range), allowing for remote powering.
However, during this initial design phase, these constraints are relaxed, in particular the circuit is powered externally via wires, and its shape is designed to be narrow and elongated, so it can be manually placed close to the target neuron.
The main design specifications considered in this work are summarized in Table 5.1.

Input signal	10 - 50 µV
Bandwidth	10 Hz - 1 kHz
Transmission frequency	95–105 kHz
Supply voltage	±0.3 V
Maximum area	≈ 10x100 μm^2

Table 5.1: Specification for CEREBRO circuit.

The objective of this thesis is to design a Digital-Based Operational Transconductance Amplifier (DIGOTA), to serve as the analog front-end for neural signal acquisition and frequency up-conversion within the CEREBRO system.

The circuit was developed in Cadence Virtuoso, using TSMC 180 nm CMOS technology, with the goal of satisfying the project requirements in terms of signal-to-noise ratio, gain, working frequency, and, in particular, area and power consumption.

To achieve this, the design adopts a digital-based architecture, which exploits logic gates to implement a traditional analog block. Since this approach avoids the need for bias currents, it naturally leads to lower power consumption and a smaller silicon footprint.

Moreover, the self-oscillating behavior of DIGOTA is directly exploited to generate a high-frequency output in the form of a pulse train. This eliminates the need for separate voltage-controlled oscillator (VCO) and driver blocks, contributing to significant savings in both power and silicon area.

Another innovative aspect of this design is the implementation of the amplifier's feedback network by exploiting the electrical properties of the electrodes and the surrounding biological solution, as illustrated in Figure 5.2. This strategy significantly reduces silicon area by eliminating the need for integrated resistors and capacitors.

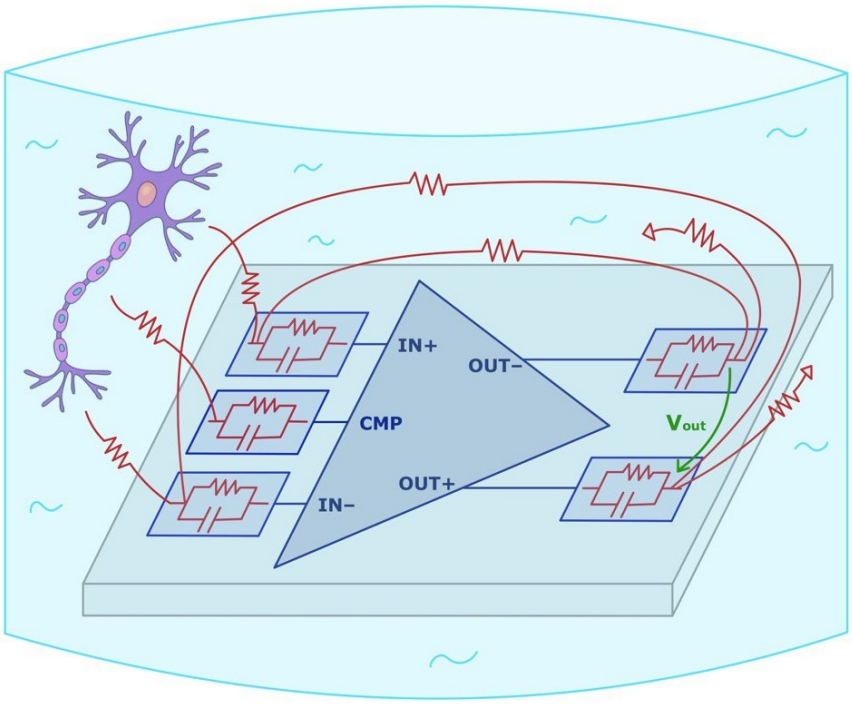


Figure 5.2: Overview of the proposed system configuration.

The design process followed a structured and progressive approach. In the initial phase, a standard DIGOTA configuration was implemented, following the configuration already proposed and studied in the literature, to meet the main design specifications.

Once the baseline performance was validated, the design was extended by incorporating electrode models into the DIGOTA configuration. This allowed for a more accurate simulation of the circuit's behavior in real operating conditions and so it is optimized for the target application.

As a final step, the electrodes were integrated into the layout, with their geometry and placement carefully optimized to reproduce the electrical behavior described in the model.

5.2 DIGOTA topology

As first phase of the design, the DIGOTA schematic was implemented without passive elements, using components from the *tsmc18* library. The resulting topology is shown in Figure 5.3.

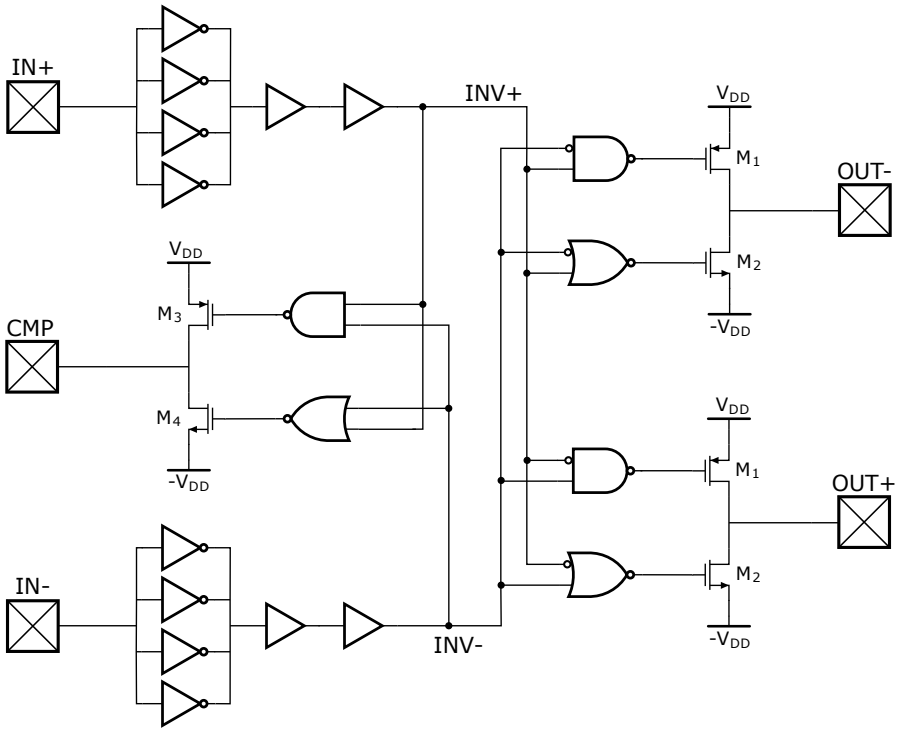


Figure 5.3: DIGOTA topology

The circuit consists of five electrodes: the non-inverting input IN+, the inverting input IN-, the two differential outputs OUT+ and OUT-, and the common-mode output CMP. The architecture is organized into three main stages:

- **Input stage:** It includes two identical branches, each composed of four parallel inverters followed by two series buffers.
  The outputs of these stages are INV+ and INV-, which respond to the input signals IN+ and IN- as summarized in the Table 5.2.

IN+	IN-	INV+	INV-
> 0	> 0	0	0
> 0	< 0	0	1
< 0	> 0	1	0
< 0	< 0	1	1

Table 5.2: Truth table of the DIGOTA input stage.

- **Compensation stage:** This stage is based on a tri-state buffer made of a pMOS transistor (M_3) and an nMOS transistor (M_4), controlled respectively

by the outputs of a NAND and a NOR gate.
Based on the signals INV+ and INV- from the input stage, the behavior of this block and the current flowing through the CMP electrode is described in the Table 5.3.

INV+	INV-	NAND out	NOR out	pMOS M_3	nMOS M_4	I_{cmp}
0	0	1	1	OFF	ON	0
0	1	1	0	OFF	OFF	< 0
1	0	1	0	OFF	OFF	> 0
1	1	0	0	ON	OFF	0

Table 5.3: Truth table of the DIGOTA compensation stage.

- **Output stages:** The circuit includes two complementary output branches, each implemented with a tri-state buffer made of one pMOS (M_1) and one nMOS (M_2) transistor. These are driven respectively by a NAND gate (with one inverted input) and a NOR gate (with one inverted input).
  The two branches receive complementary input signals: the non-inverting branch uses $\overline{\text{INV+}}$ and INV-, while the inverting branch uses INV+ and $\overline{\text{INV}-}$ as inputs to the logic gates.
  The differential structure ensures complementary behavior between the two outputs (OUT+ and OUT-) in order to improve dynamic range.
  The behavior of the non-inverting and inverting output stages are summarized in Table 5.4.

INV+	INV-	NAND+ out	NOR+ out	pMOS M_1+	nMOS M_4+	$I_{\text{out}+}$
0	0	1	0	OFF	OFF	0
0	1	0	0	ON	OFF	> 0
1	0	1	1	OFF	ON	< 0
1	1	1	0	OFF	OFF	0

INV+	INV-	NAND- out	NOR- out	pMOS M_1-	nMOS M_2-	$I_{\text{out}-}$
0	0	1	0	OFF	OFF	0
0	1	1	1	OFF	ON	< 0
1	0	0	0	ON	OFF	> 0
1	1	1	0	OFF	OFF	0

Table 5.4: Truth table of the DIGOTA output stages.

5.3 Conventional configuration

After the circuit was designed at schematic level, a series of transient simulations was carried out on ADE Enviroment to test and optimize the circuit so that it could meet the target specifications.

These tests were carried out using the standard DB-OTA architecture in a non-inverting differential configuration, shown in Figure 5.4. The testbench includes ideal resistors and capacitors to emulate the summing network, the output and compensation stages, and the amplifier feedback loop.

The ideal gain of this configuration is:

$$G = \frac{R_f}{R_{in}}. \tag{5.1}$$

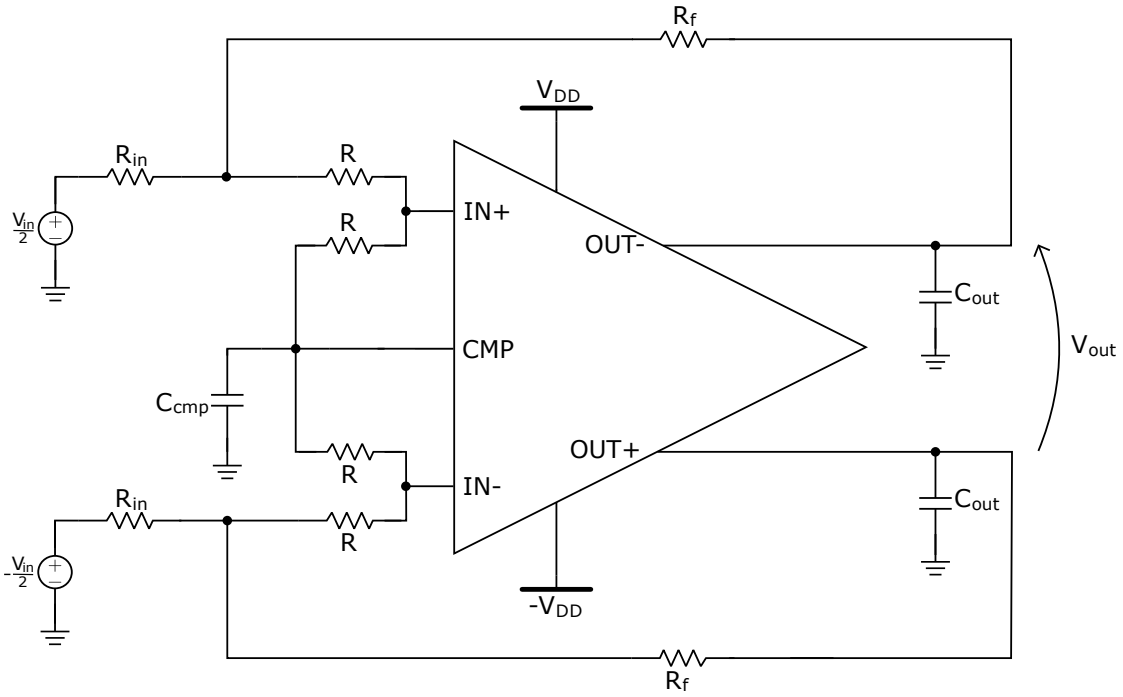


Figure 5.4: Differential configuration

5.3.1 Circuit behavior and internal signals

Internal signals were plotted to verify the correct operation of each block in the architecture. The design parameters used in this test are reported in the Table 5.5.

The circuit was tested by applying a sinusoidal input at 1 kHz, which corresponds to the upper limit of the required operating bandwidth and with amplitude of

Parameters	Value
$L_{\text{out}} = L_{\text{cmp}}$	440 nm
$W_{\text{out,n}} = W_{\text{cmp,n}}$	220 nm
$W_{\text{out,p}} = W_{\text{cmp,p}}$	440 nm
R_{in}	10 MΩ
R	1 GΩ
R_f	1 GΩ
$C_{\text{out}} = C_{\text{cmp}}$	300 pF

Table 5.5: Design parameters of the DIGOTA circuit.

10 µV and 100 µV, which match the extremes of the input range specified for neural signal acquisition.

As shown in Figure 5.5, the amplifier is able to reconstruct the input signal with a maximum gain of approximately 30 dB for the smaller input amplitude and around 37 dB for the larger one.

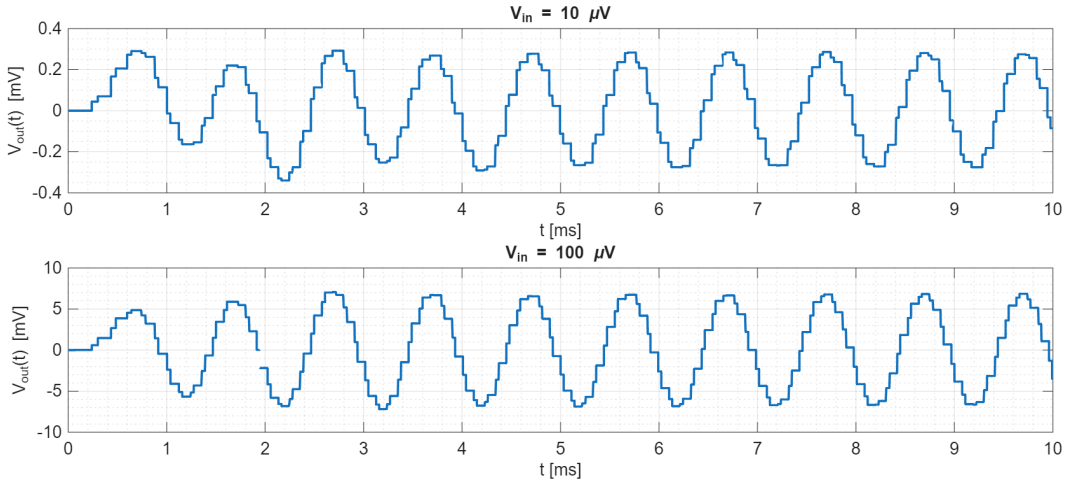


Figure 5.5: Differential output V_{out} for different input amplitudes

The internal signal behavior is illustrated in Figures 5.6 and 5.7.

Figure 5.6 shows a zoomed view of the INV+ and INV- signals, which are generated by a chain of inverters and buffers that convert the analog inputs into a square waves. They then drive the NAND and NOR gates, which control the gates of the pMOS and nMOS transistors in both the compensation and output stages. The behavior of these signals is consistent with the logic described in the previous truth tables.

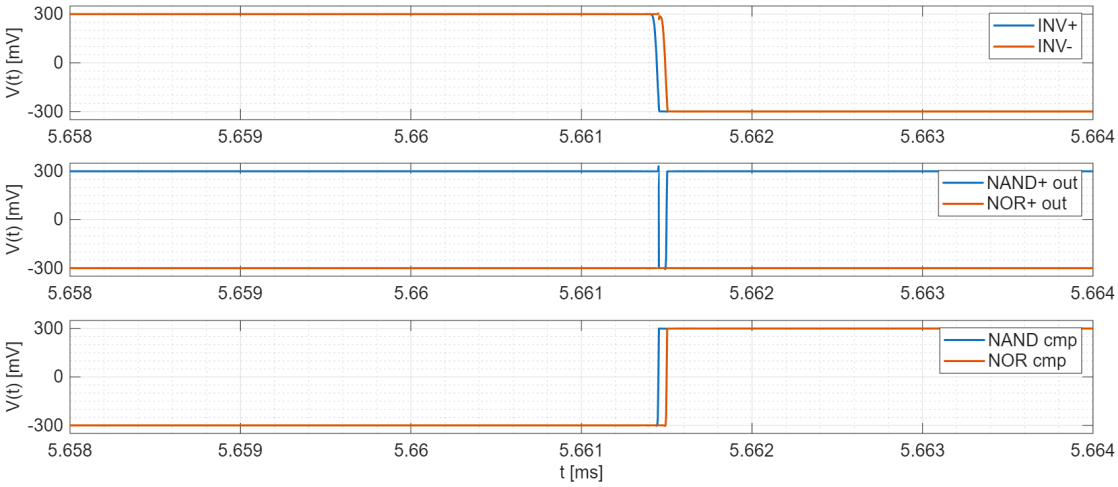


Figure 5.6: INV+ and INV- logic signals and gate voltage signals for output and compensation transistors.

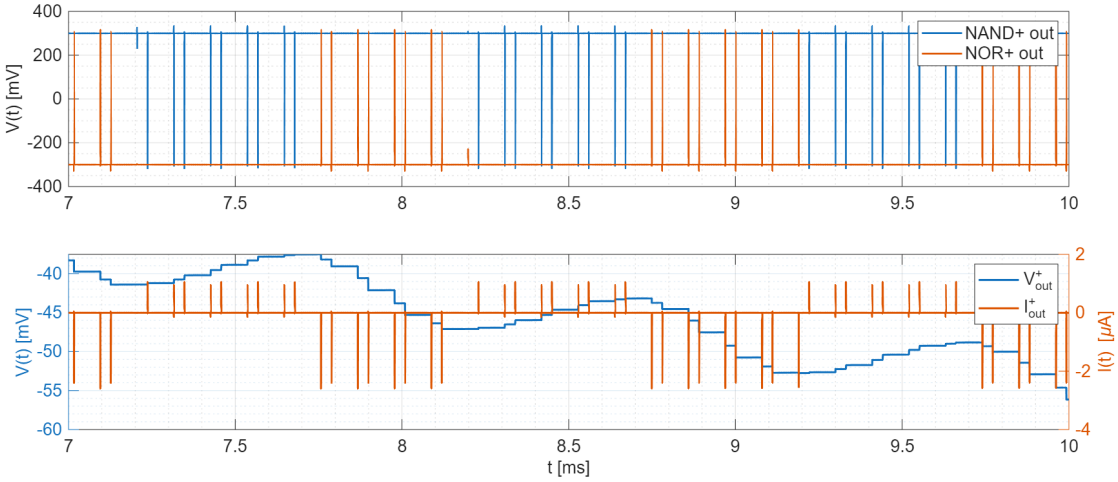


Figure 5.7: Output stage logic signals and resulting V^+_{out} and I^+_{out} signals.

Figure 5.7 shows the outputs of the NAND and NOR gates in the positive output stage. These gates generate short pulses that turn the pMOS or nMOS transistors ON, creating current spikes that charge or discharge the output capacitor C_{out}, respectively. As a result, V^+_{out} is a staircase waveform that follows the shape of the input signal. A complementary process occurs in the negative output stage.

Consequently, as shown in Figure 5.8, the differential output $V_{out} = V^+_{out} - V^-_{out}$ amplifies the differential input signal while rejecting the common-mode component and compensating for the mismatch between the amplitude of output current of pMOS and nMOS.

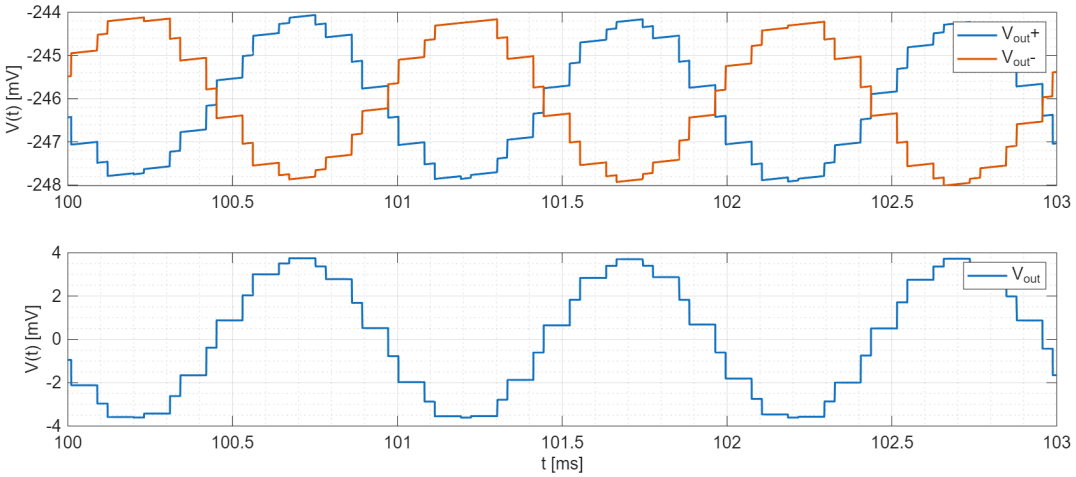


Figure 5.8: V_{out}^{+}, V_{out}^{-} and V_{out} signals.

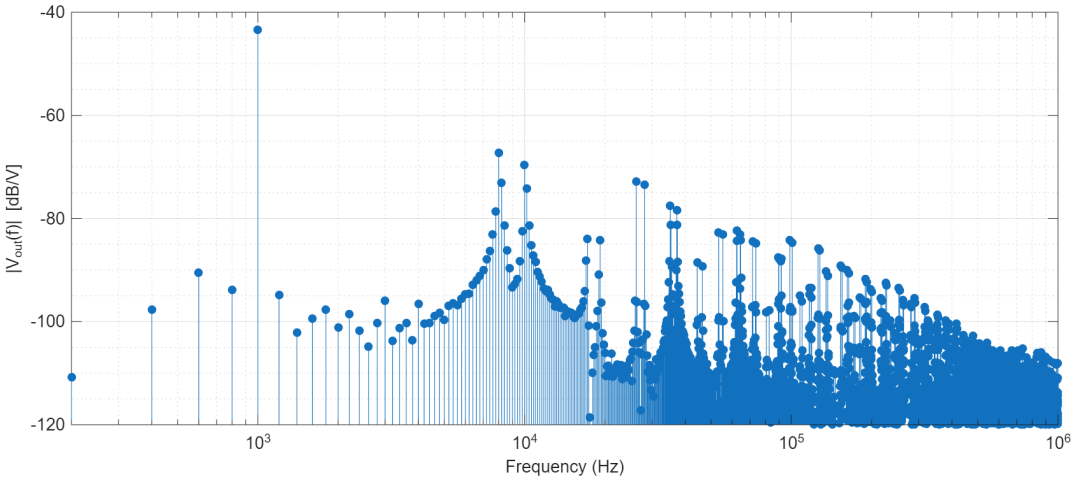


Figure 5.9: FFT Magnitude of V_{out}

By analyzing the FFT of the output signal V_{out}, shown in Figure 5.9, it is possible to verify that the main information is preserved: in fact, the fundamental peak is clearly located at $f = 1\,\text{kHz}$, corresponding to the input frequency.

Additionally, other prominent harmonics can be observed at higher frequencies. These are related to the periodic structure of the waveform and, more specifically, to the frequency of the current pulses used to charge and discharge the output capacitors. Since the output voltage is reconstructed as a staircase approximation of the sinusoid, where each step results from a discrete charging or discharging event, the time interval between these steps introduces a secondary periodicity.

5.3.2 Bandwidth

Since the architecture is based on digital components, only transient simulations can be performed. Therefore to evaluate the frequency response of the circuit, the Bode diagram was obtained by performing multiple transient simulations. In each simulation, a sinusoidal input signal with fixed amplitude was applied, while the input frequency f_{in} was varied over the desired range.

For each frequency f_{in}, the Fast Fourier Transform (FFT) of input V_{in} and output V_{out} signals was computed, and the module of the Bode diagram was calculated as follows:

$$|H(f_{\text{in}})| = \frac{|V_{\text{out}}(f_{\text{in}})|}{|V_{\text{in}}(f_{\text{in}})|} \tag{5.2}$$

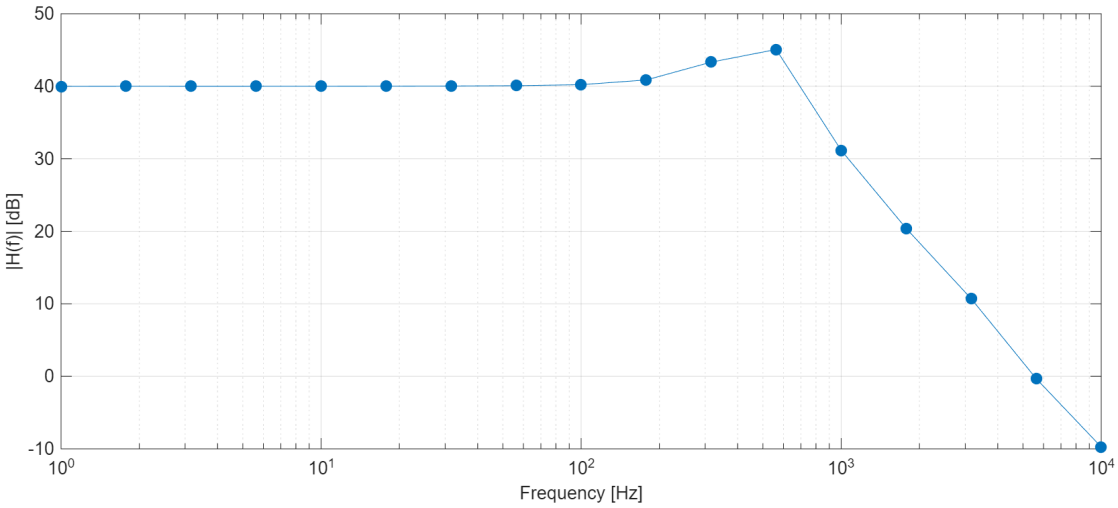


Figure 5.10: Magnitude of Bode Diagram

The resulting Bode diagram, shown in Figure 5.10, was obtained by applying input signals with constant amplitude of 100 µV, and sweeping the input frequency from 1 Hz to 10 kHz.
The plot shows a -3 dB bandwidth of approximately 700 Hz with a gain of about 39 dB. At 1 kHz sufficient gain (about 31 dB) is maintained, in line with the requirements of the target application.

5.3.3 Noise

Minimizing noise is essential in this architecture to enable the detection of neural signals with amplitudes on the order of tens of µV. For this reason, particular attention was given to the input stage of the circuit, because the noise introduced

at this stage is then amplified by the subsequent stages. According to the Friis formula for cascaded systems:

$$\mathrm{F_{tot}} = \mathrm{F_1} + \frac{\mathrm{F_2} - 1}{G_1} + \frac{\mathrm{F_3} - 1}{G_1 G_2} + \dots \tag{5.3}$$

where F_i and G_i are the noise factor and available power gain of the i-th stage, respectively, the first stage has the greatest impact on the overall noise performance.

To optimize noise, several simulations were carried out by varying the number of inverters used in each input branch and the strength of the logic gates in the input stages. The input-referred noise was computed using:

$$V_{ni,rms} = \sqrt{\int_{f_{\mathrm{initial}}}^{f_{\mathrm{final}}} \frac{|V_{out}(f)|^2}{G^2}\, df} \tag{5.4}$$

where G is the nominal gain, and f_{initial}, f_{final} define the bandwidth of interest.

The best trade-off between input-referred noise, power consumption, and area was obtained using four inverters in parallel per input branch. The results are summarized in Table 5.6.

Configuration	*Input-Referred Noise*	*Power Consumption*	*Area*
1 inverter	$19\,\mu\mathrm{V_{rms}}$	$590\,\mathrm{nW}$	$\approx 650\,\mu\mathrm{m}^2$
4 inverters	$12\,\mu\mathrm{V_{rms}}$	$1.11\,\mu\mathrm{W}$	$\approx 1{,}000\,\mu\mathrm{m}^2$
8 inverters	$17\,\mu\mathrm{V_{rms}}$	$1.8\,\mu\mathrm{W}$	$\approx 1{,}400\,\mu\mathrm{m}^2$

Table 5.6: Comparison for different numbers of input inverters per input branch.

The improved performance with four inverters can be explained by the thermal noise behavior of MOS devices, given by:

$$S_{VG} = \frac{4k_B T \Gamma}{g_m} \tag{5.5}$$

where k_B is the Boltzmann constant, T the absolute temperature, Γ the thermal noise factor, and g_m the transconductance [17]. Placing identical devices in parallel increases the total width W, and hence the total bias current and g_m, leading to lower thermal noise. Moreover, flicker noise, which is inversely proportional to the $W \cdot L$ product, is also reduced.

To further reduce noise and ensure proper signal transitions, both the input inverters and the output buffers were designed with high strength (i.e., larger transistors).
This also ensures well-defined rising and falling edges of the digital signals INV+ and INV-, which is essential for robust switching in the output logic gates. Indeed clean transitions help reduce ambiguity when the output is momentarily stable for short intervals (on the order of tens of nanoseconds), as in the case shown in Figure 5.7.

Despite optimization, it was not possible to push the input-referred noise below 10 µV. As a result, input signals of this magnitude remain difficult to distinguish from noise. However, for higher input amplitudes, the signal can be detected, as illustrated in Figure 5.11.

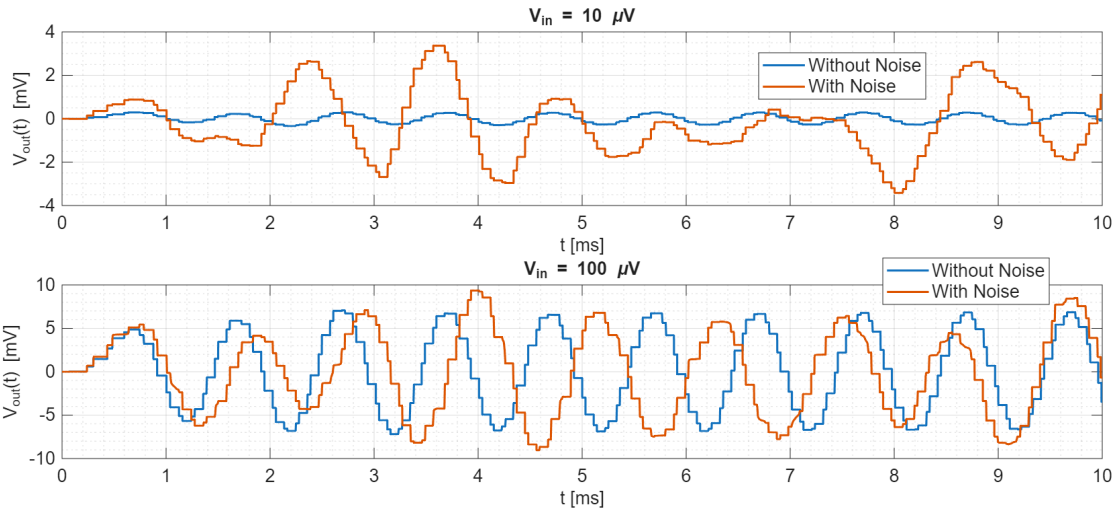


Figure 5.11: Comparison between differential output with and without noise for different input amplitudes.

5.4 Simplified Electrode-Based Configuration

After testing the DIGOTA in its conventional configuration, electrode models and a neuron model were added to the testbench, as shown in Figure 5.12.

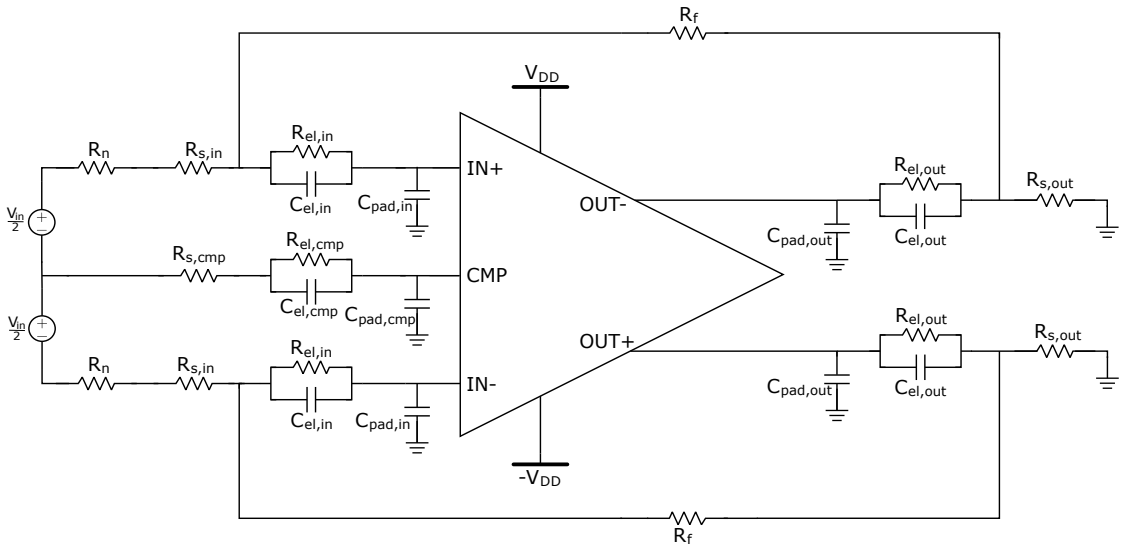


Figure 5.12: DIGOTA with electrode models configuration.

Modeling electrodes can be quite challenging because their electrical behavior depends on many factors, such as their type, geometry, material, and the solution they are immersed in.

As a starting point, we used the equivalent circuit described in the study mentioned in Section 2.1, which analyzes how the resistance and capacitance of an electrode change over time when placed in artificial cerebrospinal fluid. For times shorter than 48 hours, the electrode can be modeled as a resistance R_{el} in parallel with a capacitance C_{el}, in series with the solution resistance R_s.

To define the values of R_{el} and C_{el}, we assumed a dependence on electrode area:

- C_{el} scales linearly with the electrode area;
- R_{el} is inversely proportional to the electrode area.

The output and compensation electrodes were considered equal to $10\,\mu m \times 10\,\mu m$, while the input electrodes were larger, $20\,\mu m \times 20\,\mu m$, to ensure better coupling with the neuron.

Estimating the solution resistance R_s was more difficult due to the lack of direct experimental data. To address this, the circuit was tested across a wide range of R_s values, from $10\,k\Omega$ to $10\,M\Omega$.

Additionally, a parasitic capacitance C_{pad} was included to model the pads.

The feedback resistors R_f represent the coupling between electrodes and define the feedback configuration of the amplifier, aiming to reproduce the behavior of the previously analyzed topology.

The neuron was modeled as a voltage source in series with two resistances R_n.

Based on these assumptions, the chosen component values are reported in Table 5.7.

Parameters	Value
R_n	$25\,\mathrm{k\Omega}$
$R_{s,in}$	$25\,\mathrm{k\Omega}$
$R_{el,in}$	$300\,\mathrm{M\Omega}$
$C_{el,in}$	$1.2\,\mathrm{nF}$
$C_{pad,in}$	$120\,\mathrm{fF}$
$R_{s,out} = R_{s,cmp}$	$100\,\mathrm{k\Omega}$
$R_{el,out} = R_{el,cmp}$	$1.2\,\mathrm{G\Omega}$
$C_{el,out} = C_{el,cmp}$	$300\,\mathrm{pF}$
$C_{pad,out} = C_{pad,cmp}$	$30\,\mathrm{fF}$
R_f	$20\,\mathrm{G\Omega}$

Table 5.7: Component values of the circuit configuration considering simple electrode model.

Output behaviour

Due to the presence of additional resistors connected to the output nodes - elements that are not present in the conventional differential configuration, which typically includes only a capacitor at the output -the output voltages no longer exhibit a staircase waveform, resulting from the charging and discharging of output capacitors. Instead, in this configuration, the outputs consist of narrow voltage pulses, whose amplitudes are modulated by the input signal.
As a result, the envelope of these pulses closely follows the amplified input waveform, allowing effective amplitude modulation, as shown in Figure 5.13.

This behavior can be understood by analyzing the transfer function at the output node, which acts as a high-pass filter. In particular, if we consider the circuit shown in Figure 5.14, the transfer function can be expressed as:

$$H(s) = \frac{V_{\mathrm{out}}(s)}{V_{\mathrm{pad}}(s)} = \frac{R_s}{\left(\frac{1}{\frac{1}{R_{\mathrm{el}}}+sC_{\mathrm{el}}}\right) + R_s} = \frac{sR_{el}C_{el} + R_s}{sR_sR_{el}C_{el} + R_s + R_{el}} \tag{5.6}$$

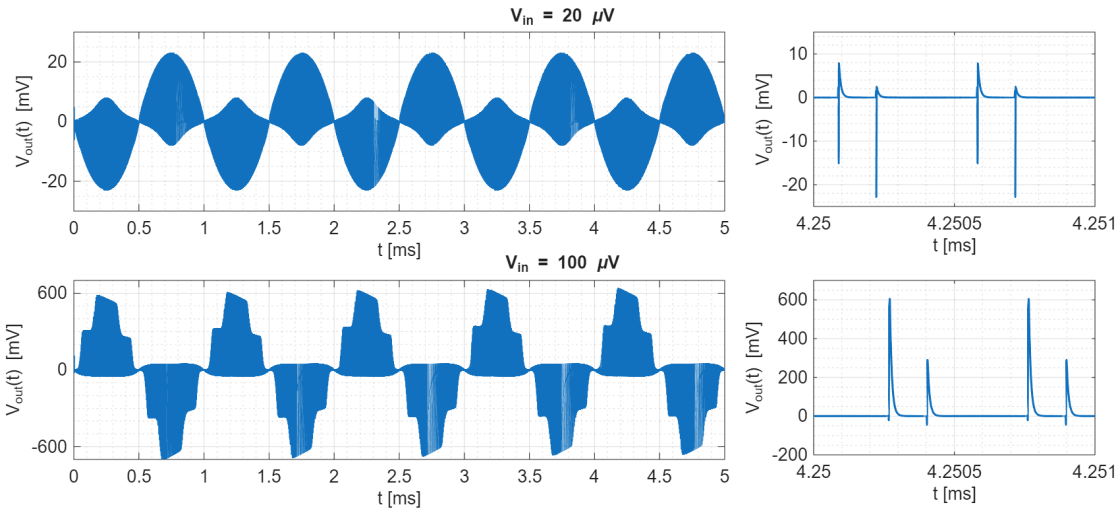


Figure 5.13: Differential output V_{out} and its zoom view for different input amplitudes.

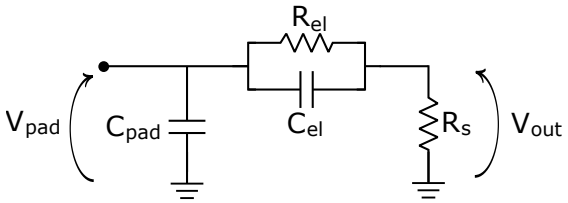


Figure 5.14: Equivalent electrical model of an output electrode.

By plotting the output response of this transfer function to a step input, we obtain the waveform shown in Figure 5.15, which confirms the high-pass behavior and closely resembles the one obtained from the Cadence simulations as shown in Figure 5.16.

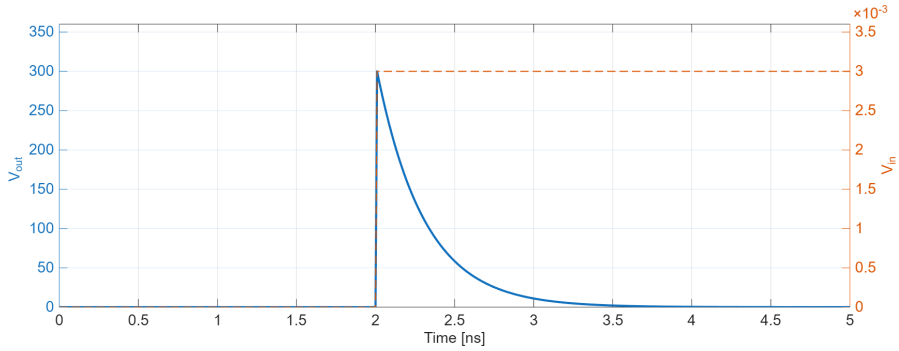


Figure 5.15: Step response of the output electrode's transfer function.

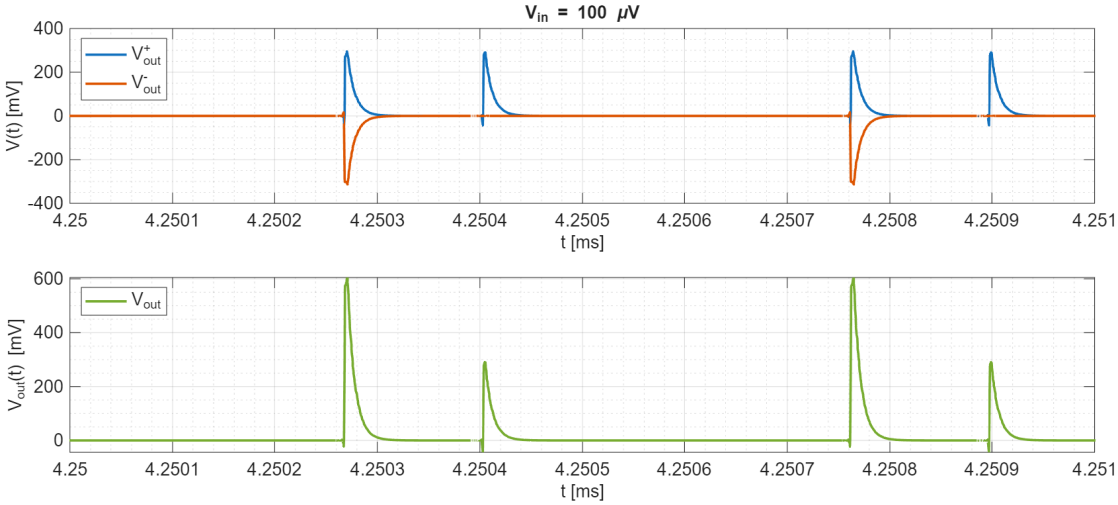


Figure 5.16: Zoom of V_{out}^{+}, V_{out}^{-} and V_{out}.

By analyzing the Discrete Fourier Transform (DFT) of the output signal, as shown in Figure 5.17, two main components can be observed: one at the input frequency $f = 1\,\text{kHz}$ and a second peak at a higher frequency, corresponding to the repetition rate of the output pulses. This confirms that the useful information is encoded not only in the low-frequency envelope, but also in the high-frequency content of the signal, which can be exploited during signal reconstruction.

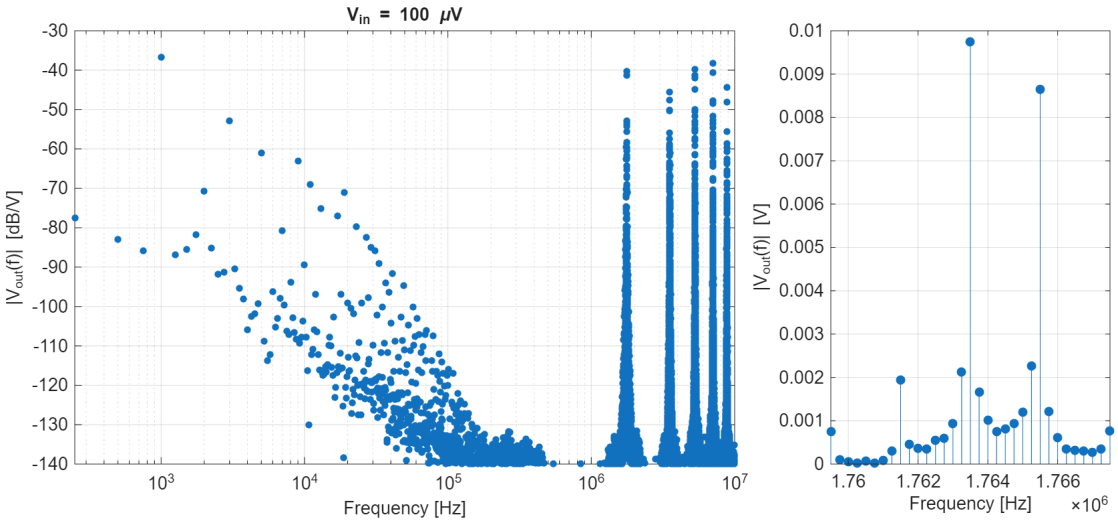


Figure 5.17: DFT magnitude of V_{out} and zoomed view around the spike repetition frequency.

This behavior is particularly advantageous for our application. In fact, thanks to this modulation mechanism, there is no longer a need for a VCO to encode the

signal onto a varying frequency for external transmission. The DIGOTA alone is sufficient to generate a signal suitable for transmission, which results in a significant saving in both chip area and power consumption.

For this reason, it is essential to ensure that the frequency of the output pulses is not too high respect the transmitter operational frequency. To achieve this, a MIM (Metal-Insulator-Metal) capacitor was added at the output of the compensation stage, in order to reduce the pulse period rate. This approach also contributes to lowering the overall power consumption of the circuit. The schematic of the DIGOTA with the added capacitor is shown in Figure 5.18.

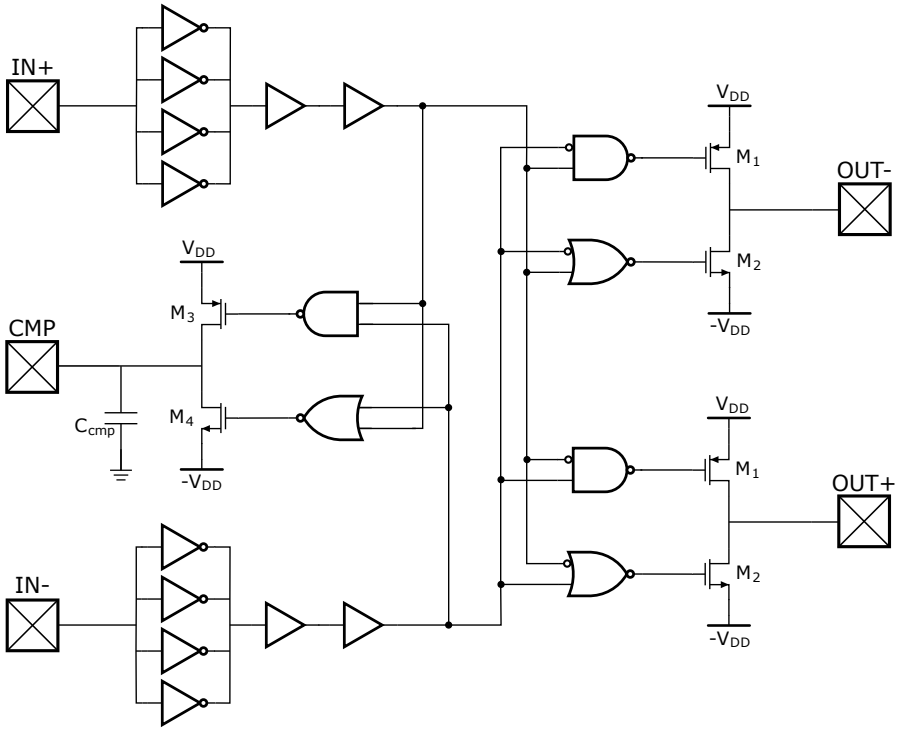


Figure 5.18: DIGOTA schematic with the compensation capacitor.

Transistor Design

In order to investigate the behavior and optimize the performance of the output and compensation blocks by varying the transistor dimensions, different simulations were carried out using a sinusoidal input signal.

In the first set of simulations, the focus was on the output stage. The minimum available channel length was selected, while the transistor width W was swept. To improve current symmetry, the width of the pMOS transistors was chosen to be twice that of the nMOS transistors. During this phase, the dimensions of the

compensation stage transitors were kept constant. The simulation parameters are summarized in Table 5.8.

Parameter	Value
L_{out}	180 nm
$W_{out,n}$	1-20 µm
$W_{out,p}$	2-40 µm
L_{cmp}	1 µm
$W_{cmp,n}$	220 nm
$W_{cmp,p}$	440 nm

Table 5.8: Transistor dimensions used in simulations for the output stage analysis.

As shown in Figure 5.19, the output gain increases with the transistor width and reaches its maximum when $W_{out,n} = 10\,\mu m$ and $W_{out,p} = 20\,\mu m$.

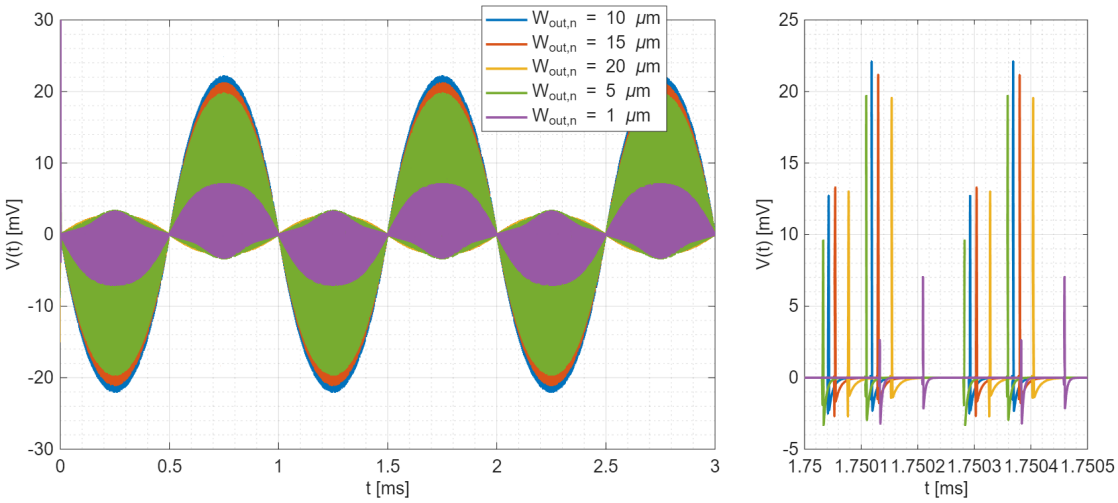


Figure 5.19: Comparison of V_{out} for different W_{out} values

Subsequently, the impact of the aspect ratio (W/L) of the transistors in the compensation stage was studied using the same approach. In this case, the output stage dimensions and the widths of the compensation transistors were kept fixed, while the length L_{cmp} was swept. Table 5.9 reports the parameter values adopted during this analysis.

As shown in Figures 5.20 and 5.21, increasing L_{cmp} results in a higher output gain, until a saturation region is reached. To ensure optimal performance,

Parameter	Value
L_{out}	180 nm
$W_{out,n}$	10 µm
$W_{out,p}$	20 µm
L_{cmp}	0.18-10 µm
$W_{cmp,n}$	220 nm
$W_{cmp,p}$	440 nm

Table 5.9: Transistor dimensions used in simulations for the compensations stage analysis.

$L_{cmp} = 5\,\mu m$ was selected, corresponding to the smallest length at which the output begins to saturate when the input signal is at its maximum working amplitude. This guarantees that the circuit provides the highest possible gain within the desired input range.

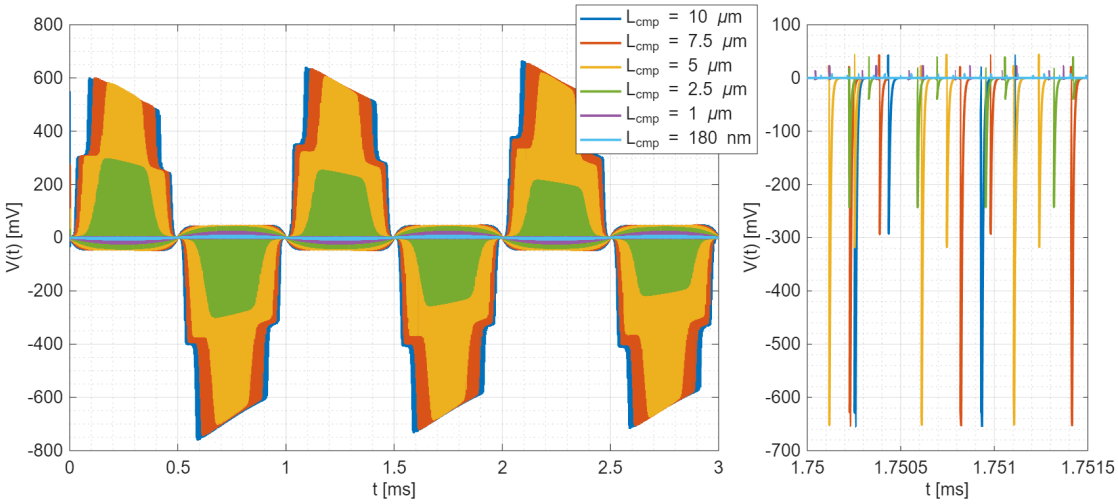


Figure 5.20: Comparison of V_{out} for different L_{cmp} values

In conclusion, the final transistor dimensions used for the output and compensation stages are reported din Table 5.10.

Varying Solution Resistance

Since the value of R_s could be critical for the correct operation of the circuit and is not precisely known, different simulations were performed by varying its order of

Parameter	Selected Value
L_{out}	180 nm
$W_{out,n}$	10 µm
$W_{out,p}$	20 µm
L_{cmp}	5 µm
$W_{cmp,n}$	220 nm
$W_{cmp,p}$	440 nm

Table 5.10: Selected transistor dimensions for output and compensation stages.

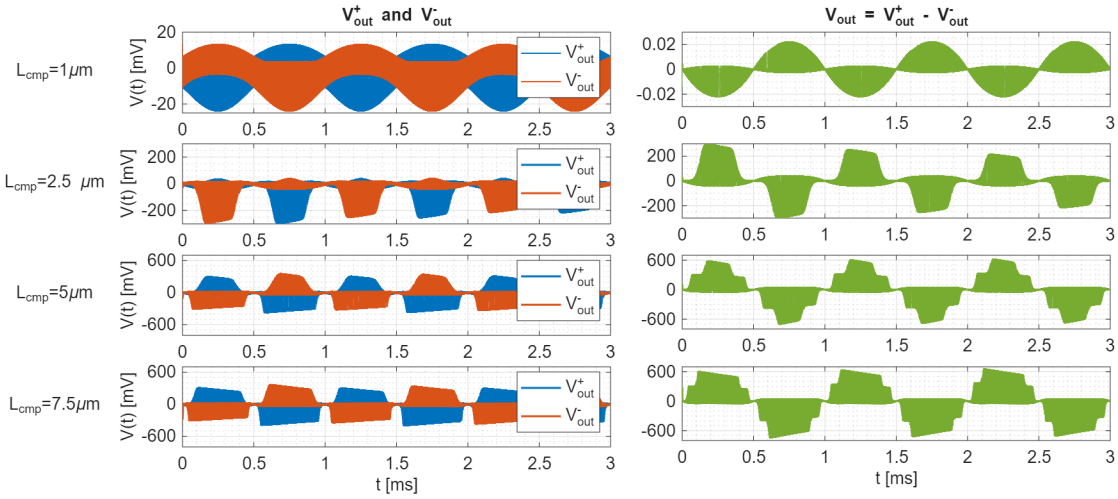


Figure 5.21: Plot of V_{out}^{+}, V_{out}^{-} and V_{out} for different L_{cmp} values

magnitude, from 10 kΩ to 10 MΩ.

Figure 5.22 shows the results obtained by sweeping $R_{s,out}$, while assuming $R_{s,in} = \frac{R_{s,out}}{4}$, since the input electrodes have four times the area of the output ones, and we consider the resistance to scale linearly with area, neglecting other effects.

As shown in the figure, the circuit continues to operate correctly in most cases. However, for $R_{s,out} = 10\,\text{MΩ}$, the output waveform behaves differently. In this case, the capacitor discharges very slowly due to the high resistance, and the typical sharp output spikes are no longer observed. When the input amplitude is higher, the capacitor does not have enough time to fully discharge to 0 V before the next charging cycle begins.

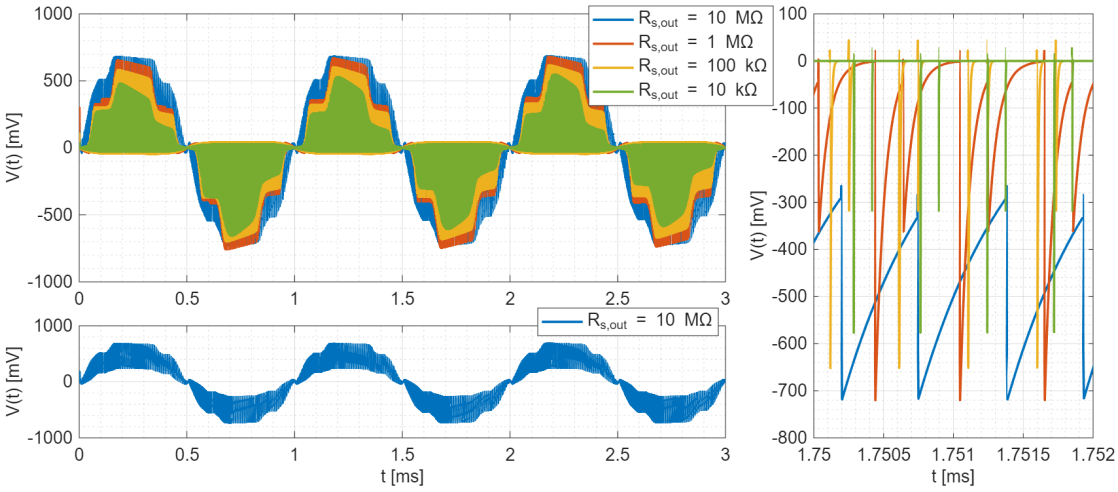


Figure 5.22: Comparison of V_{out} for different R_s values

5.4.1 Circuit behavior

The internal signals of the circuit were analyzed and compared with those obtained from the conventional differential configuration, which does not include the electrode model. In this analysis sinusoidal input signals with a frequency of 1 kHz and amplitudes of 20 µV and 100 µV were used.

The most noticeable difference is that the output signals are composed of spikes. This effect is caused by the presence of the series resistance R_s on the output electrodes, which periodically discharges the output capacitors. This behavior can be observed in Figures 5.13, and has already been described earlier in the text.

Another key difference is that each output spike is immediately preceded by a short spike of opposite polarity. This phenomenon is more evident when the input signal has a lower amplitude. For example, with an input of 20 µV, the distortion appears more pronounced, even though the spike amplitude is similar to the case with higher input amplitude, as presented in Figures 5.24 and 5.23.

At lower input amplitudes, the outputs appear as two sinusoidal signals with different gains: one non-inverting and the other inverting. This makes the distortion more visible in the single-ended outputs, while it is reduced in the differential one, where this effect is partially compensated, especially when the signal should be close to zero, as illustrated in Figure 5.25.

Another important difference, visible when analyzing the internal signals, concerns the behavior of V_{gP} and V_{gN}, which are the gate control voltages for the

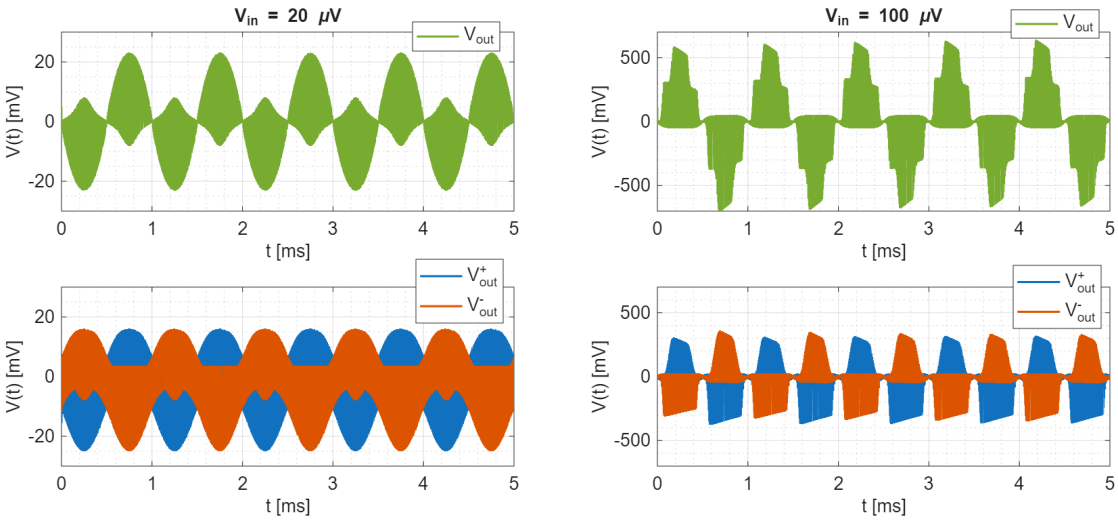


Figure 5.23: Differential output V_{out} and single-ended output V_{out}^{+} and V_{out}^{-} for different input amplitudes.

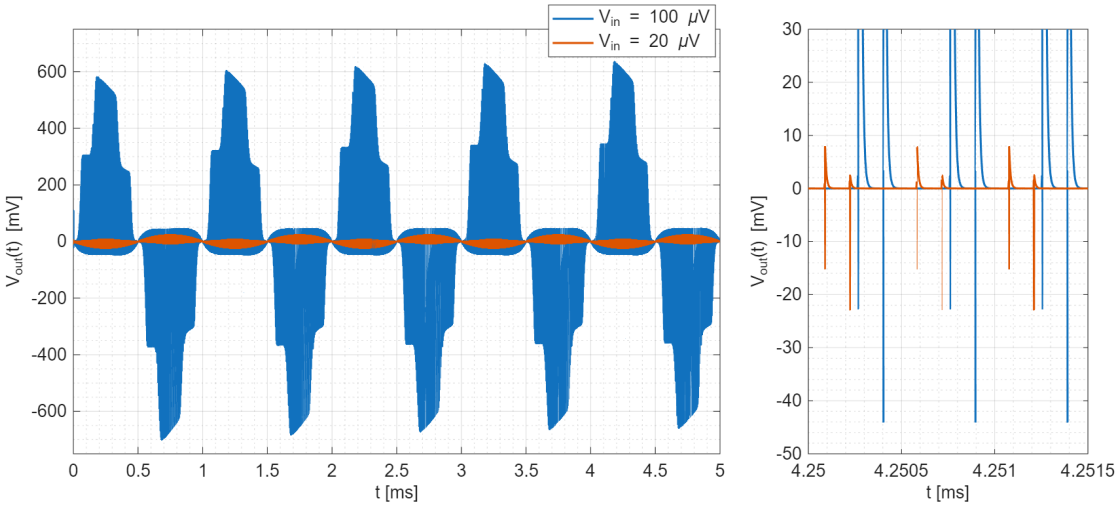


Figure 5.24: Comparison between differential output V_{out} for different input amplitudes and zoom on thier undesired spikes.

nMOS and pMOS transistors in the output stages. These signals correspond to the outputs of the NAND and NOR gates and directly control the switching of the transistors. They are illustrated in Figure 5.26, where it possible to observe the difference between their behavior in case of different input amplitudes.

When the input signal has a small amplitude, the delay between INV+ and INV– is often very short, frequently less than 1 ns, as shown in the zoomed-in view in Figure 5.27. Because of this, the logic states (0,1) or (1,0), which are responsible

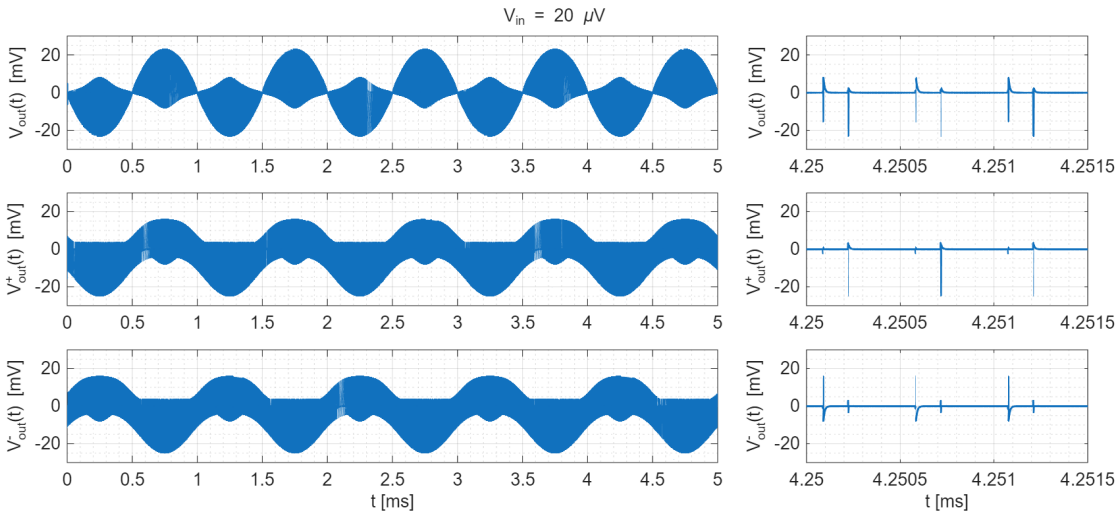


Figure 5.25: Differential output V_{out} and single-ended output V_{out}^{+} and V_{out}^{-} for $V_{in} = 20\,\mu V$.

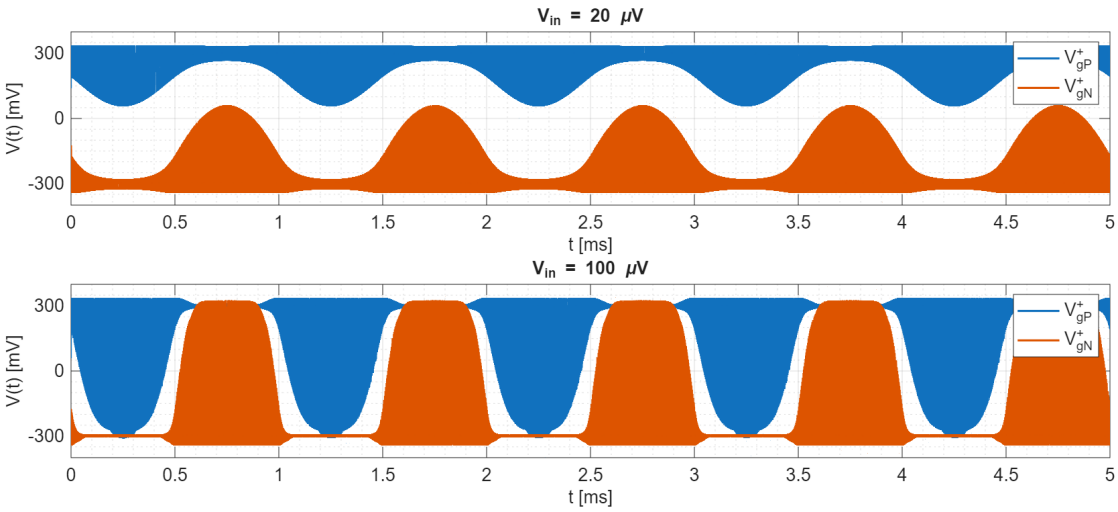


Figure 5.26: Gate control signals V_{gP}^{+} and V_{gN}^{+} (outputs of the NAND and NOR gates, respectively) for different input amplitudes.

for triggering the NAND and NOR gates, are not held long enough for the gates to properly detect the transition and update their output.

This issue is not evident when the input signal has a higher amplitude. In that case, the delay between INV+ and INV– is longer, i.e. greater than 1 ns, allowing the logic gates enough time to register the change correctly, as shown in Figure 5.28.

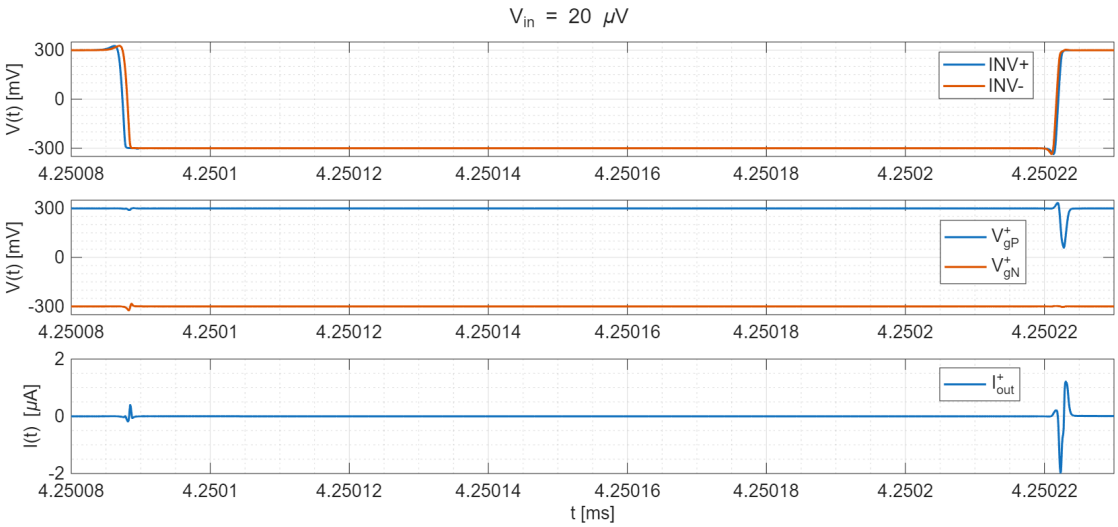


Figure 5.27: Zoom of INV+, INV-, V_{gP}^{+}, V_{gN}^{+} and I_{out}^{+} signals for $V_{in} = 20\,\mu\text{V}$.

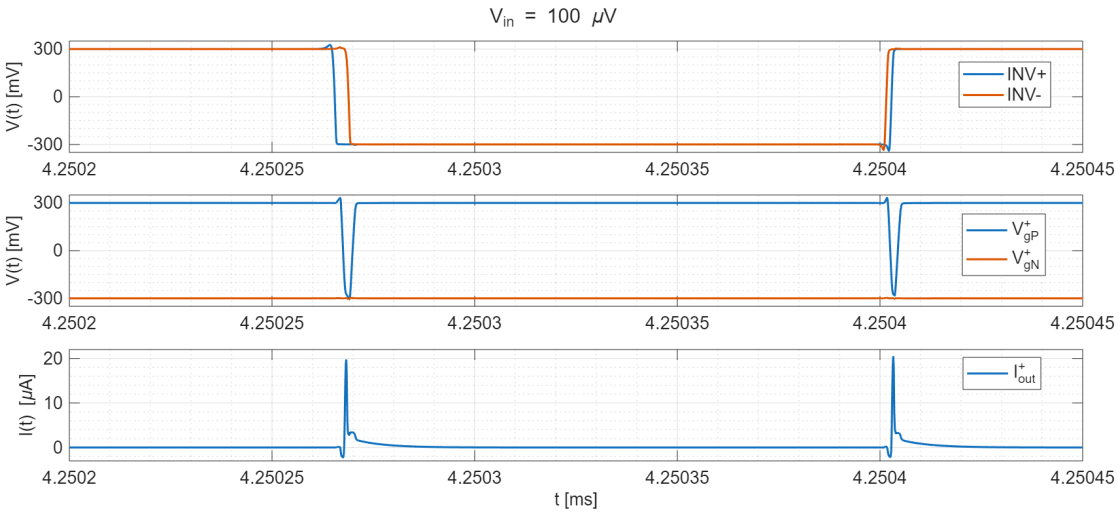


Figure 5.28: Zoom of INV+, INV–, V_{gP}^{+}, V_{gN}^{+}, and I_{out}^{+} signals for $V_{in} = 100\,\mu\text{V}$.

5.5 Enhanced Electrode-Based Configuration

After verifying the correct operation of the circuit and optimizing its performance using a simplified equivalent model for the electrodes, a more accurate model for electrodes is introduced. In particular the electrical equivalent model described in Section 2.2 and shown in Figure 5.29 is adopted.

Unlike the basic model, which consisted of a single RC branch, the enhanced version includes six parallel RC branches, to better approximate the CPE behavior

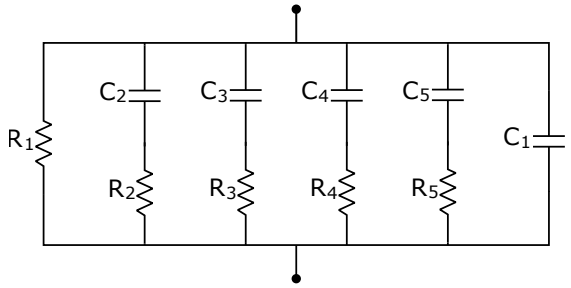


Figure 5.29: Enhanced electrode model

and capture frequency-dependent effects of real electrodes, such as capacitive saturation.

The component values, originally derived from the study in [3], were scaled and adapted to our case by assuming a linear dependence on both the previous model parameters and the electrode area. These values are reported in Table 5.11.

Parameter	Value
$R_{1,\text{out}} = R_{1,\text{cmp}}$	1.3 GΩ
$R_{2,\text{out}} = R_{2,\text{cmp}}$	44 MΩ
$R_{3,\text{out}} = R_{3,\text{cmp}}$	1.7 MΩ
$R_{4,\text{out}} = R_{4,\text{cmp}}$	507 GΩ
$R_{5,\text{out}} = R_{5,\text{cmp}}$	229 MΩ
$R_{1,\text{in}}$	325 MΩ
$R_{2,\text{in}}$	11 MΩ
$R_{3,\text{in}}$	425 kΩ
$R_{4,\text{in}}$	126.75 GΩ
$R_{5,\text{in}}$	57.25 MΩ

Parameter	Value
$C_{1,\text{out}} = C_{1,\text{cmp}}$	52 pF
$C_{2,\text{out}} = C_{2,\text{cmp}}$	222 pF
$C_{3,\text{out}} = C_{3,\text{cmp}}$	72 pF
$C_{4,\text{out}} = C_{4,\text{cmp}}$	400 pF
$C_{5,\text{out}} = C_{5,\text{cmp}}$	9 pF
$C_{1,\text{in}}$	208 pF
$C_{2,\text{in}}$	888 pF
$C_{3,\text{in}}$	288 pF
$C_{4,\text{in}}$	1,600 pF
$C_{5,\text{in}}$	36 pF

Table 5.11: Component values of the enhanced circuit configuration.

With the improved testbench configuration, illustrated in Figure 5.30, a new set of simulations was carried out. These were compared to the results obtained using the previous, simpler electrode model, in order to assess the impact of electrode non-idealities on the overall circuit behavior.

Since the exact model of the electrodes that will be used in practice is not yet available, testing the circuit with different electrode representations also helps verify its robustness. This strategy allows us to ensure reliable performance under a wider range of conditions and strengthens the design against modeling uncertainties.

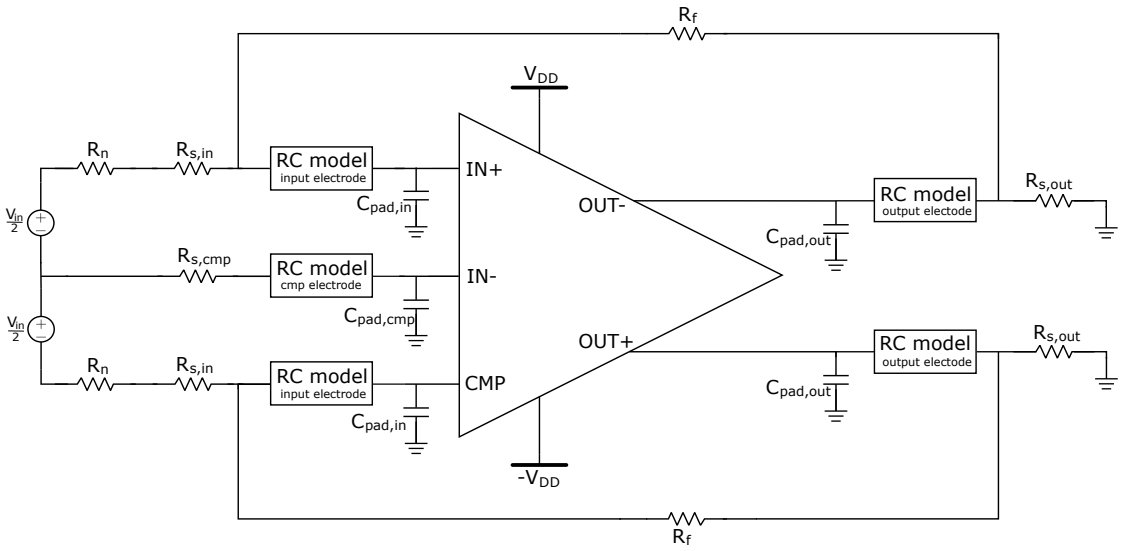


Figure 5.30: DIGOTA schematic including the enhanced electrode model

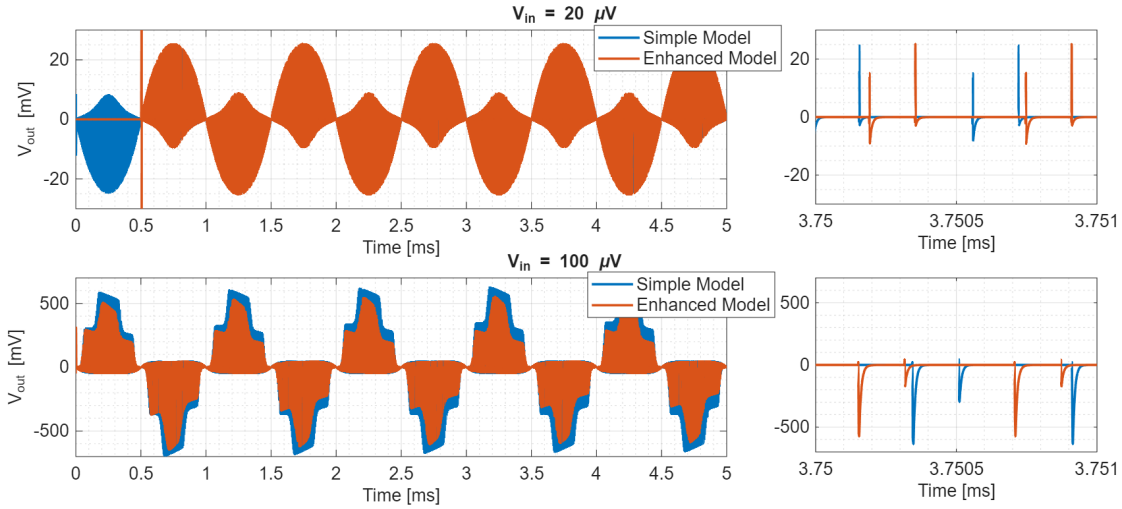


Figure 5.31: Comparison of V_{out} for different models.

Figures 5.31 and 5.32 show the output signals obtained for different input sine wave amplitudes and their corresponding frequency spectra. As can be observed, both configurations exhibit similar overall behavior. However, small differences occur in the transient response, output gain, and spike frequency. A noticeable variation is in the harmonic content around the pulse frequency: while the simpler model produces a few high-amplitude harmonics close to the higher one, the enhanced model presents a wider frequency range of lower-amplitude harmonics.

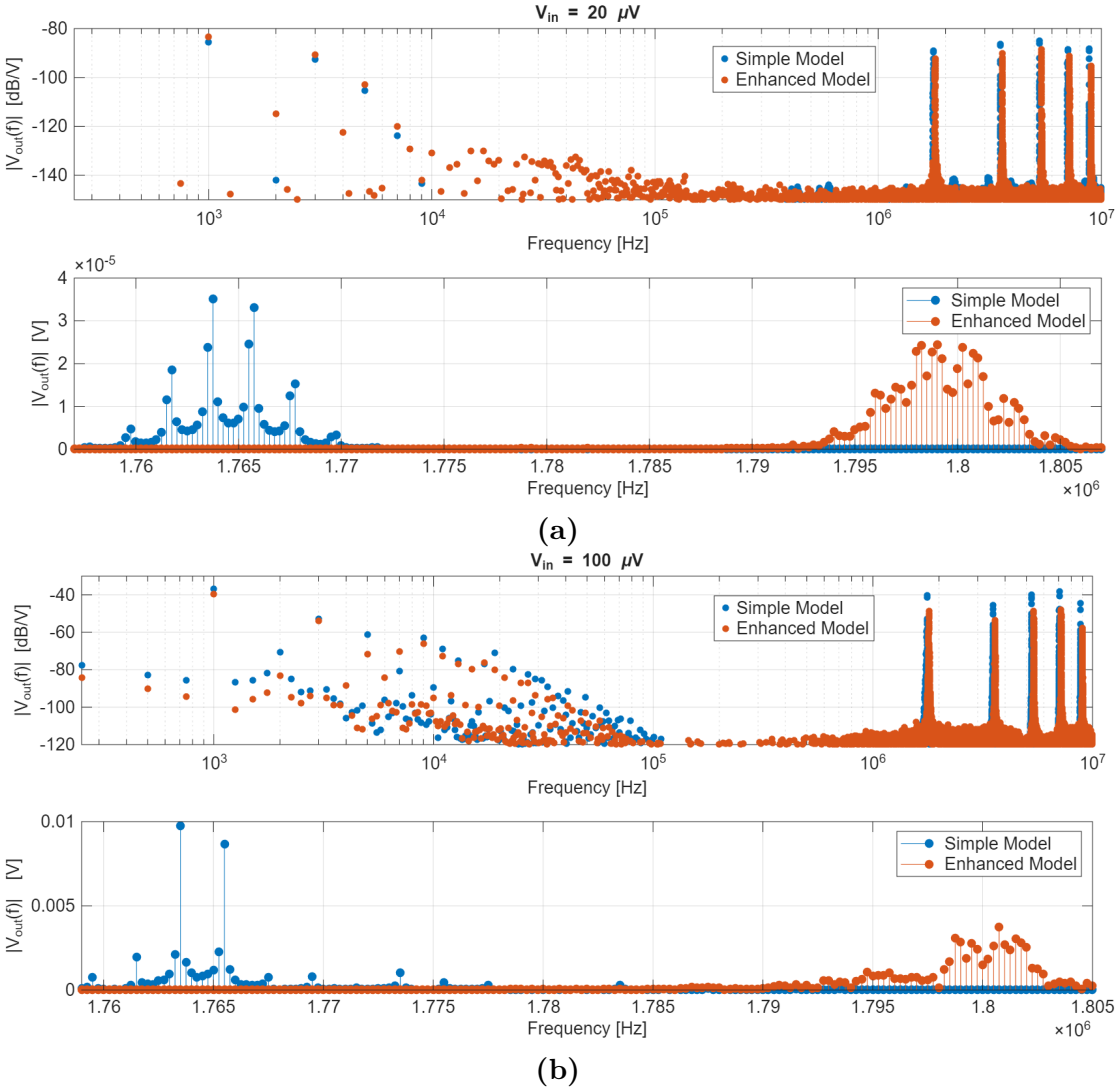


Figure 5.32: DFT magnitude of V_{out} and zoomed view around pulse frequency

5.6 Layout

Once the schematic simulation results are acceptable with respect the requirements, the layout design of the schematic can be done.

To realize the layout, standard cells and devices available in the TSMC 180nm technology library were used, including logic gates, transistors, and MIM capacitors.

The final layout is shown in Figure 5.33 and occupies an area of:

$$A = 10.86\,\mu\text{m} \cdot 91.95\,\mu\text{m} = 998.56\,\mu\text{m}^2$$

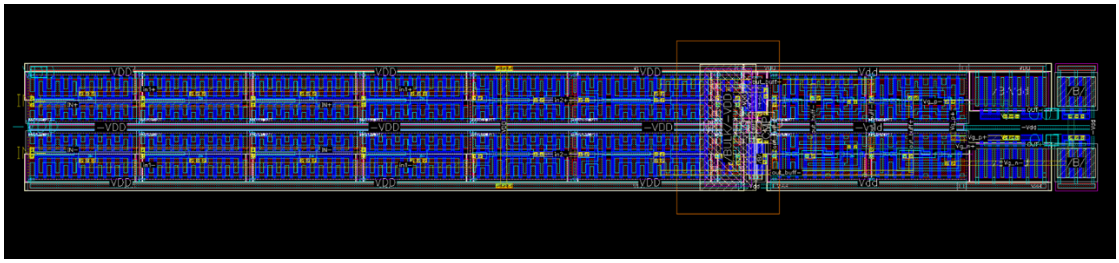


Figure 5.33: DIGOTA layout

The logic gates were placed in alignment to share power supply rails efficiently. The transistors were distributed alongside the logic block, with careful sizing to optimize the available space. In particular, the output stage transistors, characterized by large widths,were implemented using multi-finger MOS devices. While the transistors in the compensation stage, which have long channel lengths, were modeled as series connections of 2 pMOS and 2 nMOS devices, each with half channel lengths.

The input stage is the most area-consuming block due to the use of several high-drive-strength logic gates, which consequently have a larger footprint. In contrast, the compensation stage is the most compact, due to the presence of low-strength logic gates and small W/L ratio transistors.

Interconnections were routed from metal layer M1 up to M4, while the MIM capacitor was placed above the compensation stage, using M5 and M6. Additionally, a grounded M5 layer was extended across the layout to provide shielding.

After completing the layout of the circuit, a Design Rule Check (DRC) was run to make sure that no design rules were violated. Then, a Layout Versus Schematic (LVS) check was done to confirm that the layout matched the original schematic. Once the LVS was successful, the layout was extracted.

5.7 Post-Layout Simulations

The extracted view includes parasitic capacitances and resistances introduced by the interconnects and device geometries and so it provides a more realistic representation of the circuit behavior. This version was then used for new simulations in both testbenches and the resulting performance was then compared to that obtained from the schematic-level simulations.

5.7.1 Output simulations

Figures 5.34 and 5.35 show a comparison between the simulation results obtained from the schematic and extracted views of the circuit, using both electrode models, when the amplitude input sinusoidal signal is 20 µV and 100 µV respectively.

Figure 5.36 presents the frequency-domain comparison for the same 100 µV input.

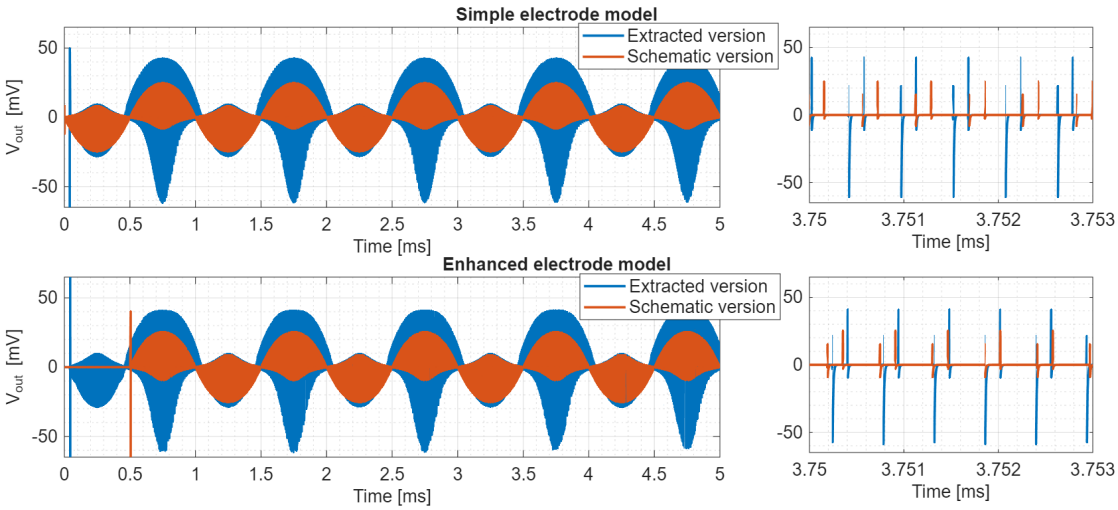


Figure 5.34: $V_{out}(t)$ comparison between schematic and extracted simulations using both electrode models, with $V_{in} = 20\,\mu V$.

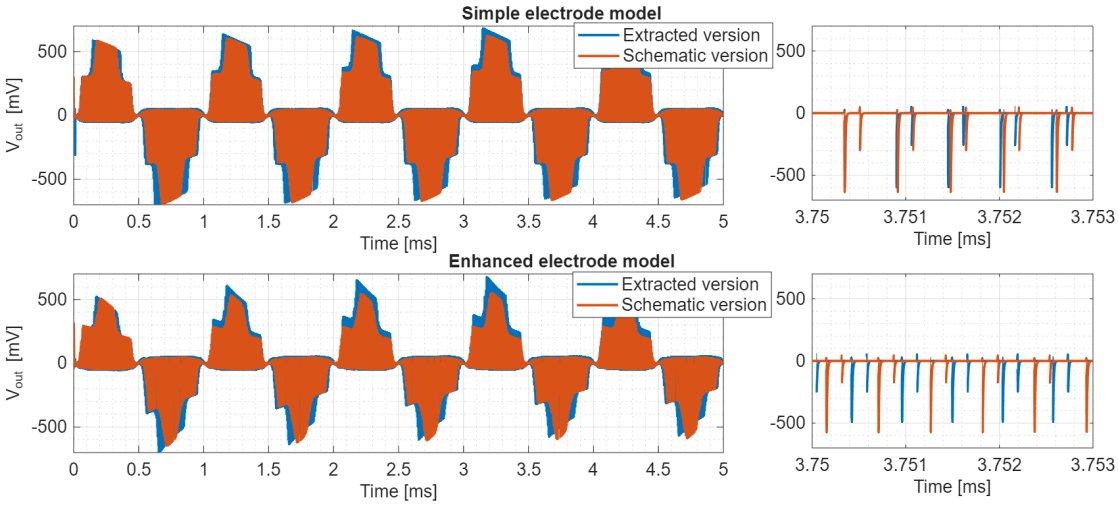


Figure 5.35: $V_{out}(t)$ comparison between schematic and extracted simulations using both electrode models, with $V_{in} = 100\,\mu V$.

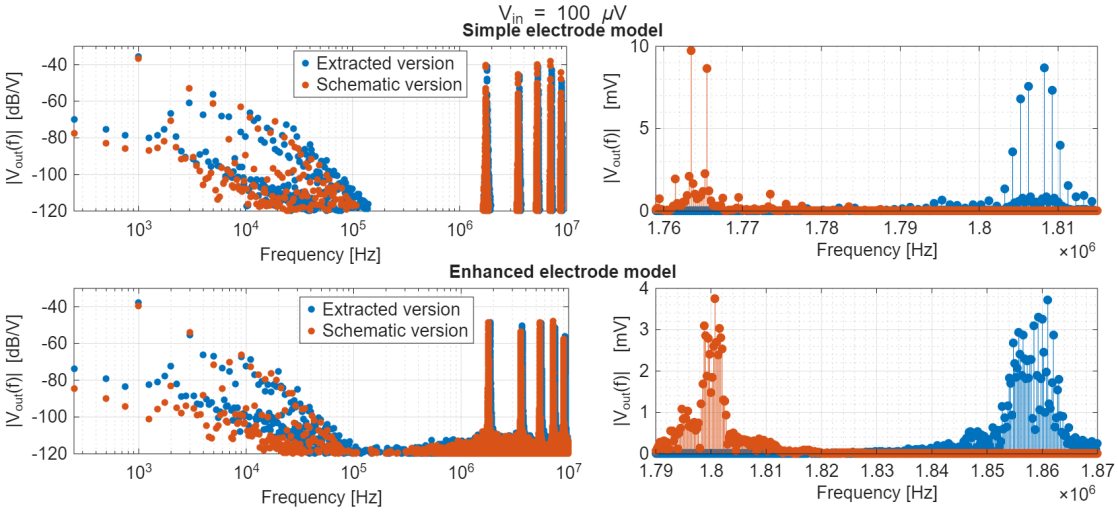


Figure 5.36: FFT magnitude $|V_{out}(f)|$ comparison between schematic and extracted simulations for both electrode models, with $V_{in} = 100\,\mu V$.

In all cases, the extracted layout version shows a behavior very similar to the corresponding schematic version and a slightly higher gain is observed in the extracted simulations. This confirms that the circuit performance is not significantly affected by layout parasitics and that the design remains robust after layout extraction.

5.7.2 Noise simulations

Transient noise was also included in the analysis, in particular simulations of the output signal were carried out using the advanced electrode model, considering the extracted layout version. Transient noise was also included in the analysis. The results are shown in Figure 5.37.

As shown in the figure, the impact of noise is much more noticeable when the input amplitude is lower. According to previous calculations, the noise level is expected to be around $12\,\mu V_{rms}$, which is quite significant compared to the signal amplitude of $20\,\mu V$. In contrast, when the input is $100\,\mu V$, the effect of noise is much less evident.

5.7.3 Corner Analysis

To evaluate the robustness of the circuit to process variations, a corner analysis was performed using the testbench with the enhanced electrode model, applied to both the schematic and extracted layout versions of the circuit. This type of analysis simulates circuit behavior under different manufacturing conditions, called

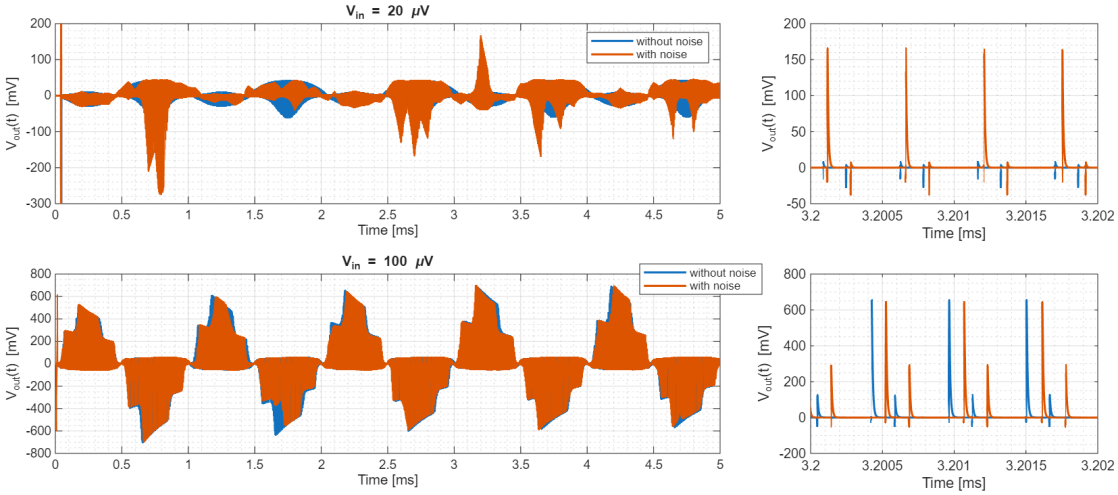


Figure 5.37: Comparison between $V_{out}(t)$ with and without noise, considering extracted layout circuit and with different input amplitudes.

process corners. In particular, the following corners were considered: Nominal (TT), Fast-Fast (FF), Slow-Slow (SS), Fast-Slow (FS), and Slow-Fast (SF).

The results are shown in Figures 5.38, 5.39, and 5.40, corresponding to input amplitudes of 20 µV and 100 µV.

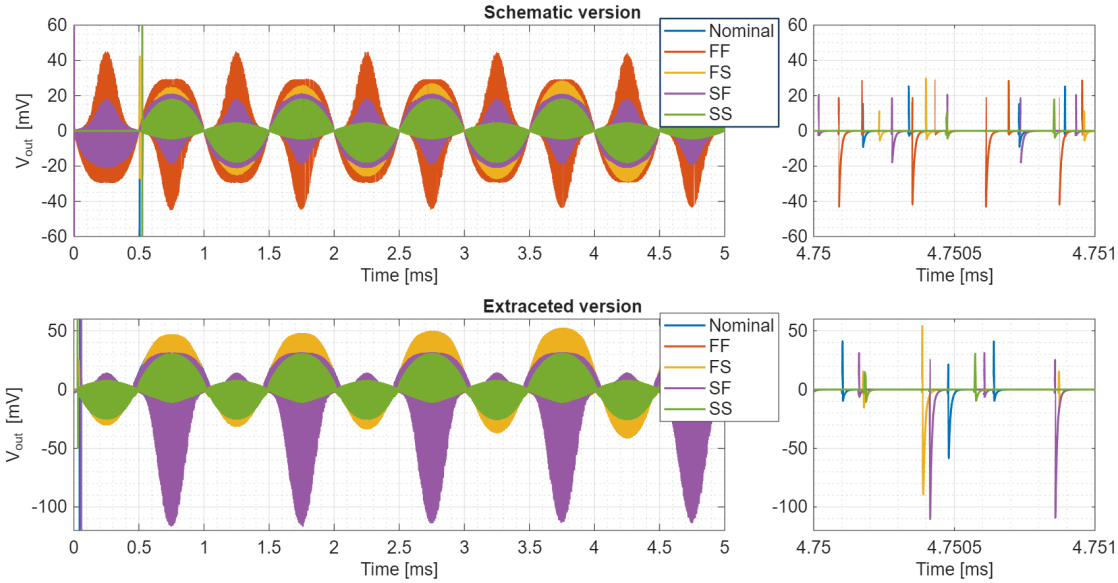


Figure 5.38: Corner analysis of V_{out}, schematic and extracted layout version, with $V_{in} = 20\,\mu V$.

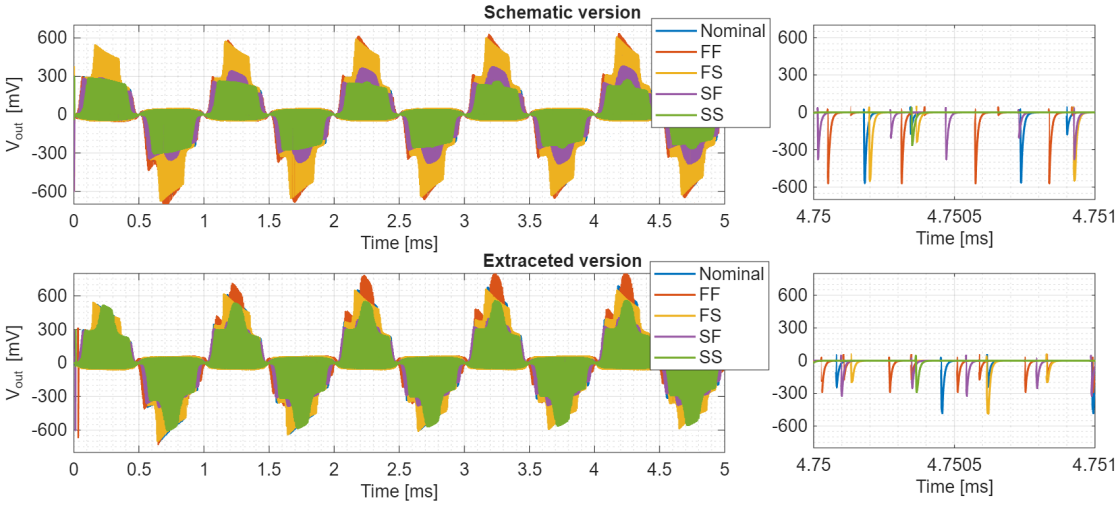


Figure 5.39: Corner analysis of V_{out}, schematic and extracted layout version, with $V_{in} = 100\,\mu V$.

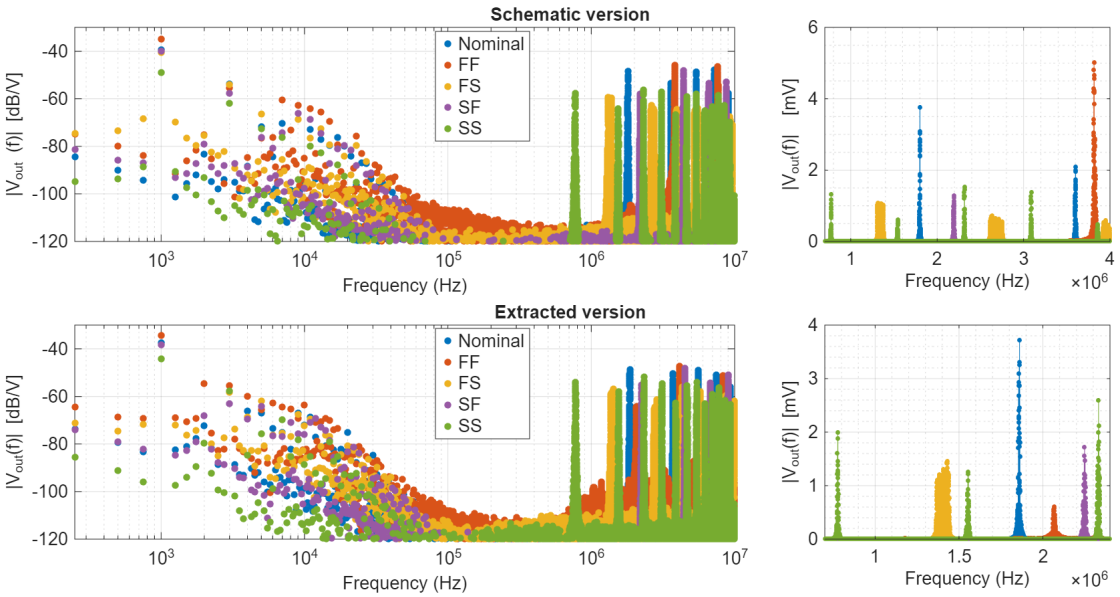


Figure 5.40: Corner analysis of V_{out} FFT, schematic and extracted layout version, with $V_{in} = 100\,\mu V$.

As observed:

- In the FF case, the output signal shows a slightly higher gain and d the spike frequency increases. As a result, the high frequency peaks in the FFT shifts toward higher frequencies.

- In the SS case, the gain is slightly reduced, and the FFT reveals more components in the higher-frequency range (approximately 1 MHz to 5 MHz).
- In the FS case, the spectrum shows a broader distribution of higher-frequency components.

These results confirm that the circuit maintains consistent performance across different process conditions.

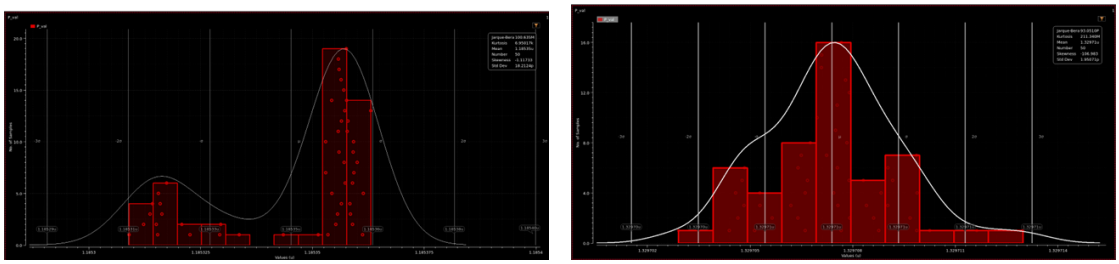
5.7.4 Monte Carlo Simulation

In order to check the statistical robustness of the design, Monte Carlo simulations were performed with 50 samples. Monte Carlo analysis is used to evaluate how random variations in device parameters (such as threshold voltage, mobility, and resistor values) affect the circuit's performance.

The simulations were carried out using the enhanced electrode model, for both the schematic and extracted layout versions of the circuit and using as input signal a sinusoid with an amplitude of 100 µV.

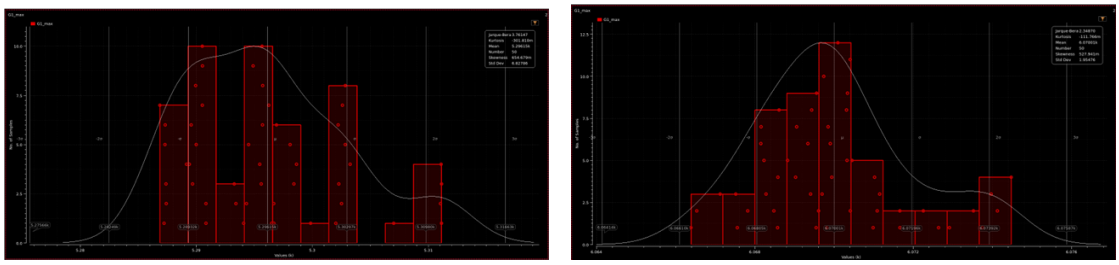
Figures 5.41 and 5.42 show the results of the Monte Carlo analysis for power consumption and gain, respectively.

As observed that parameters have a low very variability across samples in both versions, showing that the design is stable even under random parameter variations.



(a) Schematic circuit version **(b)** Extracted circuit version

Figure 5.41: Monte Carlo simulation results of power consumption.



(a) Schematic circuit version **(b)** Extracted circuit version

Figure 5.42: Monte Carlo simulation results of the gain.

5.8 Electrode Layout

Once the circuit was designed and tested, the electrodes had to be integrated into the layout.
Specifically, three electrodes were used for the outputs and the common-mode terminal, while two larger electrodes were used for the inputs.

To implement the feedback resistors R_f, we aimed to create electrical coupling between IN+ and OUT- and between IN- and OUT+, and. at the same time, it was important to avoid coupling between IN+ and OUT+ and between IN- and OUT-.

To achieve this, we carefully studied the spatial arrangement of the five main electrodes and introduced additional structures called dummy electrodes. These were used to increase or reduce the coupling as needed, depending on their position and size. Their presence was crucial to model the overall coupling behavior of the system to match the testbench model as closely as possible.

To analyze the electrical coupling between electrodes, a MATLAB code was used. This code discretizes each electrode into a grid of $1\,\mu m \times 1\,\mu m$ elements. Each element (or pixel) is considered as a point charge, and the code calculates the electrostatic potential it produces on all the others.

Based on these mutual interactions, the algorithm computes the conductance matrix G, where each element g_{ij} represents the mutual conductance between electrode i and electrode j.

By analyzing the matrix G, it was possible to guide the design of electrode structures toward controlled coupling: either by minimizing unwanted interactions or enabling coupling where needed, i.e. between IN+ and OUT-, and between IN- and OUT+. Several configurations were tested, adjusting the position and geometry of electrodes, in order to find a solution that best approximated the desired coupling behavior.

The most effective configuration found is shown in Figure 5.43. The dashed red rectangle represents the DIGOTA circuit layout area (not included in the MATLAB electrode calculation). The larger 60 µm×60 µm squares represent the neuron pads, the two 25 µm×16 µm rectangles are the input electrodes, the 10 µm×10 µm squares correspond to the outputs and the common-mode electrodes, and the two remaining rectangles are dummy electrodes.

This configuration was designed with the goal of obtaining a long and narrow configuration, suitable for the CEREBRO application. Moreover, the chosen arrangement considers that, in the TSMC 180nm technology, pads cannot be placed directly on top of the circuit layout.

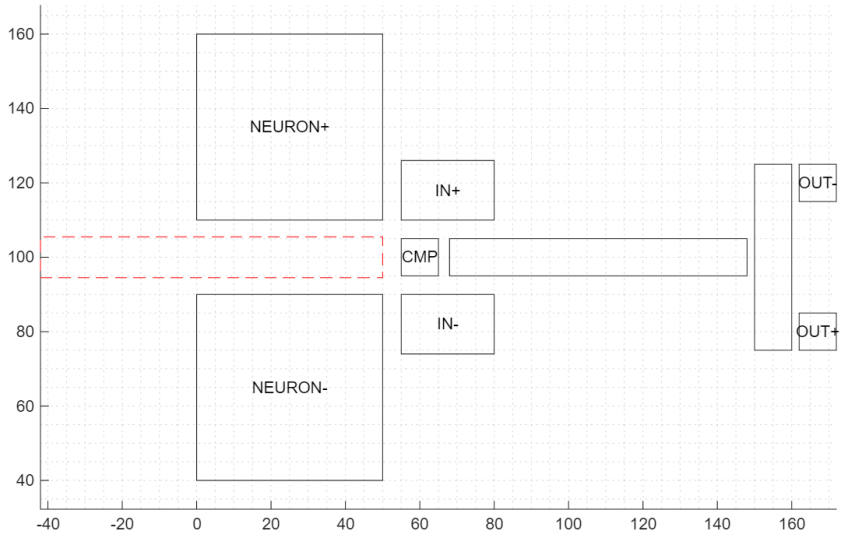


Figure 5.43: Electrode configuration used in Matlab code.

At this point, the electrode layout was created by scaling and adapting the standard pads available in the TSMC18 library (60 µm×60 µm). These were integrated with the previously designed DIGOTA layout, ensuring that no DRC violations occurred.

The final layout, including both the circuit and the electrodes, is shown in Figure 5.44.

In addition to the electrodes already described, four extra 60 µm×60 µm electrodes were added: two to verify signal transmission at the output, and two additional ones to model a neuron. These latter electrodes were placed farther from IN+ and IN- compared to the other neuron electrodes, so they could be used to study how the coupling with the input electrodes varies with distance.

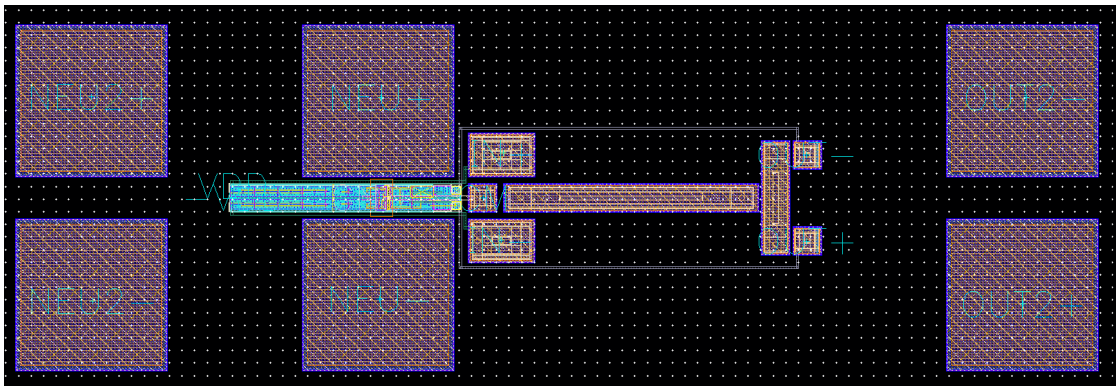


Figure 5.44: Complete circuit layout.

Chapter 6

Conclusion and Future Work

This thesis explored an innovative approach to neural signal acquisition by designing a Digital-Based Operational Transconductance Amplifier (DIGOTA) that uses the parasitic resistance and capacitance of the electrodes as functional components. This strategy enables the development of ultra-compact, low-power circuits, avoiding the need for on-chip passive elements.

The proposed DIGOTA architecture directly encodes the input signal into a high-frequency pulse train. This behavior makes the circuit especially suitable for integration into the CEREBRO project, which aims to achieve high-resolution, non-invasive brain monitoring by reducing signal attenuation through the skull.

The DIGOTA circuit was fully designed and optimized. Its functionality was validated through simulations, including the integration of electrode models, first simplified, then extended with frequency-dependent elements to better represent real conditions. These simulations allowed for the analysis of internal signals and confirmed the correct generation of the modulated pulse train at the output.

The complete layout of the circuit was implemented, and post-layout simulations are performed to evaluate the impact of parasitics. Additional robustness checks, such as transient noise, process corner analysis, and Monte Carlo simulations, further demonstrated the reliability of the design across different conditions and process variations.

Finally, the geometry and positioning of the electrodes were carefully studied to match as close as possible the models used during simulation. The selected configuration was integrated into the final layout.

The circuit has now been sent for tape-out, therefore this project moves from a phase of design and simulation to physical prototyping. Once the manufactured chip is received, the next step is to conduct test both on the standalone amplifier and in a test setup reproducing the characteristics of the operating environment,

to compare with the behavior observed in simulations and improve the future design.

One of the first priorities will be to develop a more accurate model of the electrodes. Up to this point, the electrical behavior of the electrodes was estimated using models based on data found in the literature and adjusted through simplified assumptions. While this approach was sufficient for early simulations, more detailed and specific modeling will be will be necessary to better represent the real electrode characteristics and to improve the next version of the circuit.

Another important aspect will be the analysis of how the electrodes interact with each other. In this work, a simplified MATLAB model was used to estimate resistive coupling between electrodes. While this method was helpful during the initial design phase, it is still based on approximations. Developing a more accurate and realistic model of these interactions lead to better predictions of how the electrodes behave in practice. As a result, better control over desired and undesirable coupling effects can be achieved, and a more precise and realistic circuit design is made possible.

It will also be necessary to investigate how the signal from a neuron couples with the input electrodes. In particular, the tape-out version of the chip includes two neurons, modeled by two pairs of 60×60µm electrodes, that were placed at different distances from the input electrodes. This setup will allow us to observe how signal amplitude changes depending on the distance between the neuron and the sensing electrodes, and collect useful data for future designs.

These tests will also provide the opportunity to further refine the models, improving the design and making necessary adjustments based on the measured performance.

In a later development phase, once the electrode behavior and coupling have been more precisely characterized, the aim will be to reduce the supply voltage. The final objective is to create a fully autonomous system capable of operating under tight power constraints, potentially powered through energy harvesting. Achieving this without compromising signal integrity will be one of the main challenges in the next stages of development.

This work explores different innovative design approaches that may offer valuable insights not only for future neural interfaces, but also for the broader development of compact, low-power biosensing systems. The proposed approach offers a different perspective on circuit design by utilising the physical characteristics of the electrodes and the digital logic gates in an analog front-end circuit.

By rethinking how standard components and environmental characteristics can be used within the system, the design turns limitations into useful features. This kind of architecture may be useful in many fields where strict area and power

constraints are significant challenges

Appendix A

Matlab code

A.1 Bode diagram

```
%% Compute Bode diagram and A_d by removing the transient (for
    variable alpha and fixed Cout)
t_max = 1e5; % Simulation time in Simulink
T_clk=1;
t_D_buffer = 0.1;
t_D_OUT = 0.1;
t_D_CMP = 0.1;
I_out_n = 1;
I_out_p = 1;
I_cmp_n = I_out_n;
I_cmp_p = I_out_p;
Beta = 1;
A = 1; % Input amplitude
t = 0:0.1:t_max; % Time vector
f = logspace(-4, 0, 25); % Input sinewave frequencies
ICout = 0.1; % C_out^-1
alpha_vect = 0.25:0.25:1.25; % alpha = (I/C_out)/(I/C_cmp)

v_in_t = cell(length(alpha_vect), length(f));
v_out_t = cell(length(alpha_vect), length(f));
v_cmp_t = cell(length(alpha_vect), length(f));
bode_mod_all = cell(length(alpha_vect));
bode_phase_all = cell(length(alpha_vect));
Ad_mod_all = cell(length(alpha_vect));
Ad_phase_all = cell(length(alpha_vect));

for k = 1:length(alpha_vect)
    alpha = alpha_vect(k);
    ICcmp = ICout/alpha; % C_cmp^-1
```

```
    IC_out = [t(:), ICout * ones(size(t(:)))];
    IC_cmp = [t(:), ICcmp * ones(size(t(:)))];

    for i = 1:length(f)
        f_in = f(i); % Input frequency for the simulation
        v_in = A.*sin(2*pi*f_in*t);
        v_in_data = [t(:), v_in(:)];

        % Run the simulation in Simulink
        sim('DB_OTA.slx');
        v_out = ans.v_out.Data;
        time = ans.v_out.Time;  % Non-uniform time vector
        v_cmp = ans.v_cmp.Data;
        time1 = ans.v_cmp.Time;

        % Define the signals with respect to a uniform time vector
        v_out = interp1(time, v_out, t, 'linear');
        v_cmp = interp1(time1, v_cmp, t, 'linear');
        v_d = v_in - Beta*v_out;
        v_in_t{k, i} = v_in;
        v_out_t{k, i} = v_out;
        v_cmp_t{k, i} = v_cmp;

        % Remove the first part of the simulation (transient) to
    obtain only the steady-state part
        t_start = 5e4;
        start_index = find(t >= t_start, 1); % Find the index where
    time exceeds t_start
        v_in_reg = v_in(start_index:end);
        v_out_reg = v_out(start_index:end);
        t_reg = t(start_index:end);
        v_d_reg = v_d(start_index:end);

        % FFT computation
        fs = 1 / (t_reg(2) - t_reg(1));  % Sampling frequency (
    inverse of sampling interval)
        N = length(v_in_reg);  % Number of signal samples
        f_fft = fs * (0:N/2-1)/N; % Frequencies for plotting
        fft_in = fft(v_in_reg);  % FFT computation
        fft_in = fft_in(1:N/2); % FFT for positive frequencies only
        fft_out = fft(v_out_reg);
        fft_out = fft_out(1:N/2);
        fft_d = fft(v_d_reg);
        fft_d = fft_d(1:N/2);

        [~, idx_f] = min(abs(f_fft - f_in));  % Index of f_in
    frequency in f vector

        % Magnitude computation at input frequency f_in
```

```
74          fft_in_mod = abs(fft_in(idx_f));
75          fft_d_mod = abs(fft_d(idx_f));
76          fft_out_mod = abs(fft_out(idx_f));
77          bode_mod(i) = 20 * log10(fft_out_mod / fft_in_mod);  % Gain
    in dB
78          Ad_mod(i) = 20 * log10(fft_out_mod / fft_d_mod);  % Gain in
    dB
79
80          % Phase computation at input frequency f_in
81          fft_in_phase = angle(fft_in(idx_f));
82          fft_d_phase = angle(fft_d(idx_f));
83          fft_out_phase = angle(fft_out(idx_f));
84          bode_phase(i) = (fft_out_phase - fft_in_phase)*(180 / pi);  %
     Phase in degrees
85          Ad_phase(i) = (fft_out_phase - fft_d_phase)*(180 / pi);  %
    Phase in degrees
86      end
87      bode_phase = unwrap(bode_phase * (pi/180)) * (180/pi);  % Remove
    phase discontinuities and convert to degrees
88      Ad_phase = unwrap(Ad_phase * (pi/180)) * (180/pi);
89
90      bode_mod_all{k} = bode_mod;
91      bode_phase_all{k} = bode_phase;
92      Ad_mod_all{k} = Ad_mod;
93      Ad_phase_all{k} = Ad_phase;
94  end
95
96  %% Bode and Ad of the comparator
97  for i = 1:length(f)
98      f_in = f(i);
99      v_in = A.*sin(2*pi*f_in*t);
100     v_in_data = [t(:), v_in(:)];
101
102     sim('Comp.slx'); % Run the simulation in Simulink
103     v_out_comp = ans.v_out.Data;
104     time = ans.v_out.Time;  % Non-uniform time vector
105     v_out_comp = interp1(time, v_out_comp, t, 'linear');
106
107     % Remove the first part of the simulation (transient) to obtain
    only the steady-state part
108     t_start = 5e4;
109     start_index = find(t >= t_start, 1);
110     v_in_reg = v_in(start_index:end);
111     v_out_comp_reg = v_out_comp(start_index:end);
112     t_reg = t(start_index:end);
113     v_d_comp = v_in_reg - Beta.*v_out_reg;
114
115     % FFT computation
116     fs = 1 / (t_reg(2) - t_reg(1));  % Sampling frequency
```

```
117     N = length(v_in_reg);  % Number of signal samples
118     f_fft = fs * (0:N/2-1)/N; % Frequencies for plotting
119     fft_in = fft(v_in_reg);  % FFT computation
120     fft_in = fft_in(1:N/2); % FFT for positive frequencies only
121     fft_out = fft(v_out_reg);
122     fft_out = fft_out(1:N/2);
123     fft_d = fft(v_d);
124     fft_d = fft_d(1:N/2);
125
126     [~, idx_f] = min(abs(f_fft - f_in));  % Index of f_in frequency
    in f vector
127
128     % Magnitude computation at input frequency f_in
129     fft_in_mod = abs(fft_in(idx_f));
130     fft_d_mod = abs(fft_d(idx_f));
131     fft_out_mod = abs(fft_out(idx_f));
132     bode_mod_comp(i) = 20 * log10(fft_out_mod / fft_in_mod);  % Gain
    in dB
133     Ad_mod_comp(i) = 20 * log10(fft_out_mod / fft_d_mod);  % Gain in
    dB
134
135     % Phase computation at input frequency f_in
136     fft_in_phase = angle(fft_in(idx_f));
137     fft_d_phase = angle(fft_d(idx_f));
138     fft_out_phase = angle(fft_out(idx_f));
139     bode_phase_comp(i) = (fft_out_phase - fft_in_phase)*(180 / pi);
    % Phase in degrees
140     Ad_phase_comp(i) = (fft_out_phase - fft_d_phase)*(180 / pi);  %
    Phase in degrees
141 end
142
143 % Plot of v_in(t) and v_out(t) for different frequencies
144 [~, idx1] = min(abs(f - 1e-4));
145 [~, idx2] = min(abs(f - 1e-3));
146 [~, idx3] = min(abs(f - 1e-2));
147 [~, idx4] = min(abs(f - 1e-1));
148 indices = [idx1, idx2, idx3, idx4]; % Indices of the frequencies to
    plot
149
150 figure; % Plot signals for selected frequencies
151 for j = 1:length(indices)
152     idx_f = indices(j);
153     subplot(2, 2, j);
154     hold on;
155     for k = length(alpha_vect):-1:1   % Plot v_out for each alpha
156         plot(t, v_out_t{k, idx_f}, 'Linewidth', 1);
157     end
158     plot(t, v_in_t{k, idx_f}, 'Linewidth',1,'DisplayName','v_{in}');
```

```
159     plot(t, v_out_comp(idx_f), 'Linewidth',1,'DisplayName','v_{out,
        comp}');
160     title(sprintf('f_{in} = %.4f', f(idx_f)));
161     xlabel('t');
162     ylabel('v(t)');
163     legend('show', 'Location', 'best');
164     grid on;
165     legend(arrayfun(@(x) sprintf('\\alpha = %.2f', x), alpha_vect, '
        UniformOutput', false));
166     if j == 1
167         xlim([5e4 7e4]);  % Zoom for the first subplot
168     elseif j == 2
169         xlim([5e4 5.2e4]);  % Zoom for the second subplot
170     elseif j == 3
171         xlim([5e4 5.02e4]);  % Zoom for the third subplot
172     elseif j == 4
173         xlim([5e4 5.002e4]);  % Zoom for the fourth subplot
174     end
175 end
176
177 figure; % Bode plot
178 subplot(2, 1, 1);
179 hold on;
180 for k = 1:length(alpha_vect)
181     p = semilogx(f(1:end-1), bode_mod_all{k}(1:end-1),'LineWidth',1);
182     p.Marker = ".";
183     p.MarkerSize = 15;
184 end
185     p1 = semilogx(f(1:end-1), bode_mod_comp(1:end-1),'LineWidth',1,'
        DisplayName', 'Comparator');
186     p1.Marker = ".";
187     p1.MarkerSize = 20;
188 xlabel('Frequency');
189 ylabel('|H(f)| (dB)');
190 set(gca, 'XScale', 'log');
191 grid on;
192 subplot(2, 1, 2);
193 hold on;
194 for k = 1:length(alpha_vect)
195     p = semilogx(f, bode_phase_all{k}, 'LineWidth', 0.1);
196     p.Marker = ".";
197     p.MarkerSize = 15;
198 end
199 legend(arrayfun(@(x) sprintf('\\alpha = %.2f', x), alpha_vect, '
        UniformOutput', false));
200 xlabel('Frequency');
201 ylabel('$\angle H(f) \, (^\circ)$', 'Interpreter', 'latex');
202 set(gca, 'XScale', 'log');
203 grid on;
```

```
204
205 figure;
206 subplot(2, 1, 1);
207 hold on;
208 for k = 1:length(alpha_vect)
209     p = semilogx(f(1:end-1), Ad_mod_all{k}(1:end-1),'LineWidth',0.1);
210     p.Marker = ".";
211     p.MarkerSize = 15;
212 end
213 xlabel('Frequency');
214 ylabel('|A_d(f)| (dB)');
215 set(gca, 'XScale', 'log');
216 grid on;
217 subplot(2, 1, 2);
218 hold on;
219 for k = 1:length(alpha_vect)
220     p = semilogx(f, Ad_phase_all{k}, 'LineWidth', 0.1);
221     p.Marker = ".";
222     p.MarkerSize = 15;
223 end
224 legend(arrayfun(@(x) sprintf('\\alpha = %.2f', x), alpha_vect, '
    UniformOutput', false));
225 xlabel('Frequency');
226 ylabel('$\angle A_d(f) \, (^\circ)$', 'Interpreter', 'latex');
227 set(gca, 'XScale', 'log');
228 grid on;
```

A.2 SNDR

```
1  %% Compute SNDR with respect to B (for variable Cout and fixed alpha)
2  t_max = 1e5; % Simulation time in Simulink
3  T_clk=1;
4  t_D_buffer = 0.1;
5  t_D_OUT = 0.1;
6  t_D_CMP = 0.1;
7  I_out_n = 1;
8  I_out_p = 1;
9  I_cmp_n = I_out_n;
10 I_cmp_p = I_out_p;
11 Beta = 1;
12 alpha = 0.5; % alpha = (I/C_out)/(I/C_cmp)
13 alpha_vect = 0.25:0.25:1.25; % Different values of alpha
14 ICout = 0.1;
15 B = linspace(0.01, 0.5, 10); % Bandwidth values for SNDR calculation
16 SNDR_matrix = zeros(length(ICout), length(B)); % to store the results
```

```
A = 1; % Input amplitude
t = 0:0.1:t_max; % Time vector
f_in = 1e-3;
v_in = A.*sin(2*pi*f_in*t);
v_in_data = [t(:), v_in(:)];

for k = 1:length(alpha_vect)
    alpha = alpha_vect(k); % C_out^-1
    ICcmp = ICout/alpha; % C_cmp^-1
    IC_out = [t(:), ICout * ones(size(t(:)))];
    IC_cmp = [t(:), ICcmp * ones(size(t(:)))];

    sim('DB_OTA.slx'); % Run Simulink simulation
    v_out = ans.v_out.Data;
    time = ans.v_out.Time;  % Non-uniform time vector
    v_cmp = ans.v_cmp.Data;
    time1 = ans.v_cmp.Time;

    % Define signals with respect to a uniform time vector
    v_out = interp1(time, v_out, t, 'linear');
    v_cmp = interp1(time1, v_cmp, t, 'linear');
    v_d = v_in - Beta*v_out;
    v_out_matrix(k, :) = v_out;
    v_cmp_matrix(k, :) = v_cmp;
    v_d_matrix(k, :) = v_d;

    % Remove the first part of the simulation (transient) to keep
    only steady-state
    t_start = 5e3;
    start_index = find(t >= t_start, 1); % Find the index where time
    exceeds t_start
    v_in_reg = v_in(start_index:end);
    v_out_reg = v_out(start_index:end);
    v_cmp_reg = v_cmp(start_index:end);
    v_d_reg = v_d(start_index:end);
    t_reg = t(start_index:end);

    % Compute FFT
    fs = 1 / (t(2) - t(1));  % Sampling frequency
    N = length(v_in_reg);  % Number of samples
    f_fft = fs * (0:N/2-1)/N; % Frequency axis for the plot

    fft_v_in = fft(v_in_reg);  % FFT computation
    fft_v_in = fft_v_in(1:N/2); % Keep only positive frequencies
    fft_v_in_mod = abs(fft_v_in)/(N/2); % Magnitude
    fft_v_in_phase = angle(fft_v_in); % Phase in radians

    fft_v_out = fft(v_out_reg);
    fft_v_out = fft_v_out(1:N/2);
```

```
64      fft_v_out_mod = abs(fft_v_out)/(N/2);
65      fft_v_out_phase = angle(fft_v_out);
66      fft_out_matrix(k, :) = fft_v_out_mod;
67
68      fft_v_cmp = fft(v_cmp_reg);
69      fft_v_cmp = fft_v_cmp(1:N/2);
70      fft_v_cmp_mod = abs(fft_v_cmp)/(N/2);
71      fft_v_cmp_phase = angle(fft_v_cmp);
72      fft_cmp_matrix(k, :) = fft_v_cmp_mod;
73
74      fft_v_d = fft(v_d_reg);
75      fft_v_d = fft_v_d(1:N/2);
76      fft_v_d_mod = abs(fft_v_d)/(N/2);
77      fft_v_d_phase = angle(fft_v_d);
78      fft_d_matrix(k, :) = fft_v_d_mod;
79
80      % Compute SNDR for different bandwidths
81      for i = 1:length(B)
82          band = B(i);
83
84          [~, idx_f] = min(abs(f_fft - f_in)); % Find index of
    fundamental frequency f_in
85          P_signal = (fft_v_out_mod(idx_f))^2; % Power of fundamental
    component
86          band_idx = find(f_fft <= band);
87          fft_v_out_band = fft_v_out_mod(band_idx); % FFT components
    in the selected band
88          fft_v_out_band(idx_f) = 0; % Exclude the fundamental
    component
89          P_noise_distortion = sum( fft_v_out_band.^2); % Residual
    power: noise + distortion
90          SNDR_matrix(k, i) = 10 * log10(P_signal / P_noise_distortion)
    ; % Save SNDR in dB
91      end
92  end
93
94  figure; % plot SNDR
95  hold on;
96  colors = lines(length(alpha_vect));
97  for k = 1:length(alpha_vect)
98      plot(B, SNDR_matrix(k, :), 'LineWidth', 0.1, 'DisplayName',
    sprintf('\\alpha = %.2f', alpha_vect(k)), 'Color', colors(k, :));
99      plot(B, SNDR_matrix(k, :), '.', 'MarkerSize', 15, 'Color', colors
    (k, :), 'HandleVisibility', 'off');
100 end
101 xlabel('Bandwidth');
102 ylabel('SNDR (dB)');
103 legend('show', 'Location', 'Best');
104 grid on;
```

```
105 hold off;
106
107 figure;
108 for  k = 1:length(alpha_vect)
109     loglog(f_fft, fft_out_matrix(k, :), '.', 'MarkerSize', 15, '
    DisplayName', sprintf('\\alpha = %.2f', alpha_vect(k)));
110     hold on;
111 end
112 xlabel('Frequency');
113 ylabel('|V_{out}|');
114 legend('show', 'Location', 'Best');
115 grid on;
116
117 figure;
118 for k = 1:length(alpha_vect)
119     loglog(f_fft, fft_cmp_matrix(k, :), '.', 'MarkerSize', 15, '
    DisplayName', sprintf('\\alpha = %.2f', alpha_vect(k)));
120     hold on;
121 end
122 xlabel('Frequency');
123 ylabel('|V_{cmp}|');
124 legend('show', 'Location', 'Best');
125 grid on;
126
127 figure; % plot v_out
128 for idx = 1:length(alpha_vect)
129     plot(t, v_out_matrix(idx, :), 'Linewidth', 1, 'DisplayName',
    sprintf('\\alpha = %.2f', alpha_vect(idx)));
130     hold on;
131 end
132 xlabel('Time');
133 ylabel('|V_{out}(t)|');
134 legend('show', 'Location', 'Best');
135 grid on;
136 xlim([5e3 6e3])
```

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