Master Thesis in Electronics Engineering –2024/2025

Hardware Design for Distributed AC Microgrid Management and Power Measurement

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Summary

This thesis presents the design, implementation, and validation of a three-phase energy monitoring system based on the ATM90E32AS measurement IC and an STM32 microcontroller. The system is built on a custom-designed PCB that integrates power management, measurement, control, and communication functions in a compact and isolated architecture.

The measurement IC provides real-time values for voltage, current, frequency, and power parameters. To ensure accuracy and signal integrity, the PCB layout was carefully designed with short, symmetric traces for analog inputs, clear separation of analog and digital grounds, and localized decoupling capacitors. The IC is powered by an isolated 3.3V supply, derived from a 24V input through a three-stage conversion: isolated ±15V, a buck converter to 5V, and an LDO to 3.3V. Seven onboard LEDs provide visual confirmation of power availability at each stage.

For communication, SPI lines between the MCU and the measurement IC are isolated. This ensures robust, noise-free operation and protection against electrical disturbances. A relay control section was included, allowing the MCU to switch external loads via a transistor-driven electromechanical relay. DIP switches connected to MCU GPIOs were used for configuration and address selection.

The system supports CAN communication for data exchange, using a custom DBC file to define messages and signal mapping. PCAN-USB and PCAN-View were used to send and monitor messages, while a finite state machine (FSM) enabled reading of up to six measurement registers within the limitations of the PLECS environment.

Each subsystem—including power, SPI, GPIO, relay, and CAN—was independently tested using PLECS programming, multimeters, and oscilloscopes. Results confirmed correct operation.

Acknowledgment

I would like to express my deepest gratitude to all those who supported me throughout the development of this research. Foremost among them is my beloved brother, whose constant presence, silent strength, and unwavering belief in me have been a profound source of comfort and motivation — truly, his support has always been a steady refuge in my mind and heart.

I am also sincerely thankful to my friends and classmates, whose encouragement, patience, and companionship helped me navigate the challenges of this journey. Without their presence, this path would have been far more difficult and far less meaningful.

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In Appreciation

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I hope I have lived up to the expectations of Politecnico di Torino and Professor Mandrile because, from the bottom of my heart, I truly gave my best.

می‌خواهم با تمام وجود از خانواده‌ام تشکر کنم؛

از پدر عزیزم، مادر مهربانم، برادرم همیشه همراهم، و در نهایت از خودم.

سپاس که در همه لحظات سخت، پشتم بودید.

سپاس که به من ایمان داشتید، حتی زمانی‌که خودم به تردید افتاده بودم.

هر بار که خسته و ناامید شدم، گرمای حضورتان امیدم شد و لبریز از شکرگزاری شدم که چنین گنجی را در کنار خود دارم.

مامان، تو قوی‌ترین زن دنیایی.

در روزهایی که هزار درد را در دل داشتی و من از تو دور بودم، باز هم ایستادی، بی‌صدا، بی‌ادعا.

تو معنای واقعی استقامت و عشق هستی.

بابا، قهرمان زندگی منی.

با تمام وجود امیدوارم روزی آن‌چنان تکیه‌گاهی برای خانواده‌ام باشم که تو برای ما بودی؛

مردی با شانه‌هایی محکم و دلی پر از مهربانی.

جواد، برادر نازنینم، رفیقِ راه و روزهای سخت...

اگر تو نبودی، شاید خیلی چیزها برایم فقط یک رویا می‌ماند.

و در نهایت...

مرسی از خودم؛

که با تمام زخم‌ها، فشارها، دلتنگی‌ها و روزهای طاقت‌فرسا،

نایستادم، عقب نکشیدم، و ادامه دادم.

سه سالی که ساده نبود، اما من ساده تسلیم نشدم.

به امید ایران آزاد.

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Chapter 1

1. Introduction

1.1 Introduction and Motivation

The transition toward distributed energy systems, driven by the increased adoption of renewable energy sources such as solar and wind, has highlighted the need for localized energy management solutions like microgrids. These systems not only enhance resilience and efficiency but also reduce dependency on centralized power grids by enabling the integration of renewable generation, storage, and distribution within a flexible, decentralized framework. As renewable energy sources are inherently intermittent, the importance of intelligent systems capable of managing these variations is critical for ensuring grid stability and reliability.

This thesis is motivated by the growing need for a smart microgrid node designed to address these challenges. The proposed node incorporates advanced capabilities, including managing power flow, dynamically connecting and disconnecting microgrid branches based on operational requirements, and measuring critical electrical quantities such as active and reactive power, voltage, and frequency. These features are essential for enabling microgrids to operate autonomously or in coordination with larger power systems.

The hardware developed integrates power electronics and embedded systems to achieve precise measurement and robust control of energy distribution within an AC microgrid branch. Furthermore, the design prioritizes scalability and adaptability, ensuring compatibility with diverse renewable energy configurations and grid environments. By focusing on efficient power flow management and reliable operation, this work contributes to the broader objectives of enhancing the sustainability, resilience, and efficiency of modern energy systems.

Chapter 2

2. Schematic

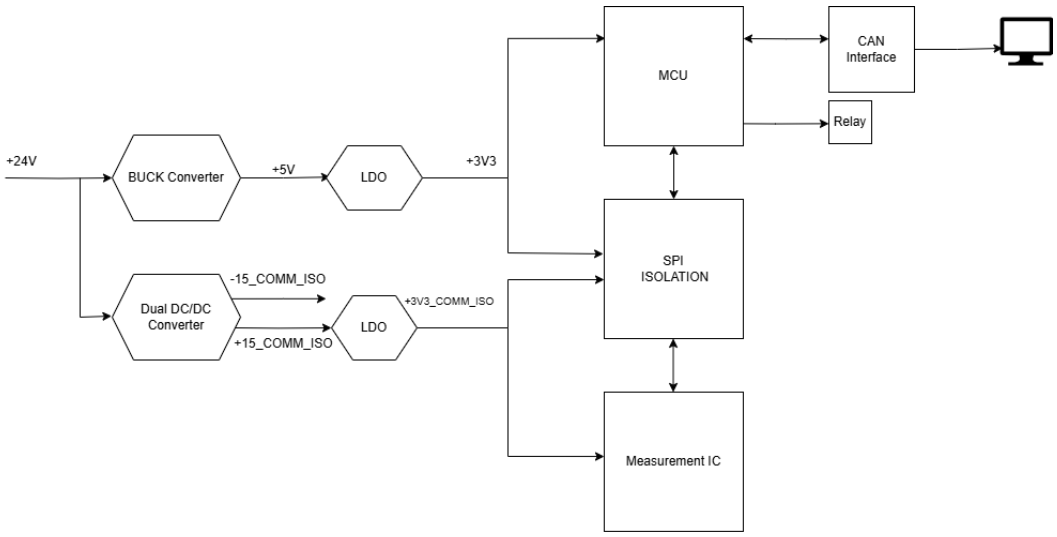

Figure 1: General Schematic

The project centers around a smart electrical monitoring system powered by a 24V input, which is carefully regulated through a series of buck converters and LDOs to supply the various voltage domains required across the board. This power architecture supports critical components such as the measurement IC, the microcontroller unit (MCU), and the communication interface.

At its core, the system measures essential electrical parameters from a three-phase source—such as voltage, current, frequency, active power, reactive power, apparent power, and power factor—using a high-precision measurement IC. To preserve signal integrity and protect low-voltage digital circuitry from disturbances in the high-voltage domain, the communication between the measurement IC and the MCU is fully isolated, including both the SPI data lines and interrupt signals (IRQ0 and IRQ1).

Once data is acquired and processed, it is transmitted to an external monitoring unit via the CAN interface, allowing for robust and efficient visualization of real-time power data. This integrated design enables accurate and immune monitoring of

electrical parameters in demanding environments, forming a compact, safe, and communication-ready solution.

2.1 Power Supply

The power supply section of this project is a critical component, providing the necessary power for the entire system to operate. It is designed to step down a 24V input voltage to two regulated output voltages: 5V and 3.3V. These voltages are essential for powering different parts of the system, ensuring reliable and stable operation of all the components. The circuit consists of two primary stages: two buck converters and a Low Dropout (LDO) regulator. Additionally, it includes LEDs to indicate the presence of supplies, simplifying monitoring and debugging.

2.1.1 Buck Converter

The buck converter in this design steps down the input voltage of 24V to a regulated 5V. It is implemented using the TPS62933DRLR, a high-efficiency synchronous buck converter from Texas Instruments which can handle up to 3A. To stabilize the input voltage and filter out noise, a 33 µF aluminum polymer capacitor (C36) is used at the input (that is the input capacitor of Isolated dual power supply. The inductor (HCM0703-2R2-R) plays a key role in ensuring a smooth current flow during the voltage conversion process.

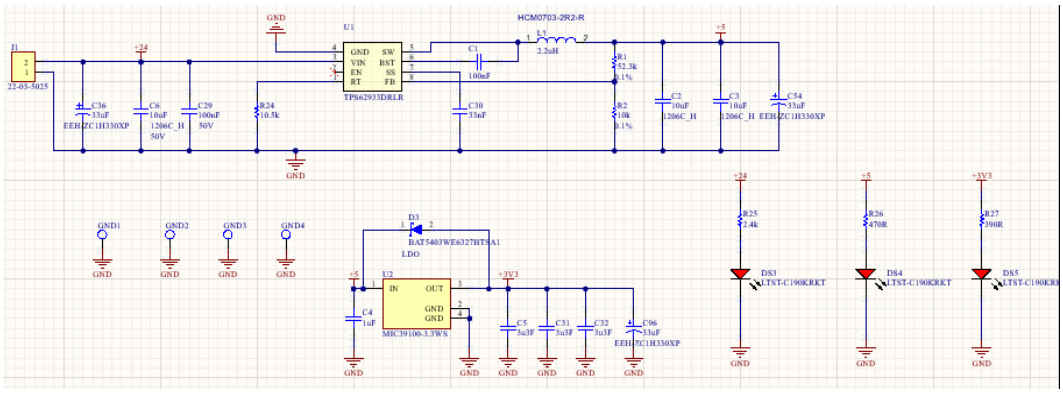

Figure 2: Power Supply

The output voltage is configured to 5V using a feedback network consisting of resistors R2 and R1. Additional capacitors (C2, and C3) are placed at the output to ensure stable operation and suppress switching noise. A bootstrap capacitor is included to enhance the gate drive voltage for the internal MOSFETs of the converter. The design of this buck converter was optimized using the "Webench Circuit Designer tool", ensuring high efficiency and reliable thermal management. The 5V output from this stage serves as the input to the next stage, the LDO, and also powers other 5V components in the system.

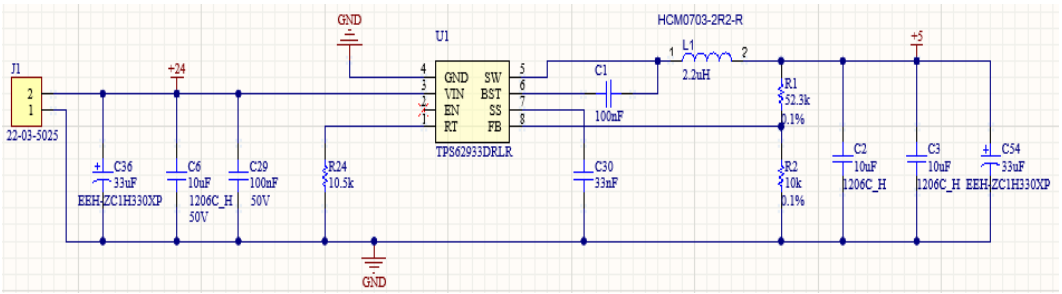

Figure 3:BUCK converter

2.1.2 LDO (Low Dropout Regulator)

The LDO regulator further steps down the 5V output of the buck converter to a clean and stable 3.3V to supply the digital control logic. This stage is implemented using the **MIC39100-3.3WS**, a low dropout regulator designed for low-noise applications. It provides a highly regulated output suitable for sensitive components in the system that require precise voltage levels.

The circuit includes an input capacitor (C4) to filter the incoming 5V and multiple output capacitors (C31, C32, C96 and C5) to ensure low output impedance and enhanced stability. To protect the LDO from reverse voltage, a protection diode (D3) is incorporated. The 3.3V output powers critical parts of the system that demand stable and noise-free voltage, ensuring the smooth operation of these components.

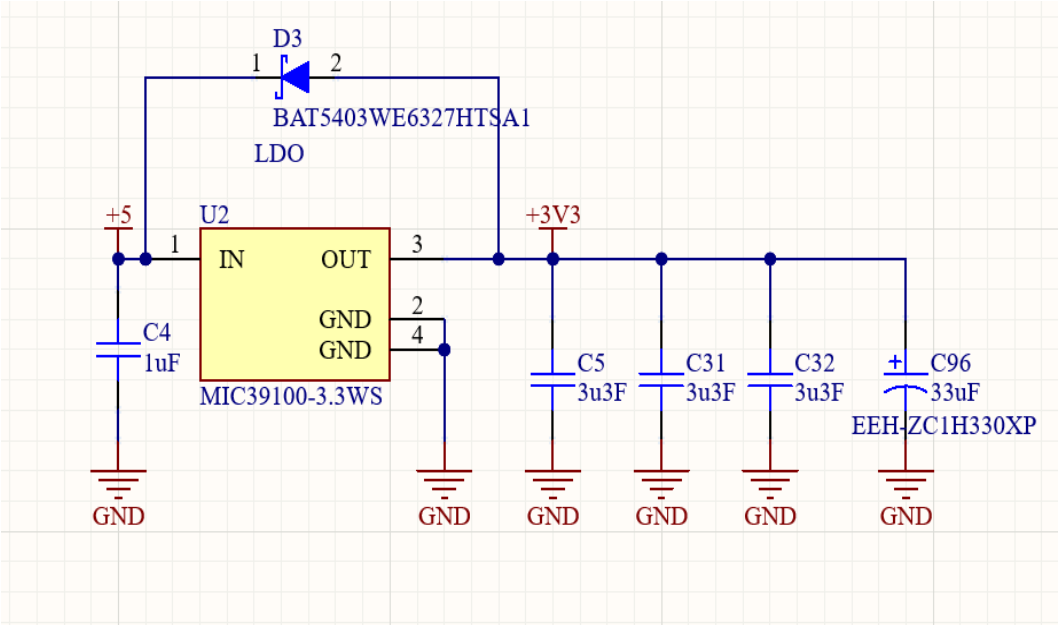

Figure 4: Low Dropout Regulator 5V to 3V3

2.1.3 LEDs

To provide visual feedback on the status of the power supply, three LEDs are included in the design, each corresponding to one of the voltage levels.

DS3 indicates the presence of the 24V input.

DS4 confirms the availability of the 5V output from the buck converter.

DS5 indicates the 3.3V output from the LDO regulator.

Each LED is connected in series with a current-limiting resistor (R25, R26, and R27) to regulate the current and protect the LEDs from damage. These LEDs allow for easy monitoring of the power supply, providing quick visual confirmation of the system's power state during operation and debugging.

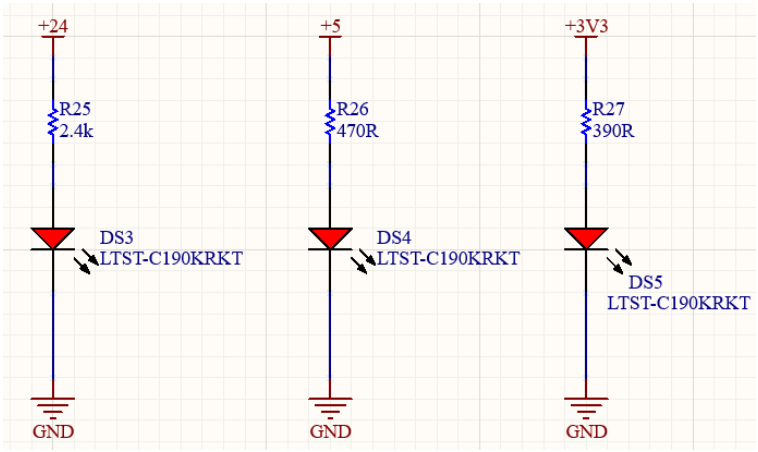

Figure 5 : MCU's LEDs

2.1.4 Ground Points (GND1:4)

The circuit includes test points, labeled GND1 through GND4, to provide convenient access for measurements and debugging. These points ensure stable ground connections for accurate voltage and current testing, aiding in performance verification and troubleshooting, especially in high-frequency circuits like the buck converter.

2.2 Micro Controller Unit

The central component of the schematic is the **STM32G474RET3**, a high-performance ARM Cortex-M4 microcontroller with an integrated Floating-Point Unit (FPU). This MCU features a wide range of peripherals, including communication interfaces, advanced timers, and analog capabilities, making it ideal for complex embedded system applications. The schematic integrates several supporting components and connections to ensure reliable operation, debugging, and communication.

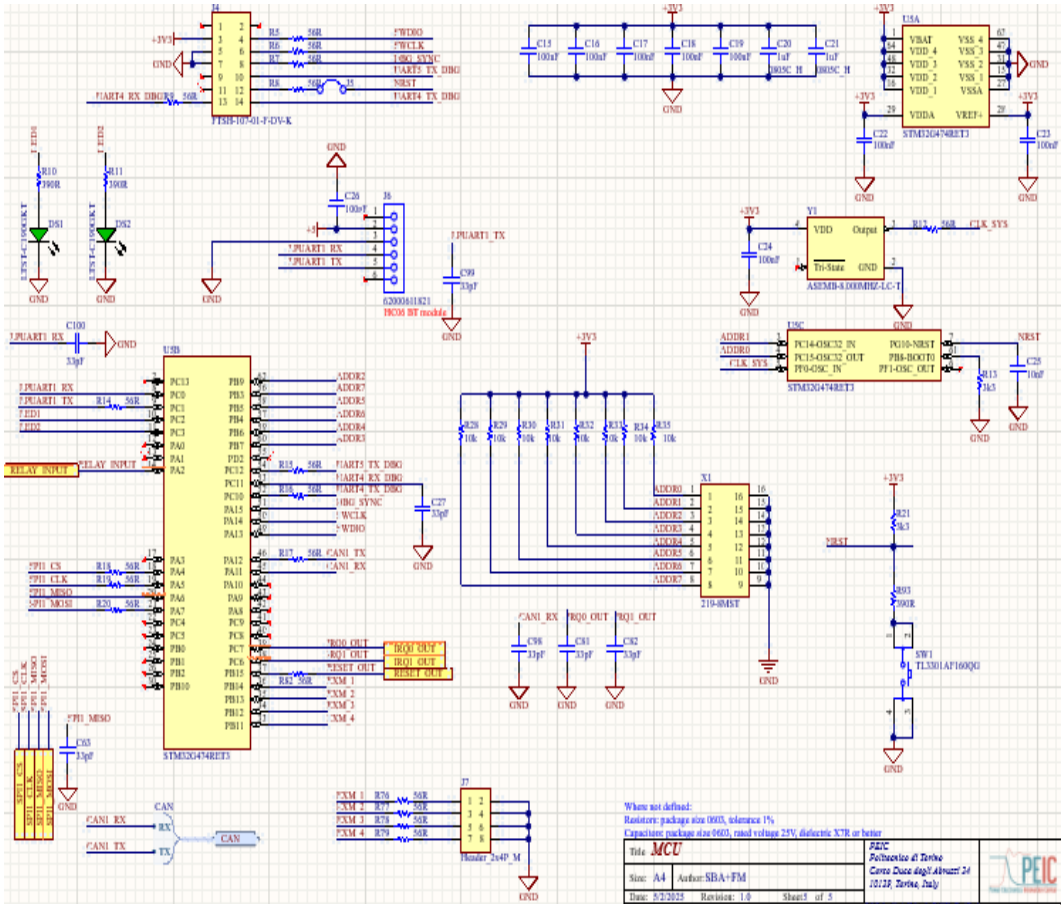

Figure 6: Micro Control Unit

2.2.1 Debugging and Communication Interface

The **FTSH-107-01-F-DV-K** connector is a 14-pin header that interfaces the microcontroller to its programmer. It provides versatile access to the microcontroller through the SWD (Serial Wire Debug) and UART protocols.

Below is a detailed explanation of each connection:

- **SWDIO (Pin 4)** → **PA13**: Serial Wire Debug Input/Output

Purpose: The SWDIO line is part of the Serial Wire Debug (SWD) interface, which is a two-wire protocol for programming and debugging ARM Cortex-M microcontrollers.

Functionality: This pin serves as a bidirectional data line, enabling communication between the MCU and the debugger. It is used to send instructions to the MCU or retrieve debugging data during operation.

- **SWCLK (Pin 6)** → **PA14**: Serial Wire Debug Clock

Purpose: The SWCLK line provides the clock signal necessary for the SWD interface to synchronize communication between the debugger and the microcontroller.

Functionality: This unidirectional signal ensures precise timing for data exchange, allowing reliable operation of the SWD protocol. Together with SWDIO, it forms the backbone of the debugging interface.

- **DBG SYNC (Pin 8)** → **PA15**: Debug Sync Signal

Purpose: The debug sync signal is used to synchronize external debugging operations or monitor specific debugging events.

Functionality: This pin can be configured as a user-defined signal to aid in synchronization during advanced debugging scenarios, such as tracking real-time events in complex systems.

- **UART5 TX DBG (Pin 10)** → **PC12**: UART5 Transmission for Debug Communication

Purpose: This pin is the transmit line for the UART5 interface, allowing the microcontroller to send data to external debugging tools or monitoring devices.

Functionality: It facilitates data logging, status reporting, or real-time communication during debugging, providing valuable insights into system behavior.

- **<u>UART4_RX_DBG (Pin 13)</u>** → **PC11**: UART4 Reception for Debug Communication

Purpose: The UART4 RX pin serves as the receive line for the UART4 interface, allowing the microcontroller to receive data from external debugging tools.

Functionality: This enables commands, updates, or configuration settings to be sent to the MCU during debugging or system operation.

- **<u>UART4_TX_DBG (Pin 14)</u>** → **PC10**: UART4 Transmission for Debug Communication

Purpose: The UART4 TX pin is the transmit line for the UART4 interface, providing an additional communication channel for the MCU to send data.

Functionality: This channel can be used alongside UART5 to provide dual-channel debugging or for system-level communication during development.

- **<u>NRST (Pin 12)</u>** → **NRST Pin of MCU**: Reset Line

Purpose: The NRST pin is connected to the microcontroller's reset line, allowing the system to be reset manually or programmatically.

Circuit Design: A debounce circuit comprising a resistor and capacitor stabilizes the reset signal, preventing unintentional resets due to noise or transient signals. A push-button switch is also included to allow manual resets.

Functionality: This feature is essential for troubleshooting and recovering the MCU from unexpected states during debugging. It ensures a clean system reboot, returning the microcontroller to a known state.

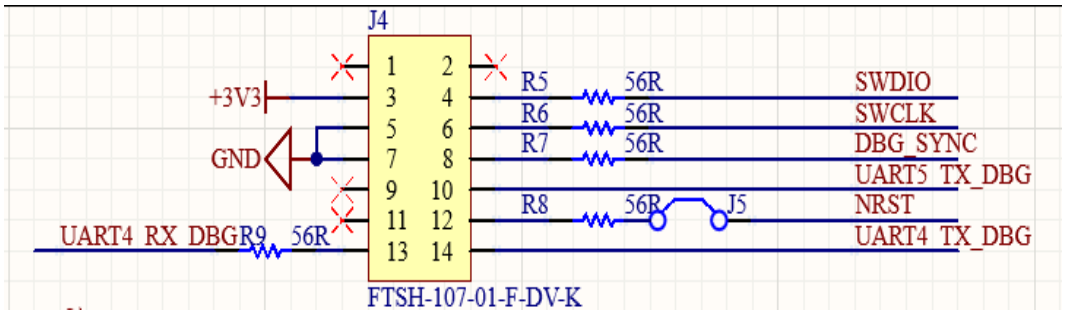

Figure 7: Connector Header for programming and debugging

2.2.2 Oscillator

The clock source for the microcontroller is an **ASEMB-8.000MHZ-LC-T** oscillator, operating at 8MHz. This ensures accurate timing and synchronization for the MCU and its peripherals.

2.2.3 LPUART1's Header

The schematic includes a 6-pin header **(62000611821)**, which is connected to the LPUART1 (Low-Power UART) interface of the **STM32G474RET3** microcontroller. This header facilitates external communication by providing access to the LPUART1's transmits and receive pins, specifically PC0 (TX) and PC1 (RX).

The LPUART1 interface is designed for low-power applications, ensuring efficient data transfer while minimizing energy consumption. This feature makes it ideal for systems requiring periodic communication with external devices, such as sensors, controllers, or diagnostic tools.

The 6-pin header serves as a connection point for external peripherals, enabling the microcontroller to send and receive data through serial communication. This design allows for straightforward integration with debugging tools, programming devices, or communication modules, offering flexibility in expanding the system's capabilities. This can be optionally connected to a Bluetooth module, allowing for wireless communication with other devices such as smartphones, PCs, or embedded systems, thereby enhancing the versatility and mobility of the overall design.

Decoupling capacitors are typically included near the header and the microcontroller to filter noise and maintain signal integrity during communication, ensuring reliable data transfer between the microcontroller and the connected devices.

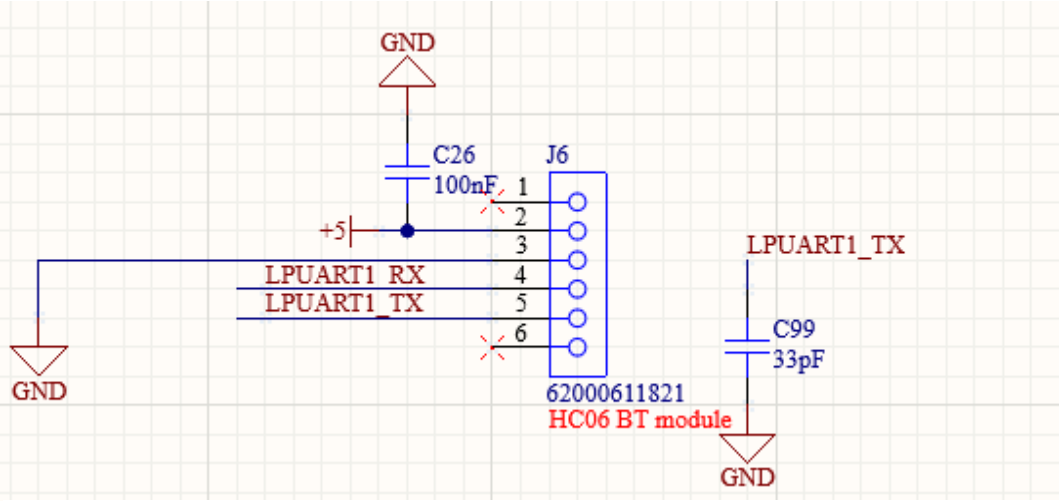

Figure 8: LPUART1 Header

2.2.4 Header_2x4P_M

The Header_2x4P_M is an 8-pin connector used in the design to provide flexibility for future expansion. It connects four general-purpose I/O pins from the MCU (EXM_1 to EXM_4) to external circuits or modules, with alternating pins tied to GND (pins 2, 4, 6, 8) to ensure proper grounding. While these EXM pins currently do not serve a specific function, they are included in the design to allow for potential use in future features, testing, or debugging without requiring a redesign of the PCB.

2.2.5 DIP Switches

The 8-position DIP switch is a simple and effective way to assign a unique address to each board in systems where multiple devices operate on the same network, such as over CAN. By manually setting each of the 8 switches to either ON or OFF, you can define an 8-bit binary value that corresponds to a decimal address from 0 to 255. This address is read by the MCU at startup and used to identify the board in communication protocols. the DIP switch allows for easily configurable, hardware-based addressing without the need for reprogramming.

2.2.6 LED

In the schematic, two LEDs are connected to the microcontroller through current-limiting resistors. These LEDs are controlled by GPIO pins and serve as general-purpose indicators. While their specific function is not fixed in hardware, they are typically used to signal the system status, such as power-on, fault detection, or communication activity. Their behavior can be defined through firmware to provide visual feedback during operation or debugging.

2.3 Relay Control

The relay control circuit is designed to enable the activation and deactivation of a relay (K2) using a low-power input signal. The control signal, labeled as RELAY INPUT that comes from the MCU, is applied to the base of an NPN transistor (Q2). This transistor acts as a switch to control the flow of current through the relay coil. When the control signal is high (above the base threshold voltage of the transistor), the transistor turns on, allowing current to pass from the +5V supply through the relay coil and the transistor. This current energizes the coil, creating a magnetic field that activates the relay's internal switch. This relay, in turn, operates the 3-phase contactor coil located in the box, enabling it to control a connected load, external devices, or systems that require isolation from the low-power control circuit.

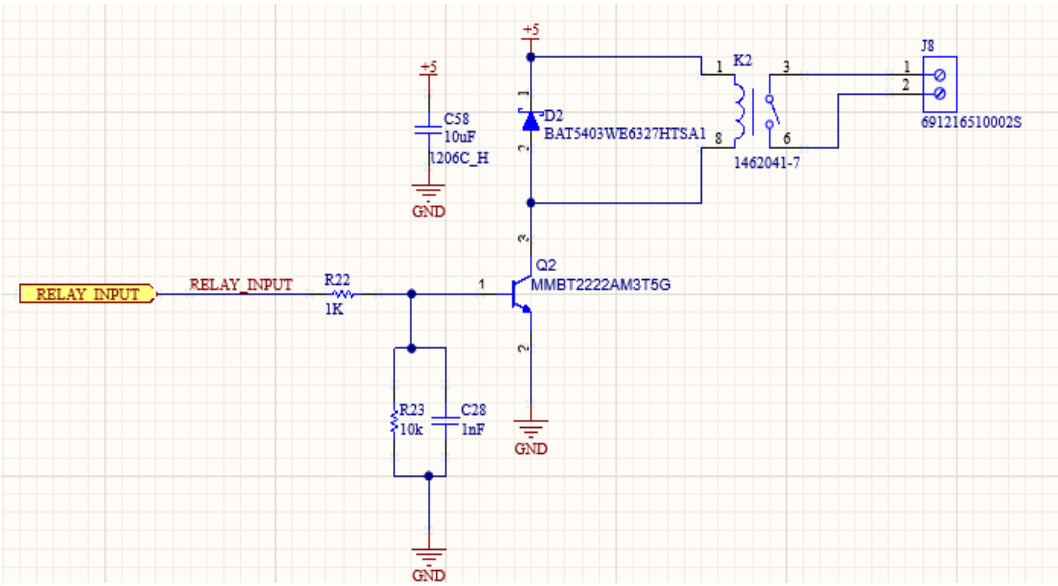

Figure 9: Relay Control

The circuit also includes protective and stabilizing components such as resistors, capacitors, and a diode. These ensure that the relay operates reliably and is protected from voltage spikes caused by the inductive nature of the coil when switching off. This design makes it possible to control high-power or high-voltage devices using a low-power control signal.

2.3.1 Electromechanical Relay:

The relay **(1462041-7)** itself is the main switching component in Relay control circuit. It contains an internal coil and switch. When the coil is energized by current flowing through it, the internal switch closes, allowing the relay to control a separate, high-power load. This load is connected via the output terminal (J8). The relay ensures electrical isolation between the control circuit and the load, making it suitable for safely switching high-power or high-voltage circuits using low-power signals**.**

2.4 CAN Interface

The Controller Area Network (CAN) is a robust communication protocol designed for efficient and reliable data exchange in distributed systems, especially in environments where high reliability and real-time data transfer are crucial. It utilizes a two-wire differential signaling system—CANH and CANL—to minimize noise interference and ensure stable communication, even in electrically noisy environments. CAN is commonly used in automotive, industrial, and embedded systems due to its ability to support multiple nodes, provide priority-based message handling, and feature robust error detection mechanisms. In this design, the CAN communication interface connects the microcontroller's pins, such as PA12 and PA11, to the respective CAN1_TX and CAN1_RX lines, allowing the microcontroller to send and receive CAN messages. When connected to an external system or PC via a USB-to-CAN adapter, the messages transmitted and received over this interface can be interpreted using a DBC (Database CAN) file. The DBC file defines the structure of the CAN messages—including message IDs, signal names, bit lengths, scaling, and offsets—allowing engineers and diagnostic software to translate raw data into meaningful, human-readable information such as sensor values, statuses, and commands

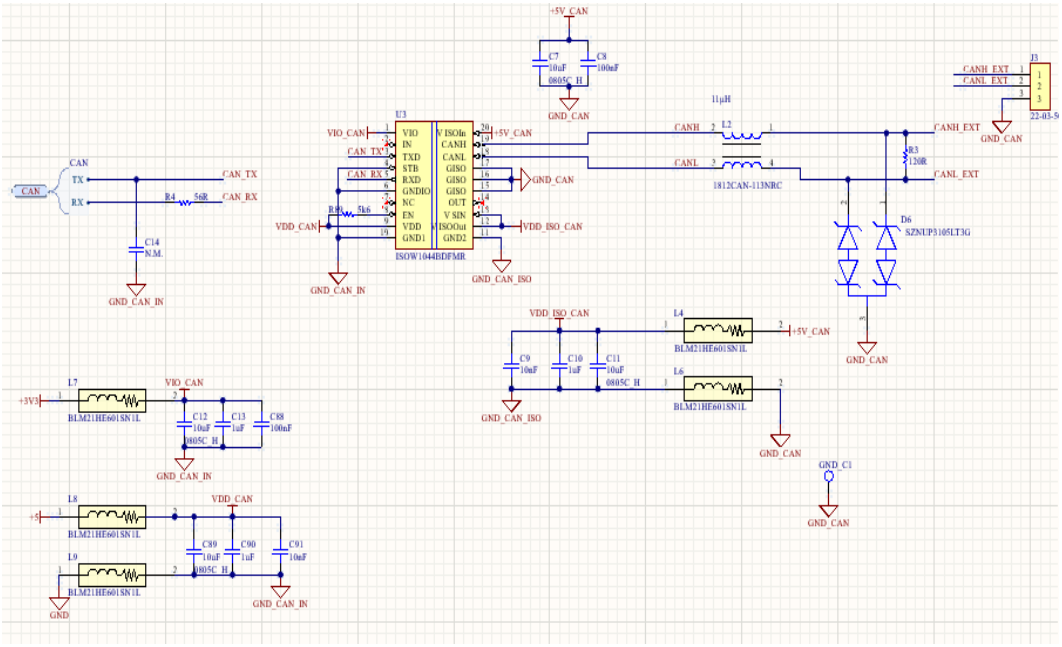

Figure 10: CAN interface

2.4.1 Isolated CAN Transceiver

The **ISOW1044BDFMR** transceiver is chosen for its ability to provide isolation while converting the MCU's digital CAN signals (TXD and RXD) into differential CAN bus signals (CANH and CANL). It ensures safe, high-speed communication in noisy environments and protects the MCU from high-voltage surges or ground loops.

ISOW1044BDFMR is the transceiver itself. It provides galvanic isolation and converts the digital signals from the MCU to differential CAN bus signals. This IC offers up to 70V bus fault protection and operates at high speeds (up to 5 Mbps), making it suitable for modern automotive and industrial applications.

2.4.2 Ferrite Beads

The ISOW1044BDFMR transceiver is selected for its integrated signal and power isolation, providing a streamlined and robust solution for high-speed CAN communication in electrically noisy environments. To ensure the stability and integrity of the power supply feeding the transceiver, BLM21HE601SN1L ferrite beads are incorporated into the power path. These components are specifically designed to suppress high-frequency noise, effectively blocking unwanted EMI from reaching sensitive sections of the circuit. By doing so, they help maintain a

clean power rail, which is essential for reliable operation of isolated communication interfaces like the ISOW1044BDFMR.

2.4.3 Common-Mode Choke

To suppress noise and improve EMI performance, the differential CANH and CANL lines from the transceiver pass through a **common-mode choke**, specifically the **1812CAN-113HRC**. This component filters common-mode noise that could otherwise affect data integrity or radiate from the board. It ensures that only the differential signal propagates while attenuating unwanted interference.

2.4.4 TVS Diodes

After the choke, the CANH and CANL lines are protected by TVS diodes, part number **SZNUP3105LT3G**. These diodes are bidirectional and provide clamping protection against voltage spikes due to ESD or other transients that could damage the transceiver or disrupt communication. They are connected from CANH and CANL to GND_CAN, offering direct transient suppression to ground.

NOTE: SPI Interface

The schematic uses the SPI1 interface of the MCU(STM32G474RET3) to communicate with the ATM90E32AS-AU-Y which is the energy measurement IC. The connections include:

PA4 → SPI1_CS (Chip Select).

PA5 → SPI1_CLK (Clock).

PA6 → SPI1_MISO (Master In Slave Out).

PA7 → SPI1_MOSI (Master Out Slave In).

In the schematic, certain capacitors such as C63 are strategically placed on communication lines to enhance signal quality. These capacitors help to filter out high-frequency noise, suppress transient disturbances, and stabilize the signal being transmitted or received. This is particularly important in high-speed interfaces like SPI, where noise or ringing can lead to data corruption. By improving signal integrity, these capacitors contribute to reliable and noise-free communication between the microcontroller and peripheral devices.

2.5 Measurement

A dedicated measurement system is implemented to monitor the main electrical quantities of the three-phase network, including voltage, current, and different forms of power. The acquired data supports system supervision, diagnostic functions, and efficient energy management.

2.5.1 Measurement IC:

The **ATM90E32AS-AU-Y** is a high-precision energy measurement IC designed specifically for polyphase power monitoring systems. It is capable of measuring various critical electrical parameters such as instantaneous and RMS voltage and current, active power (P), reactive power (Q), apparent power (S), frequency, and power factor (PF). The IC also supports harmonic distortion analysis, allowing it to monitor the quality of the power signal. It achieves a typical accuracy of ±0.1% over a wide dynamic range, making it suitable for industrial and commercial applications that require reliable and detailed energy monitoring.
The IC supports six analog inputs—three voltage inputs (AV1, AV2, AV3) and three current inputs (AI1, AI2, AI3)—and processes signals using a high-resolution delta-sigma ADC. These measurements are managed internally by a dedicated digital computation engine that handles signal processing, phase calibration, and power calculations. Communication with a host microcontroller, such as the STM32G474RET3, is achieved through an SPI interface, offering flexibility and robustness in system integration. Additionally, the ATM90E32AS-AU-Y includes on-chip memory for storing calibration coefficients and configuration data, enabling reliable standalone operation in many cases.

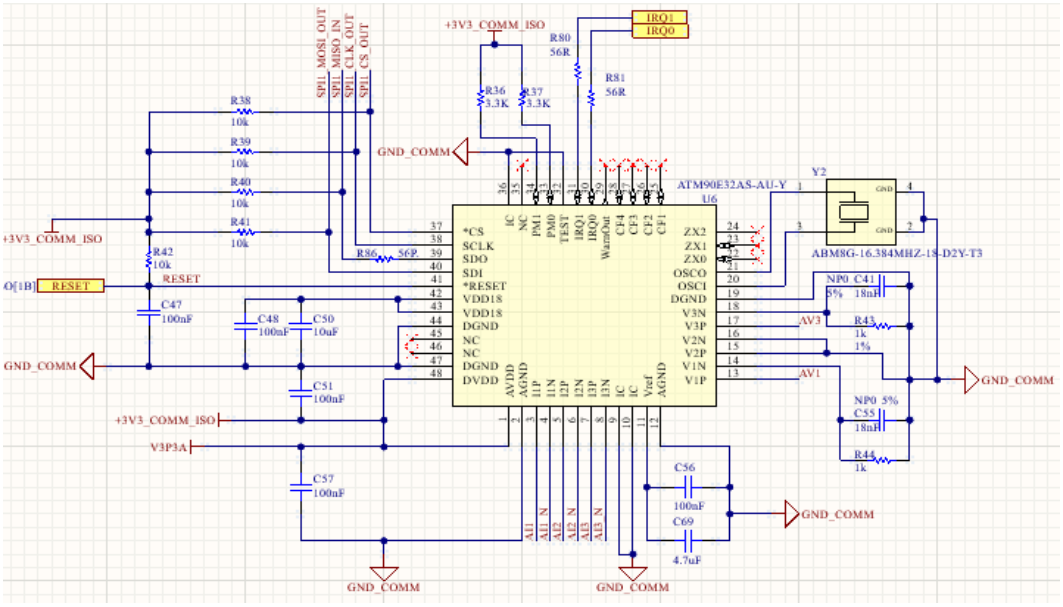

Figure 11: Measurement IC

2.5.1.1 Isolated Interrupt and Reset Interface

The IRQ0 and IRQ1 signals are interrupt outputs from the ATM90E32AS measurement IC. They are used to notify the microcontroller (MCU) when specific events occur within the energy metering system, such as abnormal voltage or current conditions, or status updates related to measurement processes. In detection mode, these pins can also indicate the output state of the current detection logic. Their purpose is to enable the MCU to respond quickly to critical changes or events in the power system without constantly polling the IC.
To ensure galvanic isolation between the high-voltage measurement domain and the low-voltage MCU domain, the signals IRQ0, IRQ1, and RESET are passed through a digital isolator, the ISO7731FBDW. This isolator transmits digital signals across an isolation barrier using capacitive coupling, protecting the MCU from electrical noise or surges from the measurement circuitry. On the input (high-voltage) side of the isolator, IRQ0 and IRQ1 are routed through 56 Ω resistors to reduce signal reflections and suppress transient currents, while a 100 nF capacitor stabilizes the local 3.3 V_COM_ISO power rail. The RESET signal is also connected here, allowing the MCU to remotely reset the measurement IC. On the output (MCU) side of the isolator, the corresponding signals IRQ0_OUT, IRQ1_OUT, and RESET_OUT connect directly to the MCU's interrupt and reset pins. Each line includes a 33pF capacitor to ground for EMI filtering, along with placeholders for optional N.M. (Not Mounted) capacitors to allow tuning of the

filtering behavior if needed. A separate 3.3 V supply powers this side of the isolator, with its own 100 nF decoupling capacitor for clean operation. This subsystem ensures safe, noise-immune, and electrically isolated communication between the measurement IC and the MCU.

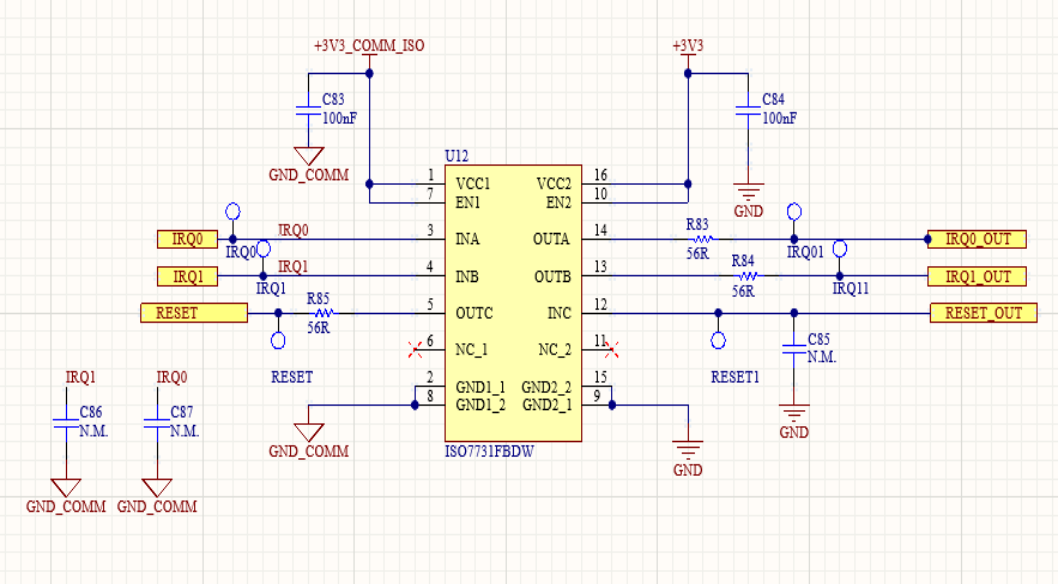

Figure 12 : Isolated Interrupt and Reset

2.5.2 Power Supply:

The **ATM90E32AS-AU-Y** requires a stable 3.3V supply for its analog and digital circuitry. To ensure measurement accuracy and electrical protection, the IC is powered through an isolated voltage rail, named +3V3_COMM_ISO. Isolation prevents ground loops, reduces noise coupling, and protects sensitive circuits from disturbances on the primary system ground.

The power supply architecture starts with a 24V DC input, commonly available in industrial environments. First, a DC/DC isolated converter **(TMR 9-2423)** generates isolated ±15V rails (±15V_COMM_ISO). Isolation at this stage ensures a complete galvanic separation between the main system power and the measurement/control sections.

From the +15V_COMM_ISO rail, a buck converter **(LMR50410YQDBVRQ1)** steps the voltage down efficiently to +5V_COMM_ISO. This intermediate step is necessary because directly converting from 15V to 3.3V using an LDO regulator would result in significant heat dissipation and reduced efficiency.

Finally, the +5V_COMM_ISO rail feeds into a Low-Dropout Regulator **(NCP1117ST33T3G)** to precisely generate the stable +3V3_COMM_ISO voltage required by the **ATM90E32AS-AU-Y**. Using an LDO in this final step ensures clean and low-noise supply voltage, which is critical for the high-precision analog measurements handled by the IC.

Thus, the three-stage approach — isolated DC/DC, buck converter, and LDO balances isolation, efficiency, and voltage accuracy to ensure robust and reliable power for the measurement system.

To monitor the correct operation of the power supplies, four LEDs are included in the design. each indicating the presence of the ±15V_COMM_ISO, +5V_COMM_ISO and +3.3V_COMM_ISO rail. These visual indicators provide a quick and reliable way to verify that all necessary power levels are correctly generated and active.

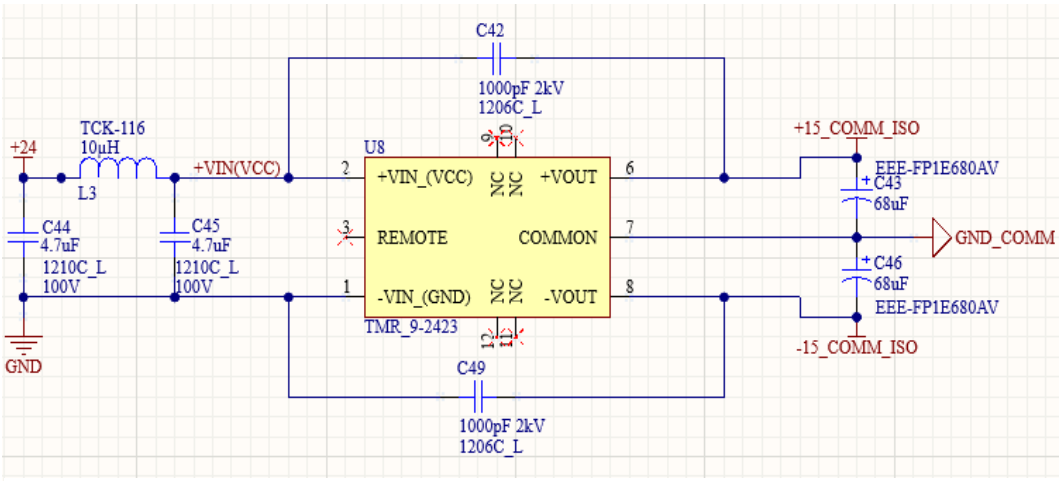

Figure 13: Dual Power Supply for Isolation +24 to ±15_COMM_ISO

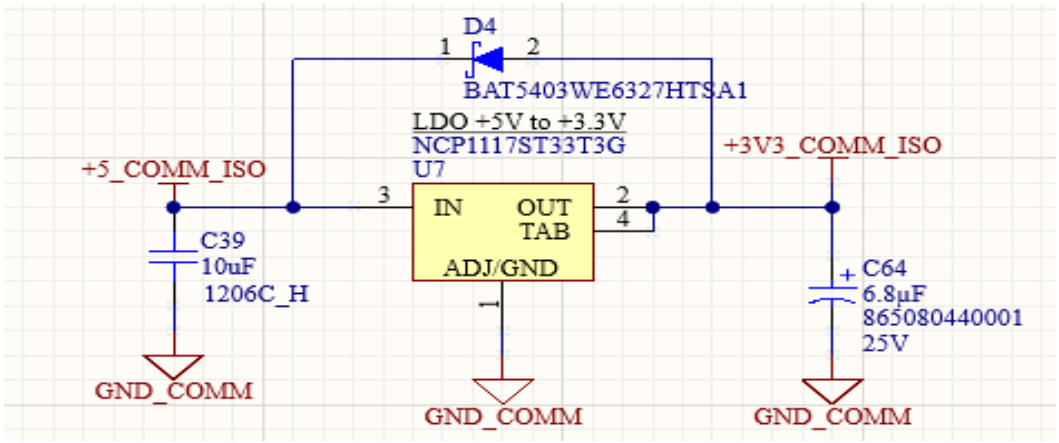

Figure 14: LDO +5_COMM_ISO to +3V3_COMM_ISO

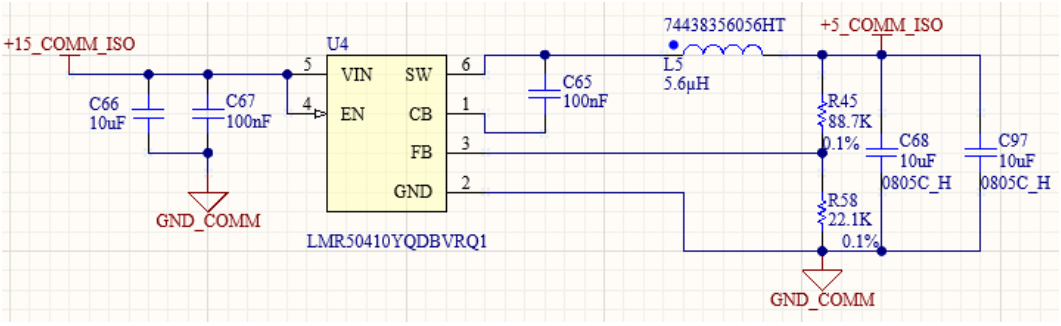

Figure 15: LDO +15_COMM_ISO to +5_COMM_ISO

2.5.3 SPI Isolation

In the design of the measurement system, the SPI interface plays a critical role in enabling communication between the microcontroller (MCU) and the measurement IC. However, because the two devices operate in separate power domains (+3V3 and +3V3_COMM_ISO), direct electrical connection could compromise system stability, introduce noise, and even pose risks to device safety. To address these concerns, galvanic isolation is implemented on the SPI lines using a digital isolator, the ISO7741DW.

The ISO7741DW is a four-channel isolator specifically suited for high-speed digital communications like SPI. It provides complete electrical isolation between its input and output sides, protecting the MCU and measurement IC from electrical noise, voltage transients, and ground potential differences. By isolating the MISO (Master-In-Slave-Out), MOSI (Master-Out-Slave-In), CLK (Clock), and

CS (Chip Select) signals, the system maintains high data integrity and ensures safe operation even in noisy industrial environments. The isolator is powered by two independent supplies: the MCU side is powered by the +3V3 rail, and the measurement side by the isolated +3V3_COMM_ISO rail. Their corresponding grounds (GND and GND_COMM) are also kept completely separate. This architecture not only preserves signal quality but also allows the measurement IC to operate within its own isolated domain, essential for accurate and interference-free power measurements.

The SPI lines are routed as follows through the isolator:

- **SPI1_MISO (input)** is isolated and forwarded as **SPI1_MISO_IN**.
- **SPI1_MOSI (output)** is isolated and received as **SPI1_MOSI_OUT**.
- **SPI1_CLK (output)** is isolated and received as **SPI1_CLK_OUT**.

- **SPI1_CS (output)** is isolated and received as **SPI1_CS_OUT**.

To ensure clean and stable operation, decoupling capacitors (**C52** and **C53**, each 100nF) are placed close to the isolator's supply pins. These capacitors minimize power supply noise and improve transient response.

Additionally, flexibility for noise mitigation is built into the design: non-mounted (N.M.) capacitors (**C59**, **C60**, **C61**, **C62**) are reserved on the isolated SPI lines. These can be populated later if signal distortion or EMI (electromagnetic interference) issues arise during testing. Similarly, non-mounted capacitors (**C33**, **C34**, and **C35**) are positioned near the SPI pins of the measurement IC itself, offering a secondary option to stabilize signals if necessary. This isolation strategy ensures robust communication, high system reliability, and protection of sensitive components, all of which are crucial for achieving high-precision measurement performance.

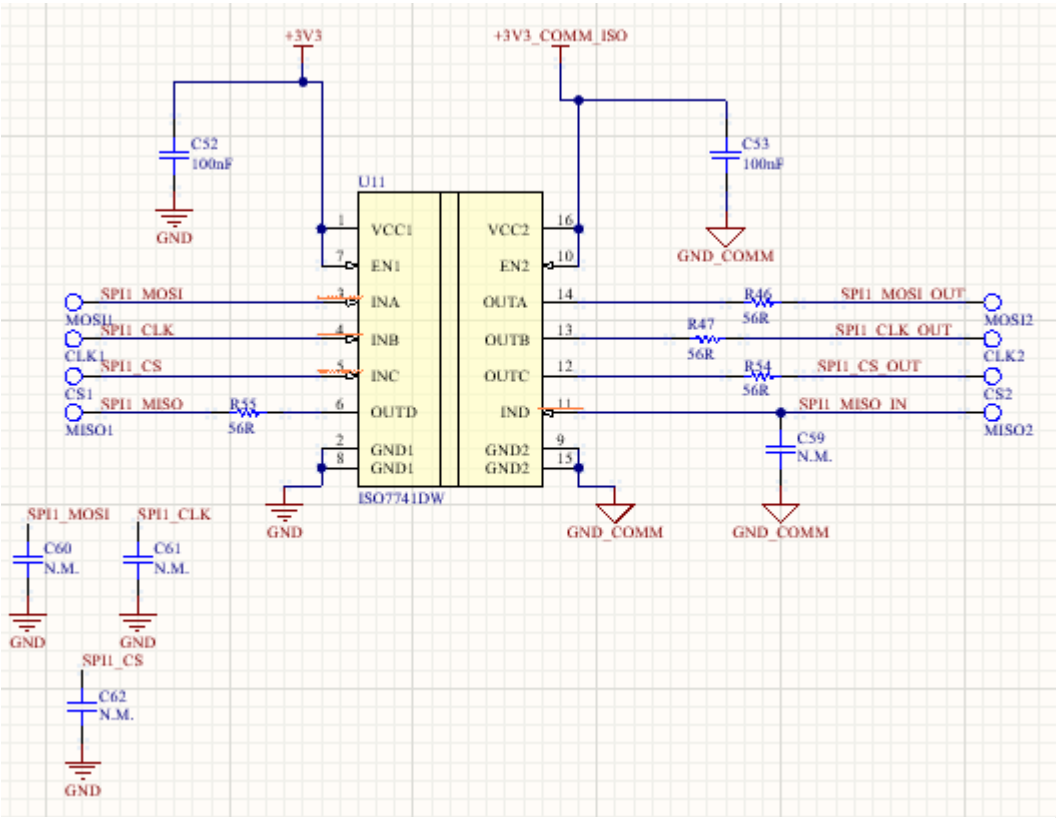

Figure 16: SPI Isolation

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2.5.4 Current Sensor

The **ATM90E32AS-AU-Y** measurement IC relies on the **LA55-P Hall-effect current sensor** to accurately monitor current in a three-phase system. This sensor delivers a voltage output proportional to the primary current while ensuring galvanic isolation between the high-voltage primary side and the low-voltage measurement circuitry — a key safety and accuracy requirement in power systems.

The **LA55-P** is selected for its high accuracy, ability to measure both AC and DC currents, and its rugged, industrial-grade design. In this application, it is configured with the following parameters:

- **Primary nominal current (Ipn)**: 50A RMS
- **Secondary nominal current (Isn)**: 50 mA RMS
- **Turns ratio (Np/Ns)**: 1:1000
- **Supply voltage**: ±15V (derived from the **TMR_9-2423** isolated DC-DC converter, which provides ±15V_COMM_ISO)

The sensor's output current is passed through a **measuring resistor** to generate a proportional voltage. According to the datasheet, for ±15V operation, a burden resistor in the range of 50–160 **Ω** is recommended. Based on performance trade-offs and standard values, a resistor of **82 Ω** (E12 series) is chosen. The resulting peak output voltage is approximately:

$$V_{out\ of\ \ current\ sensor} = 82\ \Omega \times 50 \times \sqrt{2} = 5.8V$$

Since the analog input range of the ATM90E32AS-AU-Y is **720 mV RMS** (on pins AI1, AI2, AI3), this sensor output must be attenuated and conditioned appropriately. To achieve this, a fully differential signal conditioning circuit is implemented using the **AD8138ARZ-R7** operational amplifier.

This amplifier not only provides signal scaling but also converts the single-ended sensor output into a differential signal compatible with the IC's analog inputs. The gain of the circuit is defined by:

$$\frac{V_{in\ of\ Measurement\ IC}}{V_{out\ of\ current\ sensor}} = \frac{720mV \times \sqrt{2}}{5.8V} \cong 0.176$$

The signal conditioning circuit utilizes a **AD8138** op-amp with a gain determined by the ratio of the feedback resistor to the input resistor. The gain is calculated as:

$$Gain = 2 \times \frac{R_{feedback}}{R_{input}}$$

Where R_f is the feedback resistor and R_{in} is the input resistor. The factor of 2 accounts for the fully differential configuration of the **AD8138**, which enables symmetrical drive on both output lines and improves noise immunity. By selecting R_f=12kΩ and R_{in}=164kΩ, both from the E12 series, a gain close to the target value of 0.176 is achieved.

$$Gain = 2 \times \frac{12K}{164K} = 0.1463$$

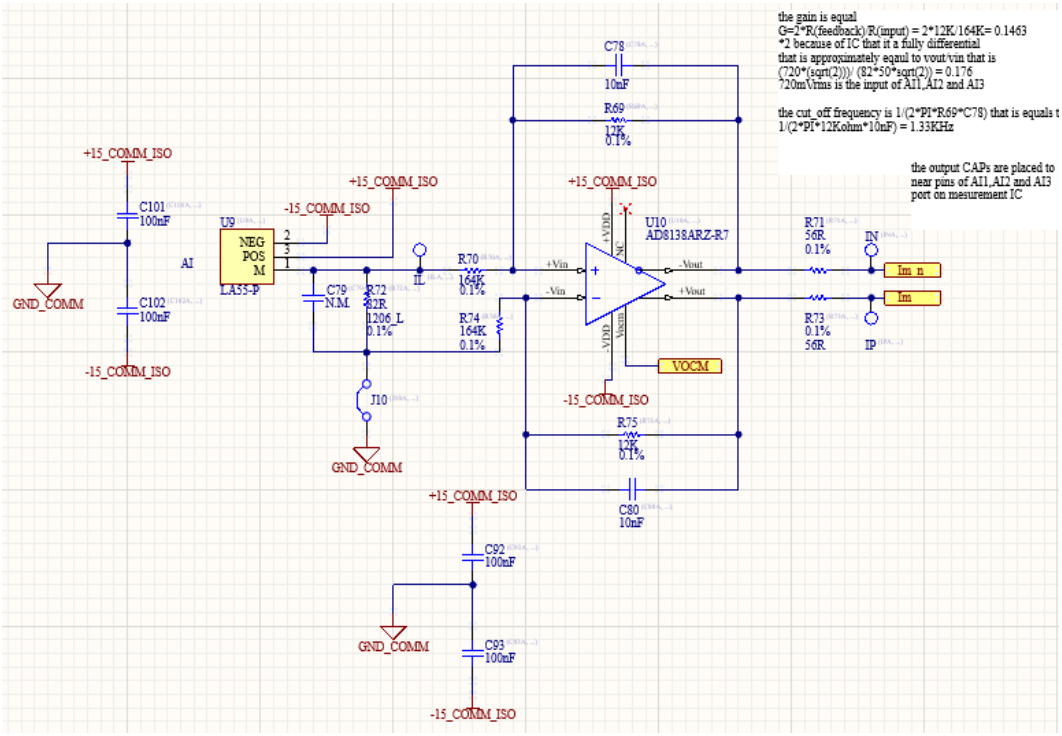

Figure 17: Current Sensor Circuit

2.5.4.1 Common-Mode Voltage Reference for Differential Driver

This circuit implements a buffered reference stage designed to provide a stable common-mode voltage for the differential output stage of the current sensing system. Its primary function is to drive the VOCM pin of the AD8138 differential amplifier, which controls the common-mode level of the amplifier's differential outputs. A precise reference voltage of 1.65 V is generated through a resistor divider consisting of two matched 10 kΩ resistors (R90 and R91) connected across a 3.3 V

supply. This midpoint voltage is then decoupled with a capacitor (C95) to suppress any noise or ripple and subsequently buffered by a low-offset, rail-to-rail **OPA365 operational amplifier** configured as a voltage follower. The buffer ensures a low output impedance, which is crucial for maintaining the stability and accuracy of the common-mode voltage, particularly when driving capacitive loads or multiple input nodes elsewhere on the PCB. Supplying a clean and constant VOCM voltage guarantees that the positive and negative outputs of the AD8138 swing symmetrically around this reference, enhancing signal integrity, ensuring compatibility with downstream ADCs or differential receivers, and minimizing susceptibility to common-mode noise.

$$VOCM = \frac{R_{91}}{R_{91} + R_{90}} \times 3.3V$$

$$VOCM = \frac{10K}{10K + 10K} \times 3.3V = 1.65V$$

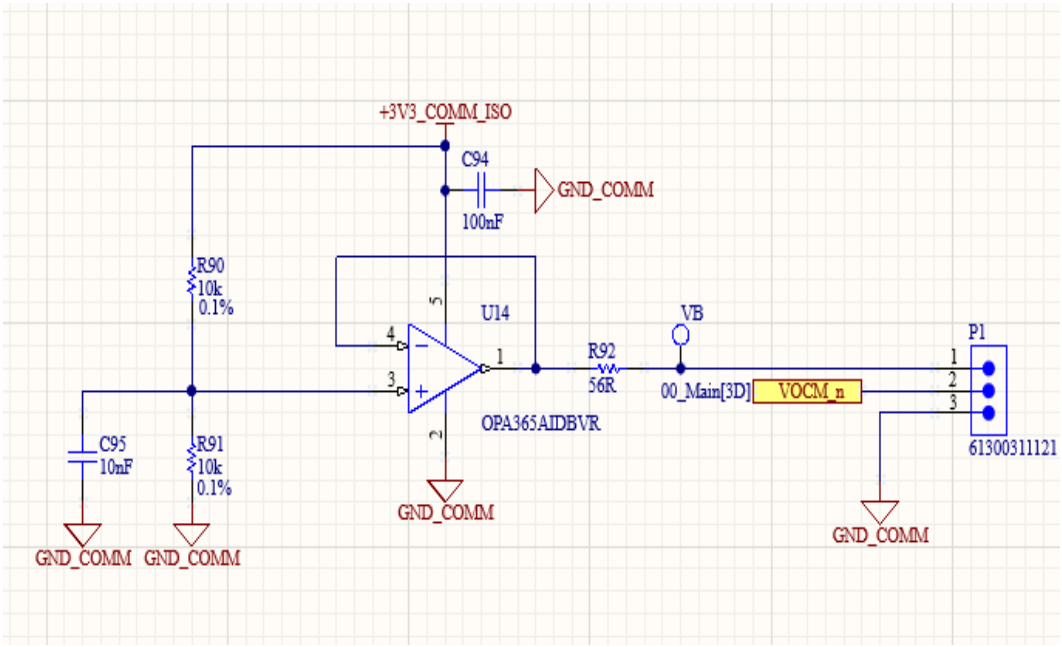

Figure 19 : Common-Mode Voltage Reference Circuit

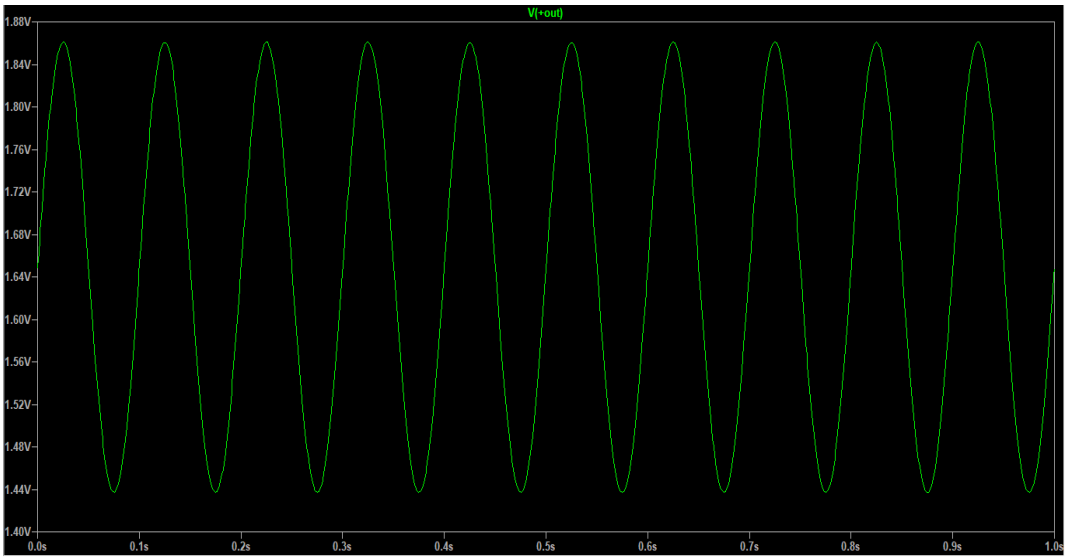

Figure 18 : +OUT output

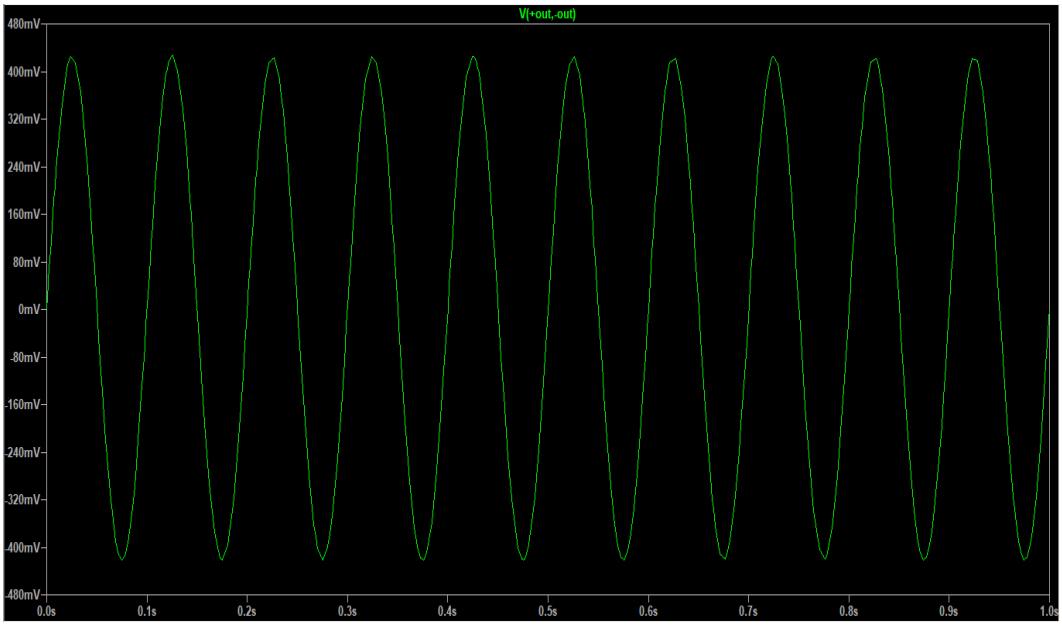

Figure 20: Differential output

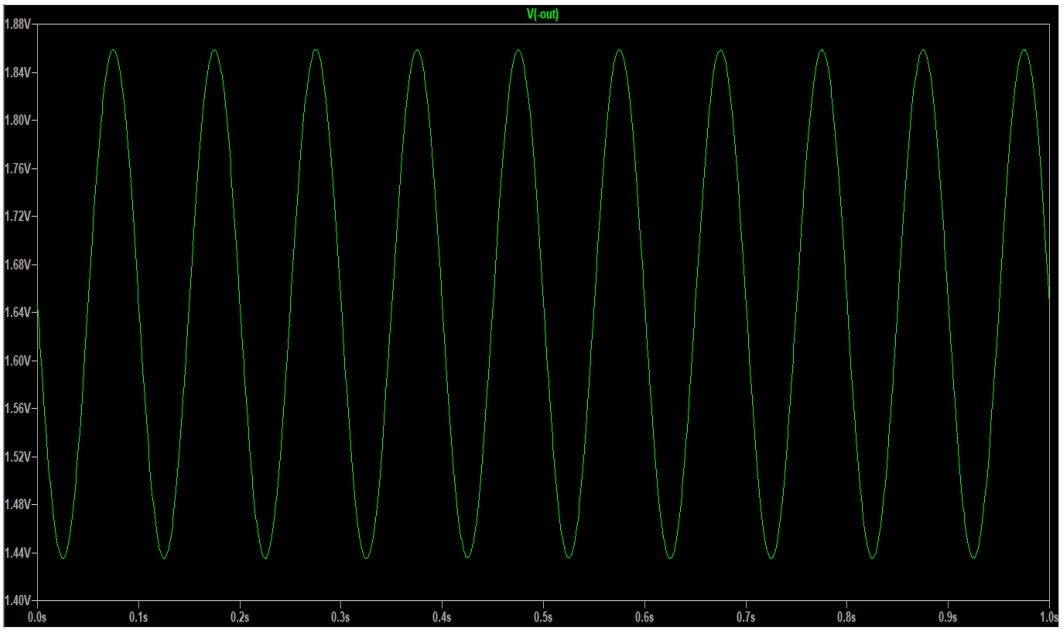

Figure 21: -OUT output

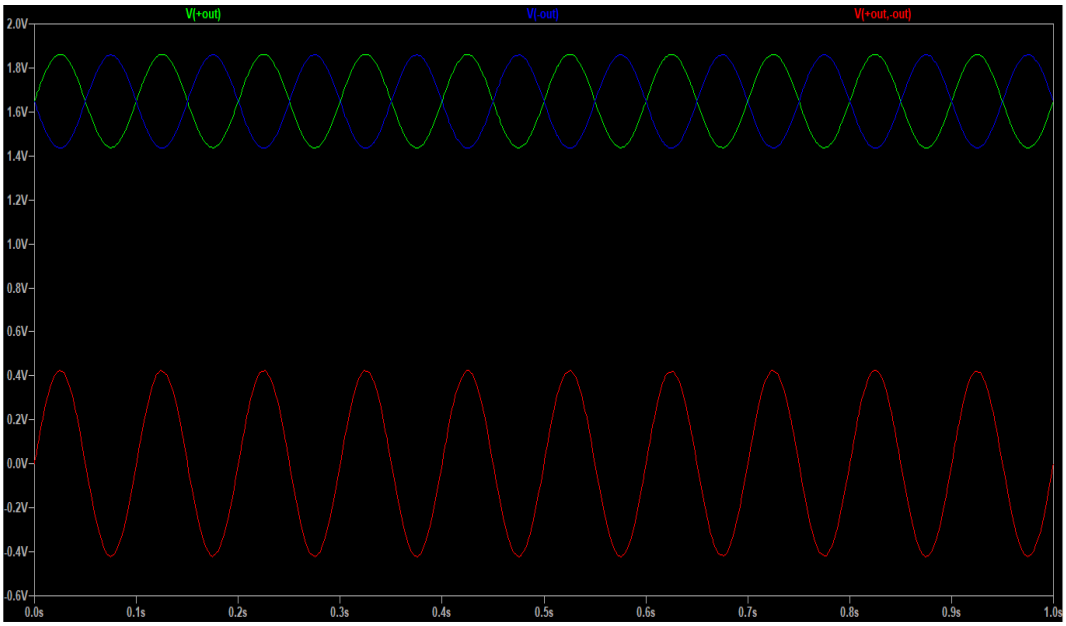

Figure 22: All outputs

Additionally, a filter is incorporated into the circuit to suppress high-frequency noise. The cutoff frequency of the filter is calculated as:

$$f_c = \frac{1}{2 \times \pi \times C_{78} \times R_{69}} = \frac{1}{2 \times \pi \times 10nF \times 12k\Omega} = 1.33KHz$$

To ensure clean signal delivery to the ATM90E32AS-AU-Y, a secondary filter is placed at the output nodes. This filter comprises a 56 Ω resistor and a 1nF capacitor and is located near the AI1, AI2, and AI3 input pins of the measurement IC. These components reduce noise and stabilize the signal further.

This entire signal conditioning circuit is repeated three times, once for each phase, to handle the outputs from the three LA55-P current sensors. Each sensor's output is conditioned and fed to the corresponding current input pins (AI1, AI2, AI3) of the ATM90E32AS-AU-Y.

2.5.5 Voltage Sensor

This circuit is a voltage divider and filtering network used for safely sensing high-voltage three-phase AC signals (VA, VB, VC) and conditioning them for input into the ATM90E32AS energy metering IC. The three-phase voltages are supplied to the system through a 1766466 connector, which brings in the line voltages from an external source.

Since typical line voltages (e.g., 230 V RMS) are far too high to be directly connected to the ADC inputs of the ATM90E32, the voltages must be scaled down to a safe and measurable range, typically around a few volts peak-to-peak. This is accomplished by a precision voltage divider, which consists of multiple high-value resistors in series—such as R61 to R67 for phase C. These resistors are selected with 0.1% tolerance to maintain accuracy and minimize error.

To further condition the signal, a **low-pass filter** is formed using R60 and capacitor C76. This helps eliminate high-frequency noise or transients that could interfere with accurate voltage measurement. The filtered, scaled voltage is then fed into the appropriate analog voltage input (e.g., AV1) of the ATM90E32 for real-time voltage monitoring and energy calculation.

In the case of the **ATM90E32AS**, the IC uses **differential voltage sensing**. This means that each voltage channel measures the **difference between two inputs**, rather than referencing all signals to a common ground. Because of this, not all three phase voltages need to be measured individually relative to ground. Instead, one of the three phases (typically **VB**) is treated as a **virtual ground or reference**, and the IC measures the voltage **differences** between AV1 and AV2 or AV2 and AV3.

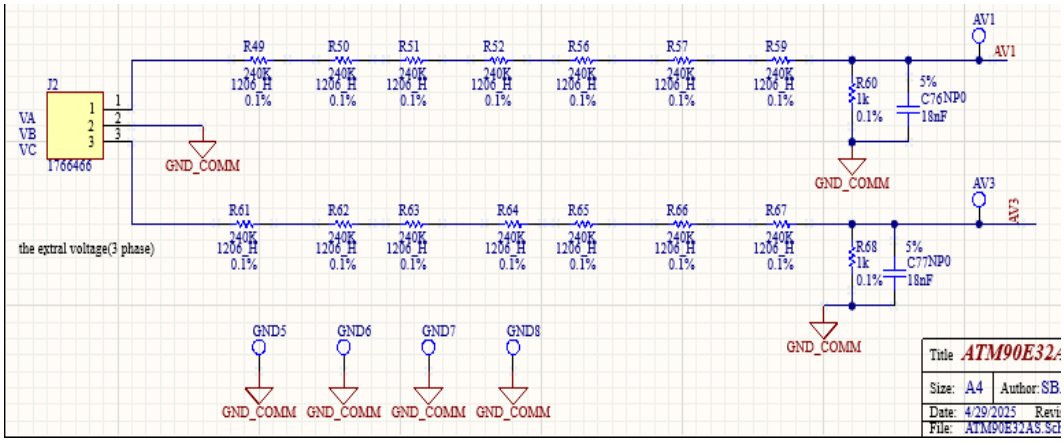

Figure 23: Voltage Sensor

Chapter 3

3. PCB

Printed Circuit Boards (PCBs) serve as the physical foundation of most electronic systems, providing both mechanical support and electrical connectivity between electronic components. The decision to use a multilayer PCB, especially in more complex systems, is essential for improving signal integrity, managing power distribution, and reducing electromagnetic interference (EMI).

In our project, we opted for a 4-layer PCB structure, which offers a balanced trade-off between complexity, cost, and performance. A multilayer PCB allows for better separation of signal and power planes, leading to improved noise immunity, ground stability, and routing efficiency. Ground and power planes reduce impedance, minimize voltage drops, and act as shields for sensitive signals.

The PCB layout was developed using Altium Designer, a professional-grade CAD tool, which enabled high precision in trace routing, via placement, and layer stack management. The size of the board, 18 × 12 cm, was selected to provide enough space for all components while keeping the board compact and organized.

Efficient PCB design also involves attention to component placement, trace width, via design, and return current paths—especially for high-speed communication lines like SPI and CAN. Care was taken to place decoupling capacitors close to IC power pins and to route sensitive signals away from noisy power lines.

The PCB for this project is structured as follows:

1- **Top Layer (Red):** This is the primary component layer where all surface-mount devices (SMDs) and connectors are placed. Signal traces on this layer interconnect the various ICs, microcontroller (STM32G474RET3), power regulators, and communication interfaces and so on. Careful routing ensures minimal crosstalk and optimal signal paths.

2- **Mid Layer 1 (Brown- Ground Plane):** Dedicated entirely as the ground plane. This solid ground layer helps reduce electrical noise and provides a stable reference for all signals. It also improves the return current path for high-frequency signals, thus enhancing the overall signal integrity of the system.

It serves multiple grounding purposes:

- **Digital Ground (GND):** For all logic and digital circuitry.
- **Analog Ground (AGND):** For analog-sensitive components like the energy measurement IC, carefully separated and then connected at a single-point reference (star grounding method).
- **Isolation Ground:** To handle isolated domains, such as the CAN transceiver section, SPI isolation, which operates across an isolation barrier. These grounds are locally grouped and separated by the digital isolator and only connected at appropriate points via controlled impedance paths or dedicated components (e.g., ferrite beads or opto-isolators).

This multilayer grounding scheme reduces ground bounce, noise coupling, and improves the performance of mixed-signal sections.

3- **Mid Layer 2 (Cyan- Power Plane):** This layer is dedicated to distributing all essential power rails, ensuring efficient and low-impedance power delivery across the board. It includes standard system voltages such as 24 V (input), 15 V, 5 V, and 3.3 V, all derived from a combination of buck converters and LDO regulators based on the requirements of different circuit sections.

   Additionally, this layer is used to route isolated power supplies, such as ±15 V_COMM_ISO and +5 V_COMM_ISO, 3V3_COMM_ISO which are essential for powering components on the isolated side of the circuit—particularly those associated with communication interfaces and SPI drivers that require galvanic isolation. These isolated rails are generated using dedicated DC-DC converters and carefully routed to maintain signal integrity and isolation barriers, ensuring noise immunity and safe communication across domains.

   This multilayer power distribution approach reduces routing congestion, improves thermal performance, and plays a critical role in maintaining the robustness and reliability of both the logic and isolated communication sections of the board.

4- **Bottom Layer (Blue):** This layer does not carry any components and is used primarily for additional routing of signal traces that could not be optimally placed on the top layer. It helps reduce congestion on the top layer and simplifies routing of complex interconnections.

This layered structure was essential to support the needs of the project, which includes power supply management, SPI communication with the measurement IC, CAN bus communication, and support for auxiliary components such as DIP switches, debug headers, and relays. Each layer was defined and managed to reduce EMI, maintain signal integrity, and ensure robust electrical performance across the board.

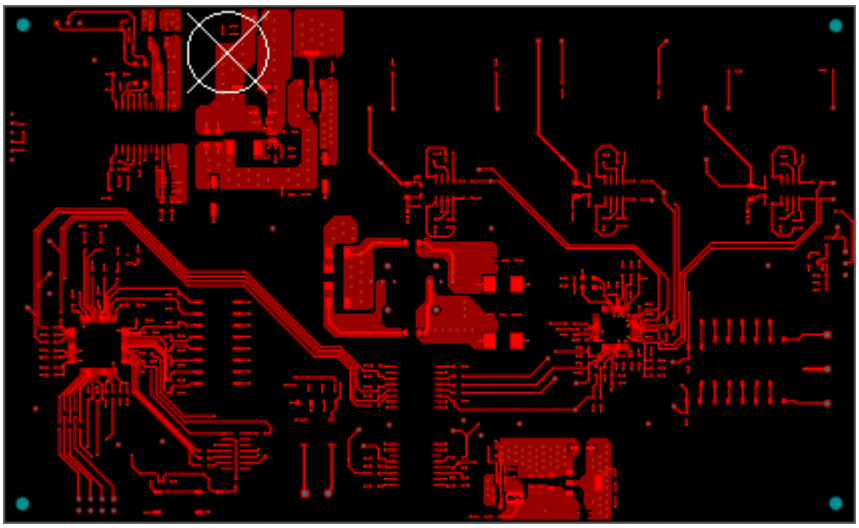

Figure 25: 2D top layer

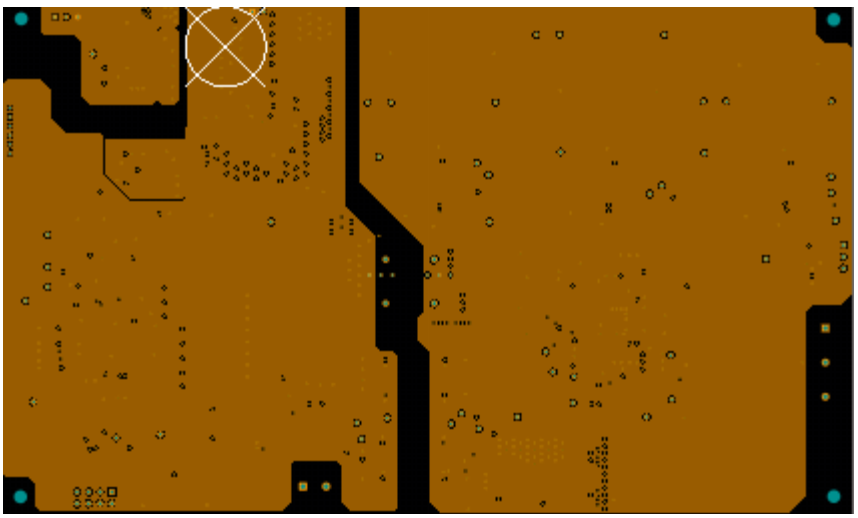

Figure 24: 2D mid_layer1

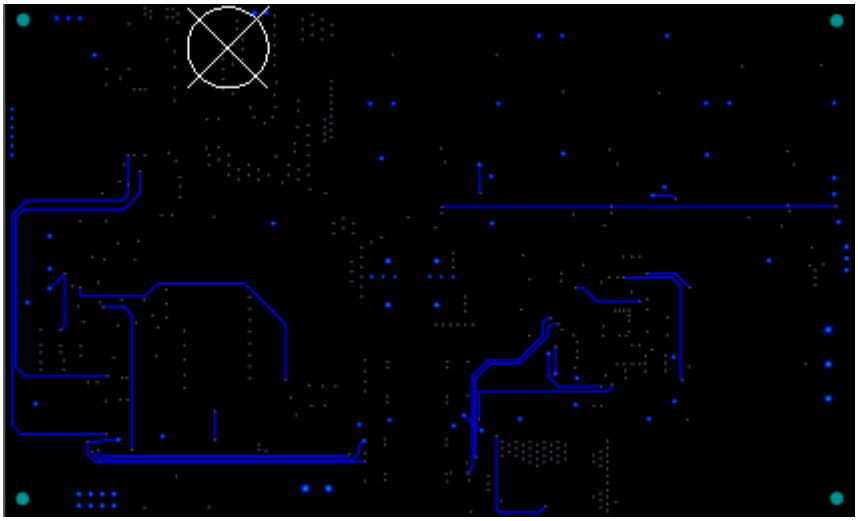

Figure 26: 2D bottom layer

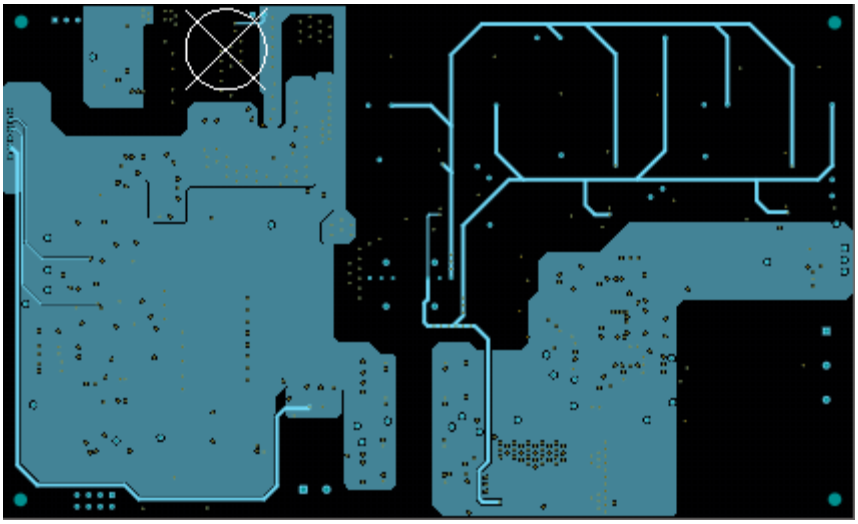

Figure 27: 2D mid_layer2

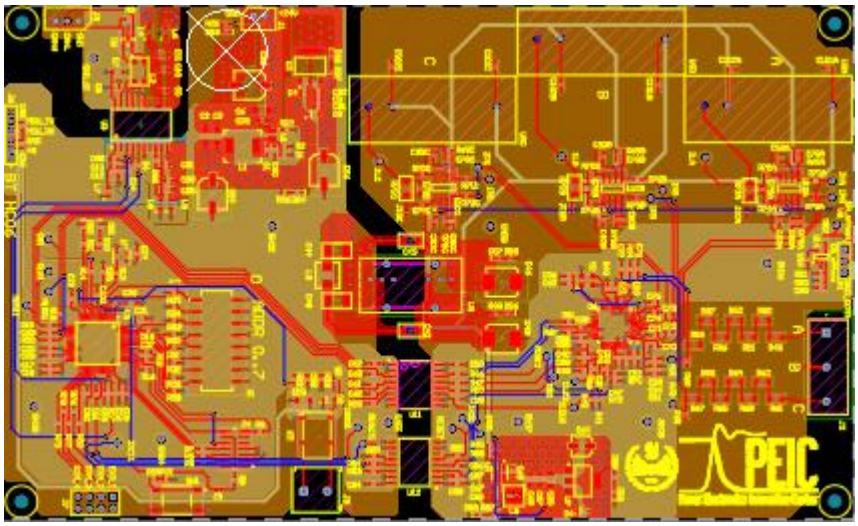

Figure 28: 2D PCB

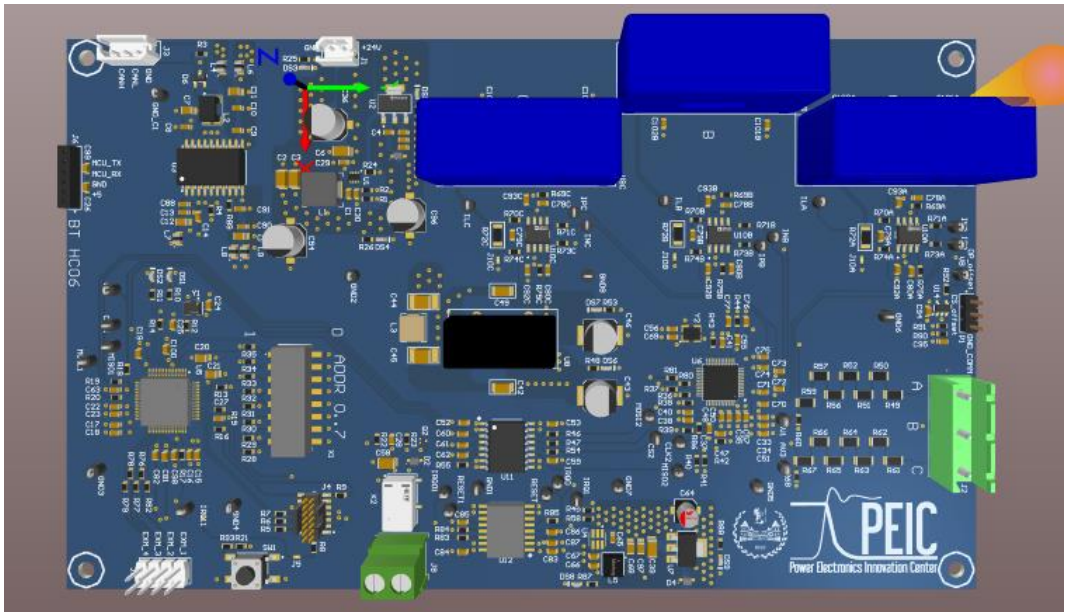

Figure 29: 3D PCB

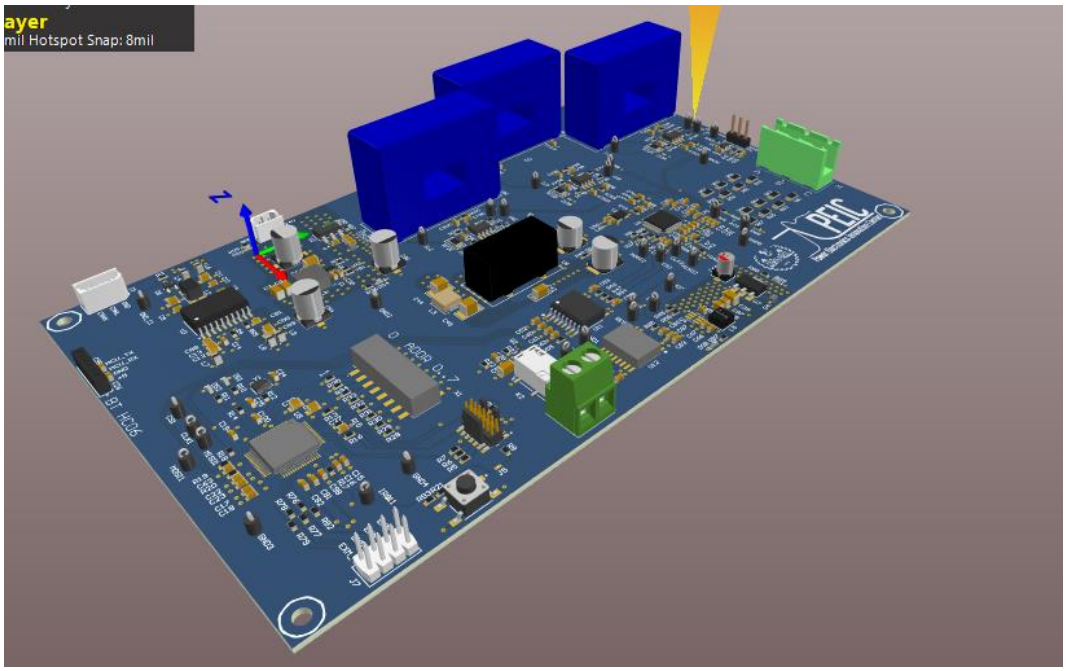

Figure 30: 3D PCB (2)

The following step provides a detailed explanation of each part of the PCB design.

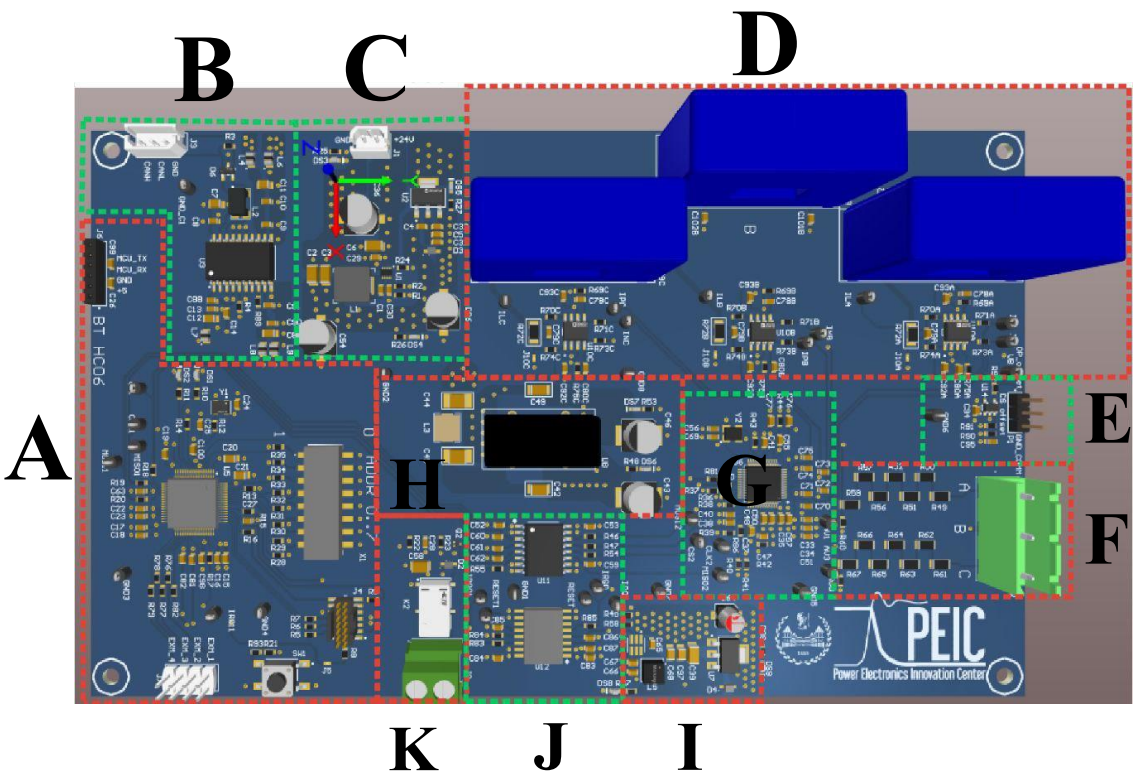

Figure 31: Different parts of PCB

3.1 Micro Control Unit

The section “A” of the PCB hosts the **STM32G474RE microcontroller**, which functions as the central processing and control unit of the entire system. The PCB layout in this area was carefully designed to ensure signal integrity and efficient routing of the peripheral interfaces, including **SPI**, **CAN**, **RELAY control**, and various **communication and debug headers**.

Special attention was given to trace width and length matching for high-speed signals such as SPI and the SWD debugging interface, minimizing noise and ensuring reliable data transfer. Decoupling capacitors are placed close to the MCU’s power supply pins to maintain voltage stability and suppress high-frequency noise.

Additionally, this section includes indicator LEDs for status feedback and an 8-position DIP switch that allows for manual configuration of a unique board address.

For a detailed overview of the MCU circuit and connections, refer to the schematic section in Chapter 2. (MCU Page 18).

3.2 CAN interface

The CAN interface “**B**” section hosts the ISOW1044 isolated transceiver and associated components, carefully placed to ensure compact routing and optimal signal integrity. Differential CANH and CANL traces are routed as tightly coupled pairs with controlled impedance to minimize noise and maintain signal fidelity. A common-mode choke is placed directly in-line with the differential pair to suppress EMI, while TVS diodes are positioned close to the connector for effective transient protection.

Power integrity is reinforced with BLM21HE601SN1L ferrite beads, placed near the transceiver’s VCC pins to filter high-frequency noise. Decoupling capacitors are placed adjacent to the transceiver for stable operation. The isolated ground (GND_CAN) and logic ground are clearly separated with appropriate clearance, ensuring robust isolation. Trace widths and spacing comply with high-speed layout practices to support reliable operation.

For detailed schematic and electrical design of the CAN interface, refer to Chapter 2. (CAN interface page 24)

3.3 Power Supply

The power supply "**C**" section is laid out to support high current handling, thermal management, and low-noise operation. It includes the buck converter (TPS62933DRLR) and LDO (MIC39100-3.3WS), along with their passive components, placed to minimize loop areas and optimize heat dissipation.

To handle higher currents and reduce voltage drop, thick traces are used on the top layer, especially along the 24V, 5V, and 3.3V power lines. Numerous vias are strategically placed to interconnect layers and distribute current efficiently between the top and bottom copper planes. This via stitching also aids in thermal relief and minimizes impedance in critical paths.

The placement of input/output capacitors is kept as close as possible to the regulators to minimize parasitic inductance and ensure stable voltage regulation. Power LEDs (DS3, DS4, DS5) are positioned for clear visual indication, with their current-limiting resistors nearby to simplify routing.

Clear separation is maintained between analog, digital, and isolated power domains to avoid noise coupling, and copper pours are used for ground planes to ensure low impedance returns and better EMI performance.

For detailed schematic and electrical design of the Power Supply, refer to Chapter 2. (Power Supply page 14).

3.4 Current Sensor

The PCB layout of the current sensing stage "**D**" section is designed with an emphasis on signal integrity, isolation, and noise immunity. It includes the LA55-P Hall-effect current sensor, the burden resistor, and the AD8138-based signal conditioning circuit.

To support the sensor's galvanic isolation function, careful attention is given to the separation between the high-voltage and low-voltage domains. Wide spacing and cutouts are used in the PCB to ensure creepage and clearance distances are maintained, in line with safety standards.

The output of the LA55-P, which is a current signal, is routed to the burden resistor with short and direct traces to minimize noise pickup. The burden resistor is placed very close to the sensor output to ensure accurate voltage conversion with minimal parasitic inductance.

The AD8138 op-amp and its passive components are laid out in a fully differential configuration, with symmetrical and balanced routing of the differential signal lines to the measurement IC (ATM90E32AS-AU-Y). This helps minimize common-mode noise and ensures precise current measurement. Feedback and input resistors are placed symmetrically around the op-amp to maintain balanced gain paths and reduce layout-induced mismatch.

A solid ground plane is placed underneath the signal conditioning circuit to provide a low-impedance return path and enhance EMI performance. Decoupling capacitors for the AD8138 are placed close to its power pins, minimizing supply noise.

For detailed schematic and electrical design of the Current sensor, refer to Chapter 2. (Current sensor page 33).

3.4 Common-Mode Voltage Reference

The "**E**" section of the PCB implements a precision common-mode voltage reference circuit required for the differential driver stage of the current sensing signal chain. The layout of Section **E** is carefully designed to ensure low-noise operation, excellent voltage stability, and minimal impedance from source to load all essential for driving the VOCM input of the **AD8138ARZ-R7** differential amplifier (the current sensor's circuit).

The reference voltage is created by a resistive divider (R90 and R91), connected between a regulated 3.3 V supply and ground. These resistors are placed in close proximity and symmetrically on the PCB to reduce mismatch due to trace resistance or parasitic coupling. The midpoint of the divider produces the desired 1.65 V reference voltage, which is then decoupled using capacitor C95 (positioned directly at the midpoint node) to suppress noise and ensure DC stability.

To achieve a low output impedance and preserve the voltage accuracy when driving the VOCM input of multiple AD8138 amplifiers, the reference node is buffered using a rail-to-rail OPA365 op-amp (U17) configured as a unity-gain voltage follower. The layout positions U17 directly adjacent to the divider network to minimize trace length between the resistors and op-amp input. The decoupling capacitor for the OPA365 power supply is placed close to its +3V3_COMM_ISO and GND pins to ensure stable supply conditions.

The buffered output from the OPA365 is routed to the VOCM pins of each of the three AD8138 amplifiers. This trace is trying to kept short, wide, and isolated from noisy signals, and it runs over a continuous analog ground plane to minimize impedance and noise pickup. By establishing a clean, constant common-mode

reference of 1.65 V, Section E guarantees that the differential outputs of the AD8138 amplifiers swing symmetrically around this midpoint. This results in improved signal integrity, reduced common-mode distortion, and optimal performance of the downstream ATM90E32AS-AU-Y measurement IC. The circuit is shared across all three signal conditioning paths to provide a unified common-mode voltage reference.

For detailed schematic and electrical design of the, refer to Common-Mode Voltage Reference Circuit Chapter 2. (Common-Mode Voltage Reference Circuit page 46).

3.4 Voltage Sensor

This section, "**F**", of the PCB implements the voltage sensing network for the three-phase AC system. The high-voltage AC signals are routed from the 1766466 (J2) connector to a chain of precision resistors configured as a voltage divider. The resistors are placed in series with adequate spacing to maintain safe creepage and clearance distances required for high-voltage traces.

After the divider, the signal passes through a low-pass filter formed by R60-C76 and R68-C77. These components are placed close together and near the ATM90E32AS input pins to minimize parasitic effects. Traces are short, symmetric, and routed over the analog ground plane to ensure signal integrity. For detailed circuit functionality, refer to Chapter 2 page 26.

3.4 Measurement Section

This section, **G**, houses the ATM90E32AS-AU-Y, the core measurement IC for voltage and current sensing. On the PCB, the IC is centrally placed to minimize the routing length to both the current (AI1–AI3) and voltage (AV1–AV3) sensing inputs, reducing signal degradation and ensuring accurate measurement.

The analog input traces for voltage and current sensing are routed with symmetry and matched lengths to preserve timing and reduce common-mode noise. Decoupling capacitors (C33, C34, C35, C37, C38, C40, and others) are placed as close as possible to the respective VDD pins, supplied by +3V3_COMM_ISO, to ensure stable power delivery and minimize high-frequency noise.

The SPI lines are routed away from noisy power or switching signals and maintain proper spacing to prevent crosstalk. Ground pours under the IC and along the analog trace paths are carefully separated to avoid noise coupling between digital and analog domains. The differential voltage and current inputs are routed with careful impedance control and minimal via transitions for signal integrity.

For functional operation and measurement principles, refer to Chapter 2 page 27 .

3.5 Dual Isolated Power Supply

This section, **H**, is responsible for generating isolated ±15V rails (±15V_COMM_ISO) from a 24V DC input, forming the foundation of the isolated power architecture used throughout the measurement and communication circuits.

Wide and thick top-layer traces are used for both input and output paths to support higher currents and minimize voltage drops. This also helps in heat dissipation and lowering parasitic inductance in fast-switching circuits.

Numerous VIA**s** are employed throughout the power section to reinforce current-carrying capacity between layers and to ensure solid return paths for power and ground. These VIAs connect top-layer traces to internal and bottom copper planes, improving thermal performance and grounding integrity—especially important in isolated power stages.

High-frequency bypass and filter capacitors (C43, C44 and C46) are placed immediately at the input and output of the DC/DC converter to suppress switching noise and enhance transient response. Clear separation between high-voltage primary (24V) and low-voltage isolated output (+15V, −15V_COMM_ISO) zones is maintained to respect safety and signal integrity.

The layout also prioritizes galvanic isolation clearance and creepage distances around the TMR_9-2423 module. This ensures that even under high voltage differences, breakdown or arcing between isolated domains is avoided.

For the functional overview and system-level context of this power conversion, refer to Chapter 2 page 29.

3.6 Isolated Power Supplies

This section finalizes the isolated power chain by generating the precise voltages required by the measurement circuitry. It consists of two critical stages: a buck converter (LMR50410YQDBVRQ1) for stepping down +15V_COMM_ISO to +5V_COMM_ISO, followed by a low-noise LDO (NCP1117ST33T3G) that further regulates +5V_COMM_ISO to +3V3_COMM_ISO.

On the **PCB**, careful attention is given to **power integrity, thermal handling**, and **layout isolation**. Wide, thick top-layer traces are used extensively in this section to carry the supply current with minimal voltage drop and to ensure lower impedance

paths. This also reduces the generation of heat and voltage ripple, particularly across the buck converter and LDO regulator.

A large number of VIAs are deployed throughout the section to distribute current efficiently between layers — especially beneath and around the regulators and output capacitors. These VIAs form a robust power network and also help manage thermal dissipation by conducting heat into internal copper planes and the bottom layer.

The buck converter and its surrounding components (inductor, input/output capacitors, and Schottky diode) are placed compactly with short, direct routing between high-frequency switching nodes. This helps to reduce EMI and improve switching efficiency. High-frequency ceramic capacitors are placed as close as possible to the regulator input and output pins to provide fast transient response and minimize voltage ripple.

The LDO stage is positioned near the ATM90E32AS-AU-Y to minimize the length of the sensitive +3V3_COMM_ISO trace. This ensures a clean, stable voltage reaches the measurement IC with minimal noise pickup.

The LED indicators for ±15V_COMM_ISO, +5V_COMM_ISO, and +3V3_COMM_ISO are placed near their respective rail outputs, and their current-limiting resistors are routed compactly to maintain visual feedback integrity without introducing excess trace noise or voltage drop.

Clear power and ground zone separation is maintained throughout this section to support galvanic isolation and minimize ground loop effects. Ground pours for COMM_ISO rails are carefully stitched with VIAs to ensure solid return paths.

For a deeper understanding of how this staged power supply design contributes to system-level performance and measurement accuracy, refer to Chapter 2 page 30.

3.7 Isolation Section

The isolation section "**J**" on the PCB is responsible for maintaining galvanic isolation between the high-voltage energy measurement domain and the low-voltage microcontroller system. This section is visually and electrically separated into two subparts: (1) the Isolated Interrupt and Reset Interface, and (2) the SPI Isolation Interface. Both are physically grouped around two isolator ICs — the ISO7731FBDW and ISO7741DW — located on the PCB near the logical boundary between isolated and non-isolated domains.

PCB Layout Explanation

In terms of layout, this section demonstrates a clean and deliberate isolation strategy. The isolators are placed along the boundary between two power domains: 3.3V_COMM_ISO on the isolated side and 3.3V on the MCU side. The PCB separates their respective grounds — GND_COMM and GND — by a visible gap in the copper plane, ensuring no direct connection and thus preserving galvanic isolation. This isolation barrier is a critical design element and is well implemented by avoiding copper pours or traces crossing between these domains.

On the left (isolated) side of the ISO7731, the IRQ0, IRQ1, and RESET signals are routed through series 56 Ω resistors, placed close to the isolator inputs. These resistors help suppress signal reflections and dampen high-frequency noise. Local decoupling is provided by a 100 nF capacitor near the 3.3V_COMM_ISO pin of the isolator, with proper trace width and via placement ensuring minimal inductive path.

On the right (MCU) side, the corresponding outputs (IRQ0_OUT, IRQ1_OUT, RESET_OUT) are routed with short, direct traces to the microcontroller region, passing through 33 pF EMI-filtering capacitors to GND. These capacitors are placed right next to the isolator output pins for effective high-frequency filtering. The inclusion of N.M. (Not Mounted) footprints provides room for future tuning without board redesign — a practical design choice for EMC optimization.

For the SPI isolation, the ISO7741DW handles four high-speed digital signals. The differentiation between signal direction (e.g., MISO as input, MOSI/CLK/CS as outputs) is reflected in the layout, with careful attention paid to consistent trace impedance and length matching, particularly for CLK and MISO which are more sensitive to timing skew.

Both sides of the ISO7741 have their own 100 nF decoupling capacitors (C52, C53) located as close as possible to the respective power pins to minimize power noise. The SPI traces from the isolator to the MCU and measurement IC are kept short, direct, and mostly free from vias, preserving signal integrity. Optional N.M. capacitor pads (C59–C62) are included on each SPI line, strategically placed mid-trace, allowing post-layout debugging and filtering if high-frequency issues arise during EMI testing.

This section follows good design practices in PCB isolation: clear isolation boundaries, well-placed filtering, decoupling, and routing discipline. The symmetrical and compact layout of isolator ICs also contributes to consistent signal timing and mechanical clarity, helping ensure both performance and safety.

Refer to Chapter 2 (page 28and 31) for a detailed description of the functional role of this isolation system in enabling safe, accurate, and noise-resistant communication between the energy measurement IC and the MCU

3.8 Relay Control

At the core of this section is the **1462041-7 relay**, which is placed close to the board edge to facilitate external connectivity through the nearby **J8** output terminal. This positioning minimizes high-current path lengths and simplifies wiring to external high-voltage or inductive loads. The relay's coil is connected to the +5V rail and switched through the NPN transistor (**Q2**), located directly adjacent to it. This short routing path from transistor to relay minimizes loop area and inductive effects.

The control signal from the MCU, labeled RELAY INPUT, enters the base of Q2 through a 1 KΩ resistor (R22), placed close to the transistor base to reduce trace susceptibility to noise. A 10 KΩ pull-down resistor (R23) and 1 nF capacitor (C28) are placed in parallel between the base and ground to filter out spurious switching due to transient noise or floating input states. These filtering components are physically compact and positioned right beside Q2 to minimize parasitic effects and ensure signal integrity.

The US1NWF flyback diode (D2) is mounted directly across the relay coil pins to suppress voltage spikes caused by the inductive nature of the coil when de-energized. Its placement is optimized for minimal loop area — directly next to the relay and across the coil — ensuring effective clamping of back EMF and protection of the transistor switch. This diode's SMD format also supports thermal and mechanical reliability while maintaining a clean routing path.

Power and ground traces in this section are kept relatively wide, particularly the +5V line feeding the coil, to handle transient currents without voltage sag. The layout avoids vias in high-current paths and provides a direct return path to GND for the transistor emitter. This helps minimize ground bounce and switching noise, improving the overall stability of the relay actuation.

The entire relay driver circuitry is symmetrically laid out, compact, and free of unnecessary trace detours. Careful spacing is maintained between the relay's coil terminals and the signal traces to avoid coupling or unintended triggering, particularly given the inductive nature of the load. Clearance from the MCU-side digital traces is preserved to avoid crosstalk, and the positioning near the PCB edge supports thermal dissipation and routing cleanliness.

Refer to Chapter 2 (page 23) for the functional operation of this relay system, including its interaction with the 3-phase contactor and the role of the NPN driver stage in enabling low-power control of high-power switching devices.

Chapter 4

4. Results

After receiving the fabricated PCB from the manufacturer, a series of functional tests were conducted to verify the correct operation of each subsystem. These tests included checking SPI communication, the CAN interface for both read and write functionality, relay switching, and the behavior of voltage and current sensing circuits. The aim was to ensure that each section of the board performed as expected before integration into the final system.

The microcontroller was programmed using the **STLINK-V3 Debugger and Programmer** from STMicroelectronics. To validate the signals and behaviors, tools such as an **Oscilloscope**, **Multimeter**, and **PLECS displays** were employed. These measurements allowed us to confirm electrical performance, signal integrity, and interaction between system components under realistic operating conditions.

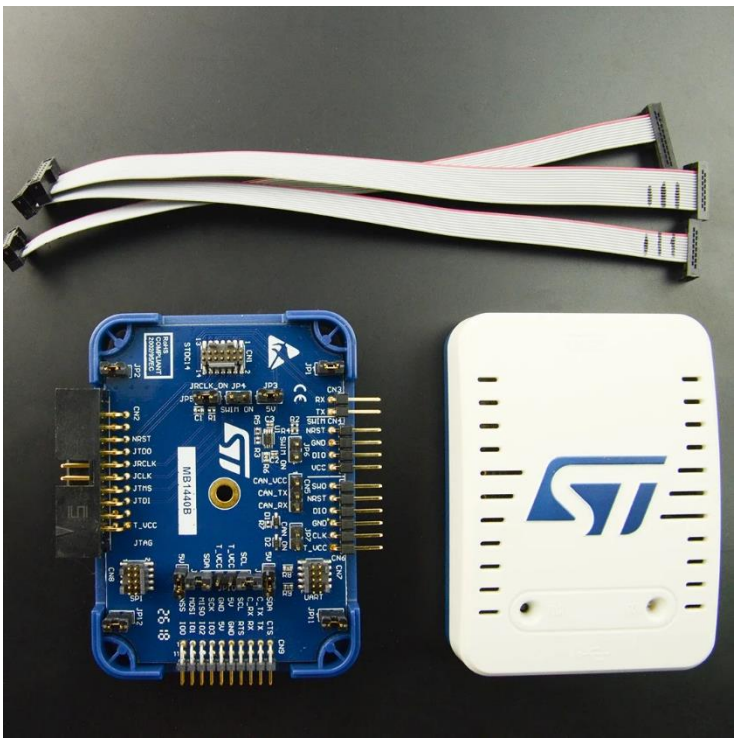

Figure 32: STLINK-V3 Debugger and Programmer

4.1 LEDs

The PCB includes a total of nine LEDs used as visual indicators for power and system status. Among them, seven LEDs are dedicated to monitoring the availability of various power rails on the board: **24V, 5V, 3.3V, ±15V isolated supplies, and 5V and 3.3V isolated voltages**. These LEDs are strategically placed near their respective regulators or power domains to provide immediate feedback during system startup and testing.

To verify the functionality of these seven power-related LEDs, the board was connected to a 24V supply. Upon powering the board, all seven LEDs illuminated as expected, indicating that the voltage regulators and isolated supply sections were functioning correctly so that these can be seen by red LEDs.

The remaining two LEDs are connected to **PC2 and PC3** pins of the STM32G474RET3 microcontroller and are intended for programmable output signaling. Identical control logic was implemented for both PC2 and PC3 via **PLECS**, and both LEDs responded correctly to the programmed toggling (we have taken the results for both of them but in this case, we put the result of **PC3**). This validated not only the GPIO functionality of the MCU but also the effectiveness of the programming and debugging setup used so that it can be seen by Green LED

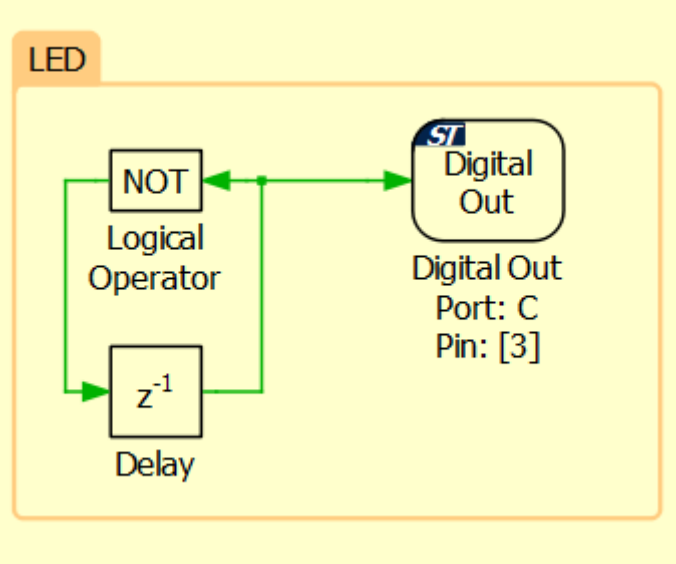

Figure 33 : LED' PLECS configuration

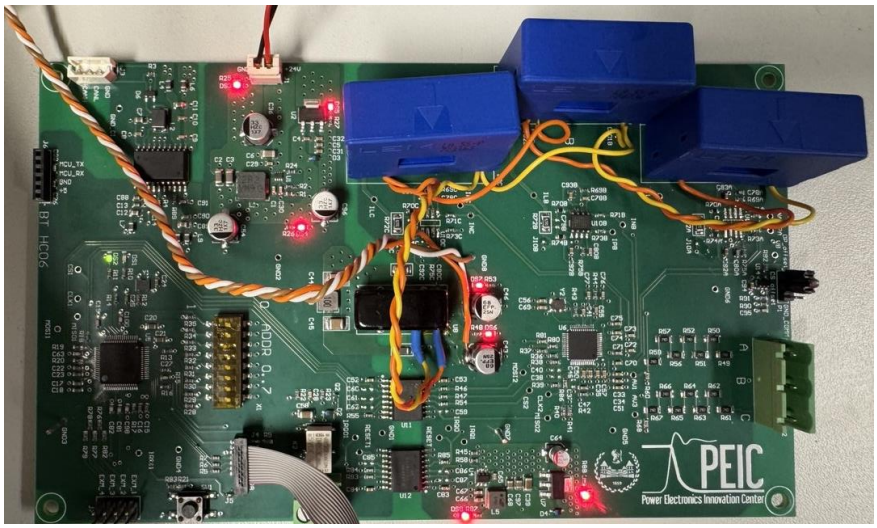

Figure 34 : Test of Blinking

4.2 SPI Communication

The general principle of the SPI communication was previously explained in Chapter 2 (page 26), and the process is also illustrated in the figure below.

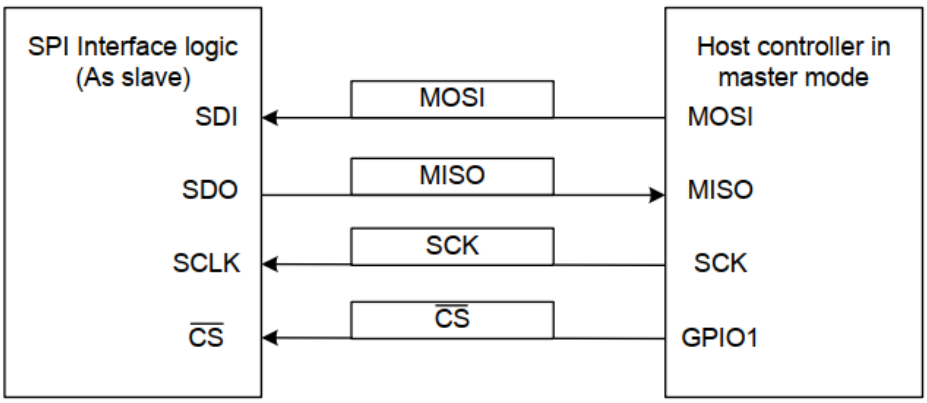

Figure 35 : SPI configuration - Slave Mode

To verify the correct operation of the SPI communication interface, a functional test was performed by reading the "**temperature**" from the measurement IC. Specifically, the goal was to confirm that the MCU could successfully communicate with the IC over the SPI bus and retrieve valid temperature data.

For this test, the SPI interface was correctly configured by assigning the appropriate pins to the SPI peripheral of the STM32 microcontroller in the simulation and programming environment (PLECS). Once the setup was validated, the communication was initiated by sending the correct command frame to the IC. In this case, the temperature register was accessed by sending the 32-bit command sequence [0x80FC, 0x0000].

This command corresponds to the appropriate register address defined in the datasheet of the measurement IC, which specifies how to structure SPI transactions for temperature or other parameters readout. Following this, the MCU received valid temperature data in SDO or MOSI2 of slave, confirming that the SPI lines on the PCB were correctly routed and terminated, and that the firmware configuration was also correct.

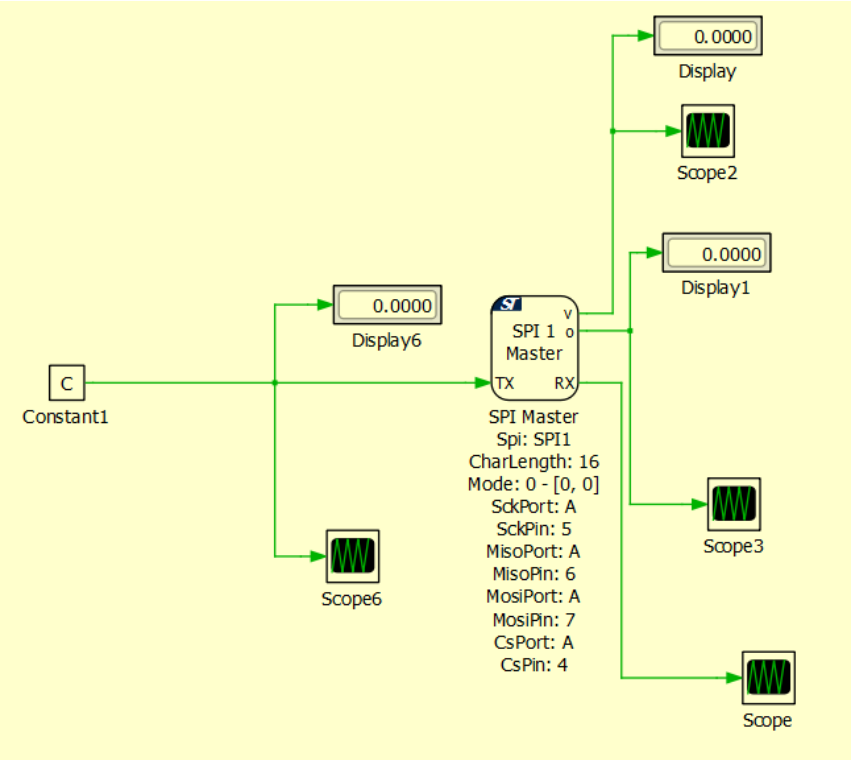

Figure 36 : SPI configuration in PLECS

Figure 37: Reading Temperature (SDO)

As shown, by sending the temperature register, we successfully received the corresponding data, confirming that our SPI communication is functioning correctly. To further validate the system, we gently placed a finger on the measurement IC to increase its temperature. This slight thermal change was accurately detected and reflected in the received data, demonstrating that both the measurement IC and the SPI interface are operating reliably.

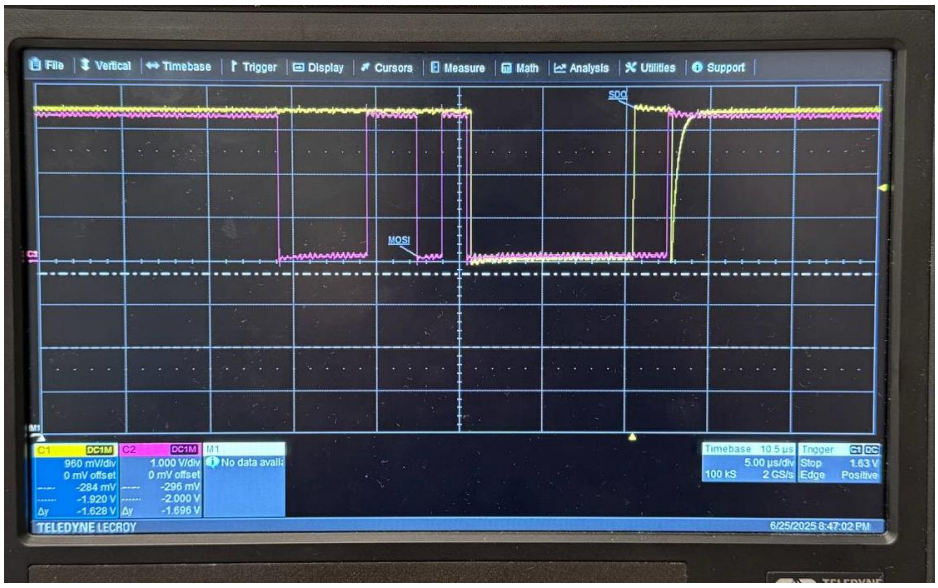

Figure 38 : Reading Temperature (SDO) 2

4.3 CAN interface

The CAN interface is used to enable communication between the measurement IC and external monitoring tools, facilitating the visualization and logging of measured data in a structured and reliable format. The concept and functional role of the CAN bus in this system were discussed in detail earlier (see Chapter 2, pages 24 and 46). At the PCB level, the CAN transceiver (U3) interfaces between the STM32 microcontroller and the physical CAN bus, allowing differential signaling for robust data transmission in noisy industrial environments.

To test and monitor the CAN communication, we used the **PCAN-USB adapter** by Peak-System, which acts as a bridge between the CAN network and a PC via USB. On the PC side, **PCAN-View** software provides a real-time interface to visualize, decode, and verify the transmitted and received CAN frames. This setup allows for comprehensive monitoring of live data from the measurement IC as sent by the microcontroller.

In order to interpret and organize the raw CAN data, a **DBC (Database CAN)** file is used. The DBC file defines the structure of CAN messages, including message IDs, signal names, scaling factors, data lengths, byte orders, and physical units. We created this DBC file using **CANdb++**, a tool that enables easy configuration of CAN signal databases. This structured approach allows PCAN-View to automatically decode incoming messages into human-readable values such as voltage, current, or temperature, based on how the data is defined in the DBC. During the test, once the board was powered and connected to the laptop via PCAN-USB, the PCAN-View software successfully displayed the live CAN messages. This confirmed that the CAN transceiver was functioning properly, the MCU was correctly configured for CAN communication, and the physical layer on the PCB was reliably implemented.

Figure 39 : PCAN-USB adapter

4.3.1 CAN_RX

To test the CAN receiver functionality, we configured our PLECS environment as shown in the figure below. After setting up the simulation, we programmed the board to request the Phase “C” Peak Voltage measurement from the IC by sending the register value [0x80F1, 0x0000].

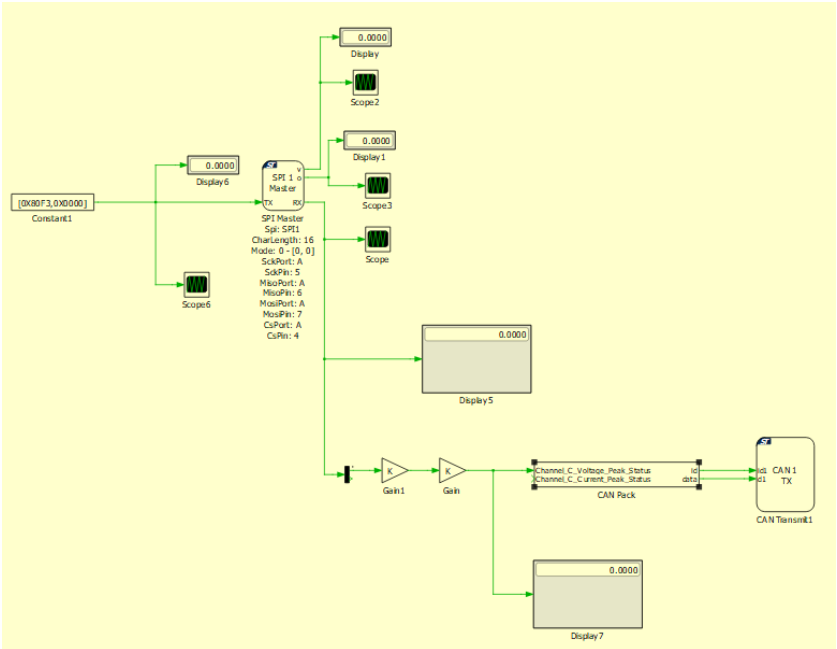

Figure 40 : CAN_RX PLECS configuration

Since each CAN message is 32 bits and the output from the measurement IC provides 16-bit data per register, we can efficiently pack two 16-bit values into a single 32-bit CAN message. For this reason, in our DBC file, we defined combined signals—for example, the Channel C Peak Status—which includes both the peak voltage and peak current of Phase C. As illustrated in the figure below, the start bit of the peak voltage is set to 32, indicating that the second 16 bits of the 32-bit CAN message represent the peak voltage of Phase C.

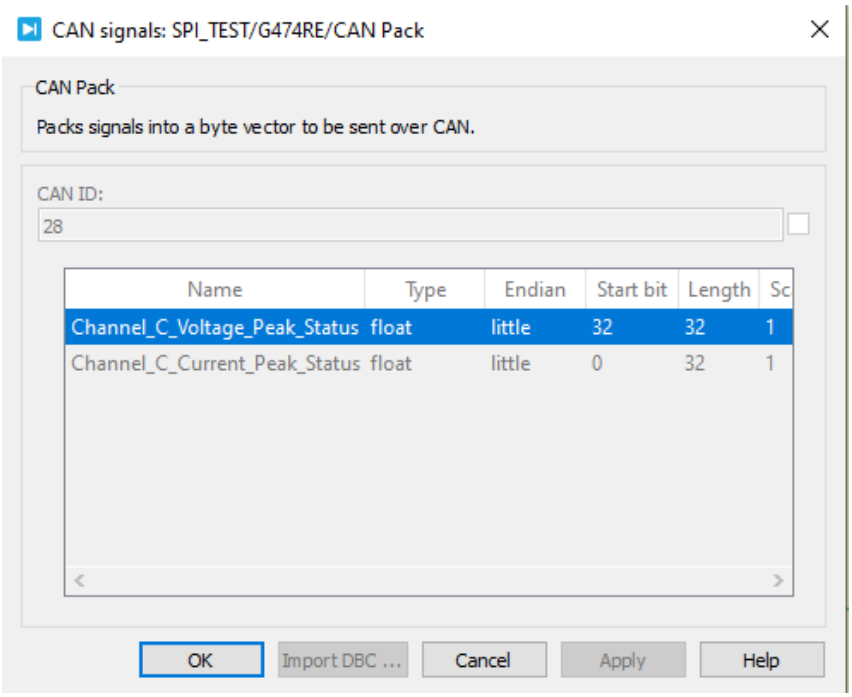

Figure 41 : Selecting proper BDC file

Once the board was running with the programmed configuration, the expected behavior was to receive and decode the temperature data over the CAN bus. This data is sent by the MCU and received through the PCAN-USB interface, where it is visualized using the PCAN-View software.

As shown in the figure below, the real-time phase “C” Peak Volage data was successfully displayed in PCAN-View Receive section. This confirmed that the CAN RX line and message decoding were functioning correctly, and the

communication between the measurement IC and the MCU was properly established and relayed over the CAN network.

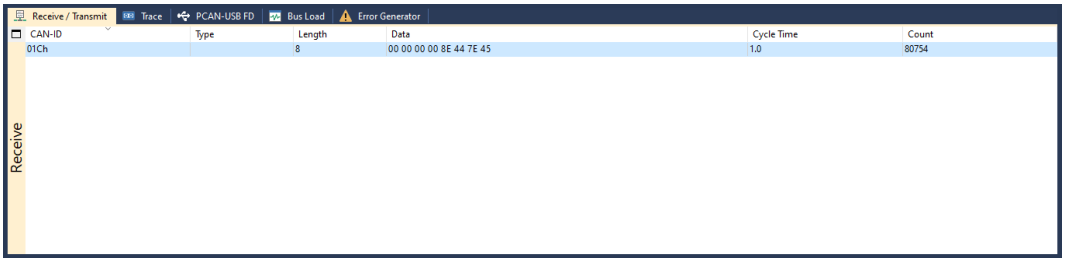

Figure 42 :visualized the PCAN-View of Phase "C" Peak Voltage

4.3.2 CAN_TX

In this part, we tested the CAN transmitter functionality by sending a command from the PCAN-View software to the MCU. To perform this test, we first added a new message in the ***Transmitter*** section of PCAN-View. In parallel, the PLECS model was configured accordingly to enable the MCU to respond to incoming CAN messages. After programming the board with this configuration, we proceeded with the transmission test.

It is important to ensure that the transmitted data corresponds to the correct CAN ID defined in the DBC file. In our project, we defined a message named **Relay_Status** with a CAN ID of 0x05. The message length was set to 1 byte, as the purpose of this command is to remotely activate the relay on the main board.

When the PCAN-View transmitted the Relay_Status message every 10 ms (as set in its cycle time configuration), the MCU correctly received the command and responded by triggering the relay. The successful activation of the relay was confirmed by the audible ***click*** or ***pop*** sound, indicating that the relay had closed as expected.

This test verified that the CAN TX path and Relay functionality—from PCAN-USB to MCU and relay control—was functioning as intended, demonstrating reliable command reception and real-time actuator response.

Note: As can be seen in the figure below, the digital output **PA2** on the MCU is configured as the control pin for the relay.

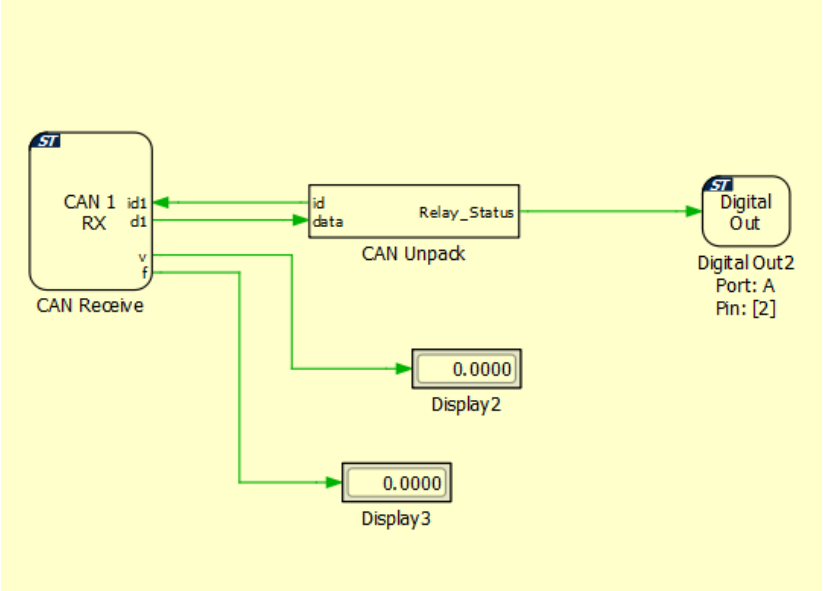

Figure 43 : PLECS configuration for CAN_TX

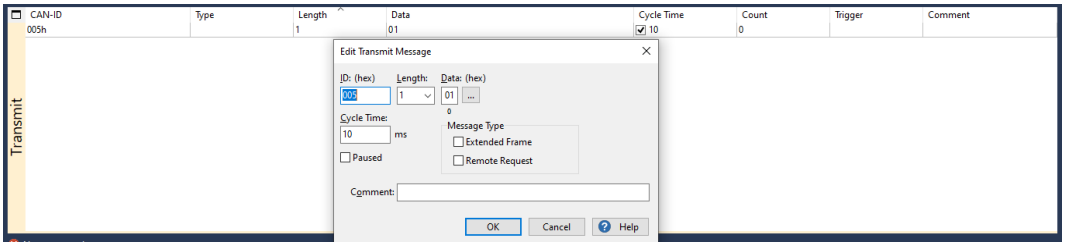

Figure 44 : PCAN_view of Transmit section

4.4 Full System Integration

After individually testing and verifying the correct operation of each subsystem (SPI, CAN, relay, power supplies, etc.), we proceeded to program and test the entire board in an integrated manner. Previously, we tested communication by reading the temperature and phase C peak voltage register of the measurement IC. However, manually writing and reading registers for every parameter is both time-consuming and inefficient, especially during real-time monitoring.

To address this, we implemented a method to send **six important measurement registers** in sequence to enable real-time data acquisition through CAN communication. This setup allows visualization of critical electrical parameters such as voltage, current, and power.

Limitation in PLECS and Workaround:

A significant limitation in PLECS is that it supports only one **CAN Transmit** block, and each block can receive a maximum of 3 messages. Since each CAN message is 32 bits and the output from the measurement IC is 16 bits per register, we are able to pack two 16-bit values into one 32-bit CAN message. As a result, we can transmit up to six parameters using three CAN messages.

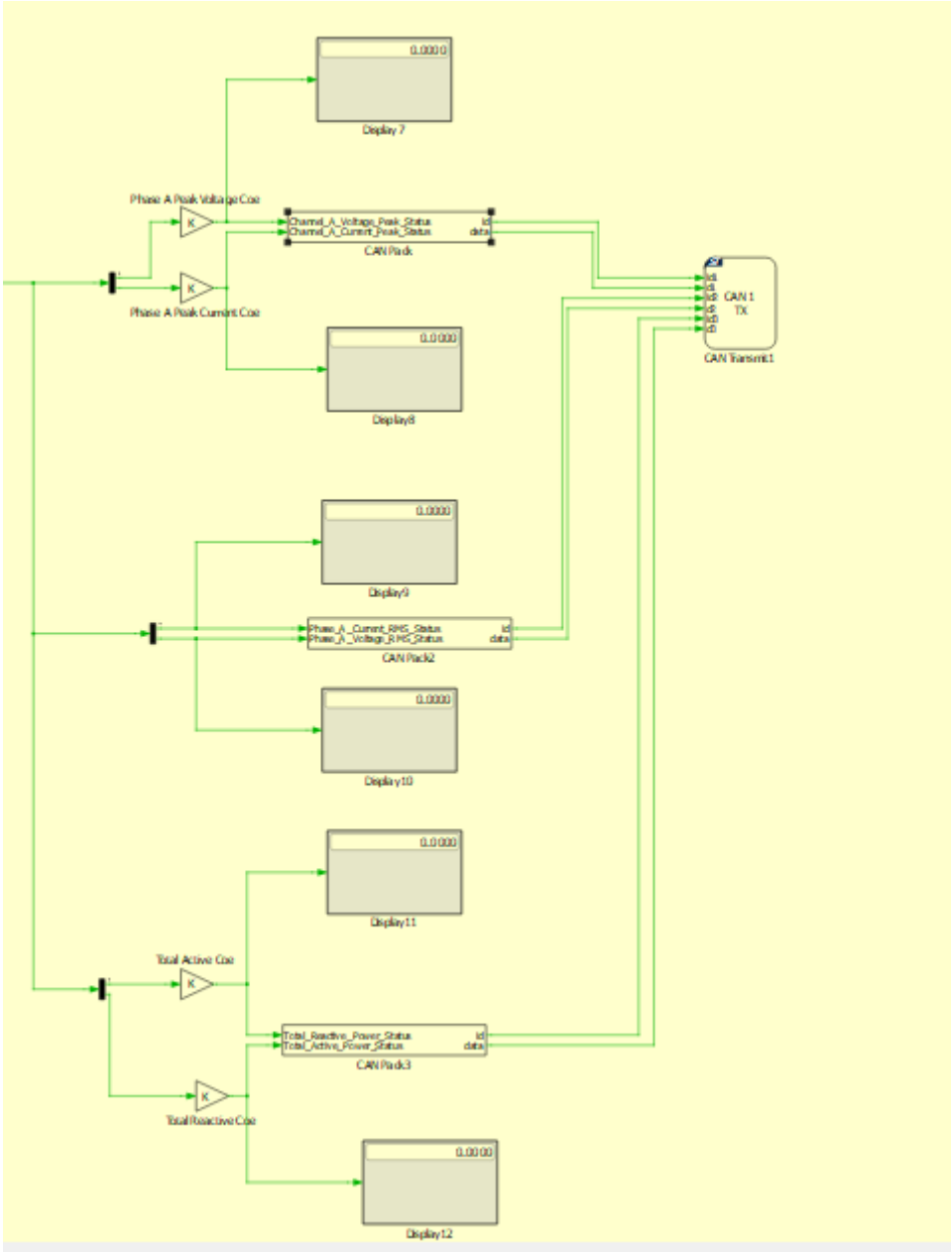

Figure 45 : 3 messages of CAN_TX

Use of Finite State Machine (FSM):

To manage this sequential data acquisition, we implemented **a Finite State Machine (FSM)**. The FSM is responsible for sending each of the six selected registers to the measurement IC at 5-second intervals, reading their 16-bit responses, and packing the results into three 32-bit CAN messages for transmission.

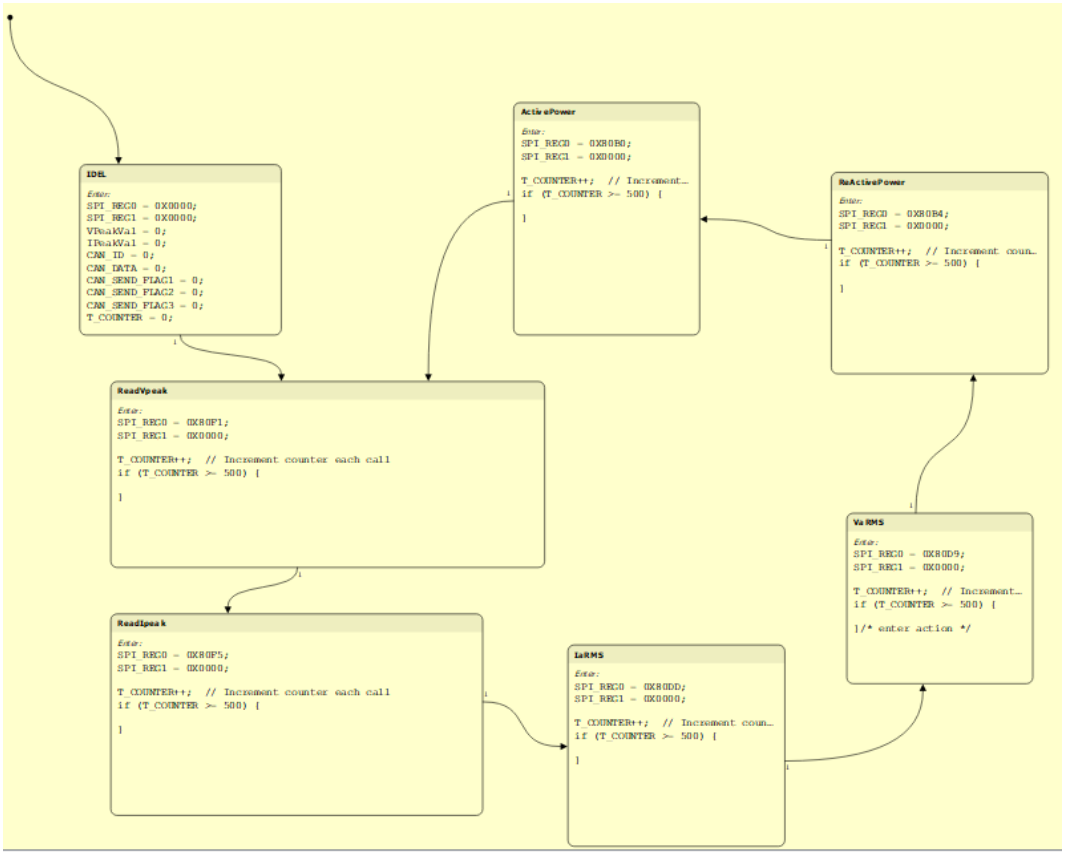

Figure 46 : FSM

These six signals are defined in the DBC file and organized into three RX messages, as shown in the figure below.

- Channel “A” Peak Status
  - 1- Peak voltage of Chanel A, [0X80F1,0X0000]
  - 2- Peak Current of Chanel A, [0X80F1,0X0000]
- Phase “A” RMS Status
  - 3- Phase A RMS Current, [0X80DD,0X0000]
  - 4- Phase A RMS Voltage, [0X80D9,0X0000]
- Total Power
  - 5- Total Reactive Power, [0X80B4,0X0000]
  - 6- Total Active Power, [0X80B0,0X0000]

Figure 47 : Six signals of FSM

This approach ensures that we stay within the communication constraints of PLECS while still providing real-time data visibility for the most critical parameters of the system.

Each CAN message is structured as follows:

- **Message 1: CAN ID 26 (Channel "A" Peak Status)**:
    - First 16 bits → Peak Voltage
    - Second 16 bits → Peak Current
- **Message 2: CAN ID 17 (Phase "A" RMS Status)**:
    - First 16 bits → RMS Current
    - Second 16 bits → RMS Voltage
- **Message 3: CAN ID 1 (Total Power)**:
    - First 16 bits → Reactive Power
    - Second 16 bits → Active Power

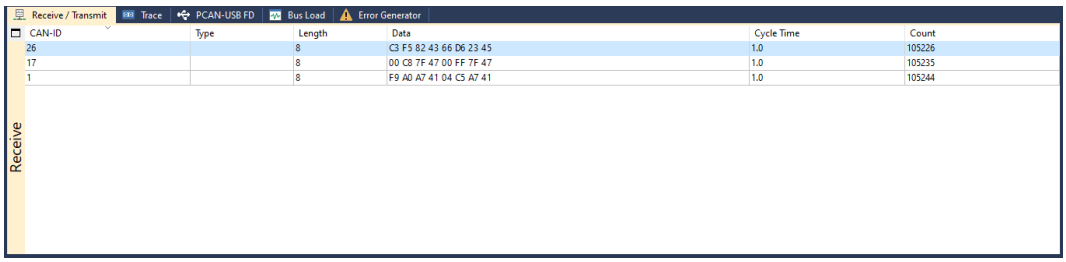

Figure 48 : Reading values of Six Signals from PCAN_view

This FSM structure allows us to flexibly change and observe up to six different parameters by updating the corresponding register values and CAN Peak.

4.4.1 REAL TEST

Due to have a real test we use a setup so that in this setup, the transformer and the METREL rheostat work together to create a safe and adjustable environment for testing electronic circuits.

The transformer takes the high-voltage AC from the mains (usually 230V) and steps it down to a lower, safer voltage—which in our case it is 135.1 Vrms—depending on its internal winding ratio. It also provides electrical isolation between the mains and our circuit, which is important for safety.

After the transformer, the METREL rheostat is connected in series with the output. It acts like a variable resistor, allowing you to adjust how much current flows into your circuit. —which in our case it is 0.779 Arms— This makes it really useful during testing or when powering up a new design, because you can slowly increase the current and observe how the system responds. It also helps protect sensitive components by preventing sudden surges or overcurrent situations.

Using a transformer with a rheostat like this is a common approach in electrical labs when testing simulating different load conditions.

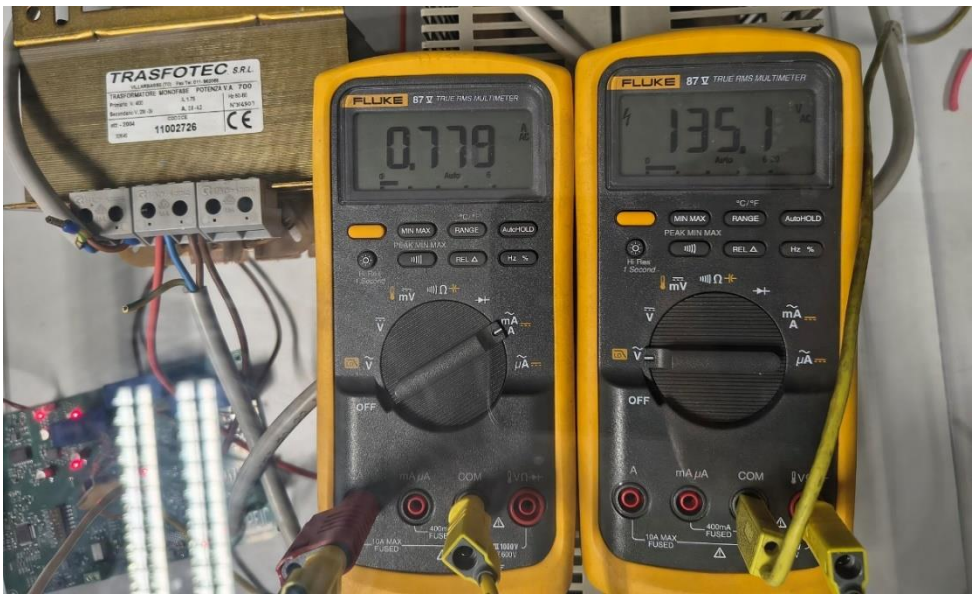

Figure 49 :Voltage and Current of Transformer and Rheostat

To validate the functionality of our setup, we configured PLECS and programmed the board three times to confirm that the system operates correctly. In the first test, we sent the command [0x80F8, 0x0000], which corresponds to the frequency register. Upon programming and running the system, the display showed a value of approximately 5000. According to the measurement IC's datasheet, this raw value must be multiplied by 0.01, indicating that the actual system frequency is 50 Hz—which confirms that the system is functioning as expected.

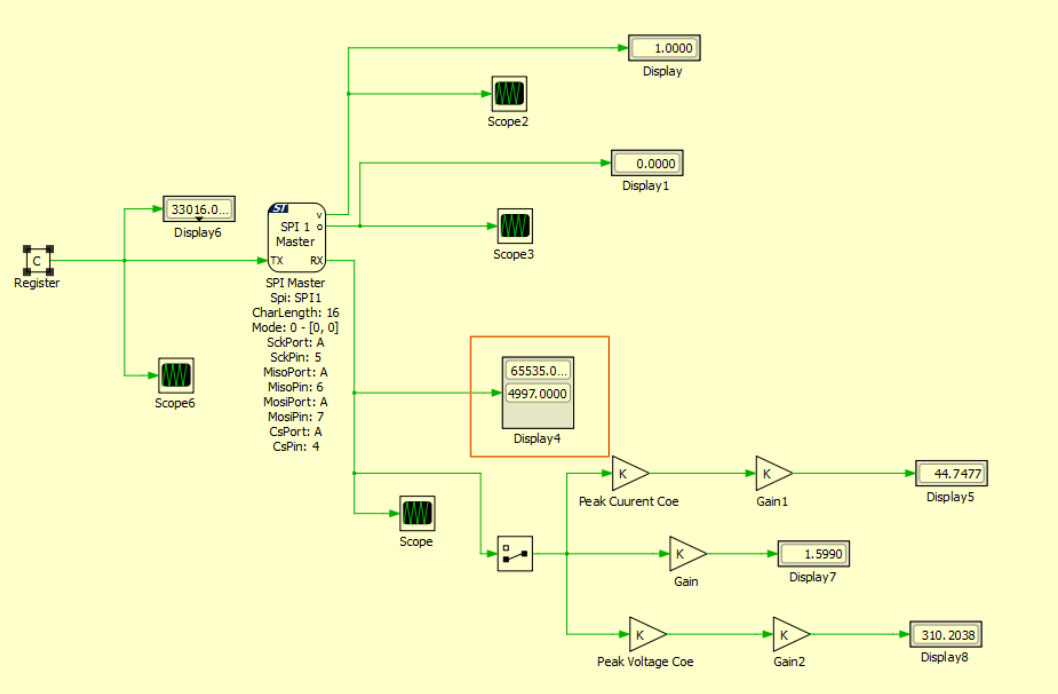

Figure 50 : Reading of Frequency from Measurement IC

F8H	Freq	R	Frequency	1LSB corresponds to 0.01 Hz

Figure 51 : Coefficient of Frequency

In the second step, we used the register [0x80F3, 0x0000] to read the peak voltage of phase C. During programming and simulation, the retrieved raw value was approximately 3077. To calculate the actual peak voltage, this value must be multiplied by a gain factor (for Peak Voltages is 0.04), as defined in the measurement IC's datasheet.

Bit	Name	Description
15:0	UPeakDataA	Channel A voltage peak data detected in the configured period. Component. Unit is V. UPeak is calculated as below: $UPeak = UPeakRegValue \times \frac{UgainRegValue}{100 \times 2^{13}}$ Here UgainRegValue is the register value of the Ugain (61H/65H/69H) register.

Figure 52 : Peak Voltage Coefficient

In our case, the UPeakRegValue is 3077 and the UgainRegValue is 0x8000, according to the datasheet. The final peak voltage of phase C, displayed on Display 8, reflects the result of this calculation that is almost 191V.

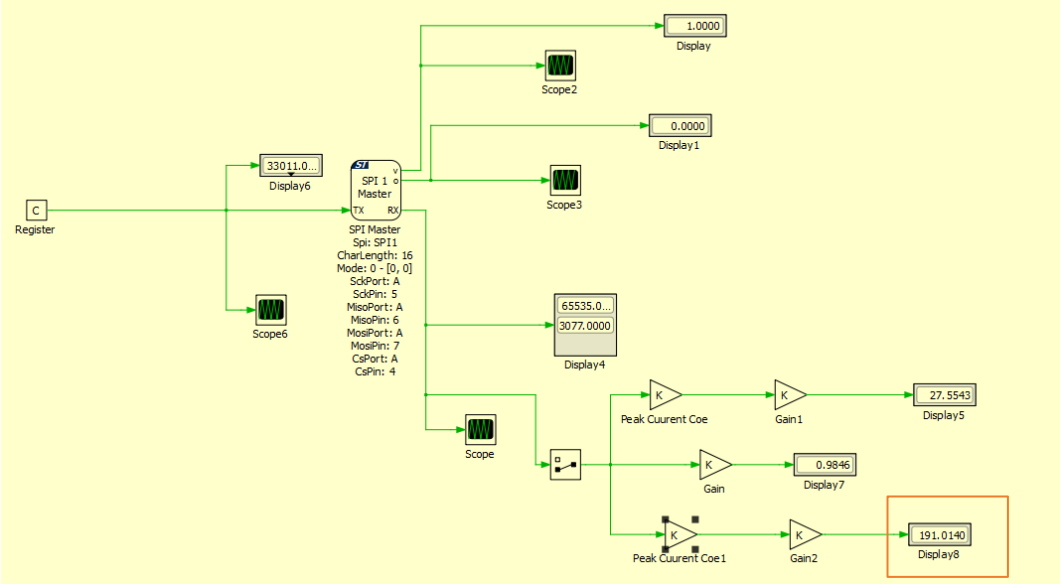

Figure 53 : Peak Voltage Phase "C"

Note: It must be mentioned that due to the internal circuitry of the board, the actual measured values from the IC are slightly attenuated. To compensate for this reduction, an additional gain factor—referred to as **Gain2** and **Gain1**—is applied. This correction factor was experimentally determined for each parameter by applying known reference values (e.g., known voltages and current) and observing the corresponding lower readings from the IC. By calibrating against these known values, we derived Gain2 to ensure accurate and reliable measurements across the system.

As final step we repeat the same procedure for Peak current phase C so that we send the command of [0X80F7,0X0000], During programming and simulation, the retrieved raw value was approximately 126. To calculate the actual peak Current, this value must be multiplied by a gain factor (for Peak Current is 0.004), as defined in the measurement IC's datasheet.

Address: F5H Type: Read Default Value: 0000H		
Bit	**Name**	**Description**
15:0	IPeakDataA	Channel A current peak data detected in the configured period. Component. Unit is A. IPeak is calculated as below: $IPeak = IPeakRegValue \times \frac{IgainRegValue}{1000 \times 2^{13}}$ Here IgainRegValue is the register value of the Igain (62H/66H/6AH) register.

Figure 54 : Peak Current Coefficient

In our case, the IPeakRegValue is 126 and the IgainRegValue is 0x8000, according to the datasheet. The final peak voltage of phase C, displayed on Display 5, reflects the result of this calculation that is almost 1.12A.

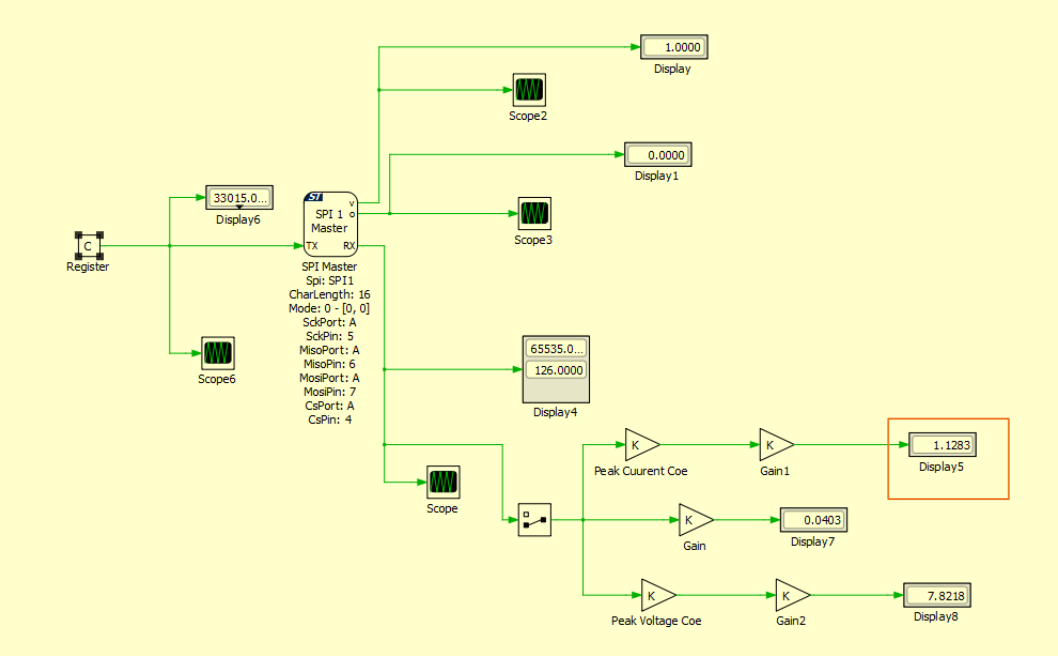

Figure 55 : Peak Current Phase "C"

It should be noted that due to the absence of a three-phase load during testing, we were not able to fully validate the system under real three-phase operating conditions. However, since each individual phase was tested and verified independently, we can confidently conclude that the system will operate correctly when connected to a full three-phase load as well.

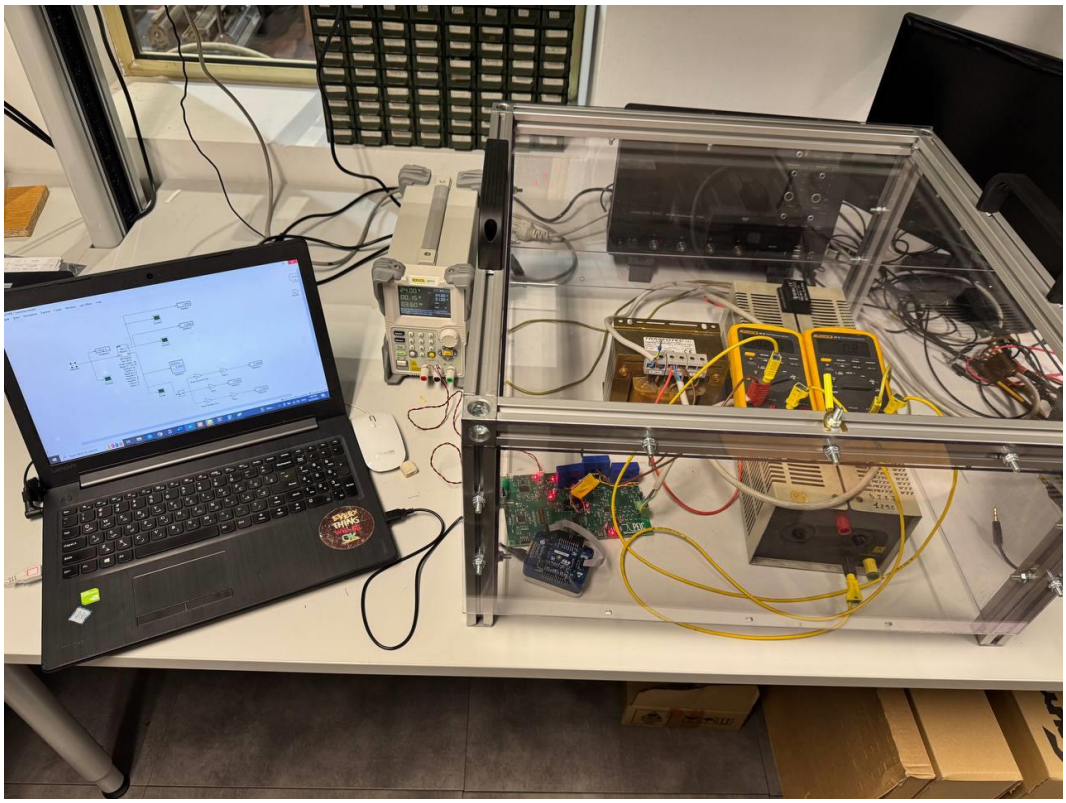

Figure 56:Final Setup

Conclusion

In this thesis, a complete three-phase measurement and monitoring system was designed, developed, and tested using the ATM90E32AS IC and an STM32 microcontroller. A custom PCB was created with special attention to isolation, power integrity, and signal clarity. All critical blocks—including isolated SPI and CAN communication, power supply, relay control, and DIP configuration—were verified through simulation and practical testing.

The results confirm the system's reliability in reading real-time electrical parameters and interacting with external systems via CAN. Even without a full three-phase load, individual phase testing demonstrated the system's effectiveness, validating the design for future integration in larger industrial setups.

References

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  -ISOW1044BDFMR-
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  -219-8MST-
  https://www.ctscorp.com/Files/DataSheets/Switches/DIP-Switches/CTS-Switches-DIP-219-Series-Datasheet.pdf
- Oscillator, Frequency 8 MHz, Supply Voltage 3V3.
  -ASEMB-8.000MHZ-LC-T-
  https://abracon.com/Oscillators/ASEMB.pdf
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- Isolated DC/DC converter. Dual output ±15V&300 mA -TMR_9-2423 –
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- Quad-Channel Digital Isolator, High-Speed, Wide-SOIC3 3V3_COMM_ISO.
  -ISO7741DW-
  https://tinyurl.com/ykze7wtn
- 4-V to 36-V, 1-A Buck Converter using for isolated +15V_COMM_ISO to 5V_COMM_ISO.
  -LMR50410YQDBVRQ1-
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  -OPA365AIDBVR-
  https://tinyurl.com/49eth5nu

Appendix

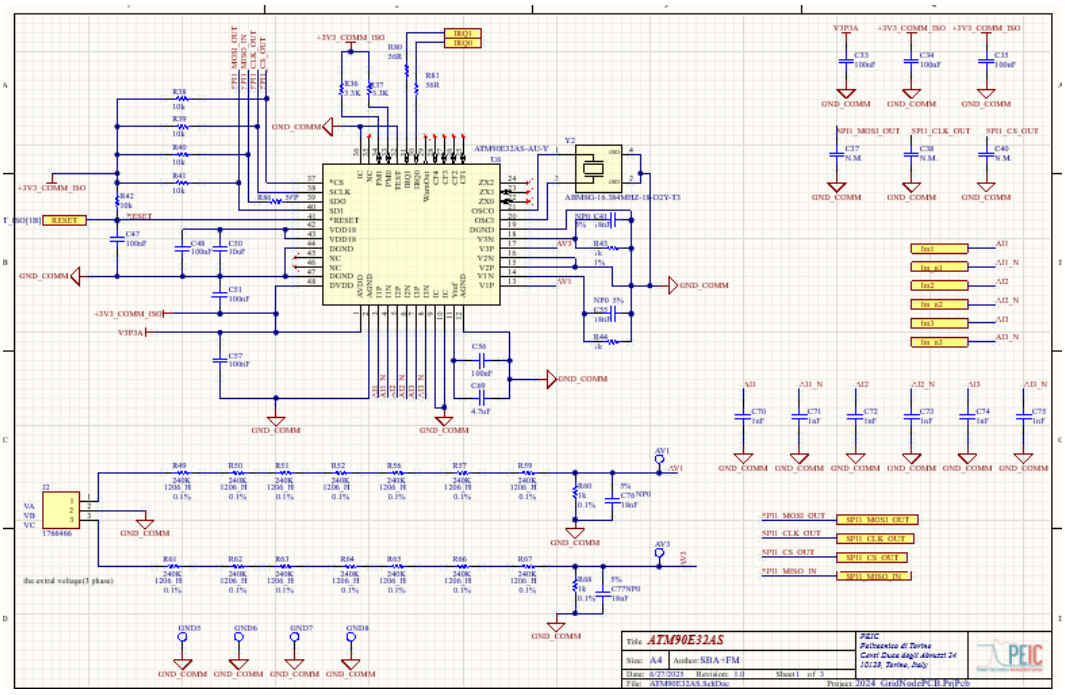

Figure 58 : Measurement IC Circuit

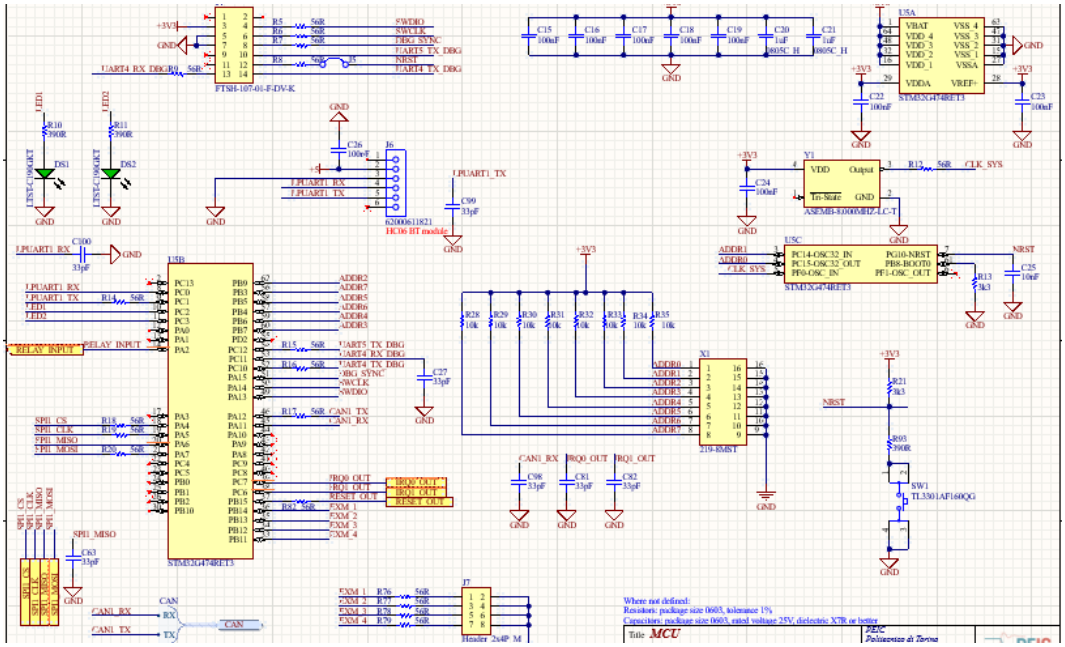

Figure 57 : Micro Controller Unit Circuit

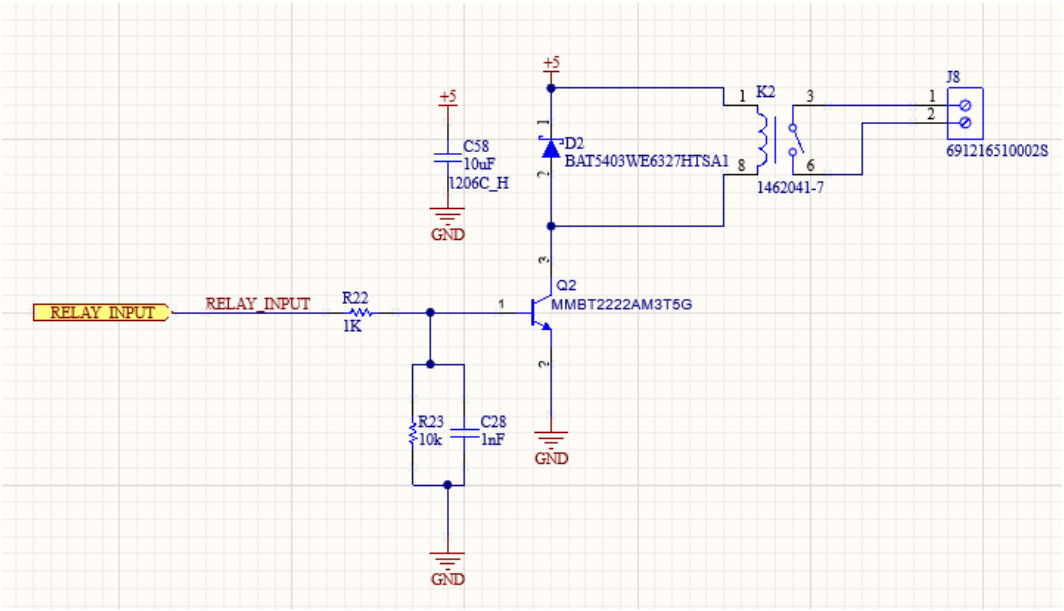

Figure 60 : Relay Circuit

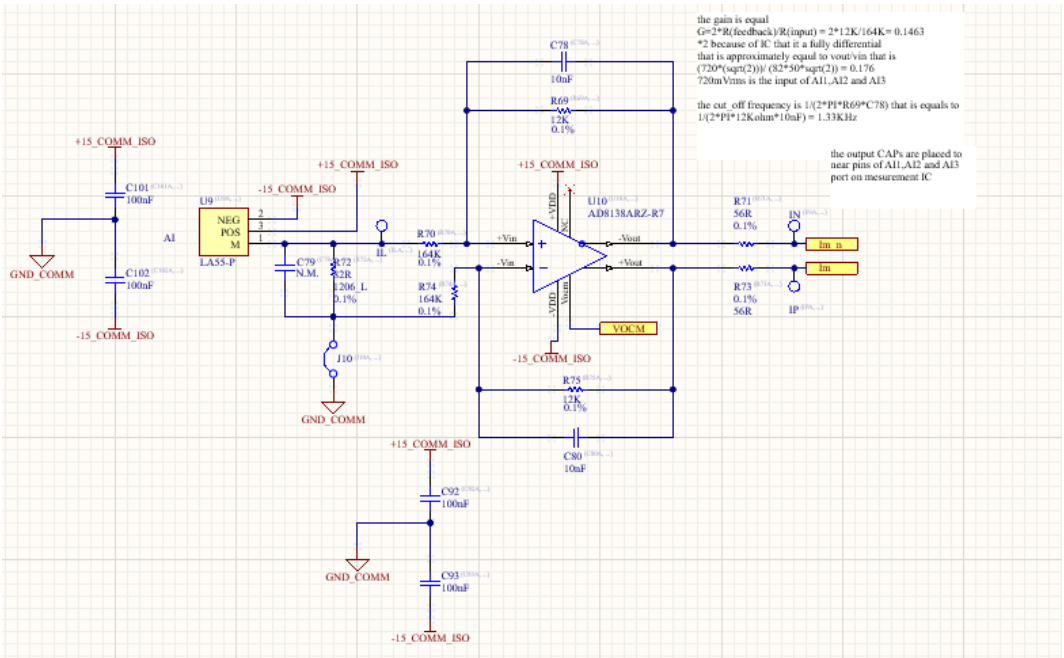

Figure 59 : Current Sensor Schematic

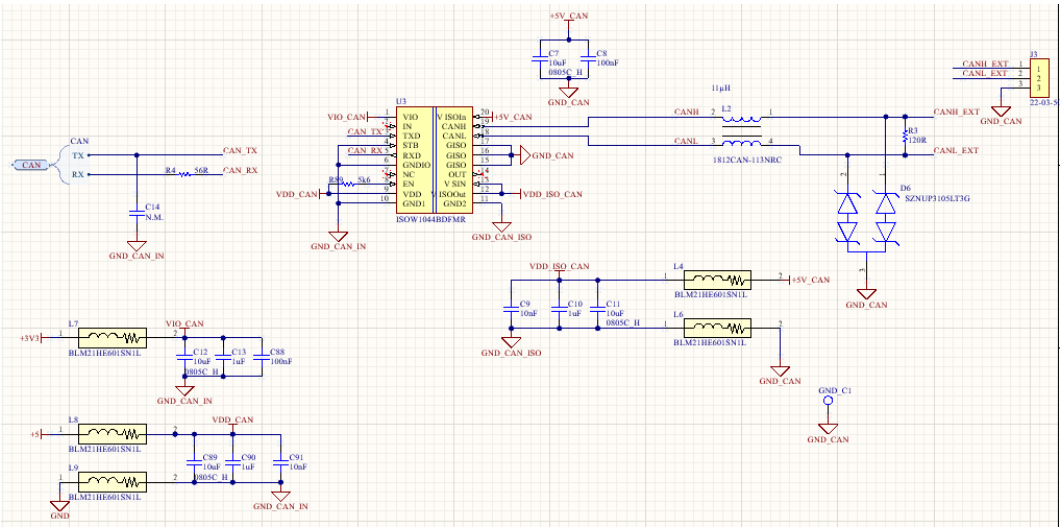

Figure 62: CAN interface Circuit

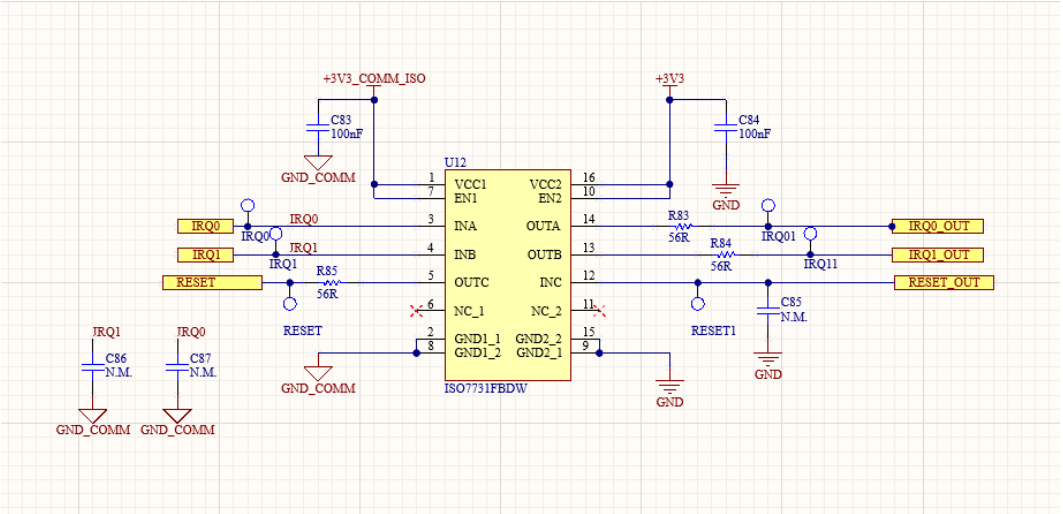

Figure 61 : IRQ Reset Circuit

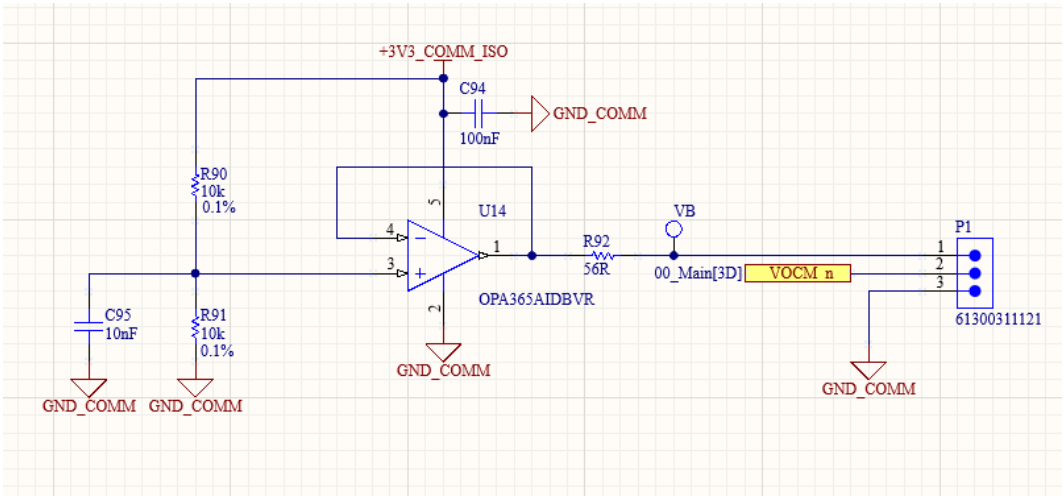

Figure 64 : Bias Circuit

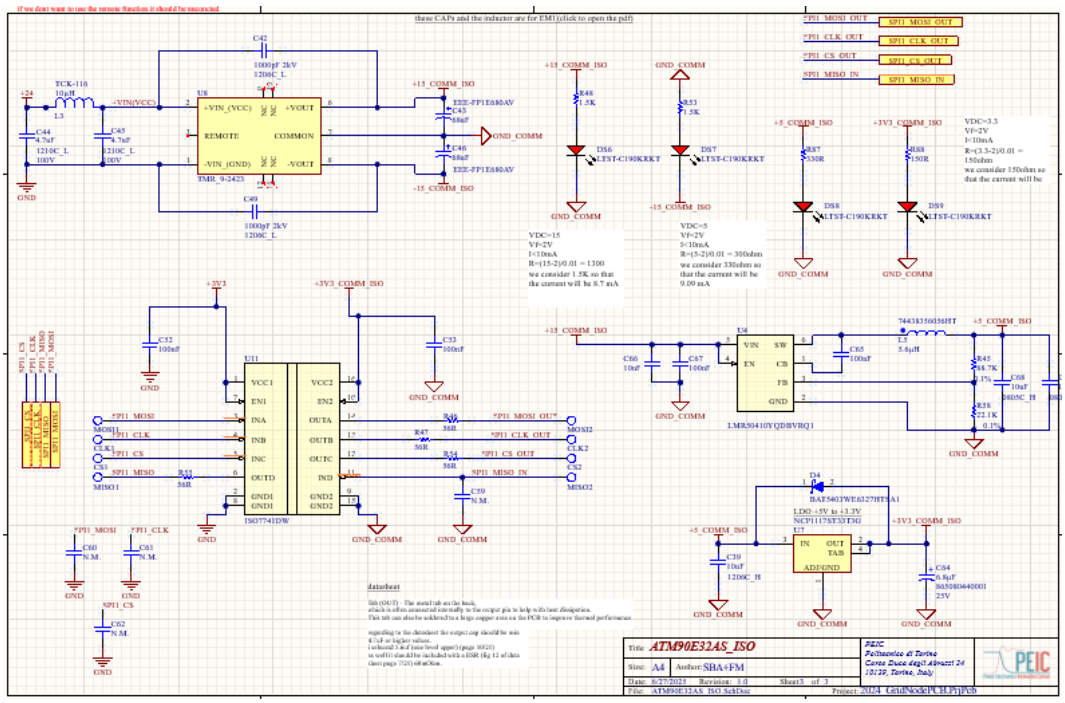

Figure 63 : Power Supply Circuit

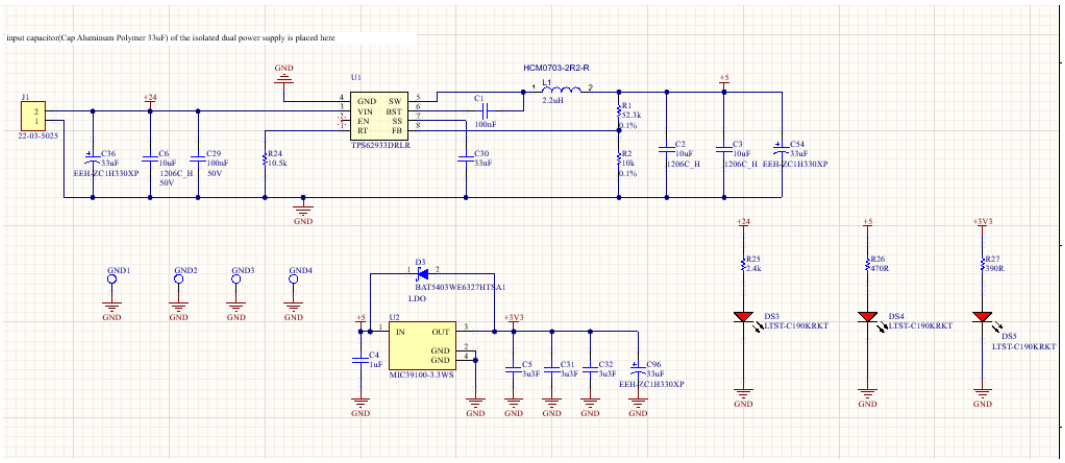

Figure 65 : Dual Power Supply Circuit