POLITECNICO DI TORINO

Master's degree programme
in Nanotechnologies for ICTs

Towards Scalable Silicon Qubits: TCAD Simulations of Gate-Defined Single-Electron Transistors

Supervisor
Prof. Matteo Cocuzza
Dr. Esteve Amat Bertran
Dr. Jordi Llobet Sixto

Candidate
Gabriele Petitto
309170

July 25, 2025

Acknowledgments

I would like to express my sincere gratitude to my supervisor, Prof. Matteo Cocuzza, for his availability and support throughout this thesis work. I am also deeply thankful to my external supervisors, Dr. Jordi Llobet and Dr. Esteve Amat, for being excellent mentors and always willing to guide me whenever needed.

I want to thank all the people I met during my thesis experience in Spain - those I had the pleasure to collaborate with and who supported me in the project, as well as those I got to know personally and share time with beyond the academic setting.

I also wish to thank all the people I met during my time at Politecnico, who made these years enriching and unforgettable. In particular, I want to thank Alex, Luca, Carmelo, Francesco, and Michele.

A very special thank you goes to Flaminia.

Finally, I am profoundly grateful to my family - my uncles and aunts, my parents, and my brother - for their unwavering support and encouragement.

Contents

Introduction

Quantum computation enables a computational speed-up over classical computers for very specific problems, by exploiting the interference between quantum states of qubits—the quantum analogues of classical bits—to evaluate multiple computational paths in parallel. The main challenge in physically implementing quantum computing platforms lies in maintaining a sufficiently long coherence time to perform the required operations on the qubits before coherence between them is lost. Spin qubits based on the spin states of confined charge carriers in semiconductor quantum dots represent a particularly attractive alternative, as they combine relatively long coherence times with high integration and scalability—essential features for the implementation of redundant qubits in Quantum Error Correcting Codes, where multiple physical qubits are used to encode a single logical qubit.

These advantages stem from the well-established manufacturing capabilities of the semiconductor industry, which has optimized fabrication techniques over decades to achieve high transistor density in small areas. One of the fundamental criteria—known as the DiVincenzo criteria—for determining whether a qubit is suitable for quantum computation is that it must be measurable via an appropriate readout mechanism. In this regard, Single-Electron Transistors (SETs) can be used as readout elements in spin-to-charge conversion-based protocols.

This thesis was carried out in collaboration with the Institute of Microelectronics of Barcelona (IMB-CNM, CSIC). The IMB-CNM is a research center of the Spanish National Research Council (CSIC), specializing in the development and fabrication of micro- and nanoelectronic devices. Located at the UAB Campus in Bellaterra (Barcelona), the institute combines cutting-edge scientific research with advanced technological facilities, including a cleanroom for microfabrication. The thesis work was supervised by the NanoNEMS group, which specializes in advanced nanofabrication techniques.

The goal of this thesis was to develop simulations that could support the group in the fabrication of gate-defined Single-Electron Transistors (SETs) for quantum-dot-based semiconductor platforms. Developing a properly functioning SET fabrication process is a crucial first step toward building semiconductor platforms for quantum computing. It provides feedback on the correctness of the process and helps identify and address potential issues. The TCAD simulations carried out in this thesis were primarily aimed

at supporting the understanding of the behavior of the devices currently under development, as well as at building a model that could closely approximate the real operation of the device. Given these objectives, the choice was to use a semiclassical model included in the Sentaurus software by Synopsys. This approach allowed for simulations that were not overly time-demanding and that provided a general understanding of the device, although at the expense of the ability to investigate single-electron effects and to simulate behavior at millikelvin temperatures, due to intrinsic limitations of the chosen model.

The fabrication processes are also presented, and the simulation results are compared with both data from the literature, showing good agreement, and preliminary electrical measurements of the fabricated devices.

Chapter 1

Silicon Quantum Dot-Based Qubits

1.1 Introduction

So far, many options have been proposed to physically implement qubits—the information units of quantum computers—including the well-known superconducting qubits, trapped ions, and photonic qubits, as well as research-level implementations such as neutral atom-based qubits [27]. Among these proposals, silicon quantum dot-based qubit technology is one of the most promising alternatives, due to the relatively long coherence times associated with the weak interaction between electron spins and the silicon crystal lattice [39], and its compatibility with CMOS manufacturing processes [25].

This latter advantage enables to exploit already consolidated and optimized processes to scale up and integrate multiple physical qubits into a single chip, as well as to manufacture chips on a large scale. Using multiple physical qubits to encode a logical qubit is essential to increase the system's robustness with respect to decoherence errors [29].

In this chapter, we will briefly revisit the concept of a qubit, which is essential to understanding the working principles of silicon quantum dot-based spin qubits—the subject of this thesis.

1.2 Qubits

The intrinsic advantage of quantum computers over classical computers in solving complex computational problems lies in the quantum nature of qubits and the entanglement established between them [29]. A qubit is the unit of information in a quantum computer; it is the equivalent of a bit in classical computing. Unlike a classical (Boolean) bit, which can assume only two states, 0 and 1, a qubit can exist in a superposition of the two basis states $|0\rangle$ and $|1\rangle$:

$$|\psi\rangle = a|0\rangle + b|1\rangle \tag{1.1}$$

where $|0\rangle$ and $|1\rangle$ are vectors in the Hilbert space $\mathbb{C}^2$, and thus the state $|\psi\rangle$ of the qubit can also be represented as a vector in this space:

$$|\psi\rangle = a|0\rangle + b|1\rangle = a\begin{pmatrix}1 & 0\end{pmatrix} + b\begin{pmatrix}0 & 1\end{pmatrix} = \begin{pmatrix}a & b\end{pmatrix} \tag{1.2}$$

According to quantum mechanics, for a pure state the normalization condition $|a|^2 + |b|^2 = 1$ must hold, where $|a|^2$ and $|b|^2$ represent the probabilities of measuring the system in state $|0\rangle$ or $|1\rangle$, respectively. This allows the state to be expressed in polar coordinates and represented as a vector on the Bloch sphere:

$$|\psi\rangle = \cos\frac{\theta}{2}|0\rangle + e^{i\delta}\sin\frac{\theta}{2}|1\rangle \tag{1.3}$$

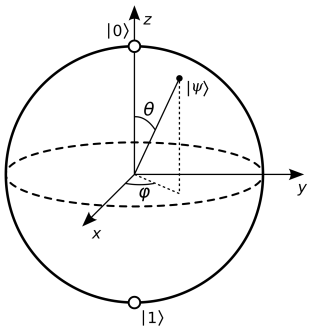


Figure 1.1: Bloch sphere representation of a generic qubit pure state [40].

The high computational power of quantum computers arises precisely from the superposition of states in qubits, which enables the machine to evaluate multiple logical paths in parallel through algorithms that exploit constructive and destructive interference between quantum states. A clear example of this—briefly mentioned here to avoid unnecessary digressions—is the Deutsch algorithm [7], one of the simplest quantum algorithms.

To better understand the advantage provided by superposition in qubits, let us compare the information content of a system of n qubits with its classical counterpart:

- n classical bits can represent 2^n different states but can only assume one configuration at a time;
- n qubits can exist in a quantum superposition of all 2^n basis states simultaneously.

This means that to represent the quantum state of n qubits, a classical computer would require 2^n complex coefficients. However, to date, only a few algorithms—most notably Shor's algorithm for prime factorization [36], and Grover's algorithm for exhaustive search [15]—are known to leverage quantum properties to achieve a speed-up over classical computation. Furthermore, individual operations on qubits are generally slower than operations on classical bits. Therefore, quantum computing becomes advantageous primarily for problems with high computational complexity, and the benefit increases as the problem size grows.

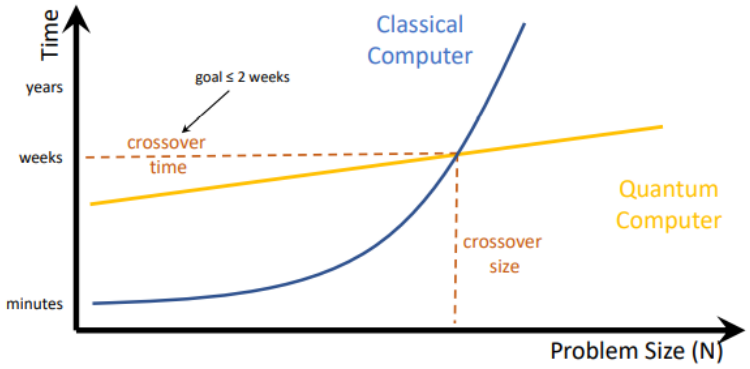


Figure 1.2: Quantum speedup [18]. The goal is to reduce the crossover time and crossover size, i.e. the time and problem size beyond which it becomes advantageous to use quantum computation.

1.3 Decoherence

In quantum computation, the decoherence of a qubit refers to the loss of quantum information due to its interaction with the external environment [29].

Decoherence in a given physical qubit platform is not a fundamental limitation per se; what truly matters is its ratio to the gate operation time, that is, the time required to perform a single operation on a qubit (calculated by measuring the period of the Rabi oscillations):

$$\frac{\text{decoherence time}}{\text{gate operation time}} \tag{1.4}$$

This ratio provides an estimate of how many operations can be performed on each qubit before the stored information is lost, and is currently the most limiting factor in building quantum computers.

Pure and mixed quantum states To better understand the implications of decoherence and how it can be measured, it is necessary to examine the concepts of pure and mixed quantum states.

A quantum state is said to be pure if there exists a measurement for which one of the possible outcomes occurs with probability 1. In the absence of interactions with the environment, a pure state evolves unitarily and remains pure over time.

In a qubit, a pure state is any state:

$$|\psi\rangle = a|0\rangle + b|1\rangle = \cos\frac{\theta}{2}|0\rangle + e^{i\delta}\sin\frac{\theta}{2}|1\rangle \tag{1.5}$$

Consequently, pure states are all those states that can be represented by a vector pointing to the surface of the Bloch sphere. A unitary transformation means that the vector evolves over time by rotating, but without changing its magnitude.

A quantum state is said to be mixed if it can be described as a probabilistic ensemble of pure states:

$$|\psi\rangle = p_1|\psi_1\rangle + p_2|\psi_2\rangle + p_3|\psi_3\rangle + \cdots + p_n|\psi_n\rangle \tag{1.6}$$

where p_i is the probability that the mixed state is in the pure state $|\psi_i\rangle$ and $\sum_i p_i = 1$. It is easy to verify that the Bloch vector associated with a mixed state always has a norm strictly less than 1, therefore it points inside the Bloch sphere.

When a qubit in a pure state interacts with the external environment it becomes a mixed state which does not maintain phase coherence over time (decoherence), hence it becomes computationally ineffective considering that any quantum computing algorithm rely on interference between the coherent quantum states of qubits.

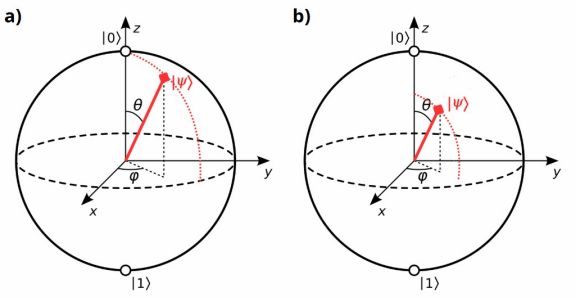


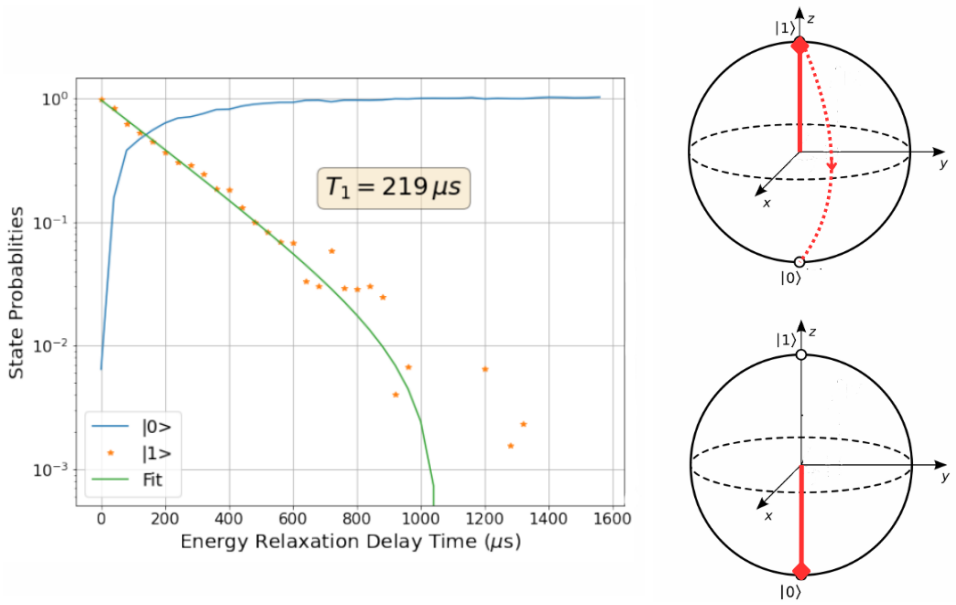
Figure 1.3: Bloch sphere representation of a) a generic pure state and b) a generic mixed state. The position along the vertical axis is related to the probabilities of the $|0\rangle$ and $|1\rangle$ components. The rotation around the same axis is associated with the relative phase between them.

1.3.1 Decoherence time

As mentioned above, decoherence is associated with the loss of quantum information. Therefore, when studying the physical implementation of a type of qubit, it is crucial to estimate its decoherence time in order to understand how many computational operations can be performed on the qubit before the information is lost [29].
The total decoherence time of a qubit consists of two contributions:

$$\frac{1}{T_2^*} = \frac{1}{2T_1} + \frac{1}{T_2} \tag{1.7}$$

- **Longitudinal relaxation time** T_1: This refers to the average time the system takes to relax from the excited state to the ground state, which is energetically more favorable. To measure it, the system is initialized in the excited state ($|1\rangle$ in Figure 1.4b, opposite to the convention used in the Bloch spheres discussed in this chapter), and then measured after increasing delay times.



(a) (b)

Figure 1.4: a) Quantum state occupancy probability vs time [14], the probability of measuring $|0\rangle$ decays as $\exp(-t/T_1)$. b) Bloch sphere representation of longitudinal relaxation.

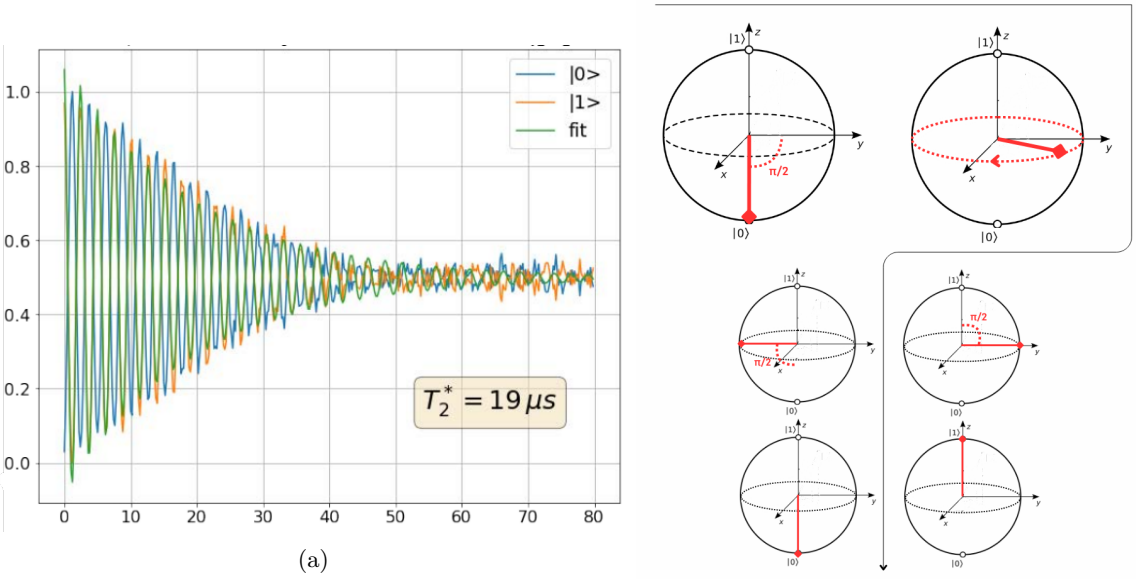
- **Dephasing time** T_2: this refers to the characteristic time over which the system loses purely phase coherence due to interactions with the surrounding environment.

The total decoherence time T_2^* can be measured by observing the decay of Ramsey oscillations. To do this, the system is initialized in the ground state. A $\pi/2$ pulse is then applied to bring the system into an equal superposition state: $|\psi\rangle = \frac{1}{\sqrt{2}}(|0\rangle + e^{i\phi}|1\rangle)$. The system is configured so that the state acquires a time-dependent phase (in the case of spin qubits, this can be achieved by applying a constant magnetic field), causing the associated vector to rotate around the longitudinal axis (Larmor precession).

A second $\pi/2$ pulse is then applied. Depending on the phase of the state at that moment (i.e., on time), this can project the qubit either into the excited state $|0\rangle$ or into the ground state $|1\rangle$. Conse-

quently, by performing repeated measurements at different times, regular oscillations in the measured state probabilities, known as Ramsey oscillations, can be observed.

However, interactions with the surrounding environment cause the initially pure state to evolve into a mixed state (decoherence). This can be visualized on the Bloch sphere by imagining that the state vector reduces its magnitude during the precession motion, due to the fact that the pure states it is composed of are out of phase. As a result, the second $\pi/2$ pulse no longer projects the system into a well-defined state. Instead, it results in a probabilistic mixture, and as $t \to \infty$, the probabilities of measuring either $|0\rangle$ or $|1\rangle$ approach 50%. This corresponds to maximum decoherence, as the Bloch vector approaches zero magnitude.



(a) (b)

Figure 1.5: a) Measurement of phase decoherence in a qubit [14] and b) Bloch sphere reepresentation. As $t \to \infty$, it becomes impossible to measure a state with 100% probability due to intrinsic uncertainty caused by decoherence.

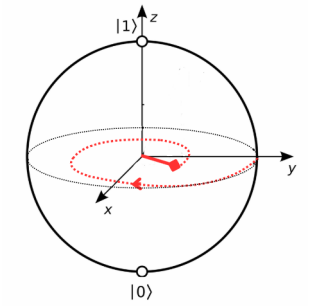


Figure 1.6: Loss of phase coherence during Larmor precession due to the interaction of the qubit with the environment.

1.4 Semiconductor qubits

To date, it is still unclear which qubit technology will ultimately prevail. Some types of qubits are characterized by an intrinsically better ratio between decoherence time and gate operation time, but in general to improve the detrimental effect of decoherence we rely on Quantum Error Correction (QEC) algorithms to make the system more fault-tolerant [36]. However, this requires the use of redundant qubits, i.e. multiple physical qubits used to represent a single, more stable logical qubit. To do this, it is necessary to increase the integration capacity, which is why semiconductor qubits are very interesting. Indeed, among all the possibilities, semiconductor qubits are a very promising option mainly because they allow to exploit the well-consolidated manufacturing capabilities of semiconductor industry to achieve a significant integration [42].

1.4.1 Semiconductor qubits platforms

We briefly present a comparison, based on the work in [], of some of the main alternatives for implementing semiconductor qubits. In general, it is important to keep in mind that the main challenge in designing qubits is achieving both strong isolation from the environment and easy access for control and manipulation. However, these two requirements are fundamentally opposed, so a trade-off is necessary.

- Nuclear spin qubits. The information is represented by the spin of the nuclei of dopant atoms in semiconductor substrates. The main advantage comes from the low interaction between the nuclear spin of the dopants and the environment, which makes them particularly stable over time. However, the fabrication process is non-trivial and difficult to scale, due to the high control required over the positioning of the atoms. Furthermore, the high isolation of the qubits comes at the cost of reduced controllability.

- SiGe heterostructures. In these structures, confinement in the vertical direction is provided by the energy gap difference between the silicon and the silicon germanium, rather than by the electrostatic control of a gate as in MOSFET-like structures. This, combined with the fact that the layers are grown epitaxially, allows for quantum wells with very low defectivity. However, epitaxy makes the fabrication process non-trivial. Also, again, the high isolation of the qubits provides good coherence but results in having less control on them.

- FDSOI and SiMOS structures. These are MOSFET-like structures built on Fully Depleted Silicon-On-Insulator (FDSOI) or bulk Silicon wafers. In this case the confinement along the horizontal plane is given by the geometry of the structure while that in the vertical direction by the inversion layer, created by the gate electrode, at the Silicon-Oxide interface . They exploit the fabrication processes of CMOS technology, which is highly optimized in terms of scalability, and allow the creation of qubits with good coherence, although they have the disadvantage of confining the qubit to the dielectric interface, which presents defects. They will be discussed in more detail in the next chapters, as they are the focus of this thesis.

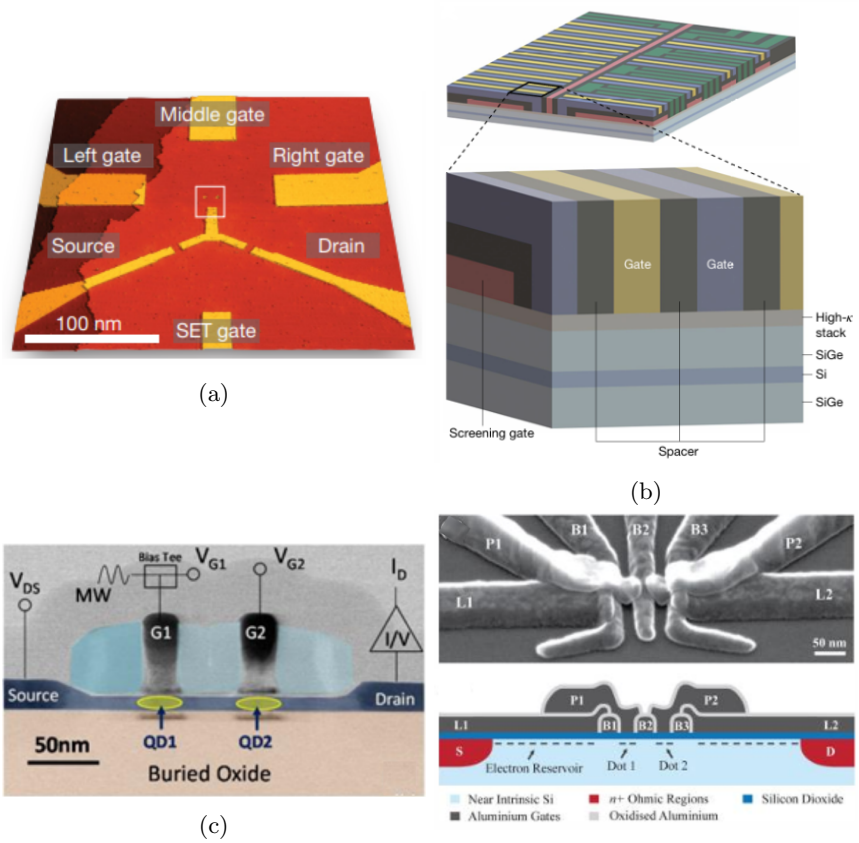


Figure 1.7: Semiconductor platforms for quantum computing. a) Nuclear spin qubits [16], b) SiGe heterostructures qubits [28], c) FDSOI quantum-dot based qubits [19], d) Planar SiMOS Double Quandum Dot qubit [22].

1.5 Quantum Dot based qubits

This Section is dedicated to discuss the information encoding mechanisms of semiconductor QD based qubits and the requirements that make QD electron spin qubits suitable for quantum computing, namely the DiVincenzo criteria. By information coding mechanisms we mean the physical property used to represent the quantum states $|0\rangle$ and $|1\rangle$ and their superpositions.

The main options consist in using nuclear or electronic spin states (spin qubits) and spatial charge configurations (charge qubits).

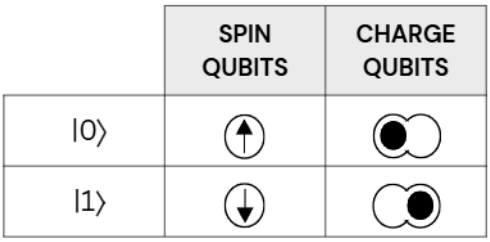


Figure 1.8: Quantum information encoding mechanism for spin (left) and charge (right) quantum-dot qubits.

1.5.1 Electron charge qubits

In electron charge qubits, information is encoded by the electron delocalization in a quantum dot structure. In a double quantum dot (DQD) configuration, such as the one shown in Figure 1.9, the two quantum states correspond to the presence of an electron in the left quantum dot ($|L\rangle$) or the right one ($|R\rangle$):

$$|\psi\rangle = p_L|L\rangle + p_R|R\rangle \tag{1.8}$$

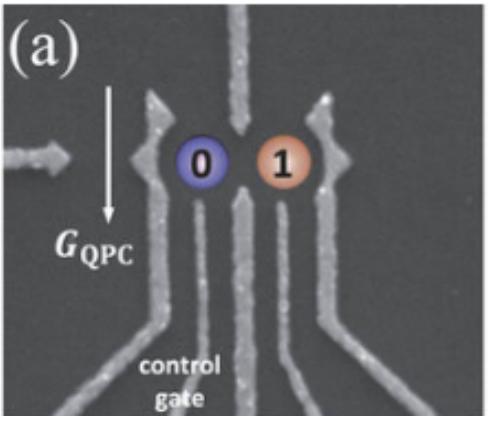


Figure 1.9: Structure of a DQD qubit with a quantum point contact (QPC) current measurement system [5]: the movement of an electron from the left dot to the right one or vice versa causes a local change in charge, which in turn leads to an increase or decrease in the QPC current. The central gate is used to tune the height of the barriers between the dots, thus controlling the coupling between the two states by changing the overlap integral of the system.

In a DQD (double quantum dot) structure, the qubit state can be controlled by tuning the system's detuning energy—that is, the energy difference between the two quantum dots, using dedicated gate electrodes. Interactions between different qubits can be achieved through the capacitive coupling between dots. The main advantage of this approach is that it is fast and fully electrostatic. However, charge qubits typically suffer from shorter coherence times, as they interact electrostatically with other nearby charges, such as those trapped in impurities, which are unstable and lead to fluctuations in the electric field.

An approach that provides greater robustness against decoherence is to use the spin of the charge carriers as the information encoding mechanism.

1.5.2 Electron spin qubits

In electron spin qubits the information is represented by the spin (↑ or ↓) of a single electron trapped in the QD:

$$|\psi\rangle = p_{\downarrow}|\downarrow\rangle + p_{\uparrow}|\uparrow\rangle \tag{1.9}$$

In this case, decoherence, i.e. the loss of information, is related to the spin orbit-coupling between the spin of the electron and that of the nuclei present in the material. In Silicon, this component is reduced, which is why Silicon integrated qubits are particularly attractive. In fact, spin qubits exhibit significantly longer relaxation (T_1) and dephasing (T_2) coherence times compared to charge qubits, with T_2 reaching values on the order of tens of milliseconds [26]. In the case of electron spin qubits, a strong magnetic field is applied to energetically separate the spin-up and spin-down states via Zeeman splitting. Qubit state manipulation is achieved by applying an alternating magnetic field resonant with the Zeeman energy, which induces Rabi oscillations, i.e., oscillations of the state vector along the energy axis.

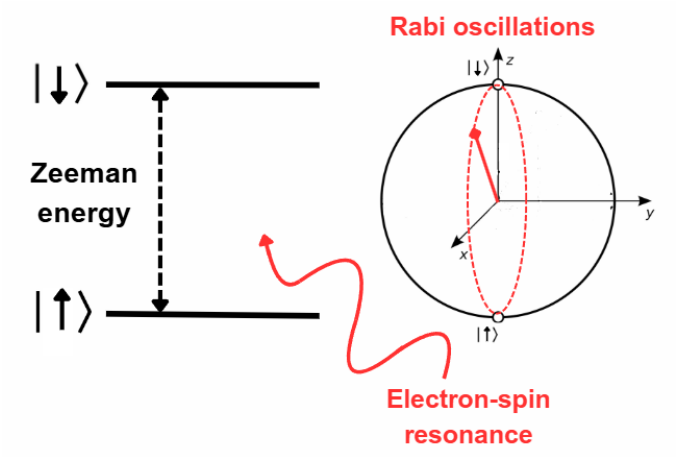


Figure 1.10: When the magnetic field is in resonance with the system's Zeeman energy, the qubit state oscillates between the spin-up and spin-down states (Rabi oscillations).

Qubits based on a single electron confined in a single quantum dot are known as Loss-DiVincenzo (LD) qubits, named after their inventors. Other more complex implementations have been proposed and are currently under validation, but they lie beyond the scope of this thesis.

1.5.3 Di Vincenzo criteria for quantum dot spin qubits

The conditions that a quantum system must satisfy in order to be suitable for quantum computation are called DiVincenzo criteria [8]. Quantum-dot based qubits satisfy each of these criteria. In the following they are discussed with reference to electron spin qubits.

1. A scalable physical system with well-characterized qubits.

   In electron spin qubits, information is represented by the spin of electrons trapped in the QD, a property that is relatively easy to manipulate. This is a scalable technology because it can exploit current lithographic techniques.

2. The ability to initialize the state of the qubits to a simple fiducial state, such as $|00\ldots0\rangle$.

An electron spin qubit can be easily initialized to the ground state (spin-up) by exploiting the charge injection from an electronic reservoir. In particular, the potential of the QD must be controlled by a specific electrode so that the Fermi level of the reservoir is intermediate between the spin-up (lower) and spin-down (higher) levels of the electron in the dot, so that the charge is injected only in the state in which it can assume spin-up (see Figure 1.12c).

3. Long decoherence times, much longer than the gate operation time.

   The decoherence time is of the order of $\sim \mu s$ (less stable than nuclear spin qubits), but they are very fast, with gates that may operate in the range of $\sim 10\ ns$, giving a ratio of ~ 100 [3].

4. A universal set of quantum gates.

   Control of a single spin qubit can be achieved through Electron Spin Resonance (ESR) [11], although selectively addressing individual qubits within an array is often challenging.

   For two-qubit operations, the $\sqrt{SWAP}$ gate, i.e. the gate that swaps the contents of two qubits, has been demonstrated, relying on the exchange interaction between spins [30]. However, to construct universal two-qubit gates, it is essential to also implement single-qubit gates, whose realization is hindered by the limited selectivity in addressing individual qubits.

5. A qubit-specific measurement capability. Single-shot measurements (Figure 1.11) have been achieved using spin-to-charge conversion mechanisms [9].

In the following, the Elzermann protocol for single-shot spin qubit read-out, presented in [9] and based on spin-to-charge conversion mechanism is presented.

1.6 Elzerman single-shot readout measurement

Figure 1.11 shows a quantum-dot spin qubit in an electrode configuration that allows the qubit state to be read in a single-shot measurement using the spin-to-charge conversion method. In this configuration the electrodes T and M control electron tunneling between the reservoir and the dot, the electrode P controls the dot potential.

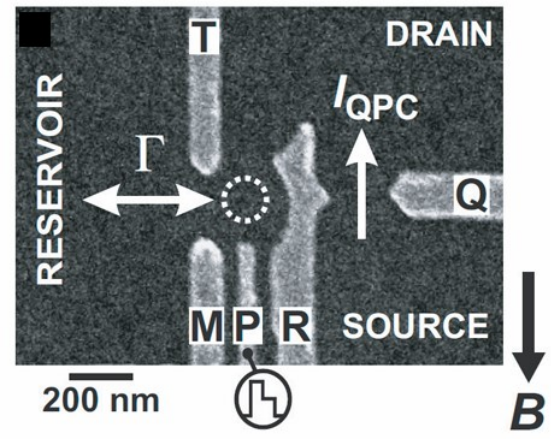


Figure 1.11: Scanning electron micrograph of a quantum-dot spin qubit in single-shot Elzerman measurement apparatus [9]. The electrodes T and M control electron tunneling between the reservoir and the dot, the electrode P controls the dot potential. The Quantum Point Contact (QPC) current is extremely sensitive to the charge in the quantum dot and can therefore detect the presence/absence of the electron

The Elzerman single-shot readout measurement exploits the separation of spin up and spin down energy levels upon application of an intense magnetic field. In particular, during the measurement a voltage ($V_P > 0$) is applied to the P electrode (which controls the dot potential) such that the Fermi level of the reservoir falls between the spin up and spin down energy levels, so that:

- if the electron has spin-down (higher energy) it tunnels into the reservoir and escapes the dot, resulting in an increase in the QPC current;
- if the electron has spin-up (lower energy) it remains in the dot, and the QPC current remains stable;

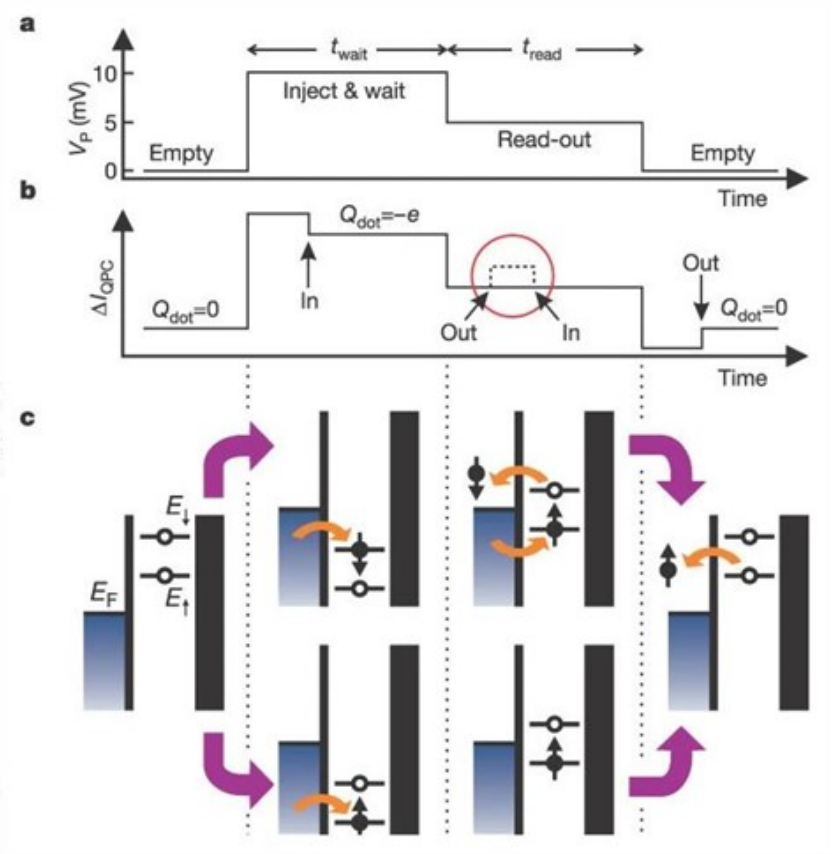


Figure 1.12: Elzerman measurement sequence for spin qubits, Injection and Read-out phases [9]. a) P-electrode voltage. b) Measured QPC current. c) Energy diagram of the quantum dot.

This method also allows the measurement of the longitudinal relaxation time T_1, i.e. the average time for a spin to flip from $\downarrow$ to $\uparrow$ in the second step, but it cannot measure the phase relaxation time T_2.

Single-charge sensors The term Elzerman readout refers to the specific protocol for spin readout that relies on spin-to-charge conversion. This mechanism is based on projecting the quantum information from a spin degree of freedom onto a charge degree of freedom, which is essential because measuring the spin of a single electron is challenging due to its magnetic moment being much smaller than the strong magnetic fields applied to achieve the Zeeman splitting. The detection of the charge state associated with the

spin configuration can be achieved using various charge sensors with single-electron sensitivity. The main three are:

- Quantum Point Contact (QPC) charge sensor. A quantum point contact (QPC) is a constriction between two conducting regions having dimensions comparable to the electron wavelength (nm). The current flowing through this constriction, i.e., the QPC current, is extremely sensitive to charge and can detect the presence or absence of even a single electron.
- Dispersive radiofrequency reflectometry. The system is coupled to a radiofrequency (RF) resonator, and variations in the phase and/or amplitude of the reflected signal are monitored, which are sensitive to the charge of a single electron. It is a non-invasive technique because no current is passed directly through the device.
- Single-Electron Transistors (SETs). These are quantum-dot based transistors, whose current can be modulated by the addition of a single charge in the dot.

It is important to note that the RF resonator-based approach requires a complex but external setup, whereas the SET- and QPC-based approaches require additional space on the device, since the sensors must be manufactured close to the spin qubit. This added footprint poses a limitation to the scalability of the chip.

The objective of this thesis is to develop compact simulations aimed at guiding and optimizing the fabrication process of Single-Electron Transistors (SETs) for spin qubit readout, currently under development at IMB-CNM. Establishing a reliable SET fabrication process represents the first step toward the implementation of a silicon quantum dot-based qubit architecture for quantum computation.

Chapter 2

Single-Electron Transistor

2.1 Introduction

As stated by the DiVincenzo criteria, the ability to read out the quantum state is one of the key requirements for the physical realization of a quantum bit, along with its initialization, control, and the coherent manipulation of single or multiple units.

The spin-to-charge conversion mechanism maps the measurement of the electron's magnetic moment, difficult to detect, onto a charge measurement. A Single-Electron Transistor (SET) can serve as a highly sensitive charge sensor. In this chapter, we briefly recall the theory behind the SET and introduce the concept of gate-defined SETs, which represent the most suitable implementation to fully leverage the manufacturing capabilities of CMOS technology.

A Single-Electron Transistor consists of a conductive island separated from carrier reservoirs by insulating barriers through which charges can tunnel and a dedicated gate that can control the potential of the island [17]. Figure 2.1a shows a schematic of a generic SET, while Figure 2.1b shows the capacitive model of the device.

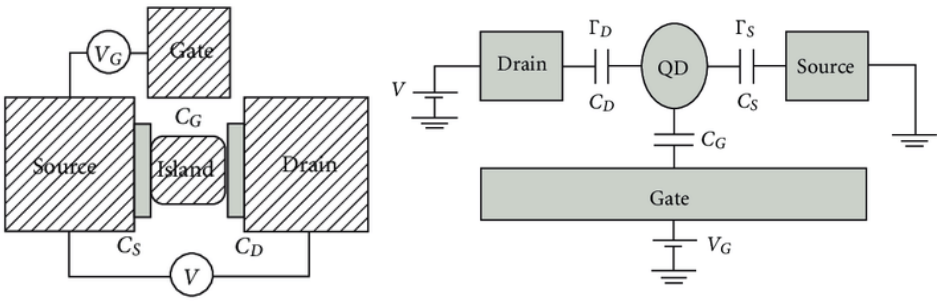


Figure 2.1: a) Schematic and b) capacitive model of a generic Single-Electron Transistor [17]. C_D, C_S, and C_G represent the capacitances associated with the Drain, Source, and Gate junctions, respectively. V is the drain-to-source voltage, and V_G is the gate voltage.

Before discussing the physical principle underlying the single-electron transistor, it is worth talking about the charging effects, first observed by Fulton and Dolan [13] in 1987, on a simple structure consisting

of a single common electrode connected to three vertical electrodes, forming three electron tunneling junctions.

2.2 Charging effects and Coulomb Blockade

Charging effects can occur in structures consisting of a small conductive island connected by resistors to big reservoirs, i.e., macroscopic pieces of metals. In this type of structure the charge inside the conductive island is quantized, since it is small and well separated from the reservoirs. The charge in the conductive island can therefore be written as a multiple of the elementary charge:

$$Q = ne \tag{2.1}$$

where n is the number of charges in the island and e is the elementary charge.

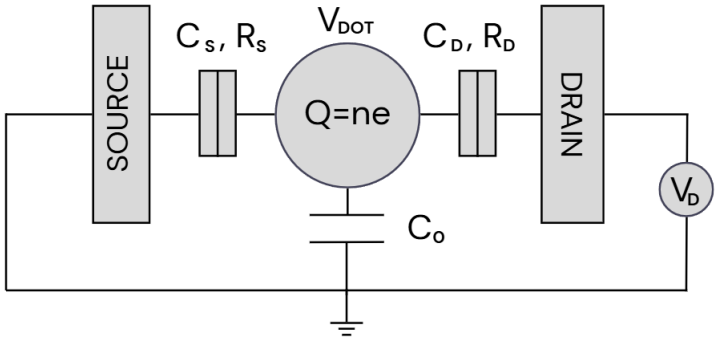


Figure 2.2: Schematic of a generic structure exhibiting charging effects. A conductive island isolated from big charge reservoirs, namely Source and Drain.

The electrostatic energy stored in the dot is given by:

$$E_C = \frac{e^2}{2C_\Sigma} n^2 \tag{2.2}$$

where C_Σ is the total capacitance of the island and is given by the sum of the various capacitive contributions:

$$C_\Sigma = C_S + C_D + C_0 \tag{2.3}$$

C_S and C_D are the capacitances associated with the junctions to the Source and Drain reservoirs, respectively, while C_0 is the stray capacitance, i.e., a parasitic capacitance intrinsic to the conductive island that depends on its geometry. In general, the smaller the island, the smaller the value of C_0.

The total capacitance of the island therefore provides a measure of how much its potential changes upon the addition of a single charge. Since the island is very small, the addition of a single electron introduces a significant amount of electrostatic energy, called charging energy, given by:

$$E_C = \frac{e^2}{2C_\Sigma}(n+1)^2 - \frac{e^2}{2C_\Sigma} n^2 \Longrightarrow E_C = \frac{e^2}{2C_\Sigma} \tag{2.4}$$

This implies that, in order to be effectively included in the island, the charge must have enough energy to overcome this repulsive contribution. If this condition is not met, charge transport is suppressed — a

phenomenon known as Coulomb Blockade. It is straightforward to see that, in order to observe Coulomb blockade, the thermal energy must be much smaller than the charging energy:

$$k_B T \ll E_C \tag{2.5}$$

Theoretically, an additional amount of energy should be added to the expression of the charging energy in 2.4, due to the quantization of energy levels in the island caused by its small dimensions. However, in gate-defined SETs, the island dimensions are typically on the order of tens of nanometers, which corresponds to energy level spacings in the neV range, small even compared to the thermal energy of ultra-low temperature devices operating in the millikelvin regime, so it is a contribution that can be neglected.

2.2.1 Resistance Requirement

As previously mentioned, in order to observe charging effects, the conducting island must be well isolated from the charge reservoirs. To quantify the required resistance of the tunnel barriers, we use the Heisenberg uncertainty principle, which states that the product of the uncertainty in energy and the uncertainty in time must satisfy:

$$\Delta E \cdot \Delta t > \hbar \tag{2.6}$$

In the case of a charge/discharge event:

- Δt is the average charging/discharging time of the island, which is related to the total capacitance C_Σ and the tunnel resistance R by:
$$\Delta t = R C_\Sigma \tag{2.7}$$
- ΔE is the energy variation during the event, which corresponds to the charging energy of the device:
$$\Delta E \approx \frac{e^2}{C_\Sigma} \tag{2.8}$$

Substituting into the uncertainty relation:

$$\Delta E \cdot \Delta t = \frac{e^2}{C_\Sigma} \cdot R C_\Sigma > \hbar \quad \Longrightarrow \quad R > R_Q \cong \frac{\hbar}{e^2} = 25 \text{ k}\Omega \tag{2.9}$$

Therefore, another requirement for observing the Coulomb blockade effect is that the tunnel resistance must be greater than the quantum of resistance $R_Q \cong \hbar/e^2 = 25$ kΩ.This is why SETs often use tunneling junctions, so as to keep the quantum dot isolated while still allowing current to be detected.

2.3 Single Electron Transistor

In a single-electron transistor, the conductive island is separated from the source and drain reservoirs by tunneling barriers, and a dedicated electrode, the gate electrode, allows control of the island's potential.

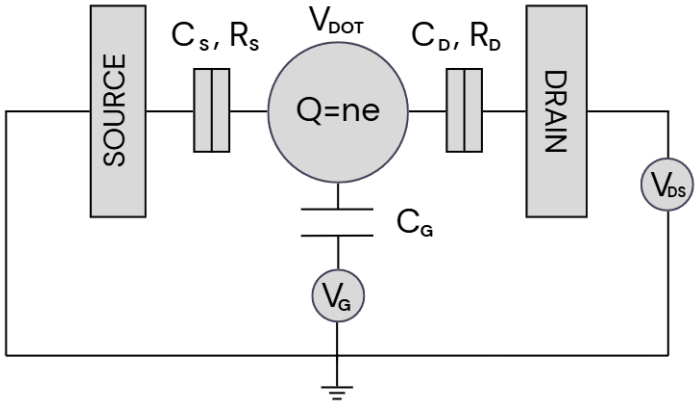


Figure 2.3: Schematic of a generic Single Electron Transistor.

Figure 3.13 shows the capacitive model of a SET. From this, it is possible to calculate the charge present on the island as a function of the applied voltages as:

$$Q = C_S V_{DOT} + C_D \left(V_{DOT} - V_{DS}\right) + C_G \left(V_{DOT} - V_G\right) \tag{2.10}$$

Consequently, the electrostatic energy of an electron at the QD can be written as:

$$U_{DOT} = -qV_{DOT} = -q\overbrace{\left(\frac{C_D}{C_\Sigma}V_{DS} + \frac{C_G}{C_\Sigma}V_G\right)}^{Vext} + \frac{Q}{C_\Sigma} \tag{2.11}$$

Where $C_\Sigma = C_S + C_D + C_G$. The first term relates to the effect of the applied external voltages, while the second is the charging effect due to the charges present in the dot. While the expression for the electrostatic energy of the dot system, consisting of N electrons, can be obtained by considering the energy required to charge the dot with N electrons and changing the applied voltage, this corresponds to calculating the integral:

$$U_{ES}(N) = \int_{Q=0,V_{ext}=0}^{-Ne,V_{ext}} \left(V_{DOT}dQ + QdV_{ext}\right) = \frac{(Ne)^2}{2C} - NeV_{ext} \tag{2.12}$$

From this expression, it is possible to derive the electrochemical potential of the dot, i.e., the energy an electron must have to enter the system. Obviously, it depends on the number of charges present in the dot and is given by the difference in electrostatic energy between the system with N electrons and the system with N-1 electrons:

$$\mu(N) = U_{ES}(N) - U_{ES}(N-1) = \left(N - \frac{1}{2}\right)\frac{e^2}{C_\Sigma} - eV_{ext} \tag{2.13}$$

It is easy to verify that the difference in energy between the electrochemical potentials is always constant and equal to:

$$\mu(N) - \mu(N-1) = 2E_C = \frac{e^2}{C_\Sigma} \tag{2.14}$$

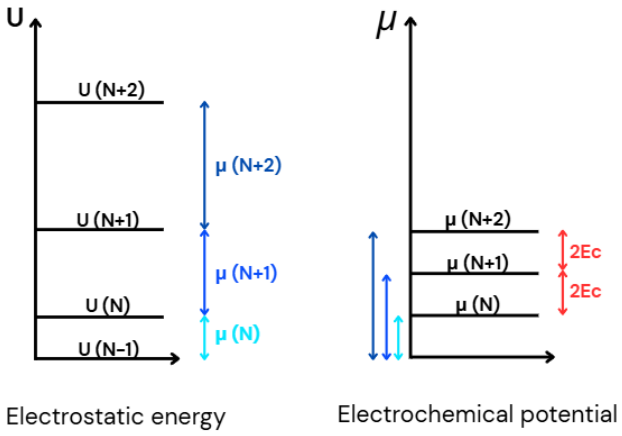


Figure 2.4: Graphical representation of the relationship between the electrostatic energy of the island and the electrochemical potential, or the energy an electron must have to enter the system.

Therefore, to enable conduction, external voltages must be applied such that the electrochemical potential of the dot lies within the Fermi bias window. Otherwise, due to charge quantization caused by the small size of the island, no conduction occurs (Coulomb blockade), because there are no electrons with sufficient energy in the reservoirs to enter the dot, and none in the dot to exit and reach the reservoirs.

$$\mu_S \geq \mu(N) \geq \mu_D \tag{2.15}$$

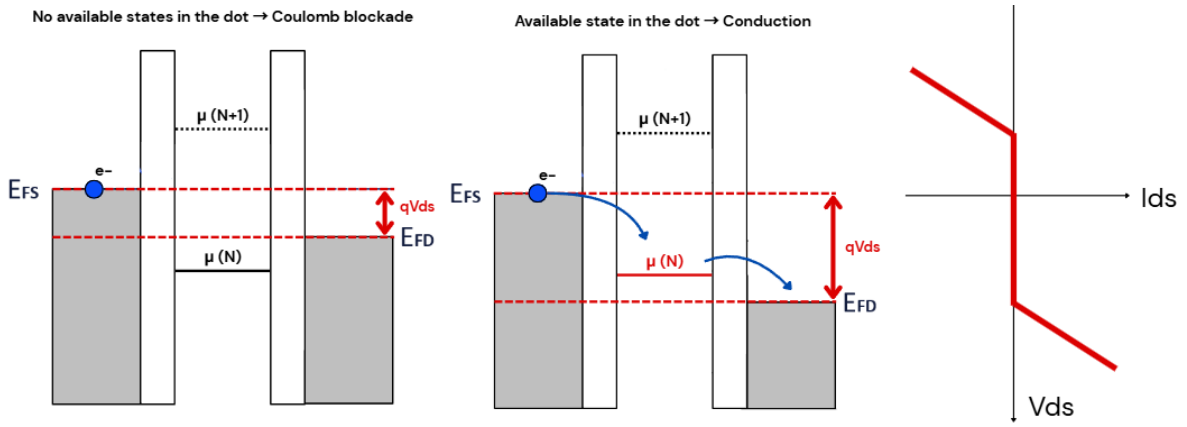


Figure 2.5: Energy diagram of a SET. Due to the discretization of charges in the conductive island, for low values of V_{DS} there are no states available for conduction. When the Fermi bias window includes the electrochemical potential of the island, conduction is activated.

The main advantage of Single-Electron Transistors (SETs) lies in the possibility of having a dedicated gate electrode that allows precise control over the potential of the conductive island.

By applying a voltage to the gate electrode, the electrochemical potential of the quantum dot can be shifted, enabling a transition from the Coulomb blockade regime—where conduction is suppressed—to a

state where current can flow. This gate control also allows for accurate tuning of the number of electrons on the island, down to the level of a single charge.

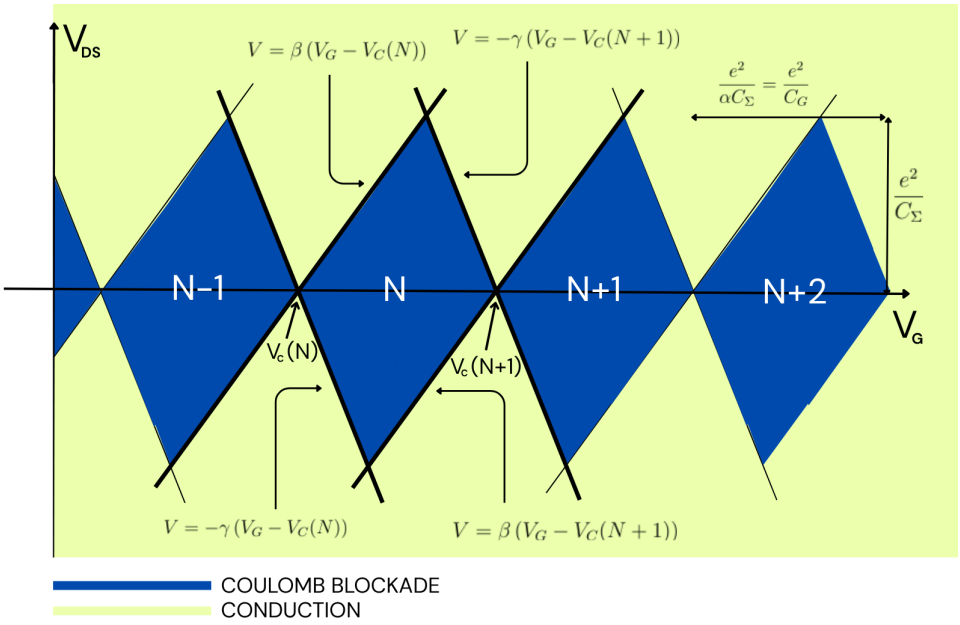


Figure 2.6: Coulomb diamonds. For specific combinations of voltages, periodic with respect to the gate voltage, the device enters the Coulomb blockade regime, in which no current flows. This results in the appearance of diamond-shaped regions, known as Coulomb diamonds, in a V_{DS} vs V_{gate} diagram, where the current is blocked.

Figure 2.6 shows a typical V_{DS}–V_G plot of a SET, displaying diamond-shaped regions where the current is suppressed—the Coulomb diamonds. There are several important features to highlight. First, these regions are periodic with respect to the gate voltage, with a period given by $e^2/\alpha C_\Sigma$, where:

$$\alpha = \frac{C_G}{C_\Sigma} \tag{2.16}$$

Moreover, the slopes of the diamond edges depend on the capacitive coupling between the island and the electrodes. In particular, with reference to the figure:

$$\beta = \frac{C_G}{C_G + C_D} \tag{2.17}$$

$$\gamma = \frac{C_G}{C_S} \tag{2.18}$$

It is straightforward to verify that the three coefficients are related by the expression:

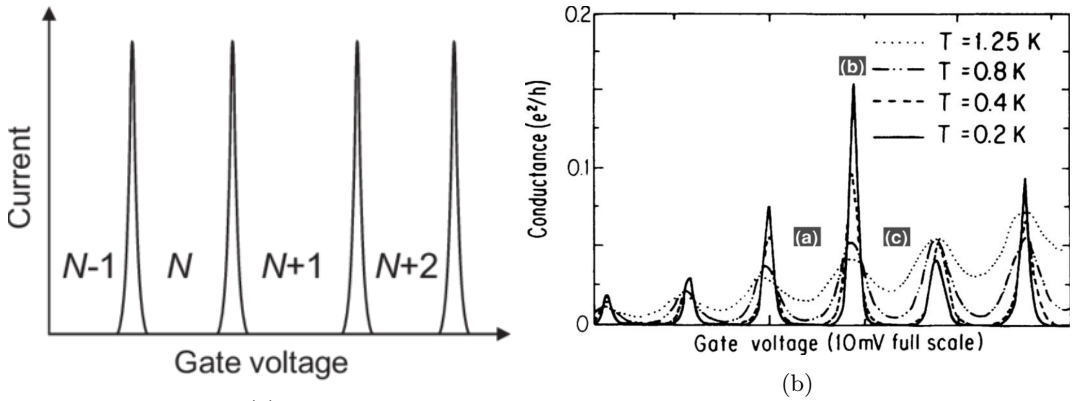
$$\frac{1}{\alpha} = \frac{1}{\beta} + \frac{1}{\gamma} \tag{2.19}$$

Therefore, if the Coulomb diamonds are not symmetric, this indicates that the capacitive coupling between the island and the source/drain contacts is asymmetric, i.e., the island is more strongly coupled to one of the two electrodes.

Furthermore, as long as the island capacitances do not depend on the number of electrons, the Coulomb diamonds will have uniform size. However, as the electron population in the dot increases, the total capacitance of the island can change, leading to smaller diamonds at higher gate voltages.

2.3.1 Coulomb peaks

If the drain-to-source voltage is kept constant and close to zero, sweeping the gate voltage results in a conductance profile characterized by current-blocked regions with a well-defined number of charges, and sharp periodic conductance peaks, known as Coulomb peaks, where the number of charges in the dot fluctuates and current can flow.



(a) (b)

Figure 2.7: Coulomb peaks correspond to gate voltage values for which the conduction is activated and the number fo charges in the islands fluctuates. a) Drain-to-source current as a function of gate voltage, at a constant and very small V_{DS}, taken from [10]. b) Degradation of the Coulomb peaks with Temperature [32].

Figure 2.7b shows how, as the temperature increases, the well-defined and sharp Coulomb peaks begin to degrade, turning into broader oscillations. This feature makes SETs particularly interesting as temperature sensors, as it is possible to establish a correlation between the amplitude of the Coulomb peaks and the temperature.

However, the most relevant application in the context of quantum computing based on semiconductor platforms is undoubtedly the use of the SET as a charge sensor. When embedded in a radio-frequency circuit, the SET is currently the most sensitive charge detector available [13, 34], and it has been shown to be capable of detecting real-time electron tunneling events on a sub-microsecond timescale [23].

2.4 SETs for charge sensing

As previously discussed, due to the small dimensions of the conductive island in a SET, the addition of a single charge significantly alters its potential, introducing a non-negligible electrostatic energy contribution.

Figure 2.8 shows the Coulomb diagram of a metal-nanoparticle-based SET [4], which displays broken Coulomb diamonds. This phenomenon occurs because individual external charges can approach the conductive island, thereby modifying its potential. As a result, the Coulomb diamonds shift along the gate voltage axis, during the measurment.

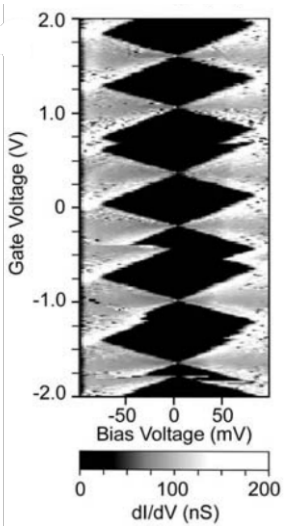


Figure 2.8: Coulomb diagram of a metal-nanoparticle-based SET showing the effect of an external charge perturbing the potential of the quantum dot, resulting in a shift of the Coulomb diamonds [4].

Consequently, by selecting the appropriate combination of voltages, it is possible to detect the presence or absence of an external charge based on whether current flows through the device.

2.4.1 SETs for spin-to-charge conversion based read-out of spin qubits

The work presented in [26] demonstrates, for the first time, single-shot, time-resolved readout of an electron spin in silicon using a gate-defined SET. In this study, the electron spin qubit is based on phosphorus atoms implanted in a 90 nm $\times$ 90 nm region, with a fluence optimized to maximize the probability of having three donor atoms located approximately 30–60 nm from the conductive island of a gate-defined Metal-Oxide-Semiconductor SET. A plunger gate electrode is used to control the potential of the qubit.

The readout protocol follows the Elzermann scheme, presented in Section 1.6. It consists of three main phases:

1. LOAD phase: The potential of the qubit is tuned via the plunger gate such that both spin-up and spin-down energy levels lie below the electrochemical potential of the SET dot. As a result, an electron tunnels from the SET dot to the qubit, occupying one of the two spin states.

2. READ phase: A suitable positive voltage is applied to the plunger gate so that the electrochemical potential of the SET dot lies between the spin-up and spin-down energy levels of the qubit. Depending on the spin state of the electron, it may or may not tunnel back into the SET dot (spin-dependent tunneling). A tunneling event results in the addition of a charge to the SET island, shifting its potential and transitioning the system from a Coulomb blockade regime to a conductive regime. This transition is detected as a current peak in the SET signal, which lasts for a characteristic time before the spin-up electron relaxes and tunnels back into the qubit as a spin-down electron.

3. EMPTY phase: The voltage applied to the plunger gate is set such that both spin-up and spin-down states lie above the SET dot electrochemical potential. Therefore, regardless of the electron's spin state, the qubit is emptied.

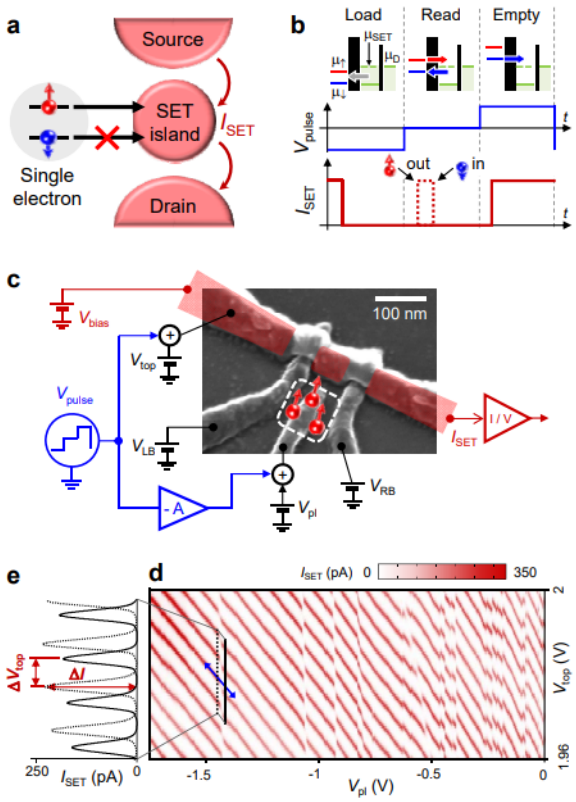


Figure 2.9: Protocol for spin-to-charge conversion based spin qubit readout [26]. a) Schematic of the measurement setup, where the qubit is tunnel-coupled to the conducting island of a SET. b) Three-phase protocol for qubit state readout. c) Circuit diagram of the measurement system, including an SEM image of the qubit and the SET. d) Shift in Coulomb peaks resulting from the addition of a charge to the SET island at a plunger gate voltage of approximately $V_{\mathrm{pl}} \approx -1.4$ V. e) Plot of the SET current as a function of the top gate voltage V_{top}, which controls the island potential, and the plunger gate voltage V_{pl}, which controls the qubit potential. The breaks in the Coulomb peak lines correspond to the addition of an external charge.

Figure 2.9d shows a plot of the SET current as a function of different combinations of the top gate voltage V_{top} and the plunger gate voltage V_{pl}. Each horizontal slice at a fixed V_{pl} corresponds to a trace of Coulomb peaks as a function of V_{top}. Notably, discontinuities in the Coulomb peak lines appear in the plot. These breaks are due to shifts in the island potential caused by the addition of external charges.

In particular, the transitions observed for $V_{\mathrm{pl}} > -0.7$ V are unstable and are most likely caused by trapped charges at the Si/SiO_2 interface. On the other hand, the stable transitions observed for $V_{\mathrm{pl}} < -0.7$ V are attributed to single charges tunneling from the qubits.

Figure 2.9e shows the Coulomb peaks measured at one of the transitions discussed above, specifically at $V_{\mathrm{pl}} \approx -1.4$ V. The shift in the peak positions is directly related to the added charge, and can be expressed as:

$$\Delta V_{\mathrm{top}} = \frac{\Delta q}{C_{\mathrm{top}}} \tag{2.20}$$

where Δq is the change in charge sensed by the SET, and C_{top} is the capacitance between the conductive

island and the top gate.

Measurement of the Relaxation Time T_1 As previously mentioned in the discussion of the Elzermann read-out, this method allows the measurement of the longitudinal relaxation time T_1 of the qubit, that is, the average time it takes for an electron in the spin-up state to relax into the lower-energy spin-down state.

This is done by measuring the probability $P_\uparrow$ of detecting a spin-up electron as a function of the waiting time τ_W, i.e., the time during which the system is held in the *load* phase. The time T_1 characterizes the decay rate of this probability, which follows an exponential trend:

$$P_\uparrow(\tau_W) = P_\uparrow(0) \exp\left(-\frac{\tau_W}{T_1}\right) \tag{2.21}$$

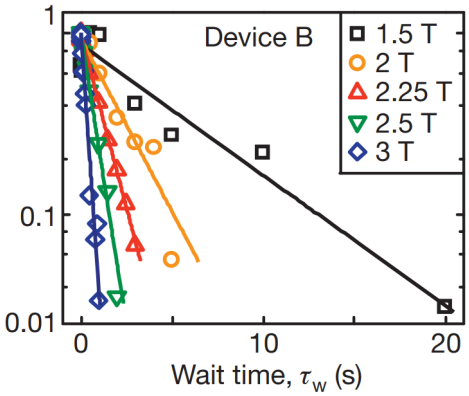


Figure 2.10: Normalized probability of the spin-up state as a function of the waiting time τ_W [26].

Figure 2.10 shows the experimentally measured decay of the spin-up probability for different values of the applied magnetic field. A relaxation time T_1 of up to 6 seconds was achieved for an applied field of 1.5 T. The readout fidelity exceeds 90% for both spin states.

2.5 Gate-Defined SETs

The simplest way to integrate a SET into a semiconductor platform for quantum computing is to use gate-defined Metal-Oxide-Semiconductor SETs, as they take advantage of the manufacturing capabilities that have been optimized over the years to achieve high integration density and scalability for MOSFET-like devices.

In a gate-defined SET, the conductive island is separated from the source and drain regions by barrier gates that locally deplete charges. Figure 2.11a, taken from the work presented in [1], shows a device based on a MOSFET structure with additional gates, namely the barrier gates, placed between the main gate (from now on referred to as the lead gate) and the silicon oxide layer, used as the gate oxide. The intermetal dielectric separating the barrier gates and the lead gate is aluminum oxide, formed as a result of the thermal oxidation of the aluminum barrier gates.

The device is an n-type FET fabricated from a near-intrinsic substrate, with phosphorus-implanted regions used to create the source and drain wells.

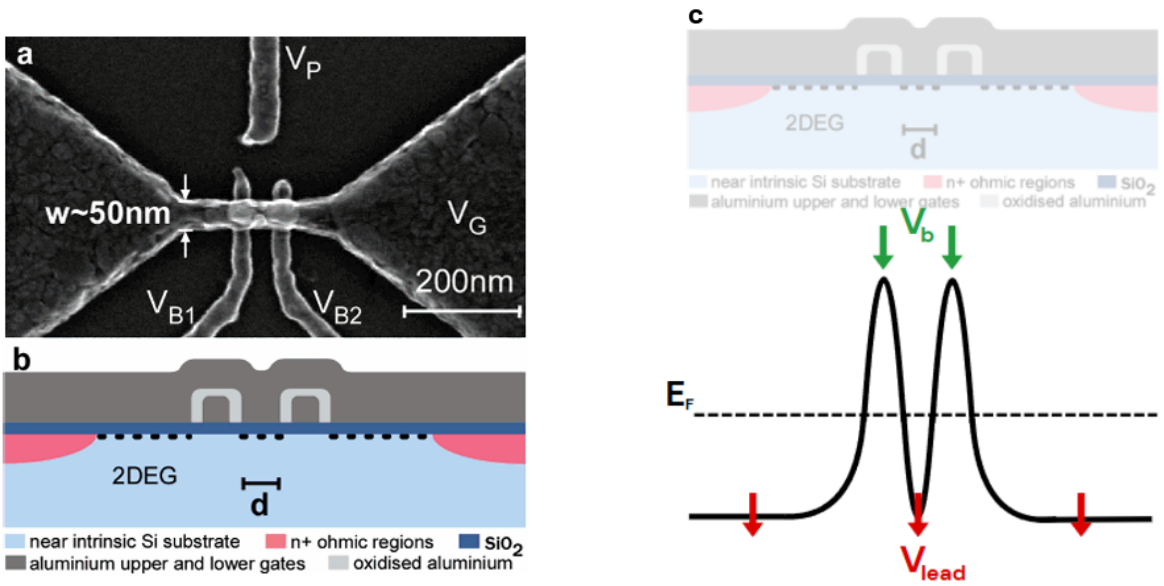


Figure 2.11: a) SEM image of a typical device [1]. b) Schematic cross-section of the channel of the device showing the depletion induced by the barrier gates [1]. (c) Schematic of the band diagram along the channel. The voltage V_{lead} applied to the lead gate is responsible for the formation of the channel and for controlling the quantum dot potential, while the voltage V_b applied to the barrier gates controls the height of the potential barriers.

The lead gate functions as the gate of a conventional MOSFET; thus, above a certain voltage ($V_{\text{lead,th}}$), it creates a thin inversion layer of charges (a two-dimensional electron gas, 2DEG) at the oxide interface, enabling conduction. If the barrier gates are kept below their threshold voltage ($V_{b,\text{th}}$), the channel beneath them is depleted of charges, thereby confining electrons in the center and isolating the quantum dot from the source and drain regions. In terms of the band diagram, this corresponds to the formation of potential barriers in the conduction band (see Figure 2.11c).

By applying increasingly positive voltages to the barrier gates, the potential barriers are lowered, and beyond a certain value the device behaves as a conventional MOSFET, as the channel becomes continuous.

As we will see in more detail in the following chapters, at room temperature the barriers are not able to effectively cut off the channel, especially in structures that are not isolated from the substrate, whereas at millikelvin temperatures they are, and the device enters conduction very abruptly. Figure 2.12 shows the voltage window for which the device is conductive, namely when $V_{\text{lead}} > V_{\text{lead,th}}$ and $V_b > V_{b,\text{th}}$. The white rectangle highlights the region where Coulomb blockade is observed; this occurs for barrier gate voltages near their threshold value. In this regime, the Fermi level of the contacts aligns with the top of the potential barriers, where they are thinner and allow electrons to tunnel in and out of the quantum dot.

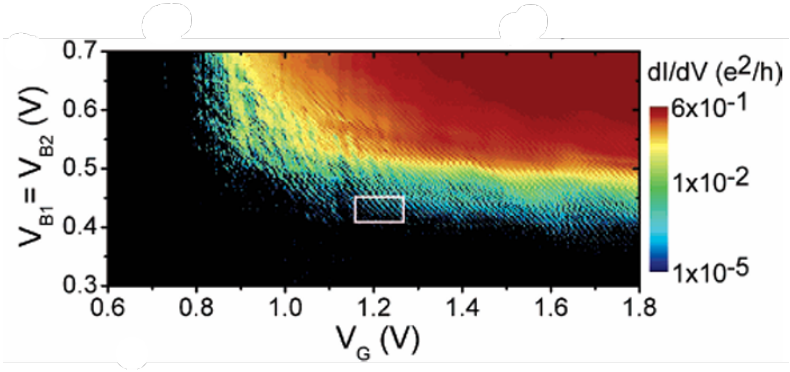


Figure 2.12: Voltage window for which the device is conductive. Single electron effects are observed near the threshold voltage of the barriers, i.e., for $V_b \approx 4.3$ V.

Figure 2.13 shows the Coulomb diamonds obtained for this device. From the size of the diamonds, a total capacitance C_Σ of 64 aF and a gate capacitance C_G equal to 20 % of the total capacitance (i.e., 13 aF) are extracted. A total capacitance of 64 aF corresponds to a charging energy of 1.25 meV. In order to observe Coulomb blockade effects, the thermal energy must be much smaller than this value, meaning the temperature must satisfy $T \ll 14$ K.

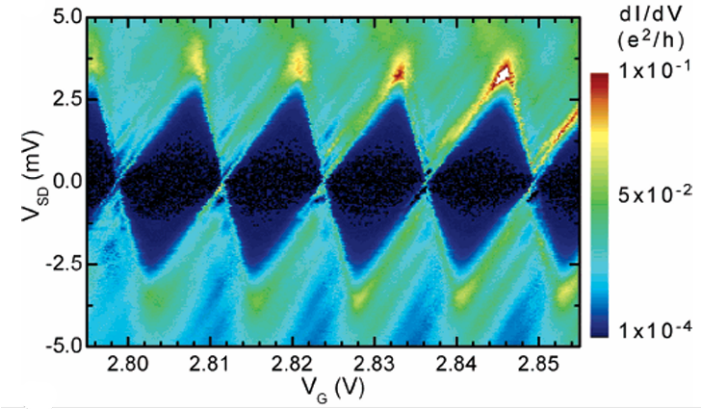


Figure 2.13: Coulomb diamonds observed in a device with a dot area of 30 nm × 105 nm [1].

Chapter 3

IMB-CNM Fabrication Processes

This chapter presents the fabrication processes developed by the NANONEMS group at the Institute of Microelectronics of Barcelona (IMB-CNM, CSIC) for gate-defined SET devices. In particular, two types of structures will be discussed.

Figure 3.1a shows a device based on a Fully Depleted Silicon-On-Insulator (FDSOI) nanowire FET, featuring multiple gates along the channel to achieve carrier confinement. The nanowire is patterned from the silicon overlayer of a SOI wafer, while the gates are deposited via lift-off in a single metal layer.

Figure 3.1 illustrates an alternative approach based on a planar MOSFET, fabricated from a lightly doped silicon wafer. In this case, the barrier gates are deposited first to enable channel depletion, followed by a lead gate deposited on top, which defines the conductive channel.

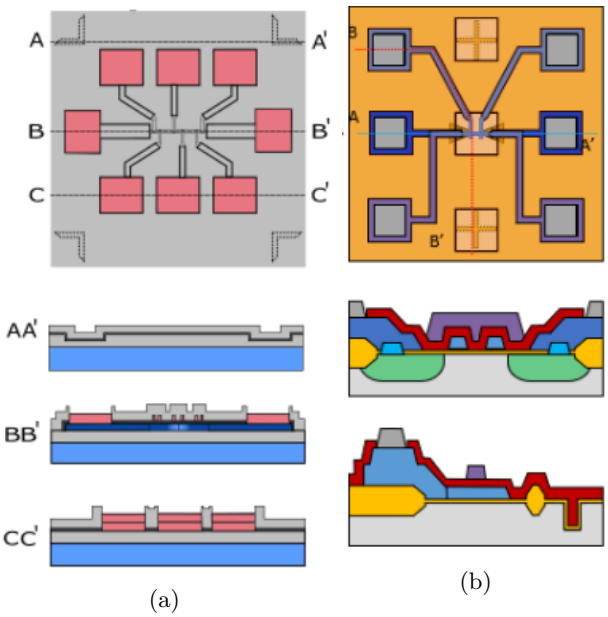


Figure 3.1: a) Schematic of the FDSOI Nanowire SET with multiple gates. b) Schematic of the planar SET device.

3.1 FDSOI Nanowire SET fabrication process

The fabrication process of the nanowire-based structure begins with a SOI wafer composed of a 50 nm-thick silicon overlayer, a 400 nm-thick buried oxide (BOX) layer, and a 700 μm-thick silicon substrate. The patterning of the devices is carried out using a mix-and-match ($M\&M$) lithography process: conventional optical lithography is used for defining large, less critical features, while high-resolution techniques such as electron beam lithography (EBL) are employed for the smaller, critical structures — namely, the nanowire and the gates. The following steps summarize the main stages of the fabrication process, which was carried out by Ziyin Sun, whose work is presented in [38].

Transferring alignment marks Alignment marks are defined using optical lithography ($OL\#1$) followed by etching of both the silicon and silicon dioxide layers. These marks are essential for ensuring proper alignment in subsequent lithographic steps. A positive photoresist, 6512, is used for this purpose; in this type of resist, the exposed areas become soluble in the developer solution.

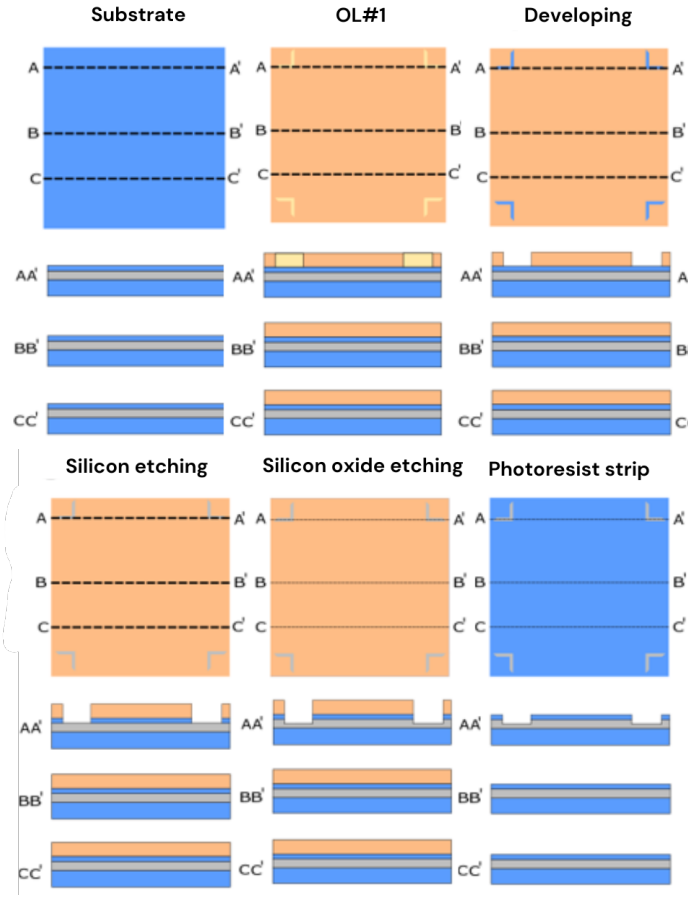


Figure 3.2: Transferring alignment marks.

Mix&Match process for nanowire patterning The photoresist 7520, a negative resist that becomes insoluble upon exposure, is sequentially exposed using an optical lithography step ($OL\#2$) to define the nanowire leads, followed by an electron beam lithography (EBL) step to pattern the nanowire itself.

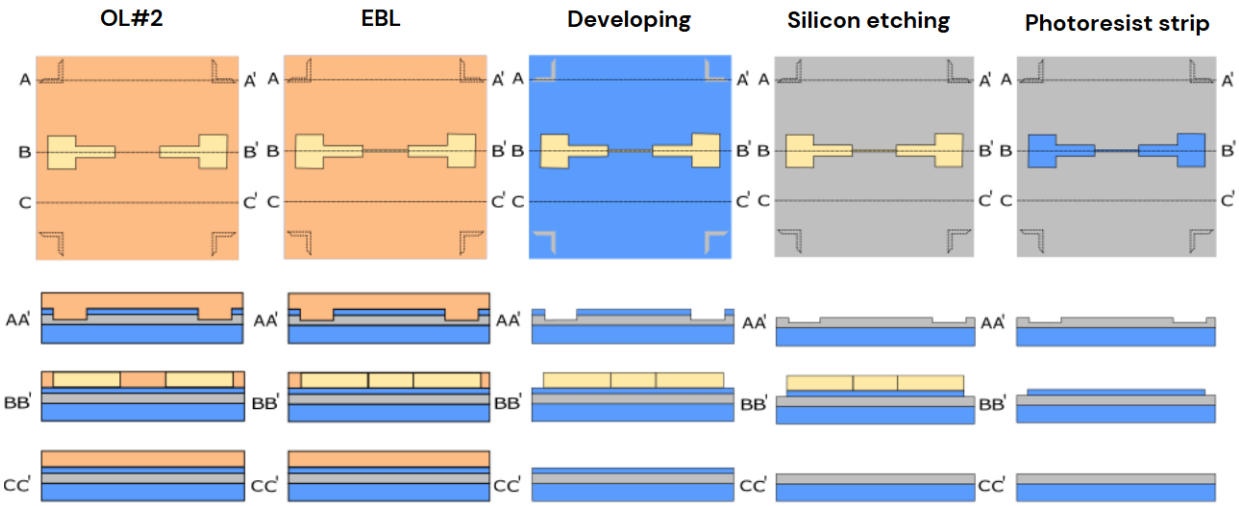


Figure 3.3: Mix&Match process for nanowire patterning.

The mix-and-match ($M\&M$) approach enables the combination of the speed and ease of optical lithography with the high precision and resolution of EBL, restricting the use of the latter to the most critical areas only.

Gate oxide growth and S/D implantation A thin silicon oxide layer (6.5 nm) is thermally grown via dry oxidation, ensuring high dielectric quality and interface integrity. The negative photoresist 7520 is patterned through optical lithography ($OL\#3$) to create a protective mask that shields the channel region during the subsequent implantation step. This mask prevents dopants from reaching the channel, allowing selective doping of the source and drain (S/D) reservoirs only. Two different implantations are performed: one with phosphorus atoms (with energy = 15 keV and dose = 2×10^{14} atoms/cm^2) to obtain n-type devices, and another with boron atoms (with energy = 7 keV and dose = 2×10^{14} atoms/cm^2) for p-type devices.

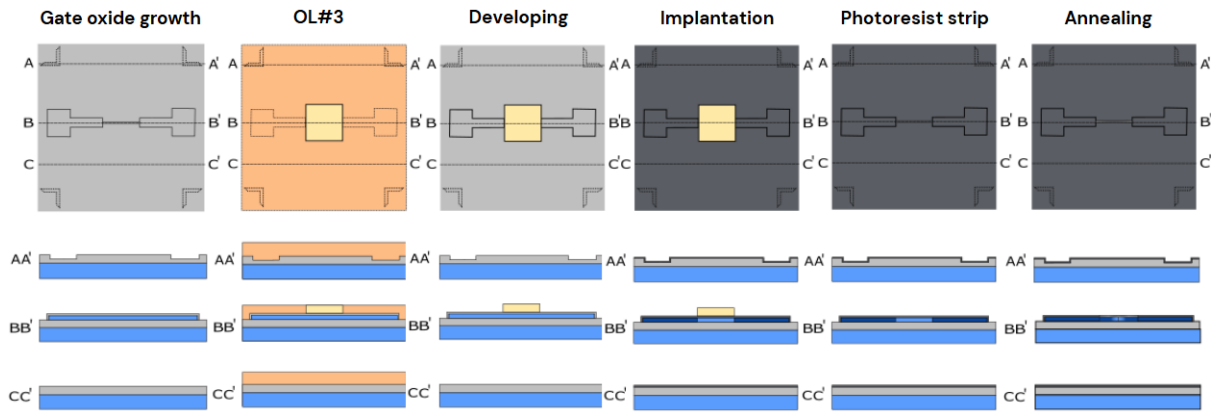


Figure 3.4: Gate oxide growth and S/D implantation.

Metal pads deposition The metal pads are deposited using a lift-off technique assisted by a Lift-Off Resist (LOR). This is necessary to achieve a cleaner lift-off and to avoid issues that may arise from the deposition of continuous metal films. For this reason, the LOR is deposited before the positive photoresist. The photoresist is then exposed in correspondence with the metal pad areas and developed. During this phase, the exposed regions of the LOR dissolve laterally, creating undercuts that prevent the formation of continuous films during the metal deposition step. Aluminum is then deposited by evaporation, followed by a lift-off process. Finally, a thermal treatment in a reducing atmosphere, known as Forming Gas Anneal (FGA), is carried out to form more stable, robust, and low-resistance contacts, and to improve the quality of the metal interface.

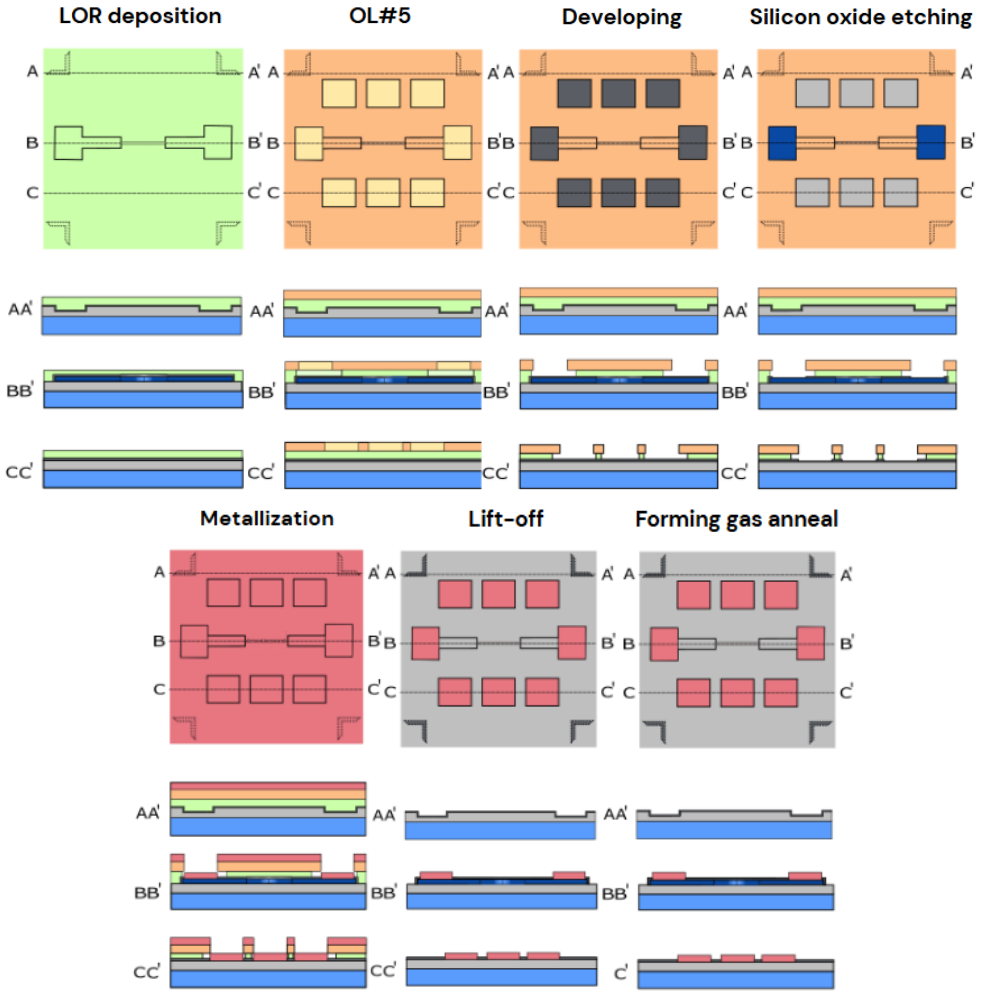


Figure 3.5: Metal pads deposition.

Metal gates deposition The gates are patterned using EBL and defined via a lift-off process: aluminum is uniformly deposited by thermal evaporation onto the surface of the photoresist (PMMA, positive) and on the exposed areas of the device (corresponding to the gate pattern). The photoresist is then stripped away, leaving aluminum only in the regions defined by the gate geometry. It is important

to note that EBL is used at this stage only for the critical regions — that is, the smaller gate features in contact with the nanowire. The larger gate tracks and contact pads are instead patterned using an additional optical lithography step.

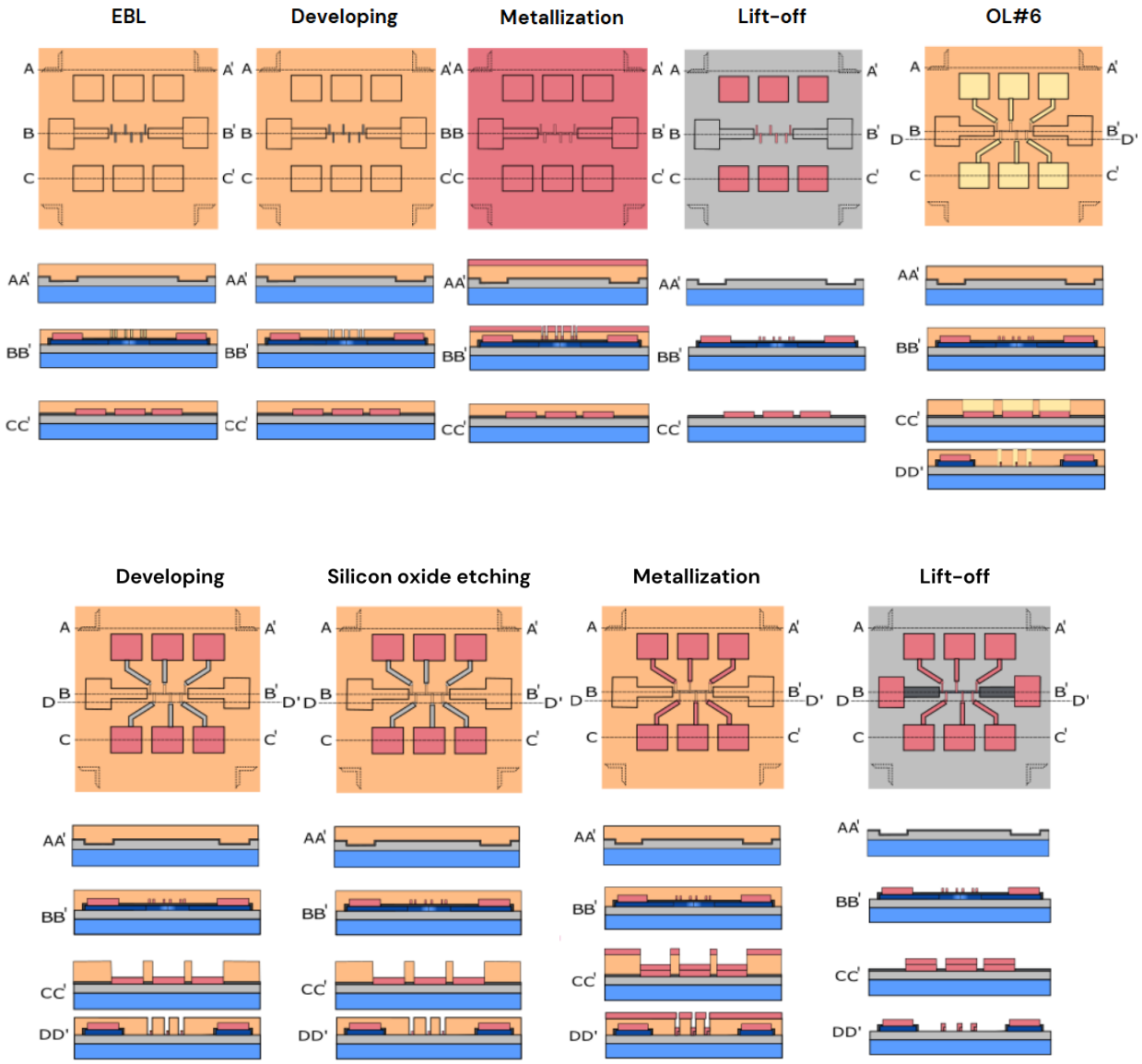


Figure 3.6: Metal pads deposition.

Metal contacts opening Finally, a passivation layer is deposited to protect the device. Therefore, in order to electrically characterize it, the metal contacts must be opened. This is achieved using direct laser writing, where a laser beam—operating in the visible, UV, or IR range—writes directly on the

photoresist, without the need for a mask, in the regions corresponding to the contact pad openings. In this case as well, aluminum is deposited by thermal evaporation and patterned via a lift-off process.

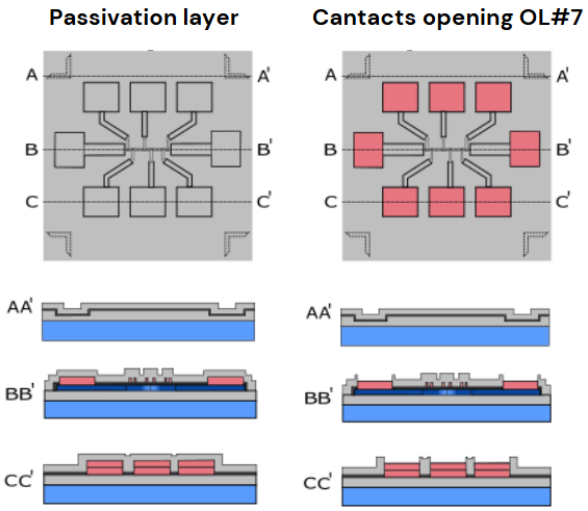


Figure 3.7: Contacts opening.

3.2 Planar SET fabrication process

The substrate used for the fabrication of the planar SET is a lightly boron-doped silicon wafer, with a doping concentration of $N_A = 1.5 \times 10^{15}$ cm^{-3}. As for the nanowire-based device, the fabrication steps are presented below in sequential order.

Transferring alignment marks First, the alignment marks are transferred onto the silicon substrate through an optical lithography step ($OL\#1$). A 1.2 μm thick layer of positive photoresist (6512) is spin-coated onto the substrate and exposed according to the alignment mark pattern. The exposed areas become more soluble and are removed during development. A 500 nm deep layer is then dry etched into the silicon to define the marks, after which the photoresist is stripped.

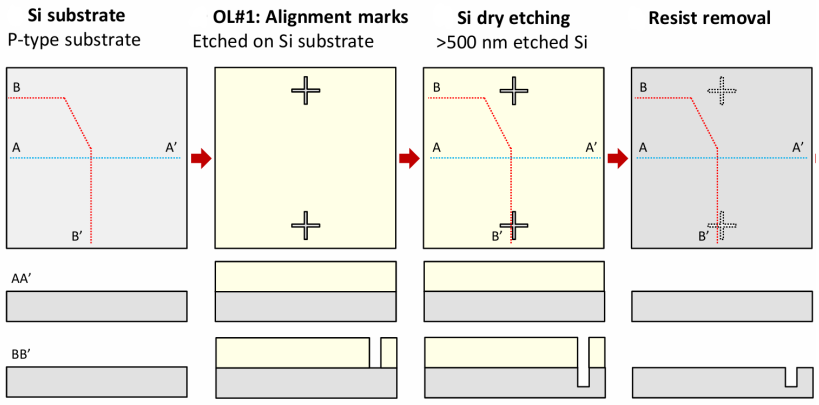


Figure 3.8: Transferring alignment marks.

Local Oxidation of Silicon (LOCOS) The Local Oxidation of Silicon (LOCOS) process is used to electrically isolate the different devices on the chip. First, an 18.7 nm thick layer of pedestal oxide is grown on the substrate by dry oxidation (at 900 °C for 36 minutes). Then, a 117.5 nm thick layer of silicon nitride (Si_3N_4) is deposited via Low-Pressure Chemical Vapor Deposition (LPCVD) and patterned using a second optical lithography step ($OL\#2$) to cover the active areas of the chip. The silicon nitride acts as a hard mask during the subsequent oxidation step, as it resists high temperatures and inhibits oxide growth underneath. A thick thermal oxide layer (∼200 nm) is then grown in the field regions to ensure proper electrical isolation between devices. After the oxidation, the resulting oxynitride is removed, the nitride is etched away, and finally, the pedestal oxide is stripped using Buffered Oxide Etch (BOE).

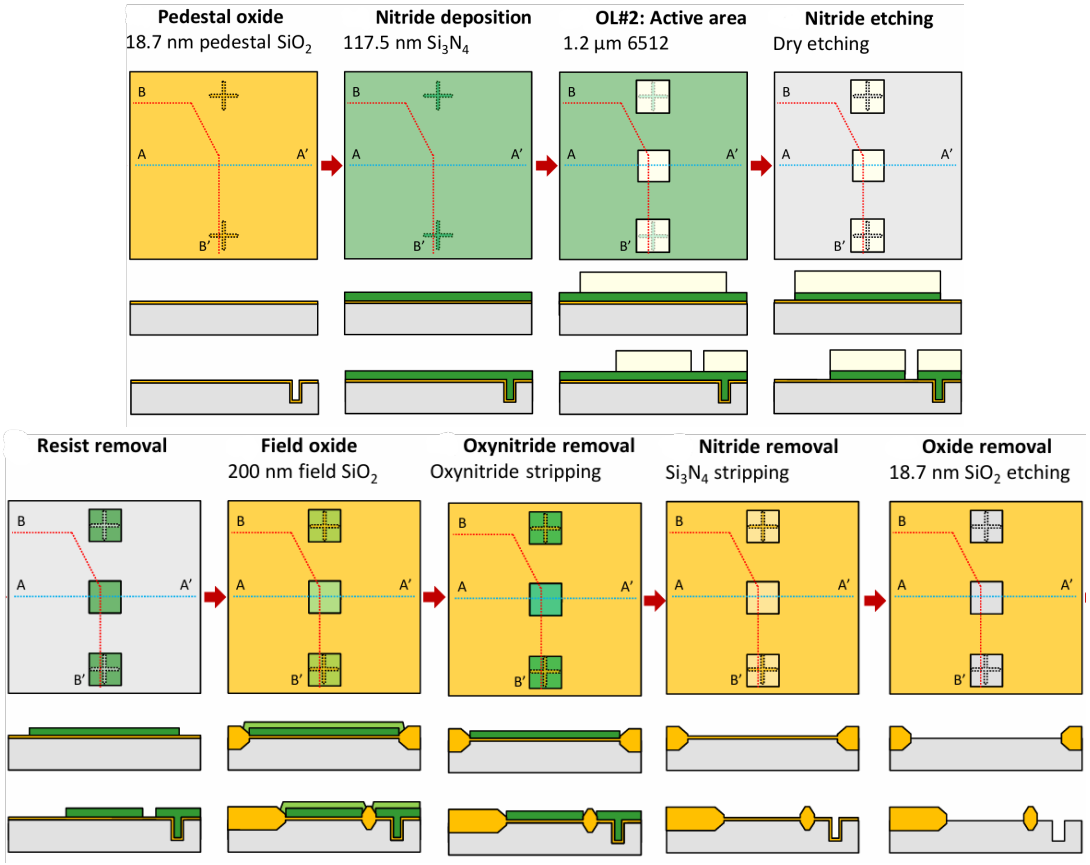


Figure 3.9: Local Oxidation of Silicon.

Source/Drain implantation Before the Source and Drain well implantation, a 36.5 nm thick layer of sacrificial silicon oxide is grown by dry oxidation (at 950 °C for 45 minutes). This sacrificial oxide serves to attenuate the ion energy during implantation and helps minimize sputtering and crystalline damage in the silicon substrate, thereby reducing the extent of amorphization caused by the ion beam.

A third optical lithography step ($OL\#3$) is carried out to open windows in the photoresist over the implantation regions. For this, a 1.2 μm thick layer of 6512 positive photoresist is used.

Subsequently, phosphorus ions are implanted at an energy of 50 keV with a dose of 4.2×10^{15} cm^{-2} to form the Source and Drain wells.

After implantation, a fourth optical lithography step ($OL\#4$) is performed using AZ negative pho-

toresist. This step is used to selectively expose the active region and remove the sacrificial oxide grown earlier.

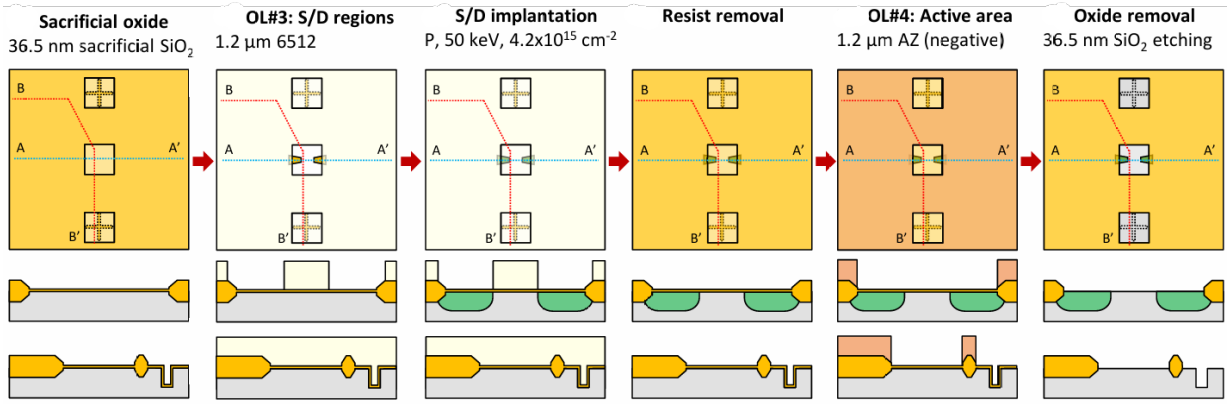


Figure 3.10: Source/Drain implantation.

Source and Drain contacts At this point, a 6.5 nm thick gate oxide layer (SiO_2) is grown via dry oxidation. The formation of the Source and Drain metal contacts begins with the definition of contact windows: openings are etched into the gate oxide to access the underlying regions.

The contact window patterning is performed through optical lithography. Subsequently, a 30 nm thick layer of aluminum is deposited onto the contact openings by sputtering (at $T = 100$ °C and $P = 400$ W).

A further lithography step ($OL\#5$) is carried out using the 6512 positive photoresist to define the areas where the Source and Drain contacts are to be formed. After development, a thicker aluminum layer (200 nm) is deposited, either by sputtering or thermal evaporation, followed by a lift-off process to finalize the metal contact patterning.

The photoresist is removed by immersion in acetone and subsequent UV treatment to ensure complete stripping.

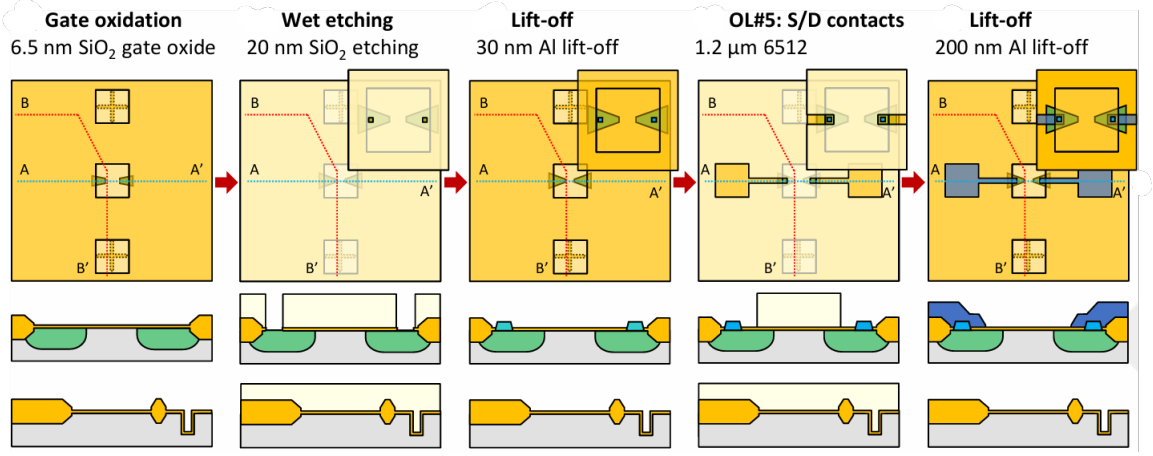


Figure 3.11: Source/Drain contacts deposition

Barrier gates definition At this stage, the structure could be used to fabricate a traditional MOSFET by simply performing an additional optical lithography step to define and deposit the gate electrode.

However, to realize a planar Single-Electron Transistor (SET), it is necessary to pattern barrier gates within the active region. Due to the small critical dimension required for these gates (approximately 30 nm), a high-resolution lithography technique—Electron Beam Lithography (EBL)—must be employed. Using EBL (*EBL#1*), a positive-tone resist (PMMA) is exposed in the regions corresponding to the barrier gate geometry. After development, 30 nm of aluminum is deposited via thermal evaporation, followed by a lift-off process to define the metal gate structures. Subsequently, a 5 nm thick layer of aluminum oxide (Al_2O_3) is deposited using Atomic Layer Deposition (ALD), a technique that ensures excellent thickness control and uniformity. This dielectric layer serves to electrostatically isolate the lead gate from the underlying barrier gates, acting as an intermetal dielectric.

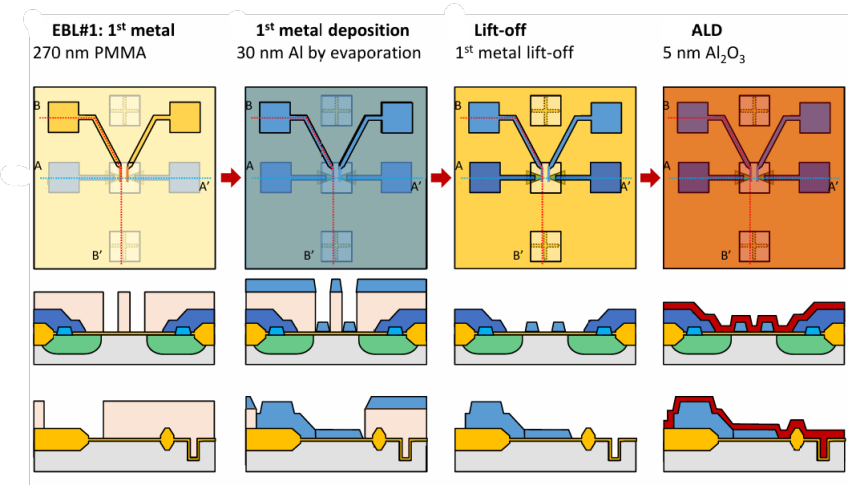


Figure 3.12: Barrier gates definition

Lead gate definition A second EBL step (*EBL#2*) is carried out to define the geometry of the lead gate, which is the electrode responsible for inducing the inversion layer in the channel. As in the previous step, 30 nm of aluminum are deposited via thermal evaporation and patterned through a lift-off process using PMMA as the resist.

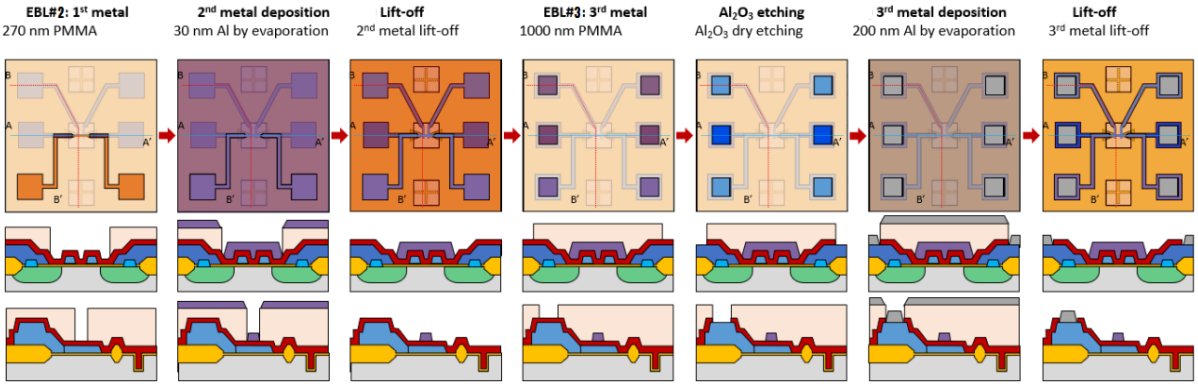


Figure 3.13: Lead gate definition and contacts opening

Subsequently, a final EBL step ($EBL\#3$) is performed to open the contact windows for the Source, Drain, and barrier gates. The aluminum oxide layer is then etched in the exposed areas using Argon milling, in order to ensure electrical contact. Finally, a 200 nm thick metal layer (aluminum) is deposited by thermal evaporation and patterned via lift-off to complete the contact definition.

In Figure 3.14, the main steps of the fabrication process for the planar structure simulated using TCAD Sentaurus are shown. The final structure obtained through this process will be analyzed in the following Chapter.

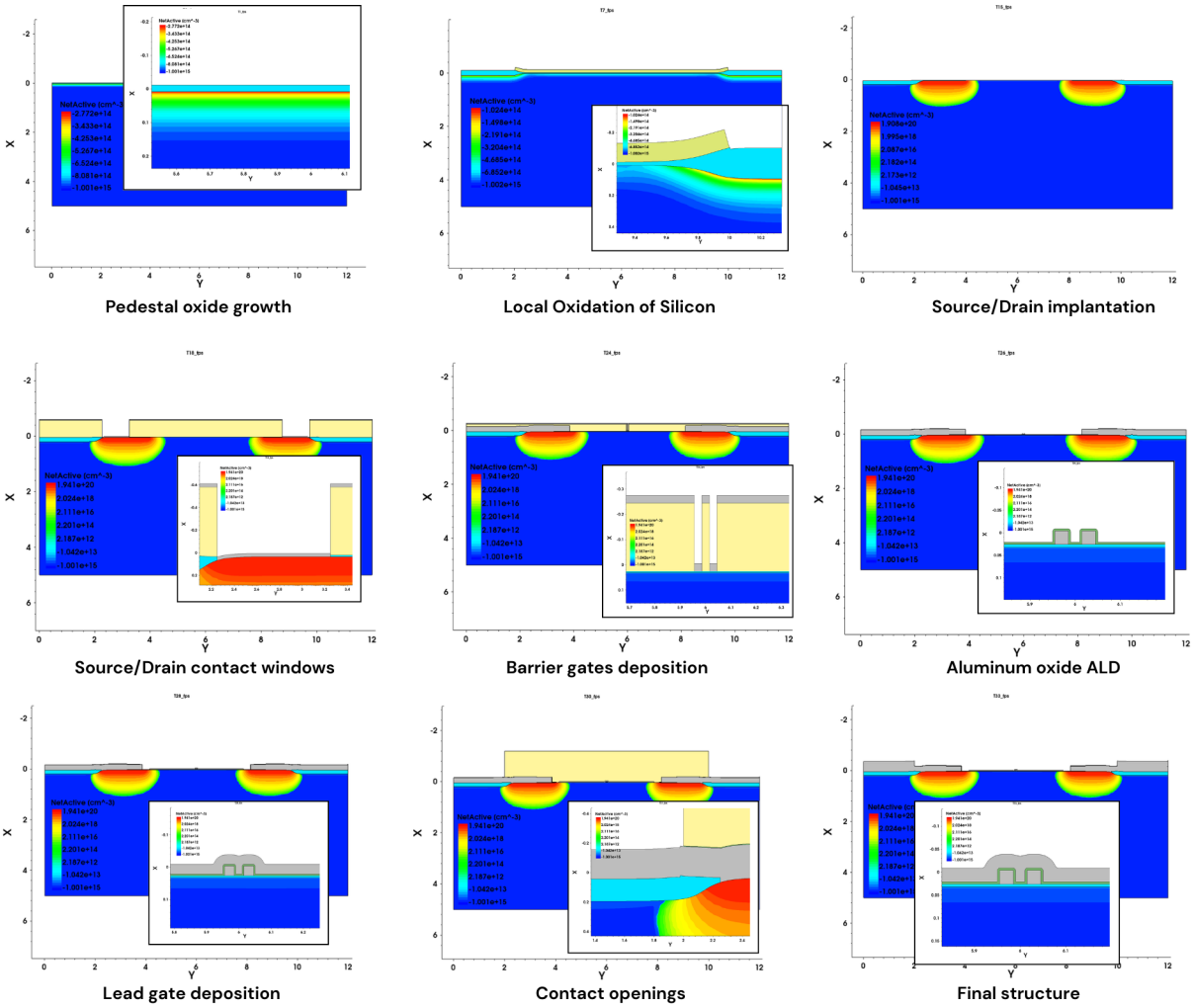


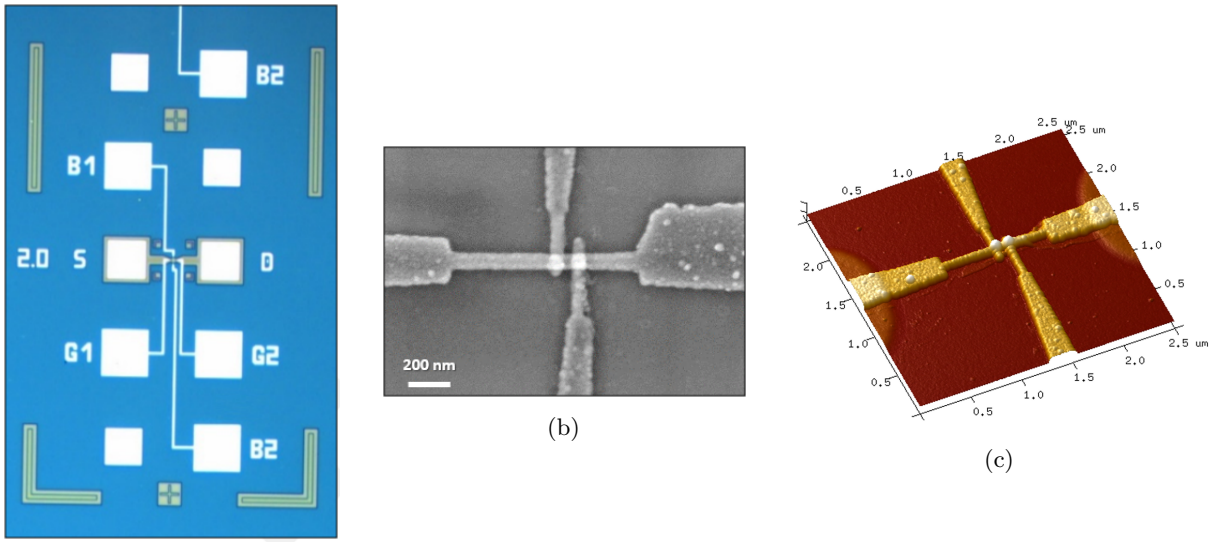
Figure 3.14: TCAD simulation of the fabrication process.

Chapter 4

Planar SET Simulations

The final chapters are dedicated to the simulations of the fabricated devices electrical behavior.

Both the planar structure and the nanowire FET are analyzed, with particular emphasis on the latter, especially under low-temperature conditions. It is worth noting that Sentaurus is not specifically optimized for cryogenic simulations, mainly due to the unreliability of certain parameter trends used in semiclassical models at low temperatures. Moreover, at cryogenic temperatures the intrinsic carrier concentration becomes extremely low, which often leads to convergence issues during the simulation process.



(a) (b) (c)

Figure 4.1: Planar SET device fabricated at IMB-CNM. a) Optical microscopy image of the device layout, b) SEM image of the central region of the device, c) topographic map of the device obtained by AFM.

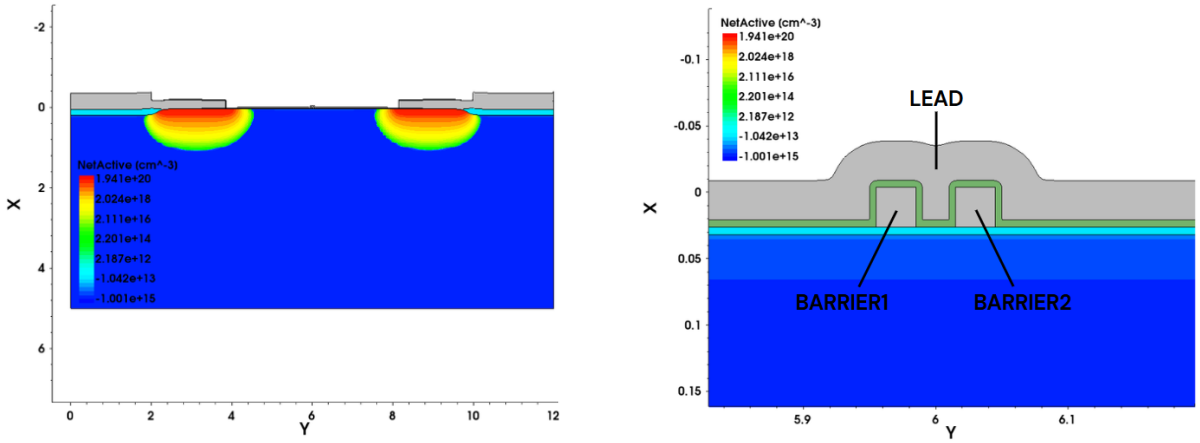
In this chapter, the electrical behavior of the planar SET is discussed, starting from the structure obtained through the simulation of the fabrication process, as presented at the end of the previous chapter (Figure 3.14). The device consists of a MOSFET-like structure, with two additional barrier gates placed between the lead gate—which controls the inversion layer in the channel—and the silicon active region.

The barrier gates are electrically isolated from the lead gate by a 5 nm thick layer of aluminum oxide, deposited by Atomic Layer Deposition (ALD).

Figure 4.1 shows the planar SET devices fabricated at IMB-CNM. In particular, Figure 4.1a presents an optical microscopy image of the device layout; Figure 4.1b shows a Scanning Electron Microscope (SEM) image of the central region of the channel; and Figure 4.1c displays a topographic map acquired using Atomic Force Microscopy (AFM).

4.1 Room temperature 2D simulations

First, the structure was tested as a traditional MOSFET, by setting the lead gate and both barrier gate voltages equal ($V_{\text{Lead}} = V_{b1} = V_{b2}$), effectively simulating a single gate controlling the inversion layer in the channel. The electrical simulation was carried out on the 2D structure obtained from the fabrication process, assuming a third dimension of 50 nm, corresponding to the width of the fabricated lead gate.

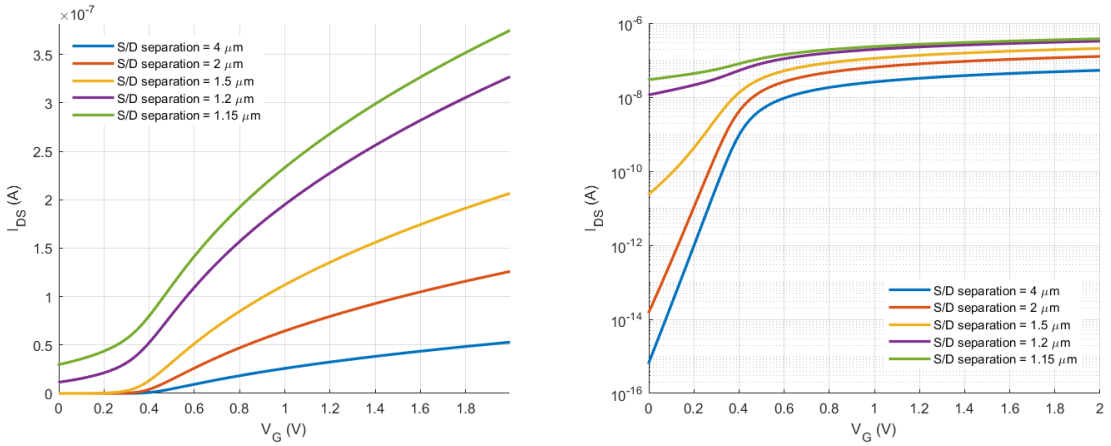


(a) (b)

Figure 4.2: a) 2D cross-section of the device obtained by simulating the manufacturing process. b) Zoom into the barrier gates region.

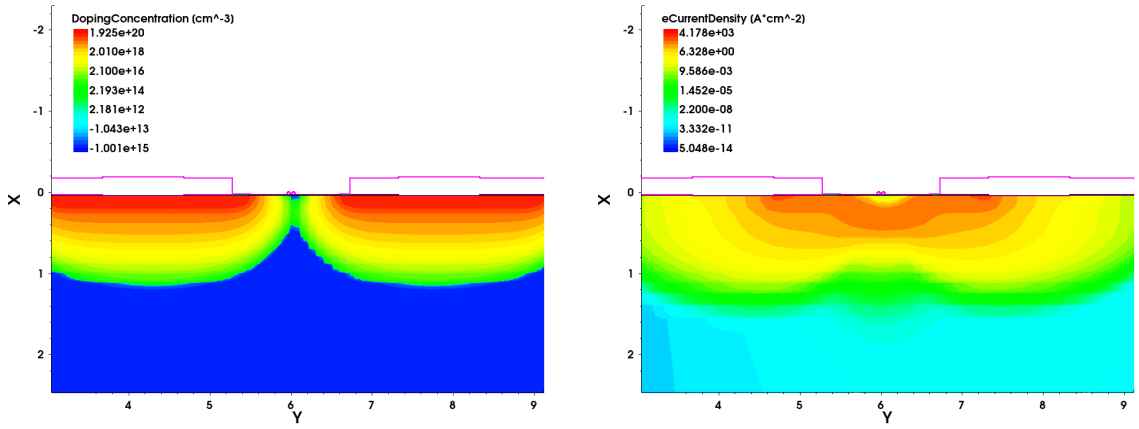
Figure 4.3 shows the transcharacteristic of the device under these voltage conditions for different spacings between the source and drain implantation wells: 4 μm (corresponding to the geometry in Figure 4.2), 2 μm, 1.5 μm, 1.2 μm, and 1.15 μm.

As can be observed, when the distance becomes too small, a punch-through current appears, leading to conduction even at gate voltages below the threshold. Punch-through refers to a breakdown process whereby source and drain electrode depletion regions merge, allowing current to flow between them regardless of the gate voltage.



(a) (b)

Figure 4.3: Transcharacteristics for different S/D separations in linear (a) and logarithmic (b) scale, where $V_g = V_{Lead} = V_{b1} = V_{b2}$.



(a) (b)

Figure 4.4: Punch-through effect arising for S/D separation of 1.15 μm. a) Doping distribution in the substrate. b) Current density at $V_g = V_{Lead} = V_{b1} = V_{b2} = 0$ V.

Figure 4.5 shows the conduction band profile along a 1D cut through the device channel for two values of gate voltage, one below threshold ($V_g = 0$ V) and one above threshold ($V_g = 2.0$ V), under the same drain-source voltage (V_{DS}). As can be observed, the behavior resembles that of a conventional MOSFET: when the gate voltage is below threshold, the potential barrier between source and channel is too high to allow thermionic emission of carriers from the source reservoir. Conversely, when V_g exceeds the threshold, the barrier is lowered, enabling current to flow through the channel.

Figure 4.6 shows the I_d–V_g and I_d–V_d characteristics of the device, again confirming the behavior expected from a standard MOSFET.

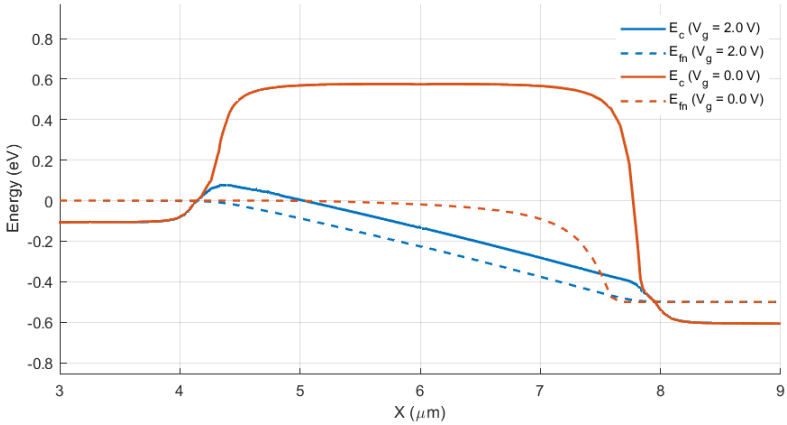
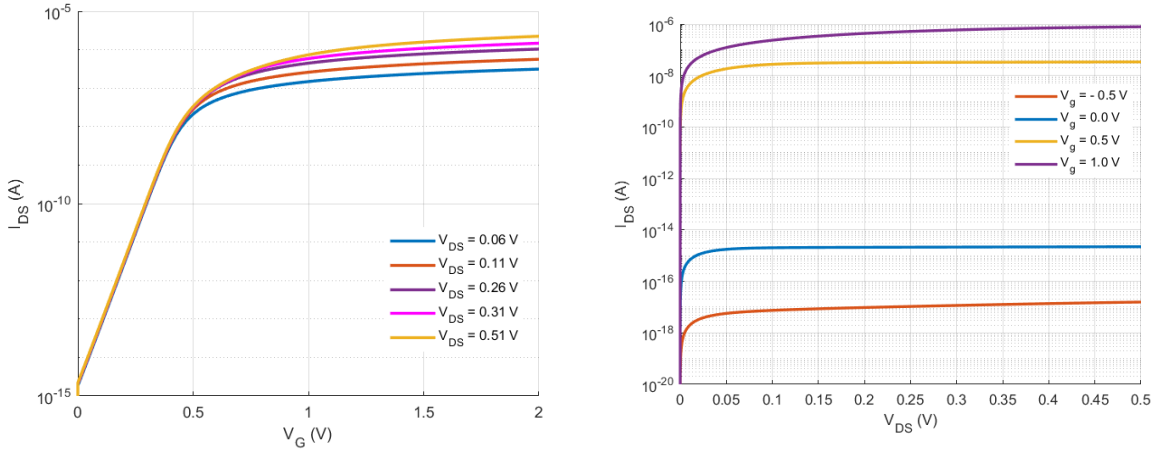


Figure 4.5: Conduction band profile along the channel for $V_g = 0$ V and $V_g = 2.0$ V, showing barrier lowering with increasing gate voltage.



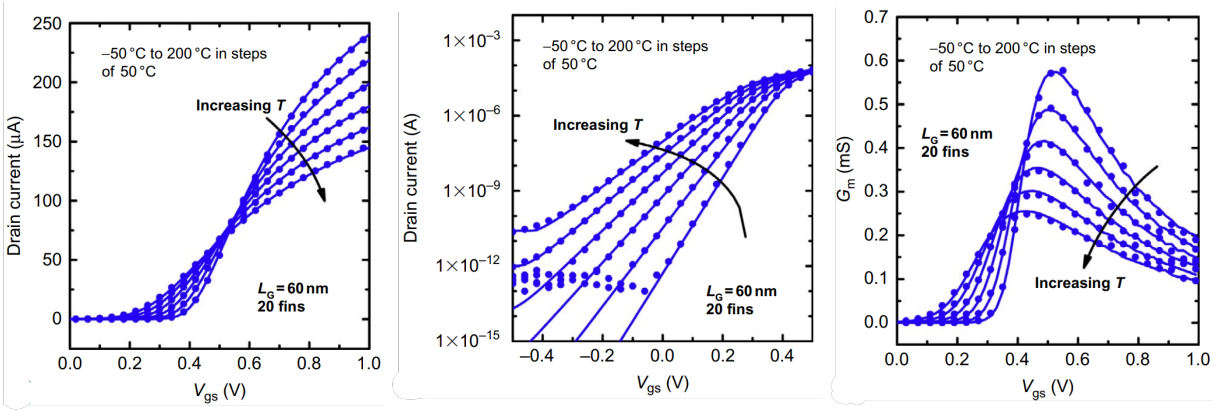
(a) (b)

Figure 4.6: a) $I_d - V_g$ transcharacteristic for V_{DS} ranging from 0.06 V to 0.51 V. b) $I_d - V_d$ characteristic for V_g ranging from -0.5 V to 1.0 V.

4.1.1 Effect of temperature on the electrical behavior

Although reaching low temperatures (less than 20 K) is not easy due to convergence problems (especially on a non-ideal structure obtained from process simulations), an analysis of the device behavior at temperature, up to $T = 60$ K, can still be done.

Figure 4.7 shows experimental measurements of a SOI FinFET taken by [6], for temperatures ranging from 200 °C to -50°C. The tested device is a FinFET but the reasoning we will discuss in the following is valid for any Field Effect Transistor.

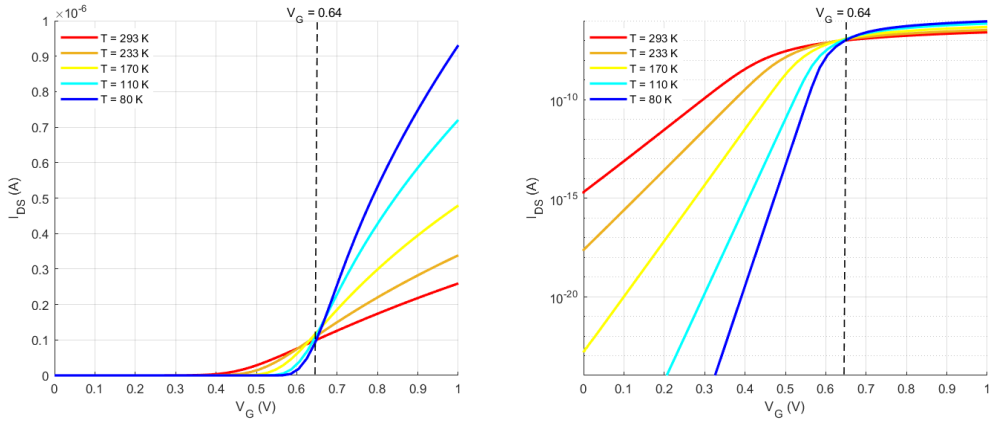


(a) (b) (c)

Figure 4.7: SOI FinFET experimental measurements for different temperatures, taken from [6].

As can be observed from the plots there is a specific gate voltage, $V_G = 0.52$ V in the measured device, for which the current remains constant as the temperature varies. This point is known as the Zero-Temperature-Coefficient (ZTC) point and arises from the interplay of two competing effects that effectively cancel each other out:

- above this voltage, the current increases as the temperature decreases. This is due to the fact that at lower temperatures there is less phonon scattering, hence the overall mobility of carriers increases;
- below this voltage the current decreases slightly as the temperature decreases, due to the fact that at lower temperatures reaching the channel inversion becomes easier resulting in a lowering of the threshold voltage V_{th}. In this regime, the effect of lowering the threshold voltage dominates over the mobility effect.



(a) (b)

Figure 4.8: Simulated $I_d - V_g$ transcharacteristic in a) linear and b) logarithmic scale for temperature ranging from 293 K to 80 K.

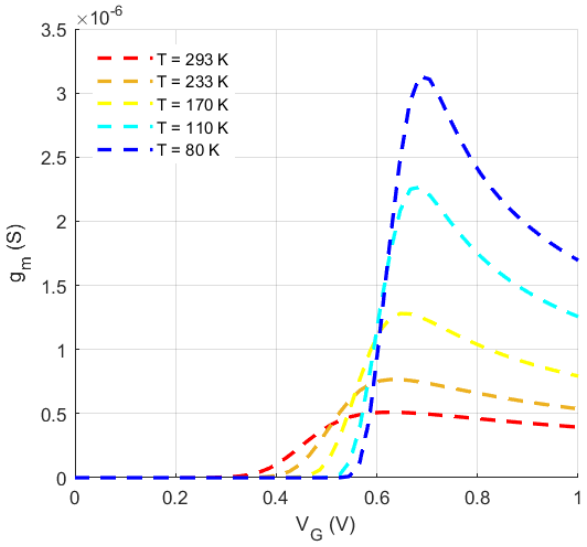


Figure 4.9: Transconductance g_m at different temperature obtained from simulations.

The plots in figure 4.8 show the $I_d - V_g$ curves simulated at different temperatures using the hydrodynamic based model discussed in detail in Section 5.3. Figure 4.9 instead shows a plot of the transconductance $g_m = \frac{dI_{DS}}{dV_G}$. The trend reflects that expected from the literature.

Figure 4.8b shows the transcharacteristic in logarithmic scale highlighting the change of the Subthreshold Slope (SS) as a function of temperature. Subthreshold Slope is a fundamental quantity in MOSFETs that describes how quickly the drain current increases with increasing gate voltage in the subthreshold region, i.e. when the transistor is "almost off" and the current increases exponentially. It is measured in mV/dec:

$$SS = \frac{dV_{GS}}{d\left(\log_{10} I_{DS}\right)} \tag{4.1}$$

The relationship between SS and temperature is linear:

$$SS = nV_T \ln(10) = n\frac{kT}{q}\ln(10) \tag{4.2}$$

where $n \geq 1$ is the ideality factor and accounts for all effects (such as charges at the oxide/semiconductor interface, defects or impurities, short channel effect ...) that make the device behavior in the substrate region less ideal, a value of $n = 1$ corresponds to an ideal device. The SS versus temperature behavior extracted from Figure 4.8b is linear and shown in the plot in Figure 4.10, the calculated ideality factor value is $n = 1.05$, so very close to ideality.

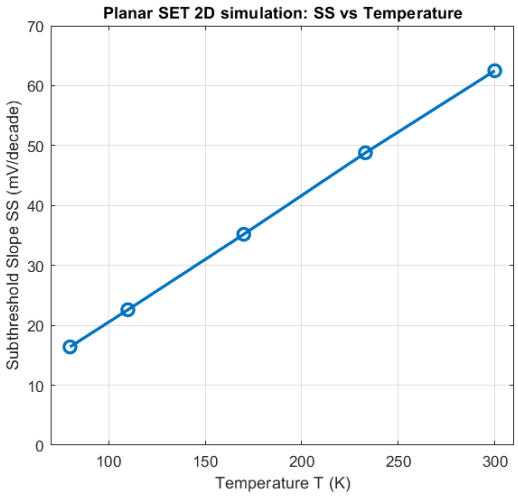
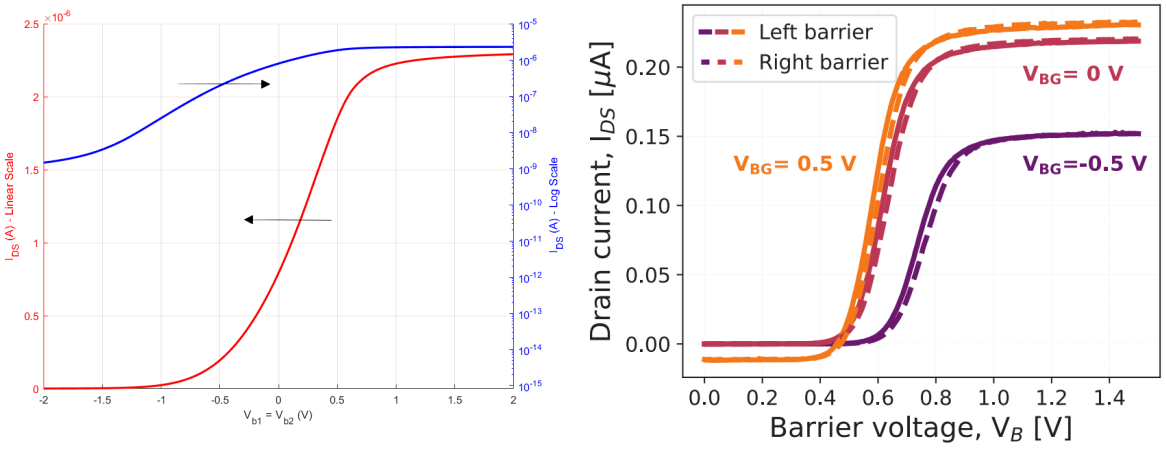


Figure 4.10: Subthreshold slope as a function of temperature

4.1.2 Effect of the Barrier Gates Voltage on Conduction

After simulating the MOSFET behavior, the analysis focuses on the influence of the barrier gate voltages. The primary function of the barrier gates is to locally deplete the electron population beneath them, once the channel is fully formed, thereby creating electrostatic confinement for the quantum dot that forms between the two barriers. To investigate this effect, a first analysis is performed at room temperature by applying a voltage to the lead gate well above the threshold, ensuring the formation of a conductive channel. The voltage applied to the barrier gates is then varied to observe how it modulates the conduction. Figure 4.11a shows the current flowing through the device as a function of the barrier gate voltage under these conditions.

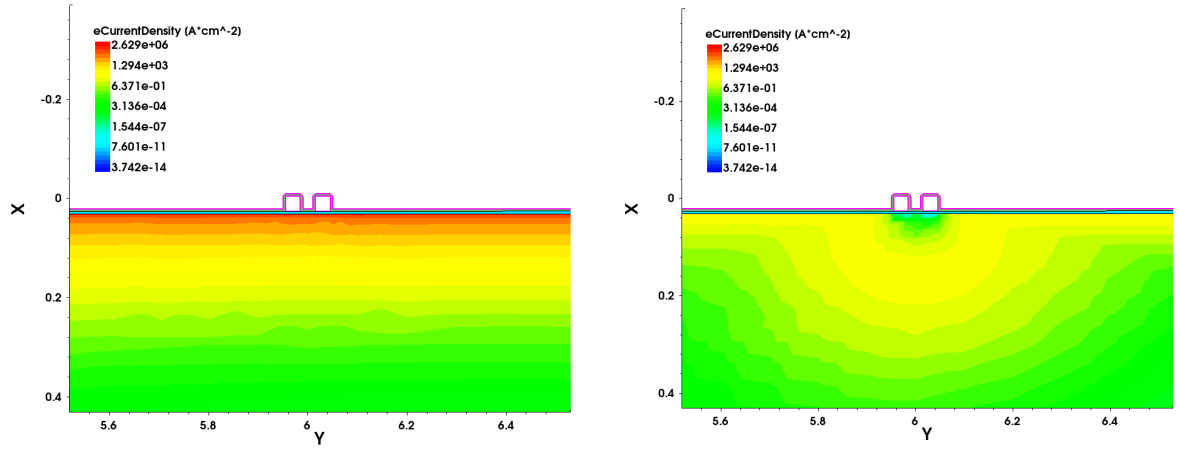


(a) (b)

Figure 4.11: a) $I_d - V_b$ curve, with $V_{Lead} = 2.0$ V and $V_{DS} = 0.5$ V. b) $I_d - V_b$ curve of a similar device taken from [2].

As can be observed, applying a negative voltage to the barrier gates reduces the current, following a trend similar to that reported in the literature [2] for comparable devices (Figure 4.11b). However, the minimum current remains on the order of nanoamperes. This is because, at room temperature, negative barrier potentials cause the electron channel to bend toward the substrate (Figure 3.13b) instead of being fully depleted.

As we will see for the nanowire-based SET, this effect vanishes at cryogenic temperatures. Under these conditions, conduction is strictly confined to the silicon/gate oxide interface, and beyond a certain threshold voltage, the barriers completely suppress conduction.



(a) (b)

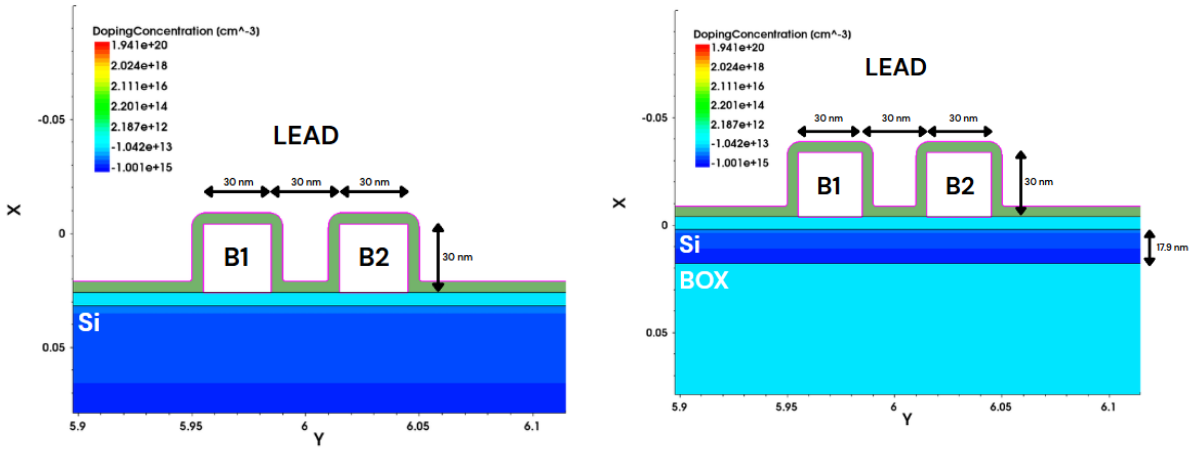
Figure 4.12: Electron current density with $V_{DS} = 0.5$ V, $V_{Lead} = 2.0$ V for a) $V_{b1} = V_{b2} = 2.0$ V and b) $V_{b1} = V_{b2} = -2.0$ V.

The same type of analysis, performed on an FDSOI device, is presented below. The goal is to demonstrate that in this device the current is more effectively turned off, thanks to the presence of the silicon active layer separated from the substrate.

4.1.3 Comparison between Bulk and SOI devices

A slight modification to the fabrication process was implemented to replicate the device on an SOI wafer featuring a 17.9 nm-thick silicon overlayer. The doping type is the same in both devices: in fact, also in the SOI wafer, the starting silicon overlayer is lightly doped with a boron concentration of 10^{15} cm^{-3}, while the source and drain wells are doped with phosphorus atoms at a concentration of approximately 2×10^{19} cm^{-3}.

A comparison between the two structures is shown in Figure 4.13. It should be noted that, in both cases, due to the way metal contacts are defined in Sentaurus, the lead gate and barrier gates are represented as empty regions.



(a) (b)

Figure 4.13: 2D simulations of a) the planar SET device fabricated on bulk silicon and b) the planar SET device fabricated on an SOI wafer. The dimensions of the metal contacts and oxide layers are the same in both cases.

The plot shown in Figure 4.14 compares the effect of the barrier gate voltage on the current in the two devices. The key result is the behavior of the current for negative values of the barrier gate voltage. In the device fabricated on a bulk wafer, the current decreases but eventually saturates at a constant value on the order of nanoamperes, due to channel bending effects that allow electrons to bypass the barrier through the substrate.

In contrast, in the SOI device, the current drops to values on the order of 10^{-14} A (before the simulation fails to converge), since the buried oxide layer prevents any current from flowing through the substrate, leading to more effective current suppression.

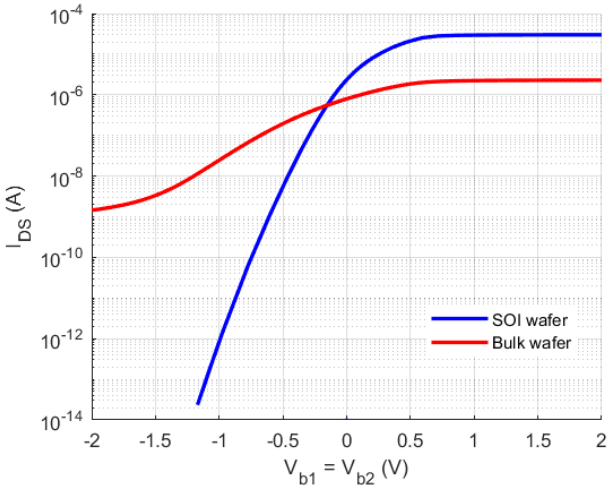
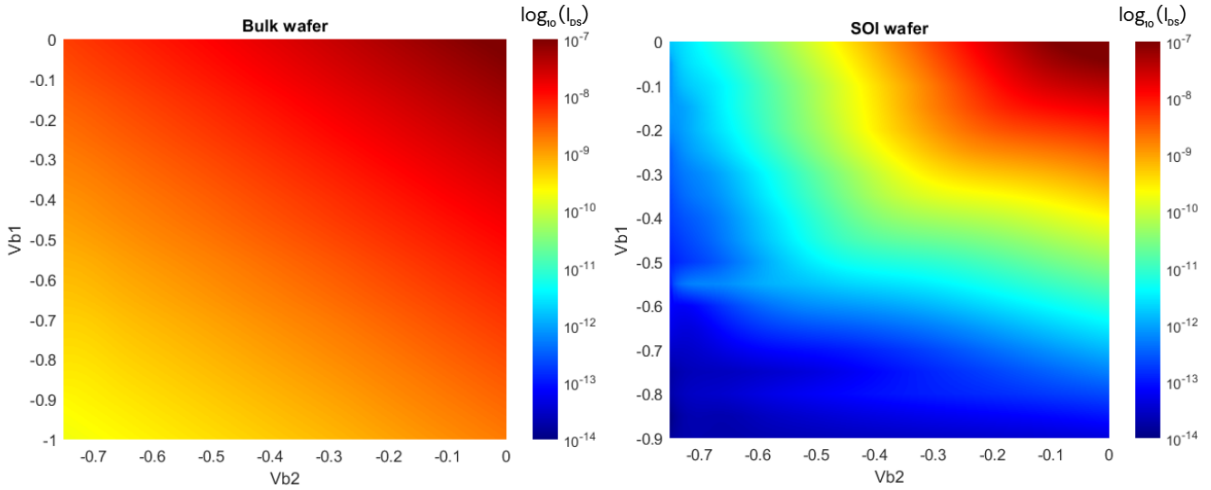


Figure 4.14: Drain current as a function of the barrier gate voltage, for $V_{DS} = 0.5$ V and $V_{Lead} = 2.0$ V.

Figure 4.15 shows the drain-to-source current as a function of the applied barrier gate voltages. It can be observed that in the SOI device, there is a well-defined threshold beyond which the conduction is effectively suppressed, indicating complete channel pinch-off.

Indeed, for voltages $V_{b1} = V_{b2} = -0.7$ V, we obtain a current on the order of nanoamperes for the bulk wafer, and on the order of picoamperes for the SOI device.



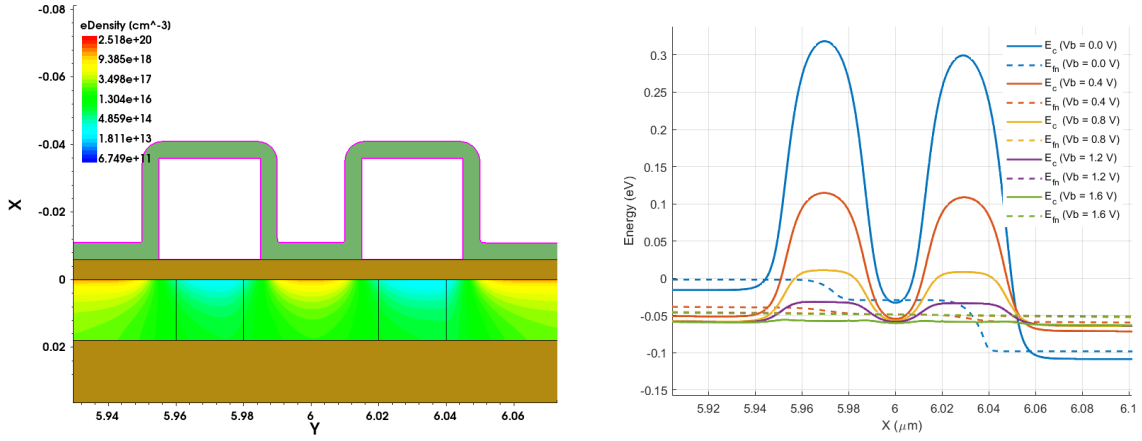
(a) (b)

Figure 4.15: Drain current maps as a function of the barrier gate voltages. (a) Bulk silicon device at $V_{DS} = 0.5$ V and $V_{Lead} = 1.0$ V. (b) SOI device at $V_{DS} = 0.5$ V and $V_{Lead} = 0.6$ V.

4.2 FDSOI Planar SET Room Temperature Simulations

The SOI structure allows for greater control of the simulation mesh in the dot and barrier regions, and enables a more accurate definition of distinct areas within the silicon active layer. This distinction is crucial for establishing the interfaces required by the tunneling model. For these reasons, the discussion in this section will focus exclusively on the SOI device.

Figure 4.16a shows the definition of the silicon overlayer into three separate regions: BARRIER1, BARRIER2, and QDOT. These subregions enable localized analysis of the conduction band profile and current flow. In Figure 4.16b, a one-dimensional cut of the conduction band along the channel (at the interface between silicon and oxide) is shown for different values of the barrier gate voltage. The formation of electrostatic barriers beneath the gates is clearly visible, as well as the reduction in their height as the voltage $V_{b1} = V_{b2}$ increases.



(a) (b)

Figure 4.16: Simulation of the SOI planar SET at room temperature. a) Electron density distribution showin the formation of the dot, b) conduction band profile along the silicon–oxide interface for different barrier gate voltages.

4.2.1 Tunneling Model

The calculation of electron tunneling through potential barriers is carried out using the non-local tunneling model implemented in Sentaurus Device [35], based on the methodology presented in [20]. This approach employs the Wentzel-Kramers-Brillouin (WKB) approximation to estimate the tunneling probability.

The main advantage of the non-local model is its capability to operate with conduction band profiles that are not predefined, as is typically the case for tunneling through insulating layers, but instead self-consistently computed by solving the Poisson equation. This allows for a more accurate estimation of the tunneling probability along specific spatial paths defined within non-local meshes.

In this study, the non-local meshes are constructed with respect to two reference interfaces, as illustrated in Figure 4.17a:

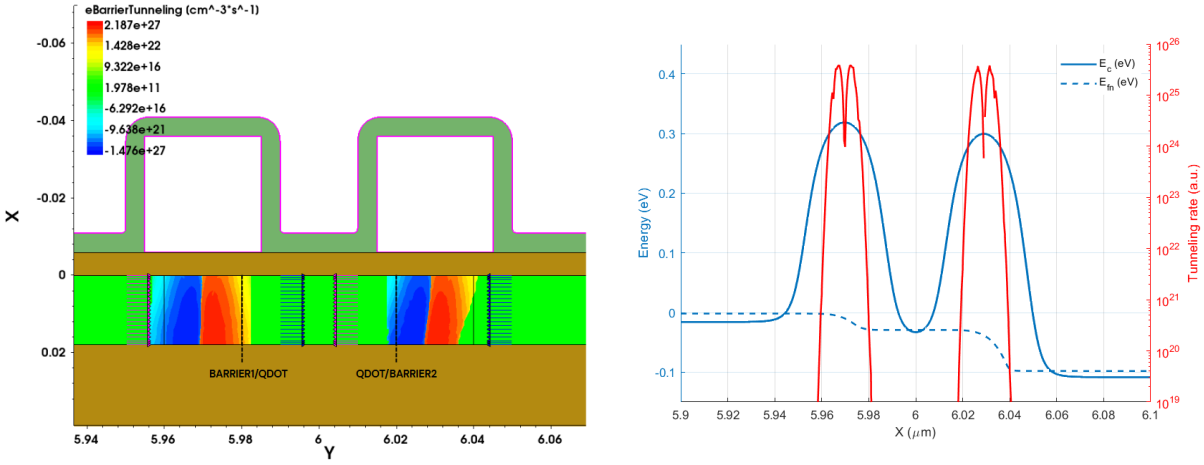
- The `BARRIER1/QDOT` interface, between the first barrier region and the central region where the quantum dot forms;
- The `QDOT/BARRIER2` interface, between the quantum dot and the second barrier region.

Each non-local mesh is defined by definind a fixed distance, set to 50 nm in all simulations, from the reference interface, ensuring that all relevant tunneling contributions are captured while maintaining reasonable simulation times. The meshes are oriented perpendicularly to the interfaces, and tunneling probabilities are evaluated at each mesh node.

Sentaurus Device also provides a parameter called `Permeation`, which extends the integration region beyond the explicitly defined interfaces. When the potential barrier is smooth, enabling this parameter (i.e., setting it to a positive value) allows the tunneling rate to be computed along the entire length of the non-local path, not just at the interface itself. In all simulations presented here, the `Permeation` parameter is set to 2 nm.

Figure 4.17a displays the normalized direction vectors along which tunneling occurs. The same figure also shows the electron tunneling rate through the barriers, computed as a generation/recombination rate (in units of $\mathrm{cm}^{-3}\,\mathrm{s}^{-1}$). Blue regions correspond to negative values, indicating electrons disappearing from

the conduction band, while red regions indicate positive values, i.e., electrons appearing in the conduction band on the opposite side of the barrier.



(a) (b)

Figure 4.17: a) Colored plot of the electron tunneling rate for $V_{Lead} = 2.0$ V, $V_{b1} = V_{b2} = 0.0$ V and $V_{DS} = 0.1$ V. b) Conduction band profile and tunneling rate (in logarithmic scale) along the channel, in the same voltage conditions.

WKB approximation The model used to calculate the tunneling probability is based on the WKB approximation and assumes a single-band parabolic band structure. According to this approximation, the tunneling probability $\Gamma_{\mathrm{CC,v}}(u, l, \varepsilon)$ of an electron with energy ε, tunneling between a lower position l and an upper position $u > l$ within the conduction band, is given by:

$$\Gamma_{\mathrm{CC,v}}(u, l, \varepsilon) = T_{\mathrm{CC,v}}(l, \varepsilon) \underbrace{\exp\left(-2\int_{l}^{u} \kappa_{\mathrm{C,v}}(r, \varepsilon) dr\right)}_{\text{Transparency factor}} T_{\mathrm{CC,v}}(u, \varepsilon) \tag{4.3}$$

where:

- $T_{\mathrm{CC,v}}$ is the interface transmission coefficient, which quantifies the coupling efficiency between the non-local tunneling path and the band edge at the interface. In this work, it is set to the default value of 1, corresponding to perfect coupling.
- The transparency factor describes the exponential suppression of tunneling. Its exponential argument is an integral over the local (imaginary) wave number $\kappa_{\mathrm{C,v}}(r, \varepsilon)$, which quantifies the spatial decay of the electron wavefunction within the barrier. This quantity depends on the local tunneling mass $m_C(r)$ and the carrier energy ε:

$$\kappa_{\mathrm{C,v}}(r, \varepsilon) = \frac{\sqrt{2 m_{\mathrm{C}}(r) \left| E_{\mathrm{C,v}}(r) - \varepsilon \right|}\, \Theta\left[E_{\mathrm{C,v}}(r) - \varepsilon\right]}{\hbar} \tag{4.4}$$

  where Θ is the Heaviside step function. The tunneling mass used for electrons is the transverse effective mass in silicon, $m_{t,e} = 0.19\, m_0$.

Gate-defined SETs are designed such that the dominant contribution to tunneling occurs near the top of the potential barriers. However, as discussed in more detail in Chapter 5, at temperatures above the millikelvin regime, the current due to thermionic emission typically dominates over the tunneling current.

To validate the tunneling model adopted in this work, a simplified conduction band profile was constructed, consisting of potential barriers with constant thicknesses and well-defined shapes (Figure 4.18). In this test structure, the energy gap of silicon was locally modified to artificially define the barriers.

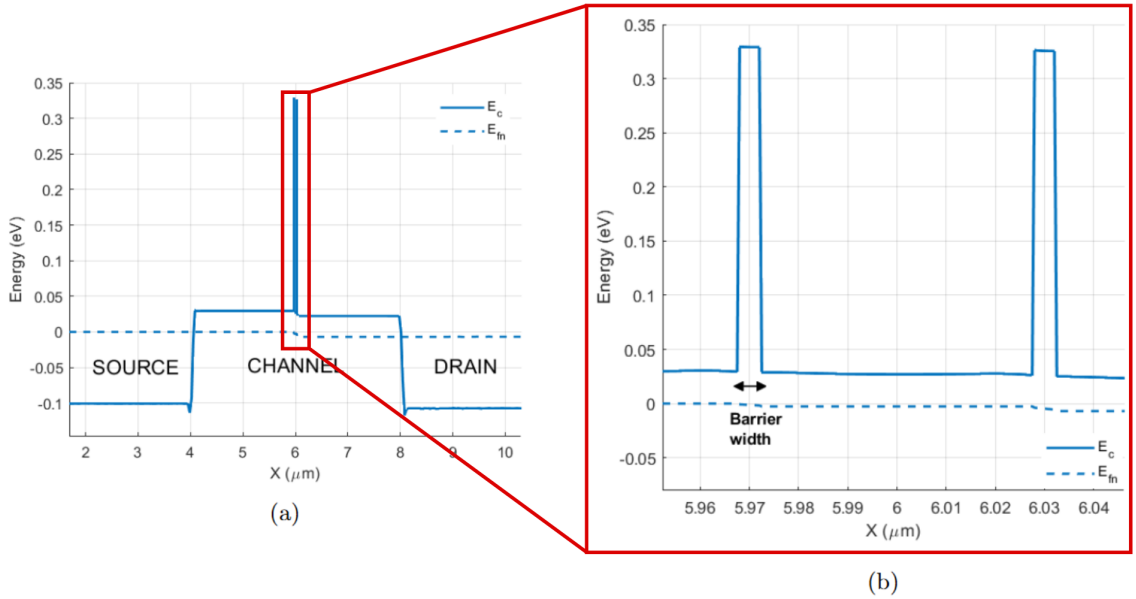


Figure 4.18: a) Conduction band profile constructed by locally modifying the silicon energy gap in correspondence with the barriers, resulting in a barrier height of 0.3 eV. b) Zoomed view into the barrier region.

Figure 4.19 shows a comparison of the simulated drain-to-source current as a function of temperature, with (solid lines) and without (dashed lines) the tunneling model enabled. As temperature decreases, the contribution of thermionic emission (dashed lines) diminishes, while the tunneling current (solid lines) remains approximately constant. However, for very thick barriers, such as those 10 nm thick, the tunneling current is extremely low, on the order of 10^{-10} A and a difference in terms of order of magnitude can only be appreciated at very low temperatures.

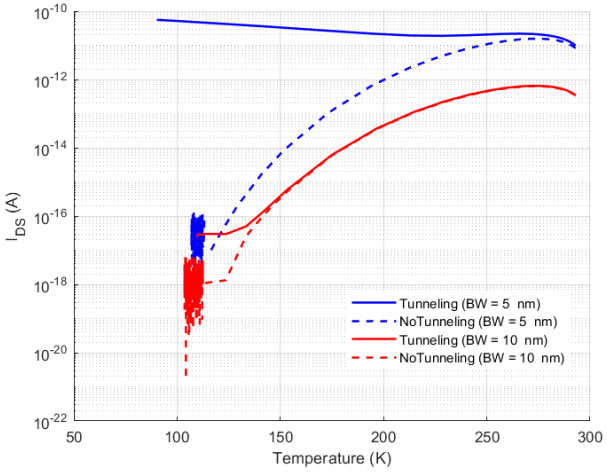
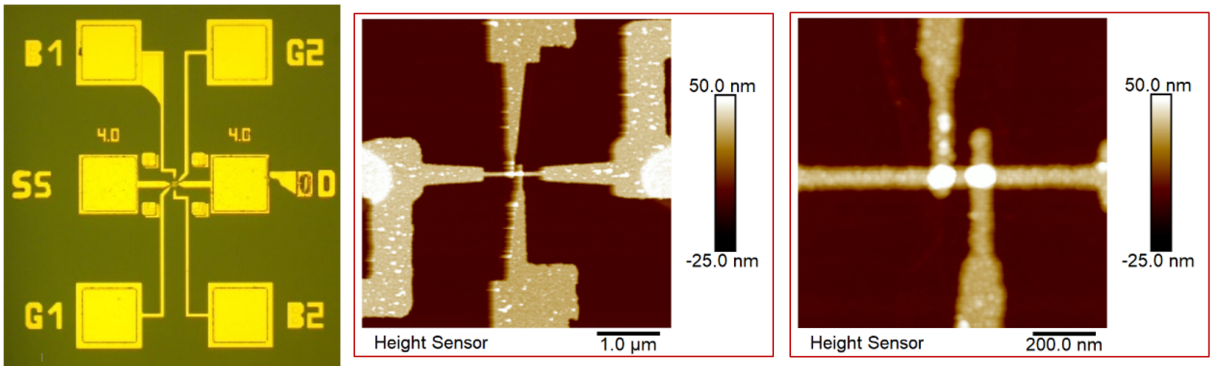


Figure 4.19: Comparison of drain-to-source current in the presence (solid lines) and absence (dashed lines) of tunneling model, for two different barrier widths.

4.3 Experimental measurements and fixed charge model

Some experimental measurements were performed at room temperature and at -40 °C on the fabricated structures to test them before measuring in cryogenic apparatus. Measurements were performed by Pol Gaya and are discussed in detail in [33].



(a) (b) (c)

Figure 4.20: Device layout. a) Optical image of the device including contact pads. b) AFM (?) image of the device active region with c) zoom into the central part.

Figure 4.20 shows the layout of the test device, along with AFM images of the active region, highlighting the terminations of the barrier gates. The device includes two contact pads labeled SS and DD for the source and drain, respectively; pads $B1$ and $B2$ for the barrier gates; and pads $G1$ and $G2$ for the lead gate. These allow for proper biasing and verification of continuity in the gate metallization.

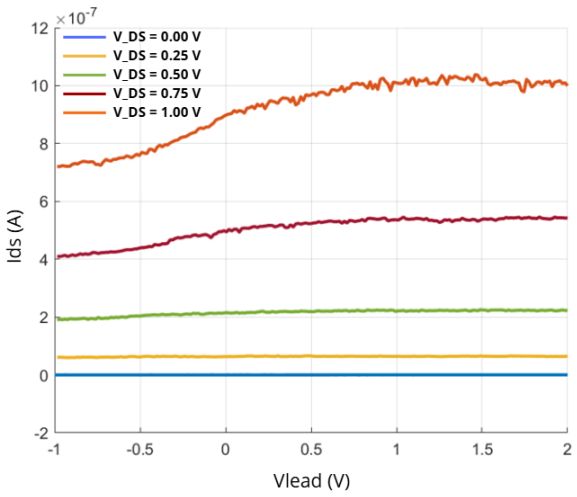
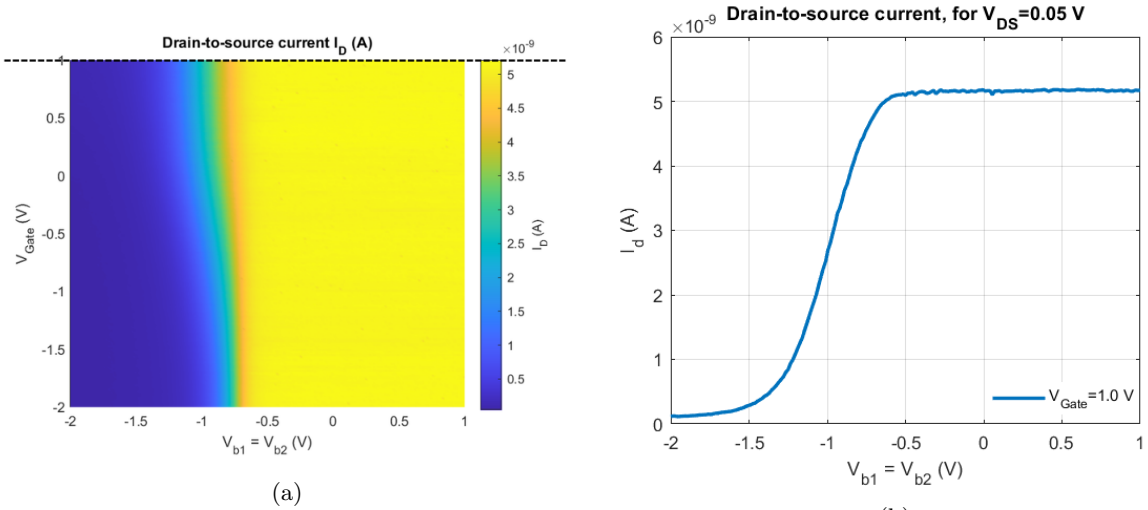


Figure 4.21: $Id - Vg$ curves for V_{DS} ranging from 0 V to 1 V obtained from room temperature electrical measurements.

Preliminary room temperature measurements (Figure 4.21) show a slight modulation of the current as a function of the gate voltage. However, conduction is never fully suppressed, even at very negative values of the lead gate voltage. Figure 4.22a displays a color map of the drain-to-source current as a function of the barrier gate voltage ($V_{b1} = V_{b2}$) and the lead gate voltage (V_{lead}), measured at a fixed drain-to-source voltage of $V_{DS} = 0.05$ V and a temperature of -40 °C.



(a) (b)

Figure 4.22: Electrical measurements performed at $T = -40$°C. a) Colored plot of the drain-to-source current as a function of the barrier gates voltage and the lead gate voltage, b) $I_d - V_b$ curve corresponding to the black dashed cut in the 2D plot, i.e. at $V_{Lead} = 1.0$ V.

As can be seen, the lead gate has a minimal effect on current modulation, while the barrier gates appear to be highly effective in suppressing conduction. This behavior can be explained by considering an

additional contribution to conduction due to the presence of fixed charges at the oxide/silicon interface.

4.3.1 Effect of the Fixed Charges on Conduction

During the fabrication process, positive charges can become trapped at the oxide/silicon interface, leading to a shift in the threshold voltage. These fixed charges are typically associated with defects or dangling bonds, contamination, or non-ideal conditions during oxide formation. The most critical fabrication steps contributing to this issue include the thermal oxidation of silicon, which forms the oxide layer, and subsequent thermal annealing steps.

Positive charges at the oxide/silicon interface lead to a reduction in the threshold voltage of an nMOSFET, as they attract electrons, facilitating the onset of inversion. Figure 4.23 shows a 2D simulation of the device on a silicon bulk wafer using Sentaurus, illustrating the behavior for different concentrations of fixed interface charges.

The threshold voltage is extremely sensitive to the concentration of fixed charges. For a charge density of $\sigma_{SiO_2/Si} = 4.5 \times 10^{12}$ cm^{-2}, the device is already conducting at a gate voltage of 0 V.

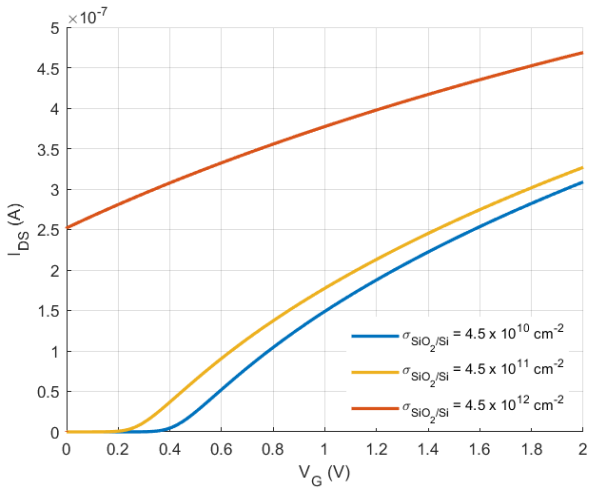
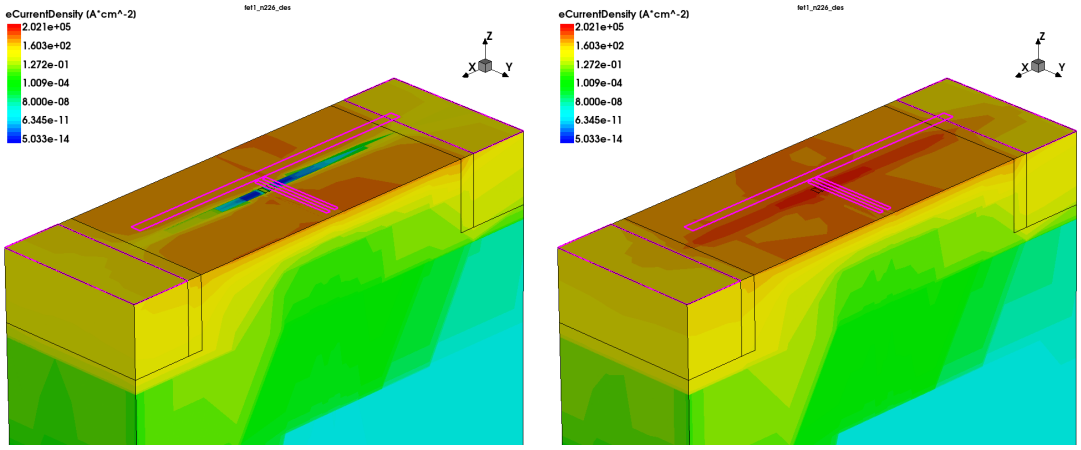


Figure 4.23: Comparison of the $I_d - V_g$ curves of the device for different fixed charges concentration at the Si/SiO_2 interface.

To explain the experimentally observed behavior, it is necessary to perform simulations using a full 3D structure. Since the lead gate voltage does not fully suppress conduction but only induces a slight modulation, it is reasonable to infer that an additional current component flows through lateral regions not effectively controlled by the lead gate. In these areas, conduction is enabled by the presence of fixed charges at the oxide/silicon interface.

Figures 4.24a and 4.24b show 3D simulations performed under different voltage bias conditions. The plots illustrate the electron current density within the device for a fixed interface charge concentration of $\sigma_{SiO_2/Si} = 5.5 \times 10^{11}$ cm^{-2}. For visualization purposes, the metallic gates have been rendered transparent to clearly reveal the spatial distribution of the current density beneath them.



(a) (b)

Figure 4.24: 3D plot of the electron current density for a) $V_{Lead} = -1.5$ V and b) $V_{Lead} = 2.0$ V.

Figures 4.24a and 4.24b refer to two different lead voltage values, $V_{Lead} = -1.5$ V and $V_{Lead} = 2.0$ V, respectively. As can be seen, due to the presence of fixed charges, a conductive inversion layer forms along the entire silicon surface interface, resulting in a parasitic current. The lead gate can only control the portion of the device below it, resulting in a reduced modulation.

Figure 4.25 shows the transcharacteristic $I_d - V_g$ of the device, the value of the concentration of the fixed charges, i.e. $\sigma_{SiO_2/Si} = 5.5 \times 10^{11}$ cm^{-2}, was chosen so that the behavior replicates the electrical measurements in terms of threshold voltage, observed around $V_{Lead} = -0.4$ V.

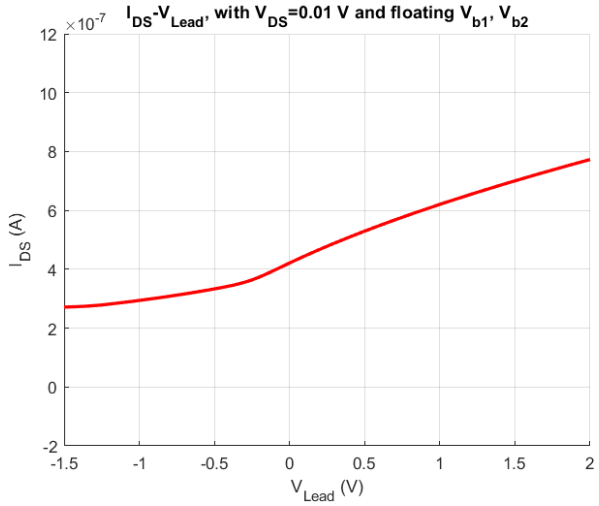


Figure 4.25: Drain-to-source current as a function of the lead gate voltage for the 3D simulation accounting for a fixed charge concentration of 5.5×10^{11} cm^{-2}.

As evident from Figure 4.25, the current remains nearly constant for negative V_{Lead} values, confirming the presence of a current component that cannot be modulated by the lead gate. The effectiveness of the barrier gates in modulating the current, on the other hand, can be attributed to the device layout.

Specifically, the barrier gates are oriented perpendicularly to the main current path, and below a certain threshold voltage, experimentally observed around $V_{b1} = V_{b2} = -1$ V, they are capable of suppressing even this parasitic conduction component.

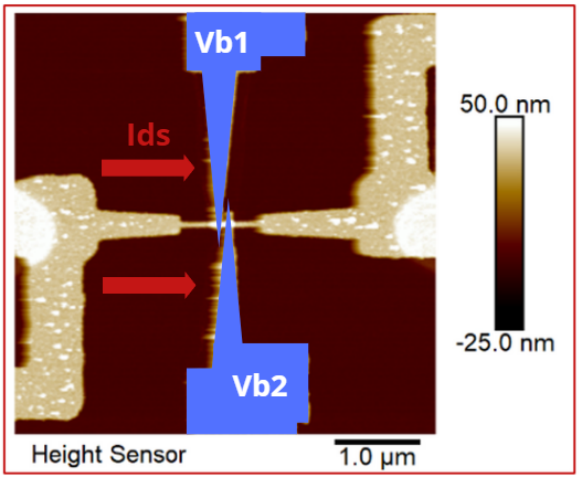


Figure 4.26: AFM image of the device active area, barrier gates effectively suppress parasitic conduction paths.

Further investigations could be carried out by simulating a structure that more closely resembles the actual device layout, or even by simulating the entire fabrication process. This would help identify which regions of the device contribute most significantly to the parasitic current, thereby providing guidance on where to intervene during fabrication to mitigate the issue. Another valuable line of analysis involves studying the effect of fixed charges at low temperatures, given that the SET is intended to operate in the millikelvin regime.

Chapter 5

Nanowire SET Simulations

The nanowire SET is based on a FDSOI Nanowire FET with additional gates around the nanowire to locally control the potential profile in the channel and achieve charges confinement. Figure 5.1b shows an SEM image of a device fabricated at IMB-CNM, with a single barrier gate patterned.

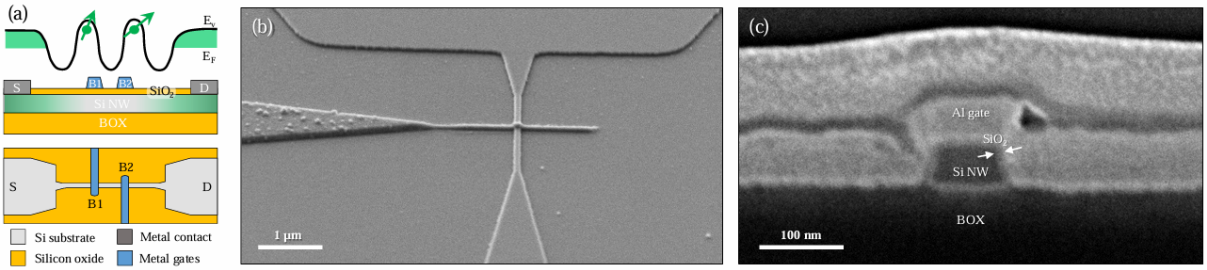


Figure 5.1: a) Schematic of a SET nanowire with two barrier gates, b) tilted SEM view of the gated Si NW, c) cross section of the device.

We first present some simulations of a simple nanowire at room temperature, together with some experimental measurements performed on the same type of device.

5.1 Preliminary simulations on a simple nanowire at room temperature

In this Section, room temperature simulations of simple nanowires are discussed and compared with experimental measurements performed on manufactured devices, with particular emphasis on the rectifying behavior exhibited for high applied voltages.

Figure 5.2 shows the devices fabricated on a SOI wafer, the width of the EBL window is 4 μm while the length of the nanowire (L_{NW}) is variable (500 nm, 1000 nm, 2000 nm, depending on the device). All nanowires have a square cross-section of around 50 nm x 50 nm.

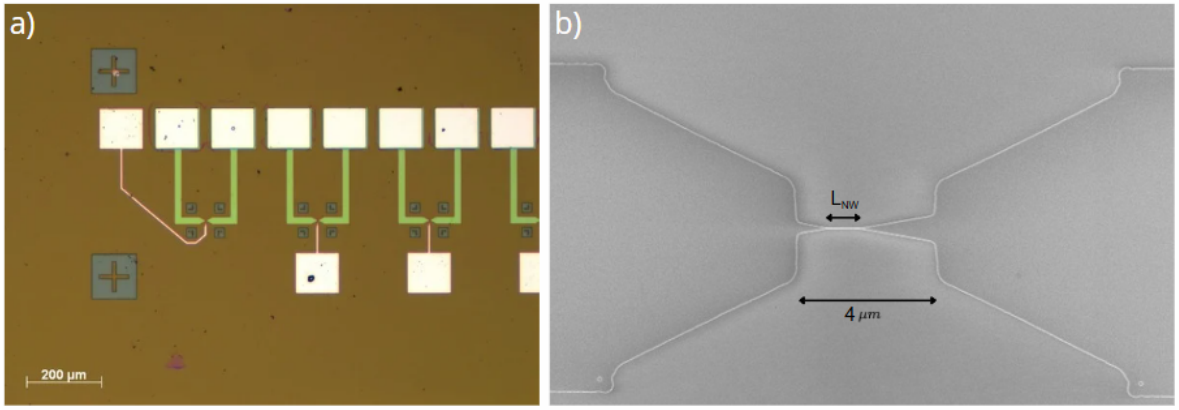
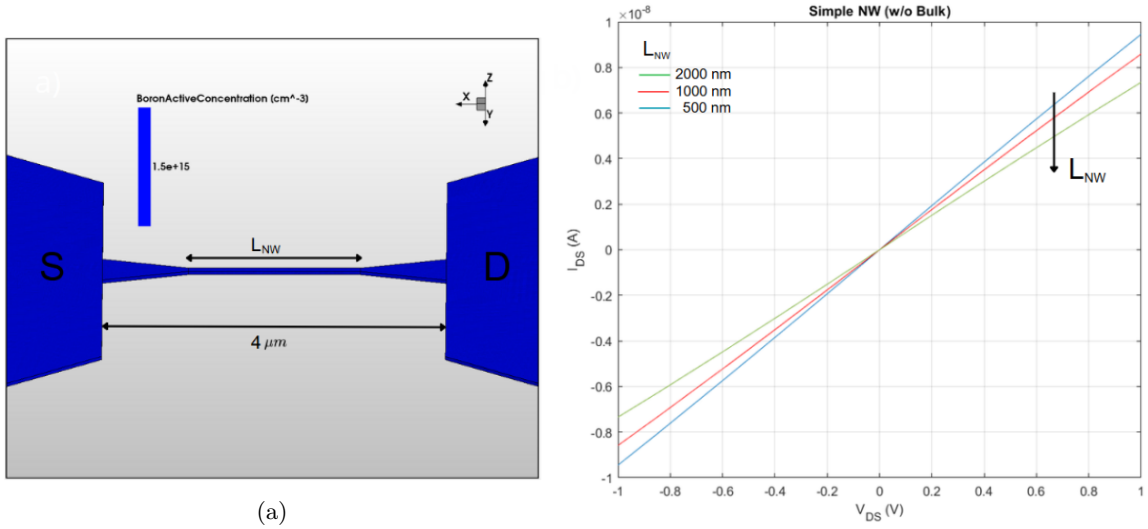


Figure 5.2: Manufactured FDSOI nanowires. a) Nanowires with Source, Drain and Gate Aluminum pads, b) zoomed SEM image of a nanowire without the gate electrode.

Figure 5.3b shows the simulated voltage-current characteristic for simple nanowires lightly doped with Boron atoms ($N_A = 1.5 \times 10^{15}\ cm^{-3}$), for different lengths.



(a) (b)

Figure 5.3: TCAD simulations of a simple nanowire without bulk. a) Structure of a simple NW lightly doped with $N_A = 1.5 \times 10^{15}\ cm^{-3}$ Boron atoms. b) $I_d - V_d$ curve simulated for different NW lenghts.

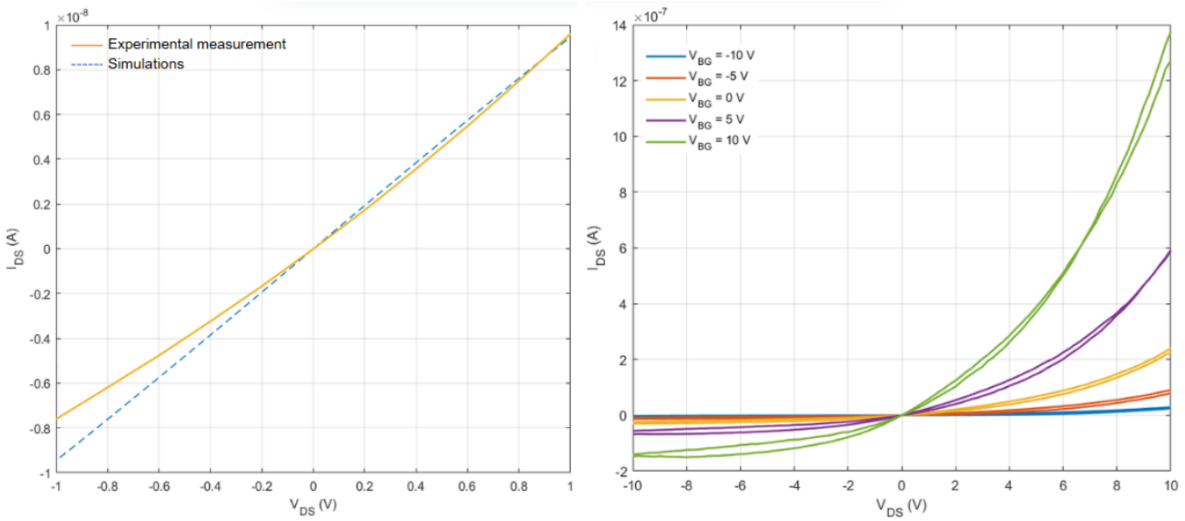
As expected, the trend obtained in the range from -1 V to 1 V is linear, and the resistance values are compatible with the theoretical ones calculated from:

$$R = \rho \frac{L_{NW}}{A_{NW}} \tag{5.1}$$

considering a resistivity equal to $\rho = 8 \times 10^{-12}\ \Omega\ cm$.

For nanowires of length 500 nm, 1000 nm and 2000 nm, resistances of 105.1 $M\Omega$, 115.6 $M\Omega$ and 134.98 $M\Omega$ are obtained, respectively.

The linear trend is also observed in the electrical measurements performed on the devices within a small drain voltage range (V_{DS} ranging from -1 to 1 V in Figure 5.4a), showing resistance values very similar to those predicted by the simulations. However, the voltage-current characteristic for higher voltage values shows a rectifying behavior rather than a linear one (Figure 5.4b).



(a) (b)

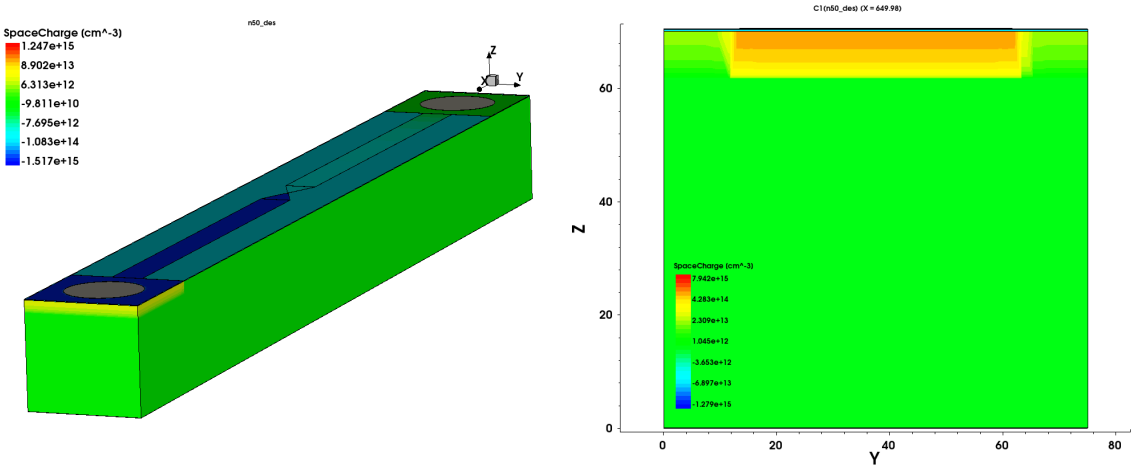
Figure 5.4: Electrical measurements of the manufactured nanowires. a) Comparison between the simulated and experimentally measured nanowire $I_{DS} - V_{DS}$ curves, with V_{DS} ranging form -1 V to 1 V. b) $I_{DS} - V_{DS}$ curves measured experimentally for various bulk voltages. Rectifying behaviour showing up for high values of V_{DS} is clearly visible.

This effect can be explained by considering the influence of the SOI substrate, which modifies the carrier density in the nanowire depending on the applied drain voltage.

5.1.1 Rectifying Behavior Induced by Substrate-Driven Carrier Modulation

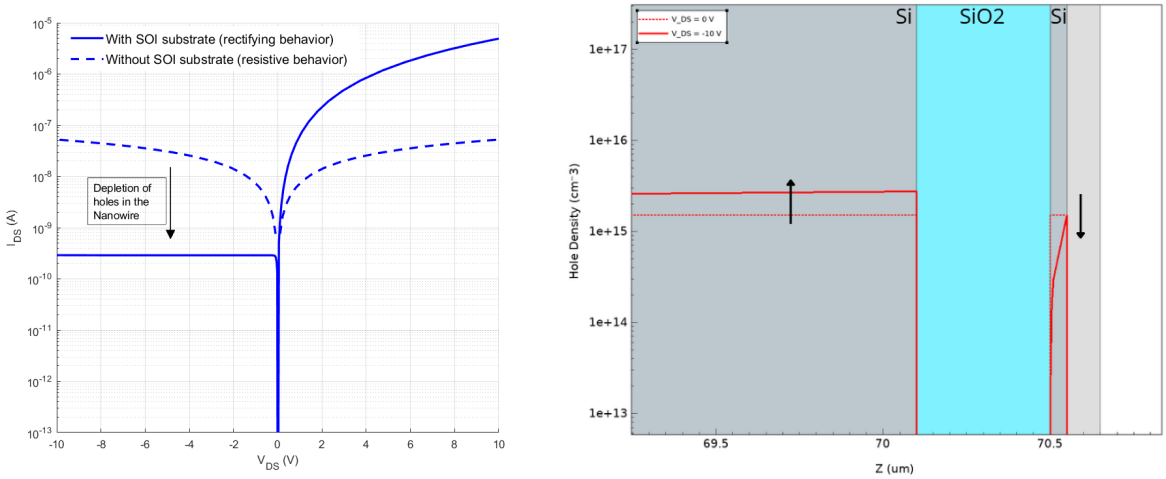
To understand the influence of the bulk on the behavior of the nanowire, let's analyze what happens to the current for positive and negative V_{DS}.

- For $V_{DS} < 0$ some positive charge accumulates in the bulk at the interface with the BOX, consequently the density of majority carriers (holes in this case) in the active silicon layer near the drain contact is reduced, resulting in a lower current;



(a) (b)

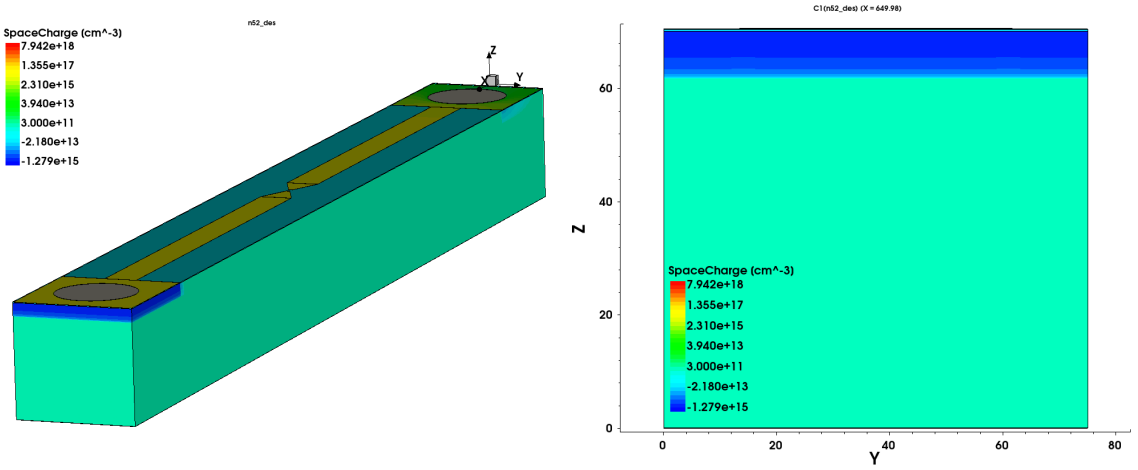
Figure 5.5: Space charge plot at V_{DS}=-10 V. a) 3D plot and b) 2D plot corresponding to cut C1 at the drain contact.



(a) (b)

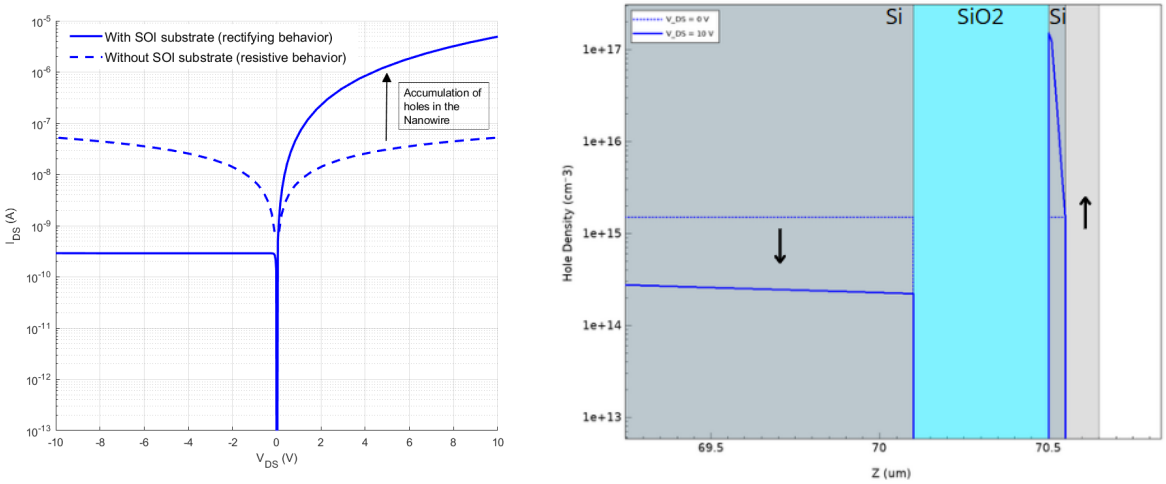
Figure 5.6: a) Comparison between the I_{DS}-V_{DS} characteristic simulated with (solid lines) and without (dashed lines) SOI substrate. For negative values of V_{DS}, the total current decreases when the influence of the substrate is accounted. b) Hole concentration profile in a 1D cut below the drain contact, due to the positive charge accumulated in the bulk at the interface with the oxide, the number of holes (majority carriers) decreases in the silicon overlayer.

- For $V_{DS} > 0$ some negative charge accumulates in the bulk at the interface with the BOX, consequently the majority carrier density in the silicon overlayer increases, resulting in a higher current, which increases with the applied voltage.



(a) (b)

Figure 5.7: Space charge plot at V_{DS}=10 V. a) 3D plot and b) 2D plot corresponding to cut C1 at the drain contact.



(a) (b)

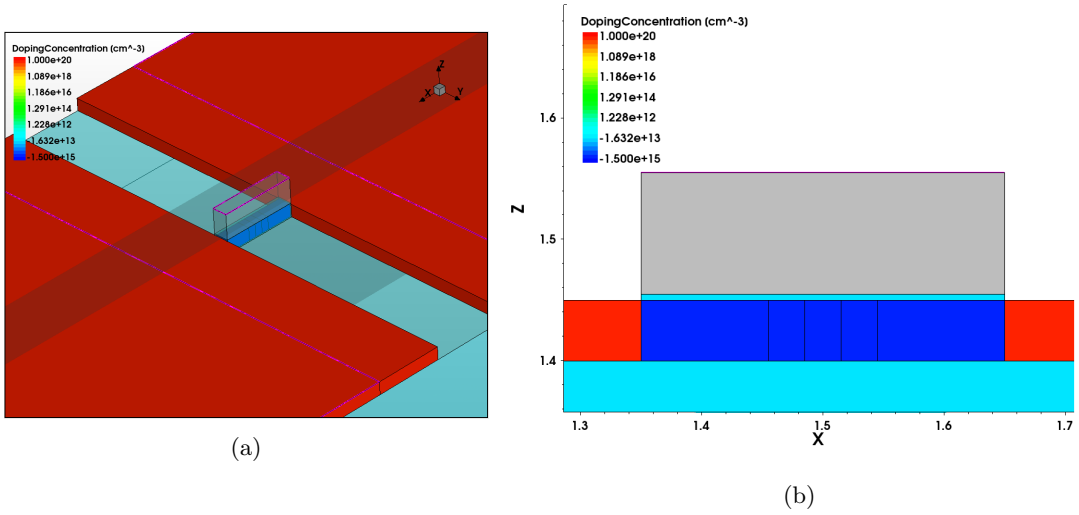
Figure 5.8: a) Comparison between the I_{DS}-V_{DS} characteristic simulated with (solid lines) and without (dashed lines) SOI substrate. For positive values of V_{DS}, the total current decreases when the influence of the substrate is accounted. b) Due to the negative charge accumulated in the bulk at the interface with the oxide (hole depletion), the number of holes increases in the silicon overlayer.

In any case, the nanowire SET should work in a very low voltage range, on the order of tens of millivolts, in this range the fabricated devices exhibit correct resistive behavior.

5.2 Nanowire Field-Effect Transistor

?? Before analyzing the behavior of a nanowire dedicated to the realization of SETs for the readout of spin quibits, it is useful to simulate a simple FDSOI nanowire FET, that is, a nanowire with a single gate (hereinafter called the lead gate) that controls the charge population along the entire channel. This stage is necessary to verify that the device behaves like a regular transistor, and to extract its important parameters, among all the threshold voltage. Figure 5.9a shows the 3D structure of the simulated FET nanowire, fabricated from a SOI substrate lightly doped with Boron atoms ($N_A = 15 \times 10^{14}\ cm^{-3}$), with Source and Drain regions implanted with Phosphorus atoms ($N_D = 1 \times 10^{20}\ cm^{-3}$). Figure 5.9b shows a 2D cross-section cut along the length of the nanowire.

The nanowire has a cross-section (square) of size 50 nm x 50 nm, one dimension is patterned during the EBL stage, the other corresponds to the thickness of the silicon overlay of the SOI wafer. The thickness of the gate oxide surrounding the nanowire is 5 nm.

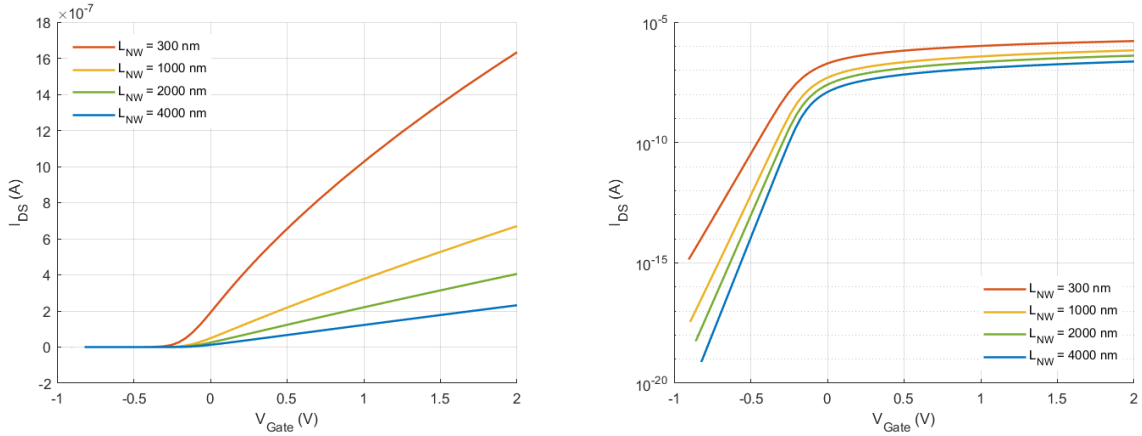


(a) (b)

Figure 5.9: Nanowire top-gated FET. a) 3D structure and b) cross secion along the lenght of the nanowire.

In Figure 5.10 the transcharacteristic $Id - Vg$ curve of the device is shown, for different nanowire lengths (i.e. 400 nm, 1000 nm, 2000 nm and 4000 nm). As it can be appreciated, with decreasing length:

- the saturation current increases as the resistance of the nanowire decreases, owing to the reduced channel length. Since $I_{\text{sat}} \propto 1/L$ in the linear regime, shorter channels exhibit less voltage drop and allow a higher drive current.
- the SS of the device worsens (i.e. increases), due to short-channel effects such as drain-induced barrier lowering (DIBL) and increased influence of source/drain potentials on the channel.
- the threshold voltage decreases slightly as the channel length is reduced.



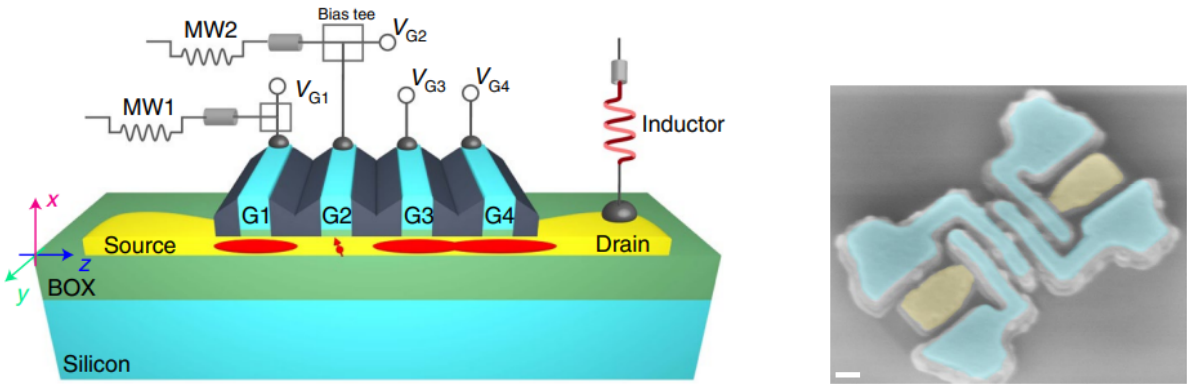
(a) (b)

Figure 5.10: $I_d - V_g$ characteristics of the device for different lengths in a) linear and b) logarithmic scale

5.2.1 Nanowire with multiple gates

A nanowire based device allows for greater control over charge confinement, and also eliminates the parasitic current problem observed for planar devices. This is why these types of structures are particularly interesting in the context of quantum computing based on electrostatically defined quantum dots.

In Figure 5.11 a platform for quantum computing based on a FDSOI nanowire with four gates is shown, taken from the work presented in [31]. In this case the device is a p-type FET, with a fully intrinsic nanowire. Gate G_2 serves to maintain the confinement of a single hole, whose spin will encode the quantum information of the qubit. Gates G_3 and G_4 instead serve to define a hole island used as reservoir and sensor for hole spin readout. Also in this case the readout is based on the 'Elzerman' spin-to-charge conversion method, but instead of using a SET to detect tunneling, dispersive radiofrequency reflectometry is used. Gate G_1 is used to provide a screening from the disorder introduced by the source region.



(a) (b)

Figure 5.11: a) Three-dimensional representation of a SOI nanowire device with four gates and b) SEM image of the device [31].

The simulated structures can be easily adapted to a similar configuration. Figure 5.12 shows 3D views of the simulated devices, with three and five gates.

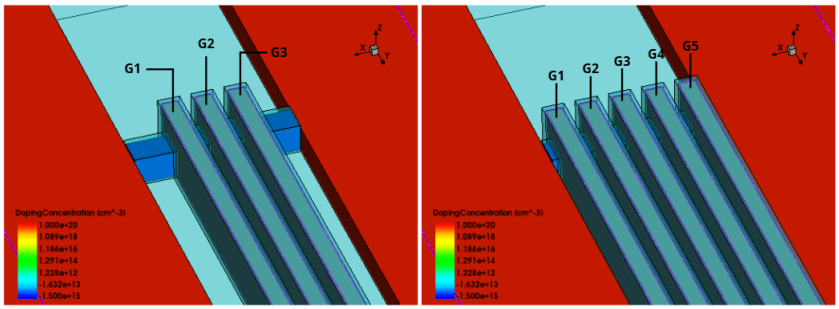
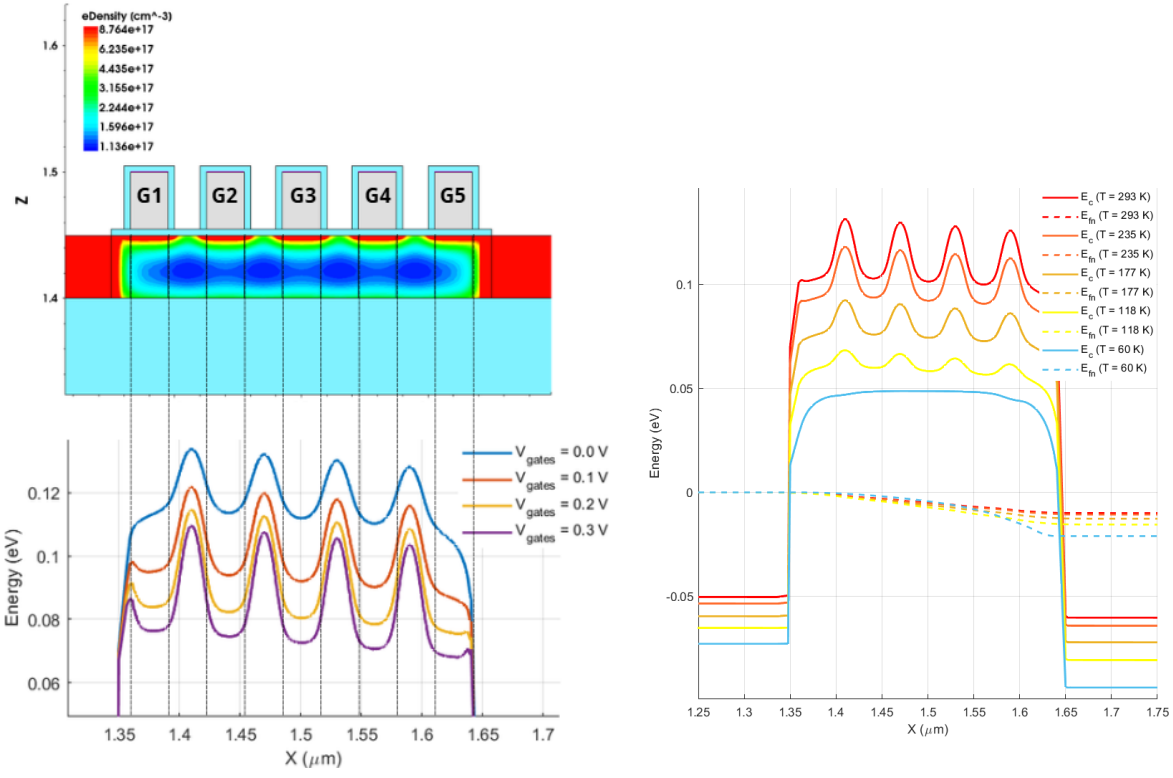


Figure 5.12: Simulated FDSOI nanowire-based qubit platform, featuring devices with three (left) and five (right) wrap-around gates.

In the following, some simulations performed on a nanowire device with five gates are presented.



(a) (b)

Figure 5.13: a) Electron density (top) with barrier gate voltage $V_b = 0.3\,\mathrm{V}$ and conduction band profile (bottom) for V_b from 0.0 V to 0.3 V. Minima correspond to gate positions, maxima to uncovered regions. b) Conduction band profile at $V_b = 0.0\,\mathrm{V}$ versus temperature, showing band flattening at low temperatures due to lack of thermally generated carriers.

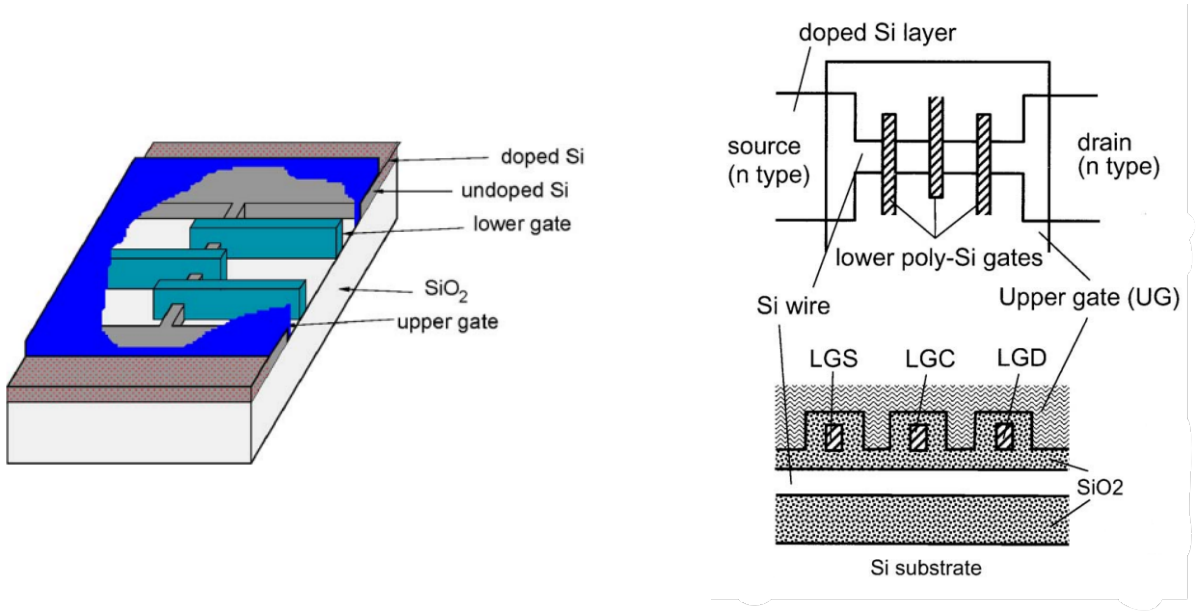
Figure 5.13a (upper plot) shows the electron density in the device with equal barrier gate voltages applied, set to $V_b = 0.3\,\mathrm{V}$. The plot below displays the conduction band profile along the nanowire channel for V_b ranging from 0.0 V to 0.3 V. The minima of the conduction band correspond to the positions of the barrier gates, while the maxima appear in the uncovered regions.

Figure 3.13b shows the conduction band profile for $V_b = 0.0\,\mathrm{V}$ as a function of temperature. It is interesting to note the flattening of the band diagram at low temperatures, caused by the lack of thermally generated carriers capable of screening the potential.

The presented structure is not very robust in terms of convergence due to the multiple voltages that must be managed, which makes the system more unstable, especially at low temperatures. Therefore, in the following sections, a similar structure with only three gates will be discussed, specifically designed to operate as a single-electron transistor.

5.3 Nanowire SET low-T simulations

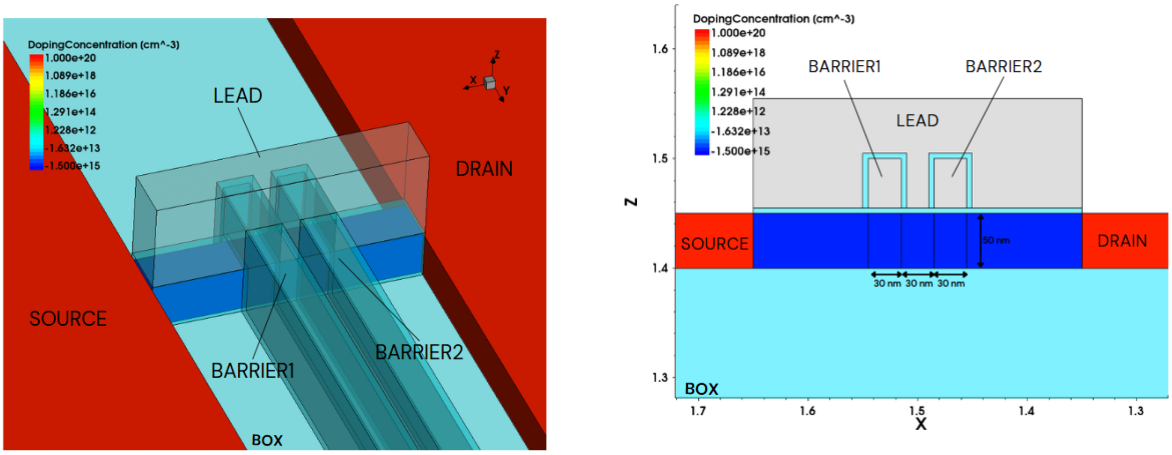
In this section, we discuss a nanowire-based SET, which operates on principles very similar to the planar device described in the previous chapter. Figure 3.13 shows some reference devices reported in the literature [41][12].



(a) (b)

Figure 5.14: Examples of nanowire-based SETs, consisting of three gates to control the tunneling barriers and an upper gate to modulate charge accumulation in the channel and in the quantum dot. a) Schematic representation of the device presented in [41]. b) Top view and cross-sectional view of the device discussed in [12].

Figure 5.15 shows the structure of the simulated device. The dimensions and materials used are almost identical to those of the planar SET; however, in this case, the intermetal oxide separating the upper gate from the barrier gates is silicon oxide instead of aluminum oxide.



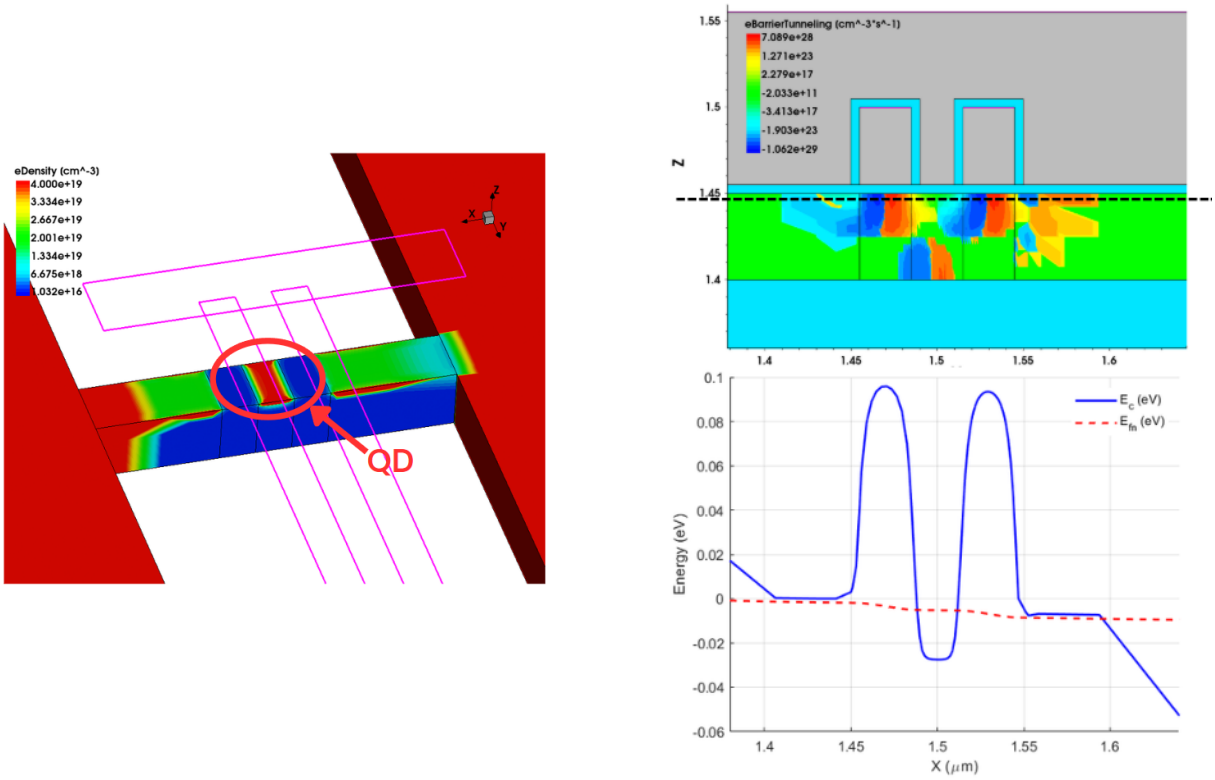
(a) (b)

Figure 5.15: Nanowire SET structure. a) 3D view and b) 2D cut along the nanowire length. For these specific simulations the nanowire has a length of 300 nm, a square cross-section of 50 nm x 50 nm and aluminum gates with a thickness of 30 nm, separated by a distance of 30 nm.

Given the simplicity of this configuration, the simulations are more robust at low temperatures, which is why it is possible to perform analyses for temperatures down to T=20 K before convergence problems arise.

Figure 5.16a shows a 3D plot of the spatial distribution of electrons in the structure at room temperature, for a gate voltage value well above the threshold, so as to create a well-defined conduction channel, while the barriers are kept at $V_{b1} = V_{b2} = 0.0$ V so as to locally deplete the regions below them and provide the confinement. Referring to the transcharacteristic of the nanowire FET shown in Section **??**, the lead gate was set to $V_{lead} = 2.0$. Under these conditions the electron density in the quantum dot is of the order of 10^{19} electrons/cm^3, having a quantum dot with dimensions equal to 50 nm x 30 nm x 5 nm, or 7500 nm^3, we can estimate that the number of electrons in the dot is of the order of 10^2.

Figure 5.16b shows a cross-section of the channel (upper plot), with the tunneling rate of electrons through the barriers, and the conduction band profile (lower plot) in the 1D cut corresponding to the black dashed line in the cross-section. At room temperature, the charge flow is not completely localized at the interface of the silicon with the gate oxide, resulting in electrons flowing also in the lower part of the nanowire, where tunneling is observed through a peak in the conduction band profile, approximately at the center of the QD. This contribution disappears at low temperatures, as shown in Figure 5.17.



(a) (b)

Figure 5.16: a) Electron density distribution in the device, for $V_{Lead} = 2.0$ V and $V_{B1} = V_{B2} = 0.0$ V, b) section of the nanowire with electron tunneling rate for the same voltage values and conduction band profile corresponding to the black dashed line.

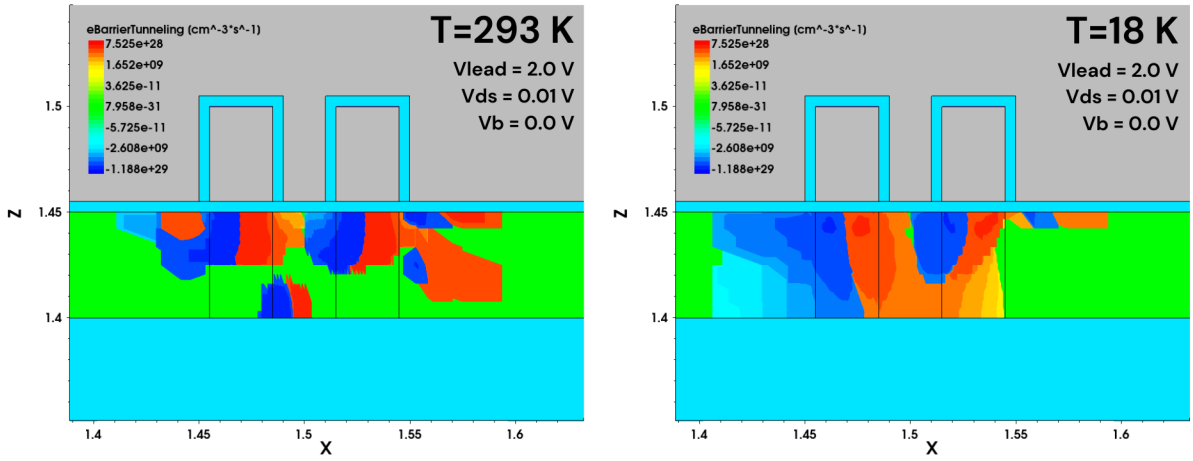


Figure 5.17: Electron tunneling rate: comparison between T=293 K and T=18 K.

As can be appreciated from the conduction band profile, the potential barriers formed by the barrier gates are too thick (about 30 nm) to observe significant tunneling. The major contribution to the tunneling current is given by the electrons close in energy to the energy maximum of the barriers (in a range of some millielettronvolts), where the profile is more tapered and the thickness perceived by the electrons is smaller, also due to the Fowler-Nordheim (FN) effect caused by the voltage V_{DS}. However, for temperatures outside the millikelvin regime, the noisy current contribution due to thermionic emission will always be larger than that due to tunneling, making it impossible to distinguish single-electron effects (Figure 5.18).

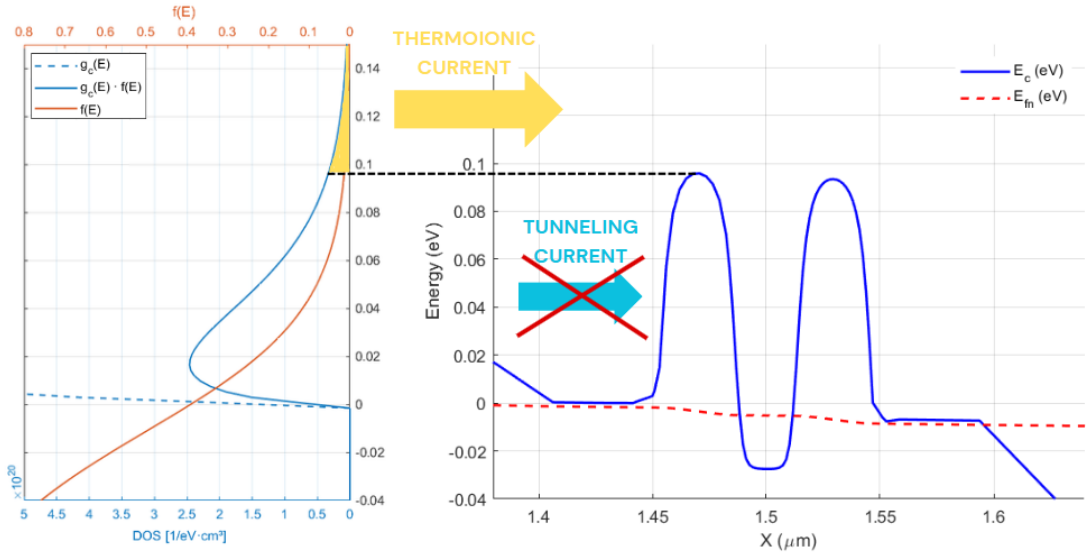


Figure 5.18: Plot of the conduction band profile in the channel at room temperature, along with the corresponding electron distribution. The parabolic approximation was used for the density of states. Due to thermal broadening, a significant number of electrons have enough energy to overcome the potential barriers via thermionic emission, while only a small fraction of electrons are energetically aligned with the conduction band maximum, where the barrier thickness allows for an appreciable tunneling probability.

5.3.1 Low-T simulations

In order to maximize the tunneling-to-thermionic current ratio, the device must operate in the millikelvin regime. At temperatures near absolute zero the Fermi distribution becomes abrupt (Figure 5.19a. Thus, if the voltages applied to the barrier gates are such that the quasi-Fermi level of the electrons is energetically aligned with the barrier maximum (this occurs near the threshold voltage for the barriers), no electrons will have enough thermal energy to tunnel through the barriers, but there will be a considerable amount of electrons available to tunnel through the tips of the barriers (Figure 5.19b).

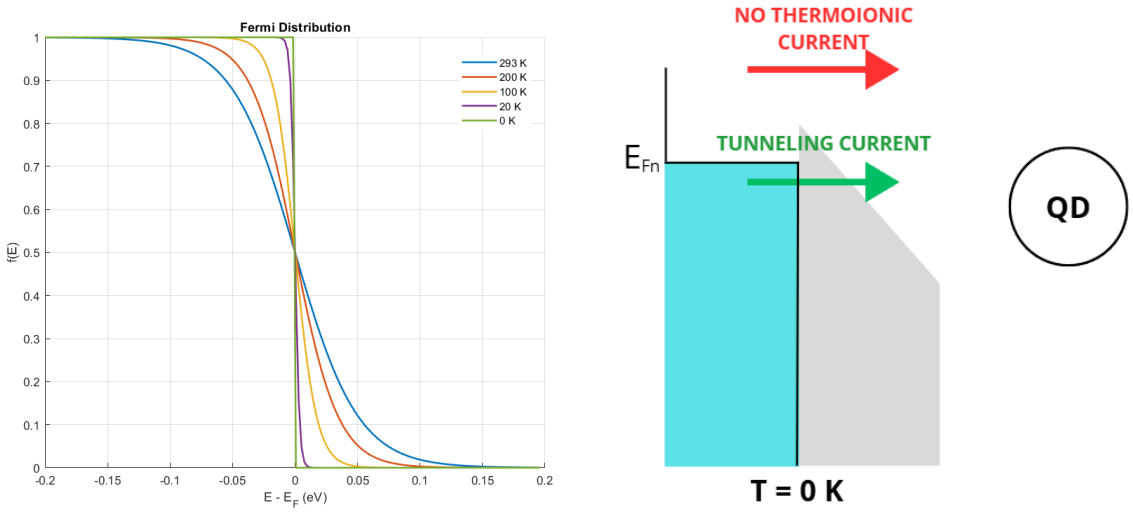
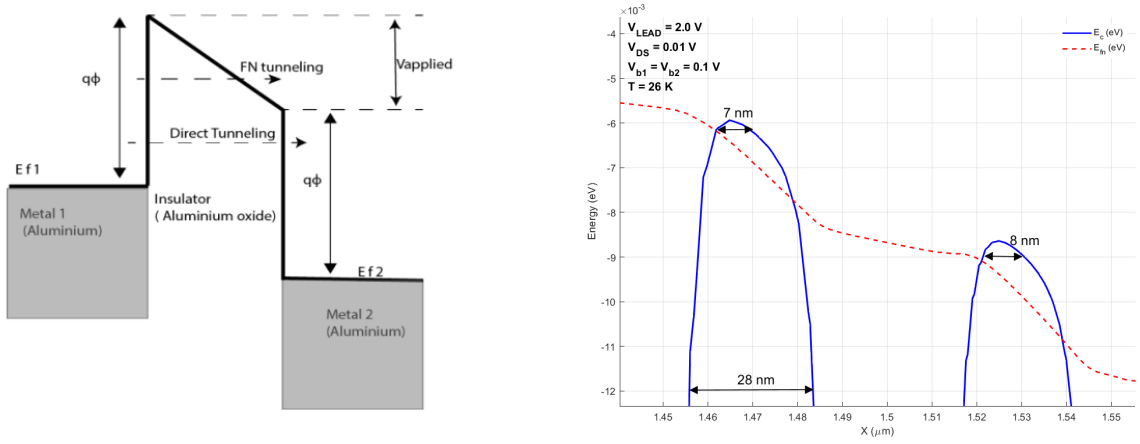


Figure 5.19: a) Fermi distribution for temperatures ranging from T = 293 K to T = 0 K. b) Schematic illustration of electron tunneling through the electrostatically defined barrier; at absolute zero, the thermionic current contribution is zero.

In this regard, the role of the Source-Drain voltage plays a fundamental role. In fact, due to the potential drop, localized almost entirely on the barriers since it is the region with the highest resistance, the top of the barriers assumes a triangular shape due to the resulting electric field. As a consequence, electrons energetically aligned with the maximum of the barriers perceive a reduced thickness and the tunneling rate is significantly higher than direct tunneling, which instead occurs through the entire thickness of the barriers, in the underlying part. This effect is known as Fowler-Nordheim tunneling [24], and is also the main tunneling mechanism through the gate oxide in nanometric transistors.



(a) (b)

Figure 5.20: a) Fowler–Nordheim tunneling through an intermetal layer of aluminum oxide [24]. b) Simulated band diagram at T = 26 K of the nanowire-based SET.

Figure 5.20b shows the conduction band profile under conditions of fully formed inversion layer (V_{Lead}=2.0 V) and barrier gate voltage close to the threshold (V_{th} = 0.1 V) for the minimum temperature that was possible to simulate in this condition, i.e. T = 26 K. The FN effect is appreciable, however the temperature is still too high to have zero thermionic current. Indeed, at this temperature the thermal energy is of the order of some electronvolt:

$$\Delta E = k_B T \approx 2.24\ meV \tag{5.2}$$

Another reason why these devices need to work at low temperatures has already been discussed in Chapter 2 and concerns the charge energy of the QD. As already mentioned, to observe single-electron effects, the charge energy of the QD must be much larger than the thermal energy of the electrons:

$$E_C \gg k_B T \Longrightarrow T \ll \frac{E_C}{k_B} \tag{5.3}$$

This requirement becomes more stringent for larger QDs, which have a higher capacitance and therefore a lower charge energy. Furthermore, it should be considered that temperature has a detrimental effect on the decoherence times of spin-qubits; in general, quantum computing systems always operate in cryogenic apparatus.

Due to convergence issues, it was not possible to obtain a reliable description of the device in the millikelvin range. Instead, we extracted the temperature dependence of the main parameters. To enable this, the simulation was adapted to be more robust at low temperatures. In particular:

- The hydrodynamic model with Fermi statistics was used [35]. The expressions for the current densities in the hydrodynamic model, used for solving the continuity equations, are:

$$\vec{J}_n = \mu_n \left(n\nabla E_{\mathrm{C}} + kT_n \nabla n - nkT_n \nabla \ln \gamma_n + \lambda_n f_n^{\mathrm{td}} kn \nabla T_n - 1.5 nkT_n \nabla \ln m_n \right) \tag{5.4}$$

$$\vec{J}_p = \mu_p \left(p\nabla E_{\mathrm{V}} - kT_p \nabla p + pkT_p \nabla \ln \gamma_p - \lambda_p f_p^{\mathrm{td}} kp \nabla T_p + 1.5 pkT_p \nabla \ln m_p \right) \tag{5.5}$$

  where the first term accounts for the carriers drift due to the spatial variations of electrostatic potential, electron affinity, and the band gap, the second one is the diffusion term, the third one corrects for Fermi–Dirac statistics in highly doped or low-temperature regimes, the fourth term is the diffusion term and takes into account the current generated by temperature gradients (Seebeck effect), the last one is related to variations of the effective mass in the device. The reason why this model is more robust at low temperatures than the classical drift-diffusion model lies in the third term, which accounts for semiconductor degeneration under low-temperature conditions.

- A model for incomplete activation of dopants has been employed [35], since at low temperatures the thermal energy $k_B T$ is not high enough compared to the activation energy of dopants (Phosphorus) in Silicon to ensure complete ionization of the dopant species. Since $N_{D,0}$ and $N_{A,0}$ are the substitutional (active) donor and acceptor concentrations, the concentration of ionized dopants is given by:

$$N_{\mathrm{D}} = \frac{N_{\mathrm{D},0}}{1 + g_{\mathrm{D}} \exp\left(\frac{E_{\mathrm{F},n} - E_{\mathrm{D}}}{kT}\right)} = \frac{N_{\mathrm{D},0}}{1 + g_{\mathrm{D}} \frac{n}{n_1}} \text{ for } N_{\mathrm{D},0} < N_{\mathrm{D,\ crit}} \tag{5.6}$$

$$N_{\mathrm{A}} = \frac{N_{\mathrm{A},0}}{1 + g_{\mathrm{A}} \exp\left(\frac{E_{\mathrm{A}} - E_{\mathrm{F},p}}{kT}\right)} = \frac{N_{\mathrm{A},0}}{1 + g_{\mathrm{A}} \frac{p}{p_1}} \text{ for } N_{\mathrm{A}} < N_{\mathrm{A,\ crit}} \tag{5.7}$$

with $n_1 = \gamma_n N_C \exp\left(-\frac{\Delta E_D}{kT}\right)$ and $p_1 = \gamma_p N_V \exp\left(-\frac{\Delta E_A}{kT}\right)$, where γ_n, γ_p are coefficients that account for the Fermi statistics.

- The carrier temperature equations are solved together with Poisson and carrier density equations in a quasi-static loop to gradually lower the temperature, following a sequence of similar quasi-static loops used to ramp all terminal voltages to their final values. This approach improves convergence, but its drawback is that it does not allow for other kinds of analysis once the minimum temperature is reached, as the system becomes highly sensitive and unstable in that regime.

In figure 5.21 the conduction band profiles and quasi-Fermi levels of electrons of the 300 nm long SET Nanowire are shown for different temperatures, down to the minimum achievable, i.e. 18 K. For clarity, only the quasi-Fermi levels at room temperature and at 18 K are shown.

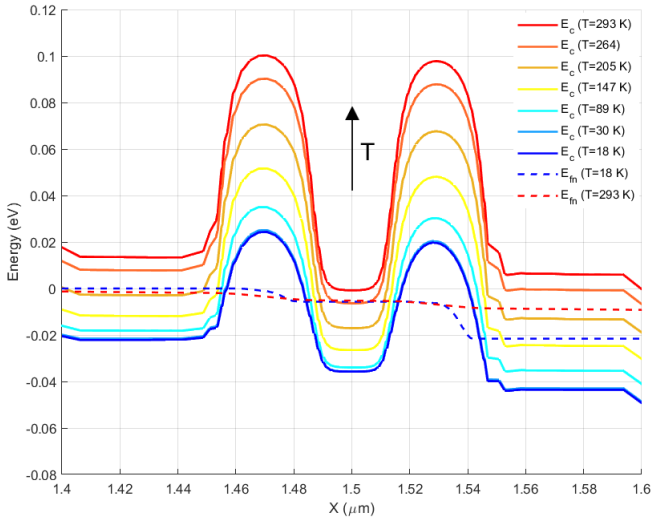
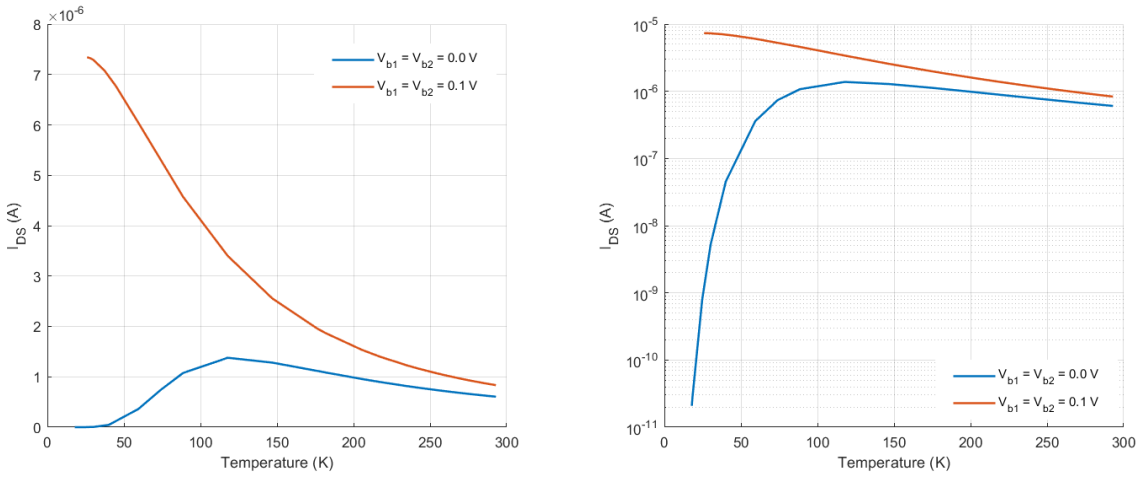


Figure 5.21: Conduction band profile for temperatures ranging from T = 293 K to T = 18 K. The electron quasi-Fermi level is shown for the two extreme temperature values. At low temperatures, fewer electrons have sufficient thermal energy to overcome the barriers. As a result, the barrier region becomes more resistive, and the entire voltage drop occurs across it.

At sufficiently low temperatures, the MOSFET channel becomes degenerate, as theorized in [21, 37], due to the electrostatically induced inversion layer and the sharp occupation of energy states near the conduction band edge, as electrons follow a step-like Fermi-Dirac distribution.

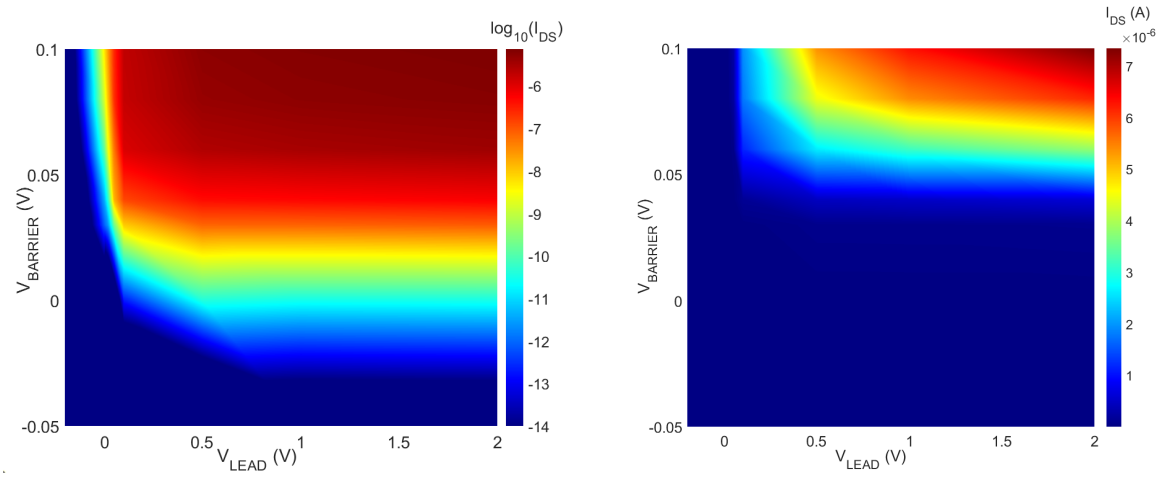
In Figure 5.22 we plot (in linear and logarithmic scale) the drain-to-source current when the gate voltage is well above the threshold ($V_{Lead} = 2.0$ V, i.e. the channel is completely formed) and the voltage applied to the barriers are $V_b = 0.0$ V and $V_b = 0.1$ V. The plot shows what was previously stated in Chapter 4 about the planar structure, in fact the application of a positive voltage at room temperature decreases the current but is not able to cut the conduction, since the channel can bend towards the substrate. At very low temperatures this effect vanishes, the only possible conduction occurs in a thin layer at the interface with the oxide and therefore a positive barrier voltage leads to a current of almost six orders of magnitude smaller at T=18 K. It is reasonable to expect that at millikelvin temperatures the current is practically zero for the same applied voltage.



(a) (b)

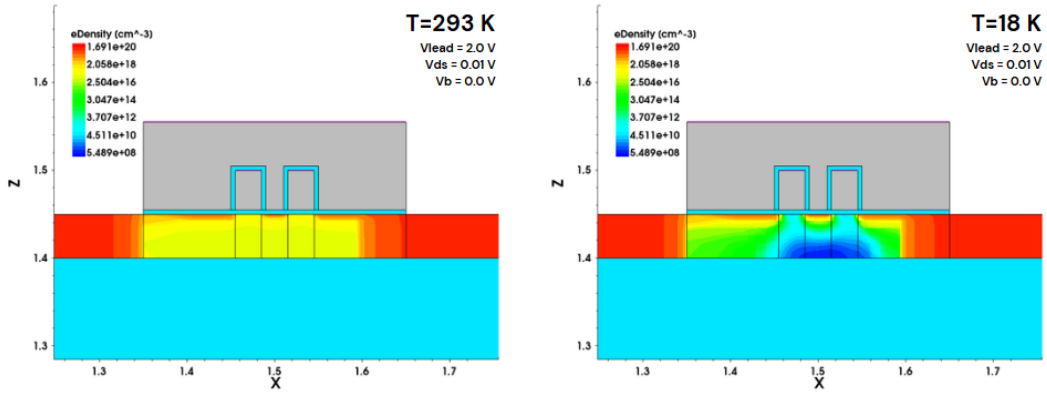
Figure 5.22: Drain current as a function of temperature (down to 18 K) for barrier gate voltages of V_b = 0.0 V (blue line) and V_b = 0.1 V (red line), shown in a) linear and b) logarithmic scale. The plots indicate that at room temperature, a gate voltage of V_b = 0.0 V is not sufficient to suppress conduction, as already discussed in the previous chapter, whereas at low temperatures it is.

Figure 5.23 instead shows a 2D colored plot at T=20 K of the drain-to-source current as a function of the barrier voltage and the lead gate voltage, in a range that includes both thresholds. As expected from the literature (see Figure 2.12), a rectangular window is obtained for which significant conduction occurs. In fact, to have a conductive channel, the lead gate voltage must be sufficiently positive to create the inversion layer, and the barrier voltage must be such as not to induce depletion in the channel.

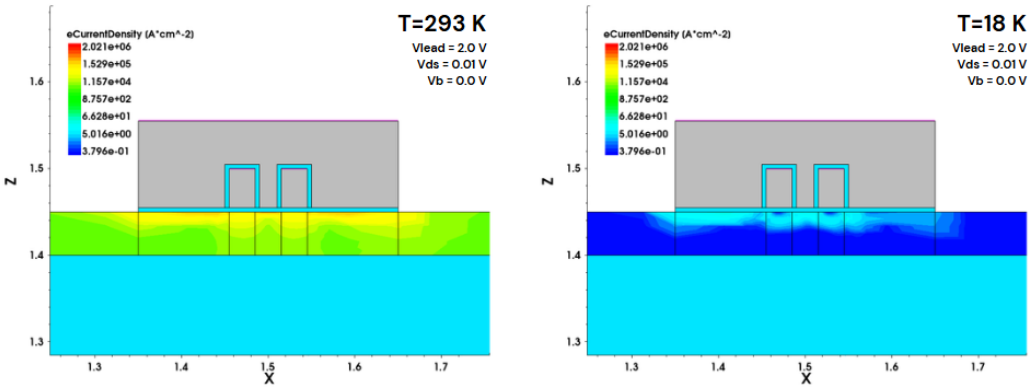


(a) (b)

Figure 5.23: Colored plot of the drain current as a function of V_{Lead} and V_b in a) logarithmic and b) linear scale, simulated at T = 20 K. The plots show well-defined thresholds, with the device turning on completely over a range of a few tens of millivolts.



(a)



(b)

Figure 5.24: Comparison of a) electron density and b) electron current density in the device at T = 293 K and T = 18 K. The applied voltages are the same (i.e., V_{DS} = 0.01 V, V_{Lead} = 2.0 V, and $V_{b1} = V_{b2} = 0.0$ V), showing that conduction is effectively suppressed only at low temperatures. Figure 3.13 further illustrates that at T = 18 K, conduction is strictly confined to the electrostatically induced electron channel, which is localized in a thin layer at the interface with the gate oxide.

Conclusions

The objective of this thesis was to develop a simulation model for gate-defined Single-Electron Transistors, in order to investigate the electrical behavior of devices currently under development at IMB-CNM, to guide their fabrication process, and to get as close as possible to the device's real working point. A trade-off between physical accuracy and simulation time led to the choice of TCAD simulations using Sentaurus by Synopsys, and in particular the semiclassical model based on the self-consistent solution of the Poisson and carrier density equations, i.e., sdevice. This allowed for straightforward investigation of fabricated devices and comparison of simulation results with electrical characterizations performed at room temperature, assisting in the correct interpretation of the observed behaviors. In particular, the rectifying behavior observed in FDSOI nanowire-based devices was highlighted, caused by the influence of the substrate on the active silicon layer, which modifies the majority carrier concentration at high applied voltages, and the effect of fixed charges at the oxide/semiconductor interface in planar devices, which results in a parasitic current that cannot be modulated by the lead gate, but can be modulated by the barrier gates due to the device layout.

However, this type of simulation does not allow for the study of single-electron effects or device behavior in the temperature range in which they are intended to operate, i.e., in the millikelvin regime. Switching to more advanced quantum transport models could solve both problems, providing greater robustness at ultra-low temperatures. The simulations performed were nonetheless adapted to achieve convergence at the lowest possible temperature, namely 18 K. This was done by adopting the hydrodynamic model with a quasi-stationary final ramping on temperature. The WKB model used to estimate the tunneling rate gives reasonable results, although at temperatures higher than a few millikelvin, the tunneling current is always negligible compared to the thermionic contribution.

Nevertheless, simulations allow for the extraction of meaningful results on the potential profile along the channel and the effect of different applied voltages, as well as on temperature dependence up to 18 K. Further studies could focus on the influence of materials and geometries on device behavior, as well as on the analysis of capacitive contributions, which determine the charging energy of the dot and the Coulomb blockade behavior.

Bibliography

[1] S. J. Angus et al. "Gate-Defined Quantum Dots in Intrinsic Silicon". In: *Nano Letters* 7.7 (July 2007), pp. 2051–2055. DOI: 10.1021/nl070949k.

[2] Fabio Bersano et al. "Multi-Gate FD-SOI Single Electron Transistor for hybrid SET-MOSFET quantum computing". In: Sept. 2022, pp. 49–52. DOI: 10.1109/ESSCIRC55480.2022.9911479.

[3] Paul Black, D. Kuhn, and Carl Williams. "Quantum Computing and Communication". In: *Advances in Computers* 56 (Dec. 2002), pp. 189–244. DOI: 10.1016/S0065-2458(02)80007-9.

[4] K. I. Bolotin et al. "Metal-nanoparticle single-electron transistors fabricated using electromigration". In: *Nano Letters or Unpublished preprint* (2003). Unpublished manuscript, Cornell University, Dated October 9, 2003. URL: https://arxiv.org/abs/cond-mat/0310573.

[5] G. Cao et al. "Ultrafast universal quantum control of a quantum-dot charge qubit using Landau–Zener–Stückelberg interference". In: *Nature Communications* 4 (2013), p. 1401. DOI: 10.1038/ncomms2412. URL: https://doi.org/10.1038/ncomms2412.

[6] "Chapter 12 - Temperature dependence". In: *FinFET Modeling for IC Simulation and Design*. Ed. by Yogesh Singh Chauhan et al. Oxford: Academic Press, 2015, pp. 245–260. ISBN: 978-0-12-420031-9. DOI: https://doi.org/10.1016/B978-0-12-420031-9.00012-9. URL: https://www.sciencedirect.com/science/article/pii/B9780124200319000129.

[7] D. Deutsch. "Quantum Theory, the Church–Turing Principle and the Universal Quantum Computer". In: *Proceedings of the Royal Society of London. A. Mathematical and Physical Sciences* 400.1818 (1985), pp. 97–117.

[8] David P. DiVincenzo. "The Physical Implementation of Quantum Computation". In: *Fortschritte der Physik* 48.9–11 (Sept. 2000), pp. 771–783. ISSN: 1521-3978. DOI: 10.1002/1521-3978(200009)48:9/11<771::aid-prop771>3.0.co;2-e. URL: http://dx.doi.org/10.1002/1521-3978(200009)48:9/11%3C771::AID-PROP771%3E3.0.CO;2-E.

[9] J. M. Elzerman et al. "Single-shot read-out of an individual electron spin in a quantum dot". In: *Nature* 430.6998 (July 2004), pp. 431–435. ISSN: 1476-4687. DOI: 10.1038/nature02693. URL: http://dx.doi.org/10.1038/nature02693.

[10] J.M. Elzerman et al. "Semiconductor Few-Electron Quantum Dots as Spin Qubits". In: vol. 667. Apr. 2005, pp. 289–331. ISBN: 978-3-540-24236-9. DOI: 10.1007/11358817_2.

[11] Hans-Andreas Engel and Daniel Loss. "Detection of Single Spin Decoherence in a Quantum Dot via Charge Currents". In: *Physical Review Letters* 86.20 (May 2001), pp. 4648–4651. ISSN: 1079-7114. DOI: 10.1103/physrevlett.86.4648. URL: http://dx.doi.org/10.1103/PhysRevLett.86.4648.

[12] Akira Fujiwara et al. "Single electron tunneling transistor with tunable barriers using silicon nanowire metal-oxide-semiconductor field-effect transistor". In: *Applied Physics Letters* 88 (Feb. 2006), pp. 053121–053121. DOI: 10.1063/1.2168496.

[13] T. A. Fulton and G. J. Dolan. "Observation of single-electron charging effects in small tunnel junctions". In: *Phys. Rev. Lett.* 59 (1 July 1987), pp. 109–112. DOI: 10.1103/PhysRevLett.59.109. URL: https://link.aps.org/doi/10.1103/PhysRevLett.59.109.

[14] Juan Jose Garcia Ripoll. *Quantum Information and Quantum Optics with Superconducting Circuits*. ISBN da completare se disponibile. Cambridge: Cambridge University Press, 2022.

[15] Lov K. Grover. "A fast quantum mechanical algorithm for database search". In: *Proceedings of the 28th annual ACM symposium on Theory of computing*. 1996, pp. 212–219.

[16] Y. He et al. "A two-qubit gate between phosphorus donor electrons in silicon". In: *Nature* 571.7765 (July 2019), pp. 371–375. ISSN: 0028-0836. DOI: 10.1038/s41586-019-1381-2.

[17] Dinh Hien, Huynh Thao, and Le Minh. "Modelling transport in single electron transistor". In: *Journal of Physics: Conference Series* 187 (Sept. 2009). DOI: 10.1088/1742-6596/187/1/012060.

[18] Torsten Hoefler, Thomas Haener, and Matthias Troyer. *Disentangling Hype from Practicality: On Realistically Achieving Quantum Advantage*. July 2023. DOI: 10.48550/arXiv.2307.00523.

[19] L. Hutin et al. "SOI CMOS technology for quantum information processing". In: *2017 IEEE International Conference on IC Design and Technology (ICICDT)*. 2017, pp. 1–4. DOI: 10.1109/ICICDT.2017.7993523.

[20] Man Ieong et al. "Comparison of raised and Schottky source/drain MOSFETs using a novel tunneling contact model". In: Jan. 1999, pp. 733–736. DOI: 10.1109/IEDM.1998.746461.

[21] M. Kantner and T. Koprucki. "Numerical simulation of carrier transport in semiconductor devices at cryogenic temperatures". In: *Optics and Quantum Electronics* 48.12 (2016), p. 543.

[22] Nai Shyan Lai et al. "Pauli Spin Blockade in a Highly Tunable Silicon Double Quantum Dot". In: *Scientific reports* 1 (Oct. 2011), p. 110. DOI: 10.1038/srep00110.

[23] Wei Lu et al. "Lu, W., Ji, Z., Pfeiffer, L., West, K. W. Rimberg, A. J. Real-time detection of electron tunnelling in a quantum dot. Nature 423, 422-425". In: *Nature* 423 (June 2003), pp. 422–5. DOI: 10.1038/nature01642.

[24] Ajay Manwani, Rajesh Junghare, and Abhishek Vaidya. "Modelling of tunnelling currents in metal-insulator-metal junction". In: *International Journal of Microelectronics Engineering (IJME)* 1.1 (2015), pp. 1–5.

[25] R. Maurand et al. "A CMOS silicon spin qubit". In: *Nature Communications* 7.1 (Nov. 2016), p. 13575. DOI: 10.1038/ncomms13575.

[26] A. Morello et al. "Single-shot readout of an electron spin in silicon". In: *Nature* 467 (2010), pp. 687–691. DOI: 10.1038/nature09392. URL: https://doi.org/10.1038/nature09392.

[27] Mikio Nakahara. *Quantum Computing: From Linear Algebra to Physical Realizations*. en. 0th ed. CRC Press, Mar. 2008. ISBN: 978-0-429-14651-0. DOI: 10.1201/9781420012293. URL: https://www.taylorfrancis.com/books/9781420012293 (visited on 04/04/2025).

[28] Samuel Neyens et al. "Probing single electrons across 300-mm spin qubit wafers". In: *Nature* 629 (May 2024). Open access, published online: 1 May 2024, pp. 782–787. DOI: 10.1038/s41586-024-07275-6.

[29] Michael A. Nielsen and Isaac L. Chuang. *Quantum Computation and Quantum Information*. Cambridge University Press, 2010.

[30] J Petta et al. "Applied physics: Coherent manipulation of coupled electron spins in semiconductor quantum dots". In: *Science (New York, N.Y.)* 309 (Oct. 2005), pp. 2180–4. DOI: 10.1126/science.1116955.

[31] N. Piot et al. “A single hole spin with enhanced coherence in natural silicon”. In: *Nature Nanotechnology* 17.10 (Oct. 2022), pp. 1072–1077. DOI: 10.1038/s41565-022-01196-z.

[32] Stephanie Reimann and Matti Manninen. “Electronic Structure of Quantum Dots”. In: *Rev. Mod. Phys.* 74 (Nov. 2002). DOI: 10.1103/RevModPhys.74.1283.

[33] Pol Gaya Salas. “Design and Fabrication of Semiconductor Spin Qubits for Quantum Computing: Electrical Characterization”. Supervised by Francesc Pérez-Murano; co-supervised by Esteve Amat Bertran; academic tutor: Núria Barniol Beumala. Unpublished. Master’s thesis. Universitat Autònoma de Barcelona, 2025.

[34] Robert J. Schoelkopf et al. “The radio-frequency single-electron transistor (RF-SET): A fast and ultrasensitive electrometer”. In: *Science* 280.5367 (May 1998), pp. 1238–1242. ISSN: 0036-8075. DOI: 10.1126/science.280.5367.1238.

[35] *Sentaurus Device User Guide*. Version K-2015.06. Confidential documentation provided under license agreement. Synopsys, Inc. Mountain View, CA, 2015.

[36] Peter W. Shor. “Polynomial-Time Algorithms for Prime Factorization and Discrete Logarithms on a Quantum Computer”. In: *SIAM Journal on Computing* 26.5 (1997), pp. 1484–1509.

[37] J.-J. Sim and J. B. Kuo. “An Analytical Delayed-Turn-Off Model for Buried-Channel PMOS Devices Operating at 77 K”. In: *IEEE Transactions on Electron Devices* 39.4 (Apr. 1992), pp. 939–947.

[38] Ziyin Sun. “Design and Development of Single-Electron Transistors Based on SOI Nanowire Platform”. Unpublished. Master’s thesis. Universitat Autònoma de Barcelona, 2025.

[39] M. Veldhorst et al. “An addressable quantum dot qubit with fault-tolerant control fidelity”. In: *Nature Nanotechnology* 9.12 (2014), pp. 981–985. DOI: 10.1038/nnano.2014.216.

[40] Wikipedia contributors. *Bloch sphere — Wikipedia, The Free Encyclopedia*. Accessed: 2025-07-13. 2024. URL: https://en.wikipedia.org/wiki/Bloch_sphere.

[41] Neil Zimmerman et al. “Electrostatically gated Si devices: Coulomb blockade and barrier capacitance”. In: *Applied Physics Letters* 89 (July 2006), pp. 052102–052102. DOI: 10.1063/1.2240600.

[42] Floris A. Zwanenburg et al. “Silicon quantum electronics”. In: *Reviews of Modern Physics* 85.3 (2013), pp. 961–1019. DOI: 10.1103/RevModPhys.85.961.

List of Figures