

POLITECNICO DI TORINO

Master's Degree
in Nanotechnologies For ICTs

Master's Degree Thesis

**Process Simulation and Compact Modelling for a Vertical
Junctionless Nanowire Transistor**



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Academic Year 2024-2025

Ai miei genitori

† A mio nonno Antonio

Summary

MOSFET have dominated the electronic industry for many years. However, the continuous dimensional scaling required to improve the integrated circuit's performances and reduce the fabrication costs, gives rise to a series of issues. The most relevant one is the so-called Drain-Induced-Barrier-Lowering(DIBL), which consists in a loss of the gate's control over the channel and results in an increase of the power consumption per chip. To overcome these issues, novel device architectures have been conceived. The most promising one is the Gate-All-Around(GAA) configuration. Moreover, as the gate length reaches the nanometer range, it becomes really challenging to precisely control the dopant atoms distribution and so to construct abrupt pn junctions. To this aim, the Junctionless Transistor (JNT) is an innovative device which does not rely on junctions and so greatly simplifies the fabrication process. In this work, the fabrication process of a Vertical JNT p type transistor is simulated by means of Synopsys Sentaurus Process, and the results of the electrical simulations performed with Synopsys Sentaurus Device are compared to the experimental data of measurements on devices fabricated at the Laboratory for Analysis and Architecture of Systems affiliated to the French National Centre for Scientific Research(LAAS-CNRS). The TCAD simulations have been tuned to obtain the experimental characteristic curves, by providing also some interesting physical insights on the functioning of the studied device. In the second part of the project, an analytical compact model of JNT, inherited from literature, has been implemented in MATLAB. The MATLAB compact model has been thus fitted and validated against the experimental data, considering three different nanowire diameters. In all the cases, an error lower than 10% Finally, the compact model parameters have been tuned based on the Sentaurus results in order to fit the simulated transcharacteristic, thus obtaining a further validation of the compact model. This physical model could be integrated into a SPICE simulator so as to simulate complex digital circuits based on the technology under study and, based on the simulation results, optimize again the device parameters, thus speeding up the production.

Acknowledgements

Finalmente sono giunto al termine di questo lungo percorso, che è stato complicato, ma anche molto appagante e stimolante. Vorrei quindi ringraziare tutte le persone che mi sono state vicine e mi hanno supportato(e sopportato). Al primo posto metterei i miei genitori, che mi hanno sempre lodato e incoraggiato dandomi la forza di andare avanti con tenacia, come anche nonna Anna, nonno Vincenzo, nonna Ninetta, zia Marianna e zio Simone. Poi vorrei ringraziare tutti gli amici che mi sono vicini da una vita: Deni, Edo, Silvi e soprattutto Cri che ha avuto tanta pazienza in questi anni. Un grazie anche a tutti gli amici del Sabato Sera, che ho conosciuto da poco, ma che hanno avuto un impatto importantissimo. Infine, ultimi ma non ultimi, un grazie particolare al professor Gianluca Piccinini, per avermi dato l'opportunità di approfondire questo argomento particolarmente interessante e a Fabrizio Mo, per la sua gentilezza, disponibilità e i suoi consigli preziosi.

Contents

List of Tables	8
List of Figures	9
I First Part	13
1 Introduction	15
1.1 Scaling issues	15
1.2 Junctionless fet	17
1.3 Thesis Objectives	18
1.4 Thesis structure	18
2 Device under study	21
2.1 Introduction	21
2.2 Fabrication procedure	22
3 Methodology	25
3.1 DTCO loop	25
3.2 TCAD softwares overview	26
3.3 FEM method overview	27
4 Physical models	31
4.1 Density gradient model	31
4.2 Interface traps	33
4.3 Mobility models	36
4.4 Velocity saturation	42
4.5 Shockley-Read-Hall recombination	43
4.6 Incomplete ionization	43
4.7 Band-To-Band-Tunneling	44
5 Process simulations	47

6	Electrical simulations	53
6.1	Subthreshold slope fitting	53
6.2	Threshold voltage fitting	55
6.3	On current fitting	56
II	Second Part	65
7	Compact modelling	67
7.1	Introduction	67
7.2	Model derivation	68
8	Compact model validation	75
8.1	Subthreshold slope investigation	75
8.2	Fitting of the experimental data	77
9	Matching the compact model with the Sentaurus results	85
9.1	Mobility and Doping extraction	85
9.2	Fitting of the Sentaurus results	88
10	Conclusions and Future perspectives	93
11	Appendix	95
11.1	Sentaurus scripts	95
11.1.1	SProcess	95
11.1.2	SDevice	96
	MATLAB scripts	99

List of Tables

4.1	IAL mobility model parameters for phonon scattering in Si	37
4.2	Masetti model parameters	39
4.3	IAL mobility model parameters for surface roughness scattering	41
4.4	Canali model parameters	42
6.1	Acceptor type device parameters	53
6.2	Simulation results for different acceptor type interface traps densities . . .	54
6.3	Simulation results for $q\Phi = 4.4$ eV	56
6.4	Parameters for the device with donor type interface traps	57
6.5	Simulation results for donor type interface traps	57
6.6	Parameters for the device with donor type interface traps,after gate $q\phi$ tuning	58
6.7	Simulation results for donor type interface traps,after gate $q\phi$ tuning . . .	58
6.8	Parameters for the device with donor type interface traps,after PtSi $q\phi$ tuning	59
6.9	Simulation results for donor type interface traps,after PtSi $q\phi$ tuning . . .	59
6.10	Final device parameters	60
6.11	Simulation results of the final device	60
9.1	Parameters of the simulation to be fitted	86

List of Figures

4.1	.Comparison between classical and quantum carriers distribution adapted from Guerrieri [2022]	32
4.2	Scattering rates for confined and bulk phonons	38
4.3	Mobility for confined and bulk phonons	38
4.4	Mean free path of the holes for a correlation length of the surface roughness (L_r) equal to 0.54 nm	40
4.5	Mean free path of the electrons for a correlation length of the surface roughness (L_r) equal to 0.54 nm	40
5.1	Main process steps	49
5.3	.Boron active concentrations along the nanowire height direction	51
6.1	.Transcharacteristics for acceptor type interface traps	54
6.2	.Electrostatic potential at equilibrium for different traps concentrations	55
6.3	.Transcharacteristic for $q\Phi = 4.4$ eV	56
6.4	.Transcharacteristic for donor type interface traps	57
6.5	.Transcharacteristic for donor type interface traps,after gate $q\phi$ tuning	58
6.6	.Transcharacteristic for donor type interface traps,after PtSi $q\phi$ tuning	59
6.7	.Final transcharacteristic	60
6.8	.Absolute error between Sentaurus and experimental results	61
6.9	.Relative error between Sentaurus and experimental results	61
6.10	.Band diagram along the nanowire vertical direction	63
6.11	.Electric field along the nanowire vertical direction	63
6.12	.BTBT map along the nanowire vertical direction	64
7.1	.Schematic diagram for the JNT	68
8.1	.Transcharacteristic for D=16 nm	75
8.2	.Transcharacteristic for D=27 nm	76
8.3	.Transcharacteristic for D=34 nm	76
8.4	.Transcharacteristic for D=16 nm with optimized fitting parameters	78
8.5	.Transcharacteristic for D=27 nm with optimized fitting parameters	78
8.6	.Transcharacteristic for D=34 nm with optimized fitting parameters	79
8.7	.Absolute error in between the compact model and the experimental results for D=16 nm	80
8.8	.Relative error in between the compact model and the experimental results for D=16 nm	80

8.9	.Absolute error in between the compact model and the experimental results for D=27 nm	81
8.10	.Relative error in between the compact model and the experimental results for D=27 nm	81
8.11	.Absolute error in between the compact model and the experimental results for D=34 nm	82
8.12	.Relative error in between the compact model and the experimental results for D=34 nm	82
9.1	Mobility and doping distributions along the vertical direction	86
9.2	.Doping concentration along the vertical direction	87
9.3	.Mobility along the vertical direction	87
9.4	.Matching of the Sentaurus results with the compact model, with BTBT included in the compact model	88
9.5	.Matching of the Sentaurus results with the compact model, without BTBT included in the compact model	89
9.6	.Absolute error between the Sentaurus results and the compact model . . .	90
9.7	.Relative error between the Sentaurus results and the compact model . . .	90

*If you cannot understand my
argument, and declare
it's Greek to me
you are quoting Shakespeare.*

[B. LEVIN, Quoting Shakespeare]

Part I

First Part

Chapter 1

Introduction

1.1 Scaling issues

Nowadays MOSFET are exploited everywhere and are essential for a lot of applications such as portable electronics and telecommunications [Rizvi and Jaiswal \[2016\]](#). The progress achieved over the last twenty years in the electronic industry has been possible due to the continuous dimensional scaling. This because by reducing the dimensions it's possible to ameliorate the device's performances, given that complex integrated circuits require high clock frequencies, that can be reached by decreasing the switching time, which is "the time needed by a transistor in order to make the gate of an identical transistor switching from the ground to the supply voltage" [Rizvi and Jaiswal \[2016\]](#).

$$\tau = \frac{Q}{I} = \frac{CV}{I} \quad (1.1)$$

Where C is the gate capacitance, V is the supply voltage and I is the transistor on state current. Therefore the best way to reduce the switching time τ is to reduce the gate length so as to reduce the gate capacitance. The continuous dimensional scaling is also related to the fabrication costs, given that by reducing the transistor's dimensions it's possible to integrate more chips per wafer [Rizvi and Jaiswal \[2016\]](#). This has lead to a huge boost of transistor's density, which was described by Moore in 1965 in the famous Moore's law, which states that "the number of devices on a chip doubles every 18 or 24 months or so as" [Rizvi and Jaiswal \[2016\]](#). However, when scaling a device, there is the need to establish a sort of rule that has to be followed in order to avoid an abrupt increase of the electric field which may lead to some unwanted effects, such as oxide breakdown, drain currents uncontrolled rising due to impact ionization and electromigration, which consists in the metal wires destroying due to the atom's displacement caused by high energies electrons. To avoid all these drawbacks, a sort of "recipe" for the device scaling has been conceived. It is known as Dennard's scaling or constant-field scaling rule and it imposes three transformations so as to keep the electric field constant from one technological node to the other [Dennard et al. \[1974\]](#). Firstly, the supply voltage is reduced by a scaling factor k (i.e. $V'_{ds} = \frac{V_{ds}}{k}$). Second, the doping is increased by the same scaling factor $N'_A = kN_A$. Finally, the gate oxide thickness is scaled, again using the same factor:

$t'_{ox} = \frac{t_{ox}}{k}$. This scaling strategy has worked fine for many years but, with the further proceeding of the scaling down, it is starting to fail since the reduction of t_{ox} and the doping increase imply a threshold voltage's reduction, which can not fall below a certain limit (≈ 0.4 V) otherwise the off current (also known as leakage current) rises too much causing power dissipation problems. As consequence, in order to allow for a large enough operating window, the supply voltage reduction has slowed down, causing an increase of the electric field. Moreover as the channel length reaches the nanometers range, a series of issues which undergo the name of short channel effects arise. They can be summarized as follow:

- **drain induced barrier lowering:** as the source-substrate and the drain-substrate depletion depth extensions reach the same order of magnitude of the gate length, the amount of depletion charge under the gate control diminishes [Chopra and Subramaniam \[2015\]](#). This results in a lowering of the barrier in between source and drain. As a consequence the threshold voltage is reduced; moreover the barrier's height and thus the threshold voltage become affected by the drain voltage [Rizvi and Jaiswal \[2016\]](#). So the barrier lowers with the drain voltage increase and this will cause an increase of the off state current of the device that on its own will cause a rising of the power dissipation.
- **gate oxide tunneling:** according to the constant field scaling rule, with the channel length reduction it's also necessary to reduce the gate oxide thickness. This will cause quantum mechanical tunneling that will increase the gate induced leakage current.
- **random doping fluctuations:** by going down with dimensions becomes increasingly challenging to precisely control the dopants atoms positions, thus the effect of randomness of the dopant distribution becomes more and more pronounced.
- **mobility degradation:** the increase of doping concentration prescribed by the Dennard's scaling rule leads to a rising of the impurity scattering rate, which degrades the device's mobility.
- **hot carriers effects:** in scaled transistors, since the channel length is very short and the supply voltage can not be scaled down under a certain limit, a strong electric field arises from source to drain which accelerates carriers to very high velocities. Given that these carriers possess very high kinetic energy, they impact against the gate oxide layer, giving rise to oxide trapped charges which lead to parasitic gate currents and mobility degradation.

Therefore the integrated circuits technology is slowing down due to the increasing power dissipation, process variabilities and fabrication costs, thus novel devices able to guarantee high performances by dissipating a low amount of power are required to further proceed with the scaling down [Chopra and Subramaniam \[2015\]](#). Up to the 22 nm node some change in the CMOS technology has been performed, such as replacing SiO_2 with HfO_2 in the gate dielectric in order to increase the gate oxide thickness without compromising the gate capacitance, or creating source and drain extensions to counteract short channel effects. However, from the 22 nm node these non ideality effects become more and more

pronounced thus new devices architectures such as Finfets or Gate All Around FET (GAA FET) should be considered in order to have a better electrostatic control over the channel and to further proceed with the technological scaling.

1.2 Junctionless fet

Nowadays all the transistors exploited in the commercial electronic industries are junction based devices, which exploit junctions in order to impede or allow the current flowing. Nevertheless, a transistor, to be defined as such, must not be necessarily based on junctions [Colinge et al. \[2010\]](#). By definition, "a transistor is just a device which regulates the current flow" [Rongon \[2022\]](#). Infact, as explained in [Colinge et al. \[2010\]](#), the transistor idea was conceived for the first time in 1925, by the Austrian-Hungarian physicist Julius Edgar Lilienfeld who promoted a device which consisted in a thin uniformly doped semiconductor film whose conductivity was modulated by a proper control of the voltage applied to a metal electrode deposited on it, with an insulating layer in between. However, the semiconductor technology at the time was still at the beginning, as a consequence the device's operation showed several issues. With the modern technologies the idea of a junctionless transistor was taken again in consideration and in 2010 Jean-Pierre-Colinge presented in [Colinge et al. \[2010\]](#) a device consisting of a uniformly doped Silicon nanowire, lying on a Silicon-On-Insulator(SOI) substrate, with a gate wrapping the channel from three sides. Then, the technology has been further refined up to arrive to a nanowire completely encircled by the gate, thus increasing the electrostatic control over the channel. Apart from the advantages in terms of reduced short channel effects, near ideal Subthreshold Slope(SS) and improved I_{on}/I_{off} ratio, this device offers a great simplification of the fabrication process, since does not rely on junctions and so does not require ultrafast annealing techniques in order to form abrupt doping profiles. This also allows to improve the electrical properties, since as soon as the channel length reaches the order of nanometers, becomes very difficult to create high quality pn junctions [S.Munjal et al. \[2021\]](#). The working principle of the device [S.Munjal et al. \[2021\]](#) relies on the modulation of the gate voltage, which induces an electric field perpendicular to the nanowire height. If V_{gs} is small enough, the complete depletion of the silicon nanowire is achieved and the device is in the off condition. This is possible if the nanowire diameter is thin enough, otherwise is not possible to totally deplete the channel and the device can not be turned off. As the gate voltage reaches the threshold value, a small portion of neutral region appears at the center of the channel and the current starts to flow. When the gate voltage is further increased, the portion of the neutral region increases more and more and when the applied voltage is equal to the flat band one the depletion region totally disappears and the entire channel is neutral, so an high amount of current will flow. If the gate voltage increases again, then the device enters in the accumulation mode and the current slightly rises up, but the junctionless fet is often designed to operate up to the flat band condition since in the accumulation region the majority carriers accumulate at the interface between Si and SiO_2 where there are interface traps which reduce the mobility, as it happens for inversion mode transistors. Moreover, since the nanowire must be thin enough to allow for the complete depletion in the off condition, the device must be highly

doped in order to allow for a sufficient amount of current flowing in the on condition [Colinge et al. \[2010\]](#). This means that impurity scattering dominates over phonon scattering and thus the mobility and the current are less temperature dependent with respect to a standard inversion mode device [Colinge et al. \[2010\]](#).

1.3 Thesis Objectives

The main objectives of this thesis project are basically three. Firstly, simulating the fabrication process a novel device which is currently under study at the Laboratory for Analysis and Architecture of Systems affiliated to the French National Centre for Scientific Research(LAAS-CNRS) and obtain a good matching of the electrical characteristics with the available experimental results. Second, implementing in MATLAB an analytical compact model presented in literature which describes the physics of the device, validating the same against the experimental results. Finally, after extracting some microscopic quantities from the electrical simulations, modifying the compact model in order to obtain a good correspondence with the simulation results.

1.4 Thesis structure

The structure of the project can be summarized as follows:

- in the **first chapter** the scaling issues which arise in the modern devices are described and the operational principle of the Junctionless FET is introduced, focusing on the benefits of this novel type of device with respect to the standard CMOS technologies.
- in the **second chapter** the fabrication procedure of the device which is going to be simulated is described in detail.
- in the **third chapter** the methodology currently adopted for the device optimization by the industries is presented, followed by a description of the simulation tools exploited in this project and by an overview of the Finite-Element-Method(FEM), which is used by the physics based simulator to solve partial differential equations.
- in the **fourth chapter** the physical models taken into account in the electrical simulations of the device are described.
- in the **fifth chapter** the process simulation is illustrated, highlighting the differences with respect to the real process described in chapter 2.
- in the **sixth chapter** the results of the electrical simulations are presented and validated against the experimental results, reporting an analysis of the relative and absolute error.
- in the **seventh chapter** the analytical compact model presented in literature is derived.

- in the **eight chapter** the analytical compact model presented in the previous chapter is validated against the experimental results, considering three different geometries. The absolute and relative errors are reported for each case.
- in the **ninth chapter** the analytical compact model parameters are optimized so as to fit the results obtained from the electrical simulations.
- in the **tenth chapter** conclusions and future perspectives are reported.

Chapter 2

Device under study

2.1 Introduction

As explained in the previous chapter, the modern technologies are increasingly suffering from problems related to the scaling. The most relevant one is the subthreshold leakage current, which causes an increase of the power consumption. To overcome this issue, novel CMOS architectures based on multi-gate devices have been developed, with the aim of increasing the electrostatic control over the channel. The design which allows to maximize the electrostatic control over the channel is represented by the GAA architectures. However, the amount of current flowing through a singular device is small due to the narrow nanowire's diameter, so these transistors have to be implemented on nanowires arrays so as to merge the excellent electrostatic control with high on current capability [Larrieu and Han \[2013\]](#), [Larrieu et al. \[2017\]](#). There are two methods used to produce nanowires arrays [Han et al. \[2010\]](#), [Larrieu and Han \[2013\]](#), [Guerfi and Larrieu \[2016\]](#). The first one is the so called bottom up approach, which is a chemical deposition technique which allows to sintetize nanowires on a substrate by means of a catalyst. The other one is the top down approach, consisting in the selective etching of a planar substrate. One method could be preferred to the other depending on the application: the bottom up one allows to grow nanowires using virtually any material but suffers from metallic contamination issues due to the the metallic catalyst, while the top down one is highly CMOS compatible and allows for a good control over nanowire's position, diameter and pitch. Moreover with the top down approach it's possible to construct nanowires arrays with an higher density with respect to those obtained by means of the bottom up approach. The nanowires based FET can be fabricated both horizontally and vertically [Larrieu and Han \[2013\]](#), [Guerfi and Larrieu \[2016\]](#). From the design point of view, vertical integration can allow for a better integration density with respect to the horizontal one. Moreover, the gate length in the vertical configuration is not defined by high resolution lithographic techniques but just by the thickness of the deposited gate material [Larrieu and Han \[2013\]](#), [Guerfi and Larrieu \[2016\]](#), [Larrieu et al. \[2017\]](#). Despite of these advantages, the vertical integration of nanowires transistors is not as mature as the horizontal one from a technological point of view [Guerfi and Larrieu \[2016\]](#), mainly because of troubles with contacts creation at

the bottom of the wires and perfect control of the thickness and smoothness of the spacer layers [Larrieu and Han \[2013\]](#). Thus the vertical integration architecture is not exploited at commercial level yet.

2.2 Fabrication procedure

The device under study is a vertical gate all around p type junctionless transistor fabricated by the Laboratory for Analysis and Architecture of Systems affiliated to the French National Centre for Scientific Research(LAAS-CNRS). The process can be divided in the following steps:

- **vertical nanowire creation:** the starting point is a 4-in. Si(100) wafer, with a Boron concentration equal to $3.5 \times 10^{19} \text{ atm cm}^{-3}$ [Guerfi and Larrieu \[2016\]](#), [Kumar et al. \[2024\]](#). The vertical silicon nanowires are realized through a top-down approach, by exploiting plasma etching to transfer an hard mask pattern onto the silicon substrate [Guerfi and Larrieu \[2016\]](#). The hard mask is realized by electron beam lithography through the patterning of an high resolution negative tone resist: Hydrogen SilsesQuioxane (HSQ) [Guerfi and Larrieu \[2016\]](#). Being an inorganic resist, it is highly resistant to plasma etching and exhibits high mechanical strength [Guerfi et al. \[2013\]](#). The HSQ resist is identified with the general formula of $(\text{HSiO}_{3/2})_n$ and upon e-beam exposure, there is a scission of the Si-H bonds which rearrange into Si-O-Si bonds(siloxane bonds), changing the cage like structure into a network one [Guerfi et al. \[2013\]](#). Firstly, the HSQ solution is spin-coated on the Si wafer at different angular speeds so as to obtain a resist thickness ranging from 70 nm to 330 nm [Han et al. \[2010\]](#). Then the sample it's baked at 80 °C for 60 s to let the solvent evaporating [Han et al. \[2010\]](#). For the exposure step, it is necessary to find a proper design strategy in order to obtain circular resist nanopillars with uniform size and anisotropy [Guerfi et al. \[2013\]](#). One possibility is using a design pattern based on concentric circles separated by a distance corresponding to the HSQ resolution. Unfortunately, this strategy leads to squared shaped nanostructures with bowed sidewalls and stitching defects. The proper design strategy is the so called star like design, consisting of lines starting and finishing at the center of the pattern. After the e-beam exposure, the resist is developed by manual immersion in 25% Tetramethylammonium Hydroxide(TMAH) at 20 °C for 60 s, dipped in deionized water and blown dry with nitrogen [Han et al. \[2010\]](#). Then the HSQ nanopillars are transfered into the substrate by means of Reactive Ion Etching(RIE). The process parameters of this step need to be properly tailored so as to obtain anisotropy and avoid micro-trenching and under-etching effects [Han et al. \[2010\]](#). After several attempts, it was discovered that the best condition is a Capacitive Coupling Plasma (CCP) chamber feeded with Chlorine(Cl_2), biased at 80 W at a 2 mTorr pressure. The Chlorine chemistry allows to obtain sidewalls with 94% of anisotropy, whereas a low pressure chamber and an high radio-frequency power source are necessary to mitigate micro-trenching and under-etching effects. The reason behind this is that these process defects are mainly caused by specular reflections of the etching species and charging of the mask layer. At low pressures, the mean free path of the ions is

long and the possibility of collisions between them is reduced, thus decreasing the specular reflections. For what concern the source, high power provides high kinetic energy to the bombarding ions which force them in a more vertical profile thus reducing the specular reflections, preventing micro-trenching. Moreover the etching time is fixed at 2 min, since over this short amount of time the charge masking is negligible. The residual resist is then removed by immersion in a diluted Fluorhydric Acid (HF) solution.

- **gate oxide creation:** then there is a dry oxidation step at 850 °C for 10 min, which has the purpose of reducing the nanowire's diameter and neutralize the defects present at the Si/SiO₂ interface. After the stripping of this sacrificial oxide layer, the gate oxide layer is realized through a wet oxidation at 725 °C for 30 min. Before the implementation of the source and drain contacts, it is necessary to etch the oxide at the top and bottom of the nanowires. This is performed by CCP using fluorine chemistry [Guerfi and Larrieu \[2016\]](#).
- **PtSi contacts creation:** then follows an anisotropic deposition of a 10 nm Platinum (Pt) layer which is annealed by a Rapid Thermal Annealing (RTA) at 500 °C for 3 min in order to form Platinum-Silicide(PtSi) [Guerfi and Larrieu \[2016\]](#). The Pt contaminations on the nanowires sidewalls are removed by a selective wet etching in aqua regia solution. Aqua regia slightly oxidizes on the outer surface of the nanowires, but this is beneficial since contributes to passivate the trap states [Han et al. \[2012\]](#).
- **source-gate spacer creation:** the creation of the source-gate isolation spacer is fulfilled by spin-coating HSQ [Larrieu and Han \[2013\]](#), [Larrieu et al. \[2017\]](#), which is exploited thanks to its excellent filling properties, low viscosity and its low dielectric constant ($k=2.7$) which makes it compatible with CMOS processes [Guerfi and Larrieu \[2016\]](#). The HSQ dielectric matrix is then etched to the proper thickness in a diluted HF solution. The HSQ etching step needs to be properly optimized so as to obtain a flat spacer surface and the desired dielectric properties [Guerfi et al. \[2015\]](#). Infact, the low HSQ dielectric constant, necessary to minimize the parasitic capacitances, is achievable upon transformation of the cage like HSQ structure (SiO_xH_y) into the network like one (SiO_x). To this aim, an annealing step is required so as to stabilize the SiO_x phase. Unfortunately, even if the annealing temperature is high, not all the SiO_xH_y phase can be transformed into the SiO_x one. The coexistence of two phases results in a inhomogeneity of the etching rate, which leads to surface holes and lack of surface smoothness. To avoid this issue, the annealing step is performed after the HSQ layer etching. However, upon the reaction between the SiO_xH_y phase and the HF present in the etchant solution, hydrogen gas can be released leading to bubble encroachments, which can increase the surface roughness of the spacer. To avoid this drawback, the HF solution is enriched by a cationic surfactant (benzalkonium chloride) , whose purpose is to remove the bubbles appearing on the surface during etching .
- **gate definition:** the metallic gate is formed by anisotropic deposition of a 18 nm Chromium(Cr) layer [Kumar et al. \[2024\]](#). As mentioned in the introduction, it is

worth to remark that the gate length is just defined by the thickness of the deposited layer and not by the lithography resolution [Larrieu and Han \[2013\]](#), [Guerfi and Larrieu \[2016\]](#), [Larrieu et al. \[2017\]](#), which is a great advantage for the scaling.

- **gate-drain spacer creation:** the procedure for the creation of the gate-drain spacer is exactly equal to the one for the source-gate spacer, the only difference is the etching rate of the HSQ layer, which is tailored so as to cover the structure up to the drain terminations.
- **contacts creation:** lastly, two via-holes are created by etching the HSQ layer up to the source PtSi termination and the gate layer. Then the contact pads are created by depositing and etching a 400 nm Aluminum(Al) layer [Kumar et al. \[2024\]](#). Finally, there is a gas annealing process in a N_2/H_2 atmosphere whose aim is to passivate the defects present at both the Si/ SiO_2 interface and at the Pt/PtSi contacts interface [Han et al. \[2012\]](#), [Guerfi and Larrieu \[2016\]](#).

Chapter 3

Methodology

3.1 DTCO loop

In the past devices optimization and system level studies were conducted independently one with respect to the other, but with the further evolution of the scaling, a strong interaction among process engineers and system designers has become mandatory in order to reduce the costs and speed up the production [Asenov et al. \[2015\]](#), [Ma et al. \[2024\]](#). This is related to the fact that the novel technological nodes require expensive fabrication techniques(e.g. EUV lithography) and often innovative materials that are still under study, so is not feasible to produce a device without knowing its reliability at circuit level. This cooperation among different groups of experts of the semiconductor industry is known as Design-Technology Co-Optimization(DTCO) and its aim is to optimize a device and its fabrication process in order to fulfil specific requirements at system level in terms of power consumption, performances and area. It can be summarized in three steps [O'Connor et al. \[2024\]](#):

- **TCAD simulation at device level:** given that with the current technological nodes dimensions the devices variabilities(such as metal gate's granularity, oxide traps and random doping fluctuations) play an important role, a preliminary optimization of the process at device level is needed and it is obtained by combining experimental data with TCAD simulations. By studying the simulations results, it is possible to figure out which are the variability sources that most affect the device performances and consequently optimize the fabrication process. Moreover, even if will not be part of this work, within this first step one can extract some device's parameters(e.g. capacitances, resistances) that, combined with the compact model extracted in the second step, allow to simulate cells based on the technology under study. This procedure undergoes the name of Parasitic Network Extraction (PEX).
- **cells simulations:** after optimizing the process at device level, more complicated circuits based on that device(i.e. cells) must be characterized. In principle, it could be possible to perform this task by means of TCAD softwares, but it would be too much computationally intensive. So a compact model suited to be integrated

in SPICE simulators must be formulated so as to conduct fast studies of the cells performances and, based on these results, optimize again the circuit at device level.

- in the last DTCO step, the cells are put together to construct more **complex circuits**(e.g.multipliers,adders) and conduct timing and power analysis.

3.2 TCAD softwares overview

As mentioned in the previous section, a trial-error approach to industrial electronics is no more feasible due to the increasing process costs and complexity and necessity to reduce the products time-to market. As a consequence, industries need to rely on reliable TCAD softwares to be exploited in the DTCO loop in order to test a device before its production. In this project, the following commercial tools by Synopsys will be exploited:

- **Sentaurus process:** it is a TCAD software used to perform simulations of 2D or 3D semiconductor devices exploited in the field of electronics and photonics [Synopsys, Inc. \[2017b\]](#). It is able to emulate the basic process steps(i.e. lithography, etching, deposition, oxidation, ion implantation, etc.) but it can not deal with more complex processes such as RIE and with rounded geometrical structures(i.e.spheres, cylinders). To this aim, more advanced tools such as Sentaurus Topography or Sentaurus Structure Editor are needed. It takes as input the so called **cmd** file which contains instructions related to the process to be simulated and the mesh of the structure, which is important to properly define so as to reduce the computational time of the simulation. It gives as an output the **tdr** file containing the structure of the device resulting from the simulation, which can be visualized with the Sentaurus Visual interface.
- **Sentaurus Structure Editor:** it is an editor which allows to modify or create 2D or 3D semiconductor devices by means of geometrical transformations [Synopsys, Inc. \[2017a\]](#). In this work will be exploited to create the cylindrical nanowire.
- **Sentaurus device:** it is a physics based simulator which takes as an input the structure and the mesh generated by the Sentaurus Process tool and solves partial differential equations with the aim of extracting some microscopic quantities and the current/voltage characteristics [Vallone \[2020\]](#), [Guerrieri and Tibaldi \[2022\]](#). As a default, it solves the drift-diffusion problem, namely the Poisson's equation coupled to the continuity equations for electrons and holes:

$$\nabla \cdot (\epsilon \nabla \phi) = -q(p - n + N_D - N_A) \quad (3.1)$$

$$\nabla \cdot \vec{j}_n = q(R_n - G_n) + q \frac{\partial n}{\partial t} \quad (3.2)$$

$$-\nabla \cdot \vec{j}_p = q(R_p - G_p) + q \frac{\partial p}{\partial t} \quad (3.3)$$

where ϵ is the material's dielectric constant, ϕ is the electrostatic potential, n and p are the electrons and holes concentrations per unit of volume, N_D and N_A are the

donors and acceptors concentrations per unit of volume, \vec{j}_n and \vec{j}_p are the electrons and holes current densities, R_n and R_p are the electrons and holes recombination rates (i.e. the variation of electrons and holes per unit of time owing to recombination mechanisms with the valence and the conduction band respectively), G_n and G_p are the generation rates (i.e. the amount of electrons and holes generated per unit of time). These equations work fine for classical devices. However, as will be shown later, as the device enters in the nm regime there is some additional effect that has to be included so as to get an accurate description of the device's electrical behaviour. The Poisson's equation coupled to the electrons and holes continuity equations forms a system of partial differential equations that can not be directly handled by the software. To this aim, the equations are discretized on the spacial domain so as to convert the partial differential equations set in a system of algebraic equations that can be easily managed by the simulator. This procedure undergoes the name of Finite-Element-Method (FEM) and will be addressed in the next section. Similarly, the voltage domain is discretized by associating to it a variable t which is ramped from 0 to 1 [Synopsys, Inc. \[2015\]](#). For each time step, the corresponding voltage is computed as:

$$V(t) = V_0 + t(V_1 - V_0) \quad (3.4)$$

where V_0 and V_1 are the upper and lower limits of the voltage interval respectively. The variable t is ramped from 0 to 1 and for each time step the corresponding voltage is computed according to (3.4), solving the drift-diffusion model so as to extract the current/voltage characteristics that are saved in a **plt** file, visualized by the Inspect tool.

3.3 FEM method overview

As previously said, a computer can not cope with differential equations, so there is the need to convert them into a system of algebraic equations that can be easily addressed by the softwares. To this aim, the most used technique is the so-called Finite-Element-Method (FEM). The basics of this technique are now explained, taking as a reference [Tibaldi et al. \[2022\]](#). As a starting point, it is useful to consider the Poisson's equation at equilibrium, since its solution is used as an initial guess to solve the drift-diffusion problem under applied bias conditions. Moreover, for the sake of simplicity, the one dimensional case is considered:

$$-\frac{d}{dz} \left[\epsilon(z) \frac{d\phi}{dz} \right] = \rho(z) \quad (3.5)$$

where $\rho(z)$ is the semiconductor charge density. This equation exhibits two problems:

- it is differential
- it is non linear, due to the relation between charge and potential.

The first problem is overcome by performing a discretization of the domain by choosing a mesh and writing the unknown of the problem (i.e. $\phi(z)$) as a linear combination of basis functions associated to each mesh node:

$$\phi(z) = \sum_{j=1}^{nn} c_j N_j(z) \quad (3.6)$$

where nn is the number of nodes of the discretization, c_j are coefficients and $N_j(z)$ are the basis functions that have to be properly chosen. To this purpose, one common choice are the so-called Lagrange's polynomials, which are piece-wise functions and are basically triangles whose supports are limited to the mesh elements adiacents to the corresponding node at which the function is associated. Thus the problem is reduced to the determination of the unknown coefficients c_j which, thanks to the fact that the Lagrange's polynomials are interpolating functions (i.e. $N_j(z_j) = 1$), coincide with the potential value associated to the j -th mesh node. Similarly the charge density $\rho(z)$ is written as:

$$\rho(z) = \sum_{j=1}^{nn} \rho_j N_j(z) \quad (3.7)$$

By substituting (3.6) and (3.7) back into (3.5), after some calculation, a matrix problem is obtained:

$$[E]\{\phi\} = [M]\{\rho\} \quad (3.8)$$

where $[E]$ and $[M]$ are known matrices and $\{\phi\}$ and $\{\rho\}$ are vectors containing the potential and the charge values associated to each mesh node. The problem has been simplified with respect to the initial one, since the differential equation has been converted into a set of algebraic equations. However, due to the relation between charge and potential, the problem is not linear, so can not be directly handled by the software. To overcome this issue, the generalized Newton's method is exploited. It basically consists in approximating the root of a non-linear function $f(x)$ with the root of its First order Taylor's expansion around a certain guess x_0 :

$$x_1 = x_0 - \frac{f(x_0)}{f'(x_0)} \quad (3.9)$$

Then x_1 is used as a guess for the next iteration and so on. To generalize, the solution at the $(k+1)$ -th iteration reads as:

$$x_{k+1} = x_k + \Delta x_{k+1} \quad (3.10)$$

where $\Delta x_{k+1} = -\frac{f(x_k)}{f'(x_k)}$ is the difference between the result of the $(k+1)$ -th iteration and the k -th one. The procedure is repeated until Δx_{k+1} is smaller than a certain threshold. When dealing with a matrix problem, the method is applied for each equation composing the system so as to obtain a linearized system of algebraic equations. For the Poisson's

case, the final result of this linearization procedure is given by the following matrix equation:

$$\begin{bmatrix}
 1 & & & & & \\
 \frac{\partial r_2}{\partial \phi_1} & \frac{\partial r_2}{\partial \phi_2} & \frac{\partial r_2}{\partial \phi_3} & & & \\
 & \frac{\partial r_3}{\partial \phi_2} & \frac{\partial r_3}{\partial \phi_3} & \frac{\partial r_3}{\partial \phi_4} & & \\
 & & \ddots & \ddots & \ddots & \\
 & & & \ddots & \ddots & \ddots \\
 & & & & \ddots & \ddots \\
 & & & & & 1
 \end{bmatrix}
 \begin{bmatrix}
 \Delta\phi_1 \\
 \Delta\phi_2 \\
 \Delta\phi_3 \\
 \vdots \\
 \Delta\phi_{nn-2} \\
 \Delta\phi_{nn-1} \\
 \Delta\phi_{nn}
 \end{bmatrix}
 =
 \begin{bmatrix}
 0 \\
 r_2 \\
 r_3 \\
 \vdots \\
 r_{nn-2} \\
 r_{nn-1} \\
 r_{nn}
 \end{bmatrix}
 \quad (3.11)$$

which in compact form can be written as:

$$[\mathbf{j}] \{\Delta\phi\} = \{r\} \quad (3.12)$$

where $[\mathbf{j}]$ is the Jacobian matrix, $\{\Delta\phi\}$ is a vector containing the difference between the potential of the current iteration and the previous one, evaluated for each mesh node. $\{r\} = [E]\{\phi\} - [M]\{\rho\}$ is the residual vector, which is different from zero due to the non-self-consistency of the problem. This linearized system is assembled for each iteration of the generalized Newton's loop until a certain convergence criteria is satisfied, which could be requiring that the residual vector $\{r\}$ does not exceed a certain threshold.

Chapter 4

Physical models

4.1 Density gradient model

As a default, Sentaurus Device exploits the drift-diffusion model to perform the electrical simulations [Synopsys, Inc. \[2015\]](#) but, as the device enters in the nanometers regime, the quantum effects start to become relevant and this approach fails, leading to a wrong prediction of the device's performances. This is due to the fact that for small dimensions carriers undergo the so called "quantum smearing effect", which is a sort of redistribution of the carriers along the transverse direction of the device. This effect does not occur in classical devices since, for standard dimensions, carriers are governed by the Boltzmann's statistic which predicts an exponential decay of the carriers concentration moving away from the Si/SiO_2 interface. However, in the quantum limit, the particles must obey to the Heisenberg's principle, so can not be confined at the interface because this would imply a huge energy imparted to them. Thus, in order to minimize their energy, instead of being all in proximity of the semiconductor's oxide interface, they tend to distribute in a more uniform way, with the maximum of the distribution displaced with respect to the interface, as shown in Fig.(4.1). This effect is reflected in a lower on-state current, since carriers flow in a region which is not affected by the maximum possible field. Moreover, at such small dimensions, quantization of the energy levels occurs. These quantized levels are characterized by higher energies with respect to the classical ones, thus becomes increasingly difficult for carriers to possess an energy high enough to populate the levels which participate to the conduction. So in order to have a faithful prediction of the device's performances, quantum effects have to be included in the device simulator [Lyumkis et al. \[2002\]](#). To this aim, the standard choices are the Poisson-Schrödinger loop or the Non-Equilibrium-Green-Functions(NEGF) approach. These models are physically accurate but are very computationally intensive. Moreover, even if they provide an excellent description of quantum mechanics, they still have to be ameliorated under certain aspects [Ancona et al. \[2009\]](#): for example they describe the scattering events by means of a simple relaxation time, they suffer from a poor knowledge of real devices and materials so fail to predict some effects(such as scattering events which occur deep in the band, the degree of strain relaxation or the exact impurity profile). Additionally, they can not describe

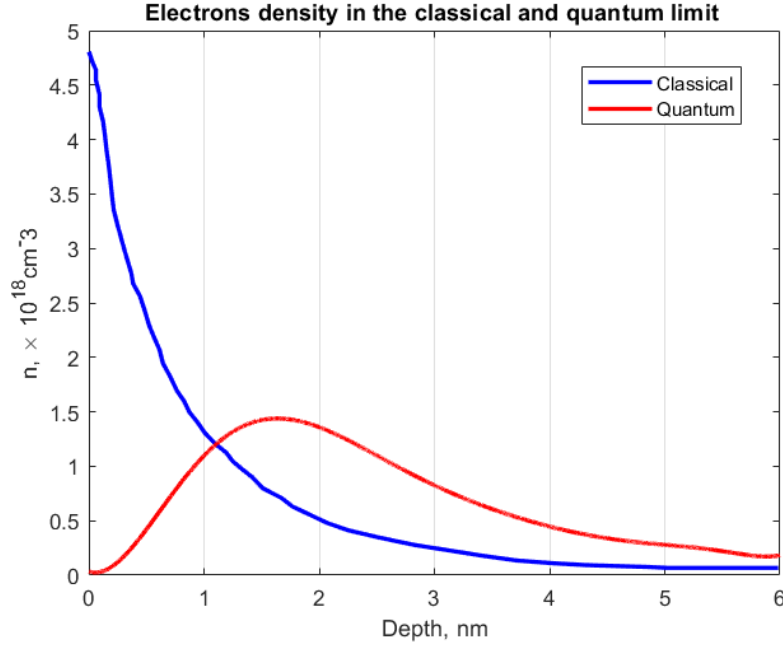


Figure 4.1: .Comparison between classical and quantum carriers distribution adapted from Guerrieri [2022]

devices in which the quantum effects are relevant only in a small portion of the device. To overcome all these drawbacks and find a balance between accuracy and computational cost, an alternative approach to treat the quantum effects has to be found. The most used one in the so called Density Gradient model(DG), which is an extension of the standard drift-diffusion approach to make it suited for quantum devices. It consists in modifying the Poisson's equation by adding an extra term to the carriers densities Han et al. [2013], Synopsys, Inc. [2015]:

$$\Lambda_n = -\frac{\gamma\hbar^2}{12m_n} \left\{ \nabla^2 \ln n + \frac{1}{2} (\nabla \ln n)^2 \right\} = -\frac{\gamma\hbar^2}{6m_n} \frac{\nabla^2 \sqrt{n}}{\sqrt{n}} \quad (4.1)$$

$$\Lambda_p = -\frac{\gamma\hbar^2}{12m_p} \left\{ \nabla^2 \ln p + \frac{1}{2} (\nabla \ln p)^2 \right\} = -\frac{\gamma\hbar^2}{6m_p} \frac{\nabla^2 \sqrt{p}}{\sqrt{p}} \quad (4.2)$$

$$n = N_C F_{\frac{1}{2}} \left(\frac{Ec - E_{F,n} - \Lambda_n}{K_b T} \right) \quad (4.3)$$

$$p = N_V F_{\frac{1}{2}} \left(\frac{E_{F,p} - E_V - \Lambda_p}{K_b T} \right) \quad (4.4)$$

where n and p are the electrons and holes densities respectively, γ is a fitting factor, \hbar is the reduced Plank's constant (1.054×10^{-34} Js), $m_{n,p}$ are the electrons and holes

effective masses, N_c is the effective density of states of the conduction band, N_v is the effective density of states of the valence band, $F_{\frac{1}{2}}$ is the Fermi integral, E_C and E_V are the conduction and valence band edges respectively, E_{fn} and E_{fp} are the electrons and holes quasi Fermi levels. The quantum corrections Λ_n and Λ_p represent an apparent band edge shift which leads to a quantum mechanical modification of the density of states so as to take into account of the quantum smearing effect [Lyumkis et al. \[2002\]](#). Eq.(4.3) and (4.4) are substituted in the Poisson's equation, leading to:

$$\nabla(\epsilon \nabla \phi) = -q \left(N_C F_{\frac{1}{2}} \left(\frac{E_C - E_{fn} - \Lambda_n}{K_b T} \right) - N_V F_{\frac{1}{2}} \left(\frac{E_{fp} - E_V - \Lambda_p}{K_b T} \right) + N_D^+ - N_A^- \right) \quad (4.5)$$

This modified Poisson's equation, solved self-consistently with the electrons and holes continuity equations, gives a result which is pretty much coherent with the one obtained with the Poisson-Schrödinger method, but with a much lower computational cost.

4.2 Interface traps

With the continuous scaling down, the fabrication process variabilities are becoming more and more important and must be included in the SDevice simulator in order to have a correct prediction of the device's electrical characteristics. One of these variability issues is the presence of interface traps at the Si/SiO_2 interface, which can lead to a degradation of the device's performances (i.e. threshold voltage shift, mobility degradation, leakage currents increase and SS increase). There are mainly four types of interface traps:

- **process induced traps:** some process steps, especially oxidation, induce some damage in the device's characteristics. The most relevant problem which arises from the oxidation step is the presence of dangling bonds, which are silicon atoms at the the interface with unpaired electrons. To overcome this issue, a passivation step in a H_2 atmosphere is performed at the end of the process so as to saturate the dangling bonds formed at the interface. However, the $Si - H_2$ bond is very unstable and, as will be shown later, under annealing and irradiation can easily dissociate giving rise to other type of interface defects [Zhang et al. \[2024\]](#).
- **irradiation induced traps:** irradiation is a common source of damage in electronic devices. It derives from different sources (i.e. x-rays, heavy ions, electron beams, neutrons etc.) which are exploited in the lithographic and characterizations steps [Zhang et al. \[2024\]](#). Moreover, as the device leaves the factory, it can be further subjected to the damage coming from other sources such as radioisotopes and cosmic rays [Zhang et al. \[2024\]](#). There are two effects which can take place in a device depending on the radiation dose [Zhang et al. \[2024\]](#): the Enhanced Low Dose Rate Sensitivity (ELDRS) and the Total Ionization Dose Effect (TID). The former is responsible for the creation of the so called E'_γ centers, the latter of the Pb centers and oxygen vacancies. E'_γ and Pb centers are formed in four steps [Song et al. \[2022\]](#): firstly, electrons and holes pairs are generated in the SiO_2 layer due to the ionizing irradiation. Second, holes travel via hopping through the oxygen vacancies ($V_{O\gamma}$) up to arrive in proximity of

the Si/SiO_2 interface, generating E'_γ centers, which are basically positively charged oxygen vacancies:



Third, thanks to its positive charge, the E'_γ center dissociate a nearby H_2 molecule by breaking the H-H bond. The result of this process is an H-passivated oxygen vacancy (V_OH) and the release of a proton(H^+):



Last, the generated proton H^+ de-passivates a surface dangling bond by destroying a Pb-H bond, thus creating a Pb center and releasing a proton (H^+) which reacts with the previous one forming an H_2 molecule.



Another source of interface defects comes from the oxygen vacancies. They are created under the action of high energy irradiated particles(i.e.TID effect), which break the Si-O bond leaving a Si dangling bond(which on its own increases the interface traps density) and an oxygen vacancy. This kind of trap increases the leakage current through the gate, since the oxygen atom acts as a barrier preventing the carriers tunneling but, as the vacancy is created, the barrier diminishes thus facilitating the leakage current mechanism [Zhang et al. \[2024\]](#).

- **stress induced traps:** another source of traps comes from the mechanical stress which arises at the Si/SiO_2 interface, for instance due to the oxidation step. Infact, differently with respect to the concave nanostructures where the oxidation phenomena is limited by the hydrostatic pressure increase which prevents the oxidant diffusivity thus impeding the further supply of oxygen molecules at the interface, in the case of convex nanostructures the factor which limits the oxidation rate is the arising of a radial compressive stress component at the interface, defined as [Krzeminski et al. \[2012\]](#):

$$\sigma_r(r) = \frac{1}{2}\sigma_c \left[\left(\ln \frac{R^2}{b^2} \right)^2 - \left(\ln \frac{R^2}{r^2} \right)^2 \right] \quad (4.9)$$

where σ_c is the critical stress threshold at which the plasticity flow appears($\approx 1\text{GPa}$), R is a reduced parameter, $b = a + t_{ox}$ where a is the nanostructure radius and t_{ox} is the grown oxide thickness, r is the radius of curvature of the nanowire. This radial stress component alters the bonds angles and lengths at the Si surface thus contributing to increase the interface's traps density [Zhang et al. \[2024\]](#).

- **hot carriers induced traps:** as mentioned in chapter 1, with the continuous downsizing, the electric field inside the device is becoming more and more strong. As a consequence carriers can gain enough kinetic energy to overcome the gate oxide potential barrier, giving rise to oxide trapped charges or interface charges, which are formed when an high energy carrier breaks a Si-H bond, leaving the surface with a dangling bond which acts as a surface trap [Chen \[2014\]](#).

The interface traps can behave as donor or acceptor states basing on their energy position inside the energy gap [Rassekh et al. \[2019\]](#). If the trap level is below the mid-gap position, it acts as a donor state which can be empty or not depending on whether its level is below or above the Fermi level. Oppositely, the acceptor states are in the upper part of the energy gap and host an electron if are below the Fermi level. Donor(acceptor) states carry a positive(negative) charge when are empty(occupied) and are neutral if occupied(empty). Moreover, the acceptor and donor states have a different impact on the device's performances depending on the doping type [Han et al. \[2012\]](#). For n-type nanowires devices, the acceptor states present at the interface decrease the majority carriers concentration in the conduction band thus causing a radial depletion of the wire. The same effect is obtained for a p-type device in presence of donor states which increase the electrons concentration in the valence band, thus reducing the holes population. Due to this this traps induced depletion effect, the electronic radius r_{elec} will be smaller than the physical radius r_{phys} [Han et al. \[2012\]](#):

$$r_{elec} = r_{phys} \sqrt{1 - \frac{2N_D}{r_{phys}N_A}} \quad (4.10)$$

thus the cross section available for the carriers flowing will be decreased, causing a degradation of the device current. For the smallest nanowires diameters, the entire device's volume can be fully depleted due to the presence of interface traps, thus blocking at all the current flow [Han et al. \[2012\]](#). So, when dealing with very small diameters devices, there is the need to carefully model the traps contribution since they can have a detrimental effect on the device's characteristics.

In this thesis project, the interface traps Density Of States(DOS) are modelled with a Gaussian distribution [Synopsys, Inc. \[2015\]](#):

$$D_{it}(E) = N_0 \exp\left(-\left|\frac{E - E_0}{E_s}\right|\right) \quad (4.11)$$

where N_0 is the traps concentration in $\text{eV}^{-1} \text{cm}^{-2}$, E_s is the distribution standard deviation, E_0 is an energy level from which the level corresponding to the maximum of the distribution E_{trap}^0 can be found as:

$$E_{trap}^0 = \frac{\left[E_C + E_V + k_b T \ln\left(\frac{N_V}{N_C}\right)\right]}{2} + E_0 \quad (4.12)$$

To obtain the total interface traps density Q_{it} , the traps density of states $D_{it}(E)$ has to be multiplied by the Fermi-Dirac occupation probability $f(E)$ and integrated over the energy gap [Rassekh et al. \[2019\]](#):

$$Q_{it} = -q \int_{E_V}^{E_C} D_{it}(E) f(E) dE \quad (4.13)$$

Q_{it} is inserted in the right hand side of the quantum corrected Poisson's equation, leading to:

$$\nabla(\epsilon \nabla \phi) = -q \left(N_C F_{\frac{1}{2}} \left(\frac{Ec - E_{F,n} - \Lambda_n}{K_b T} \right) - N_V F_{\frac{1}{2}} \left(\frac{E_{F,p} - E_V - \Lambda_p}{K_b T} \right) + N_D^+ - N_A^- \right) - Q_{it} \quad (4.14)$$

4.3 Mobility models

Mobility is another important parameter which affects the device's performances. It is composed by different contributions. The ones which are taken into account in this work are:

- **phonon scattering** dependent mobility: in a crystal there are collective vibrations of atoms around their equilibrium positions. These quantized vibrations are called phonons and, during their oscillating motion, they may interact with electrons or holes thus degrading the mobility.

The model adopted in this project to describe the phonon scattering contribution is the so called Inversion and Accumulation Layer (IAL) mobility model [Synopsys, Inc. \[2015\]](#), which takes into account of both bulk phonons and surface phonons, which affect the mobility at the interface. The former are treated according to this formula:

$$\mu_{ph,3d} = \mu_{max} \left(\frac{T}{300K} \right)^{-\theta} \quad (4.15)$$

where μ_{max} is the maximum bulk mobility ($\mu_{max} \approx 470.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for holes) and θ is a parameter, reported in table (4.1). For what concern the contribution due to surface phonons, they are treated as follows:

$$\mu_{ph,2D} = \frac{B}{F_{\perp}} + \frac{C(\alpha_{ph,2D,A}((N_A + N_2/2)/1 \text{ cm}^{-3})^{\lambda_{ph,2D,A}} + \alpha_{ph,2D,D}((N_D + N_2/2)/1 \text{ cm}^{-3})^{\lambda_{ph,2D,D}})^{\lambda}}{F_{\perp}^{1/3} (T/300 \text{ K})^k} \quad (4.16)$$

where F_{\perp} is the field which acts normally to the Si/SiO_2 interface, N_A and N_D are the acceptor and donor concentrations respectively. All the other quantities are parameters which are reported in table (4.1). The two phonon scattering mobilities are then combined together:

$$\mu_{ph} = \left[\frac{D}{\mu_{ph,2D}} + \frac{1}{\mu_{ph,3D}} \right]^{-1} \quad (4.17)$$

$D = \exp(-x/l_{crit})$, where x is the distance from the interface and l_{crit} is another parameter reported in table (4.1).

Parameter	Electron value	Hole value	Unit
θ	2.285	2.247	1
B	9.0×10^5	9.0×10^5	cm s^{-1}
C	4400.0	4400.0	$\text{cm}^{5/3} \text{s} / \text{V}^{2/3}$
$\alpha_{ph,2D,A}$	1.0	1.0	1
$\alpha_{ph,2D,D}$	1.0	1.0	1
$\lambda_{ph,2D,A}$	1.0	1.0	1
$\lambda_{ph,2D,D}$	1.0	1.0	1
l_{crit}	10^3	10^3	cm
N_2	1.0.0	1.0	cm^{-3}
λ	0.057	0.057	1
k	1	1	1

Table 4.1: IAL mobility model parameters for phonon scattering in Si

However, it should be remarked that the IAL mobility model does not take into account of an important effect which occurs in nanostructures, described in [Ramayya et al. \[2008\]](#) and [Pokatilov et al. \[2005\]](#). Infact, as the nanowire width becomes smaller than the phonon mean free path (≈ 300 nm in Si) the phonon spectrum is modified due to a mismatch of the sound velocities and the mass densities between the nanowire and the surrounding material (i.e. SiO_2). The phonons characterized by this modified dispersion relation are called confined phonons. The origin of this change can be explained by considering the material's acoustic impedance $\varsigma = \rho V_s$, where ρ is the material's density and V_s is the material's sound velocity. When a soft material (i.e. low ς) surrounds a harder material (i.e. high ς) the phonon energy spectrum of the last one is compressed and its group velocity decreases. The opposite effect is obtained when an hard material surrounds a soft one. Given that Si is acoustically harder than SiO_2 , its group velocity decreases and, being the electron-phonon scattering rate inversely proportional to the group velocity, it increases (Fig.4.2) thus degrading the material mobility (Fig.4.3). To take into account of the phonon confinement effect, the scattering events among carriers and phonons should be treated within a Monte Carlo approach, solved self-consistently with the Poisson's equation. However, it is tricky to integrate the Monte Carlo solver in the Sdevice simulator, so the phonon confinement effect will be neglected.

⁰adapted from [Synopsys, Inc. \[2015\]](#)

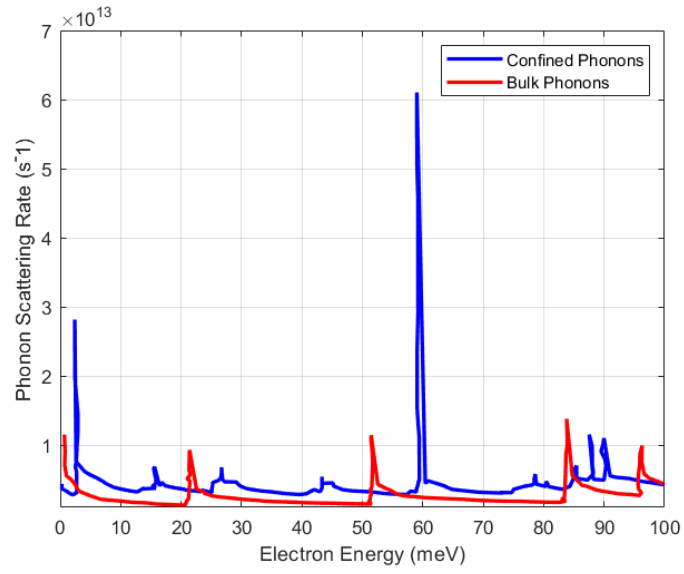


Figure 4.2: Scattering rates for confined and bulk phonons

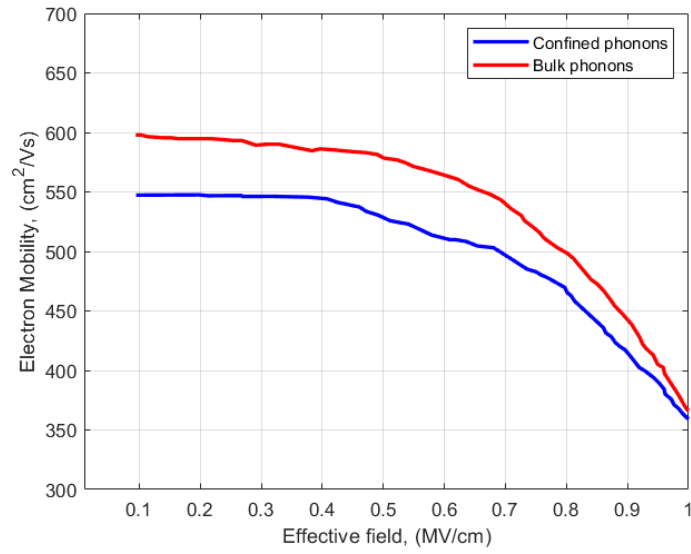


Figure 4.3: Mobility for confined and bulk phonons

⁰adapted from Ramayya et al. [2008]

- **doping** dependent mobility: dopant atoms contribute to increase the amount of carriers which contribute to the conduction, but at the same time they act as a source of impurity, perturbing the otherwise perfectly periodic potential in the lattice. This perturbation scatters the carriers during their flowing, thus degrading their mobility. The default model adopted in Sentaurus Device to treat the impurity scattering dependent mobility is the Masetti model [Synopsys, Inc. \[2015\]](#):

$$\mu_{dop} = \mu_{min1} \exp\left(-\frac{P_c}{N_A + N_D}\right) + \frac{\mu_{ph,3D} - \mu_{min,2}}{1 + ((N_A + N_D)/C_r)^\alpha} - \frac{\mu_1}{1 + (C_s/(N_A + N_D))^\beta} \quad (4.18)$$

where N_A and N_D are the acceptors and donors concentrations respectively and all the other quantities are parameters, which are listed in table (4.2).

Parameter	Electron value	Hole value	Unit
μ_{min1}	52.2	44.9	$\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$
μ_{min2}	52.2	0	$\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$
μ_1	43.4	29.0	$\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$
P_c	0	9.23×10^{16}	cm^{-3}
C_r	9.68×10^{16}	2.23×10^{17}	cm^{-3}
C_s	3.43×10^{20}	6.10×10^{20}	cm^{-3}
α	0.680	0.719	1
β	2.0	2.0	1

Table 4.2: Masetti model parameters

- **surface roughness** dependent mobility: due to the variability related to technological limitations such lithography resolution and unperfect anisotropic etching, there could be a certain surface roughness on the device sidewalls. This acts as a source of scattering for the carriers flowing near the Si/SiO_2 interface. Moreover, given that the surface roughness implies a statistical fluctuation of the nanowire's radius, the average lateral confinement could increase thus causing a shifting of the electrons and holes sub-bands towards higher and lower energies respectively [Lherbier et al. \[2008\]](#). As can be seen from Fig(4.4) and (4.5), this results in a decrease of the electrons and holes mean free path that on its own causes a degradation of the carriers mobilities, given that a lower mean free path corresponds to an higher amount of scattering events.

⁰adapted from [Synopsys, Inc. \[2015\]](#)

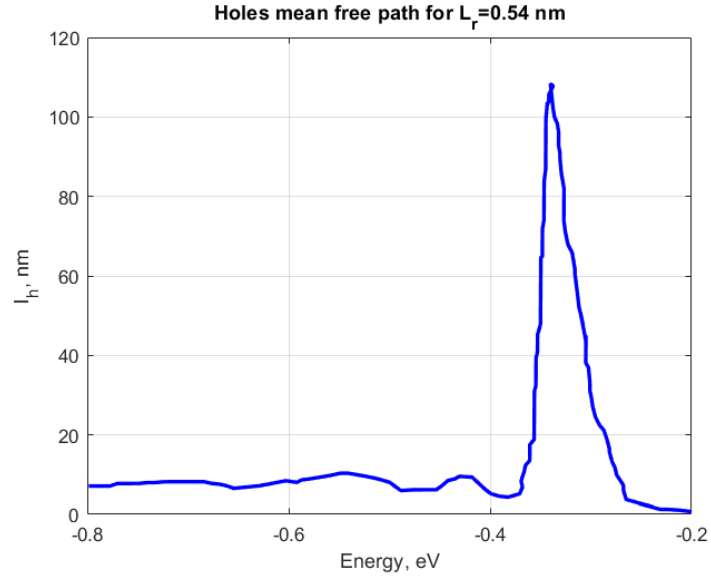


Figure 4.4: Mean free path of the holes for a correlation length of the surface roughness (L_r) equal to 0.54 nm

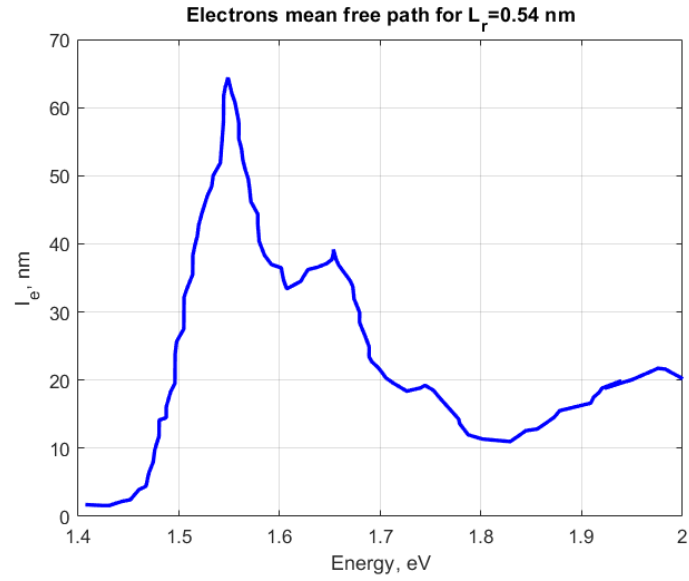


Figure 4.5: Mean free path of the electrons for a correlation length of the surface roughness (L_r) equal to 0.54 nm

⁰adapted from [Lherbier et al. \[2008\]](#)

So the effect of surface roughness needs to be taken into account when dealing with a device with a large surface to volume ratio, since it affects the carriers mobility both directly through the introduction of another scattering term and indirectly, through the alteration of the electronic structure. In the IAL mobility model [Synopsys, Inc. \[2015\]](#), the mobility contribution due to surface roughness is given by:

$$\mu_{sr} = \frac{(\alpha_{sr,A}((N_A + N_2/2)1 \text{ cm}^{-3})^{\lambda_{sr,A}} + \alpha_{sr,D}((N_D + N_2/2)1 \text{ cm}^{-3})^{\lambda_{sr,D}})^{\lambda_{sr}}}{\left(\frac{(F_{\perp}/1 \text{ V/cm})^{A^*}}{\delta} + \frac{F_{\perp}^3}{\eta} \right)} \quad (4.19)$$

where:

$$A^* = A + \frac{\alpha_{\perp}(n + p)}{((N_A + N_D + N_1)/1 \text{ cm}^{-3})^{\nu}} \quad (4.20)$$

where n and p are the electrons and holes concentrations respectively. All the other quantities are parameters listed in the following table:

Parameter	Electron value	Hole value	Unit
α_{\perp}	0	0	cm^{-3}
$\alpha_{sr,A}$	1.0	1.0	1
$\alpha_{sr,D}$	1.0	1.0	1
$\lambda_{sr,A}$	1.0	1.0	1
$\lambda_{sr,D}$	1.0	1.0	1
λ_{sr}	0.057	0.057	1
N_1	1.0	1.0	cm^{-3}
N_2	1.0	1.0	cm^{-3}
δ	3.97×10^{13}	3.97×10^{13}	$\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$
η	1.0×10^{50}	1.0×10^{50}	$\text{V}^2/\text{cm/s}$
A	2.0	2.0	1
ν	0	0	1

Table 4.3: IAL mobility model parameters for surface roughness scattering

- **coulomb scattering** dependent mobility: a further contribution to the mobility degradation is given by Coulomb scattering, which consists in a deviation of the carriers trajectories due to the electrostatic interaction among them and the ionized impurities present in the bulk and at the surface. Also this effect is modelled by the IAL mobility model. Differently with respect to the other mobility terms, the calculations are quite long and so are omitted. Further details are reported in [Synopsys, Inc. \[2015\]](#).

⁰adapted from [Synopsys, Inc. \[2015\]](#)

The different mobility contributions are combined together by the so called **Mathiessen's rule**, which reads as:

$$\frac{1}{\mu} = \frac{1}{\mu_{dop}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_c} + \frac{D}{\mu_{sr}} \quad (4.21)$$

4.4 Velocity saturation

Another effect which is taken into account in the Sdevice simulator is the saturation of the carriers velocity which occurs at high electric fields. For low fields, the velocity increases linearly to the the applied field through a proportionality coefficient which is the low field mobility (i.e.the mobility resulting from all the contributions described in the previous section):

$$v = \mu_{low} \vec{E} \quad (4.22)$$

As the field reaches high values, the scattering rate increases more and more and at a certain point the relaxation time (i.e.the time which separates two scattering events) becomes so small that the carriers don't manage to increase their momentum in between two scattering events. As a consequence the velocity increases linearly up to a certain maximum, after which remains more or less constant. The default model adopted in Sentaurus to describe the velocity saturation effect is the Canali model [Synopsys, Inc. \[2015\]](#):

$$\mu = \frac{(\alpha + 1)\mu_{low}}{\alpha + \left[1 + \left(\frac{(\alpha+1)\mu_{low}\vec{E}}{v_{sat}} \right)^\beta \right]^{\frac{1}{\beta}}} \quad (4.23)$$

where \vec{E} is the electric field, v_{sat} is the saturation velocity, α is a parameter defined in Table (4.4), β is an exponent given by:

$$\beta = \beta_0 \left(\frac{T}{300 \text{ K}} \right)^{\beta_{exp}} \quad (4.24)$$

where T is the lattice temperature, β_0 and β_{exp} are parameters defined in the following table:

Parameter	Electron value	Hole value	Unit
α	0	0	1
β_0	1.109	1.213	1
β_{exp}	0.66	0.17	1

Table 4.4: Canali model parameters

⁰adapted from [Synopsys, Inc. \[2015\]](#)

4.5 Shockley-Read-Hall recombination

In a semiconductor there could often be some defects present inside the lattice, which originate a level E_T within the forbidden energy gap. Depending on the energy position of the level E_T , the defects can ex-change carriers with one or both the transport bands. In particular, if E_T is too close with one of the two bands then it will give rise to a simple trapping mechanism, in which electrons or holes are captured by the trapping level and then remain there or are excited back to the bands from which they have been captured. If instead the level E_T is located more or less in the middle of the energy gap, then the interaction probability with both the transport bands is maximized and so an electron can be captured by the trap level and then be relaxed in the valence band, giving rise to a complete recombination process. This kind of transition is called Shockley-Read-Hall(SRH) recombination and is characterized by the following net recombination rate [Synopsys, Inc. \[2015\]](#):

$$U_{SRH} = \frac{np - n_i^2}{\tau_{n0}(p + p_1) + \tau_{p0}(n + n_1)} \quad (4.25)$$

where n and p are the electrons and holes concentrations respectively, n_i is the intrinsic concentration (i.e.the concentration of the intrinsic semiconductor), n_1 and p_1 are the electrons and holes densities that would be present in the trap level E_T if the last one would be coincident with the intrinsic Fermi level. τ_{n0} and τ_{p0} are the electrons and holes SRH lifetimes, defined as:

$$\tau_{n0} = \frac{1}{C_n N_T} \quad (4.26)$$

$$\tau_{p0} = \frac{1}{C_p N_T} \quad (4.27)$$

where N_T is the defects concentration per unit of volume, C_n and C_p are the capture coefficients for electrons and holes respectively, defined in cm^6/s . They are related to the probability for electrons and holes to be captured by the impurity level E_T .

4.6 Incomplete ionization

The amount of carriers concentration in a doped semiconductor varies as a function of the temperature following three regimes:

- **the frozen region:** within this limit, the amount of thermal energy is not enough to allow for all the impurities present in the lattice to be ionized, releasing their extra electrons or holes to the conduction band or the valence band respectively. As a consequence, some impurity atoms remain neutral, with their extra-carrier still bounded to them.
- **the saturation region:** when the lattice temperature is high enough, all the impurities get ionized and over this temperature interval the majority carriers concentration is constant.

- **the intrinsic region:** if the temperature further increases, the thermal energy becomes so high that starts to promote transitions from the valence band to the conduction band and the amount of majority carriers concentration starts to increase again.

The simulations are performed at 300 K. This temperature should in teory fall in the saturation region. However, in practice, there could be some impurities that are not ionized yet. So, in order to have a correct prediction of the amount of majority carriers which contribute to the conduction, the incomplete ionization effect must be included in the simulations. Sentaurus Device exploits the following model to treat this effect [Synopsis, Inc. \[2015\]](#):

$$N_D^+ = \frac{N_{D,0}}{1 + g_D \frac{n}{n_1}} \quad (4.28)$$

$$N_A^+ = \frac{N_{A,0}}{1 + g_A \frac{p}{p_1}} \quad (4.29)$$

where $N_{D,0}$ and $N_{A,0}$ are the total concentrations of donors and acceptors impurities respectively, g_D and g_A are the degeneracy factors for the impurity levels(i.e. the number of states which that level hosts), n_1 and p_1 are given by:

$$n_1 = N_C \exp\left(-\frac{\Delta E_D}{K_b T}\right) \quad (4.30)$$

$$p_1 = N_V \exp\left(-\frac{\Delta E_A}{K_b T}\right) \quad (4.31)$$

where ΔE_D and ΔE_A are the donors and acceptors activation energies respectively(i.e. the amount of energy which an electron(hole) hosted in the impurity level must gain in order to be promoted in the conduction band(valence band)).

4.7 Band-To-Band-Tunneling

Another effect which has to be included in the simulator so as to get an accurate description of the off behaviour of the device is the Band-To-Band-Tunneling(BTBT) mechanism. It is a phenomena which contributes to increase the off state current of the device and takes place if there is a sufficient overlap between the valence and the conduction band of the channel and drain region respectively [Gundapaneni et al. \[2012\]](#). If this is the case, in an n type device an electron can tunnel from the valence band of the channel to the conduction band of the drain, leaving behind an hole in the channel [Gundapaneni et al. \[2012\]](#). The opposite effect is obtained in a p type device, where an electron tunnels from the channel conduction band to the drain valence band. Moreover, since the BTBT rate is a strong function of the electric field [Schenk \[1993\]](#), in order to have this effect taking place in a significant way the field inside the device must not be lower than $\approx 1 \text{ MV cm}^{-1}$. The default model adopted in Sentaurus to model the BTBT contribution is the Schenk model

Synopsys, Inc. [2015], Schenk [1993], which describes the BTBT mechanism by means of a net recombination rate:

$$R_{net}^{bb} = AF^{7/2} \frac{np - n_i^2}{(n + n_i)(p + n_i)} \left[\frac{((F_c^\mp)^{-3/2} \exp\left(-\frac{F_c^\mp}{F}\right))}{\exp\left(\frac{\hbar\omega}{K_b T}\right)} + \frac{(F_c^\pm)^{-3/2} \exp\left(-\frac{F_c^\pm}{F}\right)}{\exp\left(\frac{\hbar\omega}{K_b T}\right)} \right] \quad (4.32)$$

where A is a parameter ($8.977 \times 10^{20} \text{ cm}^{-1} \text{ s}^{-1} \text{ V}^{-2}$), F is the electric field, n and p are the electrons and holes densities respectively, n_i is the electrons intrinsic density, $\hbar\omega$ is the energy of the transverse acoustic phonon which supports the transition ($\approx 18.6 \text{ meV}$). F_c is defined as:

$$F_c^\pm = B(E_g \pm \hbar\omega)^{3/2} \quad (4.33)$$

where B is a parameter ($2.14667 \times 10^7 \text{ Vcm}^{-1} \text{ eV}^{-3/2}$) and E_g is the energy gap. The upper sign in Eq.4.32 and 4.33 corresponds to BTBT generation, while the lower sign corresponds to BTBT recombination.

Chapter 5

Process simulations

The process described in chapter 2 is now reproduced by means of the Synopsys Sentaurus Process software, with the aim of matching the experimental results taken from [Kumar et al. \[2024\]](#). A similar work has been done in [Rossi et al. \[2023\]](#), however considering a different nanowire diameter and achieving different results. The device parameters are summarized in this table:

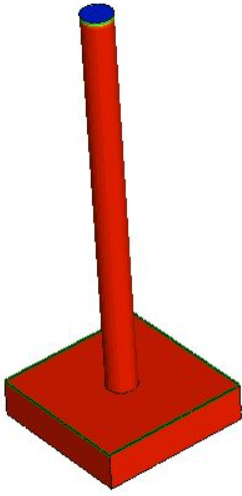
N_A	$3.5 \times 10^{19} \text{ cm}^{-3}$
D_{nw}	16 nm
H_{nm}	210 nm
T_{PtSi}	10 nm
L_g	18 nm
T_{ox}	4 nm

With the aim of reducing the complexity and the simulation time, the process steps are simplified with respect to those adopted at experimental level. They can be summarized as follows:

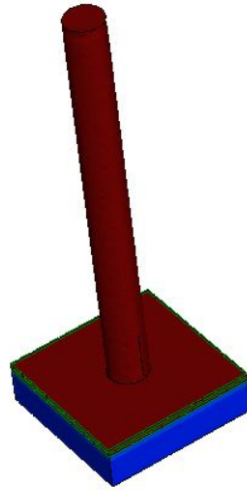
- **vertical nanowire creation** (Fig.5.1.a): given that Sentaurus Process does not support the creation of complex geometrical structures such as cylinders, the vertical nanowire is created by means of Sentaurus Structure Editor. Thus the complex lithographic process described in chapter 2 is reduced to the creation of a cylindrical resist, which acts as a mask for the etching process, which is performed by a simple anisotropic etching command, since RIE is not feasible within the Sentaurus Process framework.
- **gate oxide creation** (Fig.5.1.b): differently with respect to the real process, the oxidation is not performed in two steps of 850 °C and 725 °C for 10 min and 30 min respectively, but is subdivided in six steps of 30 s each, four at 850 °C, two at 950 °C up to obtain an oxide thickness of about 4 nm. This is related to the fact that oxidation, together with silicidation, are the most computationally intensive processes and are very mesh sensitive, thus can also lead to convergence issues. As a consequence it has been necessary to subdivide the longer oxidation steps exploited

in the real process in smaller steps. Then follows an anisotropic etching step so as to etch the oxide at the top and at the bottom of the nanowire (Fig.5.1.c).

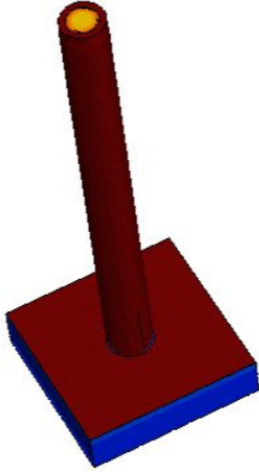
- **PtSi contacts deposition** (Fig.5.1.d): as explained in chapter 2, in the real process the PtSi contacts are created by an anisotropic deposition step followed by a rapid thermal annealing so as to activate the silicides. However it was not possible to reproduce the anisotropic deposition with the SProcess tool, since convergence issues arise due to geometrical constraints related to the fact that the oxidation process has made the top nanowire surface not completely flat. Thus the deposition of the Pt layers at the top and at the bottom of the nanowire has been realised in two steps. Firstly, a cylindrical Pt layer has been created by Sentaurus Structure Editor, so as to cover the top nanowire's surface. Then, to create the Pt layer at the bottom of the nanowire, a filling procedure was adopted. It consists in depositing a material up to a certain vertical coordinate. Moreover, the silicidation process has been skipped since it was too much computationally intensive.
- **spacers and gate creation** (Fig.5.1.e): the filling procedure was adopted also for the creation of the spacers layers and the metal gate, which are created in succession one after the other. This is another simplification since in the real process the HSQ spacers are created by a spin coating step followed by a chemical etch back.
- **contacts definition** (Fig.5.1.f): finally, the Al contacts pads are not created and the contacts are directly defined in the Pt layers. However, this is not a problem from the contact resistance point of view since the correct PtSi workfunction has been imposed in the Sdevice cmd file.



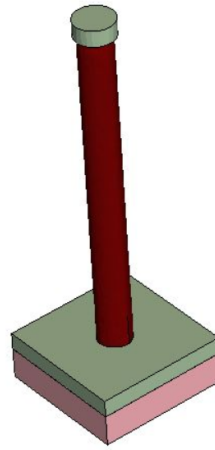
(a) Vertical Si NW creation



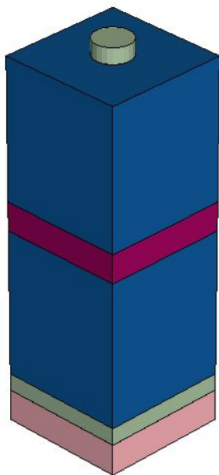
(b) Gate oxide growth



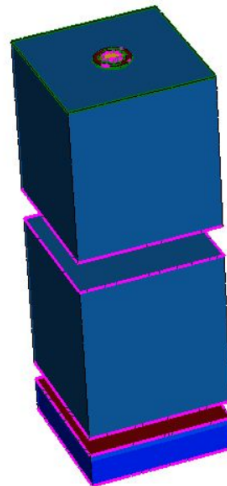
(c) Gate oxide etching



(d) Silicides contacts creation



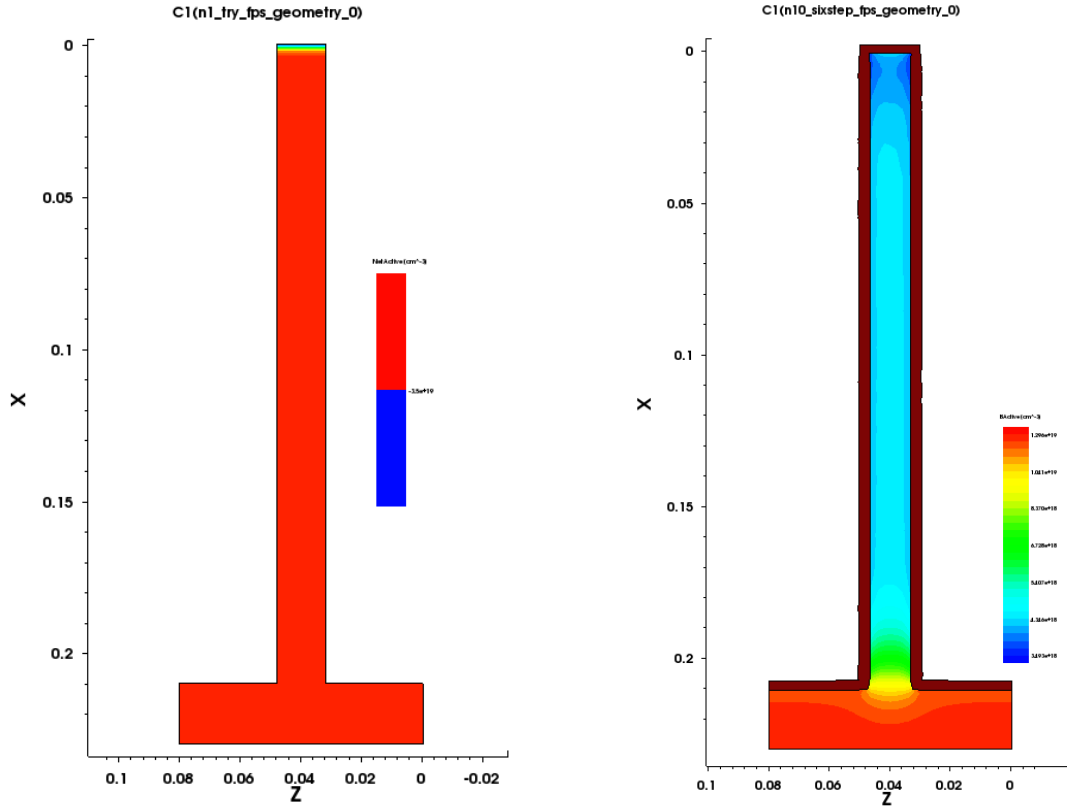
(e) Spacers and gate deposition



(f) Contacts creation

Figure 5.1: Main process steps

Some remark about the oxidation process has to be done. Firstly, as can be seen from Fig.(5.1.c), there is some residual oxide remaining at the bottom of the structure, which in the real process does not appear. The reason behind this is that the oxide anisotropic etching rate must be carefully tailored, since if it increases too much the cylindrical Pt contact deposition fails. As a consequence the oxide etching rate is a little bit reduced thus causing some residual oxide remaining at the bottom of the wire, which however, as will be shown in the next chapter, does not affect the electrical performances. The second aspect related to the oxidation step which should be highlighted is that, at the end of the process, the concentration of active Boron decreases of about one order of magnitude due to the Boron segregation into the oxide layer. This effect, already caught in [Rossi et al. \[2023\]](#) and [Rossi et al. \[2024\]](#), can be observed in the 2D and 3D Boron active distribution in the nanowire at the end of the oxidation step:



(a) Boron active concentration before the oxidation step

(b) Boron active concentration after the oxidation step

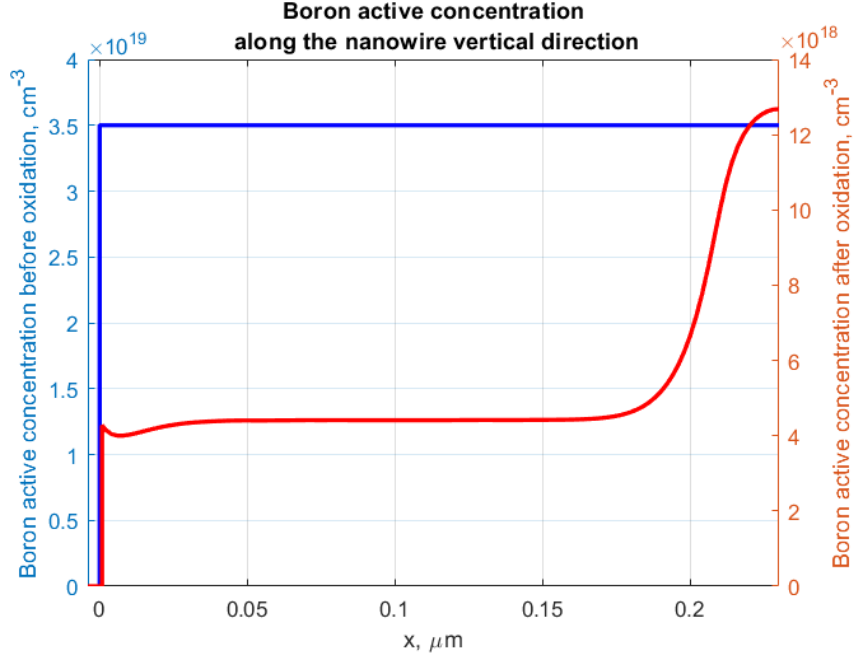


Figure 5.3: Boron active concentrations along the nanowire height direction

This abrupt decrease of the dopants concentration deeply impact on the device electrical performances and, given that the oxidation step is not performed at the same temperature and for the same amount of time as in the real process, the resulting Boron distribution could not be the same as the one of the real device. This is one of the factors which most contribute to the origin of the error between the Sentaurus results and the experimental data.

Chapter 6

Electrical simulations

6.1 Subthreshold slope fitting

The device illustrated in the previous chapter is now simulated by Synopsys Sentaurus Device with the aim of extracting the electrical transcharacteristics to be compared with the ones taken from [Kumar et al. \[2024\]](#) and extracting some microscopic quantities which will be useful to match the simulations results with the compact model which will be presented in the Second part of the project. Firstly, the effect of interface traps on the subthreshold slope is investigated. Considering a Gaussian distribution of the interface traps density of states, the traps concentration is varied between three orders of magnitude up to obtain a subthreshold slope similar to the experimental one. Firstly, acceptor types interface traps are considered, then donor type will be introduced to obtain a better fit against the experimental data. The values for the energy level corresponding to the maximum of the distribution(E_T) and the distribution standard deviation(σ_T) have been taken from [Bugliarelli \[2023\]](#). However, a traps concentration different with respect to the one adopted in that work is needed to fit the experimental results. This is probably attributed to the fact that in [Bugliarelli \[2023\]](#) an higher diameter nanowire has been simulated. Thus, being the surface to volume ratio lower, the interface properties play a less important role and so a lower amount of traps is required to have a match with the experimental results.

Cr workfunction	PtSi workfunction	Traps type	E_T	σ_T
4.2 eV	5.2 eV	Acceptor	-0.3 eV	0.2 eV

Table 6.1: Acceptor type device parameters

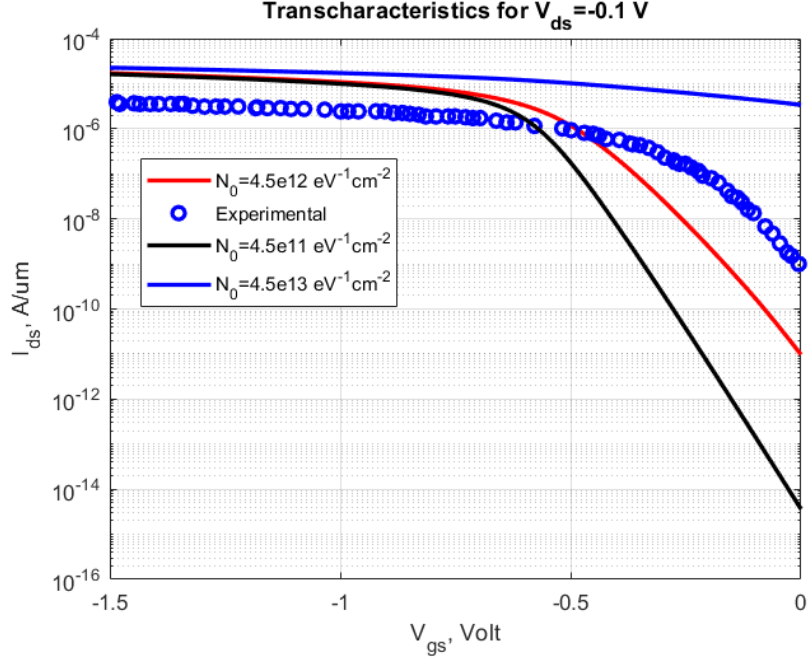


Figure 6.1: .Transcharacteristics for acceptor type interface traps

	SS	V_{th}
Experimental	74 mV/dec	-0.1 V
$N_0 = 4.5 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$	61.71 mV/dec	-0.461 V
$N_0 = 4.5 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$	77.98 mV/dec	-0.339 V
$N_0 = 4.5 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$	870.19 mV/dec	0.799 V

Table 6.2: Simulation results for different acceptor type interface traps densities

As can be seen from the upper data, the increase of the traps density results in a SS degradation, since the amount of traps affects the gate control over the channel. This statement can be verified by observing the electrostatic potential behaviour along the nanowire cross-section at equilibrium:

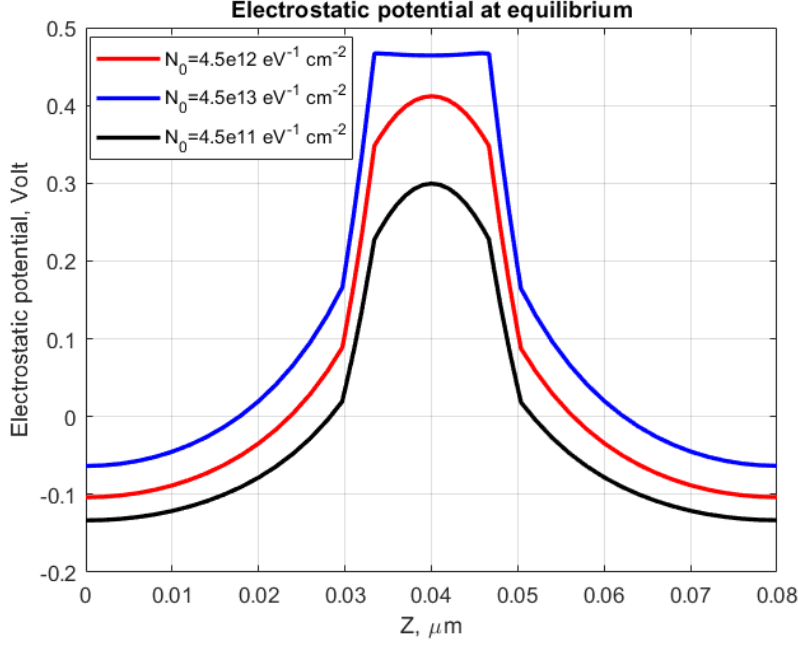


Figure 6.2: .Electrostatic potential at equilibrium for different traps concentrations

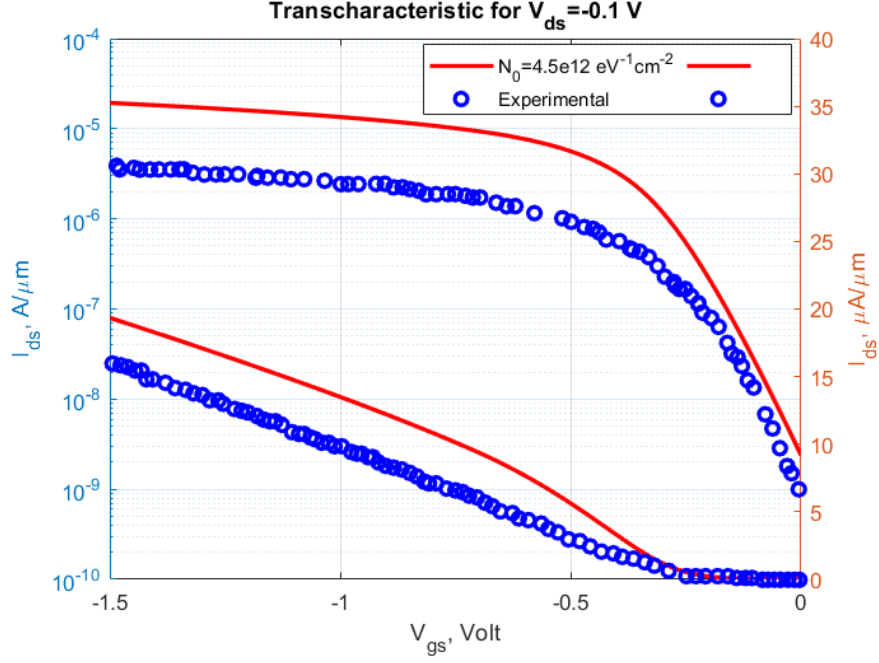
As can be seen from Fig.(6.2), an higher concentration of interface traps causes an increase of the electrostatic potential barrier at the center of the channel, so will be trickier for the gate to control the channel conductivity.

6.2 Threshold voltage fitting

For $N_0 = 4.5 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$, a SS quite similar to the experimental one is obtained. However the V_{th} is different with respect to the real value. In order to compensate for this mismatch, the Cr workfunction is tuned from 4.2 eV to 4.4 eV. This is related to the fact that the V_{th} is given by:

$$V_{th} = V_{fb} - \frac{Q_{dep}}{C_{ox}} \quad (6.1)$$

where V_{fb} is the flat-band voltage(which is the difference between the metal gate workfunction and the semiconductor one), Q_{dep} is the depletion charge and C_{ox} is the gate oxide capacitance. As a consequence, a change of the metal gate workfunction modulates the flat-band voltage which on its own causes a V_{th} shift, allowing for a better fit of the experimental results.

Figure 6.3: .Transcharacteristic for $q\Phi = 4.4$ eV

	SS	V_{th}	I_{on}
Experimental	74 mV/dec	-0.1 V	3.88×10^{-6} A μm^{-1}
$N_0 = 4.5 \times 10^{12}$ eV $^{-1}$ cm $^{-2}$	77.98 mV/dec	-0.151 V	1.93×10^{-5} A μm^{-1}

Table 6.3: Simulation results for $q\Phi = 4.4$ eV

6.3 On current fitting

As can be caught from the data of Table (6.3), the experimental on current is one order of magnitude lower than the one obtained from the Sentaurus simulation. To overcome this issue, interface traps of donor type are considered since, as explained in chapter 4, this kind of traps causes a radial depletion of carriers in p type Si nanowires. As a consequence, the current is expected to be reduced with respect to the one of the device with acceptor type interface traps.

Cr workfunction	PtSi workfunction	Traps type	Concentration	E_T	σ_T
4.4 eV	5.2 eV	Donor	$5.0 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$	-0.3 eV	0.2 eV

Table 6.4: Parameters for the device with donor type interface traps

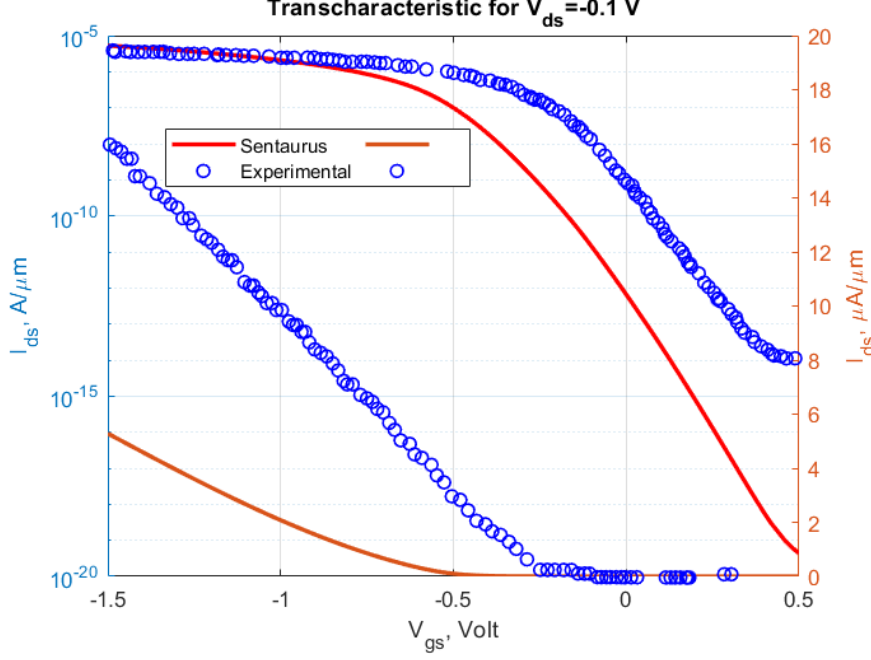


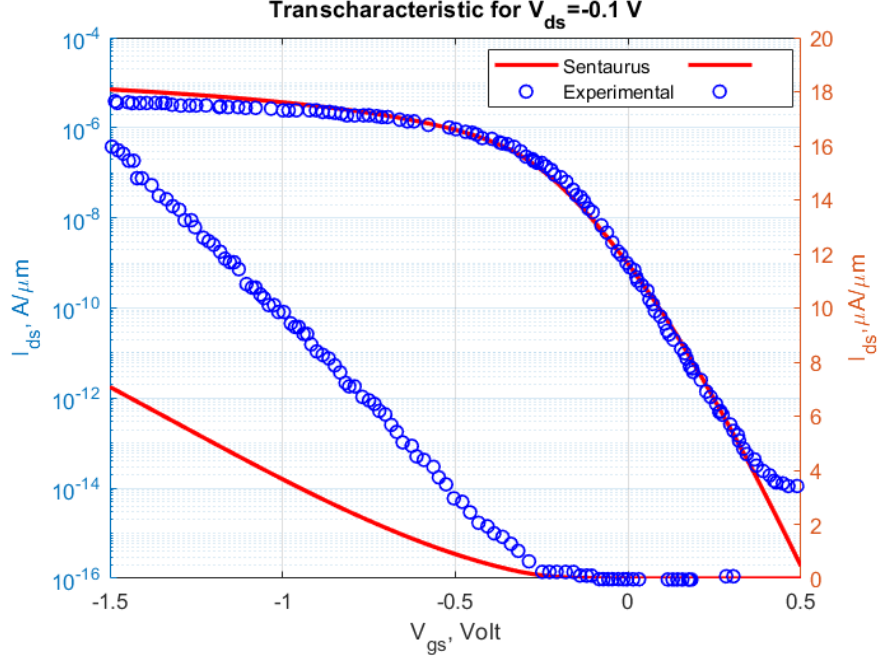
Figure 6.4: .Transcharacteristic for donor type interface traps

	SS	V_{th}	I_{on}
Experimental	74 mV/dec	-0.1 V	$3.88 \times 10^{-6} \text{ A } \mu\text{m}^{-1}$
Sentaurs	74.18 mV/dec	-0.376 V	$5.28 \times 10^{-6} \text{ A } \mu\text{m}^{-1}$

Table 6.5: Simulation results for donor type interface traps

With the aim of better highlighting the subthreshold behaviour, the operating voltage has been extended up to 0.5 V, according to the experimental data. Moreover, given that for $N_0 = 4.5 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ the simulation does not converge, the traps concentration has been increased to $N_0 = 5.0 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$. This results in a SS exactly equal to the experimental one. This could sound a little bit strange since by increasing the traps concentration one would expect an increase of the SS. The reason behind this is that the subthreshold region of the transcharacteristic is not exactly linear so depending on the region in which is fitted the SS could slightly change. Also the V_{th} is changed. Nonetheless, by adjusting the Cr workfunction, a good fit of the real V_{th} is recovered.

Cr workfunction	PtSi workfunction	Traps type	Concentration	E_T	σ_T
4.66 eV	5.2 eV	Donor	$5.0 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$	-0.3 eV	0.2 eV

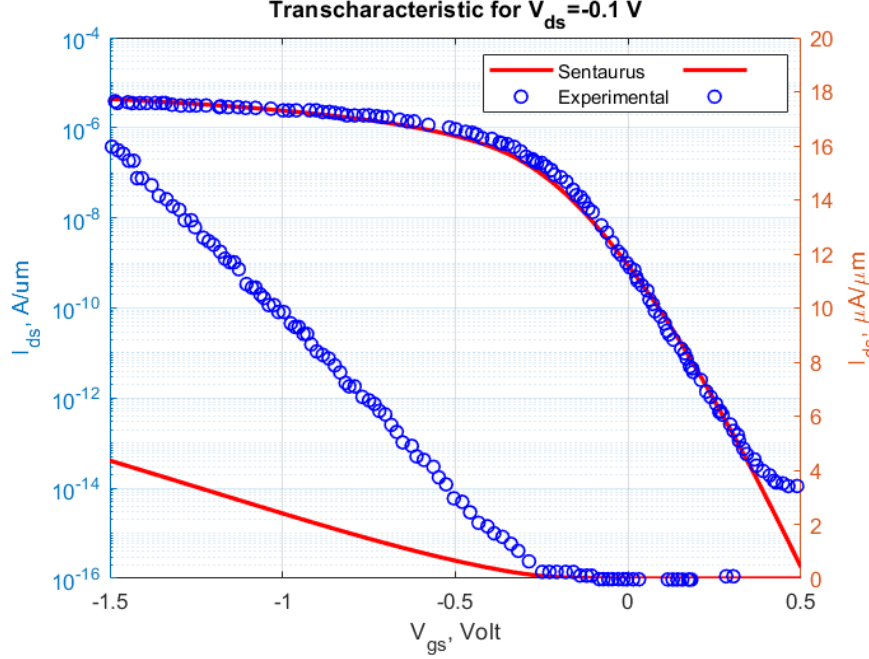
 Table 6.6: Parameters for the device with donor type interface traps, after gate $q\phi$ tuning

 Figure 6.5: .Transcharacteristic for donor type interface traps, after gate $q\phi$ tuning

	SS	V_{th}	I_{on}
Experimental	74 mV/dec	-0.1 V	$3.88 \times 10^{-6} \text{ A } \mu\text{m}^{-1}$
Sentaurus	74.18 mV/dec	-0.105 V	$7.08 \times 10^{-6} \text{ A } \mu\text{m}^{-1}$

 Table 6.7: Simulation results for donor type interface traps, after gate $q\phi$ tuning

As can be seen from the upper figure, a slight mismatch between the on current of the simulated device and the experimental one still exists. It can be eliminated by reducing the PtSi workfunction to 5.0 eV.

Cr workfunction	PtSi workfunction	Traps type	Concentration	E_T	σ_T
4.66 eV	5.0 eV	Donor	$5.0 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$	-0.3 eV	0.2 eV

Table 6.8: Parameters for the device with donor type interface traps,after PtSi $q\phi$ tuning

Figure 6.6: .Transcharacteristic for donor type interface traps,after PtSi $q\phi$ tuning

	SS	V_{th}	I_{on}
Experimental	74 mV/dec	-0.1 V	$3.88 \times 10^{-6} \text{ A } \mu\text{m}^{-1}$
Setaurus	74.18 mV/dec	-0.105 V	$4.35 \times 10^{-6} \text{ A } \mu\text{m}^{-1}$

Table 6.9: Simulation results for donor type interface traps,after PtSi $q\phi$ tuning

After the PtSi workfunction tuning, an almost precise fit of the transcharacteristic in logarithmic scale is obtained. However, in linear scale the transcharacteristic is quite different with respect to the real one. This originates a uge relative error, which exceeds 100%. So, in order to obtain an acceptable error, interface traps of acceptor type are considered again. The results illustrated in Fig.(6.3) have been a little bit ameliorated by changing the interface traps concentration and adjusting the PtSi and Cr workfunction.

Cr workfunction	PtSi workfunction	Traps type	Concentration	E_T	σ_T
4.35 eV	5.0 eV	Acceptor	$5.0 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$	-0.3 eV	0.2 eV

Table 6.10: Final device parameters

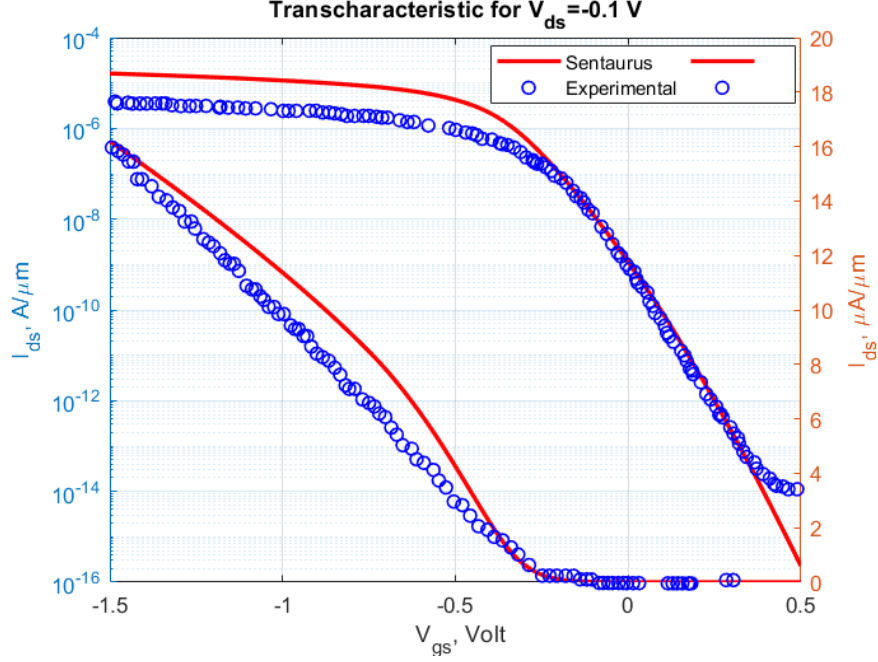


Figure 6.7: .Final transcharacteristic

	SS	V_{th}	I_{on}
Experimental	74 mV/dec	-0.1 V	15.96 $\mu\text{A } \mu\text{m}^{-1}$
Sientaurus	74.18 mV/dec	-0.179 V	16.19 $\mu\text{A } \mu\text{m}^{-1}$

Table 6.11: Simulation results of the final device

As can be caught from Fig.(6.7), the current values in logarithmic scale are not the same as in the case of donor type interface traps, but the curves in linear scale are quite similar. This helps to reduce the relative error. Notice that, due to some trouble in extracting the experimental data with the MATLAB Grabit function which can cause a divergence of the relative error, it has been necessary to compute it by taking as a denominator the maximum in between the simulated current associated to the specific gate voltage and the average of all the currents associated to each voltage of the loop performed over the bias range.

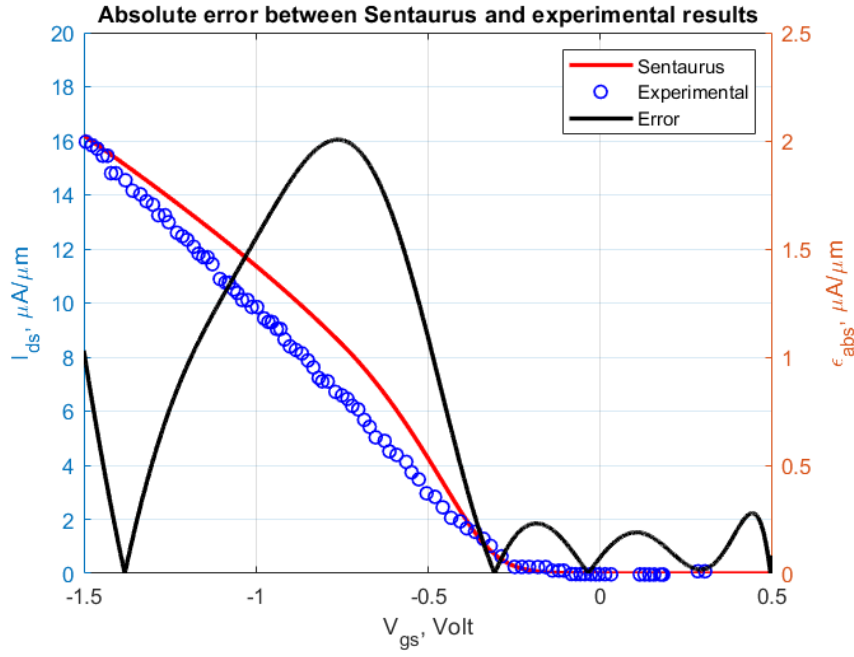


Figure 6.8: .Absolute error between Sentaurus and experimental results

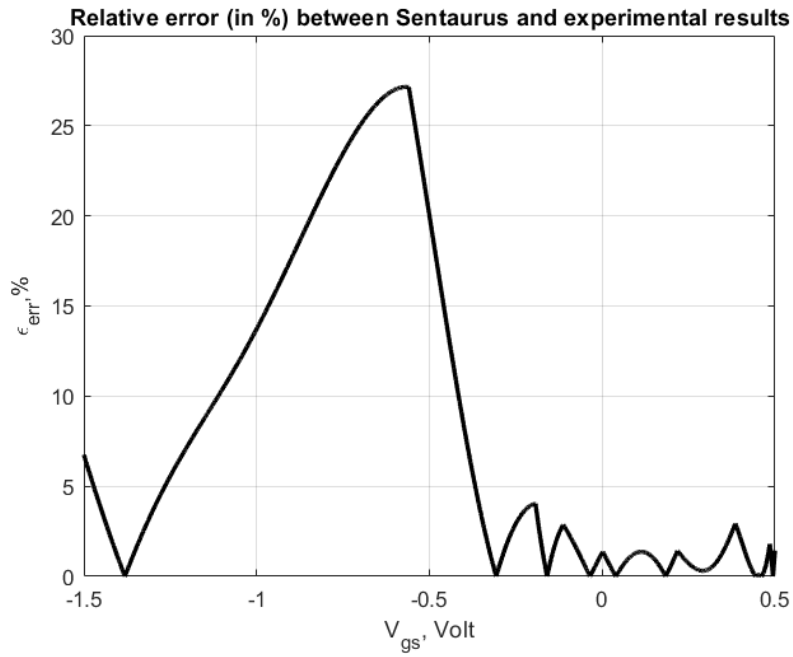


Figure 6.9: .Relative error between Sentaurus and experimental results

As shown in the aforementioned figures, the absolute error reaches a peak of about 2 while the relative one increases up to a maximum of 27.15%. The origin of the error could be attributed to three main reasons:

- **ideal process simulation:** as explained in the previous chapter, the simulated process is highly simplified with respect to the real one. As a consequence there are certain aspects which are not caught. For instance, even though in the real process the RIE step is properly optimized so as to reduce as much as possible the micro-trenching effects and maximize the anisotropy, actually the resulting nanowire is not perfectly cylindrical but tends to assume a conical shape. Thus the perfect cylinder which is created by Sentaurus Structure Editor could not faithfully describe the real geometry. Moreover, the Al contact pads are not created and the contacts are directly defined in the PtSi terminations. As already explained, this is not a problem from the contact resistance point of view since the PtSi workfunction is imposed in the Electrode section of the Sdevice file. However, in the real device there is an additional resistive contribution due to the Al contacts, which is missing in this work. This simplification contributes to the overestimation of the drain current.
- **lack of the confined acoustic phonons** contribution: as illustrated in Fig.(4.3) of chapter four, the modification of the phonon spectrum which occurs when the device width becomes smaller than the phonon mean free path results in an increase of the carrier-phonon scattering rate and as a consequence in a decrease of the carriers mobility. Given that this aspect is not taken into account in the simulations, the resulting mobility will be higher than the one of the real device, leading to a further increase of the drain current.
- **In-exact Boron distribution** in the nanowire: as previously mentioned, one of the main factors which most affects the device's performances is the resulting doping distribution after the oxidation process. Given that the parameters of the oxidation step are not the same as the ones of the real process, the amount of Boron in the device is different with respect to the one obtained at experimental level and is probably higher given that the simulated oxidation is much shorter than the real one. The higher amount of active dopants is another source which contributes to overestimate the drain current. This in-exact Boron distribution could also explain the lower off current in logarithmic scale. Infact, as explained in chapter four, one possible source of leakage which contributes to increase the off current is the BTBT. However, in order to have this mechanism taking place, there must be a sufficient overlap between the valence band and the conduction band and the electric field must be high enough ($\approx 1\text{MV cm}^{-1}$). In the case of the simulated device, given that the oxidation time is too short, the doping segregation phenomena is relatively limited and thus there is not the formation of large doping gradients which help to increase the band bending. Infact, as can be seen from Fig.6.10, the bands are quite smooth, as a consequence the tunneling width is high. Moreover, as shown in Fig.6.11, the electric field along the nanowire vertical direction is not high enough to trigger the mechanism.

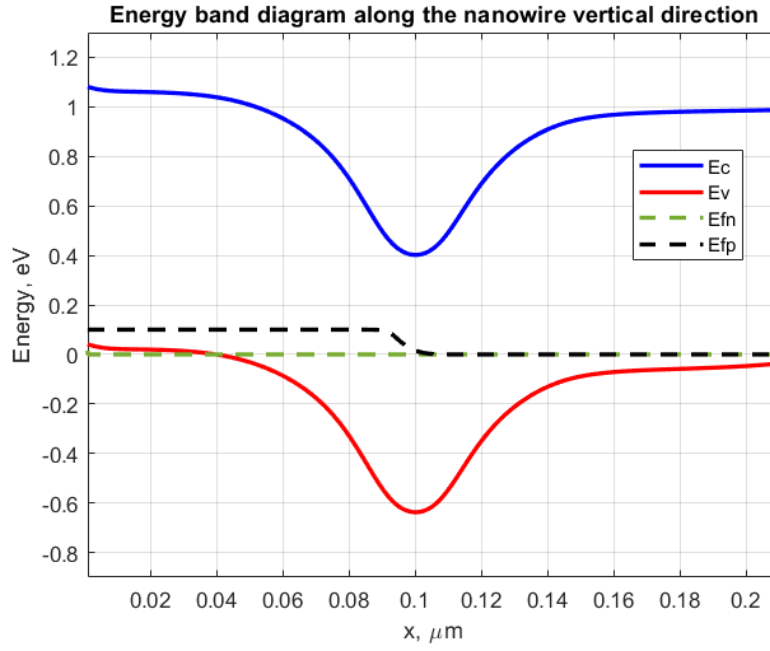


Figure 6.10: .Band diagram along the nanowire vertical direction

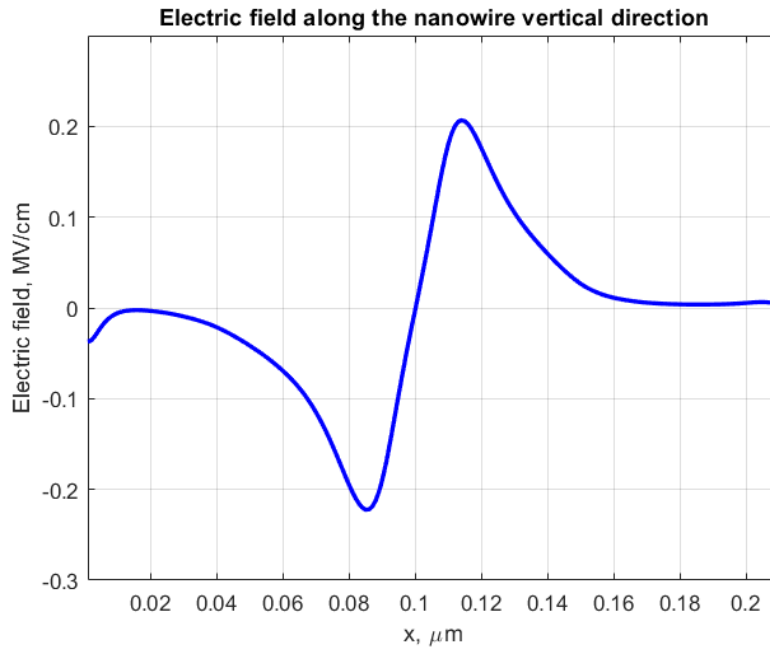


Figure 6.11: .Electric field along the nanowire vertical direction

As a result, even if the BTBT model is enabled in the Physics section of the SDevice file, it does not take place, as can be assessed in Fig.6.12. So the off current in logarithmic scale is lower than the experimental one.

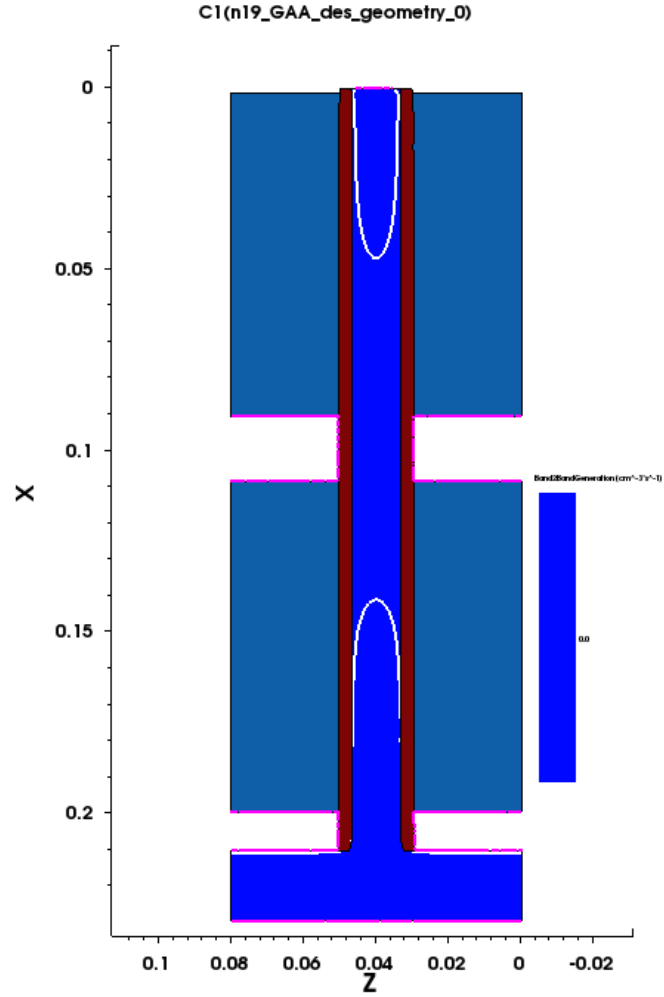


Figure 6.12: .BTBT map along the nanowire vertical direction

Part II

Second Part

Chapter 7

Compact modelling

7.1 Introduction

As explained in the first part of the thesis, the second step of the DTCO loop consists of simulating vertical JNT based logic circuits. To this aim, a compact model compatible with circuits simulators such as SPICE should be defined. This model should meet a series of requirements [Hamzah et al. \[2019\]](#): apart from being physically accurate, it must be continuous over the entire bias range, since a piece-wise model requires additional smoothing functions to unify the different operating regions. This can increase the simulation time and lead to convergence issues. Moreover, the model must have an explicit form, otherwise an iterative solution is required further increasing the computational cost. In the second part of this work, an explicit continuous model for the drain current of a vertical junctionless transistor inherited from literature is presented and its MATLAB implementation is validated against the experimental results of measurements on devices fabricated at the LAAS-CNRS. Firstly, the long channel expression for the drain current is derived, following all the steps present in [Hamzah et al. \[2019\]](#), in which the Unified Charge Based Control Model (UCCM) expression is obtained by exploiting the parabolic potential approximation and the model is made continuous by decoupling the total mobile charge into the depletion and complementary contributions, which are expressed in an explicit way by means of the Lambert's functions. Finally, the model is adapted to short channel devices by taking into account of short channel effects [Lime et al. \[2017\]](#), [Mukherjee et al. \[2021\]](#).

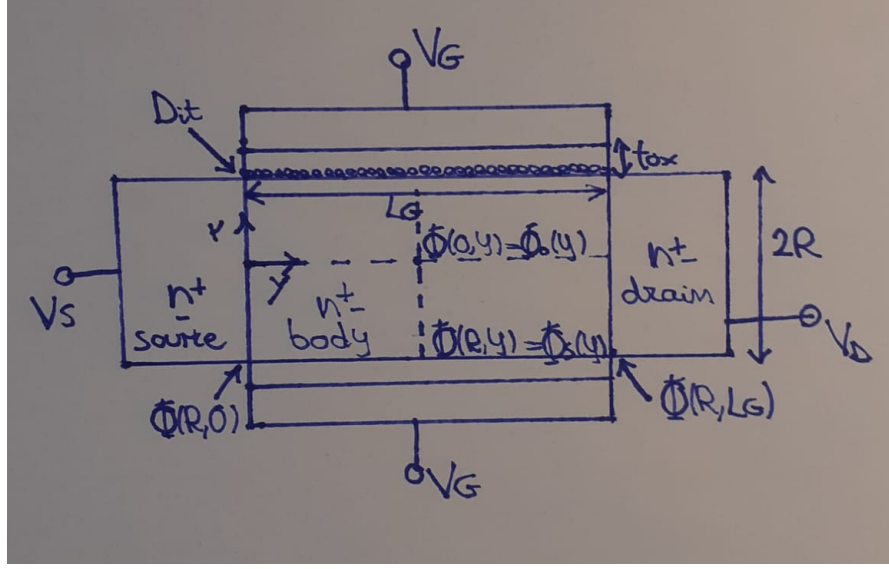


Figure 7.1: .Schematic diagram for the JNT

7.2 Model derivation

As explained in the introduction, the long channel expression for the drain current of a JNT is now derived following closely all the passages and the explanatory comments present in [Hamzah et al. \[2019\]](#). The starting point is the Poisson's equation written in radial form :

$$\frac{1}{r} \frac{d}{dr} \left(r \frac{d\phi(r)}{dr} \right) = \frac{qN_D}{\epsilon_{si}} \left(-1 + \exp \left(\frac{\phi(r) - V}{\phi_t} \right) \right) \quad (7.1)$$

In this primary version, a long channel device is considered, thus the long channel approximation can be assumed, which allows to treat the Poisson's equation in its one dimensional form. Multiplying both sides of equation (7.1) by r and integrating from 0 to r gives:

$$\frac{d\phi(r)}{dr} = -\frac{qN_D}{2\epsilon_{si}} r + \frac{qN_D}{\epsilon_{si}r} \int_0^r \exp \left(\frac{\phi(r) - V}{\phi_t} \right) r dr \quad (7.2)$$

The potential $\phi(r)$ can not be directly integrated since it is a function of the radial coordinate r . To this aim, the mobile charge approximation allows to simplify the problem: given that at the flat band condition the potential is considered constant along the nanowire radius, the mobile charge can be treated as constant and approximated as:

$$n(r) = N_D \exp \left(\frac{\phi(r) - V}{\phi_t} \right) \approx n_0 = N_D \exp \left(\frac{\phi_0 - V}{\phi_t} \right) \quad (7.3)$$

⁰adapted from [Hamzah et al. \[2019\]](#)

Thanks to this assumption, equation (7.2) can be simplified as:

$$\frac{d\phi(r)}{dr} = -\frac{qN_D}{2\epsilon_{si}}r + \int_0^r \frac{qn_0}{\epsilon_{si}}dr \quad (7.4)$$

Notice that n_0 is just a constant, thus equation (7.4) can be further integrated. Then, by multiplying both the right-hand side terms by R/R , equation (7.2) can be written as:

$$d\phi(r) = \frac{-Q_{dep} + Q_m}{R\epsilon_{si}}rdr \quad (7.5)$$

where $Q_{dep} = \frac{qN_DR}{2}$ is the depletion charge and $Q_m = \frac{qn_0R}{2}$ is the mobile charge. Substituting rdr from (7.5) into (7.2):

$$\frac{d\phi(r)}{dr} = -\frac{qN_D}{2\epsilon_{si}}r + \frac{qN_DR}{r(-Q_{dep} + Q_m)}\phi_t \exp\left(\frac{\phi_s - V}{\phi_t}\right) \left[1 - \exp\left(\frac{\phi_0 - \phi_s}{\phi_t}\right)\right] \quad (7.6)$$

One possibility to solve the problem could be the full depletion approximation, in which the potential expression is expressed like $\phi_s - \phi_0 = \frac{qN_DR^2}{4\epsilon_{si}}$ and replaced back in (7.6). This strategy is not suited for a junctionless device, since conduction already takes place in partial depletion condition. Thus an alternative method is exploited in order to obtain the potential relation, which consists in assuming a parabolic potential profile in cylindrical coordinates:

$$\phi(r) = \frac{\phi_s - \phi_0}{R^2}r^2 + \phi_0 \quad (7.7)$$

Then Gauss's law is solved at the channel interface:

$$\left.\frac{d\phi(r)}{dr}\right|_{r=R} = \frac{Q_T}{\epsilon_{si}} = \frac{-Q_{dep} + Q_m}{\epsilon_{si}} \quad (7.8)$$

thus obtaining the potential relation as:

$$\frac{\phi_s - \phi_0}{\phi_t} = \frac{-Q_{dep} + Q_m}{Q_{sc}} \quad (7.9)$$

where $Q_{sc} = \frac{2\epsilon_{si}\phi_t}{R}$ is the semiconductor charge. By replacing (7.9) back into (7.6) and considering the boundary condition $-E_s = \frac{d\phi(r)}{dr}$ at the channel interface, the surface electric field is expressed as:

$$-E_s = -\frac{qN_DR}{2\epsilon_{si}} + \frac{qN_D\phi_t}{-Q_{dep} + Q_m} \exp\left(\frac{\phi_s - V}{\phi_t}\right) \left[1 - \exp\left(-\frac{-Q_{dep} + Q_m}{Q_{sc}}\right)\right] \quad (7.10)$$

By equating (7.10) to (7.8) an expression for the surface potential is obtained:

$$\phi_s = \phi_t \ln\left(\frac{-Q_{dep} + Q_m}{Q_{dep}Q_{sc}}\right) + \phi_t \ln(Q_m) + V - \phi_t \ln\left(1 - \exp\left(-\frac{-Q_{dep} + Q_m}{Q_{sc}}\right)\right) \quad (7.11)$$

Then the Gauss law at the interface is considered, including the interface traps density of states D_{it} :

$$C_{ox}(V_g - V_{fb} - \phi_s) = -Q_{dep} + Q_{in} + qD_{it}\phi_s \quad (7.12)$$

which after rearranged gives:

$$C_{ox}(V_g - V_{fb} - \eta\phi_s) = -Q_{dep} + Q_m \quad (7.13)$$

where $\eta = 1 + \frac{qD_{it}}{C_{ox}}$ is the interface traps parameter, which is useful to model the sub-threshold degradation of the device . By inserting the surface potential expression (7.11) into (7.13) the UCCM expression is obtained:

$$V_g - V_{th} - \eta V = \frac{Q_m}{C_{ox}} + \eta\phi_t \ln\left(\frac{Q_m}{Q_{sc}}\right) - \eta\phi_t \ln\left(\frac{Q_{dep}[1 - \exp(\frac{-Q_T}{Q_{sc}})]}{Q_T}\right) \quad (7.14)$$

Where the threshold voltage is $V_{th} = V_{fb} - \frac{Q_{dep}}{C_{ox}}$ and $Q_T = -Q_{dep} + Q_m$ is the total charge. By taking the exponential of both sides of (7.14):

$$\frac{Q_m}{Q_{sc}} \exp\left(\frac{Q_m}{\eta C_{ox}\phi_t}\right) = \frac{Q_{dep}}{Q_T} \left[1 - \exp\left(\frac{-Q_T}{Q_{sc}}\right)\right] \exp\left(\frac{V_g - V_{th} - \eta V}{\eta\phi_t}\right) \quad (7.15)$$

The obtained model is piecewise continuous and so additional smoothing functions are needed to unify the various operating regions. This can cause convergence issues and increase the simulation time. Thus the model must be formulated in a non-piecewise way. To this aim, the variation of the mobile charge Q_m for the different operating regimes must be considered. In the fully depleted region ($V_g < V_{th}$) just the second term of equation (7.15) is relevant, so the total mobile charge can be simplified as:

$Q_m \approx Q_{sc} \exp(V_g - V_{th} - \eta V / \eta\phi_t)$. Under partially depleted condition ($V_{th} < V_g < V_{fb}$), the first term of (7.15) prevails so $Q_m \approx C_{eff}(V_g - V_{fb} + \frac{Q_{dep}}{C_{eff}})$, where $C_{eff} = \frac{1}{C_{ox}} + \frac{R}{2\epsilon_{si}}$ is the effective gate capacitance during partial depletion. Finally, during accumulation, the first and the third term dominate and the latter can be reduced to $(Q_m - Q_{dep})/Q_{sc}$, thus $Q_m \approx C_{ox}(V_g - V_{th})$. Based on these considerations, the total mobile charge can be decoupled into the complementary and depletion contributions ($Q_m = Q_{dp} + Q_c$), making the model continuous. Under depletion, the UCCM expression can be reduced to:

$$\frac{Q_{dp}}{Q_{sc}} \exp\left(\frac{Q_{dp}}{Q_{eff}}\right) = \exp\left(\frac{V_g - V_{th} - \eta V}{\eta\phi_t} + \frac{Q_{dep}}{Q_{sc}}\right) \quad (7.16)$$

where $Q_{eff} = Q_{sc}\eta C_{ox}\phi_t / (Q_{sc} + \eta C_{ox}\phi_t)$ is the effective charge during depletion. The solution of (7.16) can be expressed in explicit form in terms of Lambert's functions:

$$Q_{dp} = Q_{eff} LW\left(\frac{Q_{sc}}{Q_{eff}} \exp\left(\frac{V_g - V_{th} - \eta V}{\eta\phi_t} + \frac{Q_{dep}}{Q_{sc}}\right)\right) \quad (7.17)$$

Equation (7.17) well describes the current behaviour below the threshold ($V_g < V_{th}$) and in the partially depleted region ($V_{th} < V_g < V_{fb}$), but underestimates the current values

in the accumulation region ($V_g > V_{fb}$). In accumulation, equation (7.15) can be simplified to:

$$\frac{Q_c - Q_{dep}}{Q_{sc}} \exp\left(\frac{Q_c}{\eta C_c \phi_t}\right) = \exp\left(\frac{V_g - V_{fb} - \eta V}{\eta \phi_t}\right) \quad (7.18)$$

where $C_c = C_{ox} - C_{eff}$ is the corrected electrostatic control capacitance. Equation (7.18) can be further reduced to:

$$\frac{Q_c}{Q_{sc}} \exp\left(\frac{Q_c}{\eta C_c \phi_t}\right) = \exp\left(\frac{V_g - V_{fb} - \eta V}{\eta \phi_t}\right) \quad (7.19)$$

which can be solved by means of another Lambert's function:

$$Q_c = \eta C_c \phi_t LW\left(\frac{Q_{sc}}{\eta C_c \phi_t} \exp\left(\frac{V_g - V_{fb} - \eta V}{\eta \phi_t}\right)\right) \quad (7.20)$$

Q_c is the complementary part of the mobile charge, which describes the current behaviour in the accumulation region ($V_g > V_{fb}$) by acting complementary to Q_{dp} and overestimates the current values in the depletion region. Having at disposal an expression for the mobile charge Q_m , it's now possible to compute the drain current by exploiting the continuity equation:

$$I_{ds} dy = \mu(2\pi R) Q_m dV \quad (7.21)$$

By taking the logarithm equation (7.16) can be written as:

$$\frac{V_g - V_{th} - \eta V}{\eta \phi_t} + \ln\left(\exp\left(\frac{Q_{dep}}{Q_{sc}}\right) - 1\right) = \ln\left(\frac{Q_{dp}}{Q_{sc}}\right) + \frac{Q_{dp}}{\eta C_{ox} \phi_t} \quad (7.22)$$

which derivated gives:

$$\frac{dV}{dQ_{dp}} = -\phi_t \left(\frac{1}{\eta C_{ox} \phi_t} + \frac{1}{Q_{dp}} \right) \quad (7.23)$$

Similarly the logarithmic form of equation (7.18) is:

$$\frac{V_g - V_{fb} - \eta V}{\eta \phi_t} = \frac{Q_c}{\eta C_c \phi_t} + \ln\left(\frac{Q_c}{Q_{sc}}\right) \quad (7.24)$$

which derivated gives:

$$\frac{dV}{dQ_c} = -\phi_t \left(\frac{1}{\eta C_c \phi_t} + \frac{2}{Q_c} \right) \quad (7.25)$$

The decoupling of the mobile charge into the complementary and depletion contributions can be applied also for the drain current, which can be obtained by integrating the continuity equation:

$$I_{ds} = I_{dDP} + I_{dC} = \mu \frac{2\pi R}{L} \int_{Q_{dp0}}^{Q_{dpL}} Q_{dp} \frac{dV}{dQ_{dp}} dQ_{dp} + \mu \frac{2\pi R}{L} \int_{Q_{c0}}^{Q_{cL}} Q_c \frac{dV}{dQ_c} dQ_c \quad (7.26)$$

The obtained drain current expression is:

$$I_{ds} = \mu \frac{2\pi R}{L} \phi_t \left(\frac{Q_{dp}^2}{2\eta C_{ox} \phi_t} + Q_{dp} + \frac{Q_c^2}{2\eta C_c \phi_t} + 2Q_c \right) \bigg|_{Q_{dpL}, Q_{cL}}^{Q_{dp0}, Q_{c0}} \quad (7.27)$$

Where Q_{dp0} , Q_{c0} and Q_{dpL} , Q_{cL} are the depletion and complementary charges at the source and drain terminals respectively. Thanks to the decoupling of the mobile charge into the complementary and depletion part ($Q_m = Q_c + Q_{dp}$), this expression, derived by [Hamzah et al. \[2019\]](#), is continuous and independent of fitting parameters, but it predicts the current behaviour only for long channel devices. In order to adapt equation (7.27) for short channel devices, some additional effects must be taken into account, such as the velocity saturation, the channel pinch-off and the presence of the source and drain series access resistances R_s , R_d . The velocity saturation is modelled by considering an effective mobility μ_{eff} [Lime et al. \[2017\]](#):

$$\mu_{eff} = \frac{\mu}{\left(1 + \left(\frac{\mu V_{def}}{v_{sat}(L - \Delta L)} \right)^\alpha \right)^{\frac{1}{\alpha}}} \quad (7.28)$$

where $\alpha = 1$ and ΔL is the reduction of the channel due to the pinch-off effect which will be defined later. V_{def} is the effective drain voltage, defined as [Lime et al. \[2017\]](#):

$$V_{def} = V_{sat} - V_{sat} \frac{\ln \left(1 + \exp \left(A \left(1 - \frac{V_d}{V_{sat}} \right) \right) \right)}{\ln(1 + \exp(A))} \quad (7.29)$$

where A is a smoothing parameter and V_{sat} is the saturation voltage, given as [Lime et al. \[2017\]](#):

$$V_{sat} = \frac{V_s}{\frac{V_s}{V_{max}} + 1} \quad (7.30)$$

with $V_s = \frac{Q_m(0)}{C_{ox}} + \frac{V_{max}}{\frac{V_{max}}{V_{min}} - 1}$. For numerical reasons, the saturation voltage has an upper V_{max} and a lower limit V_{min} , defined as [Lime et al. \[2017\]](#):

$$V_{max} = \alpha \frac{v_{sat}}{\mu} L \quad (7.31)$$

$$V_{min} = 2\phi_t \quad (7.32)$$

For what concern the effective gate length $L_{eff} = L - \Delta L$, it models the effect of the reduction of the channel length ΔL due to the channel pinch-off, which is calculated as follows [Mukherjee et al. \[2021\]](#):

$$\Delta L = S \sqrt{\frac{\epsilon_0 \epsilon_{si} R}{2C_{ox}}} \ln \left(\frac{(V_d - V_{def}) \left(1 + \sqrt{1 + \left(\frac{2 \frac{v_{sat}}{\mu} \sqrt{\frac{\epsilon_0 \epsilon_{si} R}{2C_{ox}}}}{V_d - V_{def}} \right)^2} \right)}{2 \frac{v_{sat}}{\mu} \sqrt{\frac{\epsilon_0 \epsilon_{si} R}{2C_{ox}}}} \right) \quad (7.33)$$

Where v_{sat} is the saturation velocity and S is a parameter defined in order to make ΔL tending to zero below threshold:

$$S = \sqrt{1 - \frac{1}{1 + B \frac{Q_{dp0} + Q_{c0}}{C_{eff}\phi_t}}} \quad (7.34)$$

where B is a smoothing parameter.

Finally, to adapt the model in the limit of short channel devices, the presence of the series source and drain access resistances must be included into the equations. The series resistance can be decoupled into two contributions :

- **the nanowire resistance** R_{nw} which can be calculated as [Alothmani \[2019\]](#):

$$R_{nw} = \frac{\rho_s L_{HSQ}}{\pi r_{nw}^2} \quad (7.35)$$

where L_{HSQ} is the spacer length, r_{nw} is the nanowire's radius and ρ_s is the Silicon resistivity, given by:

$$\rho_s = \frac{1}{q\mu p} \quad (7.36)$$

where p is the holes concentration.

- **the contact resistance** R_c which can be computed with the Varahramyan model [Synopsys, Inc. \[2015\]](#):

$$R_c = R_\infty \frac{300K}{T_0} \exp\left(\frac{q\phi_b}{E_0}\right) \quad (7.37)$$

$$E_0 = E_{00} \coth\left(\frac{E_{00}}{kT_0}\right) \quad (7.38)$$

$$E_{00} = \frac{qh}{4\pi} \sqrt{\frac{|N_{D,0} - N_{A,0}|}{\epsilon_s m_t}} \quad (7.39)$$

where ϕ_b is the Schottky barrier height (given by the difference between the Silicon valence band energy and the metal workfunction), R_∞ is the Schottky resistance assuming an infinite doping concentration at the contact, T_0 is the lattice temperature and m_t is the tunneling mass.

It's now possible to write another expression of the drain current I_{ds} which takes into account of short channel effects and of the presence of the series access resistances [Mukherjee et al. \[2021\]](#):

$$I_{ds} = \frac{I_{ds,0} \eta_1 NF}{1 + 2\pi \frac{R}{L_{eff}} NF \mu_{eff} (R_s + R_d) \eta_2 [(Q_{dp0} + Q_{c0}) - \eta_3 (Q_{dp0} + Q_{c0} - (Q_{dp,VDeff} + Q_{c,VDeff}))]} \quad (7.40)$$

where I_{ds0} is the long channel drain current (7.27), NF is the number of nanowires in parallel, $Q_{dp,VDeff}$ and $Q_{c,VDeff}$ are the depletion and complementary charges computed

at the pinch of point of the channel, η_1 is a normalization factor, while η_2 and η_3 are other fitting parameters. Differently with respect to the long channel case, the model adapted to short channel devices is no more independent of fitting parameters, but is still continuous and explicit over the entire bias range, thus is suited to be included in SPICE simulators in order to simulate circuits based on this technology. Moreover it's possible to further improve the subthreshold behaviour description by including the Band-To-Band-Tunnelling(BTBT) contribution at the Schottky contacts, as done in [Mukherjee et al. \[2021\]](#), but adopting a simpler model independent of fitting parameters [Semenov et al. \[2002\]](#):

$$I_{gidl} = A_1 E_s \exp\left(\frac{-B_1}{E_s}\right) \quad (7.41)$$

where A_1 and B_1 are two constants defined as:

$$A_1 = \frac{q^2 m_r^{\frac{1}{2}}}{18\pi h^2 E_{gap}^{\frac{3}{2}}} \quad (7.42)$$

$$B_1 = \frac{\pi m_r^{\frac{1}{2}} E_{gap}^{\frac{3}{2}}}{2\sqrt{2}q\hbar} = 21.3 \text{ MV cm}^{-1} \quad (7.43)$$

where $m_r = 0.2m_0$ is the electron reduced mass, $E_{gap} \approx 3.5$ eV is the Silicon direct energy gap and E_s is the surface electric field at the gate-drain overlap point, which can be computed as:

$$E_s \approx \frac{V_{gd} - 1.2}{3t_{ox}} \quad (7.44)$$

Chapter 8

Compact model validation

8.1 Subthreshold slope investigation

The model presented in Section 7.2 is now validated against the experimental results of the junctionless transistor technology fabricated at the LAAS-CNRS, taken from [Kumar et al. \[2024\]](#). The validation is performed by considering three different diameters: **16 nm**, **27 nm**, **34 nm**. As for the TCAD part, the starting point is the investigation of the transcharacteristics at different traps densities in order to fit the experimental subthreshold slope.

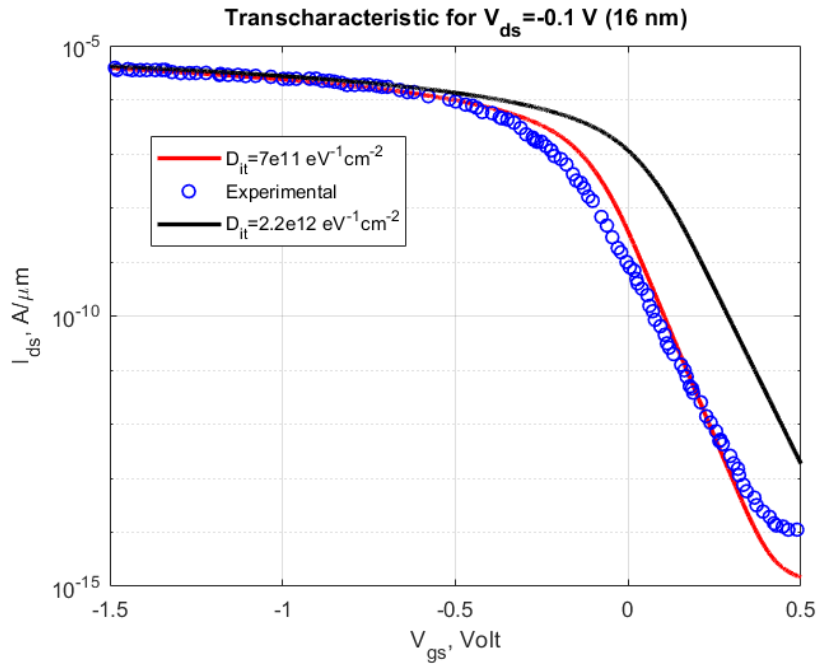


Figure 8.1: .Transcharacteristic for D=16 nm

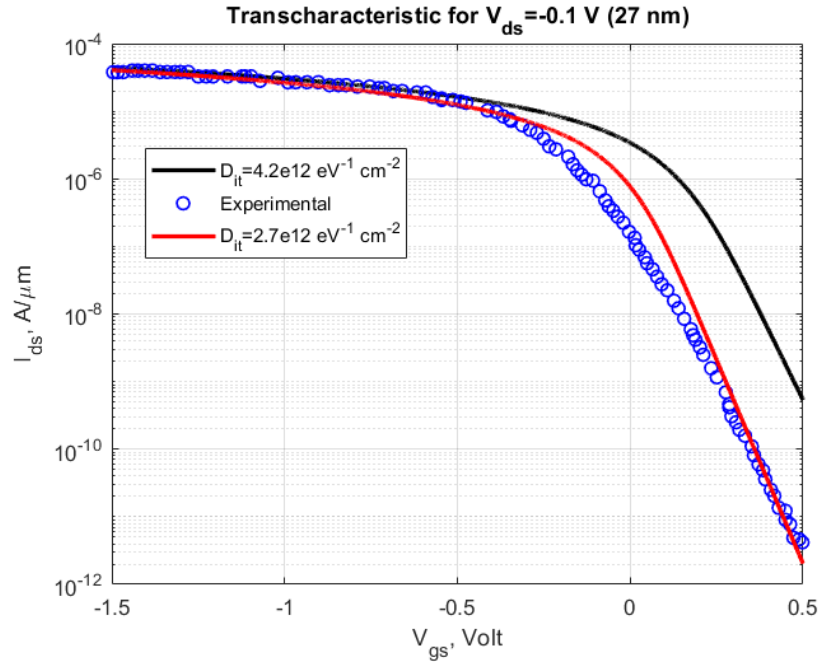


Figure 8.2: .Transcharacteristic for D=27 nm

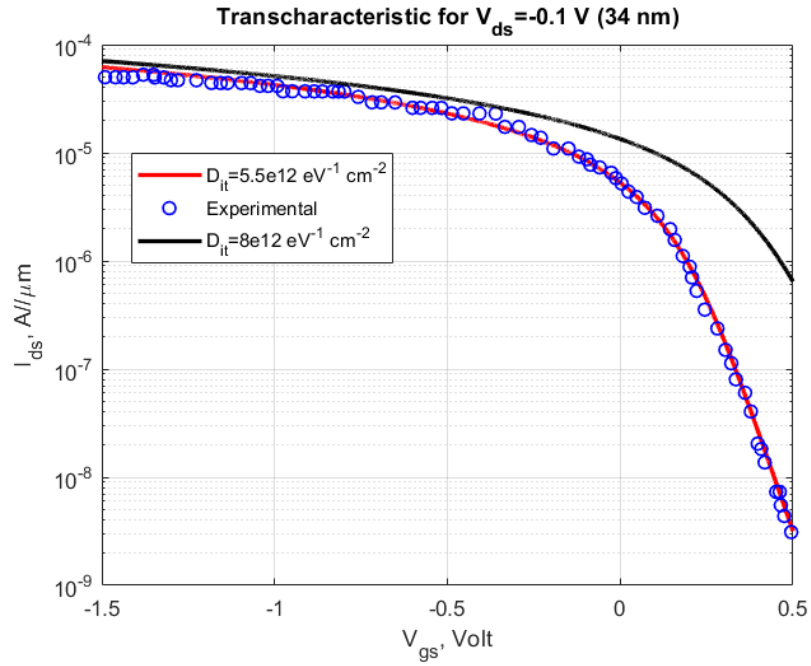


Figure 8.3: .Transcharacteristic for D=34 nm

As can be seen in the upper figures, a precise fitting of the experimental data can be obtained just for $D=34$ nm. For the other two geometries, the compact model fits quite well the measurements just in the on condition, while in the subthreshold region a slight mismatch is observed due to a different subthreshold slope. The experimental subthreshold slope can be reproduced by varying the traps density, but on the cost of a shifting of the curves along positive gate voltages. To overcome this issue, the compact model can be modified by adding a threshold voltage shift due to the interface traps Wang et al. [2023]:

$$\Delta V_{th} = \frac{\alpha q D_{it}}{C_{ox}} \quad (8.1)$$

where α is a constant. This adjustment is not needed for $D=34$ nm, since by increasing the nanowire diameter the surface to volume ratio decreases and thus the effect of interface traps becomes less relevant with respect to smaller diameters devices.

8.2 Fitting of the experimental data

Up to now the aim was just finding the correct subthreshold slope. So the fitting parameters were found by hand. In order to minimize the error between the compact model and the experimental results, a precise fitting procedure has to be exploited. To this purpose, one of the most used techniques is the so called least squares fit method. Starting from a set of data points $\{(x_i, y_i)\}$ (with $i=1,2,\dots,n$), it aims to find the vector of parameters θ in such way that the model function $f(\theta, x_i)$ fits as much as possible the set of points $\{(x_i, y_i)\}$. This is performed by minimizing the sum of the squares of the residuals in between the data y_i and the values foreseen by the model function $f(\theta, x_i)$:

$$\theta^* = \underset{\theta}{\operatorname{argmin}} \sum_{i=1}^n (y_i - f(\theta, x_i))^2 \quad (8.2)$$

In MATLAB, this task is accomplished by the function `lsqcurvefit`, whose syntax is:

$$\theta = \text{lsqcurvefit}(\text{model}, \theta_0, X_{data}, Y_{data}) \quad (8.3)$$

where *model* is the function $f(\theta, x_i)$ which aims to fit the experimental data, θ_0 is a vector containing the initial guess for the fitting parameters θ , X_{data} and Y_{data} are vectors containing the data that have to be fitted. The model function $f(\theta, x_i)$ contains the Lambert's functions which cause convergence issues in the algorithm. As a consequence, the Lambert's function has to be approximated as:

$$LW(z) \approx \ln(1+z) \left(1 - \frac{\ln(1+\ln(1+z))}{2+\ln(1+z)} \right) \quad (8.4)$$

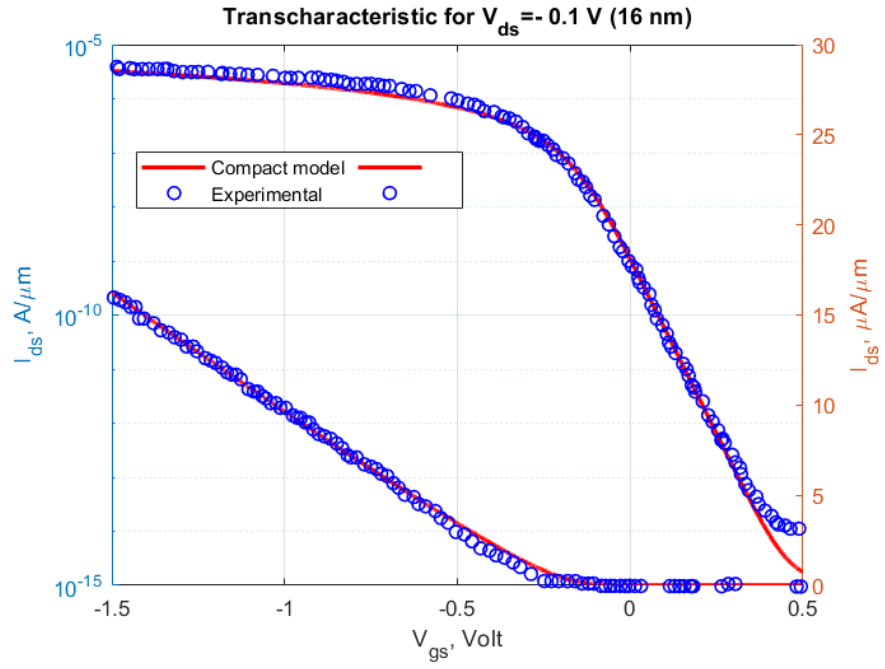


Figure 8.4: .Transcharacteristic for D=16 nm with optimized fitting parameters

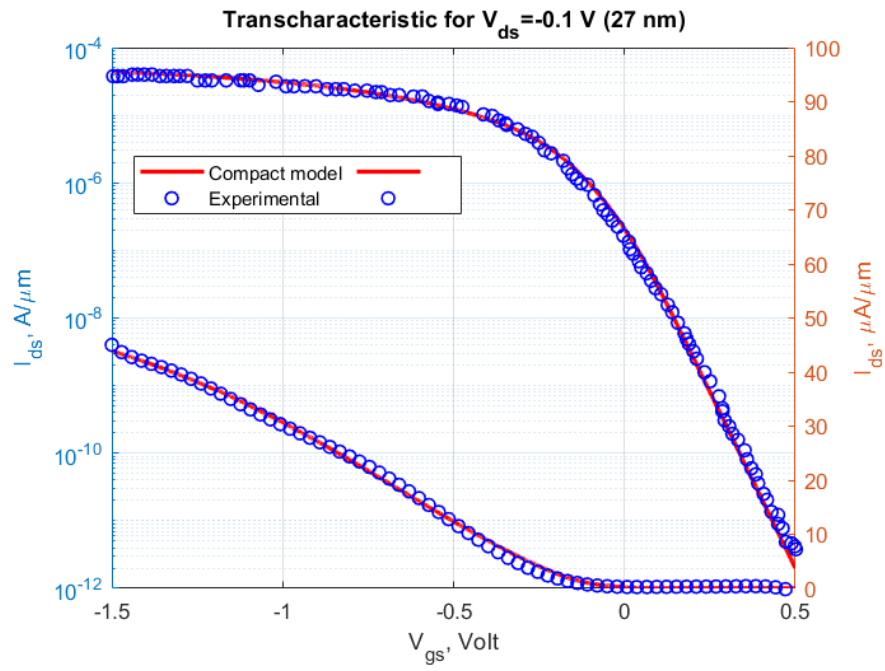


Figure 8.5: .Transcharacteristic for D=27 nm with optimized fitting parameters

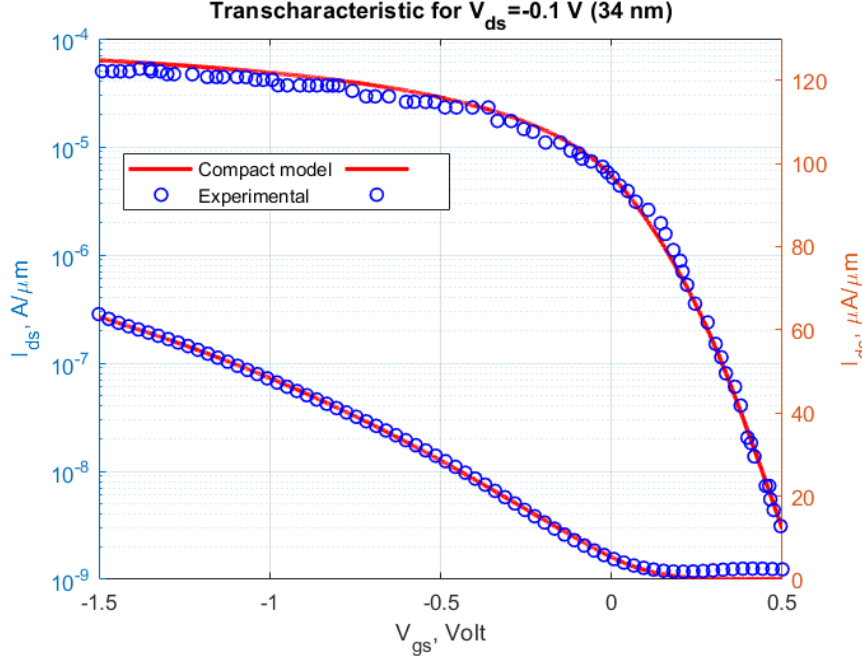


Figure 8.6: .Transcharacteristic for D=34 nm with optimized fitting parameters

According to these results, it is possible to observe that by increasing the nanowire's diameter there is an enhancement of the on current, since in the flat band condition the current flows over the entire cross section of the device and thus a larger nanowire width will result in an higher amount of carriers which contribute to the conduction. On the other hand, a larger diameter will lead to an higher off current since the transverse electric field imposed by the applied gate voltage is not able to completely deplete the channel, thus a conductive path remains allowing for a current flowing in the off condition. As a consequence, devices based on large nanowires diameters are exploited for high power applications, while for high density applications requiring high immunity against SCE small diameters devices are preferred [Kumar et al. \[2024\]](#).

To further validate the results, an analysis of the absolute and relative errors has been conducted. For all the geometries, the relative error is no more than 10%, which, as remarked in [Mukherjee et al. \[2021\]](#), is the maximum admissible error in industrial electronic. Similarly to what as been done in chapter six, also in this case the relative error has been computed by taking the maximum between the compact model current and its average over the bias range.

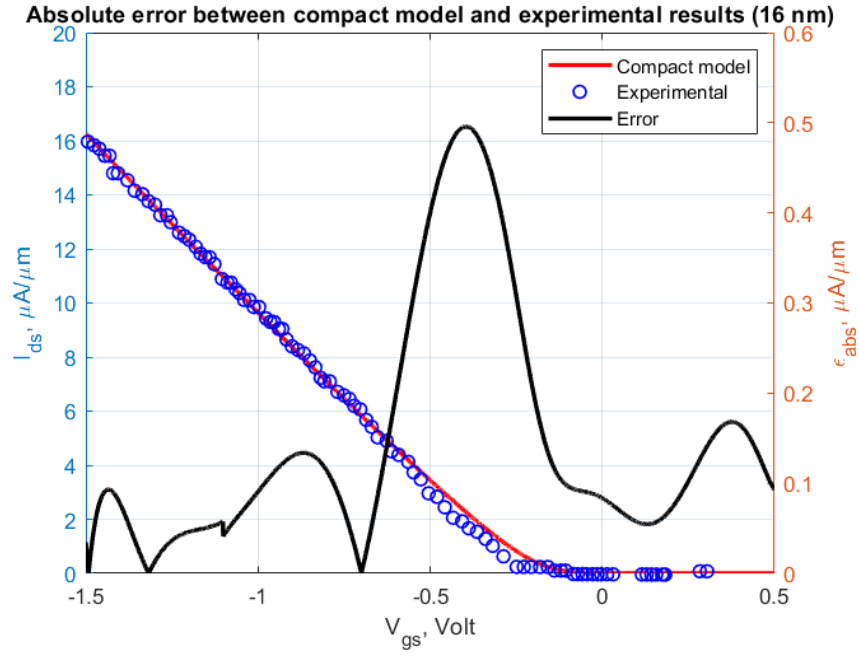


Figure 8.7: .Absolute error in between the compact model and the experimental results for $D=16$ nm

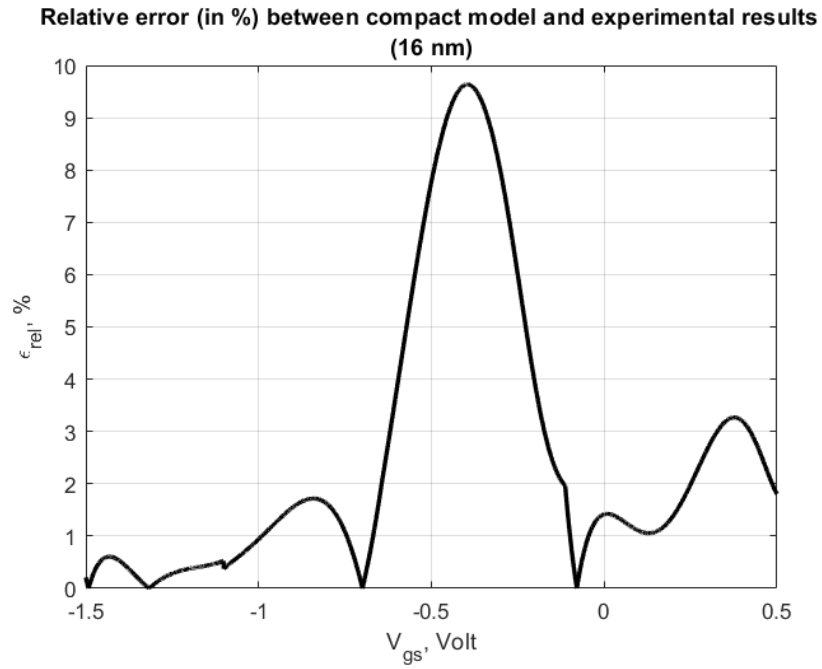


Figure 8.8: .Relative error in between the compact model and the experimental results for $D=16$ nm

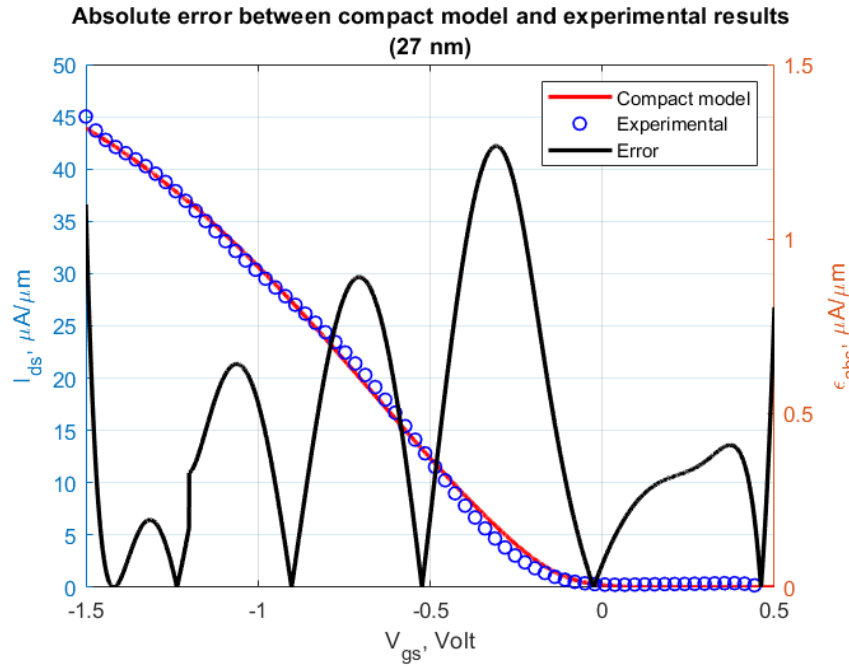


Figure 8.9: .Absolute error in between the compact model and the experimental results for D=27 nm

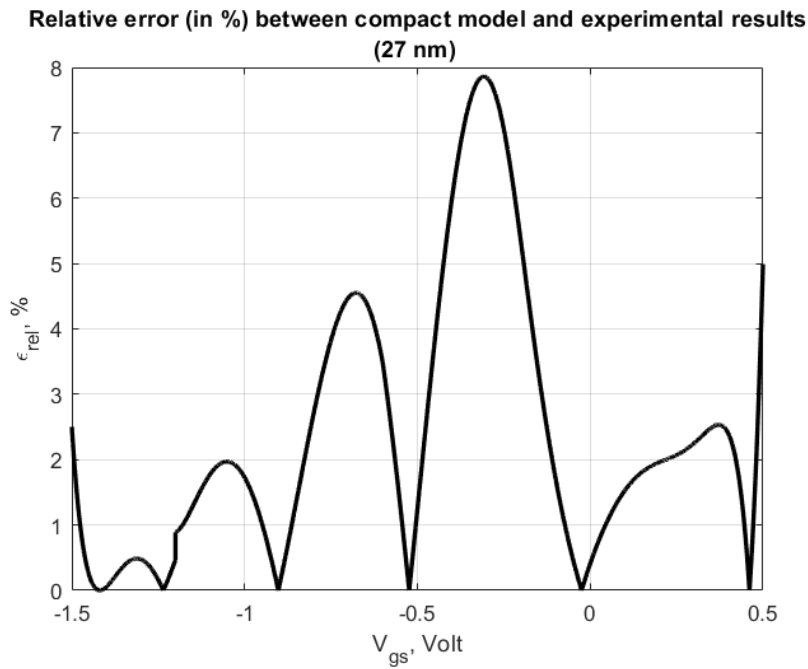


Figure 8.10: .Relative error in between the compact model and the experimental results for D=27 nm

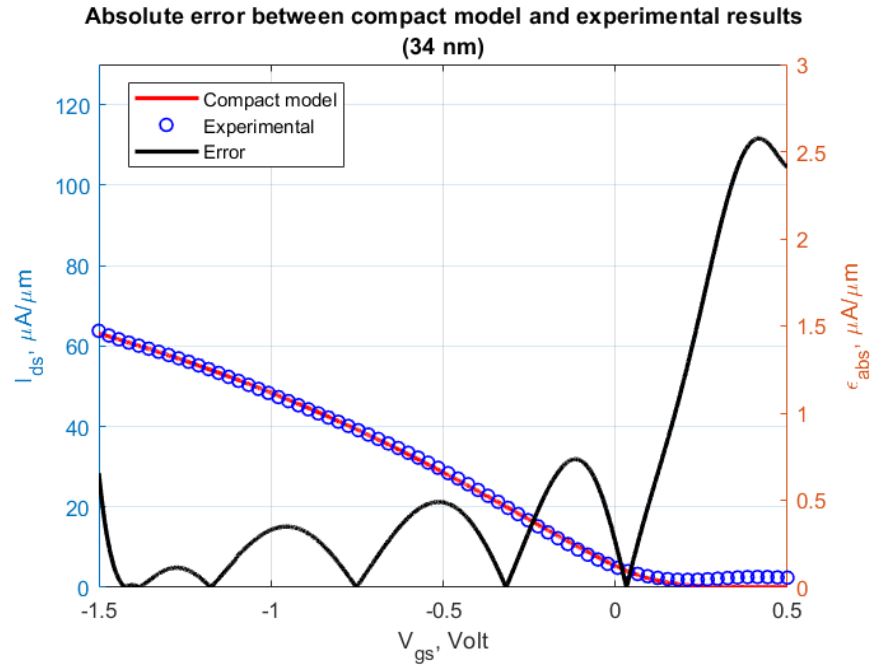


Figure 8.11: .Absolute error in between the compact model and the experimental results for $D=34$ nm

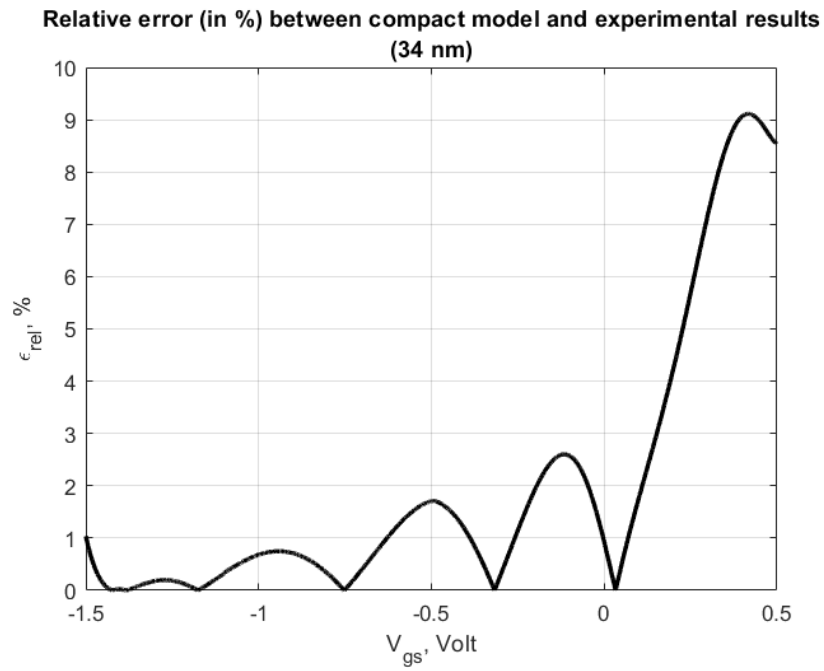


Figure 8.12: .Relative error in between the compact model and the experimental results for $D=34$ nm

As can be seen from the upper figures, apart from a peak of the error in the off condition for the 34 nm case which is just attributed to some troubles in extracting the experimental data with the MATLAB Grabit function, in all the other cases the peak of the error lies just after the threshold voltage, at the onset of the on condition. This is a clear sign of the fact that there is some aspect of the device conduction which is not correctly caught by the compact model. In the real device, one possible source of variability is the Schottky barrier height, which could locally vary due to the inhomogeneity of the metal/semiconductor junction surface morphology [Han et al. \[2012\]](#). To compensate for this variability source, differently to what has been done in [Mukherjee et al. \[2021\]](#), an additional fitting parameter multiplying the series access resistances has been introduced in the short channel expression of the drain current (Eq. 7.40).

Chapter 9

Matching the compact model with the Sentaurus results

9.1 Mobility and Doping extraction

In the previous chapter the compact model has been validated against the experimental results. Now, the goal is to optimize the model so as to obtain an acceptable matching with the results of the simulations illustrated in chapter 6. In order to perform this task some parameter has to be properly optimized. In particular, previously the doping concentration was assumed to be equal to the starting wafer concentration (i.e. $N_A = 3.5 \times 10^{19} \text{ cm}^{-3}$) and the mobility was taken from [Caughey and Thomas \[1967\]](#). However, as previously highlighted, the resulting doping concentration at the end of the oxidation process is not the same as the one of the starting wafer, due to the Boron segregation into the oxide layer. This has also an impact on the carriers mobility since one of the main contribution to the carriers mobility degradation is the impurity scattering, which depends on the dopants concentration in the active region of the device. As a consequence, to obtain a good fit of the Sentaurus results, the doping concentration and the mobility values to be inserted in the compact model must be extracted from the simulation results. To do this, an average of the two quantities along the vertical direction is considered since, as shown in Fig.(9.1.a) and (9.1.b), along the nanowire cross section the profile is more or less constant. The parameters of the simulation whose results are taken as a target for the fitting procedure are summarized in table 9.1. As explained in chapter 6, even though the interface traps of donor type give rise to an almost perfect fit of the experimental data in logarithmic scale, they deeply underestimate the on current in linear scale. So in order to have a good starting point and simplify the fitting procedure, acceptor type interface states are considered.

Cr workfunction	PtSi workfunction	Traps type	Concentration	E_T	σ_T
4.35 eV	5.0 eV	Acceptor	$5.0 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$	-0.3 eV	0.2 eV

Table 9.1: Parameters of the simulation to be fitted

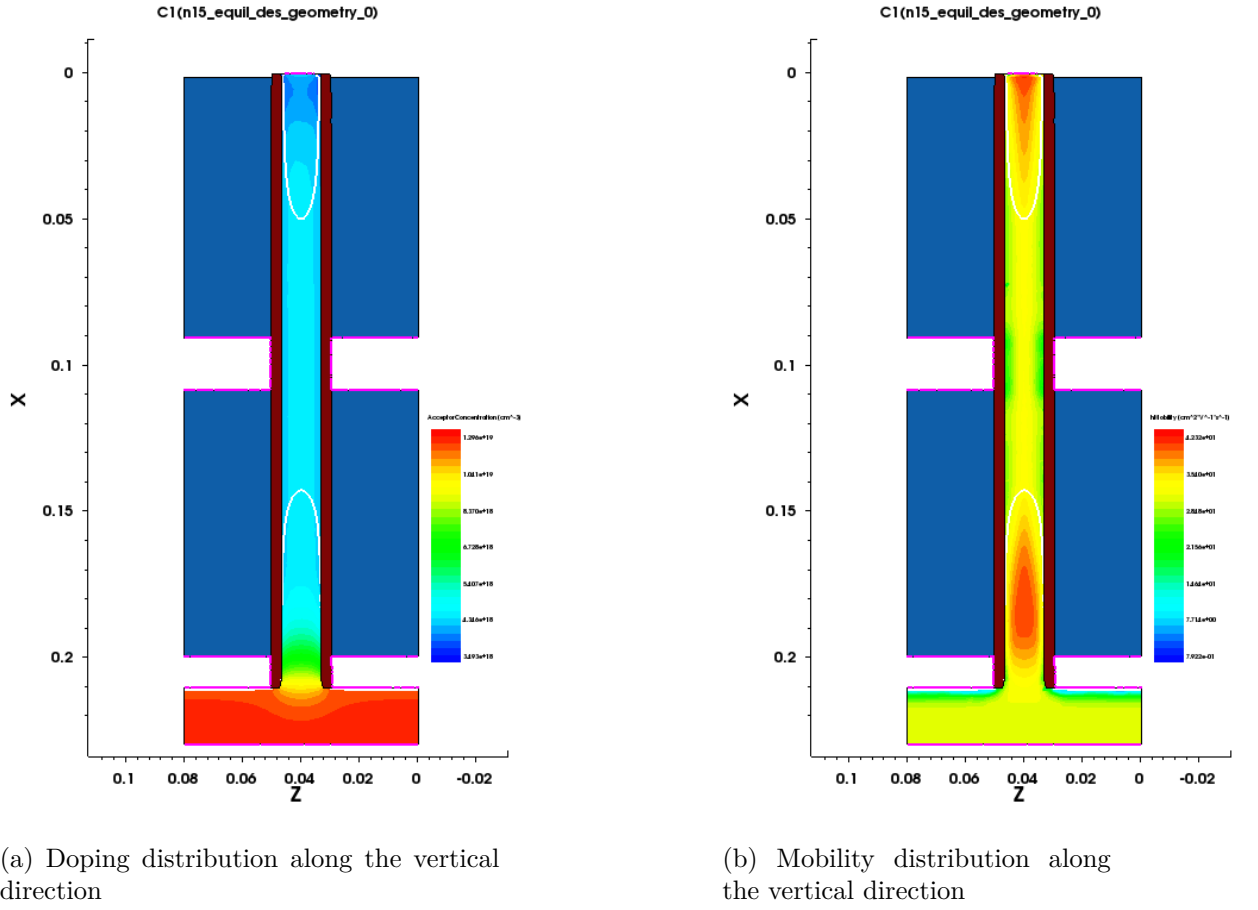


Figure 9.1: Mobility and doping distributions along the vertical direction

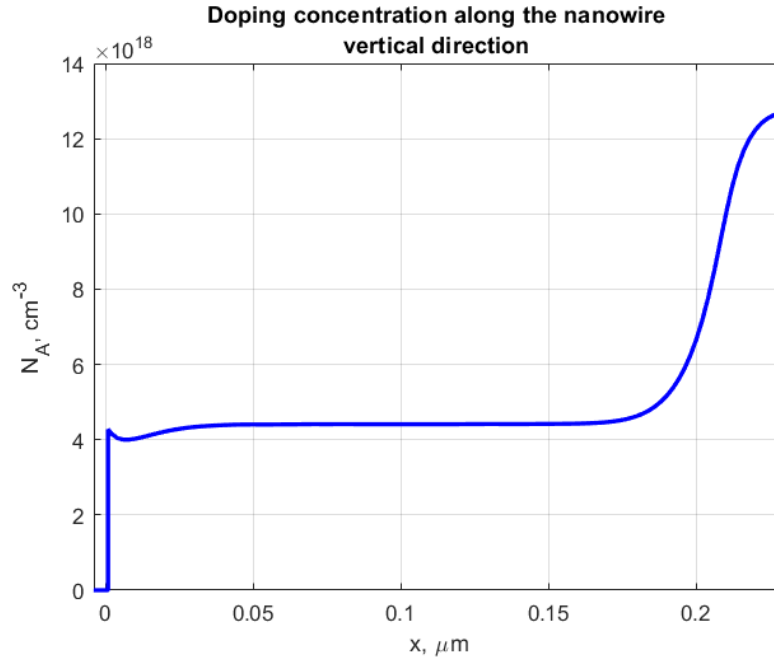


Figure 9.2: .Doping concentration along the vertical direction

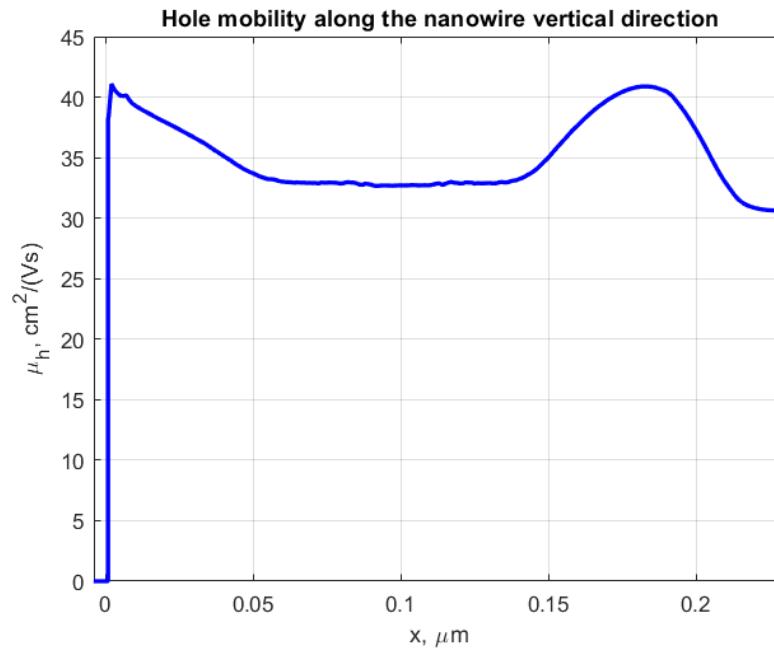


Figure 9.3: .Mobility along the vertical direction

The resulting doping and mobility values obtained by averaging the afore illustrated distributions are respectively $N_A = 3.78 \times 10^{18} \text{ cm}^{-3}$ and $\mu_h = 32.55 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.

9.2 Fitting of the Sentaurus results

After inserting the obtained average values for the mobility and the doping concentration in the compact model, the least squares procedure is adopted in order to find the optimized fitting parameters which reduce as much as possible the error in between the model and the Sentaurus results. The following results are obtained:

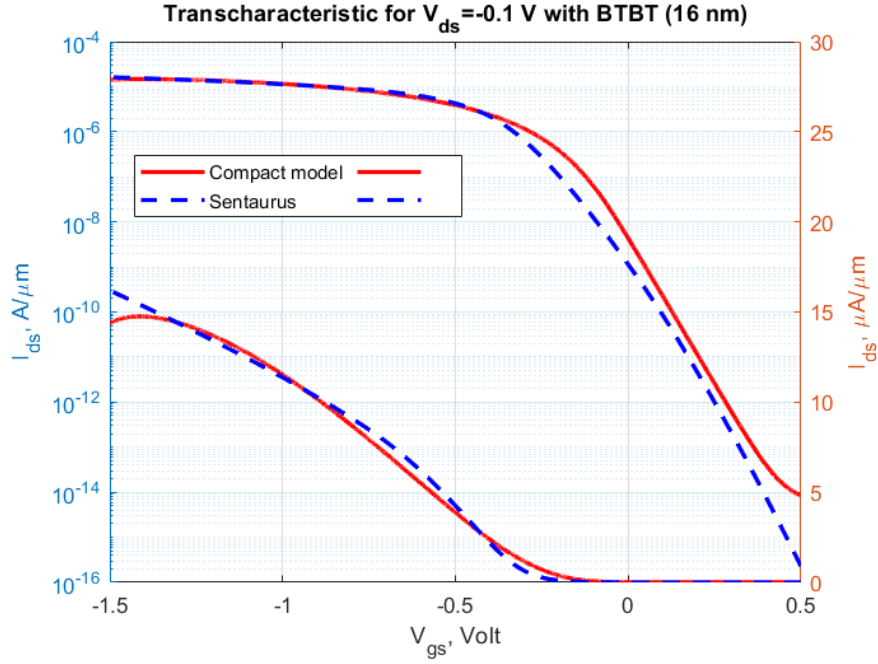


Figure 9.4: Matching of the Sentaurus results with the compact model, with BTBT included in the compact model

As can be seen from the upper figure, the compact model off current is higher with respect to the one obtained in the Sentaurus simulation. This could be attributed to the fact that the compact model takes into account of the BTBT contribution, while in the device simulated by Sentaurus this phenomena is not relevant, as explained in chapter 6. Thus in order to have a better fit, the compact model must be modified, delating the BTBT contribution to the off current.

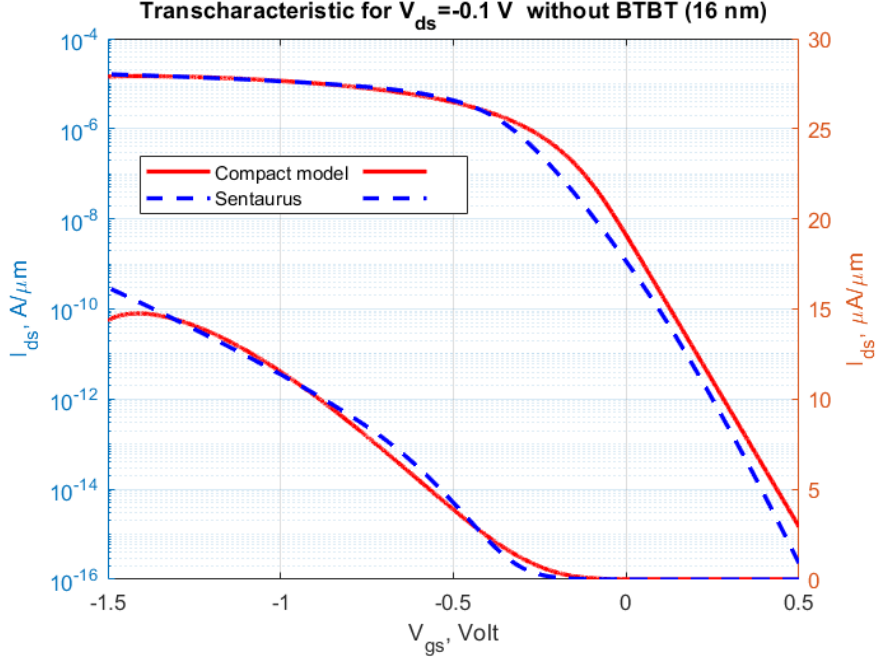


Figure 9.5: Matching of the Sentaurus results with the compact model, without BTBT included in the compact model

As can be caught from the upper figure, a slight mismatch of the transcharacteristics in logarithmic scale is still present. This could be attributed to the fact that the traps concentration adopted in the compact model ($N_0 = 2.2 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$) is not the same as the one of the Sentaurus simulation ($N_0 = 5.0 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$). Infact, for $N_0 = 5.0 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$, the SS of the compact model increases too much leading to an off current much higher with respect to the one obtained in the Sentaurus simulation. The reason behind this is that two different models for the interface traps DOS are adopted in the two cases. As previously explained, in the Sentaurus simulations the interface traps DOS are modelled according to a Gaussian distribution, while in the compact model a single energy level distribution is considered. However, this does not impact too much on the absolute and relative errors :

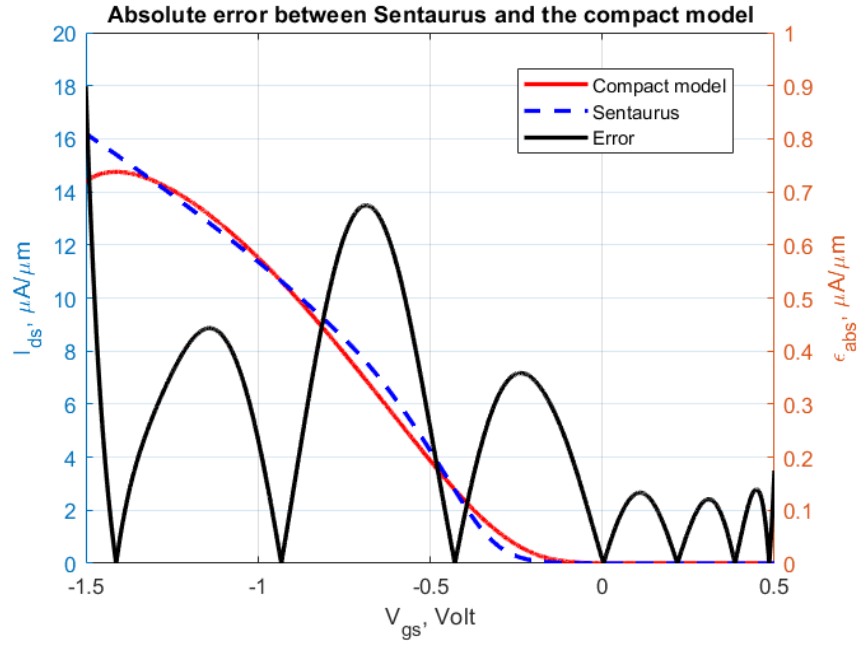


Figure 9.6: .Absolute error between the Sentaurus results and the compact model

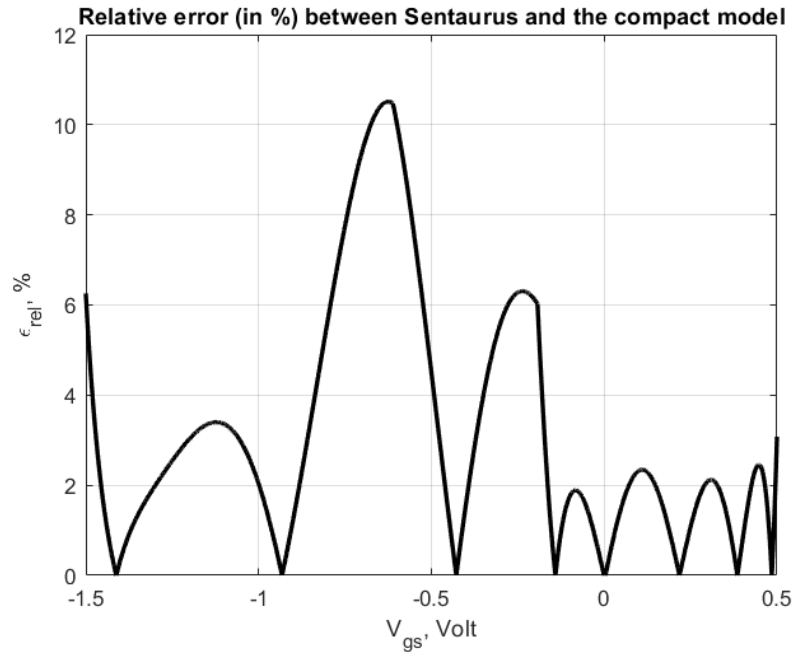


Figure 9.7: .Relative error between the Sentaurus results and the compact model

According to the upper figures, the relative error is relatively low for almost all the

bias range under study and it just slightly exceeds the 10% threshold around -0.7 V, since around that region the current obtained by the Sentaurus simulation is a little bit higher than the one obtained by the compact model. The reason behind this could be related to the fact that Sdevice, differently with respect to the compact model, takes into account of the nature of the interface traps, which are of acceptor type. This kind of traps, if their energy level is located below the Fermi level, can stole electrons from the semiconductor conduction band. In a p type semiconductor this is beneficial from the current capability point of view, since it results in a decrease of the amount of electrons which can recombine with holes in the valence band, thus increasing the amount of majority carriers which contribute to the conduction. However, this effect is counterbalanced by the fact that the simulations performed by Sentaurus include the incomplete ionization effect, neglected by the compact model. Thus overall the two currents are quite similar.

Chapter 10

Conclusions and Future perspectives

In this work, the fabrication process of a vertical GAA junctionless FET has been simulated by Synopsys Sentaurus, showing that, by properly tuning some parameters (especially the workfunctions and the amount and type of interface traps) it's possible to obtain a good fit of the experimental results. An almost perfect fit of the experimental data in logarithmic scale is obtained by including the effect of donor type interface traps. However, as previously explained, this kind of traps leads to an abrupt depletion of carriers in a p type nanowire device. Thus, in order to obtain an acceptable error, it is necessary to include acceptor type interface traps which, even though lead to a slight mismatch in logarithmic scale, however allow to obtain a better fit in linear one, with a maximum relative error of 27.15% . This is a good results, considering that in [Rossi et al. \[2023\]](#), in which is simulated the same device but with a different nanowire diameter, the maximum error is about 57.18% (notice that this error could be slightly overestimated due to the intrinsic inaccuracy of the MATLAB Grabit function) . Then, in the second part of the project, the MATLAB implementation of an analytical compact model inherited from literature has been validated against the experimental data and the results of the electrical simulations obtained in the first part, obtaining in the first case a very good match, given that the relative errors do not exceed 10%, which is the threshold under which a result is considered reliable and suited to be exploited in commercial electronics. The model has been a little bit changed with respect to the one presented in [Mukherjee et al. \[2021\]](#). In fact, as previously explained, an additional fitting parameter has been introduced in order to correct the effect of the inhomogeneity of the Schottky contacts interfaces. However, to compensate for the introduction of this additional parameter which slightly increases the computational cost, a model for the BTBT independent of fitting parameters has been adopted.

There could be some improvements and/or developments that could be done in future works:

- it could be of interest to integrate a **ferroelectric** material in the gate stack. Infact, ferroelectric materials are gaining increasingly more interest at research level, owing

to their non volatile information storage capabilities and negative capacitance, which allows to undergo the SS limit of 60 mV/dec. However, it is very complex to integrate these materials in the Synopsys Sentaurus software, since their polarization/field hysteresis loop gives rise to a lot of convergence issues. Thus it is necessary to carefully tailor the mesh and the convergence criteria of the Newton's loop.

- as mentioned in chapter 4, when dealing with devices in the nanometers regime, the phonon spectrum undergoes a modification due to the confinement effects which results in an increase of the electron-phonon scattering rate and thus in a lowering of the mobility. Given that the mobility models available in Synopsys Sentaurus can not take into account of this effect, it could be useful to compute the mobility using an alternative approach, based on a rigorous calculation of the electron-phonon scattering rate. To this aim, one possibility could be integrating a **Monte Carlo** solver in the Sentaurus framework.
- as mentioned in chapter 3, within the first step of the DTCO loop it is possible to perform the Parasitic-Network-Extraction(**PEX**), which consists in extracting some parameters, such as the parasitic capacitances and resistances, which are useful to perform circuit based simulations in the second and third steps of the loop. To this aim, an alternated frequency analysis could be conducted with the Sdevice tool.
- as explained in the introduction of chapter 7, the analytical compact model could be integrated in a **SPICE** simulator or in a **VerylogA** code so as to conduct studies on the reliability of the device at circuit level and, based on the simulation results, optimize the process and/or the device structure so as to guarantee the correct functioning of the device in a complex analog or digital circuit. To this regard, some hint can be found in [Mukherjee et al. \[2021\]](#) and [O'Connor et al. \[2024\]](#).
- another possible hint for future works could be optimizing the device mesh so as to perform an **oxidation process** of the same temperature and for the same amount of time as the one performed at experimental level. Doing so, the resulting Boron distribution in the nanowire at the end of the oxidation process could more faithfully reproduce the one obtained at experimental level, thus helping to reduce a little bit the relative error between the results of the Sentaurus simulations and the experimental data. Moreover, increasing the oxidation time, more abrupt doping gradients could arise within the device thus increasing the overlap between the valence and the conduction band. As a consequence, the tunnelling width could reach an order of magnitude such that the BTBT phenomena starts to take place, and this could allow for a better fit of the off current in logarithmic scale .

Chapter 11

Appendix

11.1 Sentaurus scripts

11.1.1 SProcess

```
math numThreads=6
math coord.ucs
line x location=0.0<nm> spacing=2<nm>
line x location=230<nm> spacing=2<nm>
line y location=0.0<nm> spacing=2<nm>
line y location=80<nm> spacing=2<nm>
line z location=0.0<nm> spacing=2<nm>
line z location=80<nm> spacing=2<nm>
region Silicon
init concentration=3.5e+19<cm-3> field=Boron !DelayFullD
grid set.min.normal.size=0.5<nm> set.normal.growth.ratio.3d=1.5
mgoals accuracy=1e-4
AdvancedCalibration
diffuse temperature=800<C> time=40.0<s>
sde on
sde external {
(sdegeo:create-cylinder (position 0 0.040 0.040) (position -0.002 0.040
0.040) 0.008 "Photoresist" "Cover")
}
polyhedron name=cylinder external.sde
insert polyhedron= cylinder
sde off
etch material= Silicon type=anisotropic time=1 rate= 0.210
strip Photoresist
diffuse temperature=850<C> time=30<s> O2
diffuse temperature=850<C> time=30<s> O2
diffuse temperature=850<C> time=30<s> O2
```

```

diffuse temperature=850<C> time=30<s> O2
diffuse temperature=950<C> time=30<s> O2
diffuse temperature=950<C> time=30<s> O2
etch material= Oxide type=anisotropic time=1 rate= {0.003}
sde on
sde external { (sdegeo:create-cylinder (position 0.00083193347597 0.040 0.040) (position
-0.009168066524 0.040 0.040) 0.012 "Platinum" "Silicide")
}
polyhedron name=cylinder external.sde
insert polyhedron= cylinder
sde off
deposit material= Platinum type=fill coord=0.200
mater add name=HSQ new.like=oxide
mater add name=Cromium new.like=Platinum
deposit material= {HSQ} type=fill coord=0.109
deposit material= {Cromium} type=fill coord=0.091
deposit material= {HSQ} type=fill coord=0.00196641534006 refinebox min= {0.0 0.030767780351
0.031585837216} max= {0.230
0.0471593080905 0.0495657880218} xrefine= {0.001}
yrefine= {0.001}
zrefine= {0.001} add
grid remesh
contact bottom name = substrate Silicon
contact name =drain x=-0.00451334953147 y=0.0400304759952 z =0.0399672213352
Platinum
contact name =gate x=0.100484673491 y =0.0215496834083 z=0.0618647441641
Cromium
contact name =source x=0.205234696624 y =0.0635784876074 z =0.0196420205515
Platinum
struct tdr=n@node@_contatto;

```

11.1.2 SDevice

```

File
{
*INPUT FILES
Grid ="n11_contatto_fps.tdr"
* physical parameters
Parameter = "sdevice.par"
*OUTPUT FILES
Plot = "n@node@_GAA_des.tdr"
* electrical characteristics at the electrodes
Current= "n@node@_GAA_des.plt"
}

```



```

    Electrode
{
{ name="source" Voltage=0.0 Workfunction=5.0}
{ name="drain" Voltage=0.0 Workfunction=5.0}
{ name="gate" Voltage=0.5 Workfunction=4.35}
{ name="substrate" Voltage=0.0}
}

    Thermode
{
{ Name = "source" Temperature = 300 }
{ Name = "drain" Temperature = 300 }
{ Name = "gate" Temperature = 300 }
{ Name = "substrate" Temperature = 300 }
}

    Physics {
eQuantumPotential(density)
hQuantumPotential(density)
Noise(Doping(Mobility))
Mobility(Enormal(IALMob),HighFieldSaturation)
EffectiveIntrinsicDensity(OldSlotboom)
Recombination(SRH)
IncompleteIonization
Recombination(Band2Band)

    }

    Physics(MaterialInterface="Silicon/Oxide") {
Traps(
Acceptor Gaussian fromMidBandGap Conc=5.0e+12
EnergyMid=-0.3 EnergySig=0.2
eXsection=1e-14 hXsection=1e-14
)
}
Physics(Material="Silicon") {

    Mobility(DopingDependence)

    Plot
{
Potential ElectricField/Vector
eEparallel eEnormal

```

```

hEparallel hEnormal
eDensity hDensity SpaceCharge
Affinity IntrinsicDensity
eCurrent/Vector hCurrent/Vector TotalCurrentDensity/Vector
eMobility hMobility eVelocity hVelocity
Doping DonorConcentration AcceptorConcentration
DonorPlusConcentration AccepMinusConcentration
ConductionBandEnergy ValenceBandEneergy
eQuasiFermiEnergy hQuasiFermiEnergy
eGradQuasiFermi/Vector hGradQuasiFermi/Vector
eAvalancheGeneration hAvalancheGeneration
BandGap DielectricConstant
BandGapNarrowing
ConductionBand ValenceBand
BarrierTunneling hBarrierTunneling * BarrierTunneling
eTrappedCharge hTrappedCharge
eDirectTunnel hDirectTunnel
eQDDGamma hQDDGamma
}

```

```

    Math
{
Extrapolate
* use full derivatives in Newton method
Derivatives
* control on relative errors
RelErrControl
* relative error= 10-Digits
Digits=3
maximum number of iteration at each step
Iterations=100
ExitOnFailure
ExtendedPrecision
-CheckUndefinedModels
Number_Of_Threads= 4
}

```

```

    Solve
{
initial equilibrium solution
Poisson
Coupled (Iterations= 100 LineSearchDamping= 1e-4){ Poisson
hQuantumPotential}
Plot(FilePrefix="n@node@_equil")
}

```

```

    NewCurrentPrefix = "IDVD_VD1"
    quasistationary (InitialStep= 1e-3 MinStep= 1e-6 MaxStep= 0.010
    Goal {name= "drain" voltage = -0.1})
    {coupled { Poisson Hole hQuantumPotential}
    CurrentPlot ( Time = (range = (0 1) intervals = 100))
    Plot(FilePrefix = "IDVD_VD1" Time=(1.0))}

    NewCurrentPrefix = "IDVG_VD1"
    quasistationary (InitialStep= 1e-4 MinStep= 1e-6 MaxStep= 0.010
    Goal {name= "gate" voltage = -1.5})
    {coupled Poisson Hole hQuantumPotential }
    CurrentPlot ( Time = (range = (0 1) intervals = 100))
    Plot(FilePrefix = "IDVG_VD1" Time=(1))}

}

```

MATLAB scripts

```

function [Itot]=draincurrent(x,Vg)
q = 1.6e-19;
Na =3.5e19* 1e6; %doping concentration
R = 8e-9; % nanowire radius
epsox = 3.9; % SiO2 dielectric constant
Vt = 0.025875; % thermal voltage
Vth =0.1013; % threshold voltage
Vd =-0.1; % drain voltage
L = 18e-9; % gate length
tox = 4e-9; %oxide thickness
eps0 = 8.854e-12; % vacuum permittivity
epssi = 11.7; % Si dielectric constant
NF=1; % number of nanowires in parallel
Cox=epsox*eps0/(R*log(1+(tox/R))); % gate oxide capacitance
%other parameters
alpha = 1;
vsat = 6e6 / 100; %saturation velocity
mu = 50/ 1e4; %mobility
Vfb = -1.16; %flat-band voltage
T = 300; %temperature
Dit = (22e11/1.12)*1e4; % interface traps dos;
n = 1 + ((Dit .* q) ./ Cox); %interface traps parameter
Qdep = (q * Na * R) / 2; %depletion charge
Qsc = (2 * epssi * Vt) / R; %semiconductor charge
Qeff = (Qsc * n * Cox * Vt) / (Qsc + n * Cox * Vt); % effective charge during depletion

```

```

Ceff = (1 / Cox) + (R / (2 * epssi * eps0)); %effective capacitance during partial depletion
Cc = Cox - Ceff; %corrected electrostatic control
Vmax = alpha * L * (vsat / mu);
Vmin = 2 * Vt;

```

```

% vectors initialization
Qdp0 = zeros(1, 10000);
Qc0 = zeros(1, 10000);
Vs = zeros(1,10000);
Vsat = zeros(1,10000);
Vdeff = zeros(1,10000);
S = zeros(1,10000);
argradice = zeros(1,10000);
DeltaL = zeros(1,10000);
Leff = zeros(1,10000);
mueff = zeros(1,10000);
QdpL = zeros(1, 10000);
QcL = zeros(1,10000);
Id0 = zeros(1,10000);
zdp0=zeros(1,10000);
zc0=zeros(1,10000);
zdpL=zeros(1,10000);
zcL=zeros(1,10000);
zdpdeff=zeros(1,10000);
zcdeff=zeros(1,10000);
Ids=zeros(1,10000);
Vgd=zeros(1,10000);
Es=zeros(1,10000);
Igidl=zeros(1,10000);
Itot=zeros(1,10000);
epsilon = 1e-20;

```

```

% cycle over Vg
for i = 1:10000
% depletion charge at the beginning of the channel
zdp0(i) = (Qsc / Qeff) * exp(((Vg(i) - Vth) / (n * Vt)) + (Qdep / Qsc));

```

```

    if zdp0(i) < epsilon
zdp0(i) = epsilon; % to avoid small values
end

```

```

    Qdp0(i) = Qeff * log(1+zdp0(i))*(1-((log(1+log(1+zdp0(i))))/(2+log(1+zdp0(i)))));

```

```

% complementary charge at the beginning of the channel
zc0(i) = (Qsc / (n * Cc * Vt)) * exp((Vg(i) - Vfb) / (n * Vt));

```

```

    if zc0(i) < epsilon
zc0(i) = epsilon;
end

    Qc0(i) = n * Cc * Vt * log(1+zc0(i))*(1-((log(1+log(1+zc0(i))))/(2+log(1+zc0(i)))));

    if Vg(i)<Vfb
Qc0(i)=0;
end

    Vs(i) = ((Qdp0(i) + Qc0(i)) / Cox) + (Vmax / ((Vmax / Vmin) - 1));
Vsat(i) = Vs(i) / ((Vs(i) / Vmax) + 1);%saturation voltage

    %effective drain voltage
if Vsat(i) > 0
Vdeff(i) = Vsat(i) - Vsat(i) * (log(1 + exp(x(1) * (1 - (Vd / Vsat(i)))))) / log(1 + exp(x(1))));
else
Vdeff(i) = 0;
end

    S(i) = sqrt(1 - (1 / (1 + x(2) * ((Qc0(i) + Qdp0(i)) / (Ceff * Vt)))));
argradice(i) = 1 + ((2 * (vsat / mu) * sqrt((eps0 * epssi * R) / (2 * Cox))) / (Vd - Vdeff(i)))^2;
DeltaL(i) = S(i) * sqrt((eps0 * epssi * R) / (2 * Cox)) * log(((Vd - Vdeff(i)) * (1 + sqrt(argradice(i)))) / (2 * (vsat / mu) * sqrt((eps0 * epssi * R) / (2 * Cox))));
Leff(i) = L - DeltaL(i);%effective gate length due to the channel pinch off
mueff(i) = mu / (1 + ((mu * Vdeff(i)) / (vsat * Leff(i)))alpha)(1/alpha); %effective mobility

    %depletion charge at the end of the channel
zdpL(i) = (Qsc / Qeff) * exp(((Vg(i) - Vth - n * Vd) / (n * Vt)) + (Qdep / Qsc));
    if zdpL(i) < epsilon
zdpL(i) = epsilon;
end
QdpL(i) = Qeff * log(1+zdpL(i))*(1-((log(1+log(1+zdpL(i))))/(2+log(1+zdpL(i)))));

    %complementary charge at the end of the channel
zcL(i) = (Qsc / (n * Cc * Vt)) * exp((Vg(i) - Vfb - n * Vd) / (n * Vt));

    if zcL(i) < epsilon
zcL(i) = epsilon;
end
QcL(i) = n * Cc * Vt * log(1+zcL(i))*(1-((log(1+log(1+zcL(i))))/(2+log(1+zcL(i)))));
if Vg(i)<Vfb

```

```

QcL(i)=0;
end

%long channel drain current expression
Id0(i) = mueff(i) * ((2 * pi * R) / Leff(i)) * Vt * ((Qdp0(i)^2/(2 * n * Cox * Vt)) +
Qdp0(i) + (Qc0(i)^2/(2 * n * Cc * Vt)) + 2 * Qc0(i) - (QdpL(i)^2/(2 * n * Cox * Vt)) -
QdpL(i) - (QcL(i)^2/(2 * n * Cc * Vt)) - 2 * QcL(i));

zdpdeff(i) = (Qsc / Qeff) * exp(((Vg(i) - Vth - n * Vdeff(i)) / (n * Vt)) + (Qdep /
Qsc));
if zdpdeff(i) < epsilon
zdpdeff(i) = epsilon;
end
Qdpdeff(i) = Qeff * log(1+zdpdeff(i)) * (1-((log(1+log(1+zdpdeff(i))))/(2+log(1+zdpdeff(i)))));

zcdeff(i) = (Qsc / (n * Cc * Vt)) * exp((Vg(i) - Vfb - n * Vdeff(i)) / (n * Vt));
if zcdeff(i) < epsilon
zcdeff(i) = epsilon;
end
Qcdeff(i) = n * Cc * Vt * log(1+zcdeff(i)) * (1-((log(1+log(1+zcdeff(i))))/(2+log(1+zcdeff(i)))));
if Vg(i)<Vfb
Qcdeff(i)=0;
end

%short channel expression
Ids(i)=Id0(i)*NF./(1+2*pi*(R/Leff(i))*NF*mueff(i)*32332*x(3)*
((Qdp0(i)+Qc0(i))-x(4)*(Qdp0(i)+Qc0(i)-(Qdpdeff(i)+Qcdeff(i)))));

%gidl
Vgd(i)=Vg(i)-Vd;
Es(i)=(Vgd(i)-1.2)/(3*tox);
Bgidl=21.3*1e8;
h=4.136e-15;
mo=9.1093837015e-31;
mr=0.2*mo;
Egap=3.5;
Agidl=((q^2) * (mr^0.5))/(18 * 3.14 * (h^2) * (Egap^1.5));
Igidl(i) = Agidl * Es(i) * exp(-Bgidl/Es(i));
if Vg(i) < Vth
Itot(i) = Igidl(i) + Ids(i);
else
Itot(i) = Ids(i);
end
end

```

```
Itot=flipr(abs(Itot)*1e6);
```

```
end
```

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