POLITECNICO DI TORINO

Master's Degree in Electronic Engineering

Master's Degree Thesis

Optimization of contact metallization for cryogenic HEMTs

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Abstract

The development of high-performance quantum computers requires readout systems capable of energy-efficient amplification with minimal noise at cryogenic temperatures. Low-noise amplifiers (LNAs) based on InGaAs high-electron-mobility transistors (InGaAs HEMTs) are commonly employed to read low-power signals from a quantum processor, achieving a noise temperature of 2-4 K and a DC power consumption of a few milliwatts.

As future quantum computers scale up the number of qubits, the number of required LNAs may increase, potentially limiting power dissipation due to constrained cooling power.

Optimizing ohmic contact to reduce access resistance is crucial for minimizing signal loss, enhancing device efficiency, and reducing power dissipation at cryogenic temperatures.

This work investigates novel ohmic contact configurations and analyzes their effects on the performance of state-of-the-art InGaAs HEMTs. The metal stack has been optimized, and metal thicknesses were systematically varied to observe their impact on contact resistance and noise indication factor.

Various electrical characterization techniques have been employed, including transmission line measurements (TLM) to analyze the role of metal thickness in device performance.

The measurements aimed to determine the individual parasitic resistive components and assess the DC performance of the fabricated HEMTs at both room temperature and cryogenic conditions.

The results provide important insights into the correlation between the metal layer thickness and the contact resistance, contributing to the advancement of InGaAs HEMTs for quantum computing applications.

I would like to express my sincere gratitude to my supervisors, Cezar Zota and Eunjung Cha, for their invaluable guidance, continuous support, and constructive feedback throughout the development of this research. Their expertise and insights have been fundamental in shaping this work, and I am deeply grateful for the opportunity to have learned from them. I am truly appreciative of the help of Alberto Ferraris throughout the entire experience, particularly for their assistance with the measurement setup. Thanks to Maryline Sousa for performing TEM within this project and Antonis Olziersky for the great support during e-beam lithographic steps.

I also extend my sincere thanks to IBM Research Zurich for providing the necessary resources and a stimulating research environment that has greatly contributed to the success of this study. I am grateful to my colleagues and fellow researchers for their valuable discussions and collaboration, which have enriched both the scientific and personal aspects of this journey.

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Acronyms

HEMT
: High electron mobility transistor

LNA
: Low noise amplifier

RT
: Room temperature

2DEG
: Two dimensional electron gas

TLM
: Transfer length method

FET
: Field effect transistor

HFET
: Heterostructure field effect transistor

SCE
: Short channel effect

SEM
: Scanning Electron Microscopy

Chapter 1

Introduction

InP high electron mobility transistors (HEMTs) have long been studied for their outstanding properties, such as high-frequency and low-noise performances. Due to these characteristics, these devices represent the main focus in the design of low-noise amplifiers (LNAs) for quantum computing. Such amplifiers are electronic devices able to amplify small signals while reducing the noise added during the amplification process. They are used in various applications such as satellite communications, RF receivers and radar systems.

In this work, advancements in InP HEMTs for cryogenic low noise performances for quantum computing applications are presented. The improvement of noise properties of the InP HEMTs have shown great progress by optimizing heterostructures, such as adjusting gate to channel distance and introducing an InP etch stop layer [1]. However to take full advantage of HEMTs merits, the reduction of parasitic resistive component is crucial. Source resistance (R_s) is influenced by others individual resistive components whose impact is studied with *Transfer length method* (TLM) [2] and *Transmission line model* [3].

A comprehensive review of the state-of-the-art HEMT performance is essential to define the objectives of optimization: recent results of cryogenic InGaAs HEMTs such as the one published by Zeng *et al.* [4] report $R_{on} = 330\,\Omega\,\mu\text{m}$, $g_m^{max} = 1.8\,\text{mS}/\mu\text{m}$ at $V_d = 0.7\,\text{V}$, $SS_{min} = 18\,\text{mV/dec}$ at $V_d = 0.1\,\text{V}$ and $F_{min} = 0.22\sqrt{\text{Vmm/S}}$ at $P_{DC} = 1.6\,\text{mW/mm}$ for a 100 nm gate length. Remarkable performances have been obtained for cryogenic InGaAs HEMTs with cryo-optimized Ohmic contacts by Cha et al. [5] recently explored at IBM Research Europe where $R_{on} = 290\,\Omega\,\mu\text{m}$, $g_m^{max} = 1.75\,\text{mS}/\mu\text{m}$ at $V_d = 0.8\,\text{V}$, $SS_{min} = 8\,\text{mV/dec}$ at $V_d = 0.1\,\text{V}$ and $F_{min} = 0.18\sqrt{\text{Vmm/S}}$ at $P_{DC} = 0.5\,\text{mW/mm}$ were reported for a 130 nm gate length at 4 K. Research at IBM proceeded with cryogenic InGaAs HEMTs with optimized indium channel contents and contacts similar to the previous work by Cha et al. [6] obtaining a to-date record performance with $R_{on} = 198\,\Omega\,\mu\text{m}$,

$g_m^{max} = 2.3\,\mathrm{mS/\mu m}$ at $V_d = 0.7\,\mathrm{V}$, $SS_{min} < 10\,\mathrm{mV/dec}$ at $V_d = 0.1\,\mathrm{V}$ and $F_{min} = 0.15\sqrt{\mathrm{Vmm/S}}$ for a 170 nm gate length at 4 K.

The work presented in this thesis was undertaken in the Cryogenic Electronics team at IBM Research Zürich. The impact of different nickel (Ni) thicknesses on the same metal stack has been investigated observing the implications on the performance of state-of-the-art cryogenic InGaAs HEMTs. Ten different ohmic contact stacks were explored using two different epitaxial structures. Metal deposition was performed by evaporation in order to avoid problems in the fabrication related to sputtering. Resistive components were extracted with transfer length method, this method allows the analysis of the individual parameters influencing the source resistance. Then HEMTs DC characterization was carried out to observe the influence of the ohmic contacts on the HEMTs performance. The analysis was executed over different devices obtained by varying device widths and gate lengths. The influence of the design parameters and of the different epitaxial structures were investigated. All the measurement were performed both at room temperature (RT) and 4 K. Significant results have been achieved, showing a trend in contact resistance with the variation of the nickel thickness, moreover improved cryogenic performances have been recorded.

In chapter 2 a brief theory overview about the working principle of HEMTs and TLM can be found . Chapter 3 presents the experimental processes followed from the design to the fabrication of the devices. In chapter 4 the results are presented and discussed. Finally, chapter 5 briefly summarizes the conclusions and provides an outlook.

1.1 Background

Quantum computing is an emerging field of computer science gaining significant attention. The pioneer of this new area of research was Richard Feynman [7] who in the 1980s argued the need for quantum processors in the simulation of quantum physics phenomena.

Quantum mechanics relies on some key principles, such as entanglement, superposition and interference [8], which enable quantum systems to solve problems exponentially faster than classical computers. While the building block of a classical computer is the bit, which in principle is a transistor that can be either "0" or "1", the building block of a quantum computer is the qubit. It is possible to think to the qubit as a continuous object.

Referring to the superposition principle, the quantum bit is a linear combination

of the ground state and the excited state.

$$\Psi = \cos\frac{\theta}{2}\langle 0\rangle + e^{i\varphi}\sin\frac{\theta}{2}\langle 1\rangle \tag{1.1}$$

The two logical states of each qubit correspond to the eigenstates of a suitable physical system. A fundamental and illustrative example is the spin. [9]. A system of two qubits can be described as a linear superposition of four basis states: *00*, *01*, *10* and *11*. More generally, a system of N qubits would result in a superposition of 2^N states. This inherent property introduces a natural parallelism, which can be harnessed to achieve extraordinary computational capabilities, surpassing those of even the most advanced classical computers [10].

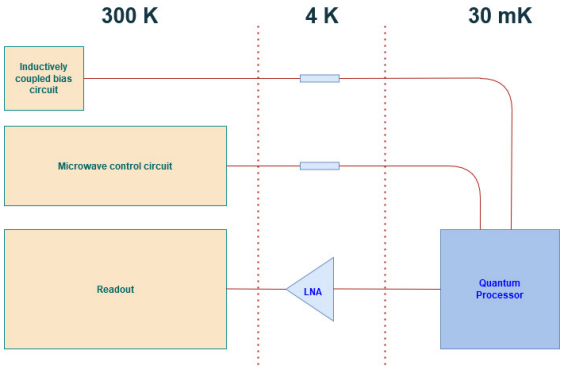


Figure 1.1: Quantum computer control system schematic

In figure 1.1 a block scheme of a quantum computer is shown, where three different temperature stages are observed. The actual quantum microprocessor is placed in the dilution refrigerator at a temperature close to 10 mK since the qubits need a cryogenic regime for the correct computation[11]. This has to do with the thermal noise and coherence between qubits.

The present work focuses on the HEMT LNAs present at the 4 K stage of a quantum computer. The exponential increase in the number of qubits integrated into quantum processors necessitates high-performance cryogenic LNAs for qubit readout[12]. To reduce interconnect losses and improve qubit readout sensitivity, it is beneficial to place the InP HEMT LNA at a cooling stage closer to the quantum processor, which operates at 10 mK [1]. However HEMT LNA for quantum computing operates at a 4 K stage, dissipating several milliwatts of power. Due to the cryogenic refrigerator's limited cooling capacity, it is not feasible to position the cryogenic LNA at a colder stage closer to the quantum processor[13]. Since the majority of the heat dissipation in the LNA arises from the transistors, it

becomes necessary to achieve improvements in the low-noise performances and in the low-power operation of HEMTs [13].

Chapter 2

Theory

To understand the phenomena underlying this study, it is essential to introduce the theoretical principles governing HEMTs. This chapter will discuss the fundamental concepts related to the conduction mechanism in these particular devices, and noise and parasitic resistive components will be discussed with the explanation for the extraction of these parameters, providing the necessary context for interpreting the experimental results. Particular attention will be given to the transfer length method, as it plays a central role in the analysis conducted in this work.

2.1 High Electron Mobility Transistors

High electron mobility transistors are heterostructure field-effect transistors offering higher power capacity and low noise performances. These achievements are possible due to particular material combinations exploited for the design of the epitaxial structure. The following discussion is based on Neamen [14].

In the majority of other devices, the channel region is always located within a doped layer of bulk semiconductor; this involves the majority carriers and impurities being in the same region. The consequence of these two kinds of particles being in the same area is a decrease of mobility due to the ionized impurity scattering that the majority carriers experience. In HEMTs the usage of heterostructures enables the separation of the two. In general, one doped semiconducting material named *barrier* is brought into intimate contact with an undoped semiconducting material, with a different bandgap with respect to the previous one, the *channel*, causing a band discontinuity at the interface between the two. The band discontinuity forms a two-dimensional electron gas (2DEG), a triangular-shaped potential well that confines electrons in one direction while leaving them free to move in the others. In figure 2.1 the band diagram of a generic InGaAs HEMT is shown.

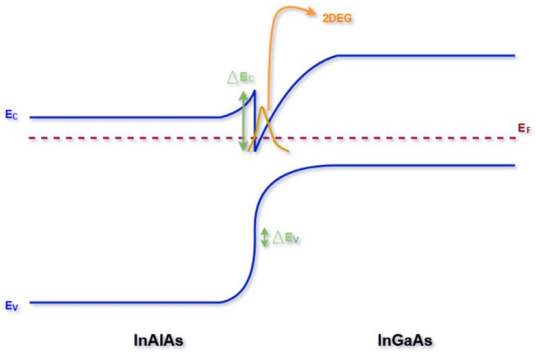


Figure 2.1: Simplified band diagram of an InGaAs HEMT

Despite the separation of the channel and the barrier, a Coulomb attraction can still be present between electrons and donor atoms. That is why a *spacer* is usually added: a layer of undoped material, as the one of the barrier, separating the barrier and the channel as shown in the generic cross section of an HEMT in figure 2.2. The disadvantage of this kind of structure is a decrease in the electron density. By adding a doping sheet of silicon atoms in the barrier layer, it is possible to tune the carrier concentration in the 2DEG.

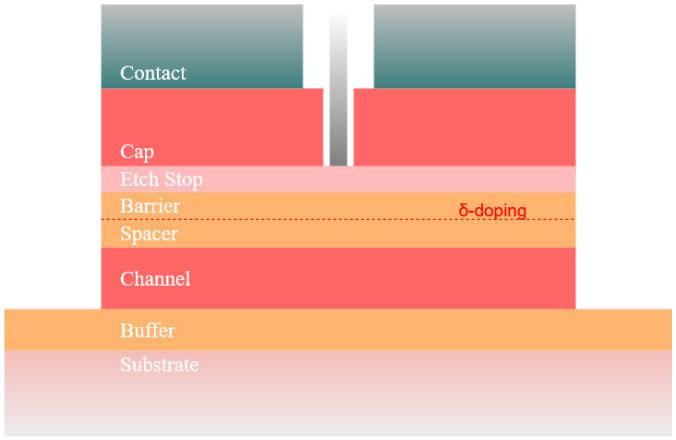


Figure 2.2: Generic HEMT cross section

A highly doped *cap* layer allows the formation of low-resistance ohmic contacts while gate is placed in a recess in the cap layer between source and drain, forming a Schottky contact. The gate modulates carrier density in the channel, enabling or disabling the conduction [15]. An *etch stop* layer may be included to ensure greater accuracy in the selective etching of the cap layer, preventing any impact on the

barrier [16].

The typical gate used in modern HEMTs is T-shaped gate or Y-shaped one, in fact the gate width is directly proportional to the electron transport time in the channel, which in turn determines the operating frequency of the device. While reducing the gate width enhances the frequency characteristics, it also increases the impact of gate resistance, negatively affecting high-frequency performance and noise figure. To mitigate this, a T-shaped gate configuration has been proposed, wherein a wide head and a narrow foot reduce gate resistance, thereby improving frequency response while maintaining a low noise figure [17].

2.1.1 Noise characterization and resistive components of cryogenic InP HEMT

HEMTs have widely been studied for their ultra-low-noise performances, the optimization of noise at low power is strictly necessary in fields such as quantum computing.

The modeling of noise performances of field effect transistors has been provided by Pospieszalski [18] [19]. Noise parameters are related to equivalent circuit elements following the semi-empirical approach of Fukui [20] [21]. Taking into account the elements of an equivalent circuit of a field effect transistor (FET), the minimum noise temperature can be expressed as:

$$T_{min} \approx 2\frac{f}{f_T}\sqrt{(R_s + R_g + R_i)T_g g_{ds} T_d} \tag{2.1}$$

where f_T is the cut-off frequency, R_s is the source resistance, R_g is the gate resistance, R_i is the intrinsic gate-source resistance, g_{ds} is the drain conductance, while T_g and T_d represent the gate noise temperature and the drain noise temperature respectively.

Equation 2.1 shows that the minimum noise temperature is a function of two frequency-independent constants (T_g and T_d), where the equivalent drain temperature is dependent on the drain current but not on the ambient temperature, while the equivalent gate temperature is often approximated by the device temperature, which at cryogenic temperatures can be higher than the ambient temperature due to self-heating [19][15].

The only dependence on the bias of the transistor is represented by f_T, which is itself proportional to the transconductance g_m and T_d, which is proportional to I_{ds}. Therefore, the bias dependence of the minimum noise temperature can be expressed as:

$$f(V_{ds,I_{ds}}) \cong \frac{\sqrt{I_{ds}}}{g_m}. \tag{2.2}$$

This expression indicates the *noise indication factor (F)* [18]. The optimal bias for lowest noise is thus found at the minimum of the noise indication factor.

Looking at equation 2.2 it is possible to observe that a low-noise HEMT should exhibit high transconductance while operating at a low drain current. To meet low-power requirements, the minimum noise figure must occur at the lowest possible drain voltage and drain current, as the DC power consumption is defined by $P_{DC} = V_d I_d$ [15].

It is now fundamental for the scope of this thesis to analyze the most important contributions of resistive components affecting the low-noise performance of the device. The source resistance is a key parameter because it affects the minimum noise temperature (T_{min}), thus the minimum noise figure (F_{min}) in FETs and HFETs as shown in equation 2.1.

The source resistance can be considered as the sum of four different resistance contributions: the contact resistance (R_c) between the metal and the cap layer, the resistance in the cap layer ($R_{sh,cap}$), the barrier resistance (R_b) formed among the heterostracture cap/barrier/channel and the channel resistance ($R_{sh,ch}$) [22].

At this point, it is important to analyze which of these contributions becomes critical at cryogenic regime. The contact resistance is expected to grow as the temperature decreases following the field-emission model [23]. When examining the metal-cap interface, the main source of current arises from carriers tunneling between the top of the donor band lying in the cap and the metal. In a cryogenic regime, the number of carriers in higher energy states declines due to a decrease in the temperature, resulting in a lower tunneling probability and a slight increase in contact resistance [24]. However the contact resistance does not represent the only critical resistance contribution at cryogenic regime. The barrier resistivity (ρ_b) is governed by a thermionic field-emission process [25] meaning that a thermal contribution promotes the tunneling of the electrons through the barrier to the cap. At cryogenic regime an increase of R_b can thus be observed due to the reduction of the thermal contribution. However for what concerns alloyed contacts a decrease in barrier resistance at low temperatures can be expected, this is attributed to the enhanced conductivity of the diffused metal within the barrier layer [5].

2.2 The Transfer Length Method (TLM)

The characterization of ohmic contacts is essential for assessing the performance of advanced electronic devices. Such contacts can be analyzed with the *Transfer length method* (TLM) introduced by Schockley [2]. In this section the contact characterization will follow Schroder analysis [26].

The computation of the resistive parameters requires the implementation of special test structures as the one shown in figure 2.3b. The working principle

consists of the application of a voltage between the source and drain contacts, causing a current flow. Due to the absence of a recess, the current will flow from the contact to the cap, then it will flow through the cap along the whole source-drain distance to finally arrive at the other contact. This can be summarized by the following equation:

$$R_{total} = 2R_M + 2R_C + R_{sheet,cap} l_{sd} \tag{2.3}$$

where R_C is the contact resistance, R_M the metal resistance which can be neglected, $R_{sheet,cap}$ is the sheet resistance of the cap, while l_{sd} is the distance between the source and the drain. Being the structure symmetric twice the values of R_M and R_C must be considered. In these structures contributions from the others resistive components are neglected since the cap is highly conductive and the current tends to follow the less resistive path.

At this point, different contacts are placed apart while varying gradually l_{sd} forming a structure as the one depicted in figure 2.4. Varying l_{sd}, a change in the measured resistance will be observed. When $l_{sd} = 0\,\mu m$ the computed resistance will just refer to the resistance that electrons will face at each interface between the cap and the ohmic contact. Looking at equation 2.3 it is possible to observe that plotting the measured resistances as a function of l_{ds}, $R_{sh,cap}$ can be extracted as the slope of the line and $2R_C$ as the y-intercept point; it is important to underline that R_{tot} is expressed in $\Omega\,\mu m$ meaning the measured resistance must be normalized by multiplying its value for the width of the device.

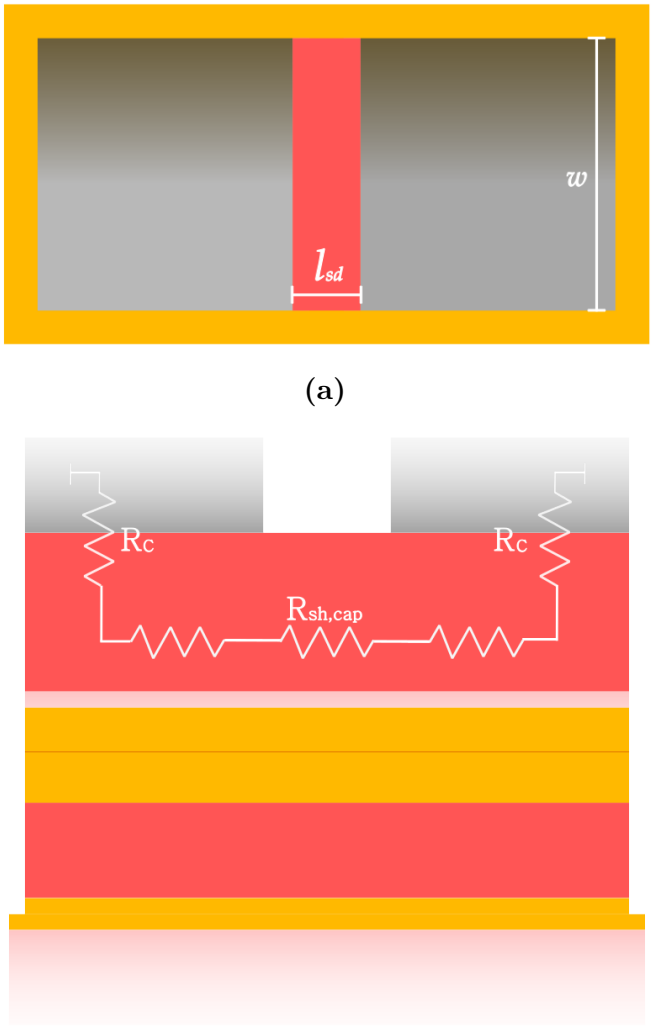
To ensure that the current flows only through the intended path, the area beneath the contacts must be electrically isolated from the surrounding substrate. This isolation can be accomplished in two ways: either by limiting the implanted or diffused regions using planar fabrication techniques or by etching away the surrounding material to create an elevated mesa structure [26].

The computation of the contact resistivity (ρ_C) requires the introduction of the *transfer length* (l_t). Indeed the traditional computation (ρ_C=$R_C A_C$) would not lead to a correct result since the current flow in the contact is not uniform all over the contact pattern, meaning that the real contact area is different from the physical one. The transfer length represents the length of the path the current is flowing under the contact and can be defined as the distance between the contact edge and the point where the voltage distribution reaches the "1/e" value [26].

$$l_t = \sqrt{\frac{\rho_C}{R_{sh,cap}}} \tag{2.4}$$

Being l_t the effective contact length and being the width already contained in normalized R_C the contact resistivity can be expressed as follows:

$$\rho_C \approx l_t R_C. \tag{2.5}$$



(a)

(b)

Figure 2.3: a) top view of TLM structure, b) simplified equivalent circuit of a TLM structure

Being $\rho_C = l_t^2 R_{sh,cap}$ from equation 2.4 and substituting to $R_C \approx \rho_C / l_t$ from equation 2.5 it is possible to write equation 2.3 as follows:

$$R_{tot} \approx 2 l_t R_{sh,cap} + R_{sh,cap} l_{sd}. \tag{2.6}$$

This linear dependence is valid if $l_{sd} \gg l_t$. Looking at equation 2.6 it is possible to extract l_t by the x-intercept of the R_{tot} line.

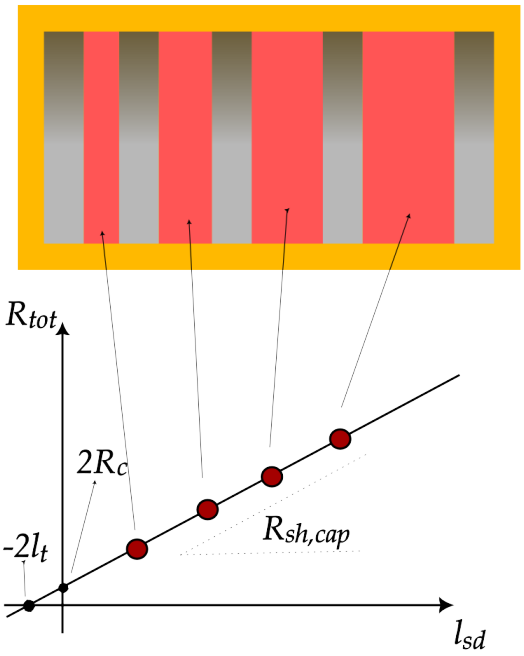


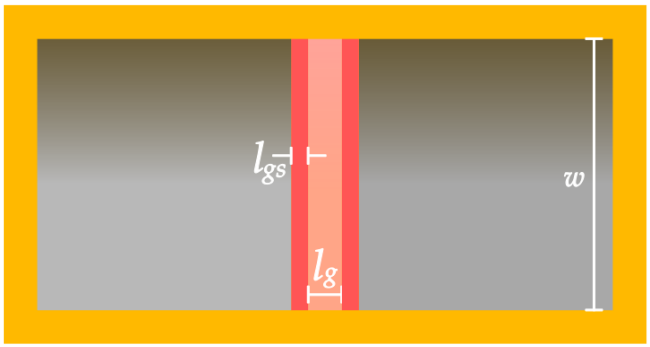
Figure 2.4: Schematic plot for the extraction of resistive components in non-recessed TLM structure

2.2.1 Recess Transfer Length Method

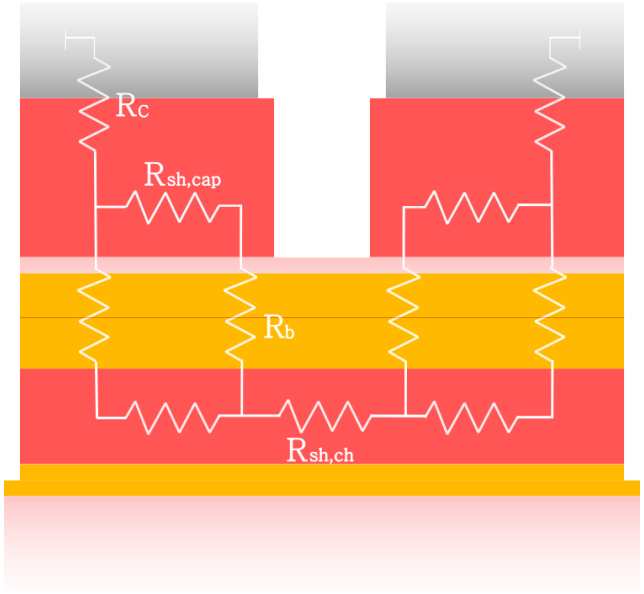
A simple one-layer model as the one described in the previous section is not able to describe the more complex structure of an HEMT with a gate recess. As shown in figure 2.5b in a recess TLM structure it is possible to distinguish three different regions: the ohmic electrode region is described by a three-layers transmission line where the electrons are injected from the ohmic metal to the cap layer and then to the channel through the barrier, the source access region described by a two-layers transmission line and the side-recess region governed by a simple one-layer transmission line [27].

Different models have been proposed for a theoretical analysis of the system such as [3] [27] [28], all using transmission line model [29]. In the present work the same experimental method of Lee *et al.* will be used, whose results showed the consistency with the analytical model [28].

The procedure to apply for the characterization of resistive components in a recessed TLM structure is similar to the one applied to the non-recessed TLM structures. It it is possible to distinguish two significant geometrical parameters: l_g which is the length of the recess and l_{gs} which is the distance from the recess to the contact. The channel sheet resistance $R_{sh,ch}$ is extracted like the $R_{sh,cap}$ in the



(a)



(b)

Figure 2.5: a) top view of a recessed TLM structure, b) simplified equivalent circuit of a recessed TLM structure

previous section by varying l_g exactly like l_{sd} was varied for TLM structures. This is performed at different l_{gs} obtaining a plot like the one shown in figure 2.6a where the slope of the lines is $R_{sh,ch}$. Being the channel sheet resistance a parameter independent on the contact to recess distance, the lines should be parallel. As in the case of non-recessed TLM structures the y-intercept point is extracted; these values (one for each l_{gs}) represent twice the *access resistance* (R_a). The access resistance is then plotted as a function of l_{gs} as shown in figure 2.6b. The y-intercept point corresponds to the sum $R_C + R_b$ while the slope of the line is the effective sheet

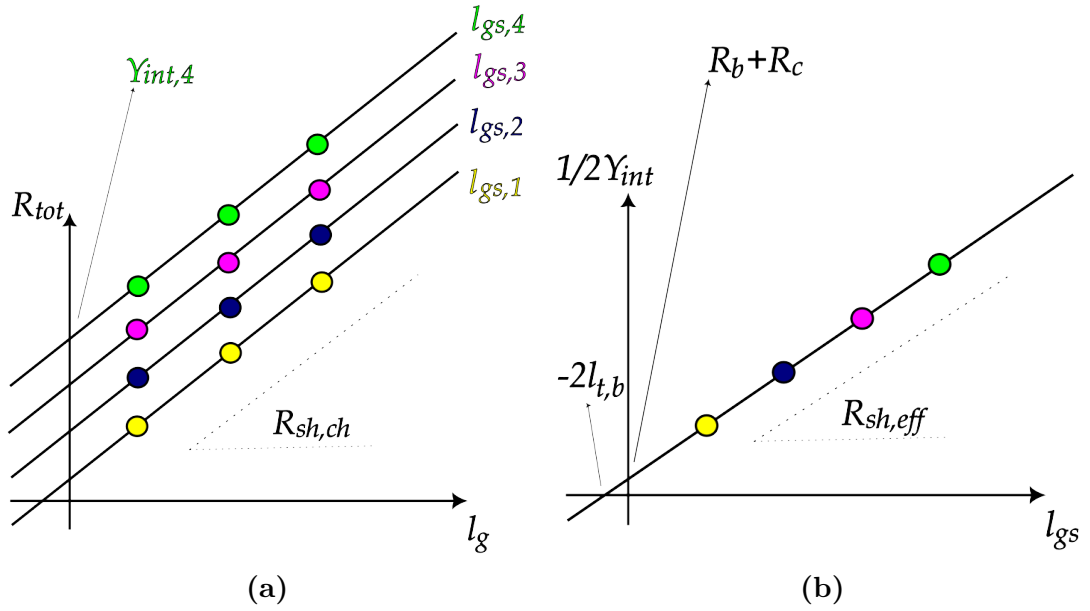


Figure 2.6: a) Schematic plot for the extraction of $R_{sh,ch}$ and the y-intercepts, b) Schematic plot for the extraction of $R_{sh,eff}$ and R_b

resistance ($R_{sh,eff}$):

$$R_{sh,eff} = \frac{1}{\frac{1}{R_{sh,cap}} + \frac{1}{R_{sh,ch}}}. \tag{2.7}$$

Knowing R_C from non-recessed structures, the barrier resistance computation is possible.

As concerns the barrier resistivity (ρ_b) a similar discussion as the one that arose for the contact resistivity can be held. The *barrier transfer length* ($l_{t,b}$) can be defined:

$$l_{t,b} = \sqrt{\frac{\rho_b}{R_{sh,cap} + R_{sh,ch}}}. \tag{2.8}$$

The linear dependence of the access resistance with l_{gs} is just possible for $l_{gs} \gg l_{t,b}$, otherwise a saturation is expected.

Chapter 3

Experimental

This chapter provides an insight into the experimental methods exploited in the present work. First, the design of the transistors and the TLM structures is analyzed, after that details about the epitaxial structures and the fabrication process are provided. Finally, the data evaluation techniques are described.

3.1 Design

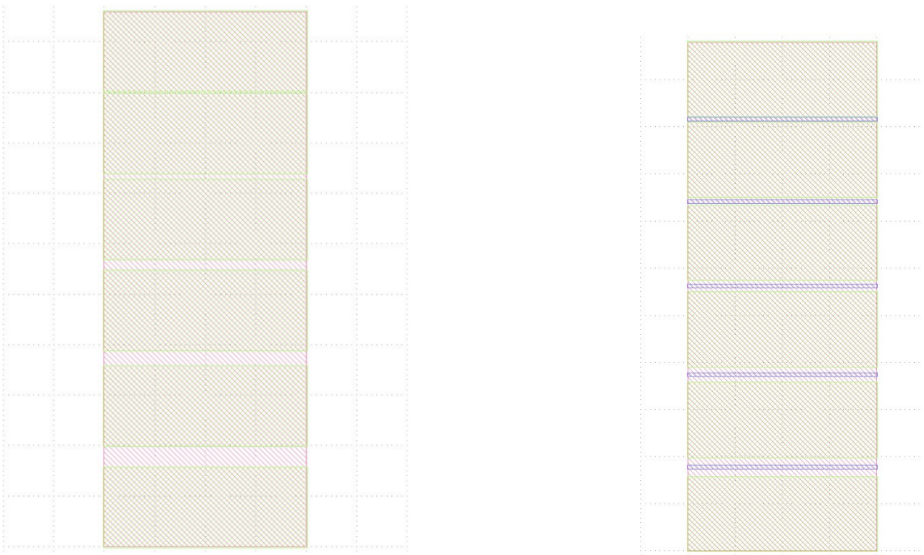
The analysis of the impact of different nickel thicknesses of the ohmic contact on InGaAs HEMTs performance employs different TLM structures. The e-beam lithography for the realization of those structures and for the HEMTs requires the design of different patterns acting as a mask for the exposure. The design was carried out by *KLayout Editor*.

3.1.1 TLMs

As concerns the TLM structures, one geometric parameter needs to be taken into account: the source-drain distance l_{sd}. The impact of device width could also be an interesting aspect to investigate, indeed, a first layout was realized with different structure widths. However, this aspect was no longer taken into account because of the time consuming measurements needed for the study. In this case the investigation was performed with $w = 200\,\mu m$.

Non-recessed TLM structures were obtained by varying source-drain distances ($l_{sd} = 2\,\mu m$, $5\,\mu m$, $10\,\mu m$, $15\,\mu m$, $20\,\mu m$) as shown in figure 3.1a.

Concerning the recessed TLM structures, two geometric parameters need to be taken into account: the recess length (l_g) and the gate-source distance (l_{gs}). Five different recess lengths ($l_g = 0.6\,\mu m$, $1\,\mu m$, $2\,\mu m$, $4\,\mu m$, $8\,\mu m$) were considered and, for each of those recess length a structure obtained by varying the gate-source



(a) TLM design **(b)** Recessed TLM design, $l_g = 2\,\mu m$

Figure 3.1: TLM layout

distance ($l_{gs} = 1\,\mu m$, $2\,\mu m$, $4\,\mu m$, $6\,\mu m$, $8\,\mu m$) was designed.

Figure 3.1b shows an example of recessed TLM structure design with $l_g = 2\,\mu m$, the l_{gs} length instead varies from the top to the bottom of the structure.

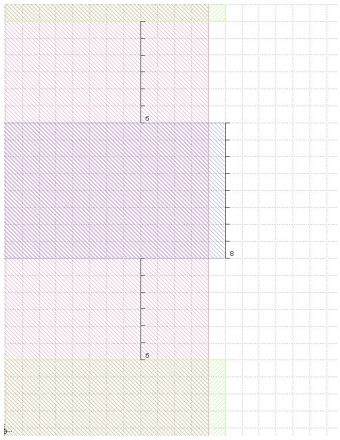


Figure 3.2: Example of recessed TLM design, $l_g = 8\,\mu m$, $l_{gs} = 6\,\mu m$

Figure 3.2 shows a closer view of a recessed TLM structure, precisely the $l_g = 8\,\mu m$ and $l_{gs} = 6\,\mu m$.

3.1.2 HEMTs

The HEMTs were designed as two-finger transistors. In this case, different device widths have been investigated; the selected values were $w = 10\,\mu m$, $30\,\mu m$, $50\,\mu m$, $100\,\mu m$. For each width, gate lengths of $l_g = 40\,nm$, $70\,nm$, $100\,nm$, $130\,nm$ were designed. In addition, large measurement pads were designed with a consistent outline, regardless of device dimensions, to facilitate automated measurements.

3.2 InP Technology

3.2.1 Epitaxial structure

In the present work, cryogenic InGaAs HEMTs were investigated. Two different epitaxial structures were used, respectively labeled *epiA* and *epiB*.

Figure 3.3: Epitaxial structure A

Figure 3.4: Epitaxial structure B

In figure 3.3 and 3.4 the two different cross sections are shown.

The two different epitaxial structures (epi) were grown by molecular beam epitaxy. These heterostructures were sourced from a commercial vendor and were not designed as part of this project. Details cannot be shared for confidentiality, however, it is important to underline epiB peculiarity: the cap presents an additional δ-doping. The impact of the epitaxial structure on the performance of the devices will be analyzed in chapter 4.

3.2.2 Fabrication

The fabrication process for the realization of the previously described devices was conducted at the Binnig and Rohrer Nanotechnology Center (BRNC) using state-of-the-art nano and microfabrication tools.

Two different wafers were used, whose epitaxial structures are described in section 3.2.1. 3-inch InP wafers were purchased from a commercial vendor and were diced into 1.5 x 1.5 cm^2 chips and eBL alignment markers were deposited. A total of 5 chips were fabricated by means of a 5-ebeam step process. The e-beam exposure was handled by BRNC operative team.

The first fabricated sample was intended for a preliminary study to identify potential trends in contact resistance as a function of Ni thickness of the ohmic contact, or other indications that would lead to the choice of the thicknesses of the Ni layer in the following samples. This led to the realization of TLM and recessed TLM structures without HEMTs for the first sample, therefore **GATE** and **METAL1** step were not performed for this chip. The second sample was realized with **epiA** as the first one. Here, four different metal thicknesses were studied by extracting the resistive components using TLM and recessed-TLM structures, along with the DC characterization of HEMTs. The following samples were fabricated using epiB. However, for greater process reliability, only one thickness was deposited on the third and fourth samples, while two thicknesses were used for the last one.

In the following, a description of the fabrication process can be found. Details could not be mentioned due to confidentiality:

- **MESA**: the realization of the mesa required for the isolation of the devices was carried out by removing the cap, the etch stop, the barrier, the spacer, the channel and the parts of the buffer between the structures. To begin, the chip surface was either dehydrated or treated with the adhesion promoter. Next, a negative e-beam resist was applied via spin coating, followed by a soft bake. After the e-beam exposure of the rectangular patterns that define the TLMs and HEMTs, the resist was developed. The proper development was verified using a digital microscope. Any remaining resist residues were then removed in a plasma asher, then the sample underwent a hard bake. After the development, since a negative resist was used, the exposed rectangular pattern remained covered with resist, unlike the rest of the sample. This allowed for the selective etching of the required layers, leaving behind standing structures. The etching process used throughout the fabrication was wet etching. First, the cap layer was etched, followed by the removal of the etch stop. Finally, the barrier, channel, and parts of the buffer were also etched. The consistency of the etched height was verified using a surface profiler. The strip of the resist was then performed. In figure 3.5 the original epitaxial structure and the mesa are shown. EpiA was chosen as an example for the images in this section.

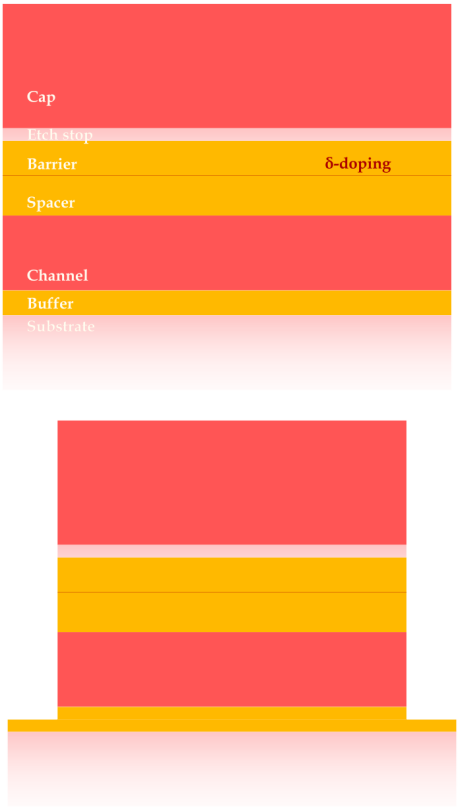


Figure 3.5: Epitaxial structure (top), MESA creation (bottom)

- **RECESS**:the second step aims at the definition of the recess into the cap layer. The surface of the chip was dehydrated and coated with two layers of positive e-beam resists before soft baking. The recess patterns were then exposed with ebeam lithography. During the development, since a positive resist was used, the exposed areas were stripped of resist, while the unexposed regions remained covered, providing protection for the subsequent etching process. The sample was then treated in plasma asher and hard baked. First, the wet etching of the surface oxide was performed, followed by the etching of the cap layer. After verifying the complete removal of the cap layer for the recess, the resist was stripped, following the same procedure as in the previous step. In figure 3.6 the recess creation is shown.

- **OHMICS**: In this step the definition of the ohmic contact patterns and the

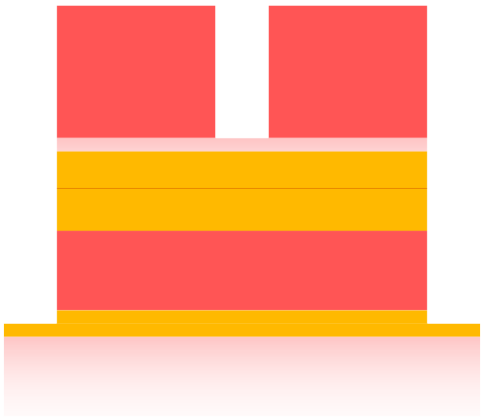


Figure 3.6: Recess

metal deposition were carried out. First a demoisturizing bake was undertaken, then samples were coated with two layers of positive resist. After the soft baking the patterns of the ohmic contacts were exposed by ebeam lithography and the development was performed. After verifying the correct development of the resist under the microscope, the samples were subjected to oxygen plasma treatment and baking. Next, the deposition of the ohmic contact metals was carried out. As previously mentioned, five samples were fabricated. For all samples, the metal stack consisted of a first layer of nickel (Ni), a second layer of platinum (Pt), and a final thicker layer of gold (Au). Pt is used as a diffusion barrier for Au as Au is diffusive. The thickness of Ni was varied while the thickness of the other two layers was kept constant at 20 nm for the platinum and 150 nm for the gold.

Sample	**Epi**	**Thickness 1**	**Thickness 2**	**Thickness 3**	**Thickness 4**
SA1	EpiA	Ni 3nm	Ni 6nm	Ni 10nm	–
SA2	EpiA	Ni 0.6nm	Ni 1nm	Ni 2nm	Ni 3nm
SB1	EpiB	Ni 1nm	–	–	–
SB2	EpiB	Ni 3nm	–	–	–
SB3	EpiB	Ni 2nm	Ni 6nm	–	–

Table 3.1: Nickel thicknesses in the fabricated chips

In table 3.1 the different Ni thicknesses deposited for each sample are summarized. In the following to discuss about a specific metal stack the name *Epitaxial structure-nickel thickness* will be used. For example EpiA-1nm will be used to refer to the contact stack with 1nm Ni thickness built on epiA.

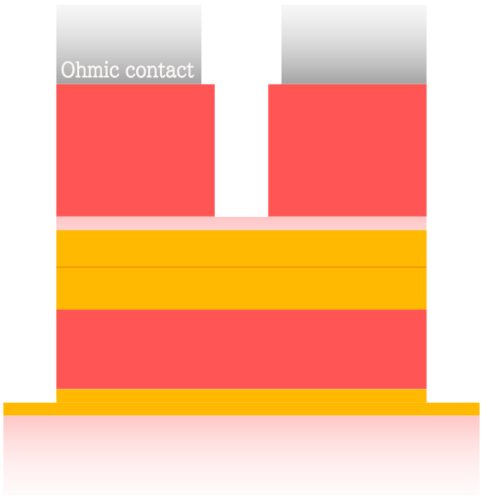


Figure 3.7: Ohmic contact deposition

The metals deposition was performed through evaporation. For what concerns the deposition rate different recipes were used. In **SA1** all the metals were deposited with a 0.2 nm/s deposition rate. For what concerns the other samples, the deposition rate of Pt and Au was kept at 0.2 nm/s while the Ni one was changed to 0.05 nm/s to improve adhesion and uniformity of the thin film. After the metal deposition the lift-off was performed, using ultrasonic bath for a better removal of the metal layer.
Since different metal stacks were designed on a single sample, the entire step was repeated multiple times, each time exposing different ohmic patterns. In figure 3.7 the deposition of the metal for the ohmic contact is shown.

- **GATE**: as already discussed in section 2.1, modern HEMTs mainly employs T-shaped or Y- shaped gates that are known to improve frequency response [17], however in this thesis HEMTs performances are evaluated only by DC characterization techniques making the impact of the gate design not really meaningful. For this reason an I-shaped gate was considered for all the fabricated devices making the fabrication process easier.
  This step is quite similar to the previous one. First a demoisturizing bake was undertaken, then samples were coated with two layers of positive resist. After the soft baking the ebeam lithography for the gate structures was performed. After the development the sample was subjected to oxygen plasma and baking. The deposition of the gate metal was performed right after the etching of the surface oxide. The gate consisted of 3 nm Pt, 20 nm Ti, 10 nm Pt and finally 150 nm Au. The deposition rate was kept at 0.2 nm/s for all the layers. After

the metal deposition the lift-off was performed. In this case the ultrasonic bath was not recommended because the tiny structures of the gate would have been damaged by the high frequency vibrations. In figure 3.8 the gate deposition is shown.

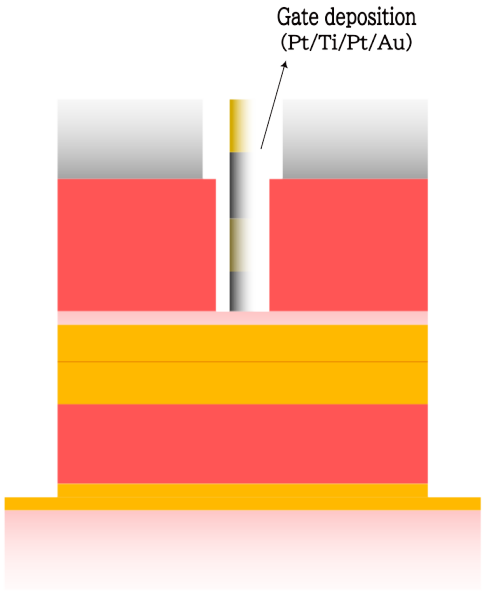


Figure 3.8: Gate deposition

- **METAL1**:the same procedure followed in the previous step was performed, in this case the deposition involved 30 nm Ti and 200 nm Au. Even in this case the ultrasonic bath could not be used during the lift-off because of the tiny gate structures that would have been affected. In figure 3.9 the deposition of the metal pads is shown.
- **ANNEALING**: in platinum-based gates annealing is a common process that allows Pt to diffuse from the first gate layer through the etch stop into the barrier layer, forming a buried gate. This is known to be beneficial for the device performances since it reduces short channel effects (SCEs) and causes a positive shift of the threshold voltage [30]. For this reason, an annealing at 270°C for approximately 20 minutes in an atomic layer deposition chamber was undertaken. Ohmic contacts can also be annealed to form alloyed contacts. However, the use of non-alloyed contacts has been shown to improve device performance [24]. Depending on the metal, the required annealing temperature for the contacts can vary significantly: it can be much higher than the gate annealing temperature or, in some cases, lower, as with nickel. Annealing the gate at 270°C inevitably affected the metal layer, leading to the formation of

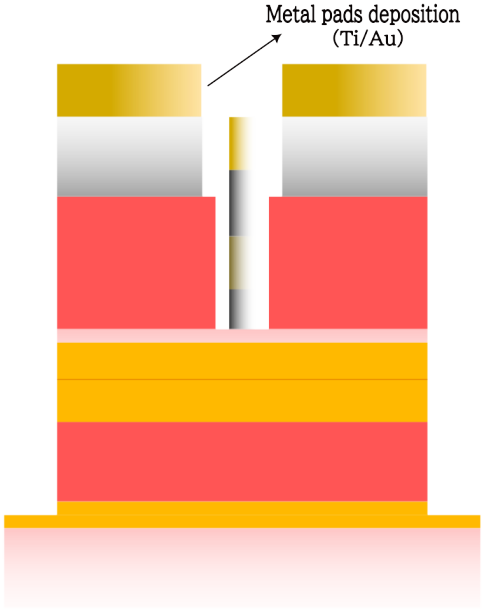


Figure 3.9: Metal pads deposition

alloyed contacts. The present step was carried out only for samples made with epiA and represented their final fabrication step. A different step was instead required for epiB chips, the reasons behind this choice will be discussed in the following.

- **PASSIVATION**:epiB presents a thinner *barrier* with respect to epiA meaning that some surface traps formed in the recess area after the etching process are closer to the channel. This could influence cryo device performances [31]. Therefore the samples needed to be passivated with Al_2O_3 in atomic layer deposition chamber. The deposition was performed at 270°C, moreover this step enabled the formation of a buried gate, making unnecessary the annealing step required for epiA. The patterning of Al_2O_3 (only active area needed passivation) required a further eBL step, followed by HF etching.

3.3 Measurements

3.3.1 Measurement setup

The measurement of the fabricated TLM structures and HEMTs were held by two different measurement setups. Both these setups were provided of *Keysight Agilent B1500A* semiconductor device analyzer (SDA) with four source measurement units

(SMUs) operated by the EasyEXPERT software. The first setup shown in figure

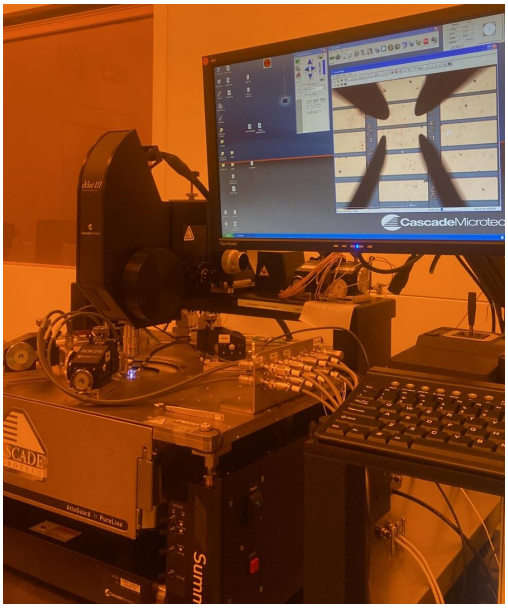
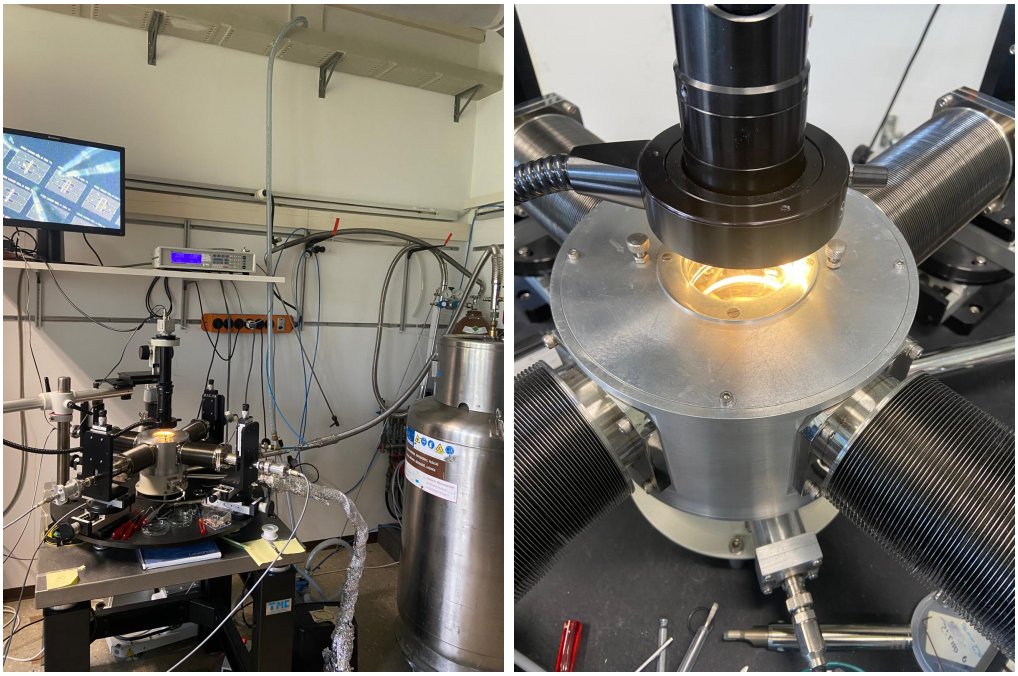


Figure 3.10: Probe station used for RT measurements

3.10 consisted of a custom probe station designed for semi-automatic measurements at room temperature. The system was controlled by Velox software, which managed the measurement process, while the platen movement had to be operated separately using dedicated software.

For low-temperature measurements, a custom-designed probe station equipped with a cryostat was used as shown in figure 3.11. The cryostat housed a sample mounting chuck and provided access to four probe arms, along with an evacuation system and a helium transfer line. Each probe arm could be manually adjusted using precision screws, enabling fully manual probing under cryogenic conditions. A window in the cryostat, coupled with a digital camera, allowed for precise monitoring of probe positions. The helium transfer line was connected to a liquid helium dewar, enabling cooling to approximately 4 K. During experiments, the chuck temperature fluctuated between 3 K and 5.5 K; however, for simplicity, all temperatures will be referred to as 4 K unless otherwise specified. Alberto Ferraris and Eunjung Cha assisted in loading and unloading the cryostat. Due to the manual operation of the low temperature setup, only a selection of TLM structures and HEMTs could be analyzed at 4 K. Concerning recessed TLM structures, no repetition on devices with identical dimensions was performed.



(a) **(b)**

Figure 3.11: a) Cryogenic probe station with helium pump, b) zoom on the chuck of the cryogenic probe station

3.3.2 Evaluation of resistive components

The measurements of the TLM structures were performed using a four-probe configuration, where each probe was connected to a Source Measurement Unit (SMU) of the Semiconductor Device Analyzer (SDA).

Two probes were used to apply a current sweep from 0 to 1 mA with 10 µA steps and a 100 mV compliance voltage, while the remaining two probes measured the voltage across the device. From the obtained I-V curves, the total resistance was extracted by normalizing the inverse of the slope by the nominal device width (w). To achieve an accurate estimation of the parasitic resistance components, it is essential to consider the actual geometric parameters of these structures, as process variations can lead to deviations between the designed and fabricated dimensions, impacting resistance calculations. To correct for these deviations, the real geometric parameters were measured using Scanning Electron Microscopy (SEM), which highlighted differences between the fabricated and designed structures. A more detailed discussion on this topic is provided in section 4.1.

The uncertainties related to the geometric parameters (l_g, l_{ds}, l_{gs}, w) and the total resistance R_{tot} were neglected. However, multiple repetitions of each TLM

structure were fabricated, allowing for statistical analysis. For what concerns TLMs, the total resistance value for each l_{ds} was determined as the mean of different measurements, while its standard deviation was computed using:

$$\sigma_i = \sqrt{\frac{1}{n-1}\sum_{i=1}^{n}(R_{tot,i,j} - \overline{R_{tot,i}})^2} \tag{3.1}$$

where $\overline{R_{tot,i}}$ is the mean of the total resistance for a given l_{ds}. The division by *n-1* in the standard deviation calculation is known as Bessel's correction, which accounts for the fact that the true population mean is unknown and only access to a finite sample is assured. The *-1* in the denominator corrects for the bias, ensuring that the standard deviation is not underestimated [32].

As discussed in the previous sections, plotting the total resistance as a function of l_{ds}, it is possible to retrieve the resistance value of the contact. Weighted linear regression was exploited for the total resistance plot. It computes a straight line with slope and intercept, minimizing weighted square errors where the weights are expressed as:

$$w_i = \frac{1}{\sigma_i^2} \tag{3.2}$$

A higher standard deviation corresponds to a lower weight, reducing the influence of that point in the final regression. So:

- The intercept of the regression corresponds to twice the contact resistance ($2R_C$)
- The slope of the regression corresponds to the sheet resistance $R_{sh,ch}$

The standard deviation of the slope was computed as:

$$\sigma_{Rsh,cap} = \frac{\sigma_{residue}}{\sum w_i(l_{sd,i} - \overline{l_{sd}})^2} \tag{3.3}$$

where $\overline{l_{sd}}$ corresponds to the weighted mean :

$$\overline{l_{sd}} = \frac{\sum w_i l_{sd,i}}{\sum w_i} \tag{3.4}$$

and the residual standard deviation is calculated as:

$$\sigma_{residue} = \sqrt{\frac{\sum w_i(R_{tot,i} - \widehat{R_{tot,i}})^2}{\sum w_i - 2}} \tag{3.5}$$

where

- $\widehat{R_{tot,i}}$ is the total resistance predicted by the linear regression model.
- $\sum w_i - 2$ represents the degrees of freedom (two parameters: slope and intercept).

Similarly, the standard deviation of the intercept was given by:

$$\sigma_{intercept} = \sigma_{slope}\sqrt{\frac{\sum l_{ds,i}^2}{n}} \tag{3.6}$$

where n is the number of data points. Thus, the standard deviation of the contact resistance is:

$$\sigma_{R_C} = \frac{\sigma_{intercept}}{2}. \tag{3.7}$$

The process used to determine $R_{sh,ch}$ and R_b follows the same statistical methodology. Bessel correction and weighted linear regression were applied to plot R_{tot} as a function of the recess length (l_g) for different gate-to-source distances (l_{gs}). The sheet resistance ($R_{sh,ch}$) was obtained as the slope of the regression.

Once the slope, intercept, and their standard deviations were computed, the access resistances (the intercept points) divided by two were plotted as a function of l_{gs}. In this case, the same weighted linear regression model was used, with the standard deviation of the intercept points divided by 2 as the weighting factor. However, in this step, the Bessel correction was not applied because these points are not derived from independent measurements; rather, their uncertainties originate from the linear regression model of the previous plot.

The final intercept represents the sum $R_C + R_b$. The standard deviation follows the same principles as before:

$$\sigma_{R_b} = \sqrt{\sigma_{R_C+R_b}^2 + \sigma_{R_C}^2} \tag{3.8}$$

Regarding cryogenic measurements, on average, fewer measurements were performed compared to those at room temperature due to the complete absence of an automated setup.

3.3.3 HEMTs DC characterization and Noise Indication Factor

High electron mobility transistors (HEMTs) were measured using the same setup exploited for the TLM structures with a three-probes configuration, one connected to the gate, one to the source and one to the drain. Each probe, as in the previous case, was connected to a SMU of the SDA.

To fully analyze the behavior of the devices in different operating conditions two different curves were analyzed: the transfer curve and the output curve.

The ***transfer function*** is obtained by plotting the drain current (I_d) as a function of the gate-source voltage (V_{gs}) at different drain-source voltages (V_{ds}). The gate voltage V_g was swept from $-0.4\,\mathrm{V}$ to $0.6\,\mathrm{V}$ with $10\,\mathrm{mV}$ steps while the source was grounded for fixed V_d values ($V_d = 0.1\,\mathrm{V}$ to $V_d = 0.7\,\mathrm{V}$). The compliance voltage was set to $5\,\mathrm{mV}$ for the gate and $100\,\mathrm{mV}$ for the drain. The parameters recorded from the SDA were I_d, I_g and g_m. These parameters were normalized by the nominal device width w. In general, three different regions can be observed in this curve:

- **cut-off region**: for V_g values lower than the threshold voltage the channel does not conduct meaning $I_d \simeq 0$;
- **active region**: for V_g values higher than the threshold voltage the drain current I_d rapidly grows;
- **saturation region**: after a certain V_g, the current I_d saturates due to different effects such as mobility and velocity saturation.

The first parameter that can be computed with the transfer function is the threshold voltage. In the present work it was extracted exploiting the generalized Constant Current method (CC) which uses an arbitrary current criterion [33] (in the present work $I_{th} = 1\,\mathrm{nA/mm}$) to determine threshold voltage.

The **transconductance (g_m)** can be extracted from the slope of the transfer curve, indeed:

$$g_m = \frac{\delta I_d}{\delta V_{gs}} \tag{3.9}$$

It should be high enough to assure high gain [34] and good low noise performances, however not too high since it could degrade input dynamic range [35].

Another important parameter for the low noise performances of the devices is the **noise indication factor (F)**:

$$F = \frac{\sqrt{I_d}}{g_m}. \tag{3.10}$$

The minimum noise temperature is obtained approximately at F_{min} representing the optimal bias for low noise performances. Therefore an high g_m at a low I_d is desired [36].

Finally, the **subthreshold swing** can be computed, which gives important information about the switching behavior of the device:

$$SS = \frac{\delta V_{gs}}{\delta log_{10} I_d} \tag{3.11}$$

The subthreshold slope is related to the ratio g_m/I_d indeed:

$$\frac{g_m}{I_d} = \frac{log(10)}{SS} \tag{3.12}$$

[37]. Thus in order to have a high transconductance at low drain current a low subthreshold swing is needed.

The second function analyzed for the study of HEMTs performances was the ***output function***. It is obtained by plotting the drain current (I_d) as a function of the drain-source voltage (V_{ds}) at different gate voltages (V_g). The drain voltage V_d was swept from 0 to 0.7 V with 7 mV steps while the source was grounded for fixed V_g values ($V_g = -0.3$ V to $V_g = 0.6$ V). The compliance voltage was set to 10 mV for the gate and 100 mV for the drain.

The parameters recorded from the SDA were I_g and I_d. These parameters were normalized by the nominal device width w.

In general three different regions can be observed in this curve:

- **linear region (ohmic)**: for low V_{ds} values, I_d grows in a linear way and the channel behaves like a resistance;
- **saturation region**: for higher V_{ds} the drain current I_d saturates at a constant value due to the channel pinch-off;
- **breakdown region**: at very high V_{ds}, the current I_d rapidly grows, this region is usually avoided because it can lead to the breakdown of the device.

An important parameter that can be extracted from this curve is the on-state resistance R_{on} defined as:

$$R_{on} = \frac{V_{ds}}{I_d} \tag{3.13}$$

which represents the resistance exhibited by the device in the linear region. Being a parameters that describes the resistance that the currents encounters in the channel of the device, a low R_{on} is desired. In some cases, a "kink" has been observed in the output curve, attributed to the presence of heavy dopants that introduce traps within the channel [38]. This effect is increased at cryogenic regime since the decrease of the temperature is found to enhance the surface traps [31]. This phenomenon manifests itself as a sudden increase in I_d in the saturation region, leading to undesired non-linearities in device operation.

Various measurements were conducted to analyze the performance of the HEMTs. Regarding room temperature measurements, all fabricated devices were tested, ensuring that each combination of gate length (L_g) and device width (w) included at least two measurements. Conversely, at cryogenic temperatures, only devices with a width of 10 µm were measured due to the absence of an automatic setup. Even in this case, at least two measurements for each geometric parameter combination were ensured.

Chapter 4

Results and Discussion

This section presents and discusses the results obtained throughout the study. First, the fabrication quality is evaluated through optical and electron microscopy inspections, ensuring that the technological process yielded well-defined structures. Next, the extracted electrical measurements are analyzed, providing insight into the key parameters of the devices and their statistical reproducibility. Finally, the obtained results are compared with previous studies, highlighting similarities, discrepancies, and potential advancements achieved in this work.

4.1 Fabricated devices

The fabricated structures were checked at the optical microscope to look for fabrication defects. As concerns TLM structures, no significant differences could be observed, moreover, electronic measurements exhibited consistent behavior in most of the structures. As a result, the data provided reliable statistics and ensured good reproducibility, reinforcing the credibility of the measurement results.

For a correct extraction of resistive parameters a big accuracy of the design parameters is necessary. At this purpose SEM was used. As expected some differences with respect to the design parameters were underlined; this does not represent a problem since the computation of the resistive components was performed with the corrected parameters.
In figure 4.1 a SEM image showing real device lengths can be observed. Minimal variations were observed between structures within the same sample and were therefore neglected. In figure 4.2 the corrections with respect to the nominal lengths can be observed. Columns not shown in the plots presented some issues that will be discussed later in this paragraph. EpiA-1nm was included in the plots as it was the only stack exhibiting differences compared to other stacks within the same sample. Corrections in l_{sd} are negative, indicating that the actual source-drain

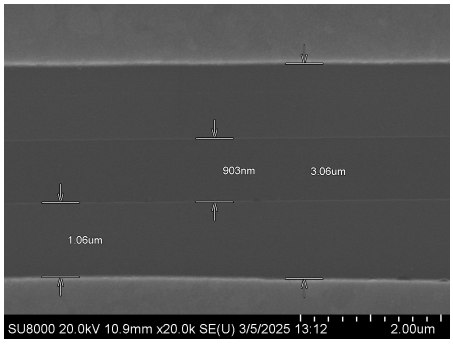
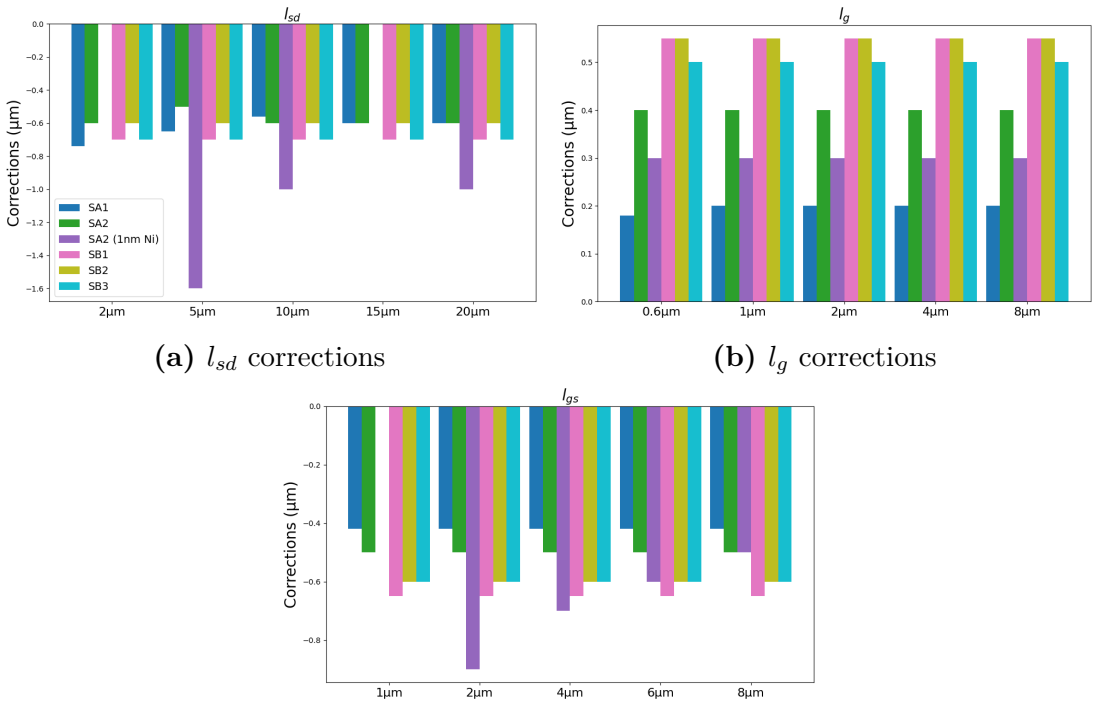


Figure 4.1: SEM image of recess-TLM for design lengths of $l_g = 0.6\,\mu m$ and $l_{gs} = 2\,\mu m$



(a) l_{sd} corrections

(b) l_g corrections

(c) l_{gs} corrections

Figure 4.2: Corrections of geometric parameters in TLM structures

distances are smaller than expected. This is attributed to metal deposition during the eBL process. The wet etching process seemed to contribute to larger actual l_g. A combined effect of these factors influenced the corrections in l_{gs}, which defines the distance between the ohmic metal and the recess, ultimately leading to a reduction in actual l_{gs}.

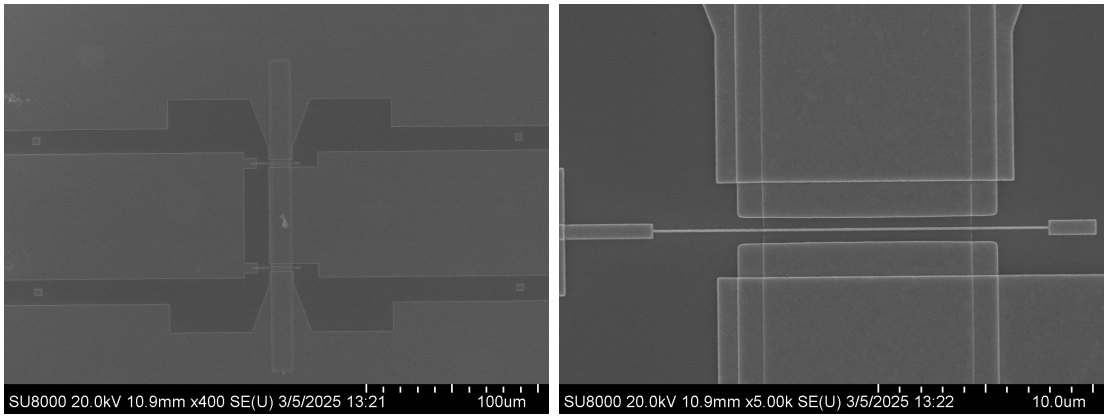


Figure 4.4: SEM images of a working HEMT with $L_g = 100\,\text{nm}$

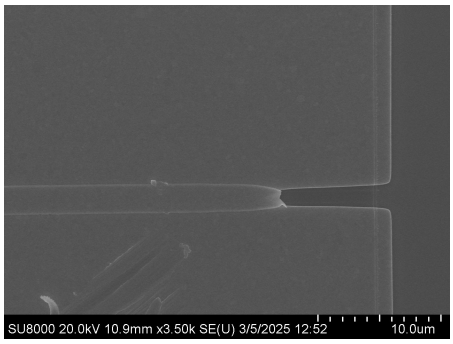


Figure 4.3: SEM image of shorted recessed TLM for design lengths of $l_g = 0.6\,\mu\text{m}$ and $l_{gs} = 14\,\mu\text{m}$

In some cases a not complete lift-off could be observed for small contact distances, such as $l_{sd} = 2\,\mu\text{m}$ for non-recessed TLM structures or $l_g = 0.6\,\mu\text{m}$ and $l_{gs} = 1\,\mu\text{m}$ for recess TLM structures as shown in figure 4.3.

For HEMTs devices, more irregularities in the fabrication process could be observed due to the significantly small structures taken into account on the order of some nanometers. In figure 4.4 SEM images of working devices can be observed. However in some devices as EpiA-1nm, SEM revealed some problems in the lift-off of the ohmic contact, probably caused by an incomplete resist development in the area between the contact pads and the gate. This caused all the structures to be shortened thus unreliable as shown in figure 4.5.

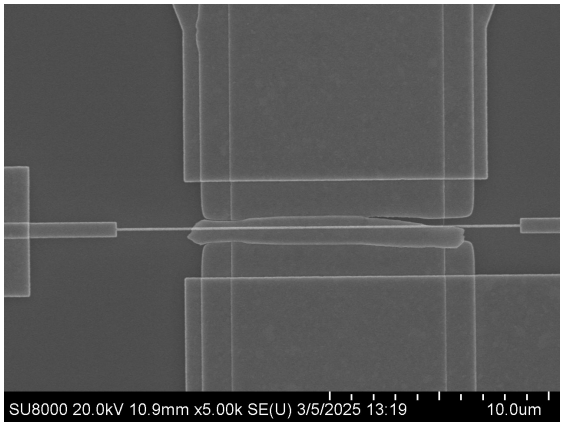


Figure 4.5: SEM images of a HEMT with non-completed gate lift-off, EpiB-1nm $L_g = 100\,\text{nm}$

Furthermore devices with metal stack EpiB-6nm were revealed to be damaged too.

4.2 Measurements

4.2.1 TLM Structures

Data extracted from the TLM structures measurements were exploited to retrieve the individual resistive components of the fabricated devices. Measurements were performed for each fabricated structure. Two different epitaxial structures were used for the fabrication and in each device Ni thickness in the ohmic contact was varied. Measurements have been performed both at room temperature and at 4 K.

For what concerns room temperature computations, due to the presence of a semi-automatic measurement setup, two different structures for each metal stack were measured for both TLM structures and recessed-TLM ones.

For cryogenic regime computations instead just one structure was measured for recessed-TLMs, due to the absence of an automatic setup. In this section results from the TLM analysis of sample EpiB-1nm will be discussed.

Figure 4.6a shows RT TLM measurements, thus the total resistance R_{tot} as a function of the drain-source distance l_{sd} at room temperature. The detailed description about the computation has already been discussed in section 2.2. As expected R_{tot} increases linearly with l_{sd}, on the graph a vertical bar should represent the dispersion between resistance measurements at the same l_{sd}. The vertical bar is not really visible meaning that the measurement are highly reproducible. The coefficient of determination (R^2) close to 1 assesses the quality of the fit. The average contact resistance R_C is $31.95\,\Omega\,\mu\text{m}$ with a standard deviation $\sigma_{R_C} =$

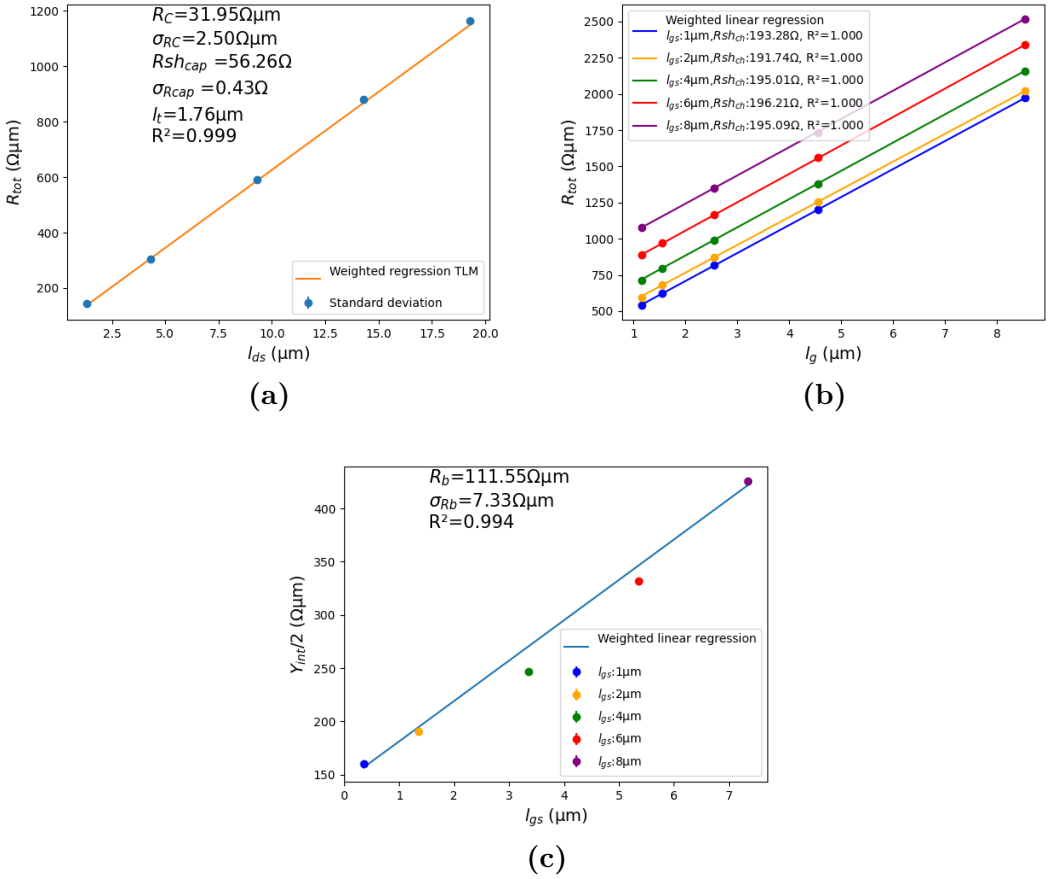


Figure 4.6: Resistive parameters extraction for EpiB-1nm at RT

2.5 Ω μm while the average cap sheet resistance $R_{sh,cap}$ is 56.26 Ω with $\sigma_{R_{sh,cap}} =$ 0.43 Ω and a transfer length $l_t = 1.76$ μm.

For what concerns recessed TLM structures, R_{tot} was plotted as a function of the recess length l_g and the channel sheet resistance was computed from the slope of the weighted linear regression of the points. Looking at room temperature results, $R_{sh,ch}$ for the different gate-source distances l_{gs} resulted to be very similar, with $R_{sh,ch}$ ranging from 191.74 Ω to 196.21 Ω with R^2=1 showing an incredibly accurate linear regression. The graph in figure 4.6c shows half of the access resistances as a function of the gate-source distance l_{gd}. Here a slightly lower value of R^2 can be observed with a resulting barrier resistance of $R_b = 111.55$ Ω μm and $\sigma_{R_b} =$ 7.3 Ω μm.

Figure 4.7 shows the measurements performed at 4K. Even in this case, R_{tot} increases linearly with l_{sd} and the bar of the standard deviation is not really visible

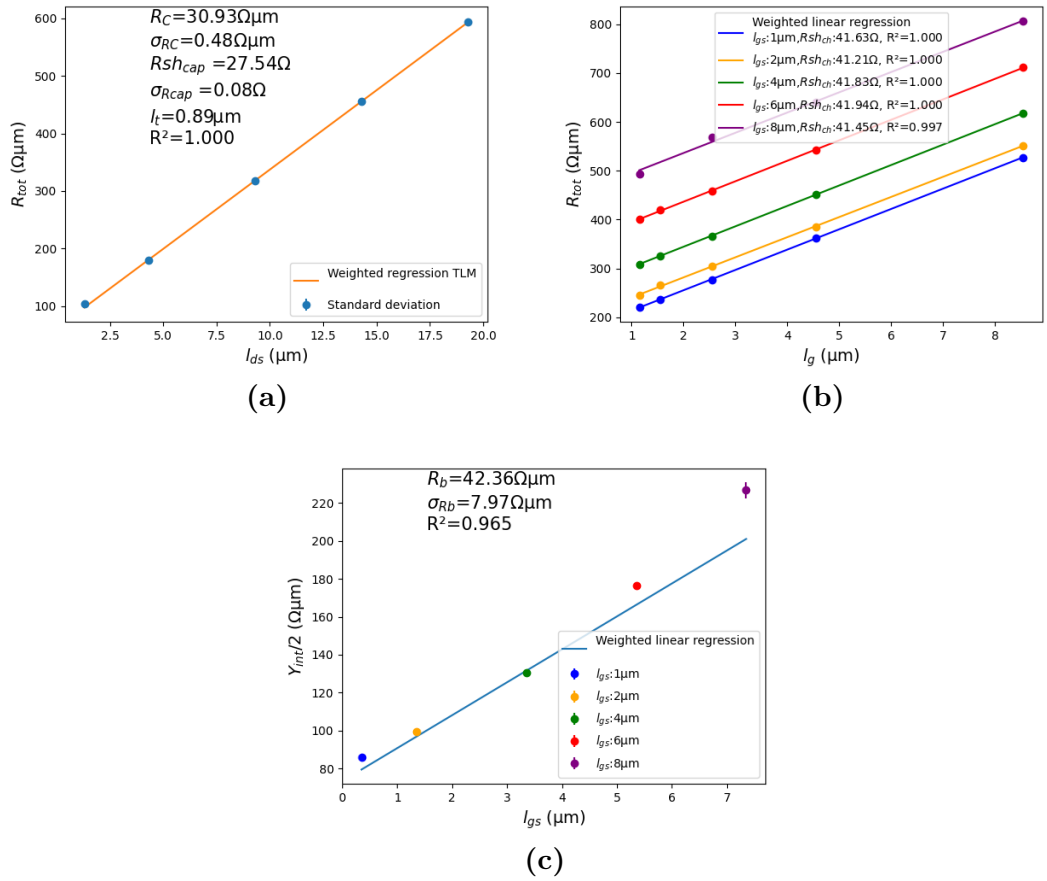


Figure 4.7: Resistive parameters extraction for EpiB-1nm at 4K

meaning that the measurements are highly reproducible. Surprisingly, R_C does not seem to vary with the decrease of the temperature; in the following sections, this phenomenon will be discussed. The cap sheet resistance instead shows a significant decrease as expected due to the decrease of the phonon scattering at cryogenic regime [24] with values ranging between 4.21 Ω and 41.94 Ω. Channel sheet resistance results are even more stable, with a lower variation as a function of l_{gs} with respect to the room temperature case. However this can be due to a reduced number of measured structures at cryogenic regime. Barrier resistance shows a decrease with $R_b = 42.26\,\Omega\,\mu m$ and $\sigma_{R_b} = 7.9\,\Omega\,\mu m$. This can be due to an enhanced conductivity of the diffused metal within the barrier layer [5] due to the alloyed contacts as discussed in section 2.1.1.

4.2.2 HEMTs DC Charcterization

In this section results from the HEMT DC analysis will be discussed taking as a reference one of the fabricated devices. In this case $L_g = 100\,\text{nm}$ and $w = 10\,\mu\text{m}$ from epiA with nickel thickness of 2nm will be discussed. Results will be reported for both RT and 4 K.

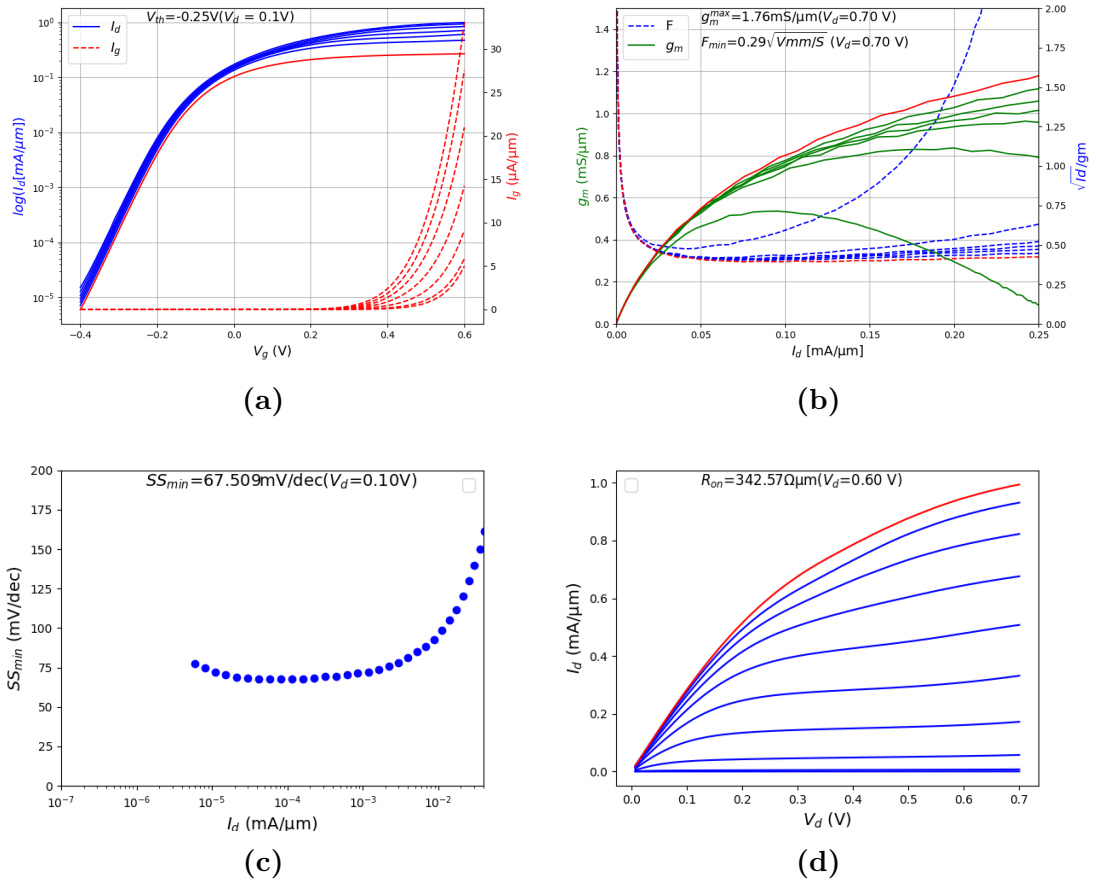


Figure 4.8: HEMTs DC characterization for EpiA-2nm $L_g = 100\,\text{nm}$, $w = 10\,\mu\text{m}$ at RT

In figure 4.8a the drain current I_d in logarithmic scale as a function of V_{gs} is shown for different drain voltages. The device shows the typical behavior explained in section 3.3.3. Gate current I_g is very small reaching values on the order of μA/μm even at high voltages. This is important for good device performance since I_g represents a source of leakage. For what concerns 4 K measurements ,an overall improvement of I_g can be observed in figure 4.9a which is reduced by a factor of 10 with respect to RT results. I_d is increased instead resulting in an overall improved

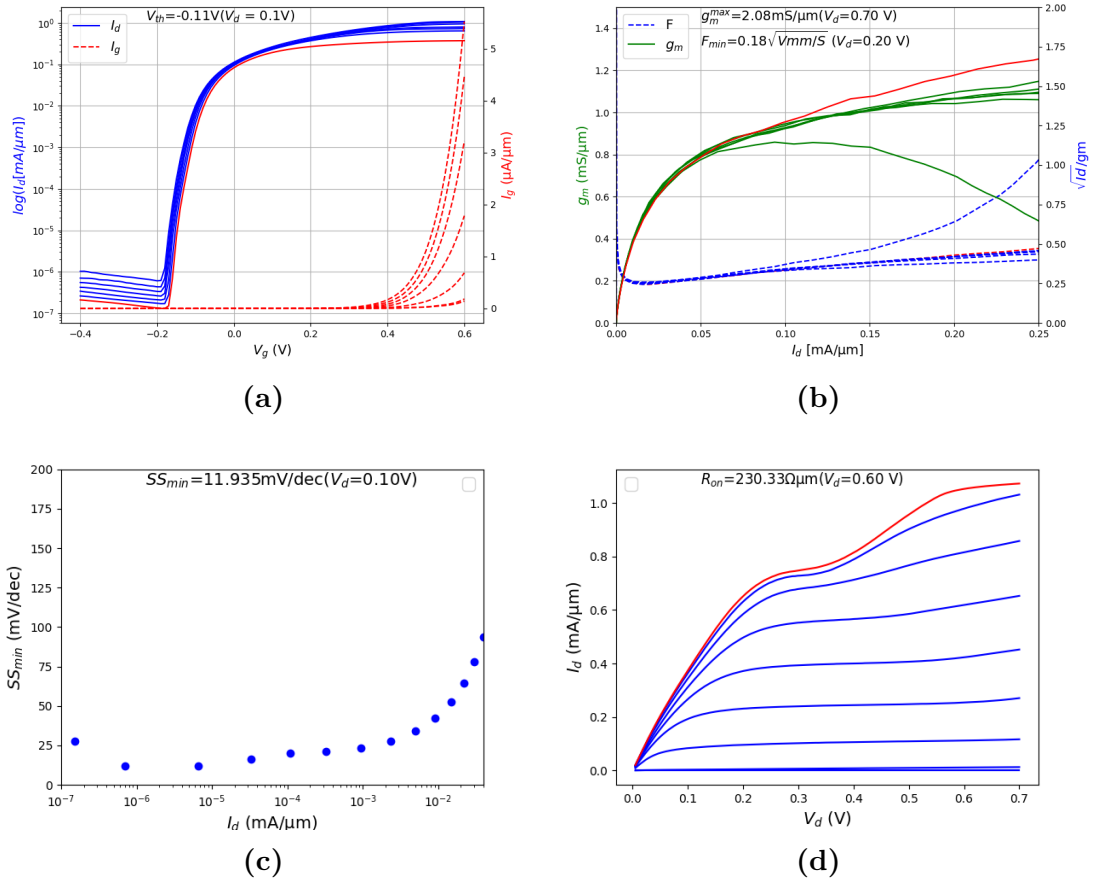


Figure 4.9: HEMTs DC characterization for EpiA-2nm $L_g = 100\,\text{nm}$, $w = 10\,\mu\text{m}$ at 4 K

behavior. The threshold voltage is extracted using the constant current method at $V_d = 0.1\,\text{V}$ and an increase at cryogenic regime can be observed.

In figure 4.8b transconductance g_m and noise indication factor F are shown as a function of I_d. As expected an overall improvement of the performances is observed at 4 K as shown in figure 4.9b. The increased I_d at cryogenic regime over the same V_{gs} swing can explain the increase of g_m. This is then linked to a reduction of F as shown in equation 3.10. The curves that register the best g_m and F are highlighted in red.

The Subthreshold Swing is shown in figure 4.8c and 4.9c. The SS at $V_d = 0.1\,\text{V}$ is extracted as a function of I_d (in logarithmic scale). As expected a significant decrease of the SS can be observed at 4 K leading to an improved switching behavior of the device due to the increased ratio g_m/I_d as shown from equation 3.12.

Finally, figures 4.8d and 4.9d show the output curves of the device both at RT and 4 K. R_{on} was extracted by taking the minimal resistance of the output curves between all the V_g values applied. A significant reduction of the R_{on} can be observed at 4 K due to a steeper slope in the linear region. This behavior was expected since a higher I_d is observed at cryogenic regime. A kink effect can be observed, attributed to traps in the channel as discussed in section 3.3.3.

4.2.3 Influence of nickel thickness and epitaxial structure

Resistive components extracted from the transfer length method and the HEMTs performances for different Ni thicknesses of the ohmic contact were compared, since EpiA-3nm was realized in two different samples showing similar results, just the structure fabricated in SA1 is considered in the following.

Looking at figure 4.10a the contact resistance in the different fabricated structures is shown at both RT and 4 K.

As concerns epiA, both the temperature regimes show a similar trend of the contact resistance: decreasing the Ni thickness the contact resistance decreases, remaining almost stable with thicknesses lower than 3 nm. At room temperature R_C ranges between 70.49 Ω µm to 23.14 Ω µm considering the whole range of thicknesses while it remains included between 23.1 Ω µm and 27.8 Ω µm for thicknesses below 3 nm. Decreasing the temperature to 4 K the contact resistance follows the same trend, however the resistance values result slightly higher with respect to the room temperature measurements probably due to the dominant thermionic emission conduction mechanism that leads to a fewer thermally excited electrons able to cross the barrier [24]. As concerns epiB instead, the contact resistance does not seem to vary much either as a function of the Ni thickness, or as a function of the temperature. The resistance ranges between 24.6 Ω µm and 31.95 Ω µm showing a big improvement at 4 K with respect to epiA for higher Ni thicknesses (for 6 nm Ni the contact resistance results more the halved with respect to epiA). The absence of a temperature dependence may be due to the different epitaxial structure used. The δ-doping in the cap layer may increase the doping enhancing the tunneling mechanism over the thermionic emission making the conduction less dependent on the temperature.

In figures 4.10b and 4.10c the variation of $R_{sh,cap}$ and $R_{sh,ch}$ is shown. Results do not show significant differences over the considered structures. The sheet resistances of both the cap and channel layers significantly decrease at low temperatures. This reduction is primarily due to the suppression of phonon scattering, which is the dominant factor affecting the resistivity in highly doped semiconductors [39].

In figure 4.10d the barrier resistance can be observed for all the fabricated metal stacks. As expected a decrease in the barrier resistance at cryogenic regime is shown, due to the improved electrical conductivity of the diffused Ni within the

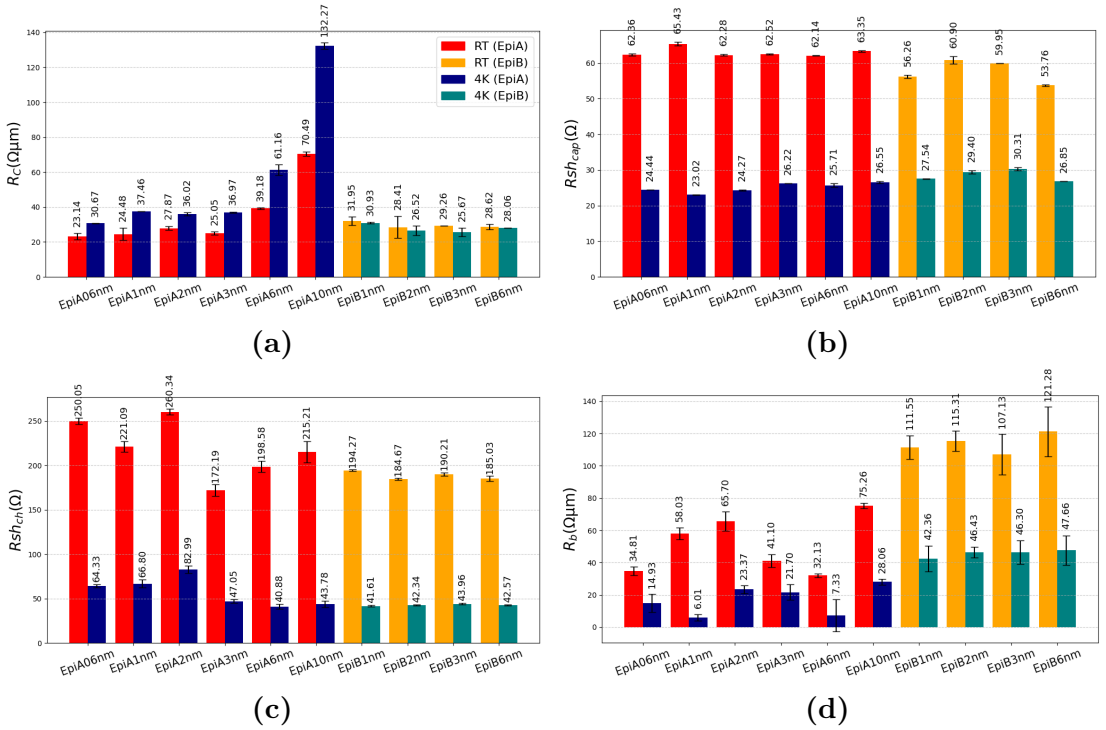


Figure 4.10: Resistive components variation among the fabricated devices

barrier layer [5]. Observing the results, not real trend can be observed for this parameter when varying the metal stack, especially for epiA thus no significant discussions can be made with these results. This can be attributed to errors in the extraction of barrier resistance: linear dependence was considered between R_a and l_{gs}, however if $l_{t,b}$ is comparable to l_{gs} the linear model is no longer correct and a saturation of the total resistance can be observed. The usage of a linear dependence can lead to an underestimation of the extracted parameter [28].

Since the extraction of the single resistive components is not enough to evaluate the performance of the devices, a more accurate comparison can be made by evaluating the DC characterizations. That is why the transfer curves and output curves of all the fabricated devices were measured. In the following, a comparison between all the meaningful parameters extracted from all the different fabricated devices at fixed gate length and device width can be found. The analysis refers to devices with $L_g = 40\,\text{nm}$ and $w = 10\,\mu\text{m}$.

In figure 4.11a the trend of the threshold voltage in all the different devices is shown. The devices are normally on and a negative gate voltage is applied to turn off or pinch-off the device. For epiB, the barrier thickness is 4 nm, thinner with respect to epiA, this means that the gate is closer to the channel and a less negative voltage is needed to turn off the device. The difference in barrier thickness

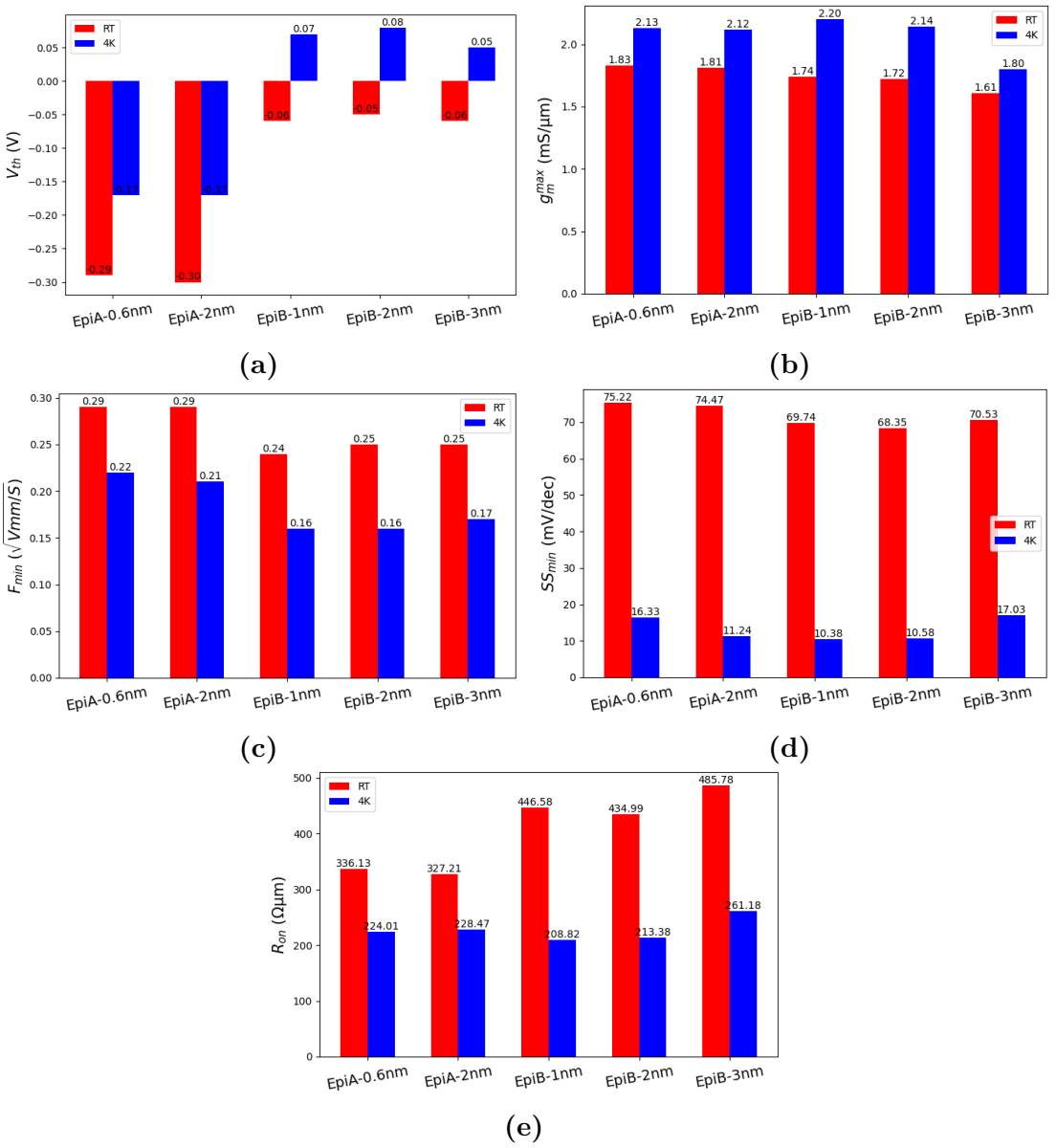


Figure 4.11: Variation of HEMTs metrics among the fabricated devices for $L_g = 40\,\text{nm}$ and $w = 10\,\mu\text{m}$

lead to the difference in V_{th} between the two epi.

Figure 4.11b shows the maximum transconductance of the considered devices. As expected, performances are worsened at RT. No significant differences can be seen for the two different epitaxial structures, however it is interesting to observe that while at RT devices fabricated with epiA show a higher g_m^{max} with respect to

epiB, for cryogenic regime this trend is reversed. Furthermore, observing the F behavior in figure 4.11c it is possible to conclude that epiB seems to offer the best cryogenic performances. Indeed surprisingly low values can be observed reaching $F_{min} = 0.16\sqrt{\text{Vmm/S}}$. Looking at both g_m^{max} and F_{min} a slight improvement of the performance for lower Ni thicknesses can be observed.

Looking at figure 4.11d it is possible to observe the SS_{min} behavior over different fabricated devices. The overall performances are really similar to each other with a significant reduction in SS at cryogenic regime.

Finally in figure 4.11e the on-state resistance is observed. As discussed for the g_m^{max} results, even in this case better performances at room temperature are attributed to epiA while the trend is reversed at 4 K.

4.2.4 Influence of gate length on HEMTs performances

In this section, the key parameters affecting HEMT performance, extracted from DC characterization, are compared. The goal is to analyze how these parameters vary as a function of L_g while keeping the device width constant. At this purpose $w = 10\,\mu\text{m}$ was chosen.

In figure 4.12a the trend of the threshold voltage as a function of the gate length is shown. A slight decrease of the threshold voltage at lower gate length is appreciable. This can be connected to short channel effects that reduce the gate control on the channel. A reduced channel length can cause high electric fields under the gate thus phenomena like band banding that can facilitate electron tunneling in the drain region decreasing V_{th}[40]. The variation of g_m^{max} is observed in figure 4.12b. As expected the transconductance shows the highest values for lower gate length due to an increased drain current density. In figure 4.12c it is possible to observe F_{min} trend, which slightly increases as a function of the gate length for epiB, this can be attributed to the inverse dependence with g_m. EpiA instead shows a stable behavior. The transconductance trend is also linked to the SS_{min} one showed in figure 4.12d, the subthreshold swing is significantly reduced at higher gate length. Finally, the R_{on} can be observed in figure 4.12e. In this case a clear trend with respect to the gate length is not observed.

At this point it is important to analyze if these trends are kept constant at cryogenic regime.

Looking at figures 4.13a, 4.13b, 4.13d and 4.13e it is possible to notice the same trend reported for RT measurements. It is important to underline that the maximum transconductance values reported have been extracted from the curve $V_d = 0.5\,\text{V}$ and not for the maximum V_d supplied. This is due to the fact that for EpiB-3nm at high V_d, a sudden increase of the drain current was observed which caused peaks in the g_m plot. This phenomenon can be attributed to electron-hole pair generation due to impact ionization, to which high indium-content devices

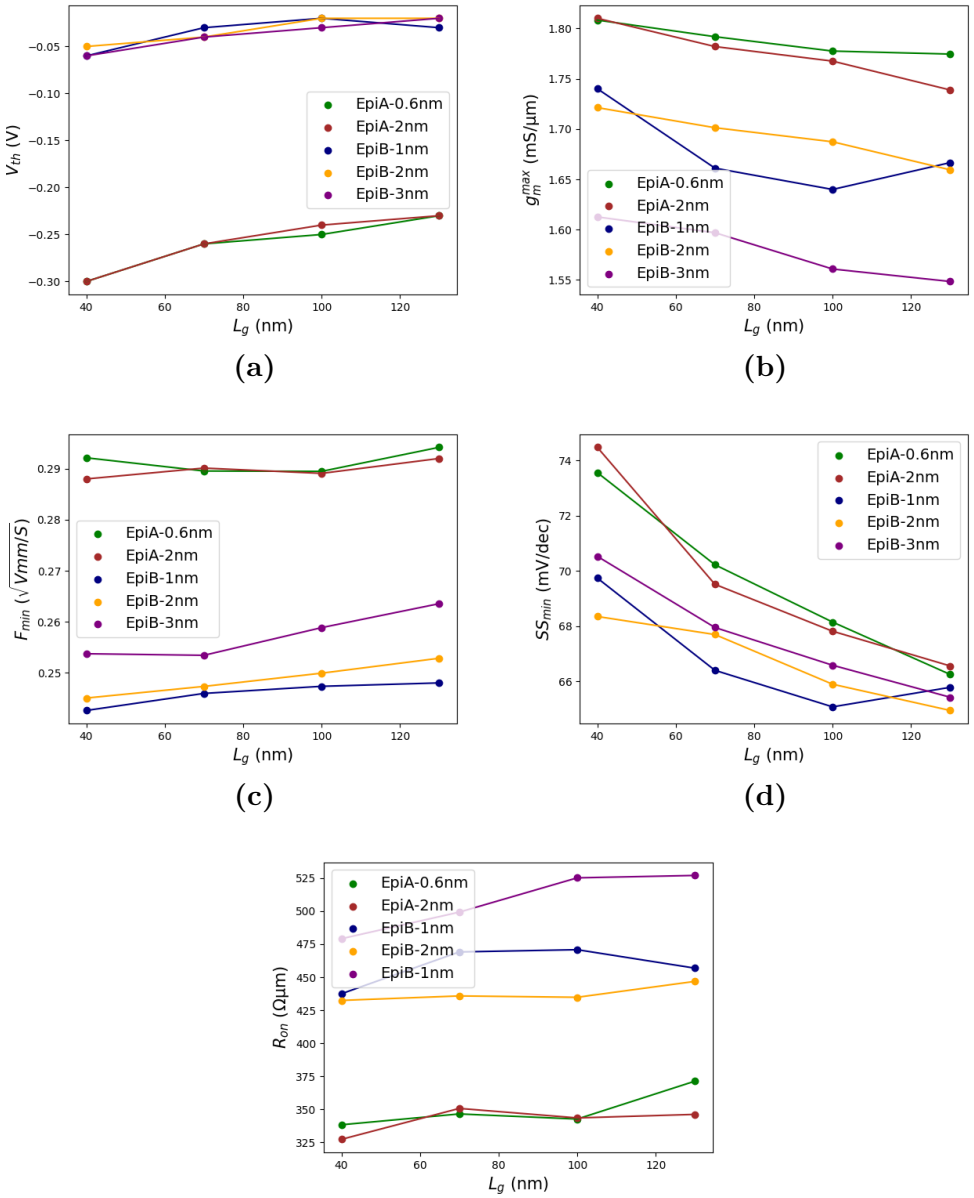


Figure 4.12: Dependence of HEMTs metrics on gate length for $w = 10\,\mu m$ at RT

are highly subjected for high V_d [41]. Since the comparison just makes sense for the same drain voltage, all the maximum values of the transconductance where extracted from $V_d = 0.5\,V$ curves. The only parameter that shows a different trend at 4 K with respect to RT measurement is F_{min} as shown in figure 4.13c. This

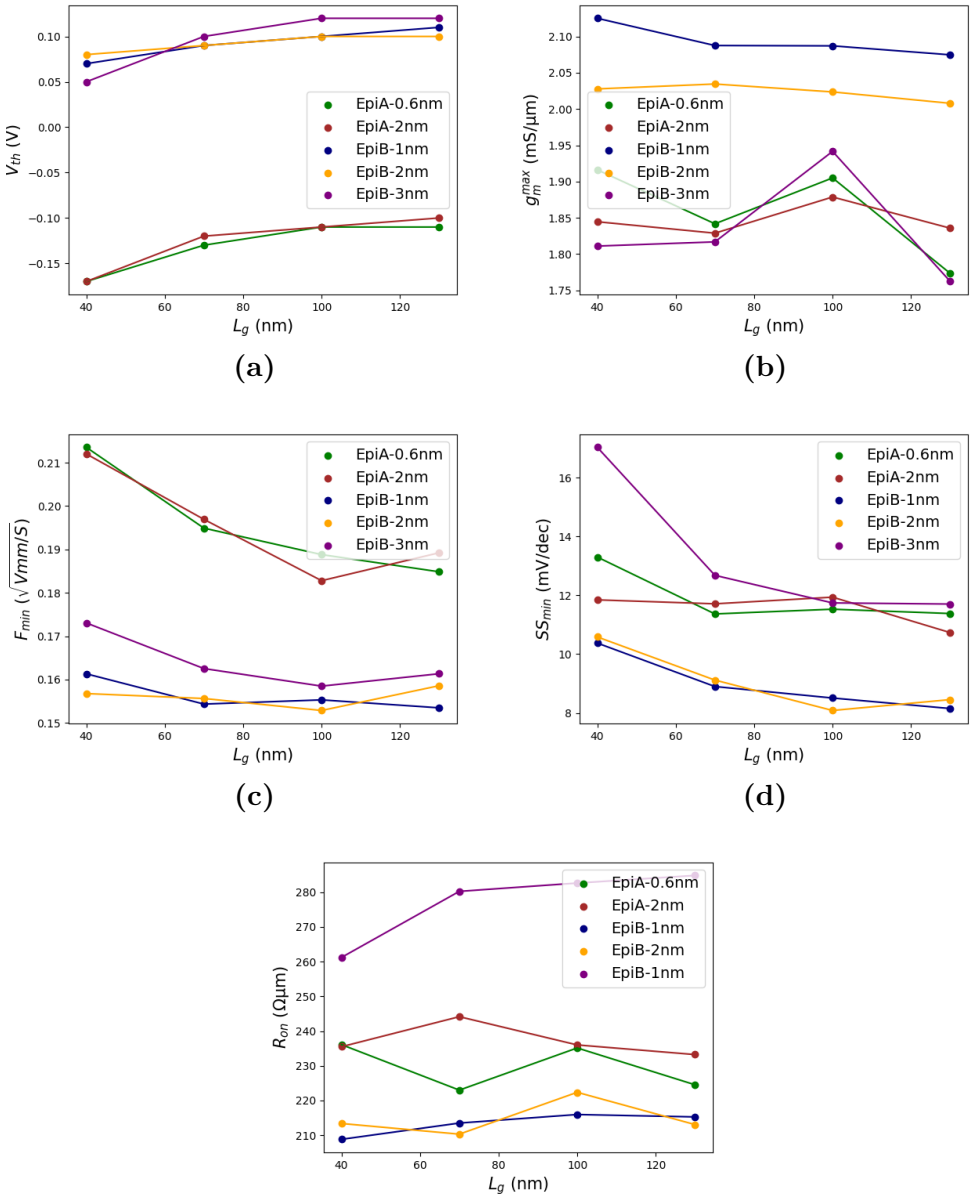


Figure 4.13: Dependence of HEMTs metrics on gate length for $w = 10\,\mu m$ at $4\,K$

can be due to the reduction of scattering events so an enhanced probability of quasi-ballistic transport for short channel devices at low temperature which makes $\sqrt{I_d}$ grow faster than g_m with a resulting decrease of the noise indication factor at higher gate lengths.

4.2.5 Influence of device width on HEMTs performances

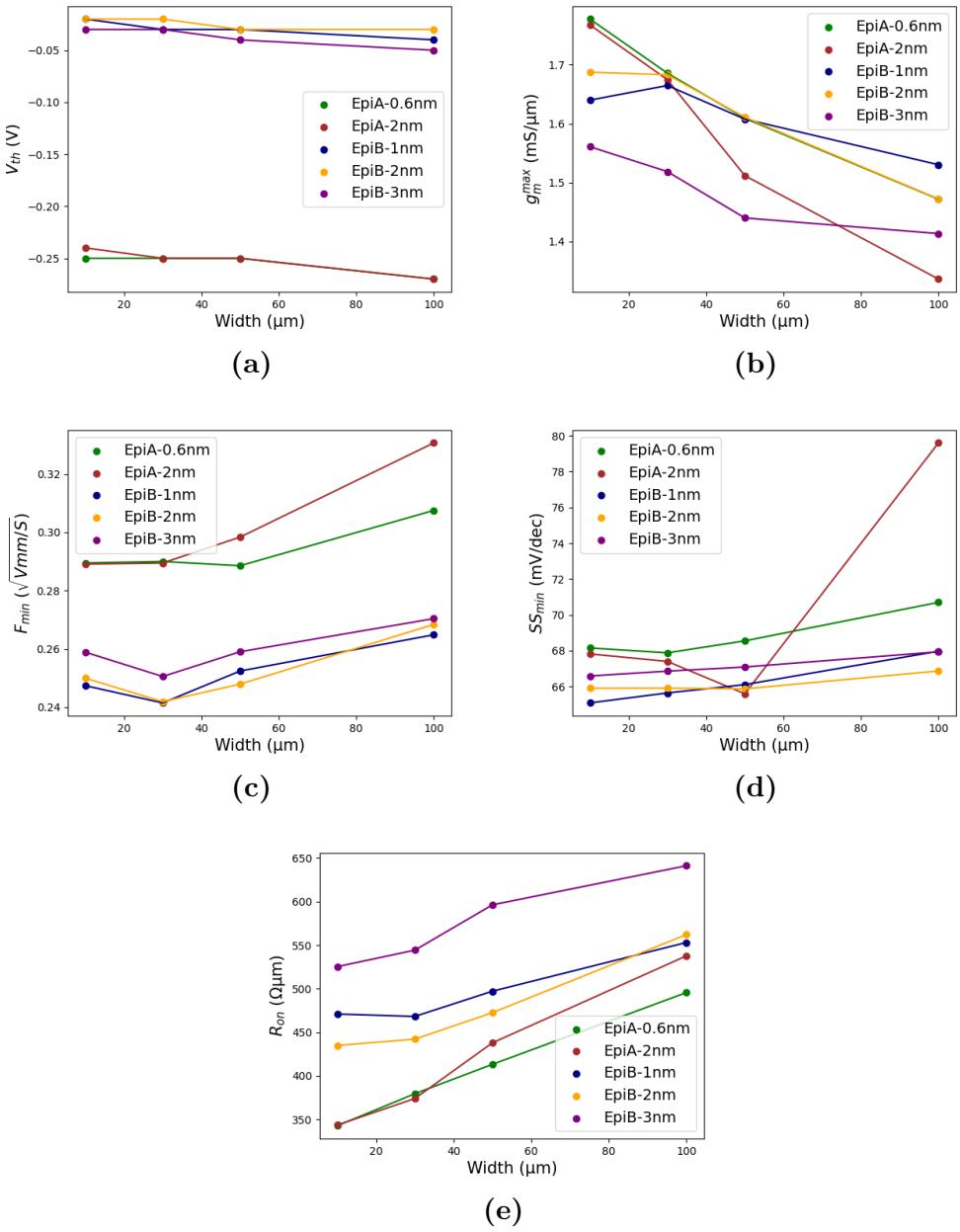


Figure 4.14: Dependence of HEMTs metrics on device width for $L_g = 40\,\text{nm}$ at RT

In this section, the dependence of HEMT performance on the device width is

analyzed. In figures 4.14a, 4.14b, 4.14c,4.14d and 4.14e the trends for a fixed gate length of 100 nm can be observed. The parameters analyzed were normalized by the device width, so there should theoretically be no direct dependence on the width. However, this is not the case, probably because the normalization was based on the design width, while the actual measured width was not considered. To better understand the width dependence of these parameters, further research is needed, such as analyzing the resistive parasitic component as the width varies. This could be considered the foundation for future studies.

4.2.6 Comparison with previous works

In this section the best results recorded in the present work are compared with cryogenic InGaAs HEMTs with cryo-optimized ohmic contacts by Cha et al. (2023)[5] and optimized indium channel contents by Cha et al.(2024) [6] investigated in IBM which represent the to-date record for cryo-optimized contacts.

	$R_C(\Omega\,\mu m)$
IBM 2023	30.6
IBM 2024	33
EpiB-1nm	30.9
EpiB-2nm	26.5

Table 4.1: Contact resistance comparison with to-date records at 4 K

	$R_{on}(\Omega\,\mu m)$
IBM 2023	290
IBM 2024	198
EpiB-1nm	215
EpiB-2nm	213

Table 4.2: On-resistance comparison with to-date records at 4 K

Results shown in table 4.1 reveal a record cryogenic contact resistance for 2 nm Ni thickness. As concerns HEMTs, on-state resistance was considered since it well summarizes the DC performances of the devices. Results shown in table 4.2 refer to gate length $L_g = 130$ nm with the exception of [6] (2024) whose gate length considered is $L_g = 170$ nm. The present work shows a smaller on-state resistance with respect to cryo-optimized contacts (2023), with really close performances to to-date record results.

Chapter 5

Conclusion and outlook

This work investigated the impact of nickel thickness variation in ohmic contacts on the cryogenic performance of InGaAs HEMTs. The goal was to analyze how different Ni thicknesses influence parasitic resistances and overall device performance at both RT and 4 K. To achieve this, TLM structures and HEMTs were designed, fabricated, and characterized, a statistical evaluation of the results was carried out. Five different samples and ten different stacks were fabricated.

The findings revealed that Ni thickness has a significant impact on the contact resistance at cryogenic temperatures. Two different metal stacks were identified as optimal for achieving low-resistance ohmic contacts, minimizing parasitic contributions, and enhancing the DC characteristics of the fabricated devices. The study also confirmed that standard contact designs optimized for room temperature operation do not necessarily yield the best performance under cryogenic conditions.

These results contribute to a deeper understanding of metal-semiconductor interactions at cryogenic temperatures and provide valuable insights for the development of low-noise cryogenic HEMTs. Future research should focus on further refining ohmic contact designs, exploring more accurate models for the analysis of the barrier resistance in TLM structures. Addressing these open questions could lead to significant advancements in quantum computing.

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Appendix A

Appendix

A.1 TLM measurements

In this section TLM measurements for all the fabricated structures at both RT and 4 K are shown.

A.2 HEMTs DC characterization

In this section HEMTs DC characterization for $L_g = 40\,\text{nm}$ and $w = 10\,\mu\text{m}$ are shown at both RT and 4 K.

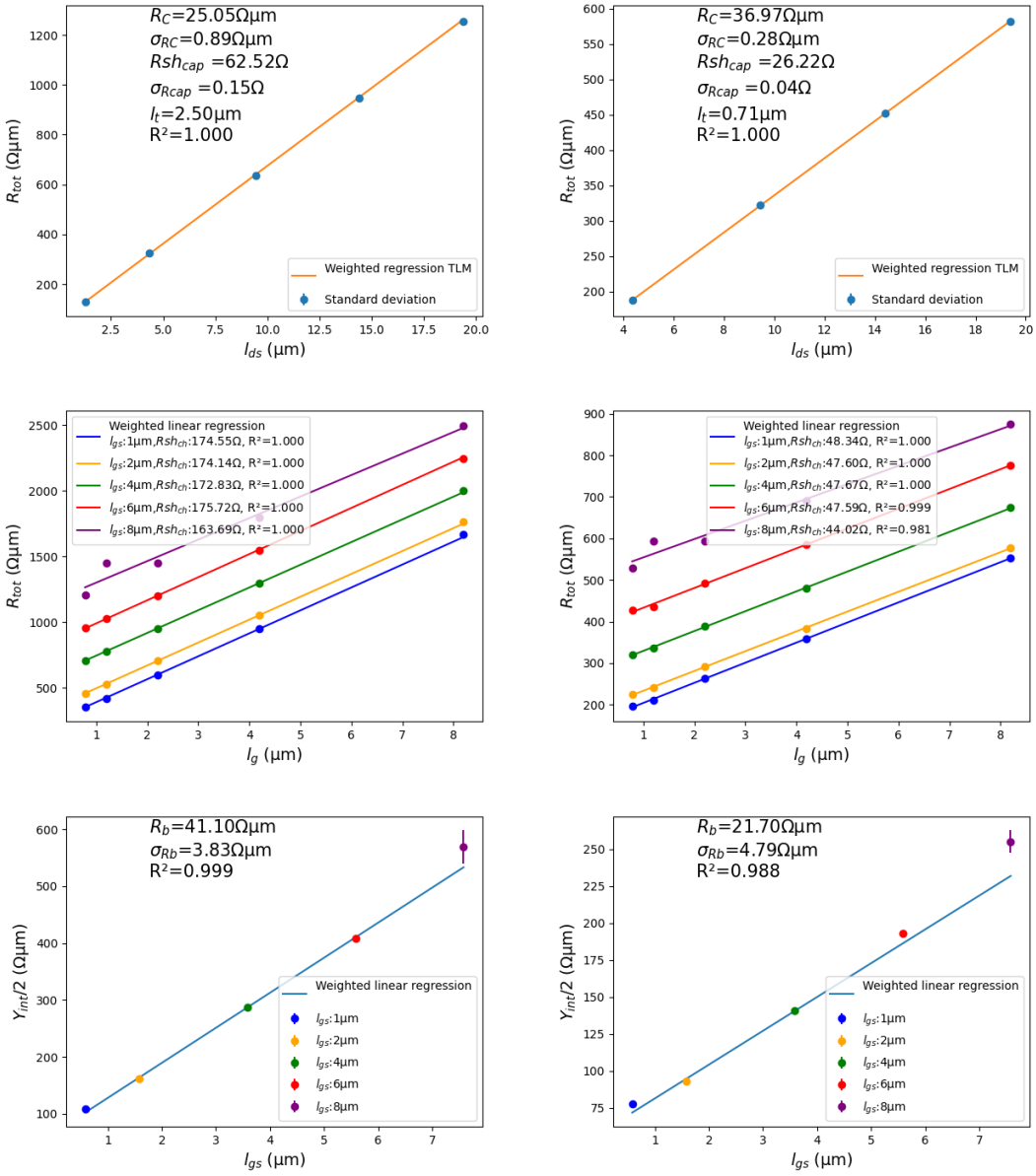

Figure A.1: TLM, sample *SA1*, *EpiA-3nm*, RT (left), 4 K (right)

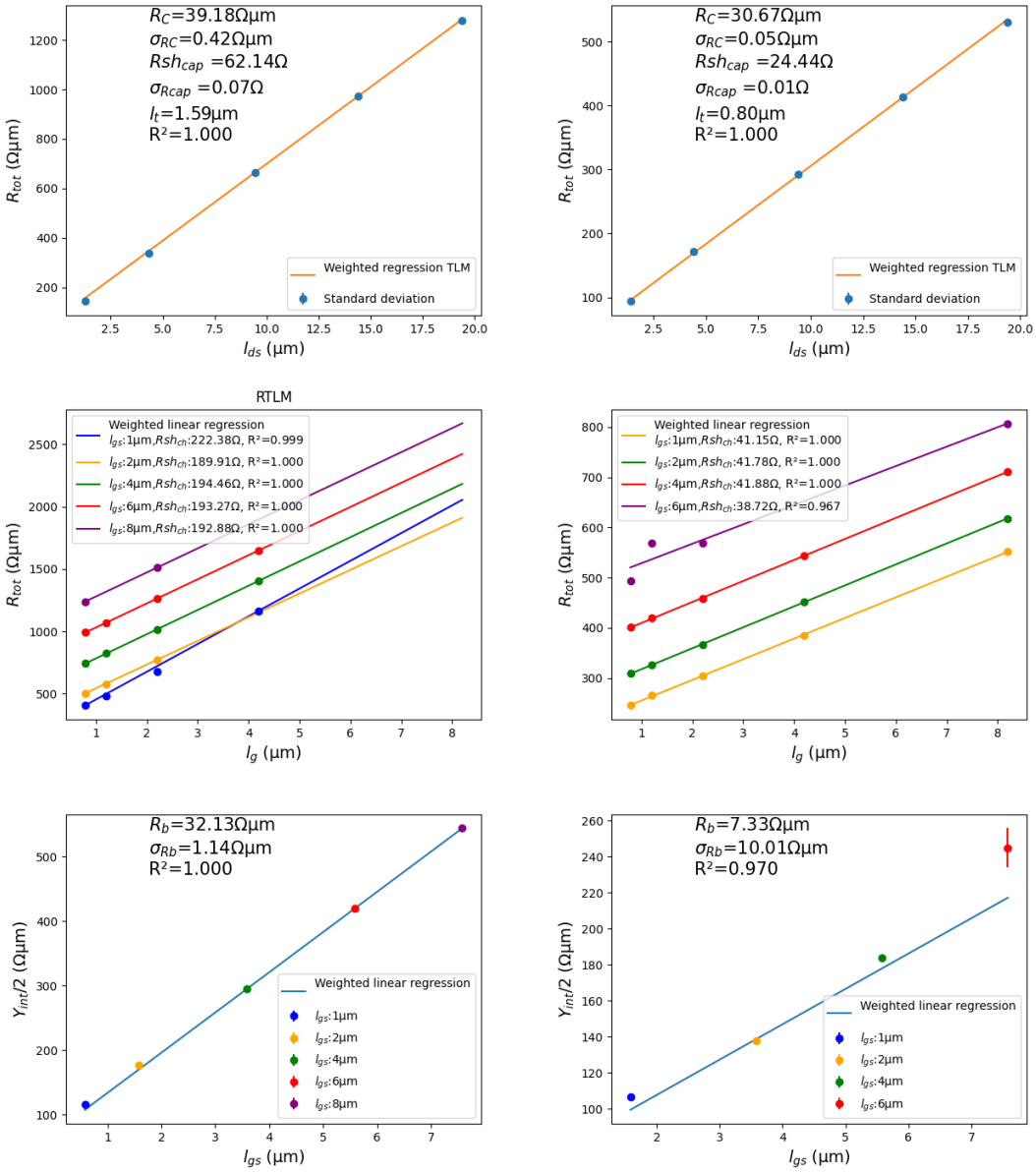

Figure A.2: TLM, sample *SA1*, *EpiA-6nm*, RT (left), 4 K (right)

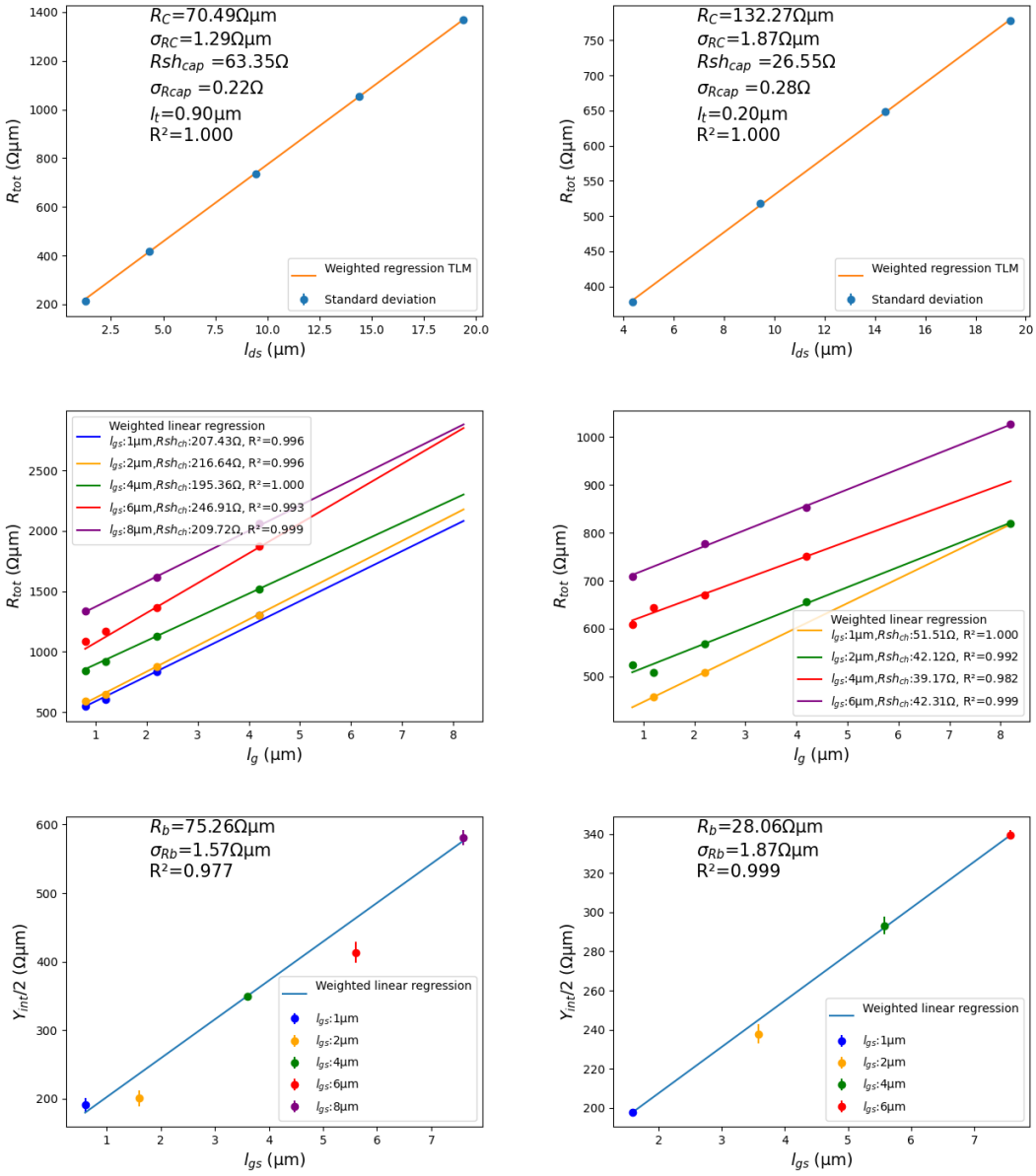

Figure A.3: TLM, sample *SA1*, *EpiA-10nm*, RT (left), 4 K (right)

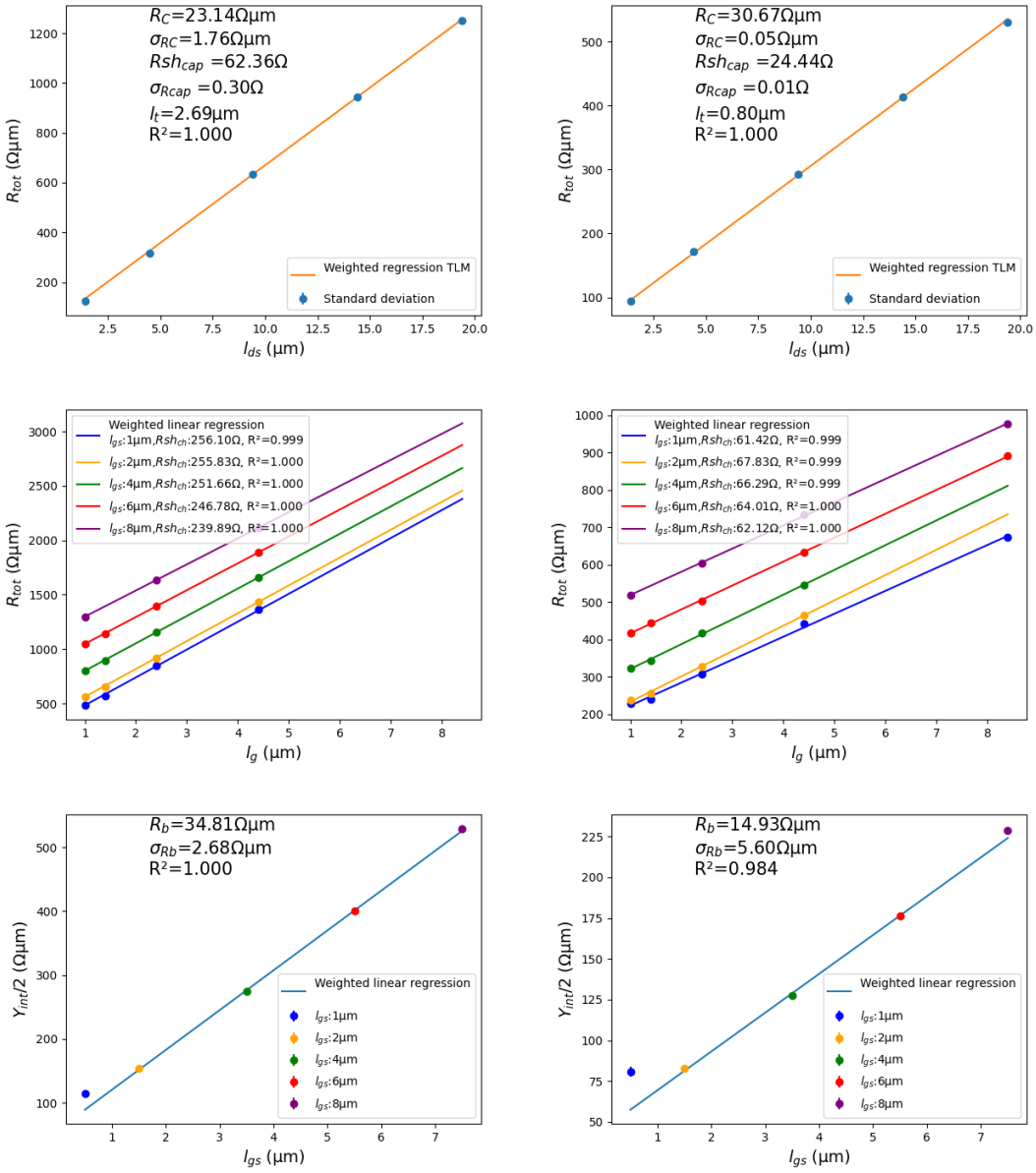

Figure A.4: TLM, sample *SA2*, *EpiA-0.6nm*, RT (left), 4 K (right)

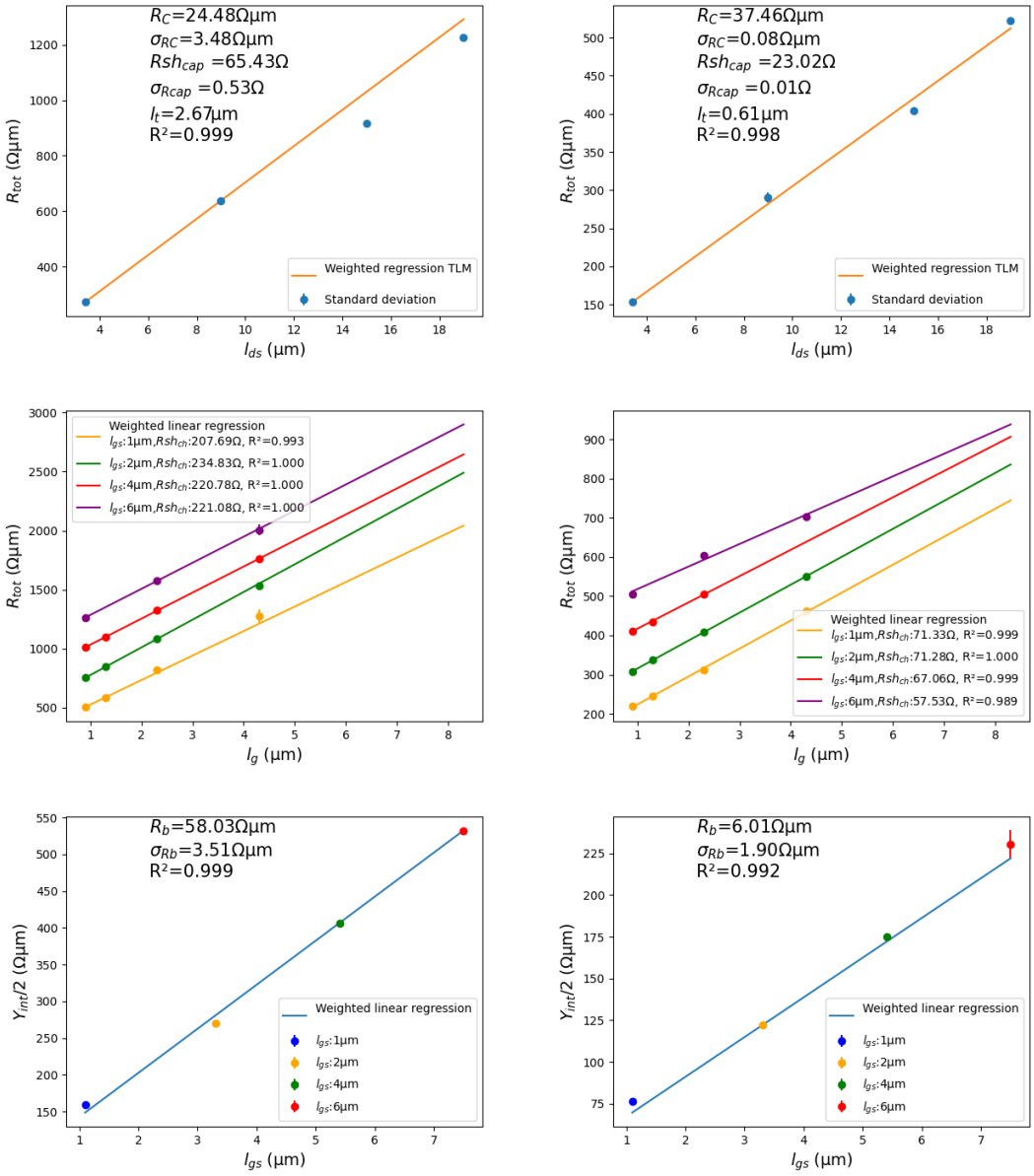

Figure A.5: TLM, sample *SA2*, *EpiA-1nm*, RT (left), 4 K (right)

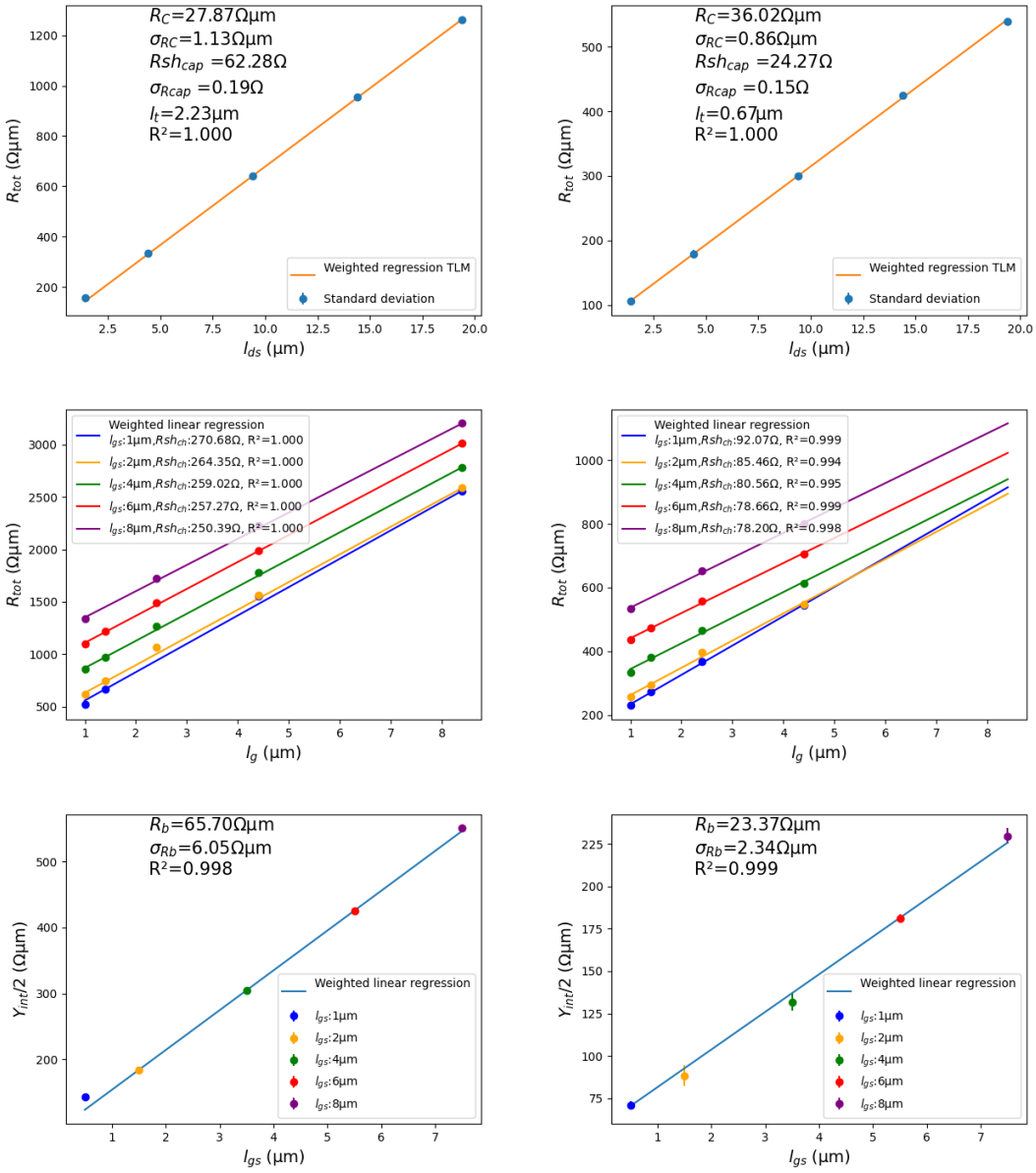

Figure A.6: TLM, sample *SA2*, *EpiA-2nm*, RT (left), 4 K (right)

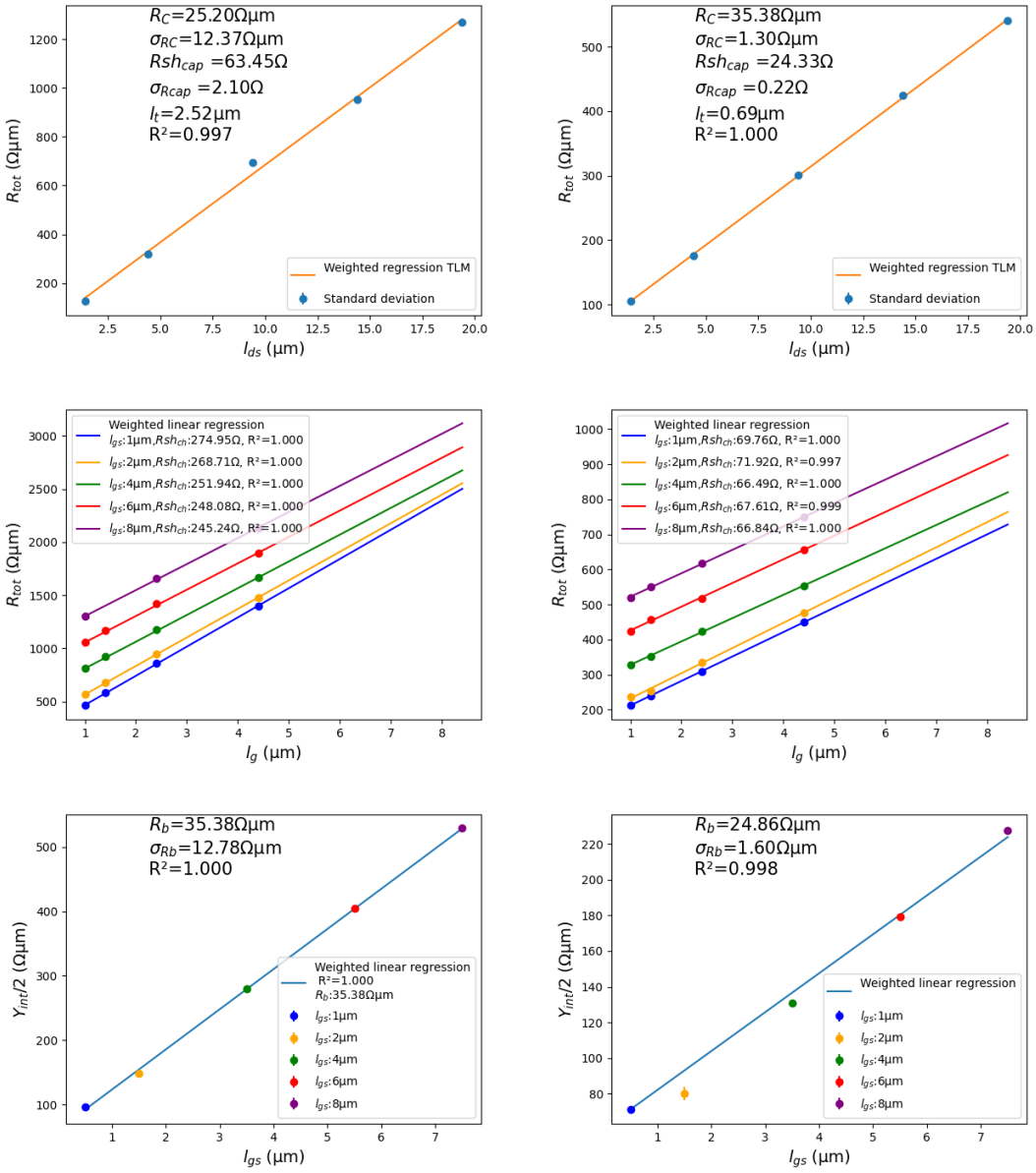

Figure A.7: TLM, sample *SA2*, *EpiA-3nm*, RT (left), 4 K (right)

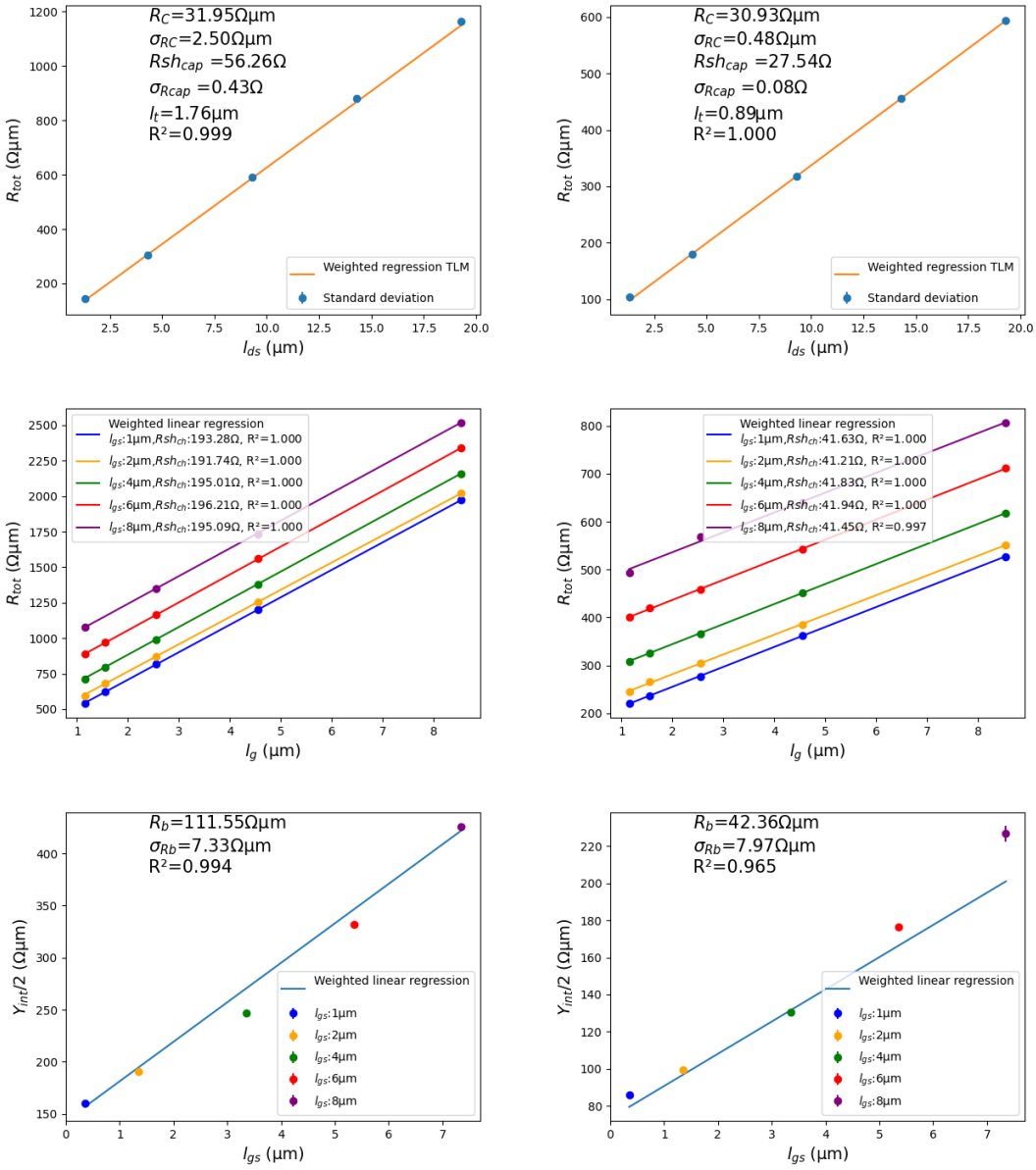

Figure A.8: TLM, sample *SB1*, *EpiB-1nm*, RT (left), 4 K (right)

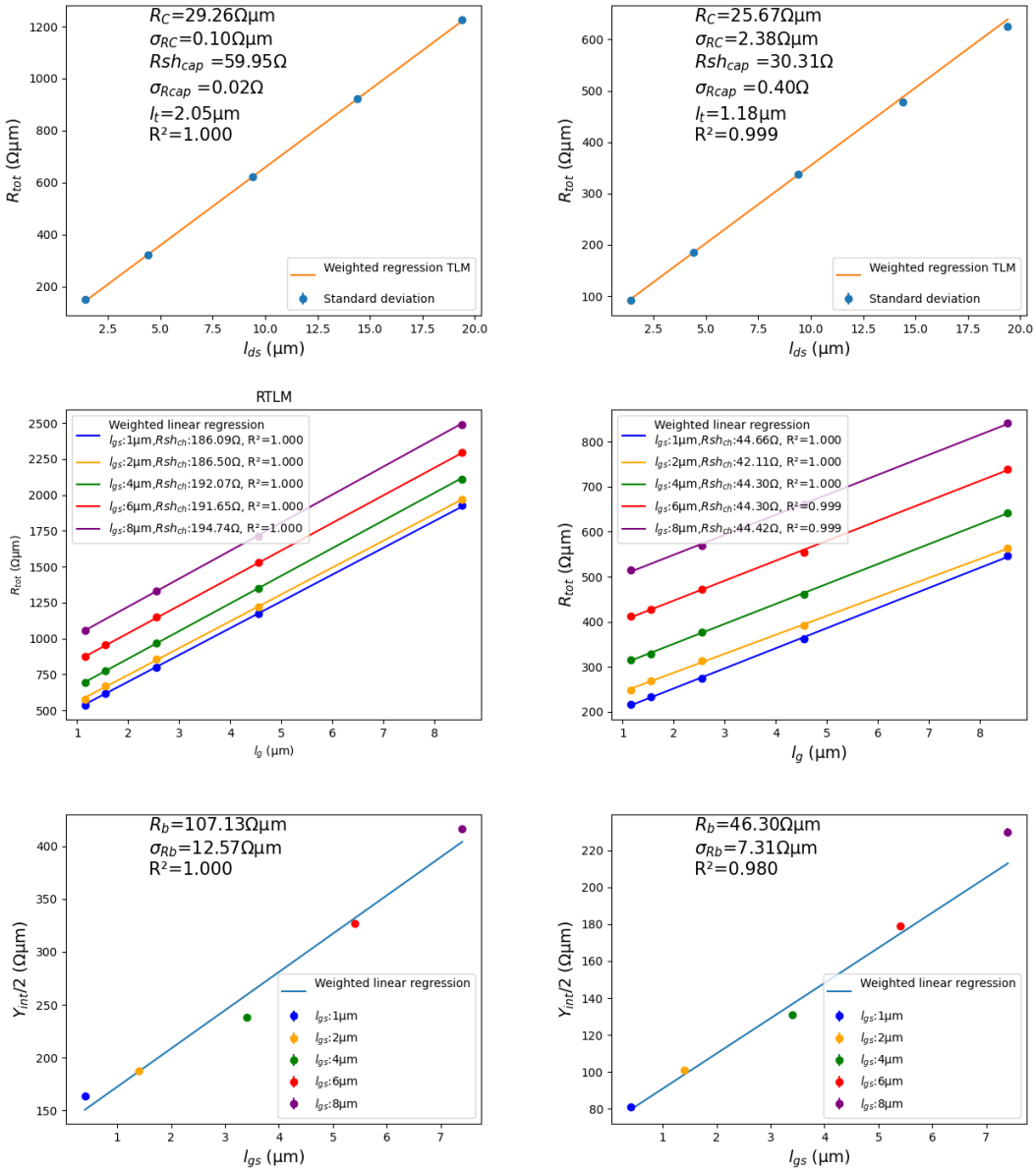

Figure A.9: TLM, sample *SB2*, *EpiB-3nm*, RT (left), 4 K (right)

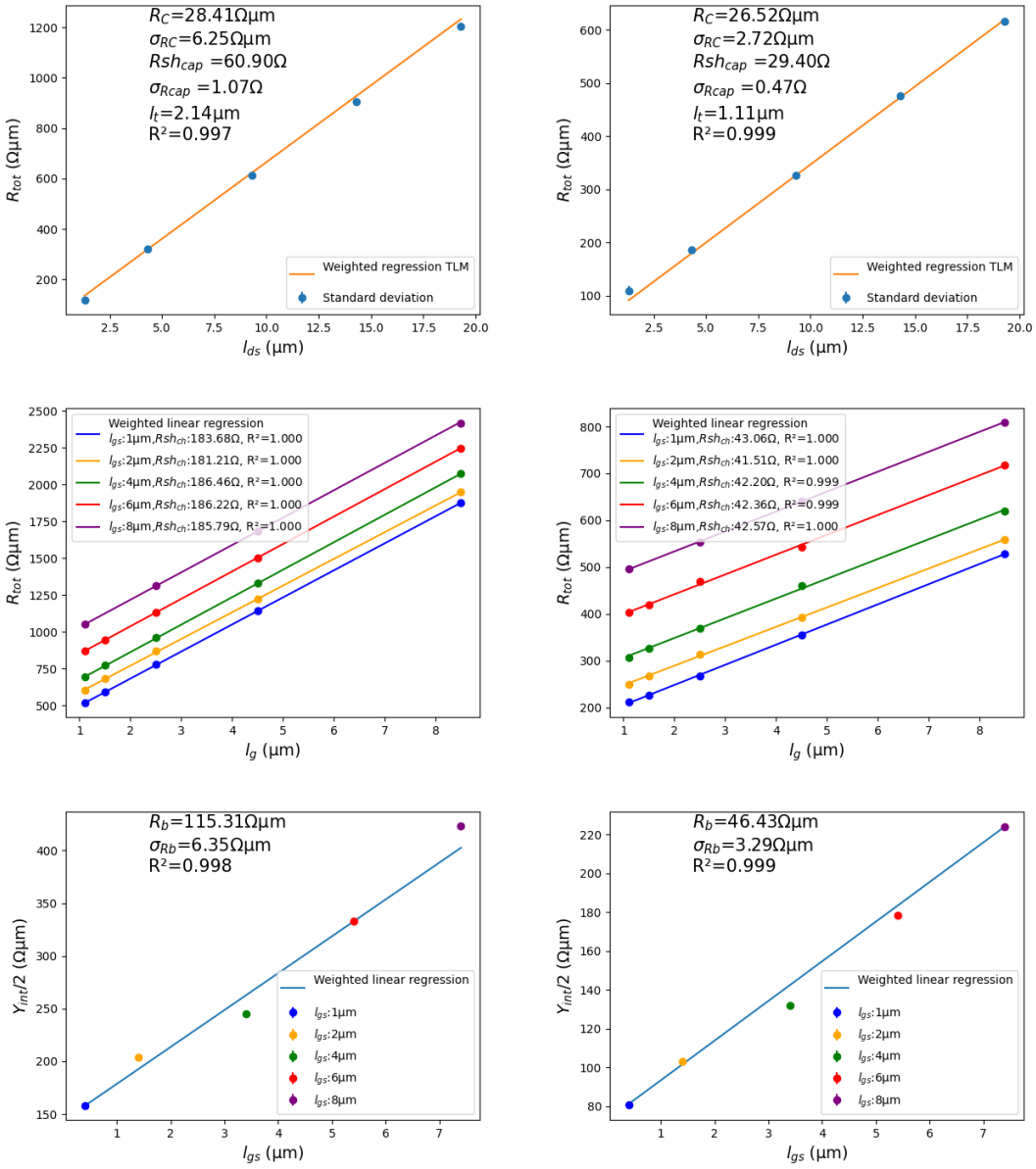

Figure A.10: TLM, sample *SB3*, *EpiB-2nm*, RT (left), 4 K (right)

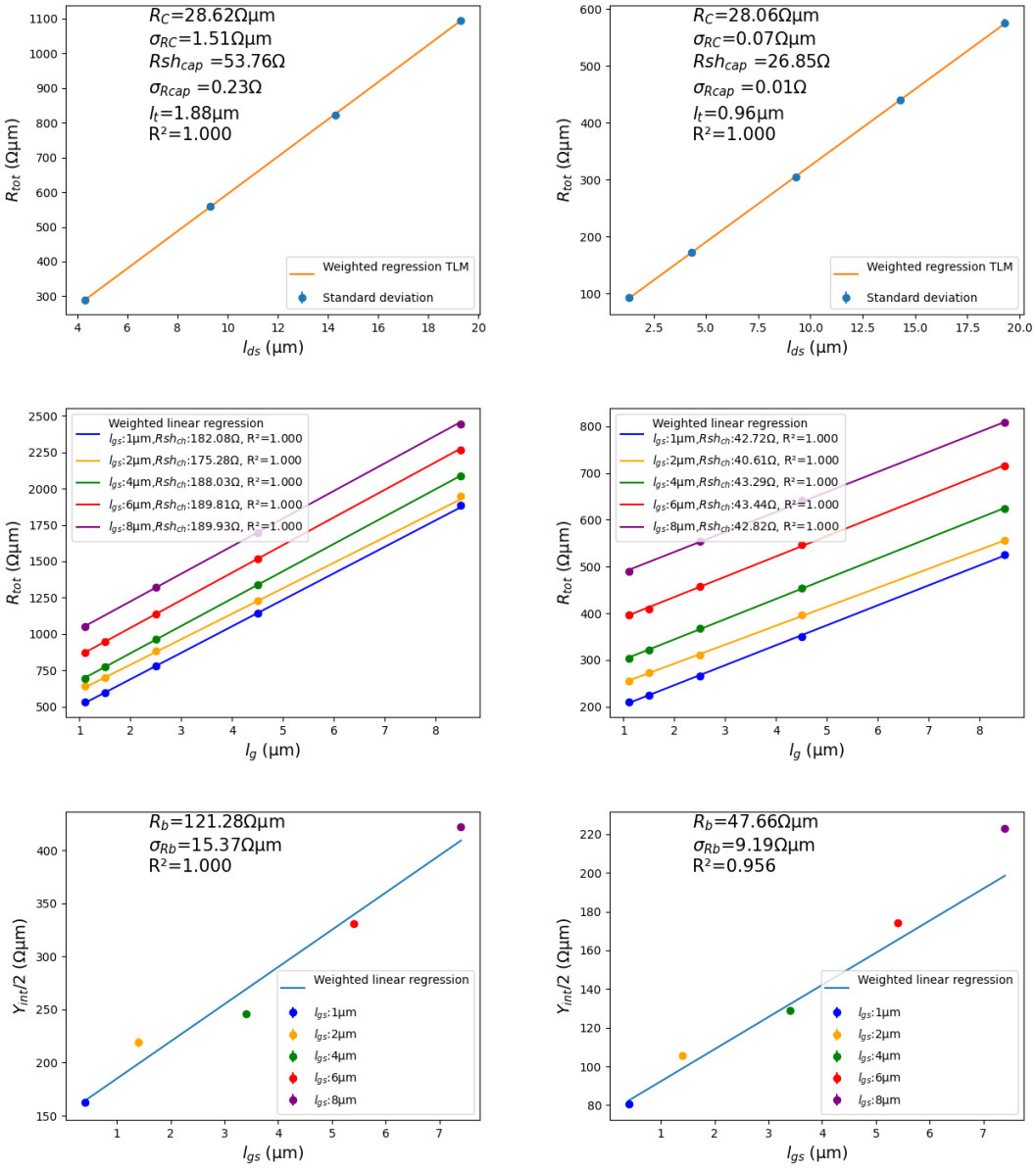

Figure A.11: TLM, sample *SB3*, *EpiB-6nm*, RT (left), 4 K (right)

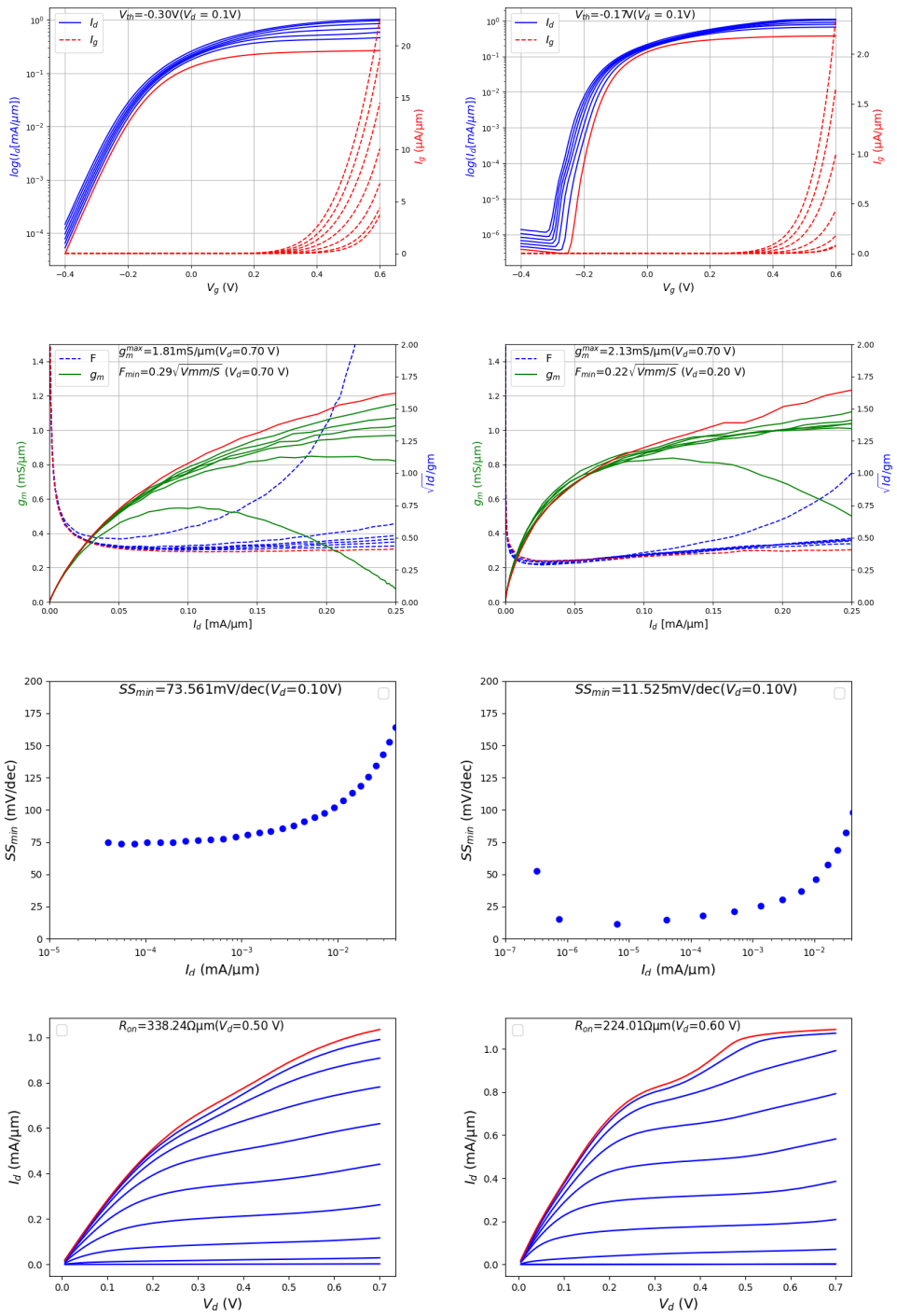

Figure A.12: HEMT DC: sample *SA2*, *EpiB-0.6nm*, for $L_g = 10\,\text{nm}$ and $w = 10\,\mu\text{m}$ at RT (left) and 4 K (right)

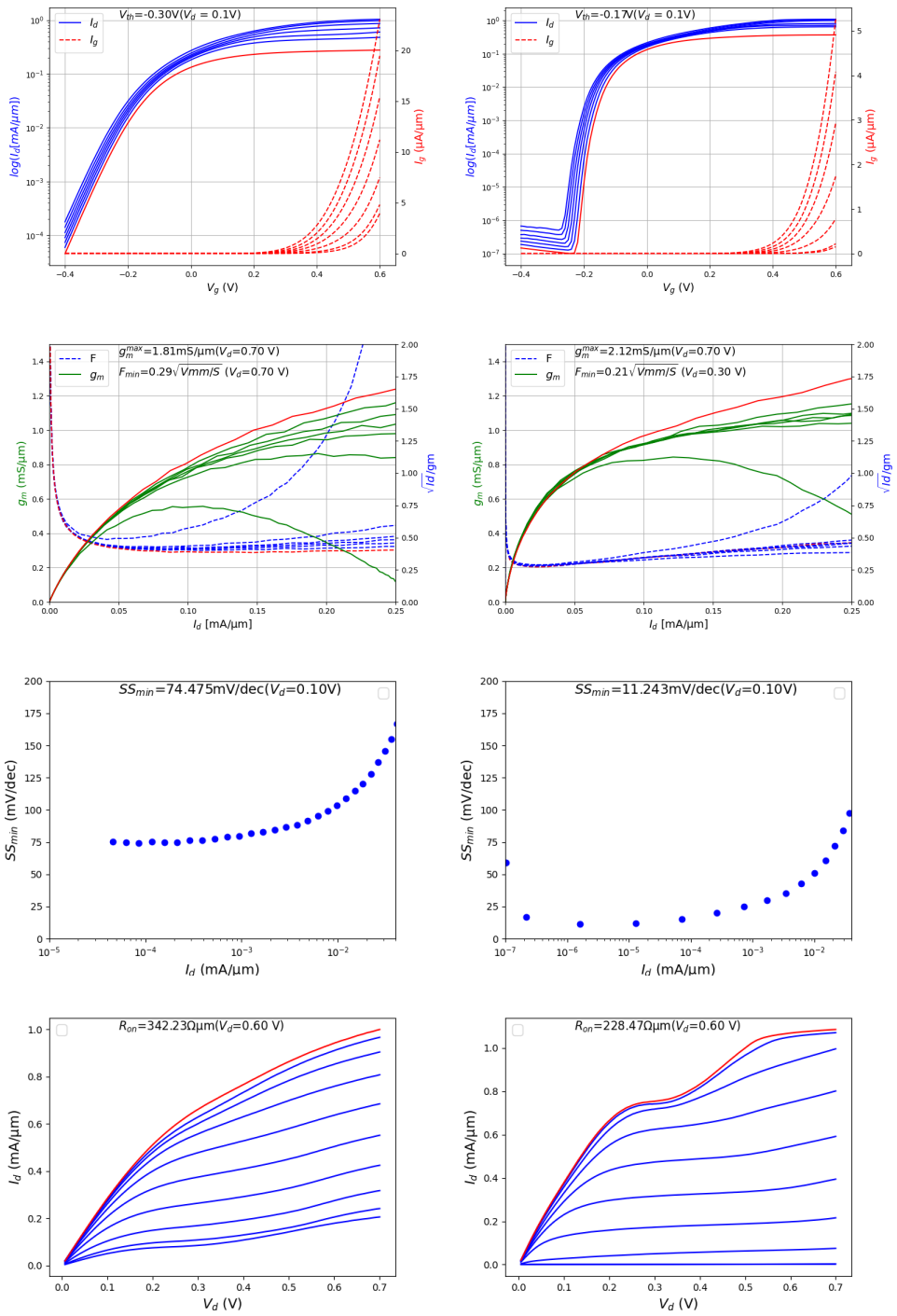

Figure A.13: HEMT DC: sample *SA2*, *EpiB-2nm*, for $L_g = 10\,\text{nm}$ and $w = 10\,\mu\text{m}$ at RT (left) and 4 K (right)

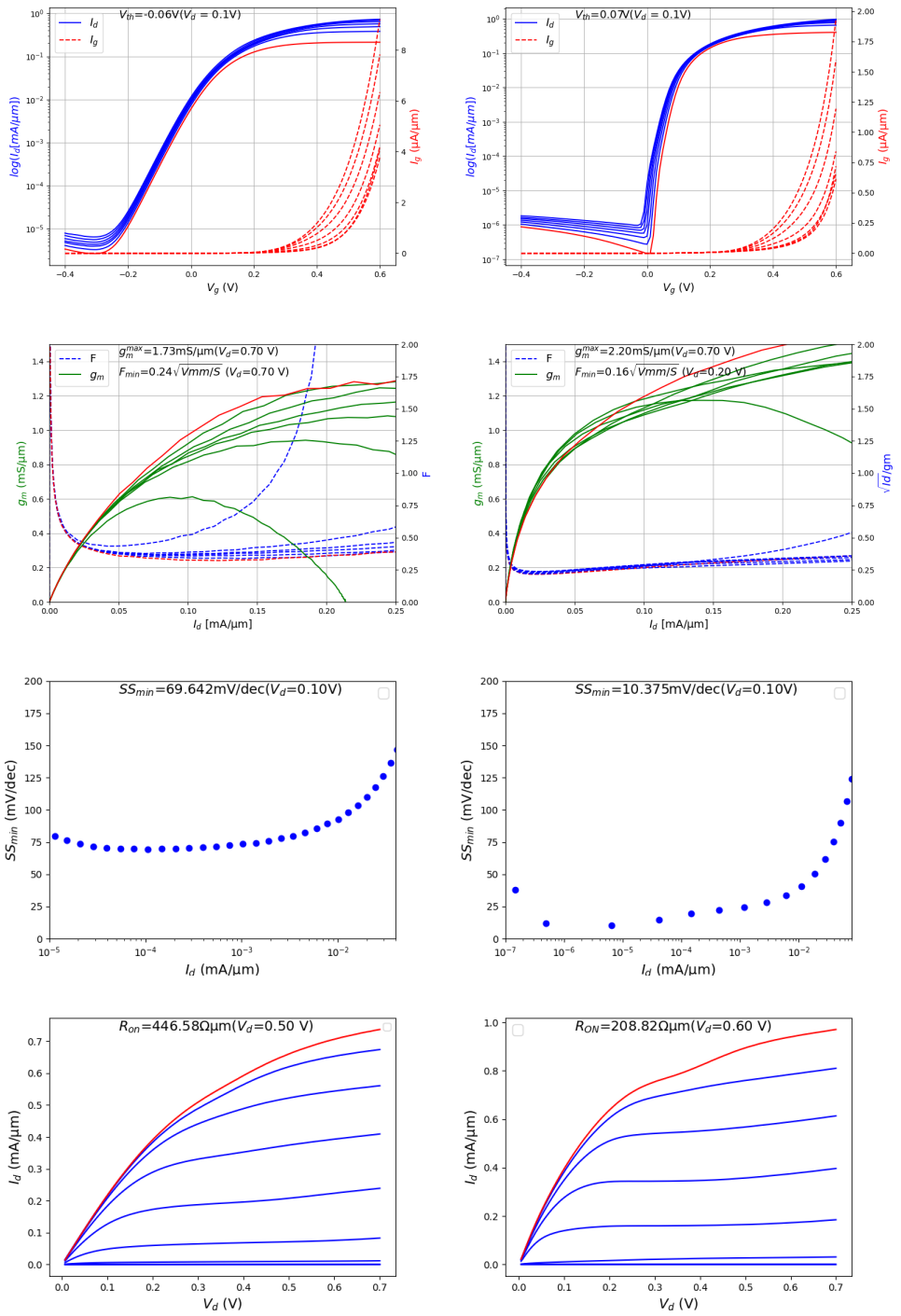

Figure A.14: HEMT DC: sample *SB1*, *EpiB-1nm*, for $L_g = 10\,\text{nm}$ and $w = 10\,\mu\text{m}$ at RT (left) and 4 K (right)

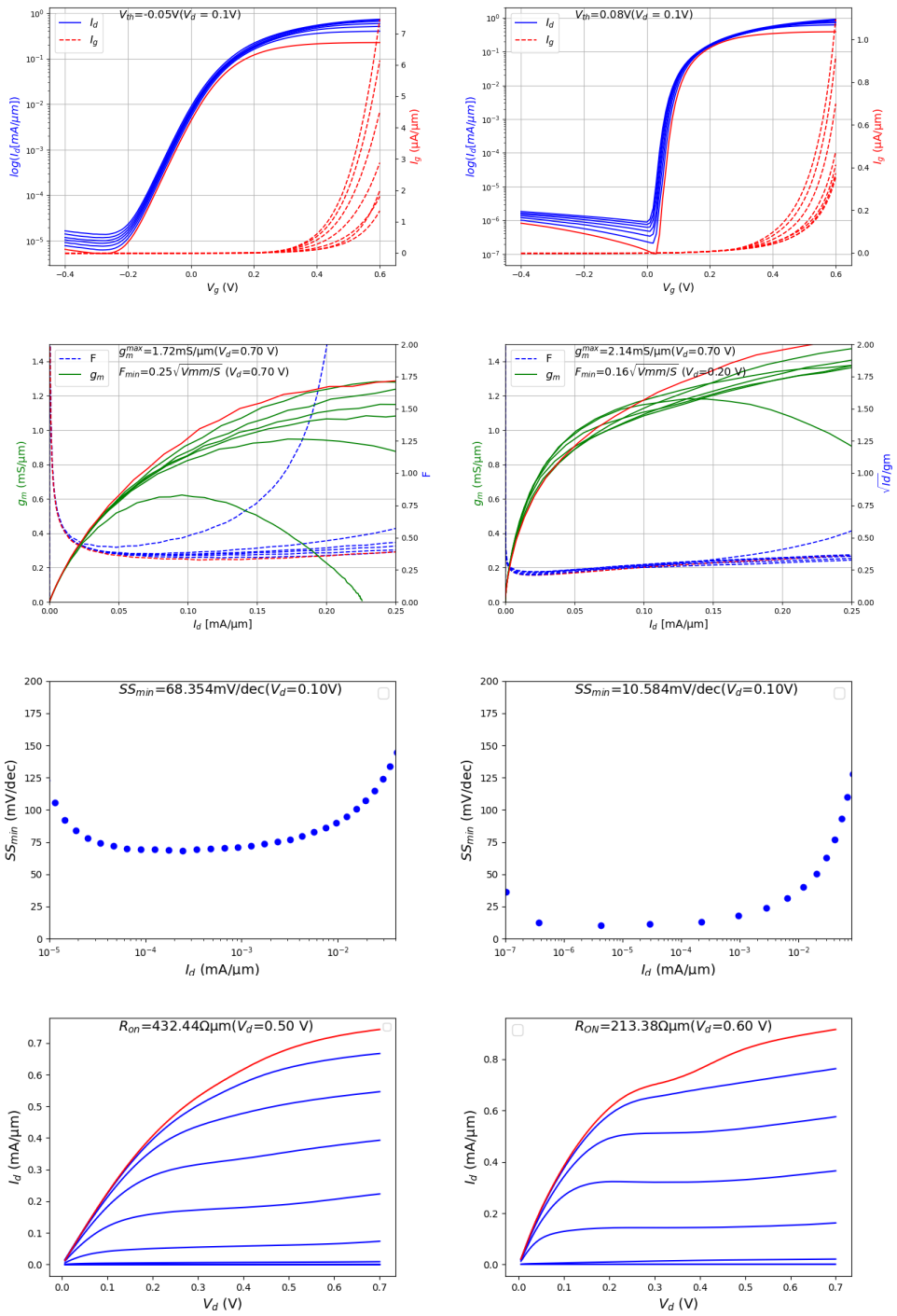

Figure A.15: HEMT DC: sample *SB3*, *EpiB-2nm*, for $L_g = 10\,\text{nm}$ and $w = 10\,\mu\text{m}$ at RT (left) and 4 K (right)

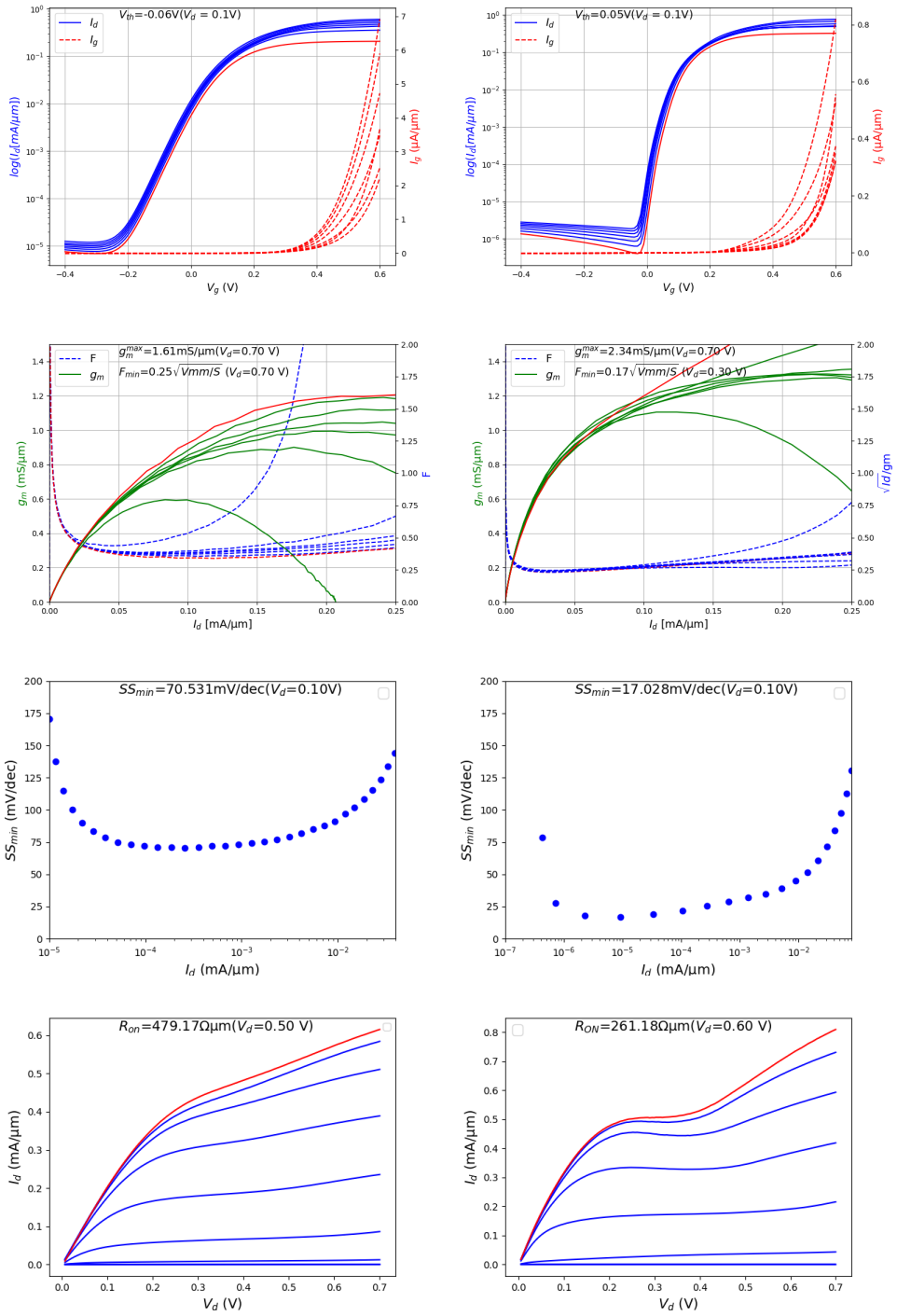

Figure A.16: HEMT DC: sample *SB2*, *EpiB-3nm*, for $L_g = 10\,\text{nm}$ and $w = 10\,\mu\text{m}$ at RT (left) and 4 K (right)