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Study and Development of a Control Loop Implementation for a Low-Power Capacitively Isolated DC-DC Converter

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Summary

This thesis continues the analysis of a Capacitively Isolated Low-Power DC-DC converter, building on previous work, by incorporating a control loop to regulate the output voltage under varying conditions and maximizing the system's performance. To achieve this, a comprehensive mathematical model is develop to better understand the system's behaviour and dynamics.

The operating point is carefully selected to optimize performance by exploiting the sub-harmonics in the gain curve and Partially Damped Oscillations (PDO). This approach significantly reduces switching losses and ensures Zero Voltage Switching (ZVS) across all operating points.

Various control strategies are presented, highlighting the advantages and disadvantages of each. The strategies include Frequency Modulation (FM) control, Pulse Width Modulation (PWM) control, Bang-bang control and Dyadic Pulse Modulation (DPM) control.

The system is designed as a consumer electronics power adapter, capable of delivering $50W$ of output power at a constant $20V$ output voltage with an efficiency greater than 85%.

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Table of Contents

List of Tables VIII

List of Figures IX

1 Introduction 1
1.1 Thesis objectives . . . 2

2 Scheme and Building blocks of a CPT converter 3
2.1 Building blocks of the converter . . . 3
2.1.1 Inverter . . . 3
2.1.2 Capacitive interface . . . 5
2.1.3 Compensating network . . . 6
2.1.4 Output rectifier . . . 8
2.1.5 Feedback . . . 8
2.2 Topology . . . 9
2.3 Specifications . . . 10

3 Mathematical model 12
3.1 Building blocks . . . 13
3.1.1 Half-bridge inverter . . . 13
3.1.2 Resonant tank . . . 14
3.1.3 Full-bridge rectifier . . . 16
3.1.4 Output filter . . . 16
3.1.5 Open Loop model . . . 19
3.2 Analysis of Damped Oscillations . . . 19
3.2.1 Quality factor . . . 21
3.3 Harmonics analysis . . . 21
3.4 Zero Voltage Switching analysis . . . 22

4 Selection of Operating Point 25
4.1 Selection of Parameters . . . 25

4.1.1 Interface capacitor . . . 25
4.1.2 Resistive load . . . 25
4.1.3 Compensating inductor . . . 26
4.2 Static characteristic . . . 28
4.2.1 Output voltage . . . 28
4.2.2 Varying Q factor . . . 32
4.2.3 Duty cycle variation . . . 33
4.2.4 Inductor current and capacitor voltage . . . 34
4.3 Spice simulations . . . 38
4.3.1 ZVS verification . . . 41
4.4 Ripple analysis . . . 43

5 Control strategies 45
5.1 Frequency modulation control . . . 46
5.1.1 Frequency range . . . 46
5.1.2 System dynamics . . . 47
5.1.3 PI controller . . . 48
5.1.4 Control formula . . . 49
5.1.5 Selection of controller parameters . . . 50
5.1.6 Simulations . . . 50
5.2 Pulse Width Modulation control . . . 53
5.2.1 Duty cycle range . . . 54
5.2.2 Control formula . . . 57
5.2.3 Simulations . . . 57
5.3 Bang-bang control . . . 59
5.3.1 Simulations . . . 61
5.4 Dyadic Pulse Modulation control . . . 63
5.4.1 Simulations . . . 66
5.5 Comparison . . . 68
5.5.1 Ripple . . . 68
5.5.2 Overshoot . . . 68
5.5.3 Settling time . . . 69

6 Selection of components and board design 70
6.1 Selection of components . . . 70
6.1.1 Half-bridge inverter . . . 70
6.1.2 Interface capacitors . . . 73
6.1.3 Inductor . . . 75
6.1.4 Full-bridge rectifier . . . 79
6.1.5 Input and output capacitor . . . 80
6.1.6 Feedback loop . . . 82

6.2 Board realization 83
6.2.1 Schematic 84
6.2.2 Board layout 85

7 Results 87
7.1 Setup 87
7.2 Open-loop measurements 88
7.2.1 Low voltage input 88
7.2.2 High voltage input 91

8 Conclusions 95
8.1 Future work 95

Bibliography 96

List of Tables

2.1 Comparison of inverter configurations 4
2.2 Comparison of compensating networks topologies 7
2.3 Circuit characteristics 10
2.4 Specifications 11

5.1 Comparison among the implemented control strategies. 69

6.1 Transistors requirements and characteristics. 73
6.2 Interface capacitor requirements and characteristics. 75
6.3 Italtras inductor requirements and characteristics. 78
6.4 Full-bridge rectifier requirements and characteristics. 80

List of Figures

2.1 Block diagram of the complete CPT system 3
2.2 (a) Half-bridge and (b) Full-bridge configuration 4
2.3 Switching node voltage for (a) Half-bridge and (b) Full-bridge configuration 5
2.4 Compensating networks: (a) L, (b) LC and (c) LCLC. 7
2.5 Full-bridge rectifier (a) Passive and (b) Active 8
2.6 Voltage mode control for a DC-DC converter 9
2.7 CPT circuit 10

3.1 Circuit schematic 12
3.2 Equivalent circuit 13
3.3 Building block of resonant tank 16
3.4 Building block of full-bridge rectifier 16
3.5 Output node 17
3.6 Building block of output filter 18
3.7 Output node with output capacitor's ESR 18
3.8 Building block of output filter considering C_{out}'s ESR 19
3.9 Open Loop model of CPT circuit 19

4.1 Output voltage as a function of the switching frequency, at $d = 50\%$, for different inductance values 27
4.2 V_{out} vs. f_{sw}, with $R = 8\Omega$, $L = 33\mu H$, $C = 15nF$ and $f_{res} = 320\,\text{kHz}$ 29
4.3 I_0 vs. f_{sw}, with $R = 8\Omega$, $L = 33\mu H$ and $C = 15nF$ 29
4.4 (a) Output voltage and (b) Initial inductor current zoomed-in at the selected frequencies 31
4.5 (a) Output voltage and (b) output current transient at $f_{sw} = 122kHz$ 32
4.6 V_{out} vs. f_{sw}, with $R > 20\Omega$, $L = 33\mu H$ and $C = 15nF$ 33
4.7 V_{out} vs. f_{sw} using (a) $d = 25\%$ and (b) $d = 33.3\%$ 34
4.8 $i_L(t)$ and $v_C(t)$ waveforms at $f_{sw} = 120$ kHz. Notice that the converter is operating in the PDO mode 35
4.9 $i_L(t)$ and $v_C(t)$ waveforms at $f_{sw} = 120$ kHz. CDO condition 36

4.10 Peak values of (a) i_L and (b) v_C vs. f_{sw} for different R values . . . 37
4.11 RMS values of (a) i_L and (b) v_C vs. f_{sw} for different R values . . . 38
4.12 Circuit schematic for simulation . . . 39
4.13 Output voltage transient from LTSpice . . . 40
4.14 $v_{sw}(t)$, $i_L(t)$ and $v_C(t)$ . . . 41
4.15 Hide-side FET $v_{DS}(t)$ and $v_{GS}(t)$ using (a) $t_{dead} = 100ns$, (b) $t_{dead} = 30ns$ and (c) $t_{dead} = 15ns$ . . . 42
4.16 Output voltage ripple as a function of C_{out} and ESR at $V_{out} = 20V$ with $V_{in} = 330V$, $f_{sw} = 122kHz$ and $R = 8\,\Omega$. . . . 43
4.17 Complete circuit with grid voltage input. . . . 44
4.18 Input voltage of the CPT circuit . . . 44

5.1 V_{out} vs. f_{sw}, varying load . . . 46
5.2 V_{out} transient for different f_{sw} . . . 47
5.3 V_{out} transient selected frequency range . . . 48
5.4 Block diagram for Frequency Modulation control . . . 50
5.5 Frequency control: (a) V_{out} and (b) f_{sw} for a load step from $R = 8\Omega$ to $R = 12\Omega$ . . . 51
5.6 Frequency control: (a) V_{out} and (b) f_{sw} for a load ramp from $R = 8\Omega$ to $R = 12\Omega$ . . . 51
5.7 Frequency control: (a) V_{out} and (b) f_{sw} for a constant $R = 10\Omega$ with not constant V_{in} . . . 52
5.8 V_{out} comparison for Open-Loop and Closed-Loop . . . 53
5.9 V_{out} vs. d at $f_{sw} = 120kHz$ and $R = [8; 20]\Omega$ . . . 54
5.10 Initial inductor current at v_{sw} transitions vs. d at (a) $0V \rightarrow V_{in}$ and (b) $V_{in} \rightarrow 0V$ . . . 55
5.11 $I_{0V \rightarrow V_{in}}$ and $-I_{V_{in} \rightarrow 0V}$ vs. d at $f_{sw} = 120kHz$ and $R = 8\Omega$ . . . 56
5.12 PWM control: (a) V_{out} and (b) d for a load step from $R = 8\,\Omega$ to $R = 12\,\Omega$ to $R = 25\,\Omega$ . . . 58
5.13 PWM control: (a) V_{out} and (b) d for a load ramp change from $R = 8\,\Omega$ to $R = 25\,\Omega$ . . . 58
5.14 PWM control: (a) V_{out} and (b) d for sine wave input . . . 59
5.15 $V_{out}(t)$ using a bang-bang controller . . . 60
5.16 Closed-loop block diagram using bang-bang controller . . . 61
5.17 Bang-bang control: V_{out} for load step changes from $R = 8\,\Omega$ to $R = 12\,\Omega$ to $R = 25\,\Omega$ . . . 62
5.18 Bang-bang control: V_{out} for load ramp changes from $R = 8\,\Omega$ to $R = 25\,\Omega$ . . . 62
5.19 Bang-bang control: V_{out} with sine wave input for $R = 10\,\Omega$ . . . 63
5.20 $v_{sw}(t)$ and ON-OFF state . . . 63

5.21 Output voltage as a function of skipped pulses n with $N = 8$ for different loads . . . 64
5.22 Switching node voltage $v_{sw}(t)$ for (a) $n = 1$(b) $n = 4$ and (c) $n = 7$. 65
5.23 DPM control: V_{out} for load step changes from $R = 8\,\Omega$ to $R = 12\,\Omega$ to $R = 25\,\Omega$ . . . 66
5.24 DPM control: V_{out} for load ramp changes from $R = 8\,\Omega$ to $R = 25\,\Omega$ 67
5.25 DPM control: V_{out} for load step changes from $R = 8\,\Omega$ to $R = 12\,\Omega$ to $R = 25\,\Omega$ . . . 68

6.1 Wide bandgap transistors . . . 71
6.2 MASTERGAN1 features . . . 72
6.3 MASTERGAN1 schematic . . . 72
6.4 PHE850EB5150MB15R17: (a) Dimensions, (b) Technical data . . . 74
6.5 ESR vs. f . . . 75
6.6 Magnetics core 0076312A7 . . . 76
6.7 Italtras inductor . . . 77
6.8 ACR vs. f . . . 77
6.9 Würth Elektronik inductor dimensions . . . 78
6.10 Würth Elektronik inductor ACR vs. f . . . 79
6.11 Both inductors ACR vs. f . . . 79
6.12 CDBHM220L-HF dimensions . . . 80
6.13 860021374027 dimensions . . . 81
6.14 MAL215099014E3 dimensions . . . 82
6.15 AMC1351 circuit diagram . . . 82
6.16 Voltage divider . . . 83
6.17 1779205141 circuit diagram . . . 83
6.18 Schematic . . . 84
6.19 3D view (a) Top view and (b) Bottom view . . . 85
6.20 (a) Top layer and (b) Bottom layer . . . 85
6.21 3D top view highlighting the different sections of the circuit . . . 86

7.1 Circuit setup . . . 87
7.2 Low voltage measurements: Dashed lines represent simulated values, while circular markers represent measured values. Shown are: (a) V_{out}, (b) $I_{L_{peak}}$, (c) $I_{L_{RMS}}$, and (d) efficiency η for different R and f_{sw} values. . . . 89
7.3 Low voltage measurements: Inductor current waveforms with $V_{in} = 30V$: (a) $R = 15\Omega$ and $f_{sw} = 110kHz$, (b) $R = 10\Omega$ and $f_{sw} = 115kHz$, and (c) $R = 20\Omega$ and $f_{sw} = 120kHz$ . . . 91
7.4 High voltage measurements: (a) V_{out}, (b) $I_{L_{peak}}$, (c) $I_{L_{RMS}}$, and (d) efficiency η for different R and f_{sw} values. . . . 92

7.5 High voltage measurements: Inductor current waveforms with $V_{in} = 230V_{RMS}$: (a) $R = 20\Omega$ and $f_{sw} = 120kHz$, (b) $R = 15\Omega$ and $f_{sw} = 130kHz$, and (c) $R = 10\Omega$ and $f_{sw} = 120kHz$ 94

Chapter 1

Introduction

In recent years, Wireless Power Transfer (WPT) has gained significant attention in electronics, particularly for battery charging applications. New-generation devices are incorporating this feature, ranging from low-power devices such as smartphones [1] to high-power devices such as electric vehicles [2]. With the growth in the number of battery-powered devices, WPT has become increasingly important. However, this growth also raises concerns about environmental sustainability, particularly due to the energy consumption of millions of devices. Improving the efficiency of wireless power systems is, therefore, not only a technical challenge but also a step toward reducing energy waste and minimizing the environmental footprint of electronic devices. Another advantage of this technology is the absence of a direct electrical connection, reducing the risks of electric shocks.

WPT technologies are categorized into two main types based on transfer distance: far-field WPT, which is considered as a radiating type, and near-field WPT, considered as non-radiative. The energy transfer of the latter depends on the coupling techniques, which are: magnetic resonant coupling, inductive coupling, capacitive coupling, and magneto-dynamic coupling [3].

The most common coupling techniques are inductive coupling and capacitive coupling. The first one, often referred to as Inductive Power Transfer (IPT), relies on magnetic fields to transfer energy, while the latter, referred to as Capacitive Power Transfer (CPT), utilizes electric fields for energy transfer.

This thesis is focused on Capacitive Power Transfer (CPT), which presents several advantages over IPT. The reduction of magnetic materials results in a more lightweight and cost-effective solution for certain applications. Furthermore, it reduces electromagnetic interference (EMI) since the electric fields present better directionality compared to magnetic fields. [4] However, CPT presents some disadvantages. The coupling capacitance between the transmitter and receiver plates is typically very small (in the order of pico or nano-farads). This small capacitance makes the compensation network more complex.

This introductory section will show the importance of implementing a control system in order to maintain a specific parameter at a desired constant value and the thesis objectives.

The implementation of a control system in a DC-DC converter is essential to ensure stable and reliable operation under varying circuit conditions, such as changes in load, input voltage, or environmental factors. A well-designed control system compensates for disturbances, ensuring that the controlled variable, typically the output voltage, remains stable and tracks the desired reference value accurately.

Additionally, control systems play a vital role in enhancing system performance by reducing output voltage ripple, improving transient response, and minimizing overshoot or oscillations during dynamic load changes.

The variable to control in this project is the output voltage.

1.1 Thesis objectives

The primary objective of this thesis is to complete the analysis of the Capacitively Isolated Low-Power DC-DC converter system and investigate different control strategies for its implementation. Continuing the work from previous theses, this thesis focuses on designing and implementing the control loop to ensure a stable output voltage and efficient performance under different operating conditions. Specifically, the steps are:

- **System Modelling**: To understand the behaviour of the system when any variable or parameter changes. It is also important to implement the control loop.
- **Simulation and Validation**: To simulate the system and validate the model.
- **Control Strategy Implementation**: To analyse the different control strategies applicable to the system and compare their advantages and disadvantages.
- **Prototype**: To select the most suitable components and design a PCB.
- **Experimental Testing**: To conduct open-loop and closed-loop measurements using both low input voltage and grid voltage input.
- **Grid-Voltage Testing**: To perform experimental measurements using a $230V_{rms}$ grid voltage input, which was not feasible in previous theses.

The state-of-the-art review of CPT systems was conducted in detail in previous theses [5] [6]. Therefore, this thesis will focus on the control system design and implementation for CPT-based DC-DC converters.

Chapter 2

Scheme and Building blocks of a CPT converter

2.1 Building blocks of the converter

Figure 2.1 shows a general block diagram of the CPT system, indicating each building block.

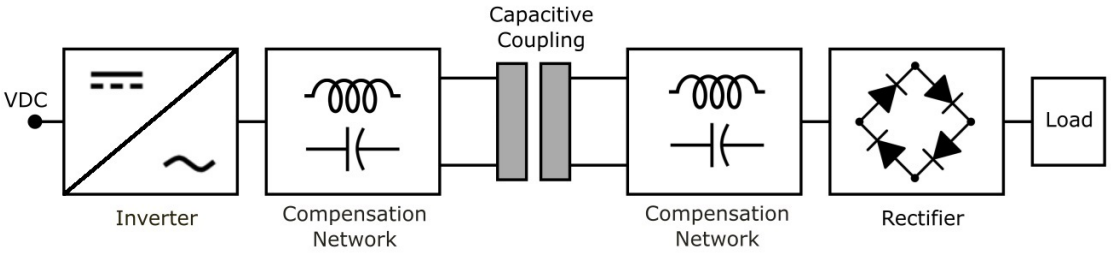


Figure 2.1: Block diagram of the complete CPT system

2.1.1 Inverter

The inverter is a fundamental power electronic block responsible for converting a DC input voltage into an AC voltage. In CPT systems, the inverter generates a high-frequency alternating voltage in the form of a rectangular waveform, with a specific switching frequency f_{sw} and duty cycle d.

Inverters can be implemented with different topologies, and the two most common configurations are the **half-bridge inverter** and the **full-bridge inverter**.

The half-bridge inverter consists of two switches (e.g., IGBTs, MOSFETs, or HEMTs, depending on the circuit) that operate in a complementary manner: when

one switch is on, the other is off. This result in an output voltage at the switching node that alternates between $0V$ and V_{DC}, making it an unipolar output.

The full-bridge rectifier consists of four switches arranged in an H-bridge configuration. By controlling the switching in pairs (e.g., diagonally opposite switches turning on simultaneously), the output voltage alternates between $-V_{DC}$ and $+V_{DC}$. Therefore, the voltage swing is double respect to the half-bridge configuration, resulting in a bipolar output.

In Figure 2.2 both inverter configurations are depicted.

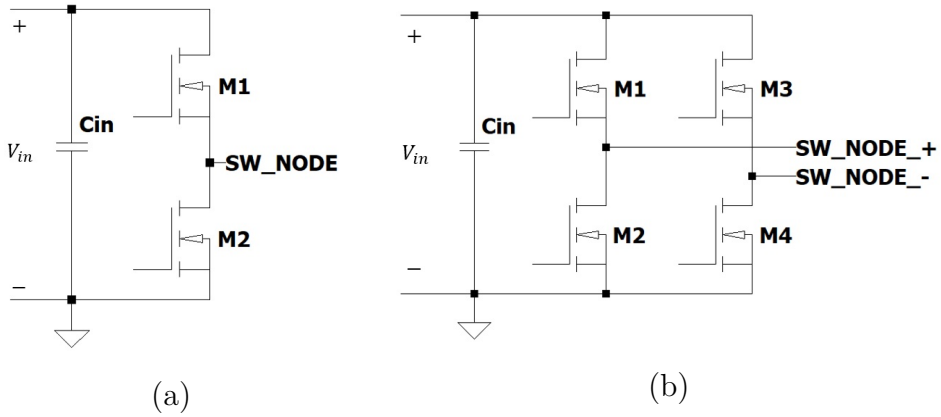


Figure 2.2: (a) Half-bridge and (b) Full-bridge configuration

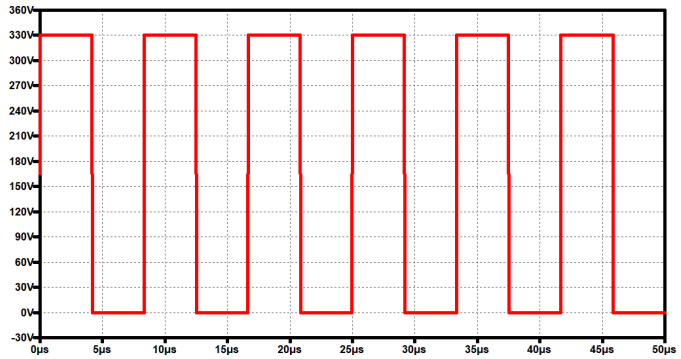
Figure 2.3 shows the switching node voltage for both configurations. These waveforms are performed with an input voltage $V_{in} = 330\,\mathrm{V}$, switching frequency f_{sw} equal to 120 kHz and a duty cycle d at 50%.

A comparison of both configurations is presented in Table 2.1.

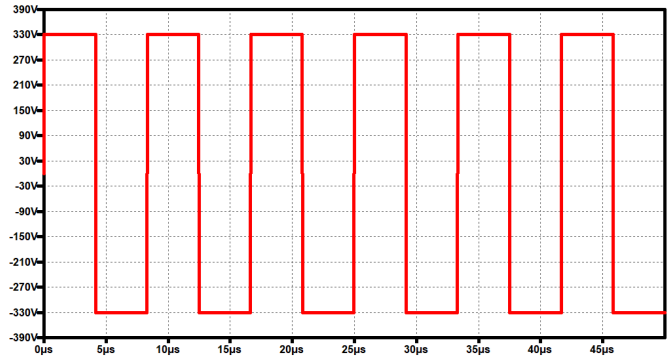
Property	**Half-Bridge**	**Full-Bridge**
Components	2 switches	4 switches
Voltage amplitude	$0V$ to V_{DC}	$-V_{DC}$ to V_{DC}
Conduction losses	Lower (fewer switches)	Higher (more switches)
Typical power level	Low to Medium Power	High Power

Table 2.1: Comparison of inverter configurations

The selected configuration for this project is the **half-bridge inverter**. Since the application requires lower power, the conduction losses will be reduced. In addition, the complexity is lower, as the number of switches is lower than the full-bridge.



(a)



(b)

Figure 2.3: Switching node voltage for (a) Half-bridge and (b) Full-bridge configuration

2.1.2 Capacitive interface

The capacitive interface in CPT systems consists of plates that transfer energy through electric fields generated between them. The arrangement and number of plates play a critical role in the effectiveness of the power transfer.

The value of the effective capacitance is determined by several factors that are:

- **Distance between plates**: Smaller gaps between the transmitter and receiver results in higher capacitance [3].
- **Plates area**: Larger surface areas increase capacitance and improve energy transfer efficiency [7].
- **Dielectric material**: The dielectric constant of the material between the plates significantly impacts the capacitance [8].

- **Plates configuration**: The arrangement and number of the plates affects the capacitive coupling.

The effective coupling capacitance can reach up to few hundreds of picofarads or a few nano-farads [9].

In this project, discrete capacitors are used to replicate the behaviour of the capacitive interface, providing a controlled and stable capacitance for analysis and implementation.

2.1.3 Compensating network

Compensation topologies are essential for CPT systems. Due to the limited size of the coupling plates and the low permittivity of the air, the coupling capacitance is small, resulting in a high coupling impedance This impedance is generally much larger than the load impedance, which can significantly affect efficient power transfer [10].

Therefore, compensating networks are used to counteract the effects of the high coupling impedance. There are different compensating network topologies, which are:

- **L-Compensation**: This topology consists of a single inductor on the primary side or two inductors, one placed on the primary side and the other on the secondary side.
- **LC-Compensation**: An extension of the L-compensation, this topology includes two additional capacitors, one placed on the primary side and the other on the secondary side.
- **LCLC-Compensation**: This topology consists of two inductors and two capacitors on both the primary and secondary sides.

Figure 2.4 shows circuit diagrams of each topology.

Additionally, Table 2.2 provides a comparison of the compensating network topologies discussed, highlighting the characteristics mentioned in [10] and showing the advantages of each topology.

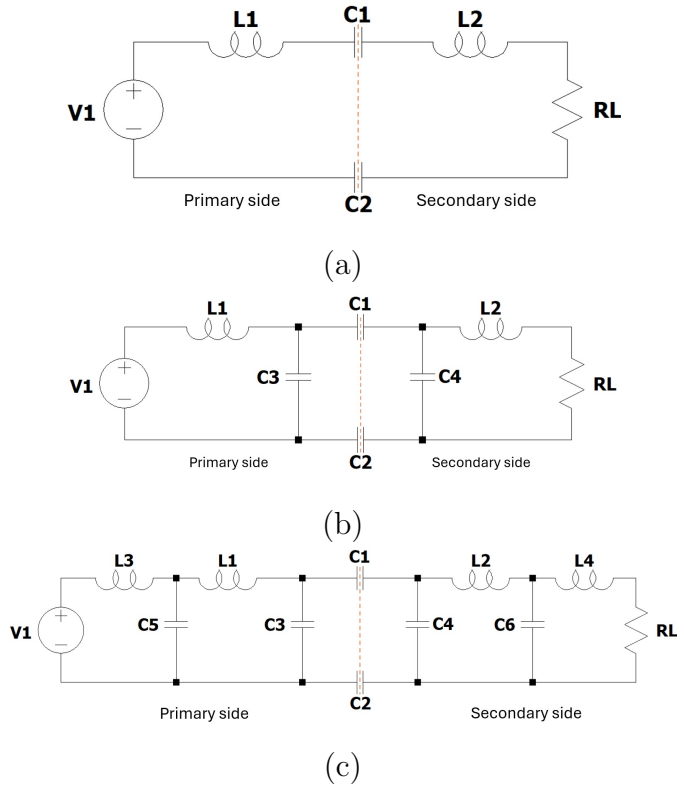


Figure 2.4: Compensating networks: (a) L, (b) LC and (c) LCLC.

Property	**L**	**LC**	**LCLC**
Complexity	Low	Medium	High
Required Inductance	High	Medium	Low
Suitable Power Level	Low to Medium	Medium to High	High
Cost	Low	Medium	High
Sensitivity to Misalignment	High	Medium	Low
Frequency Tolerance	Low	Moderate	High

Table 2.2: Comparison of compensating networks topologies

The chosen topology for implementation in this project is the single L compensation, as it is well-suited for low-power applications and significantly reduces both cost and complexity. However, the inductance and, thus, the size of the inductor is expected to be high, leading to significative losses.

2.1.4 Output rectifier

The rectifier is responsible for converting the AC voltage from the secondary side of the compensating network into a DC voltage, ensuring stable power delivery to the load.

Several rectification topologies are used in converter systems. The most common are:

- **Half-bridge rectifier**: This topology consists of a single diode, allowing the current to flow during only one half of the AC cycle. It is simple and cost-effective. However, the ripple is high, reducing the efficiency.
- **Full-bridge rectifier (Graetz Bridge)**: This topology consists of four diodes, arranged in H-configuration, and allows rectification of both halves of the AC waveform. Its complexity is higher compared to the previous topology, but it provides reduced ripple and higher efficiency.
- **Synchronous rectifier**: This topology uses controlled switches, such as MOSFETs, instead of diodes. This allows the reduction of conduction losses. It is used for high-efficiency applications. However, a drawback is the complexity, since the switches must be controlled.

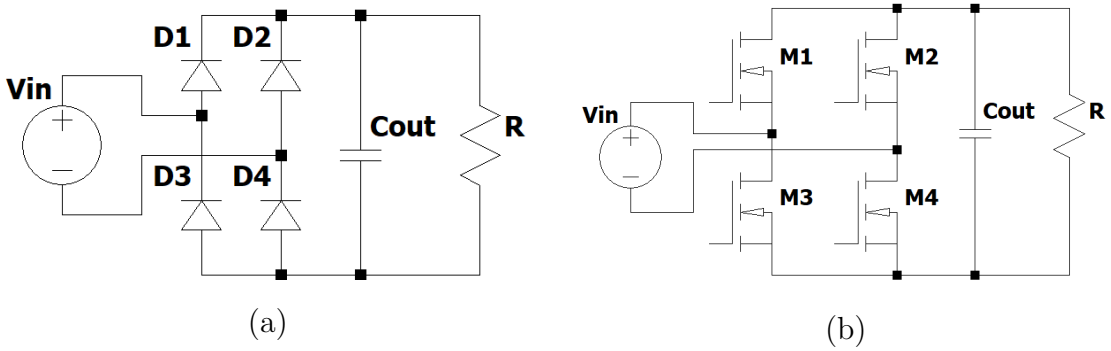


Figure 2.5: Full-bridge rectifier (a) Passive and (b) Active

The chosen rectification topology for this project is the **full-bridge rectifier** due to its balance between efficiency and simplicity.

2.1.5 Feedback

In order to control the output voltage effectively, it is essential to measure it and adjust system parameters to regulate the voltage and ensure stable operation under varying conditions. This requires the implementation of a feedback loop. The two primary feedback methods commonly used are as follows [11]:

- **Voltage Mode Control**: This method measures the output voltage and compares it to a reference voltage. The difference, also known as error, is processed by the control system, which adjust a parameter, most commonly duty cycle and switching frequency, in order to maintain the output voltage at the desired value.
- **Current Mode Control**: This technique measures the inductor current in addition to the output voltage in order to have a faster response.

The inductor current waveform in the circuit is complex and implementing current mode control would be challenging. For that reason, this control method is not considered.

Figure 2.6 shows a basic schematic of a Voltage Mode control.

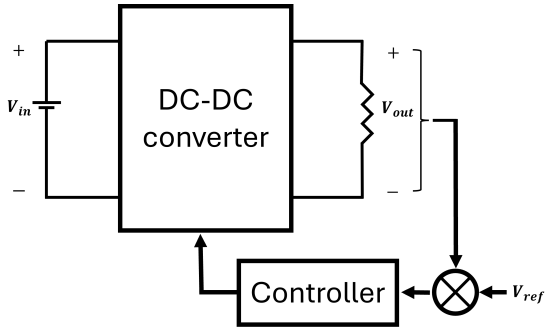


Figure 2.6: Voltage mode control for a DC-DC converter

In this project, the Voltage Mode Control will be used and the control strategies will be implemented using a microcontroller, which will determine the gate signals of the transistors.

2.2 Topology

The complete circuit for the proposed system is illustrated in Figure 2.7. The topology chosen for this project consists of a half-bridge inverter, a capacitive interface made of discrete capacitors, a secondary-side single inductor compensation network, and a full-bridge rectifier. This configuration is chosen to optimize cost, complexity, and efficiency for a low-power application.

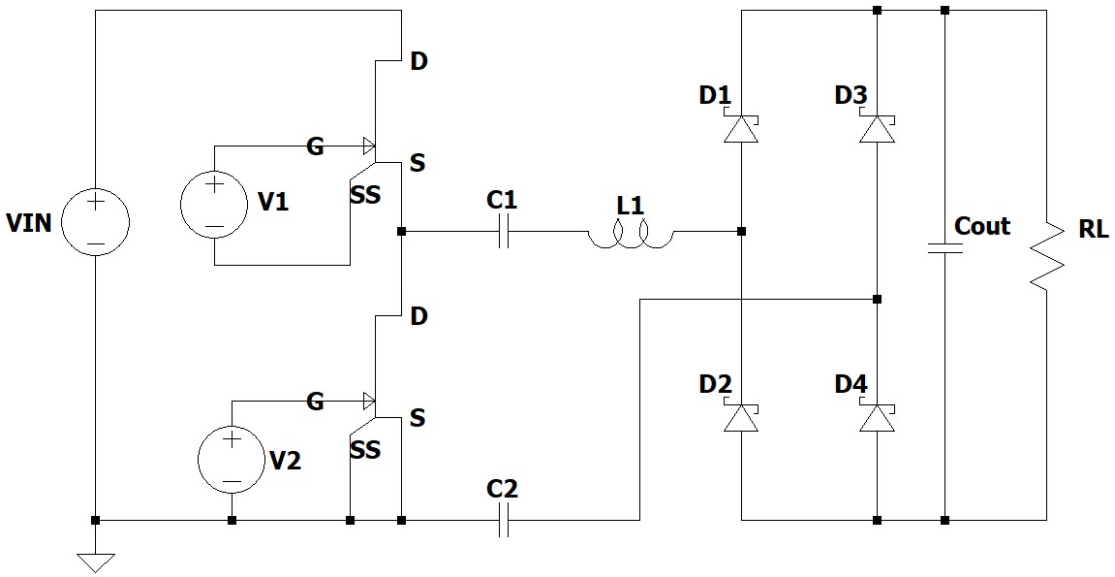


Figure 2.7: CPT circuit

Table 2.3 highlights the circuit characteristics and provides an overview of the chosen components and configurations for the subsystems of the design.

Circuit characteristics	
Inverter	Half-bridge
Capacitive Interface	Discrete capacitors
Compensation Network	Primary-side single inductor
Rectifier	Full-bridge

Table 2.3: Circuit characteristics

2.3 Specifications

The system specifications are summarized in Table 2.4. The input voltage of $330V$ is based on a rectified grid voltage. The output voltage is regulated to $20V$ with a target power output of $50W$. The system aims for an efficiency greater than 85% to ensure low power loss and high performance. These specifications are defined to meet the requirements of the application while balancing cost and performance.

Specifications	
Input voltage	$330V$ (rectified grid voltage)
Output voltage	$20V$
Output Power	$50W$
Efficiency	$> 85\%$

Table 2.4: Specifications

Chapter 3

Mathematical model

In the previous chapter, the circuit building blocks have been explained in detail. In this chapter, the mathematical model of the circuit will be developed. The derivation of a mathematical model provides a better understanding of the circuit and its behaviour.

The schematic is depicted in Figure 3.1.

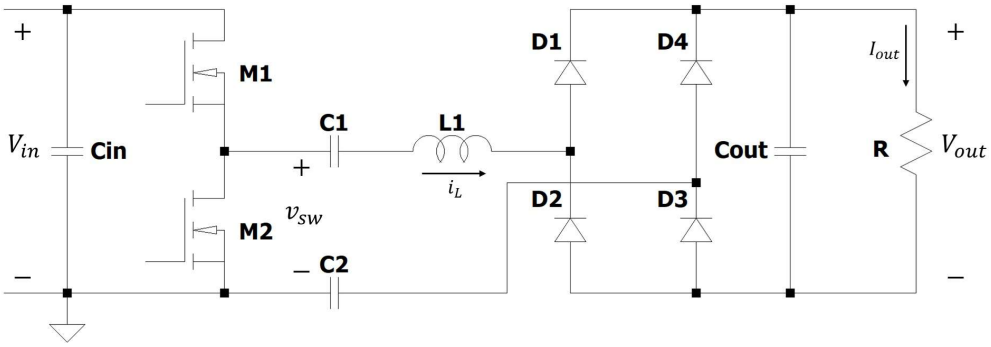


Figure 3.1: Circuit schematic

For realizing the mathematical model, the following assumptions must be considered:

1. The switching node voltage, labelled as v_{sw}, is considered as a perfect rectangular wave switching at f_{sw} at any duty cycle d.
2. Capacitors and inductor are ideal, which means they do not include any dissipative elements.
3. V_{in} is constant.
4. Diodes are ideal, except for their forward voltage V_γ.

5. Dead time is considered negligible.

The resulting equivalent circuit is depicted in Figure 3.2. This circuit is a RLC circuit, whose input signal is $v_{sw}(t)$.

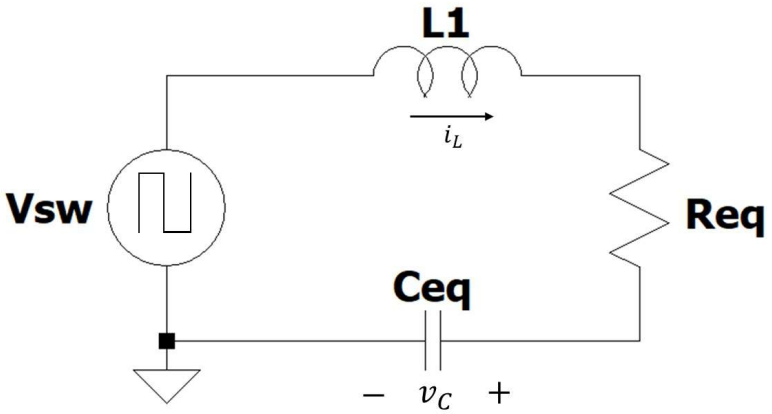


Figure 3.2: Equivalent circuit

As stated previously, the switching node voltage is replaced by a rectangular wave source, switching at f_{sw}. The equivalent capacitance is the series of C_1 and C_2: $C_{eq} = \frac{C_1}{2}$. The equivalent resistance is $R_{eq} = \frac{8}{\pi^2}\frac{R}{\alpha_\gamma}$, where R is the load resistance and $\alpha_\gamma = \frac{1}{1+\frac{2V_\gamma}{V_{out}}}$ is referred to as the rectifier efficiency. This parameter, analysed in [12], represents the equivalent resistance seen at the rectifier's input, derived from a First-Harmonic Approximation with applied corrections.

It is important to note that the voltage across the equivalent capacitor v_C is the sum of each capacitor voltage: $v_C = v_{C_1} + v_{C_2}$.

Having established these assumptions, the modelling process can now proceed stage by stage.

3.1 Building blocks

3.1.1 Half-bridge inverter

To model the switching node of the half-bridge (high side transistor's source and low side transistor's drain node), it must be considered all the possible cases:

- **High-side ON and low-side OFF:** **M1** is considered as a short circuit and **M2** as an open circuit. This causes $v_{sw} = V_{in}$.
- **High-side OFF and low-side ON:** **M1** is an open circuit and **M2** is shorted to ground, then $v_{sw} = 0V$.

- **Both transistors OFF:** Depending on the direction of the inductor (and capacitors) current at that instant, the switching node can have two possible values:

  1. If the inductor current is **positive** (flowing from left to right in the schematic) at the moment both transistors are off, the inductor resists the abrupt change in current and forces the low-side body diode of **M2** to conduct, causing the switching node to be $v_{sw} = -v_D$.
  2. On the other hand, if the inductor current is **negative** (from right to left in the schematic), the inductor forces the high-side body diode of **M1** to conduct, clamping the switching node voltage to $v_{sw} = V_{in} + v_D$.

- **Both transistors ON:** This causes a short-circuit at the input, therefore this is a **forbidden** state.

The state of both transistors OFF is called **dead time**. For simplification of the model, the forward voltage of the body diodes are considered null: $v_D = 0V$. This leads to only two possible values for the switching node voltage: $v_{sw} = V_{in}$ and $v_{sw} = 0V$.

Therefore, this building block consists of a rectangular wave, switching at f_{sw} with a certain duty cycle d.

3.1.2 Resonant tank

State-space representation is a useful mathematical tool for analysing and modelling electrical circuits. Furthermore, it is particularly useful for control strategies. When selecting state variables, it is essential to choose variables whose derivatives appear in the circuit's equations. The differential equations of the equivalent circuit are derived as follows.

Using the Kirchhoff's Voltage Law, it is possible to reach the following equation:

$$\frac{di_L}{dt} = \frac{1}{L}(v_{sw}(t) - v_C(t) - i_L(t)R_{eq}) \tag{3.1}$$

Applying the Kirchhoff's Current Law, the following expression is obtained:

$$\frac{dv_C}{dt} = \frac{i_L(t)}{C_{eq}} \tag{3.2}$$

It can be clearly seen that there are two quantities expressed in a differential way, that are inductor current i_L and capacitor voltage v_C. Therefore, these are the state variables of the circuit.

The general form to represent a state-space model is the following:

$$\dot{x}(t) = Ax(t) + Bu(t) \tag{3.3}$$
$$y(t) = Cx(t) + Du(t) \tag{3.4}$$

where:

x is called the **state vector**. y is called the **output vector**. u is called the **input vector**. A is the **state matrix**. B is the **input matrix**. C is the **output matrix**. D is the **feed-through matrix**.

In the circuit concerned, the state vector consists of i_L and v_C:

$$x(t) = \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} \tag{3.5}$$

In addition, the input vector $u(t)$ is $v_{sw}(t)$.

By combining equations (3.1) and (3.2) and rearranging them into the standard form of a state-space model, the following expression is obtained:

$$\begin{bmatrix} \dot{i}_L(t) \\ \dot{v}_C(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_{eq}}{L} & -\frac{1}{L} \\ \frac{1}{C_{eq}} & 0 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{sw}(t) \tag{3.6}$$

The state matrix A takes the form:

$$A = \begin{bmatrix} -\frac{R_{eq}}{L} & -\frac{1}{L} \\ \frac{1}{C_{eq}} & 0 \end{bmatrix} \tag{3.7}$$

The input matrix B is given as:

$$B = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{3.8}$$

The feed-through matrix D is null, since there is no direct coupling between the input and the output in the system dynamics.

The output matrix C depends on the desired state variable output. If the desired one is the inductor current i_L, C must be (3.9). Otherwise, if the output of interest is v_C, C must be (3.10).

$$C = \begin{bmatrix} 1 & 0 \end{bmatrix} \tag{3.9}$$

$$C = \begin{bmatrix} 0 & 1 \end{bmatrix} \tag{3.10}$$

Since the actual topology is a series resonant converter, it is more convenient using the inductor current as the output state variable. Therefore, C must be (3.9).

Therefore, the output vector takes the form:

$$y(t) = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} = i_L(t) \tag{3.11}$$

The building block of this stage is depicted in Figure 3.3

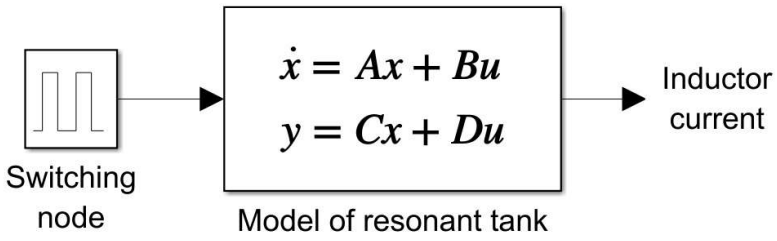


Figure 3.3: Building block of resonant tank

3.1.3 Full-bridge rectifier

The input of this stage is the inductor current i_L, coming from the resonant tank.

As the diodes in the full-bridge rectifier are considered ideal and the forward voltage drop was already considered in the expression of R_{eq}, this building block just rectify the inductor current. In other words, the mathematical block responsible for this operation is the absolute value. Therefore, the following expression is obtained:

$$i_{rect}(t) = |i_L(t)| \tag{3.12}$$

The building block of this stage is depicted in Figure 3.4

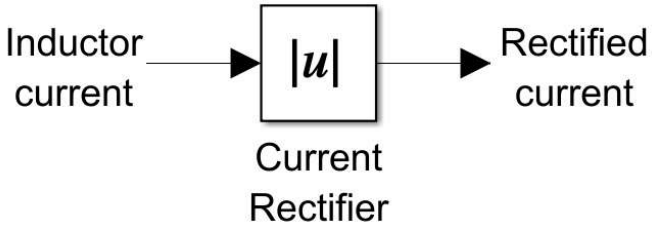


Figure 3.4: Building block of full-bridge rectifier

3.1.4 Output filter

The final stage consists of the output capacitor C_{out} and the resistive load R. The input is the rectified inductor current I_{rect} coming from the full-bridge rectifier.

The output circuit is depicted in Figure 3.5 and the expression of output current and voltage can be obtained.

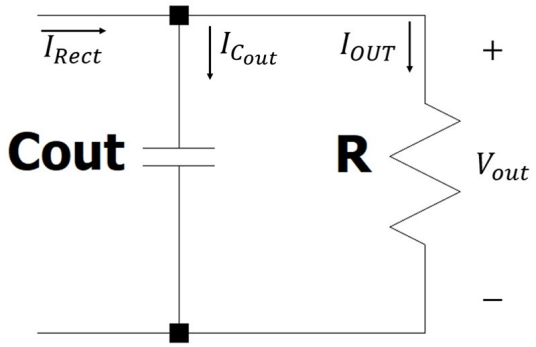


Figure 3.5: Output node

By applying KCL at the output node, the following expression is derived:

$$i_{rect} = i_{C_{out}} + I_{out} \tag{3.13}$$

where i_{rect} is the rectified inductor current coming from the full-bridge rectifier, $i_{C_{out}}$ is the current through the output capacitor and I_{out} represents the load current.

Furthermore, the expression for the capacitor and load current are given as follows:

$$i_{C_{out}} = C_{out}\frac{dV_{out}}{dt} \tag{3.14}$$

$$I_{out} = \frac{V_{out}}{R} \tag{3.15}$$

Equation 3.13 can be rewritten as:

$$i_{rect} = C_{out}\frac{dV_{out}}{dt} + \frac{V_{out}}{R} \tag{3.16}$$

Solving for $\frac{dV_{out}}{dt}$, the previous expression becomes:

$$\frac{dV_{out}}{dt} = \frac{i_{rect}}{C_{out}} - \frac{V_{out}}{RC} \tag{3.17}$$

The differential expression for V_{out} in time domain can be transformed into the Laplace domain as follows:

$$V_{out}(s) = \frac{R}{sRC_{out} + 1} I_{rect}(s) \tag{3.18}$$

By dividing by R, output current expression is obtained:

$$I_{out}(s) = \frac{1}{sRC_{out} + 1} I_{rect}(s) \tag{3.19}$$

The building block of this stage is depicted in Figure 3.6

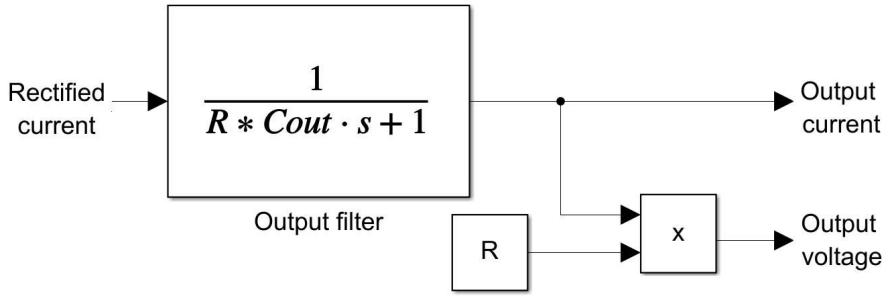


Figure 3.6: Building block of output filter

Ripple Modelling with ESR

Considering the equivalent series resistance (ESR) of the output capacitor C_{out}, as shown in Figure 3.7, provides a more realistic model of the ripple on the load.

The expressions of output voltage and output current in Laplace's domain are the following:

$$V_{out}(s) = R\frac{sC_{out}R_C + 1}{sC_{out}(R + R_C) + 1} I_{rect}(s) \tag{3.20}$$

$$I_{out}(s) = \frac{sC_{out}R_C + 1}{sC_{out}(R + R_C) + 1} I_{rect}(s) \tag{3.21}$$

where R_C is the ESR of C_{out}. Figure 3.8 shows the block diagram of the output filter, considering ESR of C_{out}.

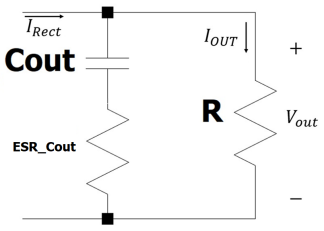


Figure 3.7: Output node with output capacitor's ESR

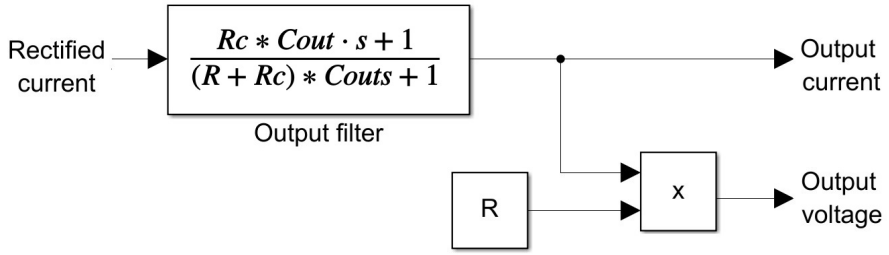


Figure 3.8: Building block of output filter considering C_{out}'s ESR

3.1.5 Open Loop model

Combining all the stages explained previously, the model of the circuit is complete and showed in Figure 3.9.

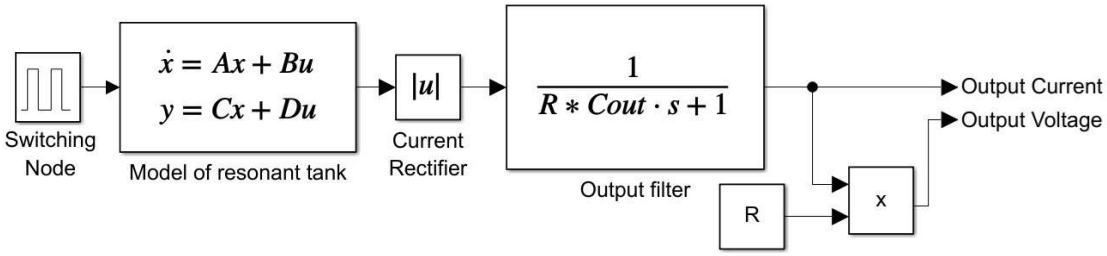


Figure 3.9: Open Loop model of CPT circuit

This model is able to simulate both transient and steady-state conditions for any given switching frequency f_{sw} and duty cycle d at the switching node. It employs numerical integration to compute key variables such as output voltage, inductor current, and other system parameters. In addition, it is useful for determining the optimal operation point and selecting the best L and C combination.

3.2 Analysis of Damped Oscillations

The waveforms of inductor current i_L and capacitor voltage v_C can exhibit **damped** or **undamped** oscillations. This depends on the parameters of the resonant tank being R_{eq}, L and C_{eq}.

An important parameter that measures the damping characteristics is the **damping factor** ζ, which is defined as:

$$\zeta = \frac{R_{eq}}{2}\sqrt{\frac{C_{eq}}{L}} \tag{3.22}$$

According to the value of ζ, there are three damping scenarios:

- $\zeta < 1$: **Underdamped**: Oscillatory response.
- $\zeta = 1$: **Critically damped**: Fastest non-oscillatory response
- $\zeta > 1$: **Overdamped**: Slow non-oscillatory response

In underdamped oscillations, two categories can be identified: **Completely Damped Oscillations** (CDO) and **Partially Damped Oscillations** (PDO). The classification depends on the behaviour of the oscillation between switching events.

CDO occurs when the waveform oscillation is completely extinguished within two switching events, meaning no residual oscillation remain. In contrast, PDO arises when oscillation persist beyond two switching events.

For underdamped responses, the oscillation follows an exponential decay envelope for an input step:

$$A(t) = A_0 e^{-\zeta \omega_n t} \tag{3.23}$$

Where $A(t)$ can be either $i_L(t)$ or $v_C(t)$ in this case and ω_n is the natural frequency, which is defined as $\omega_n = \frac{\omega_{res}}{\sqrt{1-2\zeta^2}}$.

For calculating the extinction time, which is the time where the oscillations are negligible, it is possible to use the rule of thumb of 5 time constants:

$$t_{ext} \approx \frac{5}{\zeta \omega_n} \tag{3.24}$$

The switching event occurs every half of switching period $T_{sw} = \frac{1}{f_{sw}}$. Therefore, in addition to the condition $\zeta << 1$ for both cases, the condition for PDO is expressed in Equation (3.25) and for CDO in Equation (3.26).

$$\frac{T_{sw}}{2} < t_{ext} \tag{3.25}$$

$$\frac{T_{sw}}{2} \geq t_{ext} \tag{3.26}$$

The last expression allows to determine the minimum switching frequency required to achieve PDO operation.

Substituting Equation 3.25 with previous expressions:

$$\frac{1}{2f_{sw}} < \frac{5}{\zeta \omega_n} = \frac{5}{\omega_n} \frac{2}{R_{eq}} \sqrt{\frac{L}{C_{eq}}} \tag{3.27}$$

For $\zeta << 1$, the natural frequency ω_n tends to the resonance frequency $\omega_{res} = \frac{1}{\sqrt{LC_{eq}}}$.

Thus, the minimum switching frequency required for PDO operation is given by:

$$f_{sw} > \frac{R_{eq}}{20L} \tag{3.28}$$

3.2.1 Quality factor

The Quality Factor, or Q factor, is another important parameter that describes the damping condition of the system and it is defined in a RLC series circuit as follows:

$$Q = \frac{1}{R_{eq}}\sqrt{\frac{L}{C_{eq}}} \tag{3.29}$$

Its relation with the damping coefficient is:

$$Q = \frac{1}{2\zeta} \tag{3.30}$$

The higher is the Q factor, the more selective is the frequency response in the neighbourhood of the resonance frequency.

It is desirable to have a Q factor much grater than 1, which is a practical consideration.

3.3 Harmonics analysis

Assuming an ideal pulse wave at the switching node, whose amplitude is V_{in}, switching frequency f_{sw} and duty cycle d, the Fourier series expression for the switching node voltage is the following:

$$v_{sw}(t) = \frac{V_{in}}{2} + \frac{2V_{in}}{\pi}\sum_{n=1}^{\infty}\left(\frac{1}{n}sin(\pi nd)cos(n\omega_{sw}t)\right) \tag{3.31}$$

According to the value of the duty cycle, some harmonics remain and other are vanished. These are some examples:

- For a duty cycle of 50% ($d = \frac{1}{2}$), all even harmonics disappear, leaving only the odd ones. This is the case of a square wave.
- For a duty cycle of 33.33% ($d = \frac{1}{3}$), all even harmonics remain and the harmonics that are multiple of three disappear (3^{rd}, 9^{th}, etc.).
- For a duty cycle of 25% ($d = \frac{1}{4}$), both even and odd harmonics are present except for the multiple of four (4^{th}, 8^{th}, etc.).

The consideration for duty cycles different from 50% is important for the Pulse Width Modulation (PWM) control, which varies the duty cycle. For all the other cases, a 50% duty cycle will be used.

For a square wave input, when $f_{sw} = f_{res}$, the maximum power transfer and the maximum gain are obtained. If f_{sw} is selected to be an odd fraction of f_{res} (e.g. $\frac{f_{res}}{3}$, $\frac{f_{res}}{5}$, etc.) that odd harmonic resonates and generates a local gain maximum at that fraction of f_{res}. These frequencies are known as **sub-harmonics**.The peak amplitudes decay when the frequency is lower.

This will be shown graphically in Section 4.2.1.

The proposed converter is designed to work in a sub-harmonic region of the frequency range. Among the main advantages, this approach allows to reduce significantly the switching losses of the converter transistors.

3.4 Zero Voltage Switching analysis

Another important aspect to analyse is the soft-switching condition, specifically the Zero Voltage Switching (ZVS). This section focuses on the derivation of the necessary conditions to achieve ZVS.

In order to know the condition of ZVS, it is necessary to evaluate the energy balance between the equivalent output capacitor of the transistors $C_{oss,eq} = 2C_{oss}$ and inductor L.

The energy stored in the equivalent output capacitance at the voltage V_{in} is given as:

$$E_{C_{oss,eq}} = \frac{1}{2} C_{oss,eq} V_{in}^2 = C_{oss} V_{in}^2 \tag{3.32}$$

The energy available from the inductor at the switching event is as follows;

$$E_L = \frac{1}{2} L I_0^2 \tag{3.33}$$

where I_0 is the inductor current at a switching event whose value was analysed in [12] and it is the following:

$$I_0 = -\frac{V_{in}}{\omega_{res} L} \frac{B_{fR}}{A_{fR}^2 + B_{fR}^2} \tag{3.34}$$

Where:

$$A_{fR} = 1 + e^{-\frac{\gamma}{2f_{sw}}} [-\frac{\gamma}{\omega_{res}} sin(\pi \frac{f_{res}}{f_{sw}}) + cos(\pi \frac{f_{res}}{f_{sw}})] \tag{3.35}$$

$$B_{fR} = e^{-\frac{\gamma}{2f_{sw}}} sin(\pi \frac{f_{res}}{f_{sw}}) \tag{3.36}$$

Being $\gamma = \frac{R_{eq}}{2L}$ and $\omega_{res} = \frac{1}{\sqrt{LC_{eq}}}$.

It should be noted that Equation 3.34 applies for $d = 50\%$.

The transistors output capacitance must be fully discharged by the inductor during the dead-time in order to have zero voltage across the transistor when the switching event occurs. Therefore, the inductor energy must be higher than the capacitors one, resulting in the following inequality:

$$\frac{1}{2}LI_0^2 > C_{oss}V_{in}^2 \tag{3.37}$$

$$|I_0| > V_{in}\sqrt{\frac{2C_{oss}}{L}} \tag{3.38}$$

To discharge the high-side FET capacitance, the current polarity must be negative (flowing from switching node upwards in the schematic) because the body diode of the low-side FET blocks the current.

Therefore, the condition for ZVS in the high-side transistor for $0V \rightarrow V_{in}$ transition of the switching node voltage is:

$$I_0 < -V_{in}\sqrt{\frac{2C_{oss}}{L}} \tag{3.39}$$

It can be seen from the previous expression that the initial inductor current must be negative for achieving ZVS.

Conversely, to discharge the low-side FET capacitance, the current polarity must be positive (flowing from low-side's source toward the switching node in the schematic) and the condition for ZVS for the low-side FET for $V_{in} \rightarrow 0V$ transition of the switching node voltage is:

$$I_0 > V_{in}\sqrt{\frac{2C_{oss}}{L}} \tag{3.40}$$

When the duty cycle is equal to 50%, the currents at $0V \rightarrow V_{in}$ and $V_{in} \rightarrow 0V$ transitions are equal in absolute value. Therefore, in the following analysis, only the ZVS condition for the high-side transistor, given in Equation 3.39, will be considered. If ZVS is achieved for the high-side transistor, it will also be satisfied for the low-side transistor.

It is worth noting that if CDO was employed, the current at the next switching event will be zero or near zero, making ZVS difficult to achieve.

Assuming I_0 is constant during the whole dead time, it is necessary to obtain the minimum time in which all the energy from the inductor is transferred to the transistors capacitance.

Assuming a linear capacitance discharge, the voltage transition is given as:

$$\Delta V = \frac{I_0}{2C_{oss}} \Delta t \tag{3.41}$$

ΔV is equal to V_{in} as the voltage must drop to $0V$ and Δt, which can be referred to as t_{dead}, is the time necessary for that transition.

Solving for t_{dead} in Equation 3.41, the expression for dead time is:

$$t_{dead} = \frac{2C_{oss}V_{in}}{|I_0|} \tag{3.42}$$

The dead time for the worst-case scenario can be obtained with the minimum initial inductor current I_0 as this is the slowest discharge condition. This was described in Equation (3.38):

$$t_{dead_{max}} = \frac{2C_{oss}V_{in}}{I_{0_{min}}} \tag{3.43}$$

Substituting the expression for $I_{0_{min}}$:

$$t_{dead_{max}} = \frac{2C_{oss}V_{in}}{V_{in}\sqrt{\frac{2C_{oss}}{L}}} \tag{3.44}$$

Simplifying further:

$$t_{dead_{max}} = \sqrt{2LC_{oss}} \tag{3.45}$$

This final expression provides the maximum dead time based on the output capacitance C_{oss} and the inductance L.

In the design step, when the dead time must be decided, the condition expressed in Equation (3.45) must be considered.

Chapter 4

Selection of Operating Point

4.1 Selection of Parameters

In order to select the values of the parameters, it is necessary to consider all the constrains and limitations of the circuit.

4.1.1 Interface capacitor

The coupling capacitance value depends on the structure used. This includes the area of the plates, the transfer distance, the dielectric, etc., as it was explained in Section 2.1.2.

According to [9], coupling capacitance can reach up to few nano farads.

For that reason, a reasonable value for the interface capacitors is $C = 15\,\text{nF}$, and therefore, the equivalent capacitance $C_{eq} = 7.5\,\text{nF}$.

Since this system is a CPT converter, the interface capacitance is the primary parameter to be selected. Its value dictates the operating characteristics of the circuit, influencing the design of other components

4.1.2 Resistive load

As it was stated in the design requirements, the desired output power is $P_{out} = 50W$ and the desired output voltage is $V_{out} = 20V$. The load is considered to be purely resistive. Therefore, the resistive load, for maximum power at $50W$, must be:

$$R > \frac{V_{out}^2}{P_{out}} = 8\Omega \tag{4.1}$$

For the equivalent resistance calculation:

$$R_{eq} = \frac{8}{\pi^2}\frac{R}{\alpha_\gamma} \tag{4.2}$$

Where $\alpha_\gamma = \frac{1}{1+\frac{2V_\gamma}{V_{out}}}$. Assuming $V_\gamma = 0.5V$ and plugging $R = 8\Omega$ in Equation 4.2:

$$R_{eq} = 6.81\Omega \tag{4.3}$$

The lowest output power is set at $20W$, meaning that the maximum resistance is $R = 20\Omega$.

The equivalent resistance for this case is $R_{eq} = 17.02\Omega$.

Defining a minimum load is necessary to ensure proper voltage regulation across the entire load range, as the control system is designed to operate effectively within these conditions.

4.1.3 Compensating inductor

Previously, the advantages of Partially Damped Oscillations (PDO) and high quality factor (Q) were described. The selection of previous parameters was constrained, since the capacitance value is limited by the technology used and the output load is determined by the electrical requirements.

In contrast, the compensating inductor offers a better flexibility in its selection. The inductance must:

1. Set a high quality factor of the system
2. Ensure PDO operation in the desired load range.
3. Assure the ZVS conditions in the desired load range.

For the first condition:

$$Q = \frac{1}{R_{eq}}\sqrt{\frac{L}{C_{eq}}} \gg 1 \tag{4.4}$$

Solving for L:

$$L \gg R_{eq}^2 C_{eq} \tag{4.5}$$

The worst-case output power must be considered in Equation 4.5, since a good quality factor must remain at that condition. Therefore, $R_{eq} = 17.02\Omega$ is set in the equation:

$$L \gg 2.17\mu H \tag{4.6}$$

In engineering practice, a common design approach is to select an inductance value at least ten times greater than the calculated minimum:

$$L \geq 22\mu H \tag{4.7}$$

The final selection of this value involves a trade-off between a lower switching frequency -resulting in reduced switching losses- and better **Q** factor versus cost and inductor size and losses.

A higher inductance improves the **Q** factor, which is advantageous in frequency-based control due to increased sensitivity. Furthermore, a larger **L** value results in a lower resonance frequency, meaning a lower working switching frequency. This, in turn, decreases switching losses, improving overall efficiency.

However, increasing inductance also has drawbacks. A higher **L** leads to a bulkier and more expensive inductor. In addition, the need for longer and wider wires and larger core increases both core and copper losses, impacting negatively the overall efficiency.

As it was stated in Equation 4.7, **L** must be greater or equal than $22\mu H$. Therefore, it is useful to analyse the output voltage for different switching frequencies and inductances, keeping **C** constant and using the lowest power. For this case, standard inductance values are analysed and shown in Figure 4.1.

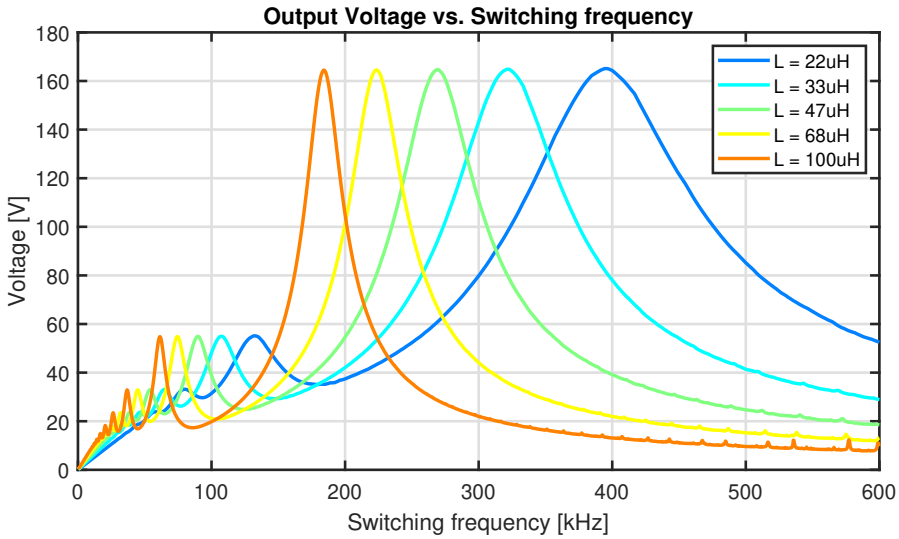


Figure 4.1: Output voltage as a function of the switching frequency, at $d = 50\%$, for different inductance values

A reasonable selection is $L = 33\mu H$, as it maintains a high **Q** factor while offering a more practical implementation compared to higher inductance values, balancing performance and manufacturability.

The resonance frequency, for $C = 15nF$ and $L = 33\mu H$ is $f_{res} = 320kHz$.

4.2 Static characteristic

Once all the parameters have been set, it is possible to plot the waveforms and analyse all the different situations that have been explained before. It will be useful to decide the switching frequency region that will be employed for both open-loop condition and closed-loop condition. All of them are obtained using the mathematical model described in Section 3.1.

4.2.1 Output voltage

In this subsection, the behaviour of the output voltage is analysed as function of the switching frequency. A frequency region must be selected that can comply all the previously mentioned requirements that are:

- $V_{out} = 20V$, for all load conditions.
- $P_{out_{max}} = 50W$
- ZVS operation

The parameters used are $V_{in} = 330V$, $R = 8\Omega$, $L = 33\mu H$, $C = 15nF$ and $d = 50\%$.

Figure 4.2 shows how the output voltage V_{out} varies with different switching frequencies. Its maximum value occurs at $f_{sw} = 320kHz$, which is the resonant frequency f_{res}. At lower frequencies, it can be seen that there are multiple peaks whose amplitude decay. These peaks are located exactly at the odd fractions of the resonance frequency and they are the sub-harmonic peaks, explained in Section 3.3. For a 50% duty cycle, these peaks are located at: $f_{subh} = \frac{f_{res}}{2k+1}$, for $k \in \mathbb{N}$

In order to comply with the requirement of V_{out}, there are three regions nearby the peaks that can reach the $20V$, which are the resonant peak, the third sub-harmonic peak and the fifth sub-harmonic peak. However, as the load resistance increases, the static characteristic of the system shifts, which may compromise the ability to achieve 20 V. This effect is analysed in more detail later.

For the resonant region, there are two possibilities, which are at $f_{sw} \approx 220kHz$ and $f_{sw} \approx 450kHz$. The second frequency is substantially high and switching and inductor losses will be significant, affecting the overall efficiency. Instead, the first frequency is reasonable. However, at that frequency, the initial inductor current I_0 will not comply the condition stated in Equation 3.38.

In Figure 4.3, the value of I_0 is shown for all switching frequencies.

It can be seen that for some frequency ranges, the initial current is positive, making the condition for maximum current expressed in Equation 3.38 not reachable, since ZVS can only be met with negative values.

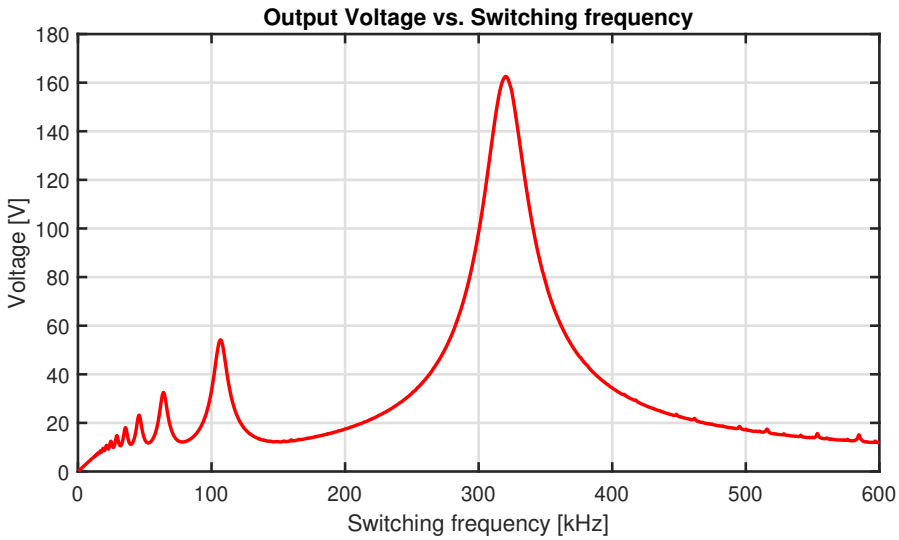


Figure 4.2: V_{out} vs. f_{sw}, with $R = 8\Omega$, $L = 33\mu H$, $C = 15nF$ and $f_{res} = 320\,\text{kHz}$

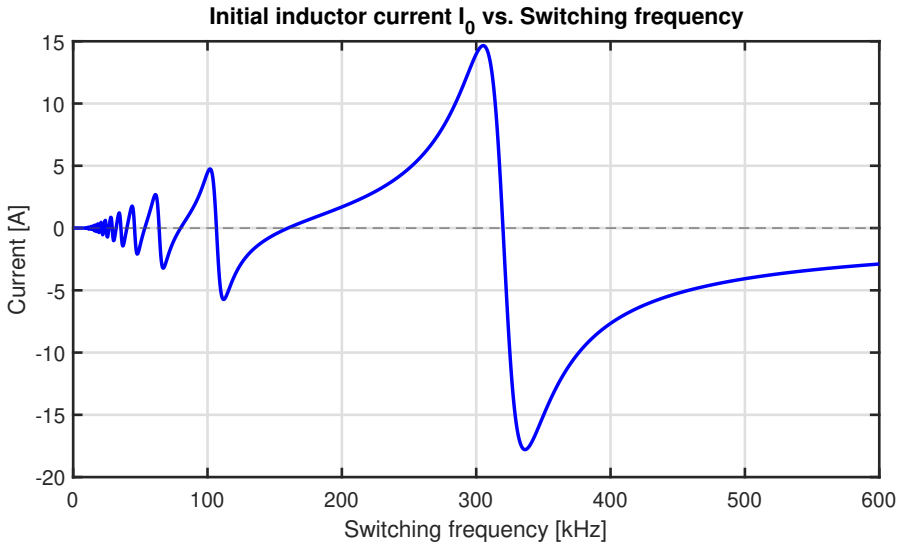


Figure 4.3: I_0 vs. f_{sw}, with $R = 8\Omega$, $L = 33\mu H$ and $C = 15nF$

These ranges, where the initial current is positive, occur between even fractions and odd fractions of the resonance frequency ($\frac{f_{res}}{2n} < f_{sw} < \frac{f_{res}}{2n+1}$, for $n \in \mathbb{N}$). Therefore, the operating switching frequency must be avoided in these ranges.

Instead, from odd to even fractions of the resonance frequency ($\frac{f_{res}}{2n+1} < f_{sw} < \frac{f_{res}}{2n}$, for $n \in \mathbb{N}$), the initial current is negative.

In Figure 4.2, those regions correspond to the right side of each sub-harmonic.

For this reason, working near the resonance peak is not convenient, even though

that, for $f_{sw} > f_{res}$, the initial current is negative and ZVS can be met. At that range, the switching losses are considerably high.

Therefore, for the parameters selected, there are two possible frequency regions which are:

1. $\frac{f_{res}}{5} < f_{sw} < \frac{f_{res}}{4}$: Right side of the fifth sub-harmonic.
2. $\frac{f_{res}}{3} < f_{sw} < \frac{f_{res}}{2}$: Right side of the third sub-harmonic.

The main advantage of working in the first region is that it allows a lower switching frequency. However, the drawback is the reduced output voltage and power swing. This is not convenient for Frequency Modulation control. In addition, the initial current is lower than in the second region, making it more challenging to achieve ZVS, especially at lighter loads.

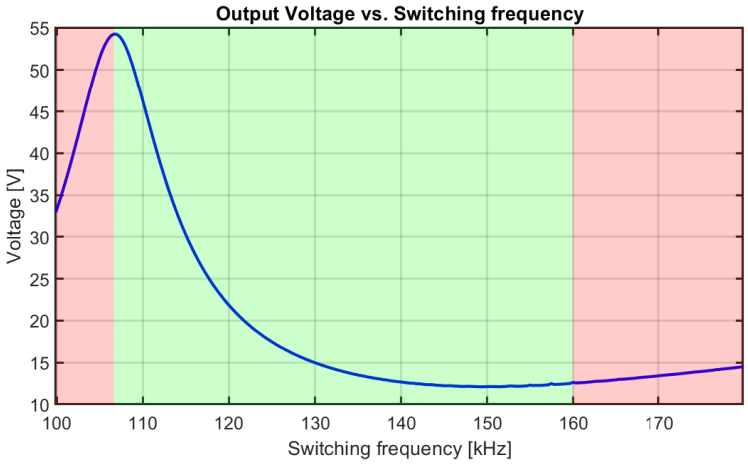
For this reason, the most appropriate working point is the second region, as it provides a higher output voltage and power swing and the increased initial current in this region facilitates ZVS operation.

Finally, the minimum and maximum switching frequency values are:

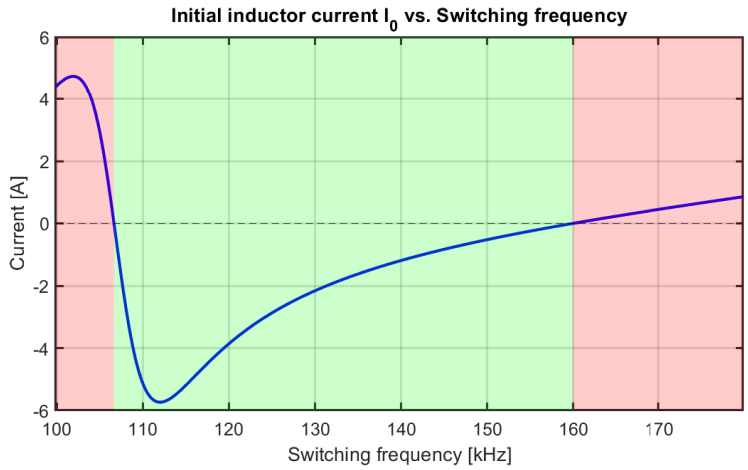
$$f_{sw_{min}} = \frac{f_{res}}{3} = 106.67kHz \tag{4.8}$$

$$f_{sw_{max}} = \frac{f_{res}}{2} = 160kHz \tag{4.9}$$

Figure 4.4 shows a zoomed-in view of the output voltage at the selected working frequencies. The green-shaded area represents the selected frequency range and the red-shaded areas are the discarded frequency regions.



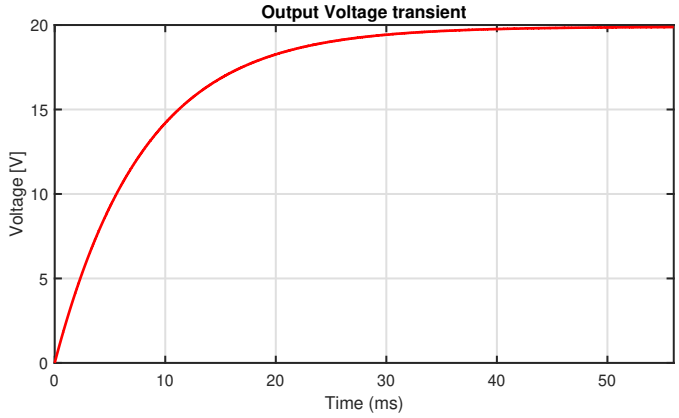
(a)



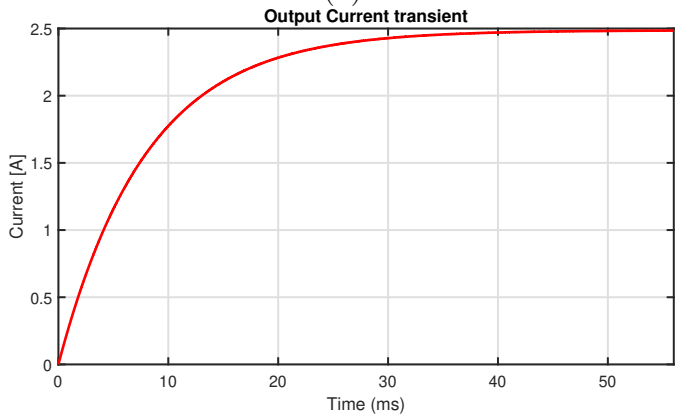
(b)

Figure 4.4: (a) Output voltage and (b) Initial inductor current zoomed-in at the selected frequencies

It can be seen, from Figure 4.4, that in order to achieve $V_{out} = 20V$ for $R = 8\Omega$, it is necessary to have a switching frequency around $f_{sw} = 122kHz$. Figure 4.5 shows both the output voltage and current transient, using the mentioned switching frequency and output capacitor $C_{out} = 1mF$.



(a)



(b)

Figure 4.5: (a) Output voltage and (b) output current transient at $f_{sw} = 122kHz$

4.2.2 Varying Q factor

If higher resistances are used, Q factor reduces significantly and there is a point where all sub-harmonics disappear and only the resonant peak remains, as shown in Figure 4.6.

These conditions correspond to the CDO mode, where the resonant capacitors store and release a fixed amount of energy and, as a consequence, the transferred power becomes independent from the load.

In this case, the working switching frequency should be selected to be greater than f_{res} if ZVS had to be reached. This causes high switching losses. This is the reason why working near the sub-harmonics is beneficial.

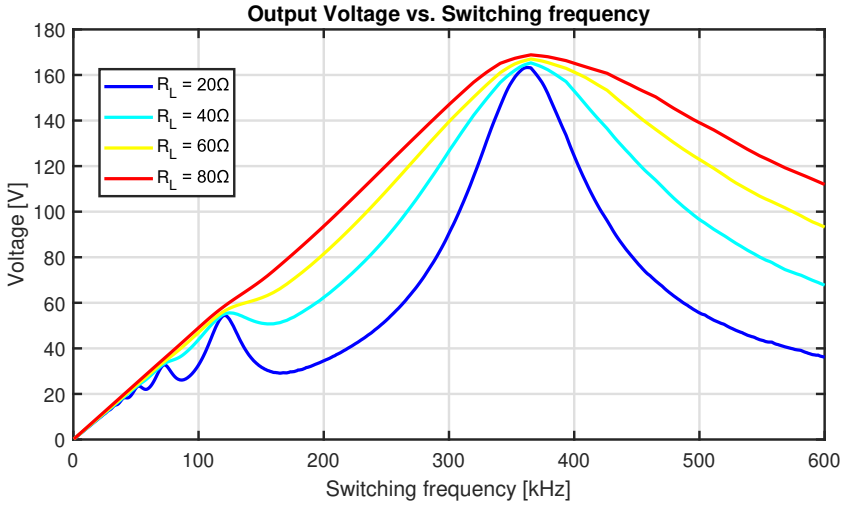
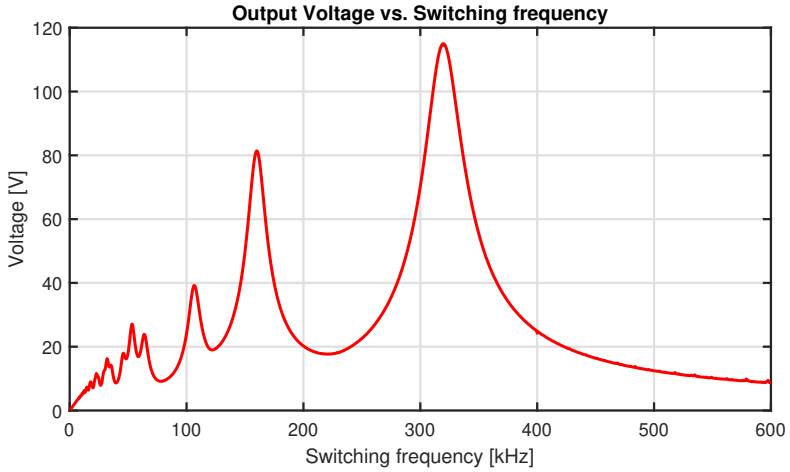


Figure 4.6: V_{out} vs. f_{sw}, with $R > 20\Omega$, $L = 33\mu H$ and $C = 15nF$

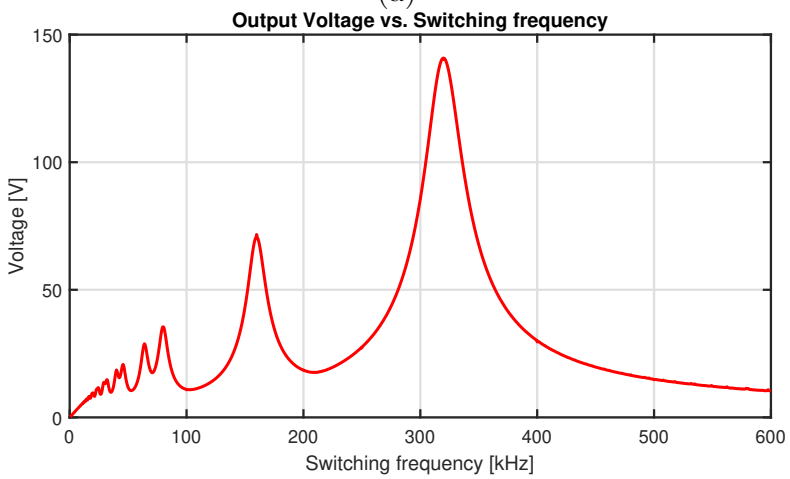
That is the reason why a proper inductor was selected for the worst-case power scenario. If the Q-factor at that operating point were too low, the sub-harmonics would be suppressed, eliminating the advantage of operating at that point.

4.2.3 Duty cycle variation

As it was explained in Section 3.3, when modifying the duty cycle of the switching node voltage, it will affect the gain curve, introducing and eliminating sub-harmonics depending on the selected duty cycle value. Figure 4.7 shows the output voltage curve for all switching frequencies. For 25% duty cycle, the frequencies that are fraction of 4 and its multiples of the resonant frequency ($\frac{f_{res}}{4}$, $\frac{f_{res}}{8}$, etc.) are suppressed, while other sub-harmonics, such as the second, third, remains. For 33.33% duty cycle, frequencies that are fraction of 3 and its multiples of the resonant frequency ($\frac{f_{res}}{3}$, $\frac{f_{res}}{6}$, etc.) are eliminated, while other sub-harmonics, such as the second, fourth, remains.



(a)



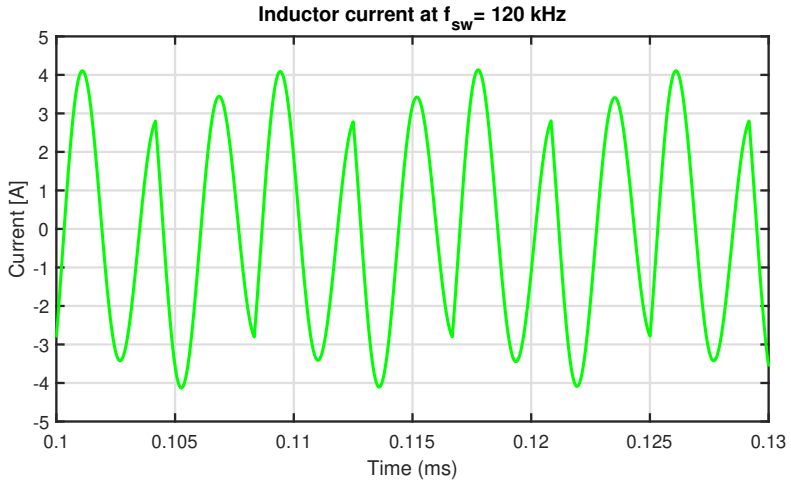
(b)

Figure 4.7: V_{out} vs. f_{sw} using (a) $d = 25\%$ and (b) $d = 33.3\%$

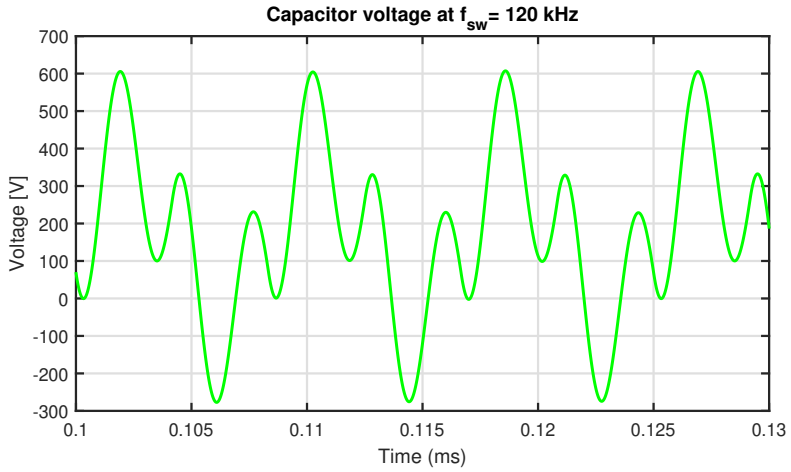
4.2.4 Inductor current and capacitor voltage

In this section, the inductor current i_L and capacitor voltage v_C waveforms are analysed. The capacitor voltage refers to the equivalent capacitance C_{eq} of the resonant tank, which results from the series combination of the two isolating capacitors. These waveforms are useful for the design and selection of components.

In Figure 4.8, $i_L(t)$ and $v_C(t)$ are shown at steady-state condition, using a load of $R = 8\,\Omega$ and a switching frequency of $f_{sw} = 120kHz$.



(a) Inductor current



(b) Capacitor voltage

Figure 4.8: $i_L(t)$ and $v_C(t)$ waveforms at $f_{sw} = 120$ kHz. Notice that the converter is operating in the PDO mode

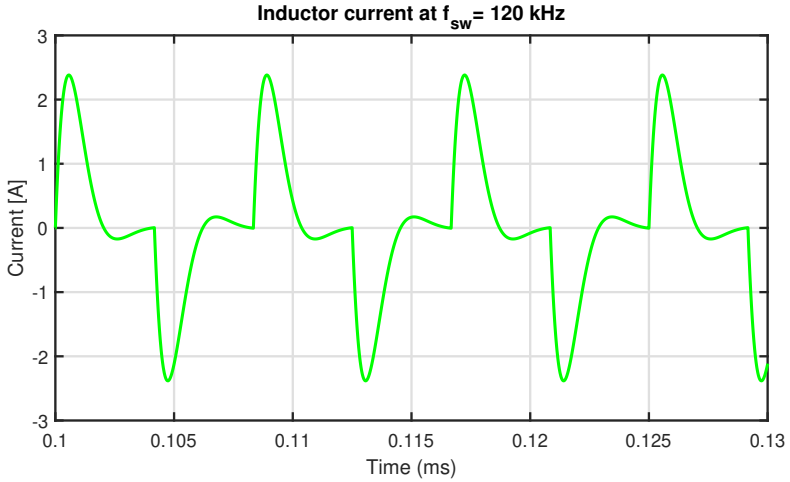
It can be seen that both i_L and v_C present partially damped oscillations, since the switching frequency used is higher than the limit of PDO stated in 3.28:

$$f_{sw} = 120kHz >> \frac{R_{eq}}{20L} = 10.32kHz \tag{4.10}$$

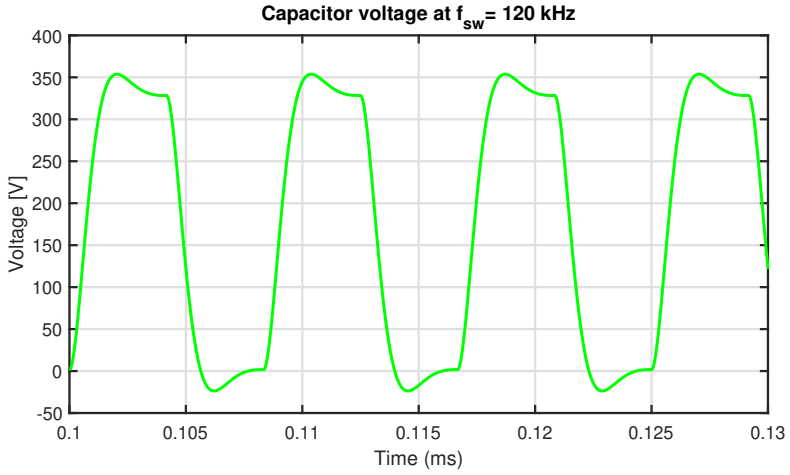
If a high R value is utilized, Q factor is worse and the CDO condition is more probable. For example, $R = 100\Omega$ is used. If the same frequency as before is used, the condition of PDO condition is not achieved:

$$f_{sw} = 120kHz < \frac{R_{eq}}{20L} = 128.95kHz \tag{4.11}$$

Figure 4.9 shows i_L and v_C in CDO condition, for the same load and switching frequency values.



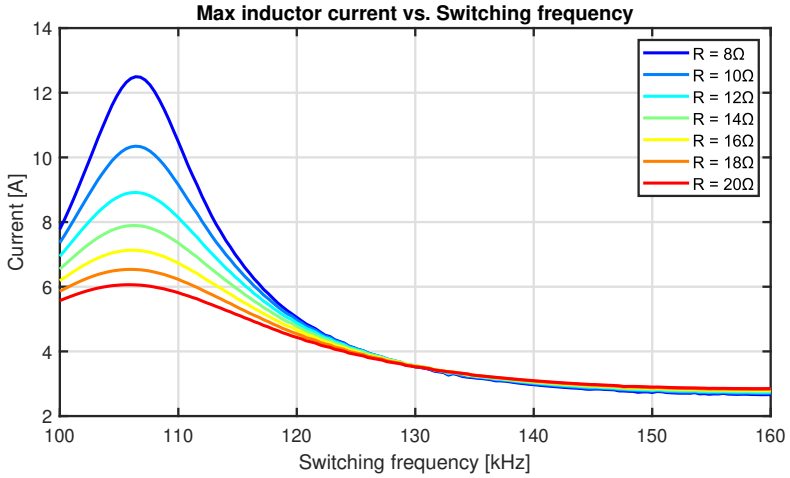
(a) Inductor current



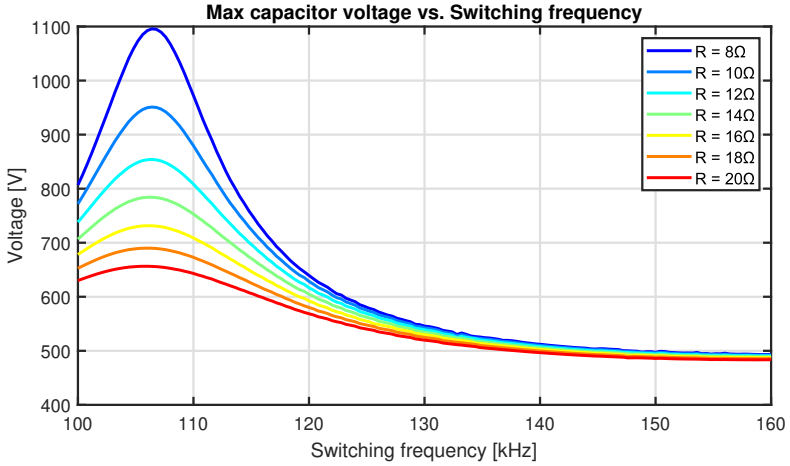
(b) Capacitor voltage

Figure 4.9: $i_L(t)$ and $v_C(t)$ waveforms at $f_{sw} = 120$ kHz. CDO condition

It is important to analyse the maximum values of both quantities, since it will be crucial for selecting components.



(a)

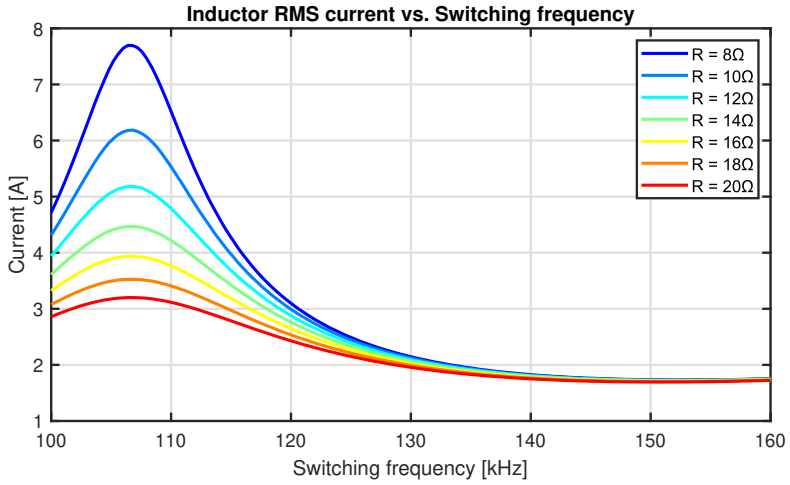


(b)

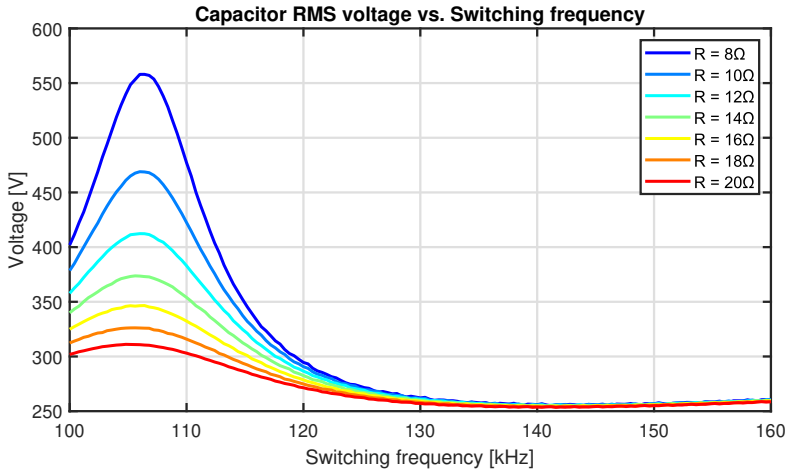
Figure 4.10: Peak values of (a) i_L and (b) v_C vs. f_{sw} for different R values

It can be seen that, for frequencies higher than $f_{sw} > 120kHz$, both peak inductor currents and peak capacitor voltages remain relatively similar for different R values. However, for $f_{sw} < 120kHz$, the peak values increases rapidly. Therefore, this behaviour must be considered for selecting the working frequency for both open-loop and closed-loop conditions.

Another important quantity is the RMS of both variables, which is depicted on Figure 4.11



(a)



(b)

Figure 4.11: RMS values of (a) i_L and (b) v_C vs. f_{sw} for different R values

4.3 Spice simulations

In this section, simulations of the circuit will be done in order to validate the waveforms made by the mathematical model and for a better understanding of the circuit. All the simulations have been done in LTSpice software [13].

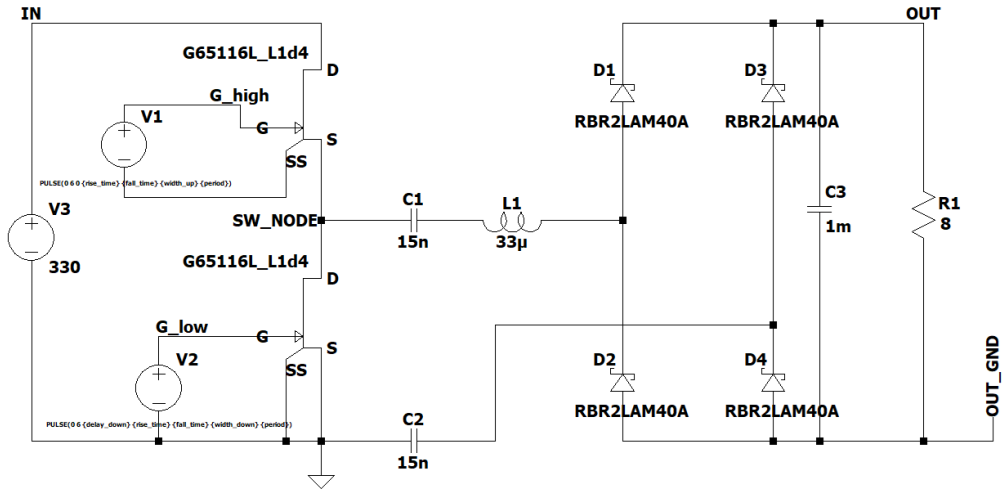


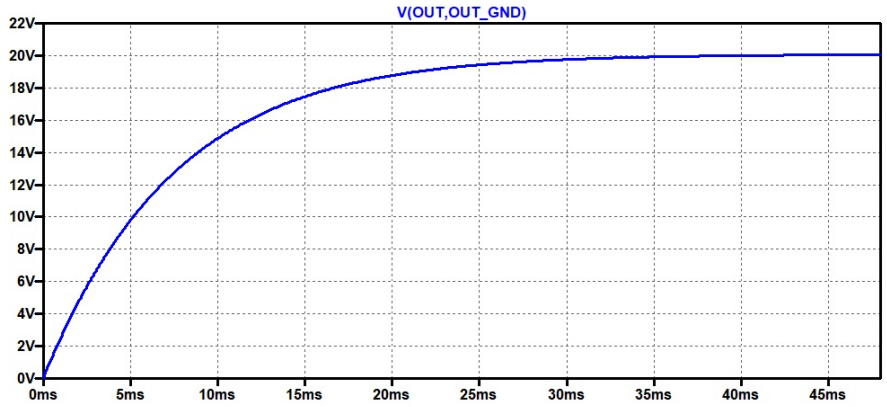
Figure 4.12: Circuit schematic for simulation

The schematic used for the simulations is show in Figure 4.12. A constant input voltage is considered. Additionally, inductor $\mathbf{L_1}$ and capacitors $\mathbf{C_1}$ and $\mathbf{C_2}$ are ideal, meaning they will not present active losses.

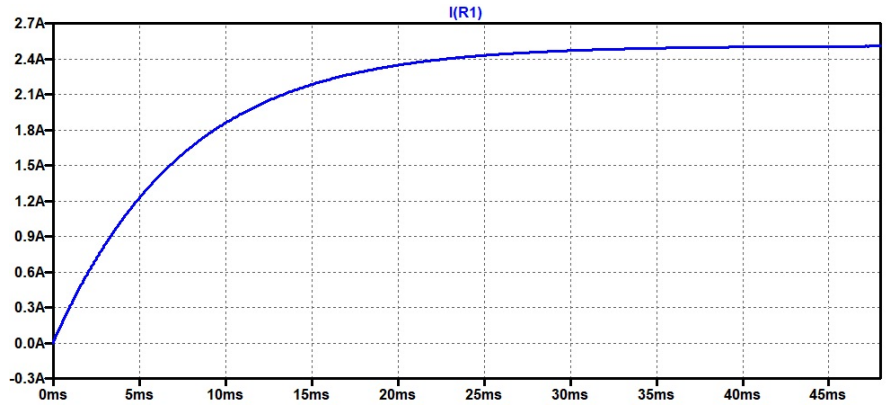
With these simulations, a verification of the previous waveforms will be done and additional checks as the ZVS.

For the Spice simulations, both transistors have an output capacitance C_{oss} equal to $20pF$.

Figure 4.13 shows the output voltage and current transient at $f_{sw} = 122kHz$. The response and final values are equal to the model, shown in Figure 4.5.



(a)



(b)

Figure 4.13: Output voltage transient from LTSpice

Figure 4.14 shows the switching node $v_{sw}(t)$, the inductor current $i_L(t)$ and the capacitor voltage $v_C(t)$ at $f_{sw} = 120kHz$ and a duty cycle of 50% in steady-state condition.

It can be seen that the waveforms match the model, both in shape and amplitude.

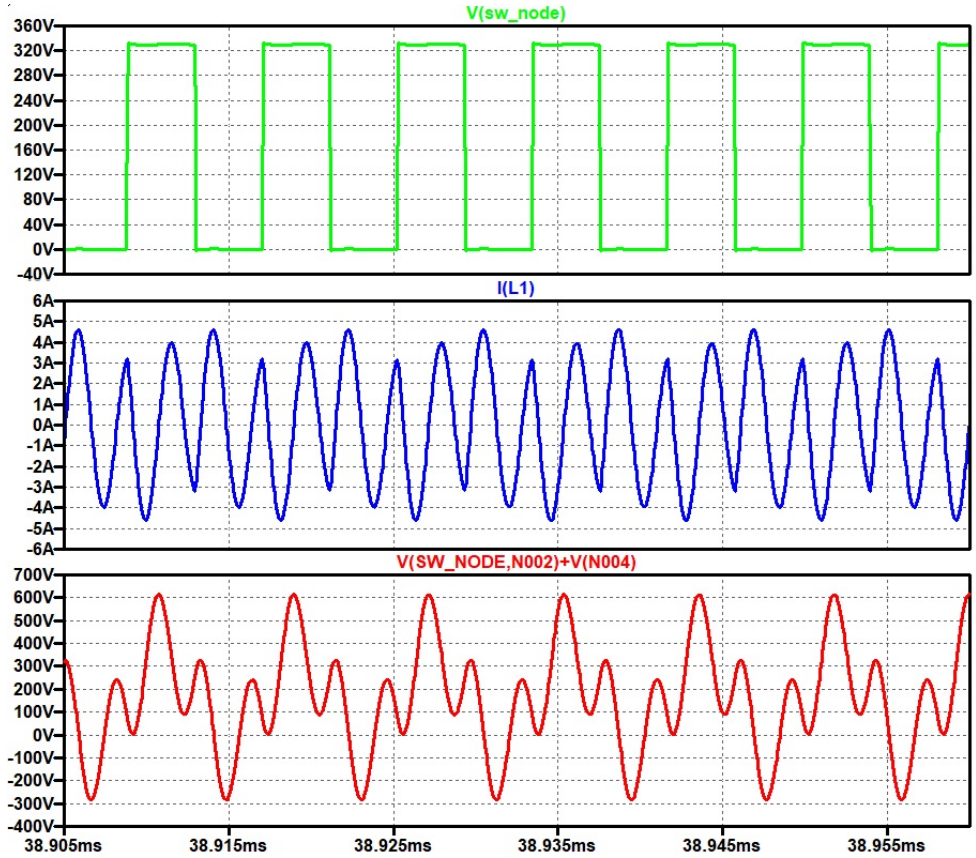


Figure 4.14: $v_{sw}(t)$, $i_L(t)$ and $v_C(t)$

4.3.1 ZVS verification

As it was stated previously, $C_{oss} = 20pF$, therefore, using the formulas obtained in the previous chapter, it is possible to verify if the ZVS is achieved.

The maximum initial current with the actual values of the simulation, using 3.39, is:

$$I_0 < -330\sqrt{\frac{2 * 20 * 10^{-12}}{33 * 10^{-6}}} = -363mA \tag{4.12}$$

The initial current is $I_0 = -3.2A$. Therefore the condition of maximum current is achieved.

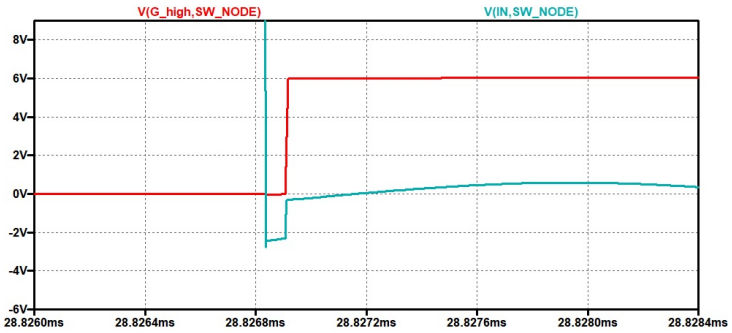
The minimum dead time to ensure ZVS is given by 3.45:

$$t_{dead_{min}} = \sqrt{2 * 20 * 10^{-12} * 33 * 10^{-6}} = 36.33ns \tag{4.13}$$

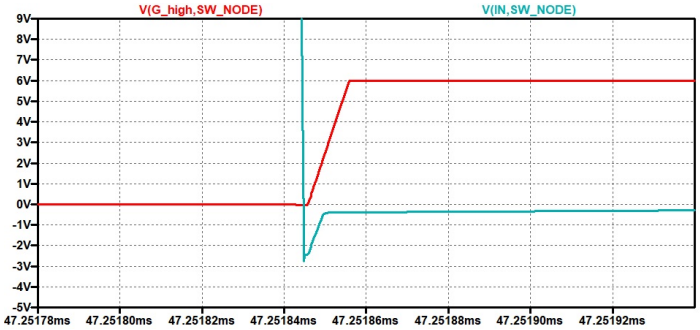
In order to check the previous statement, three dead time values will be used:

$t_{dead} = 100ns$, $t_{dead} = 30ns$ and $t_{dead} = 15ns$.

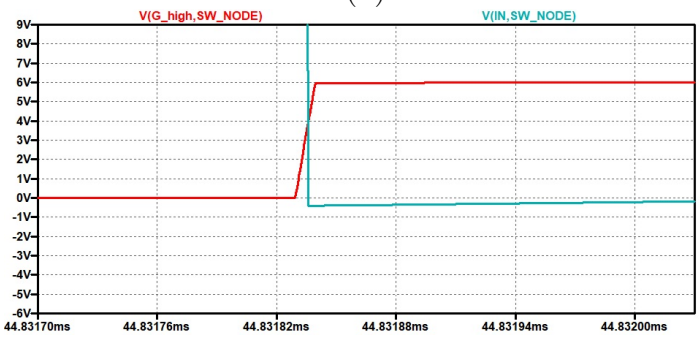
As stated previously, due to the symmetric operation at $d = 50\%$, it is sufficient to check the ZVS of the high-side transistor.



(a)



(b)



(c)

Figure 4.15: Hide-side FET $v_{DS}(t)$ and $v_{GS}(t)$ using (a) $t_{dead} = 100ns$, (b) $t_{dead} = 30ns$ and (c) $t_{dead} = 15ns$

Figure 4.15 shows high-side $v_{GS}(t)$ (in red) and $v_{DS}(t)$ (in blue) signals. ZVS occurs if v_{DS} reaches $0V$ before v_{GS} is ON.

- For the first case, with $t_{dead} = 100ns$, v_{DS} reaches $0V$ well before v_{GS} turns

ON and ZVS is achieved perfectly.

- For the second case, with $t_{dead} = 30ns$, it can be seen that it is the limit condition since v_{DS} reaches $0V$ at the moment v_{GS} is turning on.
- For the final case, with $t_{dead} = 15ns$, v_{DS} does not reach $0V$ before v_{GS} turns on, leading to a hard-switching condition.

Therefore, as demonstrated by the simulation results, Equation 3.45 is validated, confirming the minimum dead time required to achieve ZVS.

4.4 Ripple analysis

The output capacitor must ensure a reduced ripple and provide a stable DC voltage at the output. It must filter the high-frequency components introduced by previous stages, that are in the order of the switching frequency f_{sw} and its harmonics. In order to achieve this, the capacitance should be large enough to store sufficient charge and smooth out voltage variations.

The ESR of the capacitor introduces additional ripple due to the voltage drop across it, which must be accounted for in the design. A lower ESR helps to further reduce ripple and improve overall performance.

Figure 4.16 illustrates the effect of varying the value of C_{out} and its ESR on the output ripple with a constant input voltage of $V_{in} = 330V$.

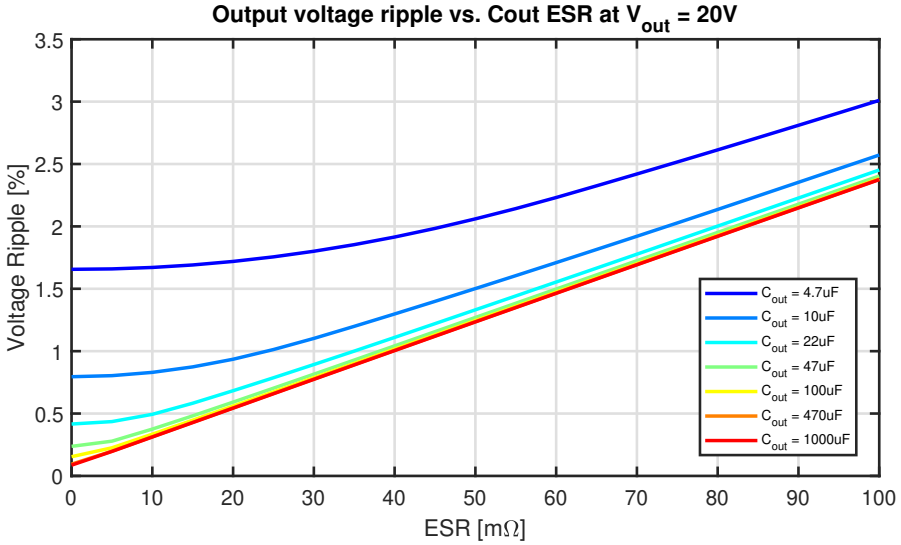


Figure 4.16: Output voltage ripple as a function of C_{out} and ESR at $V_{out} = 20V$ with $V_{in} = 330V$, $f_{sw} = 122kHz$ and $R = 8\,\Omega$.

It is important to mention that when selecting a commercial capacitor, higher capacitance values generally correspond to lower ESR.

This project uses the grid voltage as input. Therefore, a full-bridge rectifier is employed to convert the AC input into pulsating DC, followed by a filter capacitor C_{in} to smooth the voltage and reduce ripple. The complete circuit is depicted on Figure 4.17.

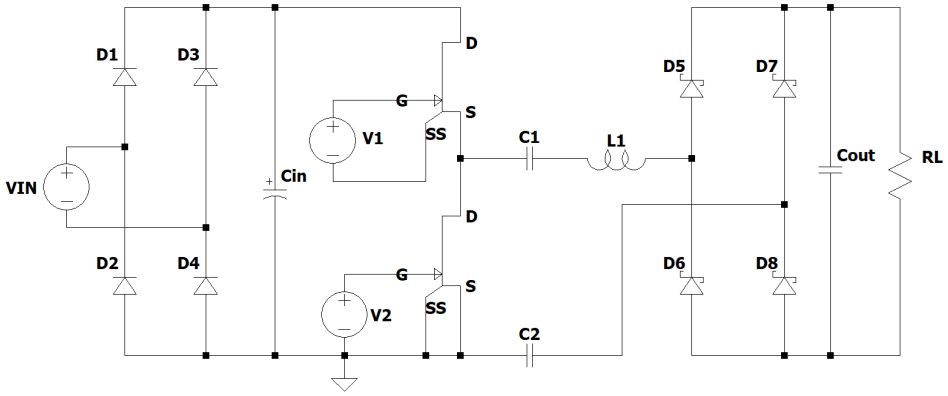


Figure 4.17: Complete circuit with grid voltage input.

The input stage introduces a low-frequency ripple, with frequency components at twice the grid frequency ($100Hz$) and its harmonics. Figure 4.18 shows the input voltage of the CPT circuit waveform.

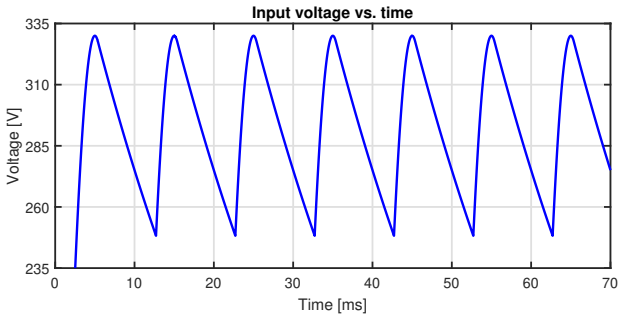


Figure 4.18: Input voltage of the CPT circuit

The output capacitor is chosen as $C_{out} = 1mF$ due to the reduced ripple in the load and low ESR compared to other values.

The input capacitor is chosen as $C_{in} = 22\mu F$, which is not sufficiently high to significantly reduce the input ripple on its own. However, this value represents a compromise, as the large capacitance of C_{out} also helps attenuate these ripple components.

Chapter 5

Control strategies

The importance of a control system lies in its ability to regulate a variable of the system under varying conditions. In any power adapter, perturbations can affect the performance of the system. Therefore, a well-designed controller is crucial for having a stable output and maintaining a high efficiency.

This chapter explores different control approaches, analysing their advantages, limitations and practical implementation. All the strategies must ensure stability, fast response and optimal efficiency.

The variable to control is the output voltage, which must be regulated at $20V$.

The perturbations are given by changes in the load R and the non-constant input voltage due to the ripple superimposed to the rectified grid voltage $V_{in}(t)$.

The control strategies to be analysed are:

- Frequency modulation (FM) control
- Pulse Width Modulation (PWM) control
- Bang-bang control
- Dyadic Pulse Modulation (DPM) control

At the end of the chapter, a comparison will be made between the different control strategies, evaluating their performance of voltage ripple, efficiency, response time, pointing out their advantages and disadvantages and the feasibility of implementation.

For all the controllers, the sampling frequency f_s will be equal to the switching frequency f_{sw}. That means that V_{out} is sampled once a switching period T_{sw} is completed.

5.1 Frequency modulation control

This control strategy consists in varying the switching frequency f_{sw} until a stable $20V$ is obtained. The duty cycle will be fixed at $d = 50\%$.

5.1.1 Frequency range

The first thing to set is the frequency range in which the controller operates. In section 4.2.1, the recommended frequency region for open loop has been identified. However, in this section, a more precise switching frequency region will be selected.

Figure 4.4 shows that there is no significant variation in the output voltage for switching frequencies in the $f_{sw} = 140kHz$ to $f_{sw} = 160kHz$ range. Therefore, this region can be not considered since it will not affect the output.

Thus, the upper switching frequency limit is $f_{sw} = 140kHz$.

For the lower limit, it is important to assure the minimum frequency in which the $20V$ is reached. In Figure 4.4, it is shown that the frequency which makes the output voltage to be the desired one is at $f_{sw} = 120kHz$ approximately.

The lower limit can be any value starting from $f_{sw} = \frac{f_{res}}{3}$. A frequency closer to this point allows to reach $20V$ faster. However, the higher currents in the circuit could be dangerous for the components.

Therefore, $f_{sw} = 120kHz$ is the most suitable lower limit, since it ensures the desired output voltage while being in a safe region.

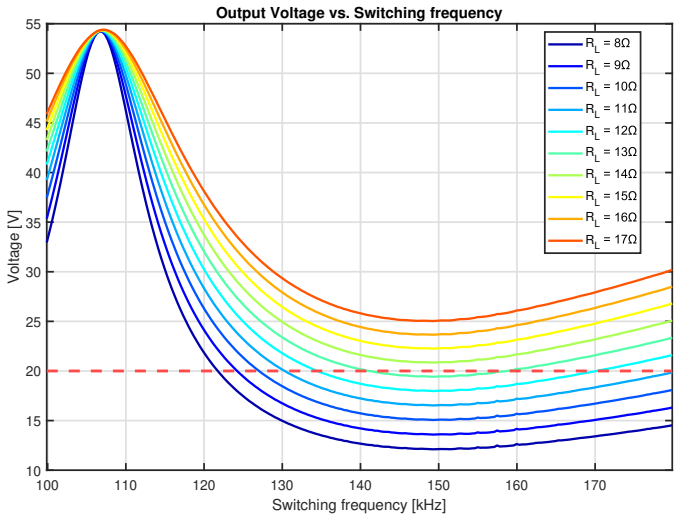


Figure 5.1: V_{out} vs. f_{sw}, varying load

The main limitation of this controller is the load variation. It was explained previously that increasing the output resistance, Q factor is worse. Figure 5.1

shows that for $R > 13\,\Omega$, there is no frequency for which the output voltage can reach $20V$.

Therefore, frequency control is effective only for load variations where $R < 13\Omega$. In other words, this controller is effective for powers greater or equal than $30W$ for $20V$.

5.1.2 System dynamics

In order to select the control strategy, it is useful to analyse the system dynamics behaviour. In previous section, the dynamics of the resonant tank has been explained.

The complete system is non-linear due to the introduction of the full-bridge rectifier. Therefore, it is not possible to obtain a transfer function expression. If that was the case, the controller design would be easier.

Instead, a method to approximate the system with a linear expression will be explored.

Simulations in LTSpice were made using $R = 8\Omega$, $C_{out} = 1mF$ and $V_{in} = 30V$. It should be clarified that the response is independent from voltage levels.

In Figure 5.2, the output voltage transient response to a step is shown. In this case, a step refers to the transition of the switching frequency from $0Hz$ to an active frequency.

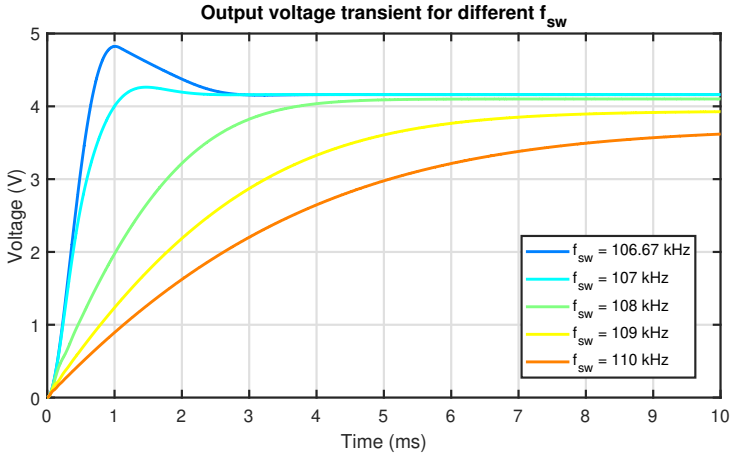


Figure 5.2: V_{out} transient for different f_{sw}

The frequencies used ranges from the third sub-harmonic peak frequency ($f_{sw} = 106.67kHz$) to $f_{sw} = 110kHz$. It can be observed that from $106.67kHz$ to $107kHz$, the output voltage presents overshooting and a faster response and settling time. While for higher frequencies, the response is completely damped.

For the first case, the behaviour of the response is similar to a second order system whose expression in Laplace domain is:

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{5.1}$$

For the second case, the response is similar to a first order system and the expression is:

$$H(s) = \frac{K}{\tau s + 1} \tag{5.2}$$

For the selected frequency range for control, that are from $120kHz$ to $140kHz$, the response is depicted on Figure 5.3.

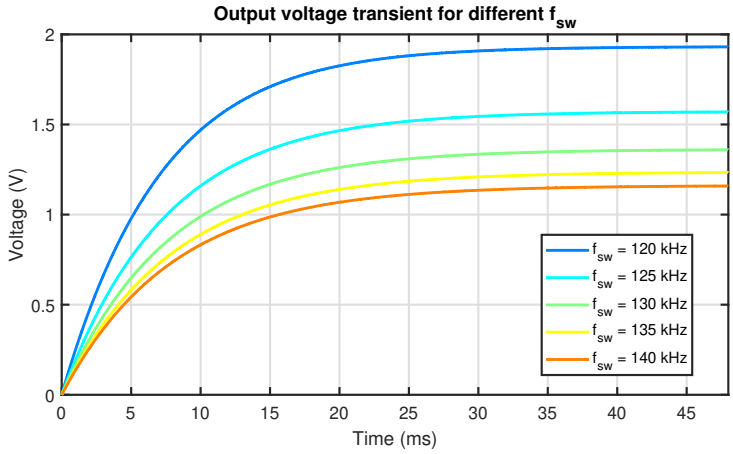


Figure 5.3: V_{out} transient selected frequency range

The response is completely damped for all cases. In addition, the settling time is equal.

The time constant τ is given by $R * C_{out}$ and the constant K depends on both f_{sw} and R. Therefore, the linear approximation of the system is given as:

$$H(s) = \frac{V_{out}(s)}{f_{sw}(s)} = \frac{K(R, f_{sw})}{RC_{out}s + 1} \tag{5.3}$$

5.1.3 PI controller

The error signal is the difference between the measured output voltage $V_{out}(t)$ and the reference and desired value, $V_{ref} = 20V$ in this case.

$$e(t) = V_{ref} - V_{out}(t) \tag{5.4}$$

The signal error is the input of the compensator, that will generate a control action $u(t)$ that will modify the switching frequency to obtain the desired output voltage.

Due to the first order nature of the system dynamics, it is convenient using a Proportional-Integral (PI) controller. A derivative (D) component will not be necessary, as it can introduce undesirable oscillations.

A PI controller consists of two parameters that are the proportional constant K_p and the integral constant K_i. The proportional component produces an output proportional to the actual error and the integral component considers the sum of previous errors and eliminates steady-state errors.

The control action $u(t)$ is given as:

$$u(t) = K_p e(t) + K_i \int_0^t e(\tau) d\tau \tag{5.5}$$

The compensator expression is the following:

$$C(s) = K_p + \frac{K_i}{s} \tag{5.6}$$

Defining $T_i = \frac{K_i}{K_p}$ called integral constant, the expression of the compensator can be rewritten as:

$$C(s) = K_p \frac{s + \frac{1}{T_i}}{s} \tag{5.7}$$

5.1.4 Control formula

Once the control action has been defined, it is important to derive a formula that relates the control action and produces the resulting switching frequency.

The limits of control action can be defined. The upper limit is $u_{max} = 1$ and $u_{min} = -1$. When $u(t)$ is positive means that the error is positive. Therefore $V_{out}(t)$ is below V_{ref}. Whereas, when $u(t)$ is negative, V_{out} is higher than V_{ref}.

For the first case, in which $V_{out} < V_{ref}$, more power must be delivered, which implies than a lower frequency has to be used. In contrast, when $V_{out} > V_{ref}$, less power must be supplied, which requires an increase in the frequency.

The expression that derives the switching frequency is the following:

$$f_{sw}(t) = \frac{f_{max} + f_{min}}{2} - u(t) \ \frac{f_{max} - f_{min}}{2} \tag{5.8}$$

Where $f_{min} = 120kHz$ and $f_{max} = 140kHz$. As $u(t)$ is constrained from -1 to 1, it is ensured that the switching frequency will be within the limits.

The block diagram of the closed-loop model for Frequency Modulation control is depicted on Figure 5.4

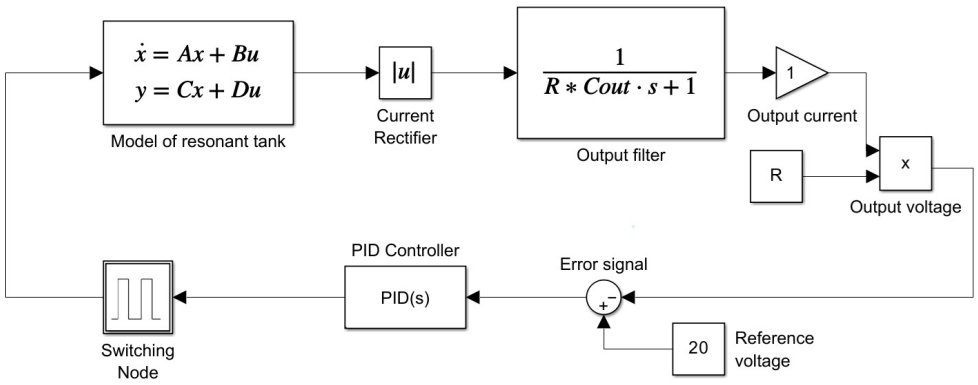


Figure 5.4: Block diagram for Frequency Modulation control

5.1.5 Selection of controller parameters

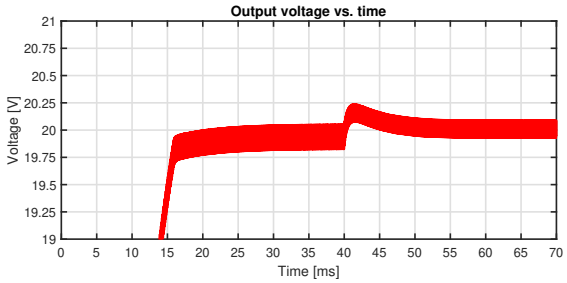
The PI controller parameters, k_p and k_i, must be selected to ensure a null steady-state error, low overshoot voltage and a fast response. A low k_p can result in overshoot when a load step occurs, whereas a higher k_p helps mitigate this. However, k_p must not be too large, as it can introduce oscillations in f_{sw} once the value is settled. Meanwhile, k_i is limited by the settling time, as higher values result in a slower response. Considering these trade-offs, the parameters are chosen to achieve a balance between response speed and stability.

As ESR of C_{out} increases, so does the ripple voltage in the load, as shown in Figure 4.16. This higher ESR introduces oscillations in the system, requiring a reduction in k_p to maintain stability.

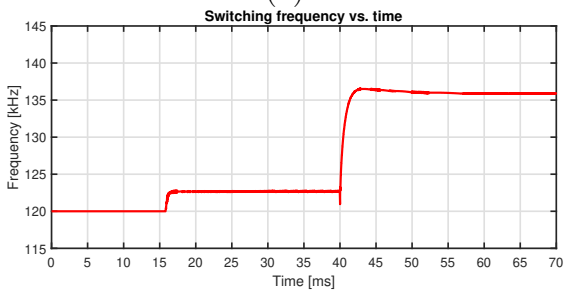
5.1.6 Simulations

Load Variation: Step and Ramp Changes

The simulation shown in Figure 5.5 is performed with an initial load of $R = 8\,\Omega$. At $t = 40ms$, a step change occurs, increasing the resistance to $R = 12\,\Omega$. In contrast, Figure 5.6 depicts a gradual transition, where R follows a ramp instead of an abrupt step. In both cases, the PI controller parameters are set to $k_p = 6$ and $k_i = 300$, ensuring a null steady-state error and a fast response.

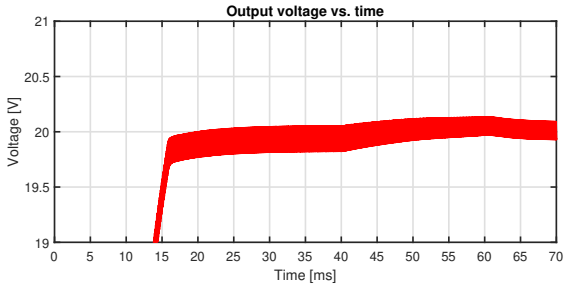


(a)

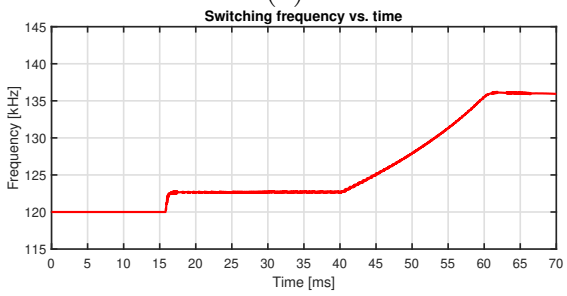


(b)

Figure 5.5: Frequency control: (a) V_{out} and (b) f_{sw} for a load step from $R = 8\Omega$ to $R = 12\Omega$



(a)



(b)

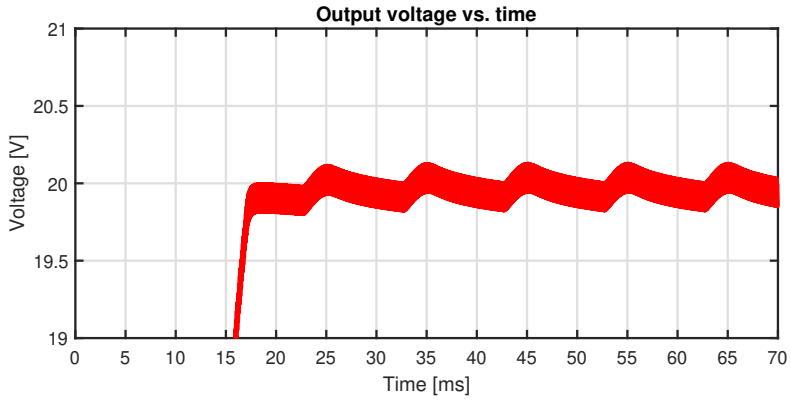
Figure 5.6: Frequency control: (a) V_{out} and (b) f_{sw} for a load ramp from $R = 8\Omega$ to $R = 12\Omega$

The switching frequency f_{sw} varies in response to V_{out}. When R increases, the output voltage rises, making an adjustment in f_{sw} to regulate V_{out} back to the reference value of 20 V.

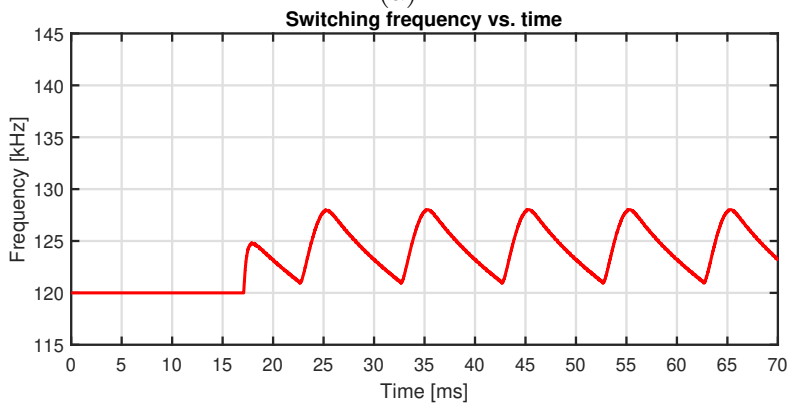
Sine wave input

Due to the rectified and partially filtered input sine wave, as depicted in Figure 4.18, a low-frequency ripple is introduced, causing V_{in} to vary instead of remaining constant. The controller is able to minimize this ripple changing f_{sw} accordingly.

Figure 5.7 shows the output voltage V_{out} using the rectified and partially filtered sine wave as V_{in}. It can be seen that f_{sw} varies in order to maintain V_{out} close to 20 V, compensating the fluctuations of input voltage V_{in}.



(a)



(b)

Figure 5.7: Frequency control: (a) V_{out} and (b) f_{sw} for a constant $R = 10\Omega$ with not constant V_{in}

Figure 5.8 shows a comparison of the output voltage ripple for open-loop (OL) and closed-loop (CL) condition. The open-loop response (blue) exhibits significant

voltage ripple due to the rectified sine wave input, with noticeable oscillations around the nominal output voltage. In contrast, the closed-loop response (red) effectively reduces the ripple, maintaining a more stable output voltage.

The ripple in open-loop condition is $V_{ripple} = 4.7\%$, whereas the closed-loop control reduces it to $V_{ripple} = 1.34\%$.

This demonstrates the effectiveness of closed-loop control in regulating the output and minimizing the ripple.

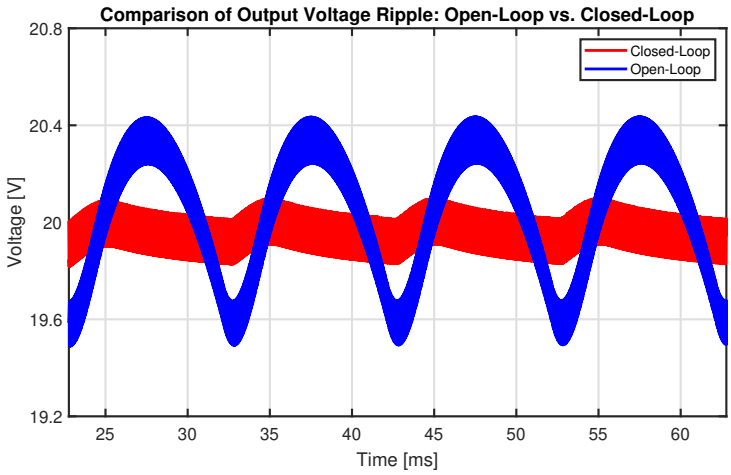


Figure 5.8: V_{out} comparison for Open-Loop and Closed-Loop

5.2 Pulse Width Modulation control

This control strategy consists in varying the duty cycle value d of the gate signals in order to regulate the output voltage.

This technique is utilized in various DC-DC converters such as the Buck converter.

In Section 3.3, the expression in Fourier series representation of the switching node voltage was presented and how duty cycle values variations alters its harmonic content of it and therefore, the sub-harmonic peaks of the output voltage, as depicted on Figure 4.7.

For this reason, when implementing a duty-cycle control strategy, it is crucial to consider this phenomenon.

The switching frequency for this strategy will be fixed at $f_{sw} = 120kHz$.

5.2.1 Duty cycle range

In order to decide the duty cycle values that will be used to modulate the output voltage, it is important to analyse its variation when the duty cycle is modified.

In Figure 5.9 it is shown how the output voltage varies when duty cycle and R are changed. This behaviour is due to the modulation of the sub-harmonics.

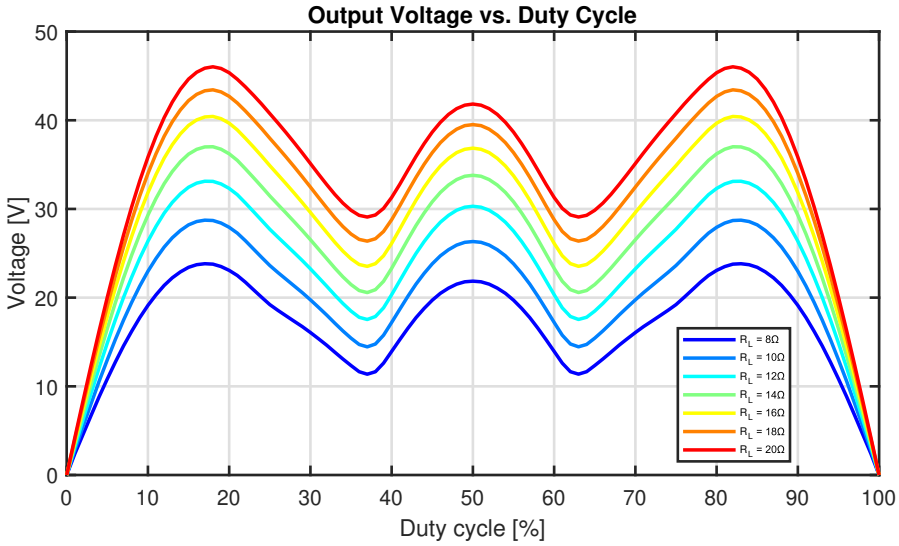


Figure 5.9: V_{out} vs. d at $f_{sw} = 120kHz$ and $R = [8; 20]\Omega$

It can be observed that the behaviour of the output voltage is symmetric with respect to $d = 50\%$. There are three maxima. A local maximum located at $d = 50\%$ and two absolute maxima at $d = 17\%$ and $d = 83\%$, for any R value.

With a constant duty cycle at 50%, the $20V$ is not reachable at $f_{sw} = 120kHz$ for any R value depicted. Therefore, duty cycle modulation is necessary. For $R \leq 12\Omega$, a modulation around the 50% peak allows reaching the $20V$ output. However, for $R > 12\Omega$, in order to reach the desired output voltage, the modulation must be done on the left of the 17% peak or on the right side of the 83% peak.

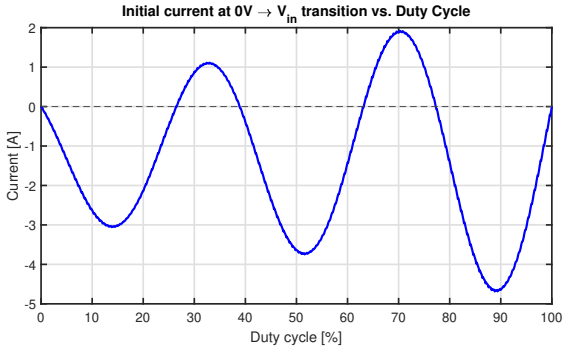
The advantage of this approach is that the desired $20V$ output can be achieved for any value of R unlike frequency-based control, which was highly restrictive.

Another important parameter to consider is the initial current I_0. In previous sections, when analysing the ZVS condition, a 50% duty cycle was assumed. For this value, it was sufficient to analyse the current at the $0V \rightarrow V_{in}$ transition of the switching node voltage as it is identical during the $V_{in} \rightarrow 0V$ transition. However, when $d \neq 50\%$ the current at both transitions must be analysed separately, as they are no longer equal.

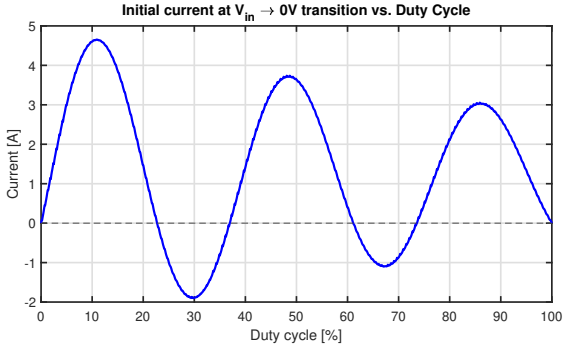
In order to have ZVS in the high-side transistor, inductor current i_L must be negative and comply with Equation 3.39 at $0V \rightarrow V_{in}$ transition. Additionally, in

order to achieve the ZVS in the low-side, the inductor current must be positive and meet the condition established in Equation 3.40 at $V_{in} \rightarrow 0V$ transition.

In Figure 5.10, the initial current I_0 is shown for different d values at a fixed f_{sw} and R for both transitions. In the top image, high-side transistor can achieve ZVS only for negative current values. Whereas, for the bottom image, the regions where low-side transistor achieves ZVS are the positive current values.



(a)



(b)

Figure 5.10: Initial inductor current at v_{sw} transitions vs. d at (a) $0V \rightarrow V_{in}$ and (b) $V_{in} \rightarrow 0V$

Therefore, in order to select a proper d range for the control, ZVS must be achieved for both transistors and the different situations are the following:

- $I_{0V \rightarrow V_{in}} > 0$ and $I_{V_{in} \rightarrow 0V} < 0$: ZVS is not achieved for any transistor
- $I_{0V \rightarrow V_{in}} < 0$ and $I_{V_{in} \rightarrow 0V} < 0$: ZVS in high-side transistor only.
- $I_{0V \rightarrow V_{in}} > 0$ and $I_{V_{in} \rightarrow 0V} > 0$: ZVS in low-side transistor only.
- $I_{0V \rightarrow V_{in}} < 0$ and $I_{V_{in} \rightarrow 0V} > 0$: ZVS achievable in both transistors.

The last situation is the desired one. Figure 5.11 shows both initial currents superimposed. It must be noted that the second curve was inverted to facilitate comparison. The green-shaded regions indicate the duty cycle ranges where the last condition is satisfied, meaning that ZVS is achieved for both transistors. Whereas, the red-shaded regions correspond to duty cycle values where ZVS is not achieved for at least one transistor.

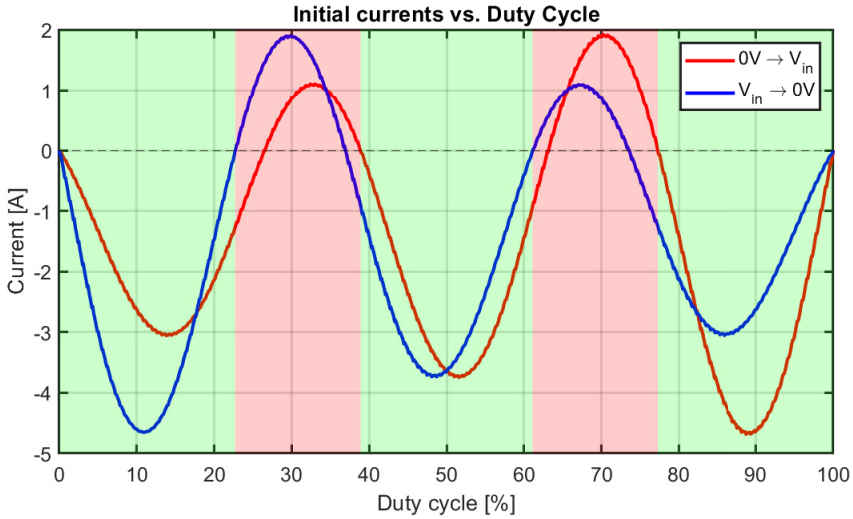


Figure 5.11: $I_{0V \to V_{in}}$ and $-I_{V_{in} \to 0V}$ vs. d at $f_{sw} = 120kHz$ and $R = 8\Omega$

The green-shaded regions correspond to the intervals $d \in [0; 23]\%$, $d \in [39; 61]\%$ and $d \in [77; 100]\%$

It can be observed that at $d = 50\%$, the initial currents coincide, as stated previously.

Finally, there are two duty cycle ranges that can reach both the desired output voltage and ZVS:

1. $0\% < d < 17\%$
2. $83\% < d < 100\%$

The output voltage varies symmetrically from $0V$ to its maximum achievable value, making both regions similar in terms of voltage swing. In terms of initial current, they are not equal and depending on the range used, the initial current will be higher for one transistor than the other.

Additionally, it is important to note that choosing one range over the other results in an imbalance in power dissipation since one of the transistors will be ON for more time respect to the other one.

5.2.2 Control formula

A PI controller is used to regulate d, for the same reasons as in Frequency Modulation control. Similarly, the control action is constrained within the range $u_{min} = -1$ to $u_{max} = 1$. When $V_{out} < V_{ref}$, more power must be delivered to the load, so duty cycle must get close to 17% peak, if first region is used or the 83% peak if second region is selected. On the other hand, when $V_{out} > V_{ref}$, power transfer must be reduced, meaning the duty cycle should move away from these peaks.

The expression that selects the duty cycle based on the control action is the following:

$$d(t) = \frac{d_{max} + d_{min}}{2} + u(t)\ \frac{d_{max} - d_{min}}{2} \tag{5.9}$$

Where $d_{min} = 0$ and $d_{max} = 17$ for the first range. For the second range, $d_{min} = 83$ and $d_{max} = 100$.

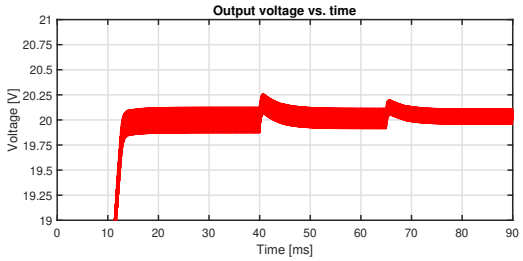
Equation 5.9 is valid for both duty cycle regions.

5.2.3 Simulations

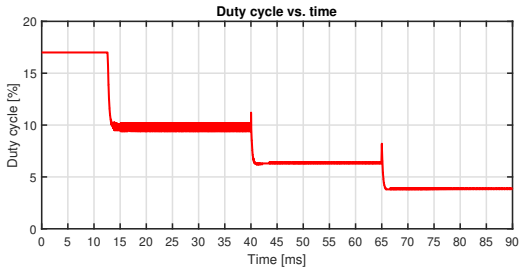
The following simulations are performed with $k_p = 3$ and $k_i = 300$.

Load Variation: Step and Ramp Changes

Figure 5.5 shows how the output voltage V_{out} is controlled by PWM for different step load changes. The simulation starts with $R = 8\,\Omega$ and changes at 40 ms to $R = 12\,\Omega$. Finally, at 70 ms, the resistance is $R = 25\,\Omega$. As explained before, this controller is able to work at any load, unlike frequency control.

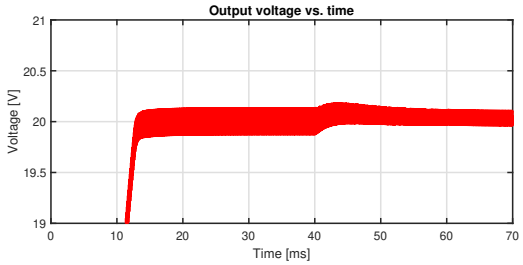


(a)

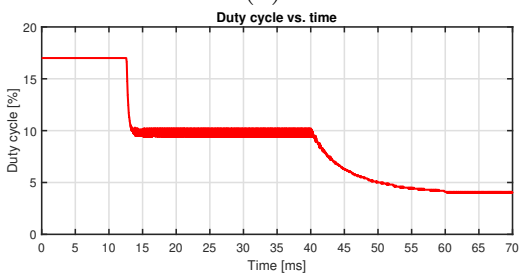


(b)

Figure 5.12: PWM control: (a) V_{out} and (b) d for a load step from $R = 8\,\Omega$ to $R = 12\,\Omega$ to $R = 25\,\Omega$



(a)



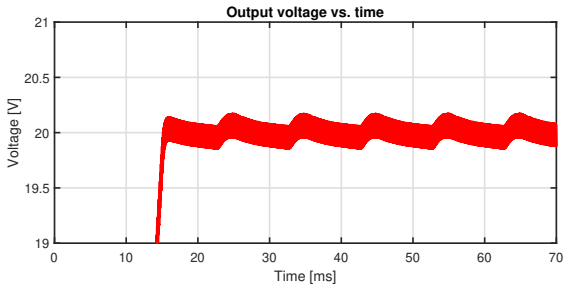
(b)

Figure 5.13: PWM control: (a) V_{out} and (b) d for a load ramp change from $R = 8\,\Omega$ to $R = 25\,\Omega$

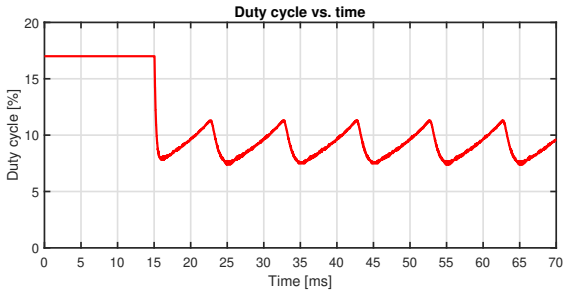
Figure 5.13 shows how duty cycle d reduces when R increases.

Sine wave input

Just as in frequency control, PWM control is also able to reduce the low-frequency ripple by dynamically adjusting the duty cycle d. By varying d, the controller compensates for fluctuations in V_{in}, ensuring that V_{out} remains close to 20 V.



(a)



(b)

Figure 5.14: PWM control: (a) V_{out} and (b) d for sine wave input

5.3 Bang-bang control

The bang-bang controller, also known as ON-OFF controller, operates by switching between two states depending on the variable to be controlled.

In Section 5.1, it has been analysed that there is a maximum R value that can be used to get the desired $20V$ output voltage for the selected frequency range at a fixed $d = 50\%$. In contrast, Section 5.2 showed that this limitation is eliminated by varying the duty cycle. However, a significant power imbalance for both transistor occurs due to the extreme duty cycle values required.

Bang-bang controller operates at a fixed switching frequency and duty cycle, alternating between two states: ON and OFF.

- **ON state**: Switching node voltage at frequency and duty cycle constant, delivering power to the load.
- **OFF state**: Switching node voltage at a constant value ($0V$ or V_{in}), where one of the transistor is ON while the other remains OFF.

The system switches between ON and OFF states based on the actual value of V_{out} and its trend. The sequence is explained as follows:

- If V_{out} is increasing and the upper voltage threshold (V_{up}) is reached, the system switches to OFF state and V_{out} decreases.
- Once V_{out} reaches the lower voltage threshold (V_{low}), the system switches to ON state, causing V_{out} to rise again.

This cyclical behaviour is called hysteresis. Figure 5.15, illustrates an example of the output voltage waveform, showing the variations between ON and OFF states, as described. Output voltage oscillates between V_{up} and V_{low}. In this representation, high-frequency ripple is ignored for clarity.

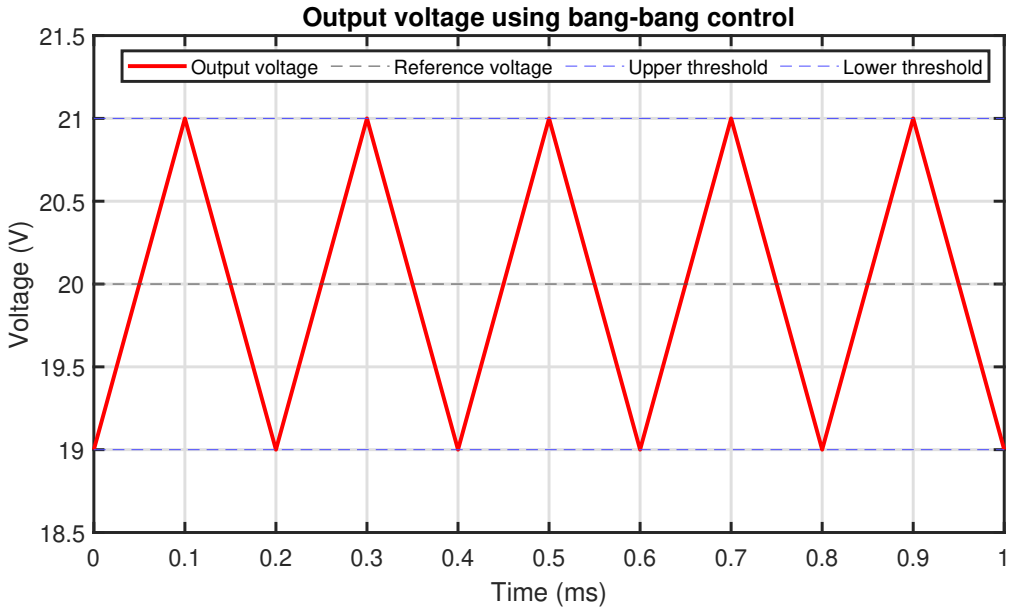


Figure 5.15: $V_{out}(t)$ using a bang-bang controller

V_{up} and V_{low} can be adjusted to set the desired ripple amplitude.

Unlike the previous controllers, bang-bang control does not require a control action signal to realize the control. Instead, it directly monitors V_{out} and switches states accordingly. In Figure 5.16, the block diagram of the complete system using bang-bang control is shown.

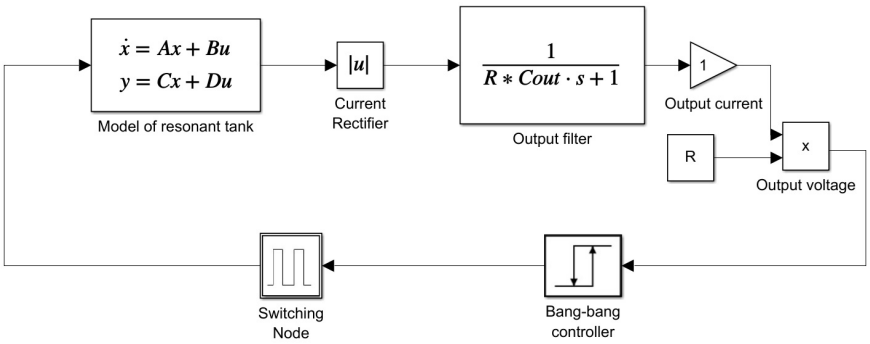


Figure 5.16: Closed-loop block diagram using bang-bang controller

A key advantage of this controller is its simple implementation. However, one drawback is the transition from the OFF to the ON state, which causes high transient peaks in the inductor current and capacitors voltage and can lead to high stresses on the components.

A possible solution to mitigate these peaks is to initialize the ON state with a higher frequency, meaning lower power delivery. Then, the system can gradually shift to the nominal switching switching. This reduces significantly the peaks generated at the OFF-ON transition.

5.3.1 Simulations

The following simulations will be done with the thresholds set at $V_{up} = 20.2V$ and $V_{low} = 19.8V$. Therefore, the expected ripple is exactly $V_{ripple} = 400mV_{pp}$.

The thresholds are chosen based on the system's response. If they are too small, the system must react rapidly to switch ON and OFF. The main constrain is the switching period T_{sw}, as each cycle must be completed before a state change can occur, preventing switching in the middle of T_{sw}.

Load Variation: Step and Ramp Changes

Figure 5.17 presents the output voltage V_{out} under bang-bang control, showing how the system responds to changes in load. The initial load is $R = 8\,\Omega$ and, at 40 ms, it changes at $R = 12\,\Omega$. Finally, at 70 ms, load changes to $R = 30\,\Omega$. In contrast, Figure 5.18 shows V_{out} for a ramp change in R. It starts at $R = 8\,\Omega$ and finishes at $R = 30\,\Omega$.

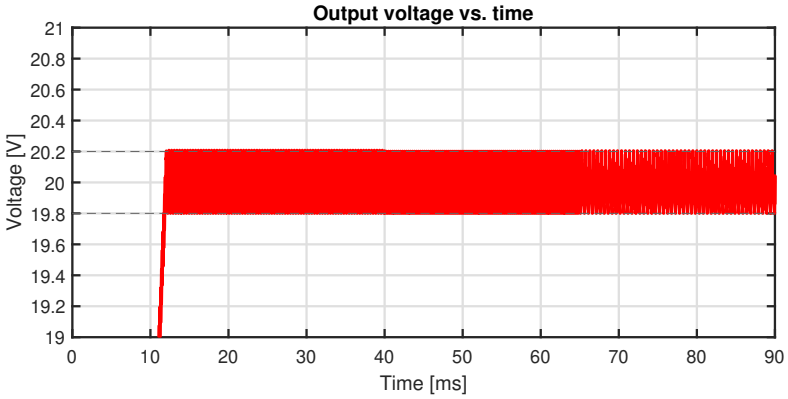


Figure 5.17: Bang-bang control: V_{out} for load step changes from $R = 8\,\Omega$ to $R = 12\,\Omega$ to $R = 25\,\Omega$

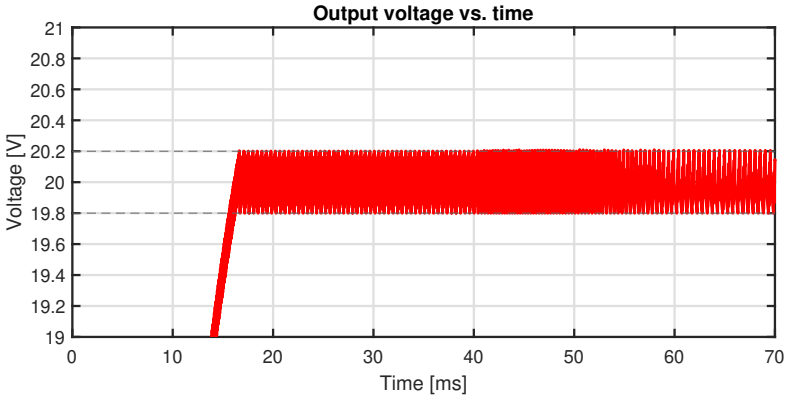


Figure 5.18: Bang-bang control: V_{out} for load ramp changes from $R = 8\,\Omega$ to $R = 25\,\Omega$

Sine wave input

As explained previously, the controllers must be able to minimize the low-frequency ripple introduced by the input. Figure 5.19 shows how V_{out} remains within the thresholds for a sine wave input.

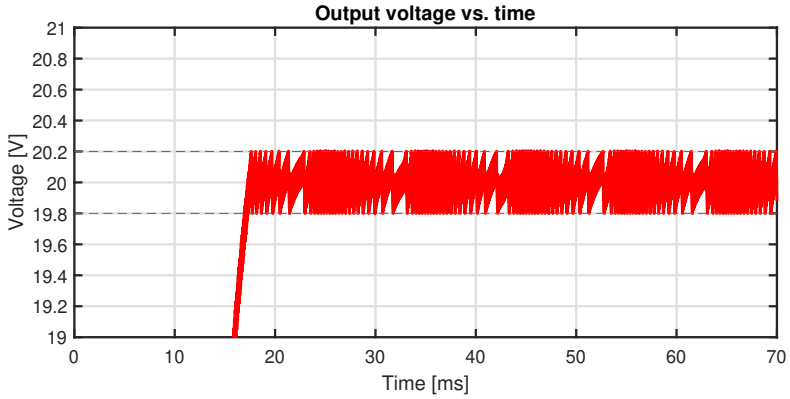


Figure 5.19: Bang-bang control: V_{out} with sine wave input for $R = 10\,\Omega$

Figure 5.20 shows a zoomed-in view of the switching node voltage $v_{sw}(t)$ being ON or OFF.

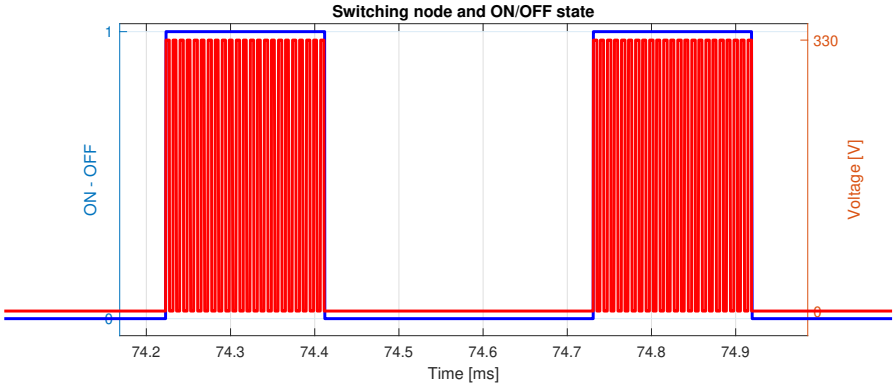


Figure 5.20: $v_{sw}(t)$ and ON-OFF state

5.4 Dyadic Pulse Modulation control

In bang-bang control, the ripple was determined by the selection of the upper and lower voltage threshold, resulting in an output voltage waveform similar to a triangular waveform.

In this section, an alternative approach will be presented. Instead of completely turning off the circuit when the output voltage is higher than the reference, some switching pulses are skipped and distributed uniformly, maintaining the desired output voltage at the reference with minimized ripple.

This modulation technique, known as Dyadic Pulse Modulation, was mathematically explained in detail in [14].

In order to regulate the output voltage, the previously described PI controller can be used to determine the quantity of pulses to be skipped. The extreme values of the control action $u(t)$ was $u_{min} = -1$ and $u_{max} = 1$. For implementing the Dyadic Pulse Modulation, it is necessary to use a value denoted as n which determines the pulses to be skipped and ranges from 0 to $(2^N) - 1$, where N represents the number of bits. Therefore a range conversion must be done with the following expression:

$$n(t) = round(\ \frac{1 - u(t)}{2}\ (2^N - 1)\ ) \tag{5.10}$$

The number n determines which pulses in the switching sequence should be active and an algorithm is employed to uniformly distributed the pulses.

As it was explained previously, when $V_{out} < V_{ref}$, $u(t)$ is positive. And when $V_{out} > V_{ref}$, $u(t)$ is negative. If $u(t) = u_{max}$, maximum power must be delivered and n is equal to 0, meaning no pulse is skipped. Conversely, when $u(t) = u_{min}$, no power must be transferred and n equals $2^N - 1$ and no pulse occurs.

Figure 5.21 shows how the output voltage varies with respect to the number of skipped pulses n, using $N = 8$:

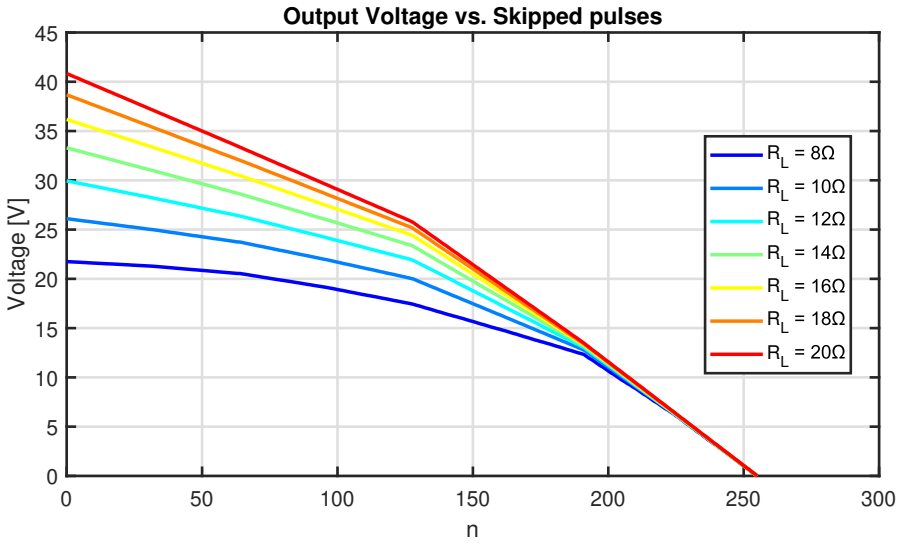
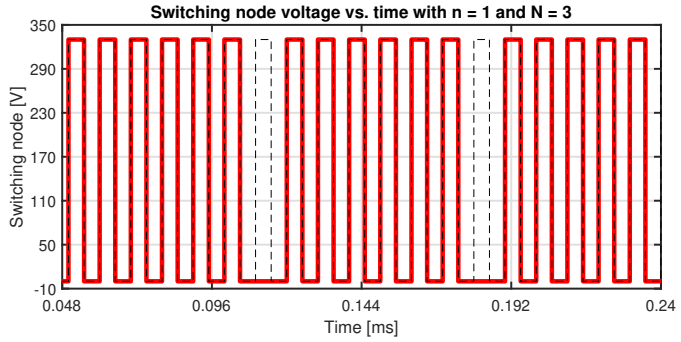


Figure 5.21: Output voltage as a function of skipped pulses n with $N = 8$ for different loads

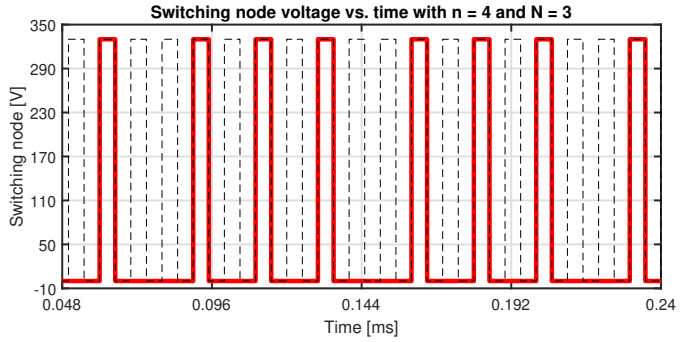
It can be observed that when $n = 0$, meaning that no switching pulse is skipped, the output voltage is maximum, for all load conditions. If $n = 2^N - 1$, all switching pulses are skipped and output voltage is $0V$.

Similar to PWM and bang-bang control, it is possible to reach $20V$ for all load conditions.

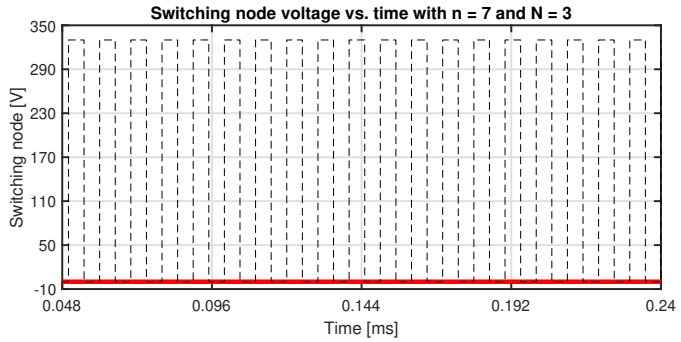
In figure 5.22, the switching node voltage is depicted for different values of n using $N = 4$.. When $n = 1$, a single pulse is skipped in every $2^N - 1 = 7$ switching pulses. For $n = 4$, four pulses are skipped, distributed uniformly across the cycle. When $n = 7$, al pulses are skipped, resulting in no voltage at the switching node.



(a)



(b)



(c)

Figure 5.22: Switching node voltage $v_{sw}(t)$ for (a) $n = 1$(b) $n = 4$ and (c) $n = 7$

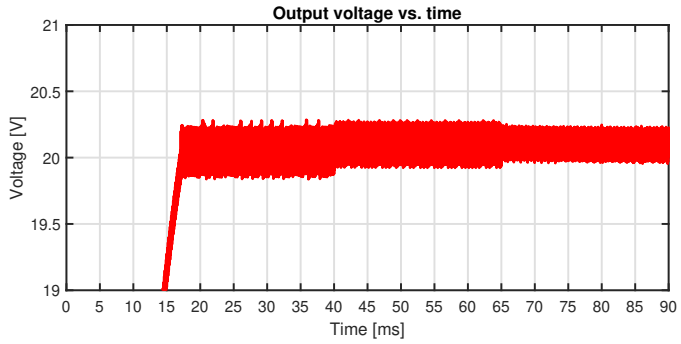
5.4.1 Simulations

For DPM control, in addition to k_p and k_i, another parameter, N, must be selected. This parameter determines the number of switching pulses in one cycle, given by 2^N.

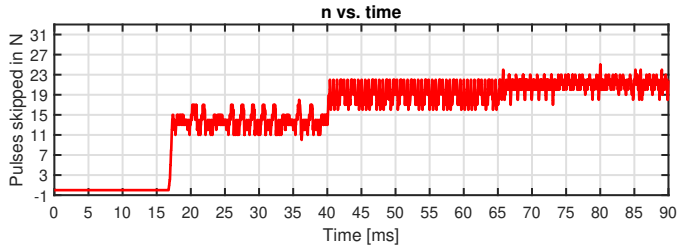
The selection of k_p and k_i depends on the stability of n as well as the overshoot and settling time of V_{out}. If k_p is too low, n will have small variations. However, when R changes, this can result in a high overshoot and a shorter settling time. Therefore, a trade-off is necessary. Additionally, k_i must be high enough to have null steady-state error.

The parameters chosen for the simulations are $k_p = 15$, $k_i = 200$ and $N = 5$.

Load Variation: Step and Ramp Changes

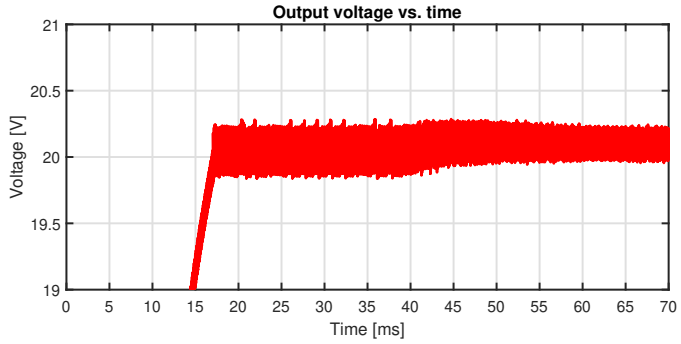


(a)

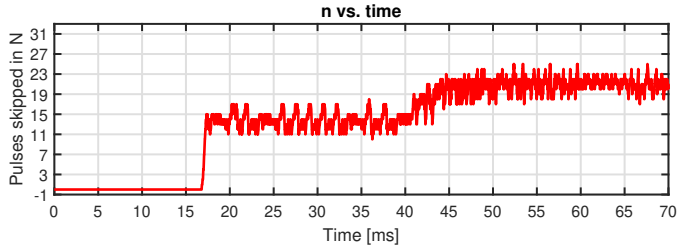


(b)

Figure 5.23: DPM control: V_{out} for load step changes from $R = 8\,\Omega$ to $R = 12\,\Omega$ to $R = 25\,\Omega$



(a)



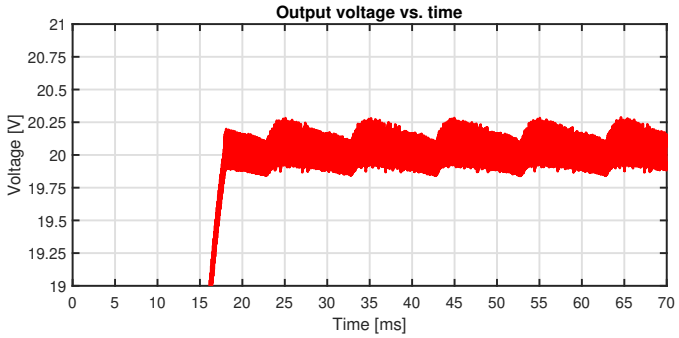
(b)

Figure 5.24: DPM control: V_{out} for load ramp changes from $R = 8\,\Omega$ to $R = 25\,\Omega$

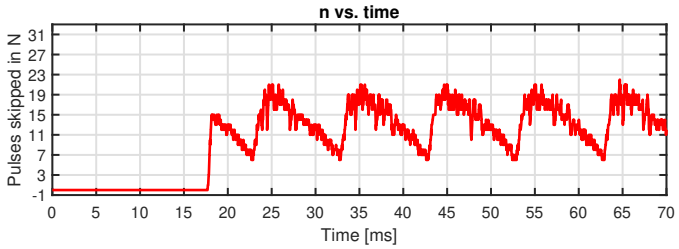
Figure 5.23 and 5.24 shows how the skipped pulses are modified when a change in R occurs, maintaining V_{out} at 20 V

Sine wave input

Similarly to previous controllers, DPM control is able to minimize the low-frequency ripple, as it can be seen in Figure 5.25.



(a)



(b)

Figure 5.25: DPM control: V_{out} for load step changes from $R = 8\,\Omega$ to $R = 12\,\Omega$ to $R = 25\,\Omega$

5.5 Comparison

This section presents a comparison in terms of voltage ripple, overshoot and settling time.

5.5.1 Ripple

In terms of voltage ripple, the FM and PWM controllers exhibited the lowest values, measuring 220 mV (1.1%) and 240 mV (1.2%) respectively. It can be observed that high-frequency ripple, caused by the ESR of C_{out} increases for lower values of R. Bang-bang control maintains a constant voltage ripple across all conditions, with a value of 400 mV (2%). The highest voltage ripple was observed in the DPM controller, reaching 490 mV (2.45%).

5.5.2 Overshoot

Overshoot represents the maximum V_{out} value reached during a load step change. In this comparison, the resistance R steps from $R = 8\,\Omega$ to $R = 12\,\Omega$.

FM and PWM strategies present overshoot values of 230 mV and 260 mV respectively, which are within acceptable limits. In contrast, bang-bang and DPM show no overshoot.

5.5.3 Settling time

The settling time is the duration required for V_{out} to stabilize to the reference value of 20 V after a load step.

FM and PWM exhibit settling time values of 15 ms and 10 ms respectively. Whereas bang-bang and DPM present null settling time.

Table 5.1 provides a summary of the control strategies, highlighting their characteristics in terms of ripple, control parameters, load range, settling time, and overshoot. This table consolidates the key aspects discussed in the previous sections.

Table 5.1: Comparison among the implemented control strategies.

Control strategy	Control variable	Frequency / Duty cycle	Controller type	V_{out} ripple	Controller parameters	Load range	Settling time	Overshoot
FM	Switching frequency f_{sw}	Variable / Fixed	PI	1.1%	$k_p = 6$ $k_i = 300$	Limited (8–13)Ω	15 ms	0.23 V
PWM	Duty cycle d	Fixed / Variable	PI	1.2%	$k_p = 3$ $k_i = 300$	Full	10 ms	0.25 V
BB	ON-OFF switching	Fixed / Fixed	Hysteresis	2%	$V_h = 20.2$ V $V_l = 19.8$ V	Full	null	null
DPM	Switching pulses n	Fixed / Fixed	PI	2.45%	$k_p = 15$ $k_i = 200$	Full	null	null

Chapter 6

Selection of components and board design

This chapter focuses on the design and selection of the components for the circuit implementation. With the operating points, component values and maximum ratings determined in previous analysis, it is possible to select real components which must ensure reliable operation under the expected conditions.

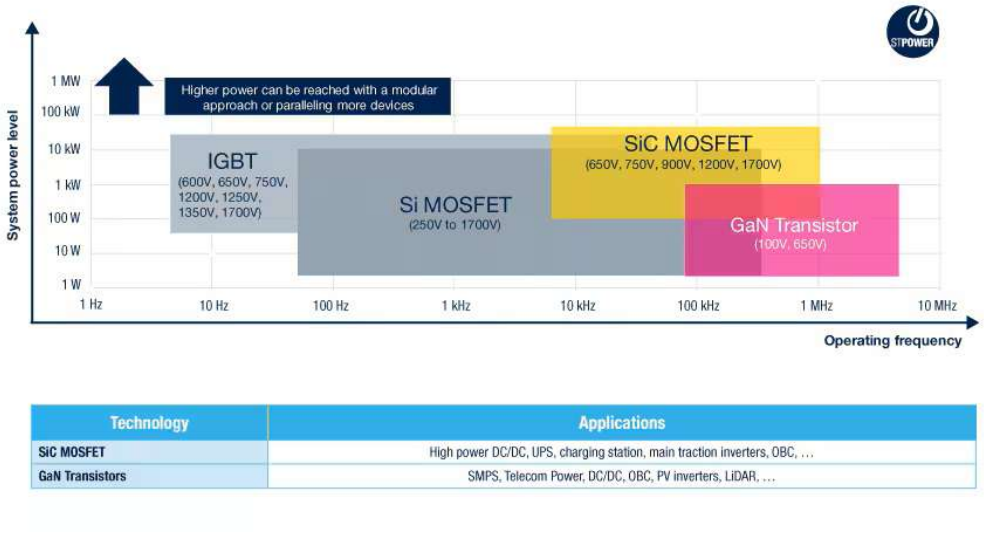
6.1 Selection of components

6.1.1 Half-bridge inverter

When designing a half-bridge inverter, it is important to select the optimal technology for the transistors in order to achieve high efficiency and performance.

Wide bandgap transistors, such as Silicon Carbide (SiC) MOSFETs and Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs), offer significant advantages over the traditional silicon transistors in terms of high switching frequency, reduced power losses and thermal performance.

Figure 6.1, available in [15], shows a comparison of the technologies for different operating frequencies and maximum power and voltages.



Technology	Applications
SiC MOSFET	High power DC/DC, UPS, charging station, main traction inverters, OBC, …
GaN Transistors	SMPS, Telecom Power, DC/DC, OBC, PV inverters, LiDAR, …

Figure 6.1: Wide bandgap transistors

In order to select the most suitable technology for this project, the maximum ratings of the design must be considered and are the following:

- $V_{DS_{max}} = 330V$
- $f_{max} = 140kHz$
- $I_{DS_{peak}} = 6A$

For this project, GaN HEMTs were chosen as the transistor technology for the half-bridge inverter, due to its reduced switching losses and high switching speed compared to SiC MOSFETs.

When selecting a half-bridge rectifier, two options are available: using two separate, but equal, transistors with independent gate drivers or opting for an integrated system-in-package chip that combines the transistors and the gate drivers in a single package. The main advantage of the second option is that it simplifies the circuit design and reduces parasitics.

In this design, the MASTERGAN1 from STMicroelectronics [16] is chosen as it meets all the requirements. In Figure 6.2 is shown all the features of this system-in-package. Furthermore, Figure 6.3 shows the schematic of the system. It can be seen that both drivers and transistors are embedded.

Features

- 600 V system-in-package integrating half-bridge gate driver and high-voltage power GaN transistors:
  - QFN 9 x 9 x 1 mm package
  - $R_{DS(ON)}$ = 150 mΩ
  - $I_{DS(MAX)}$ = 10 A
- Reverse current capability
- Zero reverse recovery loss
- UVLO protection on low-side and high-side
- Internal bootstrap diode
- Interlocking function
- Dedicated pin for shutdown functionality
- Accurate internal timing match
- 3.3 V to 15 V compatible inputs with hysteresis and pull-down
- Overtemperature protection
- Bill of material reduction
- Very compact and simplified layout
- Flexible, easy and fast design.

Figure 6.2: MASTERGAN1 features

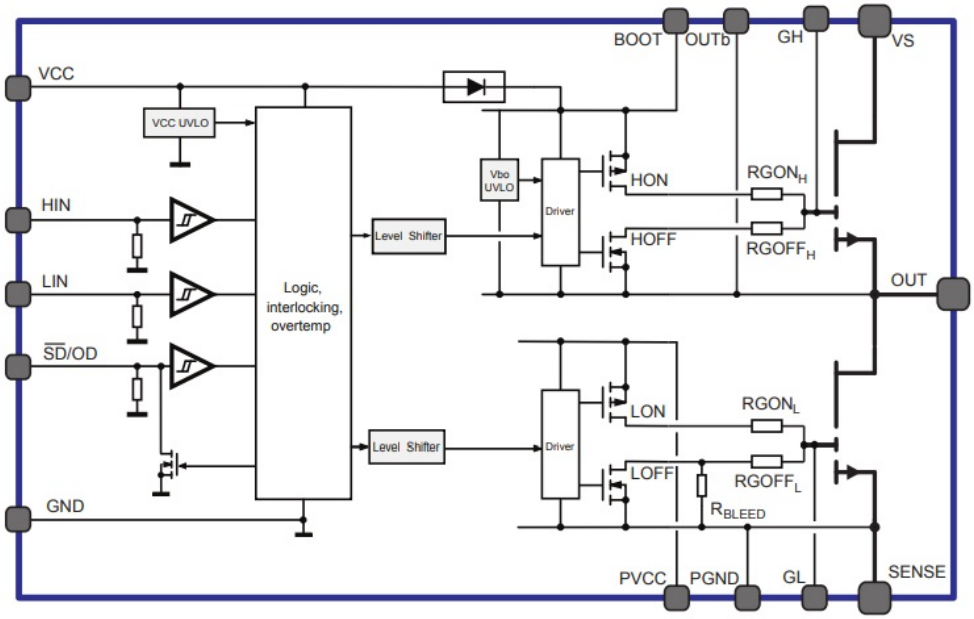


Figure 6.3: MASTERGAN1 schematic

The output capacitances of the transistors are $C_{oss} = 20pF$, being the same value used in the simulation. Therefore, ZVS will be reached easily with the decided dead time of $100ns$.

The ON resistance is $R_{DS(ON)} = 150m\Omega$, which must be considered for the loss calculation.

Table 6.1 shows a comparison of the design requirements and the characteristics of the selected component.

QUANTITY	REQUIREMENT	ACTUAL
Drain-Source Voltage MAX	$330V$	$600V$
Drain-Source Current MAX	$6A$	$10A$
Drain-Source ON Resistance	order of $m\Omega$	$150m\Omega$
Output Capacitance	below $100pF$	$20pF$
Switching Frequency MAX	$140kHz$	higher than $500kHz$

Table 6.1: Transistors requirements and characteristics.

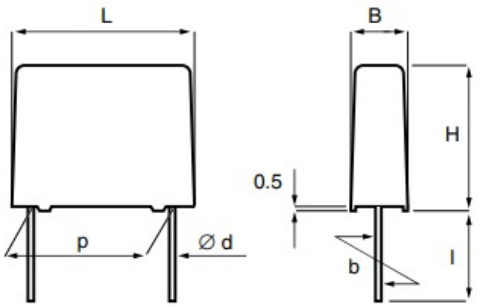
6.1.2 Interface capacitors

The interface capacitors are a crucial component of the circuit, as they provide the galvanic isolation in the circuit. A Y-type capacitor is a suitable selection due to its safety features, reducing the risk of electric shock, ensuring circuit protection and user safety.

The maximum rating for the capacitors are:

- $v_{C_{rms}} = 200V$
- $v_{C_{peak}} = 400V$

For this design, PHE850EB5150MB15R17 Y-capacitor from Kemet is chosen due to its safety characteristics and the compliance with the voltage requirements. In Figure 6.4 (a), the dimension of the interface capacitor is depicted and Figure 6.4 (b) shows the technical data.



p	d	std l	max l	b
10.0 ± 0.4	0.6	17	30	±0.4
15.0 ± 0.4	0.6/0.8*	17	30	±0.4
22.5 ± 0.4	0.8	6	30	±0.4
27.5 ± 0.4	0.8	6	30	±0.4
37.5 ± 0.5	1.0	6	30	±0.7

(a)

TECHNICAL DATA	
Rated voltage	300 VAC, 50/60 Hz (ENEC,UL,cUL)
Capacitance range µF	0.001–1.0
Temperature range °C	–55/+110
Climatic category IEC	55/110/56/B
Capacitance tolerance	± 20% standard, other tolerances on request
Approvals	ENEC, UL, cUL
Dissipation factor tanδ	Maximum values at +23 °C 1 kHz: C ≤ 0.1 µF: 0.2%; 0.1 µF < C ≤ 1 µF: 0.15% 10 kHz: C ≤ 0.1 µF: 0.3%; 0.1 µF < C ≤ 1 µF: 0.4% 100 kHz: C ≤ 0.1 µF: 0.6%; 0.1 µF < C ≤ 1 µF: –
Insulation resistance	C ≤ 0.33 µF: ≥ 30 000 MΩ C > 0.33 µF: ≥ 10 000 s
Resonance frequency	Tabulated self-resonance frequencies f_0 refer to 5 mm lead lengths.
Test voltage between terminals	The 100% screening factory test is carried out at 5000 VDC and 2500 VAC. The voltage level is selected to meet the requirements in applicable equipment standards. All electrical characteristics are checked after the test.
In DC applications	Recommended voltage: ≤ 1250 VDC

(b)

Figure 6.4: PHE850EB5150MB15R17: (a) Dimensions, (b) Technical data

The equivalent series resistance (ESR) of the capacitor can be obtained using the $tan\delta$ factor shown in Figure 6.4. As the operating frequency is higher than $100kHz$, $tan\delta = 0.6\%$

$$ESR(f) = \frac{tan\delta}{2\pi fC} \tag{6.1}$$

In Figure 6.5 it is shown how the ESR varies with the frequency.

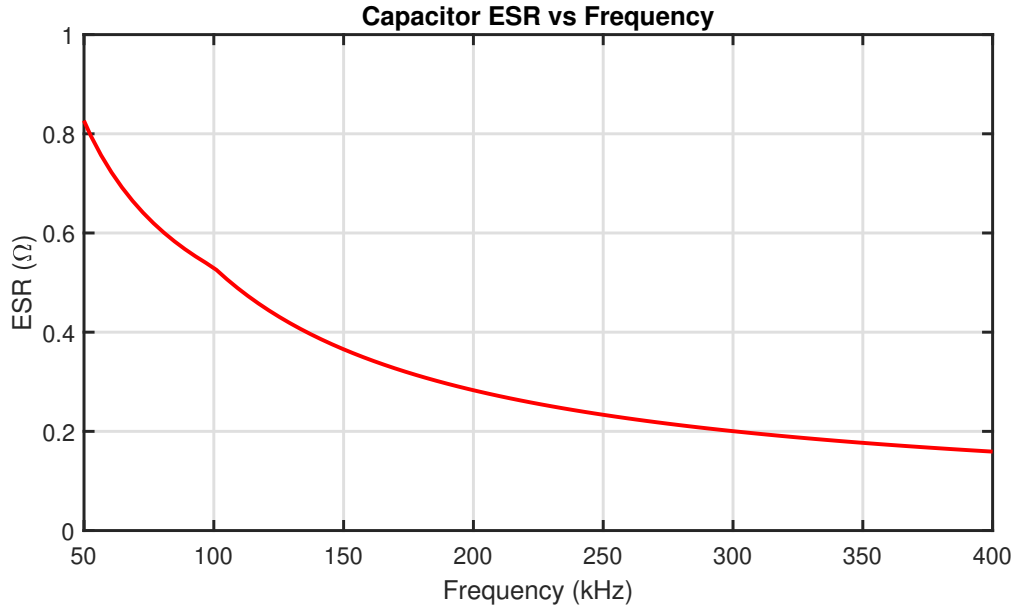


Figure 6.5: ESR vs. f

Table 6.2 summarises the chosen component

QUANTITY	REQUIREMENT	ACTUAL
Capacitor RMS Voltage	200 V	300 V
Capacitor PEAK Voltage	400 V	1250 V
ESR MAX	below 1Ω	0.5 Ω

Table 6.2: Interface capacitor requirements and characteristics.

6.1.3 Inductor

The inductor is the most critical component of the design, due to the extreme circuit requirements. The maximum ratings for the inductor are:

- $i_{L_{rms}} = 200V$
- $i_{L_{peak}} = 400V$
- $f_{max} = 3f_{sw_{max}} = 420kHz$
- $v_{L_{peak}} = 400V$

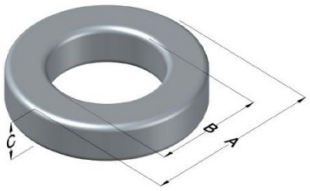
With these values, it was not possible to find a commercial component since not all the requirements were met. Therefore, two custom inductor were designed to ensure compliance with the circuit's performance and reliability needs. One was manufactured by Italtras and the other by Würth Elektronik.

Italtras inductor

Italtras designed the custom inductor with the following characteristics:

- **Core**: 2 stacked Magnetics 0076312A7 (characteristics depicted on Figure 6.6).
- **Wire**: Litz wire consisting of 245 strands, each with a diameter of 0.1 mm (AWG 38).
- **Turns**: 31
- **Measured inductance** (at $100kHz$): $37.4\mu H$

The usage of Litz wires reduces significantly the copper losses since the skin effect is minimized.



Kool Mμ H*f* Permeability (μ)	A_L (nH/T^2)	Core Marking			Coating Color
		Lot Number	Part Number	Inductance Grade	
26	18 ± 8%	XXXXXX	76312A7	N/A	Black

Dimensions	Uncoated		Coated Limits			Packaging
	(mm)	(in)	(mm)	(in)		
OD (A)	22.86	0.900	23.62	0.930	max	Bulk Pack 4 bags/box Box Qty= 1000 pcs
ID (B)	13.97	0.550	13.34	0.525	min	
HT (C)	7.62	0.300	8.38	0.330	max	

Figure 6.6: Magnetics core 0076312A7

The inductor is shown in Figure 6.7

Figure 6.7: Italtras inductor

The DC resistance of the inductor was measured with the LCR40 passive component analyser and its value is equal to $DCR = 0.2\Omega$. For the AC resistance, measurements were performed with the 4192A LF impedance analyser, and the results are presented in Figure 6.8.

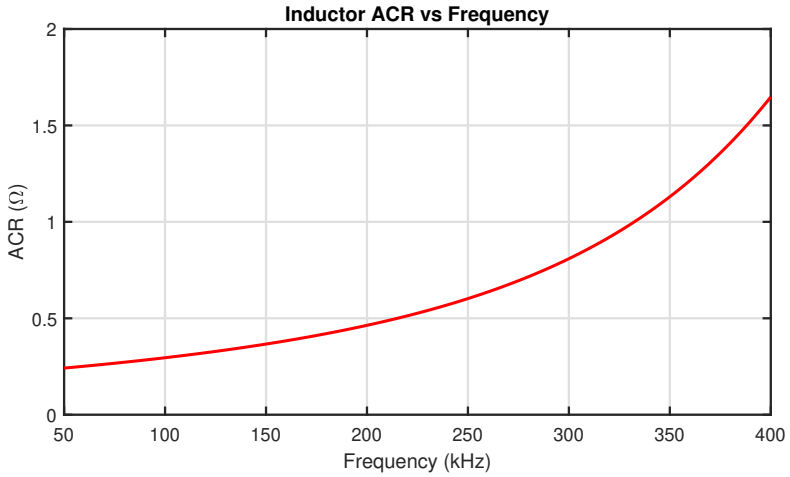


Figure 6.8: ACR vs. f

Despite the use of litz wire, the AC resistance remains relatively high, which will negatively impact overall efficiency. As a result, the inductor is expected to be the primary source of power loss in the circuit.

Würth Elektronik

Würth Elektronik modified their WE-PD HV SMT Power Inductor series to meet the specific requirements of this project, which involve high-voltage operation. The minimum standard inductance of this series is $L = 220\mu H$. To comply the required

QUANTITY	REQUIREMENT	ACTUAL
Average current	$2A$	$2A$
Breakdown voltage	$40V$	$40V$
Forward voltage	below $0.7V$	$0.55V$

Table 6.3: Italtras inductor requirements and characteristics.

specifications, Würth Elektronik customized the inductor to provide an inductance of $L = 33\mu H$. Additionally, the customized inductor complies with the current ratings.

In Figure 6.9, the dimensions of the custom WE-PD HV SMT Power Inductor series is shown.

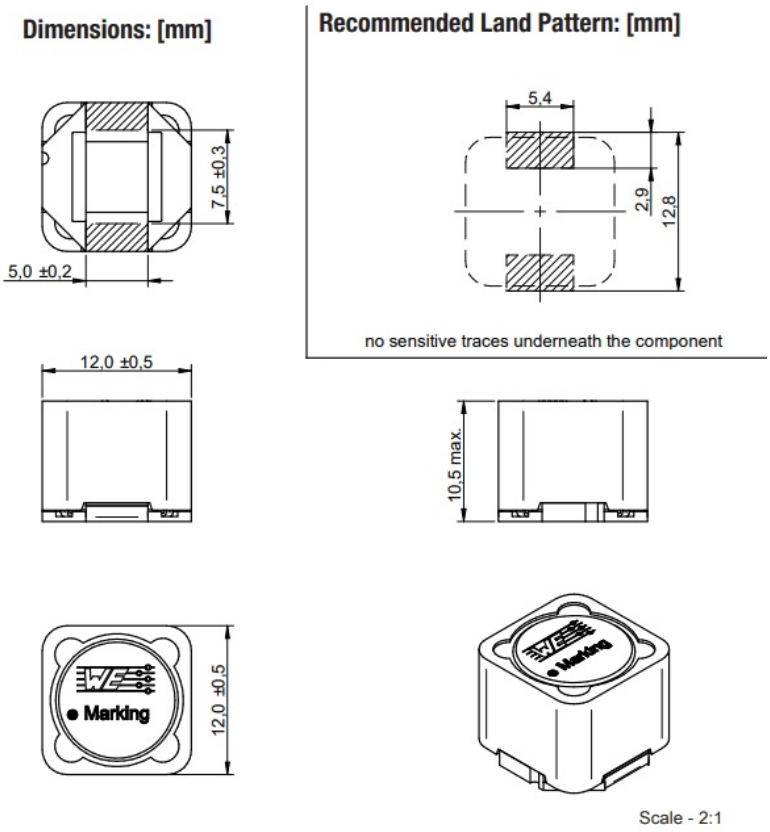


Figure 6.9: Würth Elektronik inductor dimensions

The same instruments were used to measure the inductor's DC and AC resistance. Yielding a value of $DCR = 0.135\Omega$ and the ACR vs. the frequency is shown in Figure 6.10.

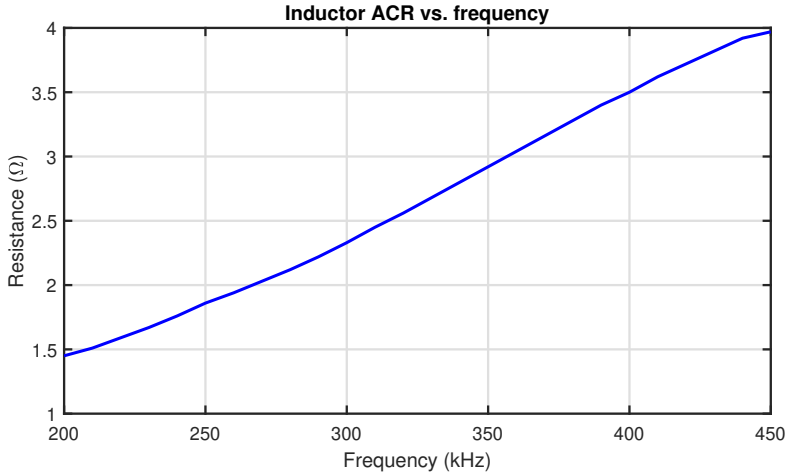


Figure 6.10: Würth Elektronik inductor ACR vs. f

Even though the DCR of the Würth inductor is lower than the Italtras, for high frequencies, it presents higher resistances, resulting in more losses. Figure 6.11 shows a comparison of ACR for both inductors.

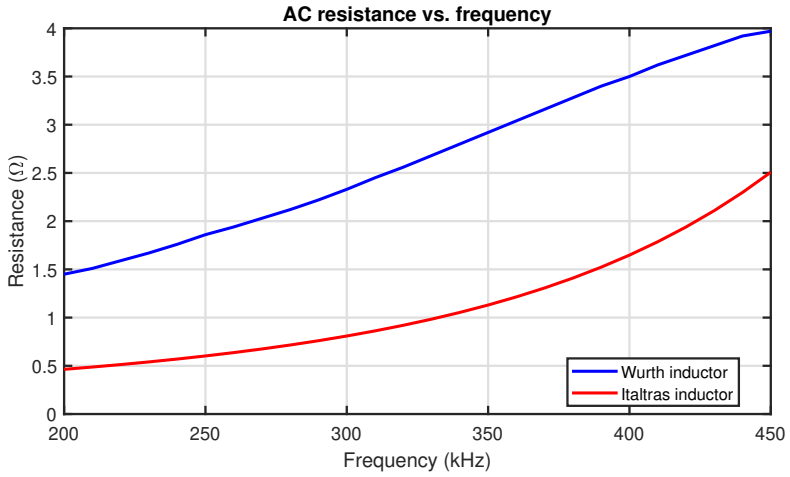


Figure 6.11: Both inductors ACR vs. f

6.1.4 Full-bridge rectifier

For the rectifier, two common diode options are the regular silicon diodes and the Schottky diodes. The first one have a higher forward voltage drop, around $0.7V$, while the second option has a lower voltage drop, that is around $0.4V$, resulting in lower conduction losses and improving the efficiency. Furthermore, Schottky diodes

offer faster switching times, making it more suitable for converter applications.

For selecting the diodes, it is important to consider the maximum ratings which are the average diode current $I_{D_{av}}$ and the breakdown voltage V_{RRM}.

With the simulations, the maximum average current of the diodes obtained was $I_{av} = 1.38A$ and in open-loop conditions, the maximum reverse voltage was $V_{RRM} = 33V$. Therefore, the maximum ratings for the diodes are:

- $I_{av} \geq 2A$
- $V_{RRM} \geq 40V$

The selected full-bridge rectifier is the CDBHM220L-HF from Comchip, where the four diodes are integrated in a single chip. Table 6.4 shows the maximum ratings and Figure 6.12 depicts the dimensions of the components.

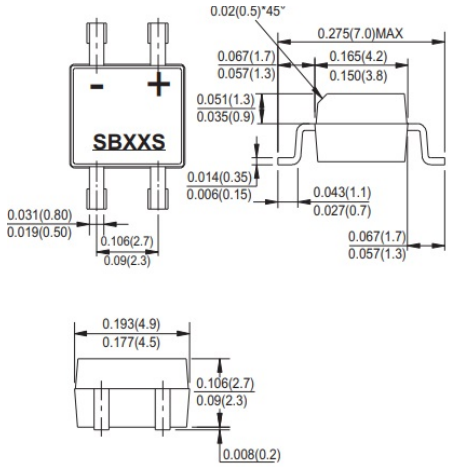


Figure 6.12: CDBHM220L-HF dimensions

QUANTITY	REQUIREMENT	ACTUAL
Average current	$2A$	$2A$
Breakdown voltage	$40V$	$40V$
Forward voltage	below 0.7Ω	0.55Ω

Table 6.4: Full-bridge rectifier requirements and characteristics.

6.1.5 Input and output capacitor

As the converter is connected to the grid, it is important to decide an input and output capacitors that guarantee the ripple in the load is minimized and the voltage

remains stable under varying load conditions. In addition, for an optimal operation, it is needed that both capacitors that must handle high ripple current and low ESR.

It was decided that the input capacitor value is $C_{in} = 22\mu F$ and the output capacitor a value of $C_{out} = 1mF$. With these values, the results are satisfactory and meet the design requirements.

The input capacitor selected is the 860021374027 Aluminium Electrolytic capacitor from Würth Elektronik, which dimensions are shown in Figure 6.13

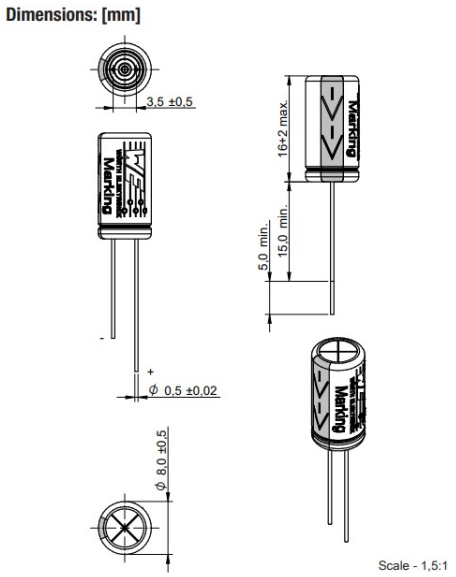


Figure 6.13: 860021374027 dimensions

For the output capacitor, MAL215099014E3 Aluminium Electrolytic capacitor from Vishay was selected. Its dimension is presented in Figure 6.14

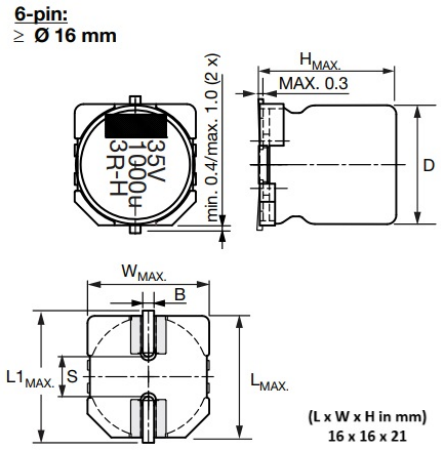


Figure 6.14: MAL215099014E3 dimensions

6.1.6 Feedback loop

In order to measure the output voltage, it is important to isolate the output port with the logical circuit. Furthermore, as the output voltage reference ground is different from the logic and power ground, it is necessary to reference the output voltage signal to the logic one.

Texas Instrument's AMC series provides isolated amplifiers where, at the input, the output voltage is connected and at the output, the signal is amplified with a different ground reference. For this project, the AMC1351 was selected and its circuit diagram is shown in Figure 6.15.

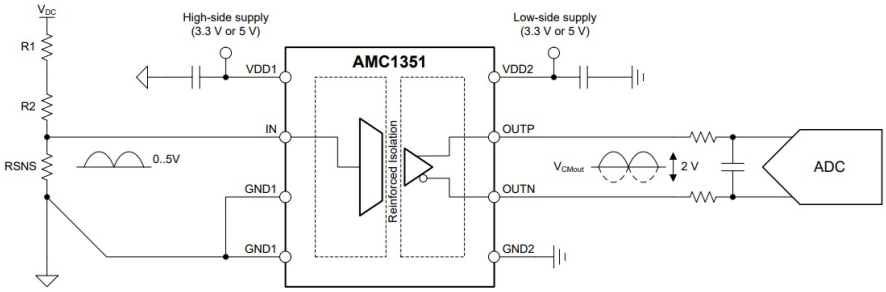


Figure 6.15: AMC1351 circuit diagram

It can be seen that the input is unipolar with a maximum voltage of $5V$. Therefore, a signal attenuation must be made with a voltage divider.

As the maximum voltage in open-loop condition is $33V$. The attenuation must be:

$$Att = \frac{5}{33} = 0.152 \tag{6.2}$$

Using a voltage divider, whose representation is in Figure 6.16, the previous expression is used for calculating the resistances.

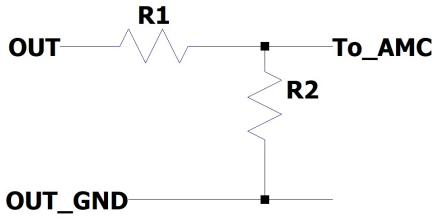


Figure 6.16: Voltage divider

$$Att = \frac{R_2}{R_1 + R_2} = 0.152 \tag{6.3}$$

Selecting $R_1 = 1M\Omega$, R_2 must be $178k\Omega$ in order to satisfy the previous equation.

Since output of the AMC1351 is differential, so the ADC must be set to differential mode.

The low-side supply must be done with the microcontroller's supply. For the high-side supply, it is not possible to feed it with the microcontroller's supply since the output voltage is not referenced to logic ground.

Therefore, an isolated DC/DC converter must be used in order to reference the microcontroller's supply to the high-side of the AMC.

The 1779205141 Isolated DC/DC Converter from Würth Elektronik was chosen, since the input is $5V$ and the output is $5V$ too. Figure 6.17 presents the circuit diagram for this component.

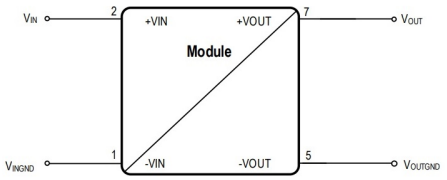


Figure 6.17: 1779205141 circuit diagram

6.2 Board realization

The PCB design was made in Altium Designer. This software allowed the creation of both the schematic and the PCB layout.

6.2.1 Schematic

In Figure 6.18 the schematic is shown, where all the components used for the project can be seen.

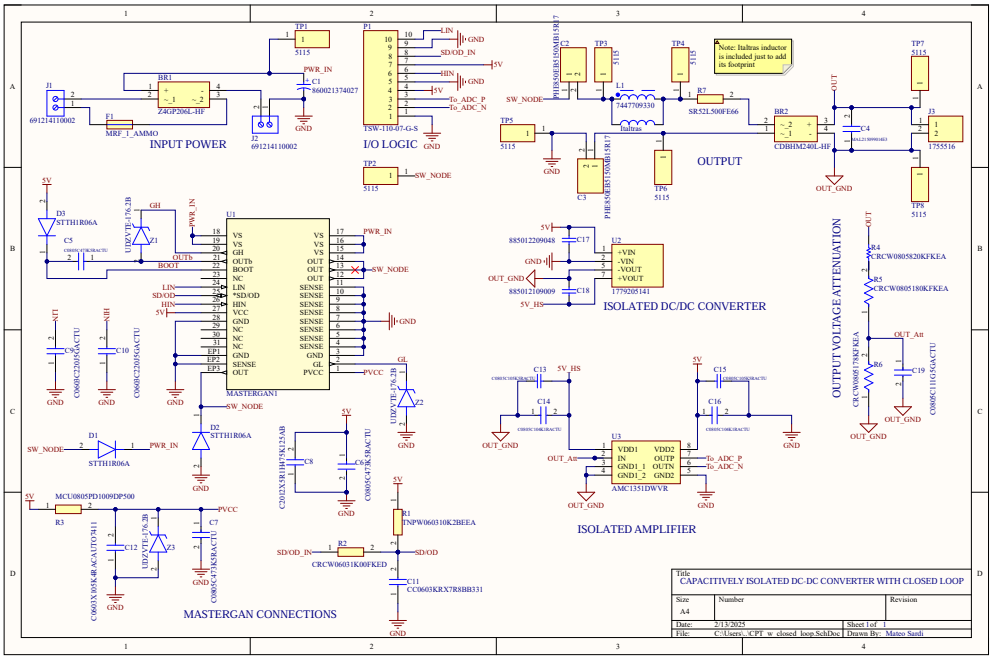


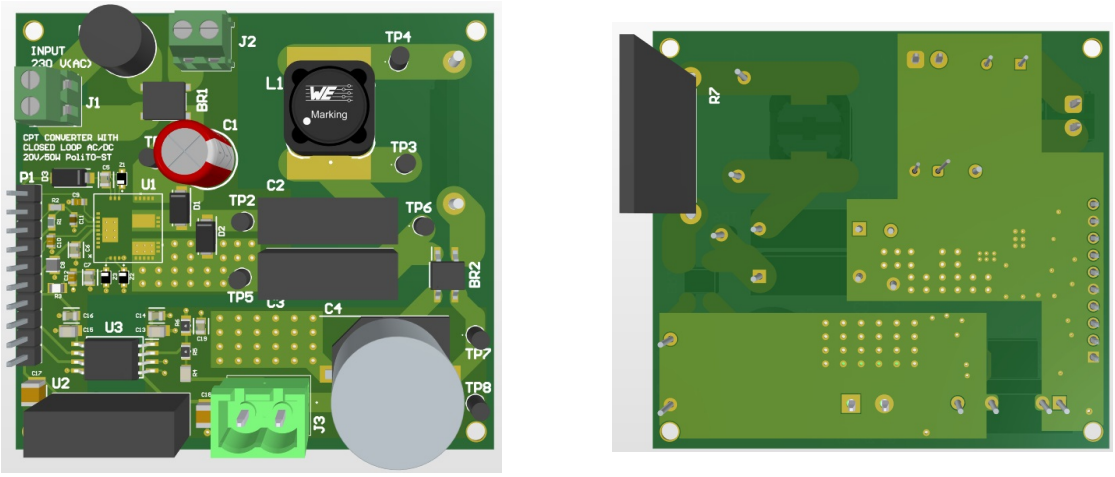
Figure 6.18: Schematic

The Schematic is divided by the following sections:

- **Input power**: This section includes the input $230V_{rms}$, the input bridge rectifier and the input capacitor.
- **I/O Logic**: This section contains the pin header where all the inputs and outputs are connected.
- **MASTERGAN connections**: All the components necessary for the MASTERGAN to work properly are are located in this section.
- **Output**: This section includes the power components such as the inductor, interface capacitors, the output rectifier and capacitor.
- **Feedback**: This final section consists of the voltage divider, the isolated DC/DC converter and AMC.

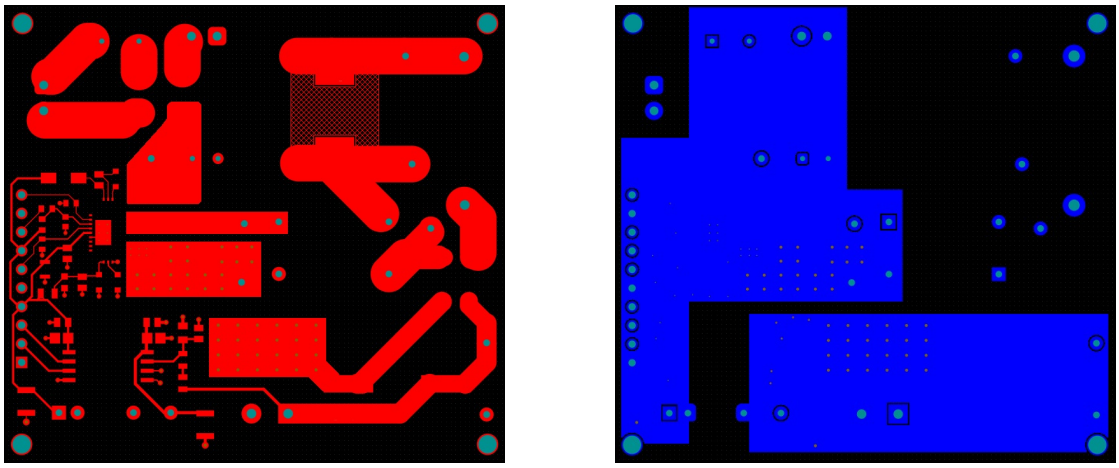
Test points has been added in order to measure the waveforms at different parts of the circuit.

6.2.2 Board layout



(a) (b)

Figure 6.19: 3D view (a) Top view and (b) Bottom view



(a) (b)

Figure 6.20: (a) Top layer and (b) Bottom layer

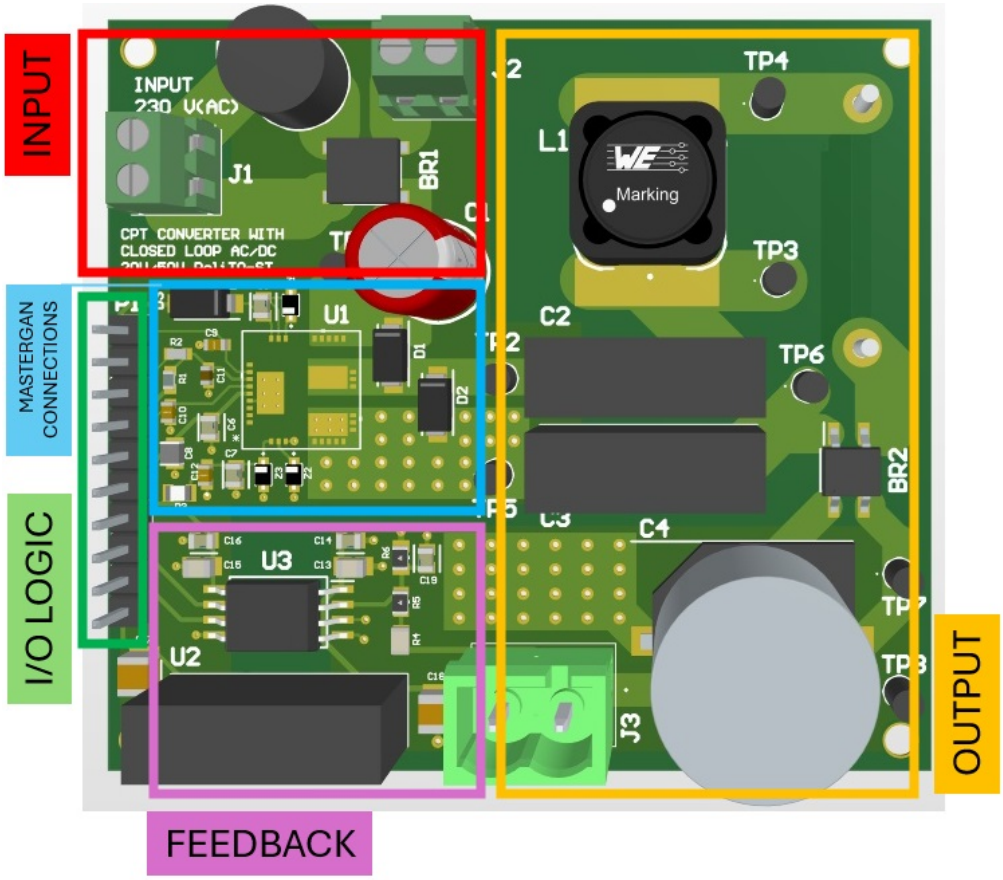


Figure 6.21: 3D top view highlighting the different sections of the circuit

Chapter 7

Results

7.1 Setup

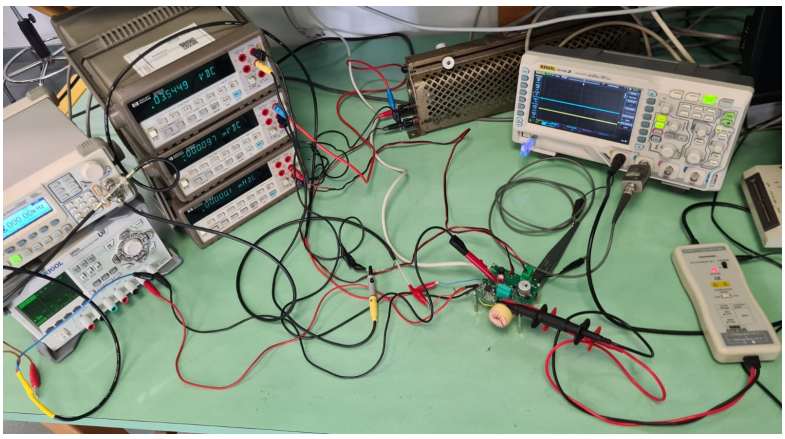


Figure 7.1: Circuit setup

The following instruments were used:

- **Oscilloscope**: RIGOL DS1054
- **Waveform generator**: RIGOL DG1022
- **DC Power Supply**: RIGOL DP832
- **Multimeters**: HP 34401A
- **Rheostat**: SECI Milano 100Ω 2.5A

7.2 Open-loop measurements

The open-loop measurements presented in this section were obtained using a board designed by the predecessor of this thesis project [6].

For both, low and high voltage measurements, the following quantities will be measured:

1. **Output voltage** V_{out}
2. **RMS inductor current** $I_{L_{RMS}}$
3. **Peak inductor current** $I_{L_{peak}}$
4. **Efficiency** η

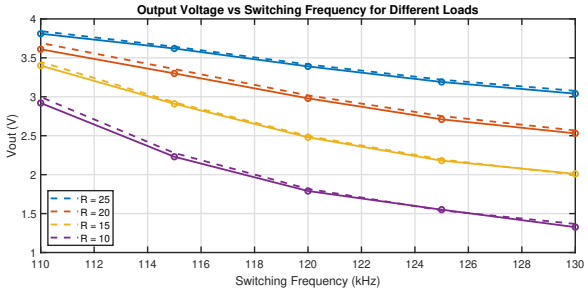
Furthermore, a comparison between the simulated waveform and the measured real-world waveform will be done

7.2.1 Low voltage input

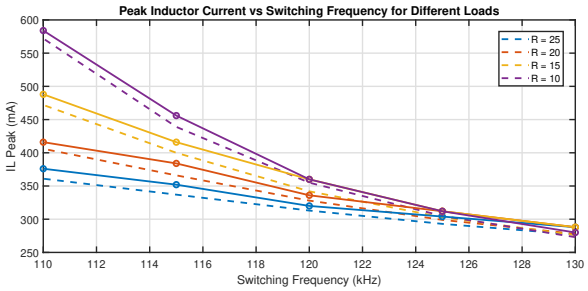
The measurements were performed with an input DC voltage of $V_{in} = 30V$.

Given the low power conditions of the circuit due to the low input voltage, it is possible to use frequencies lower than $120kHz$.

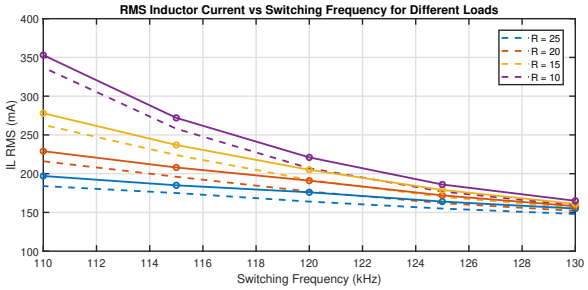
The frequencies chosen for the measurements are $f_{sw} = 110kHz$, $115kHz$, $120kHz$, $125kHz$ and $130kHz$. The load used are $R = 10\Omega$, 15Ω, 20Ω and 25Ω.



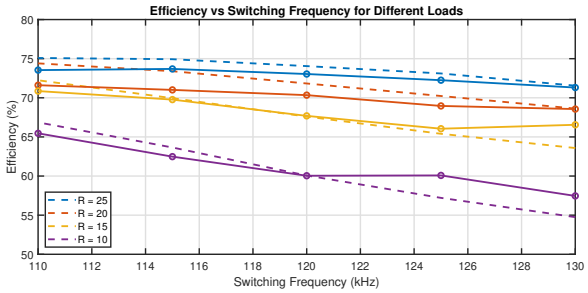
(a)



(b)



(c)



(d)

Figure 7.2: Low voltage measurements: Dashed lines represent simulated values, while circular markers represent measured values. Shown are: (a) V_{out}, (b) $I_{L_{peak}}$, (c) $I_{L_{RMS}}$, and (d) efficiency η for different R and f_{sw} values.

In Figure 7.2 it is shown a comparison of the expected values obtained in the simulation and the measured in the circuit.

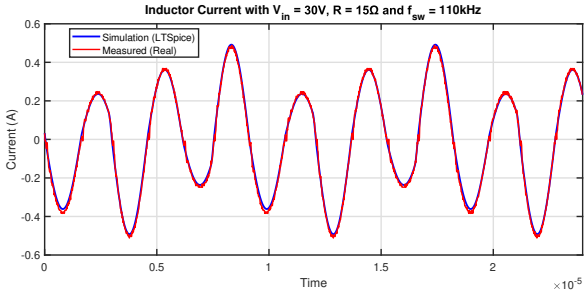
The expected output voltage and the obtained are quite similar. When f_{sw} decreases, V_{out} increases, as it was analysed in the mathematical model and in Spice simulations. Additionally, when R increases, V_{out} increases, as expected. The maximum value obtained is $V_{out} = 3.8V$, which corresponds to the minimum frequency and maximum output resistance.

For both current quantities, RMS and peak, the simulated and obtained results are similar, both in value and tendency. Frequencies closer to the resonance frequency make the current increase faster. For frequencies higher than $f_{sw} = 125kHz$, current values for all loads have similar values.

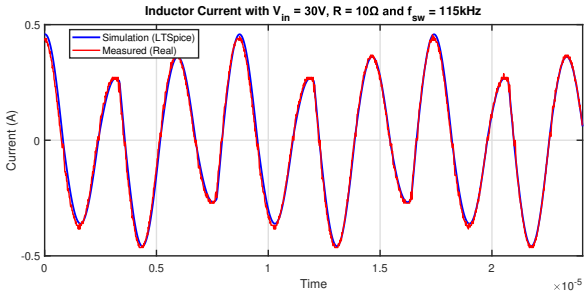
The efficiency is expected to be lower in low voltage input. For higher resistance values, the efficiency is higher. While for lower switching frequency values, the efficiency slightly increases . The higher efficiency obtained is 74% at the lower switching frequency and higher resistance. While the lowest is 57%, obtained at the highest frequency and lowest resistance value.

A comparison of the inductor current waveforms are done in order to corroborate the simulations in Figure 7.3.

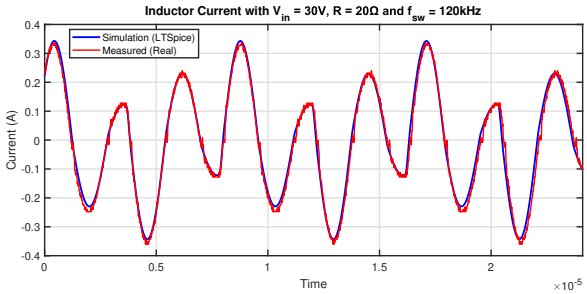
It can be seen that, for different values of R and f_{sw}, the simulated and measured waveforms coincide.



(a)



(b)



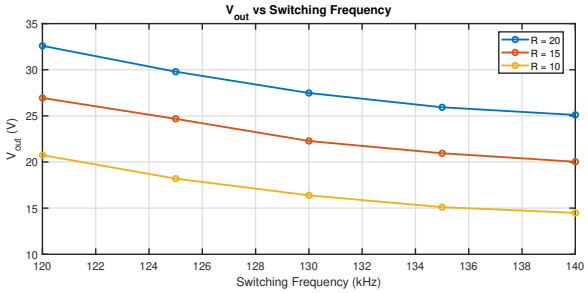
(c)

Figure 7.3: Low voltage measurements: Inductor current waveforms with $V_{in} = 30V$: (a) $R = 15\Omega$ and $f_{sw} = 110kHz$, (b) $R = 10\Omega$ and $f_{sw} = 115kHz$, and (c) $R = 20\Omega$ and $f_{sw} = 120kHz$

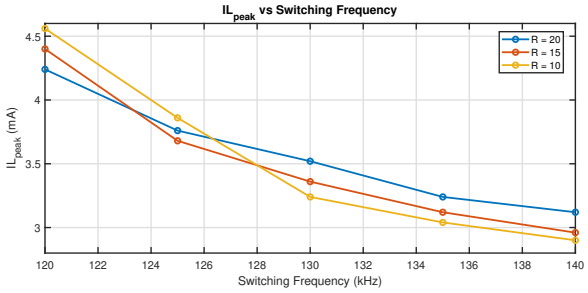
7.2.2 High voltage input

The following measurements were performed with the grid input voltage $V_{in} = 230V_{RMS}$.

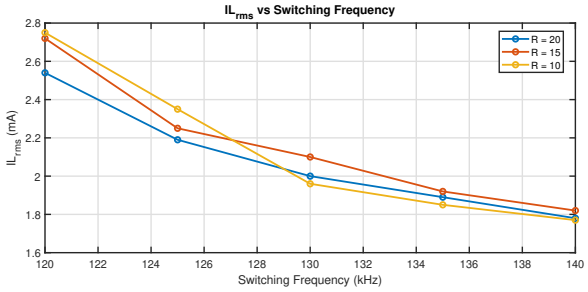
The frequency selected for this measurements are $f_{sw} = 120kHz$, $125kHz$, $130kHz$, $135kHz$ and $140kHz$, which is the frequency range selected in previous chapters. The load used are $R = 10\Omega$, 15Ω and 20Ω.



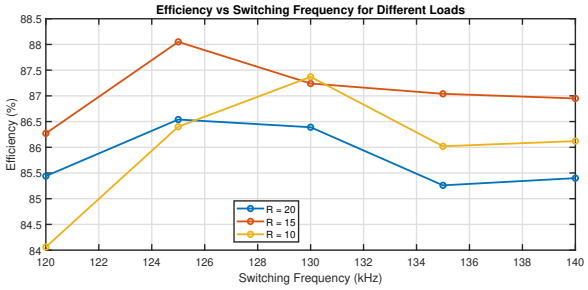
(a)



(b)



(c)



(d)

Figure 7.4: High voltage measurements: (a) V_{out}, (b) $I_{L_{peak}}$, (c) $I_{L_{RMS}}$, and (d) efficiency η for different R and f_{sw} values.

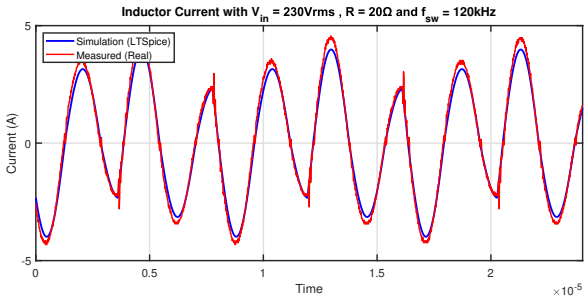
In Figure 7.4, the measured quantities are shown.

It can be seen that, for $R \geq 15\Omega$, the $20V$ output voltage cannot be reached, as it was expected. The tendency of the output voltage is equal to the low voltage input measurements. The maximum voltage obtained is at $f_{sw} = 120kHz$ and $R = 20\Omega$ and it is equal to $V_{out} = 33V$.

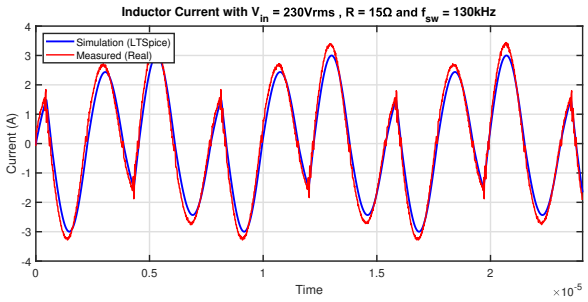
For the current quantities, the maximum peak and RMS current is obtained at $f_{sw} = 120kHz$ and $R = 10\Omega$, whose values are $I_{L_{peak}} = 4.56A$ and $I_{L_{RMS}} = 2.75A$.

The efficiency curve differs from the low input voltage measurements. This is due to the error introduced by the rheostat used. The efficiency range is from $\eta = 84\%$ at the worst case which is at $f_{sw} = 120kHz$ and $R = 10\Omega$, to $\eta = 88\%$ at the best case which is at $f_{sw} = 125kHz$ and $R = 15\Omega$.

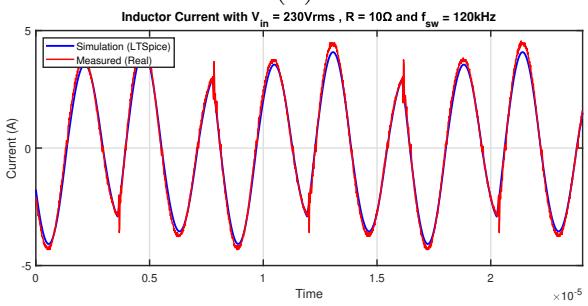
The inductor current waveforms are compared with the simulation in Figure 7.5. The waveforms are equal. However, they slightly differ in the peak value.



(a)



(b)



(c)

Figure 7.5: High voltage measurements: Inductor current waveforms with $V_{in} = 230V_{RMS}$: (a) $R = 20\Omega$ and $f_{sw} = 120kHz$, (b) $R = 15\Omega$ and $f_{sw} = 130kHz$, and (c) $R = 10\Omega$ and $f_{sw} = 120kHz$

Chapter 8

Conclusions

The mathematical model developed in this thesis was useful to predict the system's behaviour, to select the most optimal design parameters and to simulate and implement the control strategies. This model was validated with SPICE simulations and real-life measurements.

The control simulations were successful, demonstrating that all strategies were able to regulate the output voltage to the desired value under varying conditions such as non-constant input voltage and load changes. Each controller exhibits its own strengths and weaknesses, which should be considered when selecting the most suitable control approach for specific operating conditions.

One of the key objectives of the thesis was to test the circuit with the grid voltage input which was successfully achieved with promising results. The system reached efficiencies up to 88%. These results highlight the viability of the proposed CPT system and its potential for real-world applications.

8.1 Future work

Due to time constraints, the measurements using the board with feedback were not conducted. The next step is to perform these measurements, implement the control algorithms used in simulations and compare the experimental results with the simulated performance.

Another aspect to work on is exploring alternative control strategies, including the implementation of optimal controllers, such as Linear Quadratic Regulator (LQR) and Model Predictive Control (MPC).

Bibliography

[1] L. Olvitz, D. Vinko, and T. Švedek. «Wireless power transfer for mobile phone charging device». In: *2012 Proceedings of the 35th International Convention MIPRO*. 2012, pp. 141–145 (cit. on p. 1).

[2] A. Lassioui, H. El Fadil, F.Z. Belhaj, and A. Rachid. «Battery Charger for Electric Vehicles Based ICPT and CPT - A State of the Art». In: *2018 Renewable Energies, Power Systems & Green Inclusive Economy (REPS-GIE)*. 2018, pp. 1–6. DOI: 10.1109/REPSGIE.2018.8488834 (cit. on p. 1).

[3] Mehmet Zahid Erel, Kamil Cagatay Bayindir, Mehmet Timur Aydemir, Sanjay K. Chaudhary, and Josep M. Guerrero. «A Comprehensive Review on Wireless Capacitive Power Transfer Technology: Fundamentals and Applications». In: *IEEE Access* 10 (2022), pp. 3116–3143. DOI: 10.1109/ACCESS.2021.3139761 (cit. on pp. 1, 5).

[4] Alihossein Sepahvand, Ashish Kumar, Khurram Afridi, and Dragan Maksimović. «High power transfer density and high efficiency 100 MHz capacitive wireless power transfer system». In: *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*. 2015, pp. 1–4. DOI: 10.1109/COMPEL.2015.7236492 (cit. on p. 1).

[5] Filippo Fiori. «Study and Development of Innovative Capacitevely Isolated Low Power DC-DC Converter». MA thesis. Politecnico di Torino, 2022 (cit. on p. 2).

[6] Michele Annucci. «Studio e progettazione di un alimentatore AC/DC ad alta efficienza con isolamento capacitivo». MA thesis. Politecnico di Torino, 2025 (cit. on pp. 2, 88).

[7] Jiejian Dai and Daniel C. Ludois. «A Survey of Wireless Power Transfer and a Critical Comparison of Inductive and Capacitive Coupling for Small Gap Applications». In: *IEEE Transactions on Power Electronics* 30.11 (2015), pp. 6017–6029. DOI: 10.1109/TPEL.2015.2415253 (cit. on p. 5).

[8] Deepa Vincent and Sheldon S. Williamson. «Role of Dielectrics in the Capacitive Wireless Power Transfer System». In: *2020 IEEE International Conference on Industrial Technology (ICIT)*. 2020, pp. 1217–1222. DOI: 10.1109/ICIT45562.2020.9067136 (cit. on p. 5).

[9] Liang Huang, Aiguo Patrick Hu, Akshya Swain, and Xin Dai. «Comparison of two high frequency converters for capacitive power transfer». In: *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2014, pp. 5437–5443. DOI: 10.1109/ECCE.2014.6954146 (cit. on pp. 6, 25).

[10] Zonghong Hu, Matthew Goodall, Lei Zhao, Qi Zhu, and Aiguo Patrick Hu. «A Comparative Study of Different Compensation Topologies for Capacitive Power Transfer». In: *2020 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer (WoW)*. 2020, pp. 389–394. DOI: 10.1109/WoW47795.2020.9291314 (cit. on p. 6).

[11] S. N. Verma. «Overview of control Techniques for DC-DC converters». In: 2013. URL: https://api.semanticscholar.org/CorpusID:18276266 (cit. on p. 8).

[12] S. Cerutti, M. Pavone, F. Musolino, and P. Crovetti. «Modelling of a Multi-Period Damped Resonant DC-DC Converter with Capacitive Isolation». 2024 (cit. on pp. 13, 22).

[13] Analog Devices. *LTSpice*. https://www.analog.com/en/resources/design-tools-and-calculators/ltspice-simulator.html. Accessed: 2025-03-30. 2025 (cit. on p. 38).

[14] Paolo S. Crovetti. «All-Digital High Resolution D/A Conversion by Dyadic Digital Pulse Modulation». In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 64.3 (2017), pp. 573–584. DOI: 10.1109/TCSI.2016.2614231 (cit. on p. 63).

[15] STMicroelectronics. *Wide Bandgap Transistors*. https://www.st.com/en/power-transistors/wide-bandgap-transistors.html. Accessed: 2025-01-13. 2025 (cit. on p. 70).

[16] STMicroelectronics. *MASTERGAN1*. https://www.st.com/en/power-management/mastergan1.html. Accessed: 2025-02-12. 2025 (cit. on p. 71).