POLITECNICO DI TORINO

Master's Degree in Electronics Engineering

Master's Degree Thesis

ANALYSIS AND DESIGN OF A DC-DC QUADRATIC POWER CONVERTER WITH PARTIAL POWER PROCESSING ARCHITECTURE FOR PHOTOVOLTAIC APPLICATIONS

Supervisors

Prof. Francesco MUSOLINO

Prof. Paolo Stefano CROVETTI

Prof. Stefano CERUTTI

Candidate

Federico Emir RICCI

April 2025

Abstract

The increasing adoption of photovoltaic (PV) systems demands innovative DC-DC power conversion solutions. This thesis focuses particularly on micro-grid systems and standalone PV modules, where traditional array connections are unavailable, generating the need for high step-up requirements with wide input voltage variations. The analysis, design, and simulation of a novel DC-DC power converter with a Partial Power Processing (PPP) architecture is presented, designed to operate over a wide input voltage range (15–43 V) and deliver constant output voltage (350 V) across a broad power range (50–680 W), accommodating the variability of PV energy sources.

To overcome efficiency bottlenecks in DC-DC stages for single-phase grid-tied PV systems, this thesis introduces the exploitation of Partial Power Processing through a dual stage quadratic converter with Input-Parallel Output-Series (IPOS) topology, offering high performance by allowing part of the power to flow directly to the load, bypassing the converter stages. This approach achieves high efficiency, reduces component stress, and ensures reliable performance under various conditions. Simulation results reveal a California Energy Commission (CEC) weighted efficiency of 97.2% and a European (EURO) weighted efficiency of 96.8% at the rated power of 680 W.

By providing a comprehensive framework for addressing wide input voltage ranges, high step-up gains, and partial power processing, this work contributes to advancing the state of the art in PV power conversion. The methodologies and findings offer practical insights for improving efficiency in renewable energy systems while addressing challenges posed by Partial Power Processing load balancing.

Building on these innovations, this work also contributes to the DC-DC power converter design workflow by presenting developed methodologies and tools tailored to address the challenges of achieving high step-up gain values with large input voltage variation in circuit topologies highly dependent on load conditions. A detailed efficiency measurement approach, leveraging *LTSpice* and *MATLAB* integration, is introduced alongside innovative techniques for magnetic loss estimation through simulation. These contributions provide valuable insights to assist designers in optimizing converter performance for renewable energy applications.

Acknowledgements

Prima di tutto, vorrei ringraziare ai miei relatori, Francesco Musolino, Paolo Stefano Crovetti, e Stefano Cerutti, con i quali è stato un vero piacere lavorare sin dal primo giorno, grazie alla loro costante gentilezza e disponibilità.

A mis padres, que desde el día uno me han motivado a seguir cualquier meta que me proponga, siempre acompañándome con su incondicional amor en cada proceso, hito, caída y logro que se diera. Este trabajo es la culminación de una larga etapa de mi vida, y nunca habrá palabras suficientes para expresar lo agradecido que estoy por su permanente compañía y apoyo.

A mi compañera, Giulietta, quien me ha acompañado en toda esta aventura a la distancia, pero siempre cerca, velando en todo momento por mi bienestar con un cariño inmenso.

A mi colega y amigo, Mateo, a quien hoy podría prácticamente llamar un hermano. Incontables son las experiencias, desafíos y aprendizajes que hemos compartido. Ha sido un verdadero placer vivir esta etapa junto a un gran amigo como él.

Finalmente, quisiera agradecer a todas las personas que han sido un apoyo fundamental en este camino, brindándome aliento, consejos y momentos inolvidables. A mis amigos en Torino, por hacerme sentir en casa incluso a miles de kilómetros de ella.

Un agradecimiento especial a Ivo, Celina, Lara y Agustín, quienes, con su compañerismo y amistad, han convertido el camino universitario en mucho más que una simple etapa académica.

Table of Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Solar energy power systems

1.1.1 Current trends of energy production

Solar energy has seen a major growth in the last decade, it has in fact started following an exponential tendency in terms of installed power capacity across the world. Only in 2023, the global power capacity raised 34% with respect to the total capacity in 2022 [1] as it can be seen in Fig.1.1.

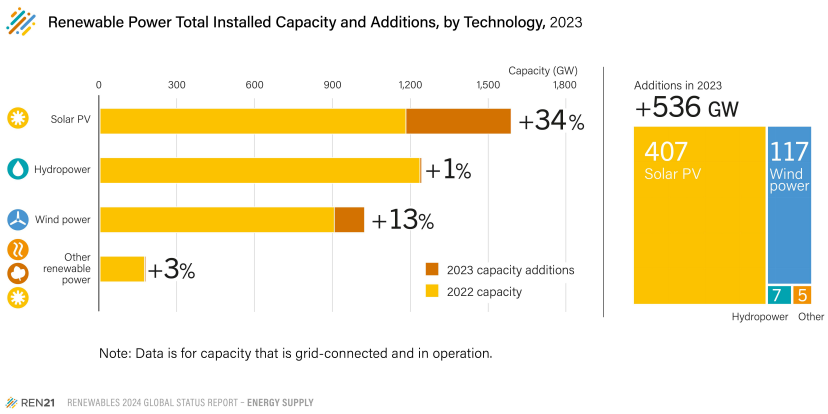


Figure 1.1: Solar energy capacity addition from 2022 to 2023

The increase in the use of solar energy is mainly driven by the exponential drop in costs over the last decade, thanks to technological advancements, making it one

of the lowest-cost sources of energy per kWh [2]. As shown in Fig. 1.2, prices are expressed in USD and adjusted for inflation to 2023 (levelized cost of energy). This downward trend in the cost of solar energy production is expected to continue, as this method of energy harnessing follows Wright's law [3], where prices decline exponentially as cumulative installed capacity grows.

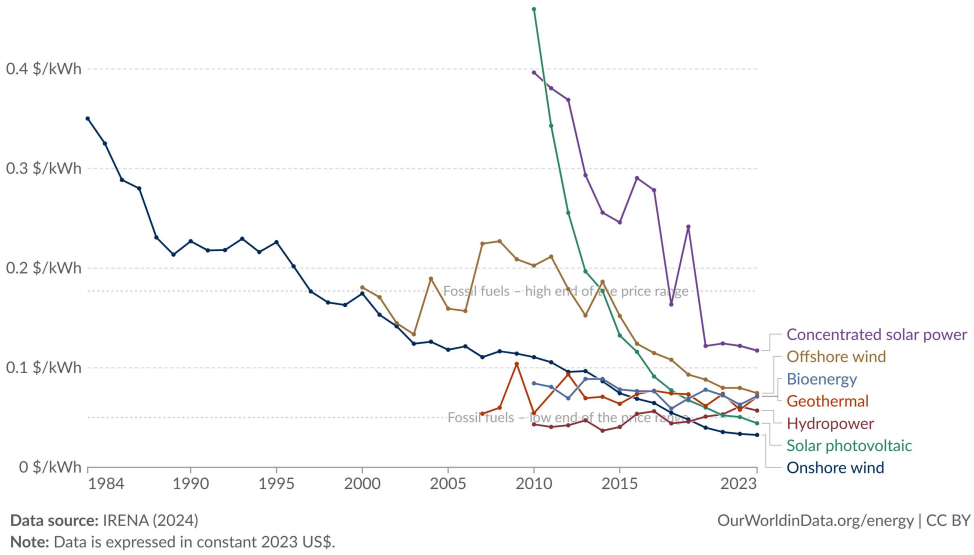


Figure 1.2: Different energy sources cost per kWh evolution in time

To achieve a better transition to renewable energy systems, not only is technology for power generation necessary, but the interfaces to merge these varying power supplies with the infrastructure are critical.

Fossil fuels have the advantage of providing an "instantly available" energy source for grid injection. In contrast, renewable energy like wind and solar exhibit uncontrollable variability due to their dependence on environmental conditions. This introduces significant challenges for the power converter interfaces such as the capacity of operating under multiple working points while ensuring seamless grid integration while maximizing efficiency. Such converters may also manage disconnections during unfavorable conditions or integrate energy storage systems for enhanced reliability. As a result, renewable sources act as complementary sources, offsetting the use of stored energy like fossil fuels and hydroelectric power when available.

In 2023, rooftop photovoltaic modules accounted for the largest share of installations in the European Union, 33% of which are in the residential segment, mainly due to increasing cost of electricity [1]. This particular application of decentralized energy production relies on power converters designed primarily for single-phase

grid-tied systems, which is the scope of this thesis.

In the context of energy production, decentralized schemes enable incremental grid capacity expansion, ensuring improved fault tolerance and scalability. Each small addition to the grid capacity, when multiplied by numerous contributions, results in a significantly larger overall capacity. This approach is more fault-tolerant, as the disconnection of one provider does not cause the entire grid to malfunction.

Several single-phase grid-tied decentralized photovoltaic system topologies exist depending on the configuration of photovoltaic panels at the input of the system [4]. The ac-module configuration uses a dedicated power converter for each photovoltaic panel connected to the grid. Having only one module presents the need for high DC voltage gains, which generates a bottleneck in the efficiency achieved by this type of system. However, they compensate their limitation in efficiency with the greatest exploitation of the maximum power that can be extracted from the photovoltaic module; they also adapt best in situations where photovoltaic panels are subject to varying conditions, such as shading, soiling, or differing orientations, as shown in Fig. 1.3, allowing each panel's power converter to adjust its control depending on the condition. In other topologies where one control scheme manages the energy extraction of numerous photovoltaic panels, the mismatch in their operating conditions leads to a reduction of the energy yield of the system.

Figure 1.3: Different photovoltaic panel energy production factors. (a) Shading (b) Soiling (c) Differing orientations

1.2 Scope of the thesis and organization of work

Photovoltaic panels present a wide input voltage range, usually low voltages for most commercial variants from 10-60 V. In the context of ac-module configuration for single-phase grid-tied systems, high step-up DC gain is needed to adapt the low voltage level of the single photovoltaic panel to the grid. Additionally, the power output of the photovoltaic panel varies significantly due to factors such as irradiance and temperature. These variations in input voltage and power present considerable challenges to the design of power converter circuits, which must operate reliably under wide input voltage and output load conditions.

Among the power conversion system between the photovoltaic panel and the grid, the high gain DC-DC converter represents the primary bottleneck in terms of efficiency. The aim of this thesis is to explore the application of Partial Power Processing (PPP) in the design of a wide-input-range DC-DC power converter stage for single-phase grid-tied ac-module photovoltaic systems. The study focuses on assessing the advantages and limitations of this technique while proposing a novel architecture based on an Input-Parallel Output-Series (IPOS) configuration to maximize the efficiency of the DC-DC stage.

The DC-AC converter, which facilitates direct grid connection, is not analyzed in depth in this work. It is treated as a simple power consumer for the sake of design of the DC-DC converter, left as a research topic for future works.

In Chapter 2, an introduction to photovoltaic energy sources is given, with the description of the state of the art connections configuration, as well as the introduction of the proposed power converter and its attributes.

In Chapter 3, a state of the art review on high-frequency power conversion is carried out, with the introduction of resonant converters as a type of high-frequency power converter, and the in-depth analysis of the particular topology used throughout this work.

In Chapter 4, the design process is explained as well as the description of the tools developed to aid this process. The optimization of the proposed architecture is performed to define and justify the selection of the necessary quantities.

In Chapter 5, an in-depth analysis on power transformers is performed, highlighting several aspects particularly important for the selected resonant topology, as well as providing the necessary models to implement power transformers and their losses in simulation environment.

In Chapter 6, device selection to implement the quantities defined in previous chapters is described, and finally the results of the analysis and design are portrayed in the characteristics retrieved from the simulation.

To conclude, Chapter 7 closes this thesis with a summarized description of the results found throughout this work, as well as proposing the next challenges to continue the development of the proposed power converter.

The analysis developed in this work, with its developed tools and conclusions, relies on the use of the following software, provided by Politecnico di Torino student licensing program:

- *PSIM* for electronic circuits simulation from Altair [5]. Specially utilized for photovoltaic panel modeling.
- *MATLAB* and toolboxes from Mathworks [6]. Utilized for developing user interfaces and processing data in the design phase of this work.
- *LTSpice* for electronic circuits simulation from Analog Devices [7]. Utilized for the SPICE simulation of the final architecture and data extraction for further report generation.

Chapter 2

PV Power Conversion Overview

2.1 PV Sources and their Characteristics

2.1.1 Modeling of photovoltaic panels

Photovoltaic cells convert solar energy into electrical energy, since these cells are photocurrent generators, the most common models are obtained by superimposing the behavior of the following lumped components:

- One or more semiconductor diodes paired with a current generator, representing the recombination and generation currents of the cell
- A series resistance representing the semiconductor material resistance, the metal contacts and interconnections in the cell
- A shunt resistance representing the leakage current within the cell.

The most straightforward model is the single-diode model [8], which represents an ideal solar cell with its voltage and current losses, its circuit can be seen in Fig. 2.1. It is a simplified model that still captures the essentials of solar cells working principle.

The circuit behavior depends strongly on the environmental conditions of temperature and solar irradiance, which determine primarily the photocurrent generated

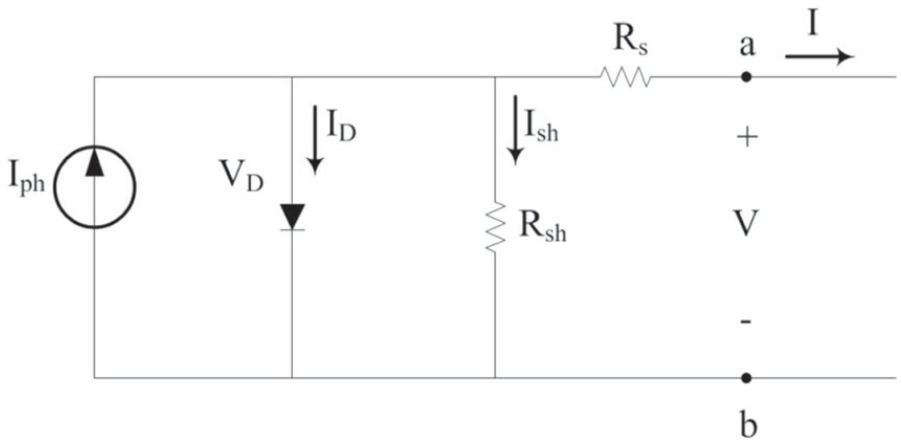


Figure 2.1: Single-diode solar cell equivalent circuit

by the cell. Usually the relationship is built in an incremental fashion, by determining certain parameters in Standard Test Conditions (STC) and incorporating them into the model.

A relationship between voltage and current is created described by applying Kirchhoff laws to the circuit model as seen in Eqs. (2.2) and (2.3). This relationship creates an IV characteristic which has the shape of a typical power supply, being able to provide a considerable current at low voltages, while dropping the ability of regulation at higher voltages. In terms of PV characteristic, this creates a point of maximum power extraction which is of interest for solar applications. By controlling the load current pulling, a controller can force the photovoltaic panel to work on this maximum power point (MPP) given a certain solar irradiance and temperature.

The current through the diode is described by Shockley equation:

$$I_D = I_S(e^{\frac{V_D}{na\frac{kT}{q}}} - 1) \tag{2.1}$$

Where V_D is the applied forward voltage to the diode, k is the Boltzmann constant, T is the cell temperature, q is the electron charge, n is the number of series cells, a is the ideality factor of the diode ranging from 1 to 2, and I_S is the saturation current, usually dependent in the temperature, solar irradiance and band-gap energy [9].

By applying Kirchhoff laws to the circuit model, the relationship linking the output current and the output voltage is found, as seen in Eq. (2.3).

$$I = I_{ph} - I_D - I_{sh} \tag{2.2}$$

$$I(V) = I_{ph} - I_S(e^{\frac{V+I(V)R_s}{na\frac{kT}{q}}} - 1) - \frac{V + I(V)R_s}{R_{sh}} \tag{2.3}$$

Although the physical model of the solar cell is not the primary focus of this thesis, it plays an important role in studying specific mission profiles and their implications for daily variations in solar irradiance and temperature based on geographic location. For the purposes of this work, however, the focus will be on utilizing empirical models derived from experimental parameters. The power converter design for this specific case will be developed in a general manner, leaving the design for a specific mission profile as a potential topic for future work.

To simplify the working behavior of a photovoltaic panel, this work will leverage a utility tool in *PSIM*, which allows the incorporation of key parameters derived from commercial photovoltaic panel datasheets. Datasheets from photovoltaic panel manufacturers typically provide parameters like open-circuit voltage, short-circuit current, and maximum power point, which are essential inputs for the *PSIM* utility tool. For working with the physical model, an inference on the circuit parameters must be done starting from the datasheet, which can be cumbersome.

By inputting parameters such as open-circuit voltage, short-circuit current, and maximum power point values, the utility tool can generate IV curves that represent the photovoltaic panel behavior under various environmental conditions. This approach enables an efficient and realistic representation of the panel electrical characteristics without delving into complex physical modeling, while still capturing the critical performance metrics required for the analysis.

The interface of the *PSIM* Solar Module utility can be seen in Fig. 2.2. Some parameters are not stated in the manufacturer datasheet but can be inferred according to the technological aspects of the photovoltaic panel such as type of semiconductor being utilized. With the initial parameters inference, small increments/decrements may be needed to fit the curve, mainly such that the maximum power point position is correct.

In the section "Operating conditions" from the interface, several curves can be extracted depending on temperature and solar irradiance. In this work, the temperature is considered to be constant (25°C) with variable solar irradiance.

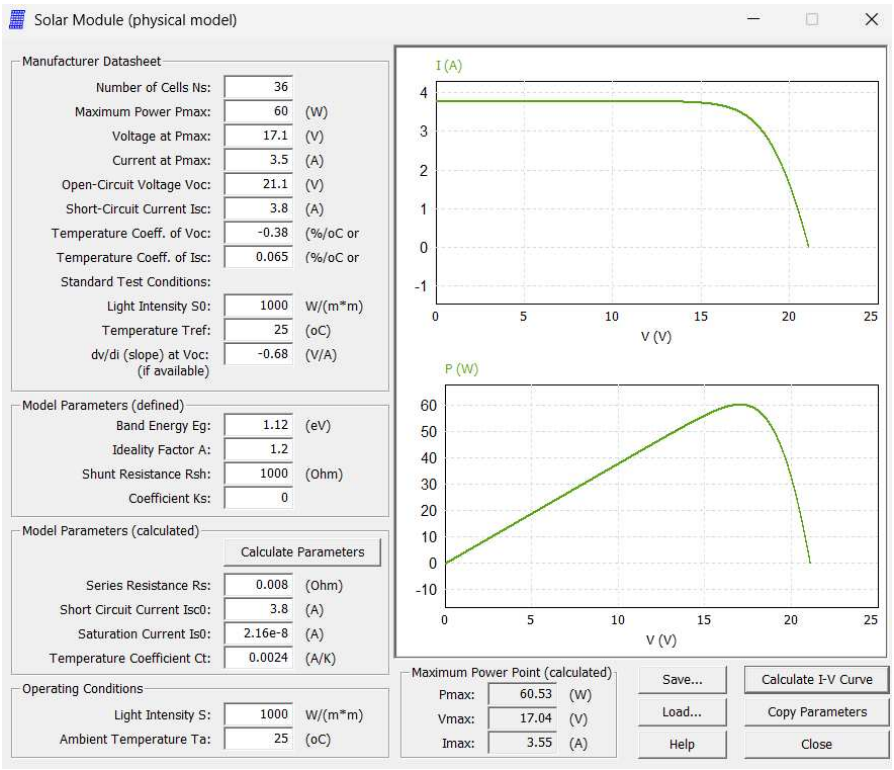


Figure 2.2: *PSIM* Solar Module utility interface

2.1.2 Selected photovoltaic panel modeling and maximum power points

The proposed photovoltaic panel for this work is the commercial model 3SHBGHA#-680 from 3SUN, which characteristics can be found in [10]. Table 2.1 summarizes the parameters used to extract the curves as well as some commentary on inferred/recommended values.

The IV curves can be extracted as a text file with the information separated in columns. This allows for then processing the information in a program like *MATLAB*, which will then further aid this work in the design phase. Figs. 2.3 and 2.4 show the ability to display the extracted data from *PSIM* in *MATLAB* for multiple irradiance values at a working temperature of 25°C, the code for processing the information is found in the Appendix A.1.

Parameter	**Value**	**Comments**
Number of Cells Ns	60	Number of series cells
Maximum Power Pmax	680 (W)	-
Voltage at Pmax	36.49 (V)	-
Current at Pmax	18.64 (A)	-
Open-Circuit Voltage Voc	44.2 (V)	-
Short-Circuit Current Isc	19.78 (A)	-
Temperature Coeff. of Voc	-0.2 ($\frac{\%}{°C}$)	-
Temperature Coeff. of Isc	0.044 ($\frac{\%}{°C}$)	-
Light Intensity S0	1000 ($\frac{W}{m^2}$)	Standart Test Conditions (STC)
Temperature Tref	25 (°C)	Standart Test Conditions (STC)
dv/di (slope) at Voc	0 (V/A)	*PSIM* documentation recommends 0 when not available
Band Energy Eg	1.12 (eV)	Typical value for Mono-crystalline n-type Si
Ideality factor	1.87	Tuned value to fit the curve
Shunt Resistance Rsh	1000 (ohm)	Typical value for Mono-crystalline n-type Si
Coefficient Ks	0	*PSIM* documentation recommends 0 when not available

Table 2.1: Summary of *PSIM* Solar Module utility tool parameters

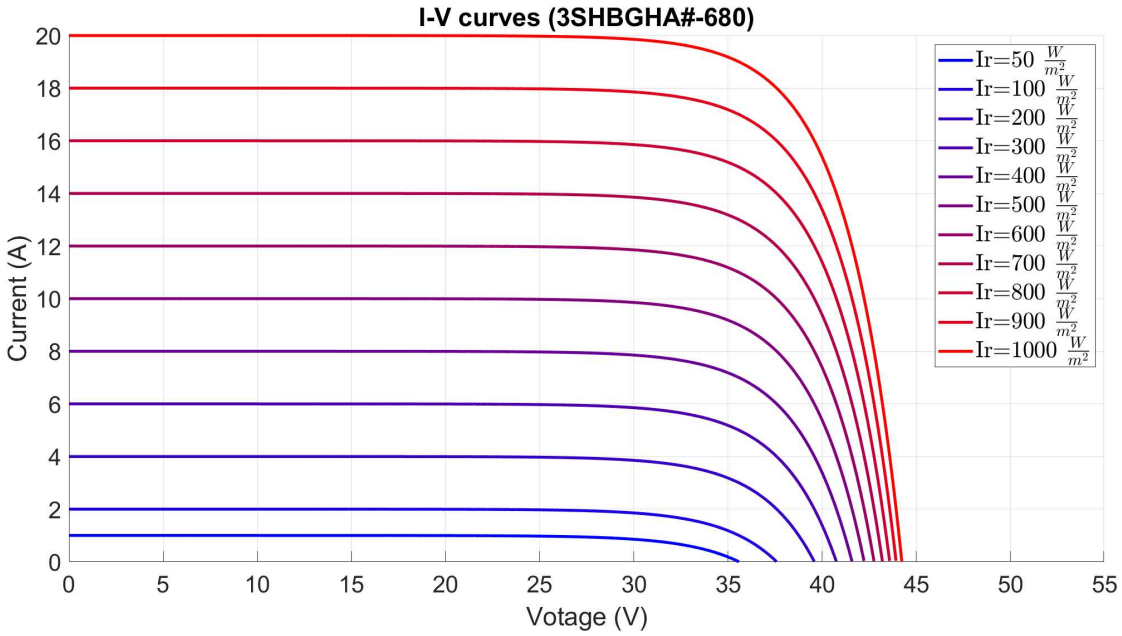


Figure 2.3: I-V characteristic for multiple irradiance values

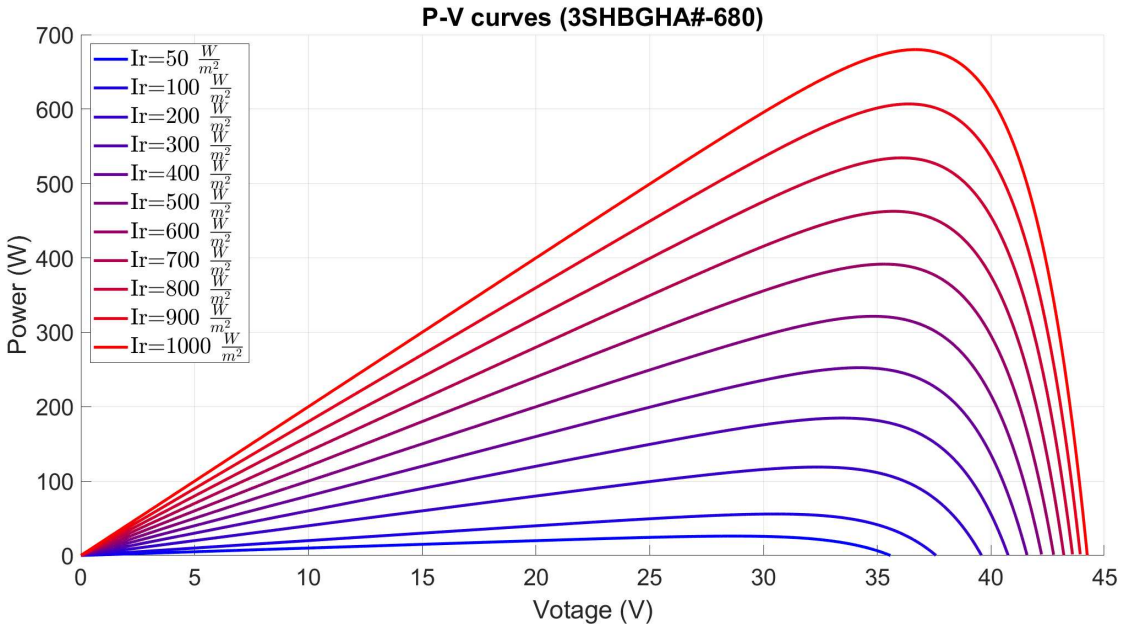


Figure 2.4: P-V characteristic for multiple irradiance values

As it can be seen in Figs. 2.3 and 2.4, the PV curves present a maximum power point (MPP) for each irradiance value. If the grid is considered as an infinite power sink, which is a reasonable assumption as renewable energy is intended for instant consumption, while other methods serve for buffering as mentioned in the introduction; it is of interest to work in the vicinities of these points, extracting the maximum power from the photovoltaic panel.

This is achieved by implementing a Maximum Power Point Tracking (MPPT) control scheme, which interacts with the driving of the power converter of the solar energy system to force this working point. There are several ways of implementing MPPT control, which are not the scope of this work, however, the concept introduces important criteria for optimization of the circuit. If the MPPs are intended to be exploited, then it is reasonable to optimize the design of the DC-DC converter so that the maximum efficiency is achieved in the input-voltage range where the MPPs happen.

2.1.3 Strings configurations and micro-inverters

A photovoltaic panel is composed of multiple solar cells connected in an array fashion, series connection of cells provides a raise of the output voltage, while parallel connection of cells provides a raise of the current capability.

This process is also applied to photovoltaic panels as seen in Fig. 2.5 [11], a string configuration is composed of multiple panels connected in series, while a PV array is a set of strings connected in parallel. This creates a variety of alternatives which set different specifications for the power conversion systems.

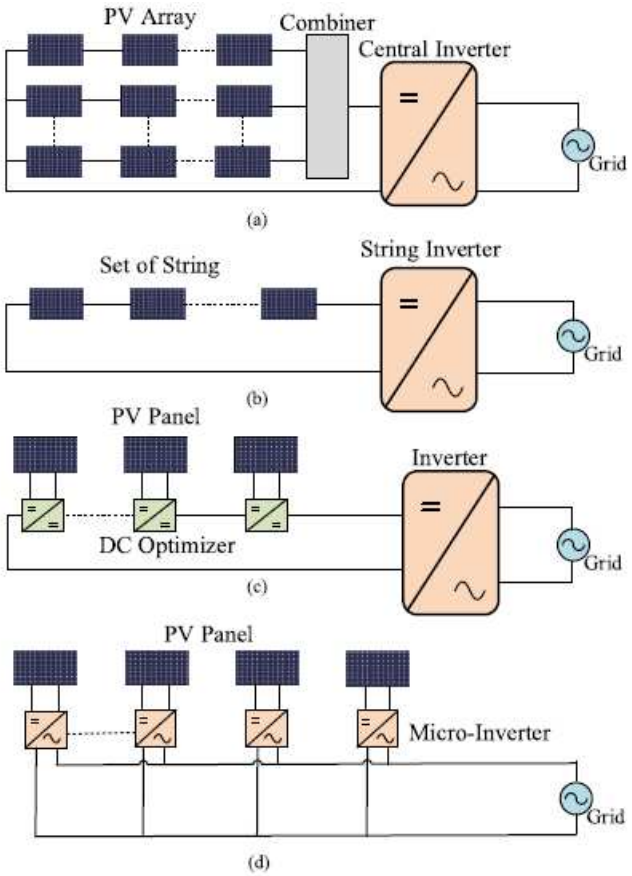


Figure 2.5: Different types of photovoltaic panels connection. (a) central-inverter system, (b) string-inverter system, (c) dc optimizer, and (d) micro-inverters built into individual panels. Picture adopted from [11].

Micro-inverter systems are analyzed in this work, they are advantageous in comparison with the other alternatives [12] in the following aspects:

- They allow for a compact design where the power converter can be attached to the back of the photovoltaic panel, increasing flexibility and modularity.
- They allow for plug-and-play type of systems where complexity of installation is greatly reduced.
- Unlike string/central systems, the malfunction of one photovoltaic panel does not affect the overall performance of the system, as every photovoltaic panel behaves as a standalone system.
- Unlike string/central systems, independent MPPT control schemes over each

photovoltaic panel ensure the maximum power extraction, making them the best option in mismatch conditions between panels. In strings configurations, the distributed MPPT control along a string may not align with the MPP of all photovoltaic panels.

- Unlike DC optimizer based systems, the malfunction of the inverter does not pull off the grid the entire power generation system.

However, they have limitations which make them non-ideal in certain scenarios:

- In large power production systems, cost is a critical factor, micro-inverter systems implement one power converter for each photovoltaic panel, making them expensive in contrast with centralized schemes.
- The absence of series string connection requires high DC gain power converters to meet the voltage requirements of the grid.

Considering the actual global electricity grid, the advantages and limitations make them a great alternative for decentralized grid expansion, as mentioned in the introduction of this work.

The power converters for micro-inverter systems vary topologically, in [11] and [12] the typical implemented schemes are showcased, varying mainly within single and double stages systems, with or without isolation as seen in Fig. 2.6.

The DC-DC converter proposed in this work is part of a double-stage micro-inverter system, where the DC-DC converter is designed to operate independently from the DC-AC inverter. The particular topology of this work is not found in Fig. 2.6 as it is a new proposal for micro-inverter topologies. The particular details of the topology implemented for this work will be expanded in the following sections.

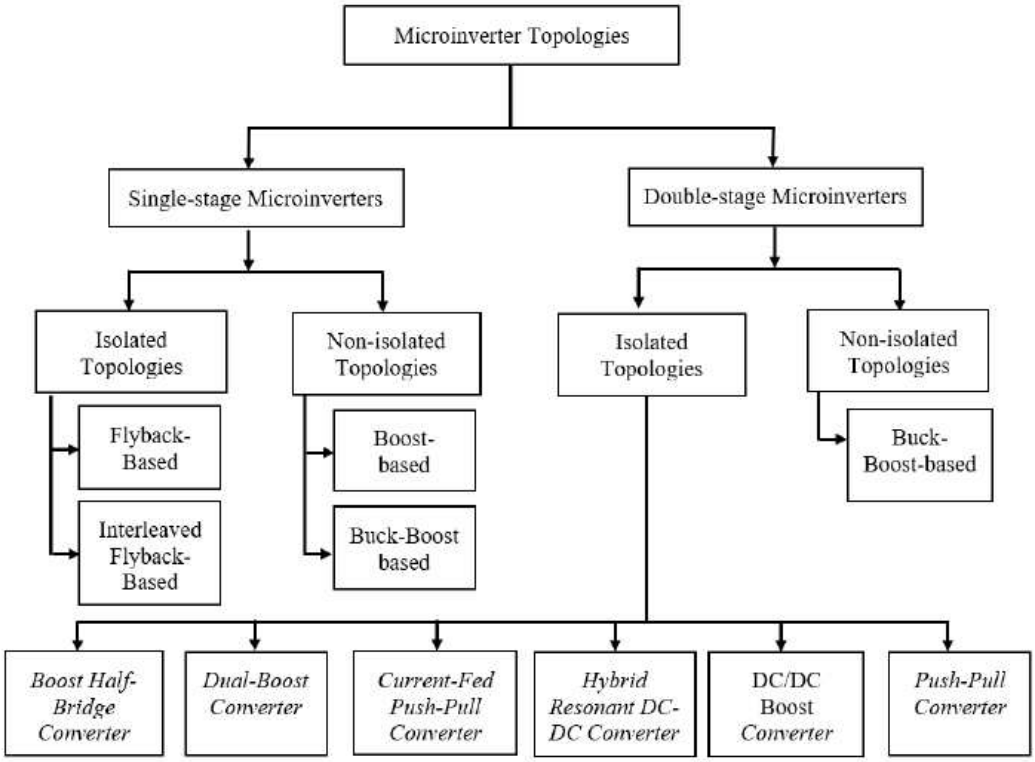


Figure 2.6: Micro-inverter topologies classification

2.2 Proposed DC-DC Converter Framework

2.2.1 Partial Power Processing: advantages and limitations

Full power processing is the most common scenario in power conversion systems. A full power converter is the one in which power flows through the architecture at a complete rate.

Partial Power Processing (PPP) is the power flow scheme in which one or more power converters do not process the entirety of the available power at the input to the output [13]. The power is split through different converters, reducing considerably voltage and current stress.

Implementations of PPP are mainly based on two different architectures, the Input-Parallel Output-Series (IPOS) configuration and the Input-Series Output-Parallel (ISOP) configuration, shown in Figs. 2.7 and 2.8. Both architectures are presented with their generalized architecture, however, in this work, the IPOS configuration is exploited with the by-pass converter in the form of a "pass-through"

converter, as shown in Fig. 2.9, providing unitary voltage gain with theoretical 100% efficiency, assuming wire losses negligible. The pass-through converter concept allows for better performance, providing a boost in efficiency given the direct path of power to the load, while also reducing stresses in terms of voltage and current of the converter devices thanks to the PPP configuration, allowing for the downsizing of components [14].

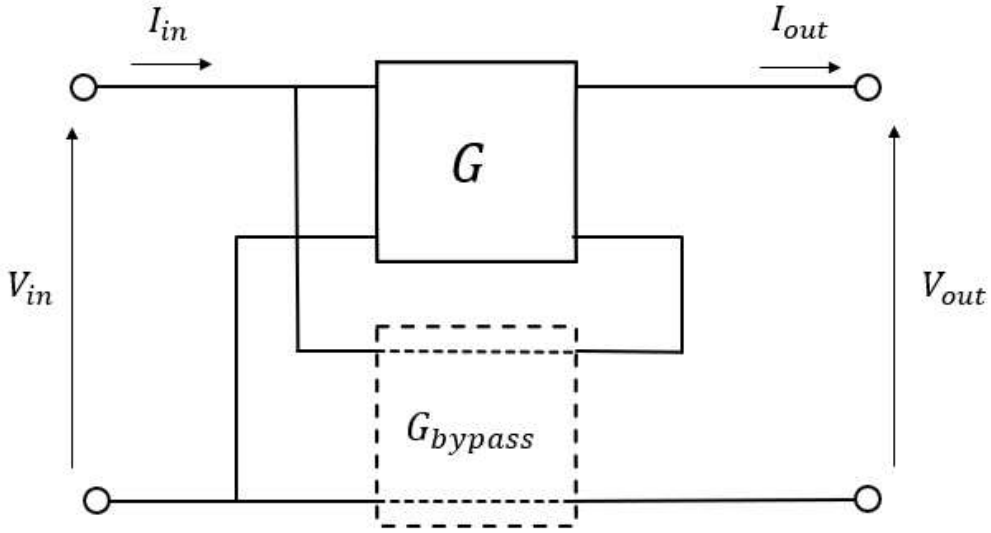


Figure 2.7: General IPOS configuration overview

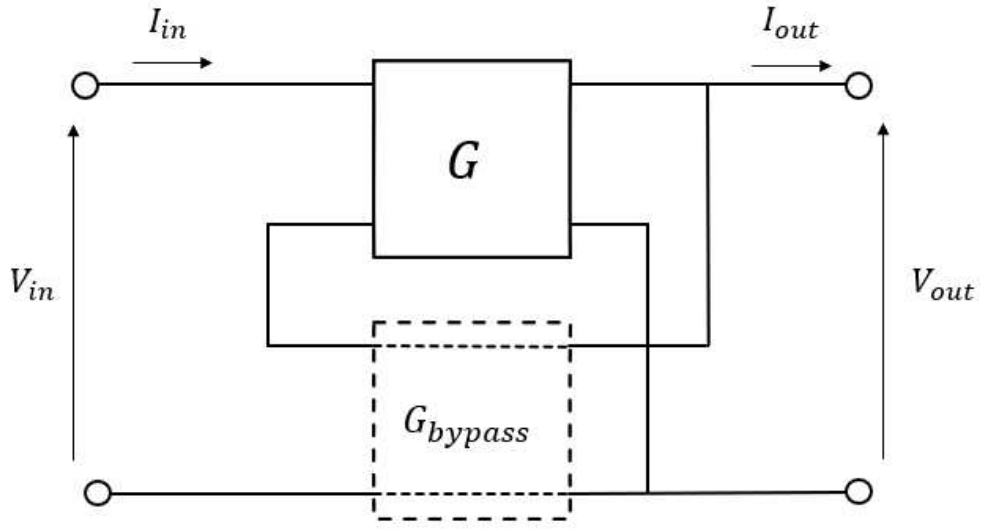


Figure 2.8: General ISOP configuration overview

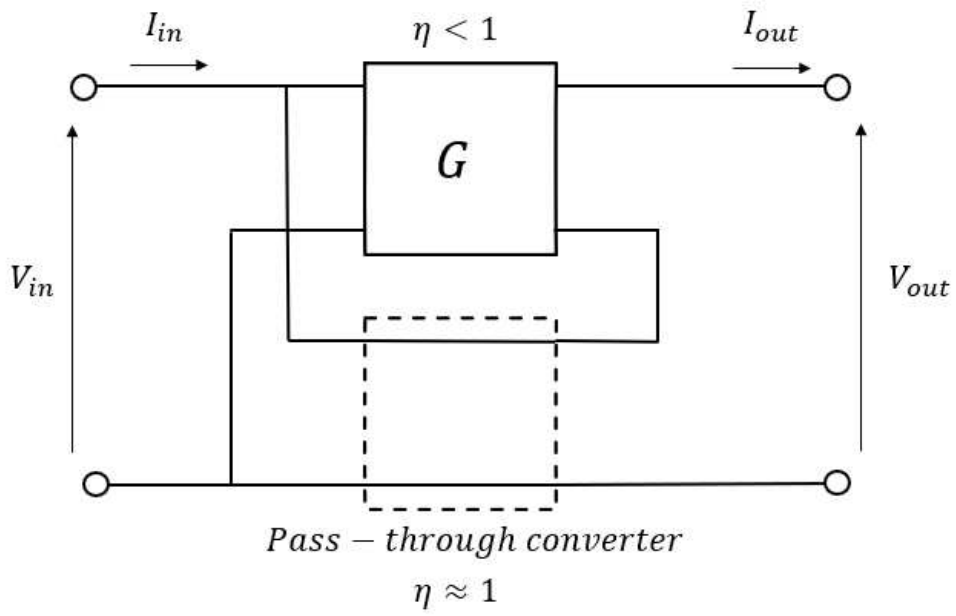


Figure 2.9: Pass-through converter IPOS configuration overview

The Pass-through IPOS converter has two main advantages with respect to full power conversion, as well as two main drawbacks.

The first main advantage is the decrease in voltage and current stress in the full power converter. Considering the input port to the power converter G, I_{in} splits into a portion of current flowing into G and a portion of current flowing into the Pass-trough converter, then reduced current stress at the input is achieved compared to the full converter which would experience I_{in} entirely. In terms of voltage, the output voltage V_{out} is formed as the series connection of V_{in} and $V_{G_{out}}$ which essentially means that $V_{G_{out}}$ is lower than V_{out}, creating reduced voltage stress at the output of the converter. This phenomenon is highlighted in Fig. 2.10.

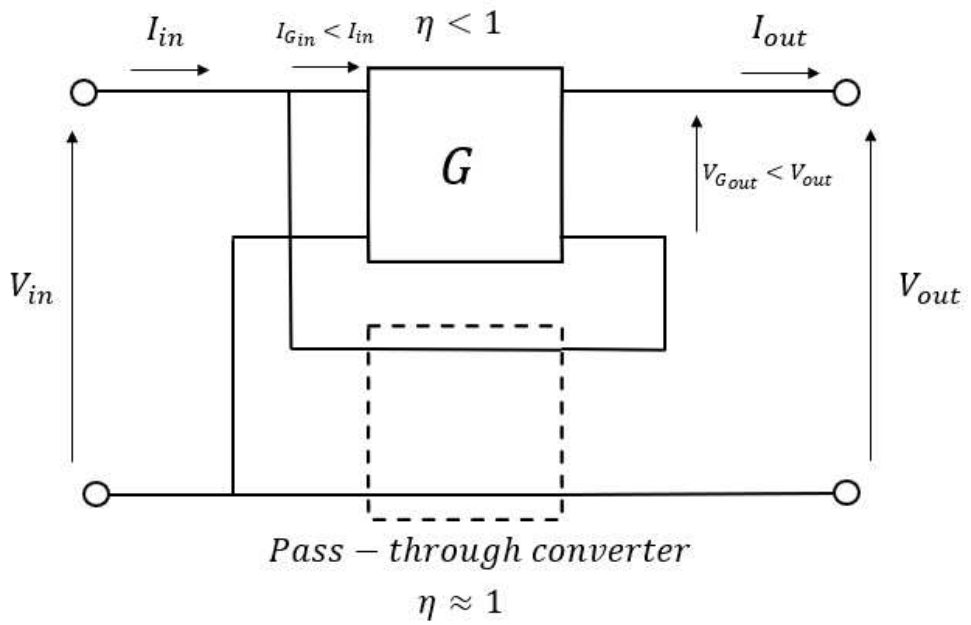


Figure 2.10: Reduced stress visualization of the Pass-through IPOS configuration

The second main advantage is the improvement in efficiency to the overall system, given that part of the power is directly transferred to the output with the theoretical 100% efficiency. The overall system efficiency can be quantized according to the power split as seen in Eq. (2.5), making use of Eq. (2.4). In Fig. 2.11, the dotted lines represent the plain efficiency values the stage could present (η_G), while the solid lines represent the overall system efficiency with IPOS configuration (assuming constant efficiency through all gain values just for visualization), it can be seen how the system efficiency is always equal or greater than η_G.

$$\eta_G = \frac{P_{G_{out}}}{P_{G_{in}}} = \frac{V_{G_{out}} I_{out}}{V_{in} I_{G_{in}}} = G\frac{I_{out}}{I_{G_{in}}} \longrightarrow I_{G_{in}} = G\frac{I_{out}}{\eta_G} \tag{2.4}$$

$$\eta_{system} = \frac{P_{out}}{P_{in}} = \frac{V_{out} I_{out}}{V_{in} I_{in}} = \frac{(GV_{in} + V_{in}) I_{out}}{V_{in}(I_{G_{in}} + I_{out})} = \frac{(G+1) I_{out}}{G\frac{I_{out}}{\eta_G} + I_{out}} = \boxed{\frac{G+1}{1+\frac{G}{\eta_G}}} \tag{2.5}$$

The first main drawback, which can also be observed in Fig. 2.11, is the fact that the efficiency boost is greatly reduced for high gain values of the power converter. This is logical, as the more gain the converter provides, the less significant is the direct V_{in} connected in series to the converter output. It is also interesting to note

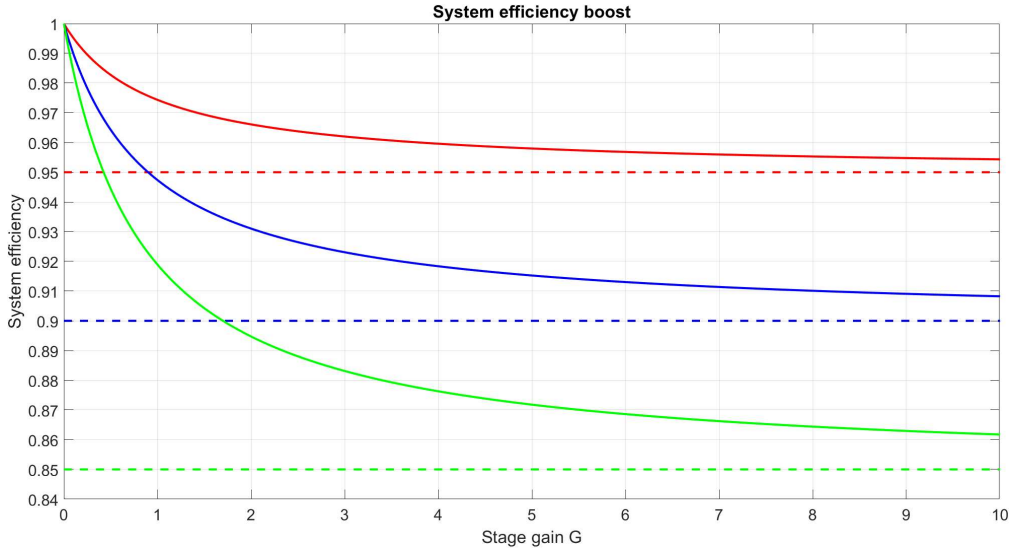


Figure 2.11: System efficiency boost of the Pass-through IPOS configuration. Stage simplified efficiency profiles (dotted lines) versus stage with same efficiency profile connected in IPOS configuration (solid lines)

how approaching lower gains takes more advantage of the power splitting effect, effectively adopting the direct path 100% efficiency at gain 0, which would be equivalent to having a pair of wires between input and output. This mechanic of gain dependence of the efficiency boost will be a critical factor for the proposed architecture.

The power flow can also be quantized to understand how lower gain values create a greater amount of power flow through the more efficient direct path. In Eqs. (2.6) and (2.7), the power split can be analyzed in terms of gain of the stage, considering conservation of power, while this can be visualized in Fig. 2.12 normalized to the total power flowing through the entire IPOS configuration.

$$P_{out} = V_{out}I_{out} = (G+1)V_{in}I_{out} = V_{in}I_{out} + GV_{in}I_{out}$$
$$P_G = V_{G_{out}}I_{out} = GV_{in}I_{out}$$
$$Normalizing:$$

$$\frac{P_G}{P_{out}} = \frac{GV_{in}I_{out}}{V_{in}I_{out} + GV_{in}I_{out}} = \boxed{\frac{G}{G+1}} \tag{2.6}$$

$$\frac{P_{pass-through}}{P_{out}} = \frac{P_{out} - P_G}{P_{out}} = 1 - \frac{P_G}{P_{out}} = \boxed{\frac{1}{G+1}} \tag{2.7}$$

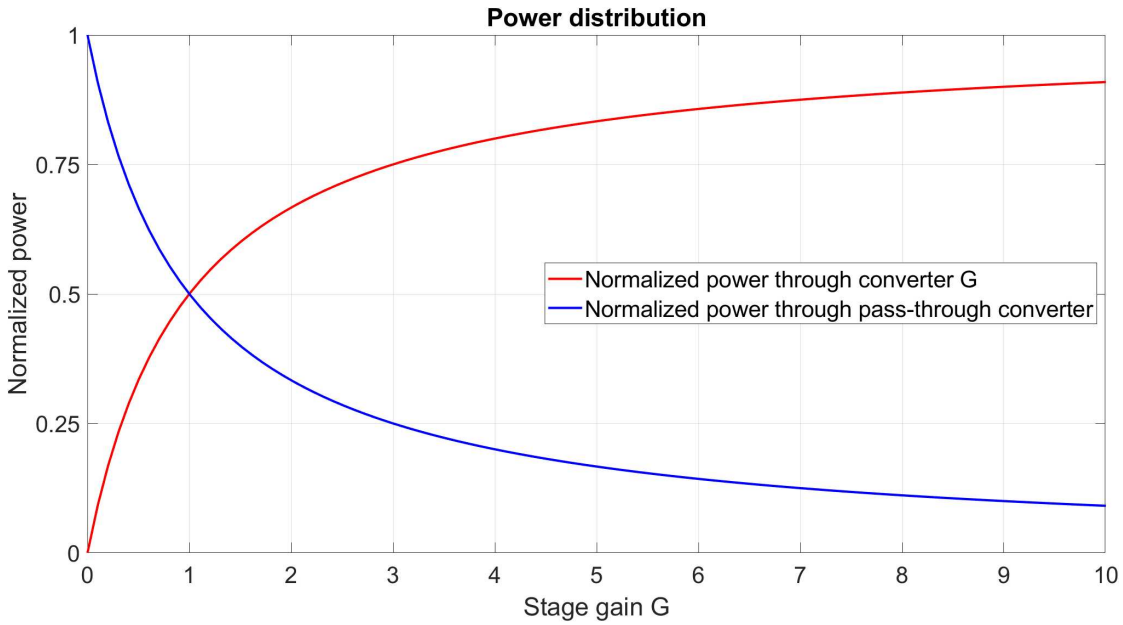


Figure 2.12: Power split and stage gain in the IPOS configuration

The second main drawback, and much more critical, is the fact that the possible topologies for G are greatly reduced, as to be able to apply the IPOS connection, non-commonly grounded topologies are mandatory. Commonly grounded topologies create a short-circuit hazard that can be visualized in Fig. 2.13, where a simple boost converter is employed as G. This aspect is critical for the topology selection in this work.

The non-commonly grounded topologies requirement is achieved by making use of isolation transformer based architectures. This creates a galvanic separation of the circuit, making the secondary side sector of the architecture floating with respect to the ground of the primary side sector. This second main drawback not only consists in a restricted selection of the topology, but also creates the need for isolation in a configuration that will essentially be non-isolated, as this property is lost due to the pass-through converter connection, the output and the input share the same ground, although the stage implements isolation.

The absence of isolation in a system can pose safety risks, such as ground faults and the circulation of common-mode currents through the stray capacitance of the photovoltaic panel to the ground [15]. However, it is important to notice that this work focuses on the DC-DC converter stage, several non-isolated architectures have been proposed to improve the performance of the system. Isolation is a requirement that depends on the specific application, the power converter stage proposed here is a fraction of the whole system, it could be used in scenarios where

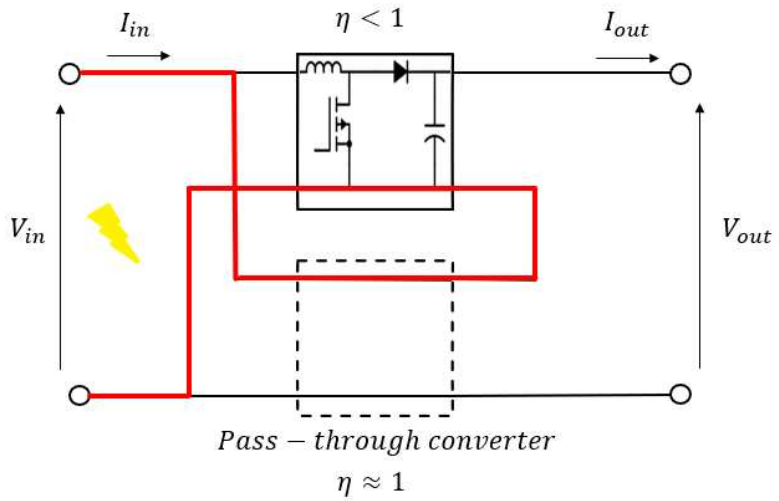


Figure 2.13: Short-circuit hazard in IPOS configuration

isolation is not mandatory, and in the case it is, isolation could be implemented in the DC-AC stage connected to the grid in the form of an isolation transformer. Transformer-less topologies for the DC-AC converter have also been proposed to reject common-mode currents in diverse ways [16].

2.2.2 Proposed power converter

In Fig. 2.4 from Section 2.1.2, it can be observed that the selected photovoltaic panel, as is generally the case, exhibits a wide input voltage range. This range needs to be stepped up to a much higher, constant voltage to feed the DC-AC converter connected to the grid. In Italy, the commercial grid operates at 230 V_{RMS} and 50 Hz, corresponding to a peak sinusoidal voltage of 325.27 V. To account for AC-DC conversion losses and provide a safety margin, the proposed converter is designed to step up the voltage to 350 V.

A limitation to the input voltage range is set between reasonable values, for this particular application the range 15-43 V is considered, which categorizes this converter as a wide-input DC-DC converter. This wide input range imposes a wide range of DC gain with values between 8.14 at maximum input voltage and 23.33 at minimum input voltage for constant output voltage.

The high gain regulation scheme threatens the IPOS configuration advantage of performance boosting. As analyzed in the previous section, higher gain implies less power flow through the pass-through converter, effectively reducing the efficiency raise of this architecture. For overcoming this situation, this new proposed converter

employs two IPOS configurations connected in a quadratic manner as showed in Fig. 2.14.

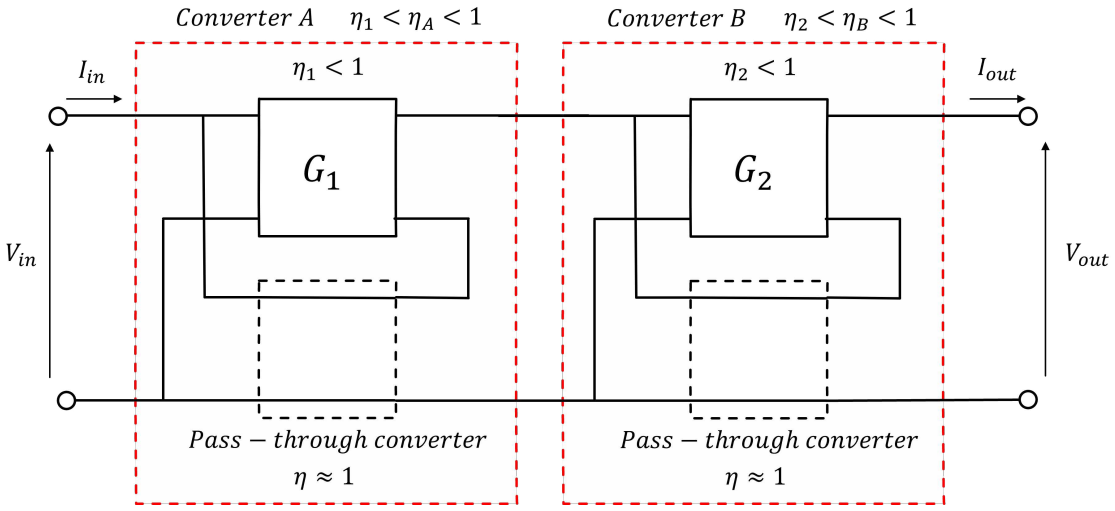


Figure 2.14: Proposed power converter architecture

In full quadratic power converters, the total system efficiency is the product of the efficiencies of each individual power converter. The proposed approach follows the same principle but offers an advantage: each stage benefits from an efficiency boost that depends on its gain. In quadratic converters, the required gain per stage can be significantly lower while still achieving a high overall gain, since the total system gain is the product of the gains of each stage, as shown in Eq. (2.8).

$$G_{total} = (G_1 + 1)(G_2 + 1) \tag{2.8}$$

The total DC-DC converter efficiency can be derived by utilizing the expression found in Eq. (2.5) considering the total efficiency as the product of both converters efficiencies, as seen in Eq. (2.9). The fact that each term is greater than the individual stage efficiency implies that this total converter efficiency with IPOS configuration is greater than the case in which the converter was only composed of the two simple stages connected in quadratic form (Eq. (2.10)).

$$\eta_{total_{proposed}} = \frac{G_1 + 1}{1 + \frac{G_1}{\eta_1}} \frac{G_2 + 1}{1 + \frac{G_2}{\eta_2}} = \eta_1 \eta_2 \frac{G_1 + 1}{G_1 + \eta_1} \frac{G_2 + 1}{G_2 + \eta_2} \equiv (<1)(<1)(>1)(>1) \tag{2.9}$$

$$\eta_{total_{full-power\ converter}} = \eta_1 \eta_2 \equiv (<1)(<1) \tag{2.10}$$

By modulating the gain of each stage, the whole gain range can be achieved, producing different efficiency impact depending on how the gain is distributed across both stages.

2.2.3 Equivalent stage loading and decoupling

Partial power processing architectures such as the IPOS configuration make designing each stage challenging as the power split dependence on the stage gain dynamically changes the stage processed power. This relationship is even more complex in this work scheme, where a decision has to be made on how to distribute the gain between two stages with changing processed power depending on each other.

For this task, proposing a decoupling method is useful, to allow designing each stage separately, modeling the influence of the other stage in simpler manner. This can be achieved by computing an equivalent impedance at the direct output of each converter.

As previously stated, the DC-AC converter of the complete system is not of interest for this work, hence it can be modeled as a power consumer which dynamics can be decoupled from the DC-DC converter. In a solar energy production system, the DC-AC converter can be approximated as a resistive load when viewed from the perspective of the DC-DC converter, given that the dynamic behavior is correctly decoupled. This modeling assumption is justified with the filtering capacitor at the output of the DC-DC converter serving as a dynamics decoupler through energy storing, effectively decoupling the switching behavior of the DC-AC converter from the DC-DC converter output. Consequently, the DC-DC converter sees the DC-AC converter as a steady load with a resistance value determined by the power drawn, which value can be estimated from the available power at the input of the system and the output voltage, as seen in Eq. (2.11). This simplified resistive model is particularly useful for analyzing power flow and optimizing the design of the DC-DC converter.

The same concept of modeling the load as a constant resistor according to the power drawn can be applied whenever there is a capacitor large enough to decouple the high-frequency dynamics of the next stage that is being replaced by the resistor. Hence, this idea can also be applied to the first stage load, considering the second stage as a steady power consumer. This equivalent loading behavior is shown in Fig. 2.15. It can be seen in Eqs. (2.12) and (2.13) that the equivalent load resistor experienced by each stage is lower than the DC-AC load equivalent resistor, and that the reduction is highly dependent on the stages DC gain. This effect will be crucial for the design of each stage.

$$R_L = \frac{V_{out}}{I_{out}} = \frac{V_{out}^2}{P_{out}} \approx \frac{(350V)^2}{P_{in}} \tag{2.11}$$

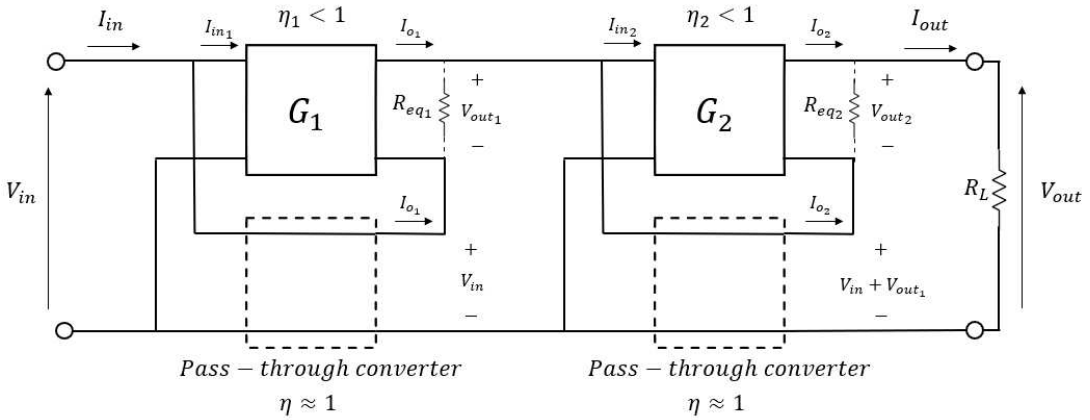


Figure 2.15: Stage equivalent load resistances

$$\begin{aligned}
R_{eq_2} &= \frac{V_{out_2}}{I_{o_2}} = \frac{V_{out} - (V_{out_1} + V_{in})}{I_{out}} \\
&= \frac{V_{out} - (G_1 V_{in} + V_{in})}{I_{out}} = \frac{V_{out} - V_{in}(G_1 + 1)}{I_{out}} \\
&= \frac{V_{out} - \frac{V_{out}}{G_{tot}}(G_1 + 1)}{I_{out}} = \frac{V_{out}}{I_{out}} \frac{G_{tot} - (G_1 + 1)}{G_{tot}} \\
&= \frac{V_{out}}{I_{out}} \frac{(G_1 + 1)(G_2 + 1) - (G_1 + 1)}{(G_1 + 1)(G_2 + 1)} \\
&= \boxed{R_L \frac{G_2}{G_2 + 1}} \rightarrow R_{eq_2} < R_L
\end{aligned} \tag{2.12}$$

$$\begin{aligned}
R_{eq_1} &= \frac{V_{out_1}}{I_{o_1}} = \frac{G_1 V_{in}}{\frac{I_{in}}{G_1 + 1}} = \frac{V_{in}}{I_{in}} G_1 (G_1 + 1) \\
&= \frac{\frac{V_{out}}{G_{tot}}}{G_{tot} I_{out}} G_1 (G_1 + 1) = \frac{V_{out}}{I_{out}} \frac{G_1 (G_1 + 1)}{G_{tot}^2} \\
&= R_L \frac{G_1 (G_1 + 1)}{(G_1 + 1)^2 (G_2 + 1)^2} = R_L \frac{G_1}{(G_1 + 1)(G_2 + 1)^2} \\
&= \boxed{R_L \frac{G_1}{G_1 + 1} \frac{1}{(G_2 + 1)^2}} \rightarrow R_{eq_2} << R_L
\end{aligned} \tag{2.13}$$

It is worth noting that the expressions found in Eqs. (2.12) and (2.13) for the equivalent resistance values are an approximation, in the sense that for their derivation, power conservation through the stages is assumed, which is equivalent as stating that the system is lossless. With high efficient stages the discrepancy is low and the results are acceptable for the design flow.

At this point, the expressions in Eqs. (2.12) and (2.13) can be graphically represented to illustrate the difference on magnitude of resistance reduction. In Figs. 2.16 and 2.17, it can be seen how the equivalent resistance at each stage normalized to the output resistance is reduced, this effect being much more pronounced for the first stage. Further into the analysis, the gain profile that will be defined for each stage will morph the system load characteristic to the equivalent resistance at the output port of each stage.

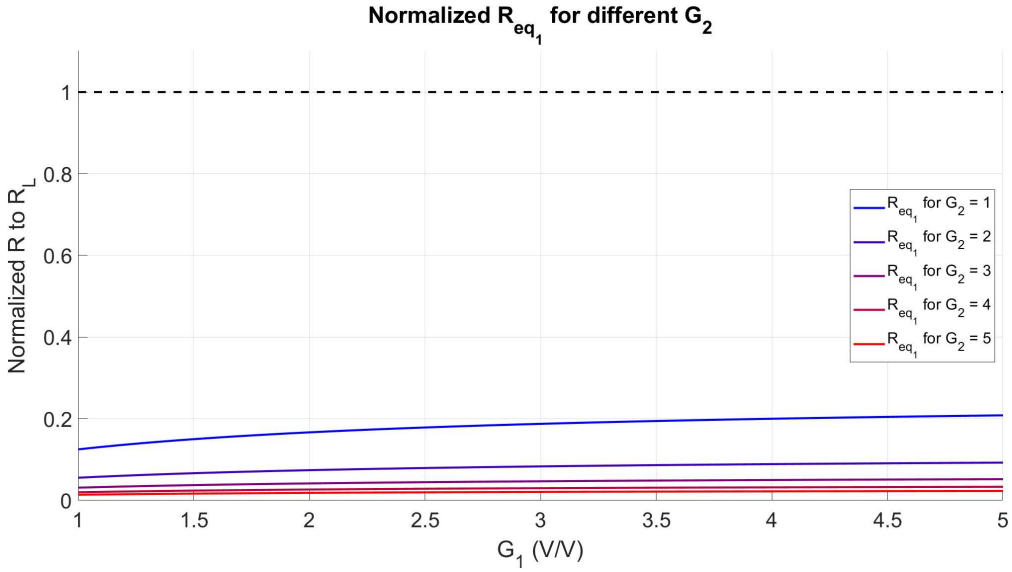


Figure 2.16: First stage equivalent load resistance reduction

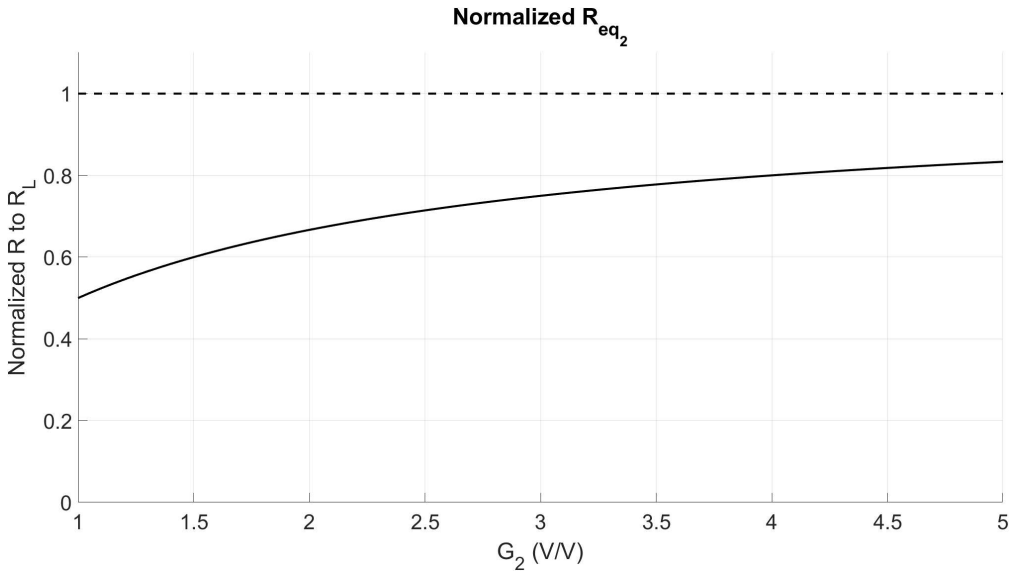


Figure 2.17: Second stage equivalent load resistance reduction

Chapter 3

Resonant Power Converters and the LLC topology

3.1 Resonant Power Converters

3.1.1 High-frequency power conversion

High-frequency non-linear power converters have emerged as the standard for power conversion in recent decades due to their superior performance in terms of efficiency and power density [17]. These converters are widely used in applications from renewable energy systems to consumer electronics, where minimizing energy losses and reducing size are critical design objectives.

One of the key factors contributing to their high power density is the increase in operating frequency. When rising the operating frequency, the size of passive components, such as inductors and capacitors, decreases due to the inverse relationship between component size and operating frequency. This allows for more compact designs, enabling the development of smaller and lighter systems.

In addition to power density, high efficiency is another main advantage of these converters. Efficiency is primarily achieved by carefully controlling the operation of semiconductor devices, such as MOSFETs and IGBTs, to minimize power dissipation. This involves operating the devices in specific regions of their characteristics: the saturation region (ON state) and the cut-off region (OFF state).

The amount of dissipated power in power converters is critical for designing these type of systems. Minimizing lost power not only contributes to a high-efficiency system which is capable of exploiting in the best way the available power, but

it also influences the safety of the system. Due to the main power dissipation phenomenon being heat, care must be taken as how this heat is handled, if not treated correctly, the rise in temperature in the circuit can lessen the lifetime of the converter, or even its rapid malfunction by surpassing temperature limits of components.

Power loss as heat dissipation in semiconductor devices is observed in two forms; the first one is the conduction loss when the device is operating in the saturation region (ON state), where the current flowing through the device will generate Joule effect losses due to the non-ideality of the channel having a non-null resistance value. This factor can be minimized in a technological approach, by selecting better devices. The second one are the switching losses, which happen at the transition between states of a semiconductor device, The ON and OFF state are low power dissipating working points, but the trajectory in the I-V characteristic of the device when transitioning from one point to the other defines the switching losses.

Implementing power conversion with high operating frequencies to enhance power density comes with its challenges, higher operating frequency introduces increased switching and magnetic losses, limiting the efficiency behavior at high frequencies.

Hard and soft switching are different techniques for going from an ON state to an OFF state and vice-versa, each one with a characteristic trajectory between the two working points. In Fig. 3.1, these different trajectories can be observed. In Figs. 3.2 and 3.3, the trajectories can be seen as a function of time for the current and voltage, and how the overlap of non-null values produce power dissipation.

The time spent during the trajectories of high dissipation is undesirable, but unavoidable due to the reactive components present in the physical architecture of power semiconductor devices, which add these disadvantageous dynamics to the device.

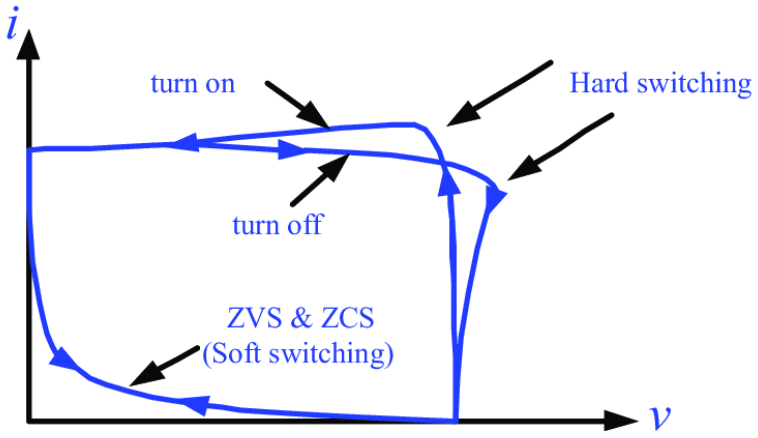


Figure 3.1: Hard and soft switching I-V trajectories

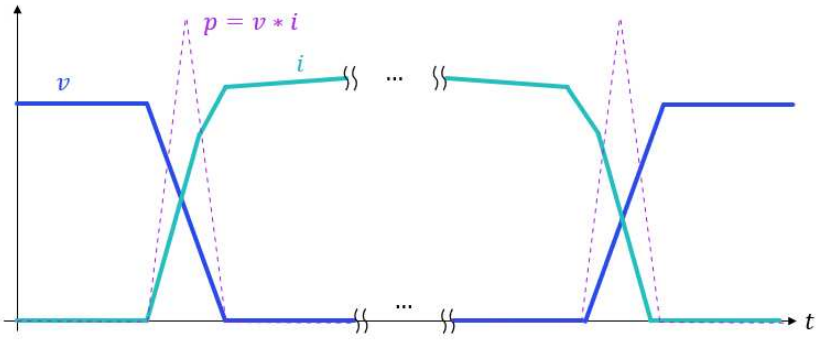


Figure 3.2: Typical hard switching waveforms

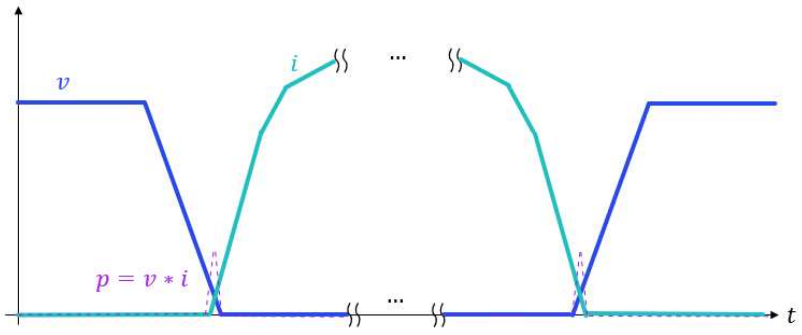


Figure 3.3: Typical soft switching waveforms

Another important characteristic is that, in most applications, hard switching causes rapid changes in current over short time intervals, resulting in significant Electromagnetic Interference (EMI) [18]. Soft switching techniques aim to shape the current waveform to reduce the rate of change of current ($\frac{di}{dt}$), thereby minimizing EMI and enabling a more robust and EMI-compliant design.

Soft-switching techniques are primarily based on shaping the current and voltage waveforms to enable smoother transitions over time. This has two main benefits: it reduces EMI by avoiding abrupt changes in current and voltage, and it intrinsically lowers switching losses. At turn-on, the current starts from or near zero and rises smoothly, while at turn-off, the current tends to decrease gradually to zero. These controlled transitions minimize the overlap between voltage and current during switching events, significantly reducing energy dissipation.

3.1.2 General architecture of resonant power converters

Resonant power converters are a type of high-frequency uni-directional power converter in which resonance is exploited to shape the current waveform in order to achieve soft-switching. Current shaping is achieved by employing auxiliary circuits, which are implemented as a resonant network. These circuits introduce resonance into the system, enabling smooth transitions in current and voltage. Various resonant techniques have been developed for soft switching, including quasi-resonant (QR) methods, series, parallel, and series-parallel resonance, multi-resonant (MR) approaches, and resonant-transition (RT) techniques [18]. Each method is designed to address specific power and frequency ranges while optimizing switching performance.

The general architecture of a resonant power converter can be observed in Fig. 3.4. It is worth noting that architectures for resonant converters exist with and without the presence of an isolation transformer.

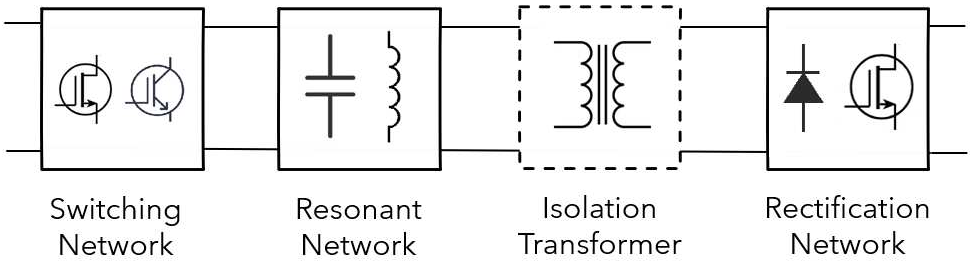


Figure 3.4: General architecture of a resonant power converter

Resonant techniques are particularly advantageous in high-frequency applications

where conventional hard-switching circuits would suffer from excessive switching losses and EMI. These approaches leverage the natural oscillatory behavior of LC networks to shape the circuit waveforms producing soft switching without the need for complex control schemes. Additionally, they allow designs to achieve high efficiency across a wide range of operating points [19].

While many resonant techniques exist, their applicability depends on the design goals and constraints of the power converter. For instance, quasi-resonant circuits are simpler and suitable for low-to-moderate power applications, whereas multi-resonant and resonant-transition approaches can handle higher power levels with greater flexibility. The choice of topology also impacts component sizing, circuit complexity, and cost.

The LLC resonant power converter, which will be analyzed in detail in a subsequent section, exemplifies the advantages of current shaping and resonance. Its ability to achieve zero-voltage switching (ZVS) and adapt to varying load conditions has made it a popular choice for high-efficiency, high-frequency applications.

Achieving this soft-switching scheme through resonance without the need of dedicated control schemes is a great advantage in terms of ease of implementation. However, the introduction of resonance in a circuit derives three main challenges:

- Increased component stress, mainly in the resonant network components, as in a resonant circuit voltage levels can surpass the ones of the input.
- The mathematical model describing the circuit operating in several working points is complex, plenty of architectures present transcendental descriptions that have to rely in numerical analysis [20].
- Paired with the previous point, the introduction of resonance creates intricate gain relationships with the operating frequency and loading of the system. Having a wide range of working points, both in terms of gain regulation and load value create a challenging scenario for the design.

3.2 The LLC Topology

3.2.1 Architecture structures analysis

The LLC topology employs a specific resonant network which categorizes this type of resonant power converter as a multi-resonant power converter. The resonant network can be pictured in a modified version of Fig. 3.4 as seen in Fig. 3.5. It presents a series resonant tank paired with a shunt inductance; this architecture is

referred as multi-resonant as the series resonance between L_r and C_r can happen, as well as the series resonance between $L_r + L_m$ and C_r can happen, the later one being load dependent, this aspect will be covered further in this work.

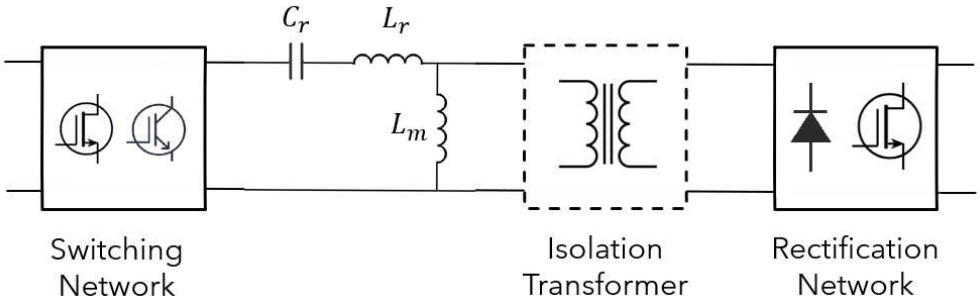


Figure 3.5: The LLC network in the general resonant power converter architecture

This specific topology is commonly used from low to high power applications, it is attractive for several factors:

- Its multi-resonant behavior creates a gain characteristic capable of achieving wide gain regulation with simple frequency modulation on the switching network, depending on the loading conditions.
- When implementing the isolation transformer, it allows to integrate the inductances from the resonant network directly into the transformer. However, this comes with a much increased complexity in the design, but with the possibility to cut on costs and improve efficiency. This aspect will be deeply analyzed in Chapter 5.
- Isolation can be achieved with the implementation of the transformer, although this work will not take advantage of this feature for achieving isolation of the system, but to be able to generate the IPOS configuration.
- The ability to achieve soft-switching, in particular Zero-Voltage-Switching (ZVS) in the switches from the switching network and Zero-Current-Switching (ZCS) in the diodes from the rectification network present the possibility for a high-efficiency conversion system.
- Reduced EMI is achieved due to the sinusoidal current waveform developed by the resonant network.

The switching network sourcing the LLC network is usually implemented as a half-bridge or full-bridge square-wave inverter. The technology of the employed

switches is decided according to the power to be processed by the system as well as the operating frequency and maximum reverse voltage to handle. A guideline from Infineon can be seen for selecting switches technology in Fig. 3.6.

Figure 3.6: Switches technology selection based on power and frequency

The architecture analyzed in this work is intended for power ranging from 50-680W and frequencies around 25-200kHz. Si MOSFETs are selected for this application for their capabilities for this application while maintaining an idea of cost reduction, as the other technologies are more expensive while not providing game-changing improvements. GaN technology offers better switching performance, but the realization of soft-switching makes this characteristic not particularly interesting, as well as considering that for the most typical power extraction scenarios, the currents through the switches is considerable, making conduction losses more important than switching losses. SiC technology is intended for applications with high reverse voltages, with the disadvantage of presenting greater conduction losses.

In terms of which square-wave inverter topology is chosen, a description on their main differences can be found in Table 3.1, where magnitudes are referred relative to the full-bridge variant. Each topology can be seen in Fig. 3.7. The half-bridge configuration outputs a square-wave with a DC offset of $\frac{V_{DC}}{2}$, in many applications this can cause problems such as core saturation of the further transformer, however, in the LLC topology this is not a problem due to the resonating capacitor also working as a DC blockage.

For this application of relatively high-power, the full-bridge configuration is chosen, primarily for the great drawback of halving the available voltage of the half-bridge configuration; having to compensate this issue with more turns in the transformer results in large losses in the copper of the winding.

The isolation transformer is of course used in this application, need for isolation in the proposed architecture has been introduced in Chapter 2, Section 2.2.1. It will also provide the ability to establish the intrinsic gain of the power converter at

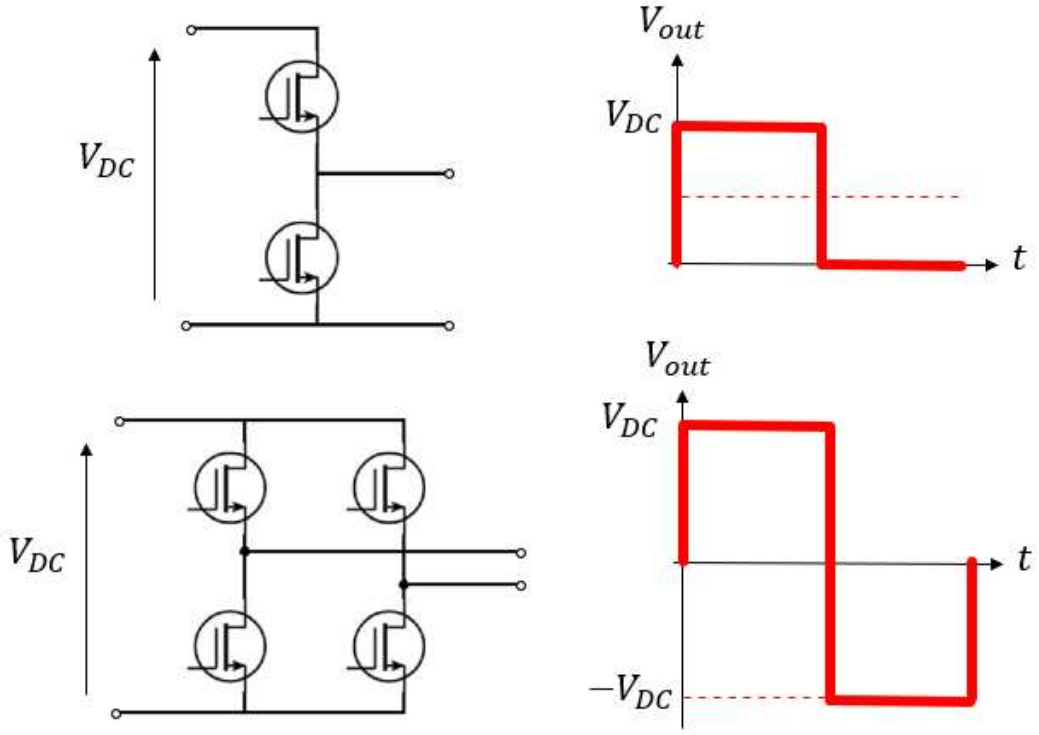


Figure 3.7: Half and full-bridge topologies

Parameter	**Full-bridge**	**Half-bridge**
Output peak voltage	x1	x0.5
Number of switches	x1	x0.5
I_{rms} through switches	x1	x2
Conduction losses	x1	x1
Switching losses	x1	x0.5
Reverse voltage	x1	x1
Number of turns needed (transformer secondary)	x1	x2

Table 3.1: Half-bridge characteristics relative to Full-bridge

resonance, an aspect crucial for achieving the intended gain profile of the system, this will be further studied in the next sections.

For the secondary side of the transformer and rectification network, several architectures have been proposed ranging from asynchronous to synchronous rectification, as well as different topologies for doubling and even quadrupling the voltage. Many architectures also implement topology morphing in the rectification circuit, allowing for multi-modes controlled often by the fixed state (ON/OFF) of semiconductor switches [21].

Asynchronous rectification was chosen for this work, trading-off slightly efficiency for reduction of cost and simplification of the control scheme. Approaches with full-wave rectification, both with center-tapped transformer (2 diodes) and full secondary winding (4 diodes) are showed in Fig. 3.8. An approach with topology morphing was also proposed to switch between normal rectification and a Voltage-Doubler-Rectifier (VDR) for aiding the wide gain regulation range, which was later discarded for increasing the cost and complexity of the system.

At the output of the rectification stage, a ripple filtering capacitor is introduced to smoothen the voltage waveform, this filtering effect also serves for the already mentioned decoupling purpose in the case of the first stage output capacitor, as the mismatch in operating frequency between stages will imply difference in the current waveforms. In this way, this "linking" capacitor acts as a buffer between the two stages.

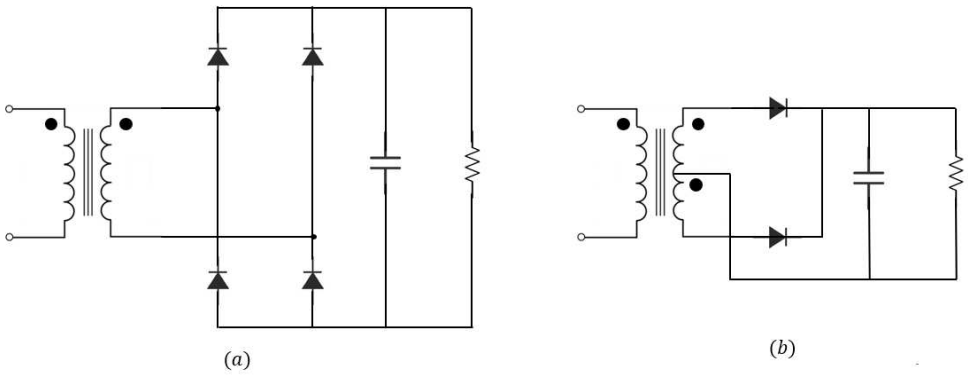


Figure 3.8: Different architectures for full-wave rectification. (a) Full secondary winding, (b) Center-tapped secondary winding

Both options with center-tapped transformer and full secondary winding transformer were employed. The criteria for the selection between both architectures can be seen in Table 3.2, where the characteristics of splitting the winding have been written relative to using the full secondary winding. When analyzing a quadratic

converter like the one proposed in this work, processing a relatively constant power (ignoring for this idea the converter losses) implies that in zones where voltage is large, current should be low, and vice-versa, due to $P = V * I$ and power being conserved. The first converter produces the first step-up in gain, the voltage being still relatively low in this section makes the current level high, making a center-tapped approach better sparing two diode losses, and although having twice the voltage stress on the diodes, the voltage is still low in this section. This concept of different stresses sections in step-up quadratic converters is illustrated in Fig. 3.9.

Parameter	**Full secondary winding**	**Center-tapped secondary winding**
I_{rms}	x1	x$\frac{1}{\sqrt{2}}$
Number of diode losses	x1	x0.5
Number of secondary turns	x1	x2
Diode reverse voltage	x1	x2

Table 3.2: Full secondary winding versus center-tapped secondary winding

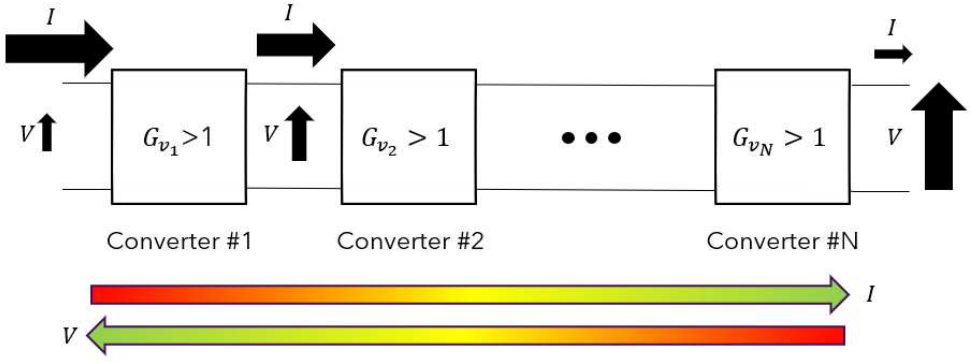


Figure 3.9: Voltage and current stress across a step-up quadratic power converter

With each block from the resonant converter with LLC network introduced, a diagram of the final circuit architecture to be studied can be presented. In Fig. 3.10, the resonant power converters are proposed in the previously described block diagram, while in Fig. 3.11, the final converter is presented in the form of the schematic, with the Pass-Through converters highlighted.

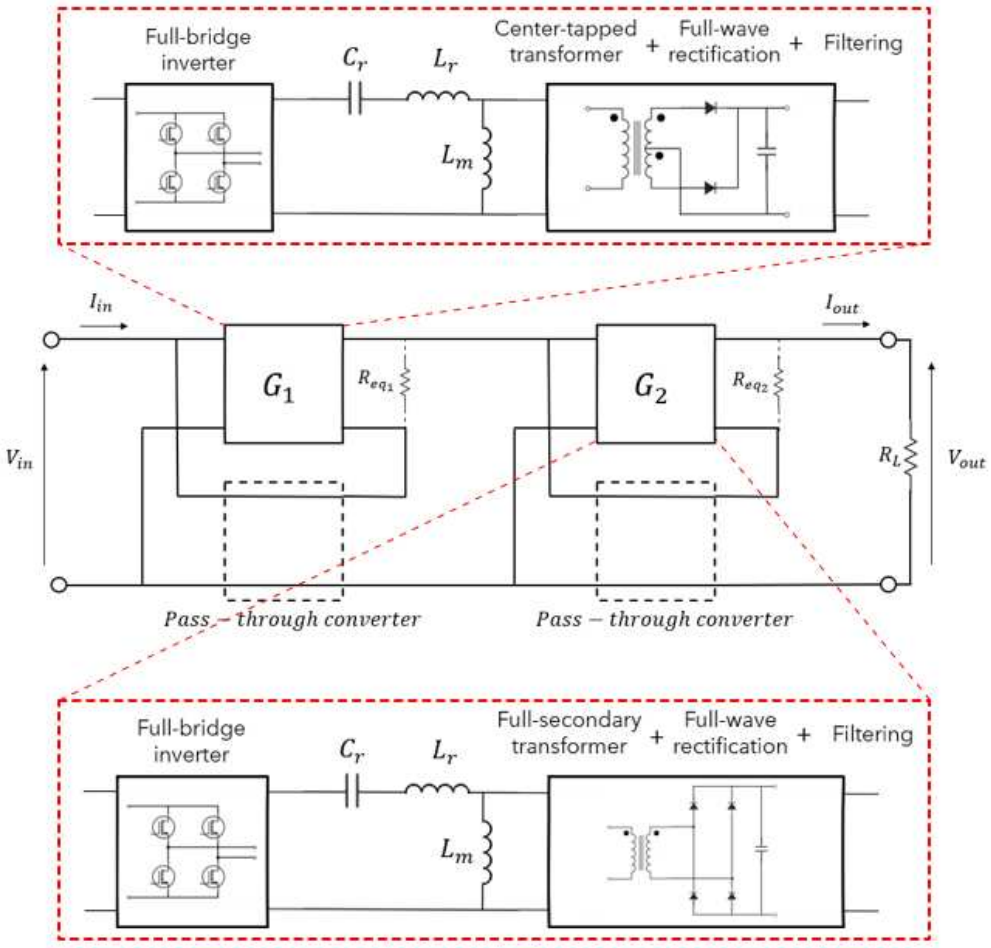


Figure 3.10: Resonant power converters in the proposed architecture

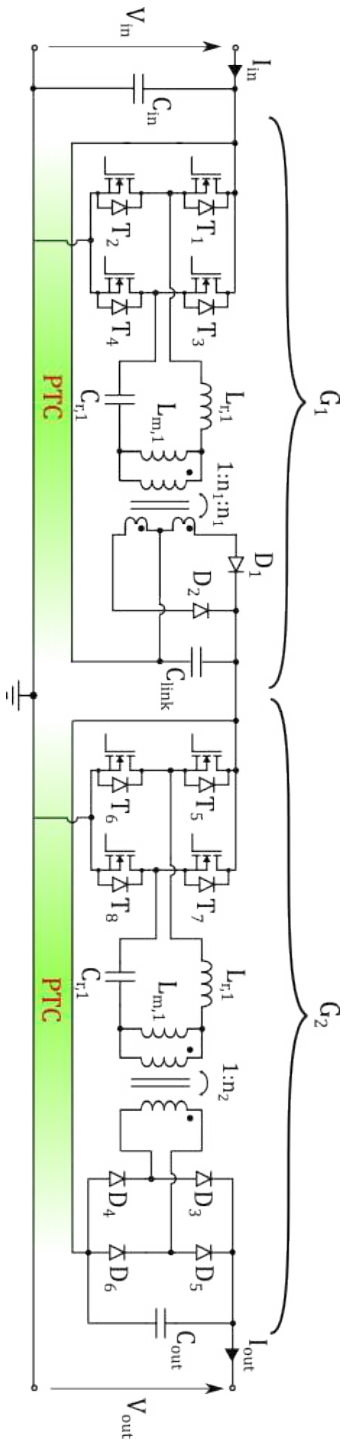


Figure 3.11: Schematic of the proposed converter. PTC: Pass-through Converter.

3.2.2 First Harmonic Approximation

As mentioned in the first section of this chapter, the introduction of a resonant network creates intricate relationships between the gain regulation capabilities and the frequency of operation and load condition. The aim of this section is to propose a model that simplifies the working principle of the LLC resonant power converter to cut difficulty in the design phase, providing a mathematical tool for evaluating the gain regulation of the system.

The First Harmonic Approximation (FHA) method is a widespread simplified model for analyzing resonant power converters based on the assumption that power transfer across the converter is essentially due to the fundamental Fourier series components of current and voltage [22]. This approach allows to find an equivalent simplified circuit for the resonant converter where linear AC analysis can be carried out in order to study gain at different frequencies and load scenarios, as well as to define necessary conditions in terms of impedance for achieving the desired soft-switching.

In order to derive the FHA model, the first step is to assume the full-bridge inverter as an ideal supply generating a square-wave voltage form with peak voltage V_{in} (DC input voltage) and frequency of operation f_{sw}, achieved by driving ON and OFF the MOSFETs alternately in pairs, with a 50% duty cycle without overlap. This voltage source will be the input to the final simplified network. This periodic square-wave with null average value can be represented in Fourier series as seen in Eq. (3.1).

$$v_{in}(t) = \frac{4V_{\text{in}}}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \sin(n\omega_{sw}t) \tag{3.1}$$

The goal of this approximation is to replace the transformer, rectification network, filtering and load with an equivalent resistor, essentially approximating a non-linear circuit with a linear one. Assuming that only the fundamental component is relevant, and considering that the series resonator is tuned to resonate at this frequency, then it is expected, at the transformer, to have applied a sinusoidal current with unknown peak value I_p. At resonance this current will not generate voltage drop in the series resonator as its impedance is null, hence the square-wave voltage waveform is applied directly to the transformer.

Analyzing the rectification and filtering, it is reasonable to assume that the capacitor is capable of filtering ideally frequencies diverse from zero, then the load R_L has a DC current flowing I_o, this DC value must be the average value of the current output of the rectifier, while the high frequency components flow through the capacitor, this is thought as a capacitor in steady state with its charge balance

law. This waveforms are illustrated in Fig. 3.12.

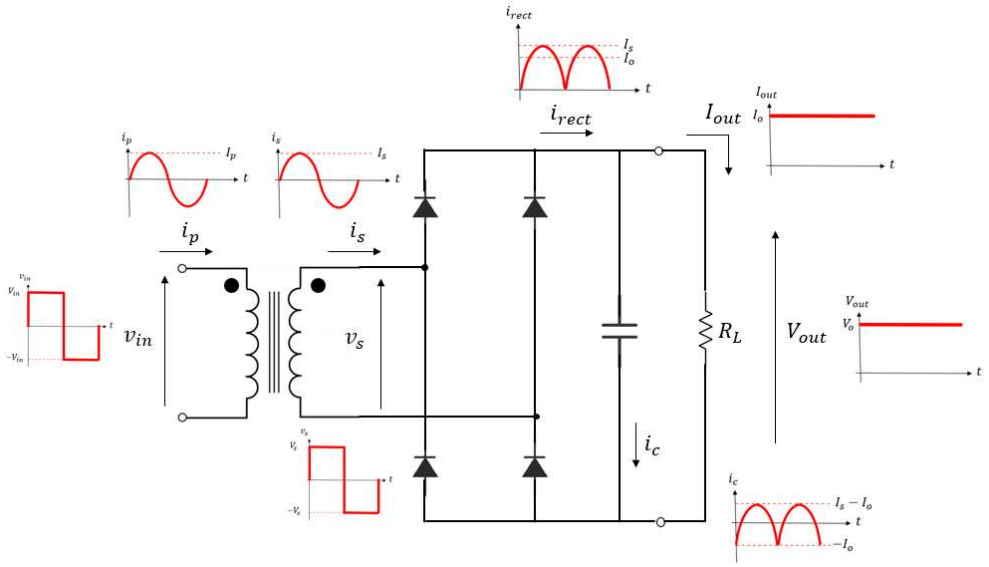


Figure 3.12: Typical waveforms of the non-linear rectification

The average value of the rectifier output current can be computed being a rectified sinusoid waveform, linking the output DC current with the peak value of the secondary current i_s, as seen in Eq. (3.2). The output voltage V_o must be the peak value of the square-wave in the secondary side (ignoring the forward voltage drop of the diodes), hence the first harmonic of the square-wave must have an amplitude according to Eq. (3.3).

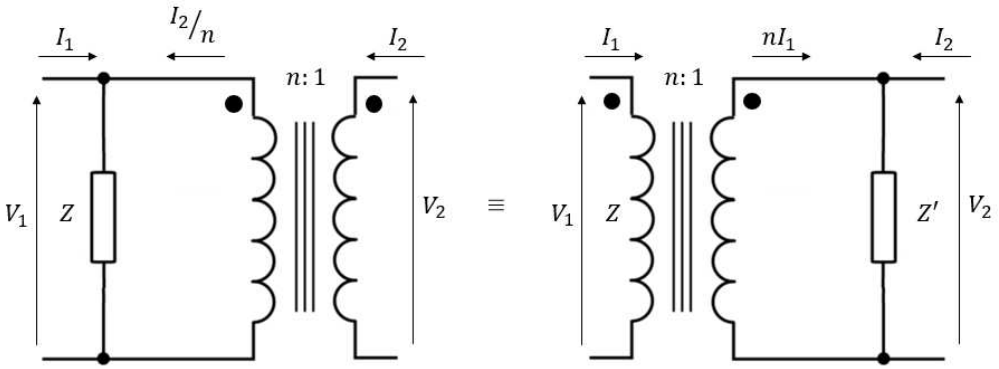
$$\begin{aligned} I_o &= \frac{1}{\pi}\int_0^{\pi} i_{rect}(\theta)\, d\theta \\ &= \frac{1}{\pi}\int_0^{\pi} I_S \sin(\theta)\, d\theta \\ &= \frac{1}{\pi} I_S \left[-\cos(\theta)\right]_0^{\pi} \\ &= \frac{2}{\pi} I_S \rightarrow \boxed{I_S = \frac{\pi}{2} I_o} \end{aligned} \tag{3.2}$$

$$V_S = \frac{4}{\pi} V_o \tag{3.3}$$

As the voltage and current in the secondary side are in phase, then an equivalent resistance value can be found considering the first harmonic that is in phase with the original square-wave, as seen in Eq. (3.4).

$$
\begin{aligned}
R_{ac_{secondary}} &= \frac{V_S}{I_S} \\
&= \frac{\frac{4}{\pi}V_o}{\frac{\pi}{2}I_o} \\
&= \boxed{\frac{8}{\pi}R_L}
\end{aligned} \tag{3.4}
$$

Finally considering that the ideal transformer has a turns ratio according to Eq. (3.5), then the final equivalent resistance can be reflected to the primary as stated in Eq. (3.6), based on the concept of impedance reflection seen in 3.13, which will be re-utilized in Chapter 5. With this process of considering only the fundamental frequency, the non-linear circuit has been replaced with a resistor, creating an equivalent linear circuit as seen in Fig. 3.14. This mechanism is also valid for the center-tapped transformer topology, the derivation steps are equal.



By exploiting transformers relations and conservation of power:

$$\left(I_1 + \frac{I_2}{n}\right)^2 Z = \left(\frac{nI_1 + I_2}{n}\right)^2 Z = (nI_1 + I_2)^2 Z' \rightarrow Z' = \frac{Z}{n^2}$$

Figure 3.13: Impedance reflection in transformers

$$n = \frac{N_P}{N_S} \tag{3.5}$$

$$R_{ac} = \frac{R_{ac_{secondary}}}{n^2} = \boxed{\frac{8n^2}{\pi}R_L} \tag{3.6}$$

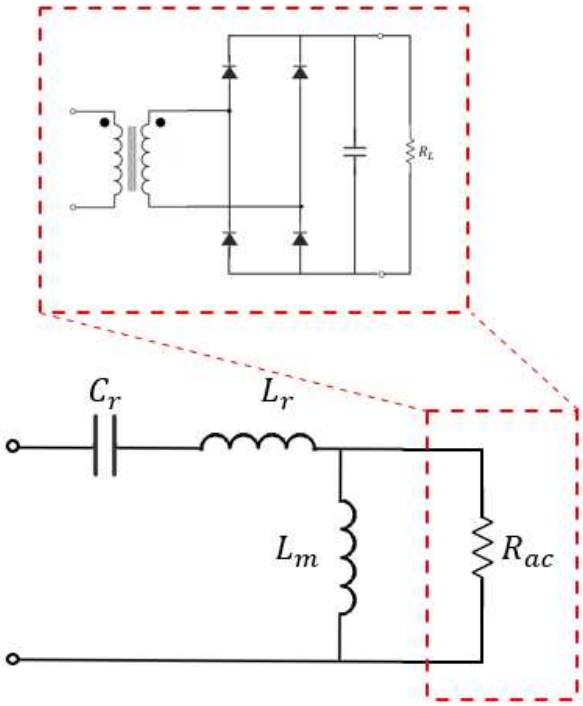


Figure 3.14: Equivalent linear circuit with FHA

With this introduced linear circuit, the gain characteristic of the system can be evaluated by the transfer function defined by the voltage across the equivalent resistance with respect to the input applied voltage, when the operating frequency f_{sw} is applied. The expression derived for this transfer function is complex and cumbersome, some figures of merit have been proposed to express the characteristics of the circuit in a more compact way, presented in Eq. (3.7). The quality factor is strictly related to the load and the resonant network values, and will place a crucial role in gain regulation, as well as m, the inductance ratio. The principal resonating frequency f_r is one of both present in the system, it is used for its property of being load independent, a key factor that will be exploited in this work. The gain characteristic is normalized in two dimensions, the gain itself is normalized to the turns ratio, as the voltage being evaluated is before the step-up of the transformer, hence a unitary value of gain corresponds to the gain of the transformer; and the frequency is normalized through F_x to the principal resonant frequency, hence a unitary value of F_x corresponds to the operating frequency being the resonant frequency f_r.

$$
\begin{aligned}
Q &= \frac{\sqrt{\frac{L_r}{C_r}}}{R_{ac}} \rightarrow Quality\ factor \\
f_r &= \frac{1}{2\pi\sqrt{L_r C_r}} \rightarrow Resonant\ frequency \\
F_x &= \frac{f_{sw}}{f_r} \rightarrow Normalized\ switching\ frequency \\
m &= \frac{L_r + L_m}{L_r} \rightarrow Inductance\ ratio
\end{aligned} \tag{3.7}
$$

The description of the gain characteristic, the modulus of the transfer function proposed, can be seen in Eq. (3.8). The steps to reduce the expression to its final form require a long derivation process through algebraic operations, the complete overview of this process can be found in the Appendix B for the reader interested in this often skipped step in the literature.

$$
\begin{aligned}
\left|\frac{v_{o_{ac}}(j\omega)}{v_{in}(j\omega)}\right| @\omega_{sw} &= \left|\frac{\frac{R_{ac}j\omega_{sw}L_m}{R_{ac}+j\omega_{sw}L_m}}{\frac{R_{ac}j\omega_{sw}L_m}{R_{ac}+j\omega_{sw}L_m} + j\omega_{sw}L_r + \frac{1}{j\omega_{sw}C_r}}\right| \\
&= \boxed{\frac{F_x^2(m-1)}{\sqrt{Q^2F_x^2(m-1)^2(1-F_x^2)^2 + (F_x^2 m - 1)^2}}}
\end{aligned} \tag{3.8}
$$

This mathematical abstraction from the initial circuit is still complex after the rough simplification of the FHA, but it provides powerful insight on the effects of the resonant network values paired with the load when analyzing if gain regulation is possible. With this proposed expression, some global behaviors can start to be introduced which will be critical in the design phase of this work. The quality factor Q is the most impactful parameter in terms of gain characteristic effect. In Fig. 3.15, the effect on Q variation is pictured for a value of $m = 10$, it is worth noting that Q depends on L_r and C_r, which are constant, but also on R_{ac}, which dynamically changes in time in normal operation. This creates a dynamic gain profile behavior for the converter which has to be accounted for being able to provide the necessary gain at each working point.

Another important characteristic that can be observed from the FHA derived behavior is in terms of impedance. The full-bridge inverter is presented with an input impedance from the circuit of value $Z_{in}(f)$, defined in Eq. (3.9) with a certain phase angle, defining a global capacitive or inductive behavior. It can be demonstrated that the maximum gain point of the gain characteristic correspondent

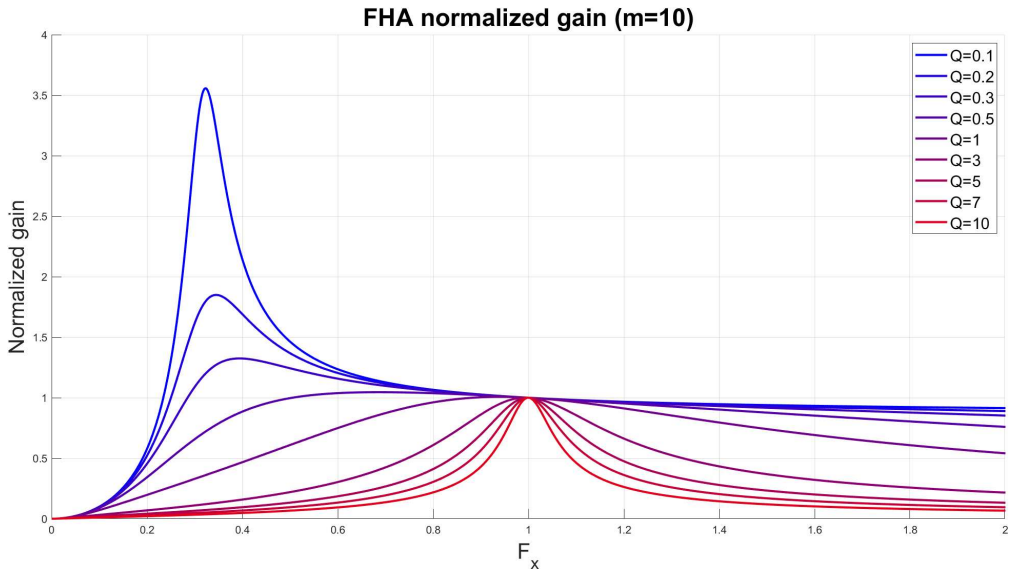


Figure 3.15: FHA gain characteristic for different Q values

to the resonance of C_r with $L_r + L_m$ (load dependent) marks the division between a capacitive region and an inductive region. This can be seen graphically by showcasing the gain characteristic with the impedance phase, as seen in Fig. 3.16. The importance of working only in the inductive region (positive impedance phase) will be further analyzed in Section 3.2.5 where soft switching capabilities of the LLC topology are discussed.

The study of the gain characteristic of the LLC resonant power converter is complex, but by working with the FHA and with the ability to automatize processing through computer aid, the design workflow can be simplified.

$$Z_{in}(f) = j(2\pi f)L_r + \frac{1}{j(2\pi f)C_r} + \frac{R_{ac}j(2\pi f)L_m}{R_{ac}j(2\pi f) + L_m} \tag{3.9}$$

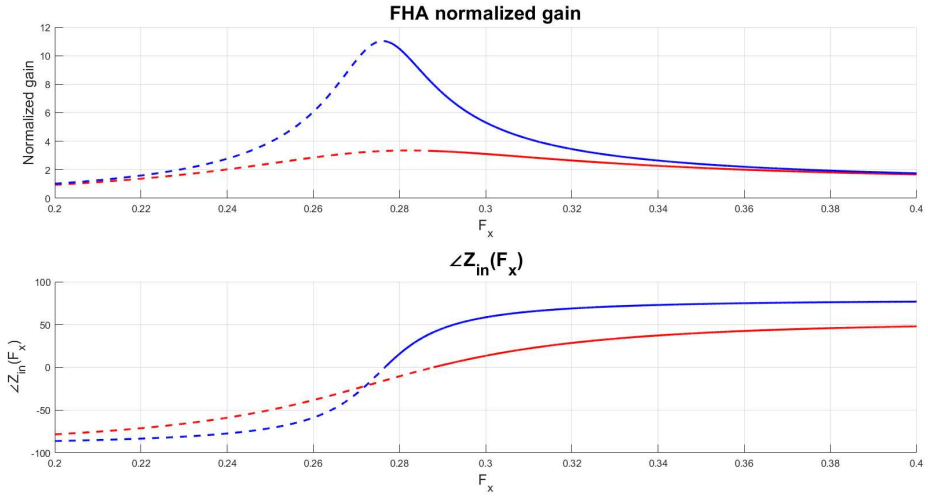


Figure 3.16: FHA gain and its relationship with impedance phase

3.2.3 Loading limitations of the LLC topology

In the previous section, the gain characteristic of the LLC resonant power converter was presented, and the relationship with the load has been established through the quality factor Q.

Each working point is composed of an input voltage value and a resistance value representing the amount of power extracted from the energy source. For a certain input voltage value there is a range of possible resistance values, which implies that each stage must maintain the same gain value for different Q values. This requires controlling the frequency of the generated square-wave by the inverter depending on the load and input voltage, but most importantly, the particular gain value that is needed must be possible to maintain through this resistance range. In this sense, the design will have a focus on complying with the worst case scenario in the entire loading range.

In terms of the LLC power resonant converter behavior upon load changes, three regions are identified depending on the operating switching frequency:

- $f_{sw} < f_r \equiv F_x < 1 \rightarrow$ When the converter operates in the inductive region in this case, hence the peak gain is to the left of $F_x = 1$, then the converter is able to increase the gain with respect to the turns ratio gain, from now on called intrinsic or resonant gain. In this region, a heavier load, or a lower resistance value, will restrain the maximum achievable gain.

- $f_{sw} = f_r \equiv F_x = 1 \rightarrow$ When the converter operates at the resonant frequency f_r all parametric curves of Q converge to the unitary gain. This property of the LLC topology is extremely important in terms of gain regulation as it offers an operating frequency in which the gain is load independent.

- $f_{sw} > f_r \equiv F_x > 1 \rightarrow$ In this region, the converter always works in the inductive region. Here, the converter is able to decrease the gain from the resonant gain value. In this region, a lighter load, or a higher resistance value, will restrain the minimum achievable gain.

These regions can be observed in Fig. 3.17. The exploitation of these regions with their minimum/maximum achievable gain constraints will define the criteria for profiling the gain for each one of the power converters proposed in this work.

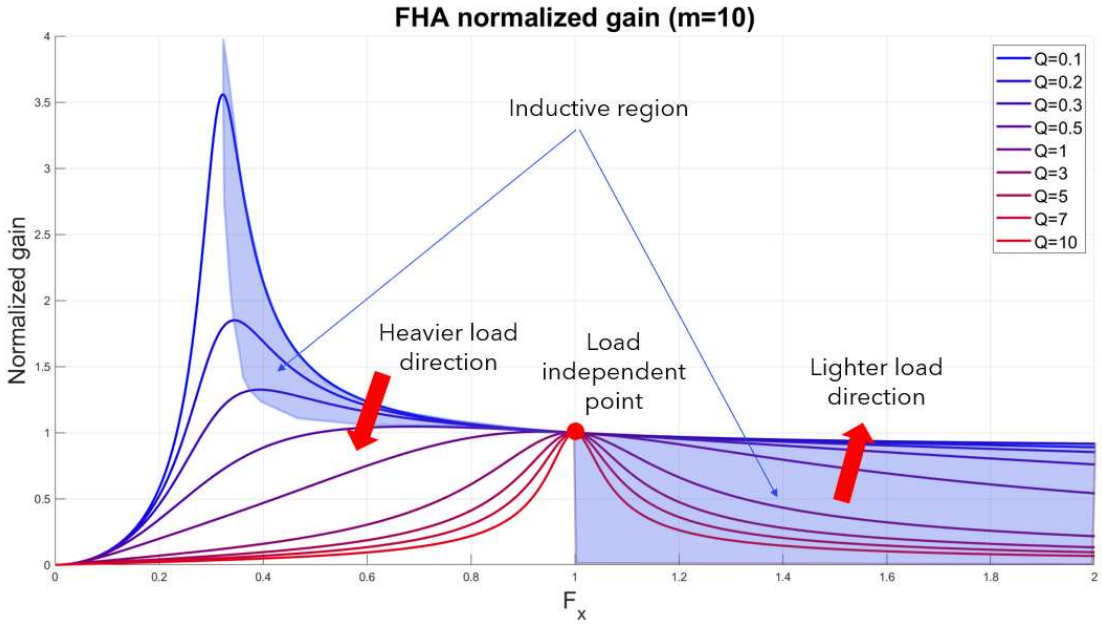


Figure 3.17: LLC topology operating regions

Extreme cases of loading are a possible threat to gain regulation, extreme heavy load scenarios are not possible due to the photovoltaic panel limitations, in fact the heaviest load scenario is the maximum power extraction case of around 680W and could be considered as the "extreme" heavy load case. However, extreme light load conditions are possible when the grid is not draining any power from the system, then the photovoltaic panel output voltage is the open-circuit voltage while the resonant power converters lose the ability to decrease the gain for not overshooting the 350V output. Resonant power converters have trouble with gain regulation in

this extreme light load condition, in fact, it can be seen as an extreme case in the gain relationship when $Q = 0$ at Eq. (3.10), rising the frequency to high values would only allow to lower the normalized gain to around the value seen at Eq. (3.11). However, the FHA has its limitations and does not work correctly when the frequency is much higher than f_r, in fact, going up in frequency may cause the gain to rise again due to harmonics effects [19]. The solution in this case is to exploit the full-bridge inverter architecture. Having a full-bridge inverter implies that one leg of it can be statically controlled to produce a half-bridge connection, as seen in Fig. 3.18, effectively cutting in half the stage gain. In this way, the stages can be forced to the need of gain increasing, which is not a problem at light load scenarios, this scenario will be referred as the "half-bridge mode".

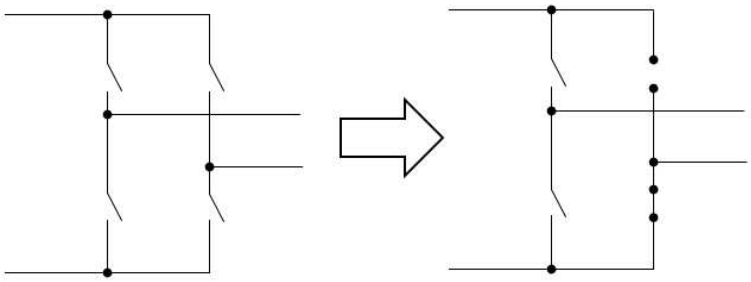


Figure 3.18: Full-bridge inverter morphing into Half-bridge inverter

$$K(0, m, F_x) = \frac{F_x^2(m-1)}{\sqrt{0^2 F_x^2 (m-1)^2 (1-F_x^2)^2 + (F_x^2 m - 1)^2}} = \frac{F_x^2(m-1)}{F_x^2 m - 1} \tag{3.10}$$

$$\lim_{F_x \to \infty} K(0, m, F_x) = \frac{m-1}{m} \tag{3.11}$$

3.2.4 Gain profiling: system gain and its effect on loading

The impact of the DC gain value in morphing the load characteristic of each stage has been presented in Chapter 2, Section 2.2.3. Many DC-DC converter topologies present a tight relationship between the load value and the gain regulation ability, in this case the link is established by the figure of merit Q. In this context, it is useful to have the tools to model the load variation at different working points according to a certain gain profile imposed to each stage. In this way, a workflow for the design and verification can be created in which the gain profiles are presented, defining the stages loading profiles, which feasibility for achieving the gain profile

can be evaluated. This iterative process seen in Fig. 3.19, aided by developed tools to sweep every possible working point, allows for the design of this complex quadratic IPOS configuration architecture and will be further expanded in the following chapters. The proposed technique is not limited to this application, but is a novel workflow that can be adapted to the design of power converters with wide range of working points and high load dependency.

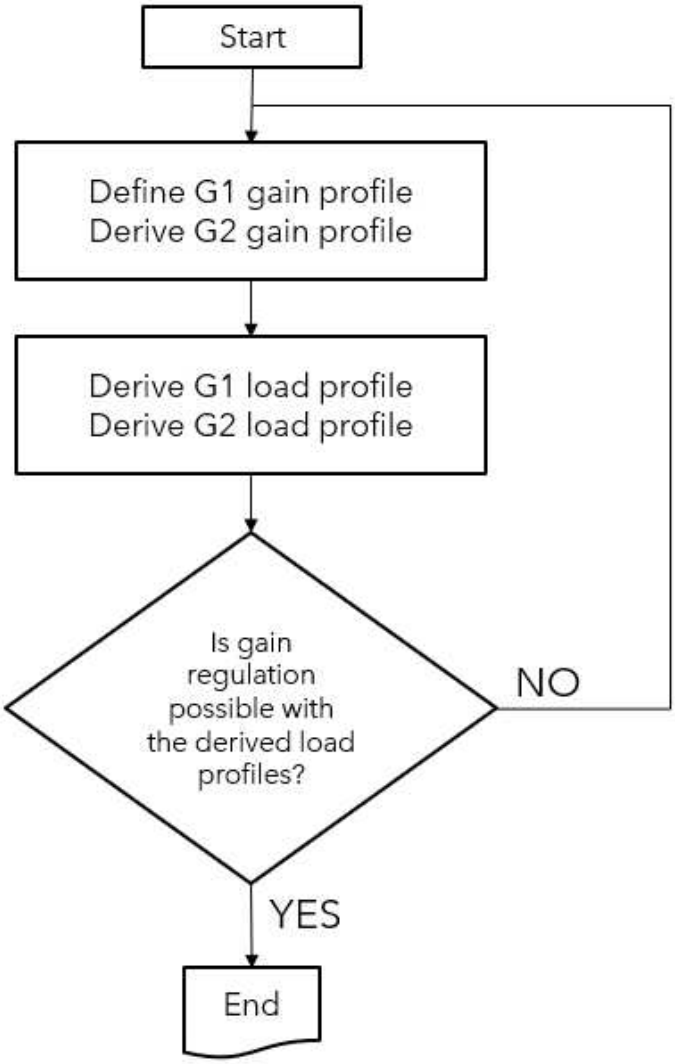


Figure 3.19: Gain and load profiling design flow

The total system gain profile is fixed and follows the expression related to maintaining constant 350 V at the output, mathematically described in Eq. (3.12) and illustrated in Fig. 3.20. From the expression presented of the quadratic converter in Eq. (2.8) it can be seen how there is essentially only one degree of

freedom for every working point; at every possible input voltage value, if the gain value of one stage is forced, then the other stage must provide a constrained gain such that the overall system gain is the necessary to output 350 V.

$$G_{total}(V_{in}) = \frac{350V}{V_{in}} \forall\, V_{in} \in [15{,}43]V \tag{3.12}$$

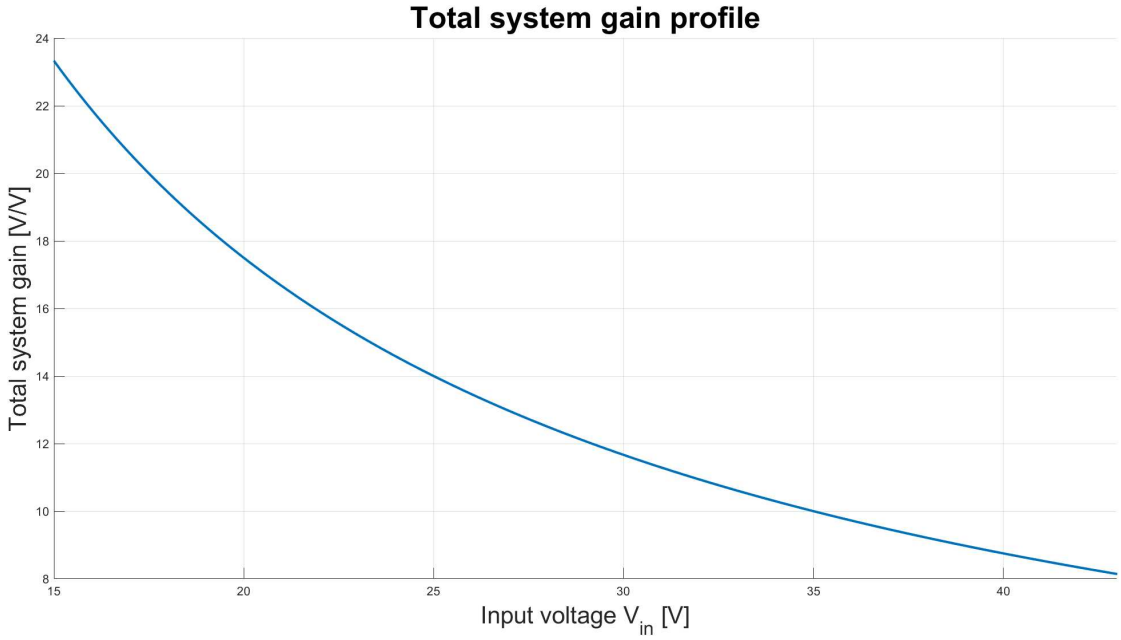


Figure 3.20: Total system gain profile

Defining the load profile for each stage is complex, as for each voltage point, the load value can change depending of the value of the solar irradiance. This can be observed in a vertical movement in the P-V curves, a picture of the highlighted operating area (50-680 W, 15-43 V) and the maximum and minimum loading scenarios is presented in Fig. 3.21. In Fig. 3.22 the load characteristic is shown, considering the resistance as the equivalent value to dissipate all the power the photovoltaic panel can provide at each point. The circles of minimum resistance represent maximum load, which represent the maximum power points.

The maximum load at any given voltage coincides with the P-V curve of maximum solar irradiance of $1000\frac{W}{m^2}$ while the minimum load corresponds to a horizontal line of 2450Ω resistance value, representing the minimum 50 W extracted power at any given voltage point, for different solar irradiance values.

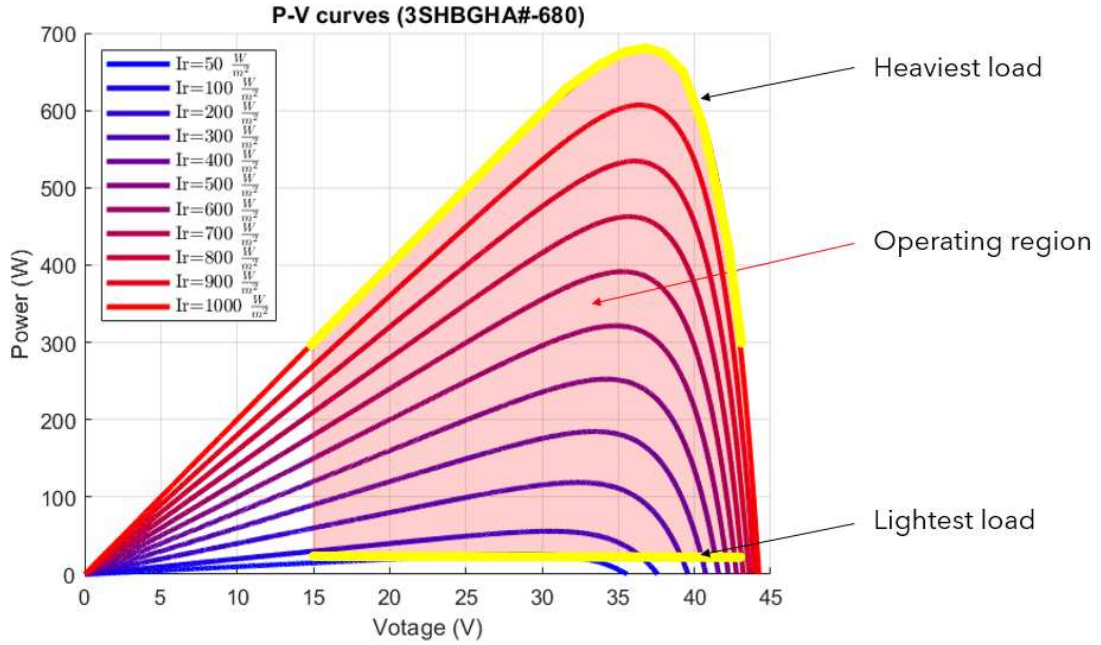


Figure 3.21: Working points of the system

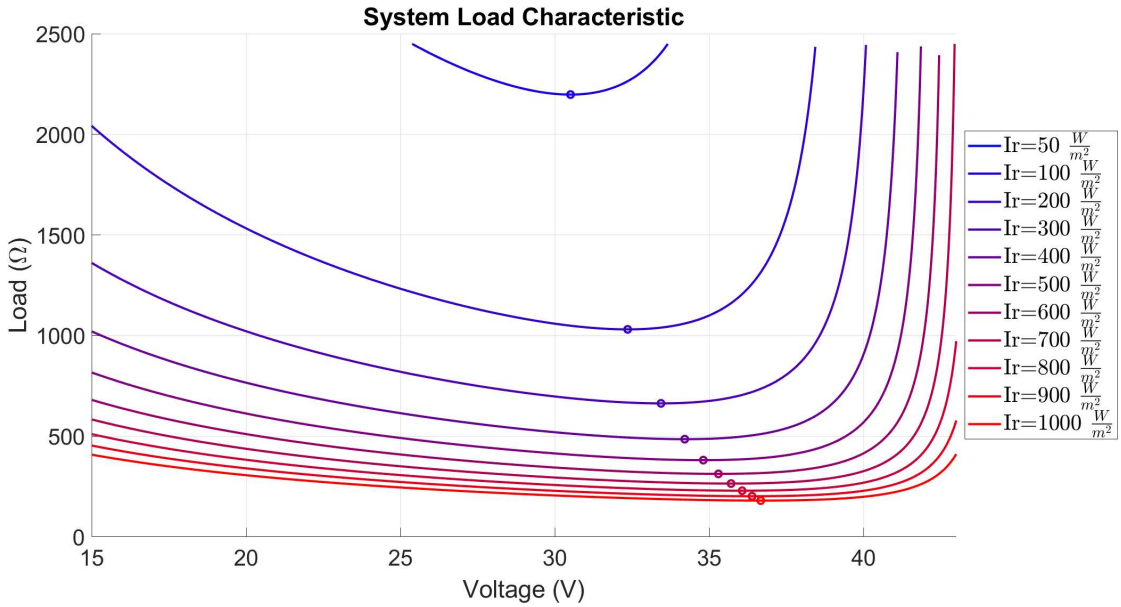


Figure 3.22: System load characteristic

3.2.5 Zero Voltage Switching (ZVS) in the LLC topology

Soft switching is one of the main advantages of resonant power converters. Achieving this feature requires specific conditions to be met, and it is typically difficult to maintain this property across the wide range of operating points. In the context of this work, necessary conditions will be imposed to ensure Zero Voltage Switching (ZVS) of the full-bridge inverter switches in the vicinity of the resonant frequency f_r, where the system will be expected to operate under the most likely scenarios.

In particular, for the LLC topology, the target transition for achieving ZVS is the turn-on of the switch. During the turn-off transition, hard switching occurs, but it has a lower impact than in other non-resonant topologies due to the natural sinusoidal tendency of the current approaching zero at the turn-off moment when operating close to resonance. ZVS at turn-on is effectively achieved by exploiting the dead time and the inductive nature of the impedance experienced by the inverter to discharge the parasitic capacitance of the switch, particularly the C_{oss} capacitance.

The physical structure of MOSFET transistors creates a variety of parasitic capacitances due to the capacitor-like behavior that appears between different substrates and regions of the component [23], as shown in Fig. 3.23. These capacitances play an important role in the dynamic behavior and analysis of the switching network, which must be considered when driving the switches and implementing soft switching schemes. Manufacturers often describe these parasitic capacitances in the datasheet as equivalent capacitors tested under specific conditions: C_{iss} for the input capacitance, C_{oss} for the output capacitance, and C_{rss} for the reverse transfer capacitance, formed from the measurement from different ports with the rest of the ports short-circuited, as seen in Fig. 3.24.

In this context, the interest is on the output capacitance C_{oss}, as its voltage defines the voltage V_{DS} of the transistor, responsible of the switching losses. During the OFF state of the transistor, the output capacitance is charged up to the input voltage; the principle of ZVS is performed by discharging the capacitor as close as possible to zero volts in the dead time introduced in the inverter to avoid a potential short-circuit hazard due to the dynamics of turn-on and turn-off of switches in the same leg of the full-bridge inverter. In order to analyze and describe the conditions to force this situation, knowledge on the value of the output capacitance is needed, which is not easy given the high non-linear relationship of the capacitance with the voltage V_{DS} applied. Manufacturers offer the characteristic of C_{oss} versus voltage V_{DS} measured in a static scenario, but since the switch operates dynamically, the description of static capacitance is not enough. At turn-off, the capacitance C_{oss} is charged to V_{in}; in this transient, the capacitance value changes dynamically due to its dependence on the voltage applied. Charging the capacitor in this dynamic

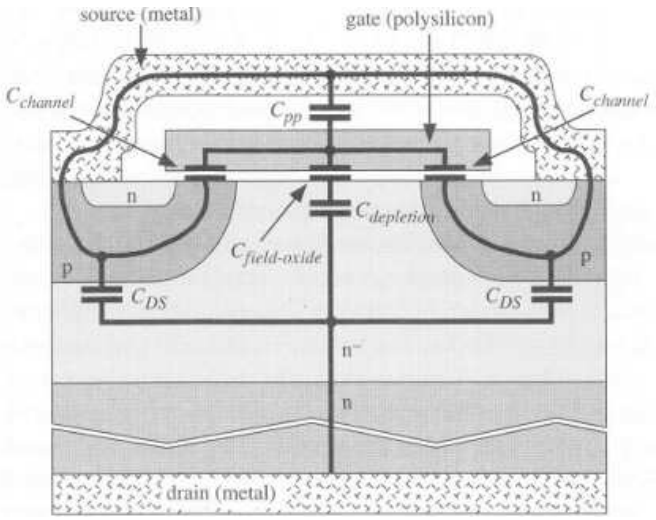


Figure 3.23: MOSFET construction and the formed parasitic capacitances

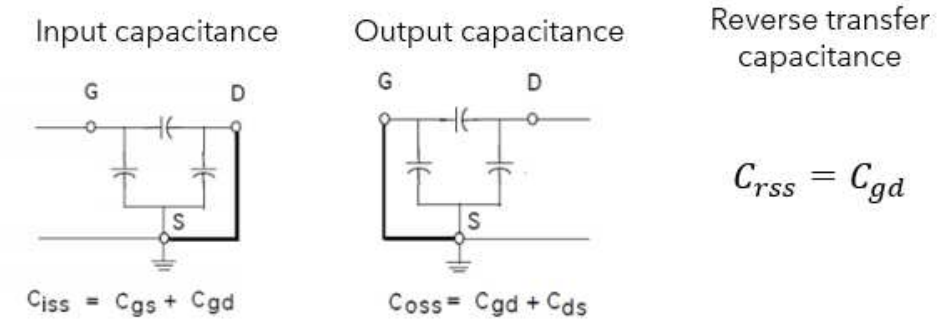


Figure 3.24: Characterized capacitances of the MOSFET transistor

way stores an equivalent charge as seen in Eq. (3.13). This creates an equivalent capacitance value $C_{eq}(V_{DS})$ in Eq. (3.14) that can be used to analyze the dynamics of switching.

$$Q_{eq} = \int_0^{V_{DS}} C_{oss}(V_{DS})\, dV_{DS} \tag{3.13}$$

$$C_{eq} = \frac{1}{V_{DS}} \int_0^{V_{DS}} C_{oss}(V_{DS})\, dV_{DS} \tag{3.14}$$

In this way, by finding a function $C_{oss}(V_{DS})$ with the static definition from the manufacturer and a tool for curve fitting, an equivalent model for the output capacitance of the transistor can be found for dynamic analysis. In Figs. 3.25 and 3.26 this workflow can be observed for a commercial MOSFET transistor from STMicroelectronics, the equivalent output capacitance found in this way is larger than the static output capacitance presented by the manufacturer and more realistic for a dynamic application.

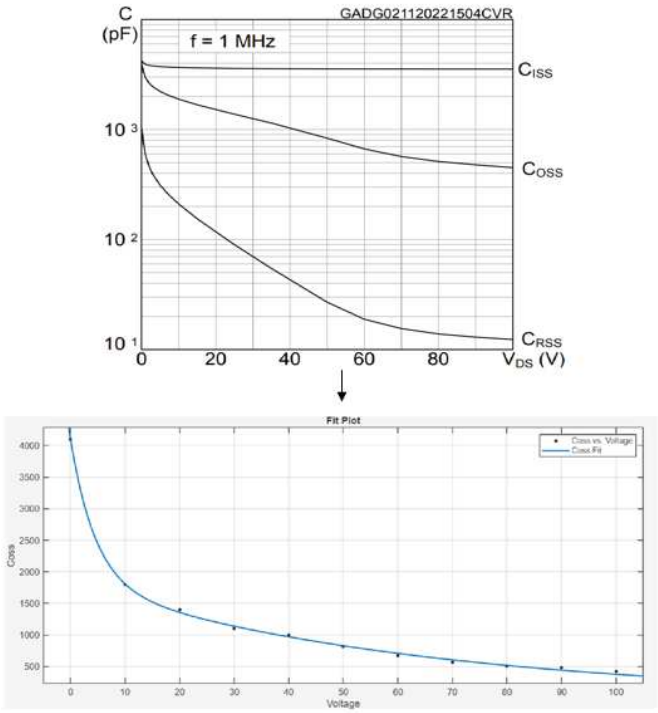


Figure 3.25: Curve fit of the manufacturer C_{oss} characteristic

With the knowledge of the input voltage to a stage, the equivalent output capacitance of a MOSFET transistor can be estimated, and the next step in generating the necessary condition for ZVS can be analyzed. To discharge this capacitance during the dead time, the inductive behavior of the resonant network provides the energy required for this transient. Specifically, the inductor L_m holds the necessary energy to force a current during the dead time, which discharges the stored charge. The inductor L_m experiences the square-wave output of the inverter at resonance, and by considering the relationship between current and voltage across an inductor in Eq. (3.15), the current can be derived through integration. In steady-state operation, the Voltage-Second Balance Law holds, as energy conservation dictates that the energy stored in the magnetic field at the start and end of the cycle must remain constant. This means that the average

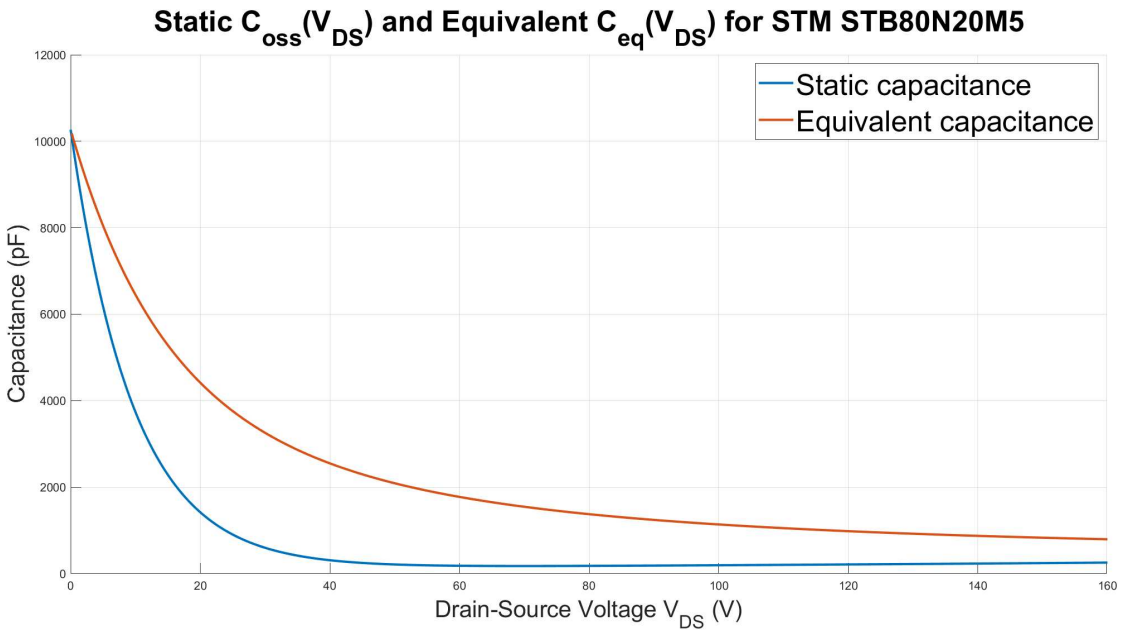


Figure 3.26: Equivalent dynamic capacitance versus static capacitance

value of the triangular waveform must be zero due to its symmetry. The waveform for $i_{L_m}(t)$ can be seen in Fig. 3.27.

$$v_L(t) = L\frac{di_L(t)}{dt} \Rightarrow i_L(t) = \frac{1}{L}\int v_L(t)\,dt \tag{3.15}$$

At each transition of the switches, the current i_{L_m} reaches its maximum value, as highlighted in Eq. (3.16), derived by knowing the average value of the waveform is null. If the dead time is small relative to the entire period, the value of current can be approximated as maintained through the dead time, meaning that the charge pulled from L_m is equivalent to the dead time multiplied by this maximum current value. The necessary condition for ZVS at turn-on is then established as the charge available from L_m being greater or equal than the charge that needs to be moved from the two MOSFETs that are about to be turned on. This relationship is built in Eq. (3.17).

$$i_{L_{m\,max}} = \frac{\Delta I}{2} = \frac{V_{in}}{4L_m f_{sw}} \tag{3.16}$$

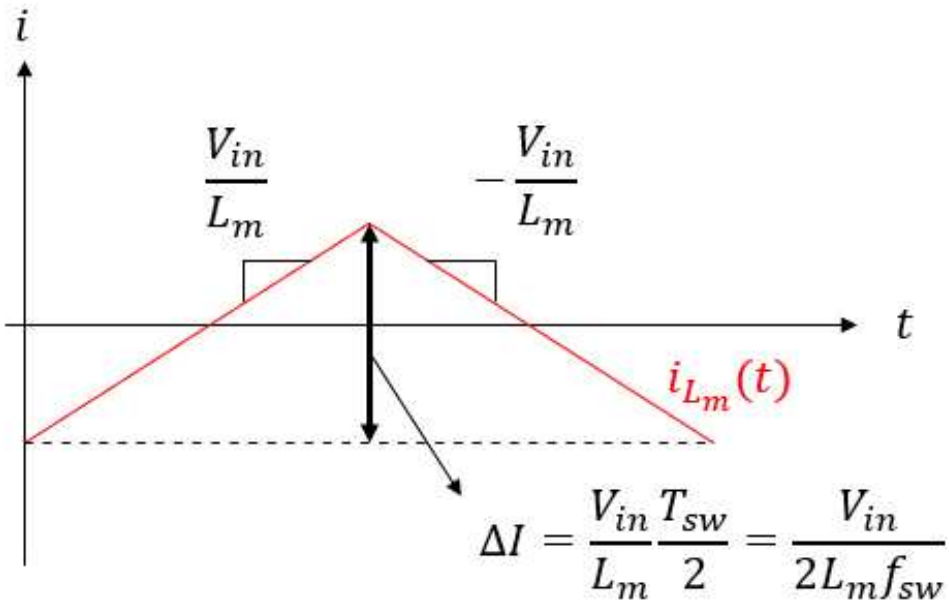


Figure 3.27: Current waveform through L_m at resonance

$$\begin{aligned} i_{L_{m\,max}} t_{dead} &\geq 2Q_{MOS} \\ \frac{V_{in}}{4L_m f_{sw}} t_{dead} &\geq 2C_{eq}(V_{in})V_{in} \\ L_m &\leq \frac{t_{dead}}{8f_{sw}C_{eq}(V_{in})} \end{aligned} \tag{3.17}$$

This established necessary condition helps define the value of L_m in order to achieve ZVS at the turn-on of the switches of the full-bridge inverters. This ZVS behavior can be seen in Fig. 3.28 extracted from a simulation in *LTSpice*, where gate driving voltages of one leg of the inverter are observed, with V_{DS} dropping to zero in the dead time to achieve the ZVS at turn-on.

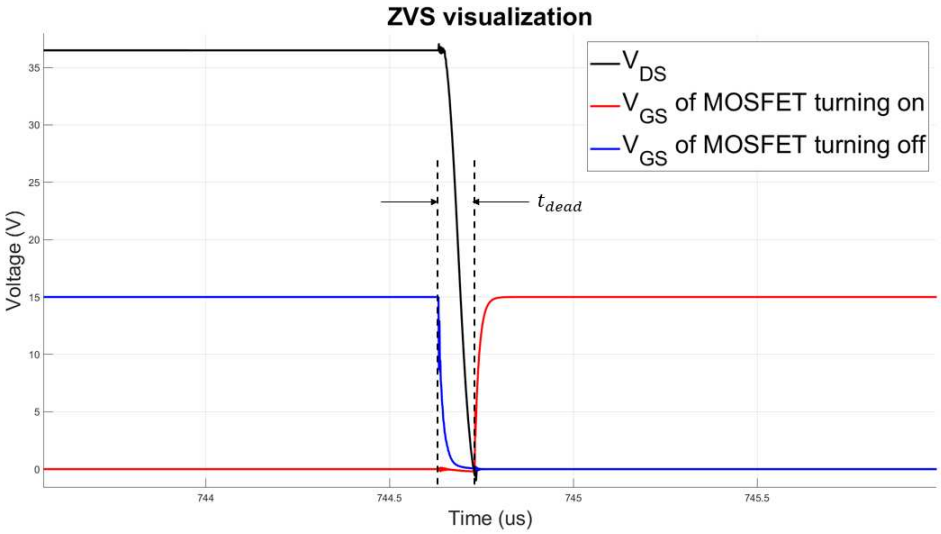


Figure 3.28: ZVS visualization

Chapter 4

Power converter Design and Optimization

4.1 Developed Design Tools

4.1.1 Gain and load profiling tool

The LLC topology resonant power converter is widely used in state of the art DC-DC power converters. Despite its broad range of applications and popularity, the complexity of the architecture and its flexibility to many applications has driven the development of multiple non-unified design methodologies found in the literature. In this context of large diversity of design methods, this work aims to present a new methodology based on gain and loading profiling, due to the inherent complexity in this matter given the quadratic IPOS configuration architecture. The developed methodology can be further transformed to work in the context of wide input range, wide output power range fixed voltage output step-up applications, for other proposed architectures.

The developed tool follows the method proposed in Chapter 3, Section 3.2.4. Gain profiles for both stages must be proposed with some criteria, these gain profiles will morph the overall system loading characteristic at the output of each stage based on the equivalent resistance analysis done in Chapter 2, Section 2.2.3. Finally, the morphed loading profiles will determine limit maximum and minimum values for the quality factor Q, which eventually limits the maximum and minimum gain values achievable by a certain stage. At this point, the gain regulations capabilities must be contrasted with the desired gain regulation capabilities for each stage at every input voltage value, to further continue the iteration with new proposed gain

profiles or to keep them and continue the design.

In addition to the degree of freedom of the definition of the gain profile, the resonant tank components L_r, C_r and L_m further defining Q and m are also available to adjust depending on gain and load. Further commentaries on this values will be addressed in the optimization part of the design process.

This proposed iterative process implements a "brute-force" approach, in the sense that the entire input voltage range is swept for different power levels, finding the morphed loading profile of each stage. With the loading profiles, the limit cases can be stated, allowing to define for each working point, through the FHA gain characteristic the minimum and maximum possible gain values. The algorithm is implemented in *MATLAB*, and can be found in the Appendix A.2, divided into 3 sections, the first one plotting the user defined gain profiles for verification, the second one calculating the equivalent stage resistances according to the found relations with the gain profile, further plotting it for visualization, and the third one calculating the gain capability in terms of maximum and minimum gain in parametric curves of the m factor. The workflow of the process taken by the algorithm is summarized in Fig. 4.1.

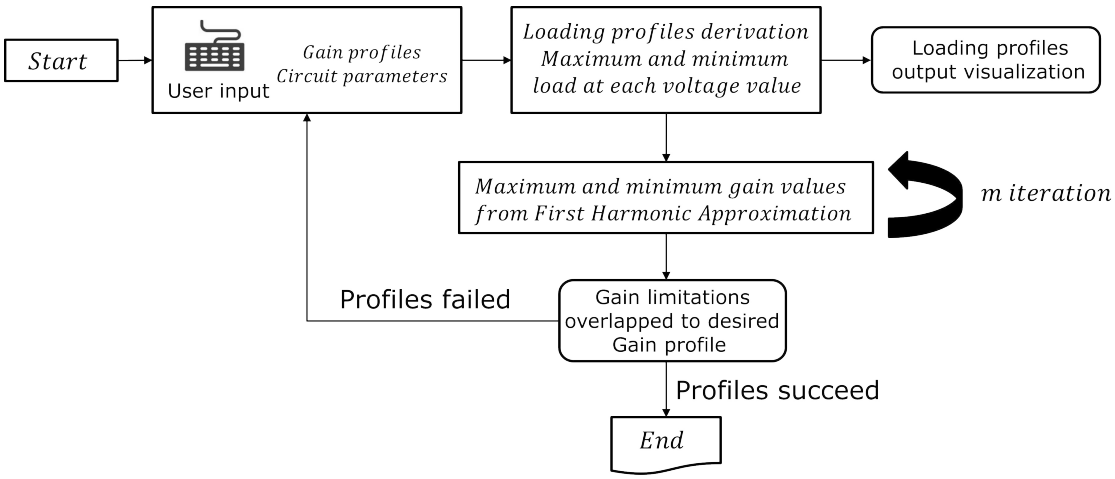


Figure 4.1: Gain and load profiling tool utilization

An example is provided to better understand the workflow and to observe the effects on load of this type of partial power processing architectures. This example consists on imposing a gain profile in which $G_1 = G_2$, this creates the relationship seen in Eq. (4.1). The proposed gain profiles can be seen in Fig. 4.2, where they are superimposed being exactly equal. These gain profiles define a loading profile for each stage, which can be seen for different values of solar irradiance in Figs. 4.3 and 4.4. It is interesting to compare these loading profiles to the total system loading

profile, as it can be seen in Figs. 4.5 and 4.6, the resistance values for the first stage are much strongly reduced in contrast with the second stage. Finally, with the loading profiles, the gain capability profiles are sketched, while superimposing the initial desired gain profile (normalized to the transformer turns ratio), as observed in Figs. 4.7 and 4.8. It can be seen that, for the proposed gain profiles, the stages struggle to regulate the gain, either because they cannot increase the gain enough, or either decrease it. The developed tool helps visualize the scenarios for multiple gain profiles, giving hints in how the system behaves at various working points, aiding the design of the system. It is worth noting with this example how the considerable load reduction for the first stage limits abruptly the ability to boost of this power converter, a factor that will be taken into consideration for defining the final gain profiles. In this example, it is clear from the figures that the scheme is not possible, the gain profiles must be discarded and introduce different ones according to the iterative design flow.

$$G_{tot} = (G_1 + 1)(G_2 + 1) = (G + 1)^2 \; when \; G = G_1 = G_2 \tag{4.1}$$
$$G = \sqrt{G_{tot}} - 1$$

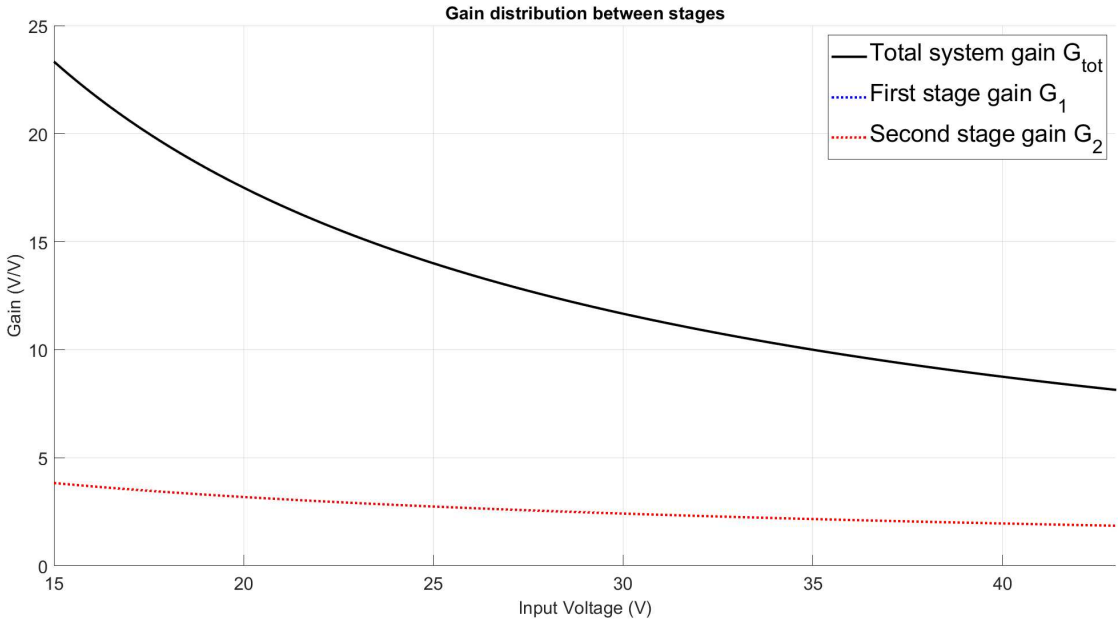


Figure 4.2: System and stages gain profiles (example)

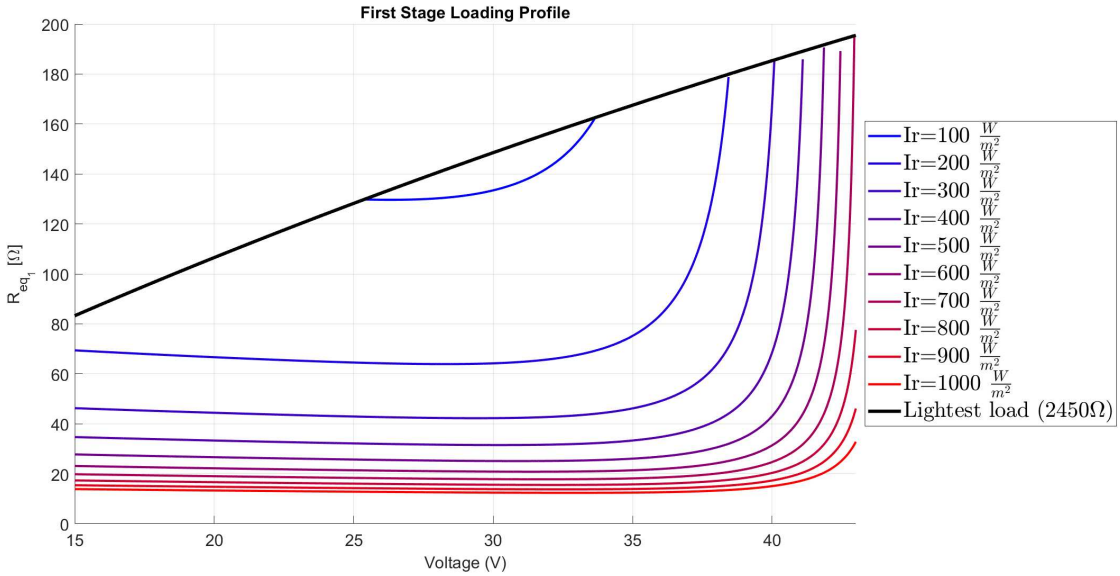


Figure 4.3: First stage loading profile (example)

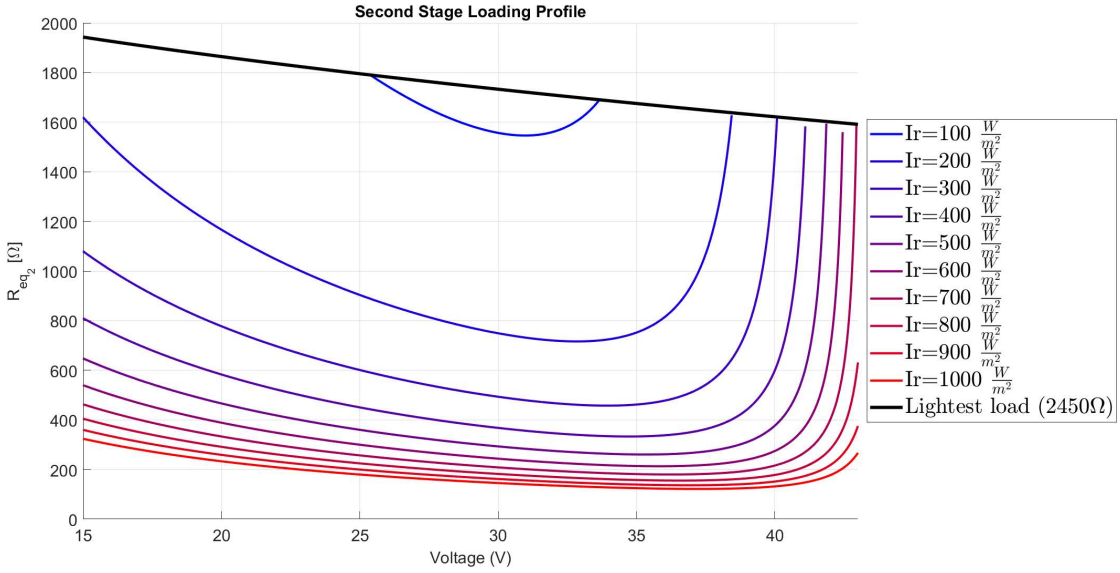


Figure 4.4: Second stage loading profile (example)

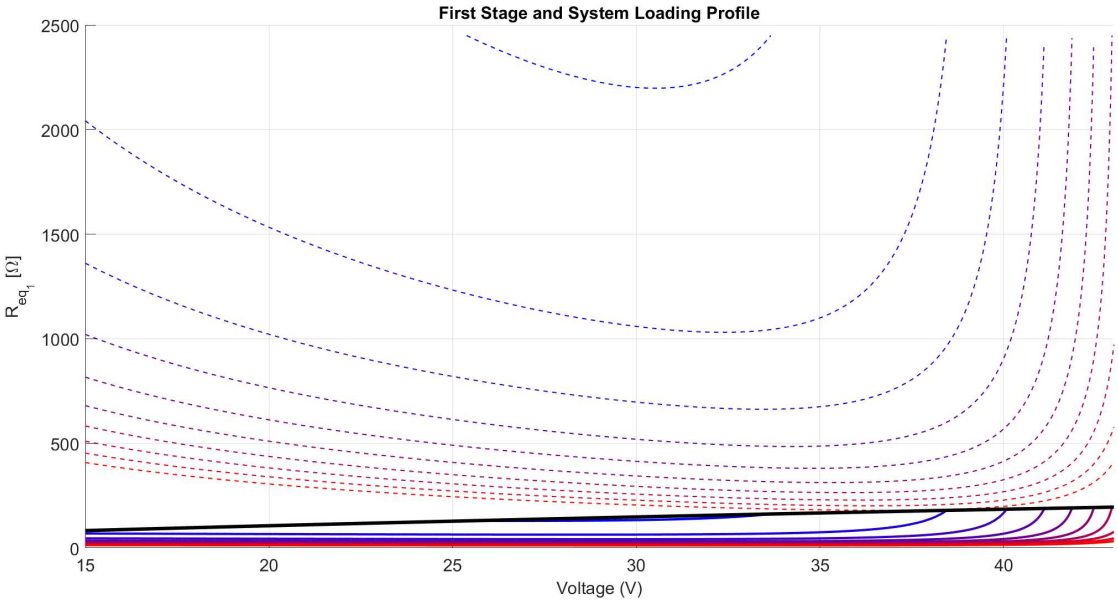


Figure 4.5: First stage (solid lines) and system loading profile contrast (dotted lines)(example)

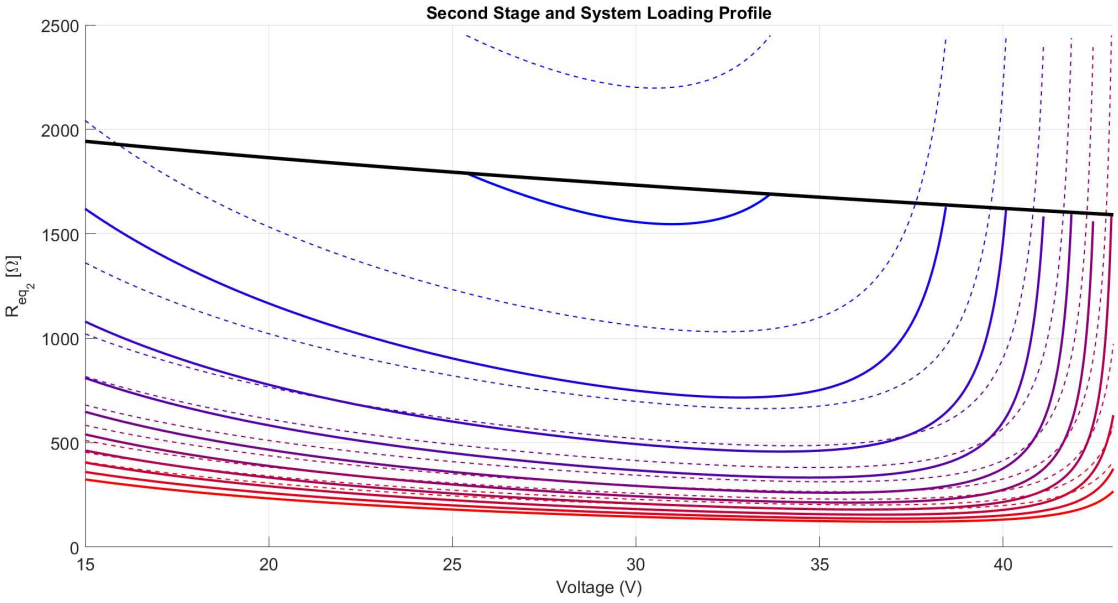


Figure 4.6: Second stage (solid lines) and system loading profile contrast (dotted lines)(example)

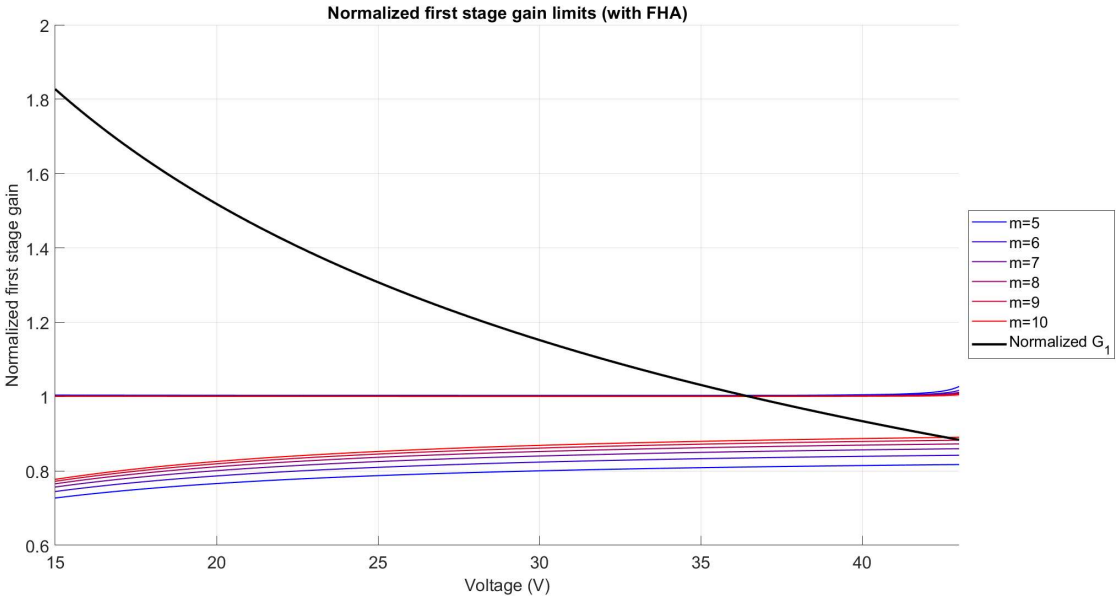


Figure 4.7: First stage gain limitations (example)

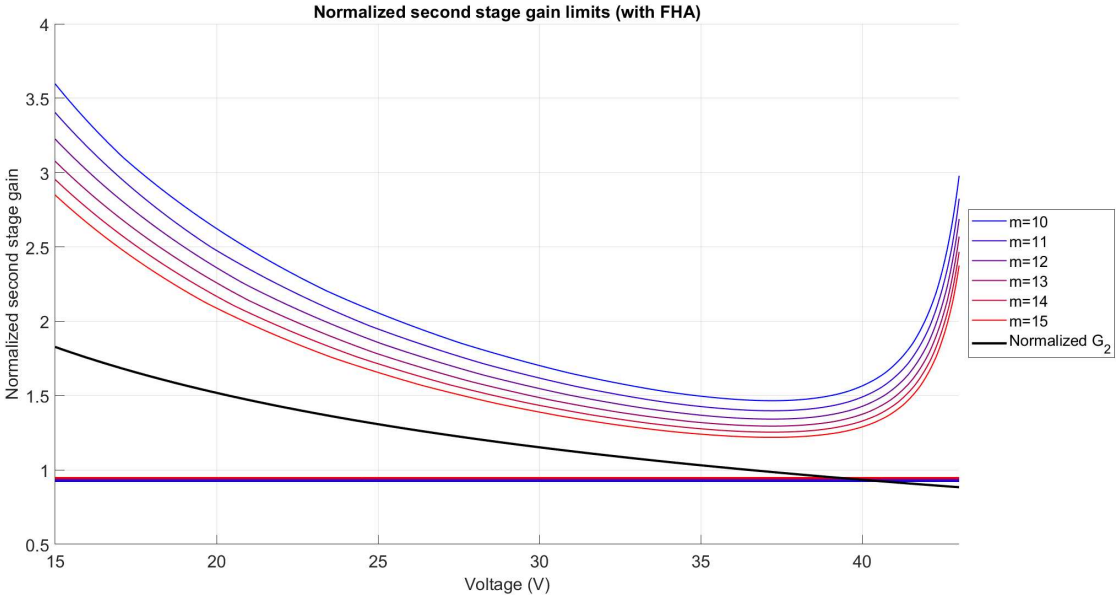


Figure 4.8: Second stage gain limitations (example)

4.1.2 FHA gain plotter

For later simulating this architecture in *LTSpice*, and to be able to analyze several working points, a complementary tool was developed to automatize the process of selecting the necessary operating switching frequency to achieve a certain gain with certain resonant network components, transformer turns ratio, and load value.

The FHA has discrepancies with the real behavior of the circuit when working far from the load independent point, however, the value taken from the application can be used as a first iteration, further applying small variations to the frequency, to achieve the desired gain. Of course in a real case the frequency would be set by a controller with a feedback control scheme implemented, however, that is not the scope of this work and hence the tests are done at open loop conditions.

The interface is presented in Fig. 4.9, developed with *MATLAB* app design tool. Its holding abilities allow for easy visualization of the gain characteristic in different conditions, as well as finding specific gain values and their normalized frequency value.

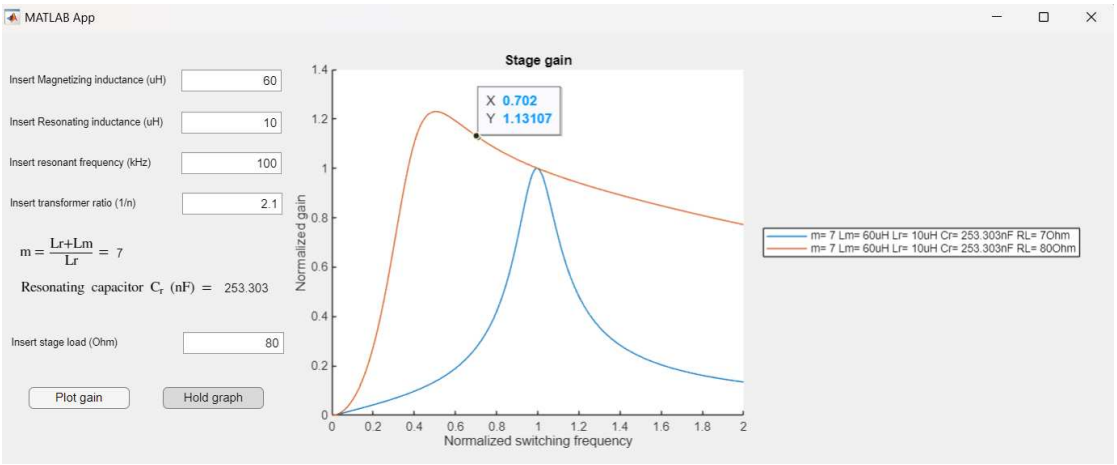


Figure 4.9: FHA gain plot tool

4.1.3 Efficiency report tool

Despite the power and versatility of *LTSpice* for electronic circuit simulations, it lacks a consistent method for exporting simulation information. This is even more noticeable when efficiency measurement is necessary, *LTSpice* offers a built-in tool for generating efficiency reports, but it requires precise circuit configurations, which may not always align with the complexities of diverse architectures. Apart from this aspect, it does not provide a reliable method to further process the efficiency report information through external software.

In this context, a developed *MATLAB* script is proposed to link the simulation output from *LTSpice* with the processing power of *MATLAB*, which can be found in the Appendix A.3. *LTSpice* allows for measurement commands that execute at the end time of the simulation, the implementation and justification for the measurements will be detailed in Chapter 6. For the introduction of this tool, it is only important to know that the console output information has a format as seen in Fig. 4.10, containing measurements of average power dissipated in multiple components, and current and voltage stresses. This information is later processed by the script to create an efficiency analysis, globally and locally at each stage, the power budget of each stage showing the main losses, and a table showcasing the components maximum stresses to assist in sizing them. Efficiency is computed considering the power consumed at the output and the power lost in the architecture as the sum of the loss at each component, as described in Eq. (4.2).

$$\eta = \frac{P_{out}}{P_{out} + P_{losses}} = \frac{P_{out}}{P_{out} + \sum P_{loss_{component}}} \tag{4.2}$$

Given the nature of the proposed architecture, it is interesting to observe the power flow through the system. The script also generates a Sankey diagram based on the power information provided by *LTSpice*, possible thanks to an existing tool from [24], showcasing in scale the amount of power derived through the stages and the pass-through converters. In Figs. 4.11, 4.12 and 4.13, examples of the output of the script can be seen.

```
pt3_mean: AVG(v(pt3))=0.381193 FROM 0.007 TO 0.008
pt4_mean: AVG(v(pt4))=0.382089 FROM 0.007 TO 0.008
pt5_mean: AVG(v(pt5))=0.152343 FROM 0.007 TO 0.008
pt6_mean: AVG(v(pt6))=0.151624 FROM 0.007 TO 0.008
pt7_mean: AVG(v(pt7))=0.151261 FROM 0.007 TO 0.008
pt8_mean: AVG(v(pt8))=0.152545 FROM 0.007 TO 0.008
pcr1_mean: AVG(v(pcr1))=1.25837 FROM 0.007 TO 0.008
pcr2_mean: AVG(v(pcr2))=0.113053 FROM 0.007 TO 0.008
pd1_mean: AVG(v(pd1))=1.99162 FROM 0.007 TO 0.008
pd2_mean: AVG(v(pd2))=1.99007 FROM 0.007 TO 0.008
pd3_mean: AVG(v(pd3))=0.702084 FROM 0.007 TO 0.008
pd4_mean: AVG(v(pd4))=0.718771 FROM 0.007 TO 0.008
pd5_mean: AVG(v(pd5))=0.71874 FROM 0.007 TO 0.008
pd6_mean: AVG(v(pd6))=0.701976 FROM 0.007 TO 0.008
pclink_mean: AVG(v(pclink))=0.0203905 FROM 0.007 TO 0.008
pcout_mean: AVG(v(pcout))=0.0106858 FROM 0.007 TO 0.008
pout_mean: AVG(v(pout))=674.351 FROM 0.007 TO 0.008
pin_mean: AVG(v(pin))=-697.402 FROM 0.007 TO 0.008
pdp1_mean: AVG(v(pdp1))=176.592 FROM 0.007 TO 0.008
pdp2_mean: AVG(v(pdp2))=274.094 FROM 0.007 TO 0.008
poutstg1_mean: AVG(v(poutstg1))=508.527 FROM 0.007 TO 0.008
poutstg2_mean: AVG(v(poutstg2))=400.257 FROM 0.007 TO 0.008
plink_mean: AVG(v(plink))=685.12 FROM 0.007 TO 0.008
max_vds_1: MAX(v(in,v1))=37.7116 FROM 0.00798 TO 0.008
min_vds_1: MIN(v(in,v1))=-3.77854 FROM 0.00798 TO 0.008
max_vtrans_1: MAX(v(v1,v6))=195.531 FROM 0.00798 TO 0.008
min_vtrans_1: MIN(v(v1,v6))=-192.243 FROM 0.00798 TO 0.008
max_vcr_1: MAX(v(v5,v6))=153.916 FROM 0.00798 TO 0.008
min_vcr_1: MIN(v(v5,v6))=-154.319 FROM 0.00798 TO 0.008
max_vd_1: MAX(v(v9,v11))=0.857544 FROM 0.00798 TO 0.008
min_vd_1: MIN(v(v9,v11))=-211.748 FROM 0.00798 TO 0.008
max_vclink_1: MAX(v(v11,in))=105.197 FROM 0.00798 TO 0.008
min_vclink_1: MIN(v(v11,in))=104.973 FROM 0.00798 TO 0.008
max_vds_2: MAX(v(v11,v13))=147.816 FROM 0.00798 TO 0.008
min_vds_2: MIN(v(v11,v13))=-7.25314 FROM 0.00798 TO 0.008
max_vtrans_2: MAX(v(v13,v18))=183.159 FROM 0.00798 TO 0.008
min_vtrans_2: MIN(v(v13,v18))=-181.716 FROM 0.00798 TO 0.008
max_vcr_2: MAX(v(v17,v18))=31.0866 FROM 0.00798 TO 0.008
```

Figure 4.10: Console output for one working point (example)

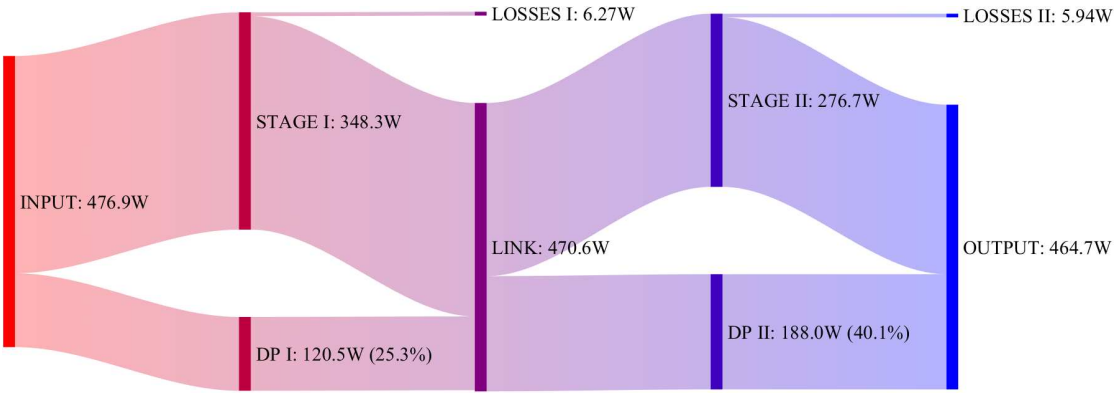


Figure 4.11: Sankey diagram for power flow visualization (example)

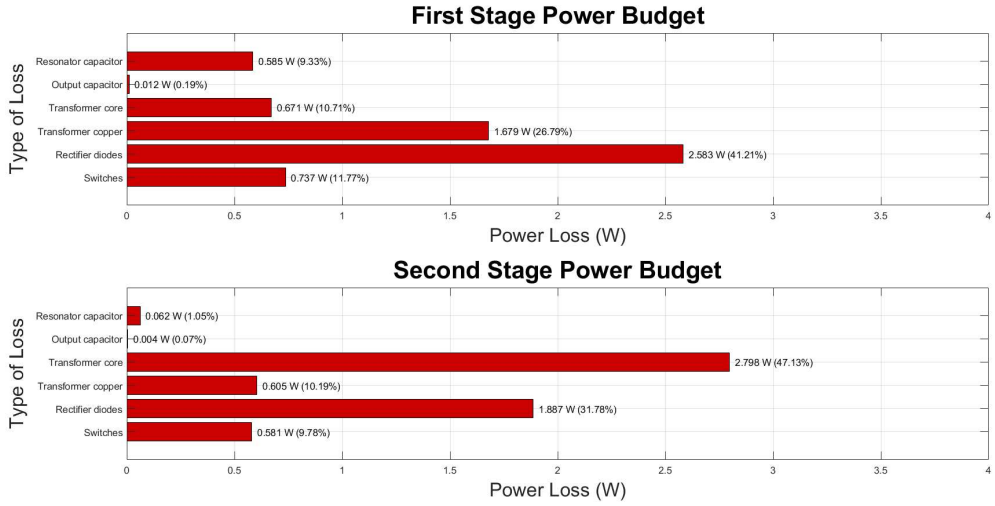


Figure 4.12: Power budget of each architecture (example)

Component	Maximum instantaneous voltage (V)	Maximum instantaneous current (A)	Maximum RMS current (A)
First stage MOSFETs stress	37.7748	16.3451	7.6120
First stage transformer primary stress	147.1980	15.7107	10.7532
First stage resonating capacitor stress	108.7210	15.7107	10.7532
First stage diodes stress	212.4060	5.3151	2.5749
First stage linkage capacitor stress	105.4880	12.6040	2.3478
Second stage MOSFETs stress	148.9470	5.0319	1.8425
Second stage transformer primary stress	174.7070	3.7726	2.6110
Second stage resonating capacitor stress	22.7228	3.7726	2.6110
Second stage diodes stress	209.8060	2.1624	1.0306
Second stage output capacitor stress	209.0950	1.4374	0.6413

Figure 4.13: Current and voltage stresses table (example)

4.2 LLC Topology Design and Optimization

4.2.1 Gain profiling based on architecture properties

Through the application of the design methodology proposed in Chapter 3, Section 3.2.4, and with the aid of the developed tool to implement this workflow, an interesting way of distributing the system gain profile was found for this type of architecture. The proposal is based on the following concepts:

- The exploitation of the strong load reduction effect of the first stage. This behavior can be exploited in a context where decreasing the gain is necessary, as low resistance values (high quality factor Q) allow for easier regulation above resonance $f_{sw} > f_r$. However, this load reduction effect does not allow the stage to increase its gain as low resistance values limit the maximum gain below resonance.
- The exploitation of the load independent point. Working at resonance allows for each stage to provide, independently of the load value, a gain equal to the turns ratio of the transformer, the intrinsic gain. This load independency behavior allows to provide step-up gain even when the load conditions do not allow increasing the gain from going below resonance.
- The tendency of efficiency to drop in value when the switching frequency goes considerably above or below the resonant frequency value. Above resonance switching frequencies mainly affect switching losses in the semiconductor devices, and copper losses in the inductive components. Below resonance conduction losses tend to rise with higher root-mean-squared values for currents through the system. With this information, the intrinsic gain of each stage is selected so at the most probable working points both of them are working in resonance, at the load independent working point, maximizing efficiency for the most typical scenarios.

With this information, the intrinsic gain of each stage is set so that at nominal input voltage from the photovoltaic panel both stages work at resonance. For this particular photovoltaic panel, the nominal voltage is of 36.5V, where the MPP for STC is located.

To the left of the nominal input voltage, where gain has to increase, the first stage with intrinsic high Q (difficulty for increasing gain) stays at resonance, hence providing a flat gain profile independent of load value with intrinsic gain value, while the second stage which experiences lower quality factor values provides the gain increase. To the right of the nominal input voltage, where the gain has to

decrease, the second stage stays at resonance, hence providing a flat gain profile with intrinsic gain value, while the first stage which experiences the high Q values provides the gain decrease in an easier manner. In the case of extreme light load conditions where the first stage is not able to decrease the gain, the first stage morphs its full-bridge inverter to the half-bridge inverter, working at resonance, while the second stage boosts the gain to maintain the voltage output, which is the already introduced "half-bridge mode". This multi-mode operation is highlighted in Fig. 4.14.

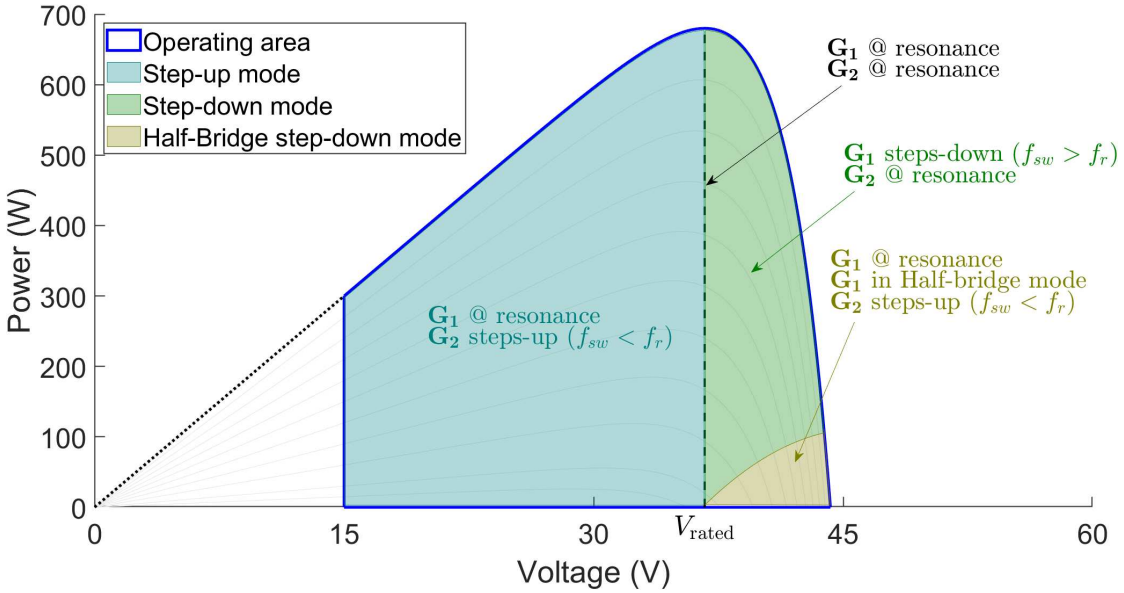


Figure 4.14: Graphical representation of the multi-mode approach of the proposed converter in the range of target working points.

The general shape of the gain profiles is proposed in Fig. 4.15, where the flat gain profile regions can be observed, while the complementary stage provides the step-up/down to the gain. Whereas at nominal input voltage both stages work at resonance providing ideally the best stage efficiency. The degree of freedom of these gain profiles relies on the selection of the turns ratio of each stage which essentially defines the intrinsic gain of each stage, the definition of this quantities will be discussed in further sections. The resonant network components must also be defined which will alter the gain regulations capabilities.

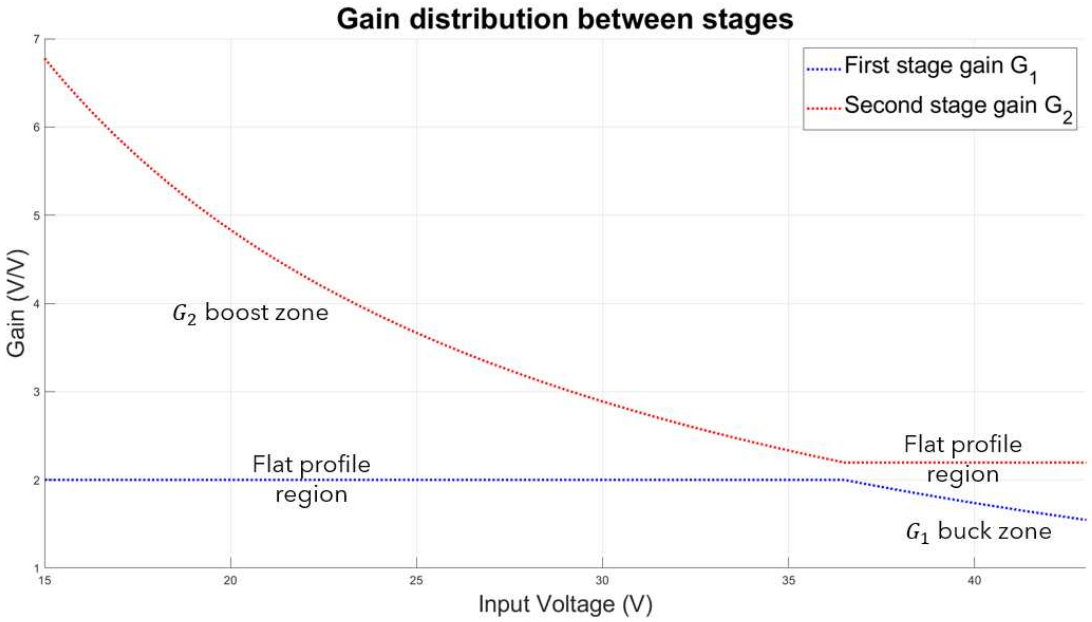


Figure 4.15: General shape of the gain profiles proposed for the architecture

4.2.2 Design and optimization for maximum efficiency

The main goal for the proposal of this architecture is the maximization of efficiency in the power conversion. In the previous section, the gain profiles general shape was proposed, missing which intrinsic gain should be assigned to each stage in particular.

The first reasonable idea is to exploit the power flow behavior of the IPOS configuration, where minimizing the gain maximizes the power flow through the ideal direct path or pass-through converter. The minimization of the intrinsic gain of each stage happens when both of them are equal, in qudratic form, as if one would decrease upon this limit, the other one should increase to compensate. In this way, imposing a turns ratio according to the expression in Eq. (4.3) derived from the case of nominal input voltage case, produces the maximum direct flow to the load bypassing the resonant power converters the most. These intrinsic gain values create the gain profiles seen in Fig. 4.16.

$$G_{tot_{@36.5V}} = \frac{350V}{36.5V} = 9.59 \tag{4.3}$$
$$G_{1_{@36.5V}} = G_{2_{@36.5V}} = \sqrt{G_{tot_{@36.5V}}} - 1 = \boxed{2.1}$$

The multi-variable nature of the LLC resonant power converter paired with the

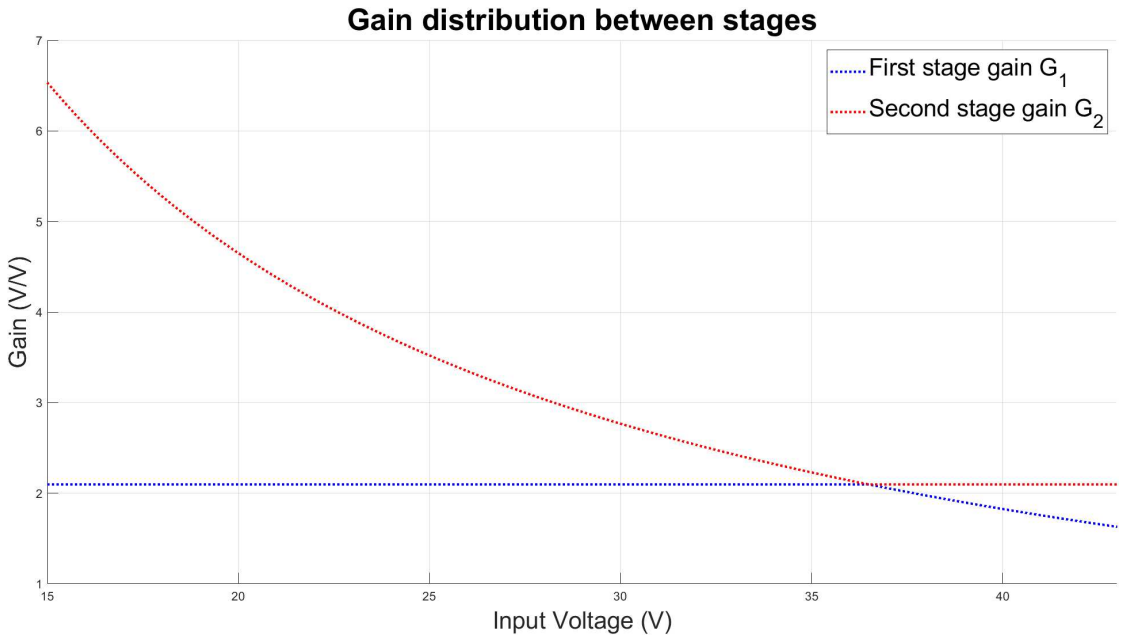


Figure 4.16: First proposal for the gain profiles

complex loading characteristic and multiple working points makes the definition of the circuit components parameters a complex challenge. This proposal for the gain profiles serves as a starting point for a process of optimization, paired with an initial proposal of the resonant network components, which are selected based on the necessary condition for ZVS (L_m limitation) and typical values for the series resonator for a certain resonant frequency f_r, according to limitations in technology. The design and optimization process in this work is based on the proposal of a first approach/iteration, further studying the behavior of the system by simulation in *LTSpice*, with data processing in *MATLAB*, for determining the effects of the variation of the resonant network components and the turns ratio of each stage. This approach resembles the process of gradient descent optimization, finding the directions of variables change in which the efficiency of the system increase and decrease to alter the initial iteration into a more refined and efficient solution.

Starting from the inductors L_m, the necessary condition derived for ZVS is imposed, creating a maximum value for the inductance. At the same time, this inductances should be ideally maximized, as lower values of inductance create greater magnitude of current flowing through it, which does not participate in the power transfer. This flowing current, although not participating in the power conversion, creates conduction losses upon the full-bridge inverters and resonant networks. However, as it will be detailed in the next chapter, having magnetic

integration where these L_m inductances are implemented as the magnetizing inductance of each transformer derives into having greater number of turns, which essentially creates more conduction loss in the transformer. As this example shows, the behaviors and relations inside resonant power converters are complex and at first glance not easy to notice in all cases, factors that initially are not covered can present a significant challenge for optimization. For this reason, the design of each stage was a process of iteration and making changes in the run to achieve the final selection of components.

Maximizing efficiency implies minimizing devices losses, in LLC power resonant converters around 70% of the total losses are due to conduction losses [25]. This tendency paired with a behavior discussed in Chapter 3, Section 3.2.1 justify the first optimization characteristic seen in Fig. 4.17. When analyzing power conservation, once again what should be considered is that ports with large voltage values will have low current values, and vice-versa. Regions with lower current values are favorable in terms of conduction losses. This leads to the thought of rising the intrinsic gain of the first stage, creating larger output voltage from the first stage, which directly translate to a decrease in the current level. The intrinsic gain of the second stage must meanwhile be lowered to compensate at nominal input voltage. In this way, the output rectifier of the first stage, the input inverter of the second stage, and the resonant network components of the second stage see reduced conduction losses. However, this also makes the first stage struggle most when decreasing the gain is necessary, and as the second stage has less intrinsic gain, increasing the overall gain can become more difficult. But rising the first stage gain to a reasonable value without relying completely into half-bridge operation for reducing the gain is desirable to boost the efficiency.

Action	Overall current stress	Efficiency	Gain regulation capabilities
$\uparrow G_1 \quad \downarrow G_2$	↓	↑	↓
$\downarrow G_1 \quad \uparrow G_2$	↑	↓	↑

Figure 4.17: First optimization action and effect

With this first optimization proposal, it was found that rising the first stage intrinsic gain from 2.1 to 3 produces a greater efficiency profile while maintaining reasonable ability of gain regulation. The new second stage intrinsic gain is restricted so that it follows the general gain profiles shape that were imposed, the value is derived in Eq. (4.4), the final value for the intrinsic gain of the second stage would be finally adjusted to 1.47 to account for the voltage drops across the

circuit. With this information, the final desired gain profiles can be proposed in Fig. 4.18. Based on the defined gain profiles for both stages, the voltage stress reduction intrinsically provided by the architecture can be characterized by comparing the output voltage of each stage for every input voltage value with gain G, to the output voltage that each stage would exhibit in a pure quadratic architecture, where the gain is defined as $G + 1$. This comparison is illustrated in Fig. 4.19.

$$\begin{aligned} G_{tot_{@36.5V}} &= (3+1)(G_{2_{@36.5V}} + 1) = 9.59 \\ G_{2_{@36.5V}} &= \frac{9.59}{4} - 1 = 1.4 \end{aligned} \tag{4.4}$$

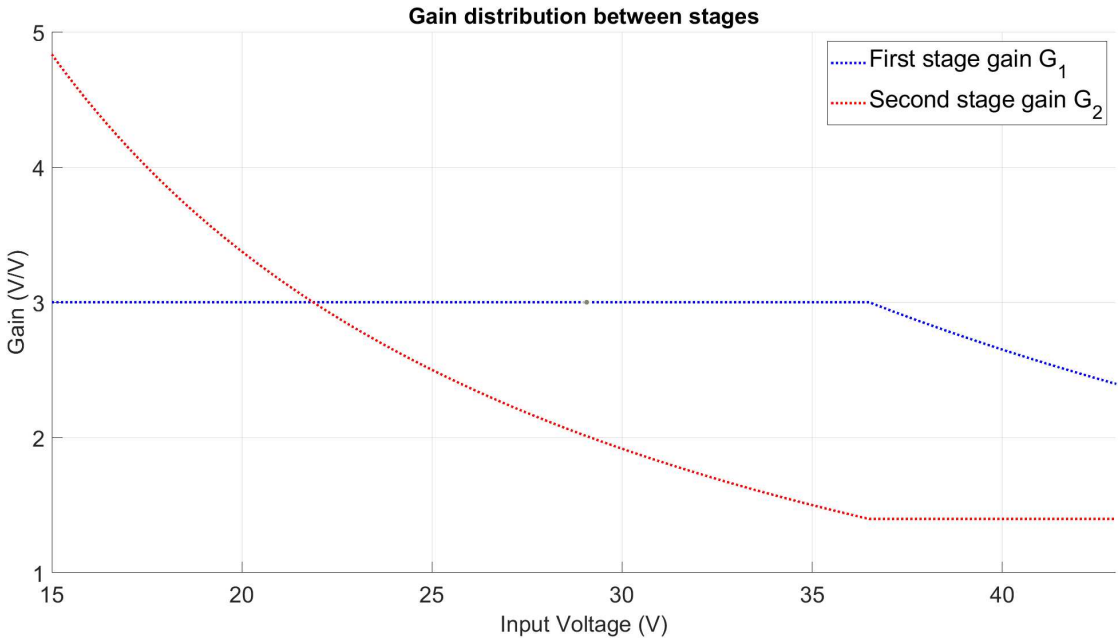


Figure 4.18: Proposed gain profiles

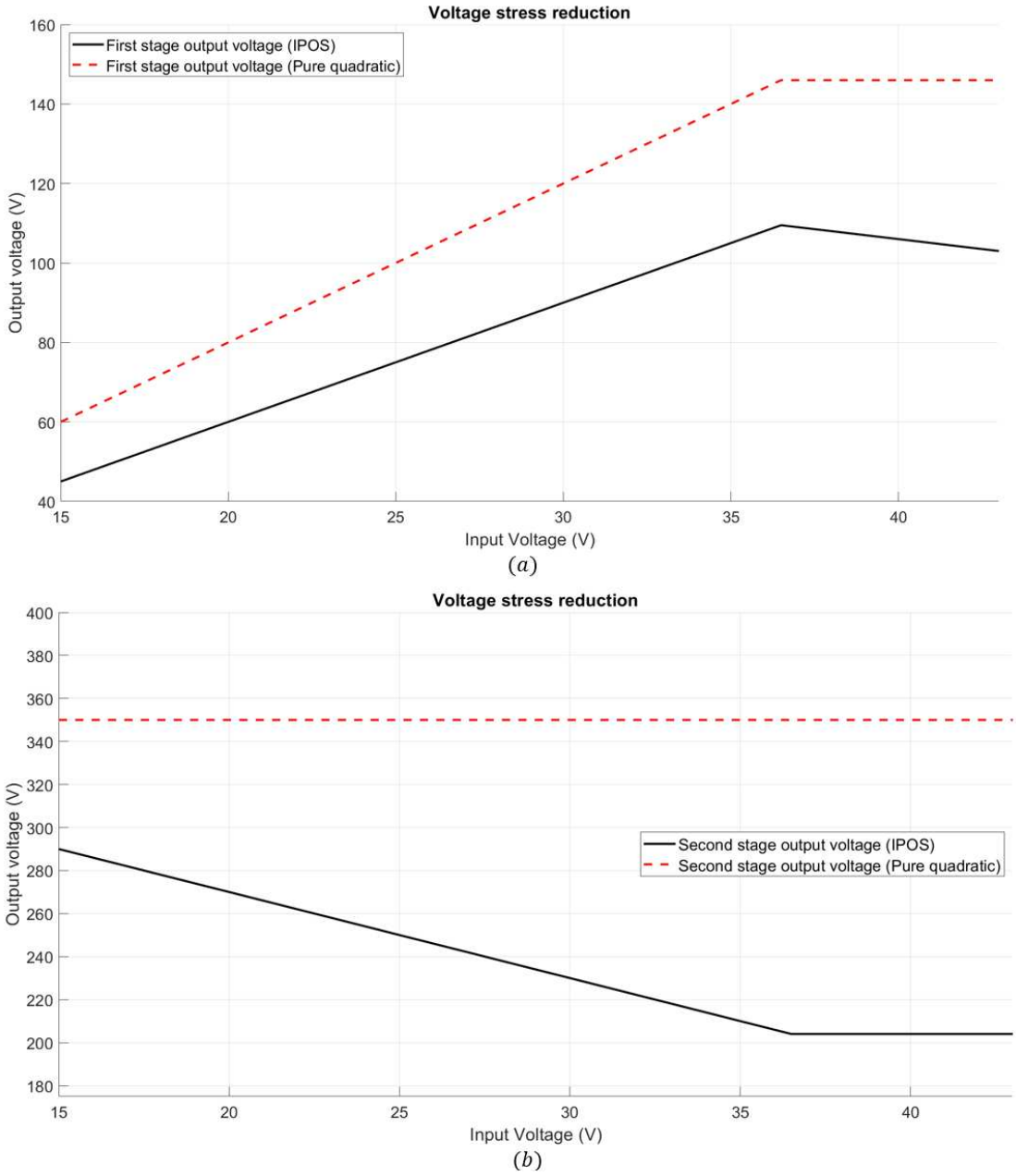


Figure 4.19: Voltage stress reduction of the IPOS configurations. (a) First stage voltage stress. (b) Second stage voltage stress

Modifying the quality factor through the series resonator values is also another proposal for optimization. As it was stated, the first stage is in charge of decreasing the gain, so it is favored by high quality factor values, while the second stage

is in charge of increasing the gain, hence favored by low quality factor values. Having beneficial quality factor values for each stage allows them to not deviate considerably from resonant frequency to regulate, creating a flatter efficiency profile across different input voltage values.

For the first stage, rising L_r and decreasing C_r by the same factor to maintain the same resonant frequency produces an intrinsic rise of the quality factor, however, at the step of physically implementing the components, it was found that capacitors of low capacitance values that can withstand large values of current are scarce in the market, this is going to be addressed in the components selection section in Chapter 6. For the second stage, rising C_r while decreasing L_r by the same factor to maintain the same resonant frequency produces an intrinsic lower quality factor, however, it was observed in simulation that this direction caused greater current stress through the architecture for the case of minimum input voltage.

The value of L_m for each stage must be selected having into consideration the ZVS condition. Achieving soft-switching in the entire working points range is complicated without sacrificing efficiency in other aspects, the values defined for the L_m inductances consider the ZVS condition to happen at least in the vicinities of the nominal input voltage for a given dead time of 100ns. Other important considerations of ZVS are:

- The dead time is a degree of freedom itself that can be altered in run-time. If the condition is not met for different working points, the dead time could be risen to provide the necessary window for V_{DS} dropping to zero.

- Not complying with the ZVS condition does not mean that ZVS is not achieved completely. Partial ZVS can happen where the voltage drops in the dead-time, but not down to zero. This behavior is still more convenient than hard-switching in terms of switching losses.

- The necessary condition imposed is not sufficient as it is a simplification of the behavior. In the real application other capacity values can affect ZVS such as the stray capacitance of the transformer windings. It is important to leave clearance in the value of the inductance for the further implementation.

The ZVS condition applied to different working points can be seen in Eqs. (4.5) through (4.9), where the capacitance value is related to the specific MOSFET transistors that will be discussed in the components selection section in Chapter 6.

$$For\ the\ first\ stage:$$

$$L_{m_1} \leq \frac{100ns}{8 * 1669.3pF * 100kHz} @36.5\text{V } 680\text{W} = 74.88\mu H \tag{4.5}$$

$$L_{m_1} \leq \frac{100ns}{8 * 1564.5pF * \sim 125kHz} @43\text{V } 300\text{W} = 64\mu H \tag{4.6}$$

$$L_{m_1} \leq \frac{100ns}{8 * 1564.5pF * \sim 175kHz} @43\text{V } 50\text{W} = 45.6\mu H \tag{4.7}$$

$$For\ the\ second\ stage:$$

$$L_{m_2} \leq \frac{100ns}{8 * 846.3pF * 100kHz} @146\text{V } 680\text{W} = 147.7\mu H \tag{4.8}$$

$$L_{m_2} \leq \frac{100ns}{8 * 1773.9pF * \sim 25kHz} @60\text{V } 300\text{W} = 281.9\mu H \tag{4.9}$$

The final values of the design to be implemented are summarized in Table 4.1, tuned to set the resonant frequency of both stages at 100 kHz, to fulfill the gain regulation necessity and to be able to comply with the ZVS conditions in the vicinities to resonance. Many iterations in *LTSpice* simulation environment led to the selection of this quantities, starting from values in the order of magnitude of similar applications such as [21]. LLC power resonant converter parameters selection is not straightforward considering the amount of combinations that can be proposed, optimization was developed in a gradient-descent-like scheme, and considering certain architecture dependent behaviors like the quality factor effect on each stage. Further optimization of this architecture could be evaluated in future works.

Parameter	**First stage value**	**Second stage value**
Resonating capacitor C_r	224 nF	270 nF
Resonating inductor L_r	11.3 µH	9.38 µH
Shunt inductor L_m	60 µH	120 µH
Figure of merit m	6.31	13.8
Transformer turns ratio $1/n$	3	1.47

Table 4.1: Summary of LLC topology parameters for first and second stage

With the proposed developed tool for design of this work, the final loading

profiles can be seen in Figs. 4.20 and 4.21 with the contrast to the equivalent system loading profile seen in Figs. 4.22 and 4.23; while the gain profiles superimposed to the gain limitations can be seen in Figs. 4.24 and 4.25. For the first stage, the gain profile collides with the minimum gain limitations, however, in this light load scenario, the half bridge mode is intended to take care of the regulation issues. The proposed gain profiles are possible with the selected parameters, which finishes the design workflow proposed in terms of gain regulation and loading.

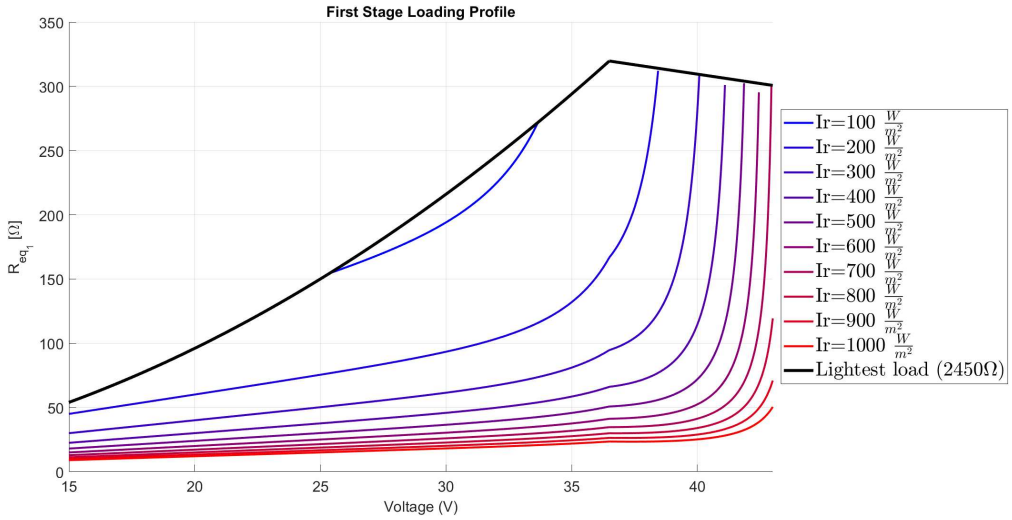


Figure 4.20: First stage loading profile (final)

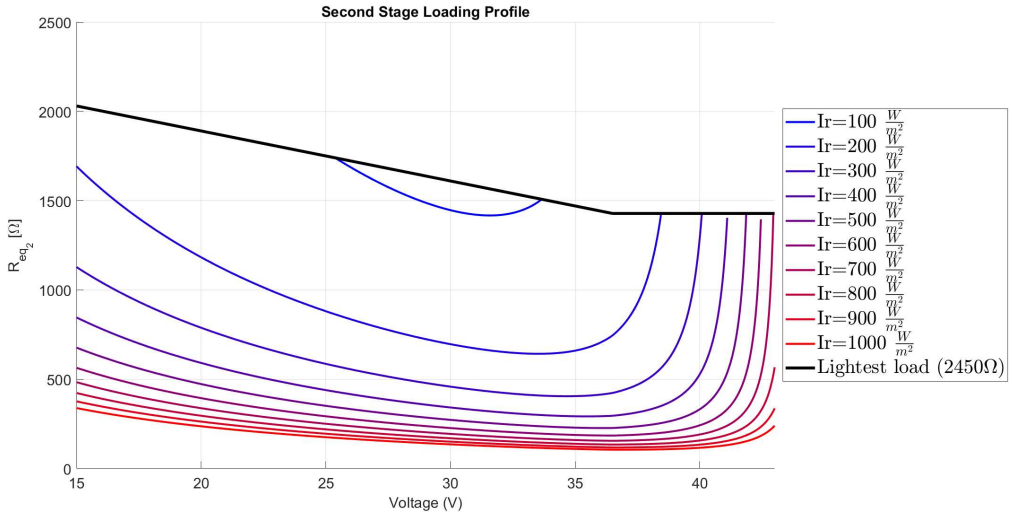


Figure 4.21: Second stage loading profile (final)

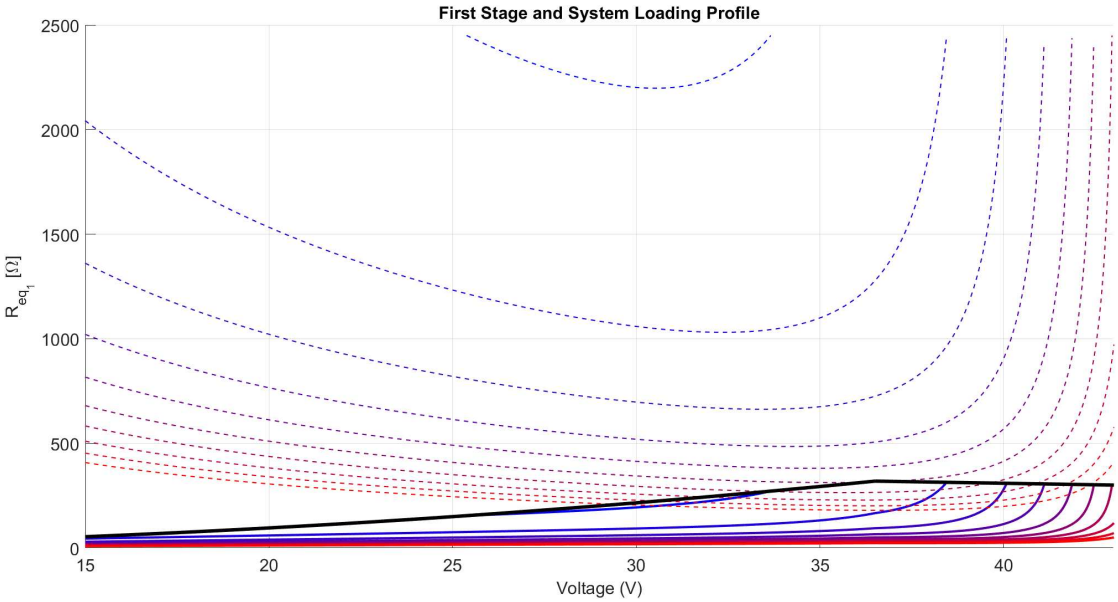


Figure 4.22: First stage (solid lines) and system loading profile contrast (dotted lines)(final)

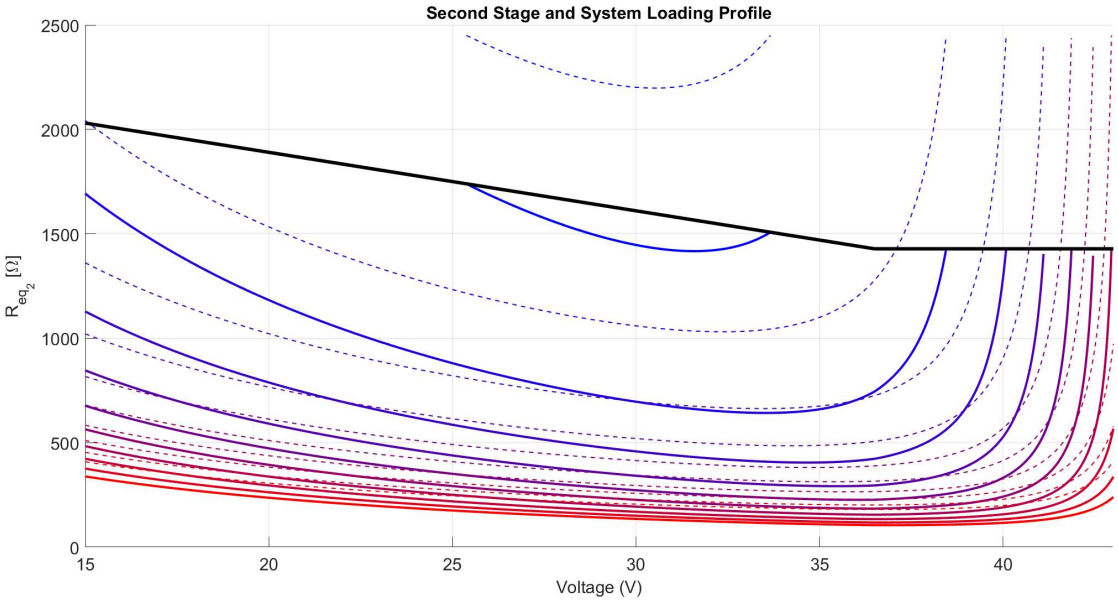


Figure 4.23: Second stage (solid lines) and system loading profile contrast (dotted lines)(final)

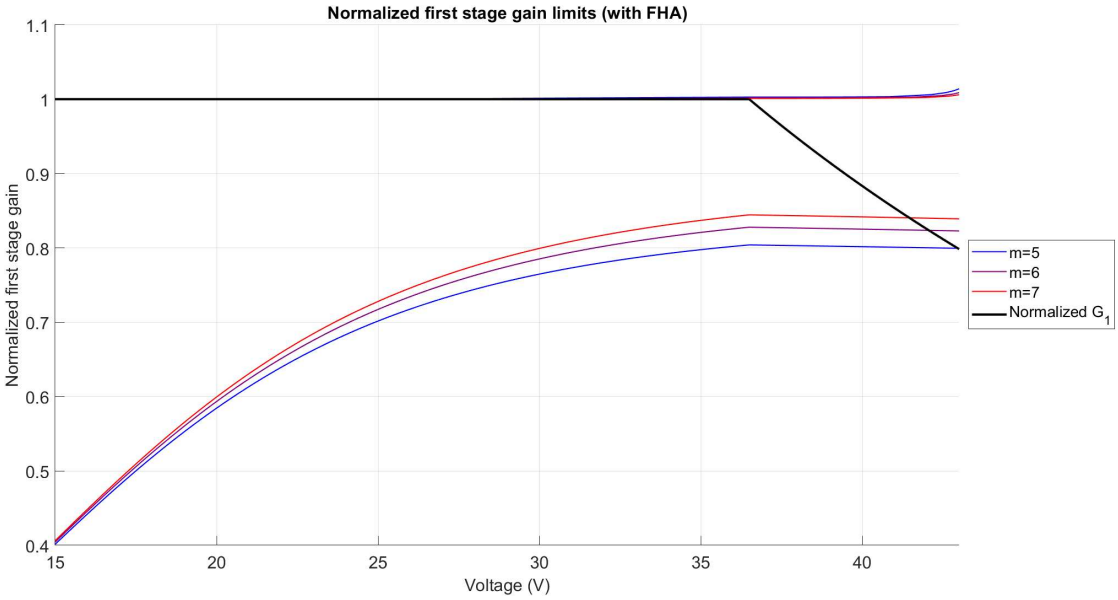


Figure 4.24: First stage gain limitations (final)

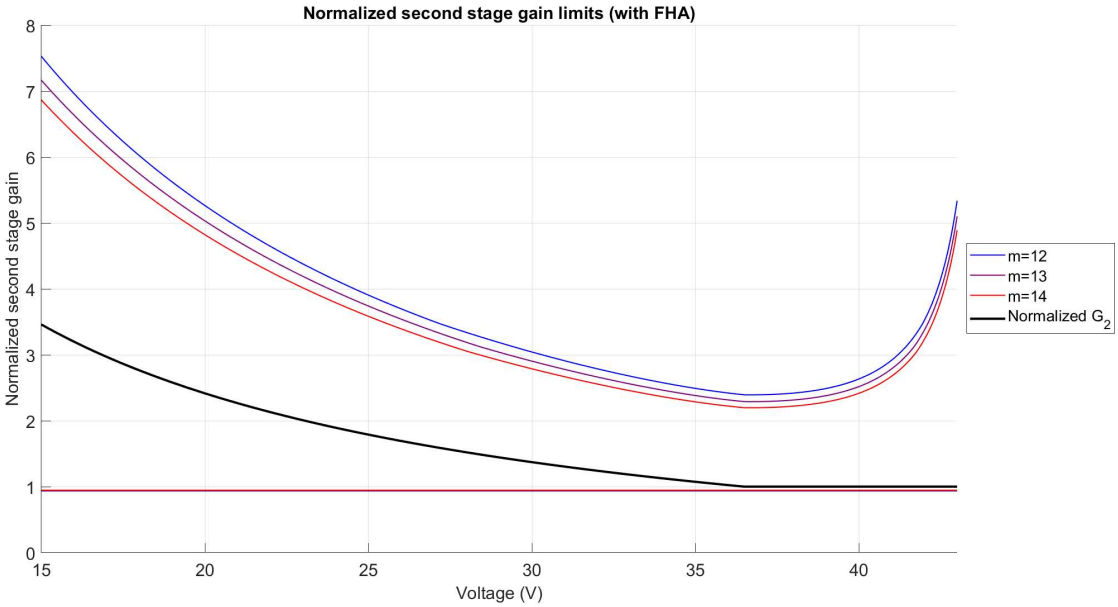


Figure 4.25: Second stage gain limitations (final)

4.2.3 Output decoupling capacitors sizing

Voltage output ripple filtering is crucial not only for achieving a stable DC voltage but also for decoupling the dynamics between stages, which is essential for implementing the proposed workflow. Referring to this mechanism as a simple low-pass filter would be misleading, as the load is inherently non-linear, with the first stage feeding the second, and the second stage driving the inverter. The fact that an equivalent resistance can be found and applied to this workflow is primarily due to the proper decoupling between each system. Therefore, this mechanism should be better described as an energy buffering system, where the previous stage delivers a pulsating amount of energy, and the next stage consumes it in a similar manner. The intermediate capacitor between them serves as a "handshake" component: it temporarily stores energy when not in use and delivers it when the next stage demands it, while the energy intake from the previous stage is done in a time-varying way.

A common approximation used in power electronics for capacitors in steady-state operation is the small ripple approximation, which assumes that in a well-designed power converter, the output voltage ripple is negligible compared to the average output voltage value [26]. In other words, after the output capacitor, the current consumed by the load is assumed to be conserve the average value from the initial current, with the capacitor absorbing all AC components, which have a zero average value, as showed in Fig. 4.26. However, this means that the capacitor voltage will vary over time as it charges and discharges in response to the AC current, as described by Eq. (4.10). The small ripple approximation assumes that this voltage variation is so small that the ripple can be considered negligible, even though it still exists. The fact that the dynamic voltage at the capacitor determines the overall ripple allows to constrain the capacitance value to meet the desired output voltage ripple specifications.

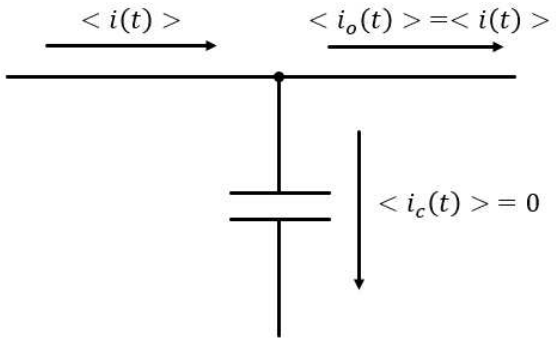


Figure 4.26: Small ripple approximation consequence on current. <i> represents average value

$$v_c(t) = V_c(0) + \frac{1}{C}\int_0^t i_c(t)dt \tag{4.10}$$

The analysis of the voltage ripple is done in steady state, which introduces an important condition for the voltage waveform of the capacitor. In steady state, the net change over one switching period of the capacitor voltage must be zero, as the voltage is neither having a tendency to increase or decrease in time. This is the capacitor charge balance law and is linked to the fact that the average current flowing through a capacitor in steady state is zero, as demonstrated in Eq. (4.11).

$$\begin{aligned} v_c(T_s) &= V_c(0) + \frac{1}{C}\int_0^{T_s} i_c(t)dt \\ v_c(T_s) - V_c(0) &= \frac{1}{C}\int_0^{T_s} i_c(t)dt \\ 0 &= \frac{1}{C}\int_0^{T_s} i_c(t)dt \Rightarrow \boxed{\int_0^{T_s} i_c(t)dt = 0} \end{aligned} \tag{4.11}$$

This implies that the positive area under the curve $i_c(t)$ must be equal to the negative area under the curve, these areas are essentially the positive and negative charge Q_+ and Q_- flowing through the capacitor. The positive charge is responsible of the increase in voltage while the negative charge is responsible of the decrease in voltage, but after a switching period, the rise and fall of the voltage must not imply a global increase or decrease of the voltage as the charge balance law establishes. This simplifies the analysis in the sense that only one type of charge should be analyzed, evaluating the voltage rise/fall that essentially represents the ripple at the output.

To carry on the analysis, knowledge on the current waveform of the capacitor is needed, which changes depending on the operating switching frequency applied to the converter, as well as the stage that is being evaluated. It is not equivalent analyzing the output of the first stage and the second stage, as the dynamics of the output current are different, the behavior that holds is the conservation of the average value due to the small ripple approximation. To simplify the derivation, the analysis is considered at resonant frequency, where the current waveform at the output of the rectifying network is a rectified sinusoid, considering maximum power extraction from the photovoltaic panel at nominal voltage. A constraint for the minimum value of capacitance will be stated for a specific voltage ripple value, serving as a starting point for the order of magnitude of the capacitance value. Then greater capacitance value can be selected to further reduce the ripple voltage and cover the cases outside resonance.

The second stage is analyzed first. Since the inverter dynamics are not studied in this work, the load is assumed to be purely resistive, which significantly simplifies the analysis. If the dynamics of the inverter are introduced in the future, the analysis of the output capacitor in the second stage would need to be revisited, following a similar approach to the one that will be described for the output capacitor of the first stage, where the dynamics are incorporated.

For the second stage, the first step is to relate the output DC current to the rectified sinusoid peak value from the output rectifier of the stage, through Eq. (4.12). The waveform for the rectifier output current can be seen in Fig. 4.27. Applying the small ripple analysis, the current waveform in the capacitor is shown in Fig, 4.28, where the charge below the curve is highlighted. In order to represent mathematically the value of the charge, the angles θ_1 and θ_2 expression are needed to integrate, these values can be derived by analyzing the zero-crossing of the function based on the concept of null average value fo the waveform, as seen in Eq. 4.13. Finally, the voltage ripple can be defined in Eq. (4.15) with its correspondent constraint.

If the ripple is constrained to 1% of the output voltage, and the current is derived by the knowledge of the maximum power being processed and the voltage at the output, while the switching frequency is the resonance frequency (100 kHz), then the second stage output capacitor is constrained as stated in Eq. 4.16. The selected capacitor to have a margin is the standardized value 4.7 µF.

$$
\begin{aligned}
I_o &= \frac{1}{\pi}\int_0^{\pi} i_{output\ rectifier}(\theta)d\theta \\
I_o &= \frac{1}{\pi}\int_0^{\pi} I_{s_{max}}\sin\theta d\theta \\
I_o &= \frac{1}{\pi} I_{s_{max}}[-\cos\theta]|_0^{\pi} \\
I_o &= \frac{2}{\pi} I_{s_{max}} \\
I_{s_{max}} &= \boxed{\frac{\pi}{2} I_o}
\end{aligned}
\tag{4.12}
$$

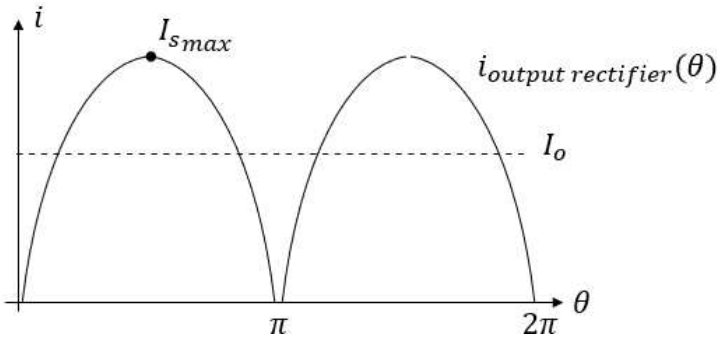


Figure 4.27: Output rectifier current waveform

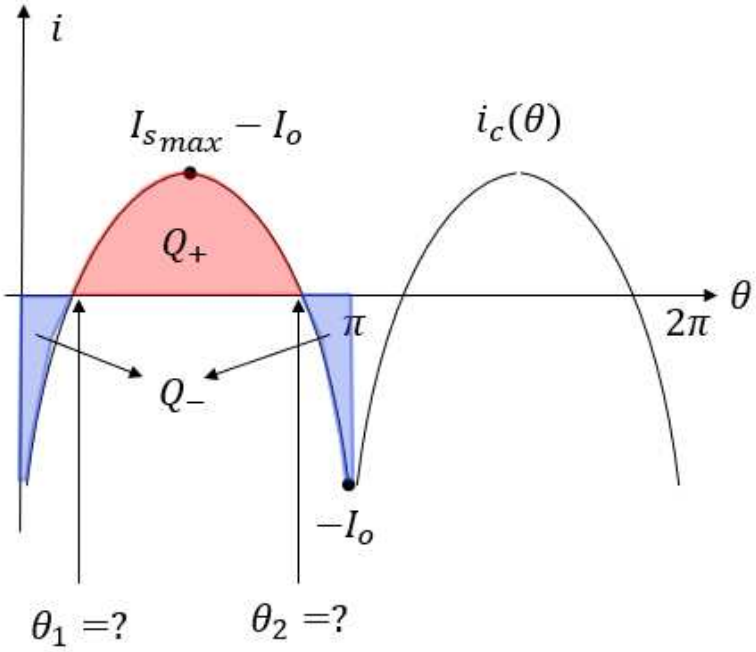


Figure 4.28: Output capacitor current waveform

$$\frac{\pi}{2} I_o \sin(\theta) - I_o = 0$$

$$\sin(\theta) = \frac{2}{\pi}$$

$$\theta = \arcsin\left(\frac{2}{\pi}\right) \Rightarrow \theta_1 = 0.69;\ \theta_2 = \pi - \theta_1 = 2.45 \qquad (4.13)$$

In terms of time :

$$t_1 = \theta_1 \frac{1}{2\pi f_{sw}};\ t_2 = \theta_2 \frac{1}{2\pi f_{sw}} \qquad (4.14)$$

$$\Delta V = \frac{1}{C}\int_{t_1}^{t_2}\left(\frac{\pi}{2}I_o\sin\left(2\pi f_{sw}t\right) - I_o\right) \leq \Delta V_{max}$$
$$\Delta V = \frac{1}{C}I_o\left[\frac{\pi}{2}\frac{1}{2\pi f_{sw}}\left(\cos\theta_1 - \cos\theta_2\right) - \frac{1}{2\pi f_{sw}}(\cos\theta_1 - \cos\theta_2)\right] \leq \Delta V_{max}$$
$$\Delta V = \frac{1}{C}0.105\frac{I_o}{f_{sw}} \leq \Delta V_{max} \Rightarrow C \geq \boxed{0.105\frac{I_o}{\Delta V_{max} f_{sw}}} \tag{4.15}$$

$$C_{out} \geq 0.105\frac{\frac{680W}{350V}}{0.01 * 350V * 100kHz} = \boxed{0.58\mu F} \tag{4.16}$$

The first stage output capacitor constraint is much more mathematically complex, as the current that flows into the next stage is not purely DC. As it was mentioned, with the small ripple approximation reasoning, what has to be conserved is the average value. While the first stage outputs a rectified sinusoid current waveform, the input to the following stage includes the DC component I_o that flows through the pass-through converter, as well as a rectified current waveform drawn by the second stage resonant power converter. The problem is that the phase between the currents is unknown, so a worst-case scenario has to be evaluated. Given that the capacitor current is the difference between the output current from the rectifier and the input current to the second stage, the phase difference will determine different possibilities for the capacitor current waveform, this phenomena can be observed in Fig. 4.29, where the effect on phase-shift of the output current affects the current waveform of the output capacitor.

The output rectifier current average value I_{o_1} is determined by the power being processed and the first stage output voltage value, as seen in Eq. (4.17). This average I_{o_1} is split to the DC current I_o directly fed to the load through the pass-through converter, defined in Eq. (4.18). The remaining average value must correspond to the rectified sinusoid fed into the second stage resonant power converter, defined in Eq. (4.19). The current thorugh the first stage output capacitor is then defined in Eq. (4.20).

$$I_{o_1} = \frac{680W}{(3+1)36.5V} = 4.66A \tag{4.17}$$
$$I_o = \frac{680W}{350V} = 1.94A \tag{4.18}$$
$$I_{in_2} = I_{o_1} - I_o = 2.72A \tag{4.19}$$

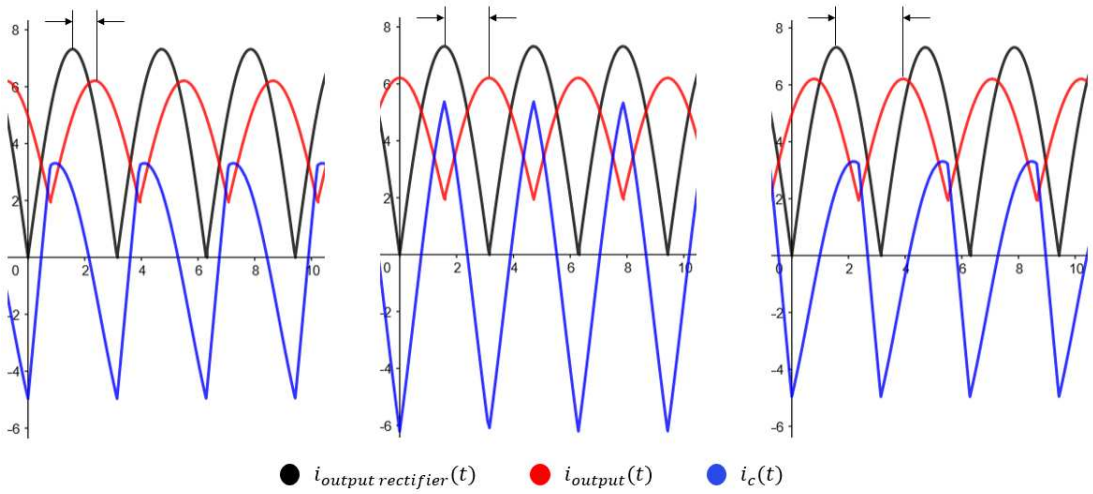


Figure 4.29: Current phase-shift effect on first stage output capacitor

$$i_C(t) = \frac{\pi}{2} I_{o_1} \left|\sin\left(2\pi f_{sw} t\right)\right| - \left[I_o + \frac{\pi}{2} I_{in_2} \left|\sin\left(2\pi f_{sw} t + \phi\right)\right|\right] \tag{4.20}$$

The expression is complex to analyze as the search for the maximum Q_+ requires the maximum search through optimization without a closed form for the zero-crossing time instants. The analysis to find the worst case scenario is done numerically with the use of *MATLAB*, by sweeping the possible phase-shift values, finding the zero-crossing instants and numerically integrating the current expression. The results are displayed in Fig. 4.30, while the code for implementing this analysis can be found in Appendix A.4.

For an output voltage ripple of 1% and the numerically calculated maximum charge, the capacitor constraint is defined in Eq. (4.21). The selected capacitor to have a margin is the standardized value 33 µF.

$$\begin{aligned} \Delta V &= \frac{Q_+}{C} \leq \Delta V_{max} \\ C &\geq \frac{Q_+}{\Delta V_{max}} = \frac{7.65\mu C}{0.01 * (3+1) * 36.5V} = \boxed{5.24\mu F} \end{aligned} \tag{4.21}$$

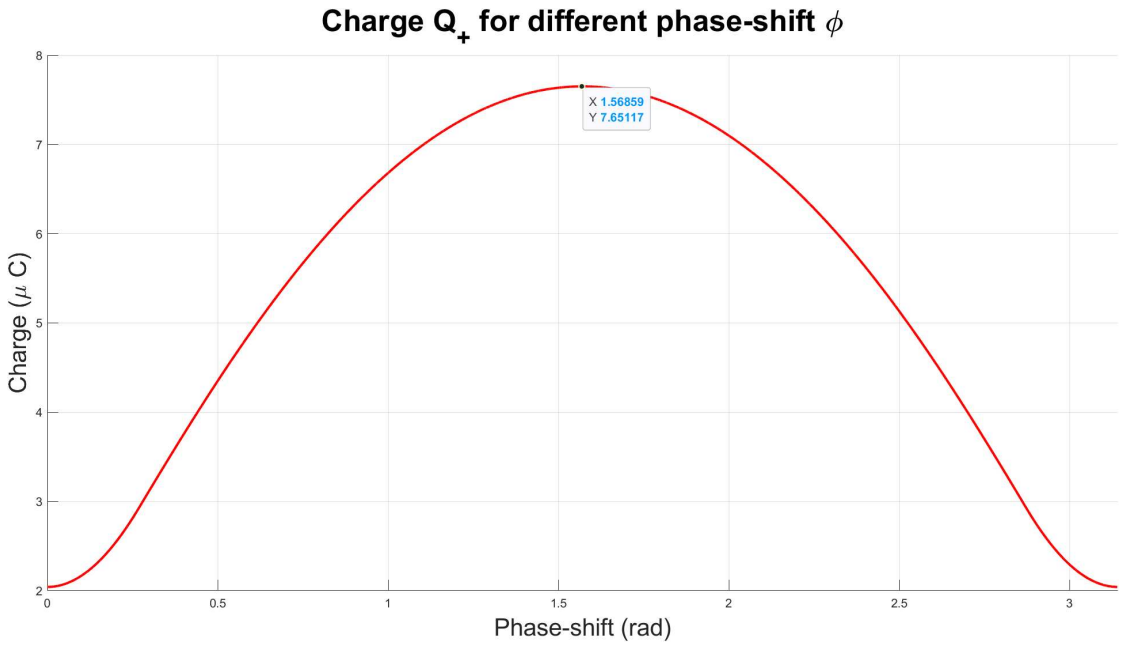


Figure 4.30: Positive charge worst case scenario analysis

Chapter 5

Magnetics Modeling

5.1 Coupled Magnetics modeling

5.1.1 Magnetic integration in the LLC topology

One of the main advantages of the LLC topology resonant power converter is the ability to integrate the inductive components of the resonant network in a single device: the transformer. Transformers can be modeled with several equivalent networks, the concept of magnetic integration exploits one of these specific networks which resembles a section of the circuit in the LLC topology. Building transformers for LLC design is an extremely complex task requiring careful control of the achieved quantities. This chapter aims to introduce the concepts involved in the definition of the transformer models, and to define the losses involved in order to integrate them in the circuit simulation. Transformers are highly non-linear and often employ empirical expressions to model certain aspects. Literature on the design of this specific component in specific applications is often scarce and misleading. An analysis with important considerations is presented in this work, specifically highlighting considerations that must be taken into account in a wide input voltage range converter scenario. The detailed analysis and construction of the transformers is left for future work.

Transformers are essentially coupled inductors, where the coupling is enhanced by a ferromagnetic core that confines the magnetic field to achieve the coupling itself. Electrically, the base for the model can be presented as in Fig. 5.1 paired with the linear algebraic analysis from Kirchoff laws in Eq. (5.1) expressed in matrix form. The expression is for additive coupling, which is defined as the entering current I_1 generating a positive contribution to V_2 and the same behavior

happening between I_2 and V_1, visually represented in the figure through the dots convention. L_1 and L_2 represent the self-inductance of the two windings. The physical definition for the self-inductance is stated in Eq. (5.2), with ϕ_i magnetic flux linked to the total number of turns N_i, when the current I_i flows through the winding. The mutual inductance M can be defined from both windings in Eq. (5.3) [27], where ϕ_{21} is the magnetic flux linking the secondary winding due to the current I_1 of the primary winding and ϕ_{12} is the magnetic flux linking the primary winding due to the current I_2 of the secondary winding. The mutual magnetic flux densities can be expressed as in Eqs. (5.4) and (5.5). k_1 and k_2 represent how the magnetic flux across the core can be linked from one winding to the other one, these coupling coefficients have a strong geometry dependence and not necessarily are equal, for example in cases of asymmetrical coupling between windings. M can be then expressed in two forms, as seen in Eqs. (5.6) and (5.7). Multiplying these two expressions generate a correspondence of M to L_1, L_2 and the coupling coefficients as seen in Eq. (5.8).

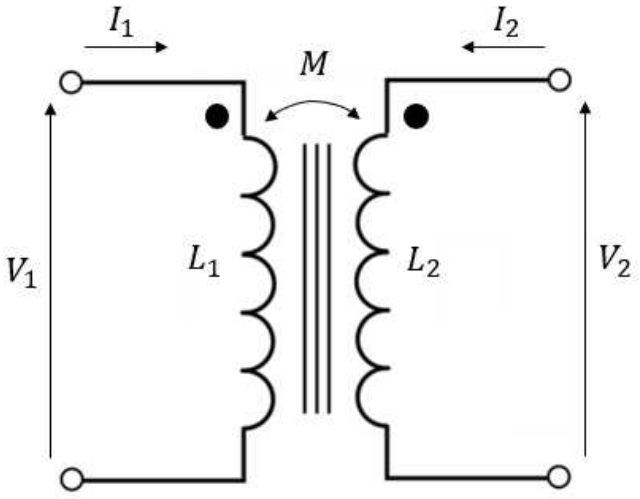


Figure 5.1: Base coupled inductors model of the transformer

$$\begin{aligned} V_1(\omega) &= j\omega L_1 I_1 + j\omega M I_2 \\ V_2(\omega) &= j\omega L_2 I_2 + j\omega M I_1 \\ \begin{bmatrix} V_1(\omega) \\ V_2(\omega) \end{bmatrix} &= j\omega \begin{bmatrix} L_1 & M \\ M & L_2 \end{bmatrix} \begin{bmatrix} I_1(\omega) \\ I_2(\omega) \end{bmatrix} \end{aligned} \tag{5.1}$$

$$L_i = \frac{N_i \phi_i}{I_i}, i = 1{,}2 \tag{5.2}$$

$$M = \frac{N_2\phi_{21}}{I_1} = \frac{N_1\phi_{12}}{I_2} \tag{5.3}$$

$$\phi_{21} = k_1\phi_1 \tag{5.4}$$

$$\phi_{12} = k_2\phi_2 \tag{5.5}$$

$$M = \frac{N_1\phi_{12}}{I_2} = \frac{N_1k_2\phi_2}{I_2} = \frac{N_2}{N_2}\frac{N_1k_2\phi_2}{I_2} = \frac{N_1}{N_2}k_2L_2 \tag{5.6}$$

$$M = \frac{N_2\phi_{21}}{I_1} = \frac{N_2k_1\phi_1}{I_1} = \frac{N_1}{N_1}\frac{N_2k_1\phi_1}{I_1} = \frac{N_2}{N_1}k_1L_1 \tag{5.7}$$

$$\begin{aligned} M^2 &= \frac{N_1}{N_2}k_2L_2\frac{N_2}{N_1}k_1L_1 = k_1k_2L_1L_2 \\ M &= \sqrt{k_1k_2}\sqrt{L_1L_2} = k\sqrt{L_1L_2} \; with \; k = \sqrt{k_1k_2} \end{aligned} \tag{5.8}$$

The fact that a transformer has several possible equivalent networks is possible as long as the proposed network parameters can be linked to the impedance matrix on Eq. (5.1), setting constraints in the value of the components and generating a linkage between models. This is exploited thoroughly in the world of transformer design as a certain equivalent model might be useful in certain situations whereas different models can be counter-intuitive for the application.

The first linear equivalent network proposed serves as an intermediate stage to derive the models used in this work, the topology can be seen in Fig. 5.2. This model is characterized by 3 inductors and an ideal transformer with turns ratio n, which link to the voltages and currents applied to it can be seen in Eq. (5.9). To analyze the two ports voltages, it is necessary to consider the possible reflection of L_μ into the secondary side of the ideal transformer, a concept already introduced in Chapter 3, Section 3.2.2, Fig. 3.13. By analyzing the left-hand side of the circuit, V_1 is affected by the current I_1 flowing through L_a and L_μ, as well as by the current $\frac{I_2}{n}$ flowing through L_μ. The same analysis is done for the right-hand side of the circuit, considering the reflection of L_μ to the secondary side of the ideal transformer. This process is summarized in Eq. (5.10), with Fig. 5.3 showcasing the use of reflection and behavior of the ideal transformer.

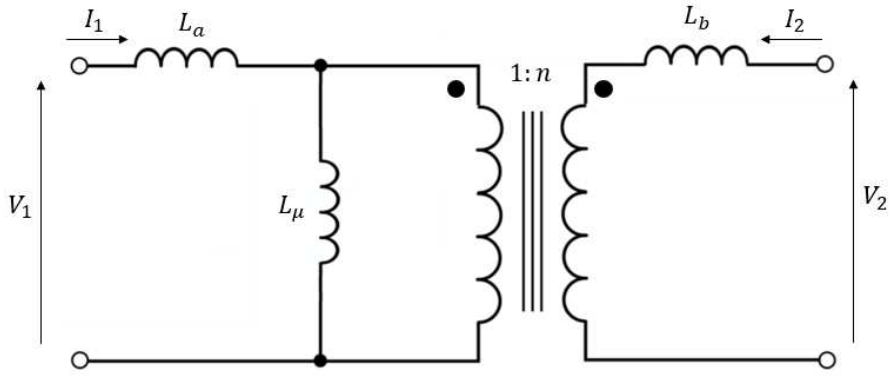


Figure 5.2: Intermediate model of the transformer

$$n = \frac{V_{in}}{V_{out}} = \frac{I_{out}}{I_{in}} \tag{5.9}$$

$$\begin{bmatrix} V_1(\omega) \\ V_2(\omega) \end{bmatrix} = j\omega \begin{bmatrix} L_a + L_\mu & \frac{L_\mu}{n} \\ \frac{L_\mu}{n} & L_b + \frac{L_\mu}{n^2} \end{bmatrix} \begin{bmatrix} I_1(\omega) \\ I_2(\omega) \end{bmatrix} \tag{5.10}$$

For the models to be equivalent, the impedance matrices must be identical, this can be imposed to build a relation between the coupled inductors model parameters L_1, L_2 and M and the intermediate model parameters L_a, L_b, L_μ and n. A forward model is created in Eqs. (5.11), while an inverse model is created in Eqs. (5.12). The proposed model offers a degree of freedom as four parameters are presented for a three parameters model, the selection of this fourth degree of freedom will of course alter the values of the other three to comply with the equalities.

$$\begin{cases} L_1 = L_a + L_\mu \\ M = \dfrac{L_\mu}{n} \\ L_2 = L_b + \dfrac{L_\mu}{n^2} \end{cases} \tag{5.11}$$

$$\begin{cases} L_a = L_1 - nM \\ L_\mu = nM \\ L_b = L_2 - nM \end{cases} \tag{5.12}$$

The selection of the value taken by n defines a new model with altered L_a, L_b and L_μ values. If n is set to represent the real turns ratio implemented physically,

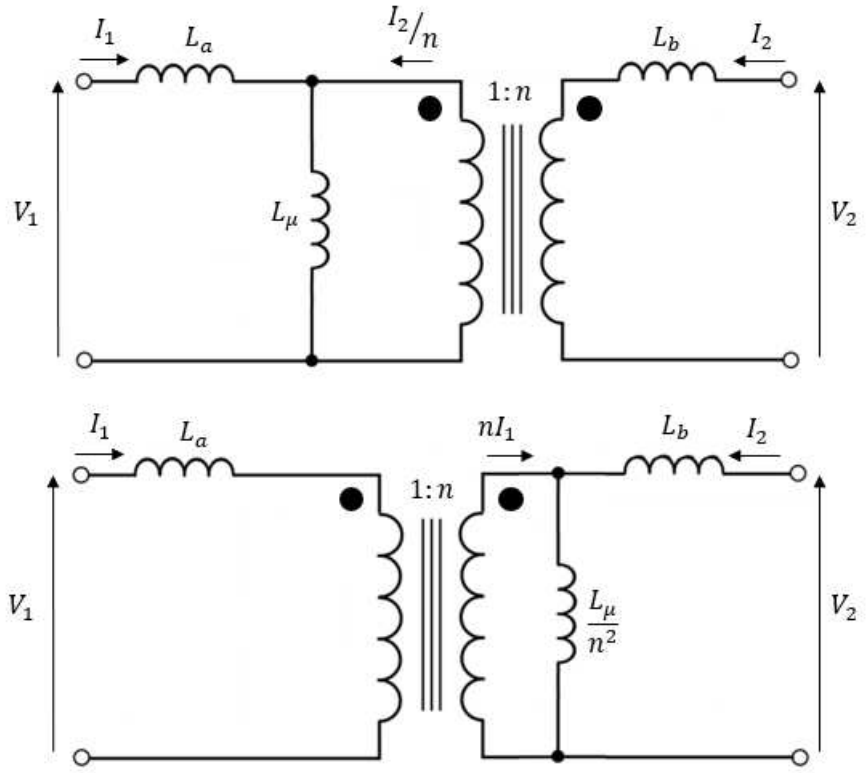


Figure 5.3: Intermediate model analysis visualization

as seen in Eq. (5.13), then the model represents the "Distributed leakage" model of the transformer, seen in Fig. 5.4. Recalling Eqs. (5.6) and (5.7), paired with the forward and inverse models of this proposal in Eqs. (5.14) and (5.15), the altered inverse model can be found for this model in Eq. (5.16). The series inductors represent the leakage inductance of each winding, remarking the "quality" of the flux linkage of each winding. This model is particularly useful for manufacturing, when prototyping a transformer, having access to inductance measurements of each winding can help infer the leakage inductance values.

$$n \equiv n_t = \frac{N_1}{N_2} \tag{5.13}$$

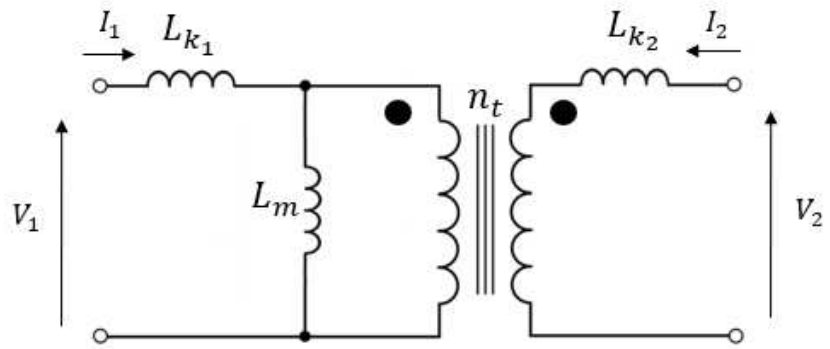


Figure 5.4: Distributed leakage transformer model

$$\begin{cases} L_1 = L_{k_1} + L_m \\ M = \dfrac{L_m}{n_t} \\ L_2 = L_{k_2} + \dfrac{L_m}{n_t^2} \end{cases} \tag{5.14}$$

$$\begin{cases} L_{k_1} = L_1 - n_t M \\ L_m = n_t M \\ L_{k_2} = L_2 - n_t M \end{cases} \tag{5.15}$$

$$\begin{cases} L_{k_1} = L_1 - n_t M = (1 - k_1) L_1 \\ L_m = n_t M = k_1 L_1 \\ L_{k_2} = L_2 - n_t M = (1 - k_2) L_2 \end{cases} \tag{5.16}$$

The model of distributed leakage inductance presents a first opportunity to resemble the LLC topology, if the secondary winding leakage inductance is minimized so that it approaches zero, then the primary winding leakage inductance is associated with the resonating inductor, the magnetizing inductance is associated with the shunt inductor, and the turns ratio is the intrinsic gain of the converter. However, this method requires digging into complex transformer architectures, as it requires implementing asymmetrical coupling between windings so that $k_1 \neq k_2$, with k_1 tending to values lower than one and k_2 tending to one. This behavior can be achieved by careful positioning of windings, in Fig. 5.5 two alternatives for the same transformer core are presented. By working with the air-gap position with respect to the windings, different flux linkage can happen between windings, as illustrated in Fig. 5.6.

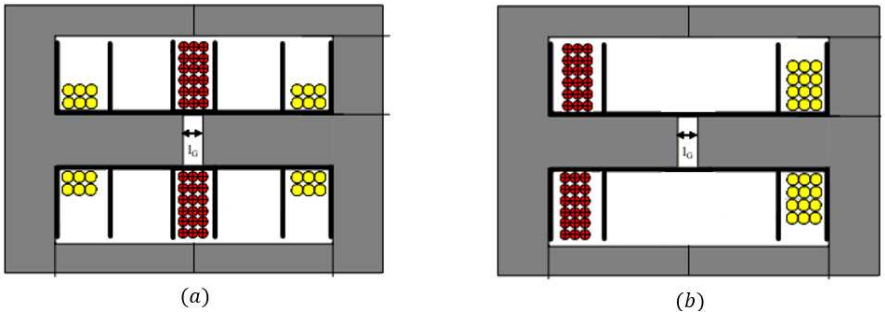


Figure 5.5: Symmetrical and asymmetrical transformer architectures. (a) Asymmetrical flux architecture (b) Symmetrical flux architecture

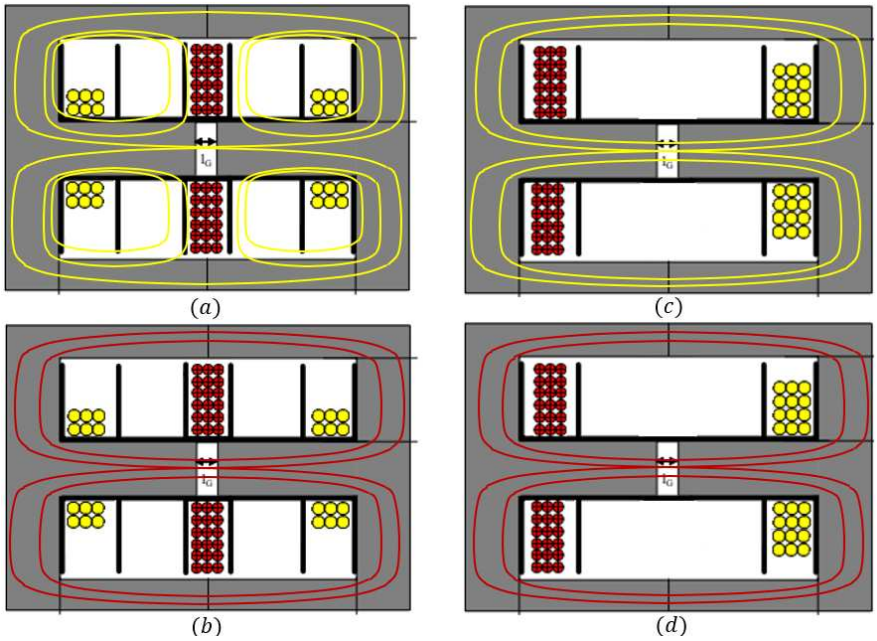


Figure 5.6: Symmetrical and asymmetrical transformer architectures magnetic flux linkage. (a) Asymmetrical architecture, primary to secondary flux linkage (b) Asymmetrical architecture, secondary to primary flux linkage (c) Symmetrical architecture, primary to secondary flux linkage (d) Symmetrical architecture, secondary to primary flux linkage

This work aims to exploit a transformer with symmetrical flux architecture, due to its simplicity of design in comparison with asymmetrical architectures. In this type of topologies with $k_1 = k_2$, both windings present non-null leakage inductance values, which do not align with the LLC topology needs. To force the compliance with the topology, a new model can be proposed by imposing to the "intermediate"

model the condition $L_b = 0$, generating the so called "All Primary Referred" (APR) transformer model, presented in Fig. 5.7. By considering a symmetrical transformer architecture, the previous definitions of M can build a commonly known in the literature relationship between the turns ratio n_t and an inductance ratio, as seen in Eq. (5.17). This expression will be useful for describing the forward and inverse modes of the APR model. The condition for the APR model is imposed in Eq. (5.18), this leads to an intriguing conclusion: since k is less than or equal to one, an LLC resonant power converter requiring a specific turns ratio for its ideal transformer (defining the intrinsic gain) will, in practice, necessitate a lower turns ratio for the actual transformer due to the underlying mathematical relationship. The forward model is described in Eqs. (5.19), while the inverse model is described in Eqs. (5.20)

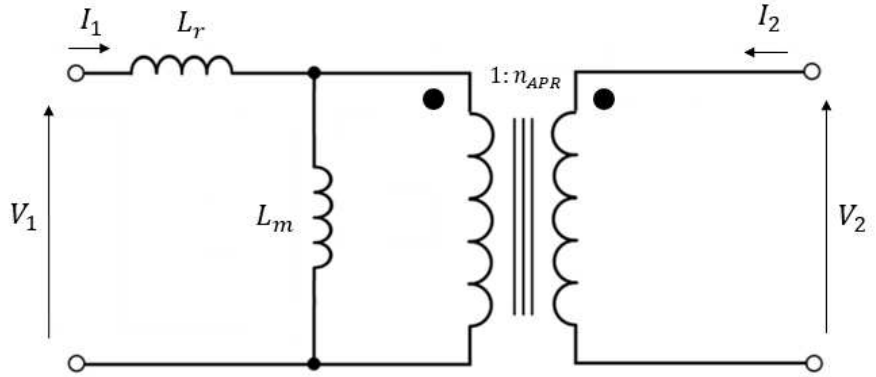


Figure 5.7: All primary referred transformer model

$$\left(M = \frac{N_1}{N_2} k L_2 = n_t k L_2\right) / \left(M = \frac{N_2}{N_1} k L_1 = \frac{1}{n_t} k L_1\right) \equiv 1 = n_t^2 \frac{L_2}{L_1}$$
$$n_t = \frac{N_1}{N_2} = \sqrt{\frac{L_1}{L_2}} \tag{5.17}$$

$$L_b = L_2 - \frac{M}{n_{APR}} = 0$$
$$n_{APR} = \frac{M}{L_2} = \frac{M}{\sqrt{L_2 L_2}} \frac{\sqrt{L_1}}{\sqrt{L_1}} = \frac{M}{\sqrt{L_1 L_2}} \sqrt{\frac{L_1}{L_2}} = k n_t \tag{5.18}$$

$$\begin{cases} L_1 = \dfrac{L_r}{1-k^2} \\ M = \dfrac{L_m}{n_{APR}} \\ L_2 = \dfrac{M}{n_{APR}} = \dfrac{L_m}{n_{APR}^2} \end{cases} \tag{5.19}$$

$$\begin{cases} L_r = L_a = L_1 - n_{APR}M = L_1 - k\sqrt{\dfrac{L_1}{L_2}}k\sqrt{L_1L_2} = (1-k^2)L_1 \\ L_m = L_\mu = n_{APR}M = k^2L_1 \\ n_{APR} = k\sqrt{\dfrac{L_1}{L_2}} \end{cases} \tag{5.20}$$

The importance of having these presented equivalent models for the transformer is their practicality for certain scenarios. The APR model is extremely useful for defining parameters compliant with the resonant power converter topology used. The Distributed leakage model is widely adopted by manufacturers. And the coupled inductors model is the baseline of them all, with a great advantage in the verification process; this model can be easily characterized with three inductance measurements, showcased in Figs. 5.8, 5.9 and 5.10, and mathematically described in Eqs. (5.21), (5.22) and (5.23) respectively.

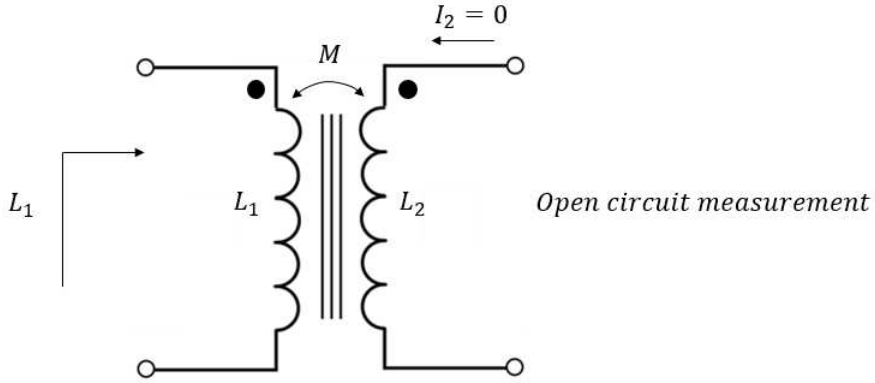


Figure 5.8: Coupled inductors measurement 1, open-circuit secondary

$$V_1 = j\omega(L_1I_1 + MI_2) = j\omega L_1I_1 \Rightarrow Z_{meas} = \frac{V_1}{I_1} = j\omega L_1 \tag{5.21}$$

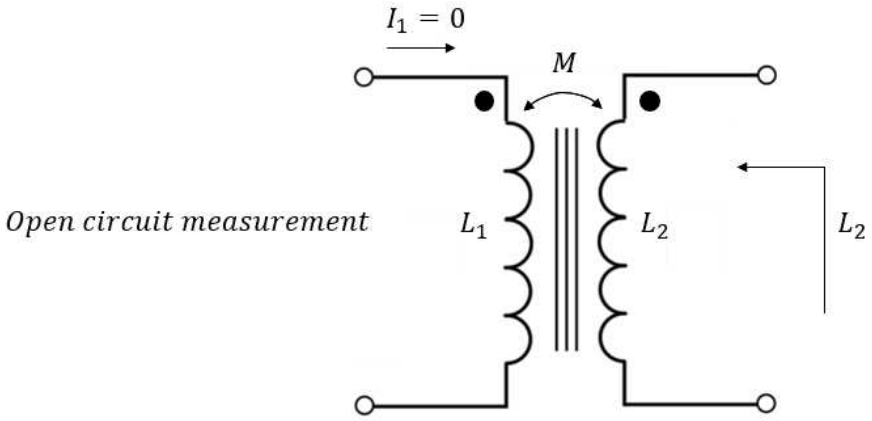


Figure 5.9: Coupled inductors measurement 2, open-circuit primary

$$V_2 = j\omega(MI_1 + L_2I_2) = j\omega L_2 I_2 \Rightarrow Z_{meas} = \frac{V_2}{I_2} = j\omega L_2 \tag{5.22}$$

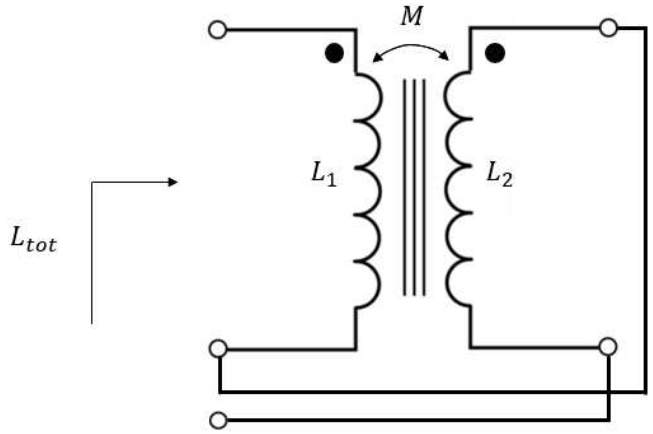


Figure 5.10: Coupled inductors measurement 3, additive series connection

$$\begin{aligned} I_2 = I_1 \Rightarrow Z_{meas} &= \frac{V_1 + V_2}{I_1} = j\omega(L_1 + M + M + L_2) \\ Z_{meas} &= j\omega(L_1 + L_2 + 2M) \\ M &= \frac{\frac{Z_{meas}}{j\omega} - L_1 - L_2}{2} \end{aligned} \tag{5.23}$$

With the introduced framework for the diverse models used in this work, the specific values for each model parameters can be computed using the relationships established in the forward and inverse mathematical descriptions. The only additional consideration is extending the concept to a secondary center-tapped transformer for the first-stage topology. To achieve this, the number of turns on the secondary winding must simply be considered as double that of a full-secondary transformer. For the latter simulation, if the distributed leakage model is to be used, the leakage inductance from the secondary winding can be reflected to the primary. This approach effectively allows the design of a center-tapped transformer by modeling it as a full-secondary transformer to calculate the parameters and then splitting the secondary winding into two equal parts. The parameters derived for the transformer of each stage can be seen in Table 5.1.

Model	**Parameters**	**First stage transformer**	**Second stage transformer**
Coupled inductors	Coupling factor k	0.9173	0.9631
	Self-inductance L_1	71.3 µH	129.38 µH
	Self-inductance L_2	2,160 µH	259.3 µH
	Mutual inductance M	360 µH	176.4 µH
Distributed leakage	Leakage inductance L_{k_1}	5.89 µH	4.77 µH
	Leakage inductance L_{k_2}	178.63 µH	9.57 µH
	Magnetizing inductance L_m	65.4 µH	124.6 µH
	Turns ratio n_t	1:5.5	1:1.416
APR	Series inductance L_r	11.3 µH	9.38 µH
	Magnetizing inductance L_m	60 µH	120 µH
	Virtual turns ratio n_{APR}	1:6	1:1.47

Table 5.1: Transformer models parameters

5.1.2 Transformers design demo

One of the primary objectives of this work is to estimate the efficiency profile of the system, which requires a detailed analysis of the transformer design. The evaluation of transformer losses, as will be discussed in subsequent sections, requires more than

just the target inductance values derived earlier. To support accurate modeling, this section delves into the technical and practical aspects of transformer design, emphasizing the specific considerations required for transformers operating across multiple working points. This analysis will be based strongly on the *Transformer and Inductor Design Handbook* by McLyman [28]. The depth of this topic could easily justify an entire thesis dedicated to inductive components design. As such, the following discussion will prioritize practical implementation, while more advanced approaches, such as Finite Element Modeling, will be reserved for future works.

The initial point to address in transformer design is the wire, specially in high-frequency power conversion systems where diverse noxious effects can make the design challenging. Skin effect is a phenomenon in conductors operating with alternating current, which tends to flow more densely near the surface of the conductor, with the current density decreasing exponentially with depth. This effect is caused by the alternating current itself inducing opposite Eddy currents, which intensity is higher at the center of the conductor. The skin effect can be characterized by the skin depth, defined as the depth below the surface of a wire, where the current density has fallen to 1/e or 37% of its value on the surface. Skin depth can be estimated by the formula stated in Eq. (5.24), which depends on a material factor and frequency of operation. When this formula is applied to the worst cases for each transformer in terms of frequency of operation (maximum), the skin depths seen in Eqs. (5.25) and (5.26) arise. For the current levels in the circuit, a wire sized to handle the current without accounting for the skin effect would experience a significantly reduced effective cross-sectional area, leading to non-compliance and excessive losses to heat, risking the eventual destruction of the device. In high-frequency applications, Litz wire or magnetic wire is used to address this issue. Litz wire subdivides the target conduction area into multiple smaller segments by using multiple isolated strands of thin wire. These thin strands have dimensions that are much closer to the skin depth, effectively mitigating the problem of reduced effective conduction area. Litz wire is standardized using the American Wire Gauge (AWG) convention, which assigns a gauge number corresponding to a specific wire cross-sectional area. A common practice for minimizing the skin effect is to select the wire gauge so the diameter is equal or lower than two times the skin depth, as expressed in Eqs. (5.27) and (5.28). Tables for wire gauge usually express the bare wire area information, the same condition can be expressed in terms of area in Eqs. (5.29) and (5.30). Wire of AWG 40 was employed in simulation for both transformers, with bare wire are of $0.0487 \times 10^{-3}\,\mathrm{cm}^2$, a value much lower than the minimums found. This gauge is selected for its commercial availability, as well as the great minimization of high-frequency losses, avoiding the risk of the transformer lifespan due to thermal management.

$$\delta = \frac{6.62}{\sqrt{f[Hz]}} K \text{ [cm] } with \ K = 1 \ for \ copper \tag{5.24}$$

$$\delta_1 = \frac{6.62}{\sqrt{170000Hz}} = 0.016\text{cm} \tag{5.25}$$

$$\delta_2 = \frac{6.62}{\sqrt{100000Hz}} = 0.021\text{cm} \tag{5.26}$$

$$D_{AWG_1} \leq 2\delta_1 = 0.032\text{cm} \tag{5.27}$$

$$D_{AWG_2} \leq 2\delta_2 = 0.042\text{cm} \tag{5.28}$$

$$A_{W(B)_1} \leq \frac{\pi(2\delta_1)^2}{4} = 0.8042 \times 10^{-4}\,\text{cm}^2 \tag{5.29}$$

$$A_{W(B)_2} \leq \frac{\pi(2\delta_2)^2}{4} = 1.3854 \times 10^{-3}\,\text{cm}^2 \tag{5.30}$$

The second point to address is related to the core saturation, it is known that ferromagnetic materials can support a magnetic flux density B up to a point in which all magnetic domains in the material are already aligned to the magnetic field, in this situation, the magnetic permeability tends to the value of the vacuum magnetic permeability and the material is saturated. The magnetic flux density is defined by the magnetic flux ϕ and the cross area of the transformer A, with the magnetic flux linked to the voltage applied to the magnetizing inductance in relation to Faraday's law, depending on the number of turns linked by the magnetic field, as seen in Eq. (5.31). This relationship will create one of the restricting conditions to the number of turns in the transformer primary to avoid the saturation of the core. The condition will be established at resonance, where the applied voltage waveform across the magnetizing inductance is a square-wave, while later in simulation the maximum magnetic flux density will be verified to remain below saturation at multiple working points, with a method discussed in further sections. The integration of the square-wave with amplitude V_{in} operating at f_{sw} creates a volt-second triangular waveform, as seen in Fig. 5.11. As the voltage has no DC bias, the magnetic flux has null average value, which is extremely important to avoid easy saturation of the core, the value $B(0)$ takes the necessary value to fulfill this scenario. From the waveform knowledge, the restriction on the maximum value for the magnetic flux density can be established in Eq. (5.32).

$$V(t) = N\frac{d\phi(t)}{dt} = NA\frac{dB(t)}{dt} \equiv B(t) = B(0) + \frac{1}{NA}\int_0^t V(t)dt \tag{5.31}$$

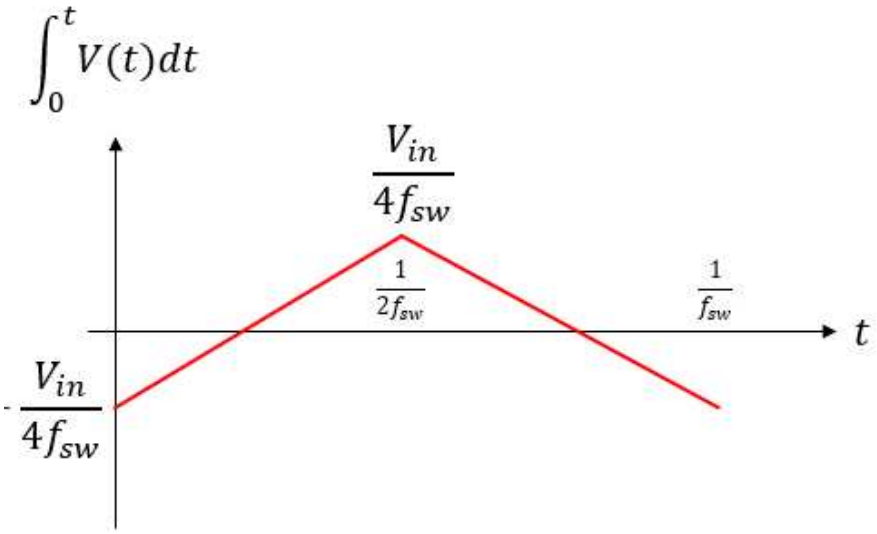


Figure 5.11: Volt-second waveform at the magnetizing inductance

$$B_{max} = \frac{1}{NA}\frac{V_{in}}{4f_{sw}} < B_{sat} \equiv N > \frac{1}{B_{sat}A}\frac{V_{in}}{4f_{sw}} \tag{5.32}$$

The primary winding turns are further constrained by the inductance to be achieved. At this point, it is necessary to introduce information about the particular core to use, for this demo, an ETD 54/28/19 N87 ferrite core from TDK [29] is used, ferrite material is often employed for applications with frequency ranging from 20 kHz to 1 MHz and low saturation magnetic flux densities (<500 mT). This core in particular manufactured with N87 ferrite is intended for applications surrounding 100 kHz. From the datasheet of the manufacturer, the cross-section area can be retrieved $A_e = 280\text{mm}^2$, also the saturating magnetic flux density with value 320 mT, as well as the inductance per squared turns quantity A_L, varying for different air gap values, which application is showcased in Eq. (5.33). Ferromagnetic cores often have high uncertainty on the magnetic permeability of the material; the need for precise inductance values requires the insertion of an air gap, effectively making the air magnetic permeability value dominant. This creates overall lower A_L values, which is equivalent to the need of more turns to achieve a certain inductance value, but with much more certainty that the inductance value in particular will be achieved precisely. The increase in turns helps reducing the

magnetic flux density but also more turns creates more wire length which will create greater copper losses. A_L values for this core are presented in Eqs. (5.34).

$$L = N^2 A_L \tag{5.33}$$

$$\begin{cases} A_L = 4450 + 30/-20\% \text{ nH } (air\ gap = 0\text{mm}) \\ A_L = 1377 \text{ nH } (air\ gap = 0.2\text{mm}) \\ A_L = 670 \text{ nH } (air\ gap = 0.5\text{mm}) \end{cases} \tag{5.34}$$

Due to the wide-input voltage, wide-output power nature of the architecture, the saturation condition can be imposed in multiple working points, where the worst case scenario must be taken into consideration. This condition is applied for the first stage transformer primary winding in Eqs. (5.35) and for the second stage transformer primary winding in Eqs. (5.36). With the values for necessary primary inductance in the previous section, the relationship with the number of turns can be established for the first stage transformer primary winding in Eq. (5.37) and similarly for the second stage in Eq. (5.38). The air-gap distance of the second stage transformer is selected higher to comply better with the saturation condition, a balance was found during the design iteration compromising copper losses with core losses, which will be described in the following sections. In Table 5.2, the conditions for core saturation avoidance and primary winding inductance are summarized, with the exact number of turns for achieving the inductance value being compliant with the saturation minimum turns limitation.

$$\begin{cases} N_1 > \dfrac{1}{0.32T 0.00028m^2} \dfrac{36.5V}{4 * 100kHz} = 1.02 \rightarrow 2 \\ N_1 > \dfrac{1}{0.32T 0.00028m^2} \dfrac{43V}{4 * 175kHz} = 0.68 \rightarrow 1 \end{cases} \tag{5.35}$$

$$\begin{cases} N_1 > \dfrac{1}{0.32T 0.00028m^2} \dfrac{60V}{4 * 30kHz} = 5.58 \rightarrow 6 \\ N_1 > \dfrac{1}{0.32T 0.00028m^2} \dfrac{146V}{4 * 100kHz} = 4.07 \rightarrow 5 \end{cases} \tag{5.36}$$

$$L_1 = N_1^2 A_L(g) \Rightarrow N_1 = \sqrt{\frac{71.3\mu H}{1377nH}} @\ g = 0.2mm \Rightarrow N_1 = 7.2 \rightarrow 7 \tag{5.37}$$

$$L_1 = N_1^2 A_L(g) \Rightarrow N_1 = \sqrt{\frac{129.38\mu H}{670nH}} @\ g = 0.5mm \Rightarrow N_1 = 13.9 \rightarrow 14 \tag{5.38}$$

Condition	First stage primary winding	Second stage primary winding
$N > \frac{1}{B_{sat}A}\frac{V_{in}}{4f_{sw}}$	$N_1 > 2$	$N_1 > 6$
$N_1 = \sqrt{\frac{L_1}{A_L}}$	$N_1 = 7$	$N_1 = 14$

Table 5.2: Primary windings turns restrictions

Finally, in terms of defining the windings turns, the secondary winding is strictly defined from the primary winding number of turns through the turns ratio of the distributed leakage model. In this way, the number of turns of the secondary winding for the first stage transformer can be stated in Eq. (5.39), and similarly for the second stage in Eq. (5.40).

$$N_2 = \frac{N_1}{n_t} = \frac{7}{\frac{1}{5.5}} = 38.5 \rightarrow 39 \tag{5.39}$$

$$N_2 = \frac{N_1}{n_t} = \frac{14}{\frac{1}{1.416}} = 19.82 \rightarrow 20 \tag{5.40}$$

With the number of turns, and the cross-section area of each strand of magnetic wire, a estimation on the number of strands for building the Litz wire can be done. This will further define the DC resistance value that each winding presents, a quantity important to define later the copper losses of the transformer. With the maximum current circulating at each winding, a condition for the number of strands can be stated based on the bare wire area defined by the gauge, and a target current density. A conservative approach in terms of further thermal management is to consider a current density of $300\frac{A}{cm^2}$. The condition can be established in Eq (5.41), while the application to each winding is established in Table 5.3.

$$J \geq \frac{I_{max_{rms}}}{k_{strands}A_{wire}} \Rightarrow k_{strands} \geq \frac{I_{max_{rms}}}{JA_{wire}} \tag{5.41}$$

For the DC resistance value, each strand resistance is calculated, while the overall resistance value of the Litz wire is considered as the parallel of the resistance from the bundle of strands. The definition of each strand resistance is based on the definition of resistance in Eq. (5.42). The length of the wire is complex to take into consideration as each turn diameter depends on how the turns are winded, how many layers are stacked, the addition of insulation layers, etc. As this work intends to do a simplified analysis, the diameter of one turn is considered as the

Winding	**AWG**	**Bare wire area**	**Maximum RMS current**	**Number of strands k**
First stage primary winding	40	$0.0487 * 10^{-3} cm^2$	17.6A	1205
First stage secondary winding	40	$0.0487 * 10^{-3} cm^2$	4.2A	288
Second stage primary winding	40	$0.0487 * 10^{-3} cm^2$	6.28A	430
Second stage secondary winding	40	$0.0487 * 10^{-3} cm^2$	2.14A	147

Table 5.3: Number of strands of magnetic wire for each winding

diameter of the center leg of the transformer, the final length obtained is then raised by a 10% factor to account for miss-estimation. Finally, the resistance value of the pack of strands considered as the parallel of them all is expressed in Eq. (5.43). This resistance value is calculated for each winding in Table 5.4 considering the center-leg geometry of the proposed core, the number of turns and strands calculated for each winding, and the resistivity of copper $\rho = 1.77 * 10^{-8} \Omega m$.

$$R = \rho \frac{l}{A} \tag{5.42}$$

$$R_{DC} = \frac{R}{k_{strands}} = \frac{1}{k_{strands}} \rho \frac{1.1 N \pi D_{center-leg}}{A_{wire}} \tag{5.43}$$

The parameters obtained in this section for the two transformers will be the base for deriving the losses models in the next section, these losses models will be further integrated in the simulation.

After this first approach for the transformers design, collaboration with Italtras SRL allowed for the creating of prototypes for both stages, based on the preliminary analysis. The final iteration for the first stage transformer is composed of a E70 core from TDK, with 5:14:14 windings configuration. For the second stage transformer, a prototype composed of a E70 core from TDK and 14:20 windings configuration was developed. The main inductance measurements at 100 kHz can be found in Tables 5.5 and 5.6, compared to the initial target values.

Winding	**Number of strands k**	**Number of turns N**	R_{DC}
First stage primary winding	1205	7	$1.41m\Omega$
First stage secondary winding	288	39	$32.8m\Omega$
Second stage primary winding	430	14	$7.89m\Omega$
Second stage secondary winding	147	20	$32.98m\Omega$

Table 5.4: DC resistance value for each winding

Quantity	**Initial target (μH)**	**Measured (μH)**
L_1	71.3	76.7
L_2	540	600
L_3	540	599
M_{12}	179	212.9
M_{13}	179	211.4
M_{23}	540	602.5
k_{12}	0.9173 (unit-less)	0.986 (unit-less)
k_{13}	0.9173 (unit-less)	0.979 (unit-less)
k_{23}	1 (unit-less)	0.998 (unit-less)
L_r	11.3	4.7

Table 5.5: Inductance measurements for first stage transformer prototype

Quantity	Initial target (μH)	Measured (μH)
L_1	130	132.44
L_2	265.3	274.6
M	180.66	188.5
k	0.9631 (unit-less)	0.983 (unit-less)
L_r	9.38	7.91

Table 5.6: Inductance measurements for second stage transformer prototype

5.2 Transformer losses

5.2.1 High frequency effects on copper losses

In the previous section, the skin effect was introduced as a factor limiting the effective copper area available for current conduction. Beyond this, the proximity effect arises due to the magnetic fields generated by the currents in neighboring conductors within a winding. These fields induce additional eddy currents, further reducing the effective cross-sectional area of each conductor. As illustrated in Fig. 5.12, the proximity effect becomes particularly significant in the case of Litz wire, where numerous conductors are packed closely together. This effect is enhanced at high frequencies, where it leads to a substantial reduction in effective copper area, increasing winding resistance and thereby amplifying Joule losses [30].

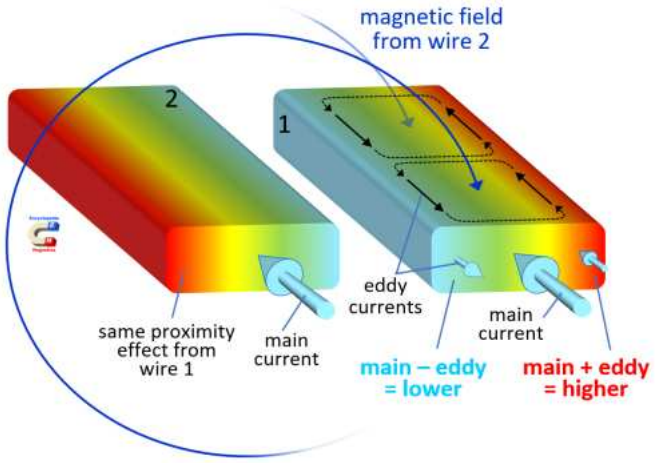


Figure 5.12: Proximity effect between two conductors [30]

Proximity losses are difficult to model and often require specific analysis through finite elements tools. The goal of this section is to estimate this effect with approximations proposed by other authors, while incorporating the capabilities of these models into the simulation, allowing for the simulation of the proximity effect at a wide range of working points (diverse frequencies).

P. L. Dowell proposed in 1966 one of the first methods for characterizing proximity effects in [31]. Nowadays, his model is still employed while variations have emerged out of the base concept. The method is based on the assumptions of 1D magnetic field, as well as orthogonality between losses due to the skin effect and the proximity effect, implying that both can be analyzed separately. By converting the round conductors of a winding into an equivalent uniform amount of foil layers, Dowell simplifies complex spatial calculations of individual conductors. Within each foil (layer), it incorporates the impact of self-induced eddy currents caused by the alternating current in the conductors through the skin depth parameter. It also considers the interaction of magnetic fields between adjacent layers in the winding. These interactions induce additional eddy currents, modifying the current distribution within each layer. The output of this method is a factor describing the ratio between the AC resistance value and the DC resistance value, this is the reason why in the previous section the definition of the DC resistance value would influence the high frequency loss mechanisms in the transformer.

Dowell's model does not account the existence of Litz wire. Wojda extended the concept of Dowell [32] of transforming round wire to foil to transforming Litz wire to foil winding. The Litz wire strands are first rearranged into multi-layer round wires, which can be transformed into the resistance equivalent square wire and finally a foil, as seen in Fig. 5.13. This extension of the Dowell's model is adopted in this work, while more complex other ones exist [32], as shown in Fig. 5.14.

The output of Dowell's model is parameterized by the penetration factor Δ and the number of foil layers N, as shown in Eq. (5.44), with parametric curves displayed in Fig. 5.15. The Wojda modification to the model introduces a modified penetration factor Δ_m, which is calculated based on the type of winding, skin depth and wire geometry, as presented in Table 5.7. In this table, FF represents the fill factor, which is the ratio of the total cross-sectional area of the conductive strands to the overall cross-sectional area of the wire, including insulation. For this work, the fill factor is assumed to be 0.6, typically corresponding to poorly packed Litz wire with significant insulation. Additionally, the number of layers is adjusted to N_{equiv}, taking into account the physical winding layers and the number of strands, as described in Eq. (5.45).

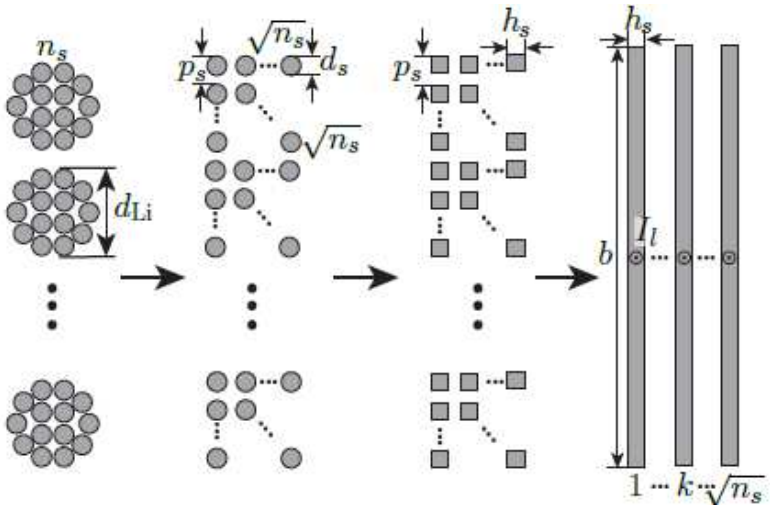


Figure 5.13: Wojda method wire transformation [32]

$$\frac{R_{AC}}{R_{DC}} = \Delta\left(\frac{\sinh(2\Delta)+\sin(2\Delta)}{\cosh(2\Delta)-\cos(2\Delta)} + \frac{2(N^2-1)}{3}\frac{\sinh(\Delta)-\sin(\Delta)}{\cosh(\Delta)+\cos(\Delta)}\right) \tag{5.44}$$

Winding type	**Porosity** η	Δ_m
Foil	1	$\frac{d}{\delta}$
Square wire	$\sqrt{FF}$	$\frac{d}{\delta}\sqrt{\eta}$
Round wire	$\frac{2\sqrt{FF}}{\pi}$	$\left(\frac{\pi}{4}\right)^{0.75}\frac{d}{\delta}\sqrt{\eta}$
Litz wire	$\frac{2\sqrt{FF}}{\pi}$	$\left(\frac{\pi}{4}\right)^{0.75}\frac{d}{\delta}\sqrt{\eta}$

Table 5.7: Wojda modified Δ parameter per winding type

$$N_{equiv} = N_{winding\ layers}\sqrt{k_{strands}} \tag{5.45}$$

Frequency dependence of the model makes it cumbersome to adopt a single value for simulation given that multiple operating frequency values are employed for each stage. The model itself is implemented for every winding through *LTSpice* .param features, as seen in Fig. 5.16, where the final output of the model are the

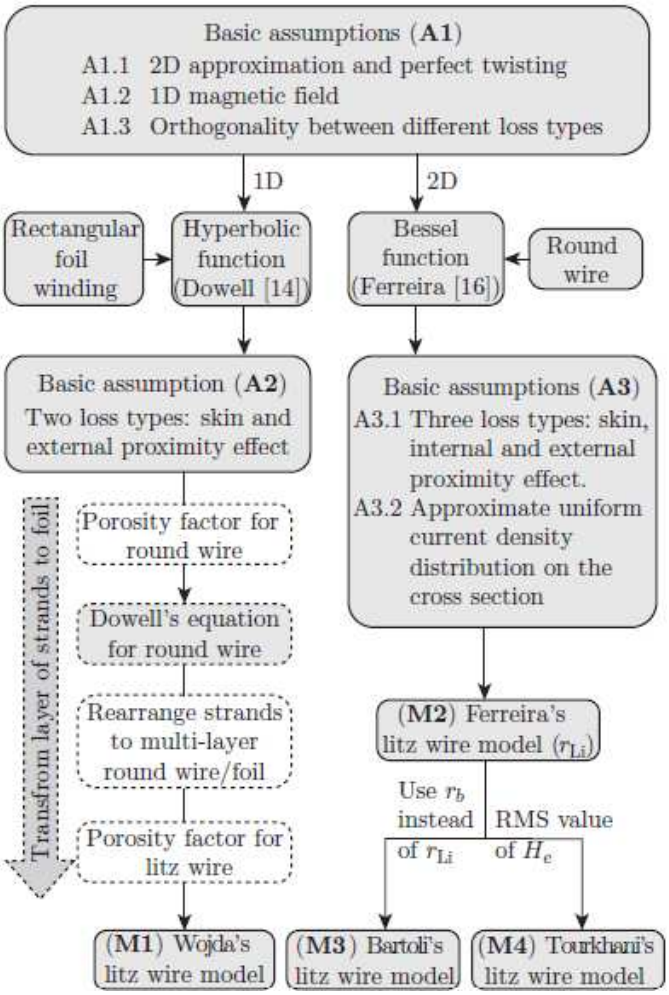


Figure 5.14: Diverse Litz wire models, citations according to references in [32]

constants k_{ij} representing the ratio between AC and DC resistance value. The resistor representing the copper losses is connected in series to each winding of each transformer.

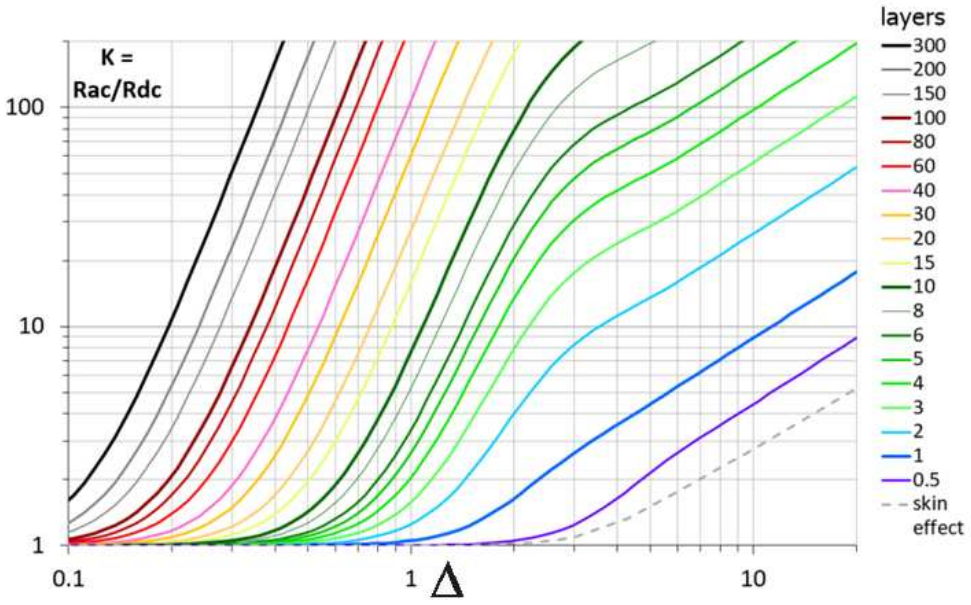


Figure 5.15: Dowell curves for different number of layers

Figure 5.16: *LTSpice* implementation of Dowell/Wojda model

5.2.2 Core losses

The transformer core with high magnetic permeability material is mandatory in the architecture of transformers to confine the magnetic field. This core suffers two types of energy losses driven by different mechanisms [33]:

- Eddy currents are induced in the magnetic material due to the varying magnetic flux crossing its area, the same base concept for transformer operation from Faraday's law is valid for closed curves inside the core, dissipating power through heat according to the resistivity of the material. Technology has minimized this type of losses either through low conductivity materials or through mechanisms as core laminations or compacted powder cores to minimize the possible closed paths across the core cross-sectional area.
- The magnetic flux density B path inside the magnetic core material does not return to its original value when the magnetic field strength, H that applied to magnetized the magnetic material is increased and then decreased back to its original value, generating an hysteresis process.Hysteresis losses arise from the continuous realignment of the magnetic domains within the core material as it cycles between magnetic polarity states. This process requires energy, which is dissipated as heat.

The second type of losses is the dominant in ferrite cores such as N87 material from the selected core in applications of relative high frequency, the first type of losses is negligible given the high resistivity of ferrite material. Hysteresis losses are greater when rising the frequency, as more cycles are developed per second, and they are less significant when the maximum magnetic flux B is minimized. The empirical Steinmetz equation, shown in Eq. (5.46) is often employed to estimate the losses in the core, expressed in power lost per volume unit. The parameters α, β and k, called Steinmetz coefficients, depend on the core material properties. TDK manufacturer allows for the Steinmetz coefficients extraction from their developed tool [34]. The equation proposed by TDK is a variation of Steinmetz equation in incremental form, shown in Eq. (5.47). It is based in the Steinmetz coefficients α, β and k_f, paired with an operating central point described by operating frequency f_b, maximum magnetic flux B_m and associated losses in Watts per set of two cores for those specific working points characterized by the volume of two cores (1 set) multiplied by the $p_{v_{sin}}$ value in Watts per cubic meter. Incremental models work the best in the vicinities of the selected operating central point, so this one is selected accordingly to each stage most likely operation, in this case, the most likely operation working point being at resonant frequency. The parameters are selected equally for both stages as they share the same resonant frequency value, and are summarized in Table 5.8.

$$P_v = k f^{\alpha} B^{\beta} \tag{5.46}$$

$$P_c = k_f V_e p_{v_{sin}} \left(\frac{f}{f_b}\right)^{\alpha} \left(\frac{B}{B_m}\right)^{\beta} \left[\frac{W}{set}\right] \tag{5.47}$$

Parameter	Value
k_f	1
V_e	$3.56 * 10^{-5} m^3$
$p_{v_{sin}}$	$108960 \frac{W}{m^3}$
f_b	100 kHz
B_m	0.1 T
α	1.4768
β	2.5003

Table 5.8: Incremental Steinmetz equation coefficients for selected core at T=40°C

Implementing this power estimation in the simulation is much more complex than the previous copper losses, which AC resistance is calculated at the start of the simulation and kept constant. In this case, the dissipated power dynamically changes with the magnetic flux density waveform. The simulation integration of this expression starts from the already derived magnetic flux density from Faraday's law, recalled in Eq. (5.48), with $v(t)$ being the voltage applied to the magnetizing inductance. This voltage can be measured from the distributed leakage model of the transformer and the magnetic flux density can be calculated in real time expressed as a voltage thanks to the behavioral voltage sources present in *LTSpice*. The challenge is measuring the maximum magnetic flux density in real time, as it is the value necessary for applying the provided expression. This is achieved with a peak detector circuit consisting of a rectifier diode, a capacitor for ripple filtering, and a resistor, the addition of the resistor serves to avoid making an absolute peak detector where the voltage across the capacitor represents the all time peak value, it allows to discharge the capacitor when the magnetic flux density maximum value tends to decrease in time, reverse biasing the diode until the capacitor has discharged through the resistor to the new maximum magnetic flux density. This circuit is fictional and does not represent any functional behavior of the circuit, its

intention is mere measurement. The peak detector circuit can be seen in Fig. 5.17, while Fig. 5.18 showcases the waveforms behavior.

$$B(t) = \frac{1}{NA}\int_0^t v(t)dt \tag{5.48}$$

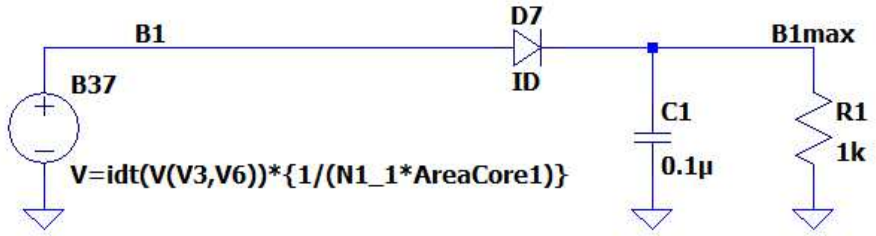


Figure 5.17: Magnetic flux density peak detector in *LTSpice*

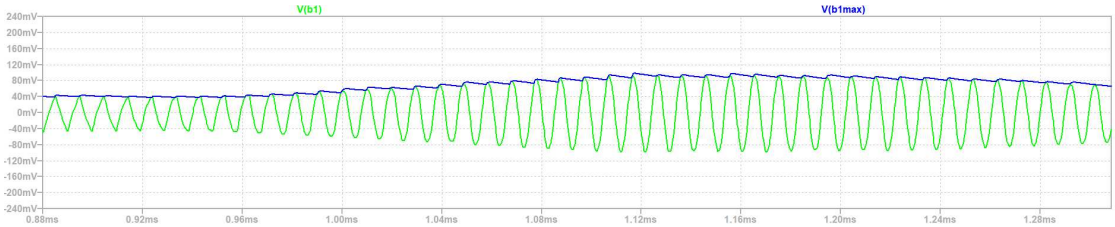


Figure 5.18: Magnetic flux density peak detection showcase. The green curve represents the instantaneous magnetic flux density, while the blue curve indicates the instantaneous maximum value of the green curve

With the instantaneous maximum magnetic flux density value, another behavioral source can be employed to calculate the power loss estimation in the core in real time, as showcased in Fig. 5.19. However, this power estimation is decoupled from the circuit itself, it is not being measured and lost in the circuit. This power loss, although low in most cases, should be due to a real current flowing though the circuit, that would generate losses in other devices. To make a more realistic implementation of this loss, an equivalent resistor that would dissipate this calculated power loss is generated instantaneously with the power loss estimation, through the relationship between voltage and power in Eq. (5.49). The resistor value is then filtered to avoid zero-crossing behaviors that generate divergence of the simulation, as seen in Fig. 5.20. The filtered resistance value is associated with a resistor parallel to the magnetizing inductance, that dynamically changes its value depending on the amount of power it should be "dissipating".

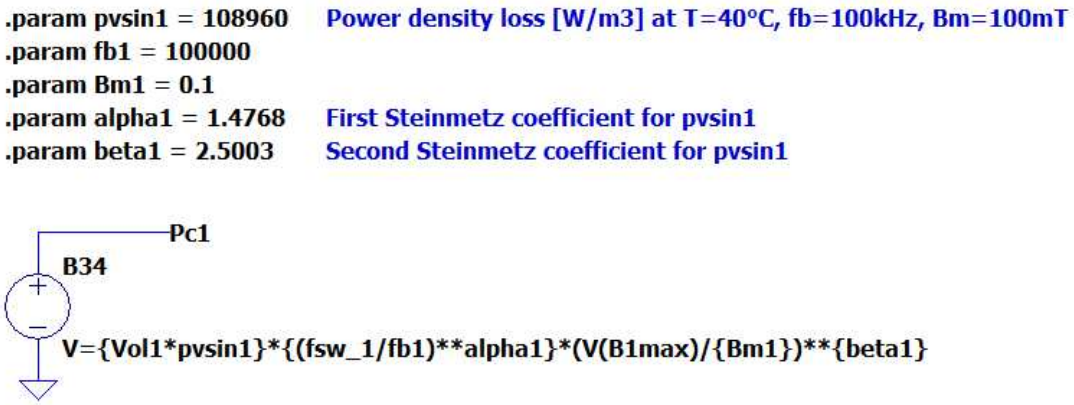


Figure 5.19: Core power loss estimation in *LTSpice*

$$R_{core}(t) = \frac{v^2(t)}{P_{core_{loss}}(t)} \tag{5.49}$$

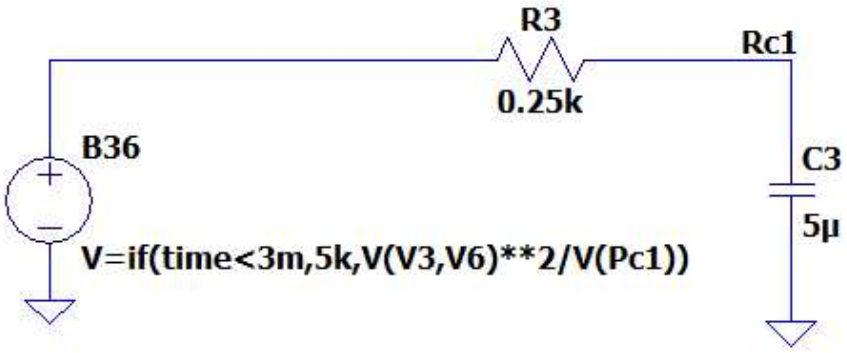


Figure 5.20: Equivalent core loss resistor filtering

Chapter 6

Simulation Analysis

6.1 Simulation Settings and Data Extraction

6.1.1 Component sizing aided by simulation

Due to the complex nature of the proposed architecture with wide range of operation, the selection of the circuit devices was carried out through results of iterative simulation, observing the worst case scenarios in terms of component stress. This process is aided by the tool presented in Chapter 4, Section 4.1.3, where a table of components stress is built automatically from the measure directives from *LTSpice*, further processed by the *MATLAB* script.

For extracting information from the simulation using the output console, the measure directives are employed. These commands are executed at the end of the simulation and can execute different type of operations. The measurements are taken between two time stamps introduced by the user, which in this case are from $t_{end} - \Delta$ to t_{end}, this allows to capture several periods of circuit operation, improving the accuracy of average and root-mean-squared (rms) measurements through coherent sampling; as well as ensuring the real maximum/minimum instantaneous voltage values are captured. An example for the first stage measurements is presented in Fig. 6.1, where T_{end} represents the parameter signaling the amount of time of the entire simulation, while $delta_{meas}$ states the span of time to consider, that was defined to two milliseconds in this case. In terms of voltage breakdown, maximum and minimum instantaneous voltage are measured, and in terms of current, the maximum, minimum and root-mean-squared values are measured. This information is displayed in the console output, and later processed by the *MATLAB* developed script already presented.

Figure 6.1: First stage voltage and current stresses measuring commands

Starting with the inverters switches, the maximum reverse voltage and maximum rms current stresses are summarized in Table 6.1. The selection of the MOSFETs was carried prioritizing low channel on-resistance, to minimize the conduction losses. For the first stage inverter, the STL120N10F8 from STMicroelectronics was selected, and for the second stage inverter, the STB80N20M5 was selected, both of them complying with the maximum presented stresses. Their small channel on-resistance creates a safe scenario for thermal dissipation without the need of heat-sinks, however, their large channel cross-section implies large output capacitance C_{oss} which created a low maximum value for L_m previously. The expressions for the dynamic equivalent capacitance value depending on the input voltage to the stage was found through the previously proposed method, from curve fitting the data from the manufacturer datasheets. The final expressions for the capacitance estimation are stated in Eq. (6.1) for the STL120N10F8, and in Eq. (6.2) for the STB80N20M5. These expressions allow to retrieve the capacitance values employed in the restrictions to L_m developed in a previous chapter.

Parameter	**First stage**	**Second stage**
Maximum reverse voltage	45 V	147 V
Maximum drain-source rms current	11.82 A	3.22 A

Table 6.1: Maximum voltage and current stress of inverters switches

$$C_{eq_{STL120N10F8}} = \frac{1}{V_{in}} \int_0^{V_{in}} \left(2279.4\ e^{-0.2199V} + 1820.1\ e^{-0.0157V}\right) dV \qquad (6.1)$$

$$C_{eq_{STB80N20M5}} = \frac{1}{V_{in}} \int_0^{V_{in}} \left(10146\ e^{-0.1033} + 121.7763\ e^{0.0046V}\right) dV \qquad (6.2)$$

The output diodes from each stage were selected prioritizing low forward voltage drop to maximize efficiency through minimization of their conduction losses. This condition is compromised when selecting devices with large reverse breakdown voltage values. The maximum reverse voltage and maximum rms current stresses for these diodes are summarized in Table 6.2. The STTH30R04-Y diode from STMicroelectronics was selected for both stages, satisfying the worst case limits. It is an ultrafast recovery diode, making the reverse recovery losses at the device turn-off negligible, which is a great advantage at high frequency applications.

Parameter	**First stage**	**Second stage**
Maximum reverse voltage	211 V	285 V
Maximum rms current	4 A	1.5 A

Table 6.2: Maximum voltage and current stress of output diodes

For the resonating network capacitors, the maximum voltage and maximum rms current stresses are summarized in Table 6.3. In Chapter 4, Section 4.2.2, the optimization suggested that decreasing the first stage capacitance would intrinsically improve the quality factor for gain regulation, however, the bottleneck in this approach is technological. As the current value through the capacitor is higher, capacity values tend to be bigger in manufacturer specifications. This is justified by the need of more area in the device to conduct greater currents, which naturally increases the possible capacitance values to achieve. The definitive capacitance value was achieved by the parallel connection of four 56 nF film capacitors from KEMET, realizing an equivalent 224 nF capacitance value, in order to withstand the conduction of the worst-case current value presented in the table. Film capacitors excel at high frequency operation due to their construction assuring low parasitic inductance values as well as low ohmic losses. For the second stage capacitor, the situation is less critical, a 270 nF film capacitor from KEMET is employed for this application, in this case, the capacitance value initially proposed was rounded-up to the first commercially available value, with the reasoning of always tending to lower the quality factor Q as stated in the design chapter. The losses of the two resonating capacitors was modeled in the simulation through the Equivalent Series Resistance (ESR) value stated in the manufacturer datasheet.

Parameter	First stage	Second stage
Maximum voltage	300 V	179 V
Maximum rms current	17 A	4.6 A

Table 6.3: Maximum voltage and current stress of resonating capacitors

For the output "buffering" capacitors, film technology was also considered. The maximum voltage and maximum rms current stresses for them are summarized in Table 6.4. At larger values of capacitance, self-resonance can appear as a considerable problem. The solution in this matter is to either select a capacitor with high self-resonant frequency, or to realize the global capacitance with multiple capacitors in parallel, each one with lower value than the goal, where lower capacitance values are associated to higher self-resonating frequency values. For the first stage capacitor, the R75IW533050H4J of 33 µF from KEMET is selected, while for the second stage capacitor, the B32774H8475K000 of 4.7 µF from TDK is selected, both film capacitors with self-resonance far from the operating frequency range of the system. Their power losses are as well modeled through the ESR values extracted from the manufacturers datasheets.

Parameter	First stage	Second stage
Maximum voltage	105 V	287 V
Maximum rms current	3 A	1.6 A

Table 6.4: Maximum voltage and current stress of output capacitors

6.1.2 Simulation configuration

LTSpice offers powerful tools in terms of simulation accuracy control and measurement methods. The simulation workload for the proposed architecture is high given the magnetic coupling present in both stages, as well as the multiple devices with SPICE models such as the inverter transistors and rectification diodes for each stage. This leads to extreme simulation times and convergence problems with the default configuration of *LTSpice* that must be addressed to allow for practical simulation.

Due to the necessity of iteration in the design, dynamic configuration of the simulation parameters was employed, with two binary selectors for increasing error tolerances in the cases where accuracy is traded off for simulation speed, these selectors and the parameters targeted can be seen in Fig. 6.2. The specific values utilized in the final analysis for efficiency profiles in the following sections are carried on with the simulation configuration summarized in Table 6.5.

SIMULATION PARAMETERS

```
.param deltaMeasMaxs=20us  Defines max and min measurements time span
.param deltaMeas=1ms    Defines average and rms time span for coherent sampling
.param Tend=18ms    Simulation time
.tran 0 {Tend} 0m

.param FasterSimulation=1          .param FasterSimulationx2=0
.options Gmin = {1e-12 + FasterSimulation*9e-12 + FasterSimulationx2*5e-12}
.options Abstol = {1e-12 + FasterSimulation*9e-12 + FasterSimulationx2*5e-12}
.options Reltol = {0.001 + FasterSimulation*0.009 + FasterSimulationx2*0.005}
.options Trtol = 5
.options cshunt=1e-14
.options gshunt=1e-14
```

Figure 6.2: Simulation accuracy controls

Parameter	**Description**	**Value**
Gmin	Conductance connected between every node of the circuit. It improves numerical stability and convergence	$1 * 10^{-11}$
Abstol	The absolute tolerance defines the smallest current difference *LTSpice* considers significant when solving circuit equations	$1 * 10^{-11}$ (default: $1 * 10^{-12}$)
Reltol	The relative tolerance defines the relative error threshold for both voltage and current in the circuit	0.01 (default: 0.001)
Trtol	The transient error tolerance affects the time-step control in transient simulations, it determines how much error *LTSpice* tolerates in the calculated transient solution at each time step	5 (default: 1)
Cshunt	It represents a small parasitic capacitance added across each node to ground, it helps suppress numerical instabilities caused by fast transients.	$1 * 10^{-14}$ (default: 0)
Gshunt	It represents a small parasitic conductance added across each node to ground, it helps improve numerical stability and convergence.	$1 * 10^{-14}$ (default: 0)

Table 6.5: Final simulation parameters values

6.2 Simulation Results

6.2.1 Efficiency results

The analysis of the circuit in terms of efficiency is executed With the tool presented in Chapter 4, Section 4.1.3. In *LTSpice*, this is possible through the measurement of the losses of each device, as well as the measurement of power flow at certain points of interest, gathered through behavioral voltage sources in the simulation performing the power calculation as the multiplication of voltage and current. In Fig. 6.3, the measurement of important power levels to define power flow are presented, while in Fig. 6.4, a demo on how the power loss is measured is given for the first stage inverter devices. These measurements allow to build the efficiency report with the power budget analysis, as well as the power flow Sankey diagram presented previously.

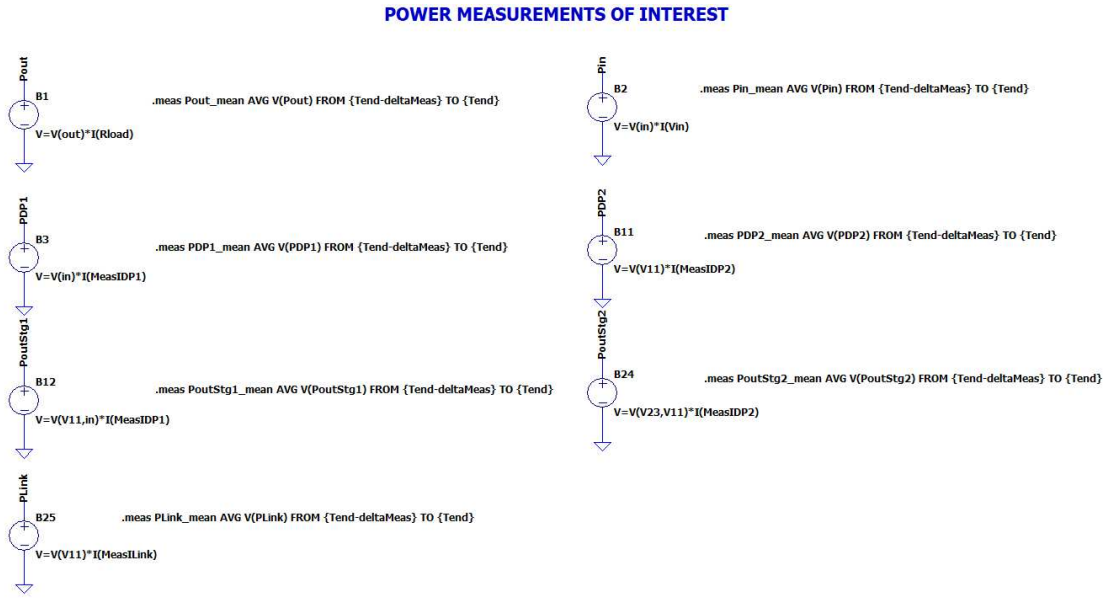


Figure 6.3: Power measurement for power flow analysis

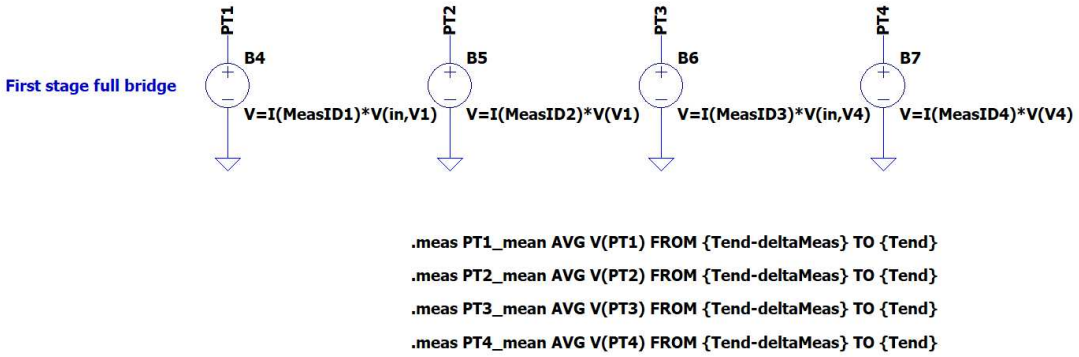
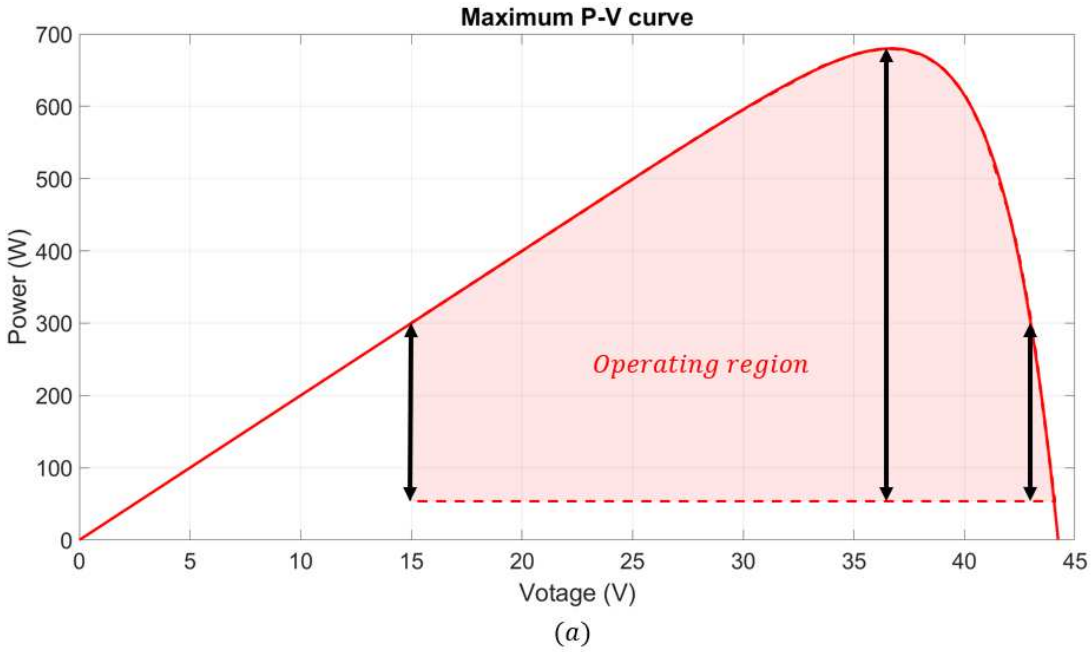
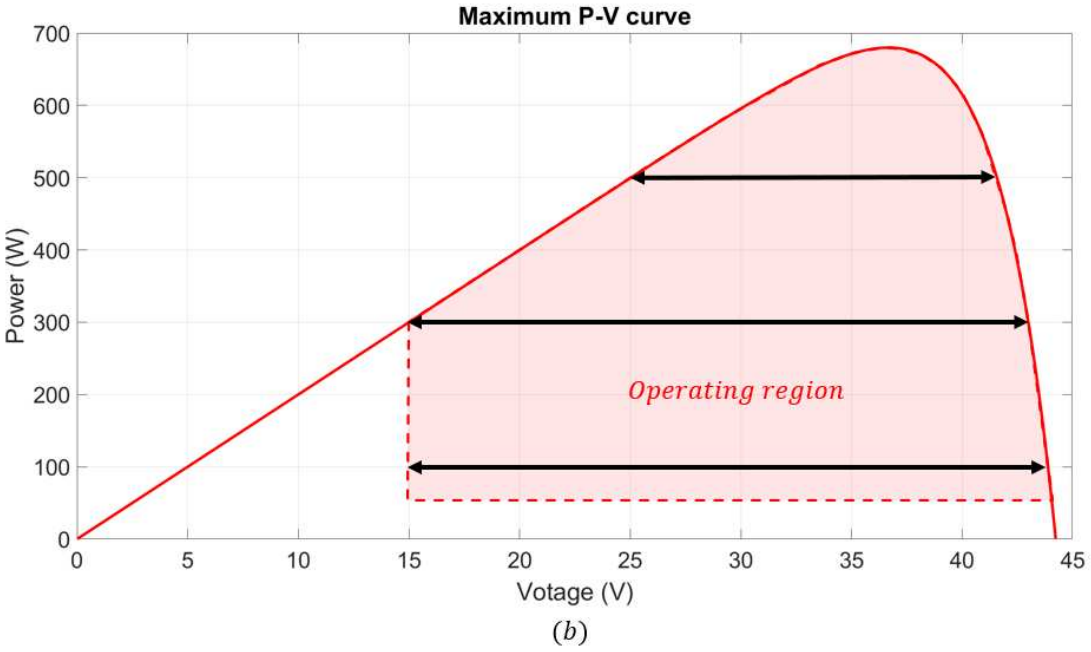


Figure 6.4: Power measurement for power losses. Example with the first stage inverter switches losses

Efficiency curves are built for different sweeps in terms of power and voltage, generating different parametric curves. The selected sweep profiles are shown in Fig. 6.5, overlapped to the maximum power-voltage curve for STC conditions. The efficiency profiles can be seen in Fig. 6.6. It can be seen that the goal of efficiency optimization in the vicinities of the nominal input voltage has been accomplished. It is interesting to notice how the overall efficiency behavior has a monotonic increasing behavior when rising the input voltage, where lower global system gain is needed, enhancing the efficiency boost provided by the architecture power flow nature deriving to the load more power through the highly efficient pass-through converters. In fact, it can be seen that even though the first stage when working at high input voltages lowers its overall efficiency as frequency has to rise to decrease the gain, the system efficiency maintains a high value as the less efficient stage process less power. This can be seen in the power flow diagrams of Fig. 6.7, where for the higher input voltage case the power derived through the pass-through converter rises by 5%.

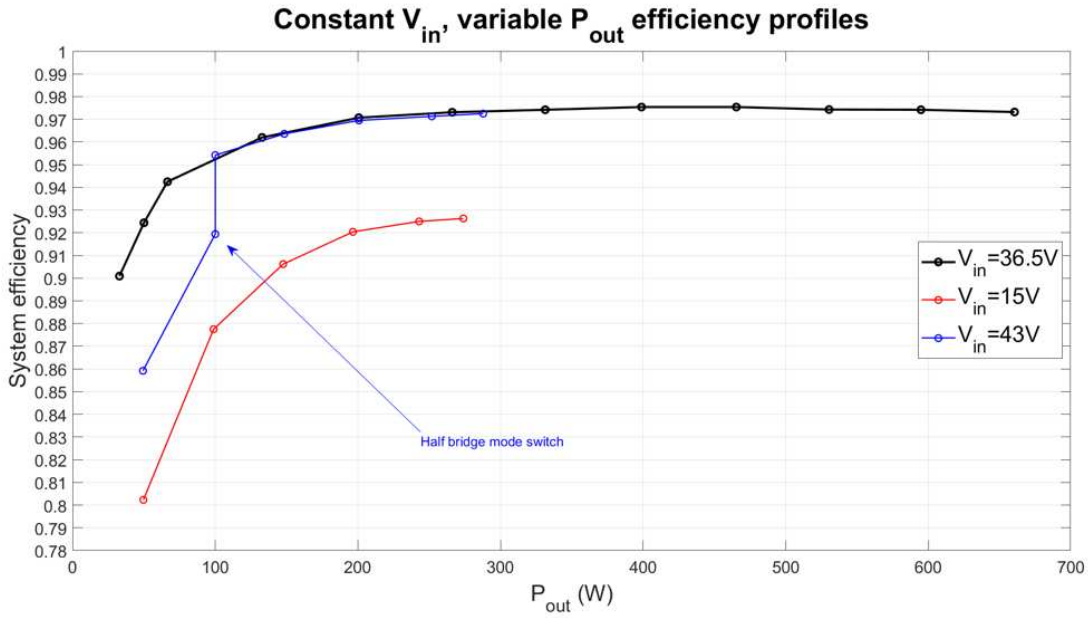


(a)

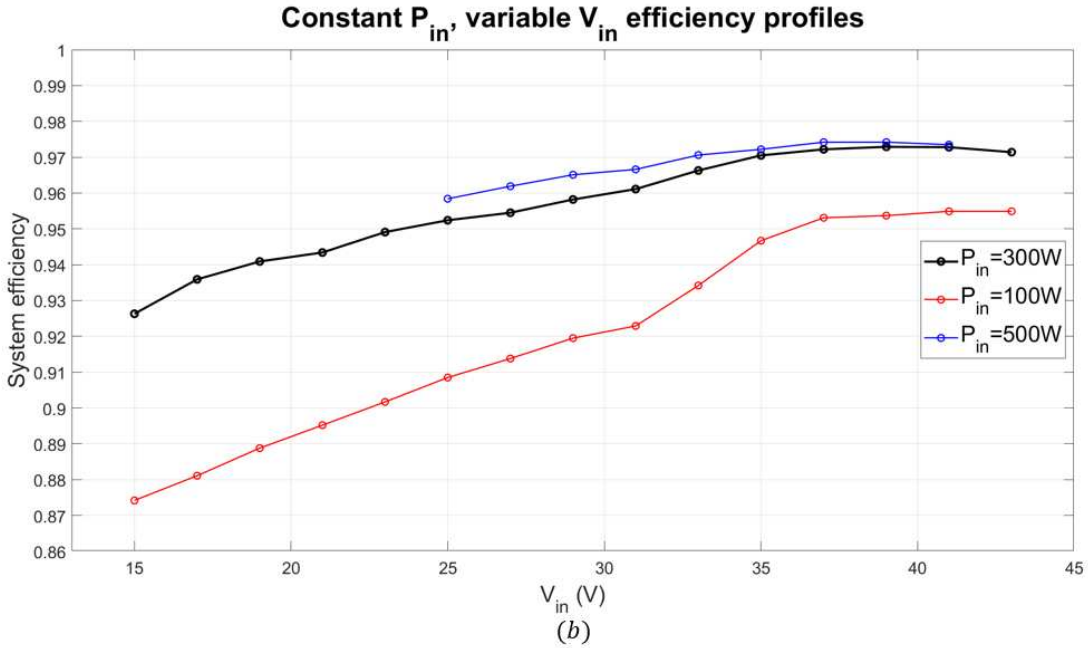


(b)

Figure 6.5: Different voltage and power sweeps. (a) Constant input-voltage, variable input-power. (b) Constant input-power, variable input-voltage



(a)



(b)

Figure 6.6: Efficiency profiles for different voltage and power sweeps. (a) Constant input-voltage, variable input-power. (b) Constant input-power, variable input-voltage

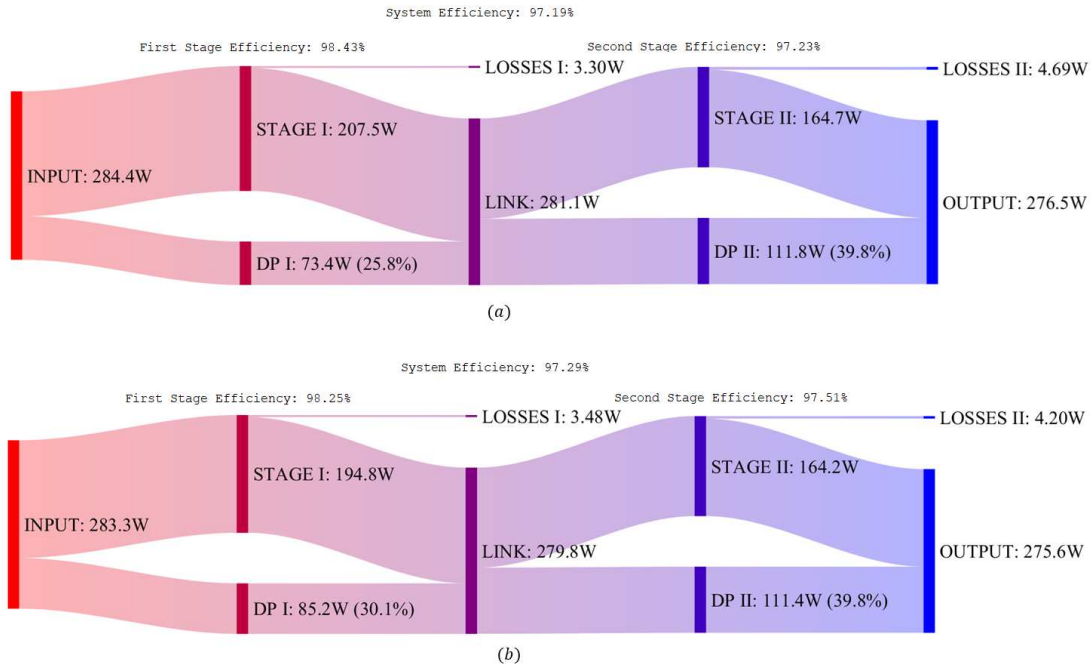


Figure 6.7: Pass-through power flow rise at high input voltage. (a) $V_{in} = 37V,\ P_{in} \approx 285W$. (b) $V_{in} = 43V,\ P_{in} \approx 285W$

In terms of power budget, the nominal input voltage case for maximum power extraction can be seen in Fig. 6.8, where the output diode losses dominate over the other types, except for the second stage were the core losses of the transformer are significant due to the higher voltage level, which leads to higher magnetic flux density values. The power flow for this case can be visualized in Fig. 6.9, it can be seen, with both stages working at resonant gain, that the first stage with higher intrinsic gain delivers less power through the pass-through converter in comparison with the lower intrinsic gain second stage.

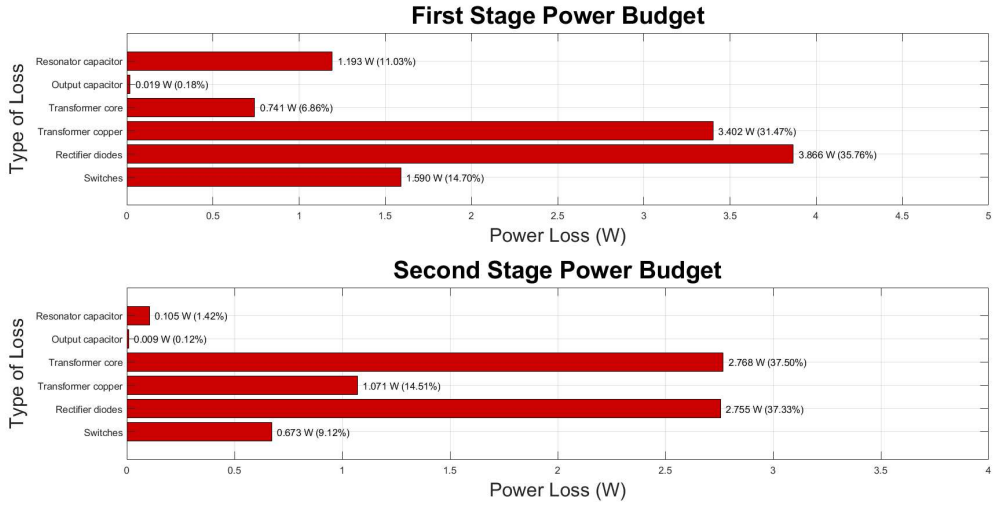


Figure 6.8: Power budget for the nominal input voltage case, extracting maximum power from the system

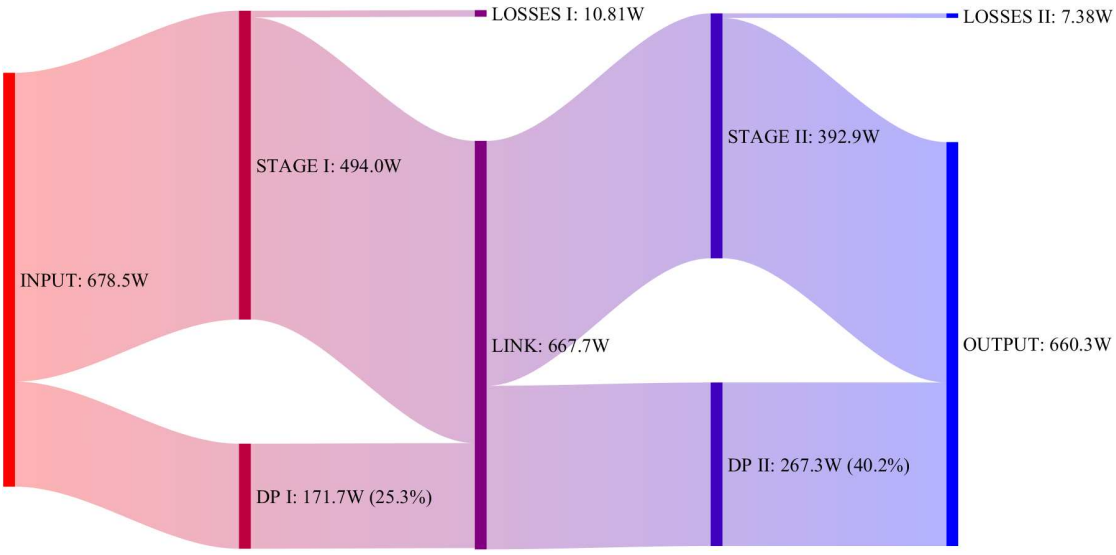


Figure 6.9: Power flow diagram for the nominal input voltage case, extracting maximum power from the system

Overall, at nominal input voltage where efficiency is the most critical, the complete converter operates at efficiency values higher than 97% for power levels above 200 W. The efficiency profile tends to have a flat behavior due to the decoupling of the system efficiency from the stages efficiencies with the highly efficient pass-through converters. In many energy conversion applications, weighted

efficiency value characterizations are performed to evaluate the aspect of efficiency at multiple power extraction points, this is particularly useful when considering systems with highly variable conditions of energy harvest such as photovoltaic applications. The weights described for each efficiency value based on the percentage of nominal output power depend on the historical averages of regional climate [35]. The two weighted efficiencies showcased for this work are the EURO efficiency, proposed by the Joint Research Center (JRC/Ispra), based on the Ispra climate (Italy), and the CEC (California Energy Commission) efficiency, for climates of higher insolations like US south-west regions. The expressions with the weights can be seen in Eqs. (6.3) and (6.4). The evaluation of these efficiency values can be found in Eqs. (6.5) and (6.6).

$$\begin{aligned}\eta_{EURO} = 0.03\eta_{5\%P_{nom}} &+ 0.06\eta_{10\%P_{nom}} + 0.13\eta_{20\%P_{nom}} \\ &+ 0.1\eta_{30\%P_{nom}} + 0.48\eta_{50\%P_{nom}} + 0.2\eta_{100\%P_{nom}}\end{aligned} \tag{6.3}$$

$$\begin{aligned}\eta_{CEC} = 0.04\eta_{10\%P_{nom}} &+ 0.05\eta_{20\%P_{nom}} + 0.12\eta_{30\%P_{nom}} \\ &+ 0.21\eta_{50\%P_{nom}} + 0.53\eta_{75\%P_{nom}} + 0.05\eta_{100\%P_{nom}}\end{aligned} \tag{6.4}$$

$$\begin{aligned}\eta_{EURO} &= 0.03 * 0.9009 + 0.06 * 0.9425 + 0.13 * 0.962 \\ &\quad + 0.1 * 0.9707 + 0.48 * 0.9742 + 0.2 * 0.9732 \\ &= 0.9680 \equiv \boxed{96.80\%}\end{aligned} \tag{6.5}$$

$$\begin{aligned}\eta_{CEC} &= 0.04 * 0.9425 + 0.05 * 0.962 + 0.12 * 0.9707 \\ &\quad + 0.21 * 0.9742 + 0.53 * 0.975 + 0.05 * 0.9732 \\ &= 0.9722 \equiv \boxed{97.22\%}\end{aligned} \tag{6.6}$$

The efficiency results of the proposed architecture are promising and can compete with other proposed solutions to these type of systems. In Table 6.6, a comparison with state of the art solutions for wide input voltage range systems is presented, comparing the accomplished efficiency values and the number of necessary devices.

Table 6.6: Comparison of Step-up Techniques

Reference	[36]	[37]	[38]	[39]	[21]	Proposed
Step-up technique	Voltage Multipliers	LLC	Multi-mode LLC	Topology-morphed LLC	Multi-mode asymmetric IPOS	Quadratic IPOS
Isolation	No	Yes	Yes	Yes	No	No
Number of switches	4	4	5	6	9	8
Number of diodes	7	2	2	7	2	6
Number of magnetic components	6 (ind.)	1 (transf.), 2 (ind.)	1 (transf.), 1 (coupled ind.)	1 (transf.)	1 (transf.), 1 (coupled ind.)	2 (transf.)
Number of capacitors	9	4	5	8	6	4
Rated power	1 kW	500 W	300 W	300 W	750 W	680W
Input voltage range	25 V – 40 V	20 V – 60 V	10 V – 60 V	20 V – 50 V	15 V – 45 V	15 V – 43 V
Min / max efficiency in the voltage range	97.2% – 97.9% (1 kW)	94.5% – 95.6% (300 W)	79% – 97.4% (custom power profile)	94.5% – 95.5% (300 W)	94.6% – 97.1% (300 W, sim.)	92.6% – 97.3% (300 W, sim.)

Chapter 7

Conclusions

This work has proposed the analysis, design, and simulation of a novel DC-DC power converter for photovoltaic applications, exploiting an innovative quadratic architecture with partial power processing. The challenges of working with wide-input voltage range and wide-output power range have been carefully studied through the description of the intricate relationship between load and gain for each of the two stages connected in quadratic form with IPOS configuration.

The simulation results obtained through the extensive use of *LTSpice* and *MATLAB* demonstrate, with a high level of detail in terms of losses modeling, that the proposed architecture is capable of providing high efficiency with a EURO weighed efficiency of 96.8% and CEC weighted efficiency of 97.2%, significant large values considering that these type of weighted efficiency values tend to penalize the converter performance far from the rated power.

Graphical and intuitive tools were developed to facilitate the designer an iterative design method tailored for a Partial Power Processing architecture, with the approach of gain and load profiling that could be extended to other topologies in the context of Partial Power Processing. These developed instruments have been provided through the Appendix for the reader interested in the design of similar architectures, as well as the simulation file for LTSpice to visualize the proposed methods for estimating losses in high frequency power transformers.

Through the development of this work, several doors remain open in terms of possible future trajectories, including:

- DC-AC Converter Design: the proposed converter is non-isolated and lacks load disconnection control. If isolation or disconnection is required, these features should be incorporated into the DC-AC inverter, which could also

handle grid integration.

- Mission Profile-Oriented Design: a design oriented with a specific mission profile could be carried out with the developed tools, including considerations of partial-shading. This could also include an analysis on the dynamics of the circuit, further implementing the control scheme with state of the art solutions such as Maximum Power Point Tracking algorithms.

- Resonant Tank Optimization: a deeper characterization of the resonant tank parameters could move beyond the First Harmonic Approximation, enabling more accurate modeling and the minimization of conduction losses through detailed current waveform analysis. This could also include the modification of the selected resonant frequency and overall switching frequency range.

- Magnetic Design: the physical implementation of the magnetic devices could imply an entire work. An approach for minimizing losses and investigating different methods for controlling the specific inductance values could be proposed, specifically for the leakage inductance.

- Cost Analysis: a detailed cost analysis should be performed to explore the commercial feasibility. With a large amount of devices, including two transformers that tend to be the most expensive component, the interesting achieved efficiency results may be challenged by economic limitations to justify the commercialization of this converter for this particular application.

- Experimental Validation: the experimental prototype, currently in progress, could not be included in the results of this work at the moment of writing this document. In the short future, a comparison between simulated efficiency and losses will be carried out to validate the accuracy of the loss modeling presented in this work.

- Alternative Applications: the proposed architecture could be applied to systems with lower gain requirements in different fields, where the intrinsic efficiency boost could be much stronger. In power converters for low power, where devices losses are critical, a greater by-pass of the stage could increase efficiency considerably. Furthermore, given the low power levels, non-isolation could represent a lower risk to have in such applications.

In conclusion, the proposed power converter has potential in terms of its capabilities to boost efficiency through power flow control. This work offers a baseline for aiding the design of this specific architecture, and it intends to be a contribution to the general methodologies exploited for the design of wide input voltage, wide output power systems with stages gain characteristics sensitive to load variations.

Appendix A

MATLAB code repository

Due to the extensive length of the developed MATLAB scripts, they have been made available in an online GitHub repository. This approach minimizes the inclusion of excessive pages in the thesis, allowing the focus to remain on the most relevant content. Each section of this chapter provides details on accessing the specific code relevant to the discussed topics.

The complete repository is accessible at the following link:

https://github.com/Federicci/Thesis

A.1 Solar panel's curves extraction

This script takes as input the .txt files describing the I-V data points extracted from the "Solar utility tool" from PSIM, to plot the I-V and P-V characteristic of the solar panel.

Code for the script can be found in:

https://github.com/Federicci/Thesis/tree/main/V-I-P-V-Curves

A.2 Gain and load profiling tool

This script takes as input the .txt files describing the I-V data points extracted from the "Solar utility tool", and requires the input from the user for the gain

profiles and component values for analyzing the system loading profiles and the subsequent gain profiles feasibility.

Code for the script can be found in:

https://github.com/Federicci/Thesis/tree/main/GainLoadAnalysis

A.3 LTSpice output processing

This script takes as input the .txt file containing the console output from LTSpice, to process it into the efficiency analysis, power budget report and voltage and current stress report. It relies on the functions developed in [24].

Code for the script can be found in:

https://github.com/Federicci/Thesis/tree/main/PowerBudgetAnalysis

A.4 First stage output capacitor charge analysis

This script executes the necessary numerical analysis to find the worst case scenario for the voltage ripple of the first stage output capacitor.

Code for the script can be found in:

https://github.com/Federicci/Thesis/tree/main/FirstStageCapacitorCharge

Appendix B

FHA transfer function manipulation

The figures of merit to be utilized are:

$$\begin{aligned} Q &= \frac{\sqrt{\frac{L_r}{C_r}}}{R_{ac}} \rightarrow Quality\ factor \\ f_r &= \frac{1}{2\pi\sqrt{L_r C_r}} \rightarrow Resonant\ frequency \\ F_x &= \frac{f_{sw}}{f_r} \rightarrow Normalized\ switching\ frequency \\ m &= \frac{L_r + L_m}{L_r} \rightarrow Inductance\ ratio \end{aligned} \tag{B.1}$$

Continuing over the first step proposed in this work:

$$\left|\frac{v_{o_{ac}}(j\omega)}{v_{in}(j\omega)}\right| @\omega_{sw} = \left|\frac{\frac{R_{ac}j\omega_{sw}L_m}{R_{ac}+j\omega_{sw}L_m}}{\frac{R_{ac}j\omega_{sw}L_m}{R_{ac}+j\omega_{sw}L_m} + j\omega_{sw}L_r + \frac{1}{j\omega_{sw}C_r}}\right| \tag{B.2}$$

Working the repeated fraction:

$$\begin{aligned}\frac{R_{ac}j\omega_{sw}}{R_{ac}+j\omega_{sw}} &= \frac{jF_x\omega_r L_m\frac{\sqrt{\frac{L_r}{C_r}}}{Q}}{jF_x\omega_r L_m+\frac{\sqrt{\frac{L_r}{C_r}}}{Q}} * \frac{Q}{Q} \\ &= \frac{jF_x\frac{1}{\sqrt{C_rL_r}}L_m\sqrt{\frac{L_r}{C_r}}}{jQF_x\omega_r L_m+\sqrt{\frac{L_r}{C_r}}} \\ &= \frac{jF_x\frac{L_m}{C_r}}{jQF_x\omega_r L_m+\sqrt{\frac{L_r}{C_r}}}\end{aligned} \tag{B.3}$$

Reintroducing this fraction into the principal expression:

$$\begin{aligned}\left|\frac{v_{o_{ac}}(j\omega)}{v_{in}(j\omega)}\right|@\omega_{sw} &= \left|\frac{jF_x\frac{L_m}{C_r}}{jF_x\frac{L_m}{C_r}+\left(jQF_x\omega_r L_m+\sqrt{\frac{L_r}{C_r}}\right)jF_x\omega_r L_r+\left(jQF_x\omega_r L_m+\sqrt{\frac{L_r}{C_r}}\right)\frac{1}{jF_x\omega_r C_r}}\right| \\ &= \left|\frac{jF_x\frac{L_m}{C_r}}{jF_x\frac{L_m}{C_r}+j^2QF_x^2\omega_r^2L_mL_r+j\sqrt{\frac{L_r}{C_r}}F_x\omega_r L_r+\frac{QF_x\omega_r L_m}{F_x\omega_r C_r}-j\frac{1}{F_x\omega_r C_r}\sqrt{\frac{L_r}{C_r}}}\right| \\ &= \left|\frac{jF_x\frac{L_m}{C_r}}{jF_x\frac{L_m}{C_r}-QF_x^2\frac{1}{C_rL_r}L_mL_r+j\sqrt{\frac{L_r}{C_r}}F_x\sqrt{\frac{1}{C_rL_r}}L_r+Q\frac{L_m}{C_r}-j\frac{\sqrt{C_rL_r}}{F_xC_r}\sqrt{\frac{L_r}{C_r}}}\right| \\ &= \left|\frac{jF_x\frac{L_m}{C_r}}{jF_x\frac{L_m}{C_r}-QF_x^2\frac{L_m}{C_r}+jF_x\frac{L_r}{C_r}+Q\frac{L_m}{C_r}-j\frac{L_r}{F_xC_r}} * \frac{\frac{C_r}{L_m}}{\frac{C_r}{L_m}}\right| \\ &= \left|\frac{jF_x}{jF_x-QF_x^2+jF_x\frac{L_r}{L_m}+Q-j\frac{1}{F_x}\frac{L_r}{L_m}} * \frac{\frac{L_m}{L_r}}{\frac{L_m}{L_r}}\right|\end{aligned} \tag{B.4}$$

The definition of m can be exploited:

$$m=\frac{L_r+L_m}{L_r} \Rightarrow m-1=\frac{L_m}{L_r} \tag{B.5}$$

Then:

$$\begin{aligned}
\left|\frac{v_{o_{ac}}(j\omega)}{v_{in}(j\omega)}\right| @\omega_{sw} &= \left|\frac{jF_x(m-1)}{jF_x(m-1) - QF_x^2(m-1) + jF_x + Q(m-1) - j\frac{1}{F_x}} * \frac{F_x}{F_x}\right| \\
&= \left|\frac{jF_x^2(m-1)}{jF_x^2(m-1) - QF_x^3(m-1) + jF_x^2 + QF_x(m-1) - j}\right| \\
&= \left|\frac{jF_x^2(m-1)}{QF_x(m-1)(1-F_x^2) + j(F_x^2 m - 1)}\right| \\
&= \boxed{\frac{F_x^2(m-1)}{\sqrt{Q^2F_x^2(m-1)^2(1-F_x^2)^2 + (F_x^2 m - 1)^2}}}
\end{aligned} \tag{B.6}$$

Bibliography

[1] REN21. *Global Status Report 2024: Energy Supply - Global Trends*. Accessed: 2024-09-12. 2024. URL: https://www.ren21.net/gsr-2024/modules/energy_supply/01_global_trends/ (cit. on pp. 1, 2).

[2] Our World in Data. *Levelized Cost of Energy (LCOE)*. Accessed: 2024-12-12. 2023. URL: https://ourworldindata.org/grapher/levelized-cost-of-energy?time=earliest..2023&facet=none (cit. on p. 2).

[3] Our World in Data. *Learning Curve: Cost reductions in clean energy technologies*. Accessed: 2025-07-01. 2024. URL: https://ourworldindata.org/learning-curve (cit. on p. 2).

[4] Samir Kouro, Jose I. Leon, Dimitri Vinnikov, and Leopoldo G. Franquelo. «Grid-Connected Photovoltaic Systems: An Overview of Recent Research and Emerging PV Converter Technology». In: *IEEE Industrial Electronics Magazine* 9.1 (2015), pp. 47–61. DOI: 10.1109/MIE.2014.2376976 (cit. on p. 3).

[5] Altair. *PSIM Simulation Software*. https://www.powersimtech.com/. Version 2024 (cit. on p. 5).

[6] MathWorks. *MATLAB*. https://www.mathworks.com. Version R2024a (cit. on p. 5).

[7] Analog Devices. *LTSpice*. https://www.analog.com/en/resources/design-tools-and-calculators/ltspice-simulator.html. Version 2024 (cit. on p. 5).

[8] Constantin Pica, Radu Munteanu, Sorin Pavel, and Horia Beleiu. «Modeling of Photovoltaic Panels». In: *2018 International Conference and Exposition on Electrical And Power Engineering (EPE)*. 2018, pp. 0769–0773. DOI: 10.1109/ICEPE.2018.8559884 (cit. on p. 7).

[9] Antony Xenophontos and Ali M. Bazzi. «Analytical modeling of PV maximum power curves under uniform and partial shading conditions». In: *2014 IEEE 40th Photovoltaic Specialist Conference (PVSC)*. 2014, pp. 1982–1986. DOI: 10.1109/PVSC.2014.6925314 (cit. on p. 8).

[10] 3SUN. *3SUN B60 Solar Panel Datasheet*. URL: https://www.3sun.com/content/dam/threesun/documents/technical/3SUN_B60_file.pdf (cit. on p. 10).

[11] Khalil Alluhaybi, Issa Batarseh, and Haibing Hu. «Comprehensive Review and Comparison of Single-Phase Grid-Tied Photovoltaic Microinverters». In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 8.2 (2020), pp. 1310–1329. DOI: 10.1109/JESTPE.2019.2900413 (cit. on pp. 13–15).

[12] David M. Scholten, N. Ertugrul, and W. L. Soong. «Micro-inverters in small scale PV systems: A review and future directions». In: *2013 Australasian Universities Power Engineering Conference (AUPEC)*. 2013, pp. 1–6. DOI: 10.1109/AUPEC.2013.6725465 (cit. on pp. 14, 15).

[13] Jon Anzola, Iosu Aizpuru, Asier Arruti Romero, Argiñe Alacano Loiti, Ramon Lopez-Erauskin, Jesús Sergio Artal-Sevil, and Carlos Bernal. «Review of Architectures Based on Partial Power Processing for DC-DC Applications». In: *IEEE Access* 8 (2020), pp. 103405–103418. DOI: 10.1109/ACCESS.2020.2999062 (cit. on p. 16).

[14] O. Gsous, R. Rizk, A. Barbón, and R. Georgious. «Review of DC-DC Partial Power Converter Configurations and Topologies». In: *Energies* 17.6 (2024), p. 1496. DOI: 10.3390/en17061496. URL: https://doi.org/10.3390/en17061496 (cit. on p. 17).

[15] Baoxing Chen. *Integration of Isolation for Grid-Tied Photovoltaic Inverters*. Accessed: 2024-18-12. 2012. URL: https://www.analog.com/en/resources/technical-articles/integration-of-isolation-for-grid-tied-photovoltaic-inverters.html (cit. on p. 21).

[16] Roberto Gonzalez, Eugenio Gubia, JesÚs Lopez, and Luis Marroyo. «Transformerless Single-Phase Multilevel-Based Photovoltaic Inverter». In: *IEEE Transactions on Industrial Electronics* 55.7 (2008), pp. 2694–2702. DOI: 10.1109/TIE.2008.924015 (cit. on p. 22).

[17] Yueshi Guan, Carlo Cecati, J. Marcos Alonso, and Zhe Zhang. «Review of High-Frequency High-Voltage-Conversion-Ratio DC–DC Converters». In: *IEEE Journal of Emerging and Selected Topics in Industrial Electronics* 2.4 (2021), pp. 374–389. DOI: 10.1109/JESTIE.2021.3051554 (cit. on p. 29).

[18] Sadeq Ali Qasem Mohammed and Jin-Woo Jung. «A State-of-the-Art Review on Soft-Switching Techniques for DC–DC, DC–AC, AC–DC, and AC–AC Power Converters». In: *IEEE Transactions on Industrial Informatics* 17.10 (2021), pp. 6569–6582. DOI: 10.1109/TII.2021.3058218 (cit. on p. 32).

[19] Qi Cao, Zhiqing Li, and Haoyu Wang. «Wide Voltage Gain Range LLC DC/DC Topologies: State-of-the-Art». In: *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*. 2018, pp. 100–107. DOI: 10.23919/IPEC.2018.8507899 (cit. on pp. 33, 49).

[20] Xiang Fang, Haibing Hu, Z. John Shen, and Issa Batarseh. «Operation Mode Analysis and Peak Gain Approximation of the LLC Resonant Converter». In: *IEEE Transactions on Power Electronics* 27.4 (2012), pp. 1985–1995. DOI: 10.1109/TPEL.2011.2168545 (cit. on p. 33).

[21] S. Cerutti, M. Pavone, F. Gennaro, N. Aiello, F. Musolino, and P. Crovetti. «Design of a Multi-Mode Input-Parallel-Output-Series Power Optimizer for Wide-Voltage Range Photovoltaic Applications». In: *2024 IEEE Energy Conversion Congress & Exposition (ECCE)*. 2024, pp. 444–451 (cit. on pp. 37, 77, 130).

[22] S. De Simone, C. Adragna, C. Spini, and G. Gattavari. «Design-oriented steady-state analysis of LLC resonant converters based on FHA». In: *International Symposium on Power Electronics, Electrical Drives, Automation and Motion, 2006. SPEEDAM 2006.* 2006, pp. 200–207. DOI: 10.1109/SPEEDAM.2006.1649771 (cit. on p. 41).

[23] Francesco Musolino and Stefano Cerutti. *Advanced Electronic Drives*. Course notes, Politecnico di Torino. Lecture course. 2024 (cit. on p. 53).

[24] Zhaoxu Liu. *Sankey Plot tool for MATLAB*. https://it.mathworks.com/matlabcentral/fileexchange/128679-sankey-plot. 2023 (cit. on pp. 66, 134).

[25] Yuqi Wei, Thiago Pereira, Yiwei Pan, Marco Liserre, Frede Blaabjerg, and H. Alan Mantooth. «A General and Automatic RMS Current Oriented Optimal Design Tool for LLC Resonant Converters». In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 10.6 (2022), pp. 7318–7332. DOI: 10.1109/JESTPE.2022.3163051 (cit. on p. 73).

[26] Robert W. Erickson and Dragan Maksimović. *Fundamentals of Power Electronics*. 3rd. Cham: Springer, 2020 (cit. on p. 81).

[27] Claudio Adragna. *A Primer To Transformers And Coupled Inductors Modeling*. Mar. 2007. DOI: 10.13140/RG.2.2.17208.57600 (cit. on p. 90).

[28] D. F. McLyman. *Transformers and Inductors Design Handbook*. 4th. Boca Raton, FL: CRC Press, 2020. ISBN: 978-0367337401 (cit. on p. 100).

[29] TDK. *TDK ETD54/28/19 core Datasheet*. URL: https://www.tdk-electronics.tdk.com/inf/80/db/fer/etd_54_28_19.pdf (cit. on p. 102).

[30] e-Magnetica. *Proximity Effect*. 2023. URL: https://www.e-magnetica.pl/doku.php/proximity_effect (cit. on p. 107).

[31] P. L. Dowell. «Effects of Eddy Currents in Transformer Windings». In: *Proceedings of the Institution of Electrical Engineers* 113.8 (1966), pp. 1387–1394. DOI: 10.1049/piee.1966.0236 (cit. on p. 108).

[32] Qingchao Meng and Jürgen Biela. «Survey and Comparison of 1D/2D analytical Models of HF Losses in Litz Wire». In: *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*. 2020, P.1–P.11. DOI: 10.23919/EPE20ECCEEurope43536.2020.9215651 (cit. on pp. 108–110).

[33] Syafruddin Hasan, Soib Taib, Surya Hardi, A. Rahim A.R, and Ahmad Shukri. «Core loss characteristics analysis of power transformer under different frequencies excitation». In: *2013 IEEE 7th International Power Engineering and Optimization Conference (PEOCO)*. 2013, pp. 619–623. DOI: 10.1109/PEOCO.2013.6564622 (cit. on p. 113).

[34] TDK. *TDK magnetic design tool*. URL: https://www.tdk-electronics.tdk.com/en/180490/design-support/design-tools/ferrite-magnetic-design-tool (cit. on p. 113).

[35] PVSyst. *Definition of the European Efficiency for Inverters*. n.d. URL: https://www.pvsyst.com/help-pvsyst7/inverter_euroeff.htm (cit. on p. 129).

[36] Haodong Lei, Ruixiang Hao, Xiaojie You, and Fang Li. «Nonisolated High Step-Up Soft-Switching DC–DC Converter With Interleaving and Dickson Switched-Capacitor Techniques». In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 8.3 (2020), pp. 2007–2021. DOI: 10.1109/JESTPE.2019.2958316 (cit. on p. 130).

[37] Saeed Pourjafar, Parham Mohseni, Oleksandr Matiushkin, Oleksandr Husev, and Dmitri Vinnikov. «Novel Isolated High Step-up DC-DC Converter with Wide Input Voltage Regulation Range». In: *2023 IEEE 64th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)*. 2023, pp. 1–6. DOI: 10.1109/RTUCON60080.2023.10413102 (cit. on p. 130).

[38] Dmitri Vinnikov, Andrii Chub, Elizaveta Liivik, and Indrek Roasto. «High-Performance Quasi-Z-Source Series Resonant DC–DC Converter for Photovoltaic Module-Level Power Electronics Applications». In: *IEEE Transactions on Power Electronics* 32.5 (2017), pp. 3634–3650. DOI: 10.1109/TPEL.2016.2591726 (cit. on p. 130).

[39] Fahad Alaql, Reza Rezaii, Abdullah Alhatlani, Sahin Gullu, Md Safayatullah, and Issa Batarseh. «Multi-Mode Rectifier-Based Dual-Input LLC Converter for Wide Voltage PV Applications». In: *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2022, pp. 1–5. DOI: 10.1109/ECCE50734.2022.9948025 (cit. on p. 130).