POLITECNICO DI TORINO

Master of Science in Electronics Engineering

Master Thesis

# Design of a high current Hot Swap controller exploiting Hysteresis control


**Supervisors**
Prof. Francesco Musolino
Eng. Davide Daprà

**Candidate**
Giuseppe Musco

7 April 2025

# Abstract

The aim of this thesis is the analysis, the design and the implementation and the experimental validation of a new high current Hot Swap controller which allows designers to overcome the limitations of state-of-art systems related to linear mode operation of Trench power MOSFETs.

A Hot Swap controller is a circuit that limits and manages the power flow during the start-up transient. This kind of circuitry is always present in rack electronic systems, especially in online servers and telecommunication equipment that provides services 24/7. In order to achieve a zero out of service time, maintenance and upgrade operations must be executed while the system is running.

The hot swap control circuit constitutes an interface between the common power supply backplane and the load circuit. The main purpose of the controller is to limit the inrush current that would flow towards the components, particularly in discharged capacitors; indeed, when the board is inserted into a live system, load circuit has a very large capacitive that causes an high current surge with dangerous voltage drop.
To mitigate such an issue, the Hot-Swap controller limits the current, protecting both the board and the surrounding system. Typically, this is achieved through an external MOSFET operated in linear mode by the controller, that senses the drain current, which is indeed the load current, and adjusts the control voltage accordingly.
In order to get started, literature and documentation were first studied to have an idea of the state-of-the art existing solutions and the related arising problems: as growth of networking services and data size has been impressive in the last decades, the power levels involved in telecom applications have seen a large increment. Furthermore, another critical aspect that has to be considered in this context is the evolution of trench MOSFETs. The devices have indeed undergone a strong optimization of their switching and on-resistance performance, reducing the capability of working in linear mode due to thermal instability. Due to the previous reasons, the implementation of hot swap controllers has become increasingly difficult during the years.

In this thesis a different control strategy is applied, aiming to avoid the problems related to the *Spirito's Effect*. The objective is to control and to limit the inrush current in a switching operation mode, avoiding the linear mode operation.
The circuit implements a buck converter where current feedback from the inductor is used to limit the load current. To ensure the limitation of the current and the transparency of the circuit after the transient, an Hysteresis control strategy is implemented. This

strategy ensures that the circuit has negligible losses when current is under defined value and cannot exceed this limit during the start-up and fault condition.

LTSpice has been largely employed to check the functionality, achieving successful results. The simulated circuit allows to charge an equivalent load capacitance of 20 mF in under 20 ms while keeping under control both the current and the switching frequency. A FPGA has been included in the real circuit to implement the controller behaviour and the circuital protections. Lastly, a prototype board has been designed and realized to perform a real test and validation of the simulated system.

This thesis work has been carried out at the Application Linear Power Systems Laboratories (ALPS) of Vishay Semiconductor Italiana S.p.A. .

# Acknowledgements

I would like to express my gratitude to Prof. Francesco Musolino for his guidance, support, and insightful advice throughout the development of this thesis.

A special thank you goes to my company supervisor, Eng. Davide Daprà, for his patience, availability, and continuous support. His experience and advice have been invaluable in overcoming the challenges of this work and deepening my knowledge in the field.

I also extend my sincere thanks to Vishay Semiconductor Italiana for providing the equipment and laboratory facilities necessary for carrying out this research. The opportunity to conduct experiments in a highly professional environment has been of great value to my academic and professional growth.

I am deeply grateful to my family for their unconditional support and encouragement throughout my academic journey. A heartfelt thank you to Elena, for always being by my side, and to Matteo, for his constant motivation and true friendship.

Finally, I would like to thank all those who, directly or indirectly, contributed to the completion of this thesis by offering their support and encouragement.

Thank you all.

# Contents

# List of Tables

# List of Figures

# List of acronyms and abbreviations

| | |
|---|---|
| **MOSFET** | Metal-Oxide-Semiconductor Field-Effect Transistor |
| **IC** | Integrated Circuit |
| **TVS** | Transient Voltage Suppressor |
| $R_{ds,on}$ | On-Resistance of MOSFET |
| $BVDss$ | Drain to Source Breakdown Voltage |
| **SOA** | Safe Operating Area |
| **CMRR** | Common Mode Rejection Ratio |
| **PWM** | Pulse Width Modulation |
| **ASFET** | Application Specific Field Effect Transistor |
| **FOM** | Figure of Merit |
| **EMI** | Electromagnetic Interference |
| **DCR** | Equivalent Series Resistor @ DC of an inductor |
| **ESR** | Equivalent Series Resistor |
| **CCM** | Continuos Conduction Mode |
| **DCM** | Discontinuous Conduction Mode |
| **PSRR** | Power Supply Rejection Ratio |

# Chapter 1

# Introduction

Nowadays, information and communication technology (ICT) is more and more addressing faster and reliable networking services, and much more secure online storage systems, among others features. These services are based on larger data and management servers which architecture typically includes rack-based computers. Ensuring that these systems are up and running almost every second of the day, all year round, implies avoiding any power interruption and protecting all the vital components on replacement boards when they are inserted into a live system; hence, when one of the boards experiences failure or ageing, it must be removed and, simultaneously, a new one should be inserted without having to shut down the whole system.

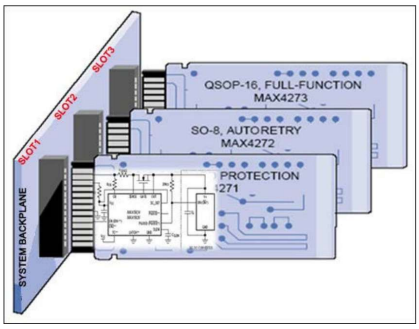



Figure 1.1: Boards on Backplane, Maxim Integrated Tutorial 4705 [1]

This maintenance operation, referred to as "hot-swap", is complicated and requires a great deal of care, especially when the power levels involved are high.
For this reason, in order to easily allow this operation, a special controller circuit is required, named *Hot-Swap controller*. The main purpose of a Hot-Swap controller is therefore to limit the initial current, known as the in-rush current. When new boards are plugged into the live back plane, high current is demanded by a large capacitive impedance seen at load side. An uncontrolled inrush current may cause several damage to the board itself, as well as brownout of the near ones and the disservice of the whole system.

In order to limit all these problems, different designs and Integrated Circuits (ICs) of Hot-Swap controllers have been developed through the years, providing inrush current limit and some additional features like short-circuit protection and over voltages protection. The main component, other than the controller itself, is the device that physically permits to limit the current. In order to reach this objective, usually a MOSFET in linear region(refer to [2]) is employed. The controller regulation is then reached through a current feedback, thanks to a shunt resistor. A simplified example is shown in figure 1.2.

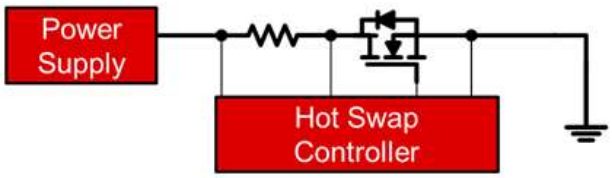



Figure 1.2: Simplified Hot Swap Circuit, TI technical article [2]

This idea has been successful in the past but new problems are currently arising, as growth of telecommunication and computing equipment has been dramatic: currents in Hot-Swap designs have been increased significantly reaching hundreds of amperes and, in the meantime, MOSFET technology evolved towards markets trend, that impose the manufacturer to optimize parameters like the $R_{ds,on}$, more useful in all the other power application. However this trend, has reduced the available Safe Operating Area (SOA) at high Drain-to-Source Voltages in according to the *Spirito's Effect* [3]. Professor Paolo Spirito explained that, as MOSFET manufacturers have increased transconductance to improve the on-resistance, there is a greater tendency for the MOSFETs to fail by forming unstable hot spots. So, since the market is more and more shifting towards this direction, making more and more difficult to find an adequate device, Hot-Swap applications have to adapt.
Another control strategy applied on the inrush current, the so called *Current Hysteresis Control*, is considered in this thesis; it consist in limiting the current absorption not by driving the limiter device in the usual way, but switching it on and off when the thresholds imposed by the controller are reached, solving the problem of having contemporary high $V_{DS}$ and high $I_D$ for an extended period of time.

The objective of this thesis is to design a modern Hot-Swap Controller capable of managing high currents and higher values of load capacitance, finding an alternative way to limit the inrush current without the risks associated to the *Spirito's Effect*.
In chapter [2] , the required background on modern MOSFET devices and Hot-Swap ICs is presented; then the basic idea behind the new control strategy adopted is discussed.
The circuital implementation of this control strategy is then explained in chapter [3] with the related circuital simulations and design. Two different solutions will be discussed; lastly a prototype printed circuit board (PCB) will be realized, allowing real functional test to be carried out and discussed in the fourth chapter [4]. The last chapter [5] will lead to conclusion and future perspectives.

# Chapter 2

# Theoretical background and state-of-the art of existing solutions

## 2.1 Power MOSFETs

Metal Oxide Semiconductor Field Effect Transistor is the backbone of all modern electronics, ranging from very small digital applications to high power designs. Even if the working principle remains the same, depending on the application, the technological implementation of a MOSFET changes: low power application (signal nMOS in 2.1) uses very fast and tiny signal MOSFETs, created on a common substrate, in which the diffused channel is formed horizontally between source and drain terminals, when the applied gate to source voltage ($V_{gs}$) is higher than the threshold ($V_{gs,th}$).

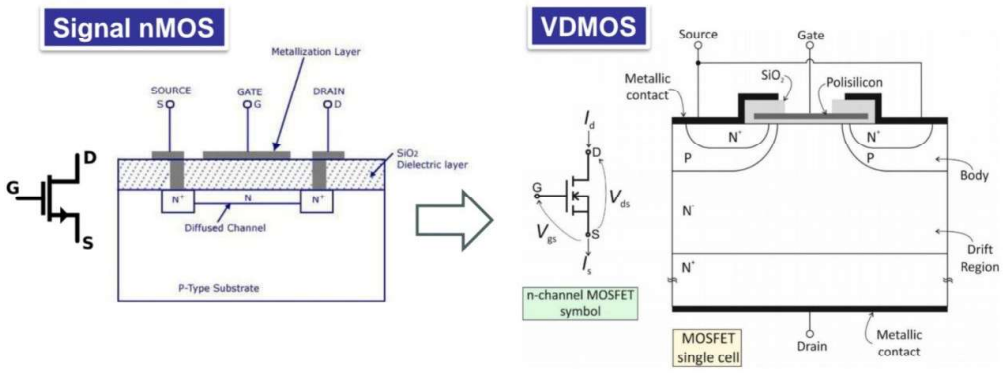



Figure 2.1: Difference between signal and power MOSFETs

Instead, to withstand larger power rating, the Vertical Diffused MOS, (VDMOS fig. 2.1) has been introduced; now the current flows vertically between the two terminals, and this type of structure permits to:

- Ensure higher Drain to Source Breakdown Voltage ($BV_{DSS}$) through an intrinsic epitaxial layer, the drift region;
- Maximize the cross-sectional area of the drift region thus lowering its resistance;
- Attach dissipative heatsink to the drain terminal (sometimes also to both drain and source);
- Make possible to pack together several MOSFET cells connected in parallel.

It is possible to recognize the usual functioning region of a classical MOSFET in VDMOS transistors (fig. 2.2):

- **Off state (interdiction, cut-off)** : if $V_{GS} < V_{GS,th}$ the channel cannot be formed, and no current can flow since the source-body and the body-drain junction are reverse biased;
- **On state**: When $V_{GS} > V_{GS,th}$ a conductive N-channel can form beneath the gate electrode, in the P-region, establishing in this way a path between source and drain terminals, depending on the voltage values, three different situations can occur:
  - if $V_{GS} > V_{GS,th}$ and $V_{DS} > V_{GS} - V_{GS,th}$ : **linear region**, here both high $V_{DS}$ and high $I_D$ are present, and so it is not used in power application;
  - if $V_{GS} > V_{GS,th}$ and $V_{DS} < V_{GS} - V_{GS,th}$ : **triode region**, this is also not used;
  - if $V_{GS} > V_{GS,th}$ and $V_{DS} << V_{GS} - V_{GS,th}$ : **resistive (or ohmic) region**, here the device acts as a resistor named $R_{ds,on}$ dependent on $V_{GS}$, and the power consumption is therefore reduced.

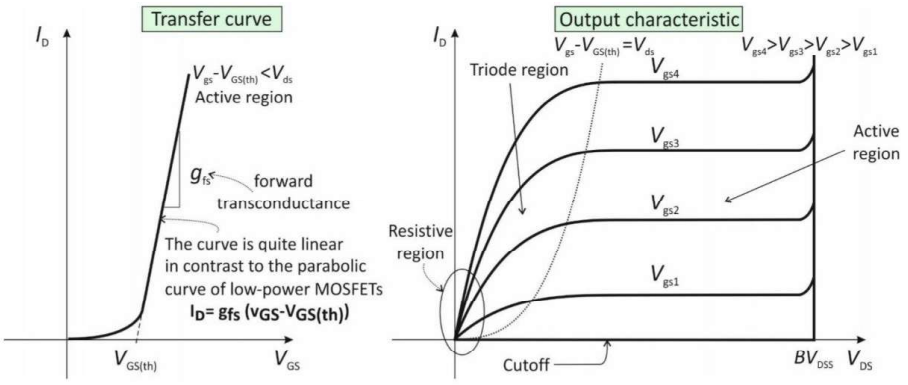



Figure 2.2: VDMOS transcharacteristic.

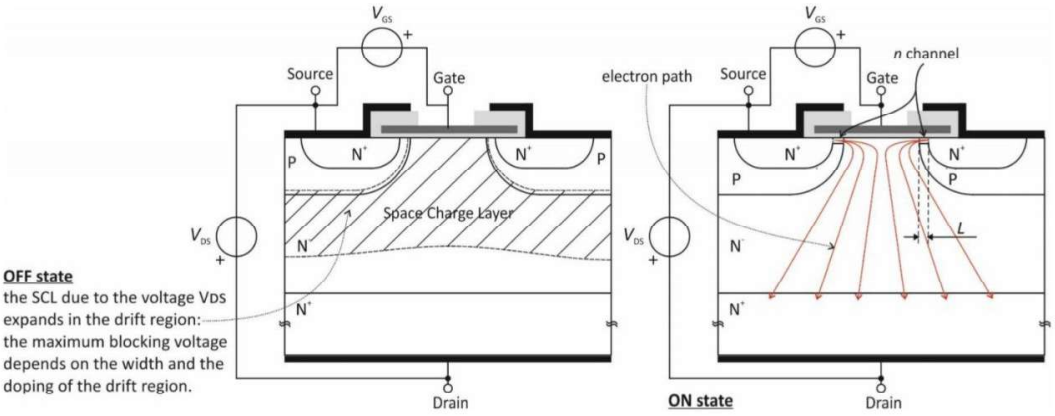



Figure 2.3: VDMOS On and Off state.

In power application, MOSFETs are usually employed as switching devices, hardly ever in linear or triode region. Therefore, one of the most important parameter is the $R_{ds,on}$, that defines the static power dissipation of the device in the ohmic region (as it can be seen in eq.2.1). Currents involved in power application are usually high, reaching order of hundreds of amps, and they will grow further as technology and application evolves.
Therefore, researches and optimizations on the $R_{ds,on}$ have been carried out, with the purpose reduce static power consumption.

$$P_{diss,static} = R_{ds,on} \times I^2_{D,rms} \tag{2.1}$$

In order to define the total resistance of the device, several contributions have to be taken into account [4], such as the resistance of the source metallization, the contact resistance between the source metal and the source N+ doped region, the channel resistance, the intrinsic resistance and finally the substrate resistance.

In practice, given their usual values, every term can be neglected, with the exception of the channel resistance and the drift component, much larger with respect to the others.

$$R_{DS,on} = R_{ch} + R_{drift} \tag{2.2}$$

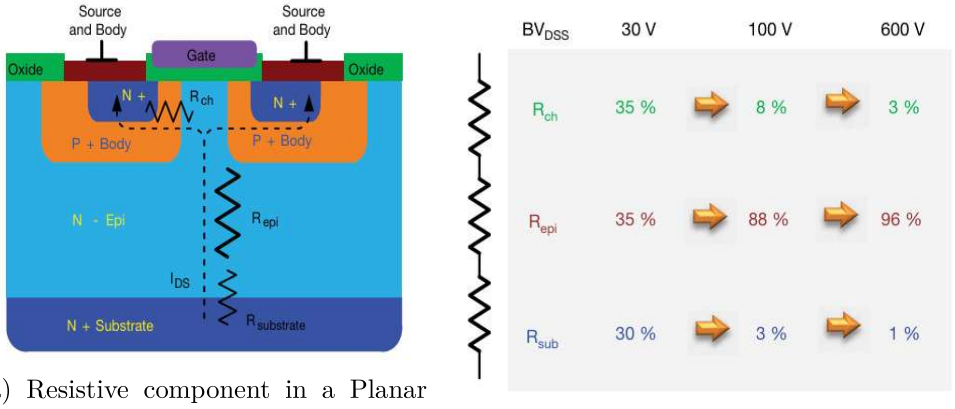
In low voltage applications, below 150 V and especially below 60 V [4], the channel resistance plays the most important role, and it can be defined as in equation 2.3.

$$R_{ch} = \frac{1}{2K(v_{gs} - v_{gs,th})}, \text{ with } K = \frac{\mu_n C_{ox} W}{L} \tag{2.3}$$

Conversely, at high voltages, the intrinsic layer must be thicker in order to sustain higher Breakdown Electric Field, as a consequence, this leads to a dominant $R_{drift}$ term:

$$R_{drift} \propto BVDSS^c \; c \in (2.5 \div 2.7) \tag{2.4}$$

.




(a) Resistive component in a Planar VDMOS.

(b) Resistive percentage in Planar VDMOS

Figure 2.4: Resistive behaviour with respect to BVDss, Vishay AN[5].

Another important parameter for optimising efficiency in power application, concerning switching losses, is the gate charge $Q_g$, which defines the amount of charge that needs to be supplied to the gate terminal to get a fully turned-on MOSFET. The higher the gate charge required, the larger is the channel and hence the lower the resulting resistance. Therefore, these two critical parameters are also correlated : the Figure Of Merit (FOM) to look at is then the product of the two, expressed as: $R_{ds,on} * Q_g$.

The growing requirements in power demand have driven the market, forcing manufacturers to find new ways and technologies to optimise device FOM, moving towards what is known as TrenchFET technology.

Throughout the last century, starting in the seventies with the first vertical V-groove gate MOSFET [4], technology improvement have allowed the delevopment of Trench MOSFET technology. Trench MOSFETs use a vertical structure with a buried gate electrode, in order to enhance channel density and with the final purpose of lowering as much as possible the $R_{ds,on}$, while keeping a reasonable $Q_g$, various techniques like field shaping or charge balance have been introduced, reaching nowadays extremely low On-Resistance with lower and lower Gate charge $Qg$.

The structures in figure 2.5, i.e. cells, are usually connected in parallel, as shown in figure 2.6, inside a single device, providing in this way the lowest resistance possible, and allowing more current capability.

If the pitch, namely the distance between two cells, is reduced, we can have more cells in the same area achieving better results in terms of resistance. Anyway, this creates serious problems if the device has to work in linear region because the transconductance is now very high:

$$g_{fs} = \frac{I_D}{(V_{gs} - V_{gs,th})} \tag{2.5}$$

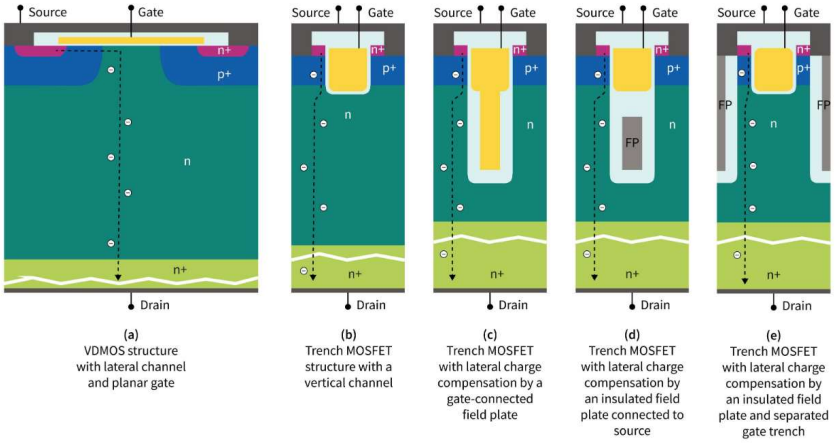
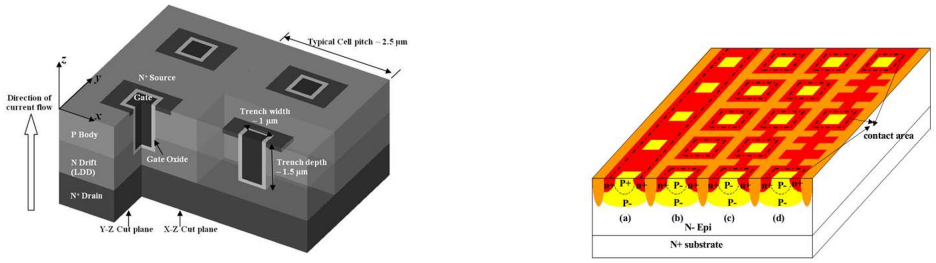



Figure 2.5: Common Power MOSFETs cell structure, Infineon [6].




(a) Simple Interconnection, [8]. (b) Example of various cells interconnection, [7].

Figure 2.6: MOSFET cells interconnections.

In terms of hot-swap or soft-start applications, the main problem that has been observed as the inrush current grows, is related in fact to the poor capability of Trench MOSFETs to operate in the linear region due to their intrinsic thermal runaway problems [3]: this type of power MOSFET presents a higher sensitivity of the threshold voltage $V_{gs,th}$ with respect to temperature (this is given by the geometry and doping of the devices). As the device temperature rises, the threshold voltage will fall, making the drain current $I_D$ rise rapidly, since the forward transconductance is higher, getting in turn temperature rising and therefore resulting in a positive reaction, in what is called a *thermal runaway* phenomena. If this type of device is driven in the linear region, phenomena such as *hotspots* with the consequent formation of *current crowding* within certain cells of the device will probably occur every time, leading to the destruction of the device without any possibility of cooling it down.

As it can be seen from figure 2.7, the variation of drain current against gate bias voltage is plotted in the transfer characteristic graph. Two lines are used to show the Trench MOSFET operation at a junction temperature of 25 °C (solid line) and 175 °C

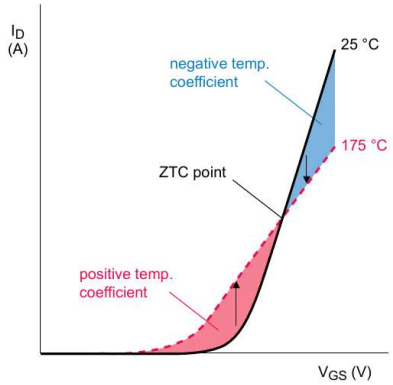



Figure 2.7: Thermal dependency of Drain Current, Nexperia AN50006 [9].

(dashed line). For a low enough $V_{\text{gs}}$, the MOSFET will conduct more current if it operates at 175 °C than at 25 °C, due to the negative temperature coefficient of the threshold voltage $V_{\text{gs,th}}$, as shown in figure (2.8).

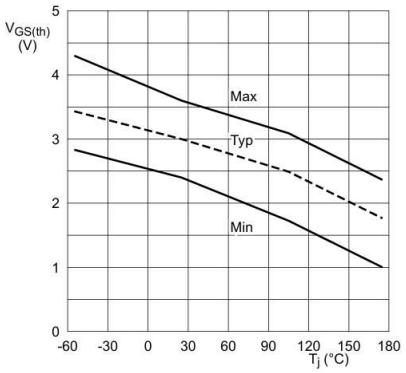



Figure 2.8: Threshold Gate to Source Voltage vs Temperature

In this case the MOSFET is operating in a region of thermal instability, identified by a positive temperature coefficient of the current. Below the Zero Thermal Coefficient (ZTC) point, if a small region is at a higher temperature than the rest of the die, it will draw more current and consequently dissipate more power becoming even hotter. This process eventually leads to thermal runaway and the destruction of the MOSFET.

Recently, the solution to this problem has been found in what some manufacturers call Application Specific MOSFET (or ASFET) [9], referring exactly to the hot-swap or soft start application, the Trench devices are then optimised with respect to the Safe Operating Area (SOA) instead of the previous FOM $= R_{ds,on} * Q_g$, but this will greatly increase the engineering and manufacturing costs.

For this reason, and since the vast majority of power circuits operate in switching mode, the following chapters present a hot-swap solution using switching Trench MOSFETs (not application specific), which reduces costs and avoids re-engineering the devices.

## 2.2 Hot Swap Circuits and Controllers

In this section, we will explore the evolution and the state of the art regarding the employed technology to perform Hot Swap. A classical example of system that requires Hot Swap capability is the telecom base transceiver station. These kinds of systems are usually based on parallel boards, containing the needed circuitry, all plugged into the same $-48\,\mathrm{V}$ back plane.

The term Hot Swap refers to the possibility of removing and plugging in a board without powering down the entire system; as an example, when a fault is flagged on one of the cards, it can be removed and substitute with a new one. When a fresh new board is plugged into the live back plane, a very large inrush current is demanded by a large capacitive impedance seen at load side, since the new board contains a lot of capacitors all discharged.

If the inrush current is not controlled, it can cause lots of undesired problems, such as ringing at the power supply side with consequent possible damage on all the board, voltage brownout of the back plane, and the consequent reset of the near cards and, in the worst case, a drop-off of the entire system.

An Hot Swap controller drives the limiter device, which is carried out by one or more external MOSFETs in active region, for the amount of time required by the load capacitance to fully charge and asset at the nominal voltage. This could provoke the exceeding of the SOA of the device. If the period of time in which the device remains in this region is not controlled, the operation of the same will be compromised, and so generally the controllers employ a SOA timer to avoid this problem.

In the past, the power required by these systems was modest and Hot Swapping techniques were carried out by using a power switch with a soft start behaviour, controlled by a relatively simple IC.

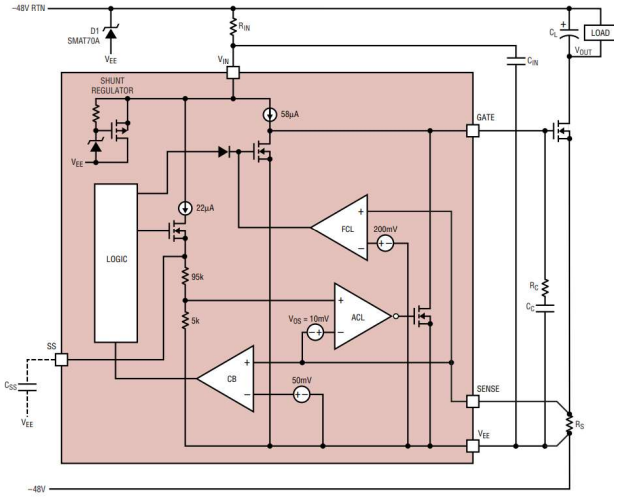
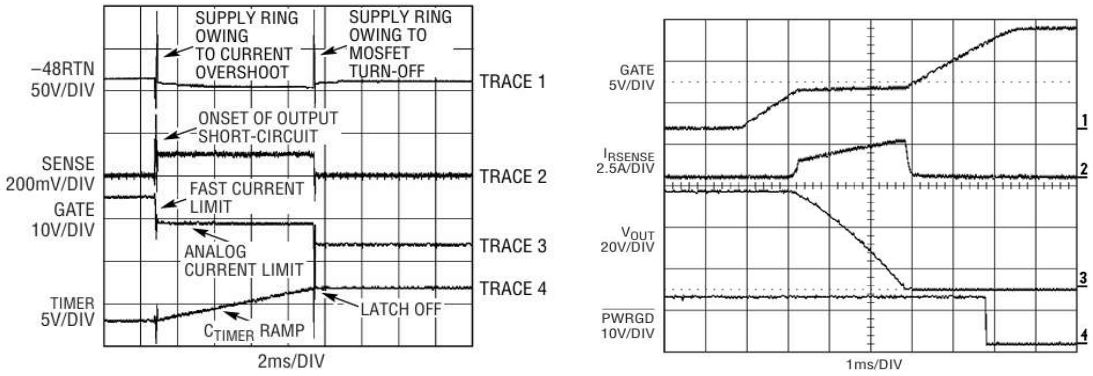



Figure 2.9: Linear Technologies, LTC4251 IC family, 2003 [10].

As an example it is presented the LTC4251 from 2003 by Linear Technologies. This system limits the current through the load, comparing the voltage drop on a sense resistor $R_s$ with three stages of thresholds: the Circuit Breaker (CB Operational Amplifier, in figure 2.9 used as a comparator) triggers when the lowest of these thresholds is exceeded, starting a timer to check that the SOA is not being violated; another fast comparator (FCL in fig.2.9) triggers if the sense voltage is four times the circuit breaker limit and, in that case, it will immediately discharge the gate and, until the voltage does not return under the limit of two times the CB (ACL in fig. 2.9), the controller will latch in this state. Then, when the voltage becomes lower the gate is released, and the compensation capacitor $C_c$ recharges the gate capacitance; if in the meantime the CB timer trips and the gate is pulled down again, this time the controller may latch here or have an auto-retry. The IC also provides a soft-start behaviour, using the $SS$ pin as a reference for the analog current limiter (ACL in fig. 2.9): if a capacitor is attached here, this limit is slowly raised up. Outside the IC, a TVS Diode is used to avoid any power supply ringing reaching the MOSFET; if this happens, the avalanche will interfere with the nominal behaviour of the IC.




(a) LTC4251 Short Circuit Fault Behaviour.

(b) LTC4251 Soft Start Behaviour.

Figure 2.10: LTC4251 Waveforms, LT Datasheet 2003 [10].

In figure 2.10 we can observe:

- On the left, figure 2.10a, the behaviour of the controller if a short circuit is applied at the load side. At first, the FCL triggers and discharges the gate. Then, the current is limited at the ACL value and the SOA Timer starts to count.Finally, when it trips, the gate is completely discharged and turned off, the controller may remain in this state, called "Latch Off" or may launch an auto-retry.

- On the right, figure 2.10b, the nominal behaviour is shown. From the gate voltage curve, the upper one shown in the figure, we can see that the device is maintained in active region ($V_{gs}$ is set constant, plateau in the curve), limiting the load current on $R_{SENSE}$. This is done for approximately 3 or 4 ms, required to reach the nominal voltage of $-48\,\mathrm{V}$ at the output load capacitance, $V_{OUT}$ trace in figure. The last trace of PWRGD goes low to signal that the hot swap was correctly performed.

Nowadays, the current demanded by new telecommunication technologies, due to higher computing performances and higher server capabilities, are much larger with respect to what shown in the LTC4251 from 2003. To have an idea, power consumption of a single board in a telecom environment is now in the order of some kW, therefore causing an exponential growth of the in-rush current, reaching up tens to hundreds of Amps.

As a consequence, it is becoming more and more difficult to find an adequate device,capable of sustaining this range of current for a period of time that is now enlarged, since the load capacitance is necessarily bigger, for all the reasons presented in the above section 2.1. To describe the state of the art of the existing solution, we can take as an example the LTC4284 IC of Linear Technologies from 2021.

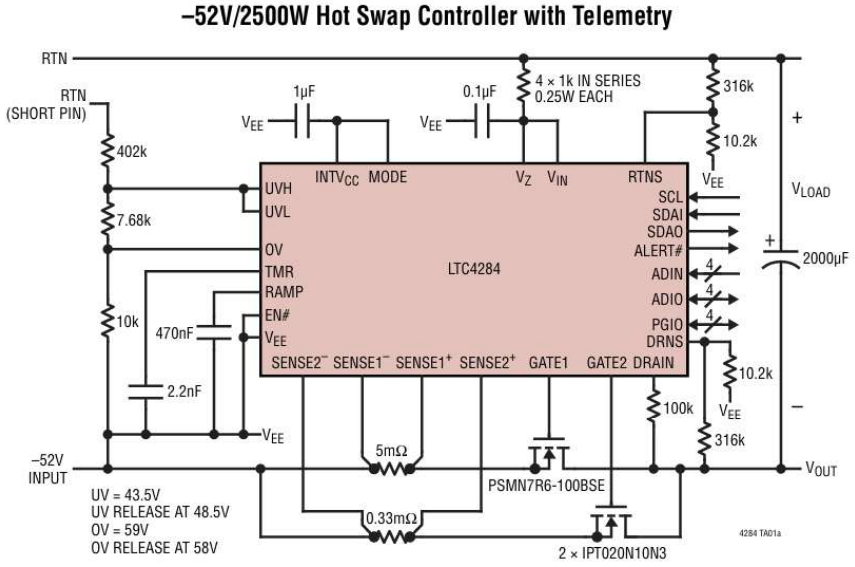



Figure 2.11: LTC4284 HotSwap Controller, Linear Technologies [11].

Now more MOSFETs are required to withstand the power requirements, whether it is by means of maximum current or SOA. This complicates the internal structure of the controller (fig.2.13) with more feedback loops, more SENSE pins and more gate driving outputs. This IC includes also various protections against Over and Undervoltages. Even in this case a timer and a RAMP pin are used like in the previous LTC4251. As it is possible to observe in fig.2.11, a serial communication has been implemented as well as other digital and programmable pins, to make the controller flexible and able to collaborate with a main controller.

From fig.2.12 it is now possible to understand that the proposed approach involves the use of one single MOSFET (connected to GATE1 pin in figure 2.11) as the limiter device, carrying less than 1 A but for a very long period of time of nearly 700 ms to respect SOA limit. This is true for a limited capacitance load, in this example of 2 mF. The GATE2 instead is used as a switch to split the nominal current and to reduce the

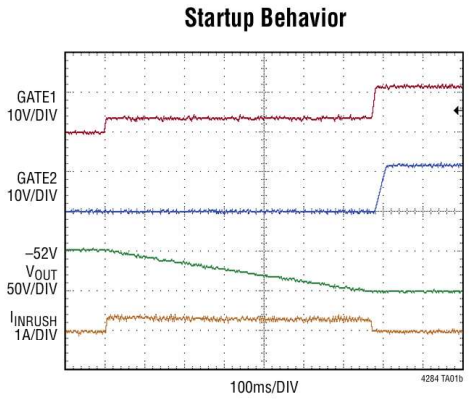



Figure 2.12: Startup Waveforms LTC4284, [11].

static power consumption. In fact, as it is possible to observe in figure 2.11, the two GATE terminals of the LTC4284 drive two different kinds of MOSFETs. The first one, in charge of limiting the in-rush current, is indeed an ASFET: the PSMN7R6 from Nexperia, with an optimized SOA for linear operating mode, at the expense of the $R_{ds,on}$. This causes the ASFET to not be able to carry large current values in ohmic region. Therefore this task is delegated to the other MOSFET driven by the GATE2 terminal, switched on (in ohmic region) only when the startup transient is completed, as it is possible to observe from figure 2.12 by referring to the second trace GATE2 on the graph.

As a conclusion, it is possible to notice how the system has become more complex with respect to the 2003 proposed system, since both an ASFET and a MOSFET are now required. This trend imposes also, more complicated controller structure (refer to figure 2.13) and increases the final costs.

From what have been exposed, the idea behind this thesis finds its own motivation: the design a Hot Swap controller that is not only capable of managing high currents and, ideally, any value of load capacitance, but also of reducing the costs, avoiding the use of ASFETs and simplifying the control strategy and, therefore, the controller operating scheme. The final purpose is to design a modern Hot Swap Circuit for Telecom Infrastructure, working with a nominal input voltage of $-48V$, nominal current of $\sim 30\,\mathrm{A}$, and inrush current limiter at $60\,\mathrm{A}$.

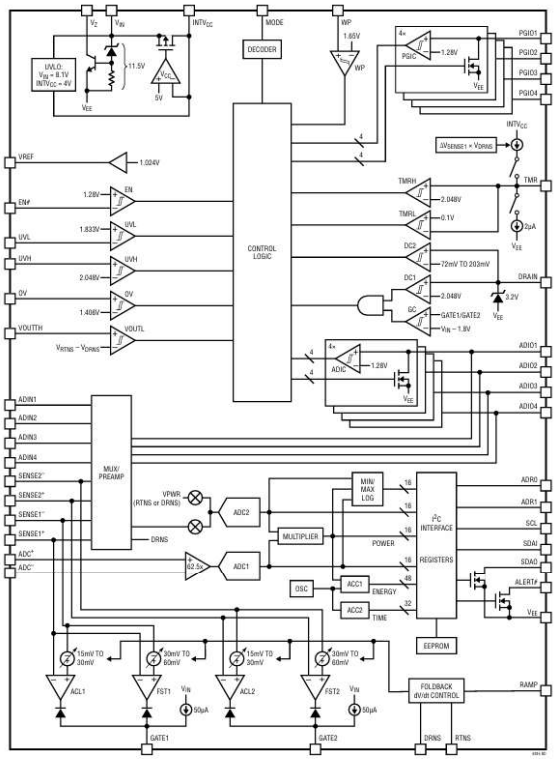
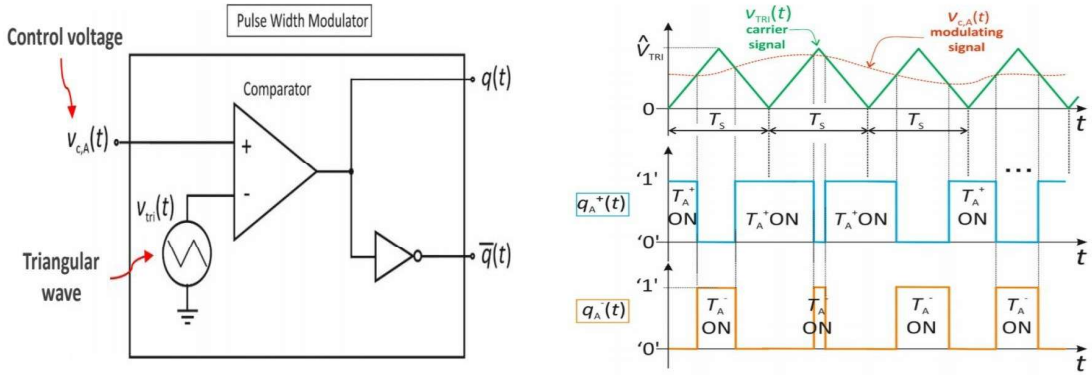



Figure 2.13: LTC4284 internal block diagram, ADI Datasheets [11].

## 2.3 Switching Current Control

Due to the issues described in the previous section related to the operation of modern MOSFETs in the linear region, the adoption of such transistors in Hot Swap controllers needs to be carefully evaluated, even in the case of ASFETs.
So, instead of limiting the inrush current by driving the device(s) for a quite large time in linear region, we want to employ them in a switching mode operation. Switching Mode Power Supplies work in a slightly similar way to what we want to design: in DC-DC converters the Duty Cycle ($D = \frac{T_{on}}{T_{sw}}$) controls the switches at a constant switching frequency $f_{\text{sw}}$ in order to obtain at the output a "constant" $V_o$ voltage, with low superimposed ripple, used as a stable power supply. This is possible through a Pulse Width Modulation. The control behaviour is applied to the circuit by means of the duty cycle, that sets the duration of the "ON" and "OFF" period of the switch.
In order to generate a PWM signal a carrier, usually a triangular or sawtooth waveform, is compared to the control voltage, that is the modulating signal, coming from the feedback. So, if the control voltage is higher than the triangular one, at the output of the analog comparator we have a logic high level, and vice versa. In this way, a constant frequency square wave signal is obtained, in which the Duty Cycle varies with the control voltage level. Hence, the variations at the modulation are impressed at the output through a variation of $D$. The control voltage is obtained from a resistive feedback of $V_o$

in Voltage-Mode power supplies or from a shunt resistor measuring the current flowing in the inductance in Current-Mode power supplies.




(a) PWM modulator. (b) PWM Waveforms.

Figure 2.14: Simple PWM generator.

This principle is applied in every Switching Mode Power Supply (SMPS), regardless of the topology; concerning the possible choices of topology, from figure 2.15 it is possible to appreciate the Buck converter, a quite convenient solution in order to implement the needed mechanism. There, we can notice that the switch is placed in series between the input loop and the output one. This is exactly what we need in order to limit the current flow, that must be sensed in order to derive a feedback and making possible to control it, by means of $D$, and consequently of average value of the current absorbed from the input side.

The working principle is now shifted, the Buck converter has to maintain the $V_o$ in a very narrow range of values. In what will follow, we start from this topology and use it as a current limiter, by adapting the circuit and the control strategy to the final purpose.

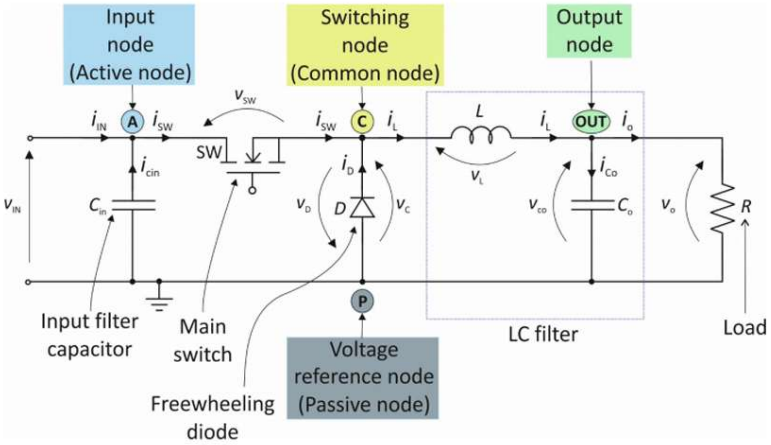



Figure 2.15: Buck Converter Topology.

### 2.3.1 Hysteresis Current Control

Hysteresis control, also known as bang-bang or on-off control, is the simplest and most primitive form of process control; it consists of two thresholds of the controlled variable (i.e. the current) which, when reached, trigger the action of the controller, that opens (or closes) the switch, forcing the variable to remain within a certain range, called hysteresis delta. The name "On-Off" actually comes from the fact that the controller only acts on the device by fully opening or fully closing it. A simple example, that provides an idea that works exactly in this way, is a thermostat in a house.

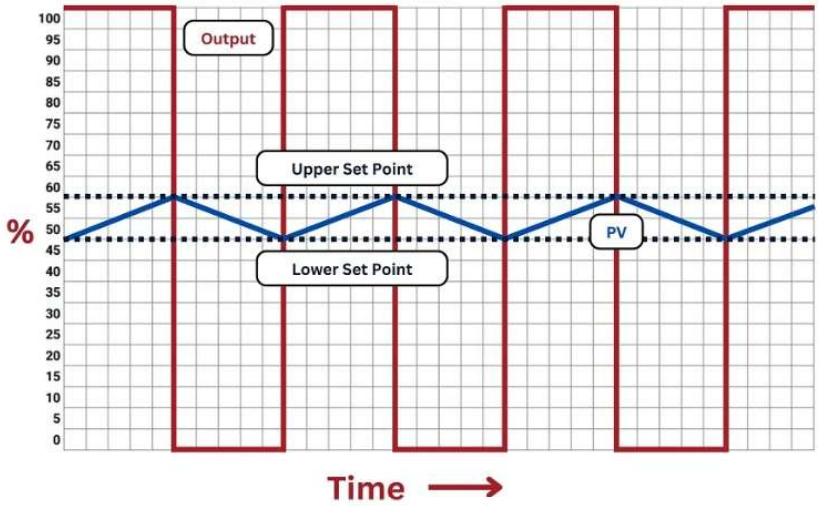



Figure 2.16: Process Variable and Controller Output behaviour, [12].

From figure 2.16 we can see that the controlled variable always remains within the two thresholds, and this is the basic idea behind the way we want to control the current flowing from the input side to the load capacitance.

The performances, when applied to an automation process, are very poor with respect to a classical controller, like the Partial Integrative Derivative (PID), in terms of error and set-point tracking. Nevertheless, this strategy is perfect for situations in which the tracking is not vital. In the specific case, in fact, we only have to limit the average value of the current below the maximum, without caring much of the exact value of it.
The principal advantage of this kind of control is that it is of simple implementation. Furthermore, it has a very fast time response.

In the next chapter of this thesis, the objective will be to apply this simplified strategy to the control of the inrush current.

# Chapter 3

# Analysis and Design

In this chapter, once all the needed background has been presented, the control idea will be applied to the circuit in figure 3.1. A Buck-like topology is employed for the reasons explained in section 2.3.1. With respect to the previously described system, we can now observe a 0 V return (RTN) common rail, dictated by the −48 V supply used in telecom, employed to avoid oxidation of cables under the ground [13].
This design allows the current to reach the maximum when the SW (S1 in 3.1) is closed and then to decrease through the right loop: the recycling diode D1 kicks in when the SW is opened, allowing the load to continue to charge with the energy stored in the inductor L1. The lower threshold is reached when the current in L1 triggers the controller to trip again, closing the SW.

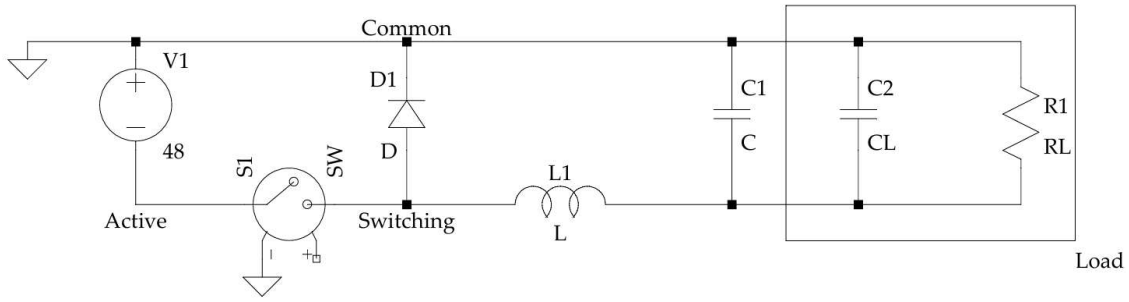



Figure 3.1: First idea of circuit design.

The inductor L1 does not only act as a reserve of energy (current source) during the off period of the switch (fig. 3.1), but it also sets the maximum rate of change of the current ($\frac{\mathrm{d}I}{\mathrm{d}t}$). These slopes, neglecting the voltage drop across D1, are defined as:

$$S^+ = \frac{V_{in} - V_0}{L}; \quad S^- = \frac{V_0}{L};$$

$S^+$ refers to $T_{ON}$, i.e. when the SW is closed, and $T_{OFF}$ hence, when SW is opened (3). In contrast to what happens in a DC-DC converter, here the $V_o$ is rising to charge the load capacitance $C_L$, causing the voltage drop on the inductor to change at every cycle,

and accordingly $S^+$ and $S^-$. Once the two thresholds have been set, i.e. the Hysteresis Delta, these result in a variable $D$ and $f_{sw}$:

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{\frac{\Delta H}{S^+}}{(\frac{\Delta H}{S^+} + \frac{\Delta H}{S^-})} = \frac{(\Delta H \frac{L}{V_{in} - V_0})}{(\frac{L}{V_{in} - V_0} + \frac{L}{V_0})\Delta H} = \frac{\frac{1}{V_{in} - V_o}}{\frac{1}{V_{in} - V_o} + \frac{1}{V_o}} = \frac{V_o}{V_{in}} \tag{3.1}$$

$$f_{sw} = \frac{1}{T_{ON} + T_{OFF}} = \frac{1}{(\frac{\Delta H}{S^+} + \frac{\Delta H}{S^-})} = \frac{1}{(\frac{L}{V_{in} - V_0} + \frac{L}{V_0})\Delta H} = \frac{1}{\frac{V_{in}}{V_o(V_{in} - V_o)} L \Delta H} = \frac{V_o(V_{in} - V_o)}{V_{in} L \Delta H} \tag{3.2}$$

Where $\Delta H$ is the Hysteresis Delta $\Delta H = I_{max} - I_{min} = [\,\mathrm{A}]$.
From this equation, we can understand the behaviour of the duty cycle ( in eq. 3.1) and of the switching frequency (in eq. 3.2) as the output voltage $V_o$ rises at the capacitive load. The duty cycle is independent from the hysteresis delta and the inductance value; it starts from 0 when the board is first plugged in and reaches 1 at the end of the transient when the $C_L$ is fully charged at $V_o = V_{in}$.

the switching frequency once again will vary according to $V_o$, but this time it depends on the inductance value and on the width of the hysteresis; this is a useful result in order to control the range of values that it can assume. As it will be done in the next section 3.1, this allows to set the maximum $f_{\mathrm{sw}}$ by means of the first derivative against $V_o$:

$$f_{sw,max} = \frac{\partial f_{sw}}{\partial V_o} = \frac{V_{in} - 2V_o}{V_{in} L \Delta H} = 0 \implies V_o = \frac{V_{in}}{2} \tag{3.3}$$

The hysteresis range will also set the duration of the start-up transient, since the average current value depends on it, and the load capacitance will reach the steady state faster if the average current is higher.

Therefore, a proper selection of the Hysteresis Delta and of the Inductor is crucial for the operation of the controller. The observance of all the requirements and the selection of the proper component is therefore discussed in the following sections.

## 3.1 Circuit Design

The circuit just described, represented in figure 3.1, gives only a first idea of what is needed, many more components need to be added to achieve the desired regulator behaviour. As we have just said, the switch is in series between the active node and the switching node, the inductor is between the latter and the load, and the diode is between the common and the switching node. This configuration makes it possible to set the maximum $\frac{\delta I}{\delta t}$ slope, allowing the exchange of charges between the two capacitances (bus bypass and load) without uncontrolled inrush.
The following specifications, are in line with what is usually requested by a customer in a telecom environment:

- Maximum Current during Charging Phase: 60 A
- $BVDss$ of MOSFETs and Diodes: 150 V
- Load Capacitance : $10 \div 20$ mF
- Steady state Power Consumption : $\sim 1.5$ kW
- Maximum Switching Frequency : $< 150$ kHz

Given these specifications, it is possible to verify that working with this value of voltage and current in a linear region is difficult, and so in these section we try to overcome the problem implementing the discussed above switching operation.

In order to apply the Hysteresis Current Control strategy, a feedback loop based on the current that flows towards the load is needed. Therefore, we need a measurement of the current, and the simplest way to do that is through a sense resistor and an adequate current sense amplifier. Others idea could be possibly implemented, as an example, through sensing the current by the voltage drop on the Equivalent Series Resistor @ DC of the Inductor (DCR), or also sensing at the $R_{ds,on}$ of the MOSFET(s); neither of these strategies, are trivially implemented, unlike the classical shunt solution, because of the high common mode voltage at the switching node, which jumps between 0 and -48V at every half period of the cycle.

The classic solution with the shunt resistor is then adopted. However, a few considerations have to be made about its position in the loop. As it was previously done ,in order to not require a very high Common Mode Rejection Ratio ($CMRR$) on the differential amplifier, the shunt must be placed in a strategic position, between two nodes, that ideally should not move during the two sub-periods $T_{ON}$ and $T_{OFF}$. Looking at the circuit, we understand that the common rail (RTN) is the simplest candidate to place it; in order to also sense the free-wheeling current through the diodes during the $T_{OFF}$ period, the sense resistor is placed on the load loop side as it can be seen in figure 3.2. With the resistor placed here, there is no common mode at the input of the amplifier, which greatly simplifies the requirements for the sense amplifier.

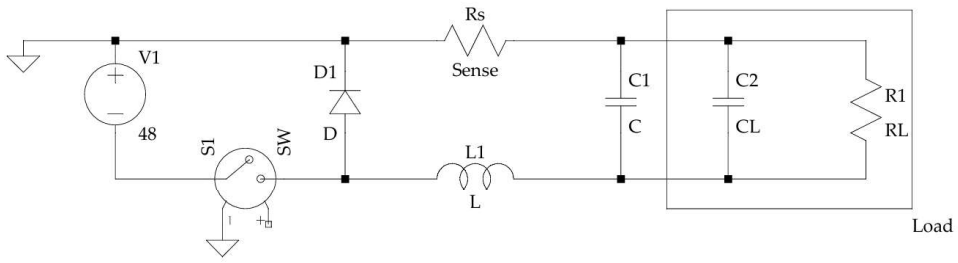



Figure 3.2: Positioning of the sense resistor on to the initial circuit

Since the power flow in our circuit is quite large, the value of the shunt, or in general, of any other resistive element or parasitic, must be as low as possible to reduce at minimum the power dissipation across it: when the transient is over, the circuit must be as transparent as possible, ideally not dissipating any static power. In practice, some power will always be dissipated by the circuit, but we can make it negligible with respect to the power that flows towards the load.

We can now proceed with some considerations about the value of the components, their parasitics, and the width of the current hysteresis delta. The final purpose of the circuit is to limit the current below 60 A, and so it may be useful to place the upper threshold here. For the lower one we have to consider different aspects: if it is placed too close to the upper one it can cause high frequency switching (see eq. 3.2 and 3.3), and it also makes it impossible to discriminate correctly the two thresholds at the sense amplifier, since it has to be very small, having two voltage thresholds close together is not a good idea at all.

A good value, as it will be explained in what follows, could be:

$$I_{min} = 40\,\mathrm{A} \tag{3.4}$$

For what concerns the value of the resistor, knowing that the nominal current absorbed by the load is more or less half the maximum in the start-up phase, the static power on the shunt, i.e. when the transient is over, will be:

$$P_{d_{R_s}} = R_s \cdot I_{L,ss}^2 = R_s \cdot (30\,\mathrm{A})^2 << P_{Load,ss} \simeq 1.5\,\mathrm{kW} \tag{3.5}$$

Where $I_{L,ss}$ represents the load current at the steady state.
By Imposing a negligible $P_{diss}$ on the shunt, around 0.1% of the load power, i.e. $1.5 \div 2\,\mathrm{W}$, a reasonable value is:

$$R_s = 2\,\mathrm{m\Omega} \tag{3.6}$$

With a similar constrain on the static power dissipation, the inductor value must be chosen looking at its DCR (Equivalent Series Resistance @ DC, 25 °C), that must be in order of magnitude similar to the shunt, for the same reason above. For what concerns the inductance value, it must be chosen in order to respect the maximum $f_{sw}$ constrain

for the Electromagnetic Interference(EMI). As it was seen in chapter 3, the switching frequency is inversely proportional to the inductance, and its maximum is reached, as demonstrated above in eq 3.3, at $V_o = \frac{V_{in}}{2} \implies D = 0.5$, where the two slopes are ideally equal, obtaining:

$$D = 0.5 \implies T_{ON} = T_{OFF} \implies \frac{V_{in} - V_o}{L} = \frac{V_o}{L} \tag{3.7}$$

$$\Delta H = T_{ON} \cdot \frac{V_{in} - V_o}{L} = T_{OFF} \cdot \frac{V_o}{L} \tag{3.8}$$

Extracting $f_{sw}$:

$$f_{sw} = \frac{V_{in} - V_o}{2L\Delta H} \tag{3.9}$$

Where $\Delta H$ is the Hysteresis Delta $\Delta H = I_{max} - I_{min} = 20$ A.
Having defined the Hysteresis Delta , and the constrain to a maximum switching frequency, inductance must be:

$$f_{sw,max} = \frac{V_{in} - V_o}{2L\Delta I_L} = \frac{24\,\mathrm{V}}{2 \cdot L\ 20\,\mathrm{A}} < 150\,\mathrm{kHz} \implies L > 4\,\mu\mathrm{H} \tag{3.10}$$

Now, the closest value in the E12 series is 4.7 µH, that sets the maximum $f_{sw} \simeq 130\,\mathrm{kHz}$. These calculations refer to an **ideal case**, in which the voltage drop on the shunt, on the diode and on the $R_{ds,on}$ and on the other parasitics are neglected; although, the approximation is good enough and it is therefore pessimistic, since the fact that, by including all these contributions, the maximum frequency will be lower. Furthermore, saying that the two slopes are equal at $V_0 = 24\,\mathrm{V}$ is an approximation, since the voltage drop on the diode and on the MOSFET is surely different. From Spice simulations it results that $f_{sw} < 120\,\mathrm{kHz}$ (see next section 3.2).

Therefore, also from this result we can understand another reason why the lower threshold have been set to 40 A. If the Hysteresis Delta is small we need a larger inductance to respect the constrains on $f_{sw}$, but a larger inductance means larger DCR, and so more static power losses. If the range is enlarged, more time is required to reach the steady state. Since we only have to limit under 60 A, there is no reason to set the average value lower.

With these values set, the drop across the shunt when the two threshold are reached is calculated:

$$V_{R_s,h} = R_s \cdot I_{Max} = 2\,\mathrm{m\Omega} \cdot 60\,\mathrm{A} = 120\,\mathrm{mV}$$
$$V_{R_s,l} = R_s \cdot I_{min} = 2\,\mathrm{m\Omega} \cdot 40\,\mathrm{A} = 80\,\mathrm{mV}$$

With these two thresholds, it is possible to use a sense amplifier with a reasonable gain of $G = 20$, allowing to have the two amplified thresholds 800 mV distant, making negligible any problem of offset error, or spurious trigger at the logic, posing them at:

$$V_{I_{meas},h} = 120\,\mathrm{mV} \cdot 20 = 2.4\,\mathrm{V}$$
$$V_{I_{meas},h} = 80\,\mathrm{mV} \cdot 20 = 1.6\,\mathrm{V}$$

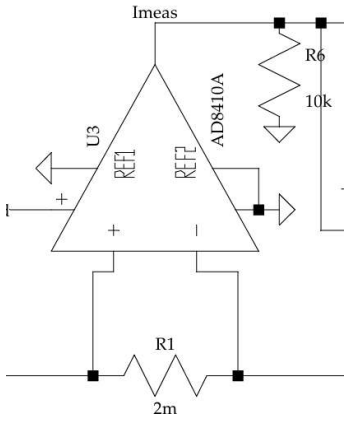



Figure 3.3: Section of the sense amplifier U3 and sense resistor R1.

The control behaviour is realized as follows: after the sense amplifier, the two voltage values must be compared with two fixed thresholds, getting a logic one when one of the two is exceeded. In first place (figure 3.4), two analog fast comparators have been used, the top one connected to a voltage reference that represents the higher threshold ($Th_h$ in 3.4), and respectively, the bottom one with the lower threshold ($Th_l$).

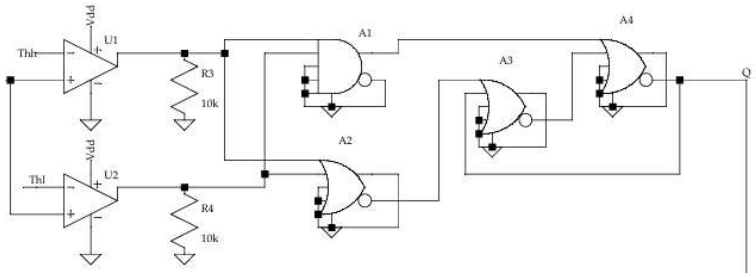



Figure 3.4: Simple controller logic.

Therefore, when both the thresholds are exceeded, the controller must take action, opening the switch through a command signal. Therefore, we can use the logic "AND" (A1 in 3.4) of the output of the two comparators. On the other hand, when both the comparators gives a logic "0" at the output, it means that both the thresholds have been exceeded below, and so a logic "NOR" (A2 in 3.4) is used this time, allowing the controller to trigger again by closing the switch. In this way a cycle is established, until the voltage drop on the load reaches the steady state. Other idea could be exploited, as we can see later (Section 3.4.2).

Now that we have defined the logic operation to get the open and close functions, we need to interface the two signals obtained at the output of the AND gate, "open", and at the "NOR", "close", with the one required by the gate driver IC, for the time being represented by an ideal voltage dependent voltage source that drives the ideal switch (E2 in 3.5). To obtain this, we can place a Set Reset (SR Latch), with the Reset input

connected to the AND gate output, to get the output at "0" when the two thresholds are exceeded, while the Set Input is connected to the "NOR" output, to achieve a logic "1" at the switch when the current goes below 40 A. The logic behaviour is summarised on the table below (Tab. 3.1).

| Th,h | Th,l | NOR | AND | SR Latch | Gate Driver |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | Set | Gd = 1 |
| 0 | 1 | 0 | 0 | Mem. | |
| 1 | 0 | 0 | 0 | Mem. | |
| 1 | 1 | 0 | 1 | Reset | Gd = 0 |

Table 3.1: First Controller Logic.

The SR Latch is useful to provide a "protecting action" as rejection of disturbances, since it prevents any change at the output of the controller if unexpectedly one of the two bit at the input changes, for example due to switching or environmental noise, as we can observe from the table:

| Th,h | Th,l | NOR | AND | SR Latch | Gate Driver |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | Mem. | Gd(t-1) |
| 1 | 0 | 0 | 0 | Mem. | Gd(t-1) |

Table 3.2: Disturbances rejection of the controller.

At the end of the transient, the controller just stops triggering without any external signal or flag. Indeed,when the load is fully charged, there will be, at some point, an instant in which the current will not increase any more over the lower threshold, since the load at steady state requires less current than $Th_l = 40\,\text{A}$. From that moment on, the switch will remain closed, ideally being transparent.

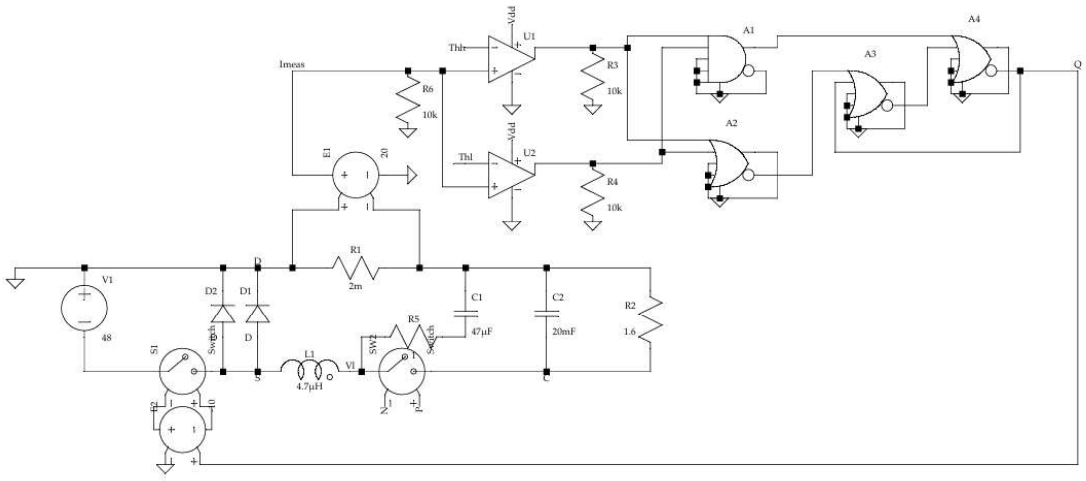



Figure 3.5: First Schematic With Ideal Components.

## 3.2 Circuital Simulation

To test the functionality of the realized system, it has been simulated with LTspice software. At first, the simulations were conducted by taking into account only ideal components, as reported in figure 3.5.In the next sections, the simulations are complicated by adding real components and parasitic behaviours. Since we need to simulate a hot plug event, an ideal switch SW2 that models this behaviour has been added at the load side. When SW2 is closed, it initiates the transient and it has been set to automatically close at 1 us.
In order to observe a real transient behaviour, the initial conditions have been set to:

- Voltage at $C_L = 0\,\mathrm{V}$
- Current in $L = 0\,\mathrm{A}$
- Voltage at $C_1 = 0\,\mathrm{V}$

In the circuit represented in figure 3.5, it is possible to notice a filtering Capacitor $C_1$ which reduces the high frequency ripple towards $C_L$, and it will be useful to close the high frequency loop with a small area (see section 3.5). The reason for this lies in the fact that the load may be somewhat distant from the Inductance L1, and we want to prevent EM noise. A series resistor of value $1\,\Omega$ is added only for simulation reasons, and it will not be present in the real circuit. It prevents current peaks at the start of the simulations, before the insertion of the load (the closure of the switch SW2). In the next figures, (figures 3.6, 3.7, 3.9), the red curve represents the load voltage at $C_L$, $V_o$. The green curve represents the controller output $V_q$ and, lastly the blue one is the inductor current $I_{L1}$

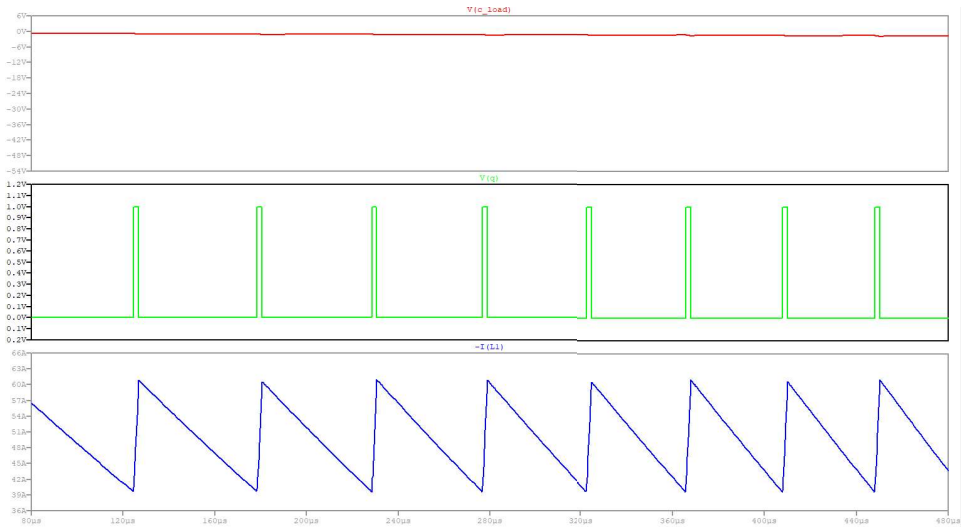



Figure 3.6: Waveforms at the beginning of the transient, ideal circuit (3.5).

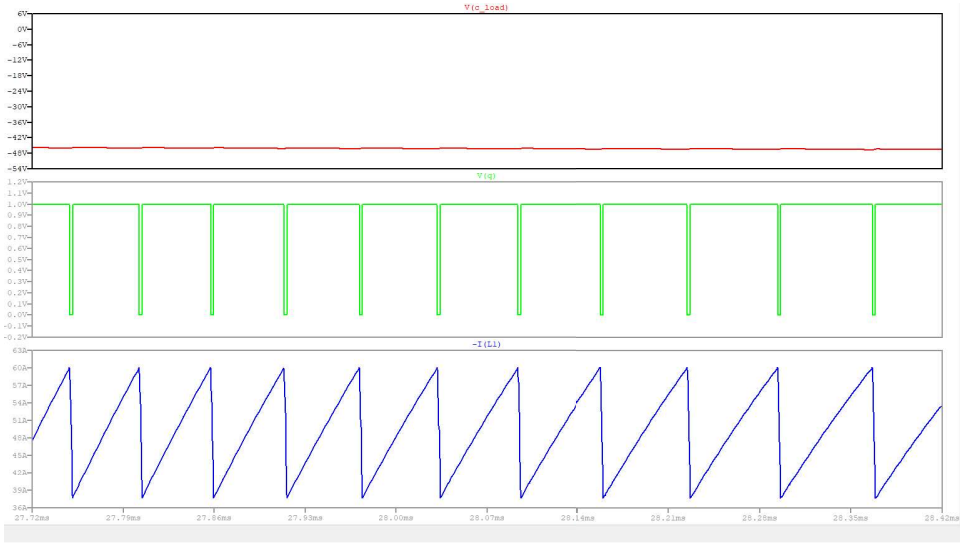



Figure 3.7: Waveforms at the end of the transient, ideal circuit (3.5).

As predicted with the equation derived at 3.1, we can see how the duty cycle ranges between 0 to 1, from the beginning (V(q) controller output in figure 3.6) to the end (V(q) in figure 3.7) of the transient. Concerning the maximum switching frequency, as it is possible to observe from figure 3.8, that it sets around 110 kHz

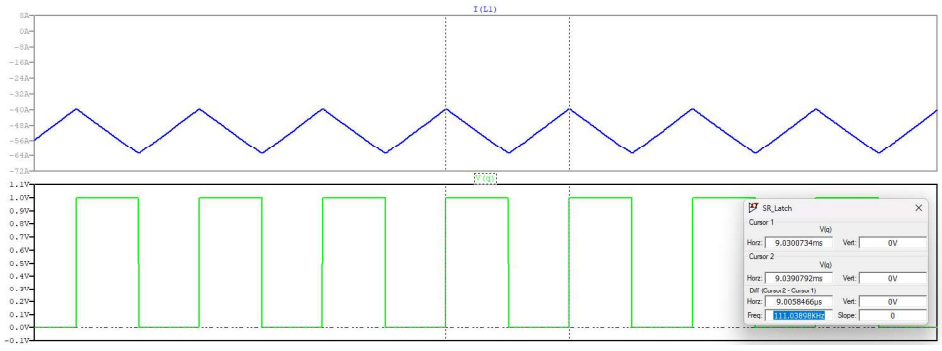



Figure 3.8: Maximum $f_{sw}$ with ideal diode and switch (3.5).

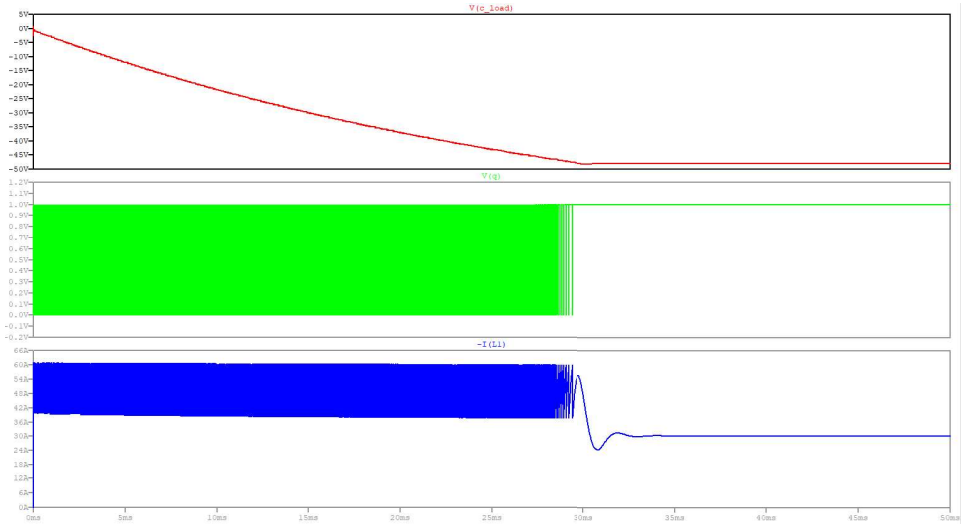



Figure 3.9: Complete Transient Behaviour of the ideal circuit (3.5).

Observing the entirety of the transient, figure (3.9) we can see that the steady state is reached within more or less $30 \div 35$ ms. Some residual oscillations in the inductor current are present, caused by the energy stored during the transient it-self, that is higher than the one at steady state.

## 3.3 Component Selection

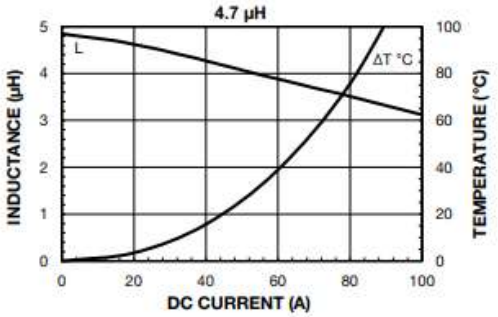
Once the ideal circuit functionality has been proven, we can move towards the real components selection, starting from passive ones and then ending with the active ones. The idea is to realize a prototype Printed Circuit Board (PCB), in order to test the functionalities and to validate what have been simulated. The values of the inductor and of the shunt have already been declared, according to the explanation given in section 3.1. Nevertheless certain precautions must be taken into account in order to select the right component.
In order to correctly choose the inductor, the following parameters must be taken into account, besides its inductance value:

- Equivalent series resistor: DCR $< 1 \div 2\,\text{m}\Omega$.
  As it was previously stated, when the output final voltage is reached, ideally no static power should be dissipated in resistive elements. This value of DCR permits to dissipate less than 1% of the load power, (as explained in 3.1) ;
- Saturation Current: $I_s \geqslant 60\,\text{A}$;
- Performances vs temperature: Since an high current flows in the circuit, we need to be sure that the rise of temperature will not be excessive in order to avoid performance degradation of the inductor.

With these requirements, from Vishay catalogue, the *IHTH-1500MZ-5A* has been selected. From the technical documentation [14] we observe:

| STANDARD ELECTRICAL SPECIFICATIONS | | | | | | |
|---|---|---|---|---|---|---|
| $L_0$ INDUCTANCE ± 20 % AT 100 kHz, 0.25 V, 0 A (µH) | DCR TYP. 25 °C (mΩ) | DCR MAX. 25 °C (mΩ) | HEAT RATING CURRENT DC TYP. (A) (1) | SATURATION CURRENT DC TYP. (A) | | SRF TYP. (MHz) |
| | | | | (2) | (3) | |
| 0.47 | 0.19 | 0.20 | 134.8 | 109.4 | 156.2 | 54.1 |
| 2.2 | 0.51 | 0.54 | 81.7 | 78.9 | 111.4 | 14.7 |
| 4.7 | 1.13 | 1.19 | 60.6 | 60.0 | 90.1 | 9.2 |

(a) IHTH-1500MZ-5A specs, Vishay Datasheet, [14].




(b) Perfomance Graph.

Figure 3.10: IHTH-1500MZ-5A, Vishay Datasheet.

From the last row, the inductance value of 4.7 uH respects all the previous constraints. Looking at the figure 3.32b performance graph, we can appreciate how woth a DC current of $\sim 30\,\text{A}$, the temperature rise will be of $\sim 20\,^\circ\text{C}$. This increase it is acceptable since in any case we will stay under the constraints of negligible static power loss. It should be noticed how we are now referring to the steady state operation, since this represents the 99.999..% of lifetime of our circuit, given that the transient lasts only few milliseconds and it does not influence the temperature.

The next passive component that needs to be selected is the sense resistor. Its main parasitic behaviour is the equivalent series inductance (ESL), which is not precisely defined in the datasheet, given that it is highly dependent on the PCB layout. In order to get a real case scenario, we added a ESL of 5 nH, indicated as the worst case in the documentation, that ensures the ESL to be in the range $0.5 \div 5$ nH

The voltage drop on the ESL is calculated as:

$$v_{ESL} = \frac{\partial I}{\partial t} \cdot ESL_s = \frac{48\,\text{V}}{4.7\,\text{uH}} \cdot 5\,\text{nH} = \frac{10\,\text{A}}{\mu\text{s}} \cdot 5\,\text{nH} \simeq 50\,\text{mV} \tag{3.11}$$

The value of $v_{ESL}$is not negligible compared to the nominal voltage drop on the shunt, which is in the range of $80 \div 120$ mV. Therefore, counteractions must be applied: if this voltage reaches the input of the Sense Amplifier, it will surely cause spurious transitions, making the switching frequency higher due to unexpected commutation at wrong values of the sensed current.

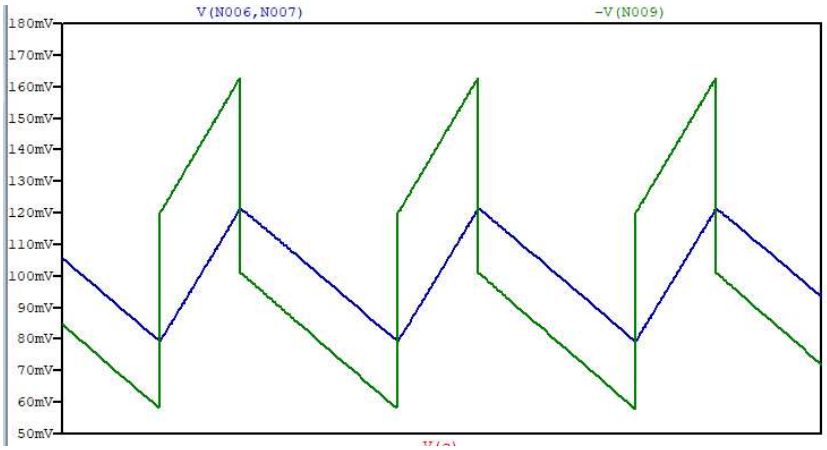



Figure 3.11: ESL parasitic behaviour and filtered shunt voltage drop.

From figure 3.11 it is possible to distinguish between the shunt voltage behaviour due to the ESL (the green curve) and the filtered behaviour (the blue curve), which is more in line with the expectations. In order to get rid of this parasitic phenomenon, and obtaining again the desired behaviour (the blue curve in figure 3.11) we need a low pass RC filter at the input of the sense amplifier. The series of a resistor and an inductor forms a zero at:

$$f_z = \frac{1}{2\pi \frac{L}{R}} = \frac{1}{2\pi \frac{5\,\text{nH}}{2\,\text{m}\Omega}} = 63.7\,\text{kHz} \tag{3.12}$$

Therefore, to compensate, we need to add a pole around the frequency value $f_z$. To reach this objective, we place the cutting frequency of the low pass filter at $f_z$ by employing a differential filter. The differential filter, as it can be appreciated in figure 3.12, is composed by the capacitor C3 and by the resistors R7 and R8. Their values have been

chosen among the standard E6/E12. Through equation 3.13, the cutting frequency is therefore set.

$$f_c = \frac{1}{2\pi 2RC} = \frac{1}{2\pi\ 2 \times 330\,\Omega\ 3.9\,\text{nF}} = 61.83\,\text{kHz} \tag{3.13}$$

The specific values of the components will be tuned during the test and validation of the prototype, remembering that the ESL is a worst case estimation and depends on the PCB layout and the currents paths.

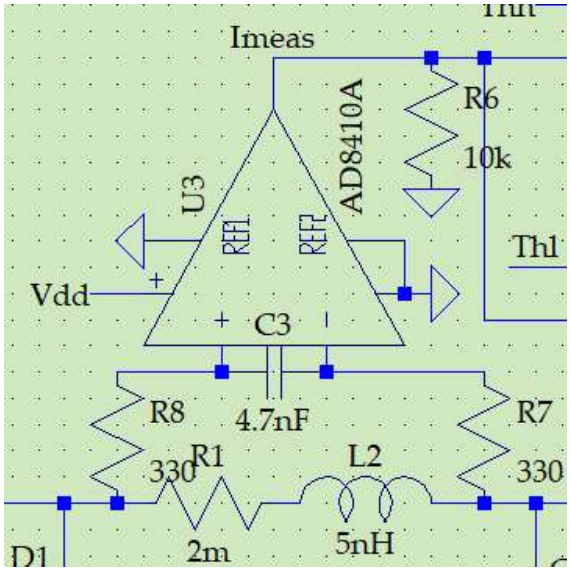



Figure 3.12: Shunt resistor and Sense Amplifier section.

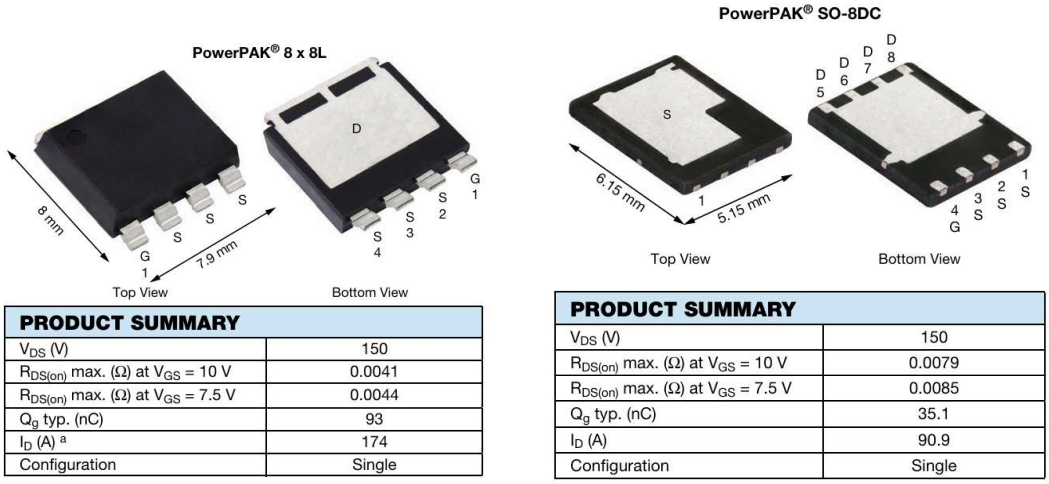
Finally, the shunt resistor must be able to sustain large currents even after the charging phase, as explained in 3.1, from equation 3.5 we can see that it will dissipate a static power of $\simeq 2\,\text{W}$. Therefore the WSLF1206 from Vishay Dale [15] has been chosen. It is a power metal strip current sense resistor, made of FeCrAl, capable of sustaining 4 W of power at a temperature of 70 °C. The resistance value, once again as explained in section 3.1, is of 2 mΩ.

After the selection of the passive components has been carried out, now we can discuss the choice of the diode and the MOSFET. For both of them we have to respect the power dissipation limits and the breakdown voltage requirements.
Starting from the MOSFET, a device with a BVDss greater than 100 V is required. This constraint stems from the backplane supply that has a nominal 48 V. Since some ringing could cause this value to spike and double itself, a BVDss = 150 V has been chosen in order to not avalanche the MOSFET in any condition. Concerning the static power dissipation, it has to be again negligible once the transient is completed and, similarly to all the resistive parasitics in the circuit, it must be:

$$P_{d,static} = R_{ds,on} * I^2_{L,ss} << P_{Load,ss} \simeq 1.5\,\text{kW} \implies P_{d,static} < 0.1\% P_{Load,ss} = 2\,\text{W} \tag{3.14}$$

Figure 3.13: WSLF1206 Surface Mounting Power Shunt Resistor, [15].

Where $I_{L,ss}$ is the steady state load current, whose maximum value is equal to 30 A, while $P_{Load,ss}$ is the corresponding power consumption. In order to get a negligible power loss on the MOSFET, the on-resistance should ideally be of the same order of the shunt magnitude. As explained in the background section 2.1, the FOM that we have to look at is $R_{ds,on} * Q_g$. Two good candidates from Vishay have been taken in consideration, the SiJH5700E [16] and the SiDR570EP [17].




| PRODUCT SUMMARY | |
|---|---|
| $V_{DS}$ (V) | 150 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS}$ = 10 V | 0.0041 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS}$ = 7.5 V | 0.0044 |
| $Q_g$ typ. (nC) | 93 |
| $I_D$ (A) [a] | 174 |
| Configuration | Single |

(a) SiJH5700E package and main characteristics, Vishay Datasheet, [16].

| PRODUCT SUMMARY | |
|---|---|
| $V_{DS}$ (V) | 150 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS}$ = 10 V | 0.0079 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS}$ = 7.5 V | 0.0085 |
| $Q_g$ typ. (nC) | 35.1 |
| $I_D$ (A) | 90.9 |
| Configuration | Single |

(b) SiDR570 package and main characteristics, Vishay Datasheet, [17].

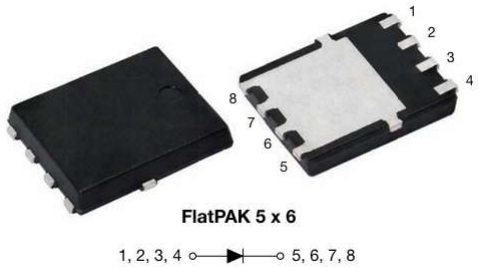
Figure 3.14: SiDR570EP, Vishay Datasheet.

The first one, SiJH5700E, offers the best $R_{ds,on} = 4.1\,\text{m}\Omega$@ 10 V. Unfortunately, the $Q_g$ required to reach a $V_{\text{gs}}$ equal to 10 V is 93 nC. Overall, the SiDR570EP, despite its higher $R_{ds,on} = 7.9\,\text{m}\Omega$@ 10 V, offers a better FOM, leading to a much lower $Q_g$, equal to 31 nC. It also presents a larger current capability at ambient temperature (30.8 A vs 17 A), better junction-to-ambient thermal resistance ($R_{\theta ja} = 20\frac{^\circ\text{C}}{\text{W}}$ **vs** $R_{\theta ja} = 45\frac{^\circ\text{C}}{\text{W}}$ ) and finally a smaller package with also double side cooling.

All these reasons lead to the final choice of the SiDR570EP. But, in order to respect the constraints of negligible power loss, we need to parallelize four of them in order to get the total on resistance of:

$$R_{ds,on} = \frac{7.9}{4}\,\mathrm{m\Omega} = 1.975\,\mathrm{m\Omega} \tag{3.15}$$

The diode selection once again starts with the reverse breakdown voltage larger than 150 V, for the same reason of the BVDss of the MOSFET; then, in order to choose a feasible device, the parameters to look at are: the average forward current $I_{F(AV)}$, the average forward voltage drop $V_F$, the junction capacitance $C_j$ and, finally, the junction-to-ambient thermal resistance $R_{\theta ja}$.




**LINKS TO ADDITIONAL RESOURCES**

3D Models

| PRIMARY CHARACTERISTICS | |
|---|---|
| $I_{F(AV)}$ | 30 A |
| $V_{RRM}$ | 170 V |
| $I_{FSM}$ | 240 A |
| $V_F$ at $I_F$ = 30 A ($T_J$ = 125 °C) | 0.72 V |
| $T_J$ max. | 165 °C |
| Package | FlatPAK 5 x 6 |
| Circuit configuration | Single |

Figure 3.15: V30K170 package and main characteristics, Vishay Datasheet [18].

During the charging phase, the diode should be able to carry the average value of the charging current. From the Vishay catalogue, a candidate like the V30K170 [18] has been chosen. It has an average forward current $I_F = 30\,\mathrm{A}$ with infinite heatsink and $I_F = 3.4\,\mathrm{A}$, if mounted on recommended pad area in free air condition. Therefore, at least two diodes are required in order to carry the average transient charging current:

$$I_{chr} = \frac{I_{Max} + I_{min}}{2} = \frac{(60\,\mathrm{A} + 40\,\mathrm{A})}{2} = 50\,\mathrm{A} \tag{3.16}$$

In order to ensure the functionality of the system and the safety of the diode and of the whole circuit, some thermal computations must be done. From the documentation, the diode has a thermal junction-to-ambience resistance of $R_{\theta ja} = 75\frac{^\circ\mathrm{C}}{\mathrm{W}}$, much larger with

respect to the MOSFET one. To get an approximation of the temperature rise on the single diode during the transient, we need to compute first the power dissipation:

$$P_{d,D} = V_F * I_{avg}(t) + V_{Rev} * I_{leakeage} + (V_D * I_{rr} * t_{rr})\frac{3}{2} f_{sw} \tag{3.17}$$

From the equation, 3.17 it is possible to observe three different contributions. The first one represents the power dissipation during $T_{OFF}$, i.e. when the MOSFETs are open and the diodes are conducting the current as in the graph below (figure 3.16). To simplify the calculations, it is possible to apply a flat top approximation on the conduction losses. Assuming $D = 0.5$ during the whole transient, the obtained conduction losses are:

$$P_{D,cond} = I_{avg} * V_F * (1 - D(t)) < I_{avg} * V_F * (1 - 0.5) = 25\,\text{A} * 0.9\,\text{V} * 0.5 = 11.25\,\text{W} \tag{3.18}$$

The second contribution represents the power dissipation due to leakage current when

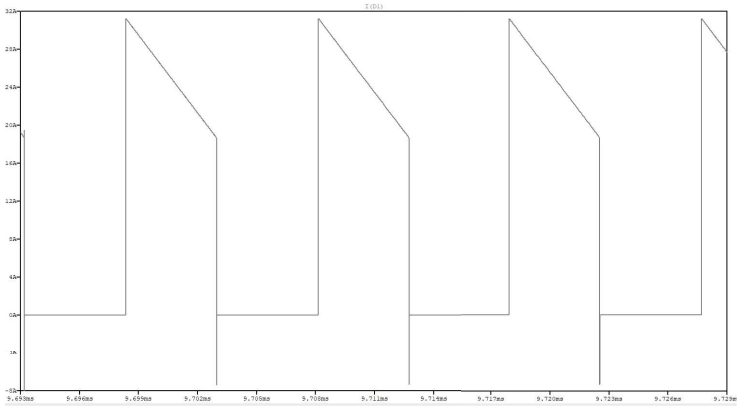


Figure 3.16: Diode Current Waveform during the transient.

the diodes are not conducting, i.e. $T_{ON}$. It could be estimated in the order of mW from the datasheet and it is surely negligible with respect to the conduction power loss just calculated.
The third and last contribution (3.17) represents the switching power losses. During the transition $T_{OFF} \implies T_{ON}$, a reverse current $I_{rr}$ flows in the diodes in order to recharge the $C_j$ during the reverse recovery time $t_{rr}$. This contribution must be taken into account at every transition, and a simple but pessimistic approach is to use the maximum switching frequency found in the simulation above (figure 3.8). The coefficient $\frac{3}{2}$ represents the shaping factor and this whole calculus leads to a switching power losses in the order of hundreds of mW, once again negligible with respect to the conduction losses.
Finally, to obtain an estimation of the temperature rise of the single diode:

$$\begin{aligned} \Delta_{T,D} &= R_{\theta ja} \cdot P_{d,\text{trns}} \simeq R_{\theta ja} \cdot [(V_F \cdot I_F \cdot (1 - D)) + P_{D,\text{sw}}] \\ &= 3\frac{^\circ\text{C}}{\text{W}} \cdot \left[(0.87\,\text{V} \cdot \frac{50\,\text{A}}{2}) + 0.2\,\text{W}\right] \simeq 35\,^\circ\text{C} \end{aligned} \tag{3.19}$$

The thermal resistance is obtained from the documentation: the diodes conduct only for the transient duration. Therefore, it is not correct to use $R_{\theta ja} = 75\frac{^\circ\mathrm{C}}{\mathrm{W}}$ since this value represents a state of continuos conduction. From the graph in figure 3.17, we can extract the value used in the equation above (3.19) of $R_{\theta ja} \simeq 3\frac{^\circ\mathrm{C}}{\mathrm{W}}$. We can assume the pulse duration values on the x-axis as a single pulse of the duration of the charging transient. This value could be approximated, considering a constant charging current of the average value from the hysteresis as:

$$\Delta t = C_L \frac{dV}{I_{avg}} = 20\,\mathrm{mF}\ \frac{48\,\mathrm{V}}{50\,\mathrm{A}} = 19.2\,\mathrm{ms} \tag{3.20}$$

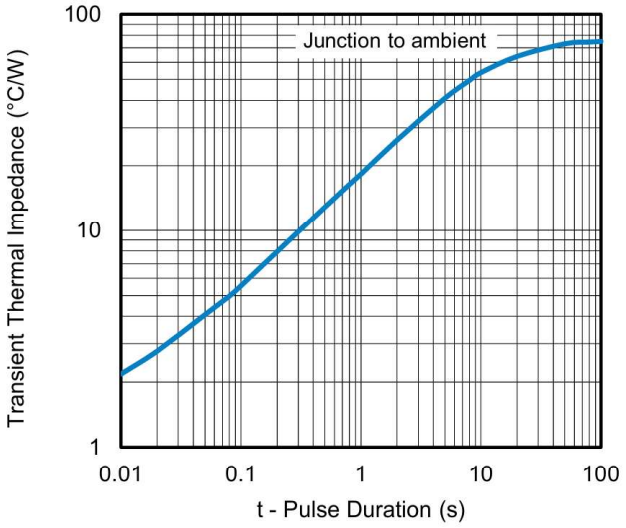



Figure 3.17: Transient Thermal impedance vs Pulse Duration, Vishay Documentation [18].

### 3.3.1 Real Components Simulation

In order to confirm the design and the selection of the components, the circuit has been once again simulated through LTSpice. This time, real model for the diodes and the MOSFET have been employed. Although, not all the simulation model of the components were available, and so similar devices with overlapping characteristics have been used. Even if the model is not exact, this simulation provides some confirmation to the design, since the parasitic behaviours are now taken into account.

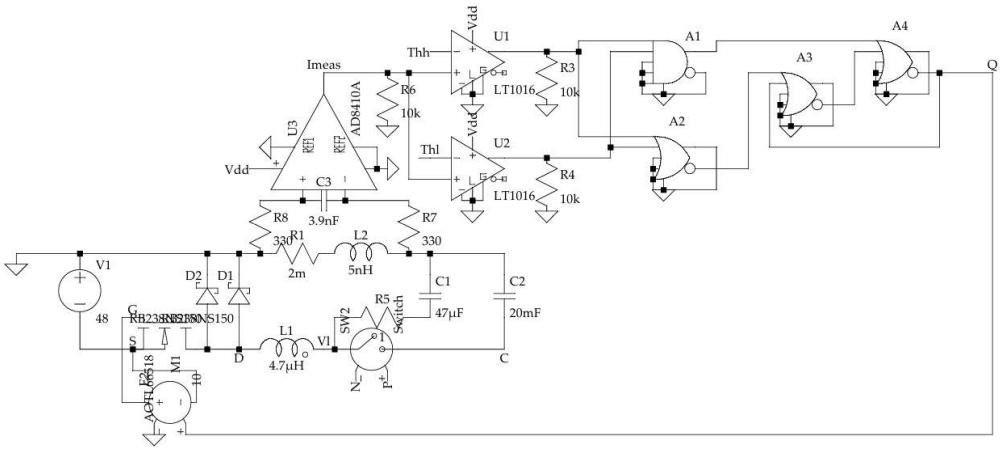



Figure 3.18: Circuit with shunt parasitic, amplifier input filter and real component.

Also in this simulation, the same initial condition and the same behaviour of the plug event have been simulated. From figure 3.18 we can observe the presence of two diodes, for the reason just explained in the section above (3.3.1). Only one MOSFET has been placed, since in this part we do not have yet considered the gate driving circuitry: placing four MOSFETs at this stage would not bring realistic information and it would only make the simulation heavier. The behaviour of the whole circuit remains the same, with the duty cycle and the frequency variation predicted in the equation (3.1) and (3.2).

From figure 3.19 we can observe that the transient extinguishes within the expected time frame from the equation 3.20.
To confirm also the discussion about the power dissipation from equation 3.17 and the consequent temperature rise at the diodes, we exploit the possibility in LTSpice to measure the average and the integral of a waveform inside a time frame.

As shown in figure 3.20, the average power dissipation over the transient on one diode is of $\approx$ 9.7 W, which confirms our over estimation of $\approx$ 11 W, and leads to a $\Delta_{T,D} = 29.1\,^{\circ}\mathrm{C}$.

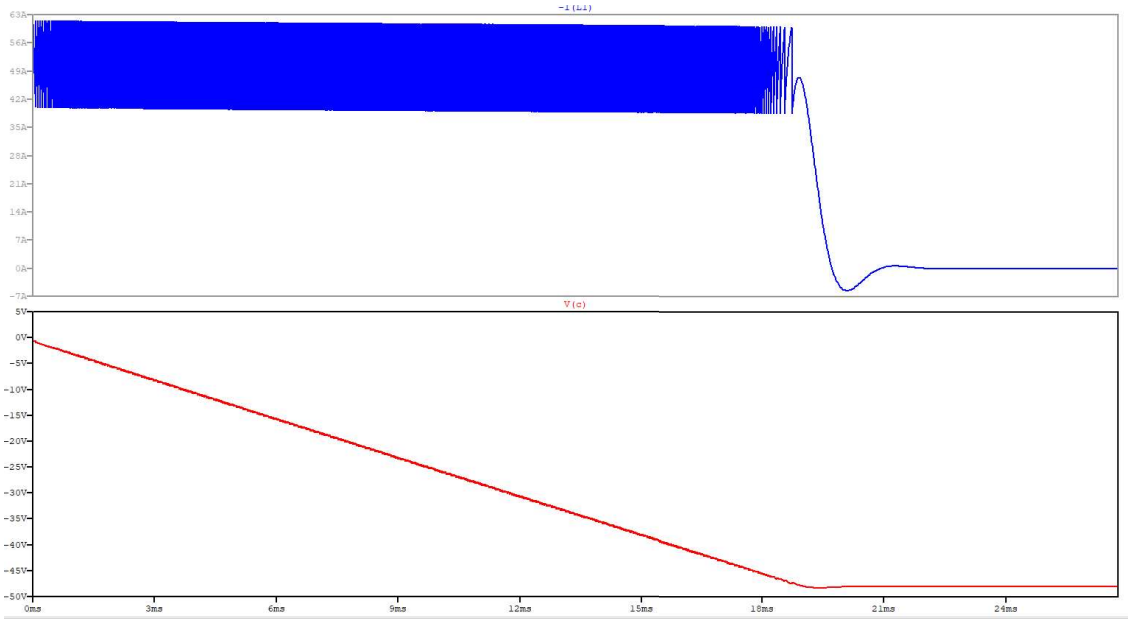


Figure 3.19: Complete transient with real model diodes and MOSFET, parasitic ESL shunt.

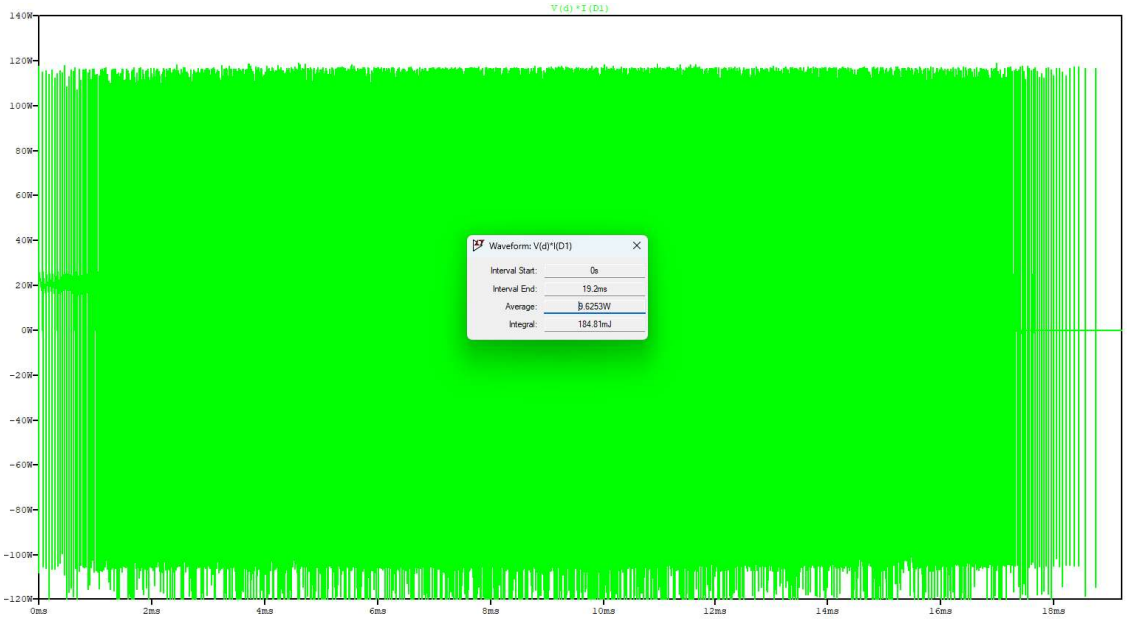



Figure 3.20: LTSpice average and integral on $V_D * I_D$ waveform.

### 3.3.2 Secondary Circuitry and Supplies

In this section the remaining of the circuitry and ICs needed for the implementation of the system will be presented; their related design, if required, will be introduced.

In order to interface with the controller logic, the two comparators associated to the hysteresis thresholds are this time represented with a model of the LT1016 IC from Linear Technologies [19]. It offers one of the best in-class solution for analog comparators, defined by Linear Technologies as "UltraFast Precision 10ns Comparator", ensuring a very fast time response of the loop. The LT1016 also offers the possibility to work on a +5 V single supply, simplifying the power distribution network design. Tight offset voltage specifications and high gain allow the LT1016 to be used in precision applications. Matched complementary outputs further extend the versatility of this comparator, the output stage also provides active drive in both directions for maximum speed into TTL/CMOS logic or passive loads.

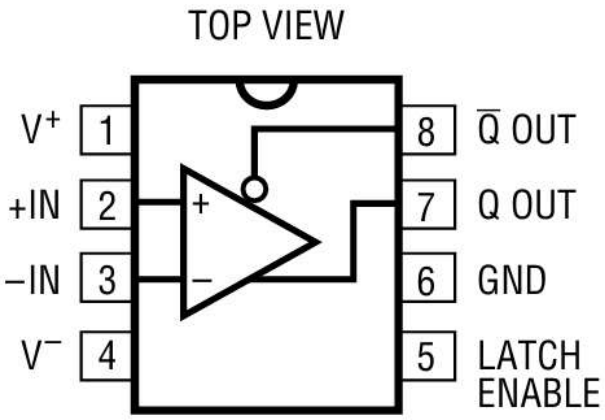
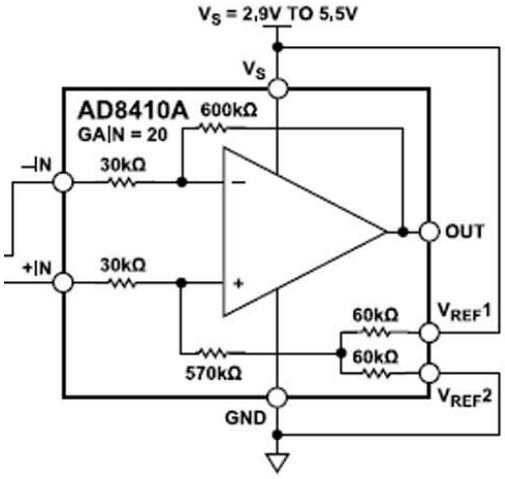



Figure 3.21: LT1016 8-pin package, top view, Linear Technologies Documentation [19].

In figure 3.18 it is possible to notice an AD8410A sense amplifier from Analog Devices [20] that perfectly fits our purpose: the AD8410A is a high voltage, high bandwidth current sense amplifier. The device features an initial gain of 20 V/V, with a 2.2 MHz bandwidth and with a maximum 0.13% gain error over the entire temperature range. The buffered output voltage directly interfaces with any typical converter. The AD8410A performs bidirectional current measurements across a shunt resistor in a variety of industrial and automotive applications. The AD8410A also offers the possibility to move the reference, i.e. the output voltage average value. If the sensed current changes direction, this allows to get all the values around the reference voltage without any negative value. In the circuit design, the amplifier is not stressed for what concerns the power dissipation, however some considerations on the PCB layout will be done in the section (3.5); for what concerns the input filter, other technical discussion is done in section(4).




(a) AD8410A functional scheme, AD Datasheet, [20].


(b) AD8410A package, AD Datasheet, [20].

Figure 3.22: AD8410A, Analog Devices Datasheet.

The fixed gain $G = 20$ of the AD8410A fits exactly the design requirements and avoids the use of external resistors, leading to a cleaner and simpler PCB design. The reference pins will be connected to the ground reference, since we do not need to move the average, and this causes the output to sit at the negative rail when there are zero differential volts at the input.
The system is powered from the $-48\,\mathrm{V}$ backplane but both of this ICs need $5\,\mathrm{V}$ single power supply, so we need to derive the secondary supplies. Two possible solutions have been taken into account, the first one uses the lower rail $-48\,\mathrm{V}$ as the low reference for the ICs, and then derives a $-43\,\mathrm{V}$ rail with a linear or a switching regulator. Although, even if this solution may seem simple, it is not the best one to apply. The sense amplifier needs to read a voltage drop on the shunt that is placed on the ground rail. If the reference of the AD8410A was tied at $-48\,\mathrm{V}$, the Common Mode voltage would be very high, causing problems to the effective readings of the shunt drop.
Therefore, a better solution is to tie the reference of the ICs to the backplane ground rail and then to derive a real $5\,\mathrm{V}$ positive power supply.

To achieve this conversion ratio we need to rely on a SMPS, since a linear regulator could not provide an output voltage higher than the input one. The first idea may be a Buck-Boost since it is an inverting topology. But looking at the position of the switch (in figure 3.23) we would notice some problems.

The source terminal of the MOSFET is connected to the output voltage. This means that an high-side driving, which requires a positive voltage above the ground level, will be needed, leading to complications of the design. It could be possible to move the switch position to the low rail, but this lead to a complete redesign of the converter, closing the possibility to use a standard IC controller.

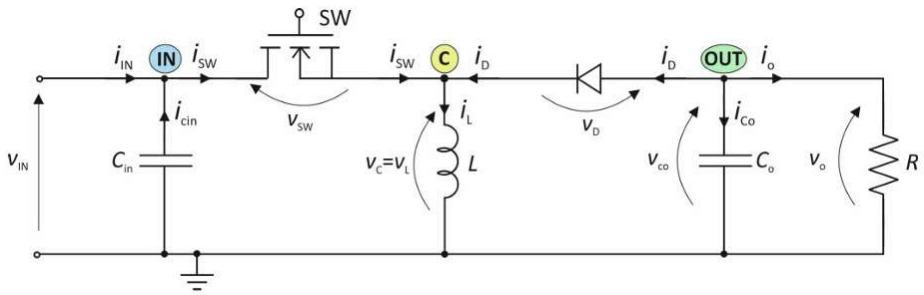
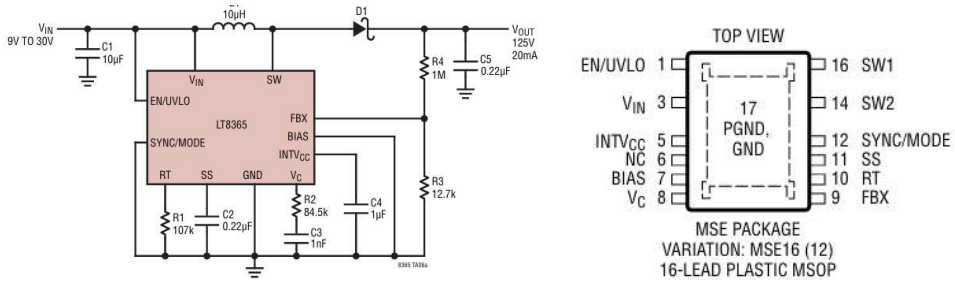



Figure 3.23: Buck-Boost topology.

Therefore, another idea must be exploited in order to employ an existing IC and avoid the design of a new controller. One possible solution is is to adapt a standard boost topology to the purpose, boosting the output voltage up to 53 V but with 5 V of this above the shared positive ground rail. This will be possible trough a level shift of the feedback voltage, that will force the controller to maintain the output voltage regardless of what is the reference.
So, in order to maintain a simple PCB design, an IC with an integrated switch will be selected. From the Linear Technologies catalogue, we choose the LT8365 [21], that is a current mode DC/DC converter with a 1.5 A, 150 V switch operating from a 2.8 V to 60 V input. With a unique single feedback pin architecture it is capable of Boost, SEPIC or inverting configurations. Burst Mode operation consumes as low as 9 µA quiescent current to maintain high efficiency at very low output currents, while keeping typical output ripple below 15 mV. An external compensation pin allows optimization of loop bandwidth over a wide range of input and output voltages and programmable switching frequencies between 100 kHz and 500 kHz. A SYNC/MODE pin allows synchronization to an external clock. It can also be used to select between burst or pulse-skipping modes of operation with or without spread spectrum frequency modulation for low EMI. For increased efficiency, a BIAS pin can accept a second input to supply the INTVCC regulator. Additional features include frequency foldback and programmable soft-start to control inductor current during startup. The LT8365 is available in a thermally enhanced 16-lead MSOP package with four pins removed for high voltage pin spacings.

The design of the passive components needed to the correct functioning of the LT8365 have been carried out following the Datasheet indications. The converter has been set to work in Discontinuous Conduction Mode (DCM). Even if the duty cycle limitation would allow the Continuos Conduction Mode (CCM), it is preferable to work in DCM, since it provides more stability. The MODE pin has then been tied to the lowest reference, forcing the converter in Burst Mode, providing low ripple and enhancing efficiency at light load. The SS pin provides the soft startup behaviour by limiting the current that flows through the inductor by closing the switch, allowing the output capacitor to be charged gradually towards its final value while limiting the start-up peak current. The RT pin is connected to a resistance that set the switching frequency of the converter. In order to limit the EMI this has been set to work at the minimum switching frequency, even if this requires higher value of inductance and output capacitance, but this will not represent a




(a) LT8365 example Boost configuration, LT Datasheet, [21].

(b) LT8365 package, LT Datasheet, [21].

Figure 3.24: LT8365, Linear Technologies Datasheet.

problem, since the maximum current load has a low value. The bypassing capacitors and the compensation network have been set following the datasheet recommendations.

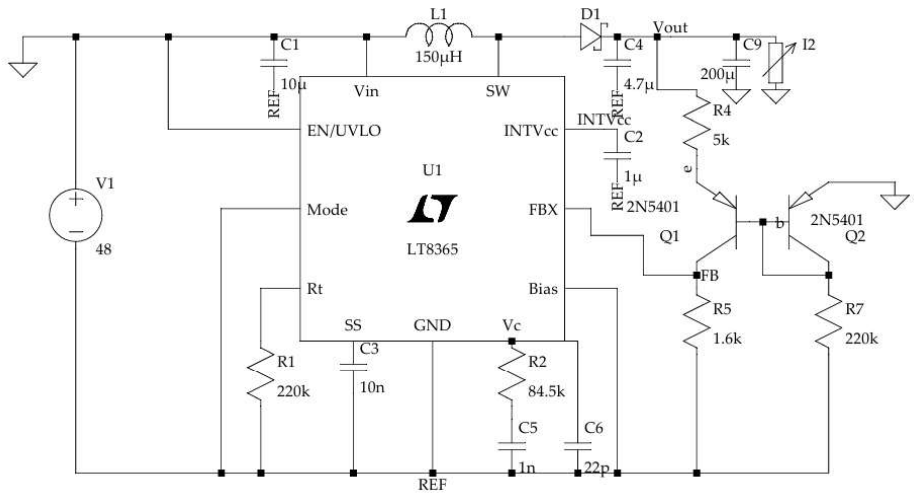



Figure 3.25: LTSpice Schematic of the LT8365.

The LT8365 is capable of generating either a positive or negative output voltage with a single FBX pin. It can be configured as a boost or SEPIC converter in order to generate a positive output voltage, or as an inverting converter in order to generate a negative output voltage. When configured as a Boost converter, the FBX pin is pulled up to the internal bias voltage of 1.60 V by a voltage divider (R1 and R2) connected from VOUT to GND.

Since we need to level shift the output, we will not simply connect a resistive network to the FBX pin but, in order to provide a 1.60 V and to maintain a 5 V output, the network on the output side of the figure 3.25 has been implemented.
As it is possible to observe, $Q_1$ and $Q_2$ have been connected in such a way that the emitter (e node in figure 3.25) is always at 0 V, forcing the emitter current through $R_4$ at 1 mA. Then the collector current through $R_5$ will be equal to the emitter one minus

a negligible base current. The value of $R_5$ is easily set at 1.6 kΩ, once the current that flows in the network has been imposed. The transistor $Q_1$ must be able to sustain at least $V_{ce,bd} > 48\,\text{V} - 1.60\,\text{V}$. To be coherent with the rest of the design, the MMBT5401LT3G from OnSemi [22] has been chosen, with a breakdown voltage of 150 V. The same considerations are valid for$Q_2$ (connected in a diode configuration), that has the role of compensating eventual drops of the $V_{e,b}$ with temperature rise. It also allows a simpler resistive network design by fixing the $e$ node at 0 V.

The output capacitor has been chosen respecting the advice from the datasheet. A ceramic X5R/X7R provides the best ripple and load current capability with the lowest ESR. A Murata MLCC X5R (GRM32ER61A107ME20K) has been chosen among the recommended ones [23].

The exact values of all the passive components have been then tuned during the simulation, since the model of the LT8365 is available in LTSpice.

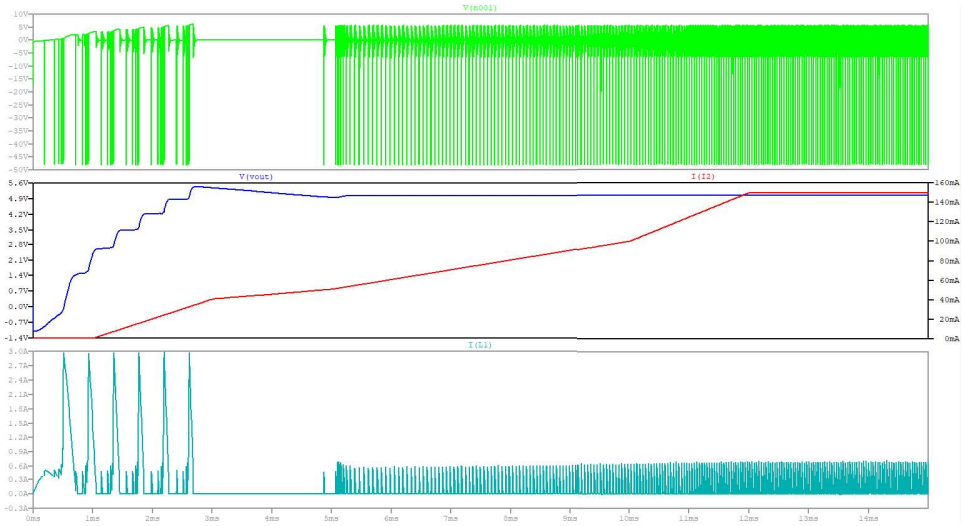



Figure 3.26: LTSpice simulation of the LT8365 design.

The power supply has been tested with a load current more than doubled with respect to the one expected, proving the robustness of the design.
From figure 3.26 we can observe a complete simulation waveform: the first plot (the green curve) represents the voltage on the SW1 and the SW2 pins of the LT8365. It confirms that the converter is working in DCM from the oscillation between one period and the other. In the second plot we can observe the output voltage (blue curve) and the output load current (red curve). Finally, the third plot shows the current in the inductor.

Figure 3.27 focuses on the the start-up section: we can observe the output voltage rising, while the inductor current is being limited.

In figure 3.28, it is possible to observe the behaviour of the SMPS design at maximum

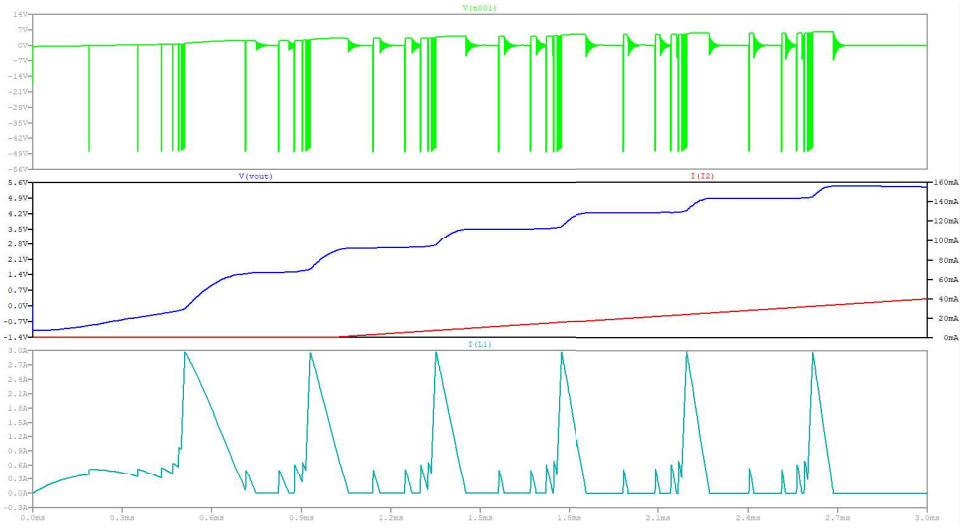



Figure 3.27: LTSpice simulation of the LT8365 design, Start-up behaviour.

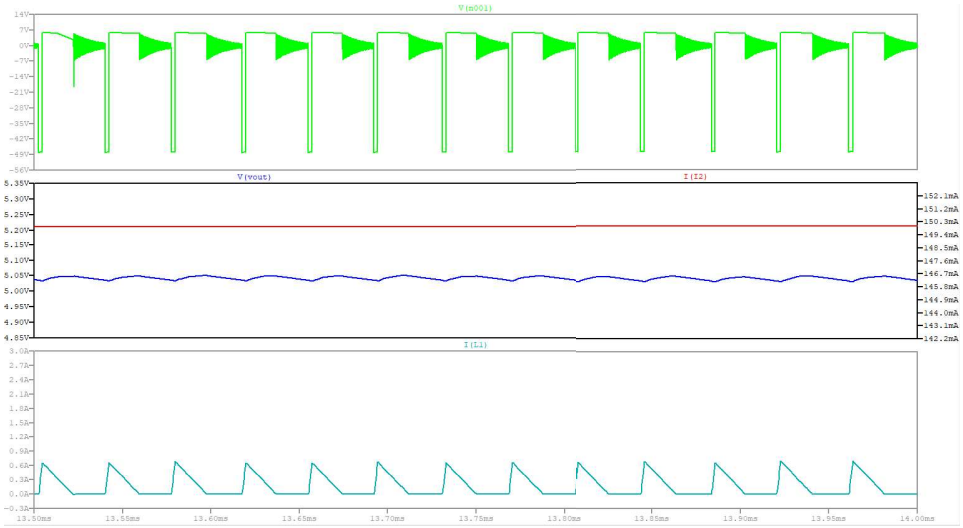
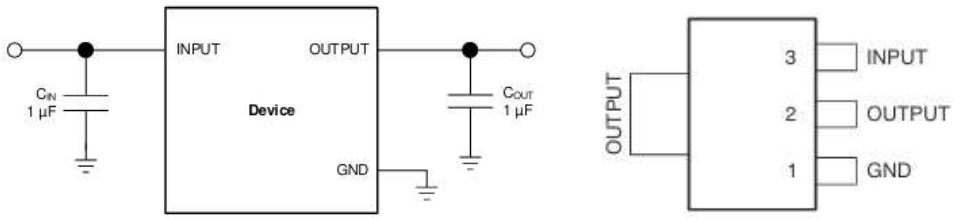



Figure 3.28: LTSpice simulation of the LT8365 design, Maximum load condition.

load condition, which is actually overestimated on purpose, proving that the output voltage remains stable and the ripple acceptable. Therefore, we can conclude that the switching power supply design is validated through these simulations.

The 5 V supply must be able to provide power to the sense amplifier and the fast comparator. Instead, the controller logic will run on 3.3 V. This other power supply is derived from the just designed 5 V unit, using a simpler linear regulator.
The TLV1117LV33DC [24] from Texas Instrument is a tiny and inexpensive low-dropout linear voltage regulator. It offers a fixed output voltage of 3.3 V and a discrete load current capability of 1 A, with very low quiescent voltage and good stability with a cost-effective ceramic output capacitor. The high Power Supply Rejection Ratio (PSRR) of

75 dB enables use of the device for post regulation after a switching regulator, as in our case. Other valuable features include low output noise and low-dropout voltage.




(a) TLV1117 example configuration, TI Datasheet, [24].

(b) TLV1117 package, TI Datasheet, [24].

Figure 3.29: TLV1117, Texas Instrument Datasheet.

The simulation of the TLV1117 has been omitted as the model is not available in any circuit simulator. Nevertheless, its capabilities are more than sufficient for our purposes, and there is no need to design any external components. The linear regulator has to supply the digital logic section, which will be implemented on an FPGA (see next section 3.4), and the analogue section, represented by the analogue-to-digital converter and the associated active input filter.
For this reason, the supply for the two sections is derived from the TLV1117, the analog section being filtered in order to remove the noise from the digital section.

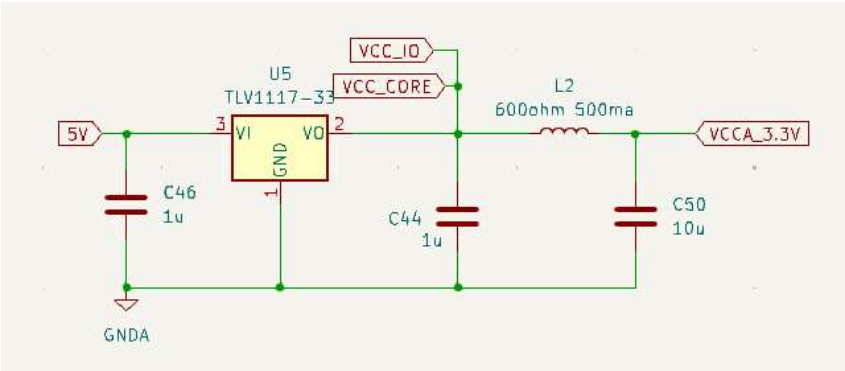



Figure 3.30: Schematic of the TLV1117, Digital and Analog section.

From figure 3.30 it is possible to observe the subdivision of the two power supply sections. VCCA_3.3V is the filtered supply for analog section, while VCC_core and VCC_IO are the digital supplies, that will be discussed in further details in the next section.

The last two components that must be addressed are the gate driver IC and its related power supply. In order to drive the four power MOSFETs, a driver is certainly required. It is not possible to employ a direct driving technique, since it would affect the switching performance. Furthermore, we need to remind that the logic is referred to the gnd level

while the source of the MOSFETs is connected to the lowest $-48$ V reference: this will also force the choice of an isolated gate driver.

The ADuM4120 is 2 A isolated, single-channel driver with isolation up to 5 kV rms thanks to the increased creepage inside the wide body 6-lead SOIC package. The galvanic isolation is provided through a pulse transformer. The ADuM4120 operates with input supplies ranging from 2.5 V to 6.5 V, allowing to be powered from the 5 V SMPS or the post-regulated 3.3 V.

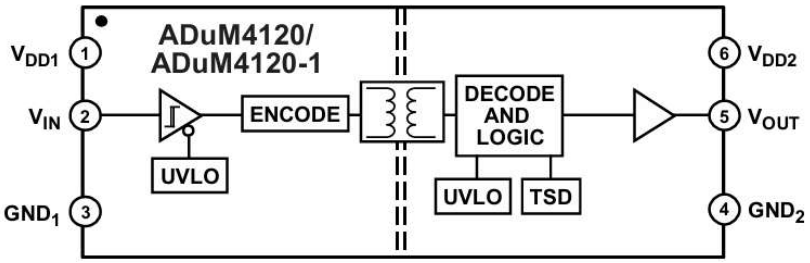



Figure 3.31: ADuM4120 Functional block diagram, Analog Devices [25].

In order to check if the peak current capability of 2.3 A of the ADuM is compatible with the circuit, we can construct an equivalent model of the four different gate loops, one for each MOSFET. Starting from the characteristics of these, we need an estimation of the input capacitances which are seen by the driver as a load. From the SiDR570 Datasheet, looking at the graph of $Q_g$ vs $V_{\text{gs}}$ it is possible to estimate a $Q_g = 50\,\text{nC}$ at $V_{\text{gs}} = 12\,\text{V}$, that will be the output stage driver supply, VDD2 in figure 3.31 .
From this, the equivalent load capacitance of a single MOSFET is:

$$C_{\text{gs,eq}} = \frac{Q_g}{V_{gs}} = \frac{50\,\text{nC}}{12\,\text{V}} = 4.167\,\text{nF} \tag{3.21}$$

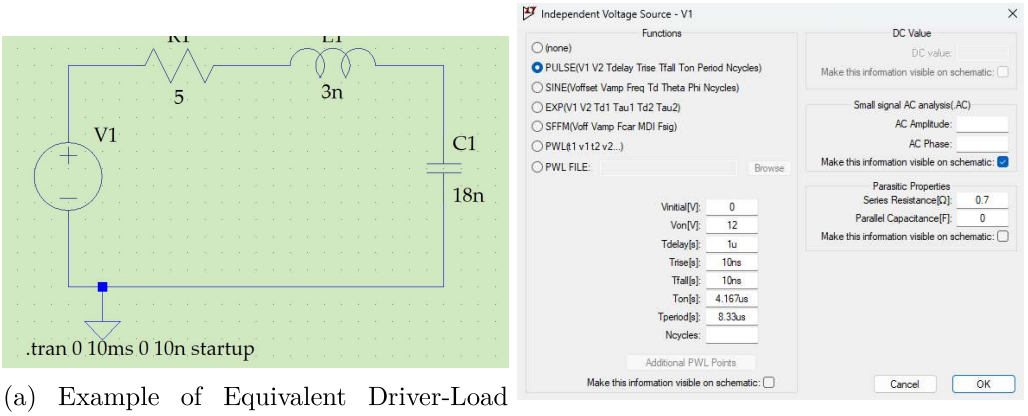
We can consider a capacitance of 4.5 nF in order to have some margin and increase the robustness of the design.

The total load capacitance seen by the driver will be four times the estimated one.

$$C_{\text{L,eq}} = C_{\text{gs,eq}} \times 4 = 18\,\text{nF} \tag{3.22}$$

The maximum switching frequency of the designed circuit is in the order of 120 kHz and the corresponding period is of $T_{min} = 8.33$ µs. Therefore, the turn-on and turn-off delays of the MOSFETs transition must be negligible with respect to $T_{min}$, setting the minimum required voltage slope on the load capacitance. This constraint must be respected but without exceeding the maximum peak current of the driver, avoiding the damaging of its output stage.
The load loop must comprehend also the output resistance of the driver and an estimation of the PCB trace inductance in order to represent a real behaviour.

This loop has been simulated through LTSpice, emulating the driver characteristics on a voltage pulse generator.




(a) Example of Equivalent Driver-Load loop.

(b) Square Pulse voltage generator driver.

Figure 3.32: LTSpice driver-load loop.

The rise time of the driver of 10 ns, reported in figure 3.32, has been extracted from the ADuM datasheet. It represents the worst-case scenario, as the minimum rise time is related to the maximum current. The output series resistors of the driver have been derived from the datasheet through an arithmetical mean of the two provided: respectively the one for the current source (off to on transition) and the one for the current sink (on to off transition).
The inductance inserted in the loop represents the parallel of the four PCB trace parasitics, estimated to be in the order of some nH. The resistor (R1 in figure 3.32) is our design focus: it represents the parallel of the four external gate resistances, one for each MOSFET gate terminal. This is the element that limits the current peaks and its value has been fixed, through an iterative simulation, at:

$$R_{eq} = 5\,\Omega \tag{3.23}$$

Leading to a peak current of $< 2$ A, as it is possible to observe in figure 3.33.

The $R_{eq}$ represents the equivalent resistance seen by the driver output, it is the parallel of the four gate resistances. In first approximation we can consider the four resistances equal to 20 Ω, the exact value is then tuned during the test and validation of the prototype board, based on the real parasitic behaviours. The resistances, inductances and capacitances also set the $Q$ parameter of every loop. This aspect will be discussed in more details during the tuning of the components. The input and output capacitors have been fixed following the datasheet recommendation.

Lastly, in order to obtain an estimation of the power consumption of the gate driver, we can overestimate the switching frequency as the maximum of $f_s = 120\,\text{kHz}$, and the total charge handled by the output stage of $Q_t = 4 \times 50\,\text{nC}$, deriving the current during the switching transient as:

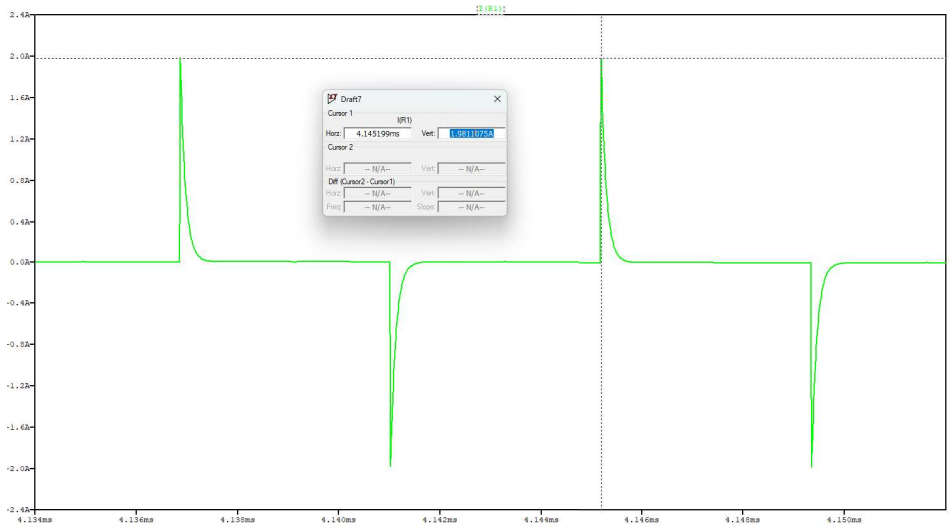


Figure 3.33: Peak driver current.

$$I_t = Q_t \times f_s = 200\,\text{nC} \times 120\,\text{kHz} \simeq 25\,\text{mA} \tag{3.24}$$

Deriving the power consumption as:

$$P_{Dr} = V_{DD2} \times I_t \simeq 0.3\,\text{W} \tag{3.25}$$

From the datasheet safe limiting power graph can be appreciated in figure 3.34, we can conclude that this value in no way represents a thermal problem.

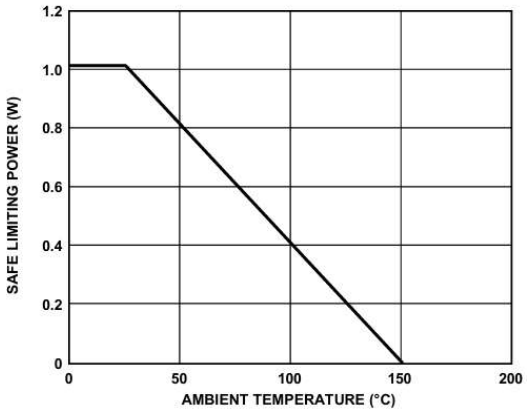



Figure 3.34: Safe Limit Power ADuM4120, AD datasheet [25].

Finally, the last circuitry needed is the 12 V supply that powers the output stage of the Gate Driver. For the reasons explained above, regarding the isolation and the reference of the MOSFETs source, we must refer this supply to the −48 V. Since the gate driver is not demanding in terms of power, we can derive the supply through a high

voltage linear regulator. Even if it is not the best in class in terms of efficiency, it is of simple implementation and inexpensive. Finally, we must consider that it has to provide power only during the hot swap event, i.e. $\sim 20$ ms.
The TL783 device is an adjustable three-terminal high-voltage regulator with an output that ranges from 1.25 V to 125 V and a DMOS output transistor capable of sourcing more than 700 mA. It is designed for use in high-voltage applications where standard bipolar regulators cannot be used.

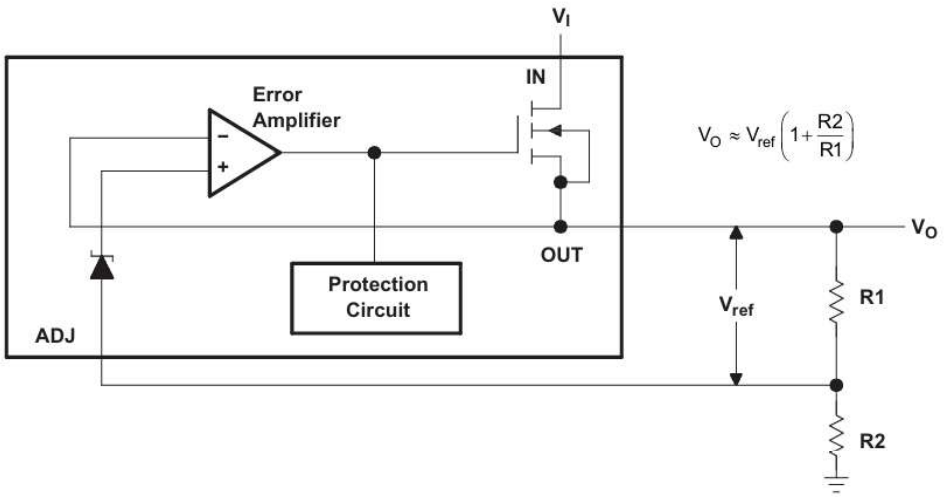



Figure 3.35: TL783 simplified schematic, Texas Instrument [26].

The output regulation is achieved trough an external resistor divider feedback to the adjust pin. The values of the resistors can be found from the equation reported:

$$V_o = V_{ref}(1 + \frac{R_2}{R_1}) + I_{ADJ} \quad R_2 \tag{3.26}$$

From datasheet: $V_{ref} = 1.26\,\text{V}$, $I_{ADJ} = 85\,\mu\text{A}$.

The linear regulator needs a minimum output load current to maintain regulation, from figure 8 of the datasheet: $I_{min} > 8\,\text{mA}$. This sets the maximum value of the resistor feedback. 10 mA has been chosen for sake of simplicity, leading to a maximum value of $(R_1 + R_2) < 1.1\,\text{k}\Omega$. Imposing $R_1 = 100\,\Omega$, we can find the ratio $\frac{R_2}{R_1}$ by reversing the equation 3.26, finding 8.5, setting $R_2 = 850\Omega$. The input and output capacitors have been fixed following the datasheet recommendation.

Finally, the last simulation is conducted, including the gate driver and the effective number of MOSFETs and diodes.

From figure 3.36 it is possible to appreciate the presence of the four MOSFETs, as explained in 3.3.1, to achieve the transparency requirements, i.e. negligible power losses,

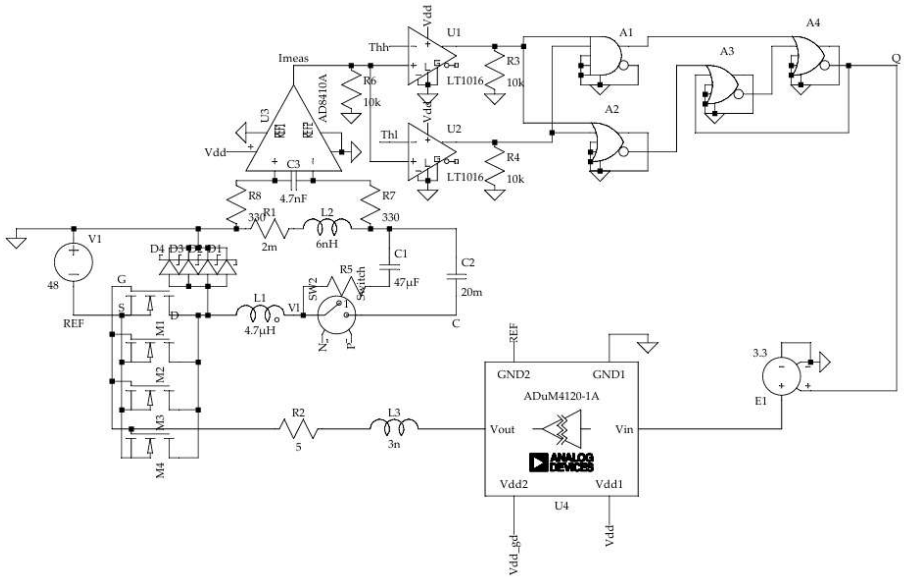



Figure 3.36: Final simulated circuit.

when the transient is completed.
This time, four diodes has been placed instead of the two predicted in section 3.3.1. In this way the current is more evenly divided leading to lower temperature rise. Furthermore, the two extra diodes ensure better short circuit capability as it will be explained in the circuit protections section 3.4. These two extra diodes may cause slightly higher switching losses, since now the total junction capacitance $C_j$ is doubled; but, as it can be seen in the calculations above (3.17), these losses will be in any case negligible.

The final simulation result is showed in figure 3.37.

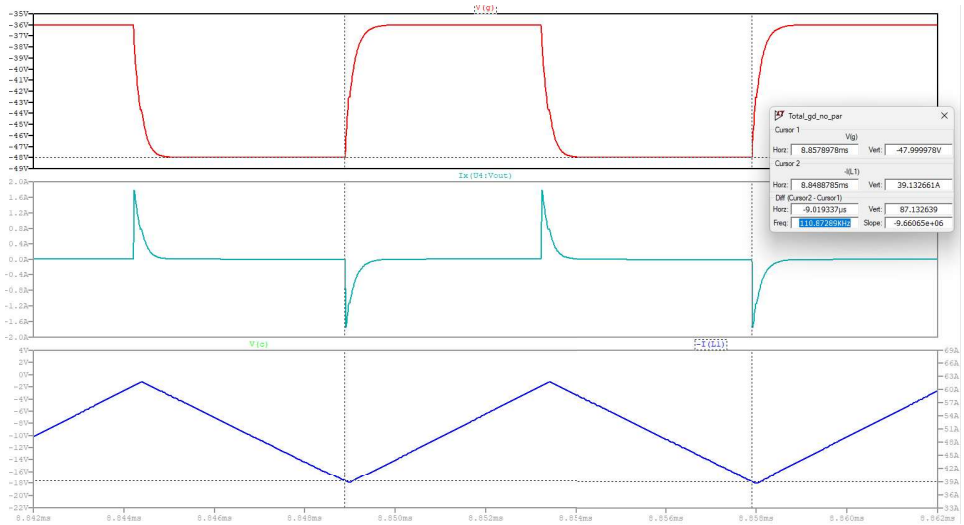


Figure 3.37: Final Simulation results.

From figure 3.37 it is possible to observe that:

1. The gate voltage $V_g$ in the first plot in red has rise and fall time negligible with respect to the switching period, ensuring the correct functionality of the system.
2. The Gate driver peak current, in the second plot, is below the datasheet limit of 2 A.
3. The inductor current, third plot blue curve, remains within the assigned range of values, the current hysteresis $\Delta H$ .
4. The maximum switching frequency is, as predicted, of 110 kHz.

All the project constrains have been respected by the simulated system, closing successfully the circuit design and simulation section.
In the next section the controller strategy and the circuit protection are implemented.

## 3.4 FPGA Solutions

The focus of this section is on the implementation of the controller logic, which has so far been represented simply by four logic gates.
In a real scenario, we have to implement not only the hysteresis control strategy, but also all the related protection and secondary digital components.

In order to implement the logic circuitry, a Field Programmable Gate Array has been chosen. It offers better performances and more flexibility compared to a microcontroller. Furthermore, the particular selected model, from the Intel Altera MAX10 family, offers key features that tipped the scales in its favour: this device family is based on flash ROM which is optimized for non-volatile integration in a Programmable Logic Deivce (PLD) and offers a instant-on feature, faster than the SRAM FPGAs that requires a longer configuration when turned on. The secure on-die flash memory enables device configuration in less than 10 ms: MAX 10 FPGAs can be the first usable device on a system board to control the bring-up of other components. Another very interesting key feature is the presence of Hard and Soft Intellectual Properties (IP) cores, that can be easily implemented in the design. One of the Hard IP core is the Analog to Digital Converter (ADC), that opens different possibilities for the Hysteresis current control implementation.
The MAX10 10M08 in the package E144 allows easy soldering on the prototype board and offers more than enough logic elements (8000) for our purpose. It requires single power supply, saving board space and costs. It represents a cost-effective solution, especially if the internal ADC is used, as it will be explained in the dedicated section 3.4.2, since it cuts the cost of the external analog comparator LT1016.


Figure 3.38: Altera MAX10 144QFP package.

The FPGA has to implement the controller behaviour described in 3.1 that, as demonstrated from the latest simulation, it is very effective despite its simplicity. The main control behaviour is therefore achieved with the same previously employed combinational logic that has at the input side the outputs of the two LT1016 analog comparators while it drives the ADuM4120 at the output side.
A Finite State Machine (FSM) is implemented in order to manage the circuital protections and the secondary functions.
Starting from the secondary functions, a PWM generator has been included to provide the two thresholds $Th_h$ and $Th_l$ to the analog comparators. The PWM generator allows to extract different average voltage levels through the Duty Cycle modulation of a square wave, as showed in figure 3.39.

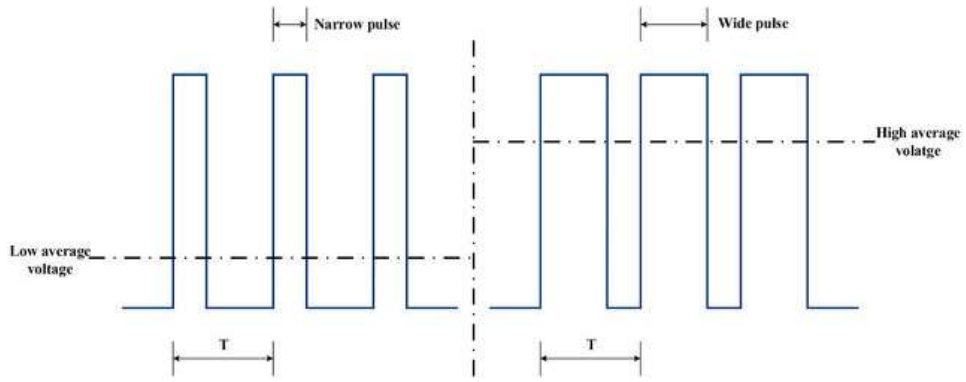



Figure 3.39: Average value of different PWM waveform, [27].

This component is implemented trough a 10-bit counter and two digital comparators: the value of the free-running counter is compared to the corresponding preset thresholds of 1.8 V and 2.4 V. A related output pin is taken at "1" (i.e. $V_{dd} = 3.3\,\mathrm{V}$) until the related threshold is reached. Then, the pin is set to "0" until the end of the period, generating in this way the two waveforms. The values of the thresholds transposed in the digital domain are obtained as follows:

$$V_{LSB} = \frac{V_{dd}}{2^{10}} = \frac{3.3\,\mathrm{V}}{1024} = 3.22\,\mathrm{mV} \tag{3.27}$$

$$Th_{l,d} = \lfloor \frac{1.8\,\mathrm{V}}{3.22\,\mathrm{mV}} \rfloor = 558 \tag{3.28}$$

$$Th_{g,d} = \lfloor \frac{2.4\,\mathrm{V}}{3.22\,\mathrm{mV}} \rfloor = 746 \tag{3.29}$$

In this way we can feed two very accurate thresholds to the external LT1016 comparator, extracted from the average value of the waveforms through a low pass filter.
The PWM generator has been described as a behavioural architecture in VHDL and its functionality has been tested using ModelSim. For the sake of brevity, they have not been reported.

The FPGA allows the first circuital protection, i.e. frequency foldback, to be easily implemented. If the measured switching frequency rises above a defined value, the lower threshold can be reduced by the control FSM through a dedicated input, in order to prevent high EMI emissions. The Register Transfer Level (RTL) view of the PWM generator with the frequency foldback protection is reported in figure 3.40. The active-low reset and the clock signal are provided externally.

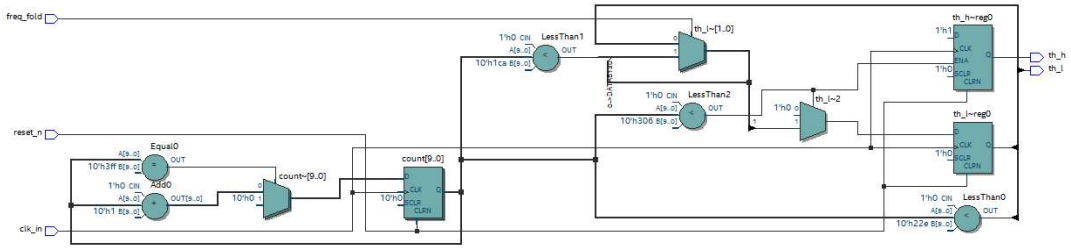



Figure 3.40: RTL view of PWM generator, Quartus Prime.

The switching frequency is measured at the output of the combinational logic, i.e at the gate driver input. These measurements will be strictly necessary to the implementation of the protection against load short circuit. The frequency meter works in the following way: the first rising edge of the measured waveform triggers the start of a known frequency counter while, respectively, the second rising edge stops it. This function is implemented through a T-Flip Flop, with the enable input set to "1" and the clock input represented by the measuring signal $Q_{meas}$ in figure 3.41). The output enables and disables the known frequency counter.

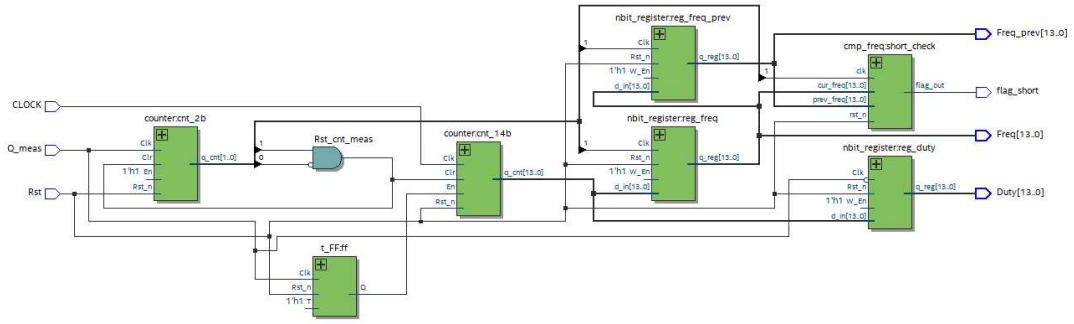



Figure 3.41: RTL view of the frequency meter, Quartus Prime.

A 2-bit counter is used to count the number of rising edges of the waveform $Q_{meas}$, then a AND logic gate asserts the store and clear of the counters value when two edges of $Q_{meas}$ are counted. The value of the core counter(cnt_14b in figure 3.41) is stored in a register and it is then synchronously cleared at the next CLOCK front. The clock frequency of the system is of 50 MHz, for this reason the core counter has been designed with 14-bit:

$$T_{ck} = \frac{1}{50\,\text{MHz}} = 20\,\text{ns} \tag{3.30}$$

Consequently the lowest frequency detectable is of:

$$T_{max} = 1/(2^{14} \times 20\,\text{ns}) \simeq 3\,\text{kHz} \tag{3.31}$$

This design permits also the duty cycle measurements, but in the following it has not been used. In a future perspective it could be useful to implement other circuital protection, like a diode thermal protection, or to implement different and more complicated control strategies.
When the write of a new frequency value is triggered, it is stored in *reg_freq* and the previous value is stored in *reg_freq_prev*; this is done in order to implement the most important circuital protection, the load short circuit prevention.

### 3.4.1 Load short-circuit protection

If the load side of the hot swap controller is closed on a short or if the load fails, the average value of the current in the diodes will rise, possibly leading to the thermal breakdown. This is the reason why four diodes have been placed instead of two in 3.36: to enhance the robustness of the design during hot short events. During these events, the duty cycle will settle to a very low value, forcing the diode conduction for almost the entirety of the switching period.
Anyway, this event could be prevented by measuring the difference of the actual and the previously measured frequency. Indeed, if the load is shorted, the switching frequency will remain always the same, differently from what happens in the normal operation of the circuit (see the frequency behaviour in the eq. 3.2). If several consecutive occurrences of same $f_{sw}$ are detected, the FSM forces the gate driver input to "0" until a reset of the whole system is triggered, stopping the current flow and preventing the diodes failure (no auto-retry features have been implemented). The VHDL description of the component is verified trough ModelSim, as shown in figure 3.42. As the number of occurrences of the same frequency measurements grows to a fixed value, 10 in this case, the status signal *flag_short* is asserted and consequently the FSM will take action. The component allows to reprogram the tolerance, i.e the difference between the measured frequency and the previous one, and the number of occurrences of being below this tolerance, in case of change of the external passive components.
In any case, the diodes will anyway have to conduct an high current for a number of periods equal to the consecutive occurrences that we will set to detect a short.
Stressing again the importance of being redundant on the diodes capabilities, we can observe the waveform during a load short failure:

As it is possible to appreciate from the figure 3.43, the switching frequency is now constant and the duty cycle is very close to "0", hence meaning that the diodes are more or less carrying the entirety of the current. The power dissipation on one diode, during the short event, has been calculated with LTSpice:

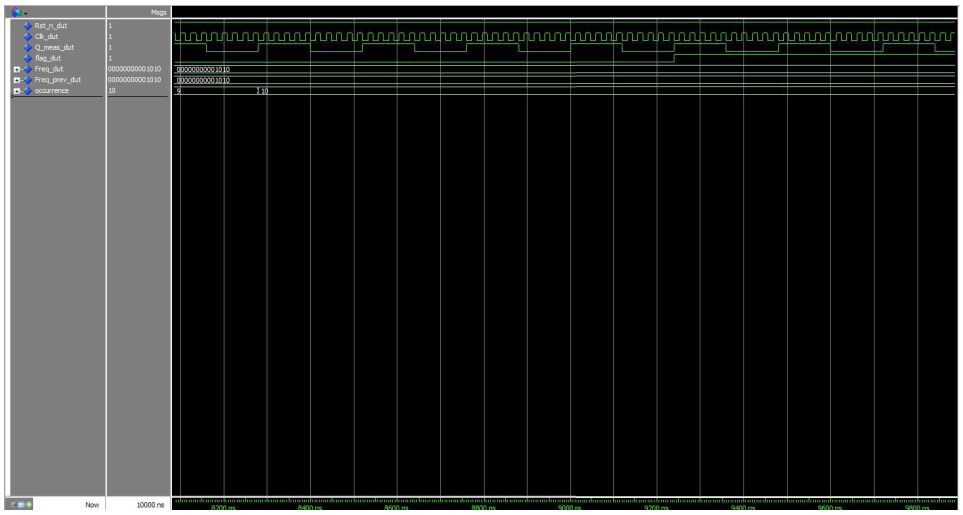


Figure 3.42: ModelSim simulation of the frequency short detection component.

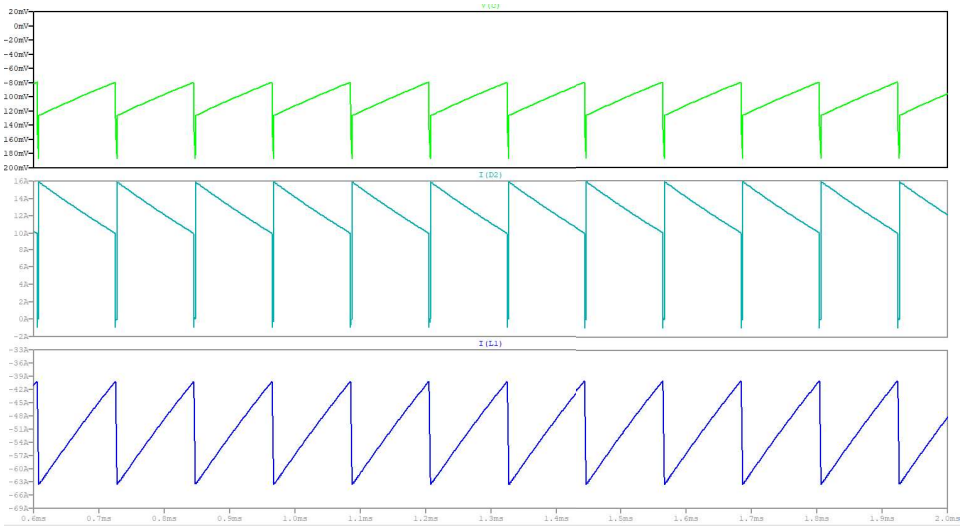


Figure 3.43: Waveform during a short circuit on the load.

The value is calculated as an average integral of the waveform in the selected time window, settling around 9.5 W. The related temperature rise is calculated with the transient thermal impedance, extracting and approximating the value at pulse duration of 2 ms from the graph reported above (3.17):

$$\Delta T_d short \simeq 0.6 \frac{^\circ\mathrm{C}}{\mathrm{W}} \times 9.5 \simeq 5.7\,^\circ\mathrm{C} \tag{3.32}$$

The detection time of the load short is related to the occurrences number needed to the FSM in order to detect the short: the initial number is set to 10, leading to a 2 ms short and the consequent 5.7 °C temperature rise on diode.
This value of $\Delta T_d$ is acceptable, but another variable must be taken into account. When

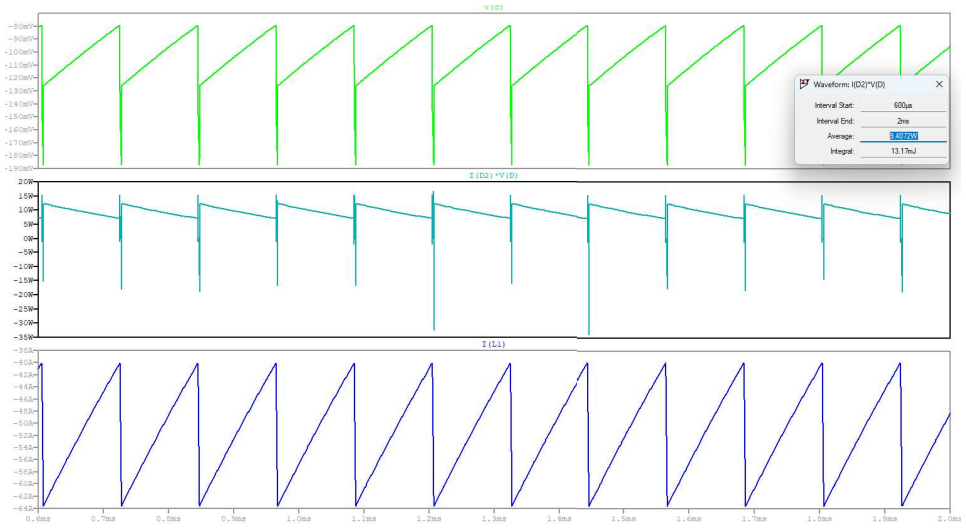


Figure 3.44: Single Diode power dissipation during a load short failure.

the short is detected, the FSM sets the gate driver input to "0", but the energy stored in the inductance does not go instantaneously to zero since it needs to be dissipated in the resistive components and parasitics. The energy stored is:

$$E_L = \frac{1}{2} L \; I_{avg}^2 = \frac{1}{2} \; 4.7\,\mu\text{H} \; (50\,\text{A})^2 = 5.875\,\text{mJ} \tag{3.33}$$

This energy will be dissipated by the resistive elements present in circuit, through the current that continues to flow in the loop. The resistive elements are: the shunt, the DCR of the same inductance and all other possible parasitics and, finally, the load short that has a finite impedance. Therefore, the total estimated resistance is estimated to be around $3 \div 4\,\text{m}\Omega$. Since the diodes are the most stressed component in this loop, the residual energy must be dissipated without reaching the critical junction temperature. A simulation of the energy dissipation transient could be done considering the exponential current decrease in the loop as a classical L/R model. In order to be conservative, the lowest resistance value is selected, corresponding to the maximum diode stresses.

$$\tau = \frac{L}{R} = \frac{4.7\,\mu\text{H}}{3\,\text{m}\Omega} \simeq 1.6\,\text{ms} \tag{3.34}$$

$$I_L(t) = I_{in} \; e^{-\frac{t}{\tau}} = 50\,\text{A} \; e^{-\frac{t}{1.6\,\text{ms}}} \tag{3.35}$$

An electro-thermal model is extracted from the $Z_{th}$ graph of the diode datasheet (in figure 3.17) and simulated through LTSpice, in order to have a better understanding of the phenomenon.

The current generator on the left represents the power as a product of the exponential decreasing current 3.35 and a constant forward voltage drop, extracted from the documentation as a worst case scenario. The voltage generator on the right corresponds to the ambience temperature. The thermal model of the diode is represented by the four parallel couple of resistances and capacitances on the left, as depicted in figure 3.45. On

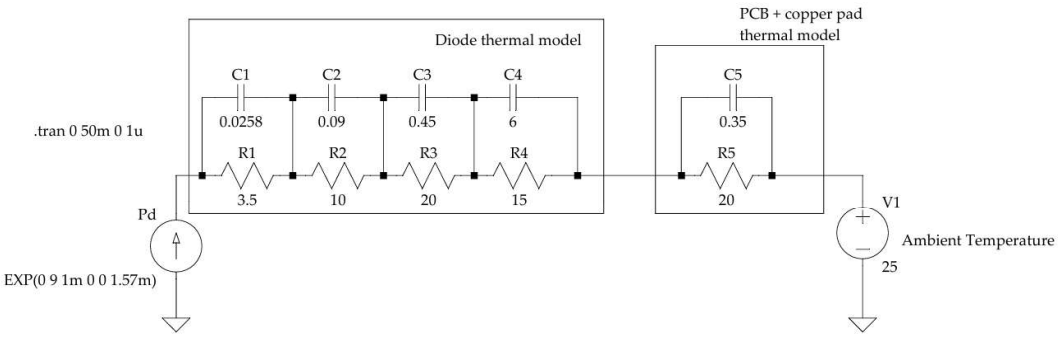



Figure 3.45: Thermo-electrical model of the V30K170 and PCB.

the right, a model of the PCB prototype has been extracted based on the characteristic (4 layers, 1oz. inner copper layers, $\sim 1$ cm$^2$ copper thermal pad).
The temperature behaviour is visualized as the voltage drop on the equivalent current generator, i.e. the red curve V(T) in figure 3.46. As it is possible to appreciate from the figure, the temperature rise is negligible and remains negligible also if summed up with the previous temperature rise during the short detection. The experimental validation of the protection against load short circuit has been tested and reported in the chapter 4.

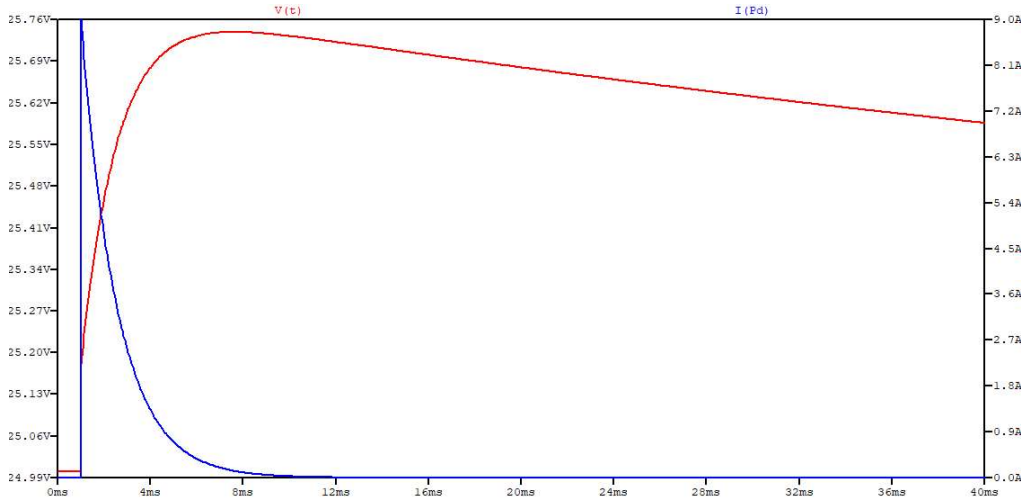



Figure 3.46: Thermo-electric simulation waveforms.

The controller logic plays a crucial role in ensuring the correct regulation of the system, including the described thermal behaviour and short-circuit protection. To this end, the FSM was implemented to efficiently manage the controller's operation. The state machine is described in the flow chart:

Four states are foreseen: IDLE is the start-up state. In this case the system waits for the start command to be asserted by a push button and the output signal to the

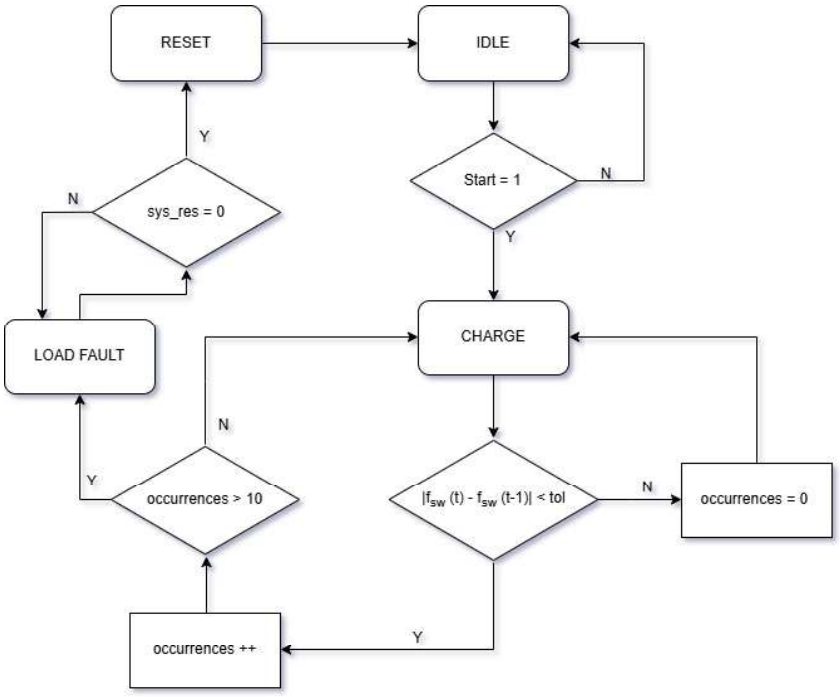



Figure 3.47: Flow chart FSM first controller.

gate driver is held low. In a real case scenario no start command will be needed, but it has been added in order to conduct the simulation and testing. The CHARGE state represents the correct functioning of the system, here the output of the combinational logic is now effectively connected to the gate driver input. If a short is detected, with the constant frequency method described, the state evolves into LOAD SHORT. Now, the driver input is again forced to zero and, since no auto-retry method is implemented, the system will remain in this state until an external reset is asserted. Two LEDs will be used to indicate the state or, alternatively, a serial communication protocol could be implemented as a future project to allow the hot-swap controller to communicate with other components on the board.

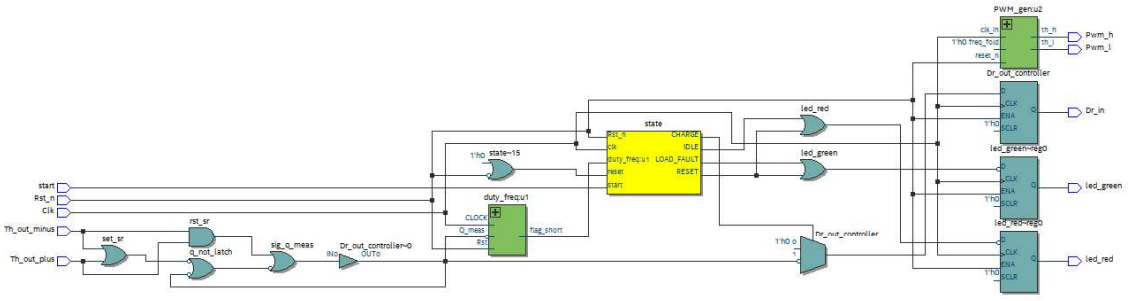


Figure 3.48: RTL view of the full system.

### 3.4.2 ADC solution with full digital control

An alternative controller implementation has been studied. The Altera MAX10 offers different Intellectual Property (IP) cores that can be instated and included as components in a VHDL described system.

The chosen model, the 10M08SAE, includes an Analog to Digital Converter hard IP core, with a SAR architecture, capable of 1 Mega Sample Per Second (MSPS) sampling rate with a 12-bit resolution.

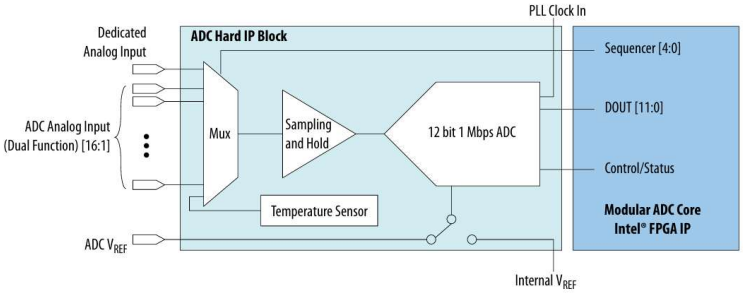



Figure 3.49: Altera MAX10 ADC Hard IP block and Modular IP, [28].

The ADC component can be instantiated in the Qsys Platform Designer software that will generate the relate VHDL file. The Modular IP core allows to choose between different functions and instantiations of the ADC block. A state machine is used to manage the control and status signals from the Hard IP, as well as the channel sequencing, sample storage and other related functions.

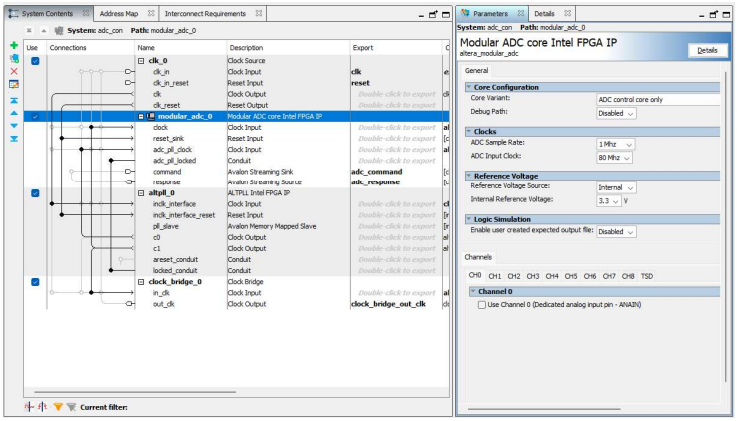
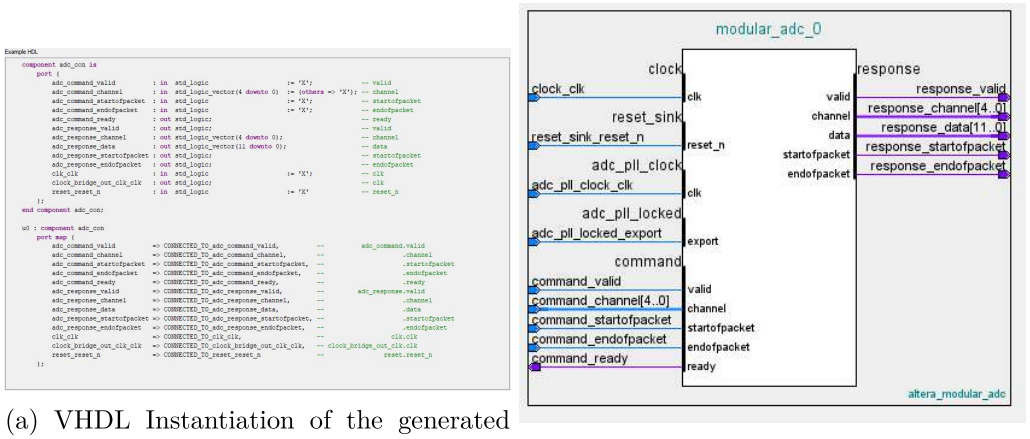



Figure 3.50: Platform Designer view of the IP cores.

Since in our design we do not need these secondary functions, the block is instantiated as simply as possible with the Hard IP and the basic control core only. The designed controller uses one channel and it is set in free-running mode. The value of the sample is read at every response valid asserted by the ADC control, i.e. at the end of every conversion.




(a) VHDL Instantiation of the generated ADC and related controller.

(b) Block scheme view of the ADC IP core.

Figure 3.51: ADC instantiation details, Qsys Platform Designer.

The ADC clock source is hard routed to the PLL (Phase Locked Loop) and cannot be sourced by an external clock. For this reason, in the generated system a PLL IP core and a clock bridge are included. The PLL has been set to work at 80 MHz, indicated by the manufacturer as the maximum operational frequency, ensuring the 1MSPs rate.

The input of the ADC is the amplified shunt voltage drop at the AD8410 output, now opportunely filtered to remove high frequency component noise and to satisfy the input impedance requirement of the ADC channel (from device documentation [29]). The basic idea of the hysteresis controller with the FSM and the related short circuit protection are the same of the first system previously described. A sampled version of the sensed voltage is now compared to the thresholds in a completely digital manner, avoiding both the previously employed LT1016, and the related PWM thresholds generation. In the second version of the controller implementation, the logic of the hysteresis control remains unaltered, but now the ADC allows to track the value of the load current at every moment, allowing the implementation of a new circuital protection, the fast breaker: if the current arises unexpectedly over the upper threshold by a certain percentage, or even worse if it saturates the ADC input, the FSM will take action by disconnecting immediately the logic and forcing the gate driver input to "0". The protection against short circuit remains the same, as well as the state logic implementation and the frequency measurement system.

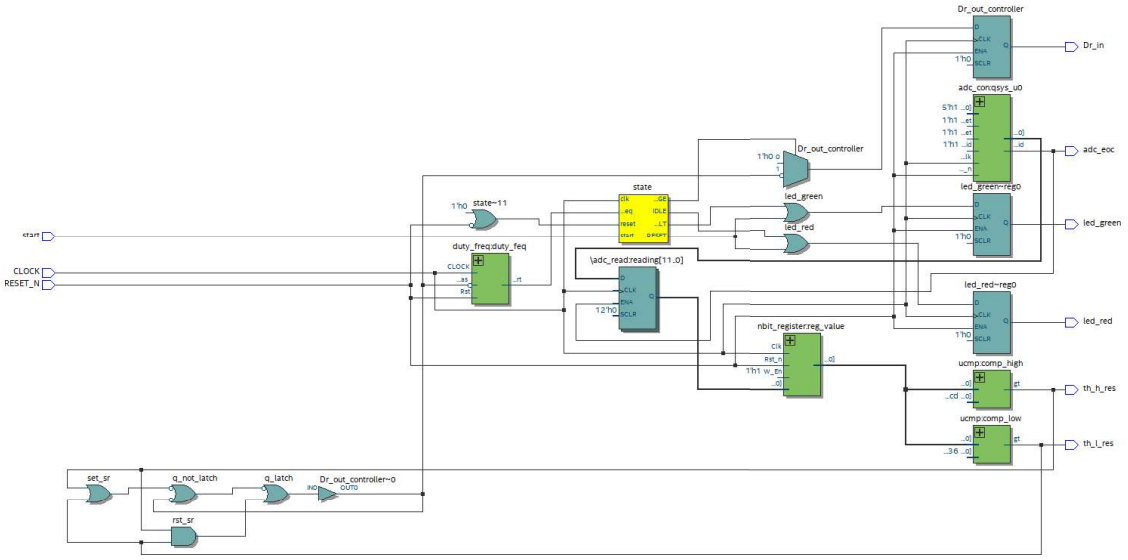



Figure 3.52: Full RTL view of the ADC system.

In figure 3.52 it is possible to distinguish between the different logic parts of the system: on the bottom left there is the described hysteresis controller logic; the yellow block represents the FSM control with the related status input and control output; moreover, registers in the system are used to store the sample value and other useful variables; the green block on the left *duty_freq* is the same frequency measurement block described in 3.41. In this Register Transfer Level view more outputs have been exported in order to facilitate the debugging operation and to show the waveforms evolution during the operation of the system. In the real controller, the only output signal really needed to the controller operation is *Dr_in*, the gate driving signal. At the input side, the analog input of the ADC is not reported by the Quartus Prime software in the RTL viewer.

## 3.5 PCB Design

A prototype on a Printed Circuit Board (PCB) has been developed in order to test the functionality of the designed system. KiCad 8.0 has been used to draw the schematic, edit components symbol and footprints and finally for the PCB routing. A 3D view of the final board design is reported in 3.53

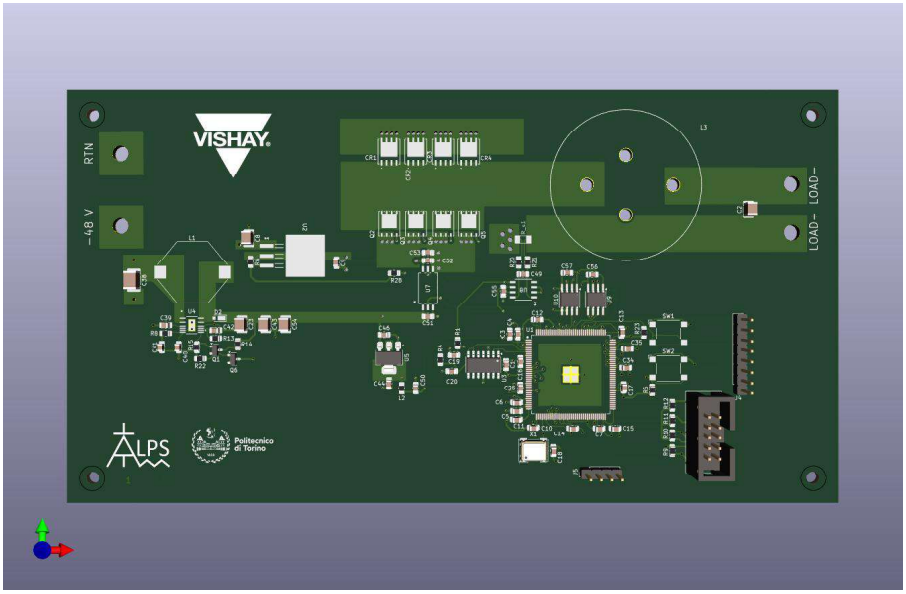



Figure 3.53: 3D-view of the designed Printed Circuit Board.

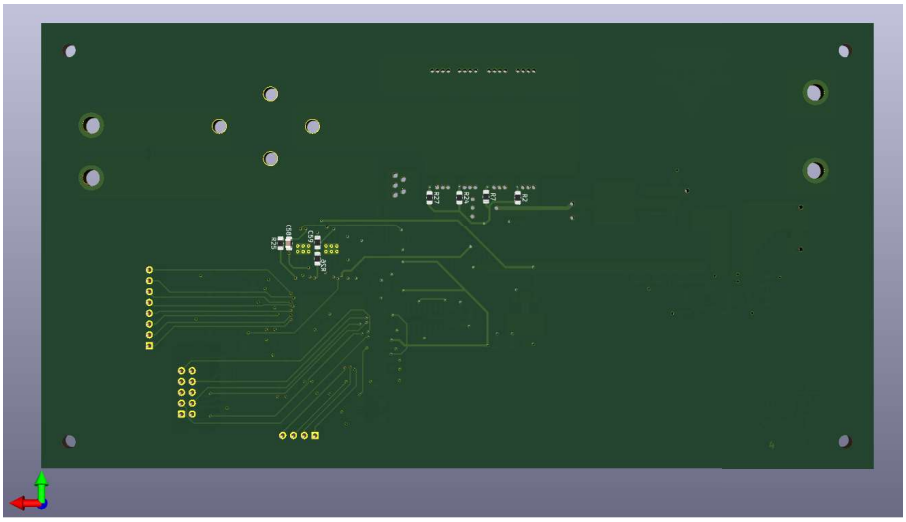


Figure 3.54: 3D-view, bottom layer.

A hierarchy has been established by dividing the different sections of the circuit, as showed in the next schematics reported.

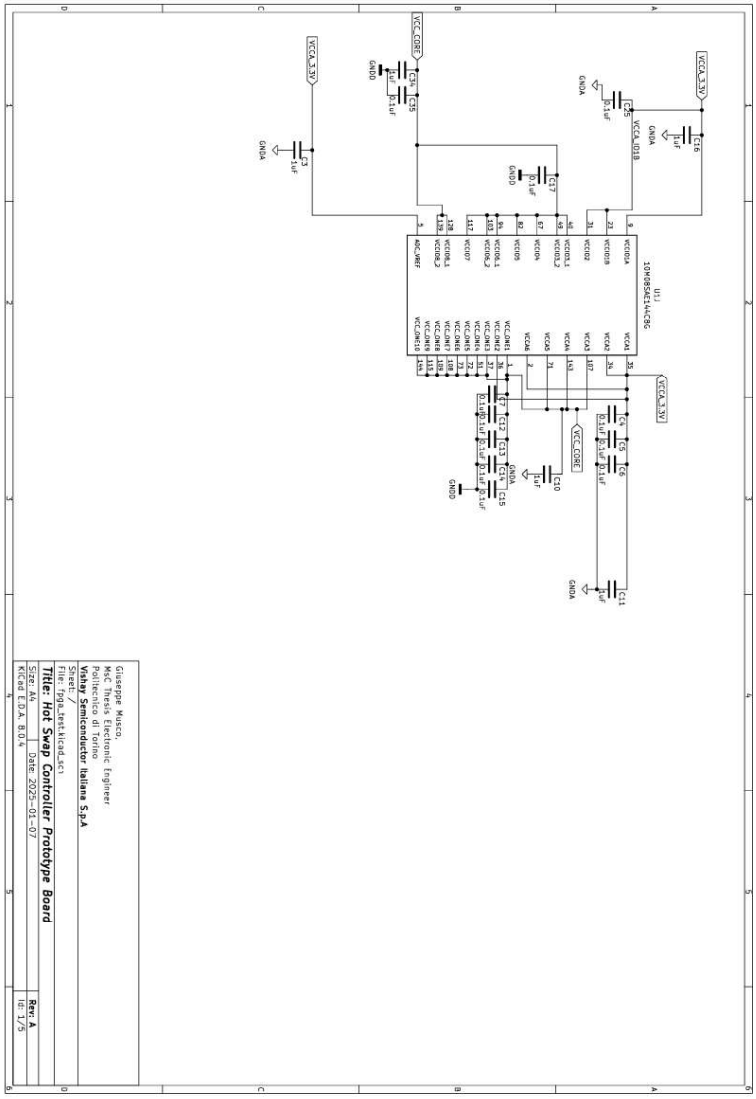



Figure 3.55: FPGA power supply input section, KiCad schematic.

As it is possible to observe from the schematic in figure 3.55, the power supply provided to the FPGA is divided into *VCC_A3.3* and *VCC_CORE*. The first one provides power to the analog blocks of the device, while the latter to the digital part. Although both are derived from the same linear regulator TLV1117 (see 3.29), the only difference is that the analog is filtered from the possible digital noise of *VCC_CORE*. This allows, in some critical routing path, to exchange the two without affecting the functioning but tolerating some noise.

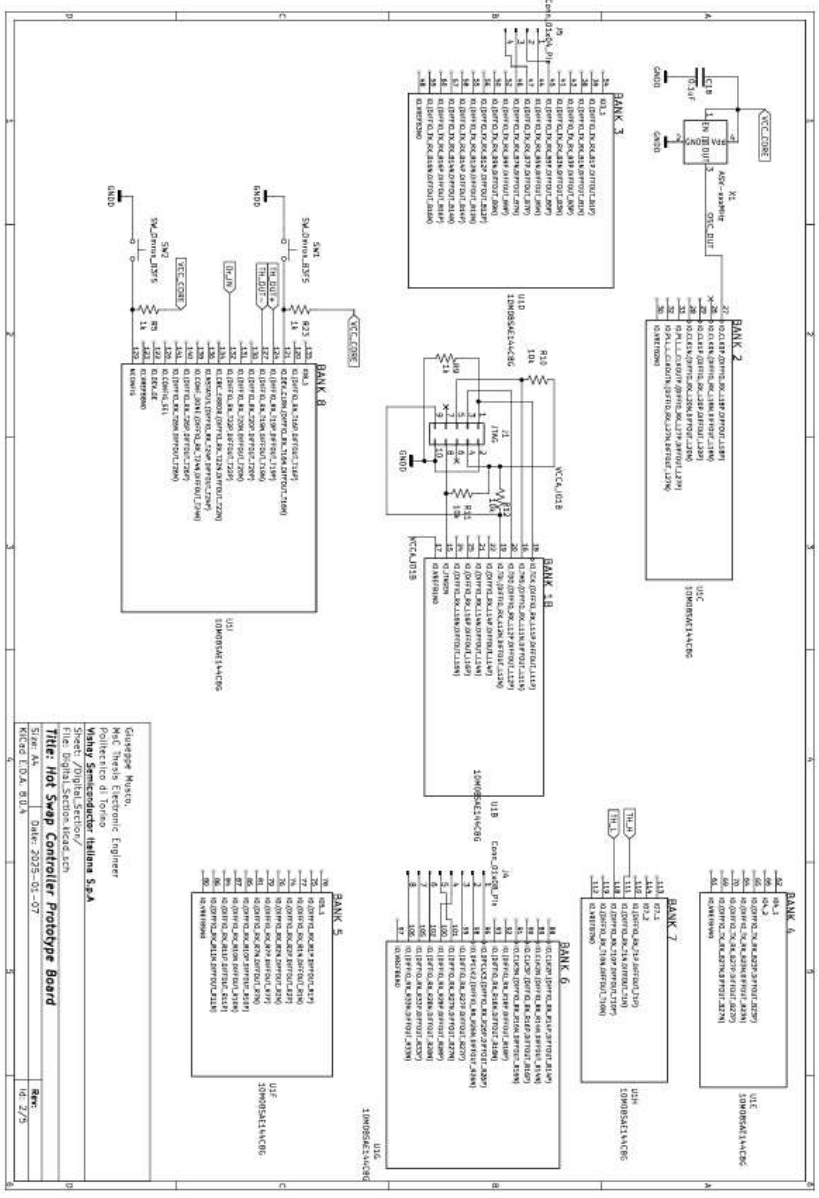



Figure 3.56: FPGA Digital section schematic.

The digital section schematic in figure 3.56 shows the different I/O Banks of the FPGA. The Bank 1B includes the dedicated pins to the JTAG connector which allows to configure the FPGA. A 50 MHz oscillator is connected to one of the FPGA Clock inputs (pin 27). Two push-buttons SW1 and SW2 are included on the board. Moreover, SW2 is connected to a dedicated input pin NCONFIG that, when pulled low, erases all configuration data, enters a reset state and tristates all I/O pins. The push-button SW1 can be configured as a soft reset, if the DEV_CLRn option is enabled, or it can be used as a user button. All the connections and routings requirements have been extracted from

documentation, [29] [30]. The different labels represent the pins used as I/O interface. Dr_IN is the FSM control output, connected to the gate driver input, TH_OUT+ and TH_OUT- are connected to the analog comparator output, while TH_H and TH_L are the PWM generated thresholds, fed to the comparators input. A couple of pin headers have been connected to general purpose I/O in order to facilitate the debugging operations.

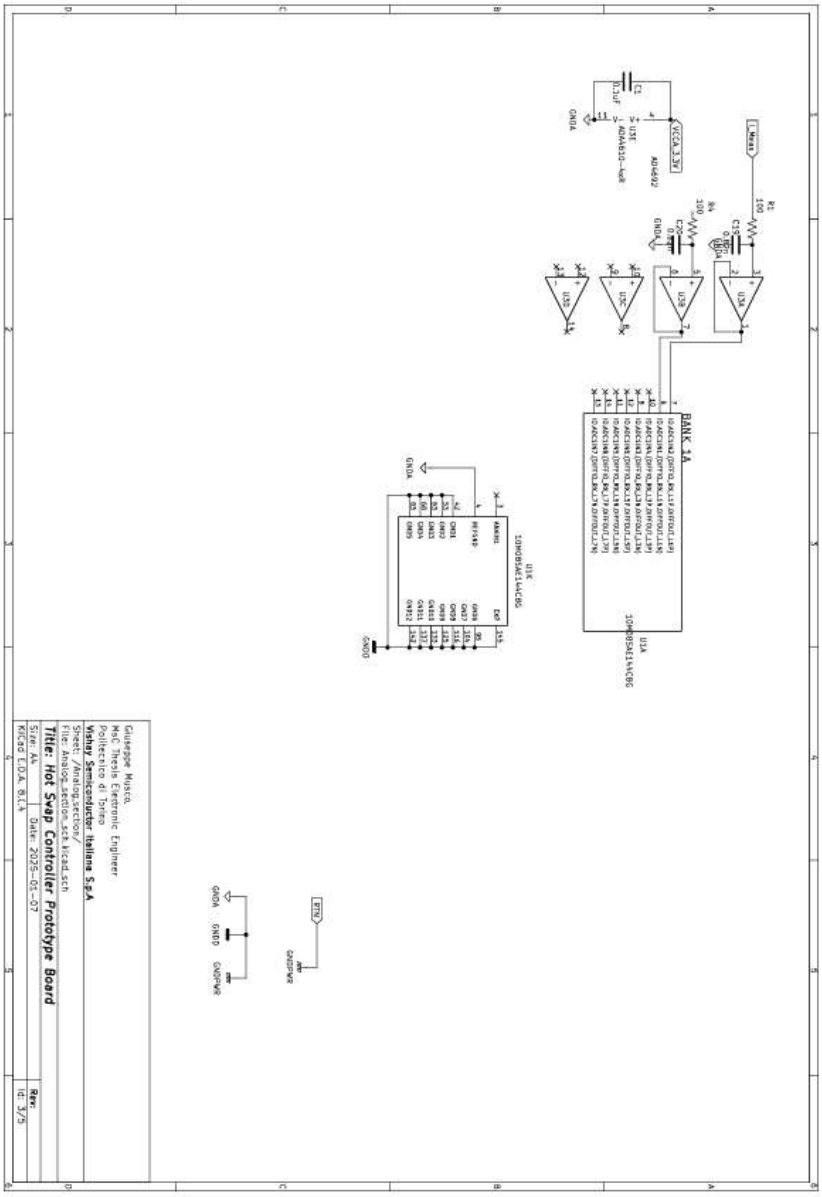



Figure 3.57: FPGA Analog Section schematic.

In the Analog section of the schematic, reported in figure 3.57, it is possible to notice

four operational amplifiers; these are used as voltage followers to separate the impedance of the filters from the ADC input channels, as recommended in the MAX10 documentation [28]. The Op-Amp IC is the AD8630 (on the schematic another code is reported, same footprint): it offers a 2.5 MHz Gain Bandwidth product, rail-to-rail output and optimal offset and derive performances. The input filter has been designed in order to not cut any harmonic content of the current sense waveform, some preliminary tests showed that this phenomenon happens for a cut frequency around 2 MHz.

$$f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi 100\,\Omega\ 820\,\mathrm{pF}} \simeq 1.95\,\mathrm{MHz} \tag{3.36}$$

We can also appreciate the connection between the different ground references: although they are different, they share the same potential reference. GNDA is the analog ground, reference for the ADC block of the FPGA and all the interface ICs (LT1016, AD8410, etc). The GNDD instead is the digital ground, reference for all the fast-changing signal of the FPGA; it is important that the commutation noise generated by the digital signal do not affect the analog signal. The return RTN and GNDPWR represent the same high reference for the hot swap circuit, that is where the load current flows. Since all these different current loops may affect each other, it is important to separate the ground plane into different areas with no interfering and tie them together only under the ADC and current sense amplifier, at the GNDA. See 3.67 for an in-depth analysis.

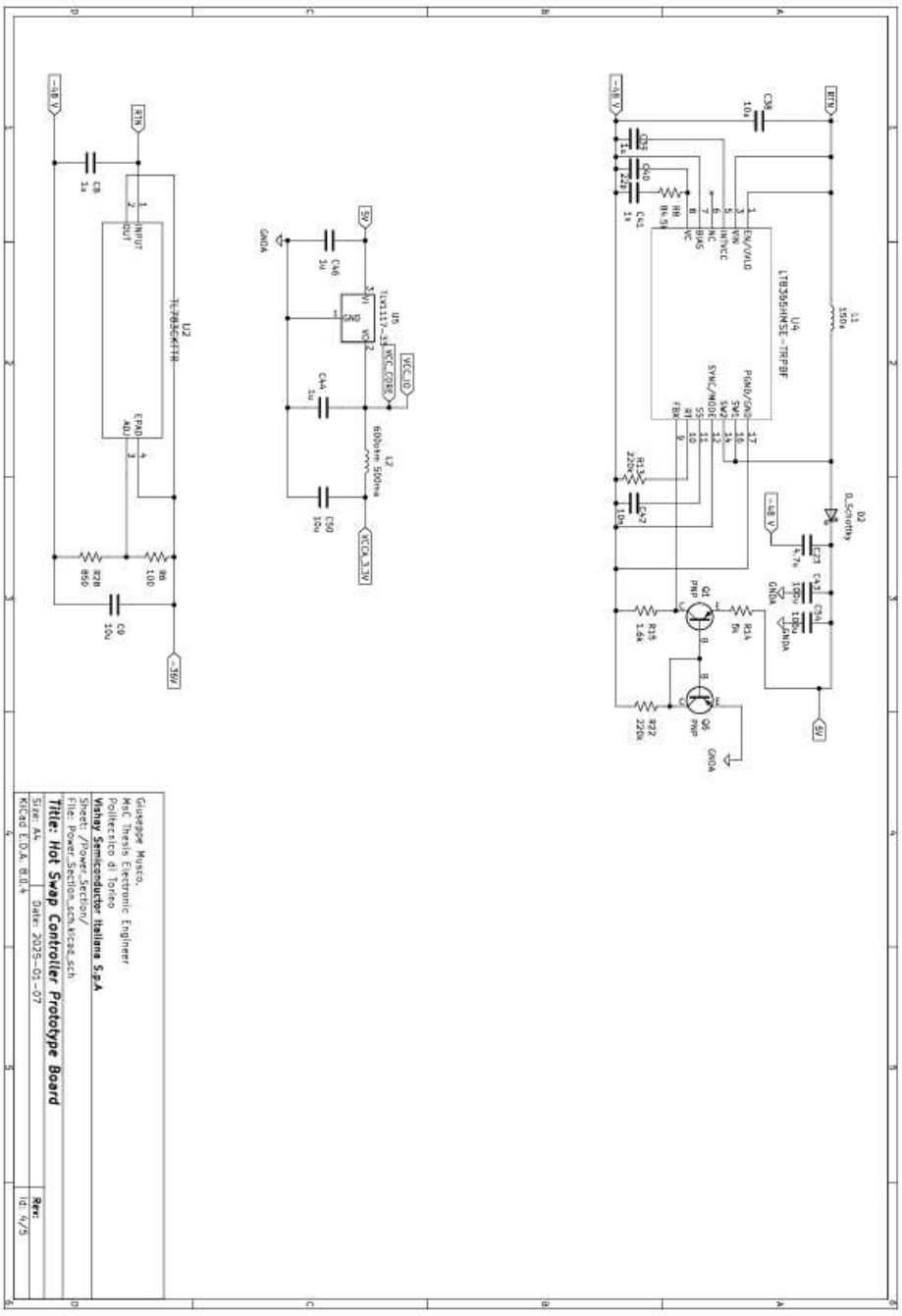



Figure 3.58: Power supplies section.

The power section reported in figure 3.58 has been already discussed and simulated in 3.3.2. The major difference noticeable now is represented by the different references.

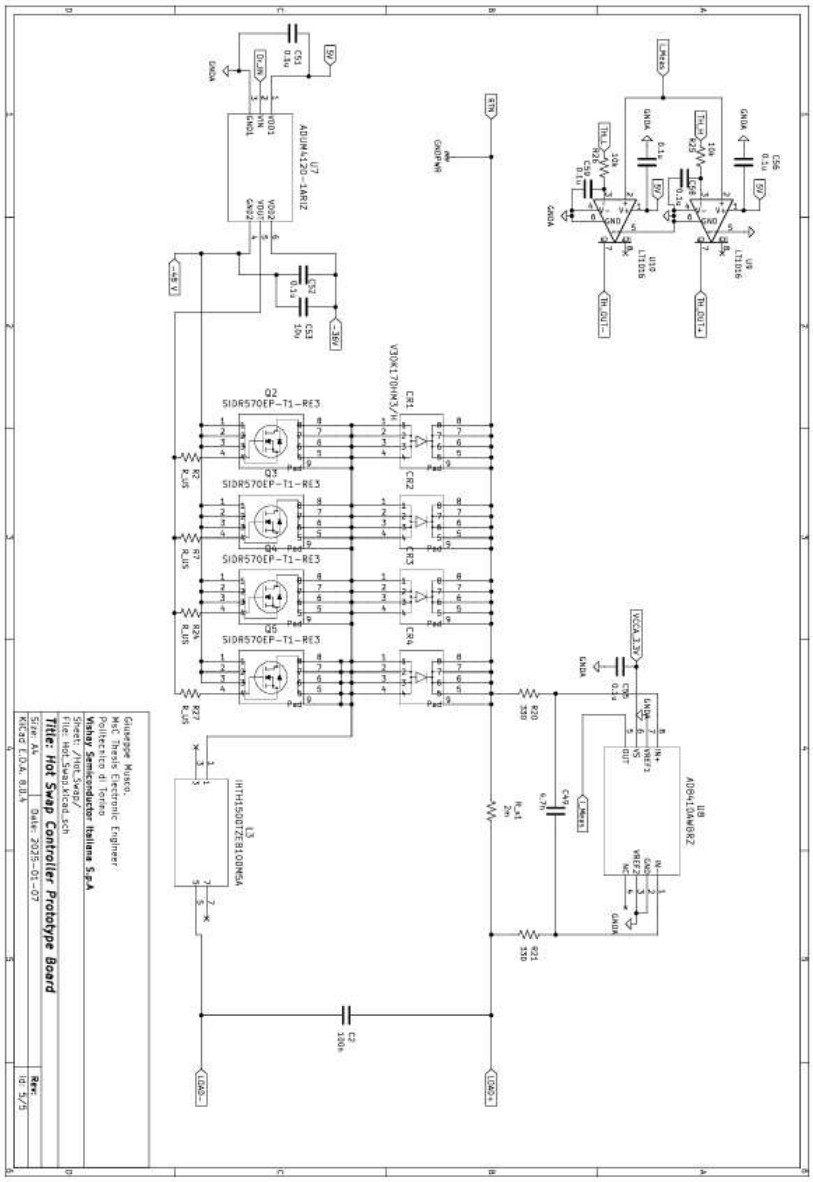



Figure 3.59: Hot Swap Circuit schematic.

On the Hot Swap schematic in figure 3.59 we can notice all the interface ICs: the two analog comparators, LT1016, with the related PWM input filter and bypass capacitor; the gate driver IC ADuM4120 with input and output capacitor; the current sense amplifier AD8410 with related filter and bypass capacitor.

Some modifications were made to the footprints before proceeding with the routing and the design of the board. Some of the footprints were not present in the KiCad library, therefore they have been added by downloading from the manufacturer website or by drawing them on the KiCad footprint editor.

A top view of the layers is report in figure 3.60.

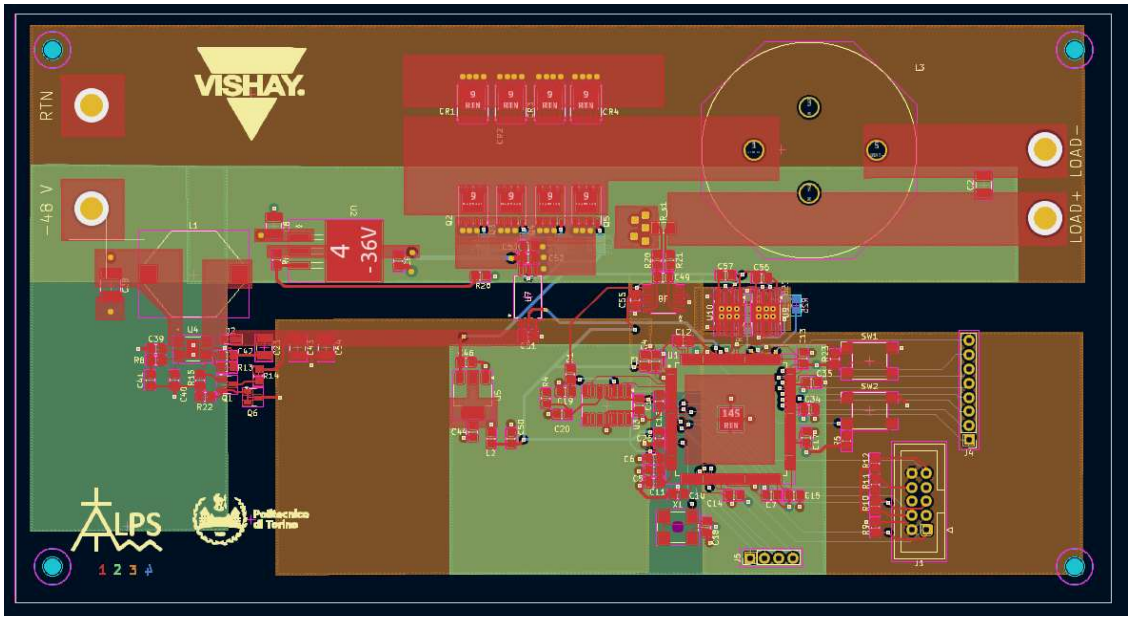



Figure 3.60: PCB layers top view.

The board is constituted of four layers, with the top and bottom being the signals layers, while the inner ones are respectively the VCC and the ground plane. In order to facilitate the debugging and testing operation, the board has been designed with a straightforward layout, maintaining all the signals accessible and divided in different compartments; this division will also facilitate the soldering operation that are conducted by hand. For the same reasonings, the board dimension has been enlarged, 100 mm x 200 mm, providing extra space for eventual adjustments.
Starting from the top layer, on the left we can observe the two input terminal mounting zones, and just below the first compartment. Here the LT8365 is placed to derive the positive voltage supply, as it can be appreciated in figure 3.61. The layout design takes inspiration from the datasheet's suggestion. Nevertheless some of the suggestions cannot be respected, as the fact that the copper area connected to the switch terminal of the LT8365 must be minimized to reduce EMI emission. The datasheet recommends to use more layers and connect the inductance L1 to the SW terminal through vias. Anyway, the design choice of using the inner layers as VCC and GND layer does not allow this implementation. Nevertheless, it is important to note that this is a prototype rather than a market-ready product. For now, this limitation is not a concern, as it does not impact the converter's functionality. The output of the converter is referred to a different plane,

for this reason the output capacitor and the feedback are shifted to the right.

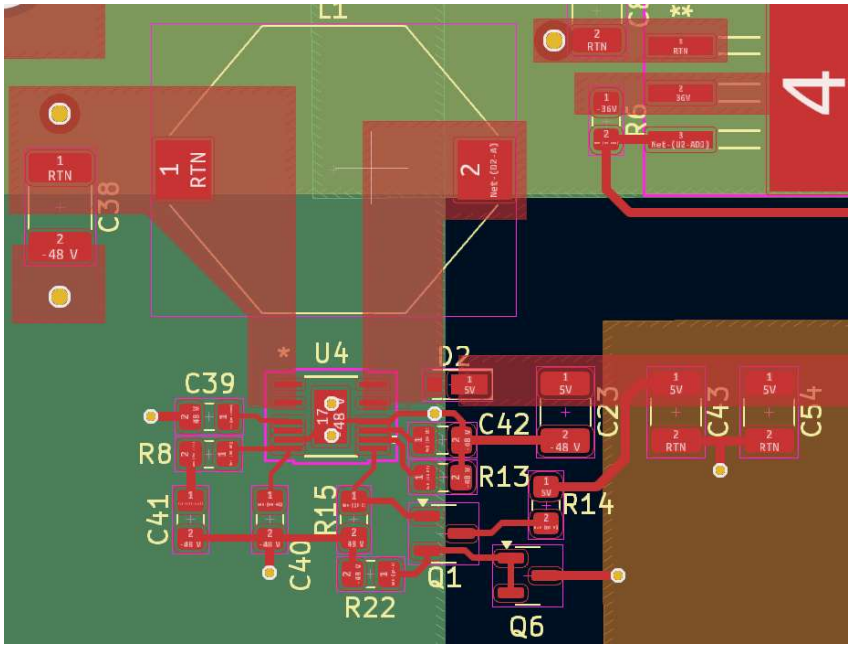



Figure 3.61: PCB Layout of the Boost Converter, LT8365.

On the right, just above the Boost converter, another power supply is derived: the TL783 derives 12 V referred to the −48 V layer below. Once again, the layout suggestions from the datasheet are taken into account. The feedback resistor divider is placed in such a way that the ohmic losses on the copper traces are compensated, with R28 placed as closes as possible to the load (ADuM4120 driver). The input and output capacitor are placed as close as possible to the respectively input and output pins, as depicted in figure 3.62.

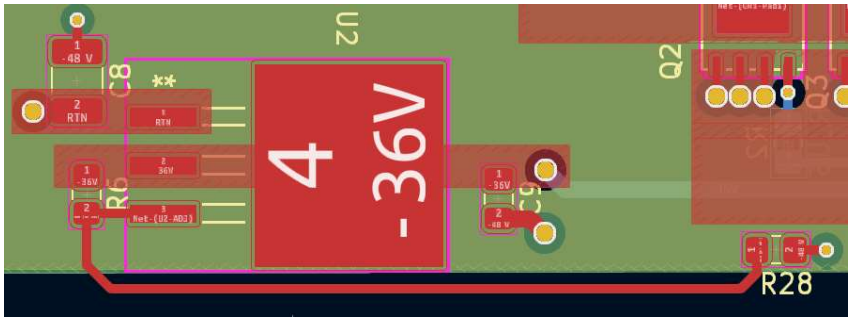



Figure 3.62: PCB layout of the TL783.

The Hot Swap circuitry is placed on the upper right; here, multiple of copper pads have been added to handle the high current and permit as much heat dissipation as possible. The current arrives from the left of the shunt, R_s1 in figure 3.63, where large vias are connected to the inner RTN plane. While, the current exits from the right

of the shunt, where a large copper pad provides conduction to the LOAD+ terminal. The current then returns to the board and successively passes through the inductance IHTH1500MZ, L3 in figure 3.63. The power inductor is a through hole mounting, and it has two extra pins that provide mechanical support, referred as 3 and 7 in figure 3.59, that must not be connected. After the inductor, another large copper pad connects the inductor to the switching node, where the current is then recirculated by the diodes to the RTN node, or to the -48 V plane if the MOSFETs are on, as described in the Analysis and Design, Chapter 3.

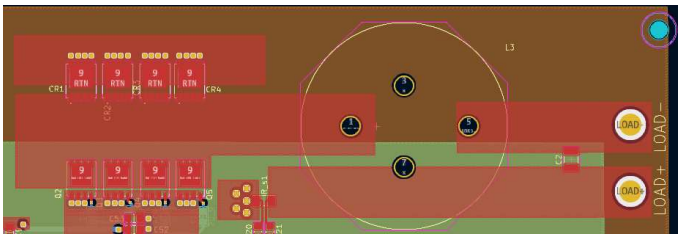



Figure 3.63: Hot Swap circuit PCB layout section.

With this layer design, the current could not return under the shunt resistor, since this would provoke the reduction of its parasitic inductance; for this reason, during the testing and validation operation, the shunt inductance will be finely measured with an impedance meter, in order to place the cutting frequency of the differential filter as close as possible to the shunt zero.
The Driver (U7 in figure 3.64) is placed as close as possible to the switching MOSFETs to minimize the loop area and reduce EMI. The related bypass capacitor and gate resistance have very low parasitic inductances. All the driver traces are kept as short and wide as possible to reduce inductance.

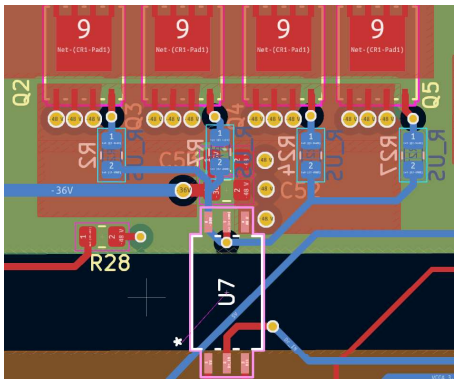



Figure 3.64: Gate Driver section PCB layout.

The sense amplifier (U8 in figure 3.65) represents the interface between the high current hot swap circuit and the input of the digital controller. The sense voltage is routed from the inner pad of the shunt to the differential input of the AD8410 as a differential pair, in order to reduce noise. The differential filter (R20, R21, C49) is placed as close as possible to the sense amplifier, to limit any parasitic inductance of the traces; for the same reasoning the passive components are chosen with the lowest access parasitics.

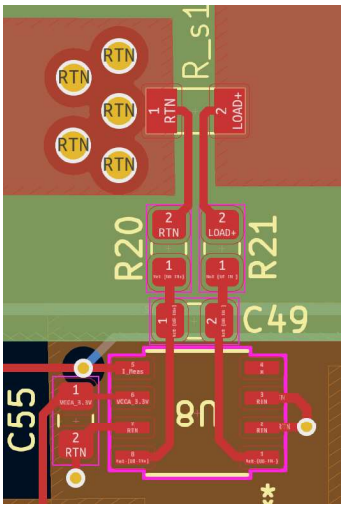



Figure 3.65: Current sensing section layout.

The last section on the board is the Digital one; it is composed by: the FPGA with its related circuitry (JTAG, oscillator, buttons, etc), the fast comparators and the ADC input filter. As it was previously done, the connections and bypass requirements have been extracted from the related documentation and respected during the routing operations. Since in this section we have fast changing signals, great part of the routing has been done on the bottom layer, in order not to affect with noise the near analog and sensing sections.

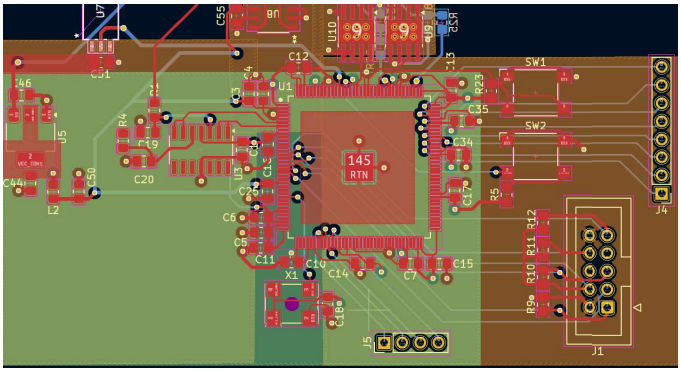



Figure 3.66: Digital section layout.

From this last observation, we can understand how the routing and layer design have been driven by the different type of signals and power levels involved. Looking at the layers breakdown, the most important feature to notice is the segmentation of the ground plane on the third layer, as it is possible to observe in figure 3.67.

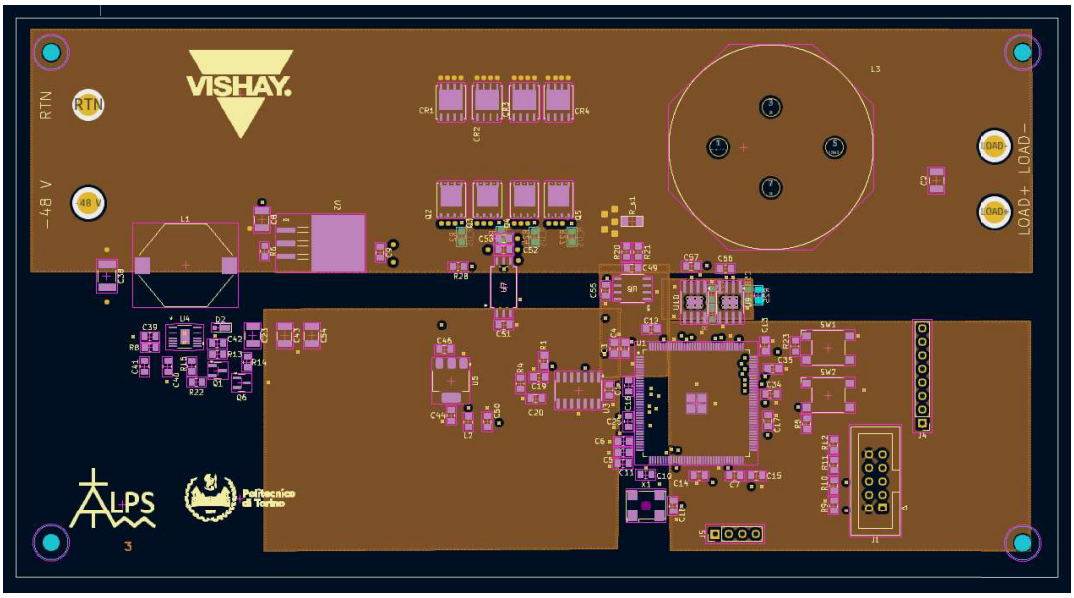



Figure 3.67: Third Layer, GND plane.

Every current returns to its source via a ground path. Currents naturally follow the path of least impedance, which means that if multiple types of signals share the same ground plane, their return paths might overlap and create interference, in what is known as "ground loops". By isolating the ground planes, we ensure that the noise from the digital section does not couple into the analog section. This isolation is particularly important for the ADC or for the sense amplifier where signal integrity is crucial. Furthermore, isolating from the power ground allows to obtain a cleaner reference, since high current may cause "ground bounce", i.e. voltage difference between the references. Although separate ground planes are used for isolation, all sections of the circuit must ultimately share a common reference voltage. A single-point or star grounding approach is employed to merge the different ground planes at one well-chosen location. A single connection point helps ensure that no significant potential difference develops between the different grounds. This avoids problems like ground loops, which can be a significant source of interference and signal distortion. The key is to select the connection point carefully, often where the analog and digital sections meet. This minimizes the possibility that noise from one domain will be injected into the other. The star ground technique is especially useful in mixed-signal environments where both analog and digital circuits operate in close proximity.

# Chapter 4

# Functional Test

As the mounting and soldering of the prototype has been completed, the testing operation began. Similar to what was done with the circuit partition during the routing operation, the circuit is now tested by compartments during validation.

The power supplies are the first sections that have been examinated. Starting from the switching converter, which provides the +5 V rail, the first test conducted is a start-up behaviour analysis. The objective is to verify the rise of the output voltage and check if there are any dangerous overshoots. This operation is performed emulating a real scenario, in which the board is inserted into a live supply, and so the overshoot phenomenon is accentuated. With a single mode acquisition of the oscilloscope connected at the output node, we obtain the following waveform shown in figure 4.1.

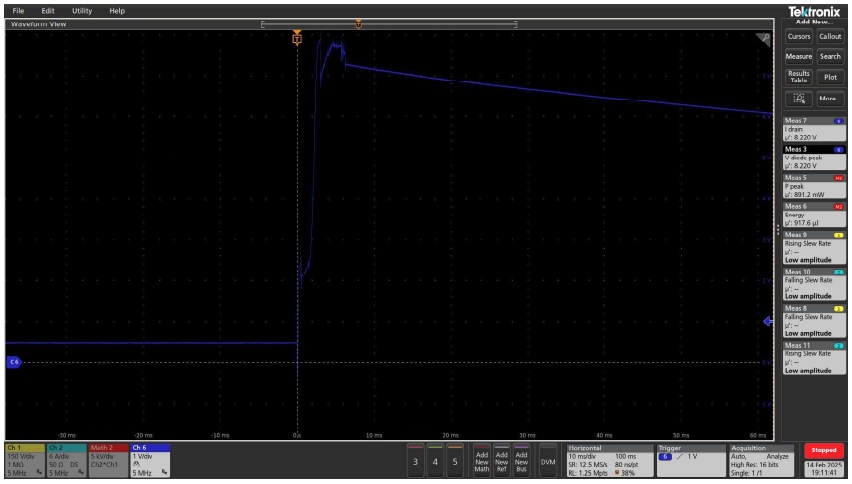



Figure 4.1: First start-up waveform, LT8365 output voltage, oscilloscope capture.

As it is possible to observe, the peak value of 8.2 V is very high in percentage with respect to the nominal 5 V and may cause several problems to the ICs powered by this rail. This test shows the worst case, since no TVS diode or similar protection have been placed in first place, neither at the output or at the input of the conversion stage; the

TVS diodes in some case are planned to be at the power supply side. For this reason, the circuit has been modified as follows in order to prevent high overshoot peak to reach the gate driver and the comparators.

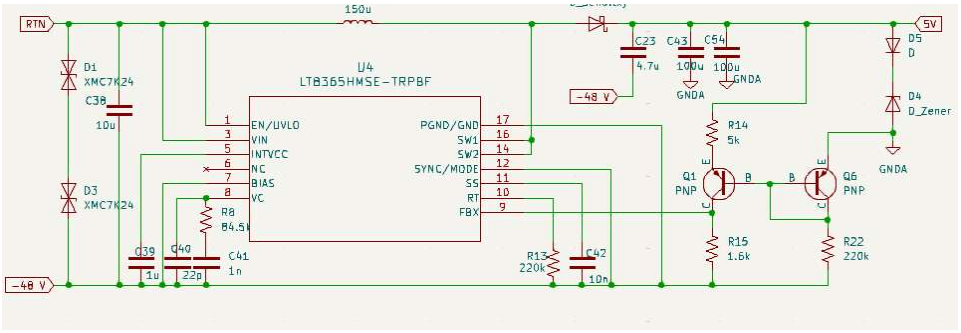
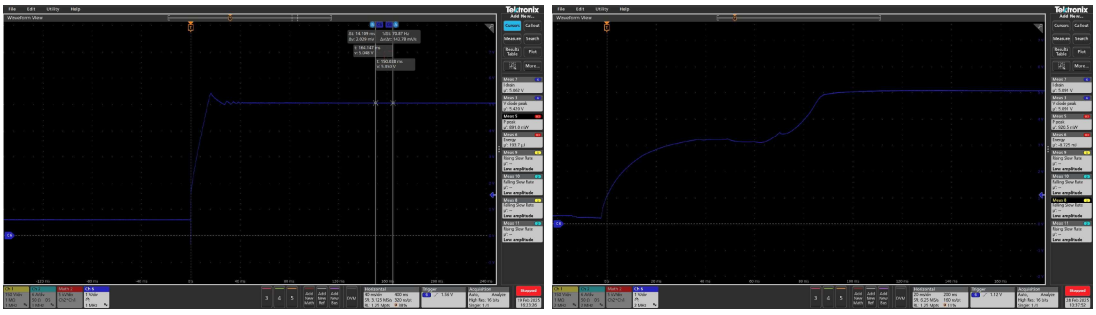



Figure 4.2: Boost converter Schematic modification after start-up test.

In order to mitigate the overall output overshoot, it is possible to act on different points. At the input side, the connection of the board could cause sparks and initial voltage spikes, for this reason two Vishay Xclamp TVS diodes XMC7K24 [31] have been added, providing bidirectional protection against spikes at the backplane. Another protection added is the series of a standard and a zener diode (D5 and D4 in 4.2); in case of overshoot these will clamp the voltage level around $5.6 \sim 5.7$ V, protecting the ICs powered by this rail. The last parameter that we can modify to reduce the overshoot is the soft start SS capacitor (C42 in figure 4.2). Inserting a larger capacitance at this point will slow down the rise of the output voltage of the converter stage. The next figures report the improvements achieved with these additions.



(a) Output voltage start-up with input and output protections.

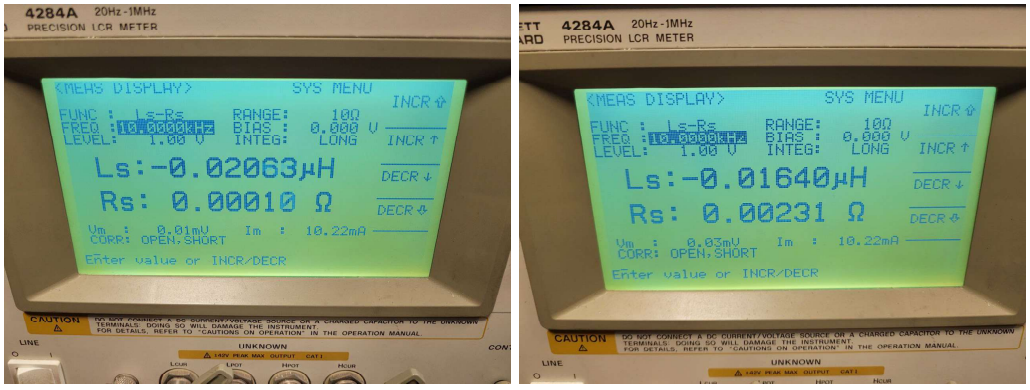
(b) Output voltage with protections and larger soft-start capacitor.

Figure 4.3: Start-up waveforms, output voltage of boost converter.

As it is possible to observe from the figure 4.3, now the output voltage rise is smoother, presenting a reduced overshoot peak. The rise time can be further controlled with large SS Capacitor, in figure 4.3b a 1 µF value can be appreciated.
The last adjustment performed regards the resistor R22, changed into a 47 kΩ, in order to ensure a better temperature compensation: Q5 now carries the same current ($\sim 1$ mA)

of Q1, ensuring the same rate of change of $V_{e,b}$ with temperature.
The other power supplies derived with linear regulators does not present the same overshoot issue of the boost switching converter. Therefore they have been easily tested with a digital multimeter, verifying the correctness of the design.

The current sense section tests start from the shunt measurement. Through an impedance meter the parasitic inductance of the shunt is obtained, in order to find the exact position of the zero that must be compensated by the differential input filter (see section 3.11). The measurement setup must be as repeatable as possible in order to obtain a valid measure. In order to connect a small 1206 SMD resistor to the instrument, two wires have been soldered to it. The effective measure is then obtained by means of difference: first we need a measurement of the impact of the wires; then, the instrument is compensated on the short to cancel off the wires effects; lastly, the shunt is soldered to the wires and the effective measure is extracted by applying the difference:




(a) Wires short connection measurement. (b) Shunt resistor measurement.

Figure 4.4: Shunt impedance measurement.

As depicted in figure 4.4 ,the obtained shunt impedance measurement is:

$$R_s = 2.2\,\mathrm{m\Omega}$$
$$L_s = 4.2\,\mathrm{nH}$$

From the obtained values, the corresponding differential filter is placed around :

$$f_c = \frac{1}{2\ \pi\ \frac{L}{R}} = 83.4\,\mathrm{kHz} \tag{4.1}$$

The last section to validate is the digital one, starting from the comparator. As it was previously done, a triangular wave form is provided at the input, then it is amplified by the the AD8410A and reaches the non-inverting of the LT1016 comparator. A fixed voltage threshold of 1.8 V is fed to the inverting input. Two probes of the oscilloscope are used to track respectively input and output behaviours. From figure 4.5 we can observe the input triangular wave, the yellow curve, on a 1V/div scale and the output green curve, that rises up when the 1.8 V threshold is crossed.

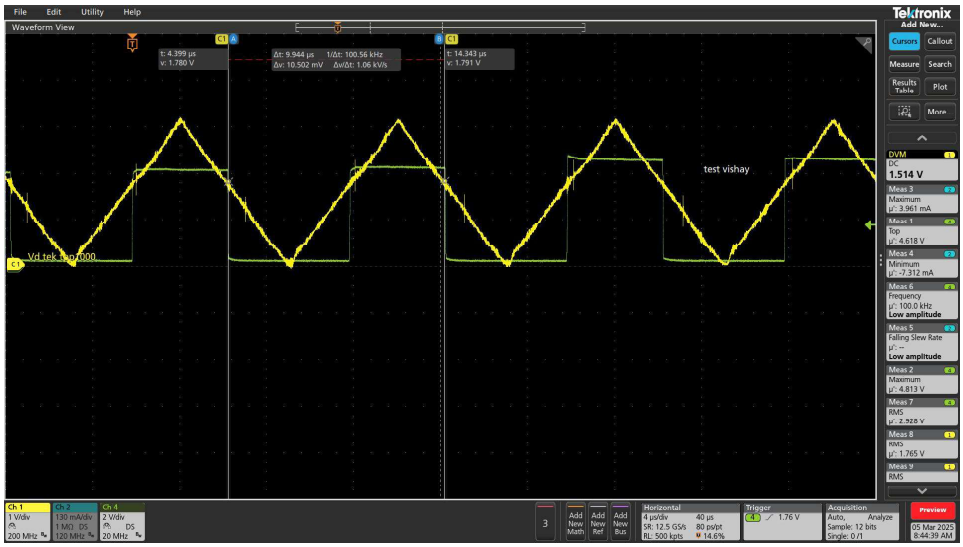



Figure 4.5: Analog comparator output, triangular wave and fixed thresholds as inputs.

After the interface front-end, the controller logic is implemented on the FPGA. In order to test the functionality of the FSM controller, the firmware is compiled in Quartus Prime and the correct pins are assigned; then the FPGA is programmed. A push button has been included to assert the start of the charging transient. The first test is the correctness of the state transition, when the START or the RESET button is pressed. Then, a standard triangular wave is provided at the input of the sense amplifier and the output of the FSM, i.e. DR_IN is acquired with the oscilloscope. The procedure is similar for both the two versions of the firmware, ADC and external comparator.

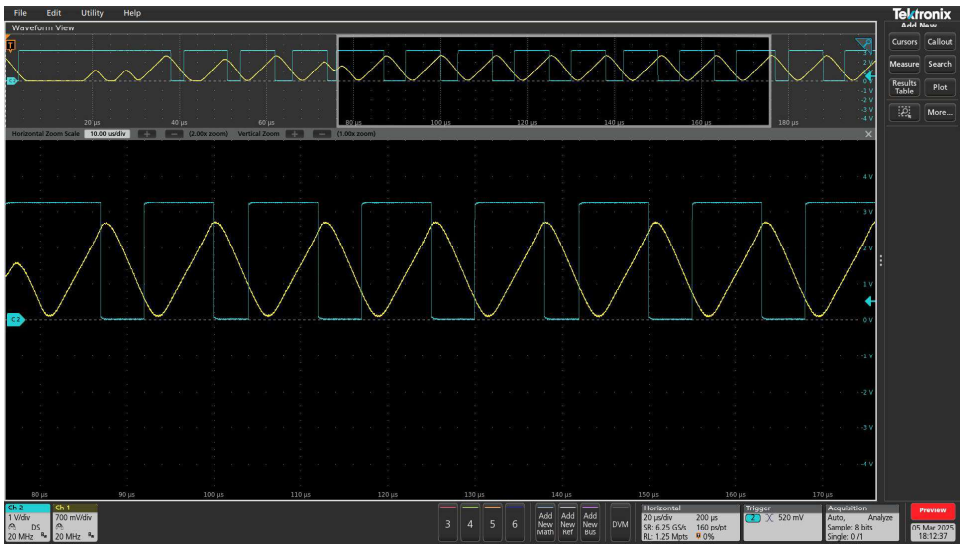



Figure 4.6: Logic waveforms behaviour in the CHARGE state.

With regard to the oscilloscope acquisition in figure 4.6, it is possible to observe the behaviour of the logic output, with the two thresholds posed at $Th_h = 1.8\,\mathrm{V}$ and $Th_l = 1.0\,\mathrm{V}$. It can be noted that the logic described in 3.1 is respected: the light blue curve represents the Gate Driver input and, as predicted, it is equal to "1" when both the thresholds are crossed below and to "0" when the thresholds are crossed above. In figure 4.6 the firmware version with the ADC is shown. The input waveform is distorted because the initial tests have been conducted with a lower cut frequency of the input filter of the ADC channel. The CHARGE state test is conducted through a frequency sweep at the input waveform, in order to not trigger the LOAD FAULT condition.

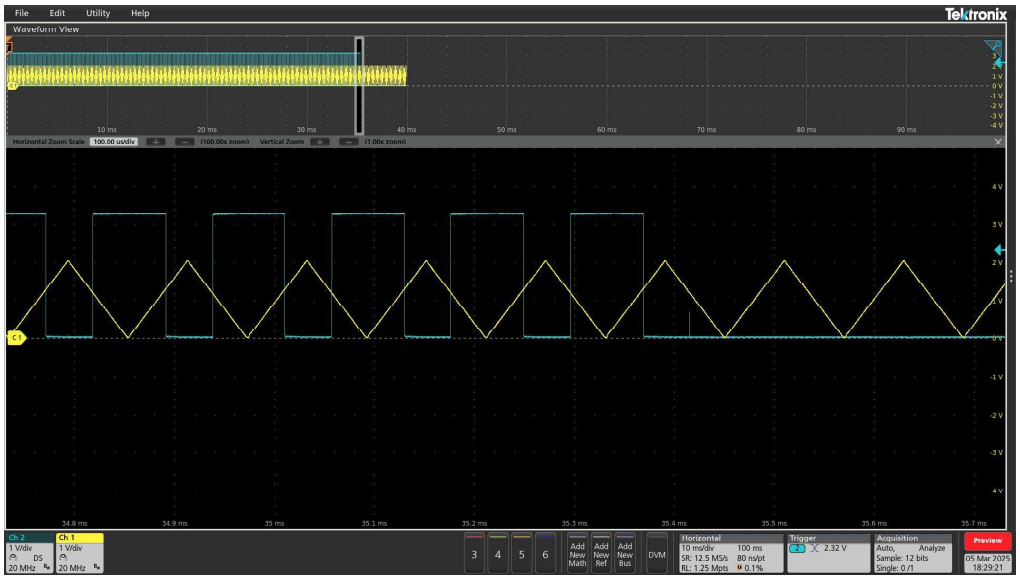



Figure 4.7: Logic Waveforms, transition from CHARGE to LOAD FAULT state.

With regards to the LOAD FAULT condition, it is shown in figure 4.7. In this case, the input waveform has a constant frequency and, as a result, after some cycles the occurrences of same frequency measured builds up, triggering the latch-off of the controller. It will remain in this safe state, with the gate driver forced to "0" until a reset command and a new start command are asserted. In order to visualize the evolution of the state machine, two led are used.

The last functionality checked before the complete charge test is the driving section. A triangular waveform is once again fed as an input to simulate the load current waveform and the effectively gate driving capability of the ADuM4120 is measured. In order to visualize both waveforms on the oscilloscope, at least one differential probe is required: since the oscilloscope and the waveform generator share the same ground from the line, it is not possible to connect two probes at different references; given that the objective of this test is a $V_{gs}$ measure and since the source is referred to the - 48 V rail, differential or, more in general, isolated probing is mandatory. The obtained waveform is shown in figure 4.8.

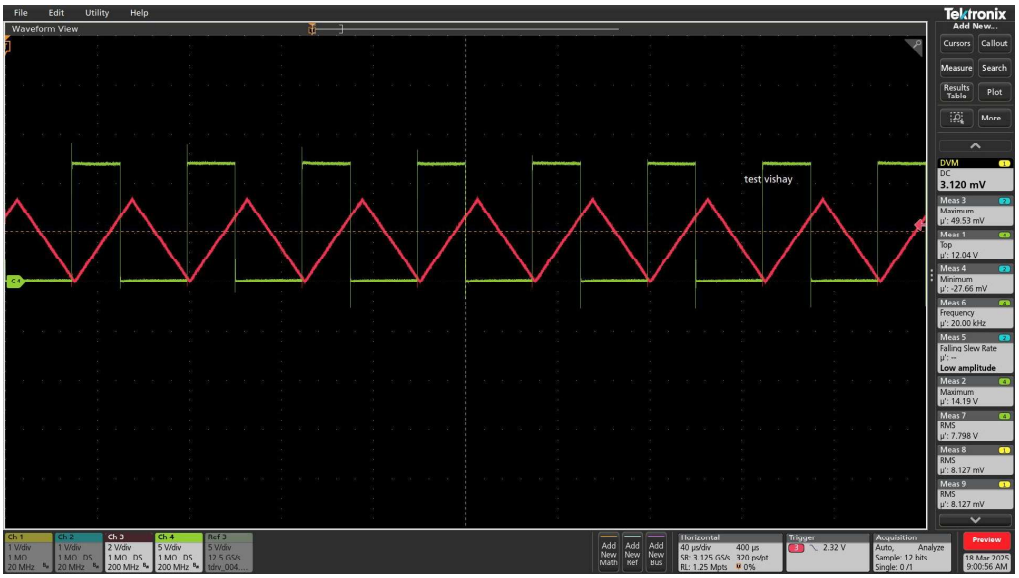



Figure 4.8: Gate Driver response.

Since we can route all intermediate signals from the FPGA as output pins, it may be useful to extract the ADC end of conversion, *adc_response_valid* in figure 3.51a. This allows us to measure the propagation delay of the combinational logic, which is useful for estimating the amplitude error in the current measurement. Since the current slew rate $\frac{\delta I}{\delta t}$ is imposed by L1, we can easily calculate and compensate the amplitude error. This is achieved by tightening the Hysteresis Delta, reducing the higher threshold while increasing the lower one of the amount determined by the following equation.

$$I_{Ea} = t_{pd,logic} \ * \ \frac{\delta I}{\delta t} \tag{4.2}$$

In figure 4.9, a measure of the propagation delay of the controller logic $t_{pd,logic}$ is reported, showing a delay of $\simeq 55\,\text{ns}$.

The corresponding amplitude error will be equal to:

$$I_{Ea} = 55\,\text{ns} * \frac{10\,\text{A}}{\mu\text{s}} = 550\,\text{mA} \tag{4.3}$$

This result is negligible with respect to the 60 A and 40 A: a compensation is therefore not necessary. This calculation regards only the logic and does not take into account the conversion time of the ADC. Its architecture is based on a Successive Approximation Register (SAR): at least 12 clock cycles are required for the actual conversion while a few additional ones are required by the control core soft IP. Therefore, assuming a total of 16 clock cycles for conversion, the total delay between the sampling and the controller action is of $\sim 375\,\text{ns}$. Hence, in the second version of the Hot Swap controller, a threshold compensation could be necessary.

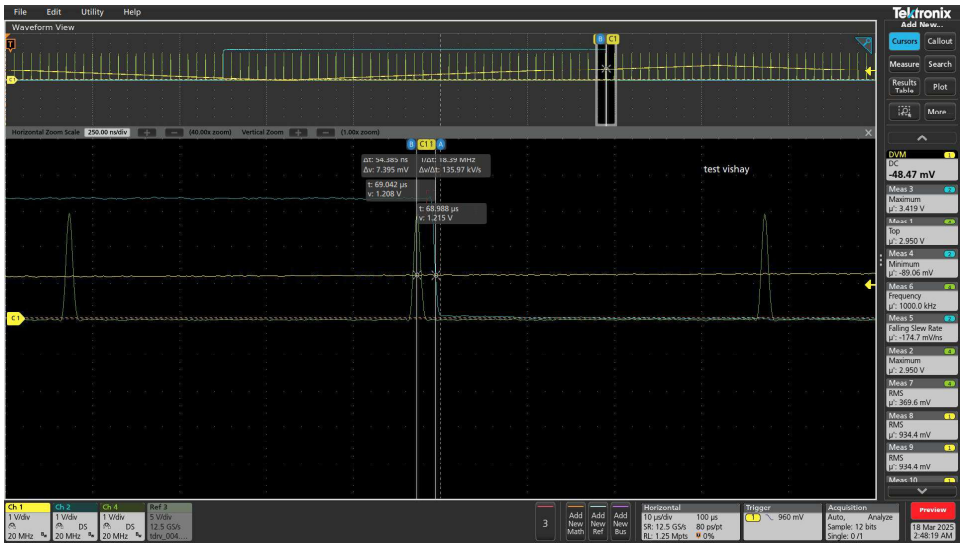



Figure 4.9: Measure of the controller logic propagation delay.

Finally, a complete charge test has been performed. It has been conducted with a scaled version of the real load capacitance and load current, in order to ensure the proper functioning of the circuit, but avoiding the risks related to high current. The working voltage has been reduced to 16 V while the charging current average value has been scaled by a factor of 40, posing the thresholds at: $t_{h,h} = 1.5$ A and $t_{h,l} = 1$ A. The shunt resistor is increased accordingly, reaching the 80 mΩ value. In order to maintain a low switching frequency, a larger value of the inductor $L_1 = 150\,\mu\text{H}$ is employed, limiting the current slew rate and consequently the switching frequency, as shown in equation 3.2. The load capacitance of the first test is $C_L = 820\,\mu\text{F}$ and, in order to prevent dangerous discharge, a resistive load $R_L = 100\,\Omega$ is connected in parallel. With this load condition, the expected charging time is equal to:

$$t_c = \frac{C_L}{I_{C_L}} V_{in} = \frac{820\,\mu\text{F}}{\frac{(1.5+1.12)\,\text{A}}{2} - \frac{16\,\text{V}}{100\,\Omega}}\ 16\,\text{V} = 11.4\,\text{ms} \tag{4.4}$$

In figure 4.10 the waveforms during the simulated hot swap event are shown.

As demonstrated in the analysis, the limitation related to the ADC performance becomes evident through the inaccurate thresholds that vary accordingly to the changes in the switching frequency and in the duty cycle vary. This is due to the fact that the sampling rate of the ADC is relatively low (1 MSPS) and since the switching frequency changes, the sampling point vaires with it. Nevertheless, this implementation successfully charges the load capacitance. However, in a real scenario the analog comparator implementation would offer better performances, as it is possible to observe in figure 4.11.

Now the thresholds are well defined and they do not change during the transient. For this test the thresholds have been set at $t_{h,h} = 1.5\,\text{A}$ and $t_{h,l} = 1.12\,\text{A}$. The resulting maximum switching frequency is calculated as:

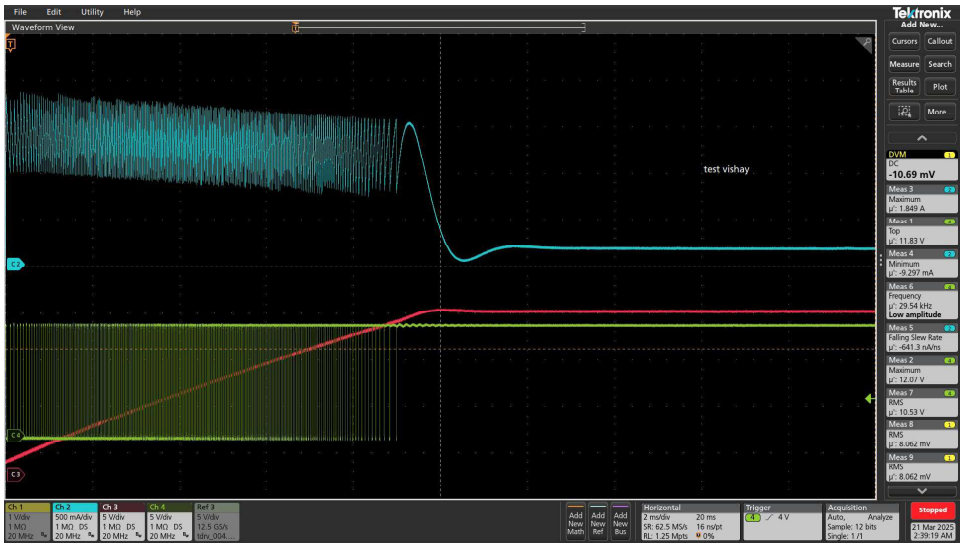



Figure 4.10: First charging test, Hot Swap event behaviour, ADC implementation.

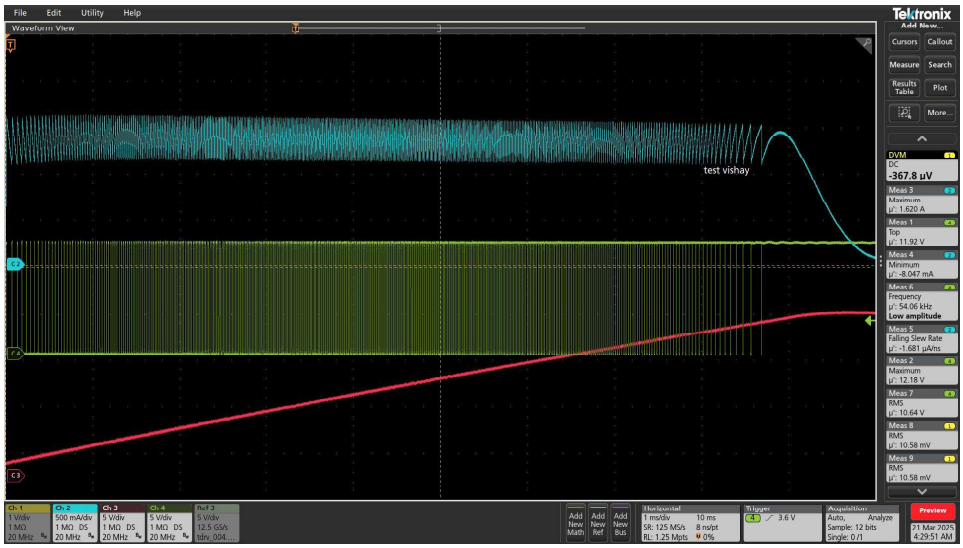



Figure 4.11: First charging test, Hot Swap event behaviour, analog comparator implementation.

$$f_{s,max} = \frac{V_{in}}{4\ L\ \Delta H} = \frac{16\,\mathrm{V}}{4\ 150\,\mu\mathrm{H}\ (1.5 - 1.12)\,\mathrm{A}} = 70.9\,\mathrm{kHz} \tag{4.5}$$

In the next figure, 4.12, it is possible to notice that the measured thresholds levels and the maximum switching frequency are coherent with the calculations.

(a) Hysteresis thresholds measurement. (b) Maximum $f_s$ measurement.

Figure 4.12: Hot swap analog comparator implementation, test measurements.

In order to observe the action of the controller in a fault condition, a short circuit has been connected at the load side.

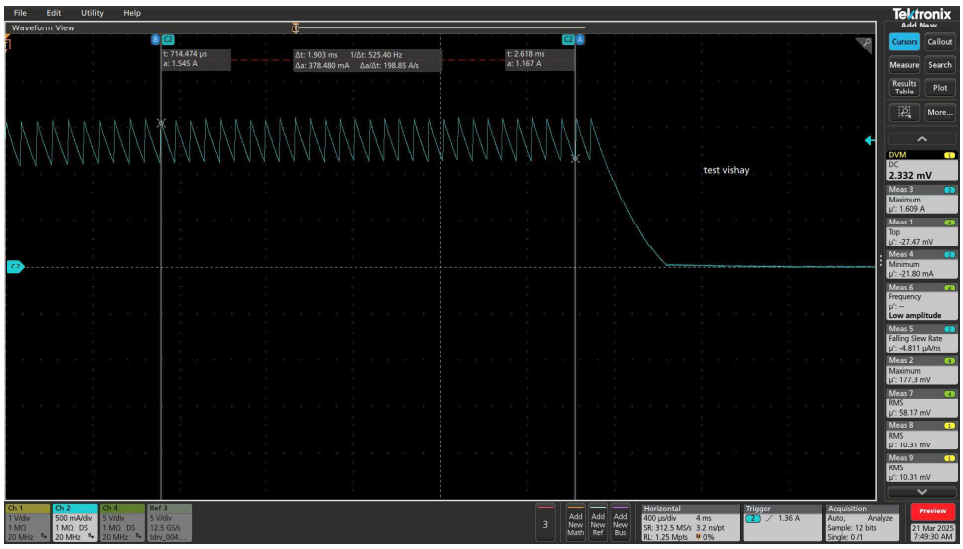



Figure 4.13: controller response to a short circuit load.

From figure 4.13 it is possible to observe that the short is detected in less than 6.5 ms, leading to a slightly larger power dissipation and to a consequent temperature rise on the diode with respect to the predicted calculations in 3.32. The total temperature rise is calculated by first extracting a transient thermal impedance of $R_{\theta ja} = 1.5\frac{^\circ\text{C}}{\text{W}}$ from the graph 3.17. Then, we employ the equivalent power dissipation on the diode during the short circuit duration of $\sim 30\,\text{W}$ from the LTSpice simulation at 3.44. The result gives the total temperature rise:

$$\Delta T_{d,short} \simeq 1.5\frac{^\circ\text{C}}{\text{W}} \times 29.45 \simeq 45\,^\circ\text{C} \tag{4.6}$$

This value is much larger with respect to the expectations. In any case, it will not lead to the diodes failure. Some adjustments could be done to the tolerance and occurrences

parameters (refer to 3.4.1 for reference) in order to find the right trade-off.
If the tolerance is too large, it could affect the normal operation of the controller during the CHARGE transient. If instead, the value of the tolerance is too low it could not be possible to the controller to detect the short leading to the Diode failure. A possible next step could be to find a more robust short detection technique, taking advantage of the duty cycle measurement, and possibly adding another feedback loop in order to be able to sense load voltage.

Another charging test have been performed with the same load, before stepping into the high current charging . This time the actual inductor $L_1 = 4.7\,\mu\text{H}$ has been used. The hysteresis current has been increased, with $t_{h,h} = 7.5\,\text{A}$ and $t_{h,l} = 2.5\,\text{A}$. The predicted switching frequency is around 170 kHz.

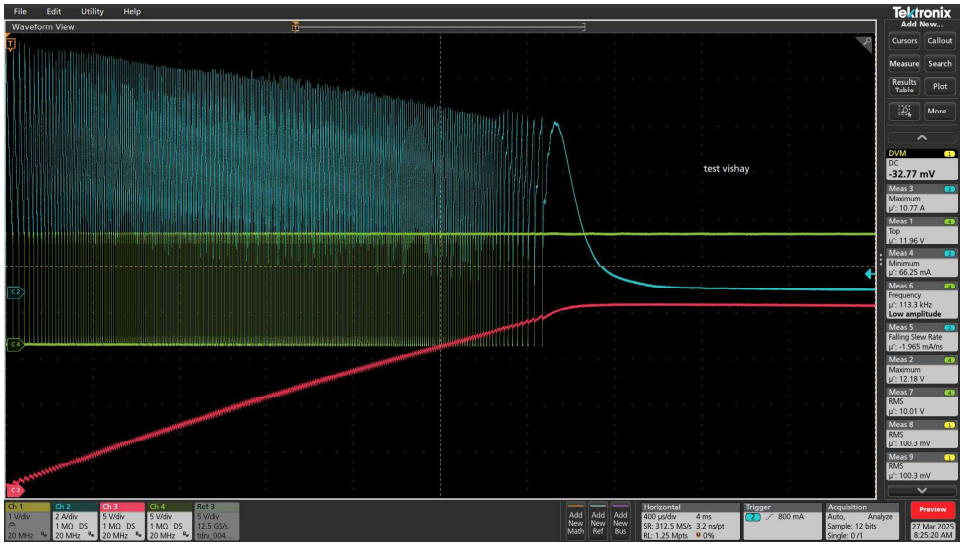



Figure 4.14: Second charging test, average charging current $I_{avg} = 5\,\text{A}$.

This time the performance of the system began to look less ideal. As the real inductor has been included in the system, the current slope is now much higher, showing that the total time delay of the loop constituted by the comparator, the logic and the gate driver is larger than the expected. From the datasheets of the component the LT1016 ensures a very low $t_{pd} < 10\,\text{ns}$, but the gate driver has a much higher propagation delay in the order of $70 \div 80\,\text{ns}$. In addition to that, there is also an asymmetry between turn-on and turn-off, making more difficult to predict the thresholds, duty cycle and frequency behaviour during the transient. The total error could be estimated as:

$$I_{Ea} = (t_{pd,logic} + t_{pd,comp} + t_{pd,drv}) \ * \ \frac{\delta I}{\delta t} = (\sim 200)\,\text{ns} * \ \frac{\delta I}{\delta t} \simeq 2\,\text{A} \tag{4.7}$$

Nevertheless, we have to remember that the circuit must contain the inrush current below the dangerous level, it is not a concern if there are a certain level of error on the thresholds and consequently on the switching frequency; in terms of this last one, we also remember that the switching happens only during the start up, and so for few

milliseconds. Furthermore, an error on the thresholds will reduce the switching frequency, as shown in the figures 4.15.

(a) Amplitude errors on the thresholds. (b) Maximum Switching frequency error.

Figure 4.15: Errors measurements.

The final charging test has been performed with the effective current and voltage levels. This last test executed on the prototype shown some issues related to the 5 V secondary supply derivation performed by the LT8365, (see figure3.24 for reference), the high current level involved and the non negligible inductance of the main supply wire created high over voltages, leading to the internal MOSFET failure of the regulator. Also the control FSM implementation must be reviewed, both for the short circuit protection and for the propagation delay. More work needs to be done before a real practical application use but, nevertheless, the design demonstrated good capabilities, motivating future studies.
The final board setup is shown below.

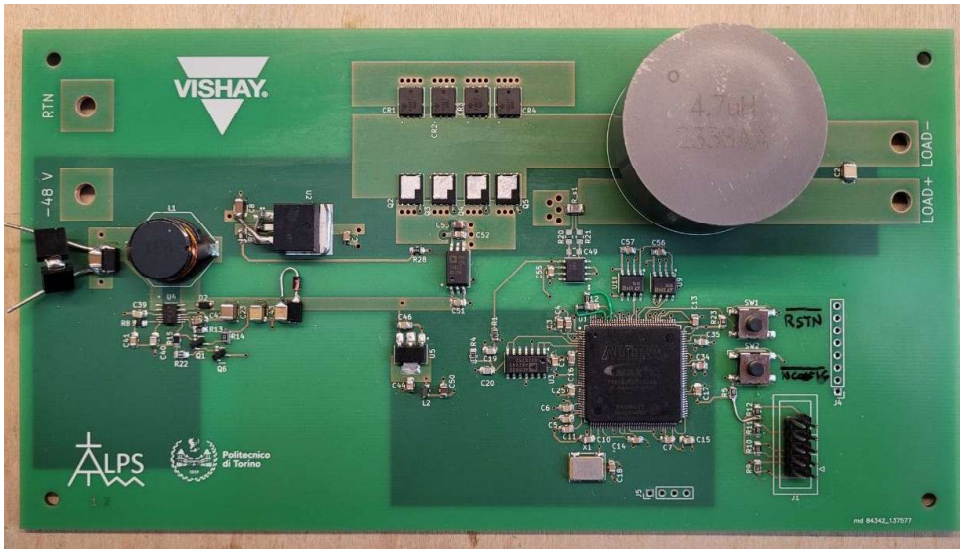



Figure 4.16: Final Assembled PCB.

# Chapter 5

# Conclusion and future perspectives

This work attempts to be a starting point, not only in the field of hot swap applications, but for all those power electronic circuits that rely on soft start, pre-charge phases or current limitation in general.

As explained in the background section 2.1, as the current levels arose in the past years, the limitation of the Trench Power MOSFETs began to look more restrictive.

The optimization of the figure of merit (FOM = $R_{ds,on} * Q_g$), i.e. on-resistance and gate charge performance of the power MOSFETs, has completely shattered the possibility of working in linear region with reasonable level of power. As described by the *Spirito's effect*, the transconductance growth yielded to problem related to thermal instability and consequently large safe operating area reduction. Some manufacturer solved the problem with new devices (sometimes referred to ASFETs), engineered for linear mode operation and larger SOA. This solution, however, can be very expensive, not only in terms of engineering cost, but the incompatibility between large linear region SOA and high current capability in resistive region, force employment of both ASFTEs and Trench MOSFETs devices in the same circuit.

Therefore, the idea carried out in this thesis take advantage of Trench MOSFETs operated in switching fashion, which is what they are engineered for, to limit a current that is usually contained through a linear region operation mode. This will eliminate the needs for SOA optimized devices, cutting the engineering and the bill of material costs.

Taking as inspiration a typical power MOSFETs switching application, a current controller circuit has been derived, starting form a standard current mode Buck topology. The control strategy implemented is as simple as possible, represented by an hysteresis controller, that acts only as an on-off control. In this way the MOSFETs works in a switching condition and forces the current inside an hysteresis band, limited by the upper and lower thresholds.

The results obtained from circuital simulation prove that this idea could represent a very valuable solution, allowing to charge larger capacitance load in shorter time, providing better current capability while maintaining the same circuital protections and keeping under control the switching frequency.

In this thesis, a prototype board has been designed and tested, showing promising results. Surely, more work needs to be done before a real practical application. Nevertheless, the tests shown good capabilities, both in term of charging performance and circuital protections implementation, motivating further future studies.

As forthcoming project, a very intriguing perspective could be an Application Specific Integrated Circuit (ASIC) implementation of the topology realized, competing with the usual integrated Hot-Swap controller like the LT4284. Surely, some studies will be needed in order to implement the discussed behaviour inside an IC, but it could represent an additional cost cut. The controller logic is much simpler with respect to the classical linear mode Hot-Swap controller. Furthermore, this will also cut the SOA optimized MOSFET from the bill of material as well as the related output stage driver and SOA timer inside the IC.

# Bibliography


[1] "The Art of Hot-Swapping in Telecom Systems: Avoid a Patchwork and Implement a More Effective Solution", Sep 20 2010. By Hamed Sanogo

[2] "How to Select a MOSFET - Hot Swap" , Texas Instrument, April 2018

[3] LT Journal of Analog Innovation : "MOSFET Safe Operating Area and Hot Swap Circuits." Dan Eddleman. April 2017.

[4] , The trench power MOSFET: Part I - History, technology, and prospects. IEEE transaction on electron devices VOL.64 NO.3 March 2017, Richard K Williams, Mohamed Darwish, Richard Blanchard, Yusuke Kawaguchi, Ralf Siemieniec, Phil Rutter

[5] Vishay Application Note AN: "Power MOSFET Basics Understanding Superjunction Technology" , Sanjay Havanur and Philip Zuk, 21 April 2015

[6] Infineon Technologies Article: "The Split Gate Trench MOSFET: A developmental milestone of Field Effect Transistors for the power electronics Industry"

[7] Feng-Tso Chien, Chien-Nan Liao and Yao-Tsung Tsai, "A novel high channel density trench power MOSFETs design by asymmetric wing-cell structure," 2007 European Conference on Power Electronics and Applications, Aalborg, Denmark, 2007, pp. 1-7, doi: 10.1109/EPE.2007.4417401.

[8] Trench Gate Power MOSFET: Recent Advances and Innovations , Raghvendra Sahai Saxena and M. Jagadesh Kumar, Nova Science Publisher, 2012

[9] Nexperia Application Note 50006: "Power MOSFETs in linear mode", 12 April 2022

[10] Linear Technologies, LTC4251 component Datasheets, 2003

[11] ADI power Linear: LTC4284 component Datasheet, 07-2021

[12] textbook "Lesson in Industrial Automation", chapter "Closed-loop Control System", control.com

[13] O. W. Zastrow, "Underground Corrosion and Electrical Grounding," in IEEE Transactions on Industry and General Applications, vol. IGA-3, no. 3, pp. 237-243, May 1967

[14] Vishay Dale, Technical Documentation, IHTH-1500MZ-5A Datatsheet.

[15] Power Metal Strip® Current Sense Resistors, Low Value (0.3 m to 3 m), Surface-Mount, High Power. Vishay Dale

[16] SiJH5700E, Vishay Siliconix, N-Channel 150V (D-S) 175 °C, Vishay Datasheet

[17] SiDR570EP, Vishay Siliconix, N-Channel 150V (D-S) 175 °C, Vishay Datasheet
[18] V30K170, Vishay General Semiconductor, High Current Desinty Surface-Mount (TMBS), Trench MOS Barrier Schottky Rectifier, Vishay Datasheet
[19] Linear Technologies, UltraFast Precision 10ns Comparator, LT1016 Datasheet (Rev. D)
[20] Analog Devices, Technical Documentation. AD8410A: 2 V to 70 V Wide Input Voltage Range, 2.2 MHz High Bandwidth, Current-Sense Amplifier with PWM Rejection and Gain 20 V/V
[21] Linear Technologies Documentation, Low IQ Boost/SEPIC/Inverting Converter with 1.5A, 150V Switch, LT8365 Datasheets (Rev.A)
[22] OnSemi technical documentation, High Voltage Transistor PNP Silicon, MMBT5401L.
[23] Chip Multilayer Ceramic Capacitor for General Purpose, GRM32ER61A107ME20 (1210, X5R, 100 µF, DC 10 V )
[24] Texas Instrument technical documentation, TLV1117LV 1-A, Positive Fixed Voltage, Low-Dropout Regulator
[25] Analog Devices technical documentation, Isolated Precision Gate Driver with 2 A Output, ADuM4120 Datasheet.
[26] Texas Instrument technical documentation: TL783, High-Voltage Adjustable Regulator.
[27] Capacity Control of a Vehicle Air-Conditioning System using Pulse Width Modulated Duty Cycle Compressor, Gwan Soo Ko, Waseem Raza, Youn Cheol Park
[28] Intel Altera MAX10 Analog to Digital Converter User Guide, Intel Altera.
[29] Intel Altera MAX10 Device Handbook - Combined.
[30] Intel Altera MAX10 Device Configuration User Guide.
[31] Vishay General Semiconductor, Surface Mount XClampRTM Transient Voltage Suppressors, XMC7K24CA Datasheet.
[32] LT Journal of Analog Innovation : "Analysis of Hot Swap Circuits with Foldback Current Limit." Vladimir Ostrerov, Josh Simonson. January 2015.
[33] Maxim Integrated, Reference Design 4163: "Telecom Hot-Swap Reference Design Is Immune to Overvoltage and Brownout Input Transients", Mar 26 2008.
[34] Maxim Integrated, Application Note 2158: " Advantages of IC-Based Hot-Swap Circuit Protection ", Sep 20 2010.
[35] Linear Technology Magazine : "Hot Swap for High Availability Systems", David Soo, November 2004.
[36] Linear Technology Magazine : "48 Volt Hot Swap Controller for Negative Voltages", Henry Yun and Robert Reay, August 1998.
[37] Linear Technology Magazine : "–48V Hot Swap Controller Offers Comprehensive Protection for Telecom Systems", YK Sim and Mitchell Lee, March 2003.