POLITECNICO DI TORINO

**Dipartimento di Elettronica e Telecomunicazioni**
**Corso di Laurea Magistrale in Ingegneria Elettronica (Electronic Engineering)**

Master's Thesis

# Design of a high-speed voltage comparator for a GaN HEMT active gate driver


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*To the women who*
*inspired me*

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# Abstract

GaN HEMTs (high-electron-mobility transistors) have been gaining popularity in power electronics applications due to their advantages with respect to silicon power transistors, such as higher speed, lower ON resistance, larger breakdown voltage and smaller size. Driving this new generation of power transistors, however, presents some challenges: the large slew rates (for both voltage and current) associated with high-speed operation can lead to EMI (electromagnetic interference) and voltage oscillations. When it comes to gate voltage range, GaN HEMTs have stricter requirements compared to silicon power transistors, which means that these voltage oscillations can either inadvertently turn on the device or outright damage it.

This thesis focuses on how to detect voltage oscillations after the turn-off of the GaN device through the use of a CMOS comparator built into the active gate driver. The most critical parameters when designing this comparator were its speed and the trade-off with power consumption.

Several existing topologies were analysed to check whether they could match the provided design specifications, until a suitable one was found. The final schematic involves a self-biased differential amplifier, an inverter and a monostable circuit, plus an ESD (electrostatic discharge) protection and conditioning circuit at the input.

The document presents the design steps as well as the results of the simulations. The inputs to the comparator are a constant reference voltage (generated through a bandgap circuit and equal to 1.242 V) and the voltage ringing at the gate of the GaN HEMT, which is modelled as a triangular impulse of duration 1 ns, period equal to 10 µs and amplitude variable between 1 and 10 V. The voltage supply is set at 3 V. The output is loaded with a 100 fF ideal capacitance to simulate a buffer, whose design is beyond the scope of this thesis.

The comparator's rail-to-rail output switches successfully in compliance with the provided specifications in terms of voltage, power consumption, and operating temperature. The monostable circuit keeps the output stable for about 10 ns after the impulse is detected, so that the active gate driver's control unit can interpret the transition correctly and protect the GaN device.

In conclusion, this high-speed comparator with wide input range can be considered a useful tool to monitor the voltage oscillations at the power device's gate terminal, providing a safety feature for the active gate driver which may help increase reliability and lifespan of the GaN power device.

# Contents

# List of Tables

# List of Figures

# Chapter 1

# State of the art

## 1.1 Theory

According to Allen and Holberg [2011], a comparator is a circuit with two analog inputs whose output is a binary value based on the comparison of the input signals. For a non-inverting comparator, the output will be high ($v_{OUT} = V_{OH}$) when the difference between the non-inverting input $v_P$ and the inverting input $v_N$ is positive and the output will be low ($v_{OUT} = V_{OL}$) when their difference is negative.
Ideally, the output will change state for an infinitesimal input difference $\Delta V$ (figure 1.1). For real comparators, a minimum input difference $v_{MIN}$ is needed for the output to switch. This parameter is called ***resolution*** (figure 1.2).
The comparator ***minimum gain***, required to saturate the output for the whole input range is then defined as:

$$A_v = \frac{V_{OH} - V_{OL}}{v_{MIN}} \tag{1.1}$$

Another cause of non-ideality is the comparator's ***offset*** $V_{OS}$. The switching point for the output goes from being centred around zero input difference to being centred around a random value $V_{OS}$ (figure 1.3).
Common mode input range (***CMIR***) also plays an important role in the comparator's performance. This is typically the voltage range for which every transistor inside the comparator operates in its intended region (usually saturation).
The values of $V_{OH}$ and $V_{OL}$ determine the output range (***OR***). Ideally, this range is rail-to-rail, but depending on the topology it might not be. If the OR does not satisfy the requirements for the next stage to interpret the logic value correctly, an additional output stage might be required for the comparator.
Since comparators share several similarities with operational amplifiers, their symbol is similar (figure 1.4).

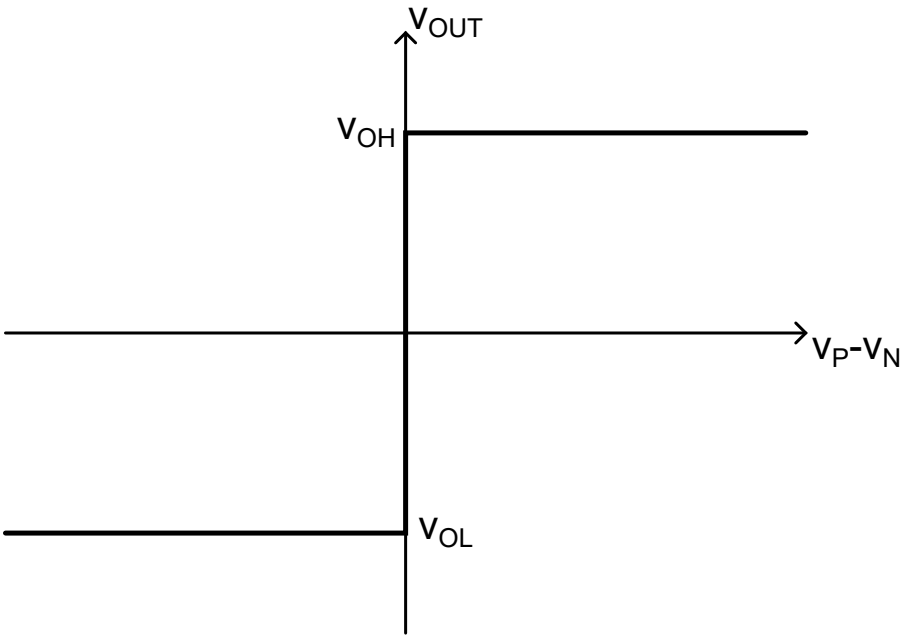


Figure 1.1. Static characteristics for an ideal comparator

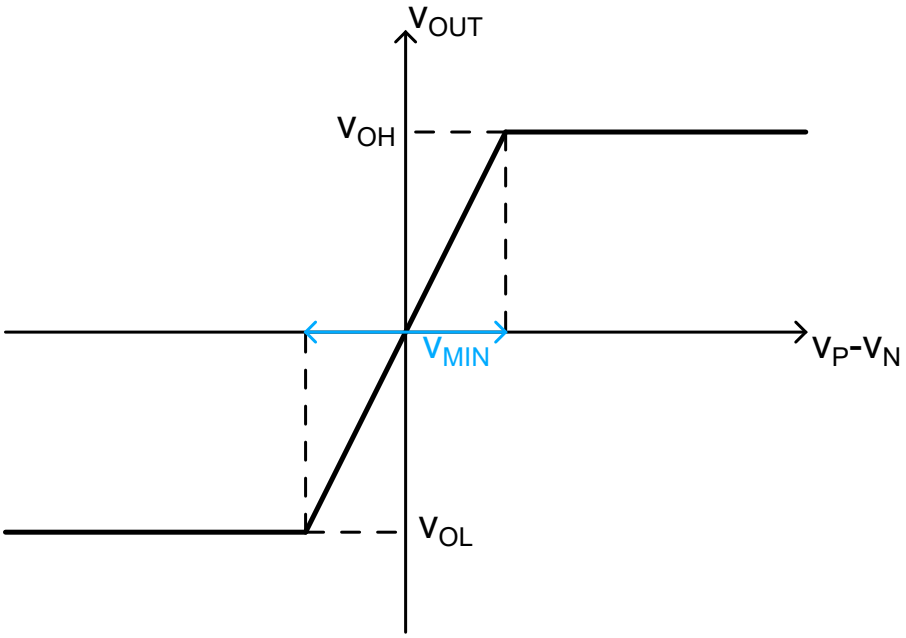


Figure 1.2. Static characteristics for a comparator with finite resolution

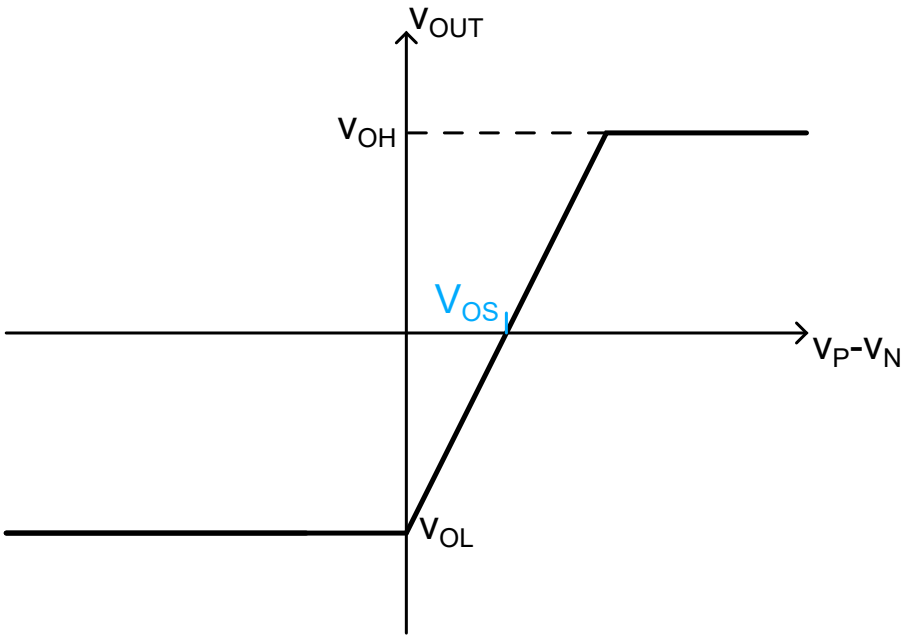


Figure 1.3. Static characteristics for a comparator with offset

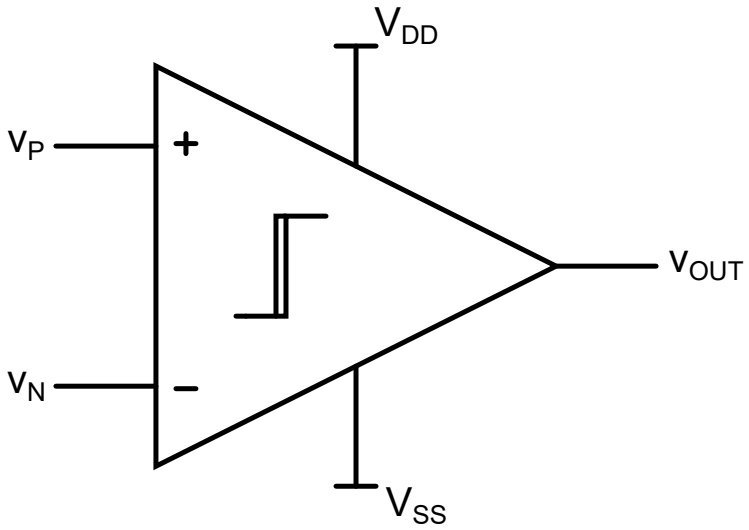


Figure 1.4. Comparator symbol

Regarding their dynamic behaviour, the main parameter of interest for comparators is their ***propagation delay***, $t_D$, which describes the time interval between the 50% variation at the input and the 50% variation at the output. This parameter depends both on the circuit bandwidth and on the amplitude of the input voltage (with larger delays for smaller inputs and vice-versa). In any case, $t_D$ can be reduced by increasing the comparator's ***slew rate***:

$$SR = \frac{dV}{dt} \tag{1.2}$$

If the load is capacitive (with negligible parasitic capacitance at the comparator's output node), the output sourcing and sinking current will be:

$$I = C_{load}\frac{dV}{dt} = C_{load}SR \tag{1.3}$$

The slew rate can then be expressed as:

$$SR = \frac{I}{C_{load}} \tag{1.4}$$

Since $C_{load}$ is usually a design constraint rather than a parameter which can be set, the only remaining margin of freedom is the output sourcing and sinking current, which means there is a trade-off between speed and power consumption.
The main difference between a basic comparator and an operational amplifier is that the comparator's output must be a binary value and so it has to saturate. This is easily achievable by using the same topologies used for operational amplifiers (provided they have sufficient gain) and using them in an open-loop configuration.
Open-loop operation means that compensation is no longer necessary, allowing for maximum bandwidth and smaller delays.

## 1.2 Two-stage OTA (open-loop)

The schematic for a two-stage operational trans-amplifier (OTA) presented by Allen and Holberg [2011] involves a nMOS differential pair (M1A, M1B) with asymmetrical loads (current mirror M2A, M2B) and current biasing through M0. The output node of the first stage is connected to a pMOS common-source (M3) biased in class A through M4 (figure 1.5). The dual topology (pMOS differential couple) is also possible to implement.
In the absence of a differential input signal and assuming the differential couple is perfectly symmetrical, the current through M1A and M1B is the same and it equals half of the current through M0 (determined by the bias network, not shown). Once a differential signal is applied and since M2A and M2B mirror the current through M1A, the first stage output node will reflect the current imbalance in the differential couple. The second stage then acts a current sink or source for the load, depending on the polarity of the imbalance: if $v_P$ is larger than $v_N$ the voltage at the gate of M3 drops, which increases the current through it and charges the load (since the current through M4 is fixed by the bias network); if $v_N$ is larger than $v_P$ the voltage at the gate of M3 rises and progressively turns it off, while the load discharges through M4.

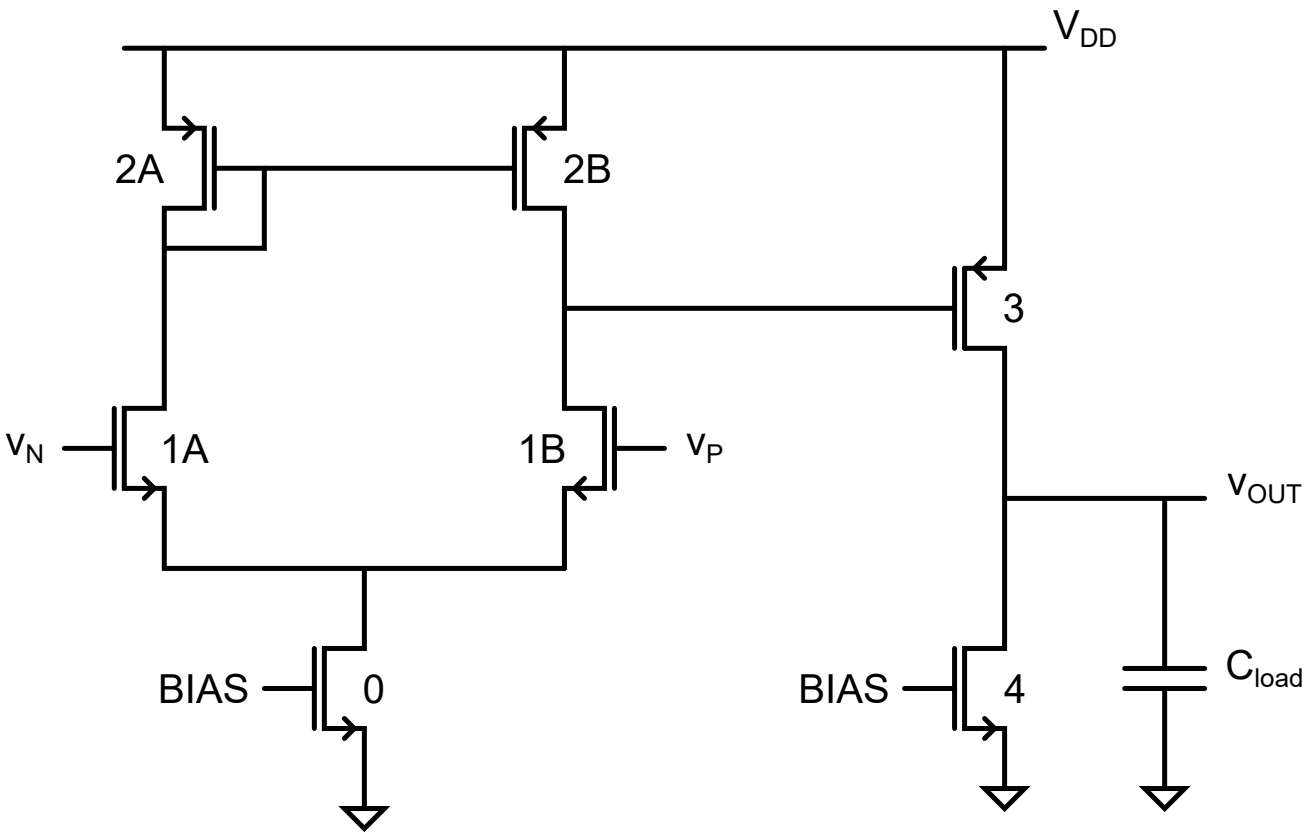


Figure 1.5. Schematic of a two-stage OTA

Allen and Holberg [2011]

Let's analyse this topology according to the parameters presented thus far:
The small-signal ***gain*** is:

$$A_v = \frac{g_{m1}}{g_{o1} + g_{o2}} \frac{g_{m3}}{g_{o3} + g_{o4}} \tag{1.5}$$

Where (assuming the MOSFETs operate in saturation):

$$g_m = \sqrt{\frac{2K' i_D W}{L}} \tag{1.6}$$

is the transconductance $\delta i_d / \delta v_{gs}$ and:

$$g_o = i_D \lambda \tag{1.7}$$

is the output conductance $\delta i_d / \delta v_{ds}$.
An ***offset*** is inevitable due to the asymmetrical nature of the topology, even if all non-idealities are neglected.
All of the MOSFETs in this topology need to work in saturation ($v_{DS} > v_{GS} - V_{TH} = v_{OD}$).
The lower limit of the ***CMIR*** is determined by M0:

$$v_{DS0} > v_{OD0} \tag{1.8}$$

$$v_{CM} - v_{GS1} > v_{OD0} \tag{1.9}$$

$$v_{CM} > v_{OD0} + v_{OD1} + V_{THn} \tag{1.10}$$

while the upper limit of the ***CMIR*** is determined by the differential couple M1A, M1B:

$$v_{DS1} > v_{OD1} \tag{1.11}$$

$$V_{DD} - v_{SG2} - (v_{CM} - v_{GS1}) > v_{OD1} \tag{1.12}$$

$$V_{DD} - v_{OD2} - |V_{THp}| - v_{CM} + v_{OD1} + V_{THn} > v_{OD1} \tag{1.13}$$

$$v_{CM} < V_{DD} - v_{OD2} - |V_{THp}| + V_{THn} \tag{1.14}$$

It is an asymmetrical range, closer to the supply voltage than to zero. The dual topology offers the opposite performance.
The ***OR*** is almost rail-to-rail, with $V_{OL}$ going all the way to zero (or VSS for dual supply) while $V_{OH}$ is limited by the voltage drop on M3, which never shuts off completely.
The ***SR*** capability of this topology is limited by its sinking current and is set by the bias network. Class A output stages are not efficient since they require a constant non-zero quiescent current, as does the current biasing of the differential couple M1A and M1B. This means that the trade-off between power consumption and speed is far from optimal for this topology.

## 1.3 Hysteresis

If a comparator with small enough ***resolution*** and high enough speed works in a noisy environment, unwanted transitions can occur at the output (figure 1.6). This problem can be solved by inserting ***hysteresis***, a phenomenon where the comparator has two trip-points instead of one (figure 1.7). This creates a "buffer zone" where small changes at the input do not trigger output switches. Hysteresis can be achieved by implementing a positive feedback loop which can be either external (such as a resistor network) or internal.

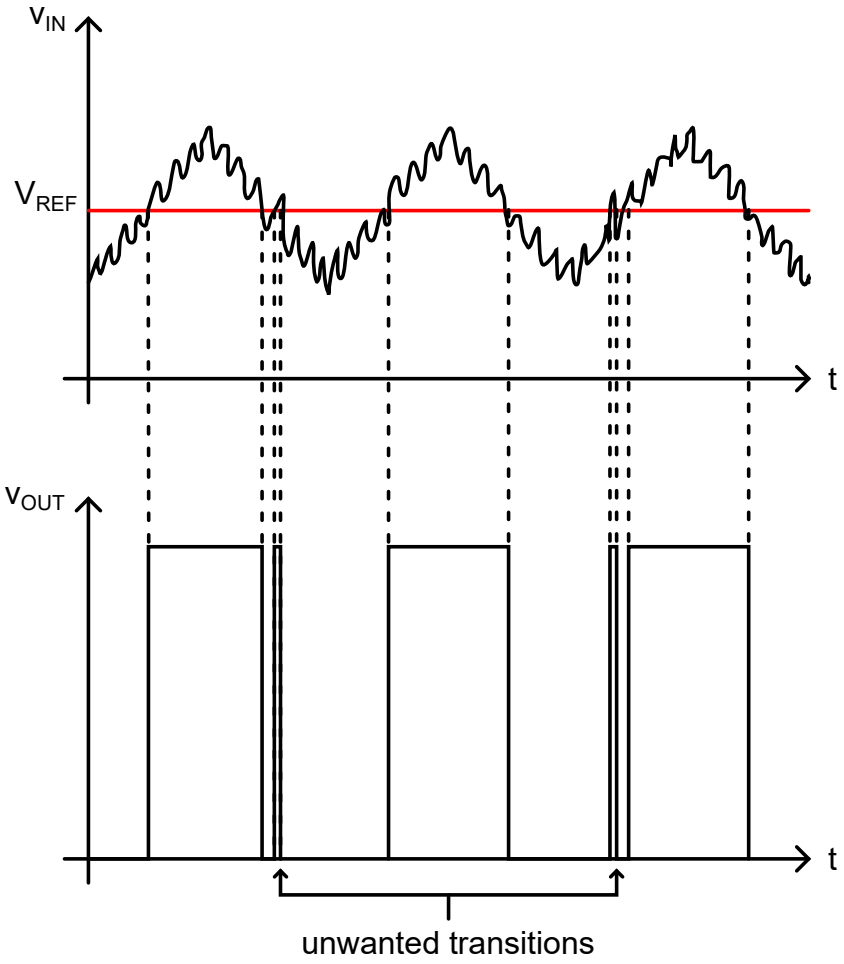


Figure 1.6. Time response of a comparator with noisy input

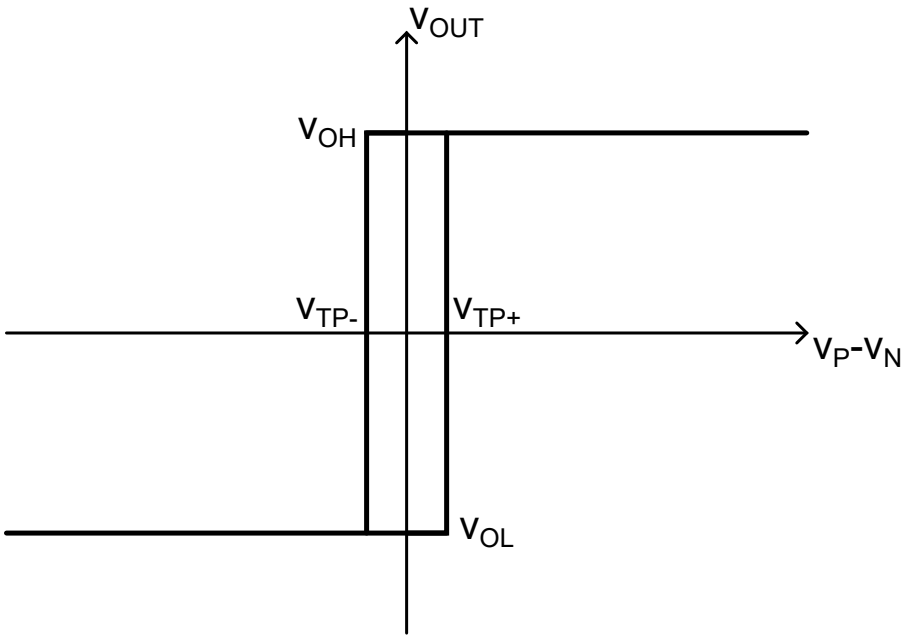


Figure 1.7. Static characteristics for a comparator with hysteresis

Let's examine a circuit with internal hysteresis as presented by Allen and Holberg [2011]. It involves a nMOS differential pair (M1A, M1B) with symmetrical diode-connected loads (M2A, M2B) and a positive feedback loop (M3A, M3B). The dual outputs of the first stage ($v_{O-}, v_{O+}$) are connected to a class AB output stage (pMOS M4, M6 and their current mirror loads M5, M7) (figure 1.8).
Just as in the OTA, in the absence of a differential input signal (assuming a perfectly symmetrical differential pair), the current through M1A and M1B is the same and it equals half of the current through M0 (determined by the bias network, not shown). Let's ignore the positive feedback loop for the moment. Once a differential input signal is applied, the current imbalance through M1A, M1B will affect the nodes $v_{O+}, v_{O-}$ which are connected to the gates of M4, M6 and determine their region of operation. The current through M4 and M5 is then mirrored to M7, provided they work in the saturation region, and the output node is charged or discharged depending on the polarity of the input. If $v_P > v_N$, then $v_{O+}$ will rise (turning off M4, then M5 and M7), while $v_{O-}$ will drop (turning on M6) and charging the output node. Once the output node is fully charged, since M7 is off, M6 will turn off too. If $v_N > v_P$, then $v_{O-}$ will rise (turning off M6) while $v_{O+}$ will drop (turning on M4, M5 and M7) and discharging the output node. Once again, when the output node is fully discharged and since M6 is off, M7 will turn off too.

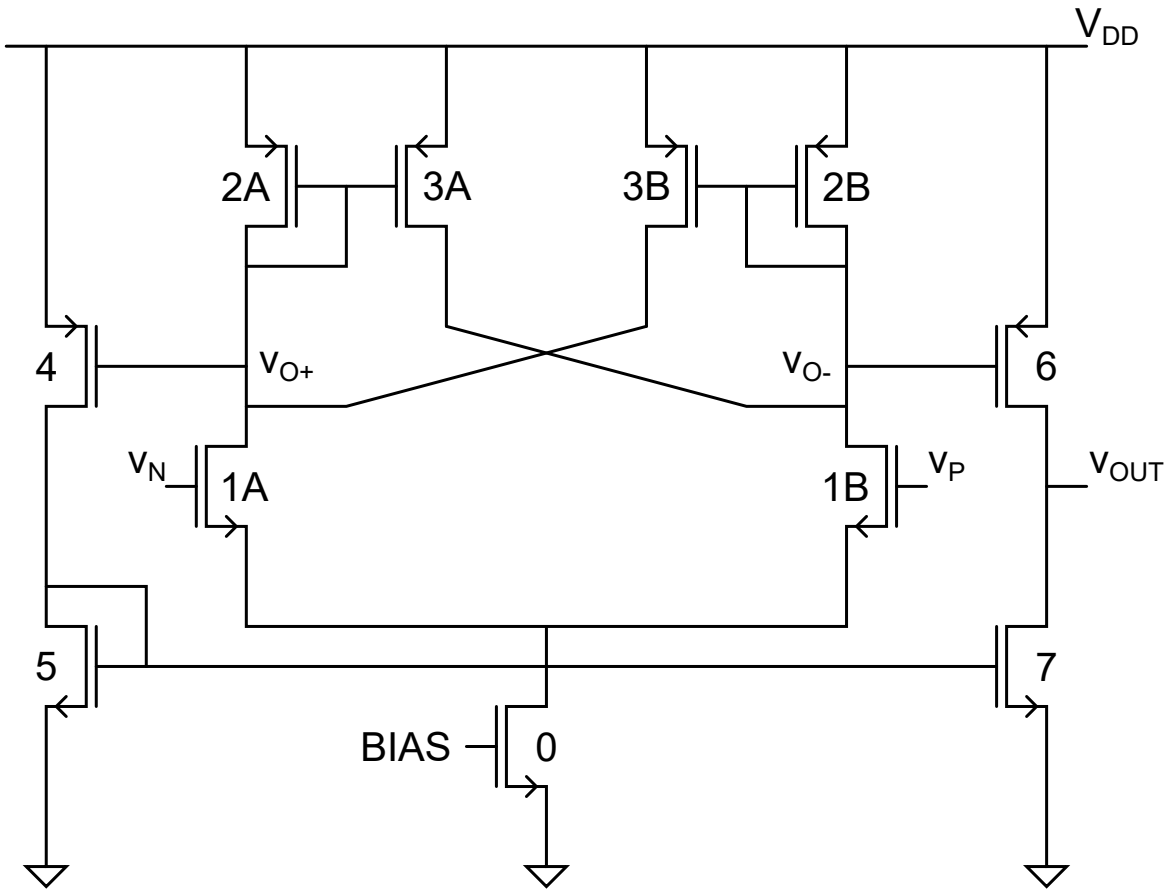


Figure 1.8. Comparator with internal hysteresis

Allen and Holberg [2011]

Now let's consider the complete circuit: in the first stage there are two paths from the inputs $v_P, v_N$ to the outputs $v_{O+}, v_{O-}$. One is the classical connection from common-source pair M1 to diode-connected loads M2 (which is inverting) and the other is a positive feedback loop through M3. In fact:

$$v_{O+} \uparrow \Rightarrow v_{SG3A} \downarrow \Rightarrow i_{3A} \downarrow \Rightarrow v_{O-} \downarrow \Rightarrow v_{SG3B} \uparrow \Rightarrow i_{3B} \uparrow \Rightarrow v_{O+} \uparrow \tag{1.15}$$

To successfully implement hysteresis inside the circuit, the positive feedback loop needs to overrule the inverting path. To do so, it is sufficient to size the MOSFETs in such a way that:

$$\beta_3 > \beta_2 = K'_p \frac{W3}{L3} > K'_p \frac{W2}{L2} \tag{1.16}$$

Where $W$ represents the channel width and $L$ the channel length. Their ratio is known as ***aspect ratio***. $K' = \mu_0 C_{ox}$ is known as ***transconduction parameter*** and depends on the technological process used to fabricate the circuit: $\mu_0$ is the surface mobility of the

channel and $C_{ox}$ is the gate oxide capacitance per unit area.
To understand when the trip points $V_{TP}$ occur with hysteresis, let's start with $v_P << v_N$ so that the differential couple is completely imbalanced towards M1A and $i_{1A} = i_0$ while M1B is off. M2A is on with $i_{2A} = i_{1A} = i_0$ and M3A, being in a current mirror configuration, tries to source:

$$i_{3A} = \frac{W3A/L3A}{W2A/L2A} i_{2A} = \frac{W3A/L3A}{W2A/L2A} i_0 \tag{1.17}$$

As $v_P$ increases towards the threshold point $V_{TP+}$ M1B will start to turn on and draw some current from M0, up to the point where $i_{1B} = i_{3A}$. Immediately afterwards, the output of the comparator switches states, marking the positive trip point. The dual reasoning is true for the negative trip point $V_{TP-}$.
The main differences with respect to the previous comparator (two-stage OTA in open-loop), apart from the implementation of hysteresis are:

- Since the topology of the first stage is symmetrical there is no systematic ***offset***.
- The ***OR*** is completely rail-to-rail because M6 and M7 both turn off after respectively sourcing and sinking the output current.
- The ***SR*** depends entirely on the sourcing and sinking capability of M6 and M7 (which is directly proportional to their aspect ratio) and is consequently independent of the bias. Note, however, that larger transistors exhibit larger parasitic capacitance, which limits the bandwidth when connected to a high-impedance node (such as the output).
- In terms of power consumption, the class AB output stage allows for higher efficiency.

Overall, this topology increases functionality, efficiency and possibly slew rate (depending on how the output stage is sized), at the cost of a larger occupied area. Still, faster comparator topologies exist for high-speed operation.

## 1.4 Clocked comparators

As the name suggests, clocked comparators rely on a timing signal to work. They function as a comparator only during part of their period and typically rely on additional memory circuits to provide reliable information during the rest. The additional complexity of these kinds of topologies is rewarded by low propagation delays, which make them suitable to high-speed applications. There are two main families of clocked comparators:

- Switched capacitor comparators
- Regenerative comparators

The focus of this analysis is concentrated on the latter.

### 1.4.1 Latches

The basis of operation for regenerative comparators is a positive feedback element known as latch (or bistable). Allen and Holberg [2011] showcase its simplest possible implementations (figure 1.9).

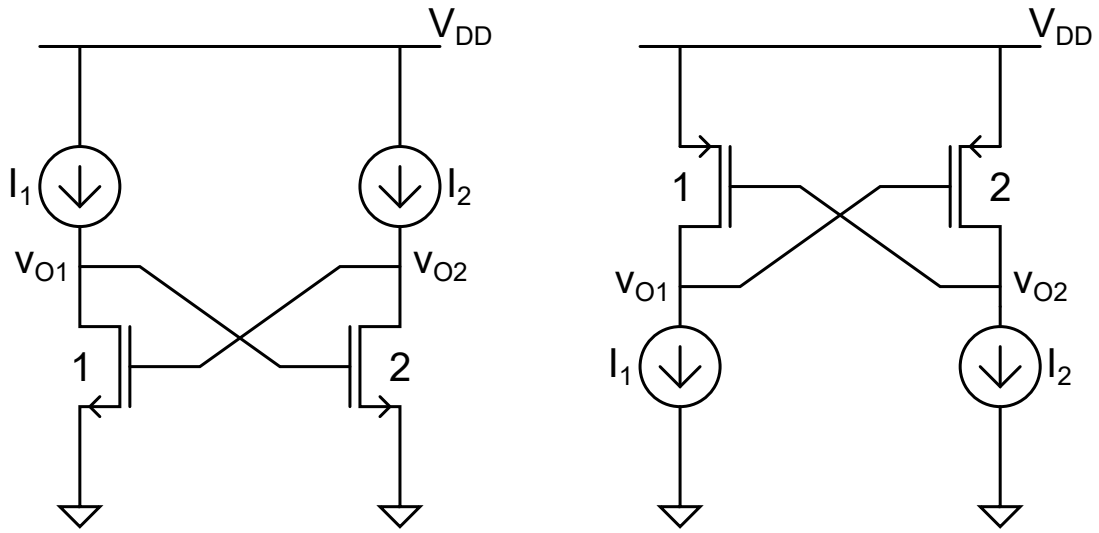


Figure 1.9. Basic latches

Allen and Holberg [2011]

Both versions (nMOS and pMOS) work according to the same principle. A clock determines two phases of operation:

1. Latch disabled → the differential input is applied and the base value for the outputs is established: $v_{O1}(t_0), v_{O2}(t_0)$.
2. Latch enabled → with positive feedback the outputs $v_{O1}, v_{O2}$ quickly reach opposite digital levels according to their base values $v_{O1}(t_0), v_{O2}(t_0)$ and the input.

Assuming that the circuit is symmetrical, its positive exponential response exhibits a time constant equal to:

$$\tau_L \approx \frac{2}{3} C_{ox} \sqrt{\frac{WL^3}{2K'I}} \tag{1.18}$$

Where $C_{ox}$ and $K'$ depend on the technological process, $W$ is the channel width, $L$ the channel length and $I$ the current. The propagation delay is:

$$t_D = \tau_L \ln\left(\frac{V_{OH} - V_{OL}}{2\Delta V_i}\right) \tag{1.19}$$

Where:

$$\Delta V_i = v_{O2}(t_0) - v_{O1}(t_0) \tag{1.20}$$

Equations 1.18 and 1.19 allow two important considerations:

- The propagation delay $t_D$ grows with the time constant $\tau_L$ and decreases when the differential signal $\Delta V_i$ increases.
- The time constant $\tau_L$ grows with the size of the MOSFETs and decreases when the current increases.

In summary, to better exploit the positive exponential response of latches it is crucial to establish a large enough differential signal during phase one and it is best to keep transistor sizing small.

### 1.4.2 Latched comparators

Figueiredo and Vital [2006] offer an overview of regenerative comparators making use of latches and present the problem of kickback noise.
The first example is a ***static latched comparator***(figure 1.10).

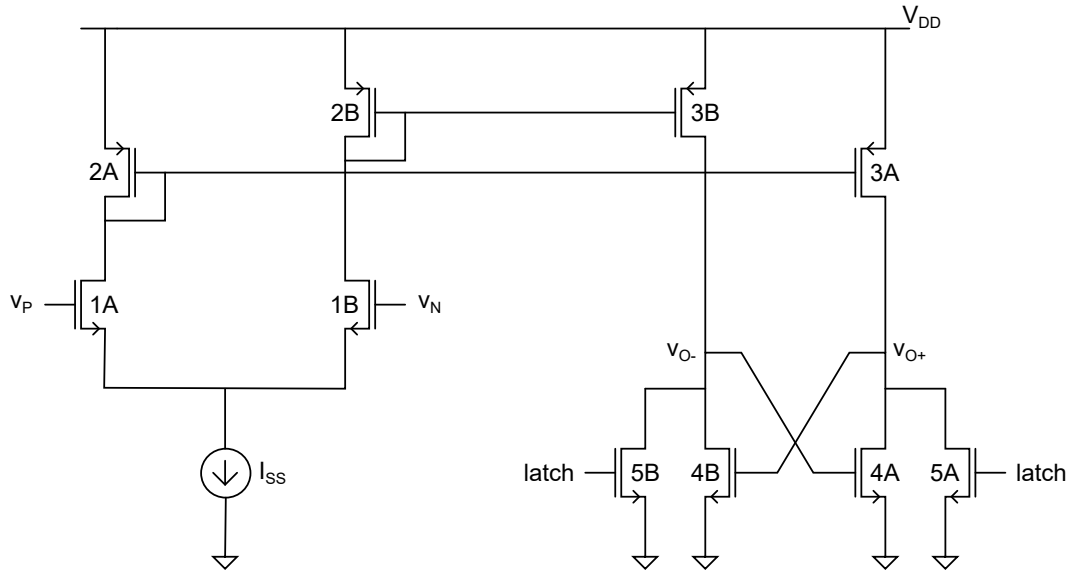


Figure 1.10. Static latched comparator

Figueiredo and Vital [2006]

The first stage is composed of differential couple M1A, M1B with current bias $I_{SS}$ and diode-connected loads M2A, M2B. The second stage mirrors the current through the differential pair via M3A, M3B. The latch is implemented by M4A, M4B and the phase of operation is set by M5A, M5B, whose gates are connected to the clock signal ***latch***.

1. When ***latch*** is high, M5A and M5B are on, discharging the output nodes $v_{O+}, v_{O-}$ to ground. The positive feedback implemented by M4A and M4B is deactivated.

2. When ***latch*** goes low, M5A and M5B are turned off. This allows the current through M3A to charge node $v_{O+}$ and the current through M3B to charge node $v_{O-}$. Since these currents are mirrored directly from the loads of the differential input pair, the polarity of the input signal will determine which node charges faster and which branch of the latch turns on first, starting the regeneration process through positive feedback and determining the logic level of the outputs.

This topology involves a class A final stage. This means that the regeneration speed is limited by the quiescent current and the trade-off between speed and power consumption is not optimal. In terms of kickback noise (propagated from the fast-changing, large-swing outputs towards the inputs) this topology performs well because first and second stage are coupled through current mirroring which provides shielding concerning voltage variations. The second example is a ***class AB latched comparator*** (figure 1.11).

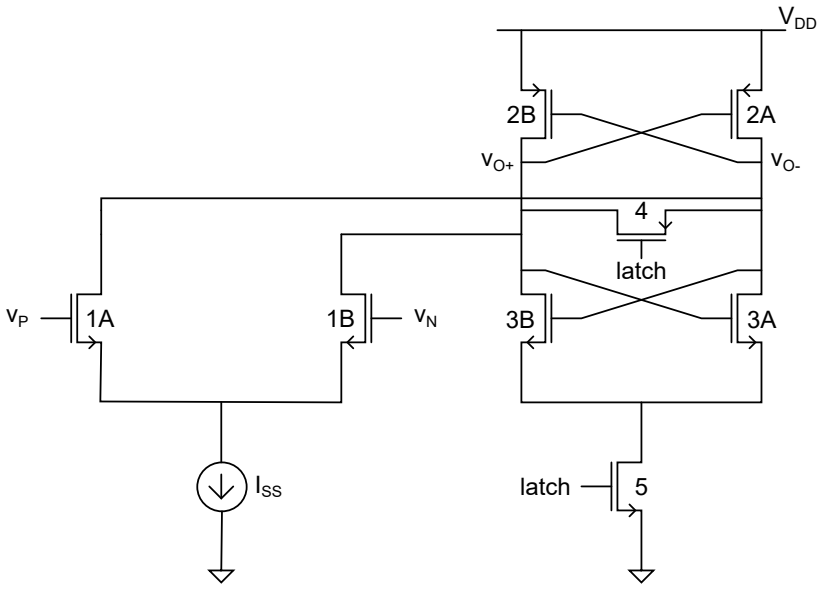


Figure 1.11. Class AB latched comparator

Figueiredo and Vital [2006]

The first stage is composed of differential couple M1A, M1B with current bias $I_{SS}$ and direct connection to the output nodes $v_{O+}, v_{O-}$. The second stage presents two latches in inverter configuration (pMOS M2A and M2B, nMOS M3A and M3B) and two reset switches (pMOS M4, nMOS M5) working alternately since they are of opposite types with both gates connected to the same clock signal ***latch***.

1. When ***latch*** is low, M5 is off (preventing current from flowing through M3A, M3B) while M4 is on. M2A and M2B serve as loads for the differential input couple M1A, M1B.

2. When ***latch*** goes high, M5 is turned on (activating M3A, M3B) while M4 is turned

off. The voltage at the outputs is regenerated to logic levels by the two latches, according to the polarity of the differential input voltage.

This topology is equipped with a class AB final stage. The regeneration speed is not limited by the quiescent current, allowing the comparator to switch faster and more efficiently. However, there is still quiescent current consumption during phase 1 and the outputs are directly connected to the input differential pair, which can be easily injected by kickback noise through their parasitic capacitances.
The final example is a ***dynamic latched comparator*** (figure 1.12).

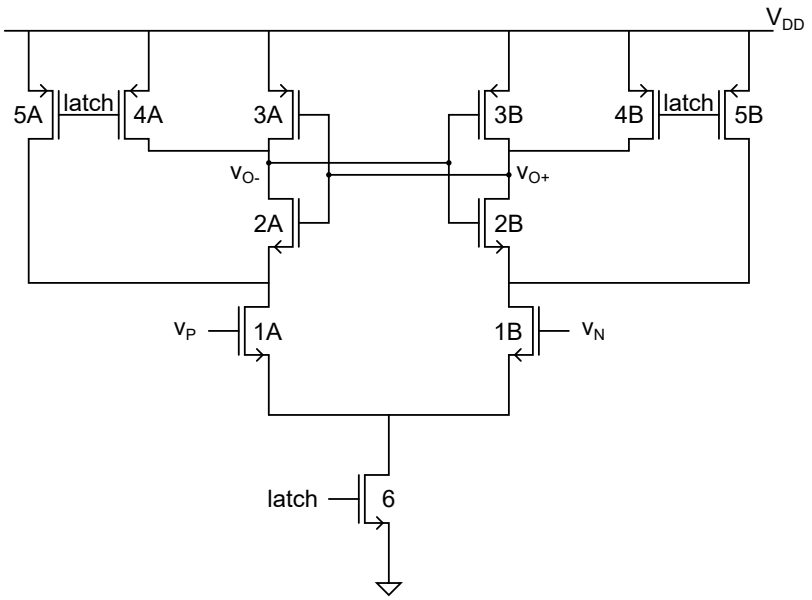


Figure 1.12. Dynamic latched comparator

Figueiredo and Vital [2006]

This topology includes a nMOS differential input pair (M1A, M1B), two latches in inverter configuration (nMOS M2A and M2B, pMOS M3A and M3B) and several switches controlled by the same clock signal ***latch***: M4A and M4B to reset the output nodes to $V_{DD}$, M5A and M5B to reset the drain nodes of the differential pair to $V_{DD}$, and finally M6 to disable current flow through the differential pair.

1. When ***latch*** is low, M6 is off (disabling the differential pair) while the pairs M4 and M5 are on, charging the output and drain nodes to $V_{DD}$, respectively.

2. When ***latch*** first goes high, the pairs M4 and M5 turn off while M6 turns on (activating the differential pair). Current starts flowing through M1A and M1B according to the differential input signal and the drain nodes are discharged at different rates according to the polarity of the current imbalance. Eventually, one between M2A and M2B turns on first, discharging the respective output node and being followed by the other.

3. Finally, when both output nodes are discharged enough to turn on both M3A and M3B, the positive feedback is activated for both latches and the outputs are regenerated to logic levels according to the input differential voltage.

This topology is called dynamic because the quiescent current is zero during the whole clock period. Current is momentarily supplied only during phase 2 (precharge) and at the beginning of phase 3 (regeneration) while the output nodes switch states. This makes this comparator faster than the static one and more efficient than the class AB. Kickback noise, however, is large: the voltage range for the drain nodes of the differential input pair is as large as the supply range. Moreover, the differential couple alternates between cut-off region (phase 1), saturation region (phase 2) and triode region (phase 3), varying their gate charges and reflecting on the input.
As pointed out by Razavi [2015], clocked comparators reflect the differential input value at the outputs only during a portion of their period. To be interpreted correctly by the following logic circuit, they need some sort of memory element (such as a SR latch) in between. Clocked signals also increase design complexity and produce EMI emissions that can affect the surrounding circuitry. Simpler topologies exist that are both fast and efficient.

## 1.5 High-speed, continuous time comparators

Baker [2019] presents the block diagram for high-performance voltage comparators (figure 1.13).

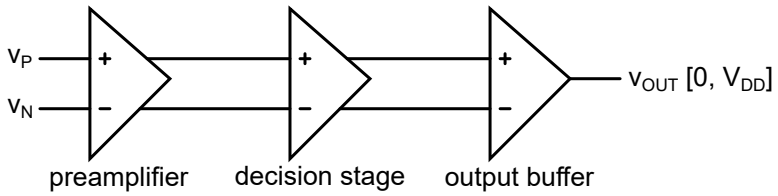


Figure 1.13. High-performance voltage comparator block diagram

Baker [2019]

The ***preamplifier*** gain must be high enough so that the minimum resolution is granted. This block also shields the input from kickback noise generated in the ***decision stage***, which generates its output levels through positive feedback and based on the outputs of the preamplifier. The output buffer must provide digital signal levels in accordance to the outputs of the decision stage and with sufficient slew rate to effectively charge and discharge the load (capacitive).
This approach is not incompatible with the clocked comparators described in section 1.4, but it can also describe time-continuous (or asynchronous) comparators.
Milovanović and Zimmermann [2013] proposed one such comparator (figure 1.14).

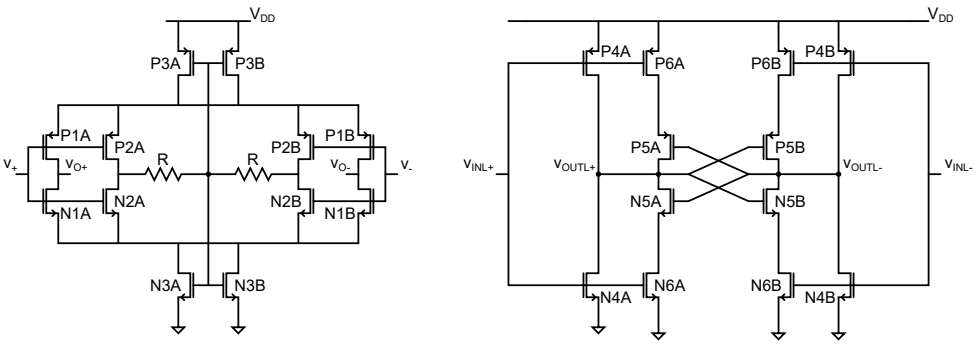


Figure 1.14. Continuous-time comparator

Milovanović and Zimmermann [2013]

The schematic on the left represents the preamplifier, which is self-biased. the schematic on the right represents the time-continuous latch, whose phases of operation are not determined by a clock signal but rather by the outputs of the preamplifier (which are connected to the inputs of the latch):

1. When $v_{INL} = v_O$ is low, MP4 and MP6 are on while MN4 and MN6 are off $\rightarrow$ the output $v_{OUTL}$ is equal to $V_{DD}$ while the regeneration circuit implemented by MN5, MP5 is deactivated. This is true for either positive (A) or negative (B) branch.

2. When $v_{INL} = v_O$ is high, MP4 and MP6 are off while MN4 and MN6 are on $\rightarrow$ the output $v_{OUTL}$ is equal to zero while the regeneration circuit implemented by MN5, MP5 is deactivated. This is true for either positive (A) or negative (B) branch.

3. Only when both $v_{INL+} = v_{O+}$ and $v_{INL-} = v_{O-}$ are near the trip point of the inverters composed by MP4, MN4 (during differential signal transitions) all MOSFETs in the circuit are on and the regeneration process is active to speed up the output switching.

This topology technically requires no output buffer because the outputs of the latch stage are already rail-to-rail. Depending on the required slew rate, however, a buffer might be necessary to provide enough sourcing and sinking current to the load. It can be as simple as a properly sized inverter.
The behaviour of the latch is completely dynamic, making it energy-efficient and fast without the need for a clock signal or memory elements.
It is crucial, however, to understand that in order to maximise the circuit performance the takeover point between preamplifier (negative exponential response) and latch (positive exponential response) needs to be set by fine-tuning transistor sizing until the optimum speed is achieved.
To better understand how the preamplifier works, let's refer to the work of Bazes [1991], who first presented the idea of a ***self-biased differential amplifier*** (figure 1.15).

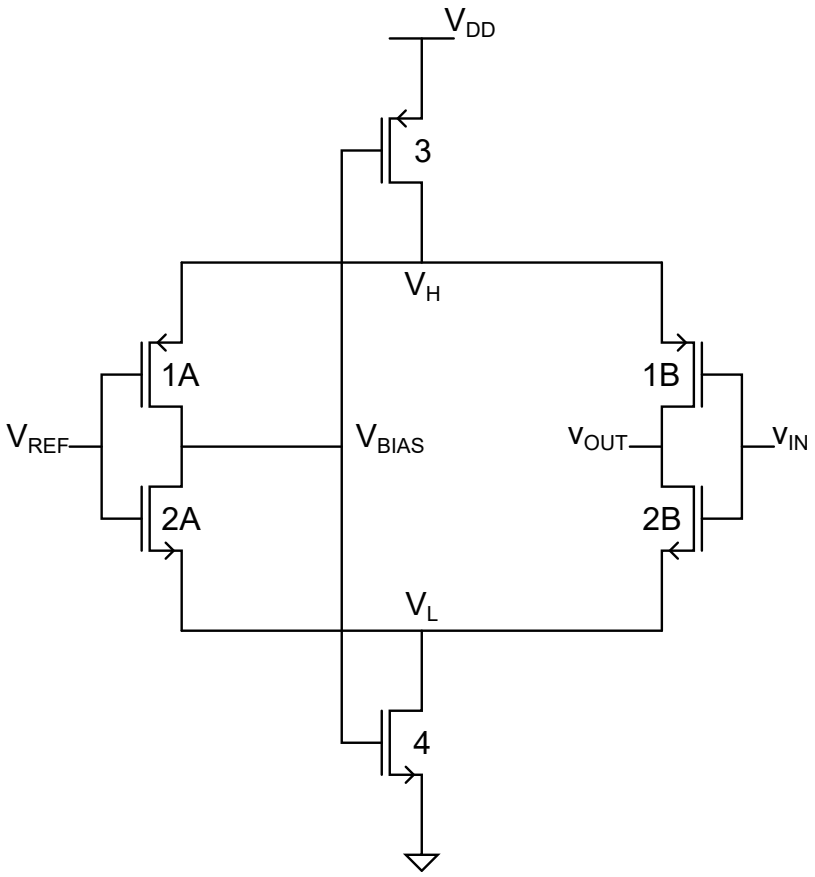


Figure 1.15. Self-biased differential amplifier

Bazes [1991]

This circuit is an evolution of the standard nMOS/pMOS differential couple with active loads and external current bias network. The differential couple is now in push-pull (inverter) configuration, with both M1A,B (pMOS) and M2A,B (nMOS) connected to the inputs. The circuit is biased internally through a negative feedback loop involving M3 and M4, whose gates are connected to one of the outputs leaving this configuration single-ended (and inverting). The main improvements with respect to the usual configuration are:

- $V_{BIAS}$ is now less sensitive to PVT (process, voltage, temperature) variations thanks to the negative feedback.
- The switching currents provided by M3 (source) and M4 (sink) are much larger than the quiescent current, offering a suitable trade-off between speed and power consumption.
- The differential voltage gain is doubled and equal to $A_v = \frac{g_{m1}+g_{m2}}{g_{out}}$

M3 and M4 should operate in the triode region. As a consequence, $V_H$ and $V_L$ are close to the supply voltage and ground respectively, so the output voltage $v_{OUT}$ has a large swing. Moreover, they are able to provide dynamic current behaviour, with low quiescent values and high peaks during commutation.
In terms of CMIR, this topology is limited by M3 and M4 having to be in the triode region for the amplifier to work as intended:

- If the voltage $V_{REF}$ drops too low, $V_{BIAS}$ will be so high that M3 turns off and it will be slow to turn on and source current to the output in case of variations at the input $v_{IN}$. Note that in this case, quiescent current consumption is null.
- If the voltage $V_{REF}$ rises too high, $V_{BIAS}$ will be so low that M4 turns off and it will be slow to turn on and sink current from the output in case of variations at the input $v_{IN}$. Note that in this case, quiescent current consumption is null.
- Only when $V_{REF}$ is close to the middle of the supply voltage range will $V_{BIAS}$ be stable in the same central range and keep both M3 and M4 on and ready to charge and discharge the output load. Quiescent current is larger than zero, but still modest compared to the maximum switching value.

The typical application for self-biased amplifiers is as preamplifiers for high-speed comparators: their trade-off between power consumption and slew rate is satisfactory and their output range is large enough to be interpreted correctly by the following decision stage (latch).
The input connected to the $V_{BIAS}$ node is typically connected to a constant reference voltage while the other input is the one varying, determining the output voltage $v_{OUT}$.
In conclusion, high-speed continuous time comparators are possible to implement with limited quiescent current consumption and were deemed the best option for the project described in this thesis. Thanks to their self-biased push-pull preamplifier and its dynamic current consumption, they have larger gain and are much faster compared to basic common-source differential amplifiers with external bias networks, while keeping static current consumption low. The presence of a decision stage makes their performance comparable to that of clocked comparators without the added complexity of a timing signal and memory circuits. Sizing the transistors, however, requires more attention since the takeover point between preamplifier and decision stage is not regulated by the clock.

# Chapter 2

# Project specifications and constraints

## 2.1 High-speed voltage comparator

The following specifications are provided:

- Supply voltage $V_{DD}$=3 V;
- Reference voltage $V_{REF}$=1.242 V;
- Quiescent supply current $I_Q \leq 100$ $\mu$A;
- Input voltage range [0, 10] V;
- Rail-to-rail, single-ended output;
- Load capacitance $C_{load}$=100 fF;
- Operating temperature range [-40, 125] °C;

The output of the comparator has to switch for a triangular input pulse of minimum amplitude 1 V and minimum duration 1 ns, which models the voltage oscillation after turn-off of the GaN device. The output must remain stable for about 10 ns after the first pulse to prevent any successive ringing of the input to cause multiple transitions at the output. The reference voltage is provided by a bandgap circuit. The load capacitance simulates a buffer.

## 2.2 Technological process

The provided technological process offers a 300 nm minimum channel length ($Lp_{min}$) for pMOS and a 350 nm minimum channel length ($Ln_{min}$) for nMOS.

The transistors were characterised according to the procedure illustrated in Allen and Holberg [2011]:

$$i_D = K' \frac{W}{2L}(v_{GS} - V_{TH})^2(1 + \lambda v_{DS}) \tag{2.1}$$

Equation (2.1) identifies the drain current through MOSFETs in the saturation region. The parameters to be characterised are:

- transconduction parameter $K'$ $(A/V^2)$;
- threshold voltage $V_{TH}$ $(V)$;
- channel length modulation parameter $\lambda$ $(V^{-1})$;

While:

- $v_{GS}$ represents gate to source voltage;
- $W$ represents channel width;
- $L$ represents channel length;
- $v_{DS}$ represents drain to source voltage;

Let's first assume that the term $\lambda v_{DS}$ is negligible so that equation (2.1) simplifies to:

$$i_D = K' \frac{W}{2L}(v_{GS} - V_{TH})^2 \tag{2.2}$$

Equation 2.2 can be rewritten as:

$$\sqrt{i_D} = \sqrt{K' \frac{W}{2L}}(v_{GS}) - \sqrt{K' \frac{W}{2L}}(V_{TH}) \tag{2.3}$$

Which is in the form:

$$y = mx + b \tag{2.4}$$

Equation (2.4) describes a straight line with slope m and b as the y-intercept.
By plotting the square root of $i_D$ as a function of $v_{GS}$ and measuring the slope of its linear portion (saturation region) the transconduction parameter $K'$ can be found through:

$$m = \frac{\Delta y}{\Delta x} = \sqrt{K' \frac{W}{2L}} \rightarrow K' = \left(\frac{\Delta y}{\Delta x}\right)^2 \frac{2L}{W} \tag{2.5}$$

Moreover, if the straight line that passes through the saturation region is extended and the intercept point on the x-axis is measured, the threshold voltage $V_{TH}$ is found:

$$y = 0 \rightarrow mx = -b \rightarrow v_{GS} = V_{TH} \tag{2.6}$$

Equation (2.1) can be also rewritten as:

$$i_D = i'_D \lambda v_{DS} + i'_D \tag{2.7}$$

Which is the same linear form seen in (2.4).
To determine the channel length modulation parameter $\lambda$ it is sufficient to plot $i_D$ as a function of $v_{DS}$ (output characteristic), measure the slope $i'_D\lambda$ of its linear portion (saturation region) and divide this value by the imaginary intercept point on the y-axis $(i'_D)$.

### 2.2.1 Simulation setup

The setup for nMOS characterisation involves connecting each terminal of the device to an ideal DC voltage generator (figure 2.1). For pMOS characterisation, the dual setup is employed (figure 2.2). To keep the sign convention consistent, the polarity of the generators can be reversed and the source current $i_S$ is measured instead of $i_D$. To avoid body effect, both $v_{BS}$ and $v_{SB}$ are set to zero.

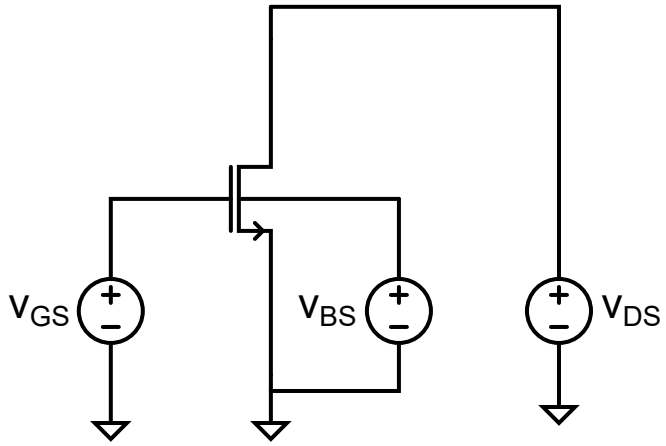


Figure 2.1. Simulation setup for nMOS characterisation

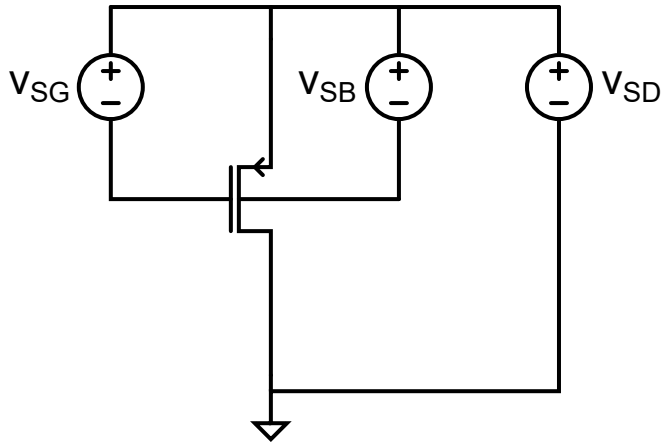


Figure 2.2. Simulation setup for pMOS characterisation

### 2.2.2 Simulation results

All the simulations were performed in the ADE L environment inside Cadence Virtuoso. A DC simulation was performed to plot $\sqrt{i_D}$ as a function of $v_{GS}$ for the nMOS (figure 2.3) and $\sqrt{i_S}$ as a function of $v_{SG}$ for the pMOS (figure 2.4). This allowed the characterisation of $K'_n$, $K'_p$, $V_{THn}$ and $V_{THp}$. Another DC simulation was performed to plot $i_D$ as a function of $v_{DS}$ for the nMOS (figure 2.5) and $i_S$ as a function of $v_{SD}$ for the pMOS (figure 2.6). These output characteristics were employed to find the value for $\lambda_n$ and $\lambda_p$.

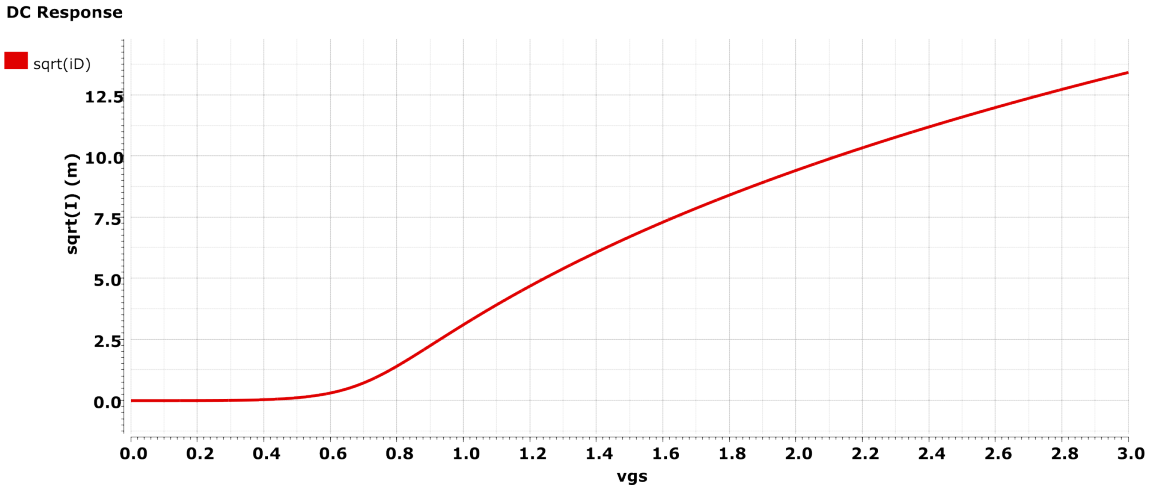


Figure 2.3. Trans-characteristics' square root (nMOS)

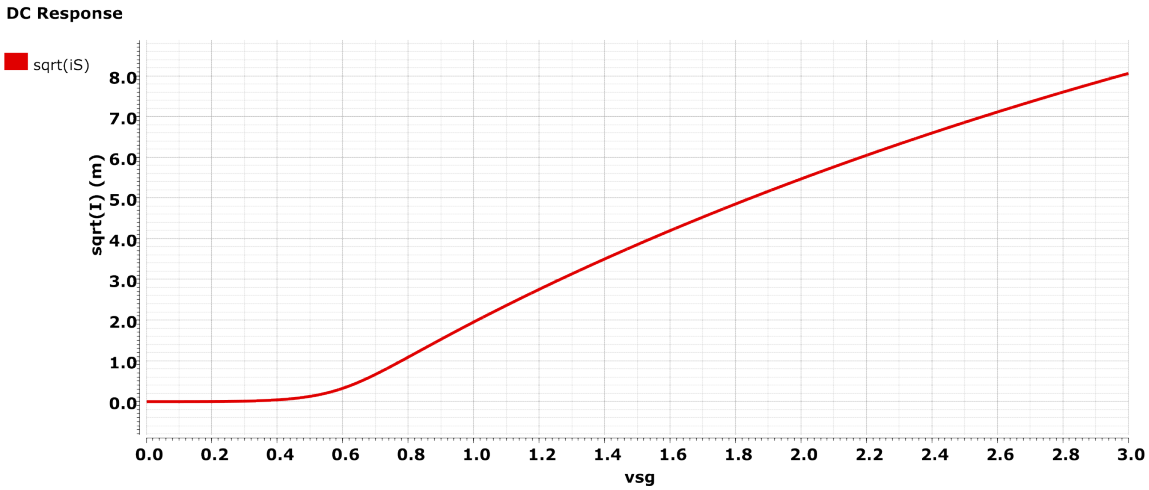


Figure 2.4. Trans-characteristics' square root (pMOS)

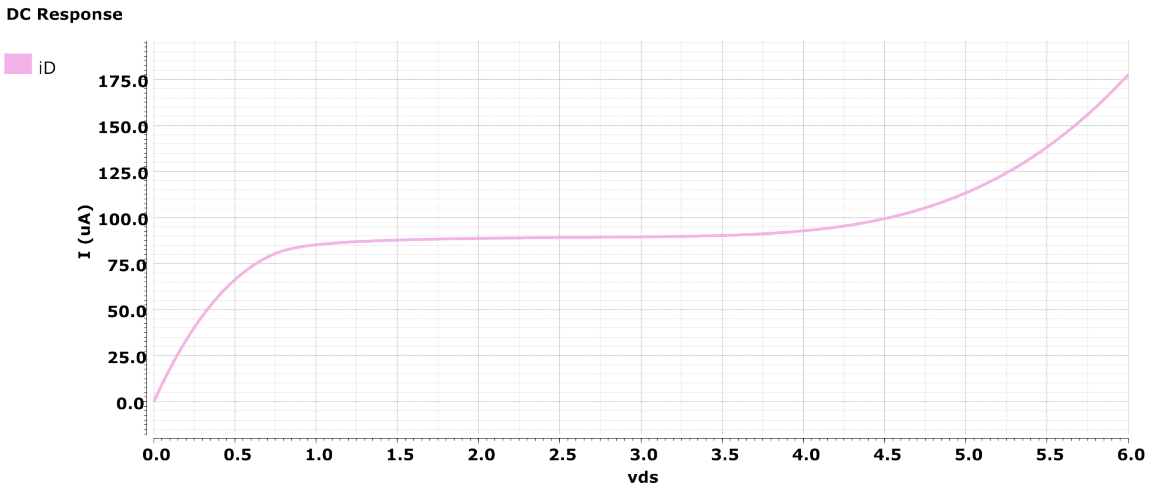


Figure 2.5. Output characteristics (nMOS)

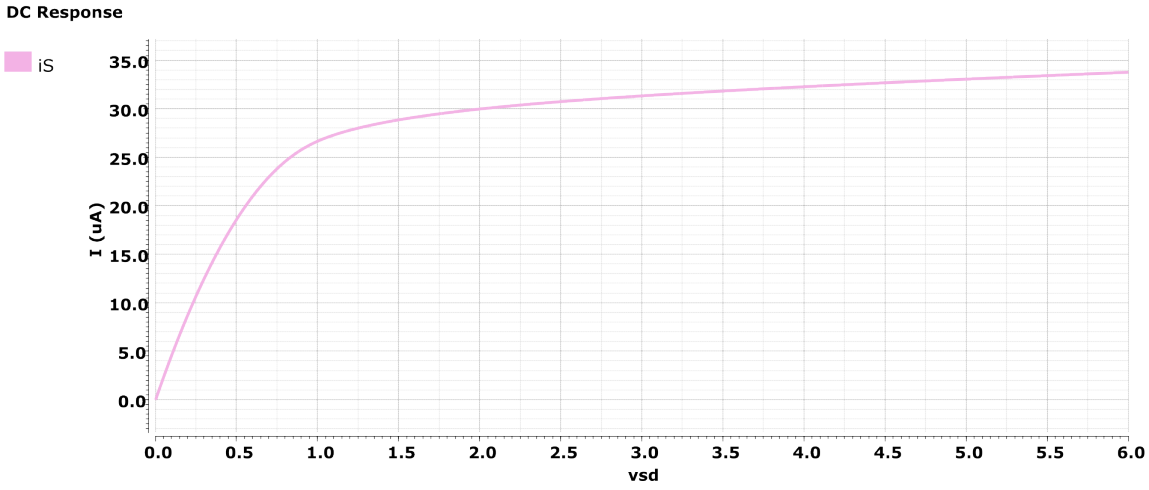


Figure 2.6. Output characteristics (pMOS)

# Chapter 3

# Design process

The design was broken down into three main blocks:

1. An ***input circuit*** with ESD (electrostatic discharge) protection, capable of conditioning the large-swing input signal into an acceptable CMOS range and providing voltage biasing for the comparator's inputs. See section 3.1.
2. A fast ***comparator*** with satisfactory trade-off between speed and power consumption. See section 3.2.
3. An ***output circuit*** with digital levels, sufficient slew rate to drive the capacitive load and capability to keep the output temporarily stable after the first pulse. See section 3.3.

## 3.1 Input

The input signal comes from the gate-source terminals of the GaN HEMT outside the active gate driver IC (integrated circuit). To provide sufficient robustness to the final design, an ***ESD protection*** is required.
For the purpose of this thesis, this signal is modelled as a triangular pulse of duration 1 ns, period 10 $\mu$s and variable amplitude in the range [1,10] V. This range not only goes far beyond the supply voltage (3 V), but it also exceeds the maximum voltage ratings for the provided MOSFETs (4 V between any two terminals). A ***voltage divider*** circuit is needed to reduce the input range to acceptable values.
Finally, to better exploit the comparator's performance, a ***DC voltage bias*** for its input terminal is necessary.

### 3.1.1 ESD protection

An input ESD protection is a type of circuit that protects the following circuits from ESD pulses (be they positive or negative) by offering an alternative low impedance path for the current to flow and by clamping the voltage on the input pad at a safe level. The ESD protection circuit must:

- Be inactive during nominal operation and activate only during an ESD event.
- React to the ESD event before it damages the following circuits.
- Be robust enough as to not receive any damage from the ESD event.
- Insert as little a time delay as possible.

The preferred topology for ESD protection circuits where the nominal input signal can be larger than the supply voltage is called ***pi-structure*** (figure 3.1).

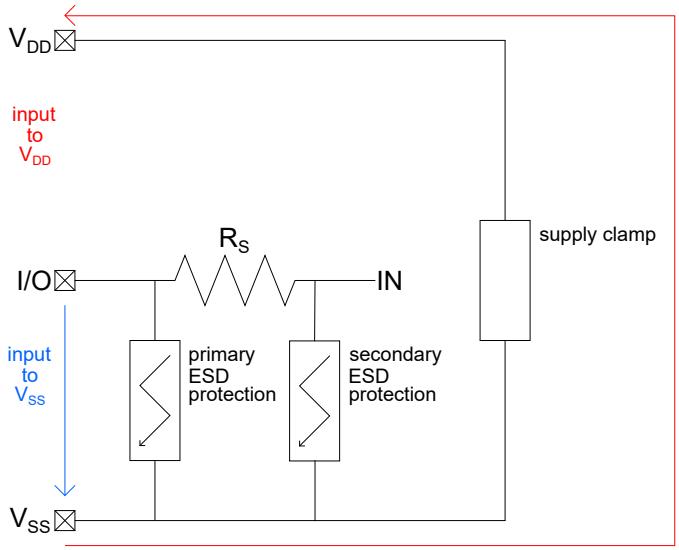


Figure 3.1. Pi-structure ESD protection circuit

The path from the input pad to $V_{SS}$ (or ground) is direct and goes through the ESD protection blocks. The path from the input pad to $V_{DD}$ requires an additional clamp on the supply.
A series resistance $R_S$ is needed to limit maximum current through the circuit. The process documentation suggests the use of a poly-resistor with a resistance value larger than 400 Ω.
To implement primary and secondary ESD protection several options are available:

- ggnMOS (grounded-gate nMOS).
- BJTs.
- SCR (silicon-controlled rectifiers).

While the best options to implement the supply clamp are:

- Diodes in series configuration.
- ggnMOS (grounded-gate nMOS).

- SCR (silicon-controlled rectifiers).

Let's focus on ggnMOS (figure 3.2) since they are easy to implement in CMOS technology and work for both blocks.

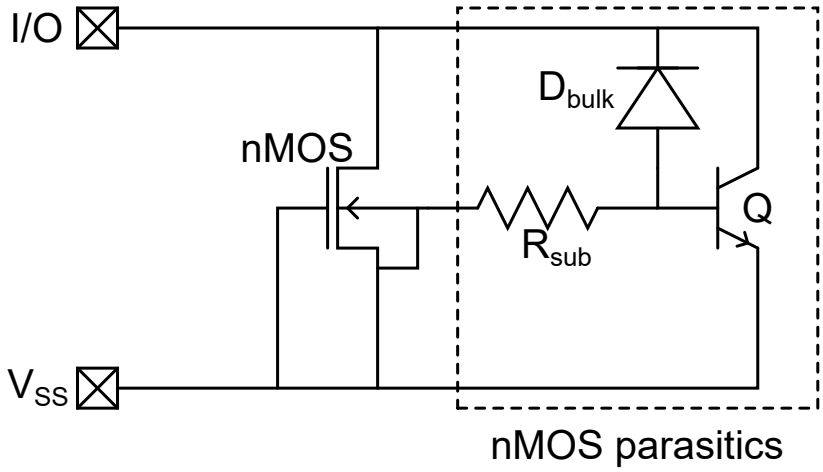


Figure 3.2. ggnMOS schematic

During normal operation, since the gate and source are shorted together, the nMOS is off. During an ESD pulse, however, the nMOS parasitic circuit will provide a path for the current to flow:

- If the pulse is positive, $D_{bulk}$ goes into breakdown. The current flowing into the substrate creates a voltage drop across $R_{sub}$ and the parasitic NPN transistor $Q$ is activated creating a discharge path.
- If the pulse is negative, $D_{bulk}$ is forward biased and conducts the current.

To design the ggnMOS effectively, several considerations must be taken into account:

- A multifinger approach for the nMOS allows better current distribution, making it more robust.
- Because of their structure, high-voltage nMOS present a different parasitic configuration which makes them unsuitable for use as ESD protections.
- The drain-source breakdown voltage which activates the ESD protection function must be higher than the maximum nominal input voltage, but low enough that it activates before the following circuits are damaged by the ESD pulse.
- To reach the desired breakdown voltage, several nMOS transistors can be stacked in series. The total breakdown voltage will be the sum of their individual ones.
- Short-circuit connection between gate and source is best avoided. It is preferable to use a low value resistor.

### 3.1.2 Voltage divider

The simplest way to reduce the magnitude of a voltage range is to use a voltage divider, a circuit whose output voltage is a fixed fraction of the input voltage.
The general idea is to use a series of two passive elements (figure 3.3).

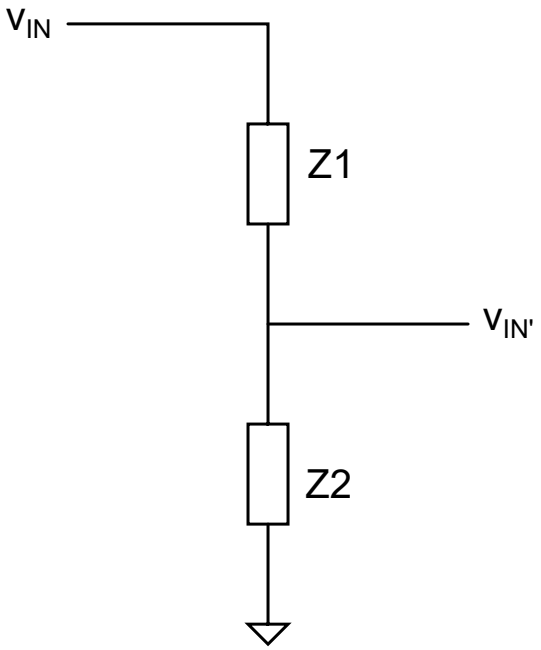


Figure 3.3. Voltage divider

A portion of the input voltage $v_{IN}$ will drop on the first passive element $Z1$, while the rest will drop on the second element $Z2$. The magnitude of the output $v_{IN'}$ will depend on the input and the ratio of the impedance values according to the law:

$$v_{IN'} = v_{IN} \frac{Z2}{Z1 + Z2} \tag{3.1}$$

For a resistive divider, for example, equation 3.1 becomes:

$$v_{IN'} = v_{IN} \frac{R2}{R1 + R2} \tag{3.2}$$

The output node $v_{IN'}$, however, is not floating: in this particular application it will be connected to one of the comparator's inputs, which can be considered a capacitive load $C_{in}$ (where $C_{in}$ is the total parasitic capacitance of the input node towards ground). The resulting circuit is a low-pass RC filter (figure 3.4).

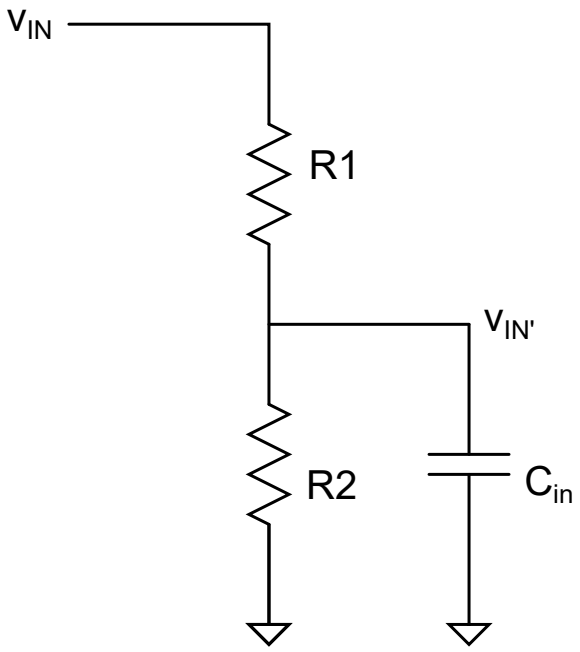


Figure 3.4. Resistive divider with capacitive load

The cut-off frequency $f_C$ for the low-pass circuit is:

$$f_C = \frac{1}{2\pi(R1\backslash\backslash R2)C_{in}} \tag{3.3}$$

The value of $C_{in}$ depends on how the MOSFETs in the comparator are sized. It will be shown in section 3.2 that this value is around 20 fF.
To ensure that the maximum value of $v_{IN}$ (10 V) corresponds to a maximum value $v_{IN'} = V_{DD}$ (3 V), the ratio of $R1$ and $R2$ is defined by:

$$\frac{v_{IN'}}{v_{IN}} = \frac{1}{R1/R2+1} \rightarrow \frac{R1}{R2} = \frac{v_{IN}}{v_{IN'}} - 1 = \frac{10}{3} - 1 = \frac{7}{3} \tag{3.4}$$

$R1$ and $R2$ are implemented with high-ohmic poly resistors with sheet resistance equal to 6 $k\Omega/\square$. Since the input pulse has a duration of 1 ns, its fundamental frequency in the spectral domain, $f_0$, will correspond to 1 GHz. To respect Nyquist theorem $f_C > 2f_0$, so:

$$R1\backslash\backslash R2 = \frac{R1R2}{R1+R2} < \frac{1}{2\pi 2 f_0 C_{in}} = 4k\Omega \tag{3.5}$$

And, substituting $R1$=$7/3R2$ into equation 3.5:

$$R2 < \frac{10}{7} 4k\Omega = 5.7k\Omega \tag{3.6}$$

Which gives:

$$R1 = \frac{7}{3} R2 = 13.3k\Omega \tag{3.7}$$

An AC simulation was performed in ADE L on the circuit thus dimensioned, using an ideal voltage generator and plotting the dB20 attenuation between output $v_{IN'}$ and input $v_{IN}$ as a function of frequency (figure 3.5).

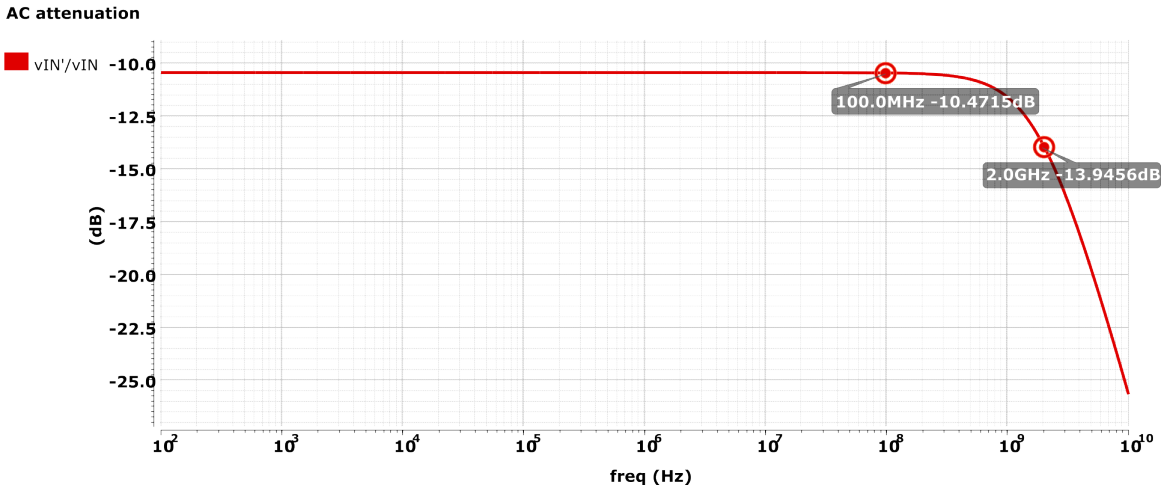


Figure 3.5. Voltage attenuation of the loaded resistive divider as a function of frequency

As expected, the circuit exhibits the typical low-pass response. The low frequency attenuation is -10.47 dB (3/10 linear) showing that the divider ratio is correct. At $f_C = 2f_0$ =2 GHz the attenuation is equal to -13.94 dB, about 3 dB less than the low frequency attenuation, showing that the resistors were sized correctly.
A transient simulation was then performed to show the time-domain behaviour of $v_{IN}$ and $v_{IN'}$ (figure 3.6).

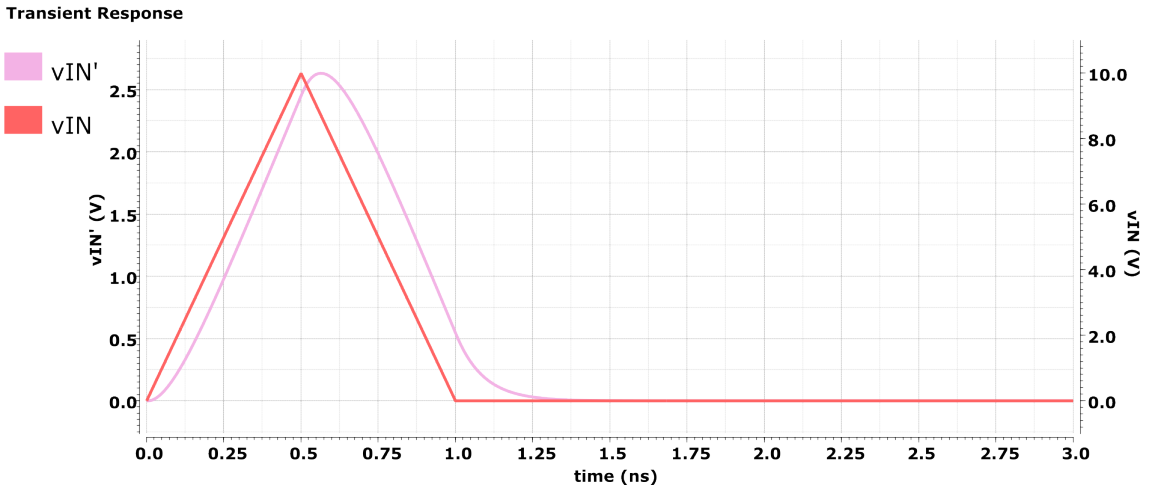


Figure 3.6. Input and output of the loaded resistive divider as a function of time

At 1 GHz, some unwanted attenuation is already introduced, together with a non-negligible time delay. Resizing the resistive divider is possible, but there is another option that removes the problem of the creation of the RC low-pass filter altogether: a ***capacitive divider*** (figure 3.7).

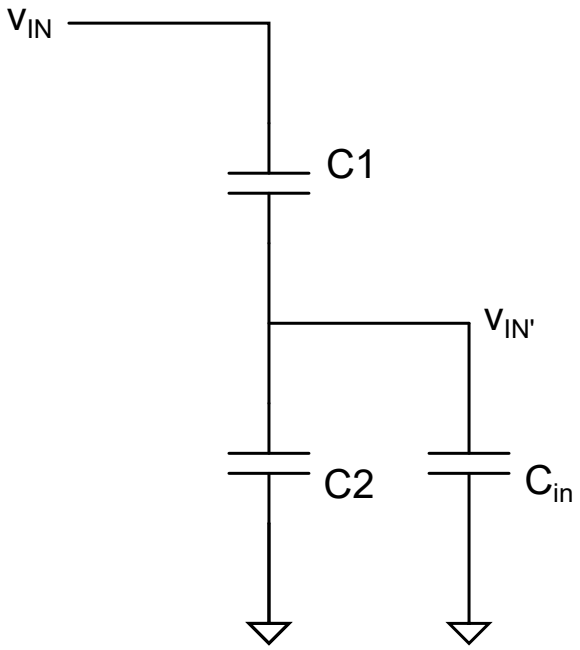


Figure 3.7. Capacitive divider with capacitive load

Since the impedance for capacitors is:

$$Z_C = \frac{1}{sC} \tag{3.8}$$

Where $s = j\omega = j2\pi f$, equation 3.1 becomes:

$$v_{IN'} = v_{IN}\frac{C1}{C1 + C2} \tag{3.9}$$

As long as the input capacitance of the comparator $C_{in}$ is negligible with respect to $C1$ and $C2$.
Capacitive dividers, however, filter the DC component of the input signal and only attenuate its AC voltage. This means that the node $v_{IN'}$ requires DC voltage biasing.
The simplest way to bias a node is to connect it to a constant voltage source, either directly or through a resistive divider. The available sources are $V_{DD}$ and $V_{REF}$.
$V_{REF}$ is provided by a bandgap circuit, making it stable with respect to supply and temperature changes. Moreover, by connecting the bias network to $V_{REF}$, no power is absorbed from the supply $V_{DD}$.

### 3.1.3 Input bias and conditioning

The resulting circuit is a capacitive AC voltage divider with resistive bias network (figure 3.8).

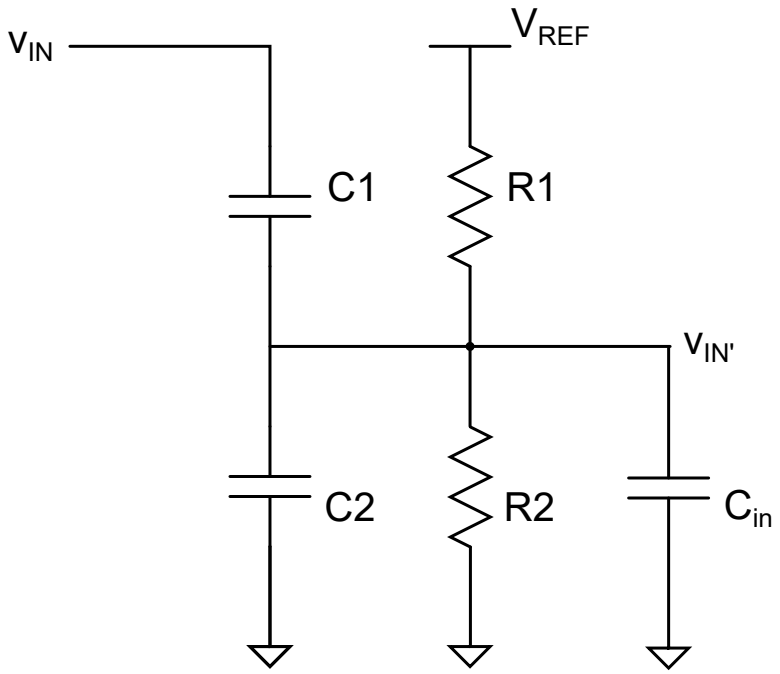


Figure 3.8. Capacitive divider with resistive bias network and capacitive load

$R1$ and $R2$ are implemented with high-ohmic poly resistors with sheet resistance equal to 6 $k\Omega/\square$. $C1$ and $C2$ are implemented with MIM capacitors with area capacitance 2 $fF/\mu m^2$.
In order to properly bias the ***input node*** $v_{IN'}$, the other input to the comparator (the ***reference node***) must be taken into account. Section 1.1 mentioned that the comparator's delay $t_D$ is inversely proportional to the differential input voltage. The idea is then to bias the input node as close to the reference node as possible.
A direct connection to the reference voltage $V_{REF}$ would be the most straightforward approach for the reference node, but if the input node's bias voltage is scaled down from $V_{REF}$ this would end up slowing down the comparator.
A possible solution is to scale down the reference input as well. Since this node does not present AC voltage swings (unlike $v_{IN'}$), a more sophisticated approach with respect to the resistive divider is possible: the ***CMOS voltage divider*** proposed by Danilov et al. [2021] (figure 3.9).

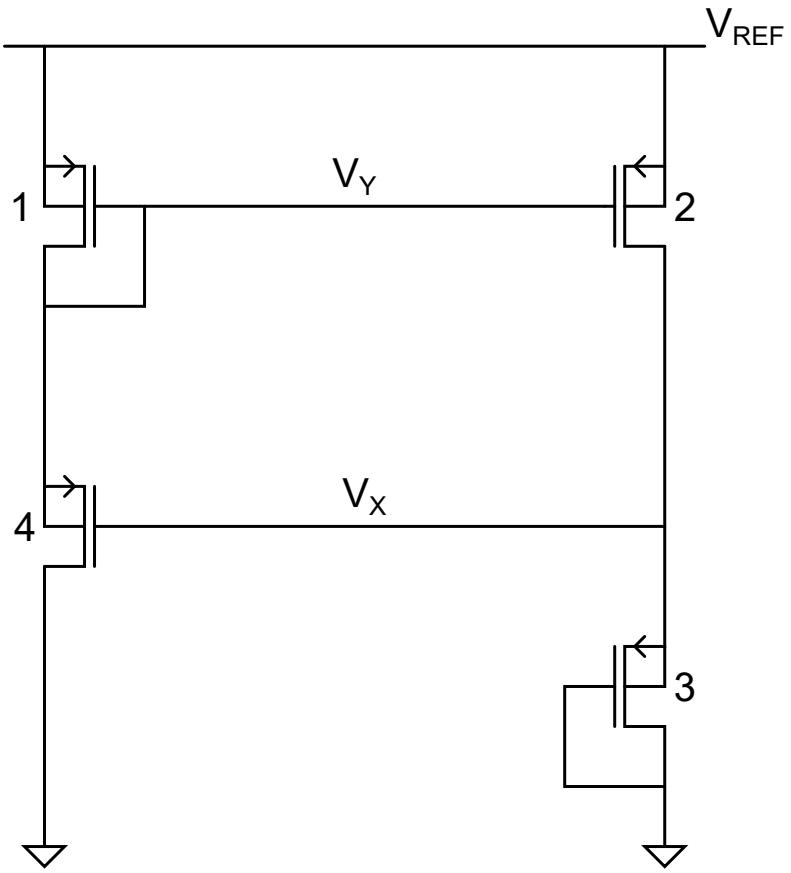


Figure 3.9. CMOS divider

This circuit requires the use of isolated pMOS devices so that their bulk and source terminals can be shorted together to avoid body effect, which would disrupt nominal operation. These devices are available in the technological process being employed and present a threshold voltage $|V_{THp}|$ of about 0.6 V.
The idea behind this topology is to provide two voltage levels, $V_Y$ and $V_X$, that are constant fractions of the supply voltage (in this case, $V_{REF}$=1.242 V) irrespectively of any temperature changes.
The circuit works for both saturation and sub-threshold operation. Let's assume that the current through M1 equals the one through M4 and the current through M2 equals the one through M3.
If the devices work in saturation:

$$\begin{cases} \frac{W2}{L2}\frac{K'_p}{2}(V_{REF} - V_Y - |V_{THp2}|)^2 = \frac{W3}{L3}\frac{K'_p}{2}(V_X - |V_{THp3}|)^2 \\ \frac{W1}{L1}\frac{K'_p}{2}(V_{REF} - V_Y - |V_{THp1}|)^2 = \frac{W4}{L4}\frac{K'_p}{2}(V_Y - V_X - |V_{THp4}|)^2 \end{cases} \tag{3.10}$$

And if the devices work in sub-threshold:

$$\begin{cases} \frac{W2}{L2} I' exp\left(\frac{V_{REF} - V_Y - |V_{THp2}|}{nKT}\right) = \frac{W3}{L3} I' exp\left(\frac{V_X - |V_{THp3}|}{nKT}\right) \\ \frac{W1}{L1} I' exp\left(\frac{V_{REF} - V_Y - |V_{THp1}|}{nKT}\right) = \frac{W4}{L4} I' exp\left(\frac{V_Y - V_X - |V_{THp4}|}{nKT}\right) \end{cases} \tag{3.11}$$

Assuming that all the pMOS have equal size and threshold voltage $|V_{THp}|$, both systems of equations can be solved as:

$$V_X = \frac{V_{REF}}{3} + \frac{-|V_{THp1}| + 2|V_{THp2}| - 2|V_{THp3}| + |V_{THp4}|}{3} \approx \frac{V_{REF}}{3} = 414mV \tag{3.12}$$

$$V_Y = \frac{2V_{REF}}{3} + \frac{|V_{THp1}| + |V_{THp2}| - |V_{THp3}| - |V_{THp4}|}{3} \approx \frac{2V_{REF}}{3} = 828mV \tag{3.13}$$

Confirming that the voltages at nodes $X$ and $Y$ depend only on $V_{REF}$ and not on any parameters that change with temperature (such as threshold voltage $V_{THp}$).
To understand the region of operation of the circuit let's first check the value of $V_{SG}$ for each pMOS:

$$V_{SG1} = V_{SG2} = V_{REF} - V_Y = 414mV < |V_{THp}| \tag{3.14}$$

$$V_{SG3} = V_X = 414mV < |V_{THp}| \tag{3.15}$$

$$V_{SG4} = V_Y - V_X = 414mV < |V_{THp}| \tag{3.16}$$

This analysis is sufficient to show that the circuit works in sub-threshold, which implies minimal current consumption from the reference circuit.
The circuit was sized for minimum area with $W = L_{min}$=300 nm and simulated with an ideal voltage generator $V_{REF}$=1.242 V in the time domain with parametric temperature in the range [-40, 125] °C (figure 3.10).

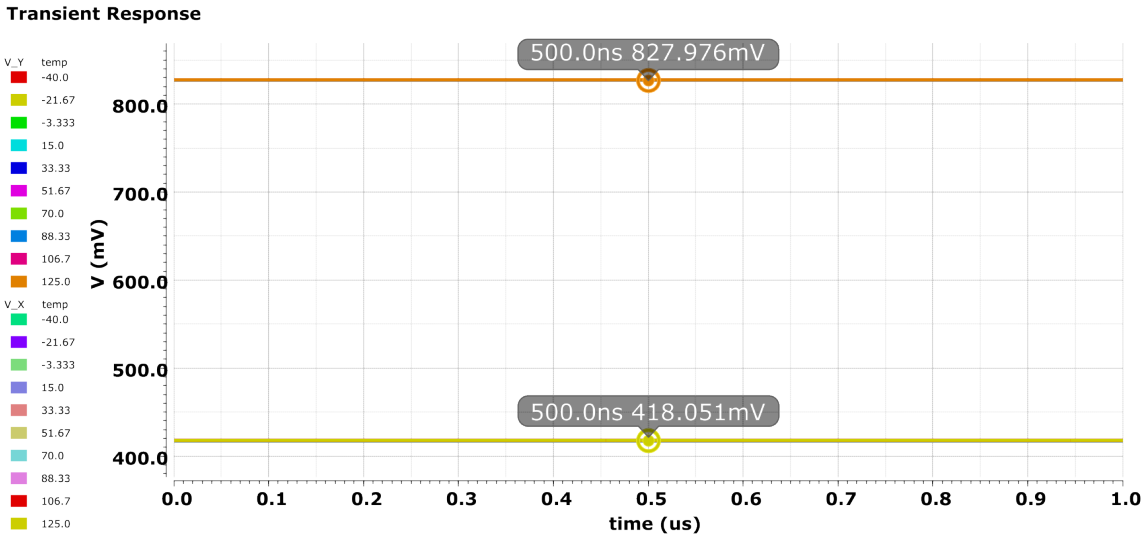


Figure 3.10. $V_X$ and $V_Y$ as a function of time with parametric temperature

The simulation results show that the voltage at the nodes $V_X$ and $V_Y$ is stable irrespectively of time and temperature.
Current absorption from $V_{REF}$ as a function of time with parametric temperature was also simulated (figure 3.11).

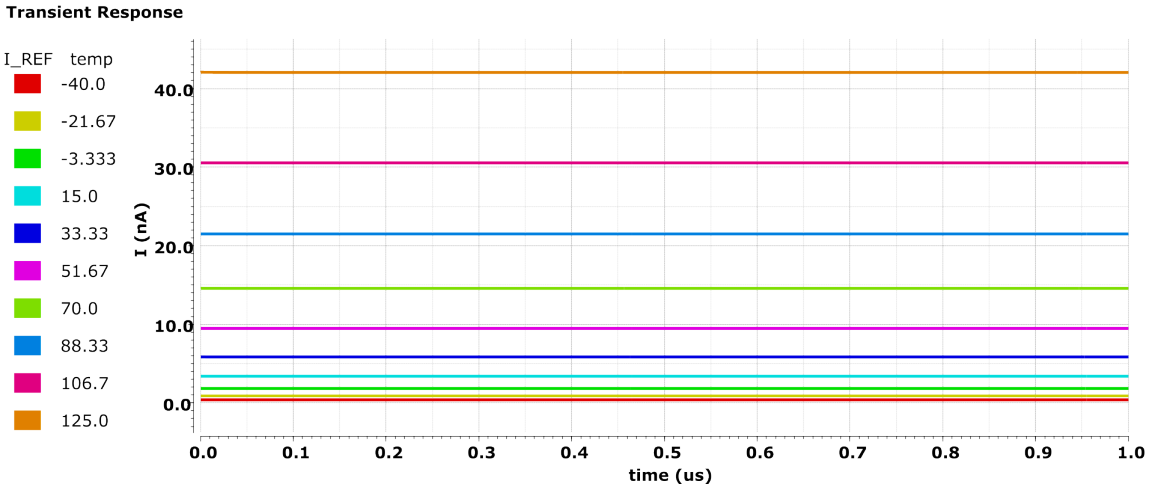


Figure 3.11. $I_{REF}$ as a function of time with parametric temperature

Confirming sub-threshold operation with a maximum current absorption of about 40 nA for T=125 °C.

Let's call the bias voltage for the reference node $V_{REF'}$. If a voltage divider is employed for the input node, the options for $V_{REF'}$ are $V_X = V_{REF}/3$=414 mV or $V_Y = 2V_{REF}/3$=828 mV. Now, let's call the bias voltage for the input node $V_{IN'}$ and set its two possible values at 400 mV and 800 mV, respectively, so they are close to the corresponding reference value. According to the superposition principle:

$$v_{IN'} = v_{in'} + V_{IN'} \tag{3.17}$$

Where:

$$v_{in'} = v_{in}\frac{C1}{C1 + C2} \tag{3.18}$$

represents the AC component and:

$$V_{IN'} = V_{REF}\frac{R2}{R1 + R2} \tag{3.19}$$

represents the DC bias.
For $V_{IN'}$=400 mV:

$$\frac{R1}{R2} = 2.1 \tag{3.20}$$

While for $V_{IN'}$=800 mV:

$$\frac{R1}{R2} = 0.55 \tag{3.21}$$

To limit current absorption from $V_{REF}$ let's set a maximum $I_{REF}$ equal to 10 $\mu A$:

$$I_{REF} = \frac{V_{REF}}{R1 + R2} < 10\mu A \rightarrow R1 + R2 = \frac{V_{REF}}{I_{REF}} > 124.2k\Omega \tag{3.22}$$

Let's pick $R2$=100 kΩ, then $R1$=210 kΩ for $V_{IN'}$=400 mV and $R1$=55 kΩ for $V_{IN'}$=800 mV.
To ensure safe operation with maximum differential voltage:

$$v_{IN'} = v_{in'} + V_{IN'} = V_{DD} = 3V|_{v_{IN}=10V} \tag{3.23}$$

Substituting equation 3.18 into equation 3.23, the result for $V_{IN'}$=400 mV is:

$$\frac{C2}{C1} = 2.85 \tag{3.24}$$

While the result for $V_{IN'}$=400 mV is:

$$\frac{C2}{C1} = 3.54 \tag{3.25}$$

Keeping in mind that $C1$ and $C2$ need to be much larger than $C_{in}$=20 fF so that the load is negligible, let's pick $C1$=200 fF, then $C2$=570 fF for $V_{IN'}$=400 mV and $C2$=708 fF for $V_{IN'}$=800 mV.
The input circuit was simulated with ideal voltage generators in the time domain, sized for both $V_{IN'}$=400 mV (figure 3.12) and $V_{IN'}$=800 mV (figure 3.13).

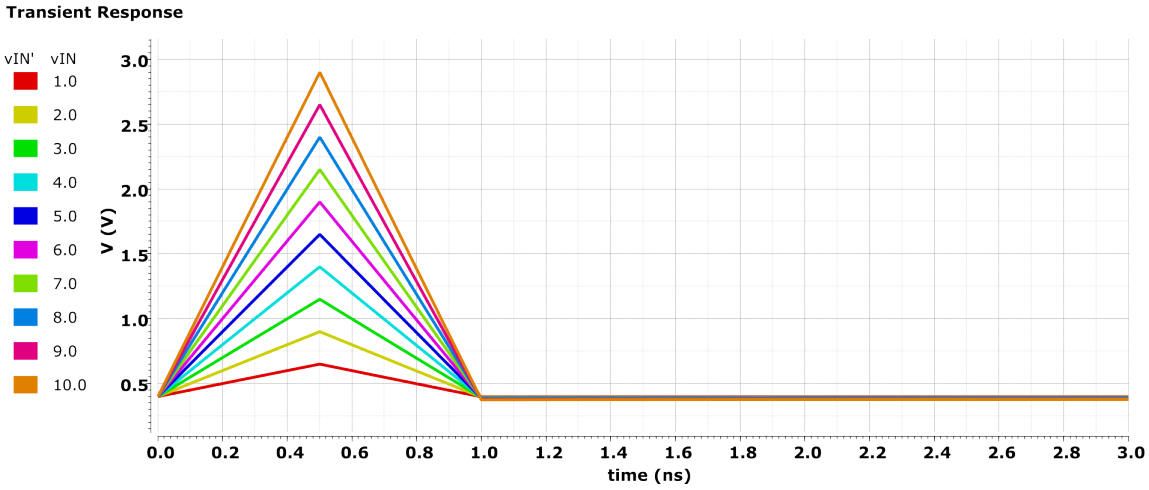


Figure 3.12. $v_{IN'}$ as a function of time with bias $V_{IN'}$=400 mV and parametric $v_{IN}$

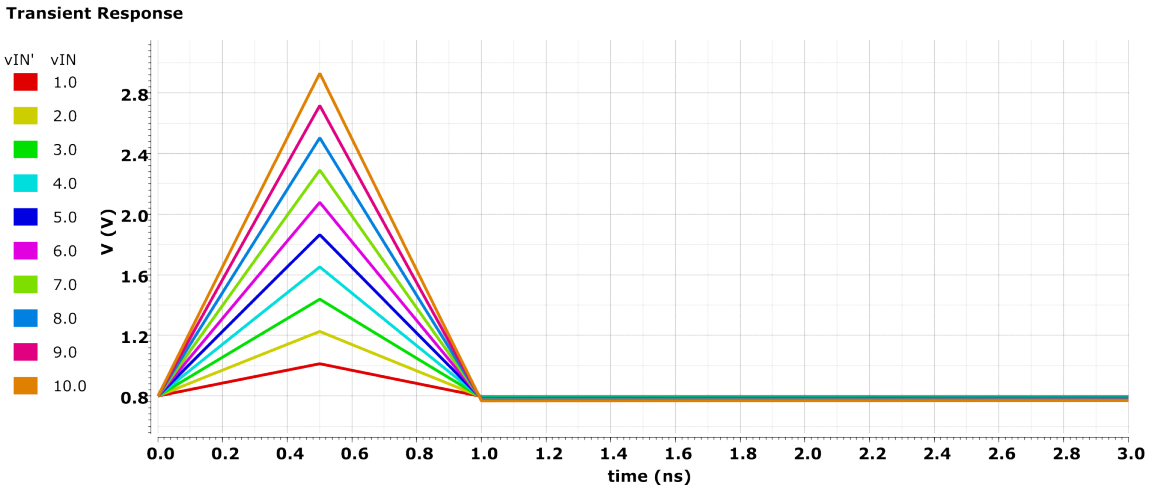


Figure 3.13. $v_{IN'}$ as a function of time with bias $V_{IN'}$=800 mV and parametric $v_{IN}$

AC voltage division and DC bias are confirmed to be consistent with the calculations. The minimum resolution $v_{MIN}$ for $V_{IN'}$=400 mV is about 250 mV and for $V_{IN'}$=800 mV it is about 200 mV.
Current absorption from $V_{REF}$ as a function of time was also simulated for both $V_{IN'}$=400 mV (figure 3.14) and $V_{IN'}$=800 mV (figure 3.15).

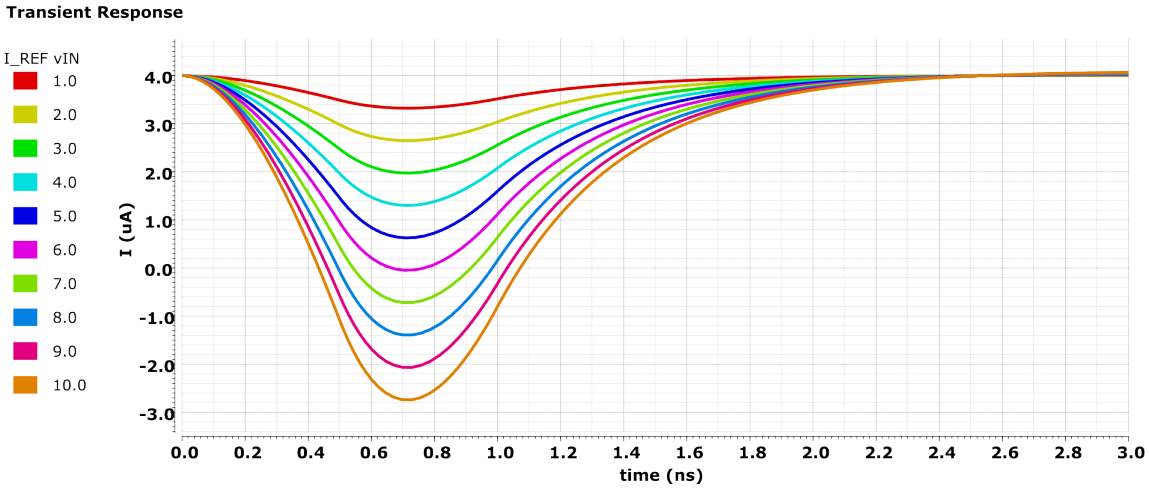


Figure 3.14. $I_{REF}$ as a function of time with bias $V_{IN'}$=400 mV and parametric $v_{IN}$

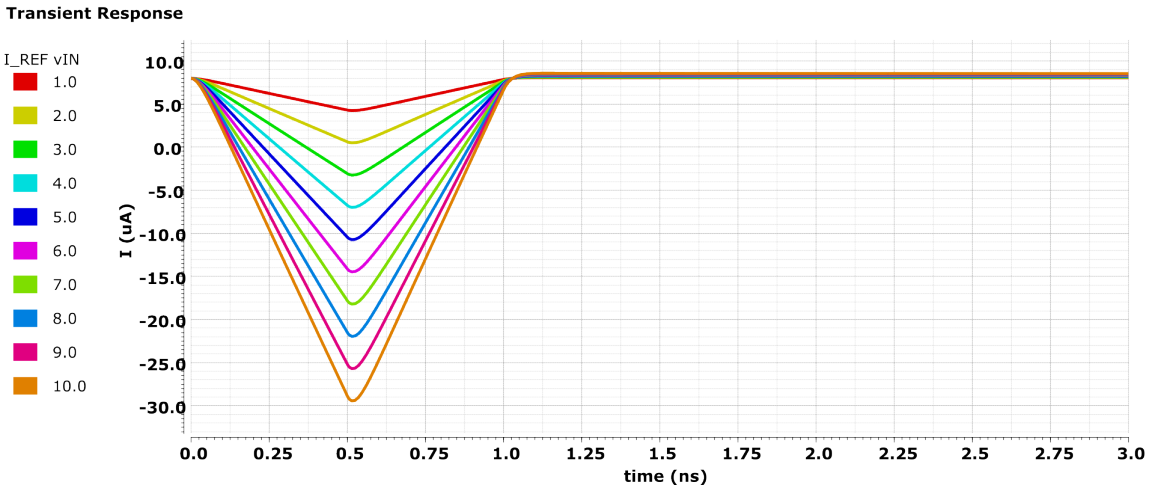


Figure 3.15. $I_{REF}$ as a function of time with bias $V_{IN'}$=800 mV and parametric $v_{IN}$

Current absorption from $V_{REF}$ is below 10 $\mu$A as predicted.

## 3.2 Comparator

The comparator itself consists of a ***self-biased single-ended preamplifier*** (figure 3.16) and a simple ***inverter*** as decision stage (figure 3.17).

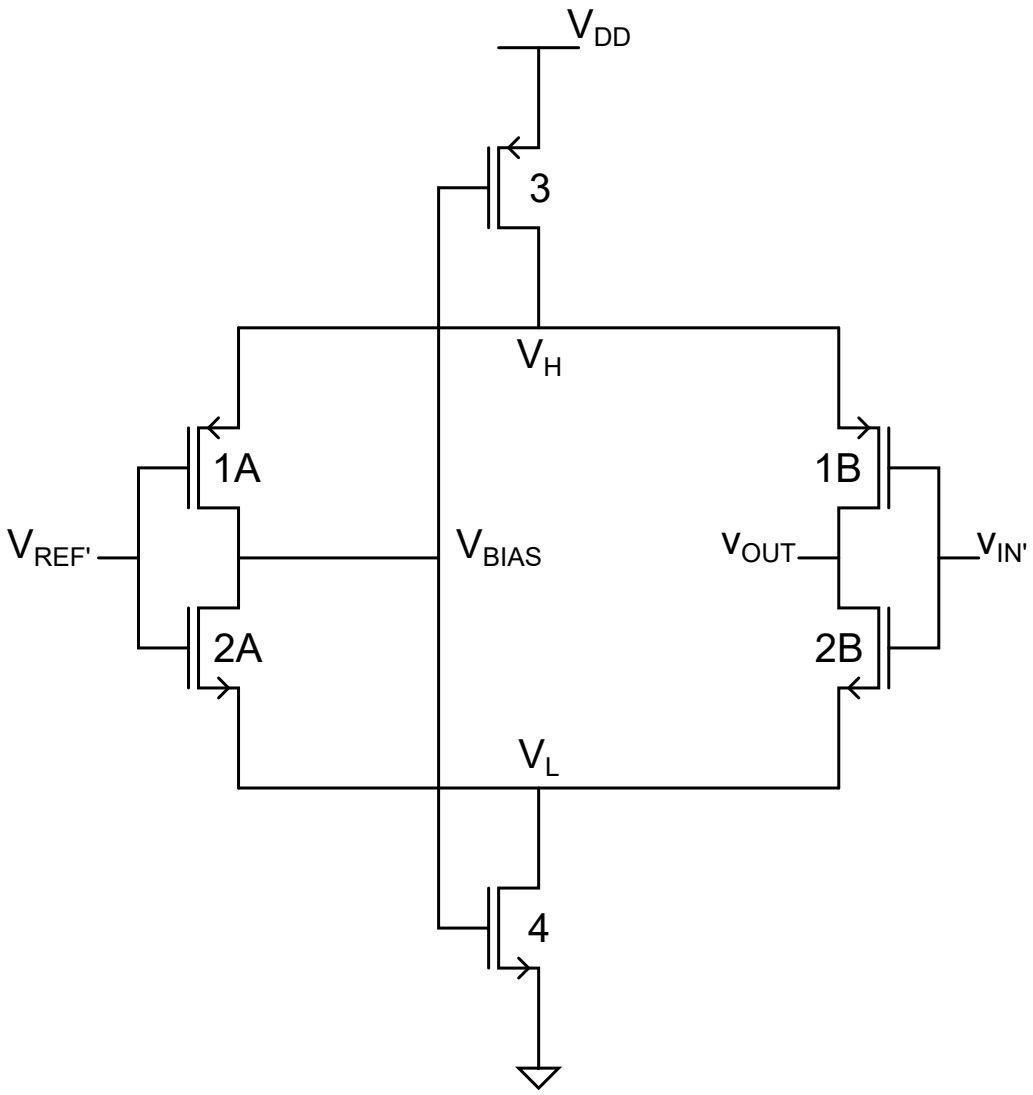


Figure 3.16. Comparator preamplifier

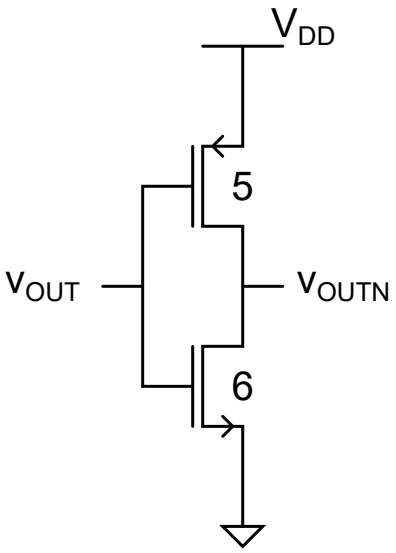


Figure 3.17. Comparator decision stage

To ensure maximum speed $L = L_{min}$ was chosen for each MOSFET. This corresponds to $L_{min}$=300 nm for pMOS and $L_{min}$=350 nm for nMOS.
Since the inverter is followed by an output stage with small input capacitance, it was sized for minimum area occupation with $W5/L5{=}W6/L6{=}1$, without concern for slew rate. To size the preamplifier the ***trip-point*** and ***input capacitance*** of the inverter must be calculated.
The trip-point for the inverter is defined as:

$$V_{TP} = \frac{\sqrt{\beta_n/\beta_p}V_{THn} + V_{DD} - |V_{THp}|}{1 + \sqrt{\beta_n/\beta_p}} \tag{3.26}$$

Where:

$$\beta = K'\frac{W}{L} \tag{3.27}$$

Substituting the values from subsection 2.2.2, $V_{TP}$ should be around 1.25 V.
A DC simulation was performed on the circuit to check this value, obtaining the result in figure 3.18.

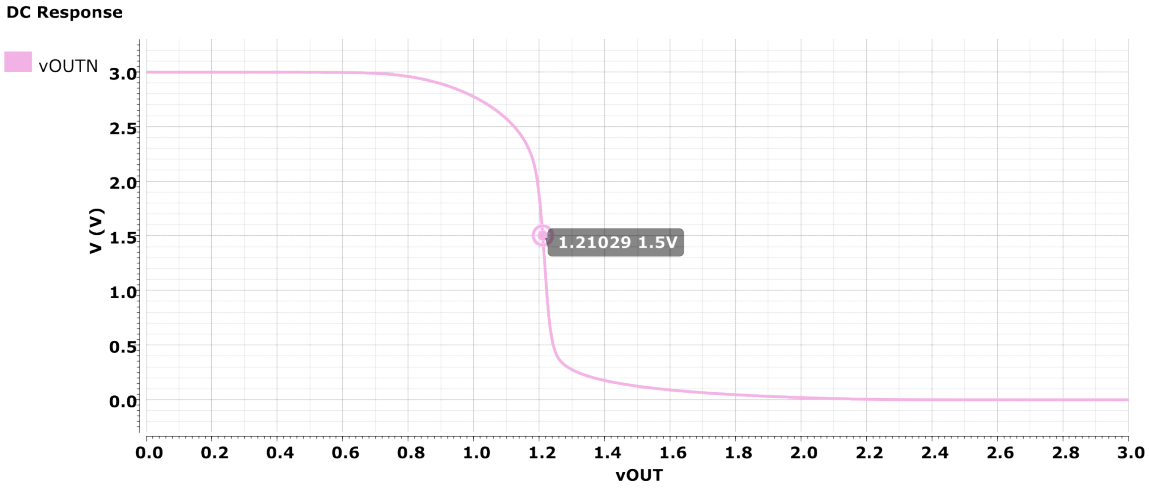


Figure 3.18. $v_{OUTN}$ as a function of $v_{OUT}$

The actual trip-point for the inverter was computed as the input value $v_{OUT}$ corresponding to a 50% variation of the output $v_{OUTN}$ and is equal to 1.21 V. The minimum input swing to ensure that $v_{OUTN}$ goes to zero is about 2 V.
To calculate the input capacitance of the inverter, let's start from the voltage across a capacitor as a function of time, described by the law:

$$V(t) = V(t_0) + \frac{1}{C}\int_{t_0}^{t} I(\tau)d\tau \tag{3.28}$$

Then, let's apply a voltage ramp of amplitude 3 V and duration 500 ps to the input of the inverter ($v_{OUT}$) and plot the input current as a function of time, $I_{in}(t)$ (figure 3.19). The value of $C_{in}$ is the integral of $I_{in}(t)$ divided by the maximum amplitude of the ramp (3 V) and corresponds to 1.4 fF. This represents the load to the preamplifier.

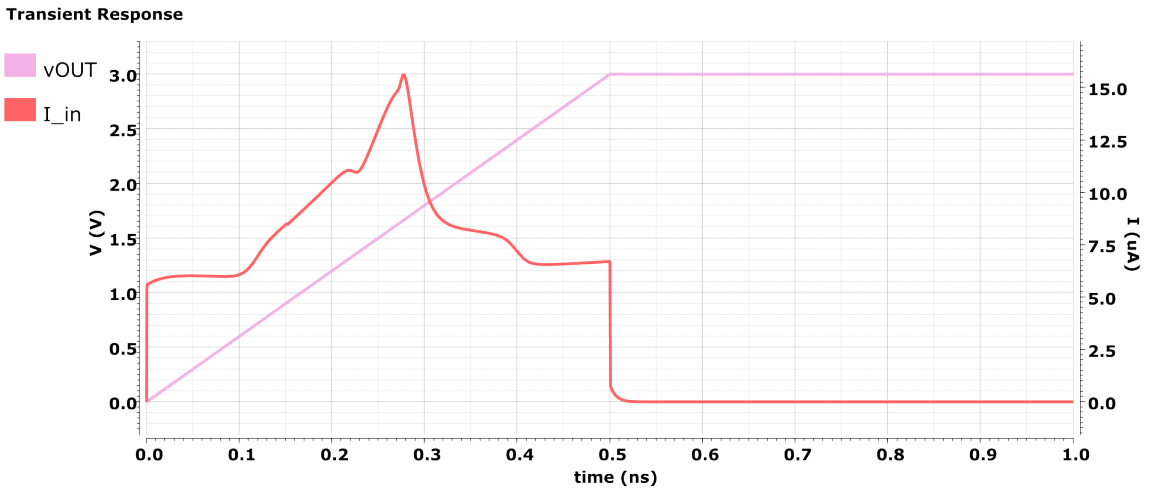


Figure 3.19. Input current as a function of time in response to a voltage ramp (inverter)

To size the preamplifier let's revisit its differential gain:

$$A_v = \frac{V_{OH} - V_{OL}}{v_{MIN}} = \frac{g_{m1} + g_{m2}}{g_{out}} \tag{3.29}$$

Where (assuming the MOSFETs operate in saturation):

$$g_m = \sqrt{\frac{2K' i_D W}{L}} \tag{3.30}$$

is the transconductance $\delta i_d / \delta v_{gs}$ and:

$$g_o = i_D \lambda \tag{3.31}$$

is the output conductance $\delta i_d / \delta v_{ds}$.
$V_{OH} - V_{OL}$ is the output swing necessary for the following stage (the inverter) to completely switch state and corresponds to about 2 V.
The minimum resolution $v_{MIN}$ was computed in subsection 3.1.3 and corresponds to 250 mV for $V_{IN'}$=400 mV and to 200 mV for $V_{IN'}$=800 mV. Let's use the latter as worst-case scenario to calculate $A_v$ as 10.
Another important parameter is the slew rate, determined by M3 and M4. Since they operate in the triode region the equation for their drain/source current is:

$$i_D = K' \frac{W}{L} \left[ (v_{GS} - V_{TH}) - \frac{v_{DS}}{2} \right] v_{DS} \tag{3.32}$$

And since the rising and falling times of the input triangular pulse are equal to 500 ps, let's set 100 ps as switching time $dt$ so that the slew rate $dV/dt$ (where $dV = V_{OH} - V_{OL}$) is equal to 20 GV/s.

To further speed up the preamplifier, Bazes [1991] suggests the insertion of a ***filter capacitor*** between node $V_H$ and GND. This provides additional charge during the switching transient (rising edge) at the output. For the implementation of this capacitor, Shen et al. [2006] offer an interesting insight. MOSFET based capacitors (figure 3.20) can be implemented by simply shorting together drain and source nodes and provide much better capacitance density with respect to MIM capacitors. The main disadvantage is that their capacitance depends on the voltage applied to their terminals.

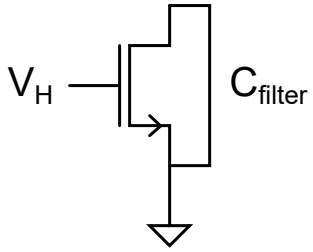


Figure 3.20. nMOS capacitor

In strong inversion:

$$v_{GS} = V_H > V_{THn} + 2n_n V_T \tag{3.33}$$

Where $n_n$ represents the subthreshold swing factor and $V_T$ is the thermal voltage $KT/q$. $C_{filter}$ corresponds to:

$$C_{max} = WLC_{ox} \tag{3.34}$$

Where $W$ is the channel width, $L$ the channel length and $C_{ox}$ the gate oxide capacitance. For the available process it corresponds to 5 fF/$\mu m^2$, against the 2 fF/$\mu m^2$ of the available MIM capacitors.
Since $V_H$ is close to the supply rail voltage $V_{DD}$, it is safe to assume that the nMOS will operate in strong inversion, thus $C_{filter}$=$C_{max}$.
To implement a 1 pF MIM capacitor $C_{filter}$, the required size is W=20 $\mu$m by L=25 $\mu$m. To implement the same capacitor with a nMOS, W=L=15 $\mu$m is sufficient.
Finally, since the input is connected to a push-pull (inverter) amplifier (M1B, M2B) it is possible to change its trip point $V_{TP}$ by making the inverter asymmetrical. To decrease $V_{TP}$, the aspect ratio for the nMOS M2B needs to be larger than the one for the pMOS M1B. To increase $V_{TP}$, the opposite line of reasoning holds true. The input signal $v_{IN}$ and its conditioned version $v_{IN'}$ are positive triangular impulses, so to optimise the preamplifier reaction (and, consequently, its speed) reducing $V_{TP}$ is a viable option.
The final sizing for the preamplifier's MOSFETs is the following:

- $\frac{W1A}{L1A} = \frac{W2A}{L2A} = 10$
- $\frac{W1B}{L1B} = 10$, $\frac{W2B}{L2B} = 20$
- $\frac{W3}{L3} = \frac{W4}{L4} = 10$

The input capacitance of the preamplifier was calculated with the same approach used for the inverter and corresponds to about 20 fF (figure 3.21).

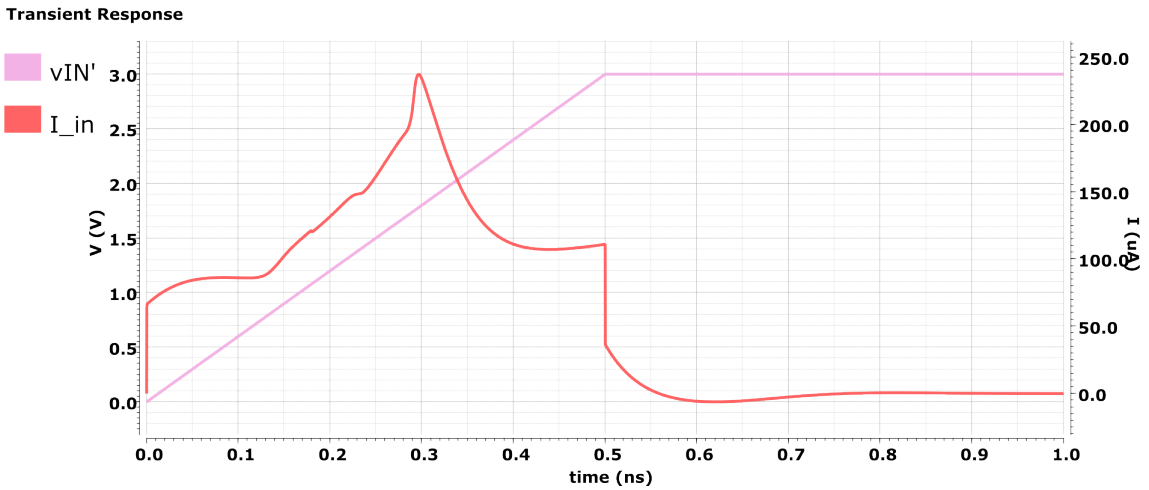


Figure 3.21. Input current as a function of time in response to a voltage ramp (preamplifier)

To examine the ***CMIR*** of the preamplifier, a DC simulation was performed with $v_{OUT}$ as a function of $v_{IN'}$ and parametric $V_{REF'}$ (figure 3.22).

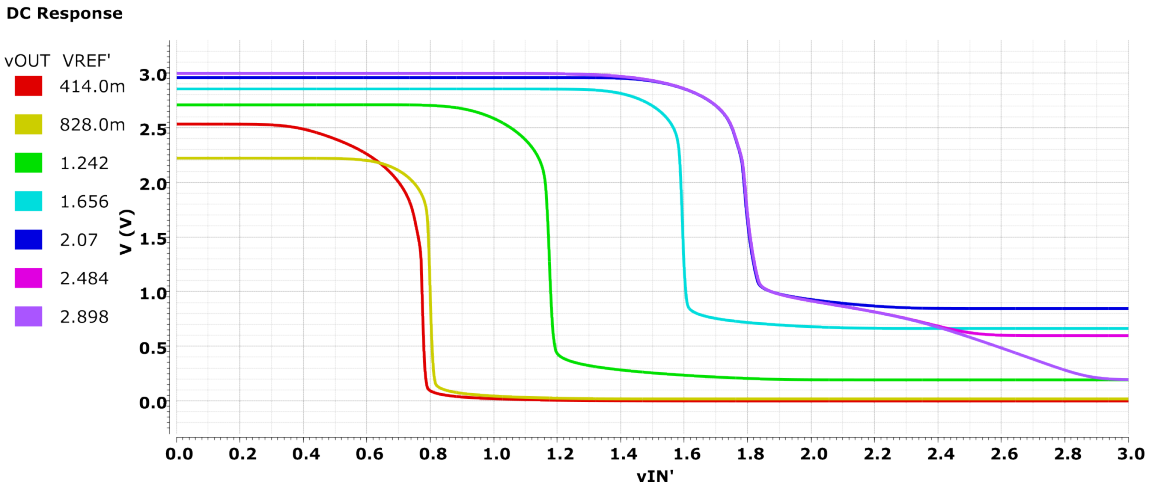


Figure 3.22. $v_{OUT}$ as a function of $v_{IN'}$ with parametric $V_{REF'}$ (preamplifier)

The CMIR for the preamplifier varies between about 800 mV and 2 V. Beyond this range the preamplifier still works as a push-pull inverter, but not as efficiently. Out of the bias options for the inputs, only $V_{REF'}$=$V_{IN'}$=1.242 V and $V_{REF'}$=828 mV, $V_{IN'}$=800 mV are within range.
The latter was selected because it allows for lower current consumption, as demonstrated by the DC analysis of the quiescent supply current $I_{DD}$ absorbed by the comparator as a function of the bias voltage $V_{BIAS}$ applied to both its inputs (figure 3.23).

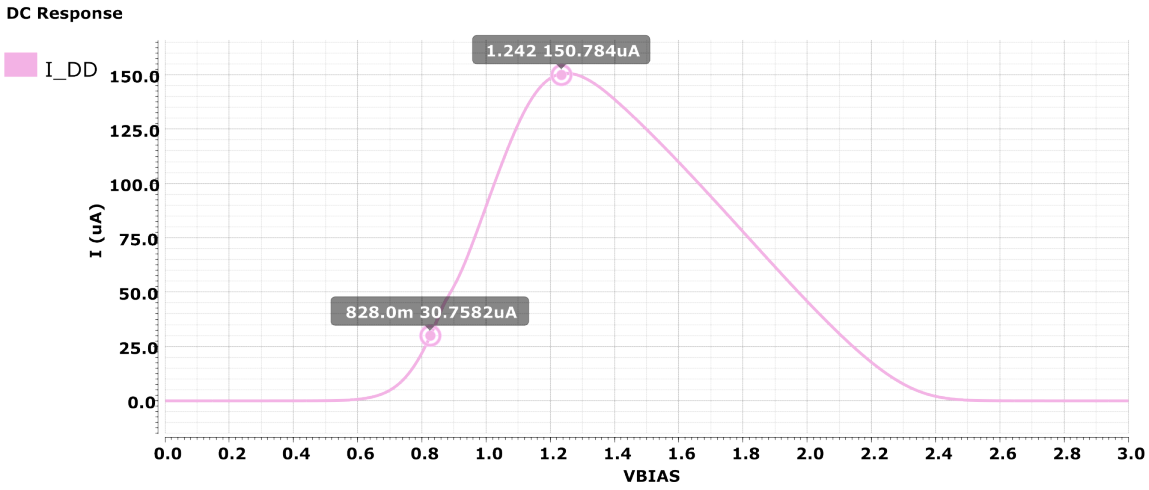


Figure 3.23. Quiescent supply current $I_{DD}$ as a function of $V_{BIAS}$

Note that in subsection 3.1.3, when describing the CMOS voltage divider, it was assumed that the voltage at its output nodes $V_X$ and $V_Y$ was stable because it would be connected to the node $V_{REF'}$ where no AC swings should be present. In practice, however, the voltage at node $V_{REF'}$ is not completely stable and this poses a risk of injecting current into the CMOS voltage divider, disrupting its nominal operation.
To solve this problem, a MIM capacitor $C_{ref'} = 100fF$ was inserted at node $V_{REF'}$ so that no current is injected into the divider and the bias voltage is actually stable regardless of time and temperature variations.

## 3.3 Output

The output block must provide a digital rail-to-rail signal and keep it stable for some time after the first pulse, irrespectively of variations at the input, so that no hysteresis is needed to prevent any successive ringing pulses from creating unwanted output transitions.
Bazes [1991] describes a family of topologies which present this exact characteristic behaviour: ***monostable*** (or one-shot) circuits.
The proposed example (figure 3.24) should react to a pulse at the input $v_{OUTN}$ with a rectangular pulse of duration $\approx 0.7RC$ at the output $v_{OUT'}$. Pulse duration can be set by sizing $R$ and $C$ appropriately.

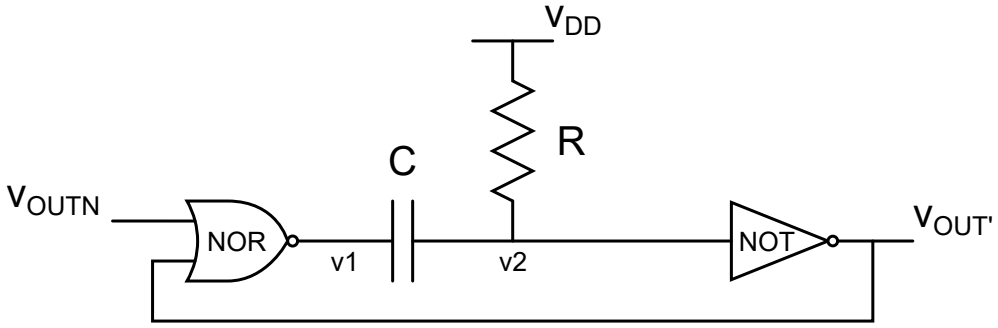


Figure 3.24. Monostable logic scheme

Bazes [1991]

Initially, both inputs to the NOR gate ($v_{OUTN}, v_{OUT'}$) are low. The output of the NOR gate ($v1$) is high. $v2$ is high due to the effect of the pull-up resistor $R$. When $v_{OUTN}$ rises above the NOR gate's trip point, $v1$ and $v2$ go low and the output of the NOT gate ($V_{OUT'}$) goes high. Capacitor $C$ is being charged through resistor R and after a time delay of about $0.7RC$ (assuming the inverter's trip point is $V_{DD}/2$), node $v2$ goes high again. The output of the NOT gate ($v_{OUT'}$) goes low. Until this moment, the output of the NOR gate ($v1$) stayed low irrespectively of the input $v_{OUTN}$, because the output of a NOR gate is high only when both its inputs are low (table 3.1).

| IN1 | IN2 | OUT |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

Table 3.1. NOR gate truth table

The CMOS implementation for a NOR gate described by Bazes [1991] (figure 3.25) requires four MOSFETs. They were sized with $W = L = L_{min}$ to minimise area, parasitic capacitance and maximise speed.

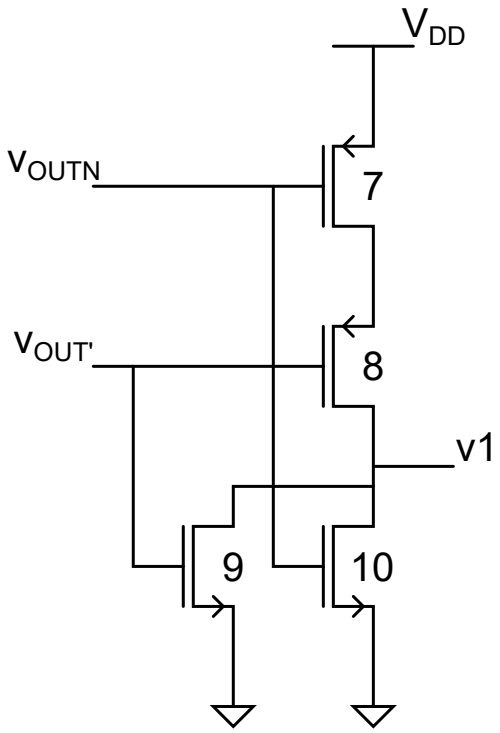


Figure 3.25. CMOS NOR gate

Bazes [1991]

The CMOS implementation for a NOT gate (figure 3.26) is a simple push-pull inverter with two MOSFETs. Since they need to drive the load $C_{load} = 100fF$ at high-speed, their channel length $L$ was set to $L_{min}$ and the aspect ratio $W/L$ was set to 10.

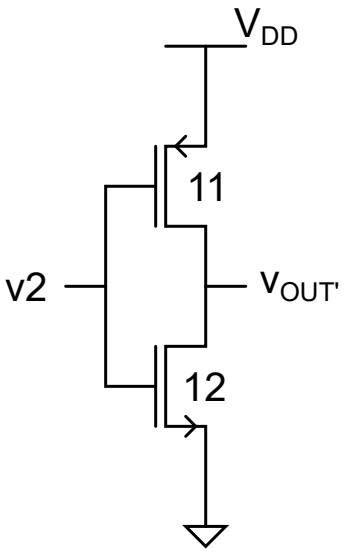


Figure 3.26. CMOS NOT gate (inverter)

The trip-point for this inverter was computed with a DC simulation of its output $v_{OUT'}$ as a function of its input $v2$ (figure 3.27).

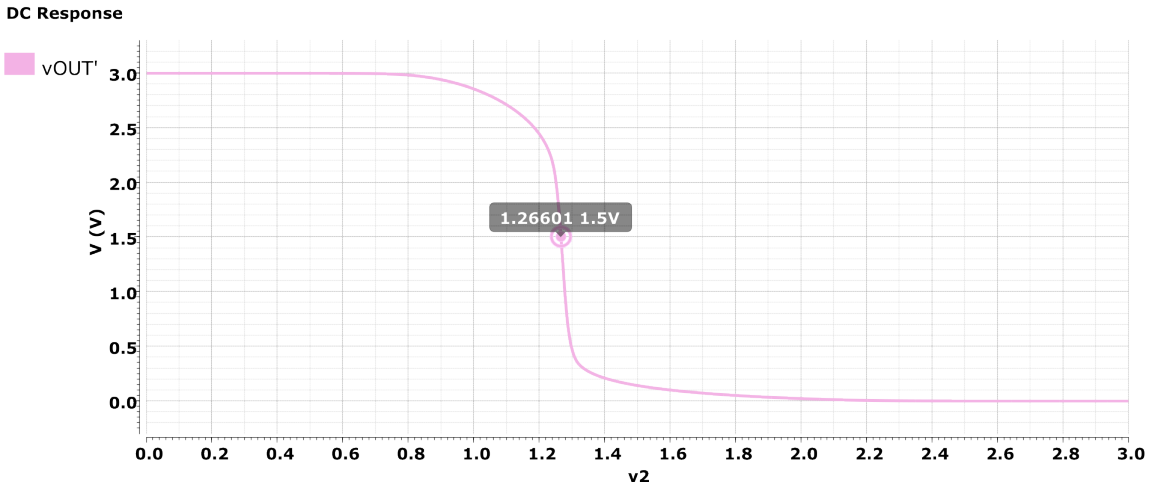


Figure 3.27. $v_{OUT'}$ as a function of $v2$

The actual trip-point for the inverter was computed as the input value $v2$ corresponding to a 50% variation of the output $v_{OUT'}$ and is equal to 1.27 V.

The voltage across capacitor $C$ as a function of time can be expressed as:

$$v_C(t) = v2(t) - v1(t) = V_{DD}(1 - e^{-t/RC}) \tag{3.35}$$

The time required to charge the capacitor to the trip-point of the inverter is:

$$t|_{v_C=V_{TP}} = RCln\frac{V_{DD}}{V_{DD} - V_{TP}} = 0.55RC \tag{3.36}$$

This is the actual amount of time during which the output of the monostable circuit $v_{OUT'}$ stays stable after the first pulse, irrespective of input variation.
To set it equal to 10 ns (ten times the duration of the first 1 ns pulse):

$$RC = \frac{t|_{v_C=V_{TP}}}{0.55} = 18.2ns \tag{3.37}$$

Let's pick $R = 100k\Omega$ so that $C = 182fF$. $R$ is implemented with a high-ohmic poly resistor with sheet resistance equal to 6 $k\Omega/\square$. $C$ is implemented with a MIM capacitors with area capacitance 2 $fF/\mu m^2$.
The circuit works as expected (figure 3.28).

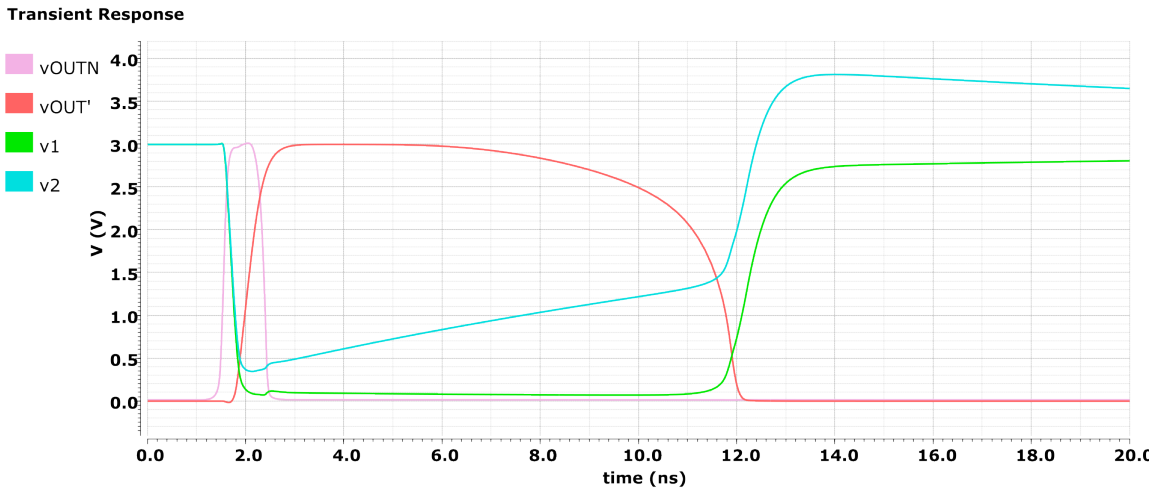


Figure 3.28. Monostable waveforms

Note that $v2$ temporarily exceeds the supply voltage $V_{DD}$ due to the action of the RC circuit. However, its peak value remains below 4 V, the maximum voltage tolerated by the employed MOSFETs.
This concludes the analysis of the design process. The simulation results will be presented in the next chapter.

# Chapter 4

# Simulation results

This chapter offers a brief review of the definitive circuit setup and presents the simulations that demonstrate its compliance with the specifications provided in chapter 2.

## 4.1 Schematic

The definitive block scheme is illustrated in figure 4.1.

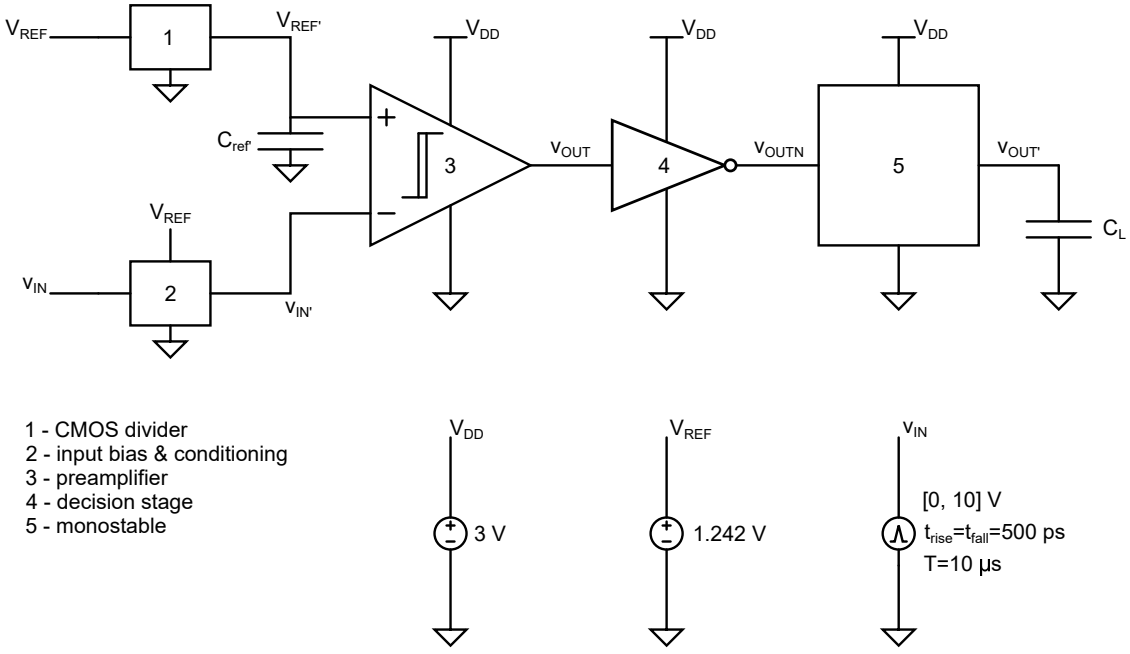


Figure 4.1. Block scheme

The constituting blocks are:

- CMOS divider (figure 4.2)
- Input bias and conditioning (figure 4.3)
- Self-biased push-pull preamplifier with CMOS filter capacitor (figure 4.4)
- Decision stage (inverter) (figure 4.5)
- Monostable (figure 4.6)

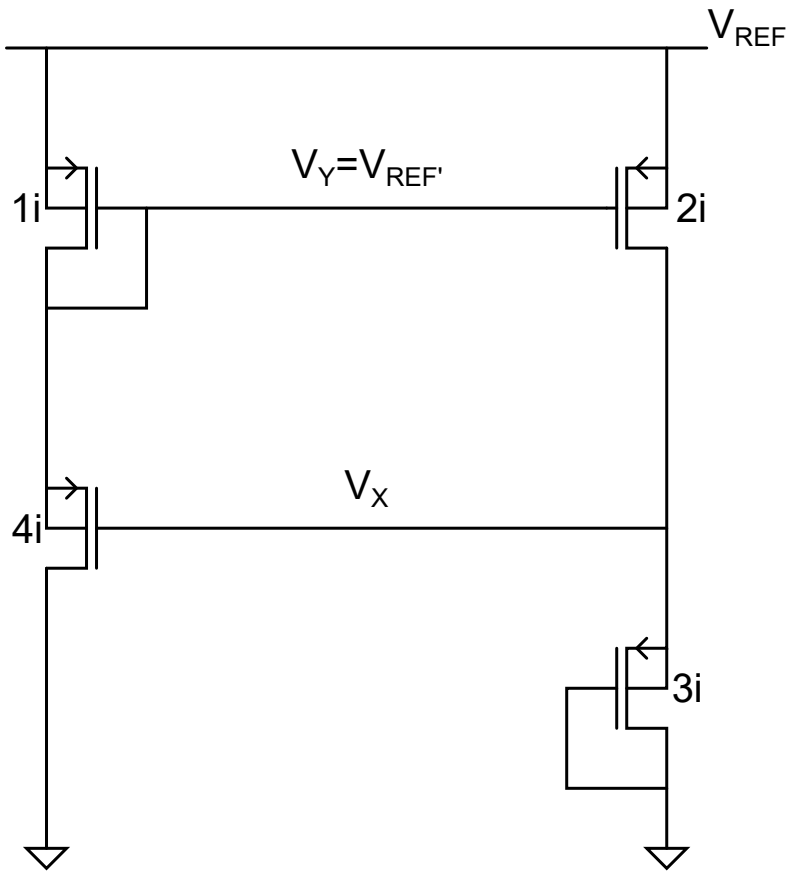


Figure 4.2. CMOS divider

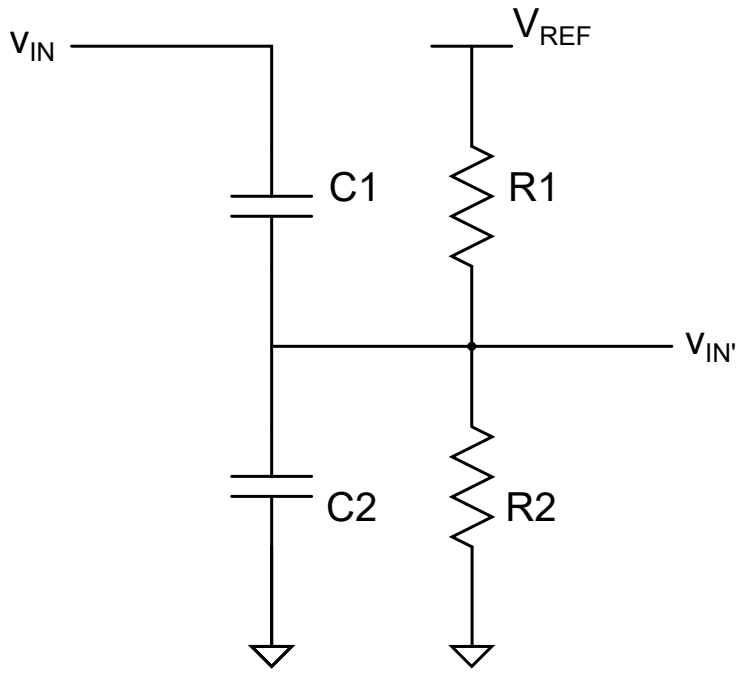


Figure 4.3. Input bias and conditioning

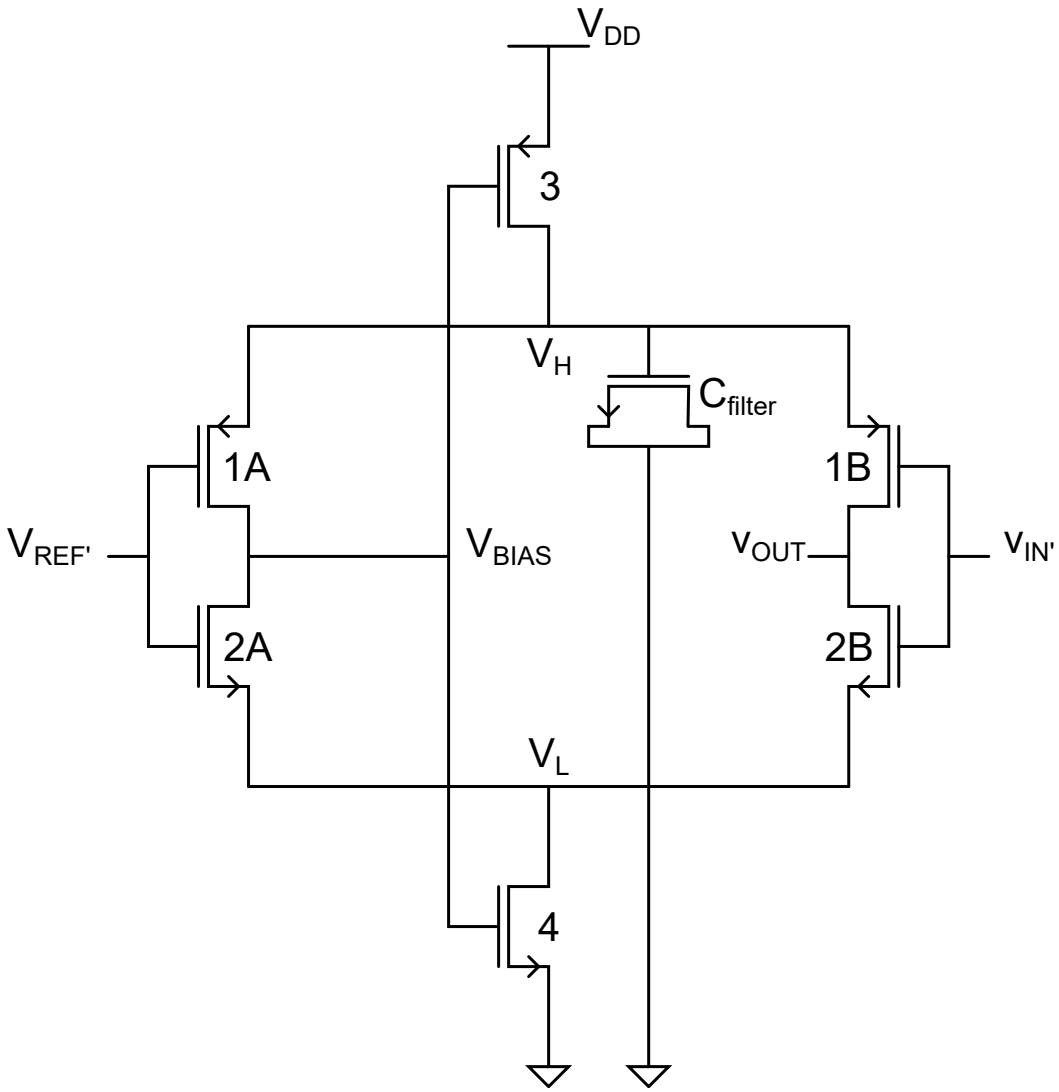


Figure 4.4. Self-biased push-pull preamplifier with CMOS filter capacitor

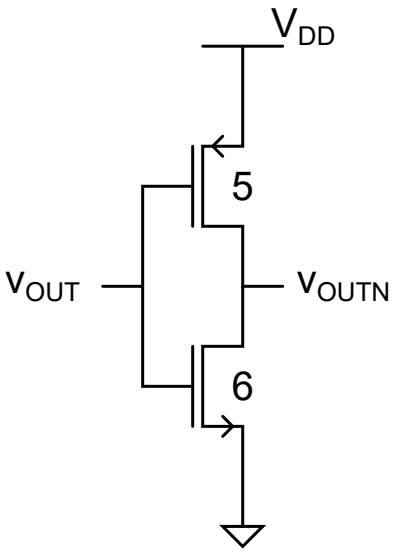


Figure 4.5. Decision stage (inverter)

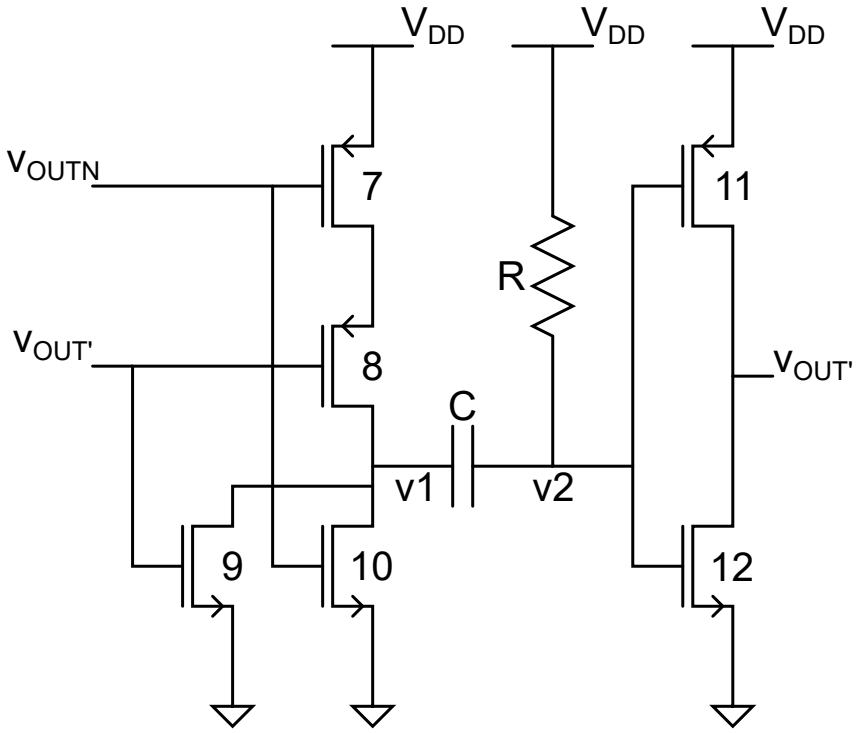


Figure 4.6. Monostable

## 4.2 Simulation

All the simulations were performed in the ADE L environment inside Cadence Virtuoso. When unspecified, the simulations were run at room temperature (27 °C). Bias voltage for input $V_{IN'}$ is equal to $800mV$, bias voltage for input $V_{REF'}$ is equal to $828mV$.

### 4.2.1 Input voltage variation

First, let's test how the output of each block behaves in response to a 1 ns triangular input pulse of variable amplitude.
The comparator's output switches successfully in the range [1, 10] V (figure 4.7).

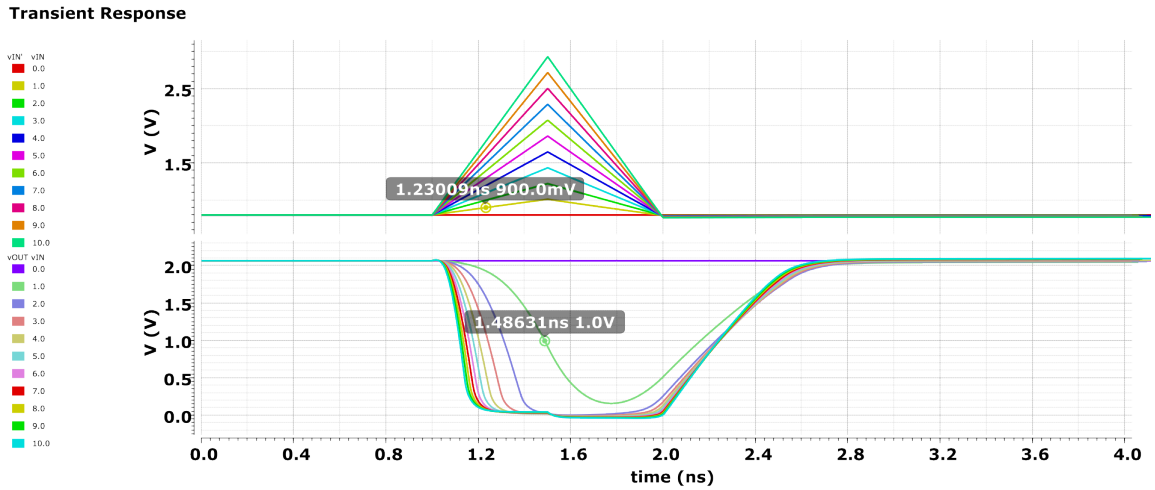


Figure 4.7. $v_{IN'}$ and $v_{OUT}$ as a function of time with parametric $v_{IN}$

The worst-case delay $t_D$ happens for $v_{IN} = 1V$ and corresponds to 250 ps.
The inverter's output switches successfully in the range [1, 10] V (figure 4.8).

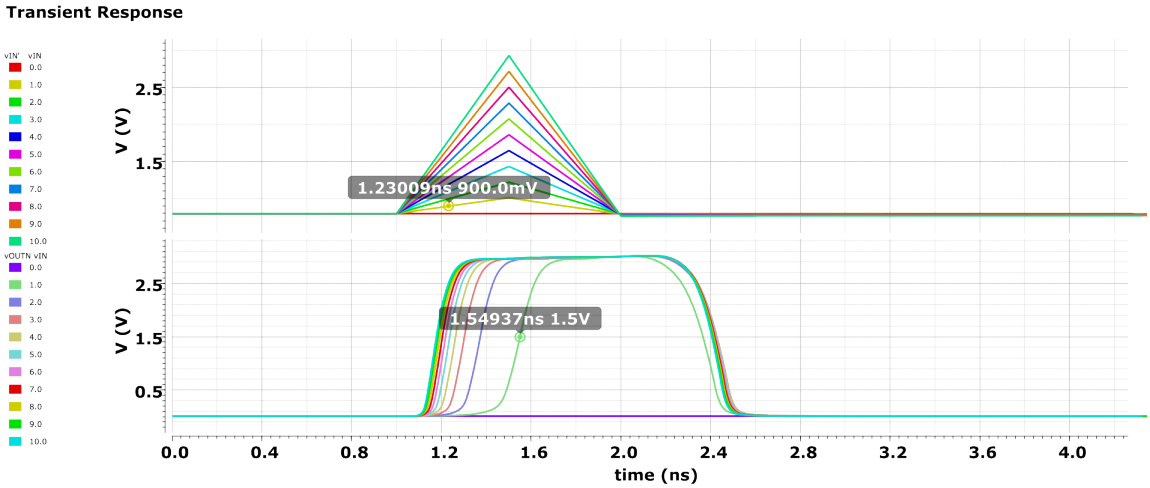


Figure 4.8. $v_{IN'}$ and $v_{OUTN}$ as a function of time with parametric $v_{IN}$

The worst-case delay $t_D$ happens for $v_{IN} = 1V$ and corresponds to 320 ps.
The monostable's output switches successfully in the range [1, 10] V and remains stable for about 10 ns (figure 4.9).

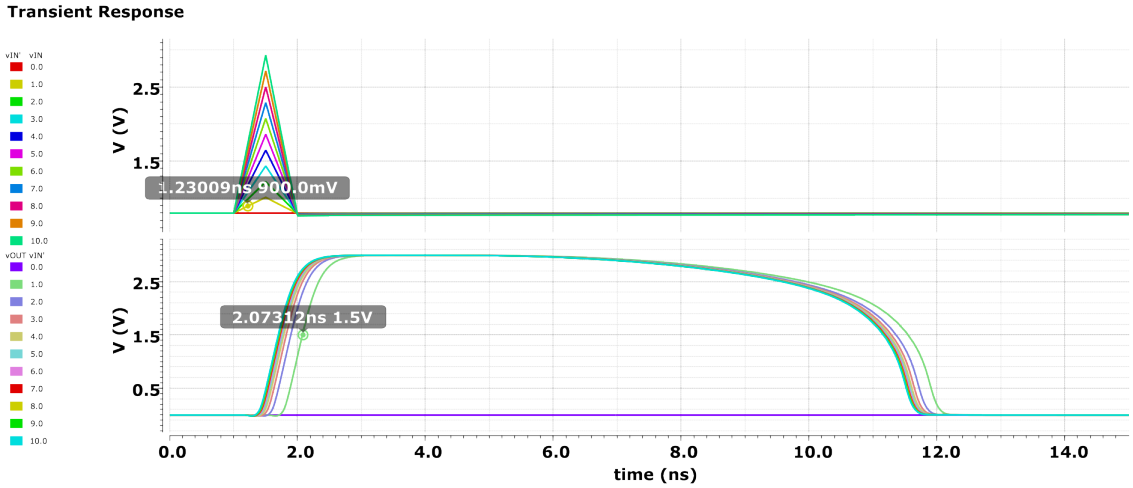


Figure 4.9. $v_{IN'}$ and $v_{OUT'}$ as a function of time with parametric $v_{IN}$

The worst-case delay $t_D$ happens for $v_{IN} = 1V$ and corresponds to 770 ps.
The circuit responds correctly to input pulses in the range [1,10] V, conform to the specifications.

Now, let's take it one step further and test the minimum ***overdrive*** (differential input voltage) for which the output switches successfully. For the sake of simplicity, let's limit this analysis to the output of the complete circuit, $v_{OUT'}$, and plot it as a function of time with $v_{IN}$ parametric in the range [0, 1] V (figure 4.10).

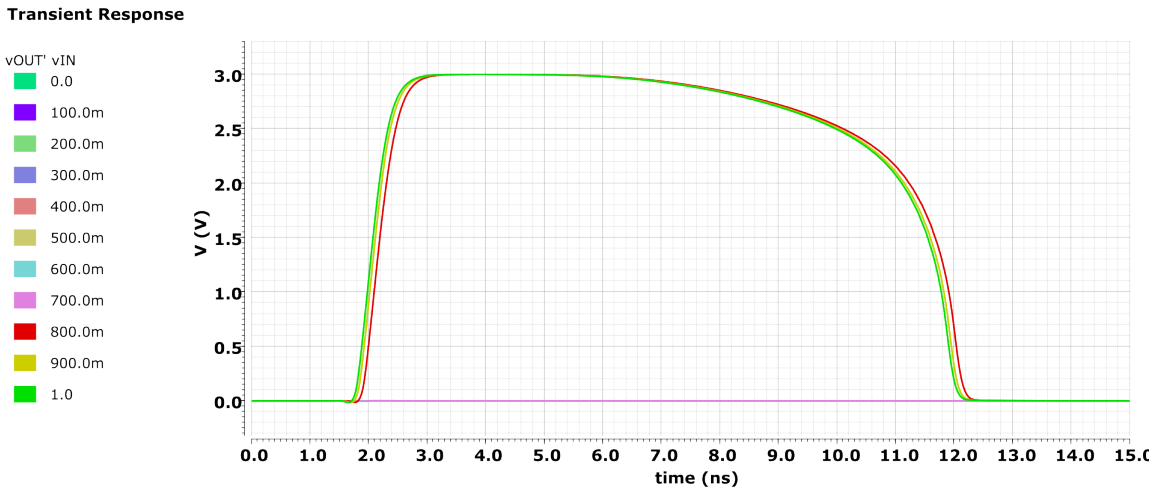


Figure 4.10. $v_{OUT'}$ as a function of time with parametric $v_{IN}$

The minimum value of $v_{IN}$ for which $v_{OUT'}$ switches to logic levels is equal to 800 mV. Considering the input conditioning circuit, this corresponds to a value of $v_{IN'}$ equal to 971 mV. Since the bias voltage $V_{IN'}$ was set to 800 mV, the minimum overdrive is about 171 mV.

### 4.2.2 Current consumption

Current consumption from the supply was simulated as a function of time and with parametric input voltage $v_{IN}$ (figure 4.11).
The behaviour of the current is strongly impulsive:

- Quiescent current is $30\mu A$.
- Peak current consumption is $620\mu A$ during the output's rising edge.
- When $v_{OUT'}$ is high and capacitor $C$ is being charged through $R$, the monostable block draws an additional $20\mu A$, temporarily bringing the quiescent current to $50\mu A$.

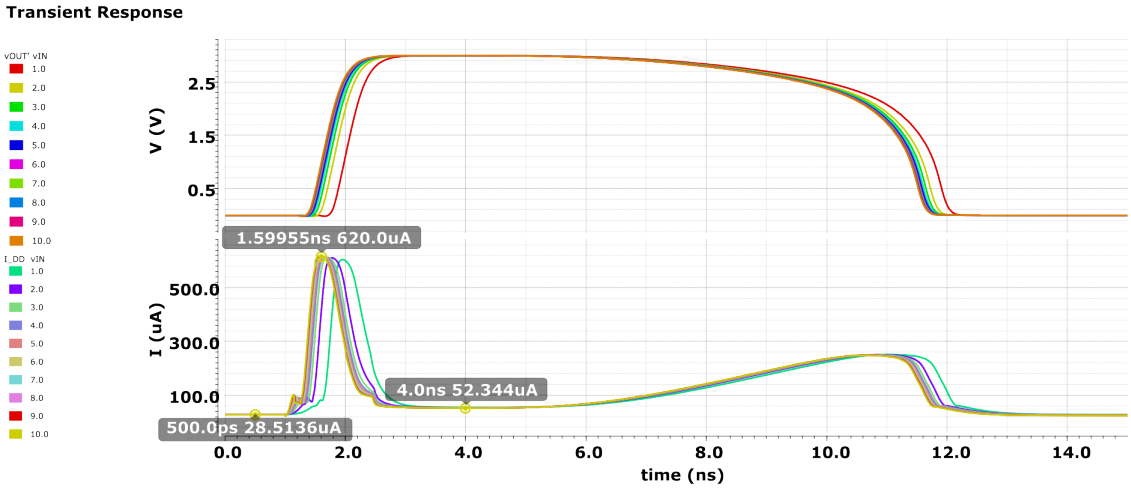


Figure 4.11. $I_{DD}$ as a function of time with parametric $v_{IN}$

### 4.2.3 Temperature

Variations in temperature affect the behaviour of the circuit in terms of both voltage and current.
The following simulations illustrate this dependency and are performed at the worst-case in terms of input voltage: $v_{IN} = 1V$.
The comparator's output switches successfully in the range [-40, 125] °C (figure 4.12).

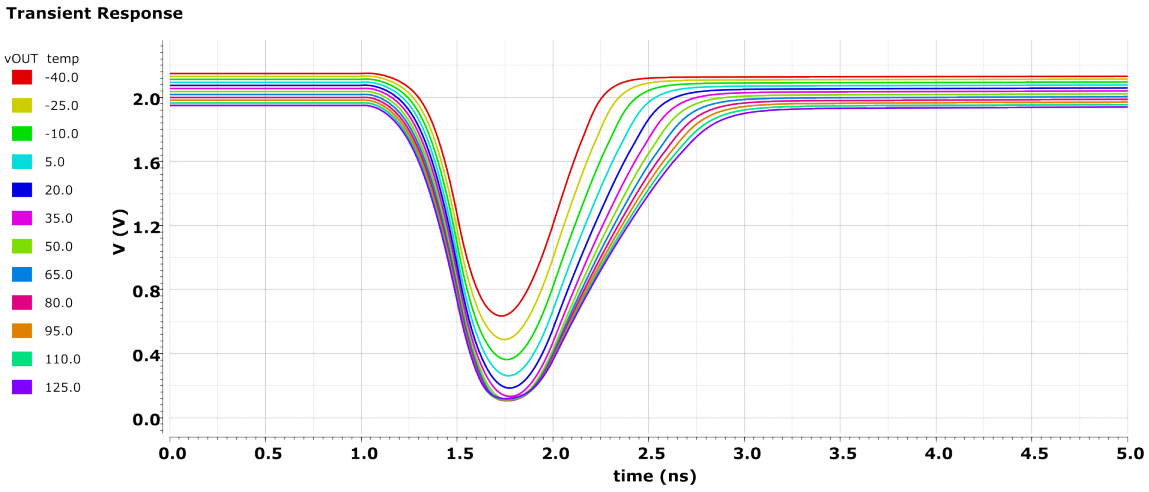


Figure 4.12. $v_{OUT}$ as a function of time with parametric temperature

The worst-case in terms of delay and amplitude swing happens for temp=-40 °C.
The inverter's output switches successfully in the range [-40, 125] °C (figure 4.13).

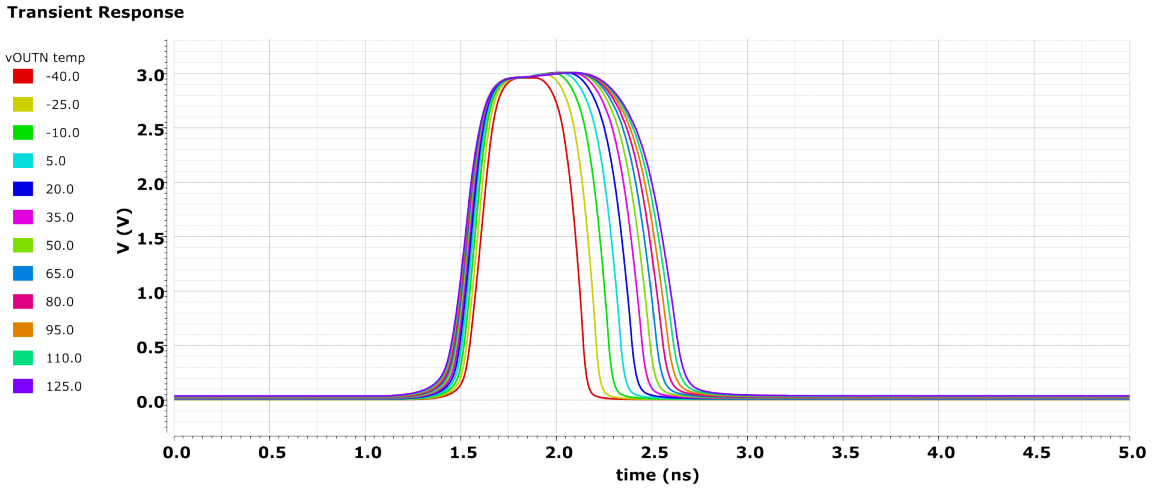


Figure 4.13. $v_{OUTN}$ as a function of time with parametric temperature

The worst-case in terms of delay and pulse duration happens for temp=-40 °C.
The monostable's output switches successfully in the range [-40, 125] °C (figure 4.14).

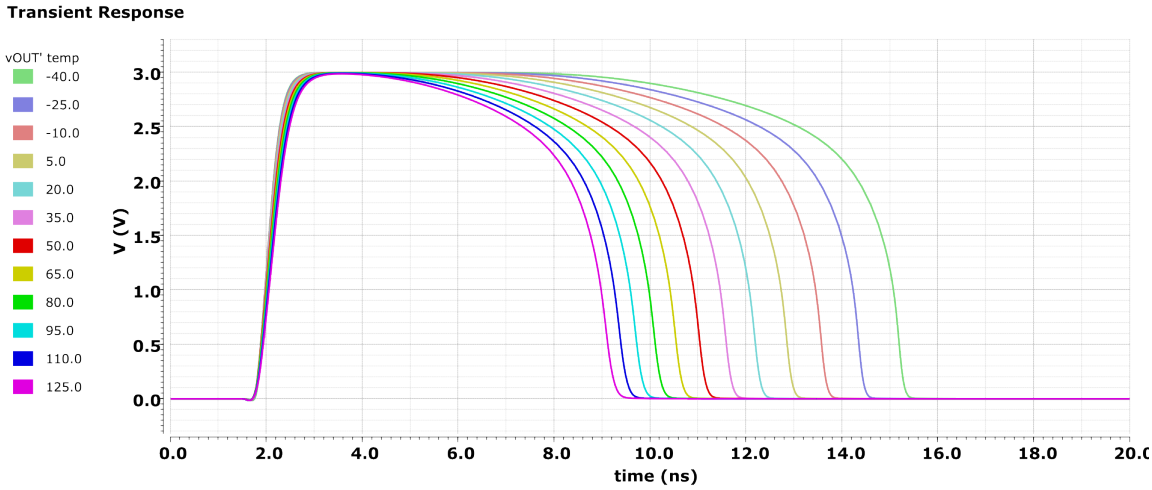


Figure 4.14. $v_{OUT'}$ as a function of time with parametric temperature

The worst-case in terms of pulse duration happens for temp=125 °C and corresponds to about 7 ns of output stability.
The circuit responds correctly to the worst-case input pulse in the temperature range [-40, 125] °C, conform to the specifications.
Current consumption from the supply was also simulated as a function of time and with parametric temperature (figure 4.15).

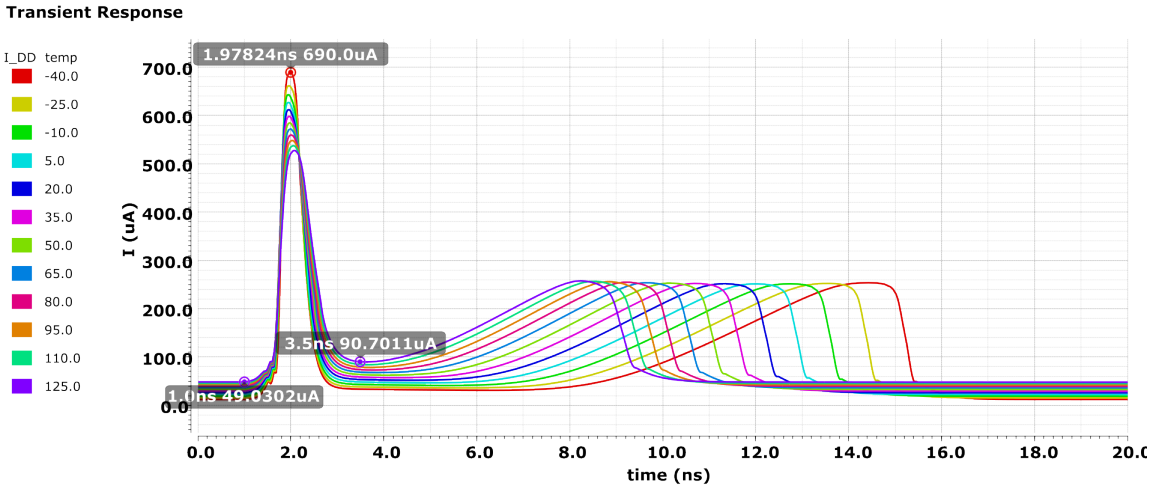


Figure 4.15. $I_{DD}$ as a function of time with parametric temperature

- Worst-case quiescent current is $50\mu A$ when $v_{OUT'}$ is low, $90\mu A$ when $v_{OUT'}$ is high at temp=125 °C.
- Worst-case peak current consumption is $690\mu A$ during the output's rising edge at temp=-40 °C.

Quiescent current never exceeds $100\mu A$, conform to the specifications.

### 4.2.4 Input Ringing

The output voltage $v_{OUT'}$ is supposed to switch state after the first pulse and remain stable for about 10 ns irrespectively of input variations. To test compliance with this specification, $v_{OUT'}$ as a function of time was plotted together with $v_{IN'}$. The ideal generator $v_{IN}$ was set to a period of 2 ns and amplitude of 1 V (figure 4.16) and 10 V (figure 4.17).
As long as the input ringing is contained within the duration of the output pulse $v_{OUT'}$, it does not cause unwanted transitions at the output of the circuit.

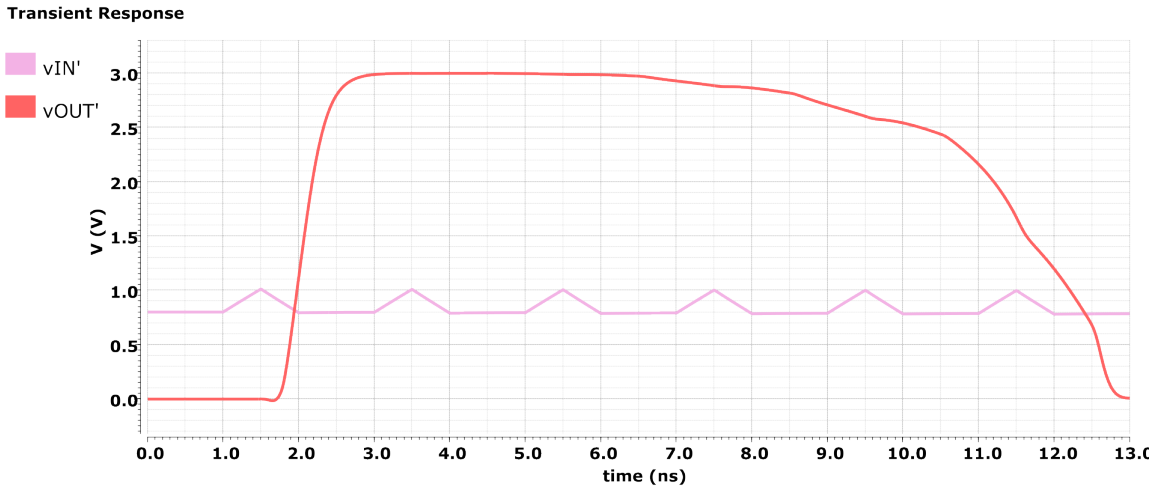


Figure 4.16. $v_{IN'}$ and $v_{OUT'}$ as a function of time with input ringing ($v_{IN} = 1V$)

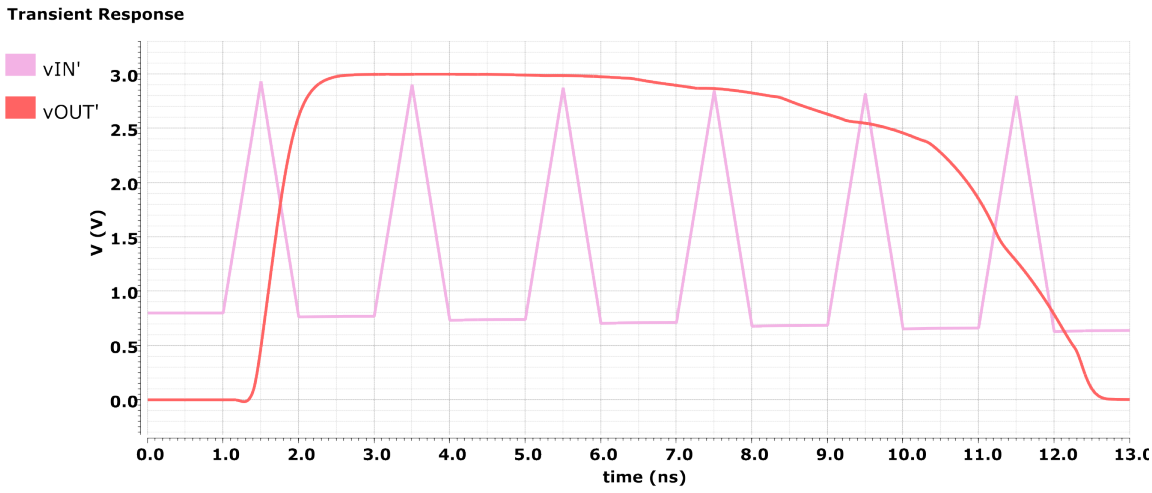


Figure 4.17. $v_{IN'}$ and $v_{OUT'}$ as a function of time with input ringing ($v_{IN} = 10V$)

# Chapter 5

# Conclusions and future work

The goal to design a comparator with sufficient speed to reliably monitor the gate-source voltage oscillations of a GaN HEMT was achieved.
Several comparator topologies were analysed: a simple open-loop OTA with class A final stage, presenting systematic offset and poor trade-off between speed and power consumption; a differential amplifier with class AB final stage and internal hysteresis, more efficient but still not suited to high-speed operation; clocked comparators based on the use of regenerative latches, potentially very fast and efficient but complex in design; finally, the best solution was found in high-speed continuous time comparators with a self-biased preamplifier and a decision stage, allowing for low quiescent current and high current peaks during commutation, guaranteeing optimal trade-off between power consumption and speed without the need for complex clock generation and memory circuits.
The final circuit is composed of: an input conditioning circuit with ESD protection, capacitive voltage divider connected to $v_{IN}$ and resistive bias network connected to $V_{REF}$ for input $v_{IN'}$; a CMOS voltage divider connected to $V_{REF}$ for input $V_{REF'}$; a self-biased differential preamplifier with filter capacitor $C_{filter}$; a decision stage made up by a simple inverter; a monostable output circuit with a CMOS NOR gate, a RC pull-up network and a CMOS NOT gate.
The circuit can safely condition the wide input range [0, 10] V to CMOS range [0, 3] V, and is equipped to withstand ESD events.
Input pulses of duration 1 ns in the voltage range [1, 10] V and in the temperature range [-40, 125] °C are elaborated correctly and cause the rail-to-rail output to switch states and remain stable for about 10 ns, so that any successive input ringing does not cause unwanted transitions.
Satisfactory trade-off between speed and power consumption is ensured thanks to the implementation of dynamic supply current behaviour, with quiescent currents no higher than 90 $\mu$A and peaks up to 700 $\mu$A during output transitions.
Paired with the active gate driver's control unit, the proposed circuit can work effectively as a safety measure to ensure nominal operation of GaN power devices.
In this thesis, gate-source voltage oscillations were modelled as triangular pulses.
In reality, these pulses follow a rectangular waveform which represents the nominal command to switch on and off the GaN HEMT device.

To avoid activating the comparator during normal operation and saturation of its input conditioning circuit, a network of switches connected to the power device enable signal could be added to the design.
This would also reduce power consumption by effectively switching off the comparator when it is not needed.

# Bibliography


Phillip E Allen and Douglas R Holberg. *CMOS analog circuit design*. Elsevier, 2011.

R Jacob Baker. *CMOS: circuit design, layout, and simulation*. John Wiley & Sons, 2019.

Mel Bazes. Two novel fully complementary self-biased cmos differential amplifiers. *IEEE Journal of Solid-State Circuits*, 26(2):165–168, 1991.

Igor A Danilov, Maxim S Gorbunov, and Alexander Y Nikiforov. A mos temperature-insensitive voltage divider and its application for voltage reference design. In *2021 IEEE 32nd International Conference on Microelectronics (MIEL)*, pages 235–238. IEEE, 2021.

Pedro M Figueiredo and Joao C Vital. Kickback noise reduction techniques for cmos latched comparators. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 53(7):541–545, 2006.

Vladimir Milovanović and Horst Zimmermann. A 40 nm lp cmos self-biased continuous-time comparator with sub-100ps delay at 1.1 v & 1.2 mw. In *2013 Proceedings of the ESSCIRC (ESSCIRC)*, pages 101–104. IEEE, 2013.

Behzad Razavi. The strongarm latch [a circuit for all seasons]. *IEEE Solid-State Circuits Magazine*, 7(2):12–17, 2015.

Bo Shen, Sunil P Khatri, and Takis Zourntos. Implementation of mosfet based capacitors for digital applications. In *Proceedings of the 16th ACM Great Lakes symposium on VLSI*, pages 180–186, 2006.