POLITECNICO DI TORINO
INSA Lyon, École Centrale Lyon
Université Claude Bernard, INL

Master in Electronic Micro and Nanosystem Engineering

Master thesis

Electrical characterisation and analysis of memories based on hafnium zirconium oxide

Politecnico di Torino

Supervisors:
Thesis Supervisor: Damien Deleruyelle
Thesis Supervisor: Gianluca Piccinini
Co-Supervisor: Jordan Bouaziz
Co-Supervisor: Bertrand Vilquin
Co-Supervisor: Mariagrazia Graziano

Candidate:
Chiara Lepri

Abstract

This thesis focuses on the electrical characterization of ferroelectric memories based on hafnium zirconium oxide (HZO). The study focuses on defining protocols that involve sequences of signals applied to the sample using a Keithley 4200 parameter analyzer and a probe station. The objective was to measure the current and voltage across the device's electrodes and analyze parameters related to the performance and reliability of these memories.
The goal of evaluating the results was to identify the relationship between technological parameters and the electrical properties of the memory. This investigation aimed to identify the best combination of parameters to improve both reliability and performance. A key aspect of this research was the detailed study of the imprint phenomenon, which significantly impacts device reliability.
Our findings contribute to a deeper understanding of the behaviour of HZO-based ferroelectric memory, providing ideas on how to increase their operating stability and efficiency.This work serves as a contribution to the development and progress of ferroelectric memory technology.

Sommario

Questa tesi si concentra sulla caratterizzazione elettrica delle memorie ferroelettriche a base di ossido di afnio e zirconio (HZO). Lo studio si focalizza sulla definizione di protocolli che coinvolgono sequenze di segnali applicati al campione utilizzando un analizzatore di parametri Keithley 4200 e una stazione di prova. L'obiettivo era misurare la corrente e la tensione sugli elettrodi del dispositivo e analizzare i parametri relativi alle prestazioni e all'affidabilità di queste memorie.
Lo scopo dello studio dei risultati era identificare la relazione tra i parametri tecnologici e le proprietà elettriche della memoria. Questa analisi era volta a determinare la combinazione ottimale di parametri per migliorare sia le prestazioni che l'affidabilità.
Un aspetto chiave di questa ricerca è stato lo studio dettagliato del fenomeno dell'imprint, che influisce significativamente sull'affidabilità del dispositivo. I nostri risultati contribuiscono a una comprensione più approfondita del comportamento delle memorie ferroelettriche basate su HZO, fornendo spunti su come aumentare la loro stabilità operativa e l'efficienza. Questo lavoro rappresenta un contributo allo sviluppo e al progresso della tecnologia delle memorie ferroelettriche.

Acknowledgements

I would like to start by thanking my professor, Damien Deleruyelle, for his guidance and support throughout this thesis project.
I am also appreciative to my tutors, Jordan Bouaziz and Bertrand Vilquin.
I am grateful for the trust they placed in me and for constantly encouraging me to push through and overcome the challenges of this project.
A special mention goes to the members of the FerroTeam, in particular to Kevin Alhada Lahbabi, Gregoire Magagnin,Edouard Lumbwe, Sara Gonzalez and Ahmed Kouissi. Working with you made this internship both productive and enjoyable.
This internship has been a valuable opportunity for me to grow, both personally and professionally. The challenges I encountered in this stimulating environment helped me gain new skills and perspectives. Wrapping up my Erasmus experience on such a positive note wouldn't have been possible without the collective support and encouragement of everyone mentioned above.
Lastly, I want to thank my friends whom I had the pleasure of meeting during my time in Lyon, who filled this journey with unforgettable memories, especially Emanuele, Alfonso, Khalil, Ricardo, Mattia, Giulia, Daniele, Carolina, Mateusz, Dusan, Marta, Reewa, Matilde, Alexis, Philippa, Paula, Roberto, Valeria and Erica.
I would also like to extend my gratitude to my friends who, even from afar, have supported me with their affection and encouragement. In particular, I want to thank my childhood friends Marta Ronconi, Francesca Torrini, Francesca Berretti, Alessandra Tatangelo, Giorgia Galeotti, and Viola Nuti, as well as my "Buddha e Pesto" friends, Stefano Dreoni and Elisa Pietracito. I am also grateful to my friend of aperitif Bernardo Mercatali, my sweet flatmate Giada La Chiusa, all the ADB and the friend groups "Panca Boys", "Locuste del Mugello" and "Variante Baku".
Additionally, I would like to extend my sincere thanks to my colleagues and friends from the Polytechnic: Caterina Verny, Vincenzo Giannone, Calin Ion Maraloiu, Hernan Toloza, Roberto Listo, Alessandro Puddu e Valeria D'Antonio. The wonderful experiences we shared together, their support during our study sessions, the breaks we enjoyed, and the encouragement we gave each other throughout every exam were instrumental to my success in this degree. I truly believe that this achievement is as much theirs as it is mine.
Finally, I want to offer a special thanks to my family. Your support has been an invaluable source of strength and motivation.

Indice

Elenco delle figure 7

1 Introduction 11
1.1 Neuromorphic architecture . . . 11
1.2 Memristor as Artificial Synapses . . . 12

2 Theoretical background 15
2.1 Ferroelectricity . . . 15
2.2 Landau Devonshire Theory . . . 17
2.3 Ferroelectric Domains and Polarisation switching . . . 18
2.4 Ferroelectric Materials . . . 19
2.5 HfO_2-based materials . . . 19
2.6 Ferroelectric Non-volatile Memory Devices . . . 22
2.7 Application of FTJ as artificial synapses . . . 23
2.8 Imprint phenomenon . . . 24
2.9 Internship objectives . . . 26

3 Methodology 29
3.1 Fabrication process . . . 29
3.2 Electrical characterization . . . 31
3.2.1 PUND measurement . . . 31
3.2.2 Endurance test . . . 34
3.2.3 Imprint measurement . . . 36
3.2.4 Recovery for the imprint . . . 41
3.3 Differential equations for the imprint phenomenon . . . 42

4 Results 45
4.1 Measurements on the reference sample . . . 45
4.1.1 Endurance test . . . 45
4.1.2 Imprint measurements . . . 48
4.2 Measurements on O_3 oxidised sample . . . 52
4.2.1 Endurance test . . . 52
4.2.2 Imprint measurements . . . 54
4.3 Measurements on O_2 oxidised sample . . . 57
4.3.1 Endurance test . . . 58

4.3.2 Imprint measurements 59
4.4 Impact of oxidized layer and oxygen vacancies 61

5 Conclusion and future perspectives 65

6 Appendix 67
6.1 Imprint measurements on the reference sample 67
6.2 Imprint measurements on O_2 oxidised sample 75
6.3 Imprint measurements on O_3 oxidised sample 81

Bibliografia 85

Elenco delle figure

1.1 Evolution of microprocessors performance. In recent years, while the clock frequency of a single processor (green squares) has plateaued, the number of cores per processors (black diamonds) has been steadily increasing, which reflects the focus on parallelisation over power[1]. 11
1.2 Von Neumann (a) [3] and Neuromorphic (b) architecture [4]. 12
1.3 Examples of artificial synapses [5]. 13
1.4 Ferroelectric tunnel junction [11] 13

2.1 Hysteresis loop [2]. 15
2.2 (a) Ferroelectricity in $PbTiO_3$-based perovskite thin films (b) Paraelectric phase for T > Tc[35]. 16
2.3 (a) First order phase transition : free energy as a function of the polarisation at T >Tc, T =Tc,and T = To < Tc ; (b) Schematic picture of hysteresis in an idealized ferroelectric [12]. 17
2.4 Ferroelectric domain [16]. 18
2.5 (a)Perovskite in the cubic phase. (b), (c) Atomic positions of PbTiO3 (A = Pb, B = Ti) in the ferroelectric tetragonal phase for up and down oriented polarisations. The Ti ion and oxygen octahedron are shifted in the same direction but the magnitude of the shift is greater for the oxygen octahedron [19]. 19
2.6 HZO phases[7]. 20
2.7 Orthorhombic HfO_2 Pbc21[7]. 20
2.8 Ferroelectric memories [22]. 22
2.9 Ferroelectric tunnel junction [11]. 23
2.10 (a) Schematic comparison between a biological synapse with pre- and postneuron connection and the FTJ used in this work. (b) Measured spike-timing-dependent plasticity (STDP) curves. The resulting resistance of the FTJ is a function of the time delay Δt between pre- andpostneuron action potentials leading to an increased or decreased resistance of the FTJ that represents a weakening or strengthening of the synapse. [14] 24
2.11 Positive imprint (a) and negative imprint (b). 25
2.12 Imprint mechanism [24],[10]. 26
2.13 Keithley 4200 parameter analyzer and 4225-RPM modules. 27

3.1 RF Magnetron Sputtering. 29
3.2 Analyzed samples. 30
3.3 Measurement set up. 31
3.4 PUND protocol. 32
3.5 Access to the bottom electrode. 35
3.6 PE signal. 35
3.7 Endurance (Sample 1, V = 2.5 V). 36
3.8 FE capacitor : Programming the "up" (a) and programming the "down" state (b). 37
3.9 Imprint protocol (positive and negative imprint measurement) 38
3.10 Positive (a) and Negative (b) imprint. 39
3.11 Switching current, applied voltage and coercitive voltage relation for the positive imprint. 40
3.12 Vc^{-}_{ref} evolution with respect to t_{pause} (a) and positive imprint (b). . . . 41
3.13 Recovery for the imprint. 42
3.14 Reference PV loop after the imprint recovery. 42

4.1 Reference sample. 45
4.2 Chronogram(b), Endurance(a) and PV loop achieved through PN measurement (c), PV loop obtained with PUND measurement (d) for 2.5 V. 46
4.3 Chronogram(b), Endurance(a) and PV loop achieved through PN measurement (c), PV loop obtained with PUND measurement (d) for 3 V. . . . 47
4.4 Chronogram(b), Endurance(a) and PV loop achieved through PN measurement (c), PV loop obtained with PUND measurement (d) for 3.5 V. 47
4.5 Positive imprint VS negative imprint. 49
4.6 Positive imprint (a) and negative imprint (b) with respect to the variable applied voltage and fixed 10^3 wake up cycles; Positive imprint (c) and negative imprint (d) with respect to the variable wake up cycles and fixed voltage at 3 V. 49
4.7 Positive imprint (a) and negative imprint (b) with respect to the variable applied voltage and fixed 10^3 wake up cycles; Positive imprint (c) and negative imprint (d) with respect to the variable wake up cycles and fixed voltage at 3 V. 51
4.8 Positive imprint (a) and negative imprint (b) on different FeCaps when 3 V and 10^5 wake up cycles are applied. 52
4.9 O_3 oxidised sample. 52
4.10 Chronogram(b), Endurance(a) and PV loop achieved through PN measurement (c), PV loop obtained with PUND measurement (d) for 2.5 V. 53
4.11 Chronogram(b), Endurance(a) and PV loop achieved through PN measurement (c), PV loop obtained with PUND measurement (d) for 3 V. . . . 53

4.12 Chronogram(b), Endurance(a) and PV loop achieved through PN measurement (c), PV loop obtained with PUND measurement (d) for 3.5 V. 54
4.13 Positive imprint (a) and negative imprint (b) with respect to the variable applied voltage and fixed 10^3 wake up cycles; Positive imprint (c) and negative imprint (d) with respect to the variable wake up cycles and fixed voltage at 3 V 55
4.14 Positive imprint (a) and negative imprint (b) with respect to the variable applied voltage and fixed 10^3 wake up cycles; Positive imprint (c) and negative imprint (d) with respect to the variable wake up cycles and fixed voltage at 3 V. 57
4.15 O_2 oxidised sample. 57
4.16 Chronogram(b), Endurance(a) and PV loop achieved through PN measurement (c), PV loop obtained with PUND measurement (d) for 2.5 V. 58
4.17 Chronogram(b), Endurance(a) and PV loop achieved through PN measurement (c), PV loop obtained with PUND measurement (d) for 3 V. . . . 59
4.18 Positive imprint (a) and negative imprint (b) with respect to the variable applied voltage and fixed 10^3 wake up cycles; Positive imprint (c) and negative imprint (d) with respect to the variable wake up cycles and fixed voltage at 3 V. 60
4.19 Sample 1 VS sample 2 VS sample 3 when 3 V and 10^4 cycles : (a) positive imprint ; (b) negative imprint. 61
4.20 Positive imprint mechanism. 62
4.21 Sample 1 VS sample 2 VS sample 3 when 3.5 V and 10^3 cycles : (a) positive imprint ; (b) negative imprint. 62
4.22 Sample 1 VS sample 2 when 3 V and 10^3 cycles : (a) positive imprint ; (b) negative imprint. 63
4.23 Sample 1 VS sample 2 when 3 V and 10^4 cycles : (a) positive imprint ; (b) negative imprint. 63
4.24 Sample 1 VS sample 2 when 3 V and 10^5 cycles : (a) positive imprint ; (b) negative imprint. 63
4.25 Sample 1 VS sample 2 when 3.5 V and 10^3 cycles : (a) positive imprint ; (b) negative imprint. 64

6.1 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 2.5 V and 10^3 cycles. 68
6.2 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^3 cycles. 68
6.3 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3.5 V and 10^3 cycles. 69
6.4 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^3 cycles. 69
6.5 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^4 cycles. 70

6.6 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^5 cycles. 70
6.7 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 2.5 V and 10^3 cycles. 71
6.8 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^3 cycles. 72
6.9 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3.5 V and 10^3 cycles. 72
6.10 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^3 cycles. 73
6.11 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^4 cycles. 73
6.12 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^5 cycles. 74
6.13 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 2.5 V and 10^3 cycles. 75
6.14 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^3 cycles. 76
6.15 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3.5 V and 10^3 cycles. 76
6.16 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^3 cycles. 77
6.17 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^4 cycles. 77
6.18 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^5 cycles. 78
6.19 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 2.5 V and 10^3 cycles. 79
6.20 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^3 cycles. 79
6.21 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3.5 V and 10^3 cycles. 80
6.22 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^4 cycles. 80
6.23 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 2.5 V and 10^3 cycles. 81
6.24 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^3 cycles. 82
6.25 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3.5 V and 10^3 cycles. 82
6.26 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^4 cycles. 83
6.27 PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^5 cycles. 83

Capitolo 1

Introduction

1.1 Neuromorphic architecture

Currently, all computers are based on the Von Neumann architecture, where communication occurs between the CPU and memories. Despite Moore's Law indicating that transistor density is exponentially increasing, leading to improved computational performance, a saturation point has been reached in processing frequency and transistor scalability (Figure 1.1.). This limit in speed and bandwidth between the CPU and memories is known as the Von Neumann bottleneck. To improve computing performance, multiple cores working in parallel are used, resulting in high power consumption. However, to address this issue, new computing paradigms such as neuromorphic computing must be developed.

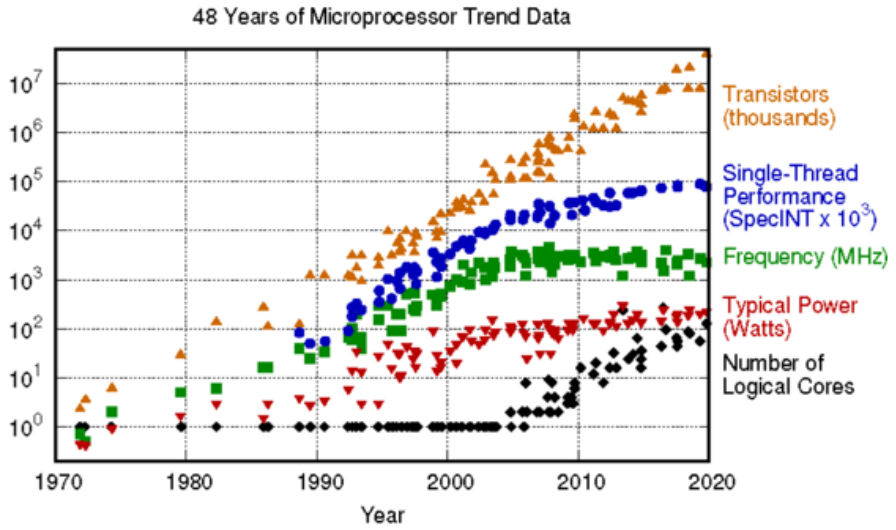

Figura 1.1: Evolution of microprocessors performance. In recent years, while the clock frequency of a single processor (green squares) has plateaued, the number of cores per processors (black diamonds) has been steadily increasing, which reflects the focus on parallelisation over power[1].

Inspired by the functioning of the human brain, a new computing method can be defined as a neural network made of neurons and synapses working in parallel. This approach increases computational speed and allows for the processing of large amounts of data with very low power consumption. This bio-inspired data processing is known as neuromorphic computing [18]. Although lab tests are promising, this technology is not yet commercially practical. The goal of research has been to improve materials, integration processes, and algorithms for large-scale commercialisation.

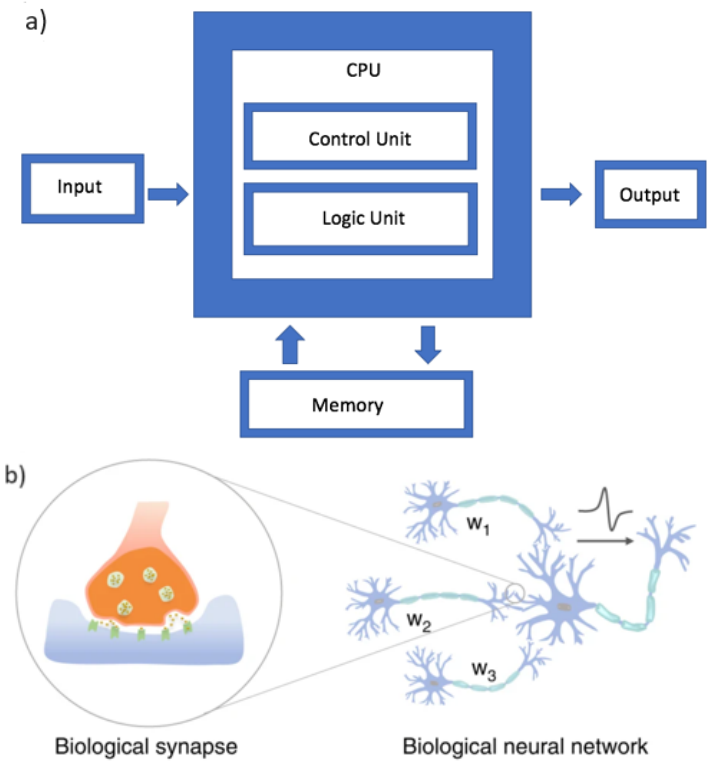

Figura 1.2: Von Neumann (a) [3] and Neuromorphic (b) architecture [4].

1.2 Memristor as Artificial Synapses

Controlling factors for developing an artificial neuromorphic system include suitable memory materials, effective integration techniques, circuit design, and algorithms that simulate synaptic processes. The theory of the memristor, proposed by Leon Chua in 1971 [6] describes a non-volatile memory device essential for brain-inspired memory arrays. Emerging technologies are capable of emulating synaptic plasticity by modulating current. Resistive memories, for example, regulate the output current flow by varying the resistivity of the metal oxide layer. Figure 1.3 shows other types include Phase Change RAM memory, magnetic resistive RAM, and ferroelectric RAM, all of which modulate output current to encode values as 1 or 0.

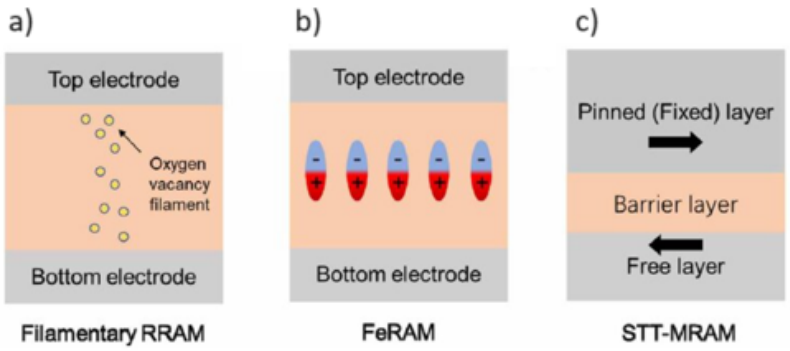

Figura 1.3: Examples of artificial synapses [5].

Among the various materials and methodologies investigated for memristors, ferroelectric materials show great promise for analog information storage due to their numerous non-volatile resistance states [17]. Previously, ferroelectric materials based on perovskites were used in non-volatile memory devices but were incompatible with the CMOS process, because of the high required annealing temperature.
The incorporation of ferroelectric memory devices into the CMOS industry was made possible by the discovery of ferroelectricity in doped hafnium oxide by Böscke in 2011 [7]. Using crossbar designs to arrange ferroelectric memristors in dense memory arrays can enhance hardware scalability. Crossbar arrays represent the idea of in-memory computing, as they perform computations directly into the memory due to their non-volatility and low-power programmability.
The goal is to use CMOS-compatible Hafnium Zirconium Oxide (HZO) to build and optimize ferroelectric tunnel junction (FTJ) memristors, illustrated in Figure 1.4, for neuromorphic applications. In order to create FTJs that accurately mimic biological synapses, a study has been conducted on the reliability and performance of such devices to identify the factors influencing these parameters. This study involves detailed electrical characterizations, followed by an analysis of the electrical measurements, structural, physical, and technological processes used in various devices based on ultra-thin HZO films.

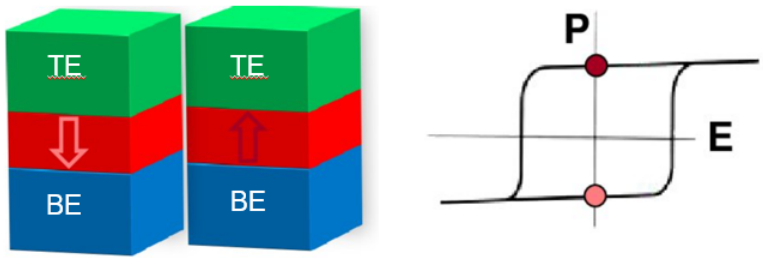

Figura 1.4: Ferroelectric tunnel junction [11]

Capitolo 2

Theoretical background

2.1 Ferroelectricity

Certain materials have a feature called ferroelectricity that allows for spontaneous electric polarisation to develop even in the absence of an external electric field. This spontaneous polarisation can be reoriented or reversed when an external electric field is applied.
These crystals exhibit spontaneous polarisation due to their non-centrosymmetric lattice structure, which results in an inherent dipole moment.
The behavior of these materials can be visualized through the hysteresis loop, a graphical representation of the polarisation versus the electric field, shown in Figure 2.1.When an electric field is applied, the polarisation changes, creating a loop that displays the ability of the material to retain polarisation even after the external field is removed (The unit of measurement for the polarisation on the y axes is charge per unit area (C/cm^2)) [26]. When a ferroelectric material is subjected to a positive electric field, its polarisation increases until it saturates. If the field is reduced to zero, a remanent polarisation (Pr) remains. Applying a negative field the polarisation is reduced and ultimately reversed.

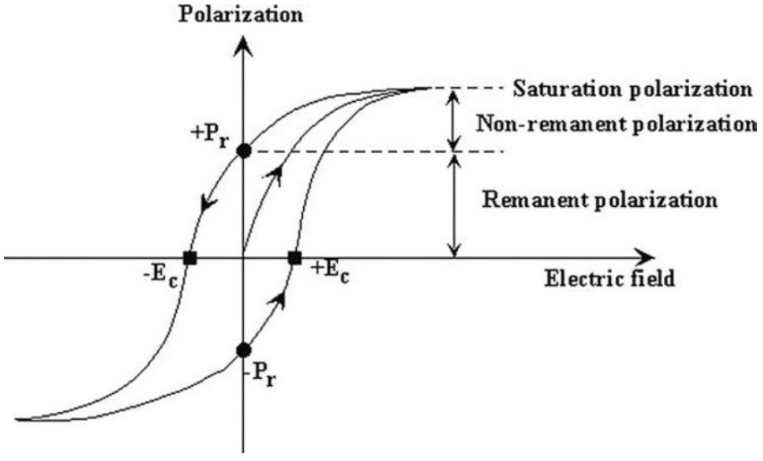

Figura 2.1: Hysteresis loop [2].

Ferroelectrics' main characteristic, which changes polarisation directions in response to an applied external electric field, occurs because these materials have at least two stable equilibrium states for their spontaneous polarisation vector.
Such characteristics to maintain a polarized state without continuous power are crucial for applications in memory storage devices, like ferroelectric tunnel junctions and transistors [28].
Ferroelectric materials often undergo a structural phase transition at a specific temperature known as the Curie temperature (Tc). Below this temperature, they exhibit ferroelectric properties, while above it, they lose their spontaneous polarisation due a transition into a paraelectric phase (Figure 2.2).
The transition at the Curie temperature can be described by the following formula:

$$P(T) = P_0 \left(1 - \frac{T}{T_C}\right)^{\beta}$$

where:
- $P(T)$ is the polarisation at temperature T,
- P_0 is the polarisation at absolute zero temperature,
- T is the temperature,
- T_C is the Curie temperature,
- β is a critical exponent that describes the nature of the phase transition.

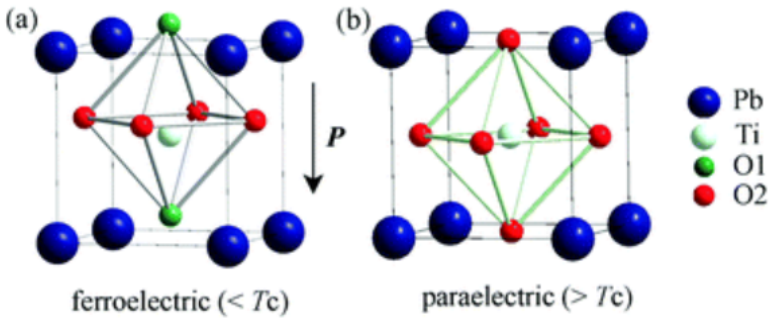

Figura 2.2: (a) Ferroelectricity in $PbTiO_3$-based perovskite thin films (b) Paraelectric phase for T > Tc[35].

Ferroelectrics also exhibit a reversible relationship between mechanical stress and electric polarisation, which makes them piezoelectric.
Therefore, the combination of dielectric, piezoelectric, and pyroelectric properties, as well as spontaneous polarisation and phase transitions at Curie temperatures, distinguish ferroelectric materials from other materials. These qualities make them useful in various advanced technological applications [28].

2.2 Landau Devonshire Theory

The Landau-Ginzburg-Devonshire (LGD) theory describes the free energy of a ferroelectric material as a function of temperature and polarisation, offering a theoretical foundation for understanding ferroelectricity.
This theory expands the free energy F as a polynomial series:

$$F = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$$

where :
- P is the polarisation
-α, β, and γ are temperature-dependent coefficients
-E is the electric field

The coefficient β plays a crucial role in determining the nature of the phase transition. In ferroelectric materials, β becomes negative below the Curie temperature, leading to spontaneous polarisation [33].

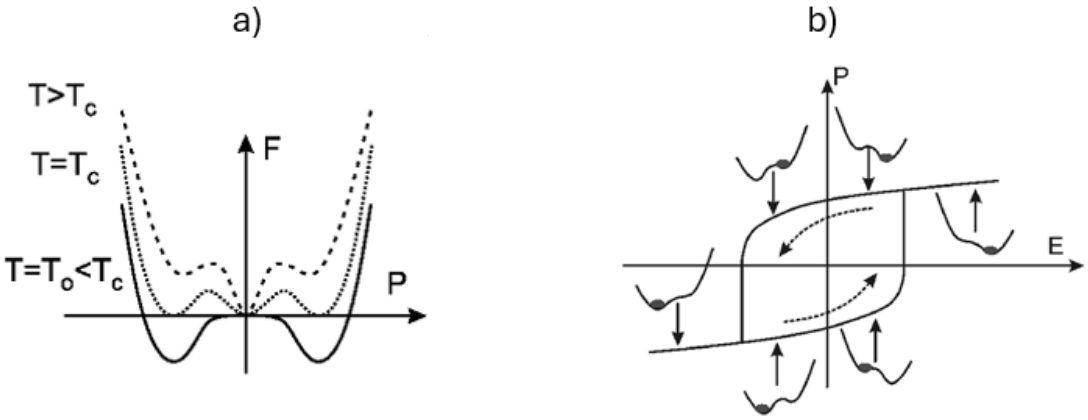

Figura 2.3: (a) First order phase transition : free energy as a function of the polarisation at T >Tc, T =Tc,and T = To < Tc ; (b) Schematic picture of hysteresis in an idealized ferroelectric [12].

The transition into the ferroelectric phase can be either first-order or second-order. In a first-order phase transition, the polarisation changes discontinuously at the Curie temperature. A second-order phase transition, on the other hand, involves no abrupt changes in polarisation but rather a gradual reduction with increasing temperature.
The LGD theory also explains the creation of domains, regions inside the material where the polarisation is uniformly aligned, and the dynamics of domain walls, which are the boundaries between these regions [36].

2.3 Ferroelectric Domains and Polarisation switching

Ferroelectric domains and polarisation switching are key aspects of ferroelectric materials that determine their functional properties.
Ferroelectric domains are regions within a ferroelectric material where the polarisation is uniformly aligned.

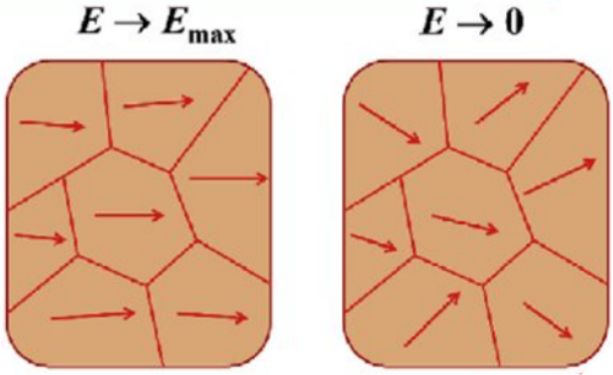

Figura 2.4: Ferroelectric domain [16].

The formation of ferroelectric domains, in Figure 2.4, is given by the need to minimize the material's electrostatic and elastic energy. When the ferroelectric crystal gets heated to a temperature lower than its Curie temperature, it experiences a phase transition from a paraelectric to a ferroelectric state, resulting in spontaneous polarisation. To reduce the overall energy, the material breaks up into domains where the polarisation vectors point in various directions, often opposite to each other [22].
Domain walls are the interfaces between these regions uniformly polarised. They can be categorized classified according to the relative orientation of the polarisation vectors in adjacent domains. The most common types are 180-degree and 90-degree domain walls. In 180-degree domain walls, the polarisation direction in adjacent domains is exactly opposite, while in 90-degree domain walls, the polarisation directions are perpendicular to each other. These domain walls have a significant impact on the material's ferroelectric characteristics and its response to external electric fields.
The polarisation switching occurs when an external electric field is applied, causing the polarisation vector in the domains to reorient and align with the applied field. However, the presence of impurities and defects can pin domain walls, making it more difficult for them to move and thus increasing the coercive field.
The study of domain dynamics and polarisation switching is crucial for optimize the performance and reliability of ferroelectric devices, by lowering switching fields, lowering the response times, and increasing endurance [22].

2.4 Ferroelectric Materials

Ferroelectric materials can be generally classified according to their crystal structures. The most well-known class of ferroelectric materials is the perovskites, which have a general formula of ABO_3. Polarisation in perovskite ferroelectrics, like barium titanate ($BaTiO_3$, is caused by the displacement of the central Ti atom relative to the oxygen octahedron, resulting in a dipole moment [19], as illustrated in Figure 2.5.

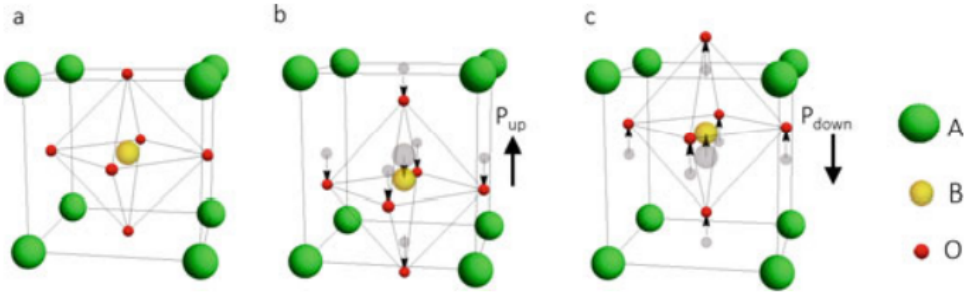

Figura 2.5: (a)Perovskite in the cubic phase. (b), (c) Atomic positions of PbTiO3 (A = Pb, B = Ti) in the ferroelectric tetragonal phase for up and down oriented polarisations. The Ti ion and oxygen octahedron are shifted in the same direction but the magnitude of the shift is greater for the oxygen octahedron [19].

2.5 HfO_2-based materials

Another important class of ferroelectric materials is HfO_2-based materials.The ferroelectricity of silicon-doped hafnium oxide (HfO_2) represents a recent discovery, first reported in 2011 [7]. HfO_2 has a complex phase diagram, which includes both stable and unstable phases.The stable centrosymmetric phases include the monoclinic phase (m-phase), the tetragonal phase (t-phase), and the cubic phase (c-phase), illustrated in Figure 2.6. The ferroelectricity in HfO_2 is attributed to the formation of an orthorhombic phase with non-centrosymmetric displacement, which allows for spontaneous polarisation [7].

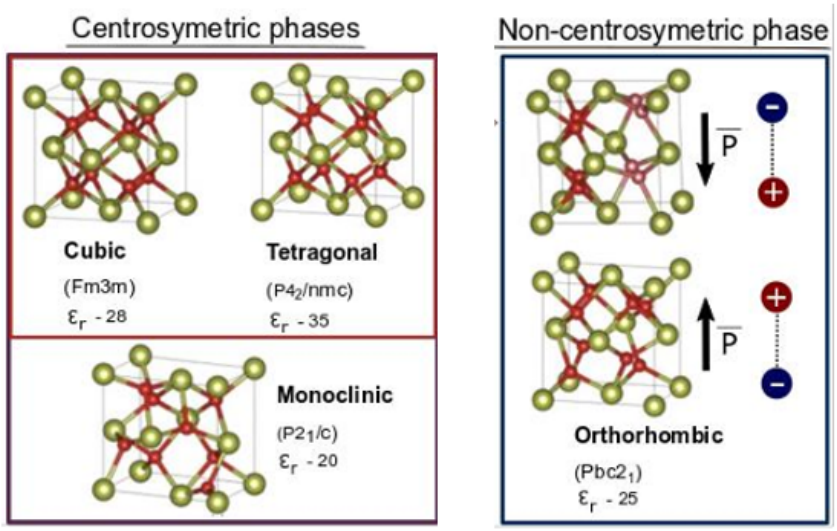

Figura 2.6: HZO phases[7].

In particular, there are three orthorhombic phases: orthorhombic I (o-phase), orthorhombic II (o-II phase), and polar orthorhombic III (f-phase). Crystallization into a non-centrosymmetric structure is induced by high-temperature annealing combined with specific pressure conditions. The transition to the orthorhombic phase from the tetragonal phase takes place during cooling [7], as illustrated in Figure 2.7.

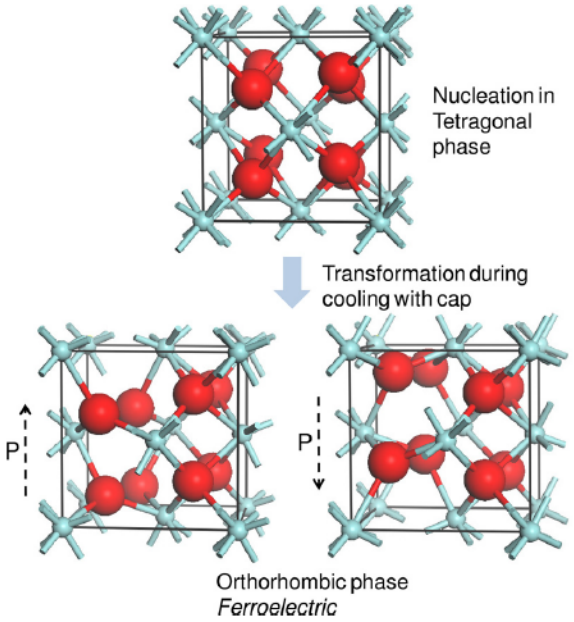

Figura 2.7: Orthorhombic HfO_2 Pbc21[7].

It has been demonstrated that doping HfO_2 with ZrO_2 significantly reduces the phase transition temperature from the monoclinic phase to the tetragonal phase in thin films, while also better stabilizing the orthorhombic phase [9]. For these reasons, Hafnium Zirconium Oxide (HZO) has received a lot of interest in recent years thanks to its compatibility with CMOS technologies. In addition since thin films of HZO exhibit robust ferroelectric properties, it makes them ideal for integration into advanced electronic devices. However, HZO exhibits strong ferroelectric properties only when treated under specific conditions. To achieve these properties, HZO must be deposited as a thin film, usually using atomic layer deposition (ALD) or chemical vapour deposition (CVD). The key factors determining its ferroelectric behaviour are:

- **Thickness:** HZO films with thicknesses ranging from 5 to 30 nanometres show optimal ferroelectric properties. Thicker films may lose their ferroelectric properties because of stress and strain effects[7].
- **Annealing:** Post-deposition annealing is required to induce the orthorhombic phase, which enables ferroelectricity.Annealing temperatures typically range from 400°C to 600°C, which promotes phase change while maintaining the material's structural integrity [27].
- **Composition:** The ratio of hafnium to zirconium significantly impacts the material's properties. A 1:1 ratio ($Hf_{0.5}Zr_{0.5}O_2$) is commonly employed to get a broad window of ferroelectricity [27].

HZO offers various advantages compared to traditional perovskite ferroelectrics (such as $BaTiO_3$):

- **CMOS Compatibility:** HZO can be integrated into standard CMOS (complementary metal-oxide-semiconductor) fabrication processes, since it requires a lower annealing temperature to induce orthorhombic phase (< 450°C). This compatibility is essential for scaling down ferroelectric devices to the nanoscale dimensions employed in current electronics [7].
- **Thermal Stability:** HZO preserves its ferroelectric properties at higher temperatures. This stability is crucial for applications in environments with variable thermal conditions [31].
- **Scalability:** HZO thin films can be deposited over large areas with uniform thickness. This scalability enables consistent device performance and manufacturing capabilities. [29].
- **Low Leakage Currents:** HZO exhibits lower leakage currents, making it suitable for non-volatile memory applications where data retention is critical [30].

Based on these features, HZO is an excellent material for next-generation electronic devices, providing significant improvements over standard perovskite ferroelectrics.

2.6 Ferroelectric Non-volatile Memory Devices

Ferroelectric memories exploit the unique features of ferroelectric materials to store data in a non-volatile way, meaning they can mantain information even when power is removed. Figure 2.8 shows the three primary forms of ferroelectric memories : Ferroelectric Random Access Memory (FeRAM), Ferroelectric Field-Effect Transistor (FeFET), and Ferroelectric Tunnel Junction (FTJ).
FeRAM operates similarly to Dynamic Random Access Memory (DRAM), however it achieves non-volatility by using a ferroelectric layer rather than a dielectric layer. In FeRAM, the polarisation state of the ferroelectric material represents binary data (0 or 1). FeRAM offers various advantages consisting of low power consumption, fast write and read speeds, and high endurance. These characteristics make FeRAM suitable for applications in embedded systems, smart cards, and different devices for consumers [13].
Instead FeFETs integrate a ferroelectric layer into the gate stack of a field-effect transistor. The polarisation state of the ferroelectric layer modulates the conductivity of the channel, allowing data storage. FeFETs combine the non-volatility of ferroelectric materials with the scalability and high-speed performance of standard transistors. This makes them promising candidates for next-generation non-volatile memory technologies employed in IoT and embedded artificial intelligence applications [32].

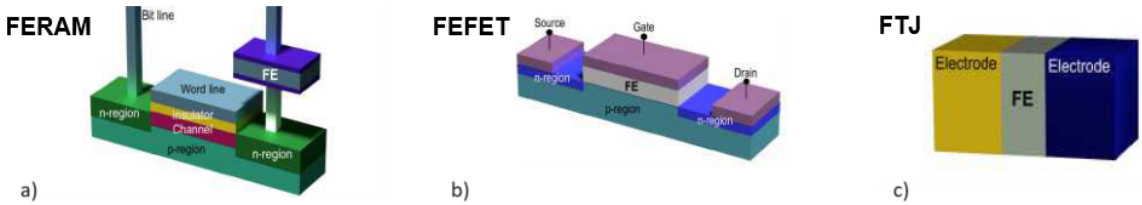

Figura 2.8: Ferroelectric memories [22].

Figure 2.8 (c) shows a model of FTJ. In that case the tunneling effect in ultra-thin ferroelectric films is used to create non-volatile memory devices. An FTJ consists of a thin ferroelectric layer sandwiched between two metallic electrodes [20]. The polarisation state of the ferroelectric layer influences the tunneling probability of electrons across the junction, allowing the device to switch between high and low resistance states 2.9. FTJs offer high density, low power consumption, and the potential for multi-level data storage, making them attractive for advanced memory applications [23].

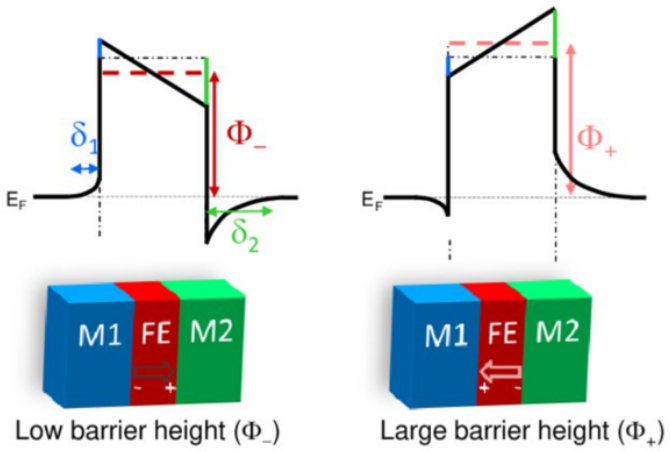

Figura 2.9: Ferroelectric tunnel junction [11].

Hafnium zirconium oxide (HZO) is particularly well-suited for FTJs due to its excellent ferroelectric properties and compatibility with existing semiconductor technology. The use of HZO in FTJs enables the development of high-density, low-power memory devices that can be easily integrated into modern electronic circuits. The ability of HZO to maintain ferroelectricity at nanoscale dimensions is crucial for the scalability of FTJ-based memory technologies [21].

2.7 Application of FTJ as artificial synapses

Ferroelectric Tunnel Junctions (FTJs) have emerged as promising components for neuromorphic computing systems, offering greater efficiency compared to current architectures. In these systems, which operate similarly to the human brain, FTJs can be used to model artificial synapses,whose information transfer and processing functions are similar to those of biological synapses.
An FTJ works by changing its resistance state through the application of an electric field, which effectively modulates the tunnelling current. This characteristic allows FTJs to mimic synaptic plasticity, a fundamental mechanism through which biological synapses increase or decrease in response to activity. By adjusting the polarisation state of the ferroelectric layer, FTJs are capable of producing multiple resistance states, enabling the implementation of synaptic weights that are essential for learning and memory functions in neuromorphic systems[14].

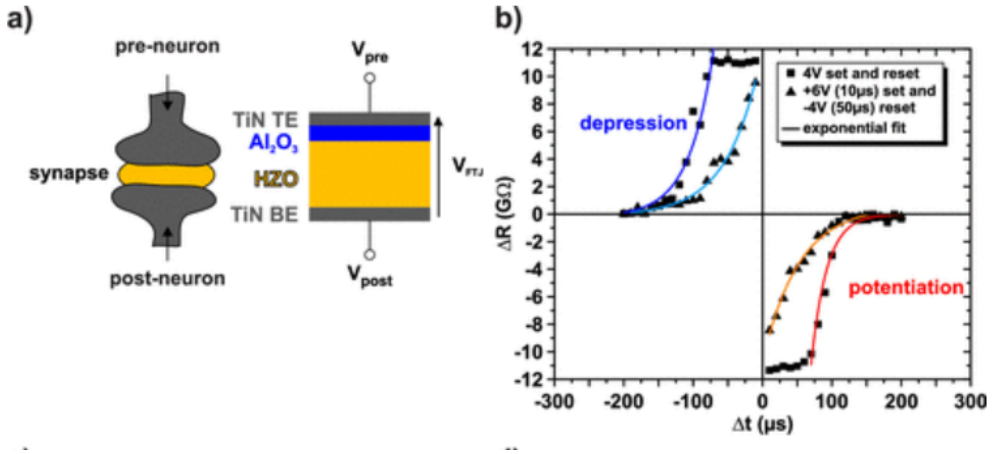

Figura 2.10: (a) Schematic comparison between a biological synapse with pre- and post-neuron connection and the FTJ used in this work. (b) Measured spike-timing-dependent plasticity (STDP) curves. The resulting resistance of the FTJ is a function of the time delay Δt between pre- andpostneuron action potentials leading to an increased or decreased resistance of the FTJ that represents a weakening or strengthening of the synapse. [14]

The ability of FTJs to operate at low power and their scalability to nanoscale dimensions make them ideal for large-scale integration in neuromorphic architectures. In addition, the non-volatility of FTJs implies that synaptic weights are kept even when the device is powered off, which is crucial for energy-efficient computing [34].

2.8 Imprint phenomenon

Among the different performance and reliability parameters, one stands out as the main topic of this thesis project: imprint. The phenomenon of imprint in ferroelectric memories, especially those based on hafnium zirconium oxide (HZO), is a significant challenge affecting device reliability.
Imprint refers to the undesired shift in the polarisation state VS voltage curve of a ferroelectric material, resulting in a shift of the coercive voltage (Vc). Notably, this phenomenon does not exhibit symmetric behavior, as seen in the Figure 2.11. For the positive imprint, so when the memory is programmed in the up state, the shift is more pronounced towards negative voltage values, corresponding to Vc^{-}. Conversely, in the case of negative imprint, when the memory is programmed in the down state, the shift that needs to be considered is relative to Vc^{+}, as it is more significant towards positive voltage values.

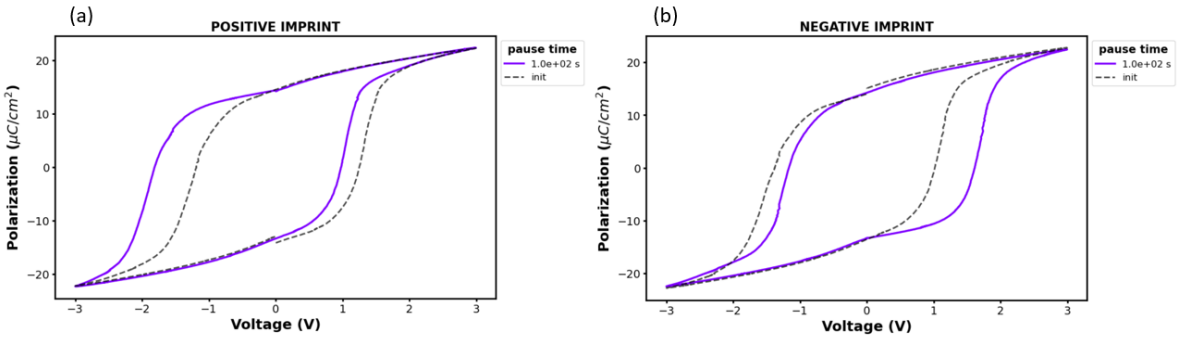

Figura 2.11: Positive imprint (a) and negative imprint (b).

This polarisation-voltage shift impacts the operational stability and retention characteristics of ferroelectric memory devices, such as Ferroelectric Random Access Memory (FeRAM), Ferroelectric Field-Effect Transistors (FeFETs), and Ferroelectric Tunnel Junctions (FTJs).
The imprint phenomenon in HZO-based ferroelectric devices is primarily attributed to charge trapping and material defects. The root cause for imprint can be categorized into three models: redistribution of mobile charges in the dead layer by depolarisation fields , domain pinning caused by oxygen vacancies and charge trapping and de-trapping in the interfacial layer [24]. When a ferroelectric memory device is subjected to prolonged electric fields or high temperatures, charges can become trapped at defect sites such as oxygen vacancies. These trapped charges produce internal electric fields that oppose the external electric field, causing a shift in the polarisation state [40].
Several studies have identified that the movement and stabilisation of oxygen vacancies are crucial in the imprint phenomenon [24]. Oxygen vacancies, particularly at the interfaces and grain boundaries, can stabilise specific polarisation states, resulting in an imprint. This can be observed in the increased activation barrier for domain generation and development following thermal treatment, which can be reduced by reversing the polarisation with additional electric pulses[10].
Electrical measurement and simulations experiments provided some significant findings about the imprint behaviour of HZO-based ferroelectric devices. For instance, baking experiments on ferroelectric capacitors and FeFETs reveal that the coercive voltage shift (ΔVc) is strongly dependent on temperature and initial polarisation state. These shifts can be attributed to charge detrapping and retrapping processes influenced by thermal and electrical stress [8].
Understanding the mechanics of charge trapping and defect migration, as well as implementing proper mitigation techniques, is essential for improving the reliability of operation of these advanced memories.

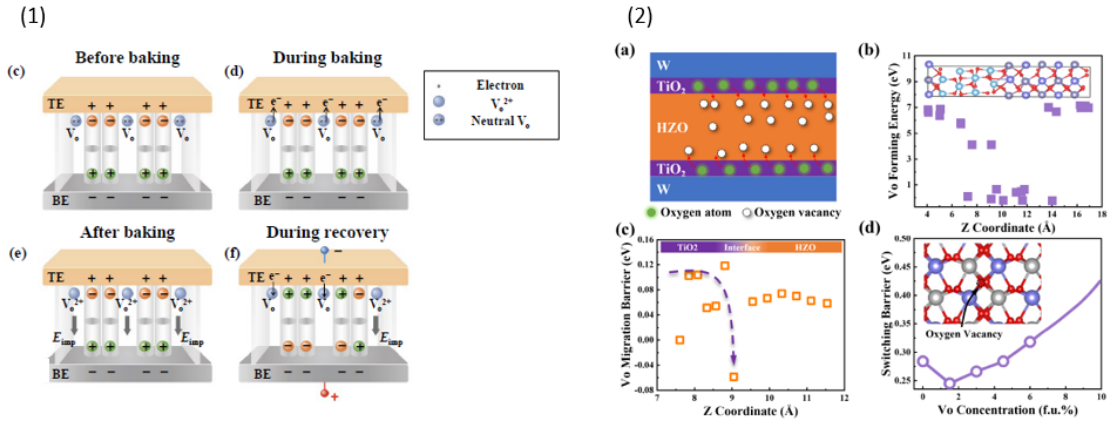

Figura 2.12: Imprint mechanism [24],[10].

Several strategies have been investigated to minimise the imprint in HZO-based ferroelectric devices. One effective approach is the modulation of oxygen vacancy concentration through interface engineering. For example the addition of a TiO_2 interfacial layer (visible in Figure 2.13 on the right), has been demonstrated to reduce the concentration of oxygen vacancies, improving the ferroelectric properties while reducing the coercive field. This results in better endurance (up to 10^{10}) and reliability of the memory [10].
A different strategy is to exploit post-deposition annealing in an oxygen-rich environment to occupy oxygen vacancies and stabilise the proper ferroelectric phase. This method maintains the polarisation state well, reducing the imprint effect through minimising charge trapping locations. [24].
Finally, there are techniques for recovering from imprint. Higashi et al. [40] demonstrated that the imprint recovery can be achieved by applying specific electrical pulses that reverse the trapped charges. In particular, using triangular pulses can successfully restore the polarisation state, reducing the imprint effect. This recovery process involves the reorientation of polarisation domains and the release of trapped charges, which restores the device's original performance characteristics.

2.9 Internship objectives

The main objective of this internship was to implement measurement protocols and then apply them by using the Keithley 4200 parameter analyser and a probe station, in order to analyse the current and voltage across ferroelectric memory devices. The goals of this internship included the following steps:

1. **Definition of the imprint protocol**: Initially, a signal sequence was defined to accurately evaluate the imprint contribution. For the positive imprint (upward programming), the shift relative to V_c^- was evaluated, while for the negative imprint, the shift of V_c^+ was analyzed.

2. **Validation of the protocol**: The protocol was subsequently transcribed into Python, adopting Keithley 4200 conventions, as this equipment is controlled by Python code. Finally the protocol was tested to ensure its reliability and accuracy.

3. **Study of imprint recovery**: The imprint recovery procedure was investigated and confirmed in order to ensure reliable imprint measuring results.

4. **Analysis of the imprint on various samples**: Samples characterized by different technological processes and structures were analyzed, and then the imprint effect was studied. In particular the evaluation of imprint was conducted on different samples as well as the same device under various stress levels.

5. **Endurance and polarisation state analysis**: The endurance and polarisation states of each sample were measured and examined in order to determine their relationship with the technological parameters of the analysed samples.

6. **Differential equations for imprint phenomenon**: In the end differential equations describing the imprint phenomena were defined and discretized using the finite difference method. This step is necessary to later define a hardware configuration that simulates imprint behavior in software such as Cadence.

For all the measurements presented in chapter 4, Keithley 4200 Parameter Analyzer, equipped with 4225-PMU (Pulse Measurement Unit) and coupled with two 4225-RPM (Remote Amplifier/Switch) modules, was used. Keithley 4200 is an advanced instrument that provides complete electrical characterization, including DC, I-V, and C-V measurements, with precise control and measurement capabilities. The 4225-PMU enables high-speed, high-accuracy pulse measurements with a current resolution of 75 nA. The two additional 4225-RPM modules further enhance the system's capabilities by offering four additional low-current ranges, providing sensitivity down to tens of pA. The 4225-RPM also reduces cable capacitance effects and allows automatic switching between the 4225-PMU, 4210-CVU, and other SMU modules installed in the chassis, enabling the operator to select the most suitable instrument for each measurement task without the need for re-cabling.

Figura 2.13: Keithley 4200 parameter analyzer and 4225-RPM modules.

Capitolo 3

Methodology

3.1 Fabrication process

The measurement protocols, presented in this chapter, were applied on various samples, each defined by different technological parameters, to investigate the effects of these parameters on the samples' performance and reliability. The results of these measurements, discussed in the next chapter, focus on three samples (Figure 3.2) that were made at the INL laboratories using the following methods:

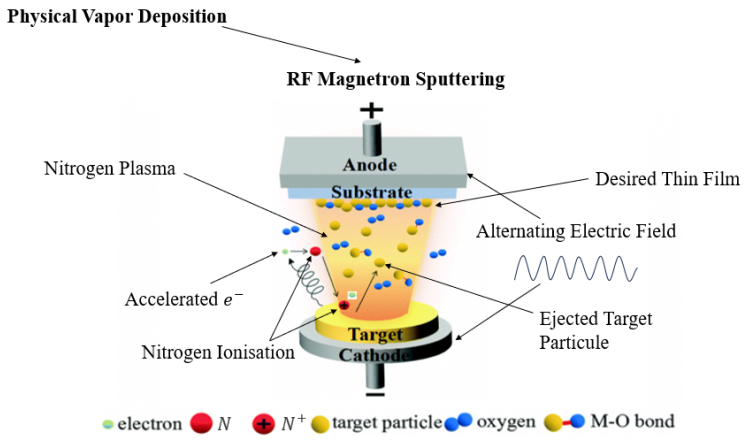

Figura 3.1: RF Magnetron Sputtering.

Deposition:
After cutting the silicon substrates into 1.0x1.0 cm² pieces, the surfaces were cleaned to remove residual dust, organic contaminants, and native oxide before the next deposition. The cleaning approach consisted of using acetone to remove grease and an isopropanol bath with an ultrasonic cleaner to remove any residual contaminants and acetone residuals. The deposition was then performed using a Physical Vapour Deposition (PVD) technique known as Radio Frequency (RF) Magnetron Sputtering, which is shown in

Figure 3.1. In this process, an alternating electric field is applied between a negatively charged target (cathode) and an anode, which is part of the chamber configuration that completes the electrical circuit and is connected to the positive terminal of the RF power supply.
The RF power energizes free electrons within the chamber, producing collisions with neutral nitrogen (or argon) atoms and ionizing them, resulting in a plasma. This plasma is then directed to the target material, removing atoms from it. These atoms migrate across the chamber and deposit on the substrate, generating a thin layer[39].

Bottom Electrode Oxidation:
A key objective of this internship was to investigate the effect of oxidizing the bottom TiN layer on the ferroelectric characteristics of HZO from an electrical point of view, particularly on the imprint phenomenon.
The reason for this oxidised TiN layer is that the literature generally states that adding an oxide layer (or interfacial layer) to ferroelectric memories can significantly improve device reliability besides the improvement of performance and longevity. For example the inclusion of TiO_2 interfacial layers in HZO ($Hf_{0.5}Zr_{0.5}O_2$) ferroelectric thin films resulted in a 30% reduction in coercive field. This reduction is the result of oxygen injection by the TiO_2 layers, which reduces the concentration of oxygen vacancies. As a result, the thin film's ferroelectricity increases, and the device's reliability improves [10].
Two oxidation methods were used for this purpose: O_2 plasma oxidation and ozone (O_3) oxidation. The O_2 plasma oxidation procedure required the injection of oxygen gas into a chamber containing the samples, resulting in an increase in pressure. Plasma produced by the ionisation of oxygen molecules, when RF energy is applied, is rich in reactive oxygen species. During its interaction with the sample surfaces, it induces oxidation or other surface changes.
For the ozone oxidation process, two samples were placed in a device that emits UV light to generate ozone. The UV radiation breaks down oxygen molecules (O_2) into oxygen atoms (O), which then combine with other oxygen molecules to form ozone (O_3). This generated ozone was used for oxidation by reacting with the samples' surfaces [39].

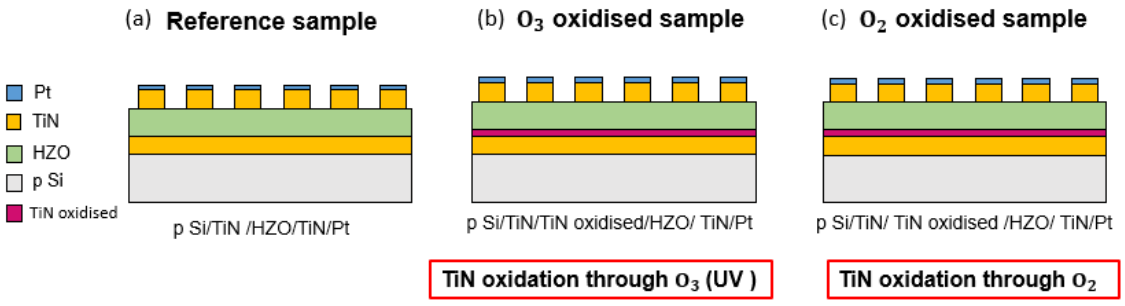

Figura 3.2: Analyzed samples.

3.2 Electrical characterization

The electrical characterization, focused on evaluating the performance and reliability of the samples, is the key point of this thesis. This characterization was carried out at the microscopic level using a Keithley 4200 parameter analyzer and a probe station at room temperature. Different protocols were used to obtain information about the electrical properties of the samples. The measurements performed include polarisation-voltage measurements using the positive-up-negative-down (PUND) technique, endurance measurements, and imprint measurements. The electrical characterization was conducted using a manual probe station, where the samples were kept in a closed environment and the electrical contact was made with two tungsten-tip probes. The voltage was applied by grounding one probe at the top electrode of the device, while the other probe was placed on the common bottom electrode where the voltage was applied, as illustrated in Figure 3.4. The various parameters were acquired on a single capacitor structure, where the Pt layer was used as the electrical contact.

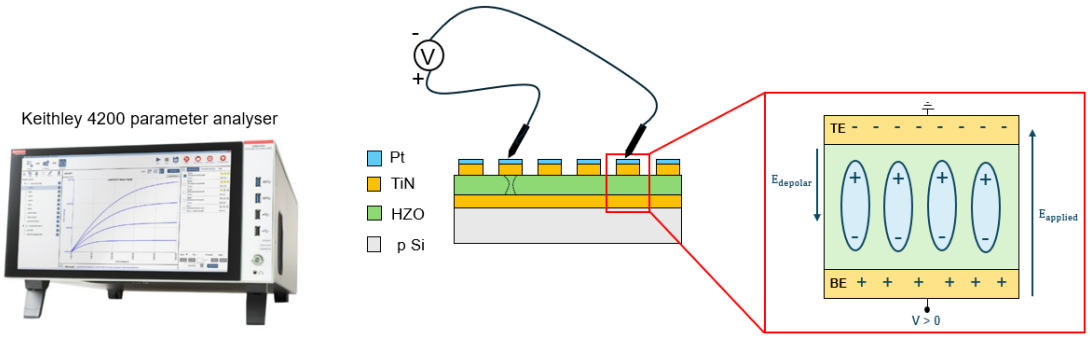

Figura 3.3: Measurement set up.

3.2.1 PUND measurement

The PUND (Positive-Up-Negative-Down) measurement is a fundamental technique used in the electrical characterization of ferroelectric materials and devices, proposed by Scott et al. in 1988 [38] to measure ferroelectric polarisation. It provides a more accurate analysis compared to simpler methods like the PN measurement by eliminating certain undesired effects, such as leakage current and non-switching components (i.e. displacement currents), resulting in a more reliable and precise hysteresis curve.
The PUND method involves applying a sequence of voltage pulses to a ferroelectric capacitor and measuring the resultant current, which consists of three main components: switching current, leakage current, and capacitive current.

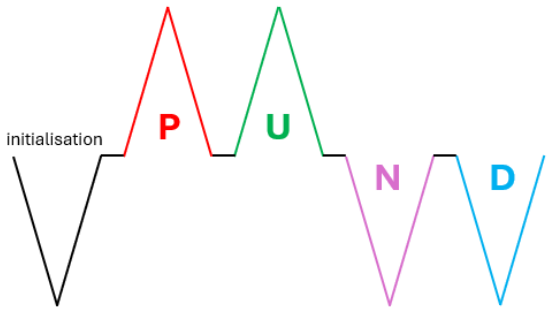

Figura 3.4: PUND protocol.

Initialization Pulse (First Down Peak):
This pulse aligns the polarisation state of the ferroelectric material. It essentially 'resets' the material, providing a consistent starting point for the measurement.

Positive Pulse (Second Peak : P):
The following pulse is applied in a positive direction, and the current measured includes both the switching and leakage current. The switching current corresponds to the change in polarisation, while the leakage current is caused by the movement of charge carriers through the material.

Positive Pulse (Third Peak : U):
Another positive pulse follows, with the primary goal of measuring the leakage current alone. This pulse helps in the isolation and quantification of the leakage component, which is then subtracted from the total current collected during the previous positive pulse to provide a more accurate evaluation of the material's real switching behaviour.

Negative Pulse (Fourth Peak : N):
The fourth peak is a negative pulse that measures both the switching and leakage currents. This step is similar to the second peak but in the negative direction.

Negative Pulse (Fifth Peak : D):
The final negative pulse is used to evaluate the leakage current only. By subtracting this leakage component from the total current measured during the previous negative pulse, the real polarisation change can be estimated.

By removing the leakage current and other non-switching contributions, the PUND measurement provides a more precise hysteresis curve, highlighting the intrinsic ferroelectric properties of the material.
The polarisation state is determined by integrating the current over time and removing the leakage current, resulting in a more accurate hysteresis loop. The following equations are used to extract the hysteresis loop:

$$\bar{D} = \varepsilon_0 \bar{E} + \bar{P} = \varepsilon_0 \varepsilon_r \bar{E} \tag{1}$$

where $\bar{D}$ is the displacement vector and ε_r is the relative dielectric constant.Considering that the current is defined as dQ/dt, the charge can be expressed as a function of the displacement vector D :

$$Q = \int I\,dt = \int_S \bar{D} \cdot d\bar{S} \tag{2}$$

where $d\bar{S}$ is the surface crossed by current I in time δt.

$$\bar{D} = \frac{1}{S} \int I\,dt \tag{3}$$

For the case of pulses P and U:

$$\bar{P} = \frac{1}{S} \int_0^{t_{pulse}} [I(P) - I(U)]\,dt = \frac{1}{S} \left(\int_0^{t_{pulse}} I(P)\,dt - \int_0^{t_{pulse}} I(U)\,dt \right) \tag{4}$$

From equation (1), D can be expressed as a function of the polarisation:

$$\bar{D} = \varepsilon_0 \bar{E} + \bar{P}(P) - [\varepsilon_0 \bar{E} + \bar{P}(U)] \tag{5}$$

$$\bar{D} = \bar{P}(P) - \bar{P}(U) \tag{6}$$

As previously explained, the pulse P includes the current response due to the switching of ferroelectric domains and additional leakage current. The second upward pulse U is exclusively due to leakage currents. In the ideal case:

$$D_{PU} = P_{PU,ferroelectric} \tag{7}$$

polarisation $P(t)$ at time t is given by:

$$P(t) = \frac{1}{A} \int_0^t I(t')\,dt' \tag{8}$$

where:

- $P(t)$ is the polarisation at time t,
- $I(t')$ is the measured current at time t',
- A is the area of the capacitor.

In particular to calculate both the polarisations from the measured currents, the following formulas are used:

$$P^{+} = \frac{1}{S} \int I_{P-U}(t)\, dt + k_1 \tag{9}$$

$$P^{-} = \frac{1}{S} \int I_{N-D}(t)\, dt + k_2 \tag{10}$$

where:

- I_{P-U} is the current difference between P and U.
- I_{N-D} is the current difference between N and D.
- k_1 and k_2 are constants.

The impact of the PUND measurement technique on the hysteresis cycle is significant.This kind of measurement results in a less sharp and more precise hysteresis curve which better reflects the material's real ferroelectric behaviour.

3.2.2 Endurance test

The endurance is defined as the maximum number of programming cycles that the memory can tolerate before breakdown occurs, leading the HZO to lose its dielectric characteristics. This type of test for such FeCaps devices begins by creating a short circuit to access the bottom electrode through the breakdown process, as shown in Figure 3.5. To achieve this connection, a voltage of 10 V was applied to induce breakdown in both electrodes. Subsequently, one of the probes was moved to another electrode to establish the top electrode of the capacitor to be analyzed.
This step provides a clear path for current flow and precise data collection.

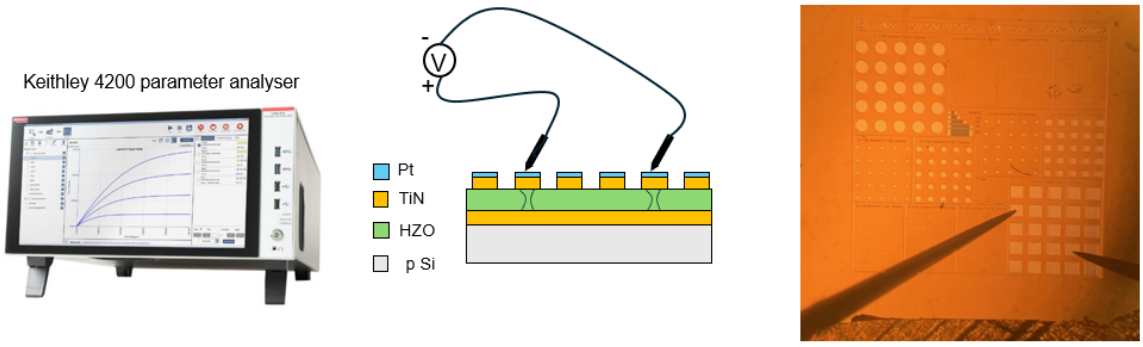

Figura 3.5: Access to the bottom electrode.

To program and erase the content of the memory, a PE (Program-Erase signal illustrated in red in Figure 3.6) signal is used.The signal consists of two voltage pulses that write and erase data within the ferroelectric material.

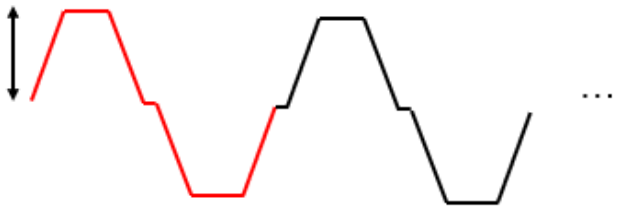

Figura 3.6: PE signal.

To evaluate the endurance,a specific number of PE cycles (indicated in red in Figure 3.6) are applied, then the ferroelectricity of the memory is measured by PUND measurements.
Typically, a voltage of around 3 V is used, but it can go up to 4 V, for the analyzed samples. The applied bias and pulse frequency significantly influence the material's stress; higher biases and lower frequencies generally make greater stress.
The endurance of the material, referring to the maximum number of programming cycles before breakdown occurs, is an important parameter. The maximum endurance for each analyzed sample goes up to 10^7 cycles, which is relatively small compared to other HZO samples in the literature, where endurance can reach 10^12. The endurance graph can be categorized into four distinct phases, visible from Figure 3.7 :

Wake-Up Effect:
Initially, the polarisation is not well-defined, with small changes in Pr^+ and Pr^-. This phase represents the initial conditioning of the material.

Good Regime:
The material reaches a stable state with constant Pr^+ and Pr^- values, indicating reliable switching. This phase indicates the memory device's optimal performance and stability.

Fatigue:
As cycles rise, both Pr^+ and Pr^- begin to degrade, with Pr^+ decreasing and Pr^- increasing. This represents the beginning of material fatigue, when the memory device loses the ability to maintain distinct polarisation states,because stressing the material over the repeated cycles causes defects in the HZO structure.

Breakdown:
At some point, the material loses its ability to maintain separate polarisation states, indicating the end of its useful life. This phase is characterised by a significant decline in performance and reliability.

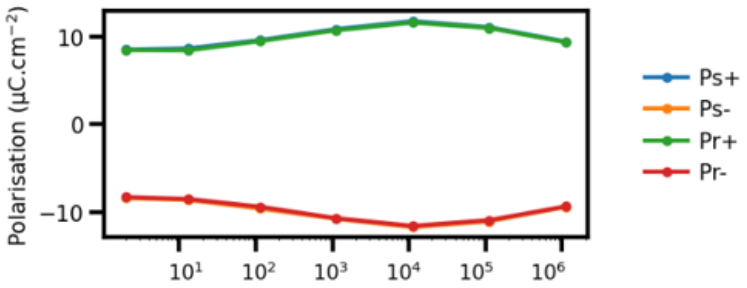

Figura 3.7: Endurance (Sample 1, V = 2.5 V).

The analysis of endurance test results allows for the identification of the correlation between technological parameters and the electrical properties of the memory. These tests provide critical information on the material's performance under electrical stress, allowing for the optimisation of both material composition, the technological parameters and operating conditions in order to optimise reliability and performance. The PUND (Positive-Up-Negative-Down) measurement, in particular, is essential for evaluating the material's switching behavior and endurance, which are critical for ensuring reliable memory operation over extended periods.

3.2.3 Imprint measurement

One of the objective of this research was to develop a protocol for measuring the phenomenon of imprint, which refers to the shift of the hysteresis loop when a memory is programmed into a specific state and left in that state for an prolonged period.This protocol is explained in detail in the current Chapter.
Positive imprint occurs when the memory is "up" polarised, whereas negative imprint

Measurement type	Frequency
PE Cycles	23 kHz
PUND Measurements	1 kHz
Imprint protocol	370 Hz

Tabella 3.1: Frequency of PE cycles, PUND measurements and imprint protocol (with $t_{pause} = 50\ \mu s$)

occurs when the memory has been programmed in the "down" polarisation state.
First of all, to program the memory state, a positive or negative voltage must be applied to the bottom electrode, as shown in the Figure 3.8, while the top electrode is used as a ground reference.

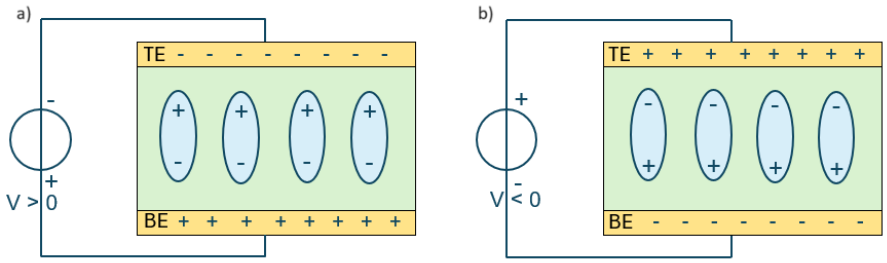

Figura 3.8: FE capacitor : Programming the "up" (a) and programming the "down" state (b).

In particular, by applying a positive voltage it is induced an "up" polarisation, while a negative voltage induces a "down" polarisation.
Before measuring the imprint, the sample was subjected to a "wake up" procedure, which induces ferroelectric properties in the sample. This process involves executing a certain number of PE cycles at a specific voltage, according to the sample's endurance graph.

To measure both positive and negative imprint in various samples, a protocol was developed, as depicted in Figure 3.9. A Python code was written to apply a sequence for the positive imprint measurement followed by negative imprint protocol to the electrodes, with varying pause durations to evaluate the imprint (i.e., the shift of the hysteresis loop) over different time intervals.

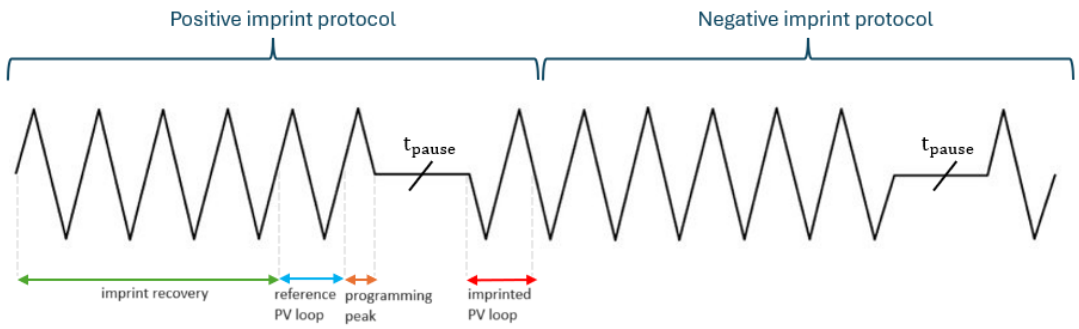

Figura 3.9: Imprint protocol (positive and negative imprint measurement)

For both the positive and negative imprint protocols, a preliminary sequence, indicated by the green arrow in Figure 3.9, is required for recovery for the imprint.
The purpose of this cycling process is to remove the imprint and recenter the PV loop on the axes, as will be explained in the next section.
Following this cycling, the PN (Positive-Negative) signal is applied for positive imprint (NP for negative imprint), as highlighted by the blue arrow.
This signal is used to evaluate the reference PV loop by integrating the switching current, as also described in the PUND measurement paragraph. However, in the case of the imprint protocol using the PN signal, the contribution of the leakage current is not excluded, therefore the resultant PV loop will be sharper than the one obtained through the PUND measurement.
Since these PV loop references are obtained after the recovery for the imprint, whether for negative or positive imprint, they should coincide and symmetric with respect to the axes' center.
For each pause time, both the reference PV loop and the shifted PV loop after the pause are measured. The latter is defined by applying the NP signal for positive imprint (PN for negative imprint), as indicated by the red arrow in Figure 3.9.
The imprinted PV loop will shift to the left in the case of positive programming (highlighted in Figure 3.9 by the orange arrow), while for negative programming, the shift will be to the right, as demonstrated in Figure 3.10.
Figure 3.10 shows the evolution of the PV loop for a pause time ranging from 1 µs to 200 s for both positive and negative imprint.

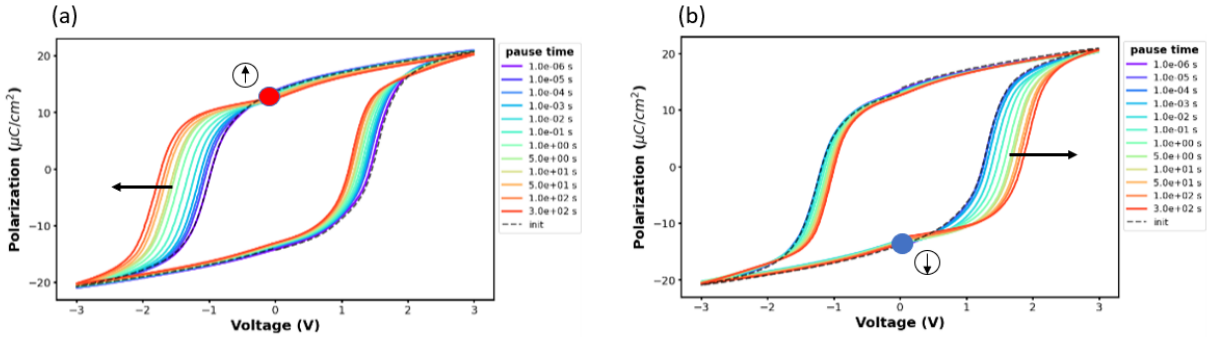

Figura 3.10: Positive (a) and Negative (b) imprint.

Regarding the pause signal, it has been defined as a 4-segment signal according to the Keithley Parameter Analyzer rules. The amplitude is always 0 V, while the duration (dt) of each segment varies depending on the value of t_{pause}.
Specifically, for t_{pause} values lower than 100 s, the pause segment is divided into four segments, each lasting $t_{pause}/4$. However, when t_{pause} exceeds 100 s, a pause signal consisting of four equal segments, each with a fixed duration of 25 s, is looped a number of times equal to $nb_{pause} = (t_{pause}/100\ \text{s})$.

```
    #Building the pause signal

        if t_pause <= 100 :
            pause            = self.device.build_pause(dt = t_pause/4 ,m_enabled = 0)
            pause_Seq        = self.device.pm.create_Seq(pause)
            dt_value = t_pause/4
            print(" pause signal dt is {} sec".format(dt_value))

        # when t_pause > 100 s we loop a pause signal with # a fixed duration equal to 100 s,
        # for nb_pause times

        else :
            pause            = self.device.build_pause(dt = 25,m_enabled = 0)
            pause_Seq        = self.device.pm.create_Seq(pause)
            nb_pause         = t_pause / 100


        #Building the positive imprint sequence

        applied = pd.concat([PN_cycle_wo_read,PN_cycle_w_read,Prog_Pos, pause,NP_read],
        ignore_index = True)
        applied_Seq = self.device.pm.append_Seq(PN_cycle_wo_read_Seq, PN_cycle_w_read_Seq)
        applied_Seq = self.device.pm.append_Seq(applied_Seq, Prog_Pos_Seq)
        applied_Seq = self.device.pm.append_Seq(applied_Seq, pause_Seq)
        applied_Seq = self.device.pm.append_Seq(applied_Seq, NP_read_Seq)

        #pause is a 4 segments signal (each one with a #duration equal to t_pause/4)
        #if t_pause <= 100 s
```

```
29
30          if t_pause <= 100 :
31              applied_SeqLoops = self.device.pm.generate_SeqLoops([1,2,3,4,5],
32              [nb_init_cycles-1,1,1,1,1])
33
34          #pause is a 4 segments signal (each one with a #duration equal to 25 s) looped nb_pause
35          #times if t_pause > 100 s
36
37          else :
38              applied_SeqLoops = self.device.pm.generate_SeqLoops([1,2,3,4,5],
39              [nb_init_cycles-1,1,1,nb_pause,1])
40
```

To estimate the actual contribution of the imprint effect, attention is directed not only to the graph showing the PV loop evolution under varying pause conditions but also to the evolution of the corresponding coercive voltages.
This voltage evaluation begins with the analysis of the switching current, whose peak corresponds to the maximum polarisation switching current hence corresponding to the coercitive voltage.
Given the asymmetry of the imprint phenomenon, the focus is on the variation of only the negative coercive voltage (V_c^-) for positive imprint, while for negative imprint, the shift in the positive coercive voltage (V_c^+) relative to the pause time is examined.

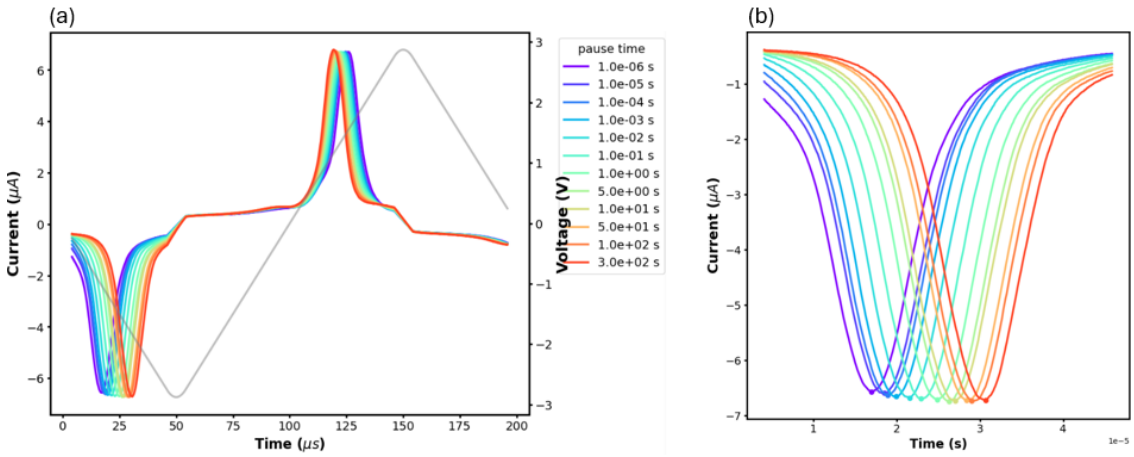

Figura 3.11: Switching current, applied voltage and coercitive voltage relation for the positive imprint.

As previously stated, this voltage is derived from the switching current. Figure 3.11 illustrates this concept for positive imprint. Graph (a) of Figure 3.11 shows the switching current corresponding to the NP signal used to assess the PV loop after the pause, with the V_c^- value being taken from the peak of the switching current at the negative peak, as highlighted in graph (b).
This V_c^- value (V_c^+ for negative imprint) is used to define the imprint contribution:

$$\text{Positive Imprint} = |Vc^-_{t_{pause}} - Vc^-_{ref}| = \Delta Vc^-$$

$$\text{Negative Imprint} = |Vc^+_{t_{pause}} - Vc^+_{ref}| = \Delta Vc^+$$

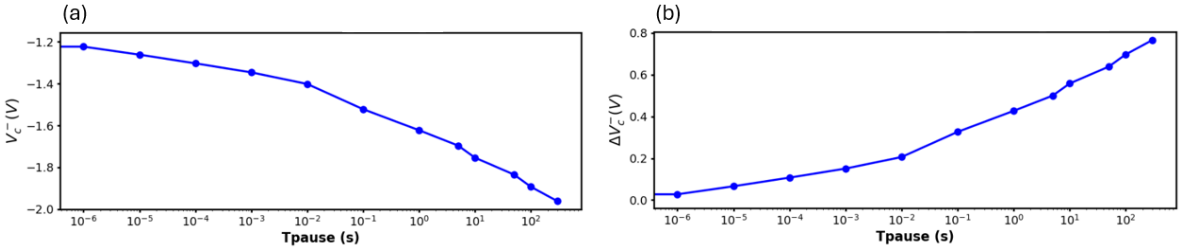

Figura 3.12: Vc^-_{ref} evolution with respect to t_{pause} (a) and positive imprint (b).

Figure 3.12 shows the graph of the coercive voltage (Vc^-_{ref}) evolution as the pause time varies (a). From the other side graph (b) illustrates the positive imprint, defined as the difference between this voltage and the initial coercive voltage measured before the pause, serving as reference voltage.

3.2.4 Recovery for the imprint

After validating the protocol, it was necessary to verify that the process used to recover the imprint was adequate.It was particularly important to ensure that, after these cycles, the following PV loop was exactly centred on the x y axis.
Several tests were conducted by varying either the amplitude of these cycles or the number of repeated PN (or NP, in case of negative imprint protocol) signals, since these methods are recommended as effective for a successful recovery from imprint in the literature [8]. The objective was to determine the optimal combination of these two parameters (indicated by the arrows in Figure 3.13) so that

$$E_{\text{imp}} = \frac{Vc^-_{\text{ref}} + Vc^+_{\text{ref}}}{2}$$

which represents the center of the hysteresis loop, was approximately zero.

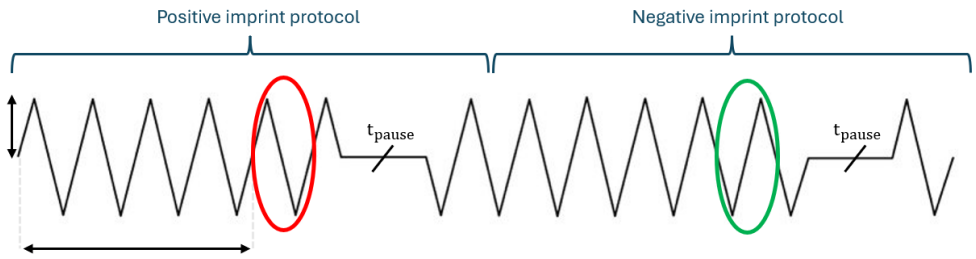

Figura 3.13: Recovery for the imprint.

If this condition ($E_{imp} \rightarrow 0$) is met, the reference PV loops circled in red and green in Figure 3.13, measured before the imprint, should be coincident and symmetric with respect to the origin of the axes, as shown in Figure 3.14.

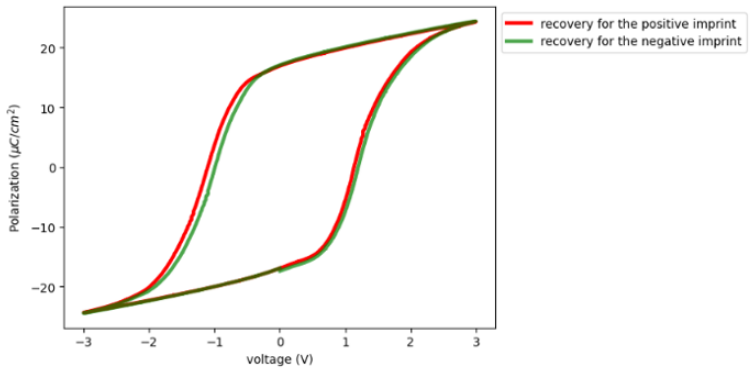

Figura 3.14: Reference PV loop after the imprint recovery.

3.3 Differential equations for the imprint phenomenon

Given the exponential trend observed in the imprint measurements, a bi-exponential fitting (exp2) was applied to the experimental data using MATLAB. This fitting helped define a differential equation that accurately describes the imprint phenomenon for both the positive and negative imprints.
This approach intended to define a differential equation that represents the imprint phenomenon, which could then be synthesized in Verilog. This allows the simulation of ferroelectric memories through the Cadence software, including the imprint behavior.
To be incorporated into these simulations, the imprint must be represented by a circuit configuration, defined starting from differential equations.

To derive a single differential equation that describes both V_c^- and V_c^+ with respect to time, a general form that encapsulates both behaviors is considered. Given that the

bi-exponential fitting that was conducted, the behavior of V_c^- and V_c^+ with respect to time can be described by a similar differential equation structure.
For V_c^- and V_c^+ the bi-exponential functions are :

$$V_c^-(t) = A_1 \exp(-k_{1-}t) + B_1 \exp(-k_{2-}t)$$

$$V_c^+(t) = A_2 \exp(-k_{1+}t) + B_2 \exp(-k_{2+}t)$$

To derive a single differential equation that can describe both V_c^- and V_c^+, a generic function $V(t)$ is introduced to switch between the parameters of V_c^- and V_c^+. However, since a single differential equation is required, the general form of a second-order linear differential equation that can encapsulate exponential decay is considered:

$$\frac{d^2V(t)}{dt^2} + (k_1 + k_2)\frac{dV(t)}{dt} + k_1k_2V(t) = 0$$

This equation assumes the form $V(t) = A\exp(-k_1t) + B\exp(-k_2t)$, where k_1 and k_2 are the decay rates.

Given the bi-exponential fitting for both V_c^- and V_c^+, the differential equation can be redefine to take into account both cases, but with different parameters. Therefore, the combined differential equation that can describe both V_c^- and V_c^+ is:

$$\frac{d^2V_c(t)}{dt^2} + (k_1 + k_2)\frac{dV_c(t)}{dt} + k_1k_2V_c(t) = 0$$

Where the parameters k_1 and k_2 will differ based on whether V_c^- or V_c^+ is being described. For practical implementation, it is necessary to substitute the appropriate k_1 and k_2 for each case.
In order to define the hardware configuration it is necessary to discretize the differential equation using the finite difference method. This approach approximates the derivatives with their finite differences.
Assuming a time step Δt, the second-order differential equation can be approximated as:

$$\frac{V(t+\Delta t) - 2V(t) + V(t-\Delta t)}{\Delta t^2} + (k_1 + k_2)\frac{V(t+\Delta t) - V(t-\Delta t)}{2\Delta t} + k_1k_2V(t) = 0$$

$$V(t+\Delta t) = \frac{2V(t) - V(t-\Delta t) - \Delta t^2\left((k_1 + k_2)\frac{V(t+\Delta t)-V(t-\Delta t)}{2\Delta t} + k_1k_2V(t)\right)}{1}$$

Finally the Verilog code is defined starting from this finite difference approximation.
This step is crucial for several reasons. First, correctly modelling the imprint phenomenon ensures that simulations closely mimic real-world behaviour, resulting in more reliable and predictable results. Second, integrating this model into Cadence software allows for complete testing and validation of memory under different kinds of conditions, including those caused by imprint.

Capitolo 4

Results

4.1 Measurements on the reference sample

This chapter presents the results of measurements performed with the previously described measurement protocols. The first sample analysed was the "classic" capacitor (reference sample), as detailed in Chapter 3 "Fabrication Process."

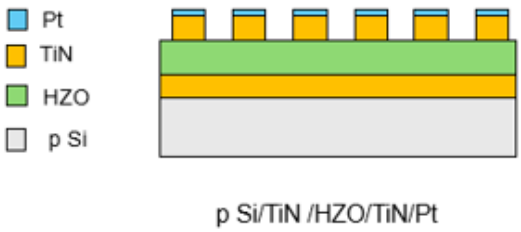

Figura 4.1: Reference sample.

For the measurements, electrodes with a diameter of 20 μm were used. Reducing the electrode size helps to minimize the number of imperfections and defects in the material. As a consequence smaller electrodes have a more uniform distribution of the electric field, resulting in a lower probability of premature breakdown and improved memory endurance.

4.1.1 Endurance test

Initially, breakdown was induced on a spare capacitor to establish contact with the bottom electrode. Following that, the endurance, or maximum number of programming cycles before breakdown occurs, was measured on other capacitor structures.
Voltage was applied to the bottom electrode, which was common to all memories, while the top probe, which is grounded, was placed on devices with a circular electrode of 20 μm diameter. The applied voltage was varied, as shown in Table 4.1, to find the optimal value for the memory to be awake, with good polarisation and endurance.

Voltage level	Electrode
2.5 V	A4 (20 μm)
3 V	A5 (20 μm)
3.5 V	A7 (20 μm)

Tabella 4.1: Voltage levels and corresponding electrodes for the endurance test.

The results are presented in Figure 4.2 for a voltage of 2.5 V, Figure 4.3 for 3 V, and Figure 4.4 for 3.5 V. Each figure includes the chronogram for various cycles (a), the endurance (b), and the PV loop obtained through PUND measurement (d) and PN measurement (c) (without removing the leakage current).

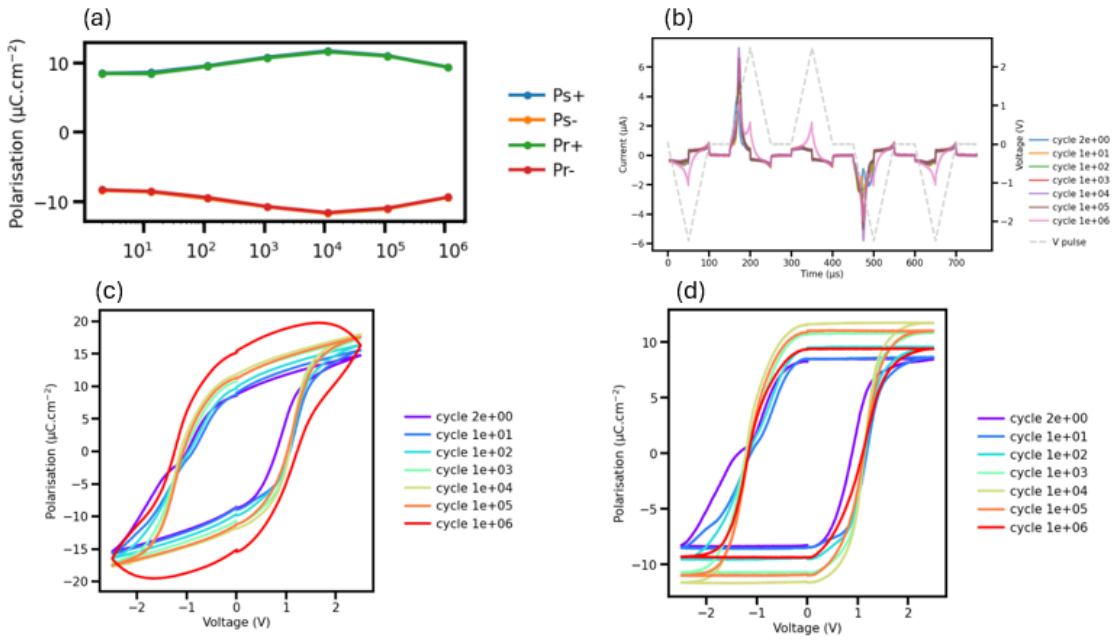

Figura 4.2: Chronogram(b), Endurance(a) and PV loop achieved through PN measurement (c), PV loop obtained with PUND measurement (d) for 2.5 V.

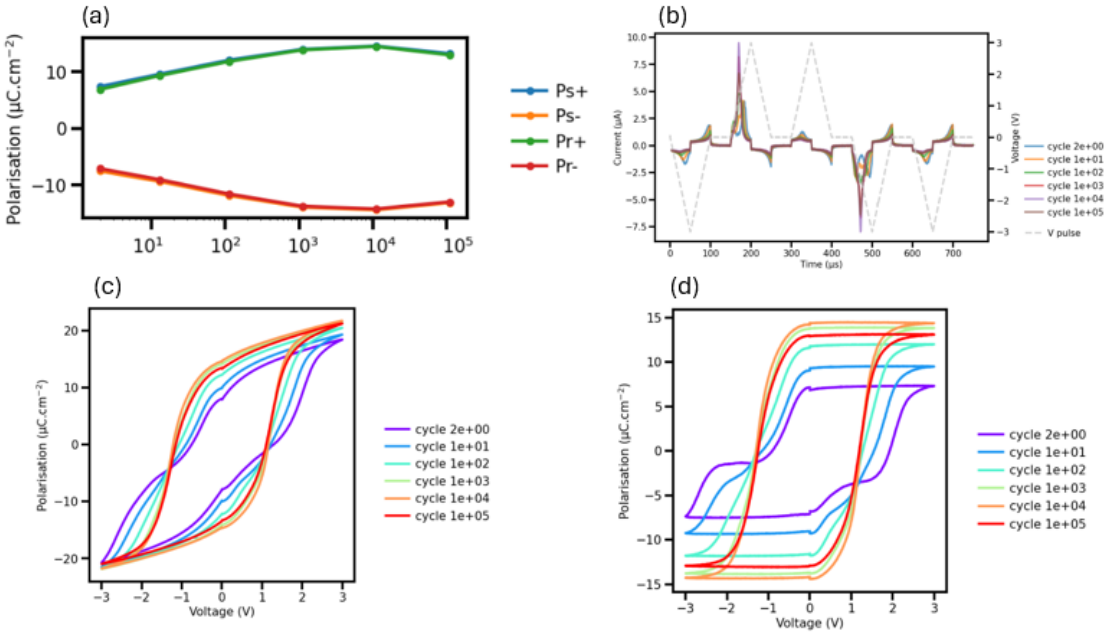

Figura 4.3: Chronogram(b), Endurance(a) and PV loop achieved through PN measurement (c), PV loop obtained with PUND measurement (d) for 3 V.

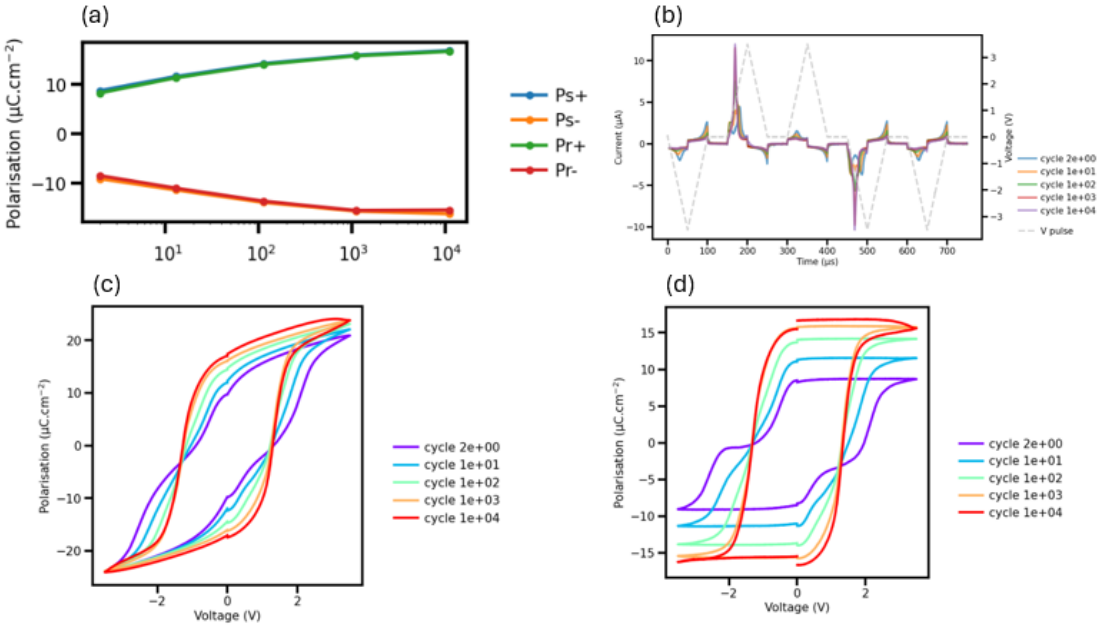

Figura 4.4: Chronogram(b), Endurance(a) and PV loop achieved through PN measurement (c), PV loop obtained with PUND measurement (d) for 3.5 V.

As the figures reveal, increasing the applied voltage reduces the endurance, resulting

in breakdown sooner. From one side higher voltages cause more domains to switch, increasing slightly the remnant polarisation and improving device performance in terms of data retention and stability. Conversely, the significant electric field accelerates the breakdown process by producing more charge traps and imperfections in the HZO layer. These defects accumulate over repeated cycling, leading to a reduction in the memory endurance.

4.1.2 Imprint measurements

To correctly evaluate imprint, it is necessary wake up the memory and induce ferroelectricity by applying a certain number of PE cycles at a specific voltage. To achieve this, the graphs acquired from the endurance test were examined to establish the optimal number of cycles required to awake the memory. It was decided to apply 10^3 cycles at 3 V before performing the imprint measurement, as the analysis of the endurance graphs indicated that these values were sufficient for the wake-up operation.

Voltage level (imprint protocol)	**Amount of cycles (wake up)**	**Electrode**
2.5 V	10^3	E3 (20 μm)
3 V	10^3	E3 (20 μm)
3.5 V	10^3	E3 (20 μm)
3 V	10^3	E6 (20 μm)
3 V	10^4	E6 (20 μm)
3 V	10^5	E6 (20 μm)

Tabella 4.2: Voltage levels and corresponding electrodes for the imprint measurements.

To study the imprint phenomenon, tests were conducted using the voltage values (for the imprint protocol) and the amount of PE cycles (for the wake up operation) specified in Table 4.2, with pauses ranging from 1 μs to 300 s, while for the recovery of the imprint, 10 cycles were applied at the same voltage used for the rest of the imprint protocol.

In general, the graphs show that all the measurements follow the same trend, more specifically the imprint follows a logarithmic trend over time. Particularly, the positive imprint is always greater than the negative imprint, as highlighted in Figure 4.5,suggesting that the increased stability of the up polarisation is probably due to a higher concentration of oxygen vacancies near the bottom electrode. When the positive voltage is applied to the bottom electrode these vacancies become positively ionized, altering the internal electric field and therefore stabilizing the up polarisation.

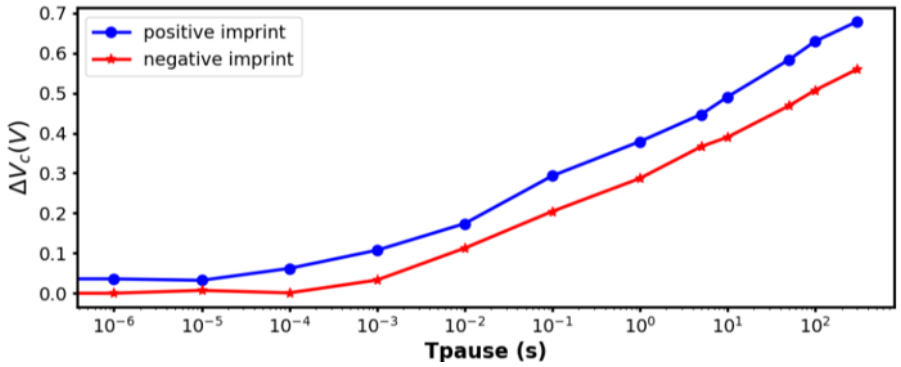

Figura 4.5: Positive imprint VS negative imprint.

The graphs in Figure 4.6 were produced to better illustrate the distinct contributions of imprint in each type of test and to study the impact of voltage and wake-up conditions on the imprint phenomenon.

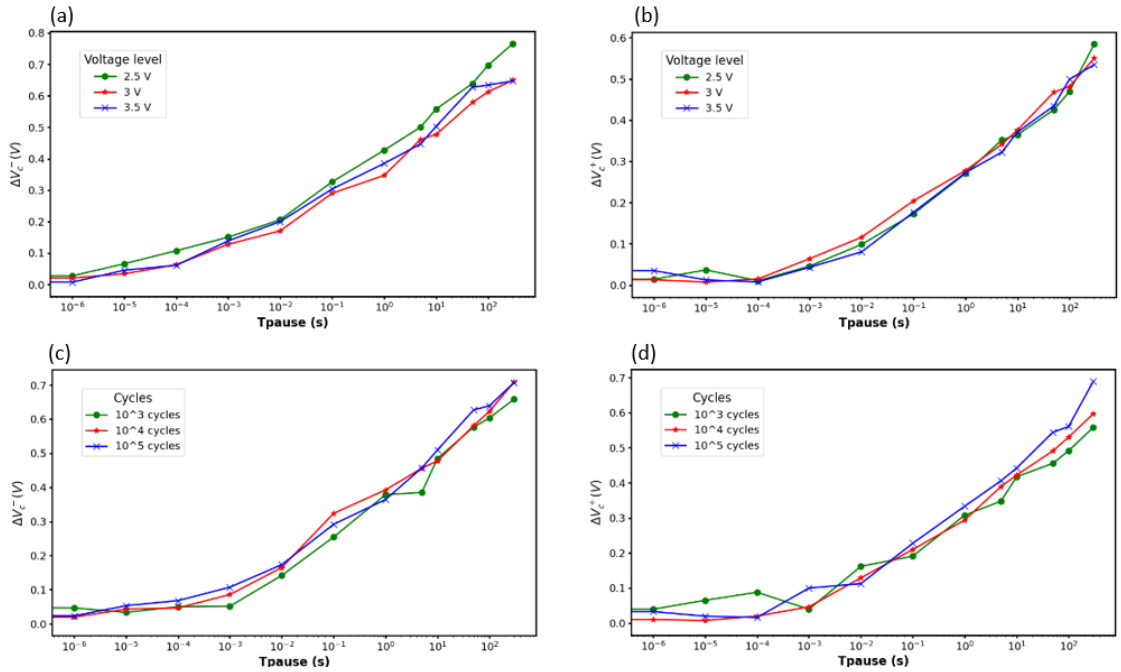

Figura 4.6: Positive imprint (a) and negative imprint (b) with respect to the variable applied voltage and fixed 10^3 wake up cycles; Positive imprint (c) and negative imprint (d) with respect to the variable wake up cycles and fixed voltage at 3 V.

As shown in the graphs in Figure 4.6, related to the reference sample, there are no clear impact between the imprint phenomenon and the applied voltage or the number of cycles used to wake up the sample. Indeed the trend of both positive and negative imprint remains relatively identical, regardless of the wake-up conditions or the voltage levels used for the signals. However, when examining graph (d), which represents the

negative imprint as a function of cycling, a slight increase in negative imprint is observed as the number of wake-up cycles increases. This suggests that, in this specific case, cycling may cause oxygen vacancies to move toward the top electrode, stabilising the down polarisation.

Another type of imprint test was conducted using different electrodes. Table 6.2 shows the first measurements, which involved varying both the voltage value for the wake-up operation and the imprint protocol signals. Similar to the previous case, a second set of measurements was performed by fixing the voltage (for both the wake-up and imprint protocol) and changing the number of PE cycles for the wake up operation. For the recovery of the imprint in this second test, 5 cycles were applied. This approach was used to investigate the consistency of the data shown in the previous figures.

Voltage level (wake up and imprint protocol)	**Amount of cycles (wake up)**	**Electrode**
2.5 V	10^3	C5 (20 μm)
3 V	10^3	B6 (20 μm)
3.5 V	10^3	C1 (20 μm)
3 V	10^3	B7 (20 μm)
3 V	10^4	B8 (20 μm)
3 V	10^5	C3 (20 μm)

Tabella 4.3: Voltage levels and corresponding electrodes for the imprint measurements.

Even in this second type of imprint test, the positive imprint contribution is slightly greater.

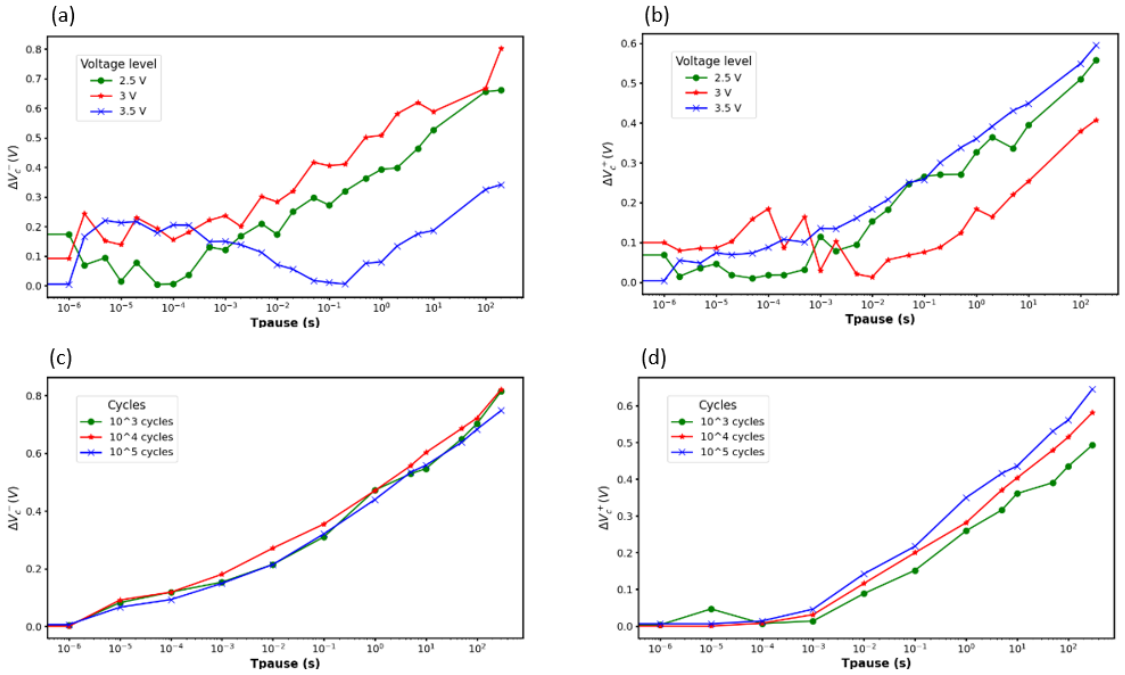

Figura 4.7: Positive imprint (a) and negative imprint (b) with respect to the variable applied voltage and fixed 10^3 wake up cycles; Positive imprint (c) and negative imprint (d) with respect to the variable wake up cycles and fixed voltage at 3 V.

As illustrated in the graphs in Figure 4.7, varying the voltage level does not result in a corresponding clear change in imprint. However, as observed in the previous case in Figure 4.6, increasing the number of wake-up cycles increases the negative imprint, while the positive imprint decreases slightly. This suggests that cycling causes the oxygen vacancies responsible for the imprint to migrate from the bottom electrode, where they are more concentrated, to the top electrode, leading to a reduction in the positive imprint and an increase in the negative imprint. imprint shows an opposite trend, with a slight decrease.
To confirm the consistency of these results Figure 4.8 illustrates the positive (a) and negative (b) imprint contributions for two different FeCaps from the same sample and PAD subjected to the same conditions (3 V and 10^5 cycles). This emphasises the reliability of the results, as the positive and negative imprint contributions are basically comparable.

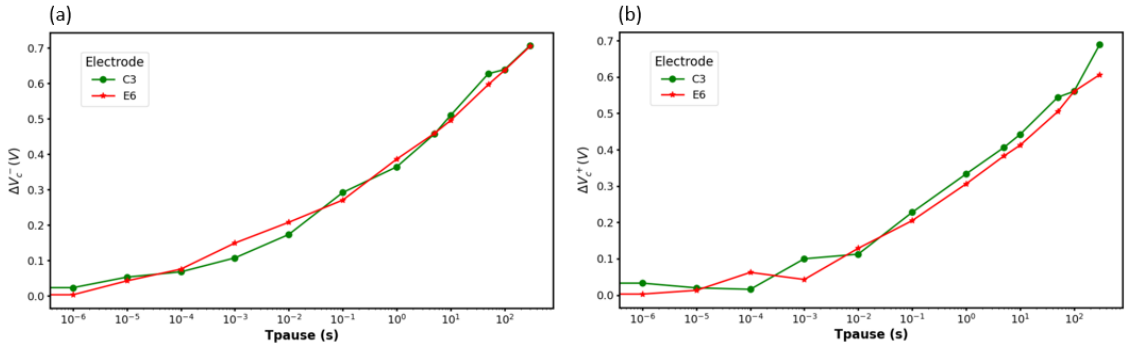

Figura 4.8: Positive imprint (a) and negative imprint (b) on different FeCaps when 3 V and 10^5 wake up cycles are applied.

4.2 Measurements on O_3 oxidised sample

The previous measurements were repeated on O_3 oxidised sample, illustrated in Figure 4.9, to evaluate the impact of the oxidized layer on reliability (imprint) and performance (endurance).

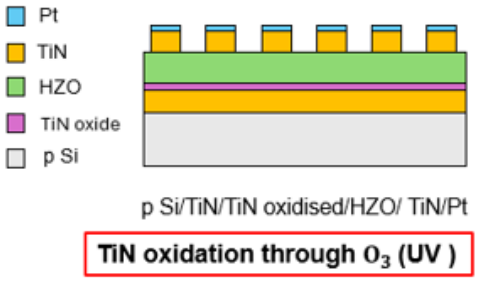

Figura 4.9: O_3 oxidised sample.

4.2.1 Endurance test

The first test conducted was the endurance test. After establishing contact with the bottom electrode through breakdown, the endurance test was performed, as described in Chapter 3 "Endurance test". Table 4.4 shows the voltages applied to devices with a diameter of 20 μm.

Voltage level	Electrode
2.5 V	A2 (20 μm)
3 V	A3 (20 μm)
3.5 V	A5 (20 μm)

Tabella 4.4: Voltage levels and corresponding electrodes for the endurance test.

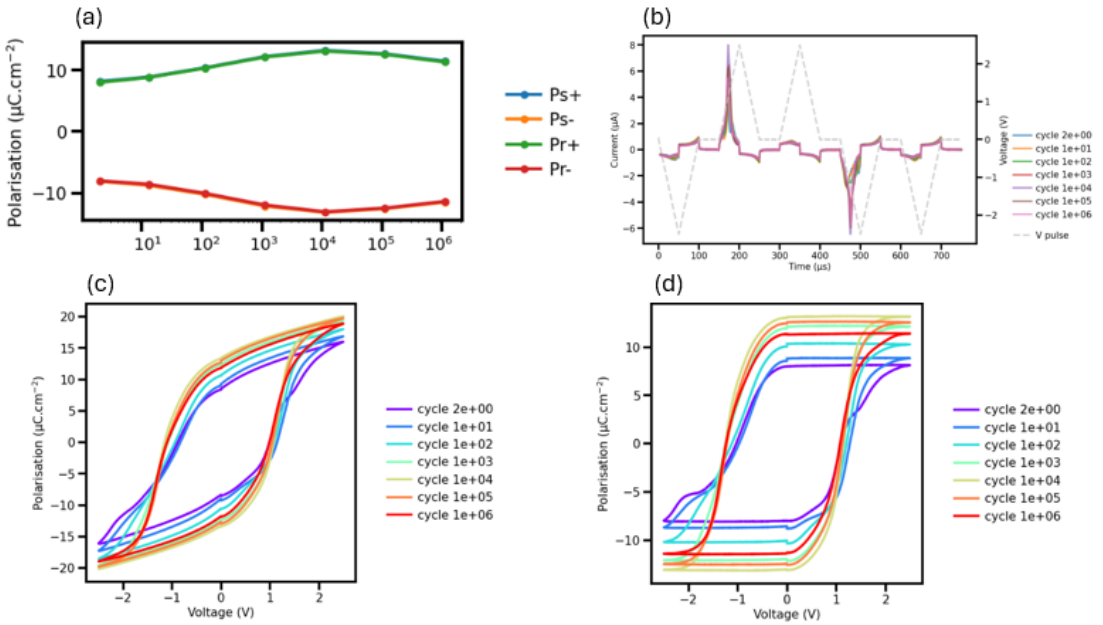

Figura 4.10: Chronogram(b), Endurance(a) and PV loop achieved through PN measurement (c), PV loop obtained with PUND measurement (d) for 2.5 V.

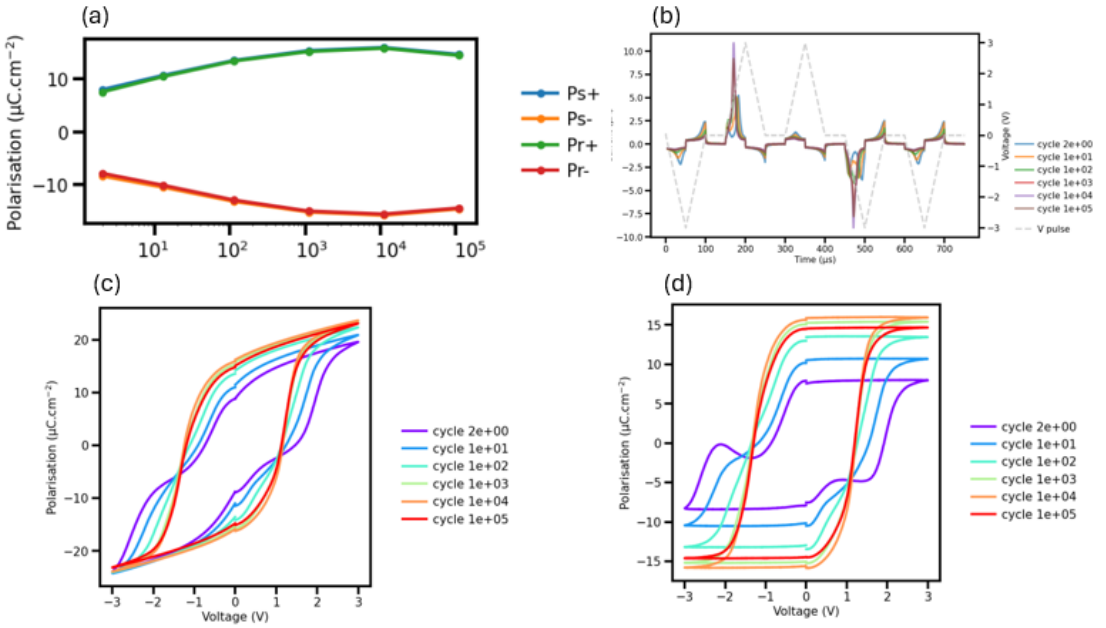

Figura 4.11: Chronogram(b), Endurance(a) and PV loop achieved through PN measurement (c), PV loop obtained with PUND measurement (d) for 3 V.

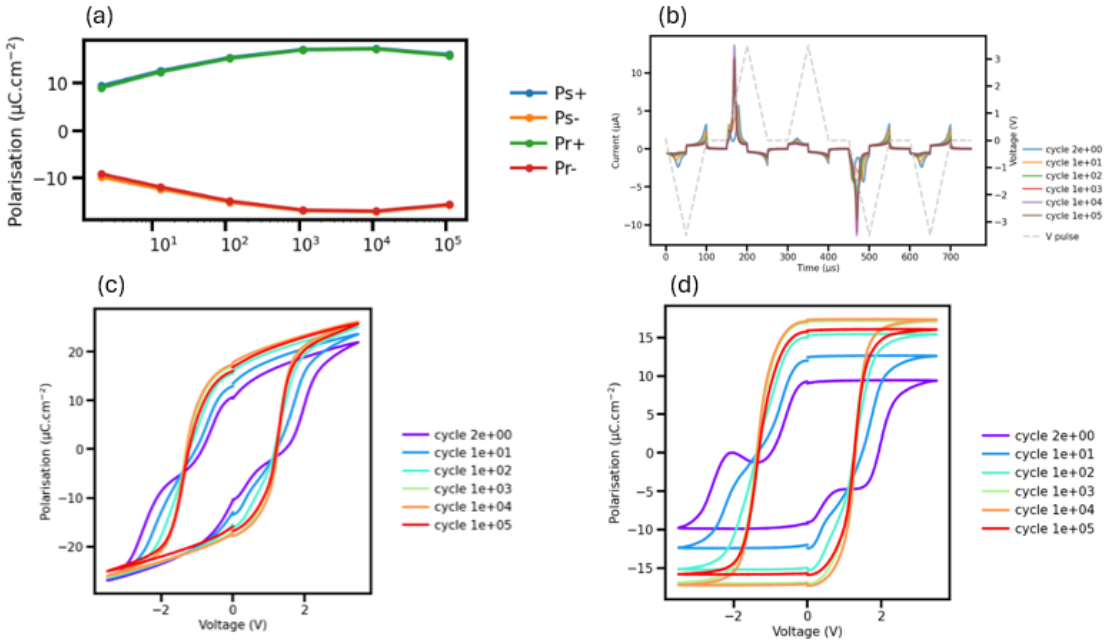

Figura 4.12: Chronogram(b), Endurance(a) and PV loop achieved through PN measurement (c), PV loop obtained with PUND measurement (d) for 3.5 V.

Figures 4.10, 4.11, and 4.12 show that the O_3 oxidised sample suggests the same considerations as the previous sample. Specifically, when the voltage increases, the remnant polarisation increases slightly while the endurance decreases.
However, in this case, both the remnant polarisation and the endurance at 3.5 V are slightly higher than the reference sample at the same voltage. This is because the additional layer of oxidized titanium results in a lower effective electric field across the HZO layer, reducing the overall stress experienced by the capacitor. The fact that this thin layer of titanium oxide, also known as a dead layer, leads to improved endurance suggests that it reduces the presence of oxygen vacancies and defects within the HZO layer.

4.2.2 Imprint measurements

The imprint measurement was conducted as described for the reference sample, with the same considerations and parameters. An initial wake-up operation was performed by applying 10^3 PE cycles at 3 V.

Voltage level (imprint protocol)	Amount of cycles (wake up)	Electrode
2.5 V	10^3	B7 (20 μm)
3 V	10^3	B7 (20 μm)
3.5 V	10^3	B7 (20 μm)
3 V	10^3	B8 (20 μm)
3 V	10^4	B8 (20 μm)
3 V	10^5	B8 (20 μm)

Tabella 4.5: Voltage levels and corresponding electrodes for the imprint measurements.

For studying the imprint phenomenon, tests were performed using the voltage values and number of PE cycles listed in Table 6.3. These tests included pauses ranging from 1 μs to 300 s. For imprint recovery, 10 cycles were applied at the same voltage used for the imprint protocol.

Overall, the graphs demonstrate that the imprint increases logarithmically over time, with the positive imprint always higher than the negative imprint,which is consistent with the observations made for the reference sample. The graphs in Figure 4.13 indicate the effects of voltage level and wake-up conditions on the imprint phenomenon.

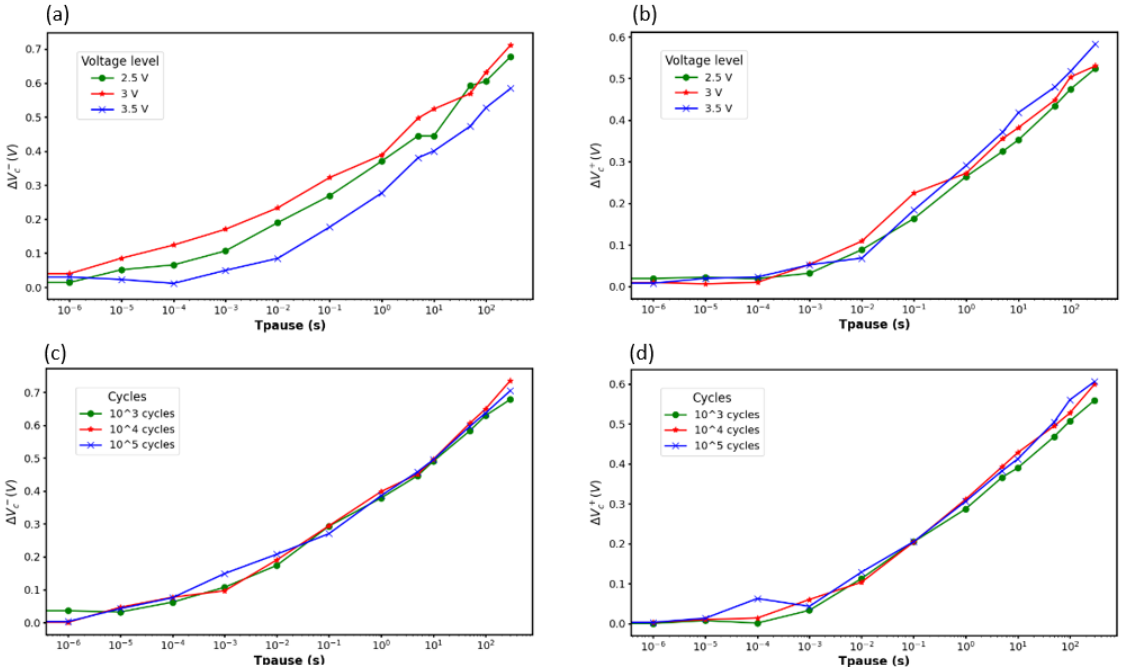

Figura 4.13: Positive imprint (a) and negative imprint (b) with respect to the variable applied voltage and fixed 10^3 wake up cycles; Positive imprint (c) and negative imprint (d) with respect to the variable wake up cycles and fixed voltage at 3 V

In this case, when the applied voltage increases, negative imprint increases slightly, as

shown in graph (b) of Figure 4.13, that means the down polarisation becomes more stable. However, this trend is not observed for the positive imprint. This is probably because a higher voltage causes more ionization of the oxygen vacancies at the top electrode, leading to a slight increase in the negative imprint, although the difference is minimal. On the other side, since the presence of the oxidized layer, there are less oxygen vacancies at that interface, so they do not significantly contribute to the imprint phenomenon. Finally, from graphs (c) and (d), it is possible to notice the positive imprint (c) remains roughly the same as the number of wake-up cycles increases. In contrast, the negative imprint shows a greater increase with more cycling. For the reference sample, it was assumed that oxygen vacancies were more concentrated at the bottom electrode. As a result, with increasing cycling, a more consistent positive imprint and a bigger change than the negative imprint were observed. This is probably due to the more significant movement of oxygen vacancies at the top electrode, considering the oxygen vacancies transitioning from a place with higher concentration to another one with lower concentration.
As a consequence, in the O_3 oxidized sample, the opposite trend is observed, since the concentration of oxygen vacancies is minimized at the bottom electrode. However, the positive imprint is still greater than the negative imprint, suggesting that in this case, the imprint is influenced not only by oxygen vacancies but also by the oxidized layer, which traps charges and stabilizes the up polarisation.

The imprint test was repeated on different electrodes, as done for the reference sample. The first test varied both the voltage values for the wake-up operation and the imprint protocol, as specified in Table 6.4. Similarly, a second test was conducted by keeping the voltage fixed for both the wake-up and imprint protocols while varying the number of PE cycles. For imprint recovery in this second test, 5 cycles were applied.

Voltage level (wake up and imprint protocol)	**Amount of cycles (wake up)**	**Electrode**
2.5 V	10^3	A6 (20 μm)
3 V	10^3	A7 (20 μm)
3.5 V	10^3	A8 (20 μm)
3 V	10^4	B1 (20 μm)
3 V	10^5	B2 (20 μm)

Tabella 4.6: Voltage levels and corresponding electrodes for the imprint measurements.

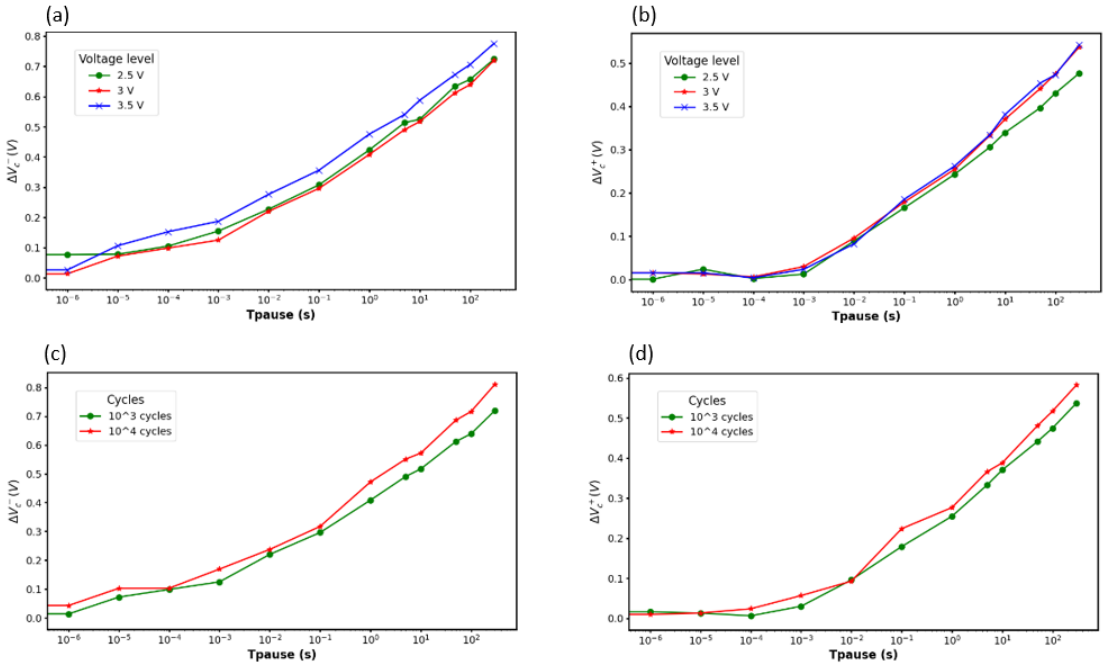

Figura 4.14: Positive imprint (a) and negative imprint (b) with respect to the variable applied voltage and fixed 10^3 wake up cycles; Positive imprint (c) and negative imprint (d) with respect to the variable wake up cycles and fixed voltage at 3 V.

The graphs in Figure 4.14, present trends similar to those observed in Figure 4.13,confirming the previous observations. This indicates that capacitors belonging to the same PAD, with the same dimensions and measurement conditions, show comparable behavior.

4.3 Measurements on O_2 oxidised sample

Finally, the same tests were also repeated on O_2 oxidised sample, where the oxidized titanium layer is made by using oxygen.

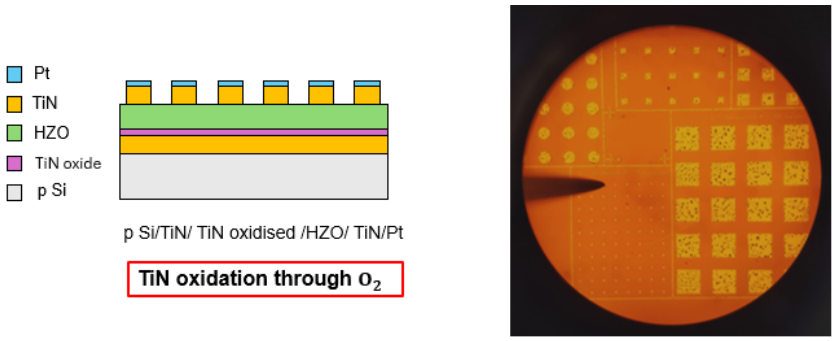

Figura 4.15: O_2 oxidised sample.

4.3.1 Endurance test

The voltage values used for the endurance test for O_2 oxidised sample are presented in Table 4.7.

Voltage level	Electrode
2.5 V	A6 (20 μm)
3 V	B2 (20 μm)

Tabella 4.7: Voltage levels and corresponding electrodes for the endurance test.

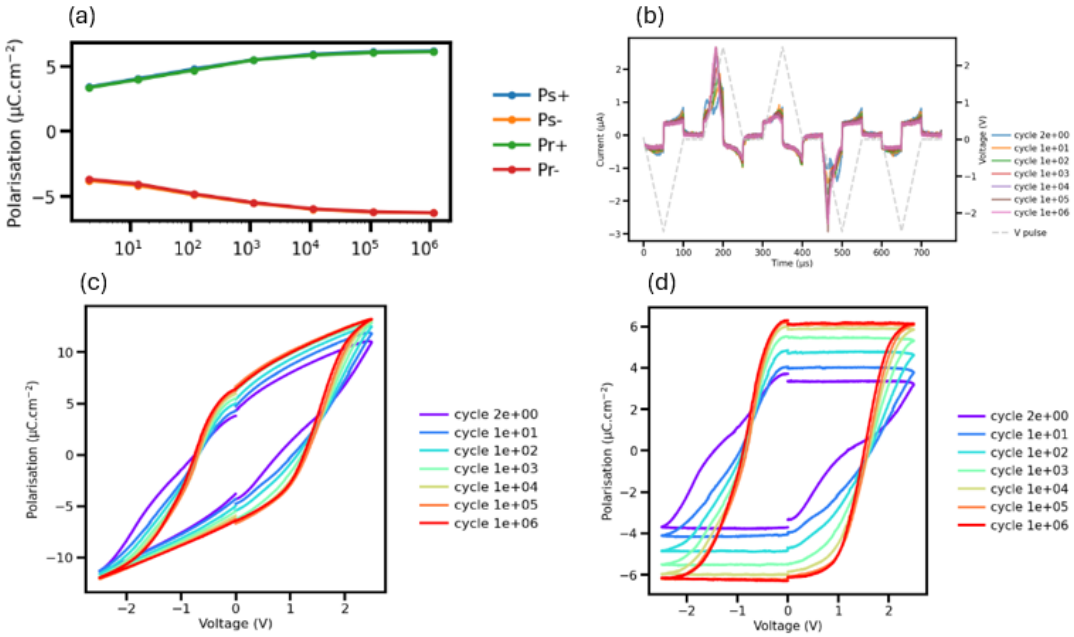

Figura 4.16: Chronogram(b), Endurance(a) and PV loop achieved through PN measurement (c), PV loop obtained with PUND measurement (d) for 2.5 V.

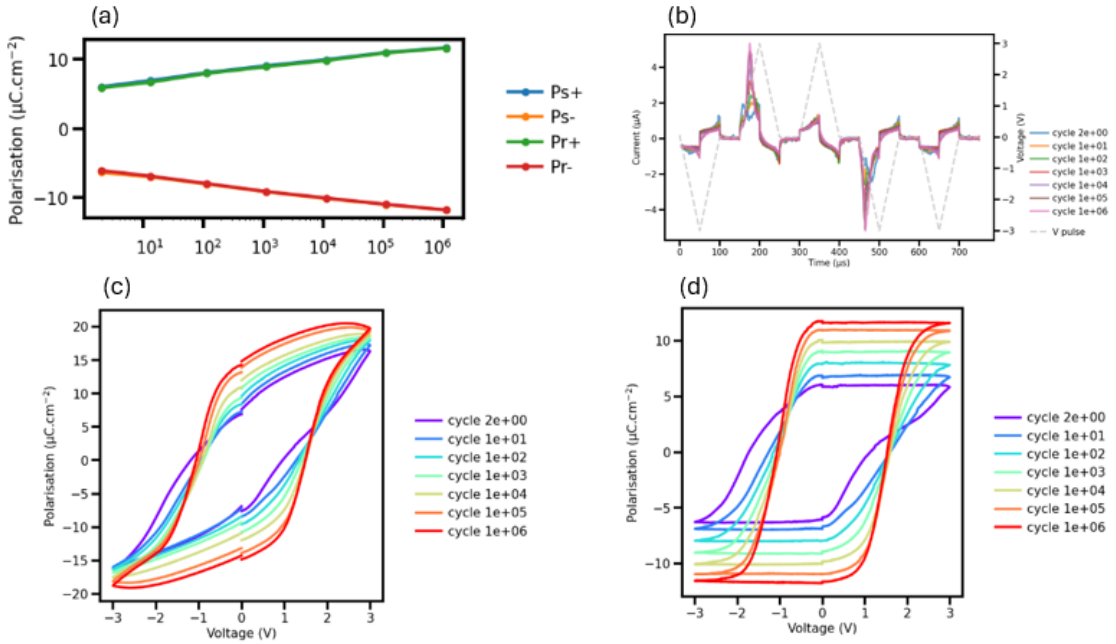

Figura 4.17: Chronogram(b), Endurance(a) and PV loop achieved through PN measurement (c), PV loop obtained with PUND measurement (d) for 3 V.

According to the results, increasing the applied voltage improves the remnant polarisation by promoting more extensive switching of ferroelectric domains. Additionally, the analysed endurance was higher compared to the previous two samples. In this case, the lower remnant polarisation, most likely as result of an incomplete wake-up process caused by insufficient voltage, resulting in the more pinched PV loops obtained through PN measurements, suggests that the additional layer of oxidized titanium in O_2 oxidised sample is larger than in the case of O_3 oxidised sample. Indeed, a too thick dead layer leads to a strong decreasement polarisation efficiency due to increased barrier effects at the interfaces, and it may also impact the capacitor's endurance by introducing potential degradation at the interfaces of the dead layer. To accurately investigate the impact of this layer, additional analysis are required, which can provide precise measurements of the nanometric thickness of the titanium oxide layer.

4.3.2 Imprint measurements

The imprint measurement was conducted in the same way as for the previous samples, using different electrodes and the parameters reported in Table 6.5. For the imprint recovery 5 cycles at the same voltage as the rest of the protocol were applied.

Voltage level (imprint protocol)	Amount of cycles (wake up)	Electrode
2.5 V	10^3	B3 (20 μm)
3 V	10^3	B4 (20 μm)
3.5 V	10^3	C2 (20 μm)
3 V	10^4	B8 (20 μm)
3 V	10^5	B5 (20 μm)

Tabella 4.8: Voltage levels and corresponding electrodes for the imprint measurements.

Figure 4.18 presents the graphs comparing the positive and negative imprints for various wake-up conditions and voltage levels.

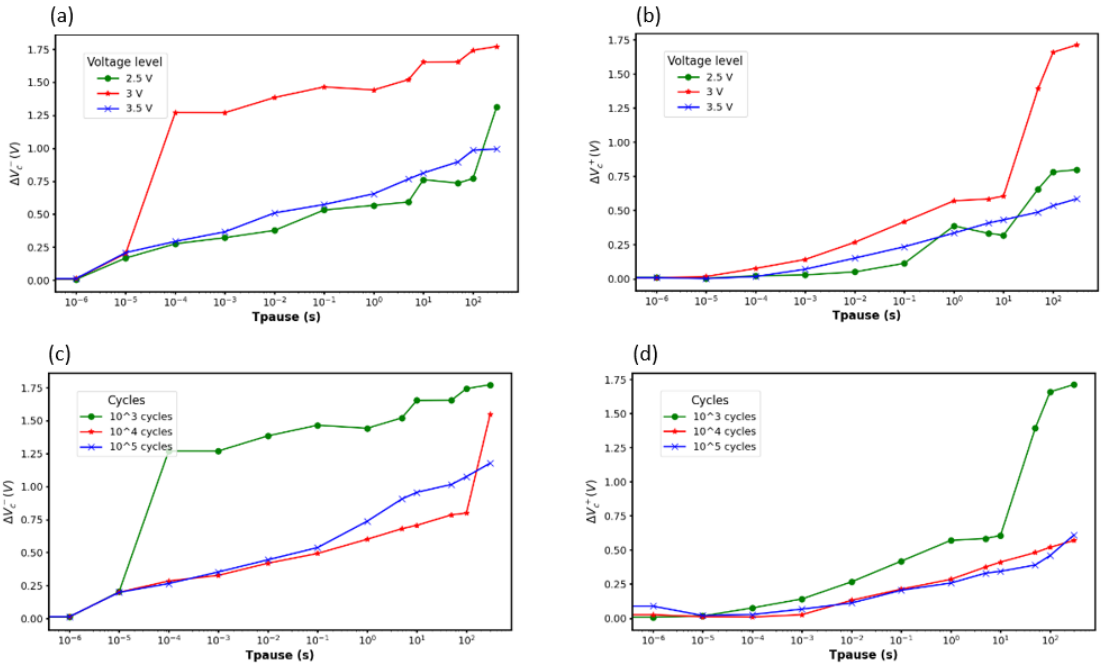

Figura 4.18: Positive imprint (a) and negative imprint (b) with respect to the variable applied voltage and fixed 10^3 wake up cycles; Positive imprint (c) and negative imprint (d) with respect to the variable wake up cycles and fixed voltage at 3 V.

As for the other two samples, also for the O_2 oxidized sample the positive imprint is consistently greater than the negative imprint, regardless of the applied voltage or wake-up cycles. Moreover, as visible from Figure 4.18, there is no clear relationship between imprint and either wake-up cycling or applied voltage. In particular, the highest imprint values ((c) and (d) in Figure 4.18) seem to occur at the lowest number of wake-up cycles. However, the PV loops for this electrode (B4 : 3 V and 10^3 wake up cycles) are quite pinched, suggesting that these conditions are insufficient to fully wake up the FeCap, making the imprint measurements for this case unreliable. In contrast, at higher wake-up cycles (10^4 or 10^5), the imprint is more regular and comparable across different conditions.

4.4 Impact of oxidized layer and oxygen vacancies

In order to identify how the oxidized layer affect the reliability of HZO-based ferroelectric memories, the following graphs representing the imprint in the three samples are shown. It is important to note that the reference sample has no oxidised layer, while the other two samples, O_3 oxidized sample and O_2 oxidized sample, have a small layer of oxidised TiN at the bottom electrode interface. This oxidized layer is believed to be thicker in the O_2 oxidized sample.
Figure 4.19 and Figure 4.21 show the comparison of imprint across three samples under various conditions.

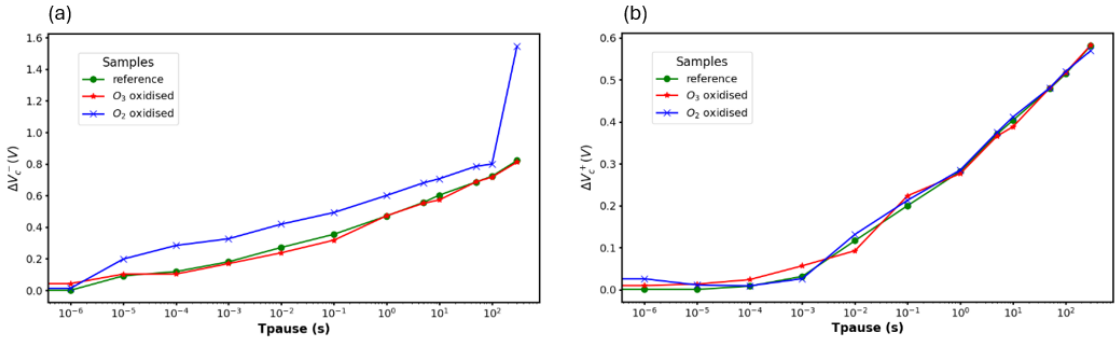

Figura 4.19: Sample 1 VS sample 2 VS sample 3 when 3 V and 10^4 cycles : (a) positive imprint ; (b) negative imprint.

The graphs in Figure 4.21 and Figure 4.19 show that O_2 oxidized sample, despite having an oxidized layer like O_3 oxidized sample, behaves differently. Except for the negative imprint (b) in Figure 4.19, where the imprint contribution is equivalent for all three samples, the O_2 oxidised sample often exhibits a stronger imprint than the other cases. This could be due to the thicker oxidized layer in O_2 oxidized sample, which probably contains a greater amount of oxygen vacancies.
These oxygen vacancies within the titanium oxide layer can act as charge traps. During imprint conditions, these trapped charges can partially screen the internal electric field that opposes the polarisation direction. For positive imprint, where the polarisation is oriented upwards, the trapped charges near the bottom electrode stabilize this polarisation state more effectively.

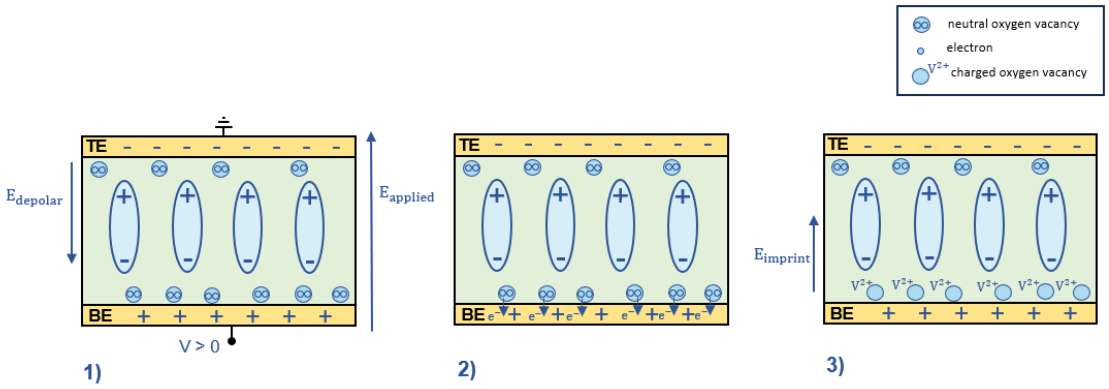

Figura 4.20: Positive imprint mechanism.

This stabilization occurs through the creation of an internal electric field that supports and improves the polarisation up, making the positive imprint more pronounced [40][24], as illustrated in Figure 4.20. In contrast, the negative imprint imprint is quite consistent over all three samples.

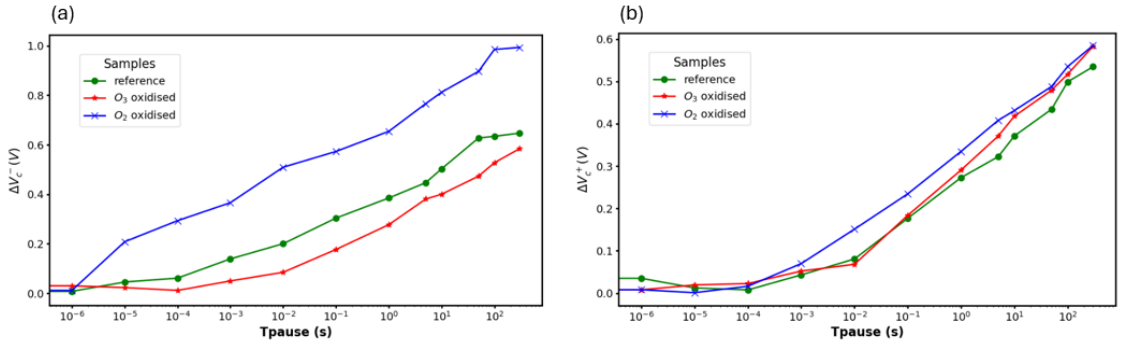

Figura 4.21: Sample 1 VS sample 2 VS sample 3 when 3.5 V and 10^3 cycles : (a) positive imprint ; (b) negative imprint.

As shown in Figure 4.21 (a), interface engineering, specifically in the case of O_3 oxidised sample, has led to a reduction in positive imprint. This result can be attributed to the lower presence of oxygen vacancies at the bottom electrode, due to the presence of oxidized TiN, which contributes positively to reducing the positive imprint.

Finally, a comparison was conducted between the reference sample and O_3 oxidized sample, based on the data obtained from different measurements performed on the same electrode.

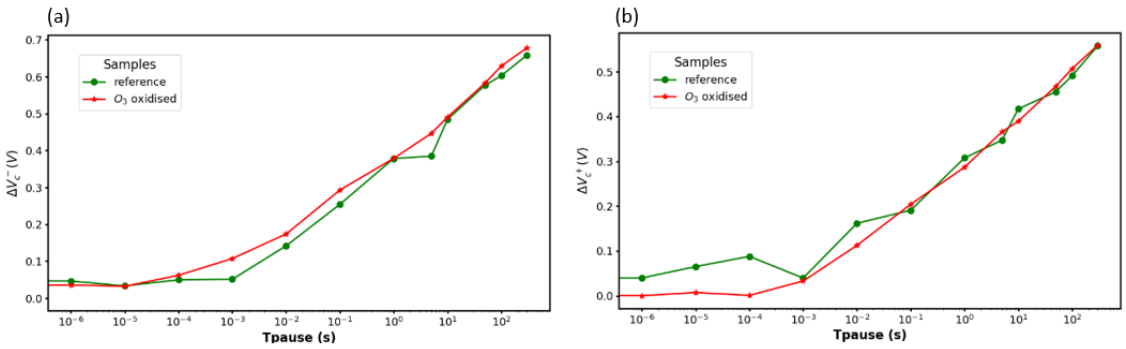

Figura 4.22: Sample 1 VS sample 2 when 3 V and 10^3 cycles : (a) positive imprint ; (b) negative imprint.

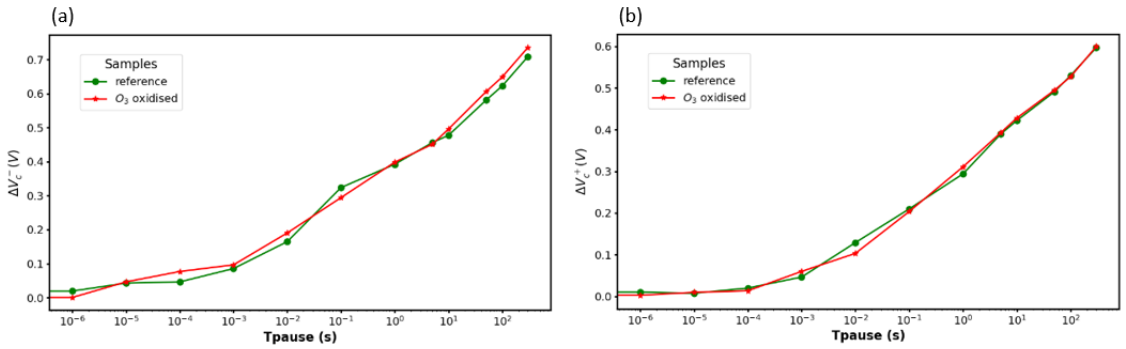

Figura 4.23: Sample 1 VS sample 2 when 3 V and 10^4 cycles : (a) positive imprint ; (b) negative imprint.

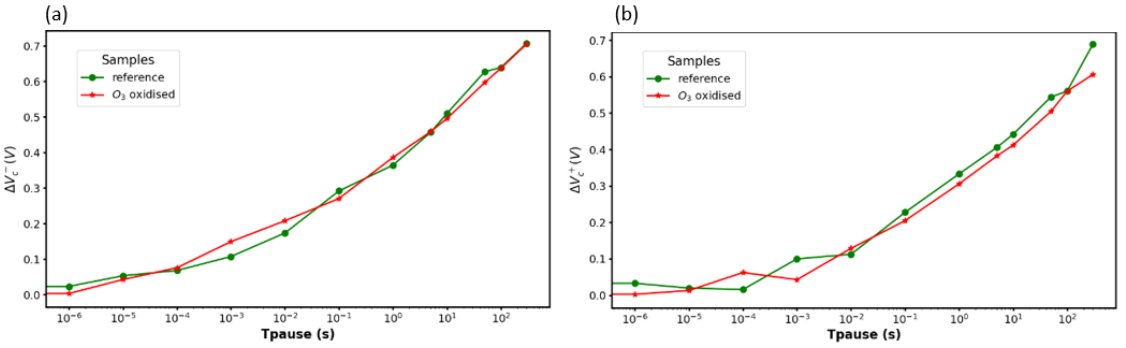

Figura 4.24: Sample 1 VS sample 2 when 3 V and 10^5 cycles : (a) positive imprint ; (b) negative imprint.

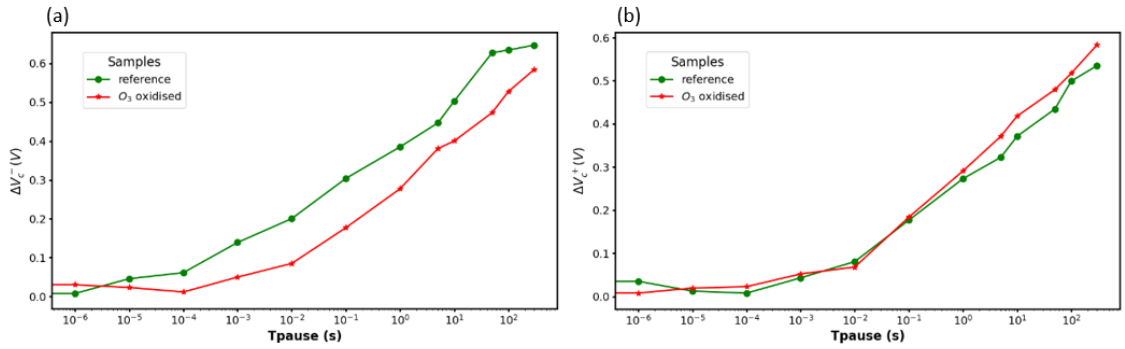

Figura 4.25: Sample 1 VS sample 2 when 3.5 V and 10^3 cycles : (a) positive imprint ; (b) negative imprint.

From these graphs, it is clear that the oxidized layer in the sample does not lead to any improvement in the negative imprint. Regarding the positive imprint, it can be observed that by increasing the wake-up cycles, the contribution of the positive imprint in O_3 oxidized sample decreases (probably due to the movement of oxygen vacancies, as previously explained), but it does not show improvements compared to the reference sample. However, in the case of positive imprint (a) in Figure 4.25, applying a higher voltage of 3.5 V seems to result in a significant improvement in the positive imprint. This is the only case investigated where interface engineering produced an advantageous result.
In general the presence of a thin or thick layer of TiN oxide can affect the imprint phenomenon in ferroelectric memories, as well the polarisation behavior and the endurance. From one side the layer can improve certain aspects of device performance, but it also introduces challenges related to charge trapping and reliability.

Capitolo 5

Conclusion and future perspectives

This thesis presents a study on the electrical characterization of ferroelectric memories based on hafnium zirconium oxide (HZO), using the Keithley 4200 parameter analyzer and a probe station. Starting from the definition and the application of imprint measurement protocol, parameters such as endurance and various imprint under different conditions were measured.
The study aims to better understand the complex behaviours and reliability of HZO-based ferroelectric memory, particularly with the inclusion of a TiN oxidised layer.
The detailed investigation into the imprint phenomenon reveals significant impacts on device reliability. In the reference sample, it was observed that the positive imprint, characterized by an induced up polarisation, is more pronounced, probably due to the influence of oxygen vacancies within the HZO material at the interface with the electrodes [25]. These vacancies act as charge traps, stabilizing the upward polarisation state more effectively than the downward state. This effect is possibly due to a higher concentration of oxygen vacancies at the bottom interface, therefore extra analysis to evaluate the presence of oxygen vacancies at both interfaces are necessary to confirm this thesis.
However, a similar trend is observed in O_3 oxidised sample and O_2 oxidised sample, which are expected to have fewer oxygen vacancies at the bottom interface due to the presence of the oxidized layer. This layer is expected to decrease the number of oxygen vacancies, consequently improving the ferroelectric property of the thin film and enhancing device reliability [10].
In fact, for the O_3 oxidised sample, a reduction in the positive imprint was observed, confirming the lower quantity of oxygen vacancies at the bottom interface.
However, regarding the stronger positive imprint compared to the negative imprint observed even for the O_3 sample, the observed results suggest that the oxidised layer may contribute to charge trapping phenomena, affecting the performance and imprint behaviour of ferroelectric memory. The thickness of this layer plays a crucial role in the imprint properties and the effective capacitance of the device. Additionally, it impacts polarisation efficiency and endurance by introducing barrier effects at the interfaces [10].
Finally the endurance tests demonstrate that increasing the applied voltage enhances the

remnant polarisation by switching more domains, but at the cost of reduced endurance due to accelerated breakdown processes. Therefore balancing polarisation efficiency and endurance is essential for optimizing device performance and reliability [40].

This research represents a first attempt towards understanding the impacts of the imprint phenomenon, the influence of oxidized layers, and the impact of various electrical stresses.
However to fully understand the imprint mechanism, future studies should focus on a detailed analysis of oxygen vacancies within the samples. In addiction, it would be useful to conduct measurements on a variety of samples fabricated using different processes, incorporating different interfacial layers, and exploring different materials. This deeper approach might offer a more comprehensive knowledge of the parameters controlling imprint behaviour, as well as contribute in the optimisation of ferroelectric memory performance.

Capitolo 6

Appendix

6.1 Imprint measurements on the reference sample

Voltage level (recovery cycles)	**Recovery cycles**	**Electrode**
2.5 V	5	D6 (20 μm)
3 V	5	D6 (20 μm)
3.5 V	5	D6 (20 μm)
3 V	5	D7 (20 μm)
3 V	10	D7 (20 μm)
3 V	25	D7 (20 μm)
3 V	50	D7 (20 μm)

Tabella 6.1: Voltage levels and corresponding electrodes for the imprint recovery test.

As described in Chapter 3 "Imprint measurement", two types of graphs were defined: the evolution of the PV loop (a)(b) and the imprint (c) with respect to different pauses respectively for the positive imprint ($|Vc^{-}_{t_{pause}} - Vc^{-}_{ref}|$) and the negative imprint ($|Vc^{+}_{t_{pause}} - Vc^{+}_{ref}|$)

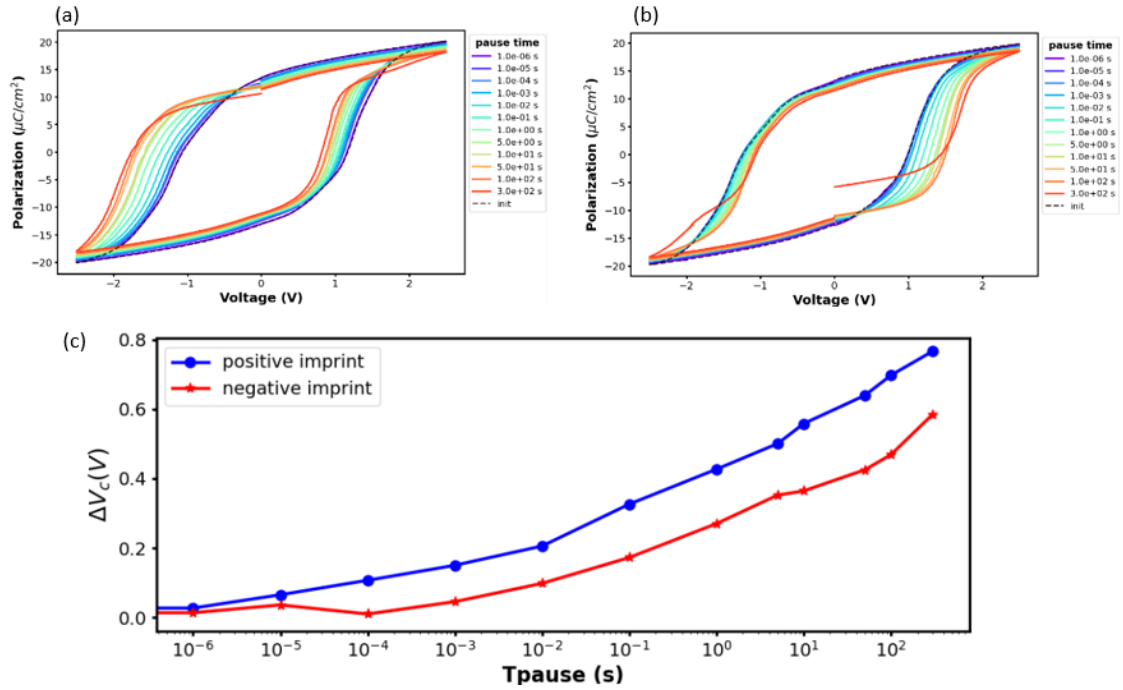

Figura 6.1: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 2.5 V and 10^3 cycles.

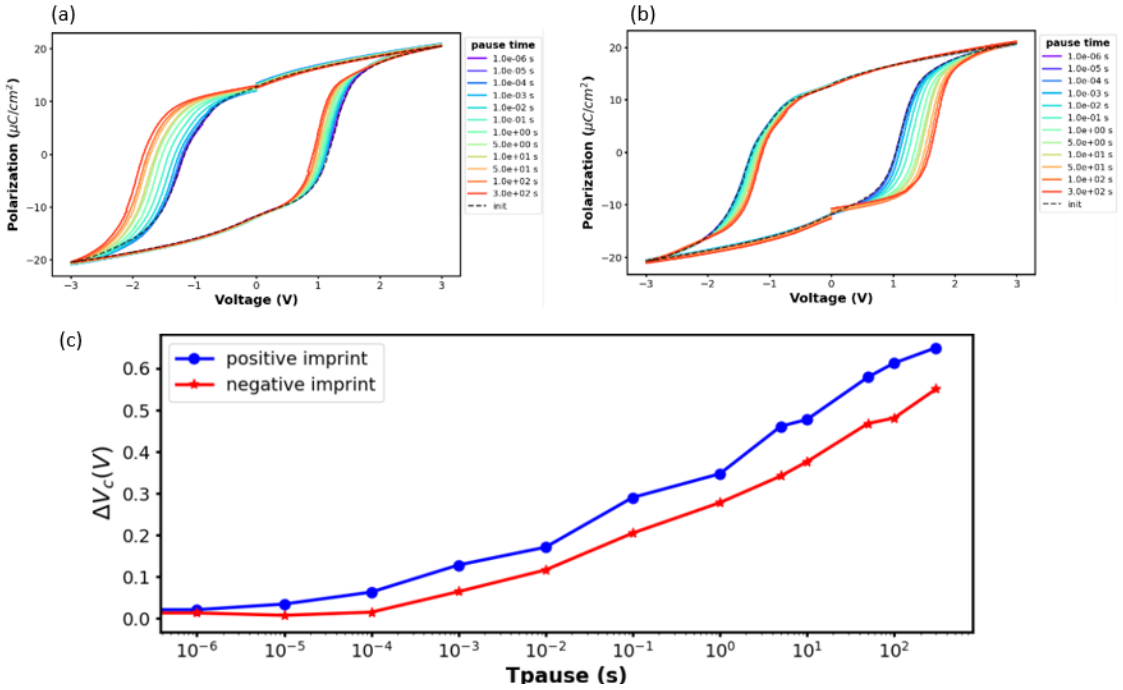

Figura 6.2: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^3 cycles.

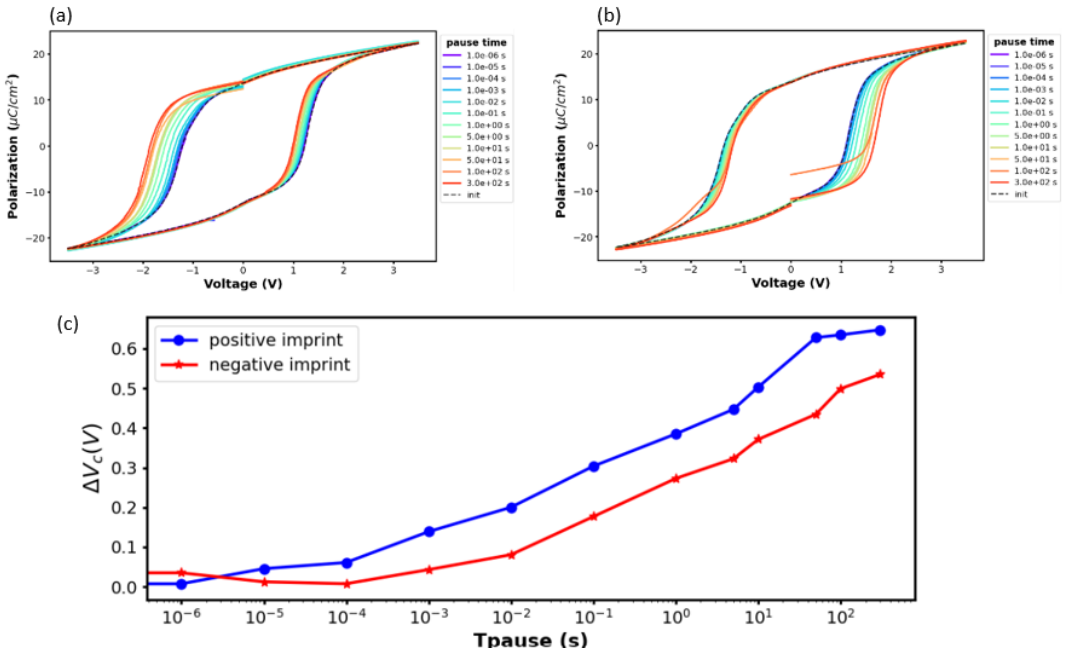

Figura 6.3: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3.5 V and 10^3 cycles.

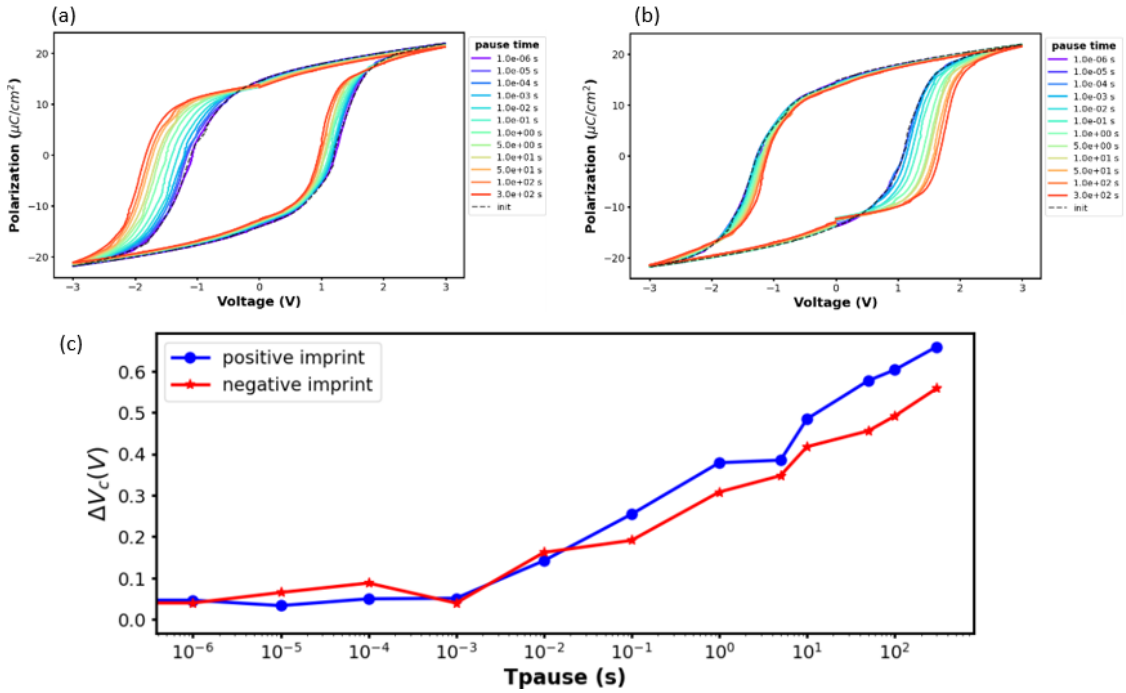

Figura 6.4: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^3 cycles.

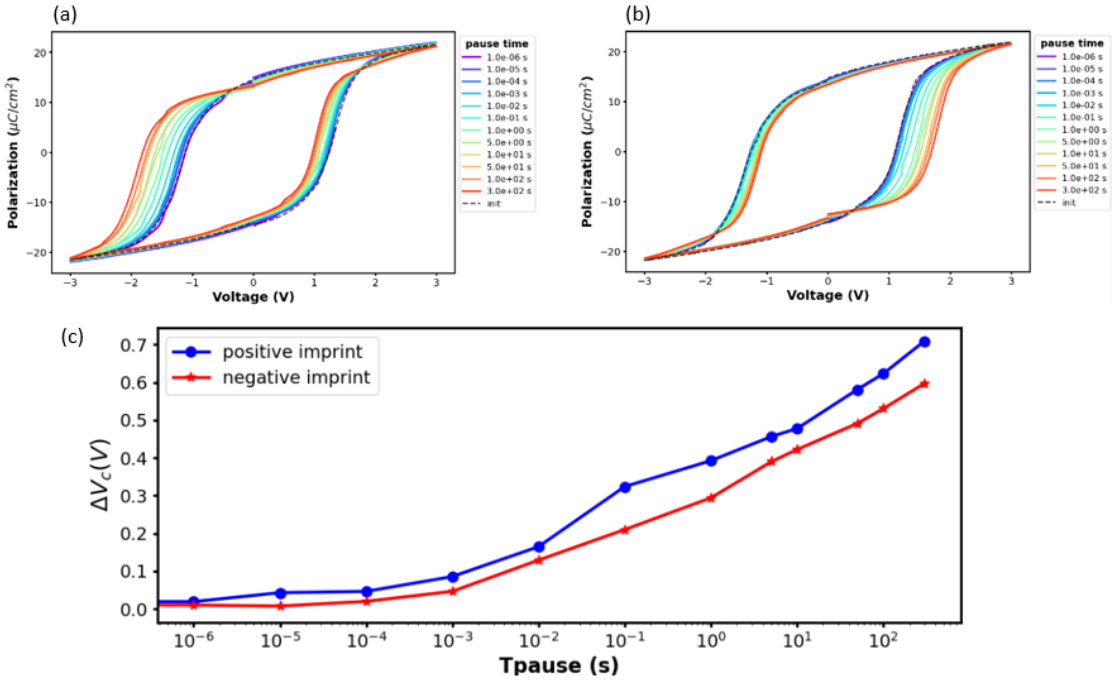

Figura 6.5: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^4 cycles.

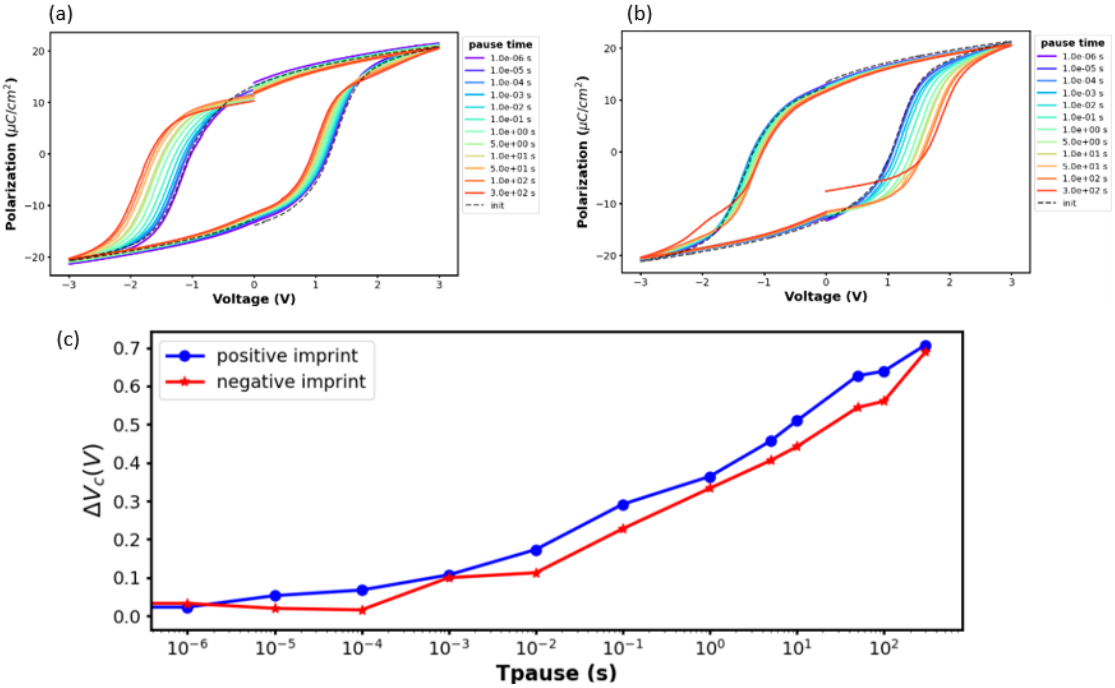

Figura 6.6: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^5 cycles.

Voltage level (wake up and imprint protocol)	Amount of cycles (wake up)	Electrode
2.5 V	10^3	C5 (20 μm)
3 V	10^3	B6 (20 μm)
3.5 V	10^3	C1 (20 μm)
3 V	10^3	B7 (20 μm)
3 V	10^4	B8 (20 μm)
3 V	10^5	C3 (20 μm)

Tabella 6.2: Voltage levels and corresponding electrodes for the imprint measurements.

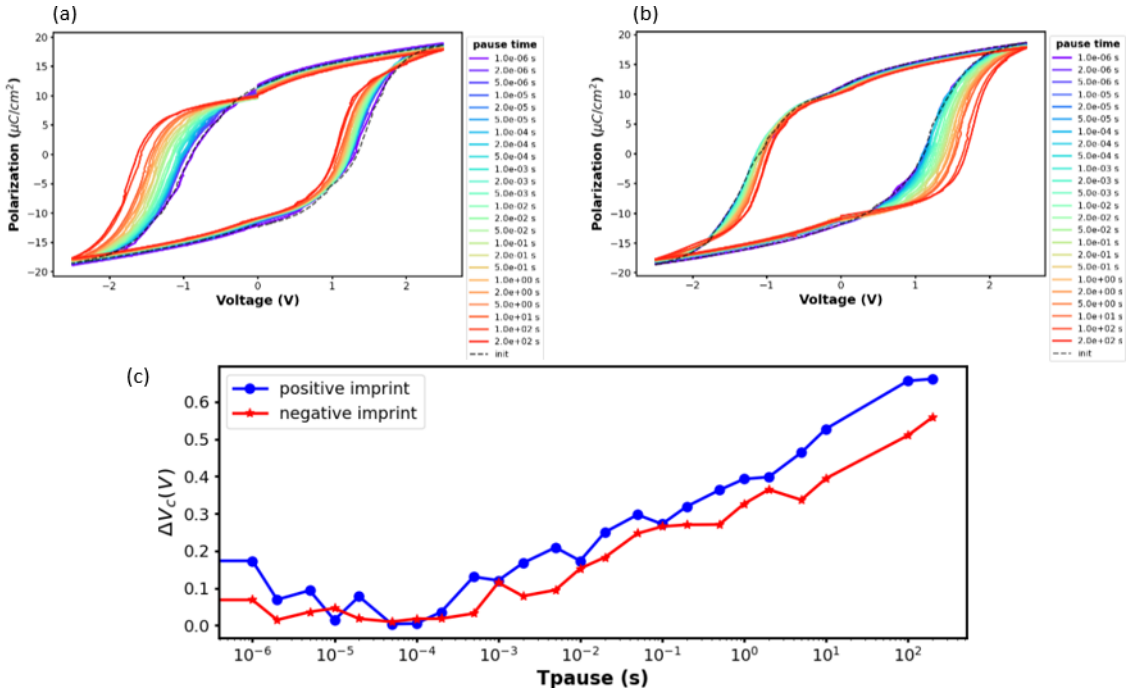

Figura 6.7: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 2.5 V and 10^3 cycles.

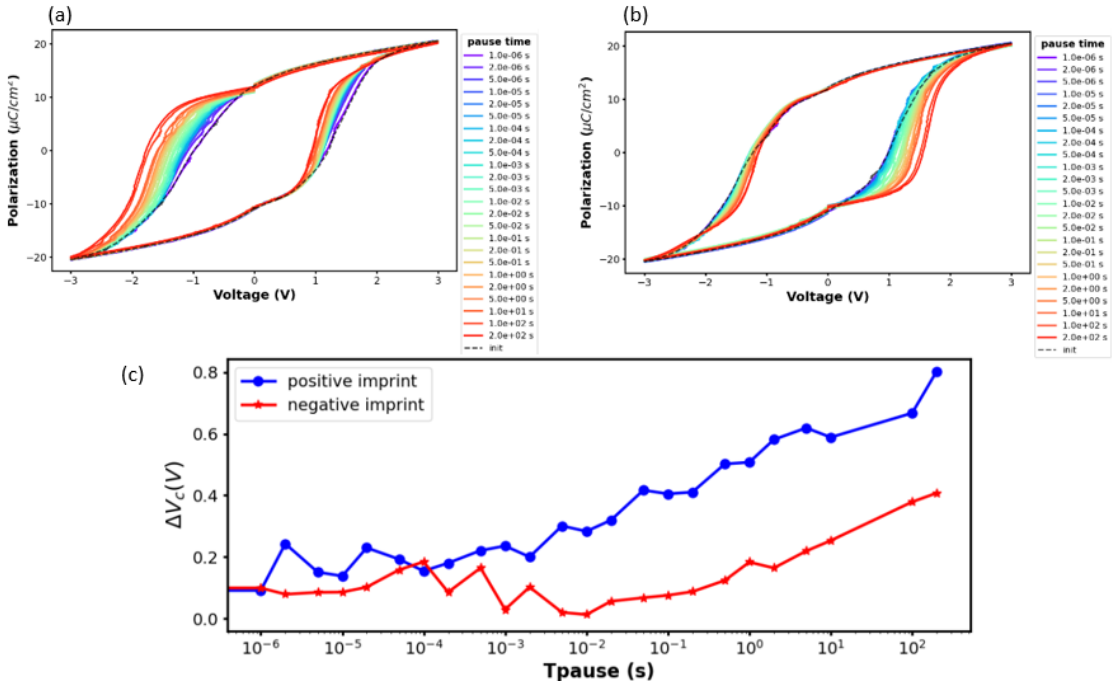

Figura 6.8: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^3 cycles.

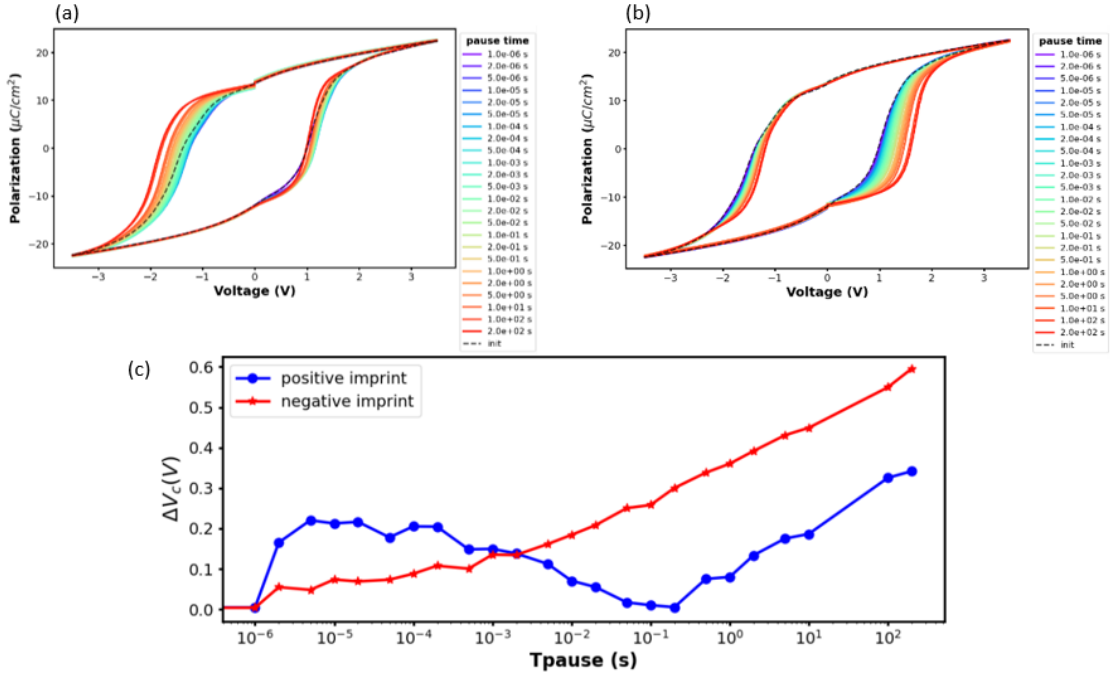

Figura 6.9: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3.5 V and 10^3 cycles.

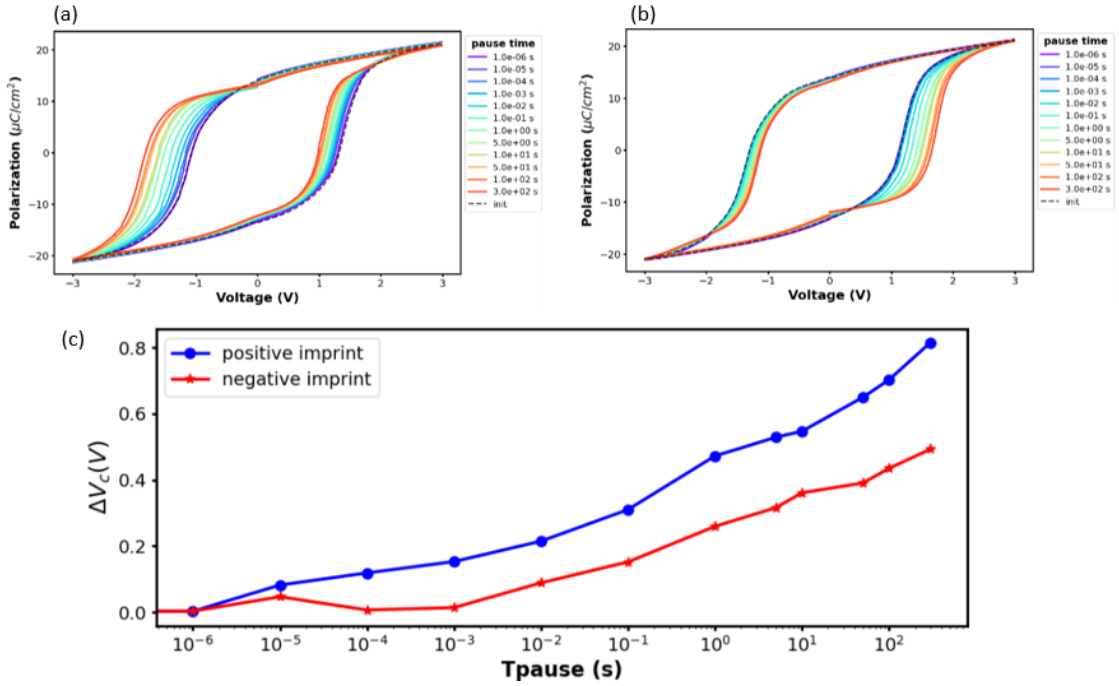

Figura 6.10: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^3 cycles.

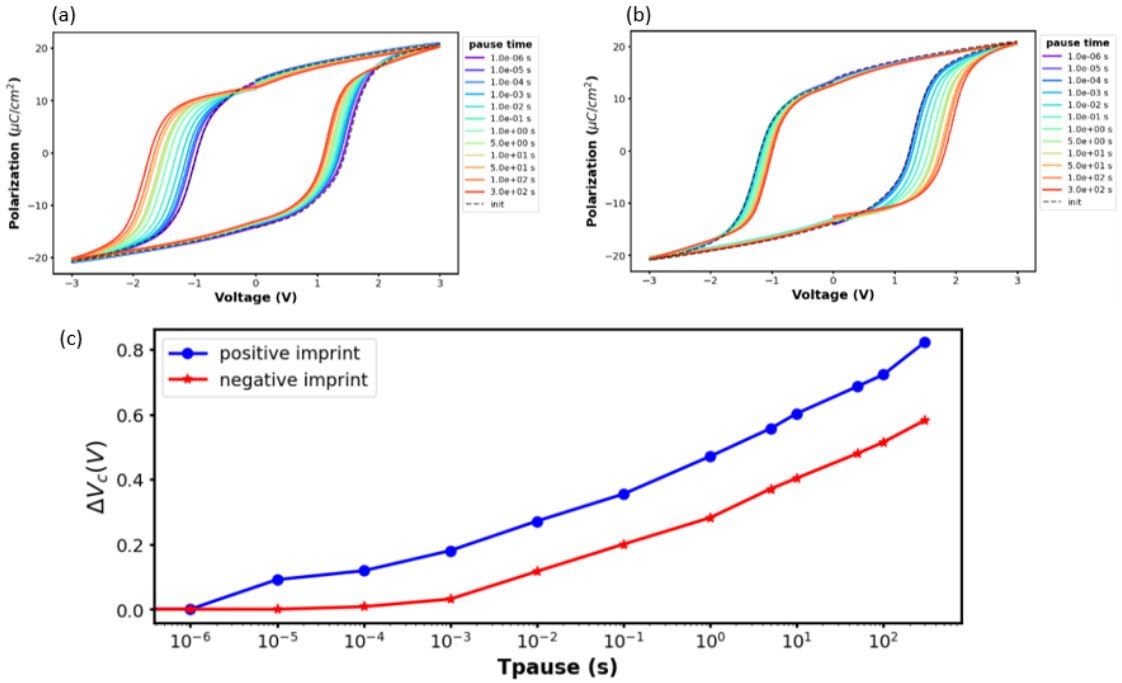

Figura 6.11: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^4 cycles.

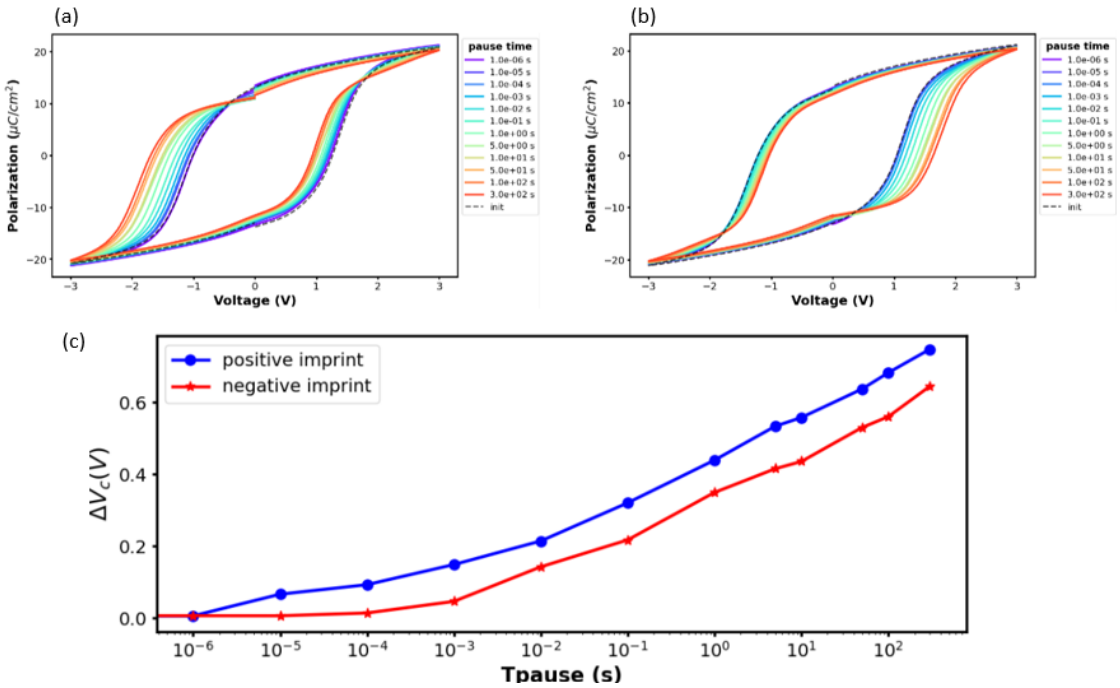

Figura 6.12: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^5 cycles.

6.2 Imprint measurements on O_2 oxidised sample

Voltage level (imprint protocol)	Amount of cycles (wake up)	Electrode
2.5 V	10^3	B7 (20 μm)
3 V	10^3	B7 (20 μm)
3.5 V	10^3	B7 (20 μm)
3 V	10^3	B8 (20 μm)
3 V	10^4	B8 (20 μm)
3 V	10^5	B8 (20 μm)

Tabella 6.3: Voltage levels and corresponding electrodes for the imprint measurements.

The figures below show the evolution of the PV loop for positive (a) and negative (b) imprint, as well as the positive and the negative imprint ($|Vc_{t_{pause}} - Vc_{ref}|$) (c) at various pauses.

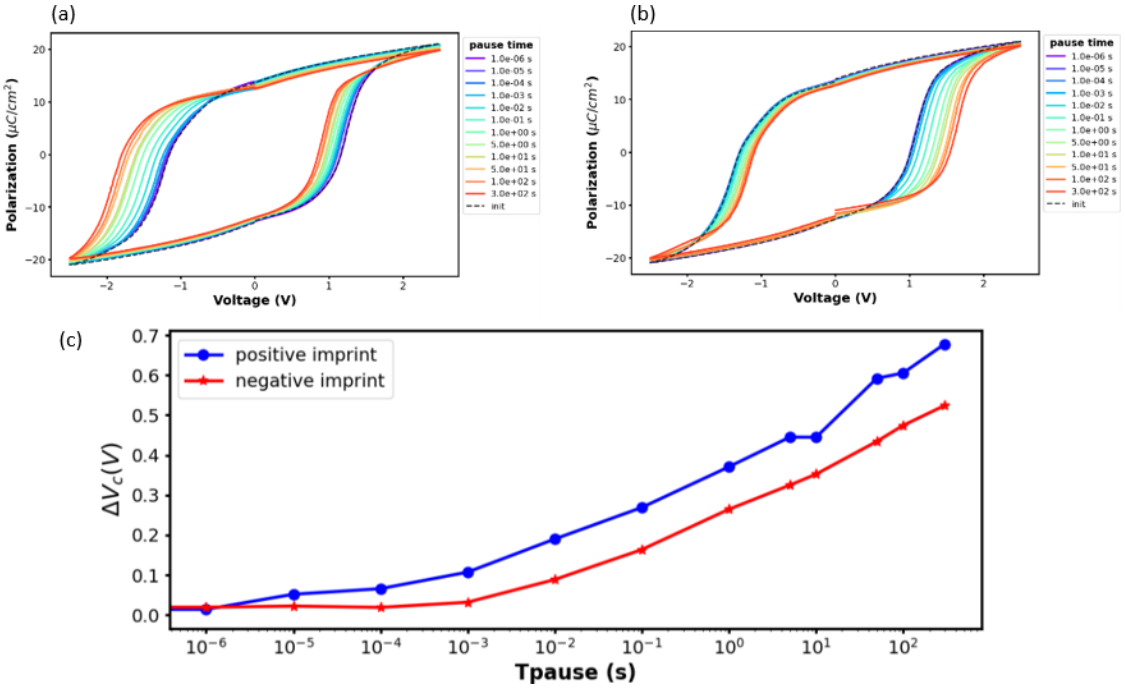

Figura 6.13: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 2.5 V and 10^3 cycles.

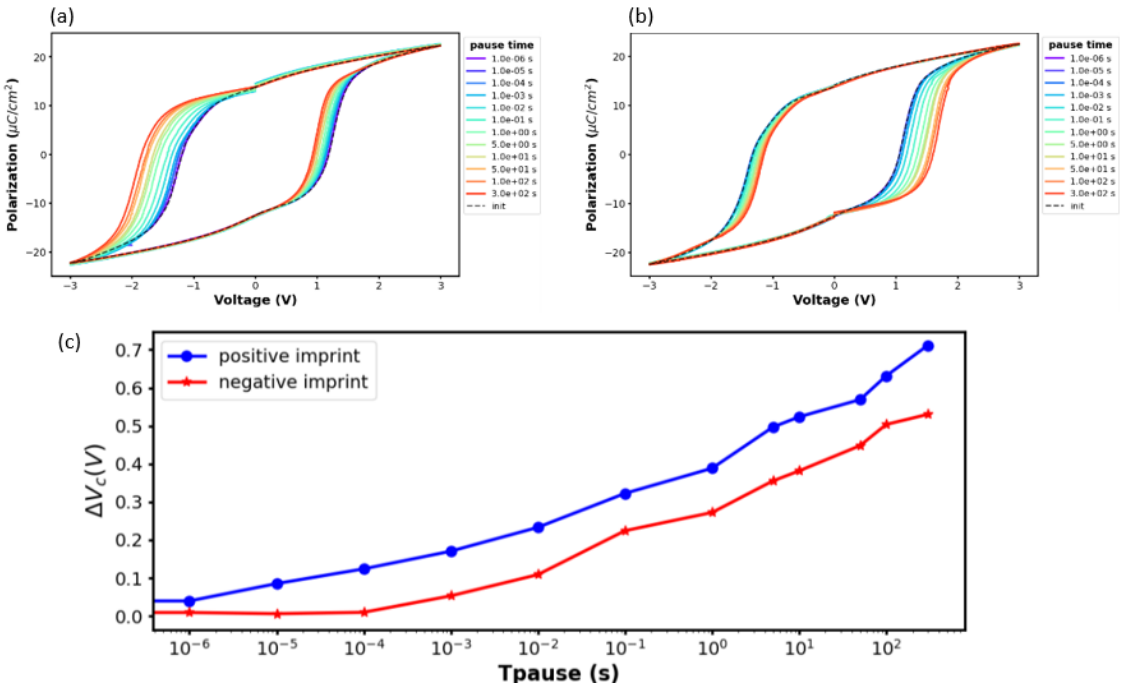

Figura 6.14: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^3 cycles.

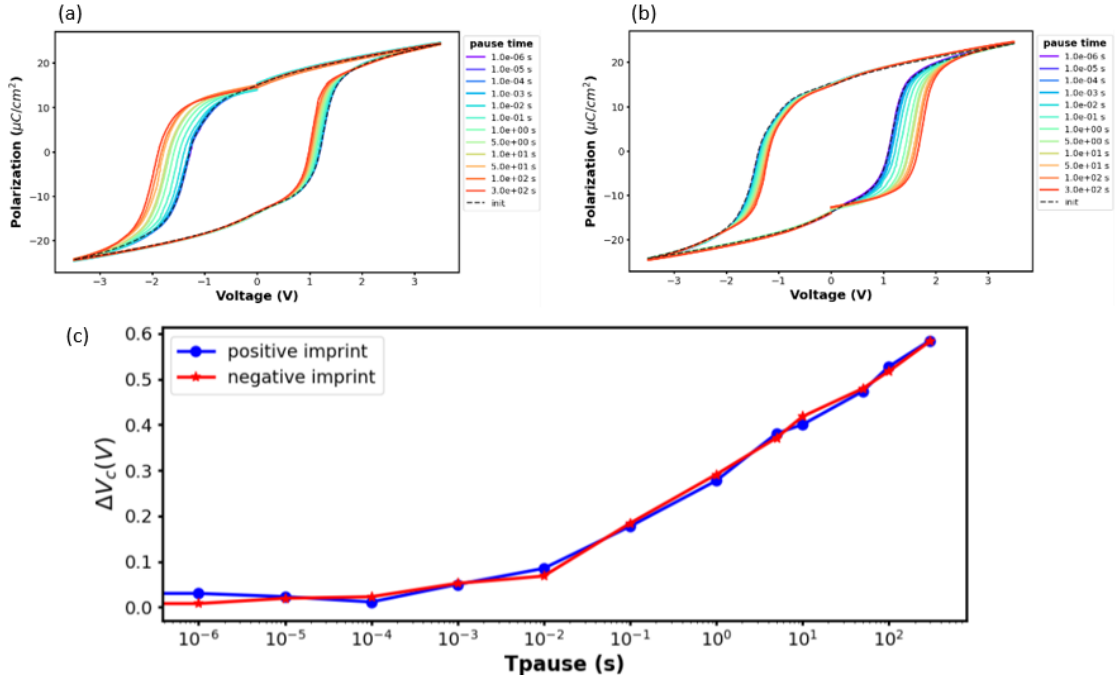

Figura 6.15: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3.5 V and 10^3 cycles.

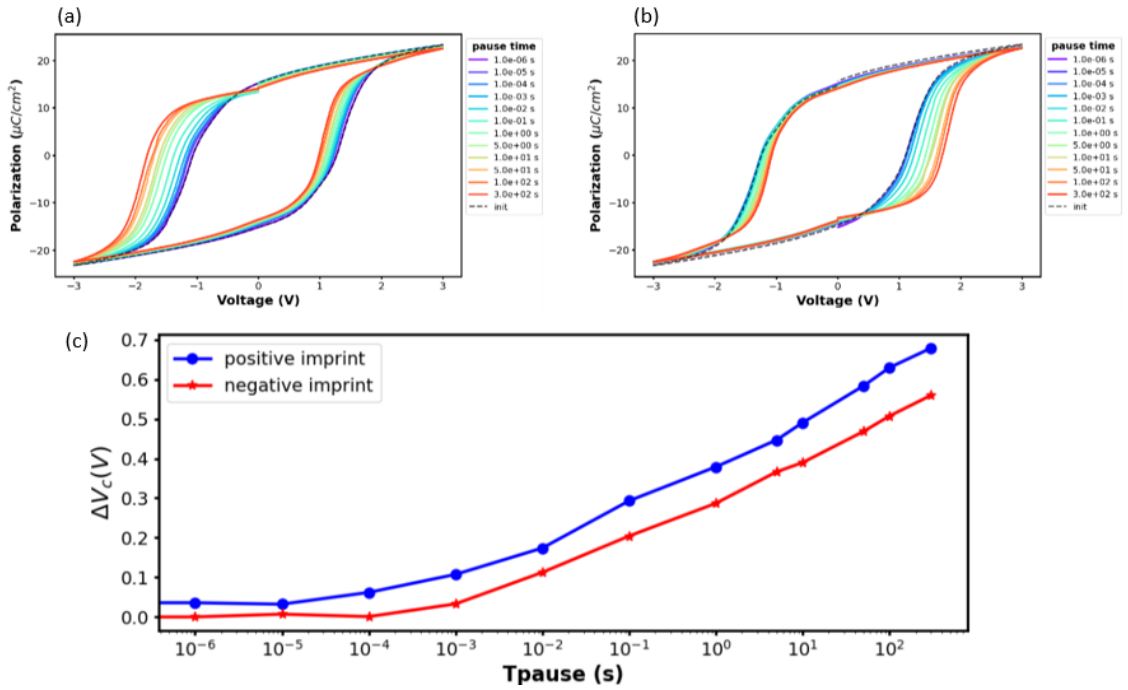

Figura 6.16: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^3 cycles.

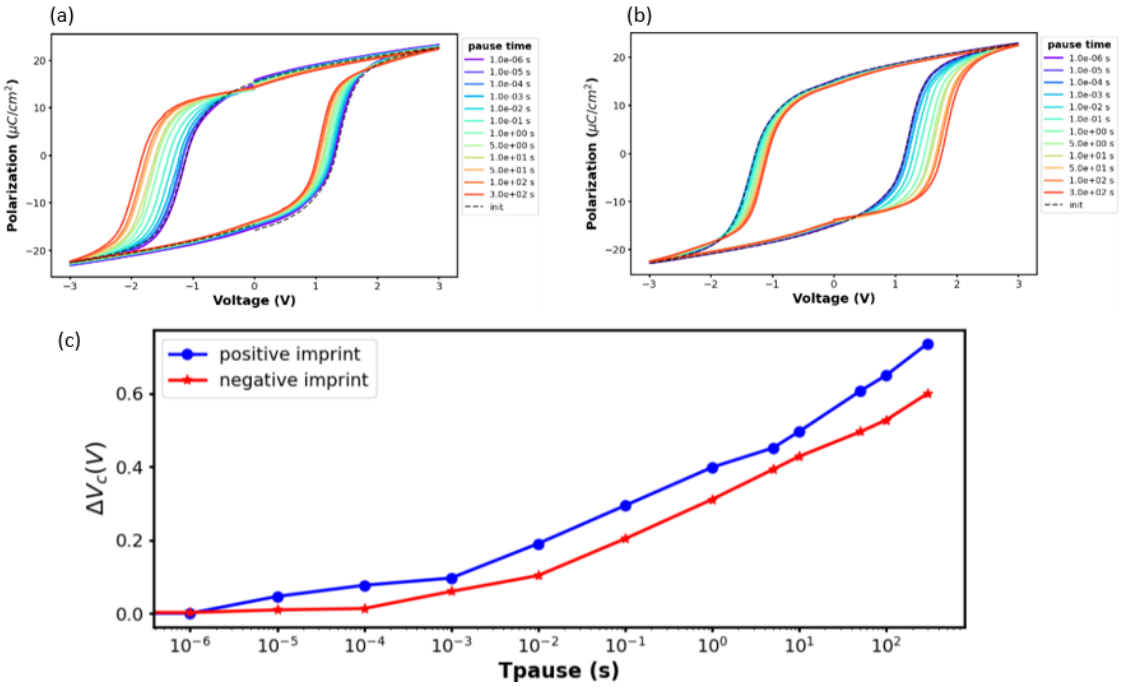

Figura 6.17: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^4 cycles.

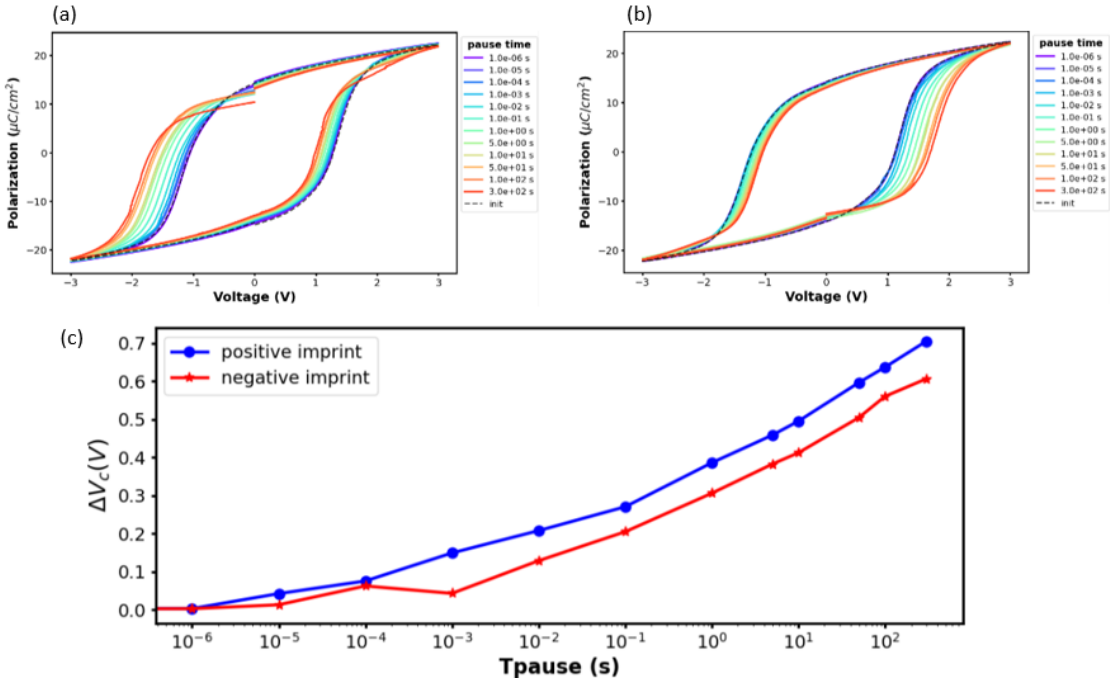

Figura 6.18: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^5 cycles.

Voltage level (wake up and imprint protocol)	**Amount of cycles (wake up)**	**Electrode**
2.5 V	10^3	A6 (20 μm)
3 V	10^3	A7 (20 μm)
3.5 V	10^3	A8 (20 μm)
3 V	10^4	B1 (20 μm)
3 V	10^5	B2 (20 μm)

Tabella 6.4: Voltage levels and corresponding electrodes for the imprint measurements.

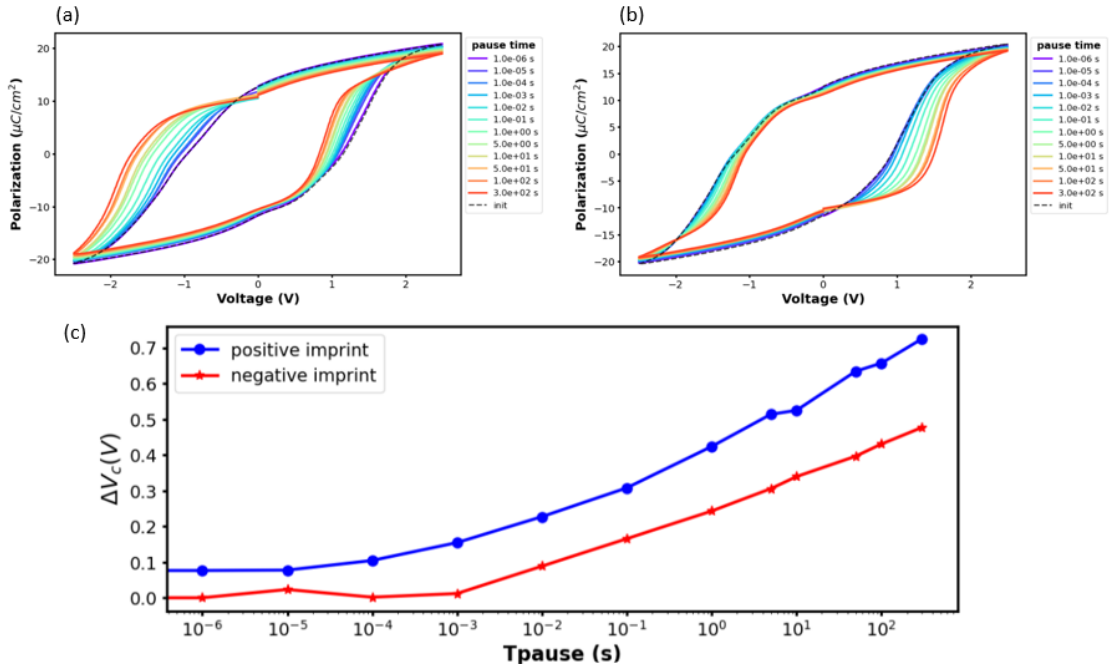

Figura 6.19: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 2.5 V and 10^3 cycles.

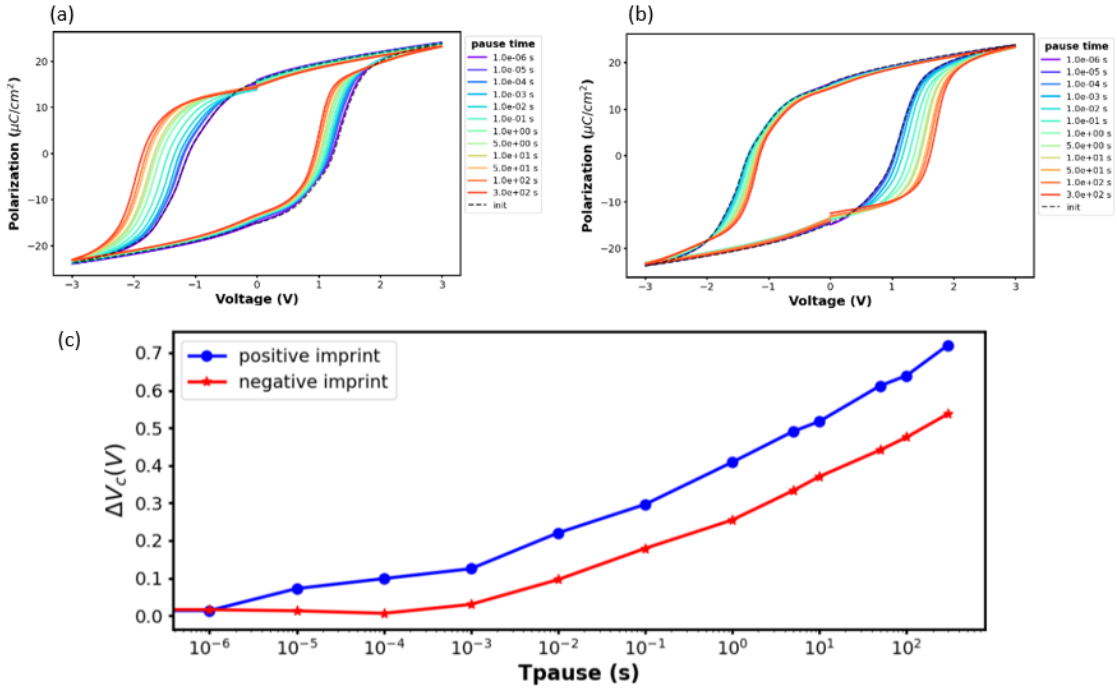

Figura 6.20: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^3 cycles.

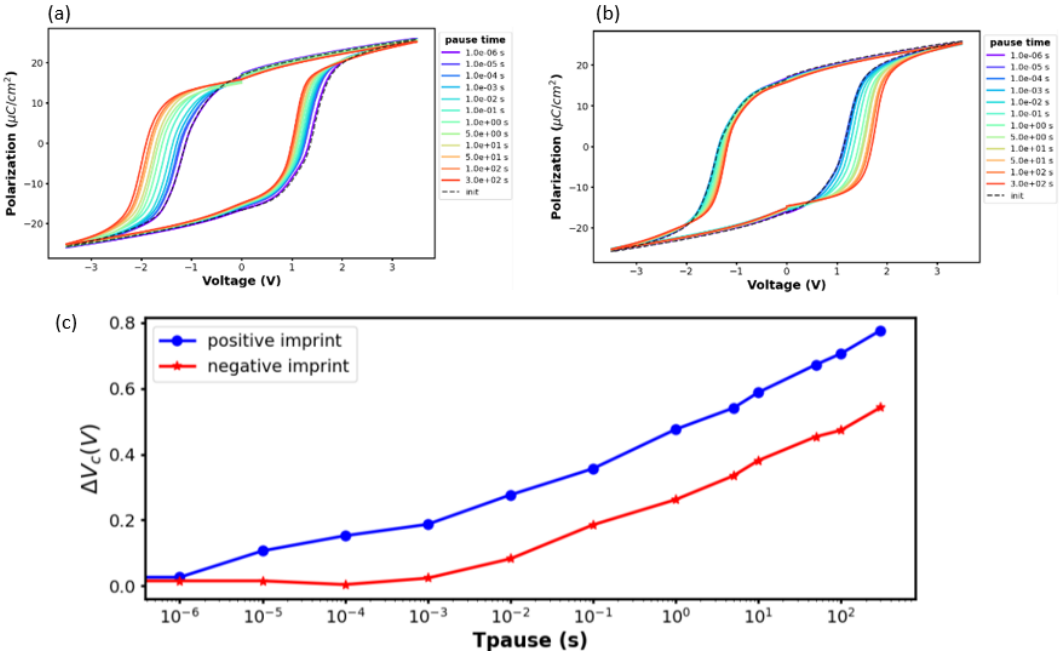

Figura 6.21: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3.5 V and 10^3 cycles.

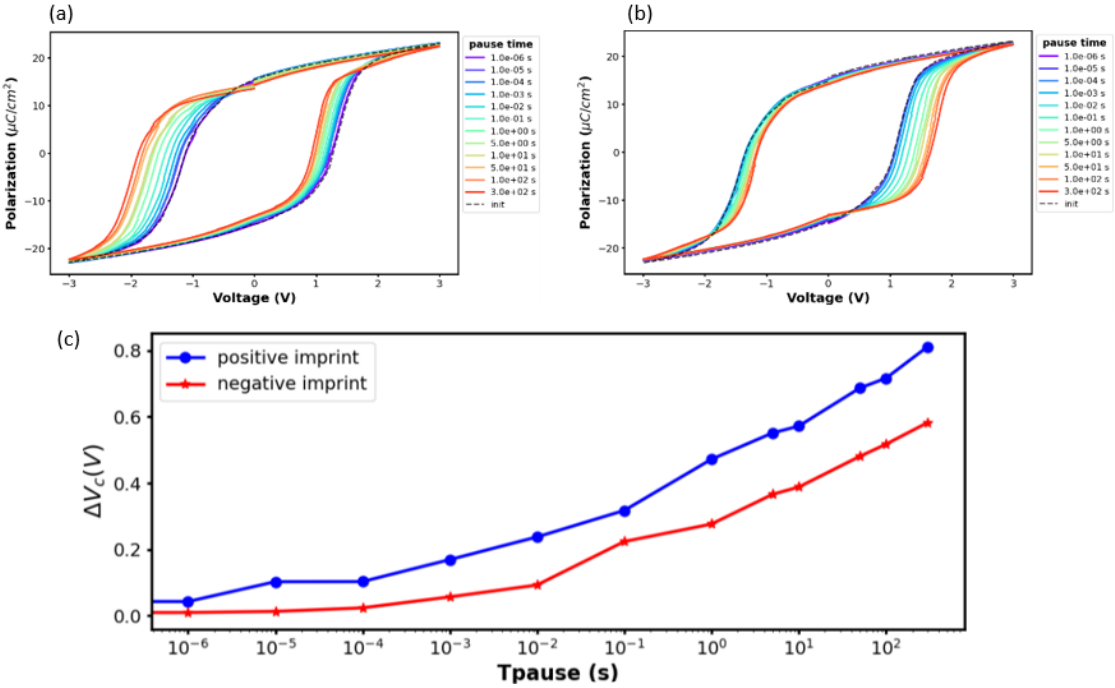

Figura 6.22: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^4 cycles.

6.3 Imprint measurements on O_3 oxidised sample

Voltage level (imprint protocol)	Amount of cycles (wake up)	Electrode
2.5 V	10^3	B3 (20 μm)
3 V	10^3	B4 (20 μm)
3.5 V	10^3	C2 (20 μm)
3 V	10^4	B8 (20 μm)
3 V	10^5	B5 (20 μm)

Tabella 6.5: Voltage levels and corresponding electrodes for the imprint measurements.

The following figures show the PV loops for both positive (a) and negative (b) imprint, as well as the imprint itself (c), for a pause duration ranging from 1 μs to 300 s.

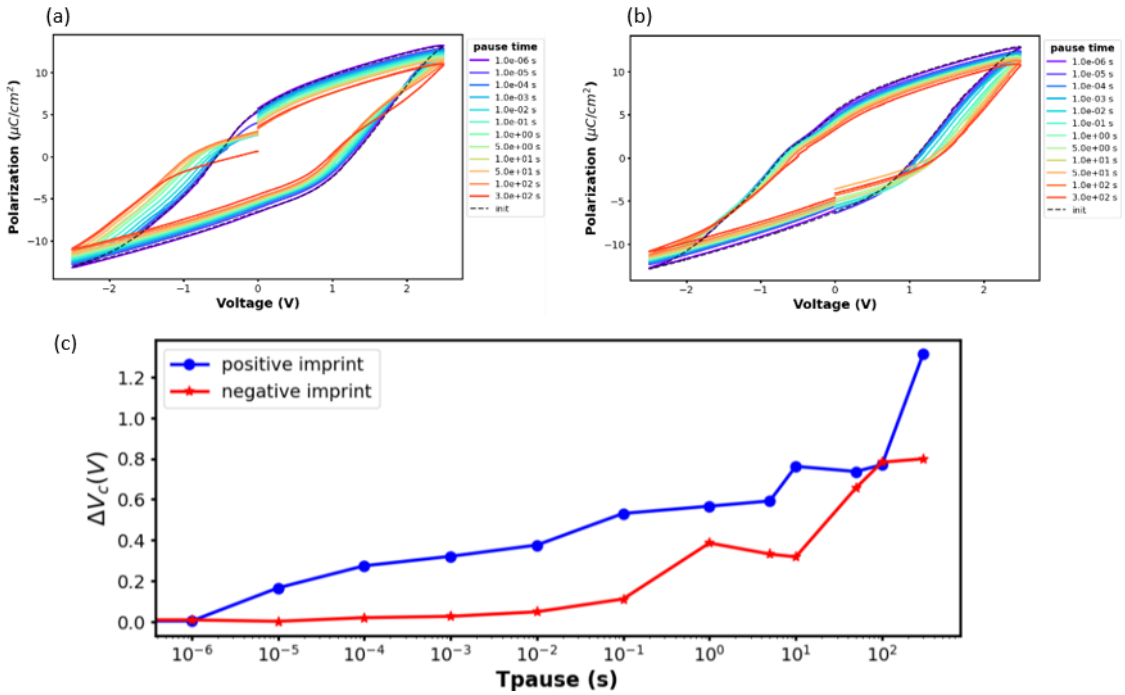

Figura 6.23: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 2.5 V and 10^3 cycles.

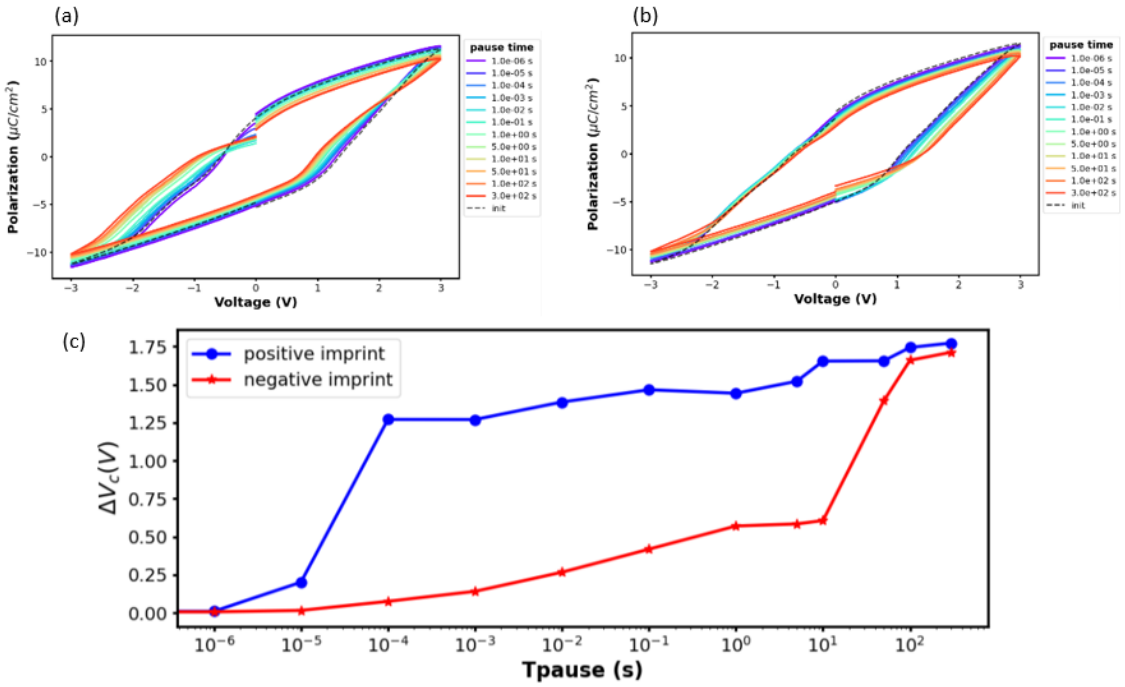

Figura 6.24: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^3 cycles.

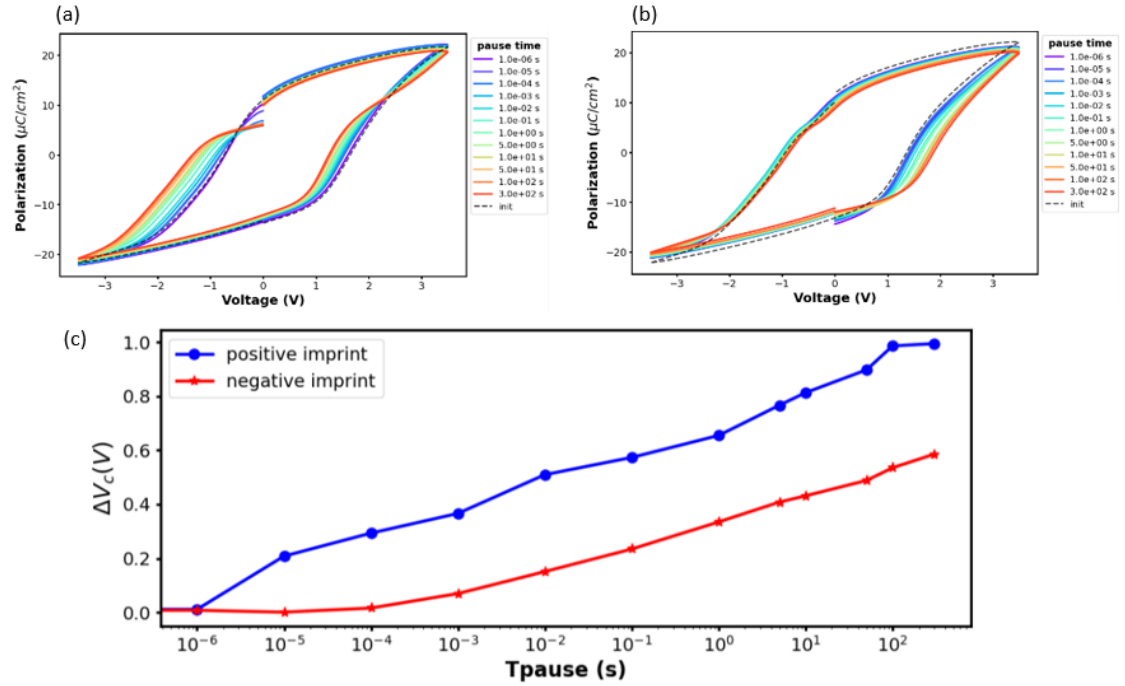

Figura 6.25: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3.5 V and 10^3 cycles.

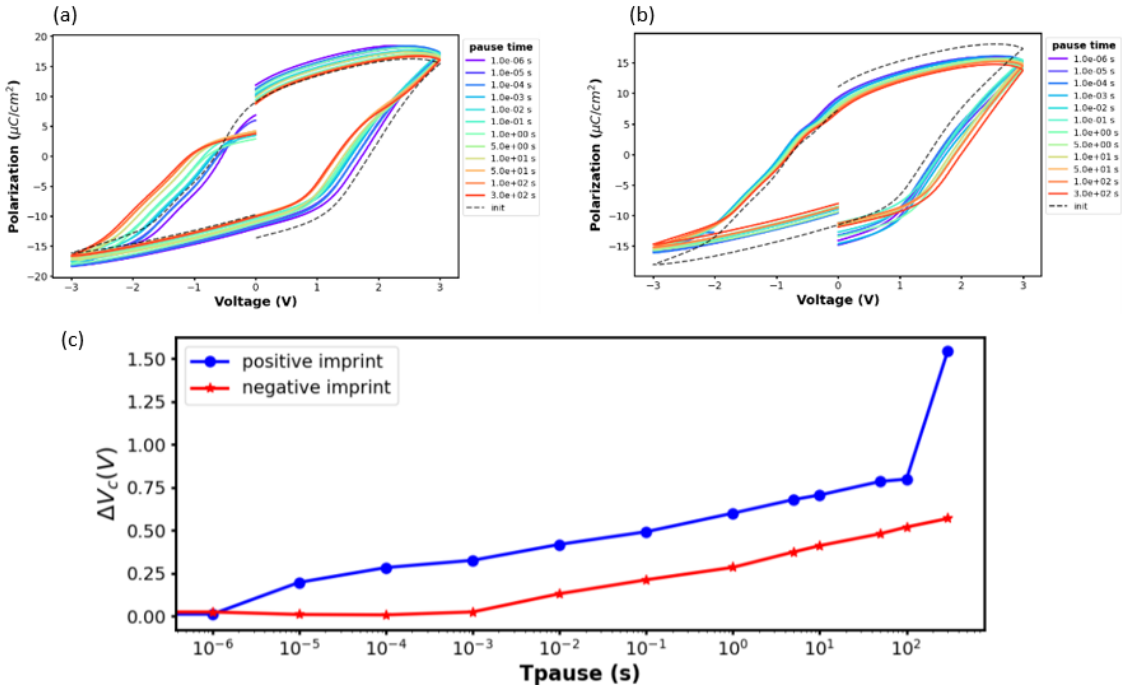

Figura 6.26: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^4 cycles.

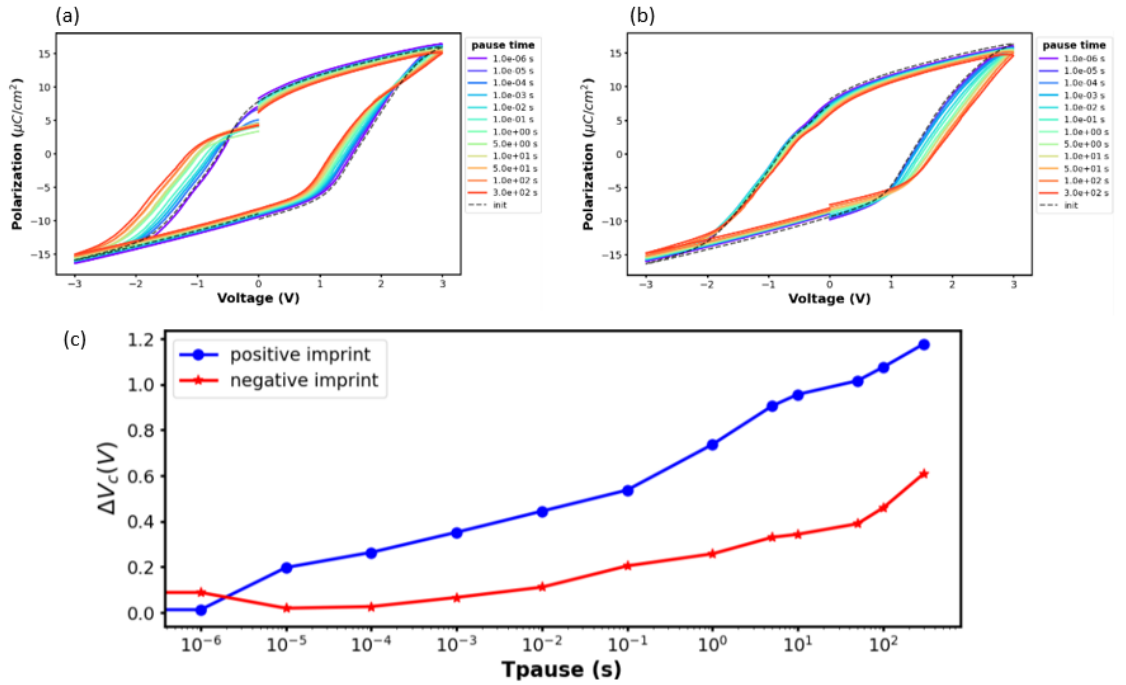

Figura 6.27: PV loop positive imprint (a); PV loop for negative imprint (b); positive imprint and negative imprint (c) for 3 V and 10^5 cycles.

Bibliografia

[1] Federico Danieli, Scott MacLachlan, "Multigrid Reduction in Time for nonlinear hyperbolic equations", 2021

[2] N. Izyumskaya,Yahya Alivov, Seong-Jun Cho, Y.-S. Kang. "Processing, Structure, Properties, and Applications of PZT Thin Films" *Critical Reviews in Solid State and Material Sciences*, July 2007

[3] Mohammadhu Faalil, Mozilla Club of UCSC

[4] Fanqing Zhang, Chunyang Li, Zhongyi Li, Lixin Dong and Jing Zhao. "Recent progress in three-terminal artificial synapses based on 2D materials: from mechanisms to applications", *Microsystems And Nanoengineering*, 2023

[5] Yixin ZhuYing, ZhuHuiwu MaoShow, Qing WanQing Wan "Recent advances in emerging neuromorphic computing and perception devices" *Applied Physics*, October 2021

[6] Chua. "Memristor—The Missing Circuit Element" *IEEE Transactions on Circuit Theory*, 1971

[7] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, "Ferroelectricity in hafnium oxide thin films," *Applied Physics Letters*, 2011.

[8] Ayse Sünbül,David Lehninger, Maximilian Lederer, et al., "A Study on Imprint Behavior of Ferroelectric Hafnium Oxide Caused by High-Temperature Annealing", *Physica Status Solidi*, 2019

[9] S. V. Ushakov, et. al, "Crystallization in hafnia- and zirconia-based systems,", *Physica Status Solidi (B) Basic Research*,2004

[10] Xuepei Wang, et al., "Oxygen Vacancy Modulation With TiO_2 Stack Interface Engineering for Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Thin Films" , *IEEE Electron Device Letters*, 2024

[11] Vincent Garcia, "Ferroelectric tunnel junctions," *Unité Mixte de Physique CNRS/Thales. Palaiseau, France*, 2011.

[12] P. Chandra and P.B. Littlewood, "A Landau Primer for Ferroelectrics", February 5, 2008

[13] J. F. Scott, "Applications of modern ferroelectrics", *Science* , Feb 2007

[14] Benjamin Max, Michael Hoffmann, Halid Mulaosmanovic, Stefan Slesazeck and Thomas Mikolajick. "Hafnia-Based Double-Layer Ferroelectric Tunnel Junctions as Artificial Synapses for Neuromorphic Computing" *Nature Materials*, 2020

[15] Y. Higashi, et al., "Impact of Charge Trapping on Imprint and its Recovery in HfO2 Based FeFET" , *IEEE*, 2019

[16] Minh D Nguyen, Chi T.Q. Nguyen, Vu Ngoc Hung, Guus Rijnders, "Experimental evidence of breakdown strength and its effect on energy-storage performance in normal and relaxor ferroelectric films",*Current Applied Physics*, 2019

[17] Kai Ni, Jeffrey Smith, Huacheng Ye, et al., "A Novel Ferroelectric Superlattice Based Multi-Level Cell Non-Volatile Memory" , *IEEE*, 2019

[18] Youngjun Park, Min-Kyu Kim, Jang-Sik Lee, "Emerging memory devices for artificial synapses", *Journal of materials Chemistry C*, 2020

[19] Philippe Tückmantel, "Scanning Probe Studies of Structural and Functional Properties of Ferroelectric Domains and Domain Walls", 2021

[20] D. Pantel and M. Alexe, "Electroresistance effects in ferroelectric tunnel barriers," *Journal of Applied Physics*, 2010.

[21] M. Hoffmann, et al., "Direct Correlation of Ferroelectric Properties and Memory Characteristics in Ferroelectric Tunnel Junctions" *IEEE*, 2019.

[22] Greta Segantini, "Fabrication of Ferroelectric Tunnel Junctions for the Implementation of Artificial Synapses"

[23] Vincent Garcia, Manuel Bibes, "Ferroelectric tunnel junctions for information storage and processing", *Nature communications*, 2014

[24] Peng Yuan, Ge-Qi Mao, et al., "Microscopic Mechanism of Imprint in Hafnium Oxide-based Devices", *Nano Reasearch*, 2021

[25] J. Bouaziz, P. Rojo Romeo, N. Baboux, B. Vilquin, "Imprint issue during retention tests for HfO2-based FRAM: An industrial challenge?" , *Appl. Phys. Lett*, 2021

[26] James F. Scott,Carlos Paz de Araujo, "Ferroelectric Memories", *Science*, January 1990

[27] Michael Hoffmann, Stefan Slesazeck, and Thomas Mikolajick, "Progress and future prospects of negative capacitance electronics: A materials perspective", *APL materials*, 2021

[28] "A century of ferroelectricity" , *Nature Materials*, 2020

[29] J. Müller, et al., "Ferroelectric $Zr_{0.5}Hf_{0.5}O_2$ thin films for nonvolatile memory applications", *Applied Phyiscs Letters*, 2011

[30] Si Joon Kim, Jaidah Mohan, Scott Summerffelt and Jiyoung Kim, "Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Thin Films: A Review of Recent Advances" *JOM*, 2019

[31] Wenwu Xiao, Chen Liu, et al., "Thermally Stable and Radiation Hard Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ ThinFilms on Muscovite Mica for Flexible Nonvolatile MemoryApplications", *Applied Electronics Materials*, 2019

[32] Cédric Marchand, Ian O'Connor, Mayeul Cantan, Evelyn T. Breyer, Stefan Slesazeck, Thomas Mikolajick, "FeFET based Logic-in-Memory: an overview", *IEEE*, 2021

[33] A. F. Devonshire, "Theory of ferroelectrics," *Philosophical Magazine*, 1949.

[34] Lin Chen, Tian-Yu Wang, Ya-Wei Dai, Ming-Yang Cha, et. al., "Ultra-low power $Hf_{0.5}Zr_{0.5}O_2$ based ferroelectric tunnel junction synapses for hardware neural network applications" , *Nanoscale*, 2018

[35] Yilin Wang,Hanqing Zhao, Linxing Zhang, Jun Chena, Xianran Xing, "PbTiO3-based perovskite ferroelectric and multiferroic thin films" *Physical Chemistry Chemical Physics*, 2017

[36] V. L. Ginzburg and L. D. Landau, "On the Theory of Superconductivity," *Journal of Experimental and Theoretical Physics*, 1950s.

[37] Dao Wang, Yan Zhang, Yongbin Guo,Zhenzhen Shang, Fangjian Fu, and Xubing Lu, "Impact of annealing temperature on the ferroelectric properties ofW/Hf0.5Zr0.5O2/W capacitor", *Chinese Physics B*, 2023

[38] Scott, de Araujo, "Ferroelectric memories" , *Science*, 1988.

[39] Koussi Ahmed , "Electrical Characterization and Analysis of Ferroelectric Memories based on HafniumZirconium oxide ($HfZrO_2$) ", 2024

[40] Y. Higashi, N. Ronchi, et al., "Impact of Charge trapping on Imprint and its Recovery in HfO2 based FeFET", *IEEE*