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Ferroelectric Thin Films Characterization for Vertical Transistor Integration Toward Future In-Memory Computing

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Abstract

With the imposition of the Artificial Intelligence as the main trend and its conflict with the sustainability goals that our world must satisfy, a new paradigm of hardware must be created to satisfy the huge request in computation that this tool requires. Such a solution can be the so-called "in-memory computing", which is meant to merge the memory component with the computational one. It is possible to do so by using Ferroelectricity of thin films (10 nm), recently discovered in Hafnium oxide (HfO_2). They can be used as the gate of a transistor, obtaining a Ferroelectric Field Effect Transistor (FeFET). This Master's thesis focuses on their electrical characterization, concerning HZO (Hf and Zr oxides) thin films, evaluating several configurations of planar capacitors, MIM and MIS (Metal-Insulator-Metal and -Semiconductor), using different fabrication methods, searching for those which give the best parameters, as the Charge per unit area and the Endurance.

Contents

1 Introduction

1.1 The host intitution

The Laboratory for Analysis and Architecture of Systems (LAAS 🔗) is a CNRS research unit linked with the Institute for Engineering and Systems Sciences (INS2I) and the Institute of Information Sciences and their interactions (INSIS). Located in Toulouse, it is also associated with the University of Toulouse. More than 500 people carry out researches in automatics, computer science, robotics and micro/nano-systems. They are devided in twenty-six teams, spread among six scientific departments, working on topics as optics, energy management, autonomous systems, networks, embedded systems, micro- and nano-systems, biological systems, etc., with various fields of applications. The team that welcomed me is the MPN (Materials, Processes and Nanodevices), especially the members of the NNE (Neuro- and Nano-Electronics) subgroup, included in the MNBT department (Micro Nano Bio Technologies). In particular, the following experiments were done collaborating with the Nanoelectronics team.

Figure 2: Main LAAS-CNRS departments.

1.2 The project

Our daily life depends on electronics since many years now, especially from the rise of "smart" devices, such as the smartphone. Its main objective has always been "performance improvement", and the main way to do so is by miniaturizing its most important component, the basis on which all of this has

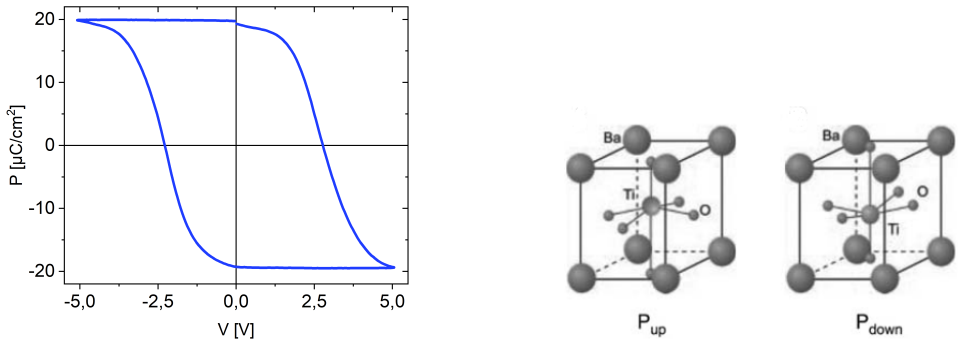
began: the transistor. Indeed, what scientists are looking for is increasing the computational power, for which we have to use many transistors, hence fitting as many as possible on a single chip. This trend is mainly represented by an historical rule, the Moore's Law, which led to the doubling of the number of components per integrated circuit every two years. However, this observation was true few years ago, before starting slowing down when the dimensions involved were reaching the fundamental limits given by semiconductor physics and dissipation issues, so that a new approach was adopted, named "More than Moore". It includes 2 main subcurrents: one oriented towards the exploitation of different materials, such as 2D semiconductors, and different architectures, like vertically oriented transistors; the other focused on the functional diversification, by integrating sensors and actuators inside the chip [1]. Such new approaches are also preparatory to a relatively new research path that has encountered the interest of the mainstream media recently: Artificial Intelligence (AI). Hardware implementation of such tool is very hard, since it relies on huge amount of data and computational components that can't be easily placed inside a small microprocessor. Typically, the AI tools we know rely on very big server farms which they can connect to through the cloud. Such method implies high power consumption due to the heat treatment of the servers and to the constant remote connection [2]. To overcome such a problem we must change the common knowledge about hardware implementation. There's one type of hardware architecture that is dominant right now, and the most used: Von Neumann [3]. Named after the first scientist that described it, it depicts the basic functional structure of a computer, showing its different components and the connections between them. In summary, there are three main parts: the Central Processing Unit (CPU), where the calculations are performed, the Memory, that store instructions about the operations and data to be handled, and the I/O interfaces. Since the beginning, CPU and Memory improved with the same speed, but in different aspects. With a better chip density, the amount of data to be stored in the same area is higher and the CPU is faster. However, this last advantage is mitigated from the memory improvement itself, since having more information implies a more difficult access, hence taking more time. Such a situation is commonly defined as the "memory bottleneck" [3], meaning that the high speed the CPU may offer is limited by the memory access time, and this is a big obstacle for the AI integration mentioned before. In order to decrease the impact of such performance limit, different solution are used, such as the introduction

of cache memory and the memory hierarchy, with the most used information stored at the top levels in order to have a faster access. There's another solution that has been discussed recently, that proposes the merge of the two main components of the processor (CPU and memory): in-memory computing [4]. In this project we will focus on a particular kind of materials, among the possible options [5]: the Ferroelectrics. There is a huge variety of such materials, like the perovskites, but the most intriguing for applications in nanoelectronics it's the Hafnium oxide (HfO_2). This material is already used as oxide layer, since it is a high-k dielectric, and now it allows to have ferroelectric films of few nanometers. By using such material as the gate oxide, one can build transistors with a defined polarization, hence information, that can be stored as memory. The main topic of this Master's thesis will be the evaluation of HfO_2 as gate of Vertical transistors, the last innovation in such field which aims at further reducing the area footprint of the microchip by exploiting the vertical orientation [6]. This is all part of a European project whose purpose is to implement AI hardware for real-time translation of languages, named FVLLMONTI 🔗. The following chapters will then focus on the electrical characterization of Ferroelectric capacitors, showing the best possibilities and process parameters to implement this new technology.

2 FERROELECTRICS: physics and applications

2.1 Ferroelectricity

Ferroelectricity is the property of a dielectric material and it consists in an intrinsic electrical polarisation, named "remnant polarisation" (P_r). It can have two possible directions, Up or Down conventionally, and it can be switched from one to the other by applying a sufficiently high electric field. Indeed, this is a fundamental requirement to demonstrate this type of materials. The field at which the switching happens is named "Coercive field" E_C. The Polarisation graph is non-linear, showing an hysteresis loop (Fig. 3a), the typical kind of curve that all memory devices present, the main purpose of this project. Common dielectrics, in fact, show a linear behavior of the P-E (or P-V) curve, while for Paraelectrics the curve is non-linear, but with neither a loop nor the P_r. Such features are due to the crystalline structure of the material,



(a) (b)

Figure 3: (a) Example of a FE hysteresis loop; one can extract the P_r by looking at the curve when V is zero, the coercive field when P is null. Crystalline structure of $BaTiO_3$, as an example, with both directions of polarisation [7].

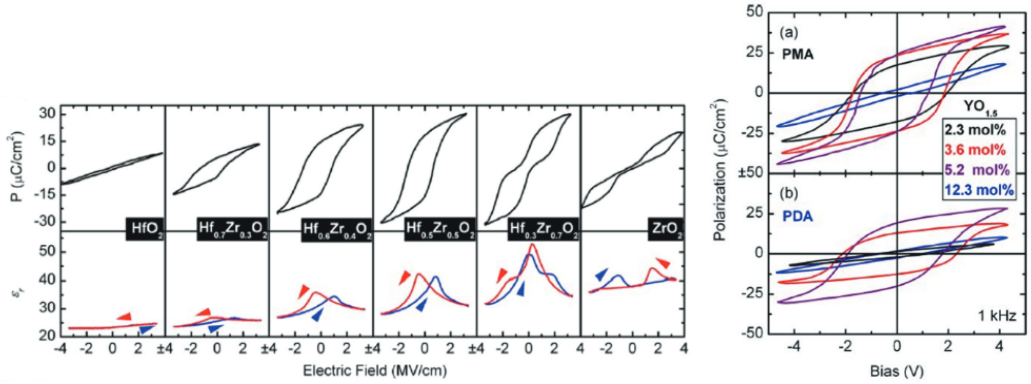
which should present a certain asymmetry in order to have a displacement between positive and negative charges (Fig. 3b). Such structure is similar to that of a Piezoeletric crystal, where the charge displacement is given only after undergoing a mechanical strain, by an external force or by the structure itself. Therefore, Ferroelectrics are a subgroup of Piezoelectric materials. In this way, an insulator may be ferroelectric (FE) only with specific crystalline

phases; the transition temperature from a non-ferroelectric to a FE is called "Curie temperature" (T_c) [7].

2.2 Materials

2.2.1 Hafnium Oxide

The most common type of FE material is the Perovskite, very much used in different kinds of ferroelectric based devices, but the one of interest for our purpose, which revolutionised the common knowledge on FE, is the Hafnium Oxide (HfO_2). A first reason comes from the possibility of making very thin films, with thickness of 10 nm and lower, differently from Perovskites that lose their properties below 100 nm [8]. Another reason is that this material is already known in electronics, since it is used since the 2000s as a high-k dielectric to improve gate thickness without losing anything in terms of leakage [9]. It exists in three different crystal phases: monoclinic at room temperature, tetragonal and cubic at higher temperatures [10]. These phases are all centrosymmetric, hence they can't show FE properties; however, in thin films structures, another one appears, the orthorhombic phase, which, in some configurations, can be non-centrosymmetric, thus not excluding FE. Usually, after annealing, it mostly stabilises towards the monoclinic, since the desired one is metastable in normal conditions. There are, however, specific solutions to obtain a higher percentage of it. One is by injection of dopants, acting as stabilisers, more or less effective depending on their percentage [11]. Common dopants are SiO_2 and ZrO_2, but there are many possibilities still under study [12]. The material used during my project was indeed HZO, 50% HfO_2 and 50% ZrO_2; this substance is defined as Zr-doped, even if it is more like a composite. Its 50-50 composition revealed to be the most effective in terms of polarization, as depicted in Figure 4a. Another solution for the stabilization is the so-called "metal capping": it consists in placing a metal layer over the dielectric, after used as the electrode, before performing the annealing; in this way, when the temperature rises, a mechanical encapsulation due to the capping increases the probability of the orthorhombic phase, reducing that of the non-ferroelectric monoclinic one [11, 10]. These methods are not strictly necessary to get a FE layer, HfO_2 can show such characterisics even without them, but with less interesting results (See Fig. 4b), especially looking at possible applications. A comparison between some tested materials is in Table 1, and it can be seen that HfO_2 is the most promising one right now, at least for a low power objective.



(a) (b)

Figure 4: (a) Evolution of hysteresis loop and dielectric constant with respect to the doping [11]. (b) Comparison of polarisations between HfO_2 Y-doped samples with different percentages, being capped (PMA, Post Metalisation Annealing) and not capped (PDA, Post Deposiotion Annealing) [11].

2.2.2 Aluminum Scandium Nitride

An alternative to HZO has been recently studied, it is the AlScN (Aluminum Scandium Nitride), a wurtzite structure material, with good FE features [13]. It has, indeed, a remnant polarisation that is very stable with temperature, a high coercive field, useful for a good memory window in memory applications, and various method for its deposition, compatible with those already used in electronics. The huge coercive field is also a disadvantage, but it can be widely adjusted by varying the Sc content or by acting on the thickness. In fact, it has been proven that it can be very thin, even 10 nm. Unfortunately it reacts very easily with the oxygen in the air, creating an oxide layer that impacts on the performances [14]. It is even compatible with GaN, and III-nitride materials in general, hence very interesting for high performance electronics [15].

2.3 Points of interest

Literature suggests that fabrication conditions as the annealing temperature, pressure and atmosphere are of great importance for the FE phase formation. The annealing can be performed in the range 400-1000 °C, but some studies noticed that higher temperatures weaken the FE properties [16], and also affect

	SBT	PZT	HfO_2	$AlScN$
Film thickness $[nm]$	>25	>70	5-30	>=10
Annealing temperature $[°C]$	>750	>600	400-1000	>600
P_r $[\mu C/cm^2]$	<10	20-40	1-40	80-150
E_c $[kV/cm]$	10-100	50	1000-2000	2000-5000
k	150	1300	30	10-16

Table 1: Comparison between parameters of different ferroelectric materials for thin films

the endurance [17]. Such results are attributed to the interfacial layer which grows during the annealing phase, especially with higher temperatures. This growth may weaken the layer and concentrate more voltage on itself, reducing the drop on the FE. The best range was, then, decided as 400-600. Concerning the atmosphere, N_2 is generally used, because the annealing step performed with oxygen seems to modify the oxygen vacancies distribution, which are important for the FE phase stabilization, hence it worsens the performances [18]. Indeed, oxygen vacancies are considered as one of the main reason behind the cycling behaviors of ferroelectrics, like wake-up effect and fatigue. These two phenomena are complementary: the first one is the increase of the P_r with the number of measuring cycles, the other is its decrease [18]. The reason behind such effects may be due to the elevated charge trapping that this type of defects can perform, which are released with time. Finally, the leakage is an important parameter to consider during the tests. It is probably caused by the aforementioned charge trapping. In fact, the gate stack can be considered as a capacitive voltage divider, where the highest voltage is across the intermediate layer, the oxide between the FE and the substrate. This high voltage allows the bending of the energy bands and, consequently, charge injection. Such charges act both as screen versus the polarization switching, having a big impact on the field effect of a transistor, and degrade the oxide, affecting the endurance. On the other side, these injected charges are transient, hence they have the tendency to leave with time or with a sufficiently high voltage.

2.4 Ferroelectric memories

There are three main configurations that can be used to implement a FE memory [19], showed in Figure 5.

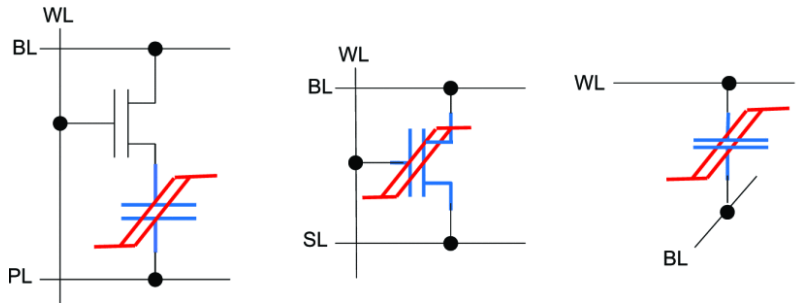


Figure 5: Possible configurations of a FE-based memory cell; from left to right: FeRAM, FeFET and FTJ [19].

FTJ The most exotic idea is the Ferroelectric Tunnel Junction (FTJ). Same principle of the more widespread Magnetic version (MTJ), it works by exploiting the polarized FE layer which separates two metal electrodes and acts as a tunneling barrier. The current flowing across the cell will have an intensity which depends on the polarization direction [20]. It requires a very thin FE layer, of 3 nm maximum, not easy to make; it needs further studies [19].

FeFET Another possibility is to implement the FE thin film in the gate stack, in this way, its polarization will influence the threshold voltage of the transistor. In order to have an effective memory cell, one needs a large enough Memory Window (MW), so to well distinguish one state from the other. To have such condition, a high coercive field is mandatory, like the one of the Hafnium oxide. As said before, this material is already a standard dielectric in electronics, a perfect starting point. This configuration is the main objective of this project because, as it can be seen in Figure 5, it has a 1T cell, hence very small, especially if coupled with the vertical nanowire transistors. There is also an alternative version which couples this type of transistor with a conventional capacitor [21]. These two components are fabricated in places physically separated, but electrically connected. One will be made during the FEOL (FrontEnd Of the Line) module, the other during the BEOL (Back-End...) one. Being dissociated in this way, one can exploit fabrication conditions which the other component, or module, may not withstand.

FeRAM A good alternative is the FeRAM, which works with the same principle of the DRAM. The configuration is simple, a 1T-1C, with the capa-

citor's dielectric substituted by the FE, which grants non-volatility, even if the reading remains destructive, a small disadvantage with respect to the other configurations.

3 Experimental process

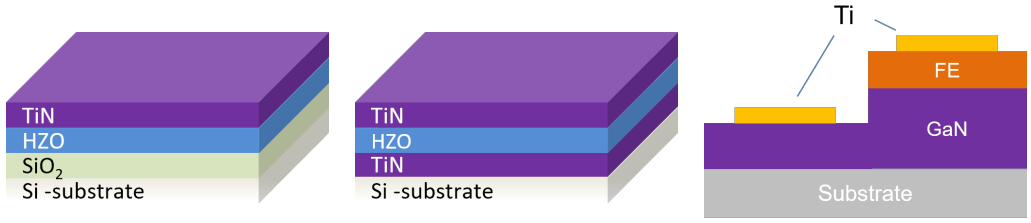
3.1 Main objective

In order to be able to implement a ferroelectric thin film as the gate of a transistor, we started from the basis, testing the behavior of planar FE capacitors. After having illustrated the basics of a FE device in the previous sections, the following ones will show their electrical characterization setup, to check if they present a remnant polarization and their endurance, comparing different fabrication procedures. Very recently, they started to fabricate directly at LAAS, although many samples come from two other institutions specialized in their production, which collaborate to the project.

3.2 Samples

The objective of this Master's thesis is to test the performances of different configurations of planar capacitors, varying by structure, fabrication methods and FE materials. The basic idea is to test the FE thin films and find the best parameters, to use them in future vertical structures and, finally, as the gate of a real working transistor. We have three main types of samples: Metal-Insulator-Semiconductor (MIS) and Metal-Insulator-Metal (MIM[1]), concerning HZO as FE material, on a Si subtrate, and a MIS-like sample which uses an heterostructure between $Al_{0.85}Sc_{0.15}N$, as FE, and GaN, all on a Sapphire substrate. While the MIM configuration reproduces a real capacitor, the MIS is meant to study the behavior of the FE layer as gate of the transistor, hence having the Si substrate acting as the bottom plate of the capacitor. The MIM type is studied looking at the alternative FeFET memory configuration explained earlier (Section 2.4). Each type has its own topology, due to the laboratory it comes from. The HZO-based capacitors have a similar ones, with lines of 10 round contacts, each row with different dimensions, in two

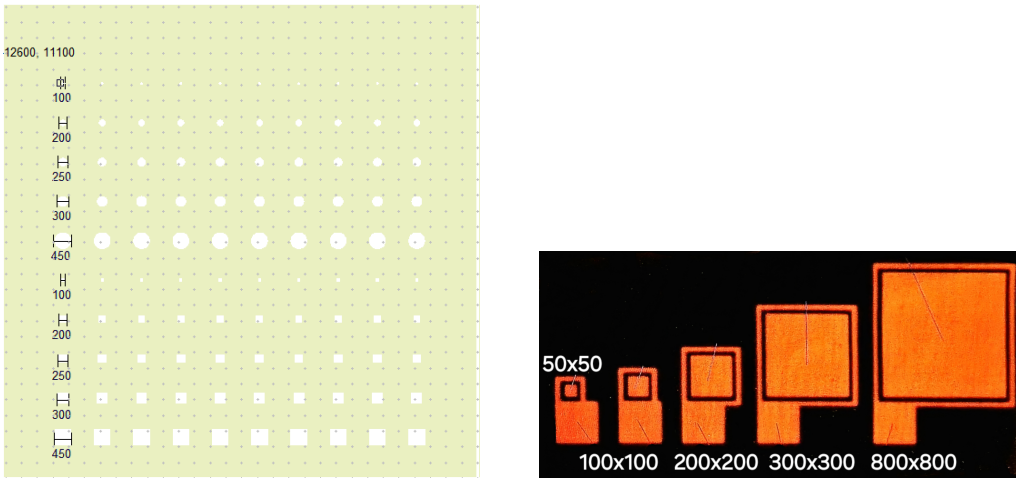
[1]Also defined MFS, MFIS or MFM in the literature, meaning Metal-Ferroelectric-[Interlayer-]Semiconductor/Metal



(a) (b) (c)

Figure 6: Capacitor's structures: HZO (a) MIS, same basic structure for both laboratories involved, and (b) MIM and (c) AlScN-based MIS.

shapes, squares and circles (Figure 7a). The topology related to the other FE has a more elaborated configuration, with top and bottom contacts already implemented; they do not need, then, a sacrificial contact to be burnt in order to perform the measurement. Concerning the HZO devices, for each of them there are multiple samples, distinguished by the annealing temperature that was applied during the process flow. This was done in order to check the best temperature for the best result. The best range to get a good working capacitor is 400-600, according to the literature (Section 2.3), and those taken are four: 400, 500, 600, 700; the last one in order to confirm the above mentioned range. Since during previous measurements the 600 resulted as the most promising one, this was fabricated with two further variations, which concern the temperature ramp-up, i.e. the speed at which the temperature rises: 20 and 50 °C/s (slow and fast), named 600s and 600f samples. In the end, we have five samples, concerning the MIS capacitors, while the MIM ones are all made using the fast annealing. All of the HZO layers are made with a 10 nm thickness, while the AlScN has three samples with different thicknesses: 7, 12 and 17 nm. Moreover, they could be distinguished by where they were produced: some of the MIS were produced at LAAS, with different fabrication procedures, the others and the MIMs from another collaborating lab, which will be referred to as "External lab 1". The last type comes from another collaborator, External lab 2. During the last few weeks, a new type of sample from the External lab 1 arrived, with a new fabrication method which is meant to improve the capacitor's endurance. It is defined Multi-level and it simply separates the HZO 10 nm layer into two of 5 nm with a very thin



(a) (b)

Figure 7: Topology of planar capacitor's samples. HZO MIS (a) and AlScN MIS (b); the dimensions are referred to the square on the top, the top contact.

layer, 1 nm, of an oxide between them, Al_2O_3 in this case [22]. This additional component should not modify much the FE properties of the capacitor, but it is meant to separate the leakage paths across the FE layer, as shown in Figure 8, hence slowing down the breakdown due to cycling. Finally, LAAS' devices were all made as the 600f, with differences in the HZO deposition. The samples are three, two deposited thermally, at 280 °C, one through a plasma medium, always at 280 °C. The two thermal samples are distinguished by the deposition ratio of HZO: "1:1", it means that one layer of HfO_2 and one of ZrO_2 are deposited alternatively, and "5:5", meaning that the deposition is 5 layers of one oxide, then 5 layers of the other and so on. In this way, we keep having 50-50 of Hf and Zr, but with a slightly different configuration. The plasma sample has only the 1:1 ratio.

3.3 Fabrication process

The process flow between the different devices obviously changes from one to the other, but, in general, they follow a similar sequence of steps. Since it

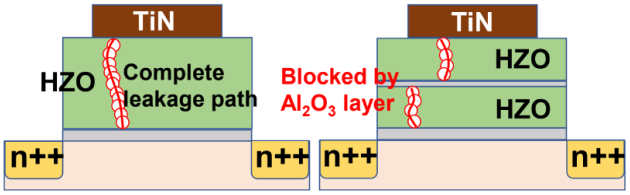


Figure 8: Example of the intermediate oxide layer efficacy, which blocks the propagation of the leakage path that would bring to dielectric breakdown [22].

is not the main objective of this thesis, the detailed steps cannot be totally described, but they can be easily deducted since a planar structure is involved (Fig. 9). The following steps are for the MIS type, since the other types are not fabricated at LAAS and the process is not known completely. Starting by a doped Silicon wafer, it is placed inside an oven for a controlled thermal oxidation, the best way to obtain an electrically good layer of SiO_2 on the surface (1.5 nm). This layer is needed in order to improve the lattice matching between HZO and Si, for better performances, having less defects at the interface [23]. Such configuration is defined as Metal-Ferroelectric-Insulator-Semiconductor (MFIS) type, different from the MFS type (also called MIS)), where only the FE is present as the insulator layer. The MIM type will probably have the bottom contact of TiN deposited at this point, made like for the top one, explained in few steps. Through Atomic layer deposition (ALD) at 280 °C, the Hf and Zr oxides are deposited, forming the HZO 10 nm layer. At this point, it doesn't have its FE properties yet. It needs the metal capping, made of Titanium Nitride (TiN), in our case, deposited by ALD too, reaching a thickness of 13 nm. At this point, the sample had already pass through a lithographic step, to print the desired topology on the surface. The Rapid Thermal Annealing (RTA) is then performed, to have the transition to the tetragonal phase, that cooling down will stabilise to the FE orthoghonal one. The presence of TiN as metal capping promotes the formation of such phase, as explained in Section 2.2.1. Different choices of temperature are available, with differences given also by the ramp-up, meaning the speed the sample takes to reach the temperature. The range studied is between 400 and 700 °C, with ramp-up of either 20 °C/s (slow) or 50 °C/s (fast). A thin layer of Titanium for the subsequent deposition is then deposited, thus the metal contact is sputtered on it, typically Platinum or Chromium.

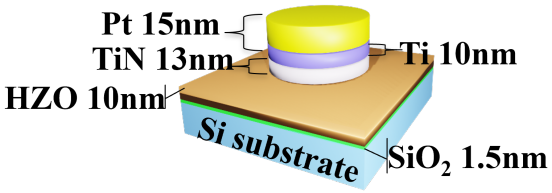
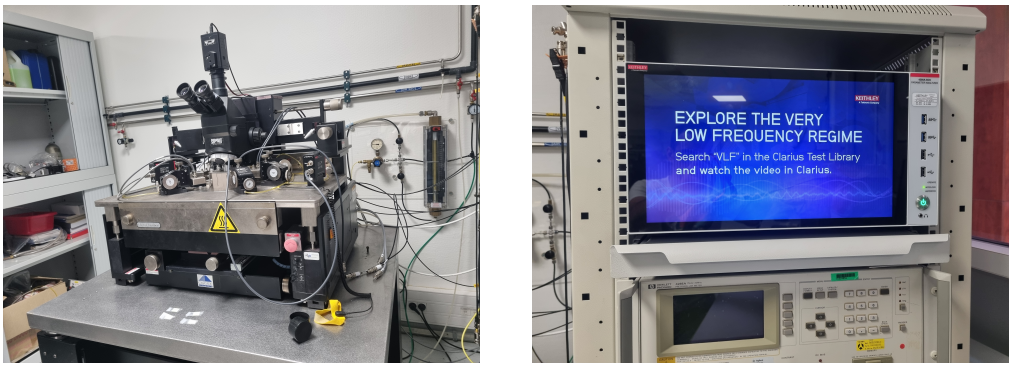


Figure 9: Structure of a single MIS capacitor with all the thicknesses reported.

3.4 Electrical measurements

3.4.1 Equipment



(a) (b)

Figure 10: Instruments used for the characterisation: Cascade 12000 (a), Keithley 4200 (b).

The electrical measurements were performed inside a dedicated room called "Characterisation platform". It is frequented by several teams, both internal and external to LAAS. There are several stations for electrical analysis, but also for RF, optical and biological measurements. The entire environment is connected to the same ground, for precision of measurements and for a safety purpose. Here, the instruments needed were two. The first one is the *Cascade Summit 12000*, in Figure 10a. It is an electrical characterisation station with six probes, made of Tungsten, and a microscope for their positioning, with also a digital camera, connected to a monitor. The sample have to be placed on a moving disc, inserted inside the machine, after applying the vacuum

to avoid the sample to move, and positioned close to the probes through a software, essential to make the machine working. Since the probes are very fragile, everything must be done carefully, following a specific procedure. The probes are connected to another instrument: the *Keithley 4200*, a waveform generator and analyser (Figure 10b). It's a very modern machine provided with several programs, each for a specific measurement approach. Everything can be settled up through the embedded software and the measurement is provided as a graph on the screen that can be exported in the '.xls' format, for better data treatment. On this point, some Matlab scripts were written by me, in order to handle easily the big amount of data that is generated every day. Another software very much used was Origin, a powerful software that allowed to create all the graphs of this report.

3.4.2 Formula

In order to well characterise a Ferroelectric capacitor one needs to know the amount of charge it can store, given by the polarisation: the amount of charge per unit area (C/m^2). To get such a value there are two main approaches. The direct one, that is exploited through the Sawyer-Tower circuit configuration [24], measures the directly related potential of the capacitor. Here it is used the indirect one, more common, which needs a current measurement $i(t)$, related to the polarisation $P(t)$ through a time derivative. The equation is the following:

$$\frac{\int_0^T i(t)\,dt}{A} \tag{1}$$

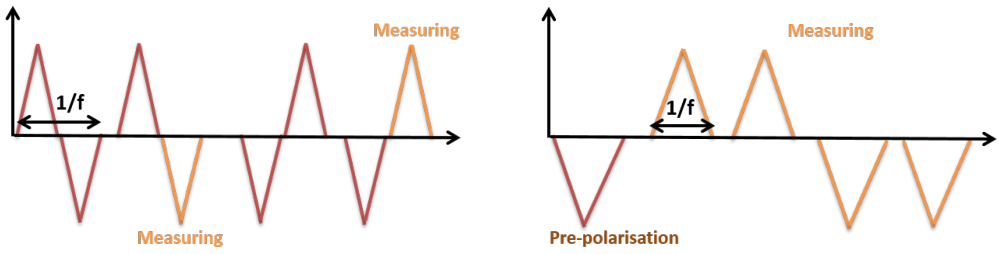
with A as the area of the metal plates. It is all calculated through the newly implemented script, which takes into account parameters as the pulse frequency, the number of measurement points and the surface area. Then, since the result gives a curve on the negative part of the y-axis, a necessary correction was introduced, which centers it in the origin. Most graphs will be represented with respect to the voltage rather than to the electric field, but the conversion from one to the other is quite immediate. By having a 10 nm thick FE layer, moving from Volts to MV/cm passes through the following:

$$\frac{MV}{cm} = \frac{V}{10nm} = \frac{V}{10^{-8}m} = \frac{V}{10^{-6}cm} = \frac{10^6 V}{cm}$$

hence the conversion is 1:1.

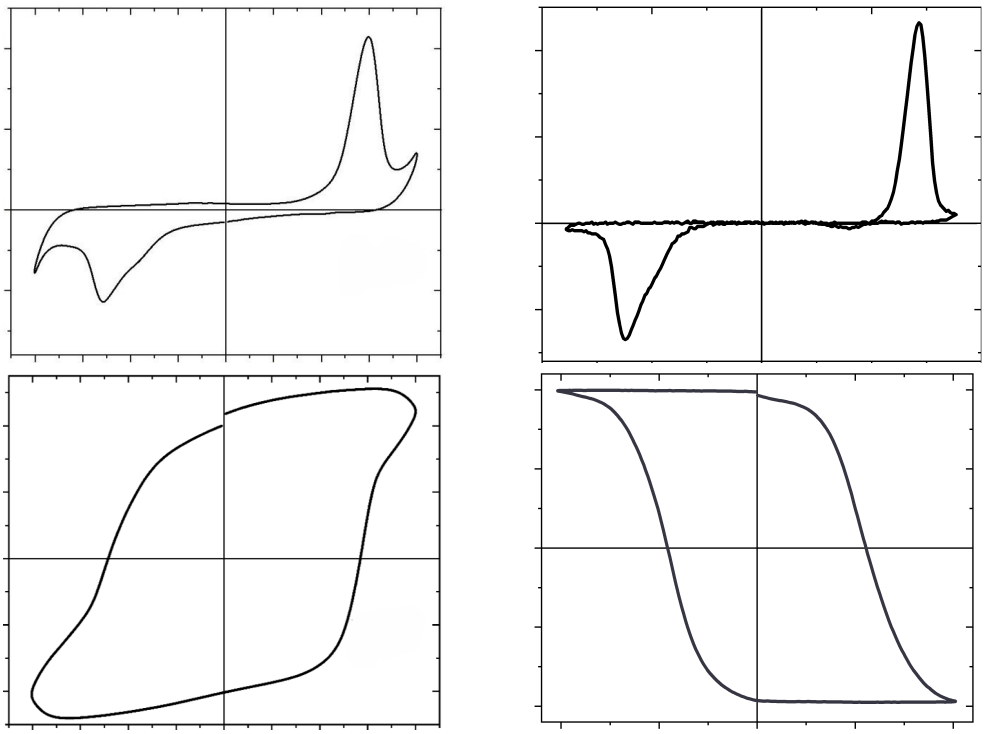
3.4.3 Approaches

As said before, the measurement of the current is needed to get the polarization. To do so, voltage pulses are sent through the contact to measure the response, that is the result of the charge switching inside the capacitor. There are two main sequences of pulses that are used for FE materials: Dynamic Hysteresis Measurement (DHM) and Positive Up Negative Down (PUND) [25, 26]. The former (Fig. 11a), is accurate in the case of ideal materials, since the measurement includes, in addition to the response due to the polarisation reversal, other parasitic factors, caused by the dielectric charging, that increases the final value of polarisation (Fig. 12a). To overcome this issue, there is the second method, which includes, after the electrical measurement, a subtraction of the extra components. This is due to the method: the sequence of pulses is composed by an initial one, useful for the pre-polarisation, in order to have a subsequent expected behavior, and 4 others, as in Figure 11b, during which we perform the measurement. In this way, for each direction of polarisation, there is a first set of measurement points that should show the switching peaks and a second one that has only the capacitive effect and the eventual leakage. At this point, by subtracting the two sets, a clean response of the ferroelectric sample is obtained (Figure 12b). In both cases, triangular waves were used, without a specific frequency, but 1 kHz was the typical one, to check if the contact was working, while the amplitude was generally 6.7 V, but also both lower and higher values were used.



(a) (b)

Figure 11: Waveforms of measurement pulses: DHM (a) and PUND (b).



(a) (b)

Figure 12: Current and Polarization responses of DHM (a) and PUND (b); They can be distinguished mainly by the peculiar shape of the respective hysteresis loop.

3.4.4 Procedure

The measurement is performed by putting the points at each electrode, that will both send the signal and measure the response, through a PMU (Pulse Measurement Unit), embedded in the Cascade machine. The available topology doesn't have an access to the bottom contact from above, therefore one can either use the conductive plate where the sample is placed, or pass through another contact, which must be burnt before, in order to not have a superposition of the responses. The first option introduces a lot of leakage in the measurement and it was used only at the beginning with the DHM method; after, PUND was used, adopting the other option. In this case the direction of the current should be considered (hence the position of the burnt contact

with respect to the working one), even if only the I-V curve is affected, while the polarization doesn't have important changes.
The objective of our studies on FE is as non-volatile memory, therefore several characteristics must be respected:

- Power consumption mainly depends on the material used; this wasn't the main concern of my project part, but the Coercive voltage and the leakage of the measurement were always considered as parameters, which are two of the main contributors;
- Endurance, one of the main points of interest, it's the maximum number of switching that a device can withstand;
- Retention, a component that is tested by other labs, it's the capability of the device to retain data in time; usually is measured as more than ten years;
- Read/Write speed was not considered, it will be more important when applied to the FE transistor, but it can be deduced by the response with different frequencies, that will be explained later;
- Cell's size should be the main advantage of using HZO, because the objective is to implement it as the gate of a transistor, as a 1T technology

The first objective, needed also to get comfortable with the equipment, was to make a Mapping of the contacts of each sample. It simply consisted in checking, for a good amount of contacts, the working ones, i.e. with ferroelectric properties. In this case the measurement through the plate was used. The next step for a good electrical characterisation of the capacitor is to know its Endurance, meaning, the number of switching cycles that the device can withstand before the breakdown. To do so, it is necessary to know the best interval for a good polarization (80-100% of P_{max}, the highest stress) in terms of pulse frequency, since there is a specific relation between them [27], and then applying it for the endurance cycling.

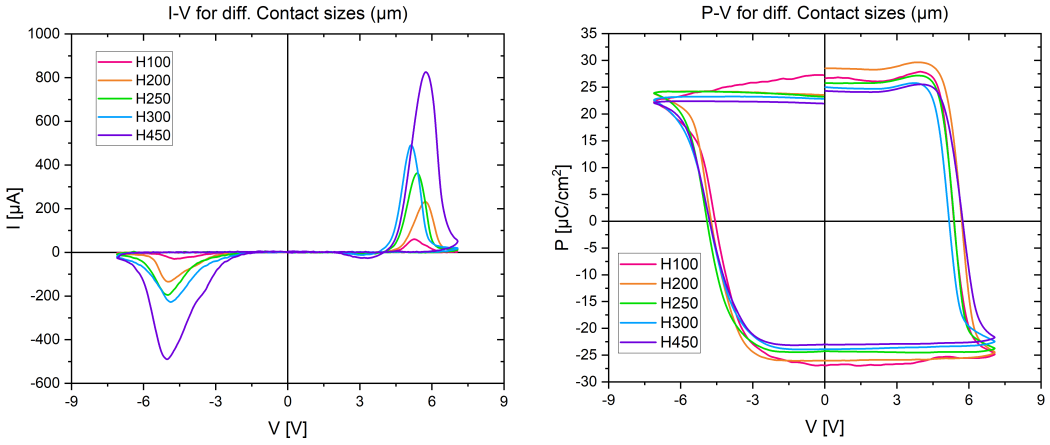
4 Results

The first task to complete was the mapping of the contacts, hence to check few working ones for each line of each sample in order to perform the desired tests

after. This was done on the MIS samples from External lab 1, the first ever measured. It was intended as a training, to get used to the instrumentation, but it is actually needed each time a new sample has to be evaluated. To do so, the DHM approach was used, taking the measurement between the desired contact, on the top, and the metal plate under the sample; this method introduces more leakage due to the great dimension of the plate, but it didn't interfere with the purpose of the experiment. Having this task completed, some comparisons could be immediately made, as the results obtained from the different contact sizes. As expected, the higher the diameter the higher the current (Fig. 13a), since it implies a bigger capacitor, hence a bigger charge stored and then switched, as given by the formula

$$C = \frac{\epsilon S}{d}$$

where d is the distance between the plates, S is their surface and ϵ is the dielectric constant. As it can be seen by Figure 13b, the polarization changes differently, reducing as the contact area increases; since the polarisation is the charge per surface area ($\mu C/cm^2$), it acts as a normalisation with respect to the area. However, one can notice that the smallest diameter has a less smooth curve and the h200 one has the highest value of polarisation; this is the reason why, from now on, almost all measurements will refer to this specific contact size. The probes may have a role in this, since they are placed manually and their dimension is comparable to the h100 contact, hence the human error in the positioning may have influenced it. According to the literature, an expected result for polarisation is a value between 10 and 40 $\mu C/cm^2$ [28], in the higher part in the case of MIMs, lower for the MIS. Many times the showed results are obtained through the DHM technique, even if not specified, it is possible to deduce it from the shape of the polarisation curve and from the values, that are higher than those obtained with PUND. In the case above, PUND is considered. In more recent papers, on the contrary, the type of measure is specified, but, unfortunately, all of the experiments are made on MIM type samples, that have better performances and so are difficult to compare with MIS. They are, instead, considered more in FeFET experiments, which often are focused on the transistor's parameters, more than the FE's ones. Concerning the endurance, MIS are attested on 10^5 at most, without innovative improvements, while MIMs are more towards 10^9 [29, 30, 31, 32]. Final remark, many values obtained with the MIS are on samples annealed at



(a) (b)

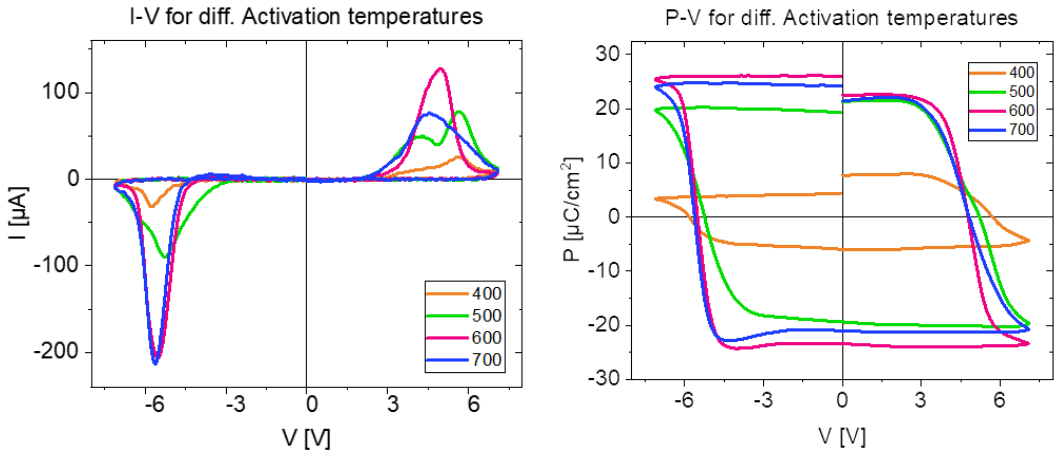
Figure 13: PUND measurement from a 600f sample, with the different contacts. The number indicates the diameter of each one of them; H is for circular contact (SQ, square, for the other type of shape)

400 or 500 °C; higher temperatures are used on samples with different doping materials, which require such conditions [11].

4.1 MIS from External lab 1

The first interesting result is the asymmetry between the peaks height, given by the different materials implied, a metal (top contact) and a semiconductor (bottom contact), due to a different behavior of the carriers inside this last type of material. Concerning the coercive field (in Fig. 14a represented as the coercive voltage), it is quite high, slightly lower than 6 V. This is not very good in a low power application perspective and it doesn't have a counterpart in the literature, where the typical values do not get over 3 V [33, 19].

Annealing temperatures Focusing on the single sample, one can notice good performances for the highest temperatures (600 and 700), with a better shape of the peaks for the 600 one, since the 700 has a less sharp peak. This is given by a not efficient switch of polarization in that direction, probably due to not yet defined FE domains that can be improved with cycling, exploiting the so-called wake-up effect (see Section 2.3). It is due to such domains also



(a) (b)

Figure 14: Comparison between the different annealing temperatures; PUND measure at 1 kHZ. It is visible the best behavior of the higher annealing temperatures, especially the 600.

the behavior of the 500 sample, that is the only one that presents multiple peaks in several contacts. Such a characteristic appears when a sample has localized domains, which are not affected by the applied voltage in the same way, and so they switch at different values, creating multiple peaks. This phenomenon appears more often with the thicker perovskites, more subjected to such independent domains [7]. In the end, 400 seems the least efficient temperature: the switching peaks are very low and less defined and, as a result, the polarization is very small (less than 10 µC/cm^2). Speaking of that, for all the samples, it spreads between 8 and 25 µC/cm^2, in good agreement with the above mentioned literature, with the 600 that results as the best candidate temperature. Also the 500 is interesting for the double peaks, which could imply a specific application in memory, since it could be used for multiple bits storage (Multi-Level Cell, MLC), further increasing the density [34]. However, in most of the cases they are very close together and on one side only. Such double peaks often appear at a lower coercive voltage then the other samples (Table 2), hence it may be a good advantage for power consumption and endurance. Further studies are needed. While the values are very close to the literature ones, the trend is different, since in some cases they have a maximum of polarization already for a 400 sample [17], and it lowers with

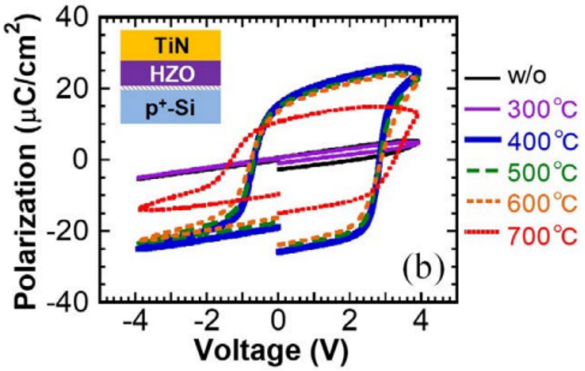
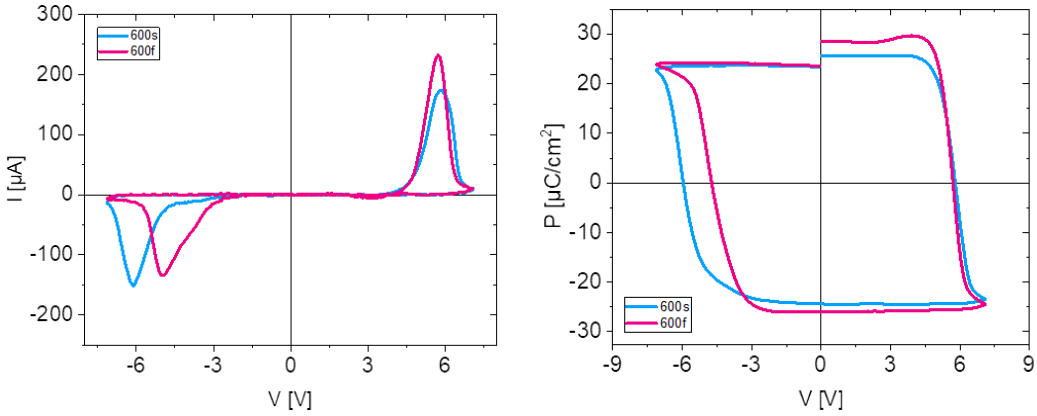


Figure 15: Results of MISs activated with different temperatures, from the literature [17]. One can notice the different trend obtained with respect to the External lab 1 samples.

higher temperatures (Fig. 15), according to the annealing effect explained in Section 2.3. It is not clear the reason behind this difference in the behaviors, since the fabrication parameters are very similar. At the same time, two other samples together were compared, both having the same annealing temperature (600), but with a different ramp-up, fast and slow: 600f and 600s. The best solution obtained is also the one used in the previous comparison with the other temperatures. The difference between the two resulted not being very big. In terms of coercive field, the fast one performs better just on one side, but since the other side has an higher coercive field, the advantage is not useful: the voltage sweep would be symmetrical anyway, with highest voltage prevailing. From the polarization point of view, the slow sample has a slightly lower P_{max}; the interest is then moved to the fast ramp-up.

T [°C]	V_C [V]	P_r [μC/cm^2]
400	6	10
500	3.7 / 5.5	21
600	5	25
700	5	23

Table 2: Parameters of interest of the MIS samples, all taken with 6.7 V sweeps and 1 kHz.



(a) (b)

Figure 16: Comparison between the two different ramp-ups; as said, the difference is not huge, but the 600f has a slightly higher polarization.

Voltage sweep With this acknowledgement we moved to further tests on this sample. Firstly, evaluating the behavior of the polarization by changing the range of the voltage sweep. One can notice that the value of the polarization is strongly influenced by the maximum voltage at which the contact is switched, increasing linearly with it, as in Fig. 17. The voltage acts slightly on the coercive field too, which increases with it, on the order of 100 mV per Volt. As a result, we must take into account the sweep when comparing with the state of the art, because a higher polarization may come from a higher applied voltage. Concerning the aforementioned values from the literature, all the experiments were done with a 4 V sweep [17].

Endurance The next test is the Endurance, meaning how many times the sample can switch before burning. This type of test is preceded by one about its behavior in frequency, the switching time test, in order to find the best frequency to perform the switching. The range of testing was from 200 Hz to 100 kHz, taken from a low enough frequency, at which there is the complete switching, to the one at which there is not, approximately. The remnant polarization is stable enough (80-100%) until 25 kHz, when it starts to drop significantly (Fig. 18a). Checking only the P_r can be misleading because, if we check on the current, one of the two peaks is outside of the voltage range, hence the switching doesn't happen in that direction. A good frequency before

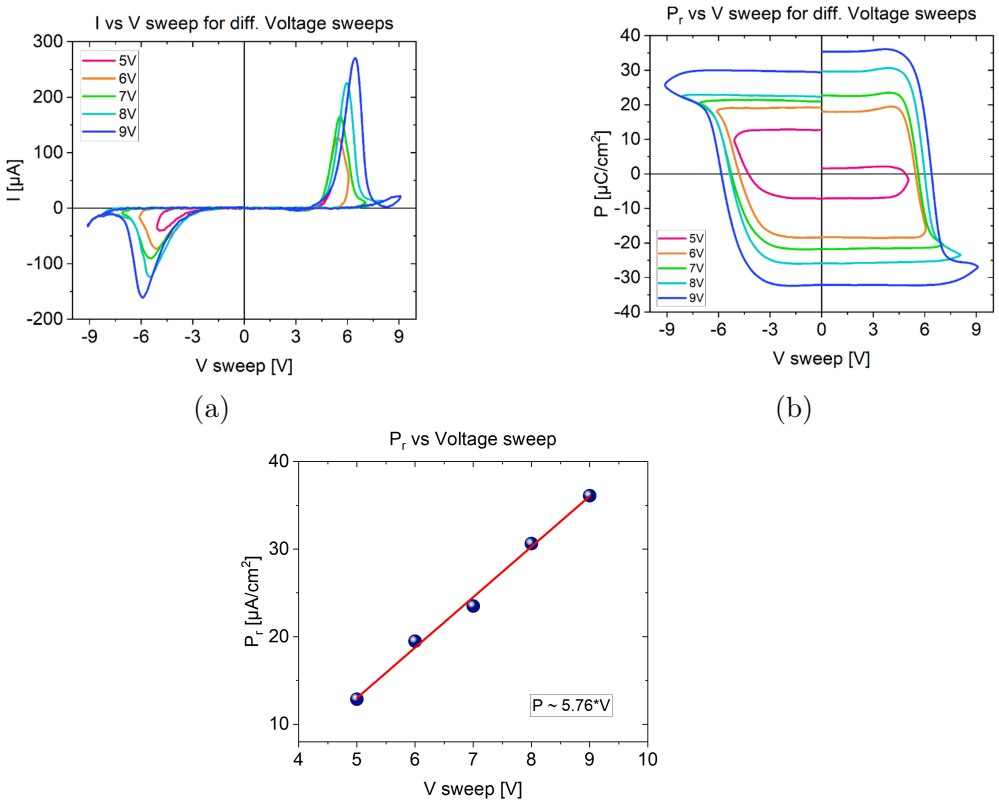


Figure 17: Results of different voltage sweeps on the 600f sample (a-b); PUND measurement at 1 kHz. There is a linear dependence between Voltage and Polarization, with a coefficient of about 5.8 (c).

such a thing happens is 10 kHz, that will be used for the next test, together to the one for the 100% switch. In general, the frequencies used to show results in the literature are 1, 10 or 100 kHz, similar to what we have found. Assuming that, the next task is to perform the actual endurance test, with 100% and 80% polarization, in order to test different stresses, that may influence the results. As shown in the first two graphs of Fig. 18, the sample maintains a stable polarization of 25/30 µC/cm^2 until the breakdown, which happens at 10^5 cycles, very low for the purpose of our research, but in accordance with the literature results described above. With the 10 kHz test it is barely visible the wake-up effect; since switching with higher frequency means doing it faster,

not all the domains are involved, the material undergoes less stress and needs few cycles to stabilize its polarization.

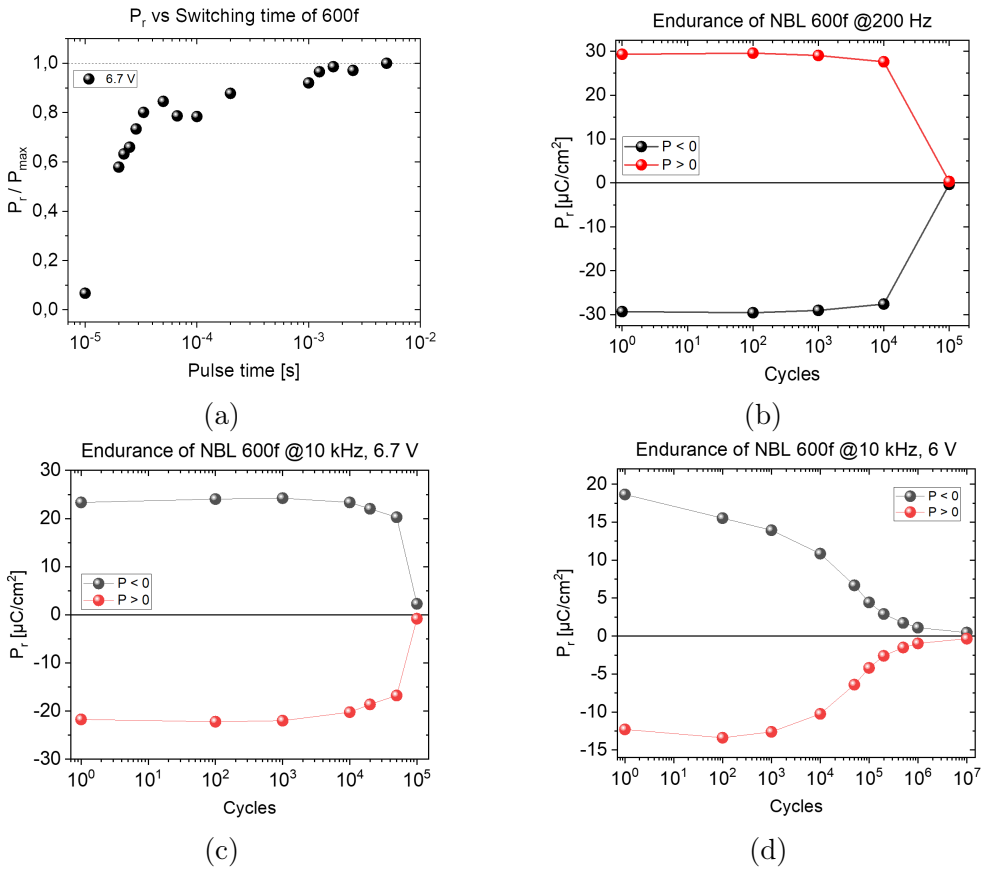


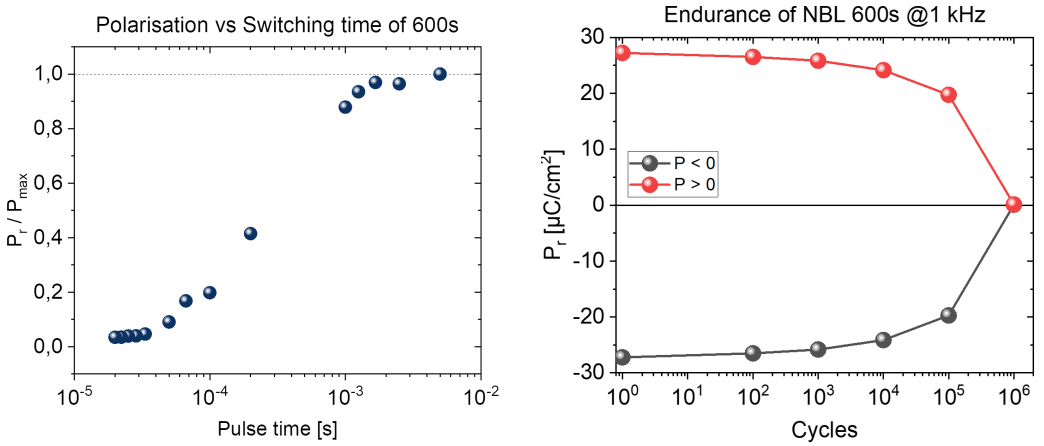
Figure 18: (a) Switching curve of the 600f vs time; it slowly decreases until 10 kHz, then it is abrupt. It also depends on the voltage sweep, because at high frequencies the switching happens out of range. Endurance tests of the 600f sample, performed at 200 Hz (b) and 10 kHz (c), in order to cover different percentages of polarization. Then, a test was done by reducing the voltage to 6 V (d).

In this case, the improvement between complete and partial polarization does not exists: evidently, the high switching voltage has a major role over the frequency on the degradation of the sample. Indeed, the main influence on endurance is the voltage across the intermediate dielectric layer, more than

that across the FE one. This situation allows a large charge injection inside the material that are detrimental, even screening the effect of the FE switching during the measurement.

Improvements There are several improvements to reduce this inconvenience, a simple one is the reduction of the voltage sweep as much as possible. A sweep of 6V was, indeed, tested, at 10 kHz, shown in Fig. 18, on the right. The sample didn't go through a breakdown until 10^7 cycles, but it is clearly visible a polarization fatigue already after 10^4 cycles, when the peaks started to become lower and lower. Another solution could be the annealing temperature, since it is demonstrated that a high one reduces the quality of the IL, which further grows with a poorer quality during the annealing step [17]. This introduces a trade-off between endurance and polarization: a lower temperature is needed to preserve the IL so to have a longer life of the device, but a higher one gives a better polarization. The possibility was not fully tested, but the 500 sample could be a good starting point, since it has even multiple peaks, some at lower voltages. A further endurance test was done on the 600s sample (slower ramp-up). In this case, the preliminary switching time shows great degradation of the P_r already after 1 kHz, at which it is around 90% (Fig. 19a). Therefore, the endurance test was performed at 200 Hz and 1 kHz. By looking at Fig. 19b, it shows interesting results, because, when not fully polarized, it reaches 10^5 cycles, one order of magnitude greater than the case of the 600f. Further studies are needed to get a clearer idea. A preliminary idea could be that the slower increasing of the temperature has a similar effect to the use of a lower temperature, causing less stress to the device. It has to be noticed that, in spite of resisting better to the same frequency of 1 kHz, hence the same stress, at higher frequencies the polarization already decreases of a great amount.

Improved batch A better improvement approach is to tailor the voltage divider across the gate stack by minimizing the voltage drop across the IL. It can be done by using a material with a higher dielectric constant or by changing the geometry of the gate stack. On this principle is based the second batch of MIS from External lab 1 (See Section 3.2). The electrical measurements are still ongoing at LAAS, because it is a very recent device structure that has just started to be studied. The first results obtained show a very high resilience, since the measurement was performed between two contacts at up to 40 V without any breakdown. Unfortunately, until now there is no evidence of a



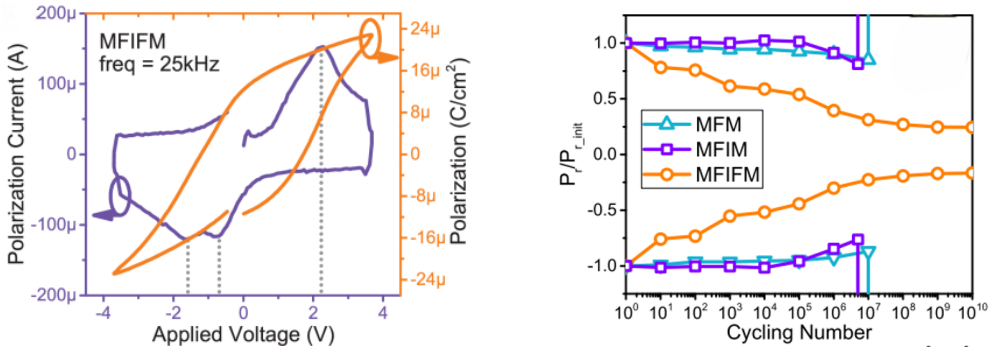
(a) (b)

Figure 19: Switching time (a) and Endurance (b) tests on the 600s sample. Better endurance results were obtained, but with a less stable polarization with respect to the pulse time.

ferroelectric behavior on our samples, at least in the usual range of frequencies: from 1 to 100 kHz. According to the literature, the results are not very different from the classical configuration, concerning P_r and E_C, as depicted in Figure 20, with a P_{max} of about 23 $\mu C/cm^2$ and a slight increase of the Coercive field [22] (it is a MIM in this case). On the other hand, the Endurance reaches 10^{10} cycles without breakdown, showing, however, an evident fatigue effect.

4.2 MIS from LAAS

Polarization LAAS production is focused on testing different methods of fabrication, concerning the FE deposition and the device structure (Section 3.2). From Figure 21 one can notice a quite linear behavior with respect to the pulse frequency, not showing clear steps from good polarization to a degraded one. Table 3 contains the values of the remnant polarization, that results to be very low. In the samples of the External lab 1, at such small values, the behavior was linear-like too, because it was in the part of the graph which was quickly decreasing to zero. Indeed, the polarization here is very small, also due to the smaller voltage used. 5 V was the highest possible value for the sweep, because higher values would directly burn the contact. Anyway



(a) (b)

Figure 20: (a) Example of I-V and P-V curves of the new proposed configuration of capacitors. P_r and E_C are slightly worse than the usual structure, but it allows an endurance higher of three orders of magnitude (b). The measures were taken with a 4 V and 25 kHz pulse, on a 10 nm HZO-based capacitor, probably using a DHM measurement.

the peaks due to the displacement current are clearly visible, with a E_C lower than before. The two batches of External lab 1 and LAAS are not easily comparable, because one does not switch with 5 V, while the other can not go over it. However, in Figure 17 one peak is visible and gives a polarization of around 10 µC/cm^2, higher than the LAAS one.

Endurance The fragility is clearer with the endurance test, done at 1 kHz, not fully polarized. It reaches 10^4 maximum, even lower with some contacts. The most promising sample is the thermal 5:5, more consistent between different measures and with the best endurance results; it even seems to have a very good symmetry of the coercive fields. The plasma one, instead, was the only one that could be used at 6.7 V as the batch of External lab 1, but the results are worse.

4.3 MIM

On the Metal-Insulator-Metal side we have a very different behavior. Since we have a symmetric structure, also the results are very symmetric.

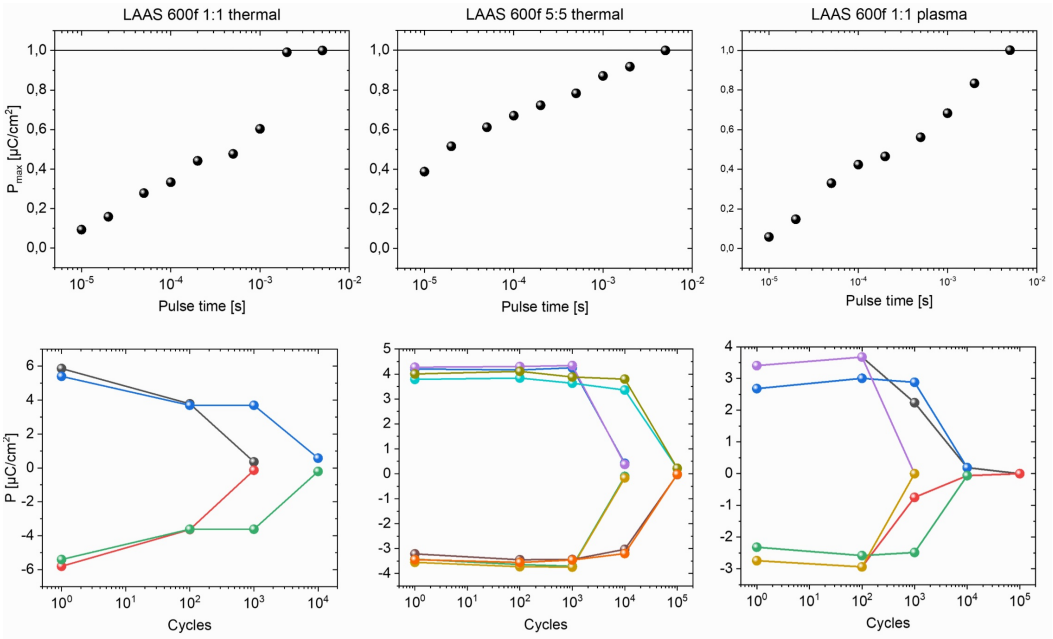


Figure 21: Switching time and Endurance tests for each LAAS MIS sample. The 5:5 shows the most stable and promising results.

First batch: Polarization Starting with the first batch that included only a 600 sample, the results are very promising. Visible in Figure 22a, the displacement current is smooth and clear with evident peaks, even at frequencies higher than before. The coercive field goes from slightly below 2 up to 3 MV/cm, depending on the frequency; the resulting remnant polarization is around 20 µC/cm^2, with a very defined and symmetric hysteresis loop. The state of the art given in the literature gives very similar values for both parameters (beginning of this Section, 4). The E_C is usually given at around 1

Sample	V_c [V]	P_r [$\mu C/cm^2$]
1:1 thermal	4.5	6
5:5 thermal	4	4
1:1 plasma	4.5	3.5

Table 3: Parameters of interest of the LAAS samples, all taken with 5 V sweeps and 1 kHz.

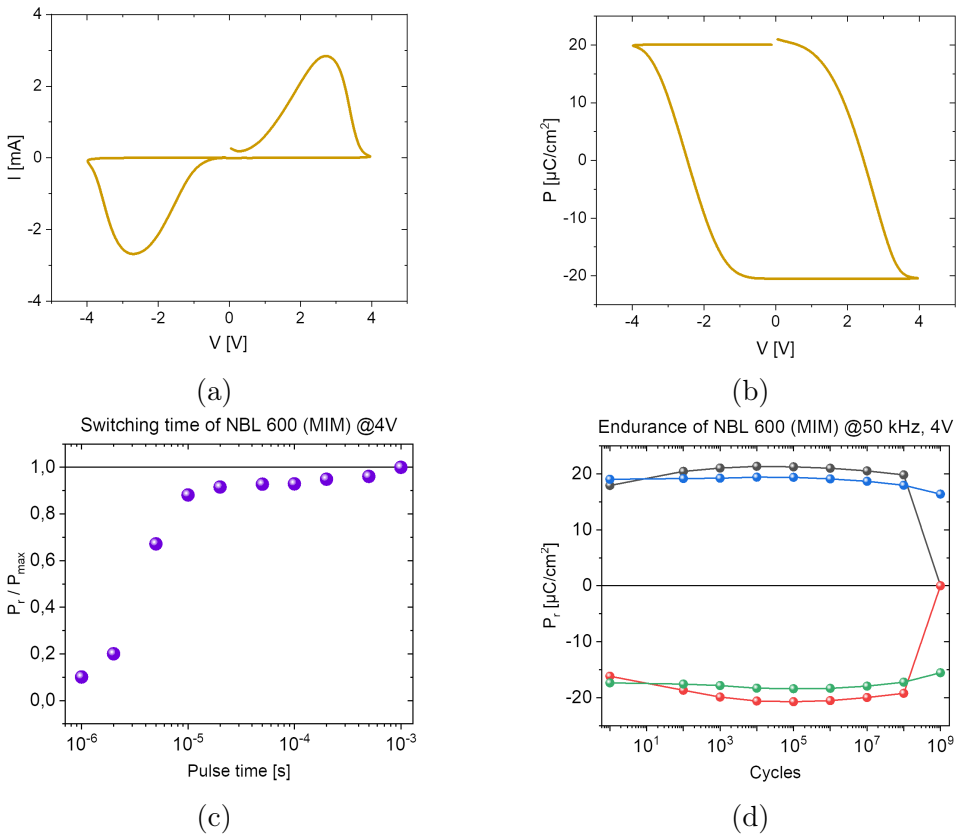
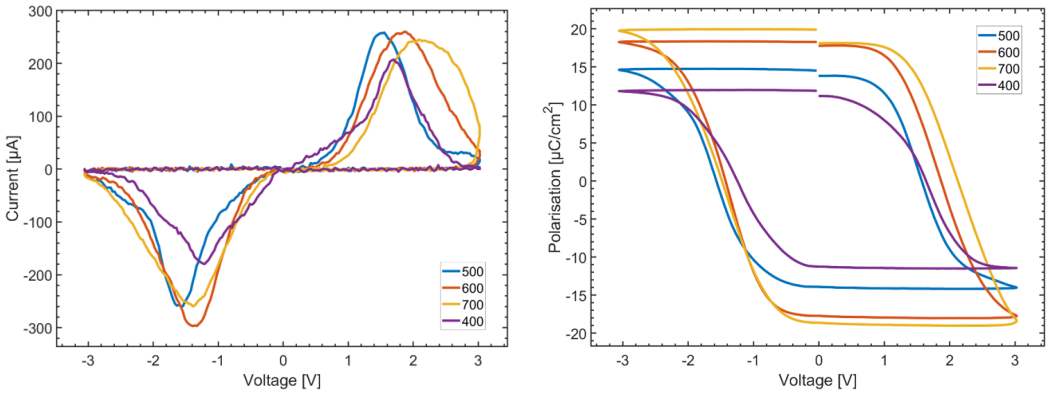


Figure 22: Example of different PUND measurements on a MIM device: (a) Current, (b) Polarization, (c) Switching time and (d) Endurance; all done at 50 kHz with 4 V sweep.

MV/cm, but such a result comes typically from the theory, the experimental ones are in accordance with ours. The polarization is perfectly in the given range, but it may vary depending on the pulse method for the measurement. As expected, the leakage is small too, thanks to the MIM configuration that reduces it. As already said, it is due to charge trapping, especially in the intermediate oxide, which is over the substrate, hence not inside the capacitor.

First batch: Endurance Moving to the endurance, the results are very promising. The measure with time shows a very good stability up to 100 kHz (Fig. 22c); this is also given by the very small coercive field that allows to have



(a) (b)

Figure 23: Comparison between the annealing temperatures of the MIM's second batch, I-V (a) and P-V (b); PUND measurement at 5 kHz.

the current switching peaks completely included even with a small voltage sweep, allowing a complete calculation of the polarization. The endurance, tested at 50 kHz and 4 V range, gives promising results, arriving at 10^9 without burning and a very limited fatigue (Fig. 22d). It is clearly visible the wake-up effect on the first 10^4 cycles, which suggests that these devices need to be cycled to unlock their full polarization potential.

Second batch: annealing temperatures Moving to the other batch, the performances are very similar, but they resulted to be more fragile, burning easily at voltages higher than 5 V and with smaller endurance. This may be due to different fabrication parameters, as some kind of error in the process flow. In general, the differences between the temperatures are very small if we focus on the I-V and P-V graphs, with also the 400 that shows acceptable results, better than with the MIS (Fig. 23). Only the 700 shows less sharp peaks, a behavior similar to that of the MIS. Due to their small coercive voltage, the sweep range could be greatly reduced, improving the endurance performances, with a 3 V sweep and a frequency of 5-10 kHz. In this case, the observed trend is the same of the literature, as in Figure 24, differently from the MIS, since we take as reference the same article [17]. The only discrepancy is with the values, but according to the shape of their curve, it seems that the DHM technique was used, hence they are overestimated.

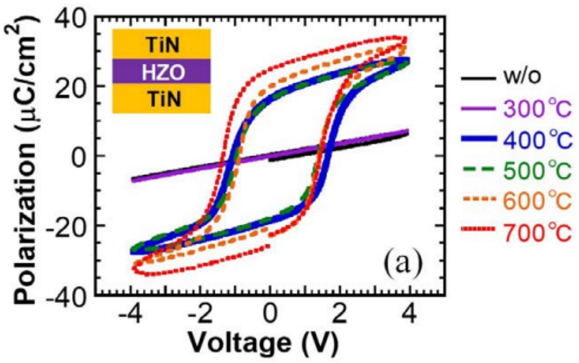


Figure 24: Results of a MIM sample for different annealing temperatures [17]. The obtained behavior is the same as the External lab 1 samples, suggesting interesting developments for these devices, with a coherent fabrication method.

Second batch: Endurance Concerning the endurance, 700 and 600 perform worse than the older sample, reaching 10^6, even with the smallest possible voltage and a quite high frequency. Much better performances are given by the lowest temperatures, which reached 10^7, in case of the 400, and at least 10^8 for the 500, with possible improvements concerning the frequency. In fact, one can see the wake-up effect during a thousand of cycles, that not only improves the polarization value, but also the sharpness of the peaks. This is not included in the endurance tests showed here, because it was noticed only during the analysis of data, but each contact can be cycled before the tests, in order to have the best results. Another improvement could be to further

T [°C]	V_C [V]	P_r [$\mu C/cm^2$]
400	1.7	12
500	1.6	15
600	1.8	19
600 (old)	2.8	20
700	2	20

Table 4: Parameters of interest of the MIM samples, all taken with 4 V sweeps and 10 kHz for the new batch, 50 kHz for the old one. This demonstrates the differences between the two fabrication methods: the first one had smaller P_r for a higher endurance.

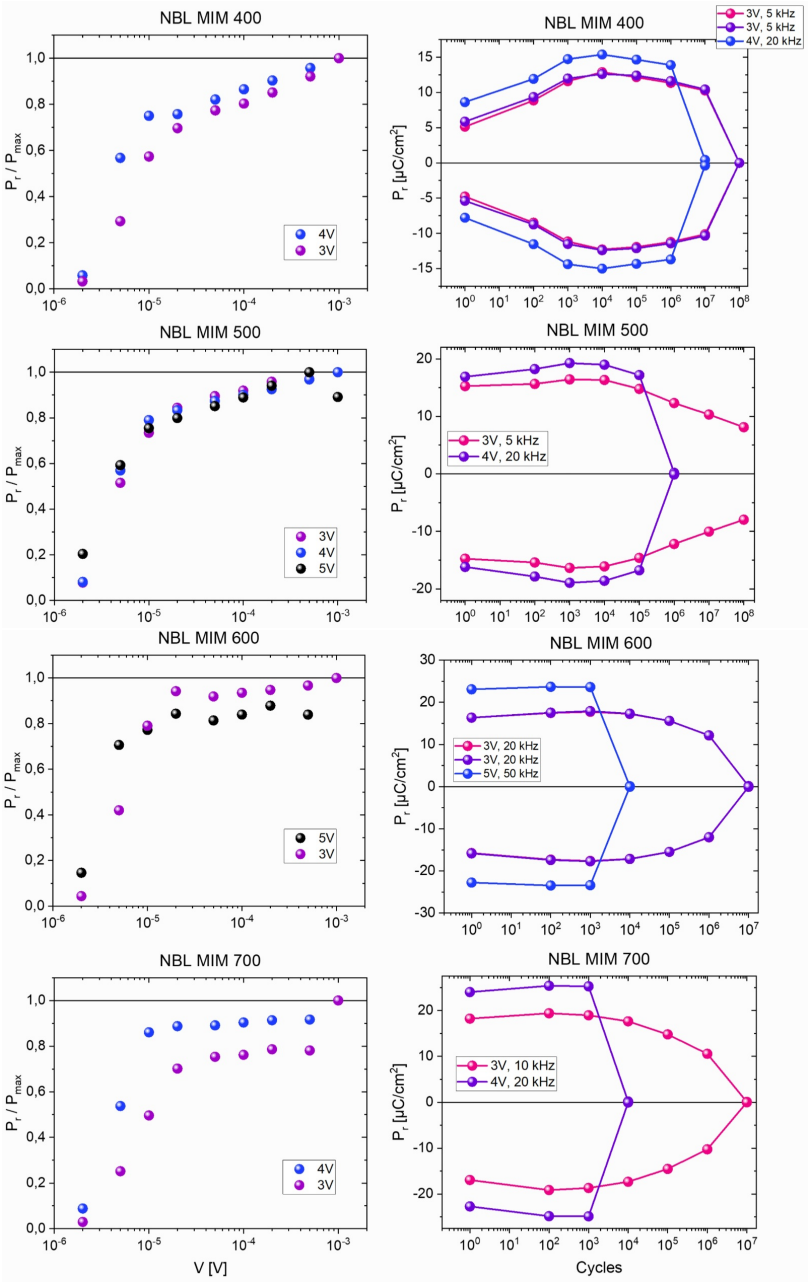


Figure 25: Switching time and endurance tests for each annealing temperature. 500 has the best performances, with some space for improving by increasing the frequency after cycling.

reducing the voltage sweep in spite of a lower frequency, since, as can be seen by the tests, reducing the stress given by the voltage has a much greater effect.

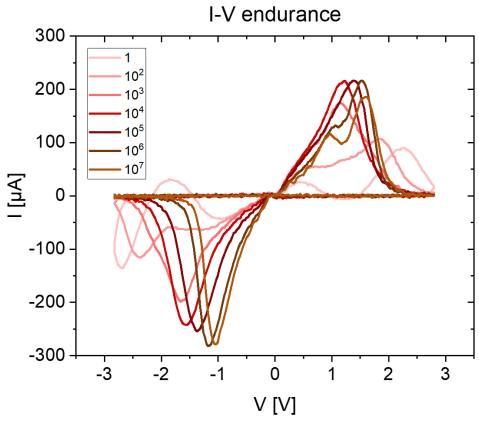
Secondary peaks To be noticed, the double peaks that in some cases are present, like in the MIS, in the 500, but also in the 400 here. They can be of interest because often there is a smaller peak at a much lower field that could be exploited. Anyway, they seem to disappear with the cycling, at least in the case of the 400 (Fig. 26a); for the 500, contacts without double peaks were taken for the tests. Always concerning the cycling of the two lowest temperatures, it seems to be needed because of the presence of secondary peaks, which appear after the switching with zero retention, meaning that they remain with multiple cycles with the same polarization direction (Fig. 26b). They can be considered as parasitic, the reason behind the strange shape of the curve concerning the first cycles in Figure 26a.

4.4 AlScN-based capacitors

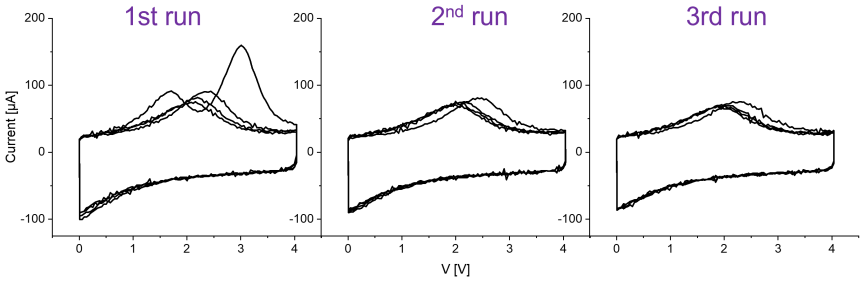
$Al_xSc_{1-x}N$	Substrate	t [nm]	E_C [MV/cm]	f [kHz]	Reference
$Al_{0.74}Sc_{0.26}N$	Si	5:100	4:6	100	[35]
$Al_{0.72}Sc_{0.28}N$	Al (MIM)	18	7	10	[36]
$Al_{0.68}Sc_{0.32}N$	Si	20	6.5	10	[15]
$Al_{0.79}Sc_{0.21}N$	Sapphire	100	4.6	10	[37]
$Al_{0.85}Sc_{0.15}N$	Sapphire	230	5.5	1.5	[38]

Table 5: Summary of the parameters considered from the literature, with their respective values.

Finally, the last variation of the capacitors comes with a different FE material: AlScN (15% Sc, 85% Al). Differently from the HZO, this compound appears in the literature with many variations, since they can differ depending on the ratio between Al and Sc. There are different combinations with the type of substrate and the thickness of the material, since it is under preliminary studies and there is not a convergence of the capacitor's structure yet. In general, the thicknesses used are very high, more than 100 nm; there are few studies on those comparable to ours. The coercive fields are quite high, they can vary from 4 to 7 MV/cm. The frequency used, in the end, are very few: 100, 10 ore 1.5 kHz. All these combinations are summarised in Table



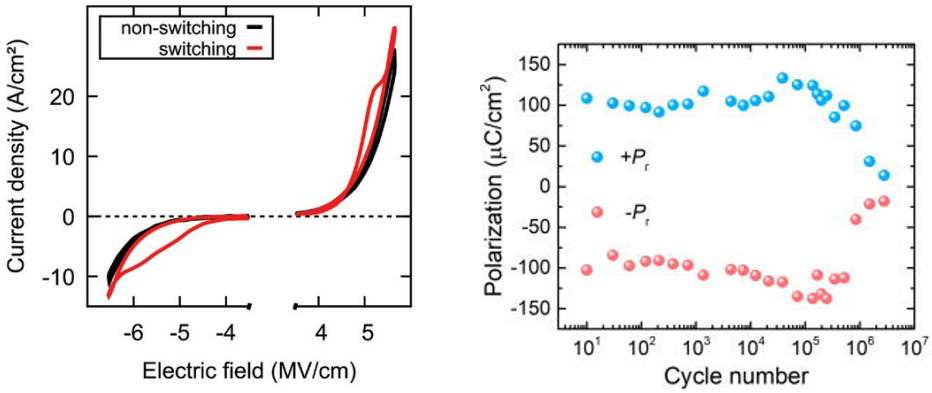
(a)



(b)

Figure 26: (a) Example of cycling during an endurance test. It is useful to see the evolution and stabilization of the peaks. (b) Parasitic peak, it always appears after the switching. Example with the the first 3 PUND cycles. It disappears with cycling (about a thousand).

5. Our experimental measurements gave no interesting results, no peaks were detected. Different strategies have been tried, like changing the frequency, the pulses' order, cycling (for the wake-up effect) and so on. Some brief examples of the results are depicted in Figure 28. The cause of such results may be due to an error during the annealing to activate the ferroelectric phase. In many cases, the leakage current due to the charge trapping happens at very low fields, hence, in some cases like in [15], the peaks may be hidden.



(a) (b)

Figure 27: (a) Example of displacement current generated by an AlScN ferroelectric capacitor, using the same materials [35], and (b) endurance test which reaches 10^5 cycles as for HZO-based MIS [37].

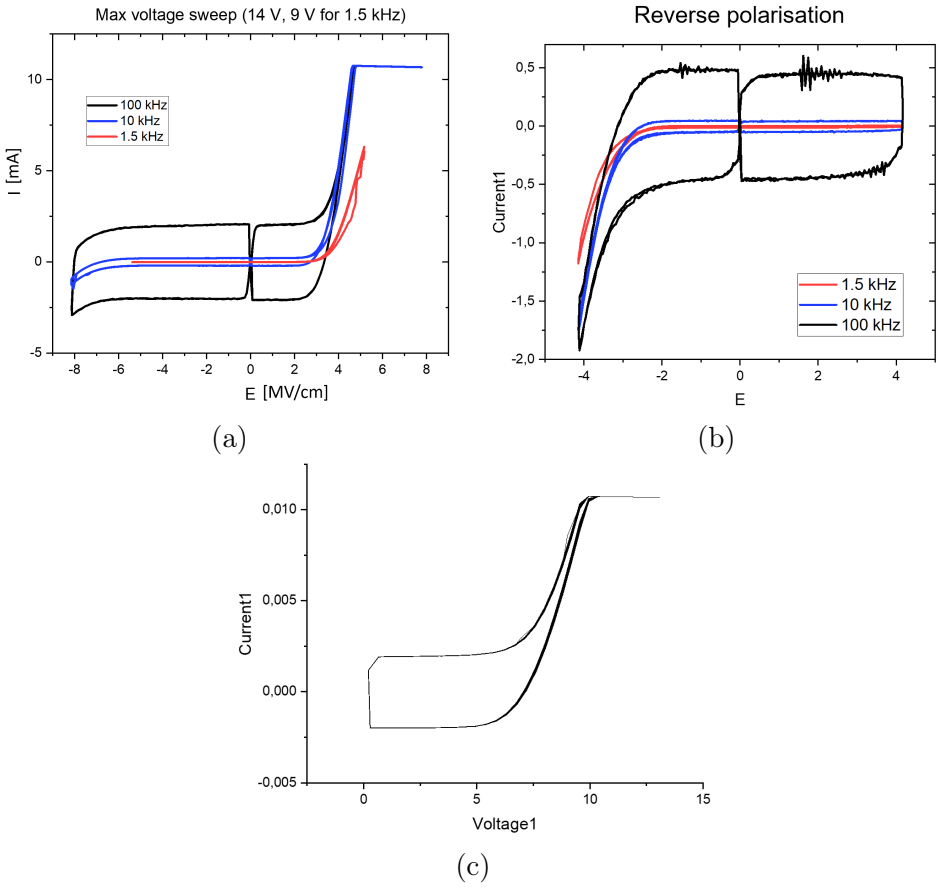


Figure 28: Variations of the measurements to find some FE behavior: (a) changing frequency, (b) reversing the polarization, (c) 10^3 cycles at the same voltage. All of them are made on the 17 nm sample; every type of contact and sample were used.

5 Conclusions

A lot of progress was made during my period at LAAS, especially concerning the Ferroelectrics. We tested several combinations of FE capacitors, evaluating their switching properties, Coercive field and Polarization, and Endurance, looking for the best combination for a FeFET implementation. Up to now, the perspective could be to continue studying them by combining the best results obtained. For the LAAS' samples the 5:5 thermal (600f) is the most promising, with results on the endurance similar to those of External lab 1 and, in addition, with a lower coercive field. The 600, especially the fast ramp-up, shows the best results for now, being reliable on all the parameters: good polarization and endurance, a bit too high coercive field in some cases. The improvements given from the previously mentioned LAAS fabrication method and from the oxide in the middle of the HZO layer may bring us to the perfect candidate. The 500 temperature showed not much worse results for both MISs and MIMs, suggesting a possible alternative to the 600 with the help of few optimizations, reducing the thermal budget. On the other hand, MIMs seems to be the closest technology for the implementation of a FeFET, giving their exceptional performances concerning every tested temperature, if compared to the MIS, and their coherence with the literature. They present one of the most important parameter for a memory: a very high endurance. Anyway, the best candidates for the development of the first memory cells are ready to be tested, since, at LAAS, also the research concerning Vertically oriented transistors is at a good point, which would help increasing the chip density, giving a glimpse on a future in-memory processor.

Appendices

A Keithley 4200: settings for the FE capacitors

The machine offers measurement presets for a lot of different experiments. In the case of FE we used the electrical capacitors' one, which allowed to create the waveform we needed to activate the polarization switching. The user interface consisted, mainly, of two windows: one for the response graph, plus the possibility to visualize the table with all the values; the other for the settings, which will be explored with more details. It is a list of parameters, each one presented as a vector of values:

- **Voltage1**, each element is a point of the waveform, referred to the amplitude, on the y-axis.
- **Voltage2**, it is possible to send multiple signals, not used in our case.
- **Segment time**, from now on we do not refer anymore to points, but to segments, connections between two consecutive points. Here we describe the waveform referring to the x-axis (time), expressing the length of each segment (each element of the vector) in seconds. It is made to set the width of the active pulses, but also of the intervals between them.
- **Measurement**, the number of measurement points for each segment, zero during the intervals, generally 100 during the pulses.
- **Segment ID**, to create groups of segments by giving them a number, their ID, which will be used for the next parameter.
- **Sequence**, it allows to create a specific sequence by putting the groups ID in the desired order.
- **Iterations**, an additional parameter where each element refers to a group ID, in order, and each value expresses the number of iterations of that group.
- **Compliance**, there is one for each of the two currents that is possible to measure; it defines the maximum value that it it possible to measure. It also defines the accuracy of the measured curve: with a small compliance

one has a better precision and the curve may be less smooth due to eventual fluctuations.

There are more parameters in the settings, but those in the list were the most used. Once the experiment is done, it is possible to export the data in the xls format. Some Matlab scripts were personally written by myself to help with the management of the high number of measurements. They are easy to use: the user have only to update the parameters at the beginning, related to the files' position, the capacitor's dimension and the pulse's settings. They work by reading multiple files inside the specified folder, but they have to be named in a specific way, specified inside the script. Their purpose is to print on screen a preliminary version of the resulting graphs, as the current without parasitics and the polarization, and save the data on a given Excel file. They also save specific sets of values as in the case of Endurance and Switching time. To calculate the polarization, the formula uses some of the parameters listed above: the segment time, extracted from the frequency, and the number of measurements, either specified by the user at the beginning or obtained from the file's name. The equation, in code form, is the following

```
P =
cumtrapz(I_clean)*(1E6)*(1/freq/2)/n_meas/(pi*(diam/2*1E-6)^2*(1E4))
```

I_clean is the current after the subtraction, to remove the parasitics, freq, n_meas and diam are the frequency, number of measurements and capacitor's diameter respectively; the multiplication by 10^6 (1E6 in the code) is to get to µC, those by 10^{-6} and 10^4 is to convert the µm of the diameter into cm; "cumtrapz() 🔗" is a Matlab function which performs the integral. The scripts are all grouped as supplementary material in the "scripts-dot-m" folder.

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