POLITECNICO DI TORINO

Master's Degree in Micro and Nanotechnologies for ICTs

Design of a Radiation-Hard Fully-Integrated DC/DC converter's control circuit for High Energy Physics experiments at CERN.

Academic Supervisors:
Prof. Fabrizio Bonani
Prof. Adil Koukab

Candidate:
Marta Macaluso

CERN Supervisor:
Dr. Stefano Michelis

Academic year:
2023/2024

Abstract

CERN, the European Organization for Nuclear Research, is globally renowned for its leading position in particle physics research. Operating the world's largest and most advanced particle accelerator (the Large Hadron Collider, LHC), CERN's mission is to explore the fundamental constituents of matter and the forces governing their interactions. Nowadays, significant engineering efforts are underway to upgrade the Large Hadron Collider (LHC) for the High-Luminosity(HL) LHC experiment. Requiring even more energy and power consumption than previous experiments, the HL-LHC was conceived to provide scientists with an amount of data, collected by particle detectors, higher than any other experiment has ever allowed. As a consequence, providing stable and reliable power to particle detectors becomes more challenging, as the levels of radiations and magnetic fields experienced at the collision sites will be enhanced. Based on the employment of DC-DC converters, the power distribution system for CERN's experiments includes different conversion stages, carefully designed to ensure reliability and conversion efficiency. This Master's thesis project, focused on the design of a Rad-Hard fully-integrated DC-DC converter's control circuit for HEP experiments, contributes to the development of radiation-tolerant electronics for converters included in CERN's power distribution scheme. More specifically, the core of this work is the design of different analog blocks in a 180nm commercial technology, that can withstand the harsh environments of HEP experiments, especially in terms of radiation levels. These blocks are designed for a 20V-2.5V converter and include: the Error Amplifier, needed to sense and stabilize the output voltage, exploiting the feedback loop; the delay generator, to avoid cross-conduction at the power stage; two level shifters, necessary to ensure voltage transition between different domains. The need for high reliability and robustness against radiation effects leads to the necessity of simulating these electronic circuits under extreme irradiation conditions starting from early design stages. Intensive simulations in radiation corners allowed to validate the design of these blocks, whose layout is being carried out and verified for radiation-hardness as well.

Sommario

CERN, l'Organizzazione Europea per la Ricerca Nucleare, è riconosciuta a livello globale per la sua posizione di rilievo nella ricerca dedicata alla fisica delle particelle. Operando il più grande e avanzato acceleratore di particelle al mondo (il Large Hadron Collider, LHC), la missione del CERN è esplorare le componenti fondamentali della materia e le forze che ne governano le interazioni.

Attualmente, sono in corso significativi sforzi ingegneristici per aggiornare il Large Hadron Collider (LHC) per l'esperimento High-Luminosity (HL) LHC. Richiedendo ancora più energia e consumo di potenza rispetto agli esperimenti precedenti, l'HL-LHC è stato concepito per fornire agli scienziati una quantità di dati, raccolti dai rivelatori di particelle, superiore a qualsiasi altro esperimento mai realizzato. Di conseguenza, fornire un'alimentazione stabile ai detector di particelle diventa più impegnativo, poiché i livelli di radiazione e campi magnetici nelle camere di collisione saranno superiori a quelli sperimentati finora. Basato sull'impiego di convertitori DC-DC, il sistema di distribuzione dell'energia per gli esperimenti al CERN include diverse fasi di conversione, ciascuna delle quali deve essere progettata con cura, al fine di garantire affidabilità ed efficienza di conversione.

Questo progetto di tesi magistrale, focalizzato sulla progettazione di un circuito di controllo per un convertitore DC-DC fully-integrated e resistente alle radiazioni per esperimenti di fisica ad alte energie, contribuisce allo sviluppo di circuiti elettronici radiation-hard per il sistema di distribuzione dell'energia al CERN. Più nello specifico, il cuore di questo progetto è la realizzazione di diversi blocchi analogici in una tecnologia commerciale in 180nm, resistenti agli elevati livelli di radiazione e campi magnetici caratteristici degli esperimenti realizzati al CERN. Questi blocchi sono stati progettati per un convertitore DC-DC da 20V a 2.5V e includono: l'amplificatore di errore, necessario per rilevare e stabilizzare la tensione di uscita, sfruttando il loop di retroazione; il generatore di ritardi, per evitare cross-conduction nello stadio di potenza; due level shifter, necessari per garantire la transizione tra diversi livelli di tensione.

Raggiungere un elevato livello di affidabilità e robustezza rispetto agli effetti delle radiazioni porta alla necessità di simulare questi circuiti elettronici in condizioni di irraggiamento estreme sin dalle prime fasi di progettazione. Grazie a tali simulazioni, il design dei suddetti blocchi è stato validato, permettendone la realizzazione del layout, attualmente in fase di sviluppo e testing per verificarne la tolleranza alle radiazioni.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

This Master's thesis project has been carried out within the Power Distribution team at CERN. Being part of the Micro Electronics section, this team's work is mainly focused on the development of DC/DC converters, based on ASICs (Application-Specific Integrated Circuits), employed in the LHC experiments and in the future HL-LHC upgrade. The main challenge of this team is to design radiation-tolerant converters, that have to be placed in close proximity with collision sites, in order to properly power particle detectors. Furthermore, the future HL-LHC experiments will require a significantly larger power consumption of the front-end circuit. The current power distribution system is not suitable for this future upgrade, as it can lead to increased power losses and a bulkier circuit [1]. This last statement justifies the need for designing new DC/DC converters, suitable for the higher energy levels that will be experienced in the HL-LHC upgrades. This thesis project is devoted to improve the current power distribution system by designing new DC/DC converters and, in particular, is primarily focused on the design of the control circuit for a fully-integrated DC/DC converter, exploiting a commercial high voltage 180nm technology and ensuring the required radiation tolerance.

1.1 CERN

Performing world-class research in fundamental physics, CERN (the European Organisation for Nuclear Research) operates the most advanced particle accelerators in the world. The main objective of the research performed within its facilities is to study the composition of matter and the interactions among its basic constituents. To this end, an accelerators complex together with particle detectors are exploited. In particular, CERN hosts the largest and more powerful particle accelerator of the world, the Large Hadron Collider (LHC), which performs the last accelerating

step in the chain and allows particles to reach an energy of 6.5 TeV per beam. In figure 1.1, it is possible to see the complete accelerating system: starting from the Linear accelerator 4 (Linac4), the source of proton beams, negative Hydrogen atoms H^- are accelerated to 160MeV, before entering the Proton Synchrotron Booster (PSB); the injection from Linac4 to PSB causes the ions to be stripped of their electrons, obtaining the proton beam. Then, subsequent accelerating stages through the Proton Synchrotron (PS) and the Super Proton Synchrotron (PSP), prepare the beam to be injected into the two pipes of the LHC. In this 27km ring, the beams in the two pipes circulate in opposite directions until they reach the final energy of 6.5TeV. Then, the two beams are brought into collision inside four detectors – ALICE, ATLAS, CMS and LHCb – where the total energy at the collision point is equal to 13 TeV [2]. These detectors surround each collision point and allow to measure the position, speed, charge, energy and mass of the particles generated during collisions. Furthermore, these devices can be divided into two categories:

- Tracking devices reveal the trajectories of charged particles through the trails they leave while ionizing matter. In a magnetic field, knowing the trajectory of a charged particle, hence its curvature, allows to know the momentum and to subsequently identify the particle.
- Calorimeters allow to identify neutral particles by measuring their energy losses while crossing the detector.

Independently on the kind of detector, these devices must be placed in close proximity to the collision sites, in order to provide sufficiently accurate information on the generated particles. This means that a fundamental requirement for the electronics developed for the detectors is tolerance of both high radiation levels (up to 200Mrad of TID and $1 \cdot 10^{15} n/cm^2$ of flux density) and high magnetic fields (up to 4T). Moreover, the future HL-LHC upgrade should provide an increased amount of data with respect to past experiments, allowing to study in more details the fundamental components of matter and the forces that bind them together. This means that the upgraded detectors must tolerate even higher radiation levels and the amount of material employed to build them should be reduced, to improve performances [3].

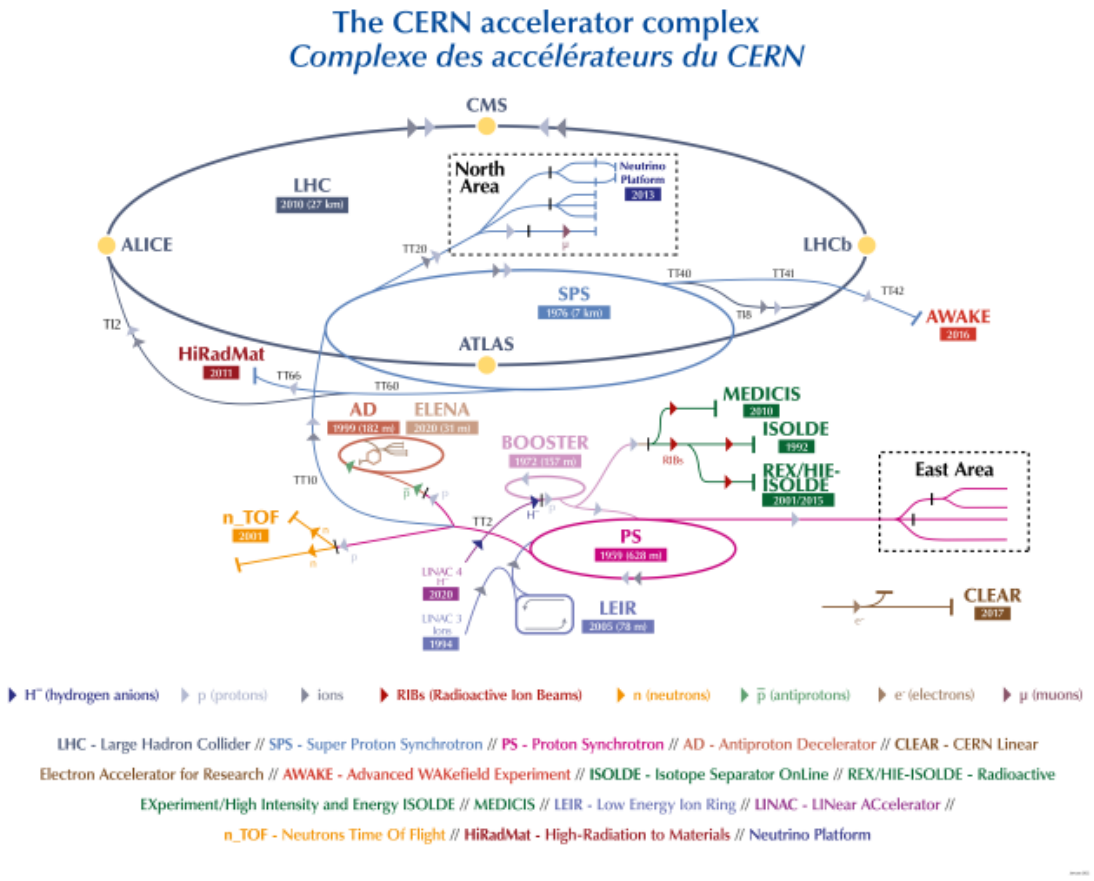

Figure 1.1: CERN accelerators complex [2].

1.2 Power distribution for HEP experiments

The main focus of the DC-DC team at CERN is to provide different supply voltages to the front-end circuits of particle detectors, while keeping power losses to the minimum. This task is quite challenging, as detectors are placed near collision sites, with a distance of around 100m from power supplies. To ensure low power losses is therefore necessary that the supply voltage is kept the higher possible until the very end of the power line, hence right before the collision sites. To step down this very high supply voltage to the one required to power detectors, is then necessary to build radiation-tolerant DC-DC converters, to be placed exactly on the detectors. In this way, the high-voltage supply of 48V will travel the 100m from the power supply location to the experiments site, keeping the losses to the minimum; then, reaching the detectors, this high voltage will be stepped down to the required value, thanks to the radiation-tolerant DC-DC converters based on

ASIC and designed by the DC-DC team at CERN. It is important to highlight that the high levels of radiation experienced by electronic circuits at the collision sites make commercial and also space-grade electronics unsuitable for building such converters, reason for which there is a designated team to realize radiation-hard ASICs for HEP experiments at CERN. In figure 1.2, it is possible to see a

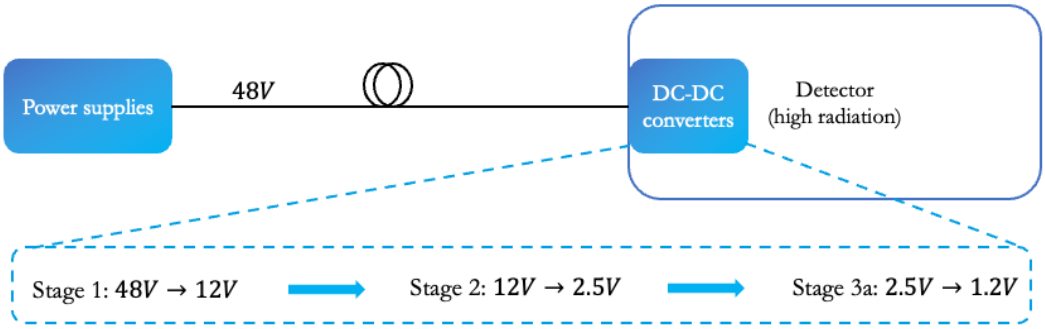

Figure 1.2: Current power distribution scheme for HEP experiments at CERN [4].

scheme of the current power distribution system employed at CERN: it consists of three main converting stages, allowing to power both the analog and digital front-ends, optoelectronic circuits and the slow control blocks of particle detectors. Further developments of the DC-DC project foresee the realization of a new power distribution scheme, possibly reducing the number of converting stages, to improve conversion efficiency and reduce losses. This thesis work finds its purpose within the R&D program for the development of this new power distribution scheme, that will require advanced DC-DC converters, sufficiently robust for the future HL-LHC upgrade.

1.3 Radiation effects on CMOS technologies

To understand some of the design choices employed in this thesis work to ensure radiation hardness, particular attention to the interaction between matter and radiation must be given. In general, the way radiation interacts with solid matter depends on the characteristics of the incident particles, in terms of charge, mass and kinetic energy, and target's atomic number and density. Particular influence on matter's reaction to radiation is caused by whether the incident particle is a charged or a neutral particle: the former, such as protons, heavy ions or electrons, interacts with matter mainly through Coulomb's interaction; meanwhile, neutral particles, namely photons and neutrons, do not experience the Coulomb force and can interact in different ways depending on their energy. Slow neutrons give rise to

nuclear reaction or elastic collisions with target's nuclei; fast neutrons give origin mainly to elastic collision, while very high-energy neutrons produce inelastic collisions. Concerning photons, the possible results of their interaction with matter are: the photoelectric effect, the Compton effect and the creation of electron-positron pairs. The probability of these three events to verify changes with the energy of the photon and the atomic number of the target. [5]
Therefore, the effects of both charged and neutral particles on matter can be grouped in two classes: ionization effects and nuclear displacement. Neutrons give origin mainly to nuclear displacement, while photons, protons and electrons are mostly responsible for ionizing effects.
The result of ionization in a semiconductor or insulating-material is the creation of electron-hole pairs, whose number is proportional to the quantity of energy transferred to the material, which is expressed in terms of *Total Ionizing Dose (TID)*, i.e. the total energy absorbed by radiation per unit of mass of the target. The Total Ionizing Dose is independent on the nature of the radiation and it is measured in *rads* ($1rad = 0.01\frac{J}{kg}$). Meanwhile, the effect of nuclear displacement is the production of neighboring interstitial atom and vacancy, together called a Frenkel pair. The radiation effect produced in a device by the generation of Frenkel pairs is called *Displacement Damage (DD)* and is quantified by the *fluence*, namely the total number of particles per unit of area that hit the target material. Frenkel pairs can then recombine in an interval of time that depends on the kind of material that has been irradiated; clearly, a short recombination time implies a good robustness of target material against nuclear displacement. This is the case of silicon dioxide, in which at room temperature 90% of Frenkel pairs recombine within a minute after irradiation stopped. [5]
Concerning the effect of radiation on MOSFETs, being devices whose operation is based on the flow of majority carriers below the SiO_2-Si interface, region that does not extend deep in the silicon bulk, it is straightforward that nuclear displacement has a negligible impact on devices performances, as eventual Frenkel pairs, that can be generated mainly at the SiO_2-Si interface, would recombine immediately. Indeed, MOS transistors are more sensitive to ionization damage: when a ionizing particle crosses a MOS device, it can generate an electron-hole pair, whose effect on device functioning depends on the region of the transistor in which the pair was generated. Electron-hole pairs would immediately recombine if they were generated in the gate of the transistor, which is made of polysilicon, or in the substrate (doped Silicon), as these materials are characterized by a very small resistance. On the other hand, in insulating materials as the silicon dioxide between the gate and the channel of the device or in the STI (Shallow Trench Isolation) between adjacent transistors, there is very high resistance against the motion of the generated electron-hole pairs, causing their mobility to drop by five

to twelve orders of magnitude. This means that pairs generated in the oxide are not able to recombine as quickly as those generated either in the gate or in the substrate. The electron-hole pairs that won't recombine immediately after being generated will be separated by the electric field in the oxide and if a positive bias is applied to the gate, electrons will drift to the gate and holes will accumulate at the SiO_2-Si interface. Here, holes can be trapped, generating a fixed positive charge in the oxide and interface traps between silicon and silicon dioxide. Instead, electrons will leave the silicon dioxide in a time interval of the order of ps, as their mobility is many orders of magnitude higher than the one of holes. Furthermore, in high-quality oxides the ratio between trapped holes and electrons is generally between 3 and 6 order of magnitudes. For these reasons, only holes transport and trapping mechanisms in SiO_2 are relevant in this discussion.
To establish the impact of electron-hole pairs generation, one needs to know the total amount of energy transferred to the matter by the incident particles, which is expressed in terms of *Linear Energy Transfer (LET)*:

$$LET = \frac{1}{\rho}\frac{dE}{dx} \tag{1.1}$$

where ρ is the density of mass of the target and $\frac{dE}{dx}$ is the mean energy deposited in the material per unit of path length [5].
Clearly, the number of generated electron-hole pairs is equal to the total deposited energy divided by the energy required to generated one pair. However, after few pico-seconds there is a partial recombination of the generated pairs, which depends on the LET of the incident particles and on the electric field applied to the oxide. Particles with higher LET generate denser column of pairs and the recombination probability is proportional to the density of generated pairs; on the other hand, increasing the electric field leads to a decrease in the recombination phenomenon, as holes and electrons, having charges of opposite sign, will be drifted in opposite directions, without being able to recombine.
Holes that do not recombine will move towards the $Si - SiO_2$ interface, supposing that the gate is positively biased. When these radiation-induced holes reach the ends of the oxide layer, they can be trapped either near the $SiO_2 - Si$ interface or the $SiO_2 - gate$. This phenomenon dominates among the other radiation-induced phenomena and, as it will be described in paragraph 1.3.1, it gives origin to a negative shift of the potential drop in the oxide ΔV_{ox}, which will affect the threshold voltage of the transistor.

Summarizing, a highly-energetic ionizing particle interacting with a MOS device can produce a sufficiently high number of electron-hole pairs to disrupt the performances of the transistor. If this transistor is part of an integrated circuit, its malfunctioning can lead to a reversible or non-reversible error: these phenom-

ena are called Single Event Effects (SEE) and are generally described in terms of Linear Energy Transfer (LET), measured in $\frac{MeV \cdot cm^2}{mg}$ [1], [5].

1.3.1 Radiation-induced effects on MOSFETs electrical parameters

Holes trapping and interface traps generation can dramatically affect the electrical parameters of a MOSFET. In particular, the main consequences of these radiation-induced phenomena are the threshold voltage shift, the increase of leakage current and the decrease of mobility and transconductance.

- *Threshold voltage shift.*
  When a device is irradiated, its threshold voltage changes and the produced shift ΔV_T is given by the sum of two contributions: ΔV_{ox}, related to holes trapping in silicon dioxide, and ΔV_{it}, due to the charge state of the interface traps. It must be noted that in more advanced technology nodes, the thickness of the gate oxide has been drastically reduced, so that the main contribution to positive charge accumulation comes from the Shallow Trench Isolation (STI, namely an oxide layer employed to isolate transistors from one another) and spacers (oxides placed at the sides of the gates).
  Concerning ΔV_{ox}, it can be proved that this shift is negative when the involved charge is positive: considering for example a p-channel device, the accumulation of holes in the oxide due to radiation-induced trapping mechanism will produce a positive charge that repels holes in the channel; consequently, to re-create the same inversion condition one previously had without irradiation, a more negative voltage has to be applied to the gate, meaning that the threshold voltage will be more negative (higher in absolute value).
  The second contribution comes from the radiation-induced interface states at the $Si - SiO_2$ boundary. These traps are donor-like if their energy is above the Fermi level, otherwise they are acceptor-like: for an n-channel device the acceptor-like traps below the Fermi level and near the interface with the oxide will be negatively charged, as they collect electrons. Therefore, further electrons are needed to produce the required inversion condition, meaning that the threshold voltage shift is positive. Similarly, for a p-channel device, donor-like state above the Fermi level will host positive charges, meaning that population inversion requires a more negative threshold voltage, hence higher in absolute value.
  As an example, in figure 1.3 one can see the threshold voltage shift as a function of the TID in the oxide for a 1.8V p-MOS in the 180nm technology employed to the design the analog blocks for this thesis work. For simplicity, only the response of a p-channel device is shown, as the threshold voltage

shift is more significant than in an n-MOS in the same technology. From this plot, the expected behaviour can be analysed: as the TID in the oxide increases, the number of holes trapped either in the oxide or within interface states increases as well, leading to a negative shift of the threshold voltage that can reach -0.25V with a TID above 10^8 rad.

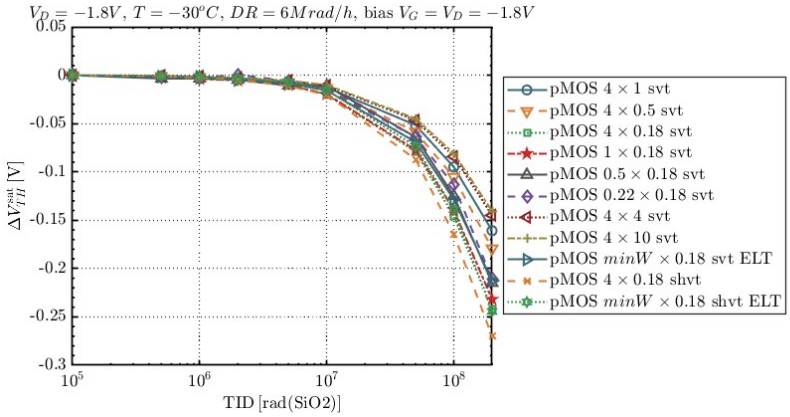

Figure 1.3: Threshold voltage shift as a function of the TID in the oxide for a 1.8V p-MOS in the 180nm technology chosen for this thesis project. The different curves in this plot are related to devices of various dimensions, reported in the legend on the right.

For completeness, in figure 1.4 it is possible to see the same response for a 3.3V p-MOS in the same 180nm technology. In this case, the drop in the threshold voltage is even higher, reaching -0.72V for a TID of 10^8 rad. This explains why working with transistors that can withstand higher gate voltages is more challenging design-wise: one has to take into account a larger shift of the threshold voltage when designing the circuit compared with the shift witnessed when dealing with low-voltage transistors. To ensure the proper functioning of the circuit even under irradiation, it is necessary to make design choices that help compensating this voltage shift, so that transistors will not go out of saturation when is not required.

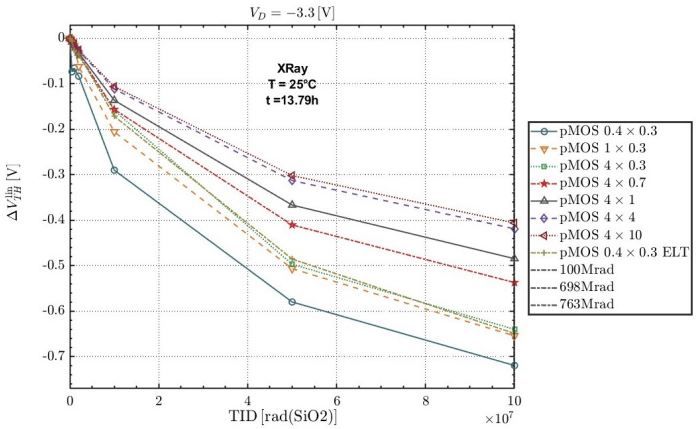

Figure 1.4: Threshold voltage shift for a 3.3V p-MOS device as a function of the TID in the oxide; results are shown for devices of different dimensions, listed in the legend on the right.

- *Increase of leakage current.*
  The accumulation of positive charges in oxides, particularly in the STI, causes also the increase of the leakage current of the device, defined as the current flowing in the channel of a MOSFET when zero V_{gs} is applied between the gate and the source. The presence of holes and interstitial charges trapped in the oxide used to build the STI can attract electrons, leading up to the creation of parasitic paths from drain-to-source at the edges of the transistor. Furthermore, these parasitic channels can be generated also between two drains of different devices, separated by an STI. In both cases, these paths allow electrons flow even when the device is in off-state, producing an increase in the leakage current, which can be detrimental for the correct functioning of the overall circuit. To be more specific, for NMOS device one should consider the increase of the "*off-current*", hence the current that flows through the device, when it is supposed to be in off-state, due to the development of parasitic paths. On the other hand, for PMOSs what is actually relevant is the "*on-current*", namely the current flow when the p-channel device should be in the on-state and equivalent to an open circuit. Indeed, for zero V_{gs} a PMOS is equivalent to a short circuit and current flow is expected; meanwhile, when negative V_{gs} is applied between gate and source contacts of the device, the latter should behave as an open circuit, obstructing current flow. In this conditions, radiation-induced parasitic paths between source and drain can produce an unwanted current flow. Concerning the exploited 180nm technology, in figure 1.5 it is possible to see the behaviour of the *off-current* as a function of the TID in silicon dioxide regions for 1.8V n-channel transistors. Meanwhile, the plot in figure 1.6 represents the behaviour of the *on-current* against the increase of TID in silicon

dioxide for 1.8V PMOSs. In both cases, different devices dimensions and layout techniques were analysed, to establish their impact on parasitic currents under irradiation. Indeed, these plots allow to understand the effectiveness of the *Enclosed Layout Transistor (ELT)* technique for the reduction of the leakage current in an n-MOS: the light-blue curve with triangular points and the red, dotted curve in the top figure regard both ELT n-MOSs, the first with the minimum dimensions allowed to design an ELT and the second one is characterized by an increased gate length. In both cases the leakage is not as dramatic as in the other curves represented in the same figure and stay almost constant with the increase of TID. Moreover, the smaller the gate length, the lower will be the off-current, as the minimum-sized ELT has a leakage current of around four orders of magnitude smaller than the device with a gate length of 0.8nm (red, dotted curve).
On the other hand, the same behaviour is not witnessed for p-channel devices: as it is possible to see from figure 1.6, exploiting the ELT solution does not bring any significant advantage to the reduction of parasitic currents.
Here, for the sake of simplicity, only the leakage current for 1.8V devices is shown, as the same behaviour is encountered for 3.3V transistors: the leakage current increases dramatically, up to fractions of mA, as the TID reaches $1 \cdot 10^8$ rad for traditional MOS, while it can be kept below the nA exploiting ELT design, but only for n-channel devices.

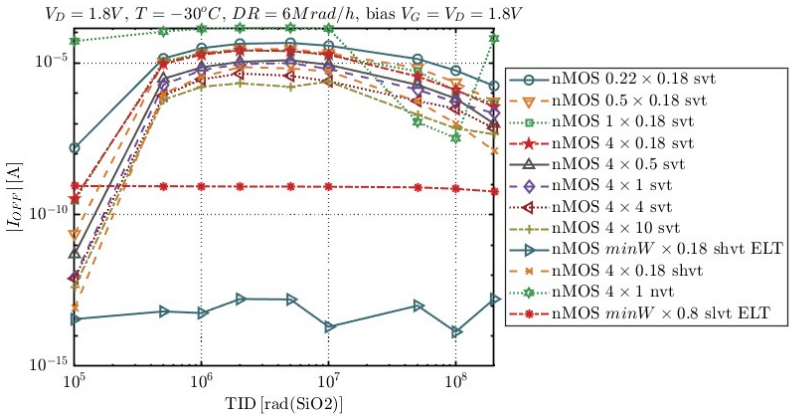

Figure 1.5: Off-current as a function of the TID in silicon dioxide for 1.8V n-channel devices, evaluated for different dimensions and layout techniques.

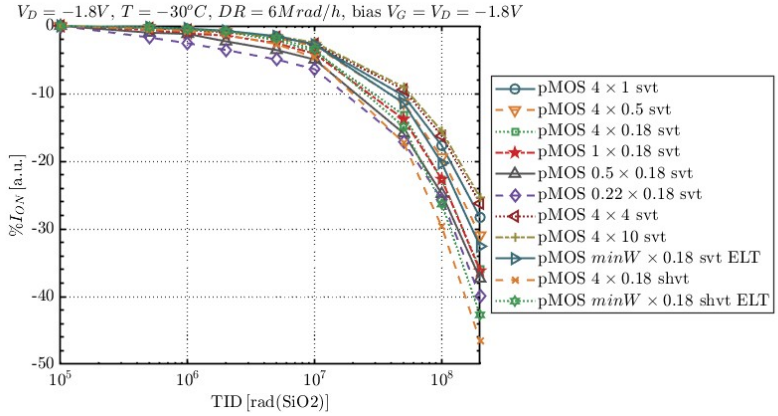

Figure 1.6: On-current as a function of the TID in silicon dioxide for 1.8V p-channel devices, evaluated for different dimensions and layout techniques.

- *Mobility and transconductance reduction.*
  Another important consequence of irradiation regards the decrease of carriers' mobility, due essentially to the increase in number of interface traps, that slow down carrier motion through the device. Furthermore, the degradation of mobility gives rise to a decrease of the transconductance of the transistor employed in an amplifying stage: for a MOS in saturation, the transconductance is directly proportional to the mobility, meaning that a reduction of the latter causes the degradation of the driving capability of the device.

1.3.2 Single Event effects

When a highly energetic particle passes through an integrated circuit, it can give rise to the so-called Single Event Effects (SEE), that produce malfunctioning of one or more transistors in the circuit, resulting in either a reversible or irreversible error; malfunctioning of the first type are called soft errors and are non-destructive, meanwhile irreversible errors are also called hard errors and are destructive.
Among soft errors the most important one is *SEU (Single Event Upset)*, namely the instantaneous and reversible complementation of the logic state of an elementary memory cell, produced by the additional charge generated along the trajectory of the ionization particle. This phenomenon can reduce significantly circuit performances when the error rate is too high, even though it is a reversible effect.
Each device is characterized by a minimum charge quantity, the critical charge, that can generate a SEU and is directly proportional to the LET of the incident particle that produces the critical charge, reason for which one can describe this phenomenon also in terms of critical LET. When multiple transistors are affected by SEU at the same time one talks about *MBU (Multiple Bit Upset)*. [1]
Concerning hard errors, the most frequent and dangerous error that can verify is *SEL(Single Event Latch-up)*. In general, in an integrated circuit (IC) it is called *Latch-up* a phenomenon that consists in the turning on of a parasitic PNPN structure called thyristor, which can cause a short between the power lines, generating an immediate current flow that can burn the device if it is not suddenly interrupted. There are several causes that can produce a SEL by turning on eventual parasitic thyristor and many of them can be addressed by the manufacturer, with the exception of the impact of a ionizing particle that, with sufficient energy transferred to the target device, could initiate a latch-up and can be destructive if the power supply of the IC is not turned off quickly. [5], [6]

1.4 Radiation hardening techniques

There are three different techniques that can be adopted to improve the radiation tolerance of a CMOS IC: the first one consists in modifying the manufacturing process with the purpose of reducing sensitivity to radiation-induced phenomena and it is called *hardening by process*; the second one relates to the adoption of special layout techniques to design more robust transistors, solving the issue of leakage currents, SEL and SEU (*hardening by layout*); the last technique, *hardening by circuit and system architecture*, regards the development of new circuits that are less sensitive than more common architectures to changes in device characteristics and unwanted charges caused by irradiation. This last strategy is effective mainly in hardening memory elements, and is not relevant when dealing with analog cir-

cuits. [5]
In the context of this thesis work, hardening by process techniques were not employed, as all the analog blocks were designed exploiting a 180nm commercial technology, which guarantees the advantages of deep sub-micron technologies, such as: high speed, low power consumption, high level of integration and high production volume. Furthermore, these advanced technologies are characterized by ultra thin gate oxide, making them inherently more tolerant to TID effects than other technologies characterized by thicker oxides.
The main strategy adopted in this work to make the designed blocks more radiation-tolerant is hardening by layout and, more specifically, it is based on the use of Enclosed Layout Transistors (ELT) for NMOS devices, to inhibit the creation of radiation-induced leakage paths between source and drain of a traditional transistor.
The main feature of an ELT device that allows to reach high radiation-tolerance is the fact that no STI is in contact with the channel, as it is possible to see from figure 1.7: the only oxide layer between the drain and the source contacts of such device is the ultra thin oxide below the gate, which, as already explained, does not contribute significantly to the generation of radiation-induced errors. Indeed, the main contribution in a standard MOS comes from the STI on the sides of the device, which in this case is not in contact with the channel, inhibiting the creation of parasitic paths between the source and drain contacts. This immediately solves the problem of leakage current increase due to TID in a single device. Furthermore, by adding a p+ guard ring between adjacent NMOS devices one can inhibit the creation of leakage paths also between n-doped regions in close proximity. Therefore, these two strategies have been extensively used in the layout-making process for the analog blocks presented in this thesis work.
Layout stratagems can be used also to solve SEL problems: the simultaneous presence of p+ guard rings around n-channel devices, and n+ layers around p-channel ones can reduce the gain of the parasitic bipolar transistors that lead to shorts between power lines under irradiation.
Finally, hardening by layout improves also the sensitivity of the circuit to SEU, by increasing the W/L ratio of the transistors or introducing additional capacitances to the most sensitive nodes. A part from layout techniques, several simulations were performed to ensure that each designed circuit was compliant with the threshold voltage shifts caused by radiation-induced phenomena. Indeed, these shifts were included in the radiation corners that will be presented in chapter 3 and exploited as a support to establish the behaviour of the circuit under irradiation conditions. This strategy allowed to understand for each designed block which circuit topology could guarantee more robustness against radiation-induced shifts of transistors' electrical parameters.

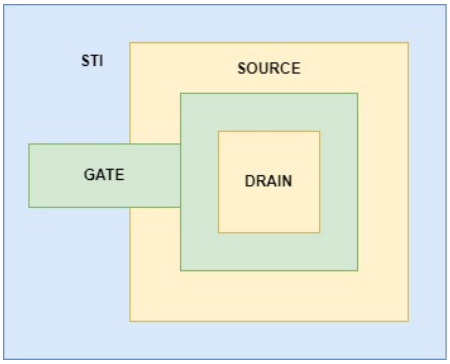

Figure 1.7: General schematic of an Enclosed Layout Transistor.

1.5 Thesis organization

This master thesis is mainly focused on the design of radiation-tolerant analog blocks for the realization of a fully-integrated DC/DC converter's control circuit in a commercial 180nm technology. The final converter is supposed to produce an output voltage of 2.5V, working with an input of 20V, and it is designed for powering detectors in the future HL-LHC experiment at CERN.
In the following chapters, a brief overview on DC/DC converters will be made, to help the reader understand better the purpose of the control circuit to be designed and why it is fundamental.
Then, all the designed analog blocks will be thoroughly depicted in dedicated chapters. First of all, in chapter 3 the focus will be on the design of one of the most important elements of the control circuit, namely the error amplifier; secondly, the delay generator will be presented in chapter 4 and, finally, the two designed level shifters will be depicted in chapter 5.

Chapter 2

Fully-integrated DC/DC converters

This thesis project revolves around the design of a fully-integrated DC/DC converter's control circuit. Therefore, in this chapter an overview on DC/DC converters is provided, discussing first the most common topologies to implement the power stage of such converters; secondly, the working principle and electronic circuit of a general control loop for DC/DC converters will be presented.
Furthermore, the need for integrated powering solution will be highlighted, especially in the context of power stages employed in HEP experiments. Indeed, to improve electronic circuits' performances under irradiation condition it is fundamental to reduce as much as possible the overall mass of the electronic component to be placed near collision sites: more massive circuits have more chances to interact with ionized particles than small, compact and integrated solutions. The search for integrated DC/DC converters solutions regards not only HEP experiments: as logic circuits scale down further and further, DC/DC converters need to follow the same trend to avoid the increase of costs and volume of an electronic system. Therefore, in literature one can find several examples of fully-integrated converter topologies that allows to achieve more compact and less expensive powering solutions, while guaranteeing high conversion efficiency and power density [7].

2.1 Overview on DC-DC converters

In the field of power electronics, the *switching converter* represents a fundamental element. In general, a switching converter is characterized by input and output ports and by a control input, fundamental to produce a well-regulated output voltage in the presence of disturbances on the input voltage or load current. Therefore,

a switching converter is generally made of two blocks: the power stage, where the voltage conversion actually takes place, and the control circuit, dedicated to the output voltage regulation. [8]
In this section, particular attention is given to the possible implementations for the power stage: first the most common step-down DC/DC converter, namely the buck converter, will be described; then, a more sophisticated solution optimized for integration will be presented.
Although there are several switching converter topologies, every implementation is realized exploiting mainly three elements: capacitors, magnetic devices (inductors and transformers) and switched-mode semiconductor devices. These components allow to develop highly efficient converters, as their power dissipation is very low; hence, resistive elements and linear-mode semiconductor devices must be avoided when designing switching converters, to avoid efficiency reduction and increase of power losses. As it will be better explained in the following paragraphs, the most common buck converter is only made of two switching semiconductor devices and an inductor; despite its simplicity, this converter is able to guarantee high efficiency and fast transient response [1]. On the other hand, the presence of the inductor makes the buck converter not the best choice for integrated solutions: magnetic elements in general are too bulky and have low power density, features that discourage their usage for on-chip integration. For this reason, other DC/DC converter topologies will be described, belonging to the category of *Switched Capacitor (SC)* power converters; avoiding the use of magnetic devices, these devices are characterized by improved power density, making them a more suitable choice for on-chip integration than buck converters.

2.1.1 Buck converter

Among the diverse solutions one can find in literature for step-down DC/DC converters, the buck architecture, although its simplicity, remains one of the most used. The reason for this relies in its high efficiency, fast transient response and in the presence of only one inductor. In figure 2.1, one can see the schematic of the power stage of a buck converter, together with the output capacitance and the load; the two transistors work as switching semiconductor devices and, to provide a brief description of the working principle of such converter, they will be considered ideal switches.
The voltage conversion mechanism of a buck converter is strictly determined by the switching activity of the two ideal switches, which controls the voltage at the node *Phase*: when the low-side switch (LS, in figure 2.1) is closed, the *Phase* node is shorted to ground; meanwhile, when the high-side switch is closed, the *Phase* node is risen to the input voltage V_{in}. Clearly, to ensure that the node switches correctly between 0V and V_{in}, there must never be cross-conduction between the

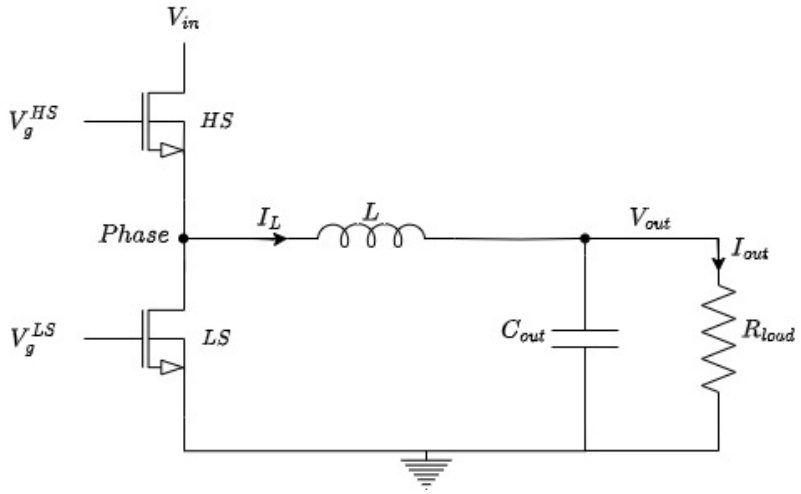

Figure 2.1: Circuit implementation of a buck converter exploiting MOSFETs as switching semiconductor devices.

two switching transistors, meaning that the two gate signals, V_g^{LS} and V_g^{HS}, must be carefully controlled to guarantee that the two switches are never in the on-state at the same time. If this condition is fulfilled, the average voltage on the *Phase* node determines the value of the output voltage V_{out}. Then, by choosing the output LC filter so that the cut-off frequency is much lower than the switching frequency, only the DC component of the *Phase* voltage is preserved, while any harmonics of the switching frequency will be suppressed. The final result is that the output voltage V_{out} will be determined by the average voltage on the *Phase* node and it can be proven that it is proportional to the duty cycle D of the square wave at the *Phase* node:

$$D = \frac{T_{on}}{T_{per}} \tag{2.1}$$

$$V_{out} = \frac{DT_{on}V_{in} + (1-D)T_{per} \cdot 0}{T_{per}} = DV_{in} \tag{2.2}$$

where T_{on} represents the time interval during which the phase node is shorted to V_{in} and T_{per} is the switching period. Concluding this brief steady-state analysis, the conversion ratio $\frac{V_{out}}{Vin}$ of a lossless buck converter is given by the duty cycle D [8]. Hence, by accurately tuning D, it is possible to fix the output voltage to the desired value.

2.1.2 Switched-capacitor converters

Exploiting exclusively capacitors and switches, *Switched Capacitor (SC)* power converters guarantee improved power density compared with other architectures that include magnetic components. Indeed, capacitors have an higher energy density than inductors or transformers and, in general, take up less space, allowing for more lightweight solutions. These characteristics are interesting in the context of HL-LHC experiments, as mass reduction of electronic components is a key factor for performance improvement under irradiation.

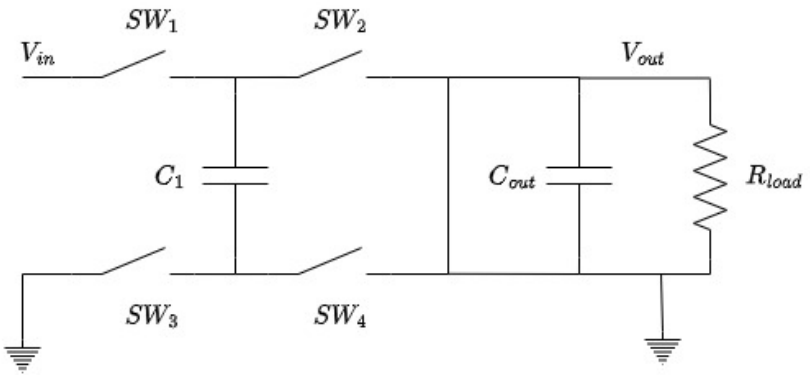

Figure 2.2: Schematic of a 2:1 Switched Capacitor converter; for the sake of simplicity, real MOS switches were represented by ideal switches (SW_1, SW_2, SW_3 and SW_4).

Even for this converter, the switching period is the result of two alternating phases: during the first one, closing only switches SW_1 and SW_4, the flying capacitor C_1 is connected between V_{in} and V_{out}; in the second phase, C_1 is connected between V_{out} and the ground node (clearly, in this case switches SW_2 and SW_3 are closed).
To achieve a DC output voltage, it is fundamental that $C_{out} \gg C_1$; then, assuming that V_{C_1} is the voltage drop on capacitor C_1, the two expressions of such voltage during the two different phases characterizing the switching period can be written:

$$V_{C_1} = V_{in} - V_{out} \tag{2.3}$$

$$V_{C_1} = V_{out} \tag{2.4}$$

Equation 2.3 relates to phase one, when SW_1 and SW_4 are on, while equation 2.4 corresponds to phase two (hence, SW_2 and SW_3 are on). Putting together these equation, one can easily recover the conversion ratio M for the Switched Capacitor converter depicted in 2.2:

$$M = \frac{V_{out}}{V_{in}} = \frac{1}{2} \tag{2.5}$$

From equation 2.5, it is clear why such converter is named a 2:1 step-down Switching Capacitor converter.
Unfortunately, SC converters are affected by a fundamental limit, namely the charge redistribution loss mechanism. To address this issue, many derivative architectures of the more traditional schematic presented in figure 2.2 have been developed. All the alternative topologies are generally based on the same key factor: the introduction of some inductive elements into the standard SC architecture such that charging and discharging phases of the flying capacitor C_1 becomes lossless [9]. This technique is called *soft-charging* and is aimed at preventing the flying capacitor to experience instantaneously a voltage drop different from zero and to absorb the voltage steps in a lossless way. Following this idea, the circuit in figure 2.2 can be modified as depicted in figure 2.3, obtaining what is called a 2:1 *Resonant Switched-Capacitor (ReSC)* step-down converter.

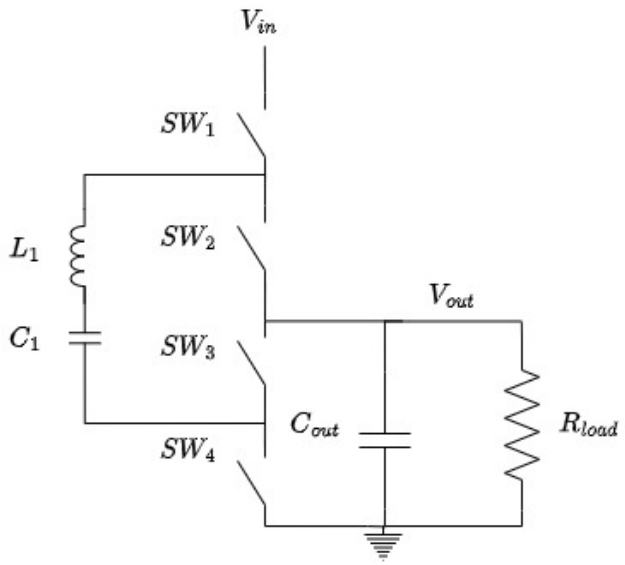

Figure 2.3: Circuit implementation of a 2:1 Resonant Switched Capacitor (ReSC) step-down converter. [1]

The introduction of the resonant tank made of C_1 and L_1 allows to both prevent voltage steps on the flying capacitor and limit the capacitor current at the switching instants, avoiding excessively high current peaks typical of SC converters [1].
It has been proven that ReSC converters allow to overcome the most significant limitations of SC converters, simply by introducing a small inductor in the circuit. The introduced soft-switching technique guarantees higher efficiency for a wide range of power densities compared to the basic SC converter. More importantly, studies show that in a 2:1 ReSC converter, the inductor size can be chosen significantly smaller than that of a traditional buck converter, justifying the choice

of the former architecture against the latter in contexts where improved power density and high efficiency are simultaneously required [10].
Concluding this digression, it is possible to affirm that with the purpose of designing fully-integrated DC/DC converters, *Resonant Switched-Capacitor (ReSC)* converters represent a valid and interesting solution to achieve improved power density and mass reduction, while guaranteeing high efficiency. Nevertheless, as the purpose of this thesis work is to design analog blocks for the converter's control circuit, it was decided to simulate the final control system using a buck converter for the power stage. This choice allowed to lighten the computational cost of the simulations performed to test altogether the designed blocks and, in particular, these blocks can be easily adapted for integrated solutions as the one described in this section.

2.2 Control circuit

A fundamental block in every DC/DC converter, in spite of the chosen architecture for the power stage, is the control circuit. In figure 2.4, a simplified scheme of the implemented control loop is shown; the highlighted blocks were realized in the context of this master thesis.

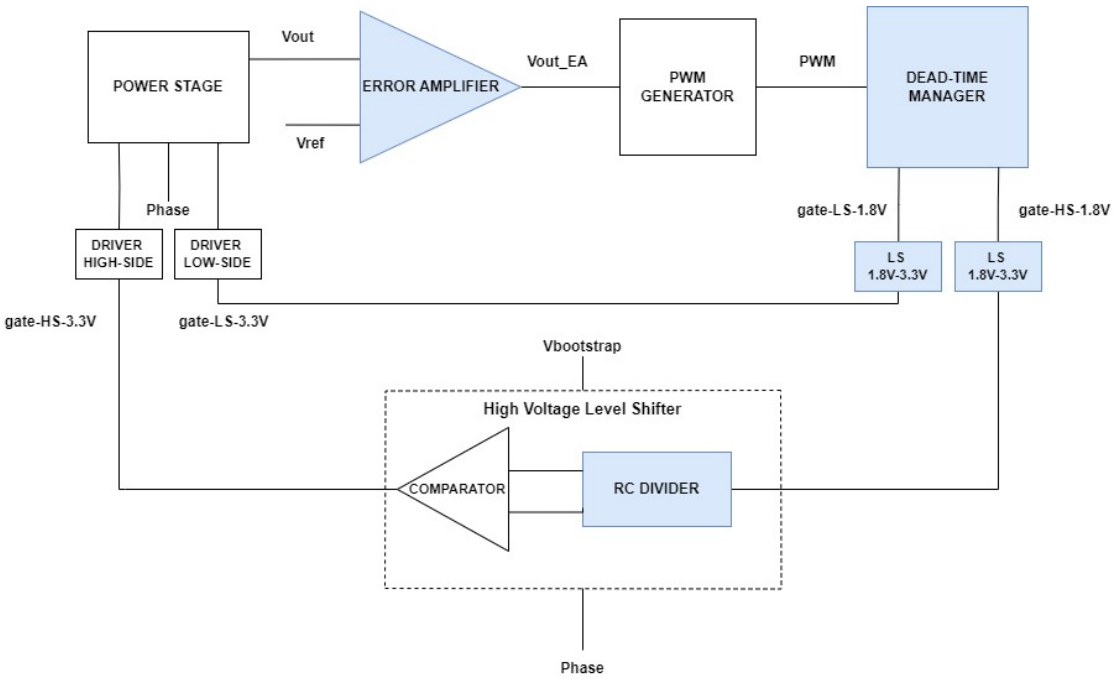

Figure 2.4: Schematic of the implemented control circuit for a fully-integrated DC-DC converter.

The purpose of such control circuit is to regulate the output voltage, ensuring that

the correct value is reached regardless of input voltage variations. To achieve such result, the first element of this loop is the error amplifier, whose purpose is to compare the produced output with the reference voltage V_{ref} of 600mV, generated by a bandgap circuit. Any significant difference detected between V_{out} and V_{ref} is then amplified and fed back to the power stage through the control loop, with the purpose of re-adjust V_{out} to the correct value.
The accomplishment of this procedure needs the operation of several different blocks: first of all, the output of the error amplifier, V_{EA}^{out}, is translated by a Pulse Width Modulator (PWM) into a duty cycle for the driving signals of the power stage, while keeping their frequency constant.
Regardless of the final structure of the power stage, it is fundamental that switches operating in different phases of the switching period do not cross-conduct. For this reason, a dead-time manager has been developed. In particular, during the realization of this project, several delay elements were designed, whose purpose is to introduce some dead-times between the driving signals of the high-side switch and low-side one, to guarantee sufficient time distance between the activation of the two switches and avoid cross-conduction. The main purpose of this dead-time manager is to control the actual delay of the designed delay-blocks through an external current; in this way, the same control loop could be exploited for different switching frequencies, making it very flexible and adaptable.
After ensuring sufficient time-distance between high-side and low-side gate voltages, these two must be shifted from the 1.8V domain to higher voltages domain to correctly drive the power stage. Indeed, as the input voltage V_{in} is equal to 20V, assuming for simplicity to implement a buck converter for the power stage, it is necessary to use high-voltage transistors as switching devices, able to withstand at least 20V between their source and drain contacts. In the exploited technologies, such high-voltage transistors need to be driven by a 3.3V V_{gs} to properly work. Hence, a 1.8V to 3.3V level shifter was designed and placed after the dead-time manager, before the drivers.
Concerning the low-side signal, this first shift is sufficient to produce the required voltage for the corresponding driver; instead, the high-side gate voltage needs more manipulation before being able to drive the high-side switch. Analysing figure 2.1, it is clear that, to properly drive the high-side switch, a difference of 3.3V is required between its gate and its source; however, the phase node moves between 0V and 20V, meaning that a gate signal varying between 0V and 3.3V is not suitable for this task. It is necessary to shift signal V_g^{HS} from the [0V, 3.3V] domain to the $[Phase, Phase + 3.3V]$, so that whenever the phase node moves, a Vgs^{HS} of 3.3V is guaranteed, ensuring proper turning-on of the high-side switch. This task was accomplished by designing a Bootstrap circuit (or high-voltage level shifter) made of an RC divider and a comparator. This circuit behaves as a level shifter: it takes

as input the high-side signal after being shifted to the [0V, 3.3V] voltage domain and translates it into the correct voltage domain, finally achieving the proper gate voltage for the high-side switch.

Chapter 3

The Error Amplifier

This chapter will focus on the design of one of the most important blocks of the control system: the error amplifier. The purpose of this block is to ensure that the output voltage is stable, while detecting any significant differences between the latter and the temperature independent voltage provided by a bandgap reference. In this way, the output node will be sensed by the error amplifier, which generates the control signal to be fed into the Pulse Width Modulator (PWM); the latter, together with the delay generator, controls the Ton, i.e. the time interval during which the phase node is shorted to V_{in}, equal to 20V in the context of this work. Hence, the control voltage produced by the error amplifier allows to control Ton, adjusting it depending on the variations detected on the output node. Therefore, being the output voltage proportional to the duty cycle (which is the ratio Ton over the whole period), the final result is that the control signal of the error amplifier sets the output voltage to the required value. The previously described control mechanism is nothing but a PI (Proportional Integral) compensation filter, that is used to increase the low-frequency loop gain, such that the output is better regulated both at DC and at frequencies well below the loop crossover frequency. The error amplifier block produces at the same time the proportional term of the feedback control system and the integral term. The former refers to the gain between the error and the control signal, while the latter accounts for past values of the error signal by integrating it over time; basically, this term seeks to eliminate the residual error by adding a control effect due to the historic cumulative value of the error [8]. For such application, the bandwidth of the error amplifier must be sufficiently larger than the bandwidth of the control loop and high stability must be ensured. The following discussion is then focused on the design strategies adopted to guarantee sufficiently high bandwidth and stability for the block under analysis, together the most relevant achieved simulation results.

3.1 Design Methodology

The adopted design methodology was aimed at discovery the circuit implementation that would enable reaching the target specifications. For this purpose, standard topologies have been investigated, and eventually modified to obtain performances compliant with both target specifications and the harsh-environment of HEP experiments in terms of radiation levels and temperature. More specifically, each circuit was tested at first in the nominal corner (power supply voltage Vdd = 1.8 V at a working temperature of 27°C); once this simulation results were compliant with target specifications, the whole circuit can be simulated in 865 different radiation corners, taking into account temperature and process variations, as well as different irradiation conditions and transistors working areas. The ultimate step of this design strategy consists in realizing the layout of the chosen topology, and subsequently perform post-layout simulations, based on the extraction of parasitic capacitances and resistances (PEX) from the layout. The latter procedure allows to assess if also the physical design will be compliant with target performances and whether the circuit implementation needs to be further optimized to compensate for the effect of parasitic extraction. Therefore, a series of radiation corners simulations will need to be performed to consolidate both the circuit implementation and the layout before concluding the design, as it will be thoroughly explained in 3.3.

3.1.1 Target Specifications

The performances of the error amplifier are mainly characterized by four parameters: the gain bandwidth (GBW), the DC gain, the Phase Margin (PM) and the input offset. In the context of designing a control circuit, it is fundamental to ensure good stability, meaning that $PM > 60°$, and low input offset (ideally within the range: -2mV|+2mV); then, it is necessary to provide a GBW at least ten times higher than the working frequency of the loop, which is the one that guarantees the highest conversion efficiency. In the context of this thesis work, the maximum achievable switching frequency of the power stage is 8MHz, hence a target GBW of 80MHz was chosen. Finally, as the purpose of the error amplifier is to detect very small disturbances on the output node, the final topology must guarantee a very high DC gain, ideally above 80 dB. Another parameter to observe is the current consumption of the block. One of the main obstacle in this design was to reach the requested GBW, while guaranteeing an acceptable current consumption. Considering that the design was realized exploiting a highly power consuming 180nm technology, a GBW of 80 MHz is really demanding in terms of current consumption. For this reason, the final implementation of this 80MHz

error amplifier will be characterized by a power consumption in terms of current of 300 µA. Nevertheless, this result is quite satisfactory if one evaluates one of the most important Figures of Merit (FOM) for an amplifier, which quotes how much GBW can be obtained for a certain load capacitance and power consumption, and is given by:

$$FOM = \frac{GBW \cdot C_L}{I} \tag{3.1}$$

where C_L represents the load capacitance, fixed by the ramp-generator at the output of the error amplifier, and I is the overall current consumption. For the final design, a value of 266 $\frac{MHz \cdot pF}{mA}$ is found, which is an excellent result if one considers that for most amplifiers this value is comprised between 100$\frac{MHz \cdot pF}{mA}$ and 200$\frac{MHz \cdot pF}{mA}$ [11].

As future application of the converter to be developed may require lower current consumption, in the end three error amplifier were designed:

1. Very high-speed Error Amplifier (EA): 80 MHz, 300 µA.
2. High-speed, low power EA: 40 MHz, 130 µA.
3. Ultra low-power EA: 20 MHz, 58 µA.

These three blocks are based on the same circuit topology, with small modifications on transistor's multiplicity and dimensions of the Miller compensation network. For this reason, the sizing approach and the encountered obstacles will be presented only with respect to the 80 MHz error amplifier, the most challenging one.

3.1.2 Analysed topologies

According to literature research, the best implementation for an amplifier that has to guarantee a very high DC gain, while ensuring a sufficiently wide dynamic range, consists of a two-stage amplifier, where the first stage is a cascode amplifier and the second stage can simply be a common source. However, it is possible to find different circuit topologies for the first stage. In this thesis work, mainly two topologies were explored: the symmetric cascode and the standard folded cascode.

- **The symmetric OTA with cascodes.** This topology was firstly explored as it is characterized by an intrinsically low offset, due to the symmetry of the structure: the input devices see exactly the same DC voltage and load impedence. As a result, matching is improved, providing better Common Mode Rejection Ratio (CMRR). Furthermore, cascodes are added to provide gain boosting, without disrupting the symmetry of the device (as they are added to each side). The final circuit consists of a two-stage amplifier where the

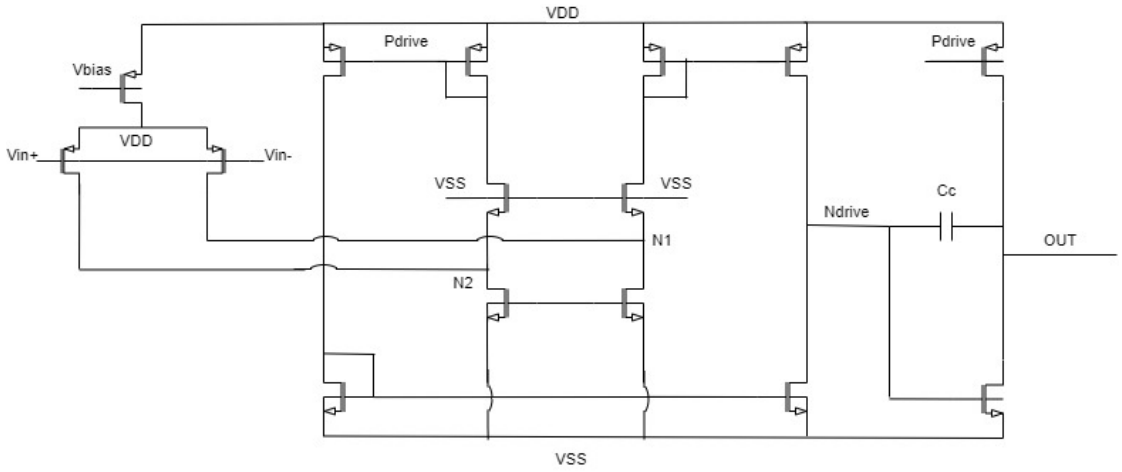

Figure 3.1: Schematic of the two-stage EA exploiting symmetric cascode as first stage.

second stage is a common source, which guarantees high output swing. To ensure stability, it was necessary to introduce a Miller capacitance to split the two low frequency poles that are otherwise generated, due to the high impedence found at nodes N1 and Ndrive. Transistors' sizes were optimized exploiting the Matlab script from Boris Murmann of Stanford University, that will be discussed in the section devoted to the sizing approach. Despite this optimization, the amplifier depicted in figure 3.1 does not allow to reach a GBW higher than 20MHz, preserving the stability and ensuring an acceptable power consumption.

Output	Specifications	Nominal Corner
GBW	> 60 MHz	18.7 MHz
Phase Margin	$> 60°$	72 °
DC gain	> 80 dB	80.4 dB
Input DC offset	range -2mV|+2mV	$-42.2\,\mu V$

Table 3.1: Simulation results for stability analysis.

In table 3.1, it is possible to analyse the simulation results for the nominal corner of the symmetric cascode amplifier. These results were achieved with a current consumption of $280\,\mu A$ and still the gain-bandwidth product (GBW) is not sufficiently high. Indeed, while ensuring very low offset and stability, the current consumption is intrinsically higher than what can be achieved with a standard folded cascode, due to the presence of two more branches in the first amplifying stage. Concluding, this topology was discarded, as it requires at least twice the power consumption that could be achieved with

a folded cascode (as it will be proven in the following) to reach the desired speed performances.

- **The standard two-stage folded cascode amplifier.** The next undertaken step was to optimize the standard folded cascode OTA topology, with a common source as second stage. This topology has the advantage of reaching an higher low-frequency gain, thanks to the possibility of introducing both P and N cascodes, which increases the output resistance of the first stage and, hence, the gain. Furthermore, the circuit is still quite symmetrical thanks to the adopted low-voltage P-type current mirror, which helps ensuring that the same voltage is reached in each node of the two branches of the cascode. Therefore, very high gain and low input offset are ensured, and also good stability can be guaranteed, exploiting Miller compensation theory.

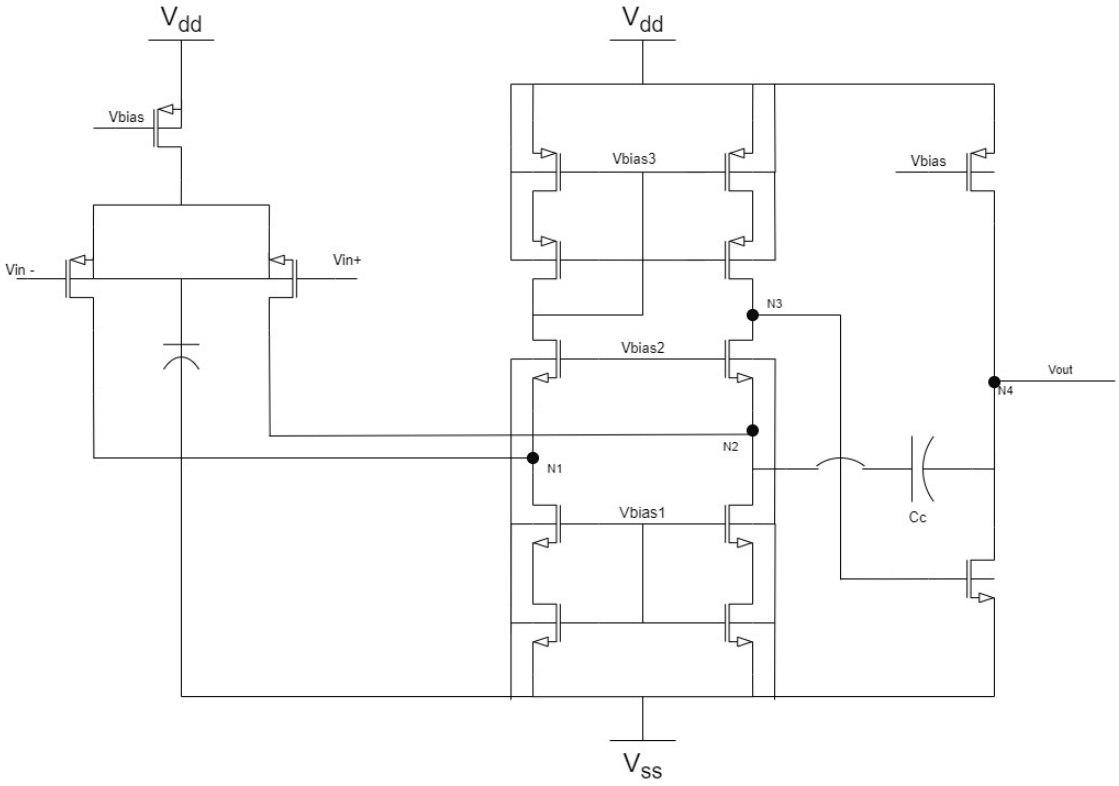

Figure 3.2: Two-stage folded cascode Error Amplifier circuit implementation.

The circuit in figure 3.2 represents the first developed amplifier adopting a folded cascode in the first stage. To the standard topology, an additive NMOS stage in the active load was introduced to increase the output resistance; as a result, the DC gain would be boosted and the dominant pole

would move towards lower frequencies, which helps improving the GBW. The DC operation of this device is based on the following mechanism: the input transistors of the differential pair are biased by the current source (PMOS) on top; in this specific case a biasing current of 64 µA was chosen, meaning that each device receives 32 µA. The same current provided by the biasing PMOS is drawn by the N-type active load, causing the difference between this current and the one coming from the input transistors to be pulled from the cascode pair. Finally, the current source above the cascodes mirrors this current. To avoid any kind of artifacts, such as asymmetrical swing or reduction of the slew rate, the two input transistors and the cascodes should see the same current of 32 µA. Notice that the choice of the current value is strictly influenced by target specifications and sizing decisions, that will be analysed in the following. Once again, Miller compensation was necessary to split the two low-frequency poles generated at the outputs of each stage, i.e. node 3 and node 4 displayed in figure 3.2. Introducing a proper capacitance between the output of the cascode and the common source splits the two poles: the pole generated by the output load CL (not shown in figure 3.2) will be moved towards lower frequencies, becoming the dominant pole; meanwhile, the pole generated at node 3, which depends on the parasitic capacitances at that node, will be moved towards higher frequencies and will now be determined by the Miller capacitance Cc, becoming the non-dominant pole. This procedure ensures stability, as each pole produces a decrease of the Phase Margin of 90°; hence, having two poles close to each other at low-frequency means having a PM close to -180°, which causes instability and the circuit would behave as an oscillator. It is important to underline that the choice of placing one end of the Miller capacitance at node N2 in figure 3.2 is not unforeseen: the connection source-gate avoids the introduction of a positive zero in the transfer function, that should eventually be compensated by a resistance placed in series to the Miller capacitance. Without this connection, the Miller compensation network would not be unidirectional, meaning that any feed-forward signal can affect the output, generating instability. The introduction of Cc at the low impedence node leads to a unidirectional compensation network, in the sense that only the feedback signal is still present, while the feed-forward current is blocked. Indeed, thanks to the new path from output to cascodes, the feed-forward current will not be able to flow through the output transistor, but will be forced to take the path through one of the cascodes [12]. As a result, the zero in the transfer function disappears and the system is stable. Concerning transistors sizing and tuning of the compensation network, the chosen approach will be depicted in paragraphs 3.1.5 and 3.1.3, as it coincides with the one adopted for the final design. Af-

ter a first optimization of this circuit, simulation results immediately proved the superiority of this topology with respect to the circuit in fig. 3.1

Output	Specifications	Nominal Corner
GBW	> 60 MHz	40.97 MHz
Phase Margin	$> 60°$	69.44°
DC gain	> 80 dB	99.07 dB
Input DC offset	range -2mV|+2mV	116.6 µV

Table 3.2: Simulation results for stability analysis for the circuit in figure 3.1.

The data displayed in table 3.2 refer to simulation performed on the nominal corner for the circuit of fig. 3.2, with an overall current consumption of 199.4 µA. Even though the GBW product is still far from the target result presented in section3.1.1, it is still a great improvement with respect to the previously analyzed topology. To further boost the gain bandwidth product, some modifications to this topology were made in order to reach the final design. Indeed, this implementation could not reach the target speed consuming less than 400 µA, meanwhile with some adjustments to the schematic, the same result was achieved with only 300 µA, as it will be explained in the following section.

- **Final implementation.**

  The final circuit is displayed in fig. 3.3. It consists of a standard folded cascode with slight modifications to the topology, in order to increase the GBW. Indeed, the standard folded cascode topology could reach 80 MHz of gain-bandwidth product with a current consumption of at least 400 µA, meanwhile, as already underlined in section 3.1.1, the ultimately designed circuit is able to reach 80 MHz, with a current consumption of 300 µA. To achieve such result, the main adjustment to the standard topology consists in moving the Miller capacitor from the low-impedence node (N2 - LZ in fig. 3.3) to the high-impedence one (N3-HZ), where also the gate of transistor M13 is connected. As it will be demonstrated in sec. 3.1.5, this connection introduces a positive zero in the transfer function, which forces the use of a resistor in series to the Miller capacitor to guarantee stability. If the value of Rc is properly chosen, the positive zero can be transformed into a negative one: the former would induce a -90° shift in the Phase Margin, behaving as a pole; meanwhile, the latter generates a +90° PM shift, which can compensate the -90° decrease induced by the non-dominant pole. Optimization of transistors sizes and tuning of the compensation network lead to the following results in the nominal corner:

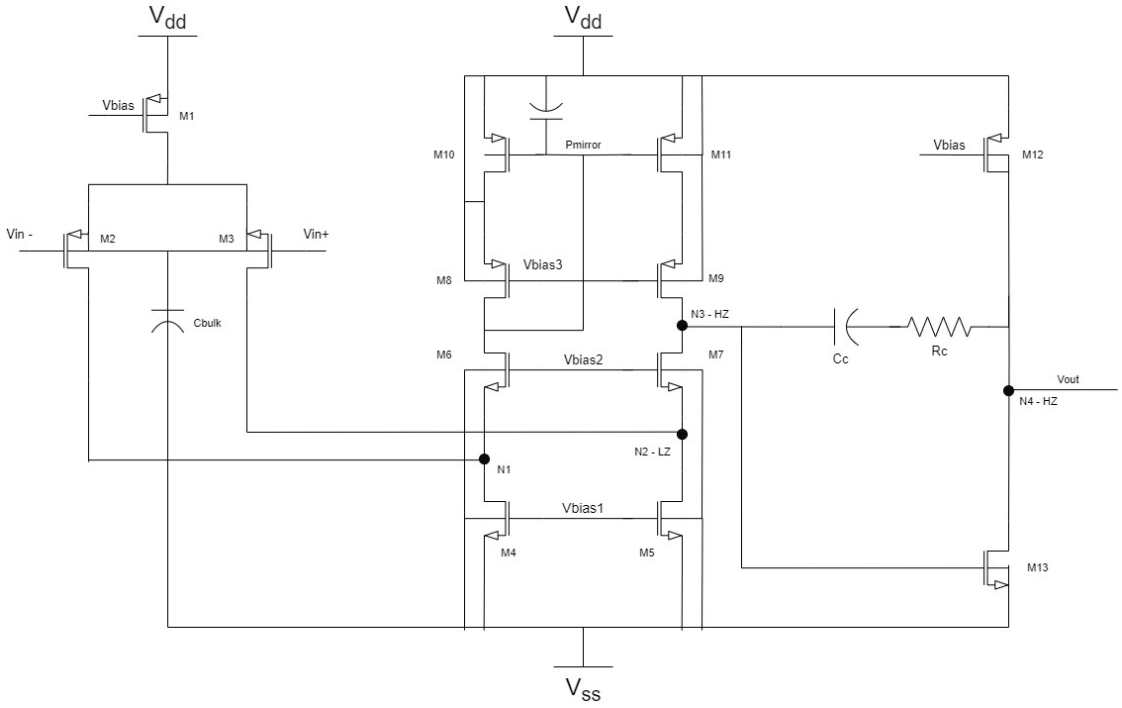

Figure 3.3: Final two-stage folded cascode Error Amplifier circuit implementation.

Output	Specifications	Nominal Corner
GBW	> 60 MHz	97.79 MHz
Phase Margin	$> 60°$	88.26°
DC gain	> 80 dB	99.6 dB
Input DC offset	range -2mV|+2mV	$-42.3\,\mu V$

Table 3.3: Simulation results for stability analysis for the circuit in figure 3.3.

As easily understandable from table 3.3, the circuit in figure 3.3 allows to meet all the target specifications, with a current consumption equal to $300\,\mu A$, which is well below the current consumption of the circuit in fig. 3.2 ($400\,\mu A$), justifying the choice of implementing the circuit in fig. 3.3 as the

final design for the Error Amplifier.

3.1.3 Sizing approach

To understand the sizing approach undertaken in designing the Error Amplifier it is necessary to introduce the EKV (Enz-Krummenacher-Vittoz) model for low-power IC (Integrated Circuit) design. Starting from semiconductor physics, this model provides expressions of the drain current of a MOS (Metal-Oxide-Semiconductor) Transistor valid in all inversion regions, both weak, moderate and strong [13]. According to [14], one of the most important parameter of a transistor in analog applications is its transconductance g_m at a given biasing point Q.

$$g_m = \frac{\partial I_d}{\partial V_g}\Big|_Q \tag{3.2}$$

From equation 3.2, it is implied that the transconudctance represents the slope of the $Id(Vg)$ curve at the chosen biasing point Q, where:

$$I_d = id + I_D \tag{3.3}$$

$$V_g = v_g + V_G \tag{3.4}$$

In equations 3.3 and 3.4, i_d and v_g represent small variations of the two signals with respect to the biasing point Q that is a function of the DC values I_D and V_G, namely: $Q = (V_G, I_D)$. A direct consequence of these formulae is the use of the transconductance g_m to amplify signals: it represents the gain in the drain current of a MOST, when the voltage V_g is applied on the gate. This discussion allows to introduce the most important small-signal amplifying parameter of a MOST: the transconductance efficiency g_m/I_d.

$$\frac{g_m}{I_d} = \frac{1}{nU_T}\frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + I_c}} \tag{3.5}$$

In equation 3.5, U_T is the thermal voltage ($U_T = \frac{K_B T}{q} \approx 26mV$, with $K_B = 1.38 \times 10^{-23} \frac{J}{K}$ being Boltzmann constant), n is a technological parameter called the slope factor (generally comprised between 1.2 and 1.6) and I_c is the inversion factor, a single parameter that allows to determine the inversion level of a transistor. The inversion factor is defined as follows:

$$I_c = \max\left\{\frac{I_F}{I_s}, \frac{I_R}{I_s}\right\} \tag{3.6}$$

where I_s is the specific current,

$$I_s = 2nK_p\frac{W}{L}U_T^2 \tag{3.7}$$

while I_F and I_R are, respectively, the forward and reverse current through the transistor channel, such that:

$$I_d = I_F - I_R \tag{3.8}$$

The complete expressions for the reverse and forward currents can be found at [14]. Depending on the value of the inversion factor, it is possible to distinguish the following situations:

- Weak inversion: $I_c \leq 0.1$
- Moderate inversion: $0.1 < I_c \leq 10$
- Strong inversion: $i_c \geq 10$

Recalling equation 3.5, it is evident that it only depends on the inversion factor: g_m, the most important amplifying parameter of the transistor, is related to the drain current at the biasing point I_D only through the inversion coefficient. If the static consumption, namely I_D, is known, as well as the operating region, the transconductance is easily deduced. Similarly, knowing g_m and fixing the inversion coefficient, is sufficient to find the biasing current, through which one can easily recover the proper size ratio $\frac{W}{L}$ for the transistor in the amplifying stage. The latter strategy is the one undertaken in this thesis work to properly size transistors in the Error Amplifier. Indeed, assuming to be in saturation (a necessary condition to operate any MOST as an amplifier), it is possible to demonstrate that:

$$I_F \gg I_R \tag{3.9}$$

and, as a direct consequence of 3.9 it is clear that:

$$I_D \approx I_F \tag{3.10}$$

$$I_c = \frac{I_F}{I_s} \tag{3.11}$$

Putting together equations 3.11, 3.10 and 3.7, it is straightforward that:

$$\frac{W}{L} = \frac{I_D}{2nU_T^2K_pI_F} \tag{3.12}$$

Equation 3.12 proves that to properly size a transistor for amplification purposes it is sufficient to know its drain current and inversion coefficient, as the other parameters of the equation depend only on the technology.

Summarizing, in the context of properly sizing transistors for the Error Amplifier designed in this thesis work, mainly two equations were exploited to obtain the ratio $\frac{W}{L}$, i.e. equations 3.5 and 3.12: the former allows to get the drain current I_D, knowing the transconductance g_m and choosing a suitable value for the inversion coefficient I_c; the latter gives the ratio $\frac{W}{L}$ as a function of the recovered drain current and the chosen I_c. That being said, the only question remains how to obtain the transconductance g_m. The answer to this question is easily recovered analysing the frequency response of a generic 2-stage amplifier with compensation network:

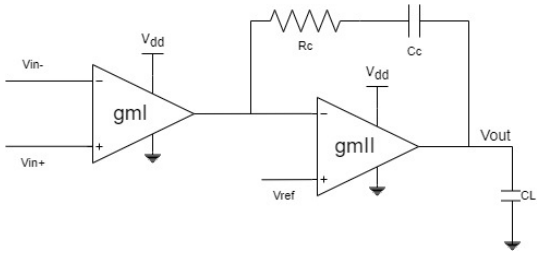

Figure 3.4: Schematic of a generic 2-stages amplifier with compensation network [12]

Figure 3.4 depicts a generic two-stage amplifier, which consists of a differential input stage that converts the differential input voltage into a current, through the transconductance g_{m_I}. A second stage follows, a common source in this specific case, with a transconductance $g_{m_{II}}$, by means of which it transforms the input current into the output voltage. The Error Amplifier designed in this work falls in to the category described above and, as already explained in section3.1.1, it is possible to highlight three fundamental specifications that guide the design of such amplifying stage: the low-frequency or DC (Direct Current) voltage gain, the gain-bandwidth product (GBW) and the phase margin. The DC gain is related to the transconductances and output resistances of each stage, respectively g_{m_I}, $g_{m_{II}}$, R_{o_I} and $R_{o_{II}}$; for a generic 2-stage amplifier, the following expression holds:

$$|A_0| = \frac{|v_{out}|}{|v_{in}|} = |A_{v_I}| \cdot |A_{v_{II}}| = g_{m_I} R_{o_I} \cdot g_{m_{II}} R_{o_{II}} \tag{3.13}$$

The full expression for the two output resistances, R_{o_I} and $R_{o_{II}}$, will be carried out in 3.1.5. Concerning the GBW, it represents the unity-gain frequency (the frequency where the gain reaches 0dB, namely the gain is equal to the unity in the linear scale) and is given by the product between the low-frequency gain and the bandwidth, which is the pole frequency of the dominant pole. For a circuit as the one in fig. 3.4, it is possible to derive the bandwidth as follows:

$$f_{pdom} = \frac{1}{2\pi R_{Miller} C_c} \tag{3.14}$$

where R_{Miller} is the equivalent resistance seen by Miller capacitor C_c and can be easily derived writing the KVL for circuit in 3.4:

$$R_{Miller} = \frac{V_{Miller}}{i_{R_{o_I}}} = \frac{|v_{in}| \cdot |A_{v_I}| \cdot |A_{v_{II}}| + |v_{in}| \cdot |A_{v_I}| \frac{R_c}{R_{o_I}}}{\frac{|v_{in}| \cdot |A_{v_I}|}{R_{o_I}}} \tag{3.15}$$

Simplifying,

$$R_{Miller} = |A_{v_{II}}| \cdot R_{o_I} + R_c \approx |A_{v_{II}}| \cdot R_{o_I} \tag{3.16}$$

Being $|A_{v_{II}}| \cdot R_{o_I} \gg R_c$.

Finally, it is possible to write the expression of the dominant pole:

$$f_{pdom} = \frac{1}{2\pi |A_{v_{II}}| R_{o_I} C_c} \tag{3.17}$$

And, multiplying by the DC gain, one can finally derive the gain-bandwidth product:

$$GBW = |A_0| \cdot f_{pdom} = g_{m_I} R_{o_I} \cdot g_{m_{II}} R_{o_{II}} \cdot \frac{1}{2\pi g_{m_{II}} R_{o_{II}} R_{o_I} C_c} = \frac{g_{m_I}}{2\pi C_c} \tag{3.18}$$

From equation 3.18, it is easily understandable the relation between the transconductance of the first amplifying stage and the GBW, given by target specifications. To get the final expression for g_{m_I} as a function of GBW, it is still needed the value of the Miller capacitance C_c; one can demonstrate that the optimum value of C_c is 2-3 times smaller than C_L [12]. As a preliminary step for the design of the Error Amplifier, the value of C_c was chosen to be equal to $C_L/2$, where C_L is the input capacitance of the ramp generator that follows the Error Amplifier and is equal to 1pF. Therefore, the final expression for the transconductance of the first stage is:

$$g_{m_I} = 2\pi \cdot GBW \cdot C_c \tag{3.19}$$

Equation 3.19 was exploited to find the value of transconductance of the first stage, knowing that $GBW = 80dB$ and initially choosing $C_c = 0.5pF$ (the latter value will be changed after optimizing the compensation network to meet specifications even in radiation corners). Knowing g_{m_I} allows to size the differential pair transistors by simply substitute the recovered value in equation 3.5 and combine the latter with equation 3.12. To get a numerical value for the $\frac{W}{L}$ ratio, one has to ultimately guess the inversion coefficient, that for instance was fixed to 10 for the differential pair. Actually, at this point of the procedure a more sophisticated approach involves the exploitation of the Matlab script developed by professor Boris Murmann to obtain a numerical solution for the width of transistors M2 and M3 of circuit 3.3. This script is based on look-up tables consisting of hundreds of

previously performed simulation results for the DC point of both P and N-channel devices. In particular, these look-up tables contain many transistor's parameters (threshold voltage V_{th}, K_p, ideality factor n) for different values of V_{DS}, W, L and V_{GS}. Indeed, while it is possible to guess realistic values for V_{th}, K_p and n from the device catalogue, those parameters still depends on transistor's dimensions and voltages; hence, the solution provided by Murmann's script is much more accurate. The actual procedure implemented in this thesis work consists of the following steps:

1. Extract the transconductance of the first stage g_{m_I} from equation 3.19;

2. Roughly estimate the inversion coefficient I_c by putting together equations 3.5 and 3.12, and using approximated parameters from the device catalogue.

3. Guessing I_c, one can have a first numerical solution for the transconductance efficiency $\frac{g_{m_I}}{I_d}$ and, knowing g_{m_I}, it is finally obtained the current of that particular transistor to reach the required transconductance in the chosen inversion condition.

4. Finally, exploiting the look-up tables generated by Murmann's script, one can extract the ratio $\frac{I_D}{W}$ as a function of V_{DS} and V_{GS} (known from circuit analysis) and the gate length L of the transistor, which has to be guessed.

5. Check the obtained result, to see if it is feasible to have a transistor of that size, and eventually optimize it playing with the values of I_c and L, hence re-iterate until a solution compliant with the purpose of the design is reached.

It is important to underline that this procedure can guarantee just a rough starting point for the sizing, as optimization through real simulations is then needed, especially to improve circuit behaviour in radiation corners. Furthermore, several iterations of this procedure, assisted by simulations, were performed to determine the smartest choice for the gate length, which had to be guessed based on some guidelines, such as the channel conductance g_{ds}, which depends on L, or the purpose of the transistor itself: for current mirrors (M8, M9, M10, M11) is preferable to have a large gate length, as it ensures almost negligible Early effect, fundamental to correctly copy the current; for the cascode pair (M6, M7) a very small gate length was chosen, to boost the dynamic output range of the first stage; finally, concerning the active loads (M4 and M5), matching with the transistor providing Vbias1 was necessary, but a multiplication factor was introduced, to ensure that the current flowing on this load was twice the current of the differential pair. Again, all the currents and lengths are known, which means that the Matlab script can be easily exploited to size all the cited transistors (M4-M11). At this point, one can also estimate the size of transistor M0, as its drain current is clearly twice

the current flowing in M1 and M2. Therefore, the above procedure can be adapted for this purpose, starting from I_{D0} and guessing I_c to find the transconductance and, finally, the dimensions of M0.

The next fundamental step is to size transistor M13, i.e. the amplifying transistor of the second stage. To achieve this result, the same procedure previously depicted was implemented, with the only difference in the extraction of the transconductance $g_{m_{II}}$, which in this case depends on the non-dominant pole's frequency. To determine the non-dominant pole's frequency, stability must be taken into account: an amplifier is considered stable when no peaking affects the frequency response and, if a square-wave signal is applied to its input, no ringing is exhibited in output. All these requirements can easily be guaranteed if a phase margin of at least 60° is ensured. Indeed, peaking or onset of oscillations would only be possible if the phase of the output transfer function approaches -180°; in this case, the negative feedback would be converted into a positive feedback, generating oscillations. Therefore, the concept of Phase Margin can be introduced: it represents the distance in degrees between the -180° line and the actual phase of the amplifier, evaluated where the loop gain is unity, i.e. at the GBW. [12].

Clearly, if Miller compensation was not exploited in the design, there would have been two low-frequency poles very close to each other and, since each pole produces a phase shift of -90°, the phase would have suddenly drop to -180°, disrupting stability. Meanwhile, the introduction of Miller capacitance allows to split the two poles: the first is moved towards lower frequencies and the second one towards higher frequencies. This procedure sure helps improving stability, but there is still one more strategy that can be exploited to have a phase margin as close as possible to 90°. It can be proven that the optimal value for the phase margin, i.e. $PM \geq 60°$ is found when:

$$f_{p_{non-dom}} = 3 \cdot GBW \tag{3.20}$$

The non-dominant pole frequency can be found using the same procedure exploited to find the dominant pole:

$$f_{p_{non-dom}} = \frac{1}{2\pi C_L R_L} \tag{3.21}$$

where R_L is the equivalent resistance seen from the capacitor C_L and can be derived from the circuit in figure 3.4, assuming that all the DC generators are turned off and that the working frequency is much higher than the one of the dominant pole, such that the Miller capacitor can be approximated to a short circuit. Under these assumptions, one can demonstrate that:

$$R_L = \frac{1}{g_{m_{II}}} - \frac{R_c}{R_{o_I} \cdot g_{m_{II}}} \tag{3.22}$$

In section 3.1.5 the full calculation for R_{o_I} will be carried out, showing that

$$R_{o_I} \gg R_c \tag{3.23}$$

Hence,

$$R_L \approx \frac{1}{g_{m_{II}}} \tag{3.24}$$

The expression of the non-dominant pole is therefore given:

$$f_{p_{non-dom}} = \frac{g_{m_{II}}}{2\pi C_L} \tag{3.25}$$

Finally, exploiting relation 3.20, the transconductance of the second stage can be derived for stability:

$$g_{m_{II}} = 3GBW \cdot 2\pi C_L \tag{3.26}$$

Repeating the same procedure previously described and using expression 3.26 in the first step, the dimensions of transistor M13 can be easily found. Furthermore, also the current in the output stage is obtained, which allows to properly size transistor M12. In this case, the gate length of transistor M13 was chosen to be the closest possible to the minimum length allowed by the technology, i.e. 180nm, to ensure sufficient speed. Meanwhile, the dimensions of transistor M12 were actually chosen to guarantee matching with the transistor providing Vbias, that will be presented in section 3.1.4, with the exception of a multiplication factor introduced to ensure the required current in the output stage.

Finally, it was possible to choose the values for the Miller compensation network: for what concerns the capacitance C_c, it was already stated that an optimum value is found to be between one half and one-third of the load capacitance. Actually, a more precise calculation of C_c requires to take into account also the parasitic capacitances connected to node N3 in figure 3.3. If the latter were to be considered, the expression of the non-dominant pole 3.25 has to be modified as follows:

$$f_{p_{non-dom}} = 3GBW = \frac{g_{m_{II}}}{2\pi C_L} \cdot \frac{1}{1 + \frac{C_{n3}}{C_c}} \tag{3.27}$$

where C_{n3} represents the sum of the parasitic capacitances connected to node N3, which are represented in 3.5: Parasitic capacitances in a MOSFET include [15]:

- Overlap capacitance, generated by the lateral diffusion of source and drain doping, because of which there will be an overlap between gate and source/drain junctions. The general expression for the overlap capacitance is given by:

  $$C_{S_{overlap}} = C_{D_{overlap}} = WC_{ox}X_d \tag{3.28}$$

  where X_d is the width of the overlapping area and W is the transistor's width.

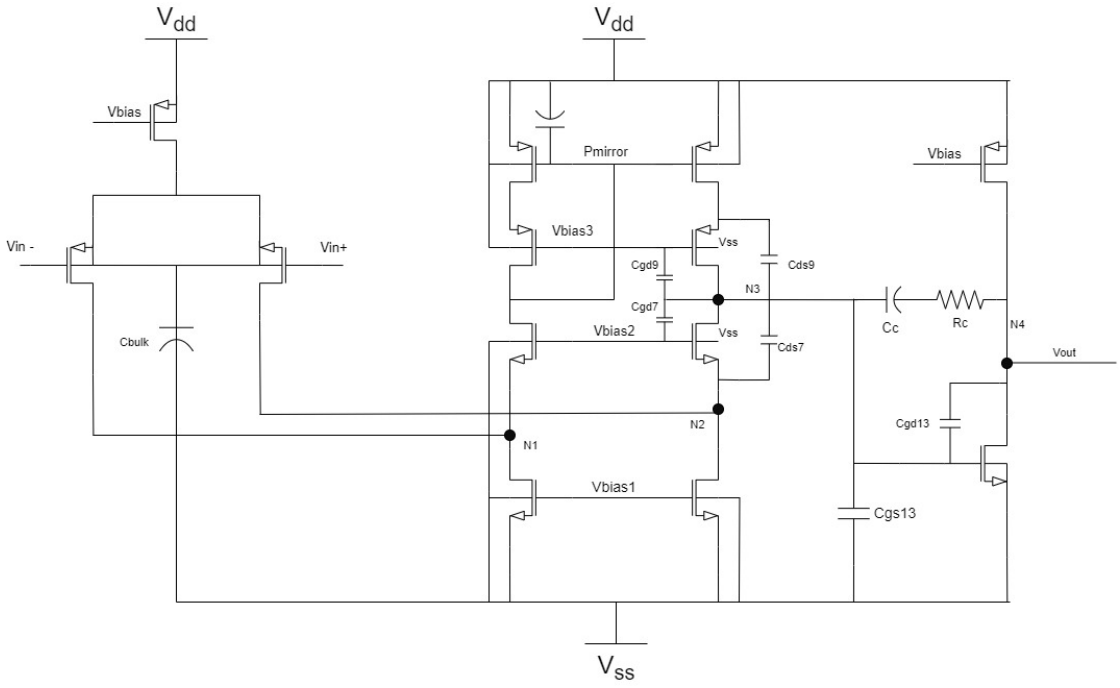

Figure 3.5: Final circuit implementation with all the parasitic capacitances connected to node 3.

- Channel capacitance, created between the gate and the charge in the channel; it is a non-linear and voltage-dependent capacitance. It can be proved that in saturation condition (the only relevant in this work), the channel capacitance is mainly between the gate and the source of the device:

$$C_{GS_{channel}} = \frac{2}{3} C_{ox} W L \tag{3.29}$$

  where L is the gate length.

- Junction capacitance, which consists of the depletion capacitance of source and drain and it depends on the bulk-source voltage:

$$C_{D_{junction}} = C_{S_{junction}} = C_J W L_s \tag{3.30}$$

  where C_J depends on technological parameters (doping and materials used) as well as V_{BS}, and L_s is length of source/drain contacts.

From this analysis, one can deduce that the only relevant contribution to the capacitance at node N3 is coming from the channel capacitance in saturation of transistor M13: $C_{GS_{channel}}$. First of all, it is possible to demonstrate that:

$$C_j \ll C_{ox} \tag{3.31}$$

Secondly, it is straightforward that:

$$L_s \ll L, \tag{3.32}$$

$$X_d \ll L \tag{3.33}$$

as both the overlap between source/drain and the gate X_d and the lengths of source/drain contacts are for sure smaller than the gate length of several order of magnitude. Consequently, all the parasitic capacitance coming from transistors M9 and M7, as well as the gate-drain capacitance of transistor M13 can be neglected with respect to the gate-source capacitance of transistor M1. Concluding,

$$C_{n3} = C_{GS_{13}} = \frac{2}{3} C_{ox} W L \tag{3.34}$$

Recalling equation 3.27, it can be proven that the correction factor $\frac{C_{n3}}{C_c}$ must be at most equal to 0.3, meaning that C_c has to be chosen not only two or three times smaller than the load capacitance, but also at least three times larger than the parasitic capacitance at node N3:

$$C_c \in (3 \cdot C_{n3}, \frac{C_L}{2}) \tag{3.35}$$

The value of the gate-source capacitance of M13 can be obtained simulating the DC operating point of the circuit in figure 3.3: $C_{GS_{13}} \simeq 20fF$; meanwhile, the load capacitance is fixed by the ramp generator's input capacitance and it's approximately 1pF. The final choice for the Miller capacitance was 300fF and in section 3.2 will be explained why neither $\frac{C_L}{2}$ nor $3C_{n3}$ were suitable options.

Finally, the value of the series resistance R_c is set by the following relation, which ensures the pole-zero compensation necessary for stability:

$$\frac{1}{g_{m_{II}}} < R_c \leq \frac{1}{3g_{m_I}} \tag{3.36}$$

The reason for this relation will be explained in section 3.1.5, where the calculation for the transfer function of the circuit in figure 3.3 will be carried out, exhibiting a zero given by the following expression:

$$f_z = \frac{1}{2\pi C_c \cdot (\frac{1}{g_{m_{II}}} - R_c)} \tag{3.37}$$

Clearly, to avoid the positive zero, it must be:

$$R_c > \frac{1}{g_{m_{II}}} \tag{3.38}$$

Meanwhile, to compensate the non-dominant pole it must be ensured that:

$$f_z = 3GBW = 3 \cdot \frac{g_{m_I}}{2\pi C_c} \tag{3.39}$$

which gives the second relation: $R_c \simeq \frac{1}{3g_{m_I}}$. Generally, it is preferable to have R_c as close as possible to the value of $\frac{1}{3g_{m_I}}$, in order to maximize the phase margin.

Substituting with the numerical values found for g_{m_I} and $g_{m_{II}}$ after optimization, one can find:

$$208\,\Omega < R_c, \tag{3.40}$$

$$R_c \simeq 1.3\,\mathrm{k}\Omega \tag{3.41}$$

While choosing $R_c = 1.3k\Omega$ ensures the pole-zero cancellation, analysing the circuit response in radiation corners it was proven that increasing R_c form this theoretical value is beneficial for the GBW, while preserving the phase margin. Indeed, the optimal value was found to be $R_c = 10\,\mathrm{k}\Omega$, as it will be explained in section 3.2.1.

Concluding, the results achieved with the sizing procedure described in this section can be summarized in table 3.4.

Device	Width	Length
M1	6 μm x 32	2 μm
M2, M3	9 μm x 24	1.5 μm
M4, M5	20 μm x 8	4 μm
M6, M7	4 μm	0.5 μm
M8, M9	10 μm x 2	0.5 μm
M10, M11	25 μm	5 μm
M12	6 μm x 96	2 μm
M13	8 μm x 2	0.18 μm

Table 3.4: Summary of sizing choices for the circuit in figure 3.3.

3.1.4 Design of the Biasing circuit

The design of a biasing circuit was necessary in order to provide the required biasing voltages to the circuit in figure 3.3, i.e. Vbias, Vbias1, Vbias2 and Vbias3. In particular, these voltages had to be generated starting from an input current of 2 µA, which is given as an input to the final Error Amplifier block.

The designed biasing circuit is shown in figure 3.6. Concerning the sizes chosen for these transistors, the same guidelines listed in section 3.1.3 were followed: to ensure correct mirroring of current, all the lengths were chosen to be above 2 µm

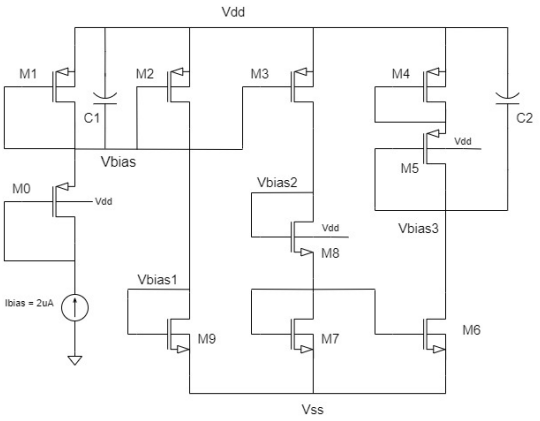

Figure 3.6: Biasing circuit

and, of course, transistors mirroring the same current had to be matched, except for the eventual multiplication factor to be introduced if more current is needed in that particular branch. Therefore, transistors M0, M1, M2, M3 were matched, as they are all copying the same current, and their dimensions determine the sizing of transistors M1 and M12 of circuit 3.3; similarly, transistor M9 is the reference to size transistors M4 and M5 in circuit 3.3. Meanwhile, for transistors M4 to M8 no particular matching was needed: their sizes were chosen to provide suitable values of Vbias2 and Vbias3, ensuring that the cascode pair and the current mirror in the first amplifying stage are always in saturation. Furthermore, these dimensions were chosen also to simplify the layout and improve symmetry of the structure.

Device	Width	Length
M0	6 μm x 2	2 μm
M1	6 μm	2 μm
M2	6 μm x 8	2 μm
M3	6 μm x 6	2 μm
M4	6 μm x 2	2 μm
M5	6 μm x 2	2 μm
M6	10 μm x 12	4 μm
M7	10 μm x 40	4 μm
M8	10 μm x 4	4 μm
M9	20 μm x 2	4 μm

Table 3.5: Summary of sizing choices for the biasing circuit in figure 3.6.

3.1.5 Small signal analysis

The circuit in figure 3.3 can be re-designed in the small-signals equivalent circuit represented in figure 3.7, to perform the small-signals analysis and derive its transfer function. The two resistances R_{o_I} and $R_{o_{II}}$ are, respectively, the output

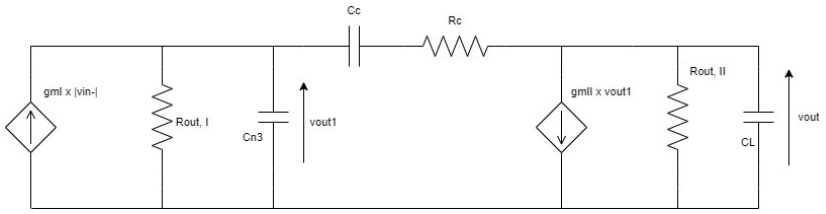

Figure 3.7: Small-signals equivalent circuit of the Error Amplifier

resistance of the first and the second amplifying stage, and can be calculated as follows:

$$R_{o_I} = R_{drain_{M7}} \parallel R_{drain_{M9}} \tag{3.42}$$

where

$$R_{drain_{M7}} = \frac{1}{g_{ds_7}}(1 + \frac{g_{m_7}}{g_{ds_5} + g_{ds_3}}) \tag{3.43}$$

$$R_{drain_{M9}} = \frac{1}{g_{ds_9}}(1 + \frac{g_{m_9}}{g_{ds_{11}}}) \tag{3.44}$$

Using the fact that, in general, for a transistor $g_m \gg g_{ds}$, it is possible to simplify relations 3.44, obtaining:

$$R_{o_I} = \frac{g_{m_7}}{g_{ds_7}(g_{ds_5} + g_{ds_3})} \parallel \frac{g_{m_9}}{g_{ds_9} g_{ds_{11}}} = \frac{g_{m_7} g_{m_9}}{g_{m_7} g_{ds_9} g_{ds_{11}} + g_{m_9} g_{ds_7}(g_{ds_5} + g_{ds_3})} \tag{3.45}$$

Meanwhile, the output resistance of the second stage $R_{o_{II}}$ is simply the parallel between the channel resistances of transistors M12 and M13 of circuit 3.3:

$$R_{o_{II}} = \frac{1}{g_{ds_{12}} +} \parallel \frac{1}{g_{ds_{13}}} = \frac{1}{g_{ds_{12}} + g_{ds_{13}}} \tag{3.46}$$

Now that the two resistances are known, it is possible to go from the time domain circuit to the Laplace domain one, represented in figure 3.8.

Writing the nodal equations (KCL) for circuit in figure 3.8 leads to the following expressions:

$$g_{m_I} V_{in} + \frac{V_{o_I}}{R_{o_I}} + sC_{n3}V_{o_I} + \frac{sC_c(V_{o_I} - V_{out})}{1 + sC_c R_c} = 0 \tag{3.47}$$

$$g_{m_{II}} V_{o_I} + \frac{V_{out}}{R_{o_{II}}} + sC_L V_{out} + \frac{sC_c(V_{out} - V_{o_I})}{1 + sC_c R_c} = 0 \tag{3.48}$$

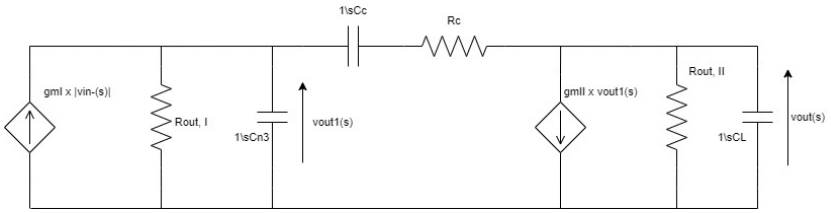

Figure 3.8: Small-signals equivalent circuit of the Error Amplifier in Laplace domain

And solving to find the ratio $\frac{V_{out}(s)}{V_{in}(s)}$, one can write the transfer function $H(s)$:

$$H(s) = A_0 \frac{[1 - sC_c(\frac{1}{g_{m_{II}}} - R_c)]}{1 + as + bs^2 + cs^3} \tag{3.49}$$

where

$$a = (C_L + C_c)R_{o_{II}} + (C_{n3} + C_c)R_{o_I} + g_{m_{II}}R_{o_I}R_{o_{II}}C_c + R_cC_c \tag{3.50}$$

$$b = R_{o_I}R_{o_{II}}(C_{n3}C_L + C_cC_{n3} + C_cC_L) + R_cC_c(R_{o_I}C_{n3} + R_{o_{II}}C_L) \tag{3.51}$$

$$c = R_{o_I}R_{o_{II}}R_cC_cC_{n3}C_L \tag{3.52}$$

If R_c is assumed to be less thanR_{o_I} or$R_{o_{II}}$ and the poles widely spaced, then the roots of the above transfer function can be approximated as [16]:

$$p_1 \simeq -\frac{1}{g_{m_{II}}R_{o_{II}}R_{o_I}C_c}, \tag{3.53}$$

$$p_2 \simeq -\frac{g_{m_{II}}}{C_L}, \tag{3.54}$$

$$p_4 \simeq -\frac{1}{R_cC_{n3}}, \tag{3.55}$$

$$z_1 = \frac{1}{C_c(\frac{1}{g_{m_{II}} - R_c})} \tag{3.56}$$

Where p_1 is the dominant pole, p_2 is the non-dominant pole, with multiplicity equal to two (hence, $p_2 \equiv p_3$), p_4 is again a non dominant pole placed at very high frequencies ($f_{p4} \approx 1GHz$) and z_1 is the zero. The corresponding Bode plots for the magnitude and phase of the transfer function are shown in figure 3.9. These results will be confirmed in section 3.2, where will be presented the outcomes of simulations aimed at extracting the magnitude and phase of the transfer function $H(s)$.

3.2 Simulation results

This section will focus on the simulations carried out to assess the performances of the designed Error Amplifier and the results achieved. The test-bench illus-

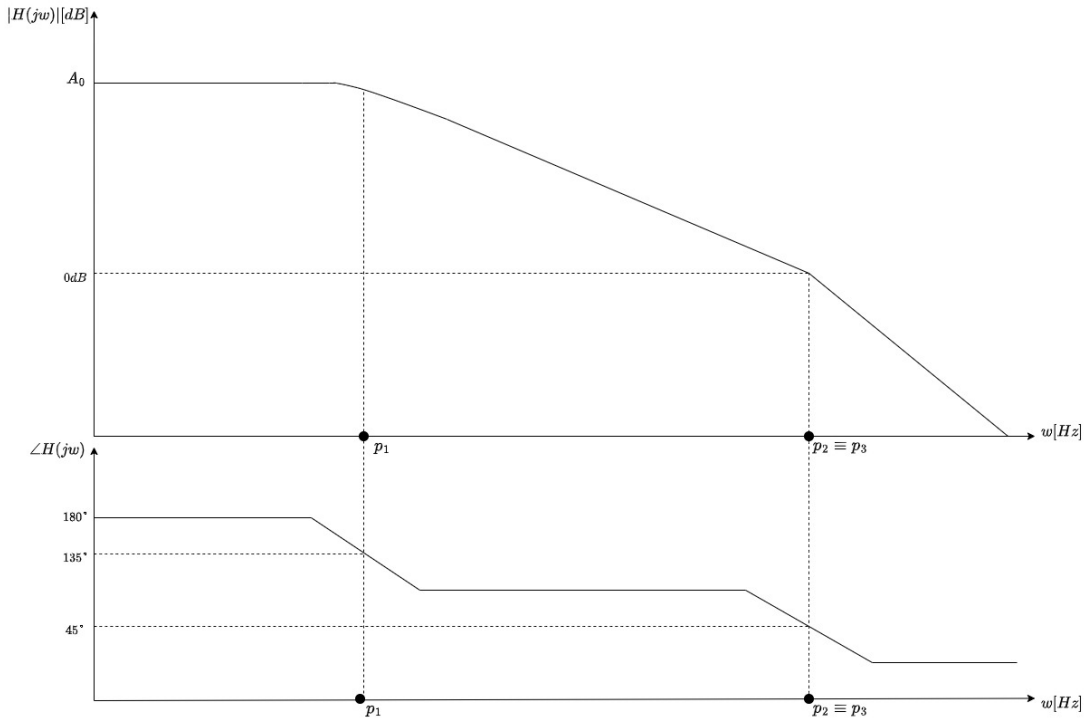

Figure 3.9: Theoretical Bode plots for the loop gain $|H(s)|$ and phase.

trated in figure 3.10 was used to simulate the circuit. The main purpose of these simulations was to determine: the DC operating point throughout a DC analysis, with special attention to the value of the DC input offset $(V_{in}-) - (V_{in}+)$; the phase margin and the gain-bandwidth product, by means of a stability analysis, performed introducing a voltage source in the feedback loop (V_{loop} in figure 3.10); the Power Supply Rejection Ratio (PSRR) of the output and the biasing voltages, obtained with the assistance of AC analysis. The circuit depicted in figure 3.3 was simulated at first only in the nominal corner, to quickly estimate the right direction for sizing, which is characterized by:

- $V_{DD} = 1.8\,\mathrm{V}$,
- Temperature $T = 27\,^{\circ}\mathrm{C}$,
- $V_{loop} = 0\,\mathrm{V}$
- Nominal values for resistors, capacitors and transistors' parameters, as defined in the device catalogue.

Then, once the achieved results in the nominal corner were found to be compliant with target specification, the circuit was simulated in 865 radiation corners that

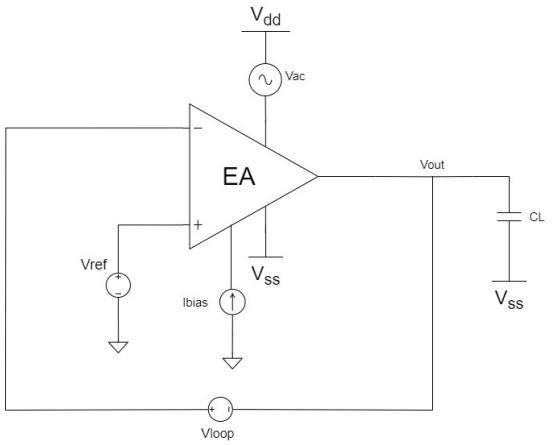

Figure 3.10: Test-bench designed to simulate the Error Amplifier.

will be better described in the dedicated section 3.2.1. Concerning the offset analysis, considering only process variations was not sufficiently accurate. Indeed, the main contribution to the offset comes from the mismatch variations and, for this reason, it requires Monte Carlo simulations to be run in order to be precisely assessed.

3.2.1 Radiation corners

The final implementation of the Error Amplifier was simulated in 865 corners to verify if the design was compliant with process variations of devices, shifts of V_{DD}, V_{loop} and the temperature, different speed conditions of transistors (typical, slow and fast) and, more importantly, the worst case scenario of irradiation. The main conditions simulated in these corners can be summarized in the following points:

- Process variations.

  Each device (transistors, capacitors and resistors) can be affected by modifications of its fundamental parameters due to fabrication; in particular, it is possible to define a range in which these parameters can vary, characterized by high and low extremities. The high and low values for capacitances, resistances and transistors threshold voltages were considered to verify the response of the circuit in the worst case of process variations.

- Temperature variations.

  The behaviour of the circuit was analysed in three different temperature conditions:

  1. $T = 27°C$, the nominal temperature.

2. $T = 100°C$, worst-case scenario for high temperatures that can be reached in HEP experiments at CERN.
3. $T = -30°C$, worst-case scenario for low temperatures that can be reached in HEP experiments at CERN.

- Variations of the power supply voltage V_{DD}.

  The harsh environments of the HEP experiments can affect the power supply voltage V_{DD}, producing a $\pm 10\%$ degradation. Therefore, three values were simulated:

  1. $V_{DD} = 1.8V$
  2. $V_{DD} = 1.98V$
  3. $V_{DD} = 1.62V$

- Transistors working regions in terms of speed.

  The response of a transistor, in general, is strictly influenced by working conditions and fabrication. For this reason, each technology provider usually individuates different worst-case working areas, to help designer assess if the developed circuit can reach target specifications under these unfavorable conditions. The latter regard mainly the speed of devices and are divided into four categories:

  1. Fast corners: both N-type and P-type transistors are assumed to work in the most favourable conditions to reach the highest possible speed.
  2. Slow corners: conversely, these corners simulate the worst-case scenario for speed, hence all the transistors are assumed to be the slowest possibile.
  3. Fast-NMOS and Slow-PMOS.
  4. Fast-PMOS and Slow-NMOS.

- Irradiation conditions.

  As explained in section 1.3, the effect of radiations can downgrade transistors performances and can be expressed in terms of TID. To ensure that the circuit will be reliable under irradiation, it is sufficient to simulate a TID of 200 Mrad.

- Variations of V_{loop}.

  The voltage source V_{loop} in the feedback loop can be used to evaluate the output range of the Error Amplifier: indeed, by sweeping V_{loop} it is possible

to establish both the maximum and minimum output voltages for which the block is still properly working under all the previously described corners and, consequently, this allows also to determine the input range of the Error Amplifier load, i.e. the ramp generator. Simulations proved that the optimal range of operation in terms of output voltage is:

$$V_{loop} \in (-500.0mV, 300.0mV) \tag{3.57}$$

which means that the output range is:

$$V_{out} \in (1.1V, 300.0mV) \tag{3.58}$$

Therefore, three values were simulated:

1. $V_{loop} = 0V$
2. $V_{loop} = -0.5V$
3. $V_{loop} = 0.3V$

Considering all these possible scenarios means simulating the circuit in 865 corners and, for the circuit to be really radiation-hard and compliant with the harsh environment of HEP experiments at CERN, it was strictly necessary that the results achieved in each radiation corner were consistent with target specifications. The following discussion will focus on the results achieved for the most relevant parameters of the designed circuit and the challenges that had to be overcome to pass all the radiation corners.

- **Gain-Bandwidth product and stability analysis.**

  While reaching the required performances was quite easy in the nominal corner, the same can not be said regarding the radiation corners. Indeed, following the theoretical results presented in section 3.1 was not enough to obtain valid results in all radiation corners. Clearly, a downgrade of performances has to be expected when working with such high ionizing doses and extreme temperatures; for this reason, the minimum limit for the GBW was chosen to be 60MHz, which is still sufficiently higher than the estimated maximum switching frequency of the power stage (8 MHz). Nevertheless, even guaranteeing 60 MHz was not trivial. The main issue was to balance the compensation network in such way that it could provide sufficiently high phase margin and GBW even in the worst working conditions. Concerning the GBW, the worst radiation corners were found to be those characterized by:

  1. $V_{DD} = 1.62V$

2. $T = 100°C$
3. Process variations of capacitance and resistance such that the former assumes the highest value and the latter assumes the lowest possible one.

Meanwhile, for the phase margin the most critical conditions were:

1. Process variations of capacitance and resistance such that the former assumes the lowest allowed value and the latter assumes the highest possible one.
2. $TID = 200Mrad$

To overcome these issues, the first strategy was to re-calibrate the compensation network to make it compatible with process variations. Several sweeps of R_c and C_c were performed in the worst corners, leading to the final result:

$$R_c = 10k\Omega \tag{3.59}$$
$$C_c = 300fF \tag{3.60}$$

Furthermore, to ensure that GBW was sufficiently high in all radiation corners, it was necessary to target a GBW higher than 80MHz in the nominal corner and very close to 100MHz. Indeed, in a few radiation corners the GBW can be affected by a downgrade of the 50% with respect to the nominal value. Having a nominal speed of 80MHz leads to a minimum GBW below 40MHz; meanwhile, targeting 100MHz allows to be very close to 60MHz. The final results for radiation corner are summarized in table 3.6.

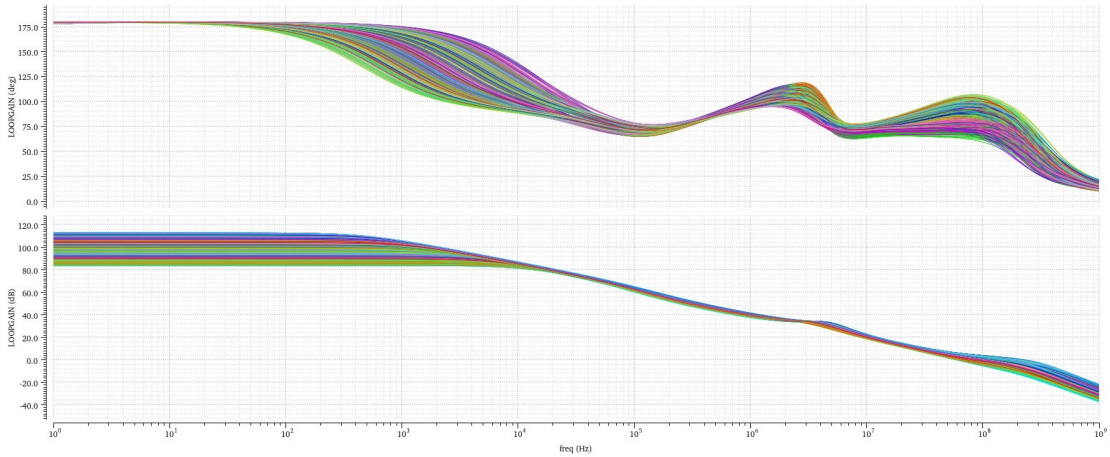

Figure 3.11: Loop-gain and phase plots for the final design.

Output	Specifications	Nominal Corner	Minimum value	Maximum value
GBW	> 60 MHz	97.79 MHz	59.02 MHz	202 MHz
Phase Margin	> 60 °	88.26°	63.64°	97.93°
DC gain	> 80 dB	99.6 dB	83.83 dB	113.2 dB
Input DC offset	range -2mV|+2mV	$-42.3\,\mu V$	$-282.3\,\mu V$	$235.6\,\mu V$

Table 3.6: Radiation corners results for the final design.

In figure 3.11, it is possible to see the plots for the loop gain and the phase of the transfer function of the error amplifier. The presence of the bumps in the phase plot is justified by the non-perfectly compensating pole-zero pair. As a comparison, in figure 3.12 are shown the loop gain and phase for the error amplifier with the compensation network not optimized for radiation corners ($C_c = 500fF$ and $R_c = 1.3k\Omega$). The phase plot results smoother, but the GBW is only 40 MHz in the nominal corner.

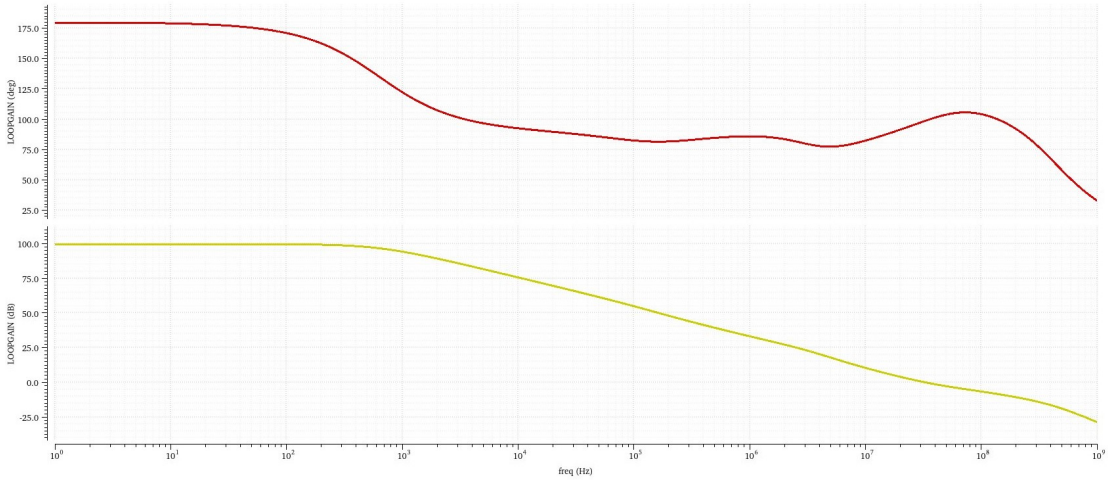

Figure 3.12: Loop gain and phase for the error amplifier using theoretical values for the compensation network.

- **Power Supply Rejection Ratio (PSRR).** The Power Supply Rejection Ratio is a measure of the immunity of the output of the circuit towards power

supply ripples. The Error Amplifier must provide a stable output voltage, independently on disturbances coming from the power rails. This stability is represented by the PSRR, namely the ratio of change in supply voltage to the equivalent output voltage it produces, often expressed in decibel [17]. In figure 3.13, it is shown the outcome of this analysis. The circuit results quite independent from oscillations of the power supply, as the gain of the function $\frac{1}{Vout}$ is very high (around 75 dB on average) for frequencies up to $\approx 100kHz$. As expected, then it starts to drop, due to the presence of parasitic capacitances. To achieve such results, it was necessary to introduce the capacitance C_{bulk} between the bulks of transistors M2 and M3 of circuit 3.3. The reason for this design choice is justified by the impossibility to connect those bulk contacts to net V_{DD}, as it would degrade the PSRR, producing oscillations of the output voltage. In general, for radiation-hardness, all the bulks of PMOS have to be connected to V_{DD}: indeed, it is not possible to simply connect the bulk to the source, as it is usually done in electronics, because if the source is at a low-impedence node any charge accumulated in the substrate of the device, due to irradiation, will circulate easily in the block, altering performances. Meanwhile, having the bulk at V_{DD}, independently on the source connection, allows the circuit to discharge any impact-ionization generated particle through V_{DD}, which is a very high impedence net. However, in the case of the differential pair designed as input stage for the Error Amplifier, the connection bulk-V_{DD} was not feasible, as already explained. When a situation like this verifies, a valid alternative to protect the output voltage from V_{DD} variations, while ensuring radiation-hardness, is to short bulk and source contacts, while introducing a rather big capacitance between the two bulks (shorted as well) and the net V_{SS}, as it was done for the Error Amplifier in 3.3. Considering again plot 3.13, some radiation corners exhibit a gain around 50 dB: these corners coincide all with the worst irradiation condition of 200 Mrad. By increasing the value of capacitor C_{bulk}, it is possible to obtain an higher gain (and a reduction of the peaks height); however, this is detrimental for both the phase margin and the gain-bandwidth product. Hence, a value of 800 fF was chosen for C_{bulk}, obtaining the discussed results.

Not only the output voltage, but also the biasing voltages of the cascode stage have to be immune to power supply disturbances. Hence, the PSRR was evaluated also for the biasing voltages and this explains the presence of the capacitor on net "Pmirror" in figure 3.3 and on nets "Vbias" and "Vbias3" in figure 3.6. The role of these capacitors is to decouple the biasing net from the power supply at very low frequencies, ensuring no oscillations. The frequency response of these voltages should be as close as possible to 0 dB,

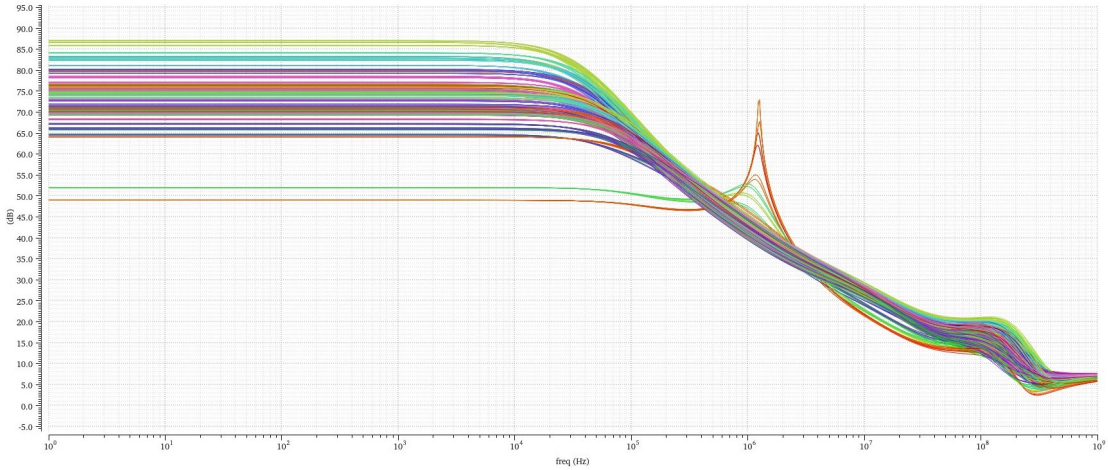

Figure 3.13: PSRR plot for the output voltage.

with eventual peaks below 500 mdB. Particularly difficult was to manage the amplitudes of the peaks exhibited at high frequency for the PSRR of Vbais and Pmirror; for this reason the values of C_1 and $C_{Pmirror}$ are quite high (5 pF and 8 pF, respectively).

3.2.2 Mismatch analysis: Monte Carlo simulations

Monte Carlo simulations were launched to verify circuit performances in the presence of mismatch variations, which are not taken into account simulating only the radiation corners. The first simulations indeed showed an input offset above 2mV in absolute value, which is not compliant with target specifications. The main cause of this offset was found to be the mismatch between the threshold voltages of the differential pair (transistors M2 and M3) and the active load (M4, M5). Further analysis showed that this mismatch can be greatly improved increasing the dimensions of such transistors; the latter statement justifies the choice of W and L for transistors M2, M3, M4 and M5. Finally, optimizing the design of the circuit led to the final result presented in figure 3.14. It is possible to see that the input offset due to mismatch is characterized by a standard deviation of 631.3 µV and ranges between -1.815mV and 1.558mV, meeting target specifications.

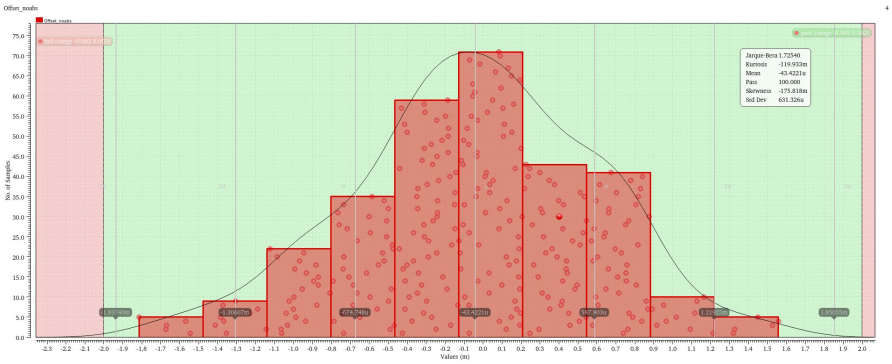

Figure 3.14: Monte Carlo distribution for the input DC offset.

3.3 Layout and parasitic extraction.

The design of the Error Amplifier was concluded with the realization of the layout, from which it was possible to extract all the parasitic resistances and capacitances, necessary to perform post-layout simulations.
The main guideline followed throughout the layout-making process was to ensure symmetry of both the geometry and the current flow. This is why common-centroid structures were preferred with respect to interdigited ones; moreover, transistors in the folded-cascode stage were placed as close as possible, to reduce mismatch and ensure that they would be crossed by the same current.
Once the layout was completed, the circuit was re-simulated, both for radiation corners and mismatch analysis. These simulations were decisive to assess the quality of layout and the effect of parasitic capacitances and resistances on the amplifier. The first post-layout simulations showed immediately the necessity to improve routing, as there was a significant drop in the gain-bandwidth, with a nominal value of 69.34 MHz, and a reduction of the phase margin from 88.26° to 72.73° in the nominal corner. Therefore, in radiation corners neither stability nor speed were preserved, as the GBW was reaching a minimum value of 39.71MHz and the phase margin dropped to 37.68°, requiring some improvements to be made.
To address this issue, the first step was to understand if the worsening of performances was caused by the parasitic capacitances or resistances; therefore, the circuit was simulated three times: once with both parasitic capacitances and resistances, secondly with only parasitic capacitances, and ultimately with only parasitic resistances.
Comparing the obtained results and especially the Bode plots, it could be proven that the main cause of the GBW degradation was the introduction of parasitic capacitances, that lead to a GBW of 69.34 MHz; moreover, from the bode plots it was possible to estimate a non-dominant pole frequency of approximately 180MHz, way lower than the one estimated for the pre-layout bode plots in figure 3.11, which

is around 323MHz (evaluated as the frequency at which the phase margin decreases to 45° and compatible with the assumption made in section 3.1.3, namely $f_{p_{non-dom}} = 3 \cdot GBW$). This result coincides with the one obtained simulating the circuit with both parasitic resistances and capacitance, while a different behaviour is exhibited simulating only the impact of parasitic resistances: the non-dominant pole is still around 290MHz and the nominal GBW is equal to 82MHz. Though even the parasitic resistors have a role in the GBW reduction, the main cause is for sure the parasitic capacitances.
The next step was to understand which node was affecting the most the frequency response. For this purpose, all the nodes with a parasitic capacitance above $10fF$ were considered, and added to the pre-layout schematic (which does not account for parasitic effects, in principle). This strategy allowed to establish that the main contribute to the drop in the GBW was coming from the parasitic capacitance between the two drains of the differential pair transistors (M2 and M3 in circuit 3.3) and between the gate of transistor M13 and net Vss.
These capacitances were affecting the stability as well, even though what had a real impact on the phase margin drop was found to be the presence of parasitic diodes between the n-well of capacitor C_c and the p-contact of the substrate (V_{ss}). The presence of these diodes is inevitable, but their size can be reduced by minimizing the dimensions of the n-well surrounding certain capacitors or transistors in the layout.
Therefore, the layout was optimized in the attempt to reduce both coupling capacitances and dimensions of parasitic diodes, and new routing strategies had to be explored to address these issues. However, once again strategies that proved to be beneficial for the GBW were compromising stability and vice versa. Optimizing both values was challenging and, in the end, it was preferred to ensure good stability, in spite of a 20% loss in the GBW.
Moreover, post-layout simulations were useful to determine the feasibility of the circuit implementation. Indeed, transistors sizes and multiplicities had to be readjusted while realizing the layout, as to ensure a very good symmetry and low mismatch it was preferable to have common-centroid structures, which guarantees that current flows in the same direction through all the connected transistors. A necessary condition to realize common-centroid structures is to have a multiplicity of at least 4; the latter statement explains why most of the multiplicities in tables 3.4 and 3.5 are multiples of four. [18]
The final results, achieved after routing optimization, that led to a great reduction of parasitic capacitances and resistances, are shown in table 3.7.
From these results, it is clear that there is still a loss of performances due to the introduction of parasitic elements compared to pre-layout simulations. Nevertheless, the amplifier remains stable in all the radiation corners, which is the most

Output	Specifications	Nominal Corner	Minimum value	Maximum value
GBW	> 60 MHz	77 MHz	47.22 MHz	135.7 MHz
Phase Margin	> 60 °	76.94°	53.73°	86.68°
DC gain	> 80 dB	99.3 dB	83.29 dB	113 dB
Input DC offset	range -2mV|+2mV	$-41.1\,\mu V$	$-290.3\,\mu V$	$261.7\,\mu V$

Table 3.7: Post-layout simulation results for radiation corners.

important achievement. The GBW is affected by a $\approx 20\%$ reduction, but the circuit remains sufficiently fast for the foreseen purpose. Concluding this discussion, in figure 3.15 it is possible to see the realized layout for the 80MHz error amplifier.

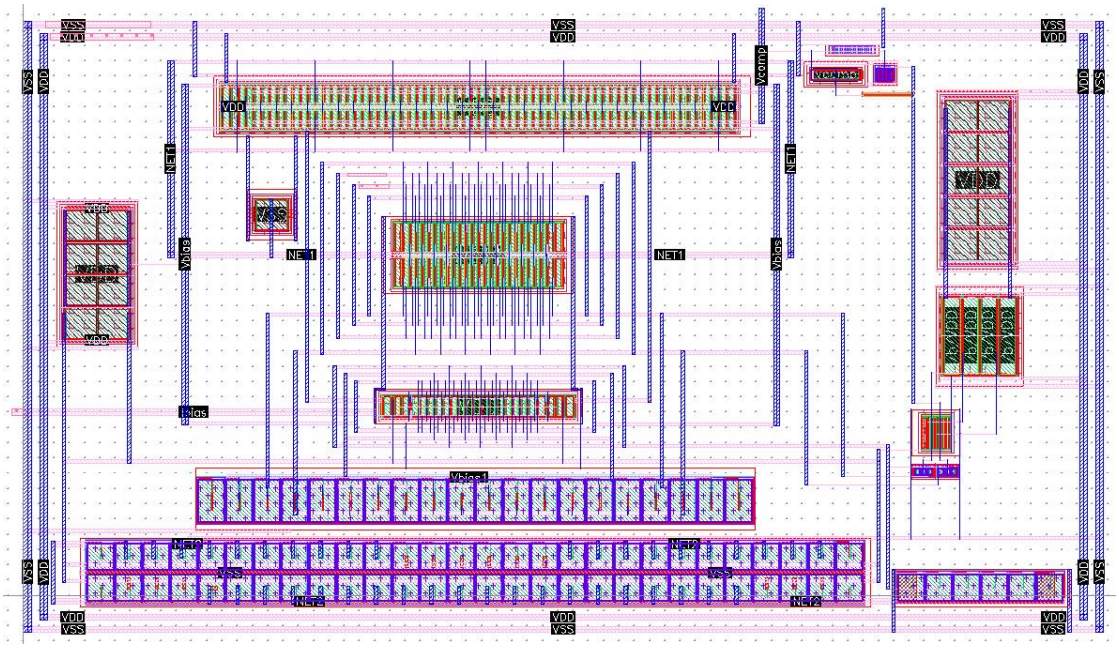

Figure 3.15: Layout of the error amplifier.

3.4 Low-power Error Amplifiers

As already explained in the introduction to this chapter, three Error Amplifiers were designed in the end. This section will focus on the design of the two low-power circuits realized to guarantee an alternative to the high-speed but power consuming block already described. The design methodology adopted, as well as the final schematic chosen to implement these two new devices are exactly the same of the 80 MHz Error Amplifier; therefore only the main results will be presented in this section, together with the eventual small modifications done to the circuit in order to reduce the power consumption.

3.4.1 40 MHz Error Amplifier for low-power consumption

To reach a gain-bandwidth product of 40MHz, while minimizing the power consumption, it was sufficient to change the multiplicity of transistor M12 in schematic 3.3 and of transistor M1 in the biasing circuit 3.6; all the other dimensions were kept the same, except for the compensation resistance that had to be adjusted to the new GBW and transconductances:

- $W_{M12} = 6\mu m \cdot 48$
- $W_{M1} = 6\mu m \cdot 2$

- $R_c = 13k\Omega$

The final results for the radiation corners simulation are represented in table 3.8 and were achieved consuming only 130 µA. Once again, the targeted GBW in the nominal corner was assumed to be higher than 40MHz to compensate for the loss due to process variations in the radiation corners.

Output	Specifications	Nominal Corner	Minimum value	Maximum value
GBW	$>$ 30 MHz	53.12 MHz	33.76 MHz	87.81 MHz
Phase Margin	$>$ 60 °	96.71°	66.5°	110.1°
DC gain	$>$ 80 dB	103.2 dB	83.87 dB	116.8 dB
Input DC offset	range -2mV|+2mV	52.36 µV	−11.35 µV	230.6 µV

Table 3.8: Simulation results for the 40MHz Error Amplifier.

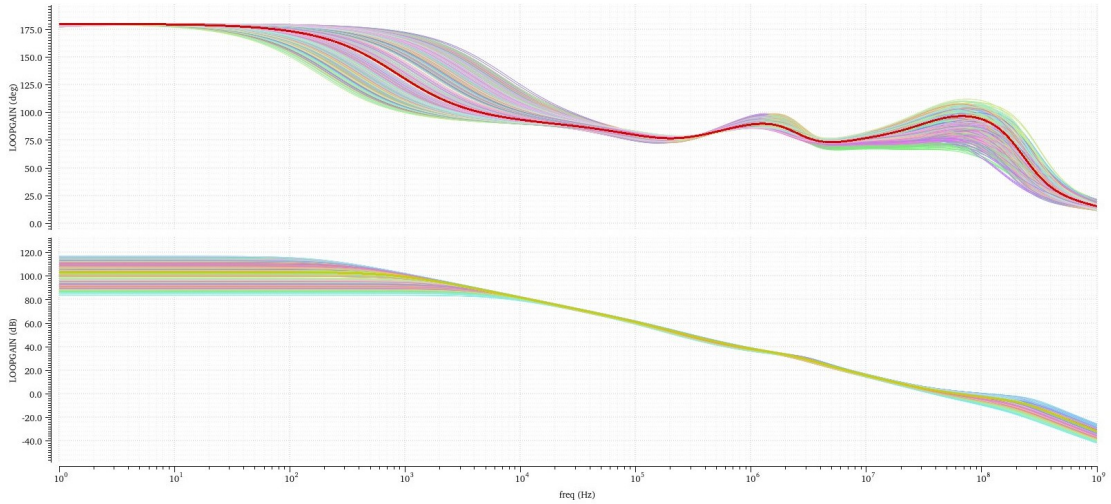

Figure 3.16: Bode plots for the 40MHz error amplifier.

In figure 3.16 are shown the plots for the loop gain and phase of the 40 MHz amplifier in all radiation corner, while in figure 3.17 the PSRR is plotted. The first two curves are quite similar to those obtained for the 80 MHz amplifier: two

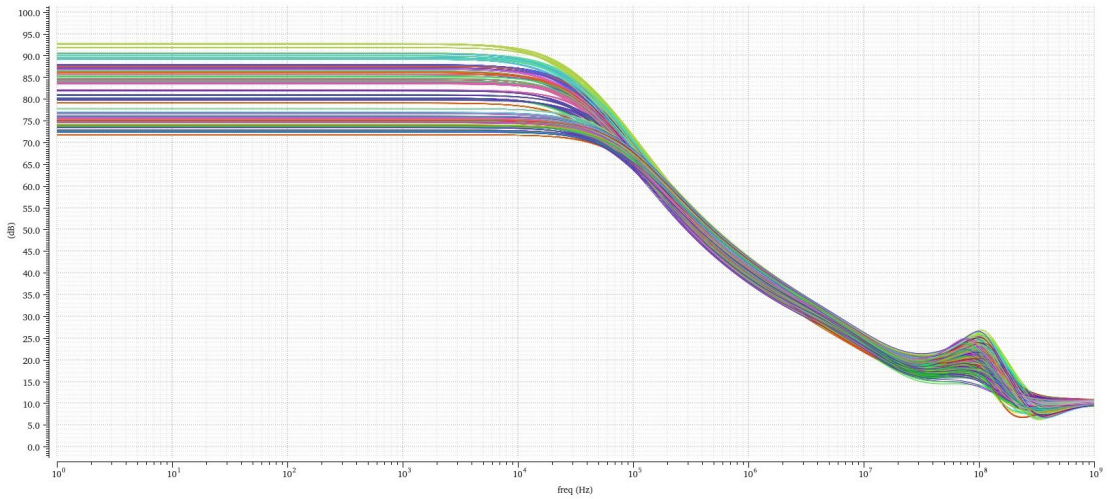

Figure 3.17: Bode plots for the 40MHz error amplifier.

bumps are noticeable from the phase margin (even if the overall plot is smoother than the one in figure 3.11), due to the still non-perfect pole-zero cancellation. The PSRR is, once again, always above 0dB, meaning that the circuit is quite independent from ripples on the power supply voltage, and this time it is possible to see a better response to the corners simulating a TID of 200 Mrad, as none of the curves exhibits a low-frequency gain below 70dB.

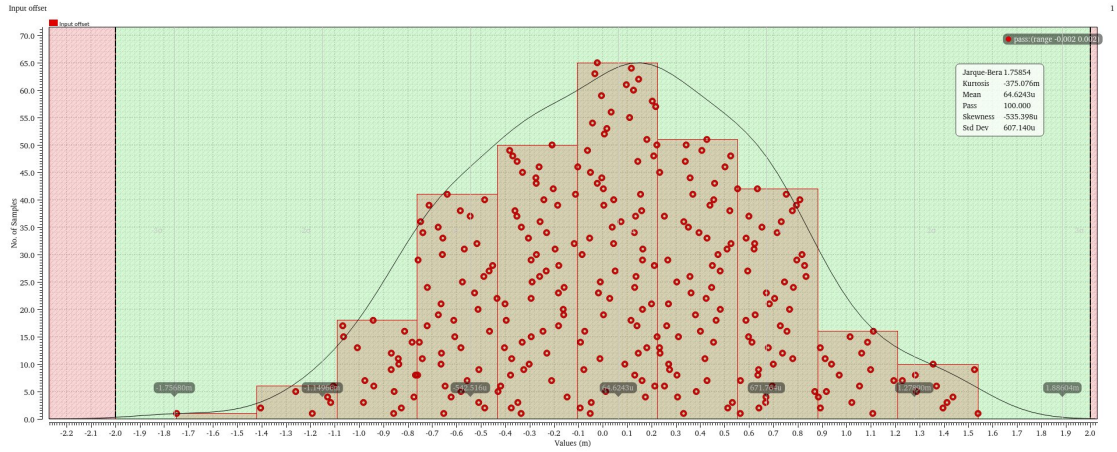

Figure 3.18: Monte Carlo distribution for the input DC offset of the 40 MHz Error Amplifier.

Monte Carlo simulations were also performed, leading to the result shown in figure 3.18. The standard deviation of the input DC offset was found to be 607.1 µV, with a minimum value of -1.75mV and a maximum value of 1.54mV.

3.4.2 20 MHz Error Amplifier for ultra-low power consumption

The third designed amplifier is capable of reaching 20 MHz in the nominal corner with only 58 µA of current consumption. To achieve this result, only a few multiplicities had to be changed with respect to the design described in section 3.1.

	Multiplicity	
Device	80MHz amplifier design	20MHz amplifier design
M1 in circuit 3.6	1	2
M1 in circuit 3.3	32	16
M4, M5 in circuit 3.3	8	4

Table 3.9: Change in transistors multiplicity between the 80MHz amplifier and the 20MHz one.

Applying the modifications reported in table 3.9 reduces the current flowing in each branch, leading to a great reduction in power consumption. Concerning the compensation network, the change in the input transconductance g_{m_I}, due to current and GBW reduction, leads to an optimal value for the resistor R_c of 8.3 kΩ, keeping $C_c = 300fF$.

Output	Specifications	Nominal Corner	Minimum value	Maximum value
GBW	> 15 MHz	24.78 MHz	19.37 MHz	28.43 MHz
Phase Margin	> 60 °	86.51°	66.02°	98.76°
DC gain	> 80 dB	106.1 dB	84.75 dB	119.3 dB
Input DC offset	range -2mV|+2mV	45.69 µV	−0.836 µV	160.8 µV

Table 3.10: Simulation results for the 20MHz Error Amplifier.

The simulation results for radiation corners are summarized in table 3.10, while in figure 3.19 it is possible to see the Bode plots (top graph) and the PSRR for all the radiation corners (bottom plot). Finally, Monte Carlo simulation was performed to assess the influence of mismatch variations on the input offset, leading

to the final distribution depicted in 3.20. The standard deviation for the DC input offset was found to be 694.9 µV, within the range [-1.801mV, 1.754mV].

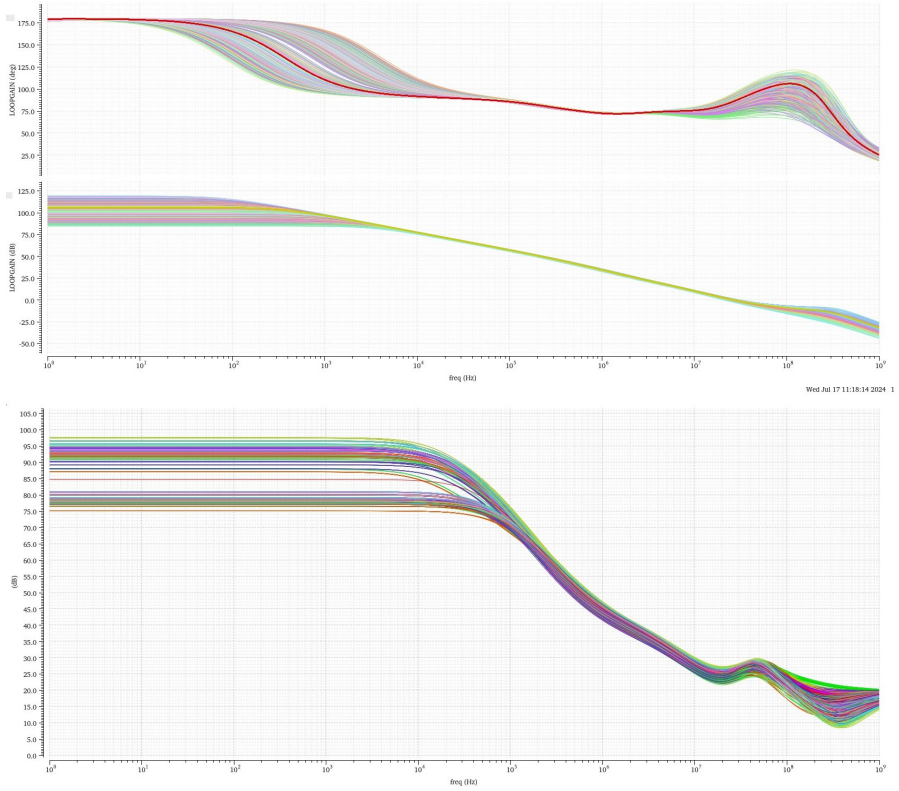

Figure 3.19: Bode plots for the 20MHz error amplifier (top image); PSRR plot for the 20MHz error amplifier. (bottom image)

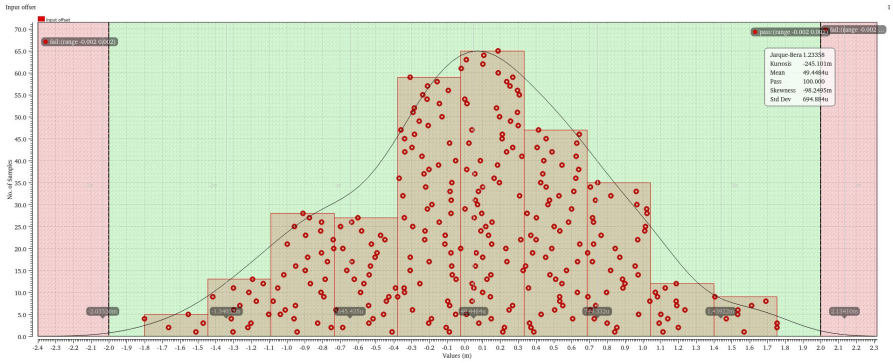

Figure 3.20: Monte Carlo distribution for the input DC offset of the 20 MHz Error Amplifier.

Chapter 4

The delay generator

This chapter will focus on the building blocks of the delay generator, implemented to guarantee that no cross-conduction verifies between the high-side and low-side signals of the power stage. Indeed, considering for simplicity a buck converter, to ensure proper voltage conversion it is necessary to introduce a delay between these two signals, so that there is no overlapping between the activation of the high-side switch and the low-side one. Eventual cross-conduction would be detrimental for the converter operation, as the phase node would not be neither at V_{in}, nor at V_{SS}, affecting the Duty Cycle, which was carefully chosen to guarantee a certain output voltage, as already explained in section 2.1. Therefore, in this chapter will be presented the strategy adopted to ensure no cross-conduction in the power stage, and consequently, a stable output voltage of the DC-DC converter.

4.1 Working principle

The main idea to ensure the proper voltage conversion was to introduce two delays or dead-times between signals gate-HS and gate-LS, which originate, respectively, from the output of the ramp generator, namely PWM, and its complement $\overline{PWM}$:

1. τ_1, the dead-time introduced between the falling edge of the low-side signal, gate-LS, and the rising edge of the high-side one, gate-HS.

2. τ_2, the dead-time between the falling edge of the high-side signal and the rising edge of the low-side one.

In figure 4.1 it is possible to see a scheme of the ideal result that is aimed with the design of the delay generator. In order to introduce these two dead-times, some delay blocks were designed, all based on the repetition of either a 0.5ns or 1.7ns delay cells. These two fundamental cells consist of a chain of logic gates, called

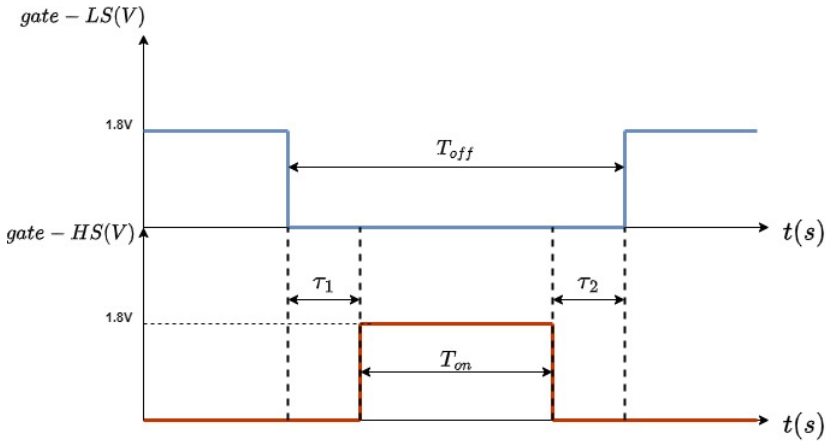

Figure 4.1: Ideal behaviour of the high-side (red pulse) and low-side (blue pulse) signals, after the introduction of dead-times τ_1 and τ_2.

delay line, that introduces the required delay depending on the provided current, which can be either fixed or tuned externally through some resistors. The main element of these delay lines that allows to control the delay by tuning the current is the so called starved inverter, described in the following paragraph.

4.1.1 The starved inverter

The first step towards the realization of the delay chain was the design of its fundamental block, namely the starved inverter, whose circuit implementation is shown in figure 4.2. While transistors M2 and M3 constitute together a standard inverting stage, transistors M4 and M1 have the purpose of either starving or feeding current to the true inverter. Indeed, tuning the two gate voltages V_{biasP} and V_{biasN}, allows to control the charging or discharging current at the output node; in other words, providing more or less current to the inverting stage changes the speed at which the capacitance at the output node, C_{out}, is charged and discharged, hence controlling the delay between the input and the output signals. Concerning the sizing of this block, initially it was decided to size the core inverter to ensure symmetry between rising and falling times. For this reason, transistor M2 was sized using the minimum dimensions allowed by ELT design (see chapter 1), namely $W_{M2} = 2.01\mu m$ and $L_{M2} = 0.18\mu m$; meanwhile, M3 was oversized to compensate for the intrinsic speed gap between pull-up and pull-down times, i.e. $W_{M3} = 6.33\mu m$ and $L_{M3} = 0.18\mu m$. Ultimately, it was decided to reduce the width of M3 to the same of M2, in the attempt of reducing the parasitic capacitance toward the output node. Indeed, it was noticed that with such a wide transistor current modulation from transistors M1 and M4 was not working per-

fectly, probably because of this parasitic capacitance that was injecting/drawing current from the output node. Hence, to ensure a better control of the charging/discharging speed of the output node, the final width of transistor M3 was fixed to $2.01\mu m$. On the other hand, the dimensions of transistors M1 and M4 depend on the final delay that is targeted. In the end, two starved inverters were designed, one optimized for a 0.5ns delay line and the other for a 1.7ns delay line. The final dimensions are presented in table 4.1.

	Starved inverter (0.5ns delay line)		Starved inverter (1.7ns delay line)	
Device	Width	Length	Width	Length
M1	2.6 μm x5	0.5 μm	2.8 μm x3	0.5 μm
M2	2.01 μm	0.18 μm	2.01 μm	0.18 μm
M3	2.01 μm	0.18 μm	2.01 μm	0.18 μm
M4	1.3 μm x5	0.5 μm	1.4 μm x3	0.5 μm

Table 4.1: Final sizes for the two designed starved inverters.

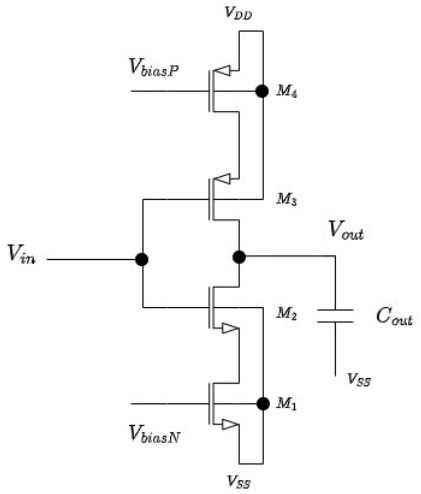

Figure 4.2: Schematic of the starved inverter.

The characteristics of the final designs are shown in figures 4.3 and 4.4, from which it is possible to see the current-starving effect on the inverter characteristic, as both the rising and falling edge are slowed down. Clearly, this effect is more noticeable for the inverter designed for the 1.7ns delay line, whose plot is showed in figure 4.4: since an higher delay is required in this case, the inverter has to be starved more, meaning that less current has to be provided by the biasing circuit. This is reflected in the slower rising and falling edges of the output characteristic in figure 4.4 with respect to the one in figure 4.3. As it is possible to see, starving more the inverted stage means that more time is required to reach either $V_{out} = V_{DD}$ or

$V_{out} = V_{SS}$, hence to fully charge or discharge C_{out}. Furthermore, it is possible to see that the slope of both the rising and falling edge is not constant: for the rising edge, the slope is very high ($8\frac{V}{ns}$) while the input voltage is below 0.9V (meaning that transistor M2 is starting to be turned off), then a plateau phase is reached around 0.9V and finally the signal is slowed down due to current starving, and the value of 1.8V is reached with a slope of $0.316\frac{V}{ns}$. Similarly, the initial slope of the falling edge is very high while the gate of transistor M3 is being charged (therefore, M3 is being turned off), then the output voltage reaches a plateau around 0.9V and, finally, the slope decreases greatly before having $V_{out} = V_{SS}$. The main reason for this asymmetry in the slopes is that turning off either M2 or M3 does not require current, so there is basically no limit in the speed at which the two transistors can be turned off; meanwhile, when the input voltage is such that either M2 or M3 should turn on, there is a limit on the speed at which their gates can be charged (or discharged, for the PMOS) imposed by transistors M1/M4, that regulates the current flowing through the inverter.

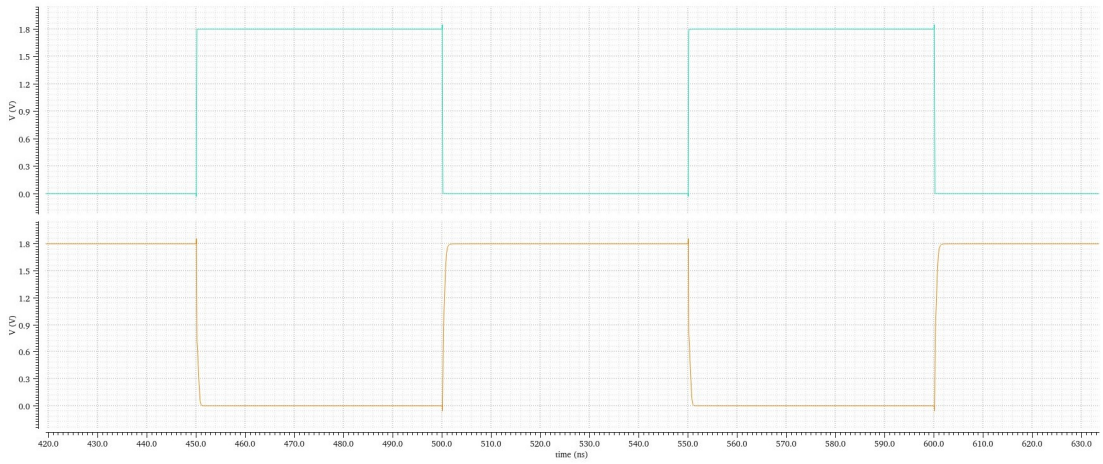

Figure 4.3: Comparison between the input (blue curve) and output (orange curve) voltages of the current-starved inverter designed for the 0.5ns delay line.

4.1.2 The delay line

Variable delay elements are inverter-based circuits used for accurate pulse delay control in high-speed integrated circuits. More precisely, these circuits are realized as chains of inverters and are called delay lines. The latter can be classified as digital or voltage-controlled delay lines: while the first ones are suitable only for coarse delay control, the second ones allow fine delay variation and, therefore, were implemented in this work to realize the fundamental delay blocks for the dead-time management. These analog voltage-controlled delay lines are efficient

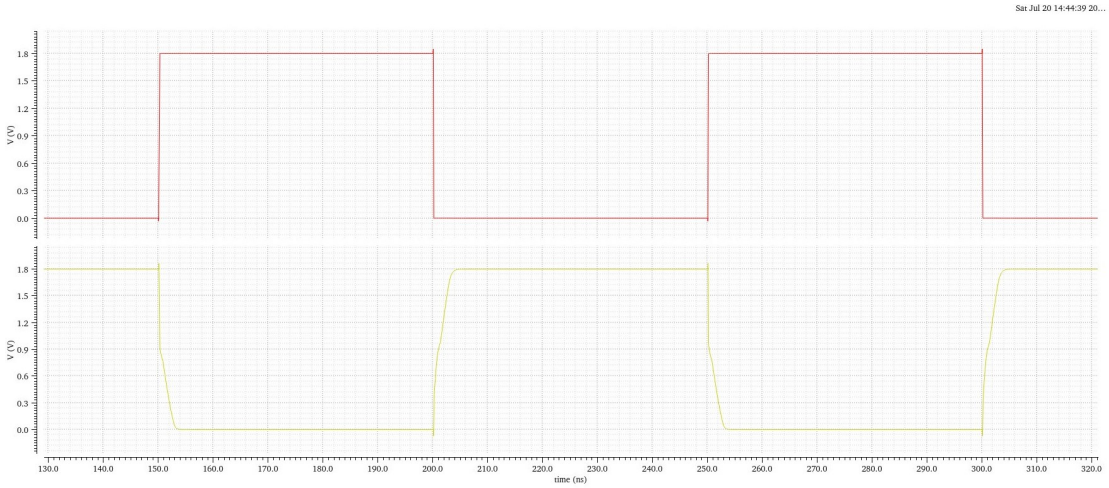

Figure 4.4: Comparison between the input (red curve) and output (yellow curve) voltages of the current-starved inverter designed for the 1.7ns delay line.

in applications where it is necessary to achieve small and precise amount of delay and, usually, are realized using either shunt-capacitor or current-starved inverters, as in the presented case [19]. Exploiting the starved inverters previously described, it was possible to realize two delay lines, that will constitute the fundamental element of the delay blocks presented in section 4.1.3. In figure 4.5 it is possible to see the circuit schematic implemented for both the 0.5ns and the 1.7ns delay chains; it simply consists of alternating buffers and starved inverters. The presence of buffers allows to rectify the output characteristic of the inverters, as it is possible to see from plots 4.6 and 4.7. Furthermore, buffers are used to balance rise and fall times which are not perfectly equal after the inverting stage, due to the previously described sizing choices for the starved inverters. Indeed, from table 4.2, the results for the overall delay of the two designed delay lines are displayed, showing perfect symmetry between the delay evaluated between the rising edges of input and output functions, and between the falling edges.

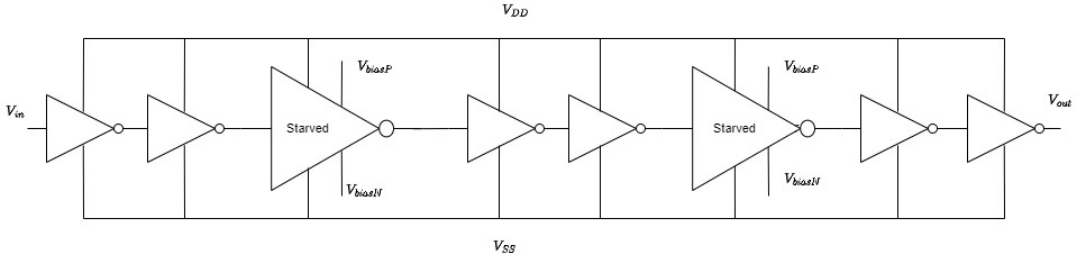

Figure 4.5: Schematic of the implemented delay line.

To assess the current required to produce the target delays, current sweeps were performed. It was found that a current of $10\mu A$ is required to reach a delay

Delay line	Rising edge delay	Falling edge delay
D1	511ps	510.1ps
D2	1.741ns	1.715ns

Table 4.2: Comparison between delays evaluated between both the falling edges and the rising edges of the input and output characteristic for the 0.5ns delay line (D1) and the 1.7ns delay line (D2).

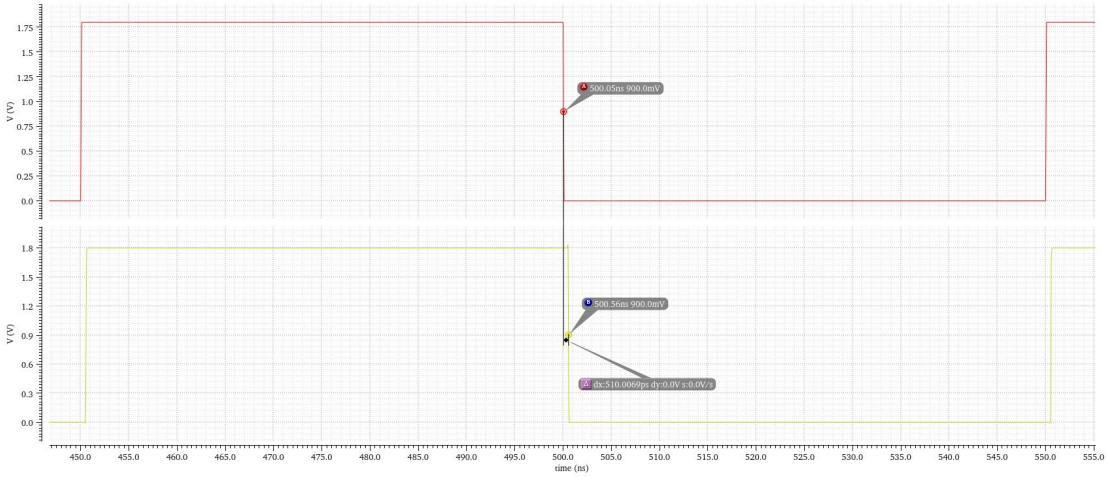

Figure 4.6: Input (red square-wave) and output (yellow square-wave) characteristics of the 0.5ns delay line.

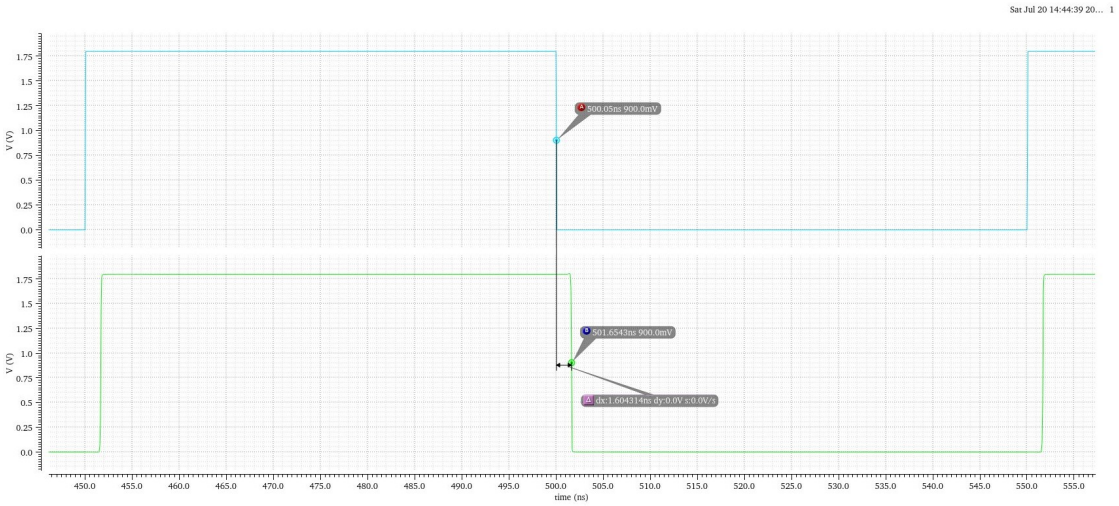

Figure 4.7: Input (blue square-wave) and output (green square-wave) characteristics of the 0.5ns delay line.

of 0.5ns; meanwhile, only $4\mu A$ are needed for a target delay of 1.7ns. The results presented in 4.2 were therefore achieved using these biasing currents.

4.1.3 Final delay blocks

The final implementation of the delay generator required the design of four delay blocks: two with fixed biasing currents and, hence, fixed delays of 3ns and 5ns, and two tunable delay blocks, whose biasing current will be controlled by means of external resistors. The 3ns delay block was realized by simply repeating the 0.5ns delay line and the optimal biasing current was found to be 12 µA; meanwhile, the 5ns delay block consists of three 1.7ns delay lines, with an optimal biasing current of 4 µA. These fixed-delay blocks are implemented within a control-logic, required to ensure that the introduction of dead-times does not cause overlaps between the high-side and low-side signals. Even if not part of this work, the implemented control logic is displayed in figure 4.8. For simplicity, only the logic that controls the high-side signal is reported, as the same circuit is exploited to control the low side one. The working principles is the following: the PWM signal outputted from the PWM generator is firstly delayed through a tunable delay block, producing the signal PWM-delayed-HS, which is the input of the 5ns fixed delay block; the high-side pulse is then generated, as the logic-nand between $\overline{PWM}$-delayed-HS and the input signal delayed of 5ns. Finally, a latch ensures that as long as the low-side signal is high, the high-side pulse will not be outputted. This control is guaranteed by the logic nand between signal $\overline{gate - LS}$, which comes from the control logic for the low-side pulse, and ensures that the output of the delay generator for the high-side, namely gate-HS, is always zero while the output for the low-side is still high and, hence, $\overline{gate - LS}$ is equal to logic zero.

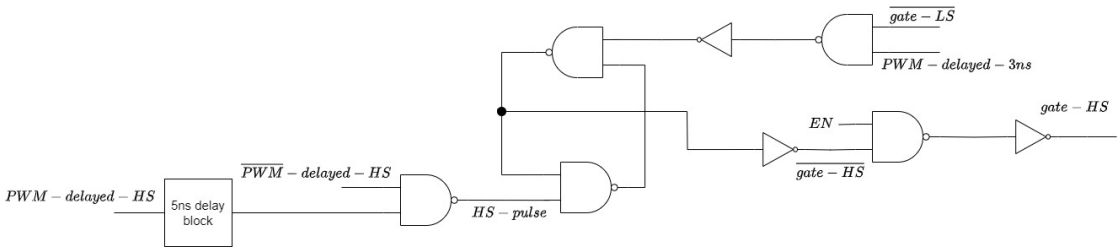

Figure 4.8: Control-logic for the high-side signal.

The other two blocks were designed to introduce the externally controlled delay on the high-side (gate-HS) and low-side (gate-LS) signals. These two blocks are based on the same identical schematic and each one has its own biasing circuit with an external resistor, giving the opportunity to tune differently the delay for the two signals, if required. To guarantee a sufficiently wide variation range for the produced delay, as well as adequate time resolution, it was decided to build these blocks using the 0.5ns delay chain repeated eight times, so that the delay is known for a current of $10\mu A$ and equal to 4ns. The two biasing currents were provided exploiting twice the circuit in figure 4.9. This circuit is based on the

following principle: the voltage follower provides a stable gate voltage for transistor M1, equal to the temperature independent voltage BGR, defined by a band-gap reference. Being the gate voltage fixed, the only way to tune the drain current of M1 is by means of the external resistor R_{ext}; changing its value, the source voltage of M1 varies, causing its drain current to change as well. The modulated current I_{reg} is then mirrored by current mirrors M2-M3 and M4-M5, which provide this current as biasing input for the last mirroring stage, that finally gives the gate voltages V_{biasP} and V_{biasN} for the starved inverters.

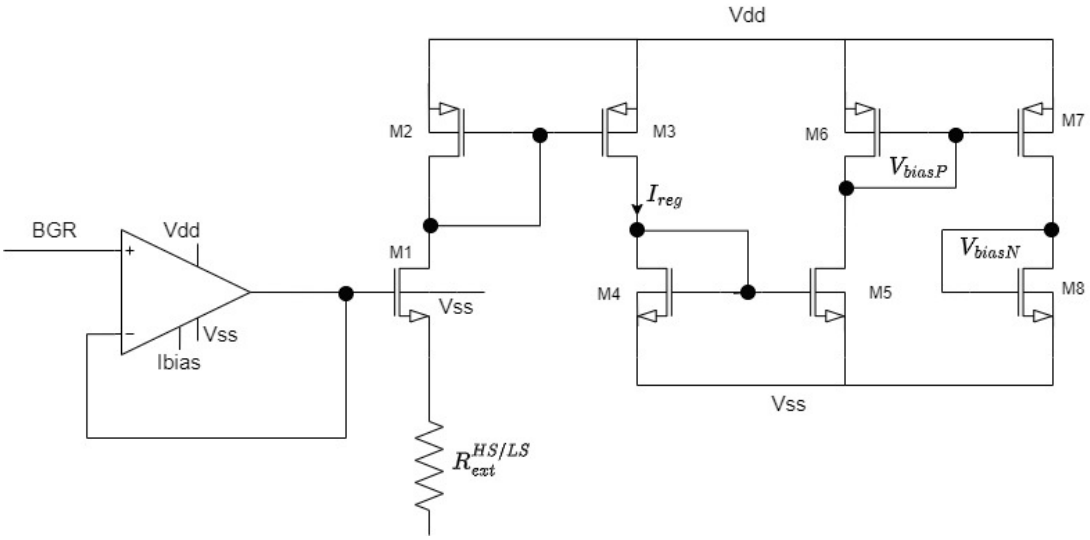

Figure 4.9: Biasing circuit that provides the externally tuned current to the delay blocks for the HS and LS signals.

4.2 Simulation results

The final output of the delay generator is displayed in 4.10, where it is possible to see both its input, the square-wave PWM, and the two outputs (gate-HS and gate-LS), superimposed to highlight the generated dead-times between the high-side signal and the low-side one. In particular, this result was achieved simulating the nominal corner and using two external resistors of $400k\Omega$; in these conditions, the produced dead-times are 14.9ns (between the falling edge of gate-LS and the rising edge of gate-HS) and 14.82ns (between the falling edge of gate-HS and the rising edge of gate-LS). Decreasing the value of the external resistors reduces the voltage drop on resistor R_{ext} in figure 4.9 and, consequently, increases the drain current of transistor M1, being its source voltage lowered. As a result, the delay of the whole block is decreased. As a comparison, in figure 4.11 it is possible to see the same plots, but in the case of two external resistors of $150k\Omega$; in this case, the

produced dead-times are equal to 4.98ns (between the falling edge of gate-LS and the rising edge of gate-HS) and 4.95ns (between the falling edge of gate-HS and the rising edge of gate-LS). The complete circuit for the delay generator was simulated in 288 radiation corners to verify the response under the worst-case scenario for irradiation and transistors' speed; the corresponding results will be presented in section 4.2.1. Furthermore, current sweeps were performed to assess the optimal biasing point for the starved inverters to produce the required delay and these results are displayed in paragraph 4.2.1.

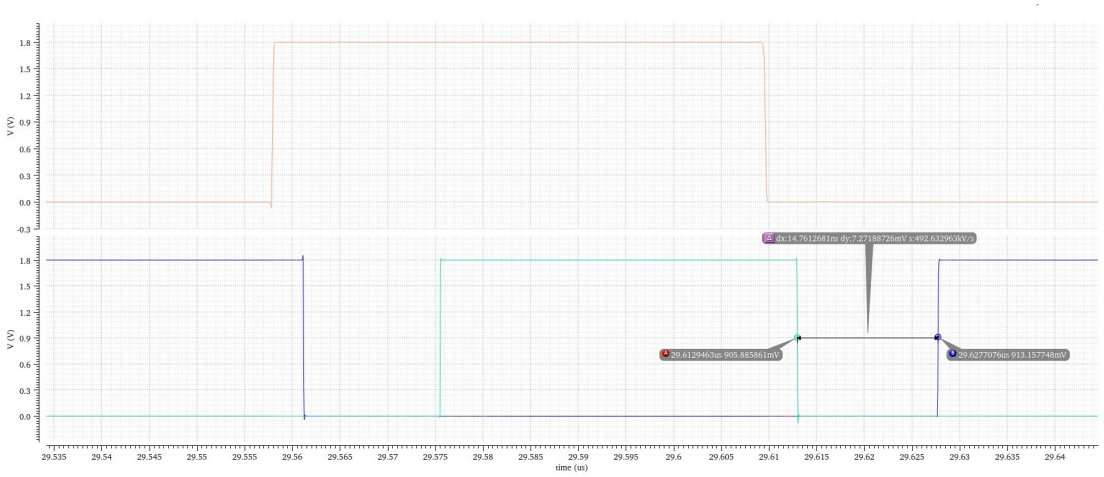

Figure 4.10: Input (PWM, orange curve) and output (gate-HS, light blue curve, and gate-LS, blue curve) signals of the delay generator; the dead-time between the falling edge of gate-HS and the rising edge of gate-LS is highlighted as well. These plots were obtained in the nominal corner.

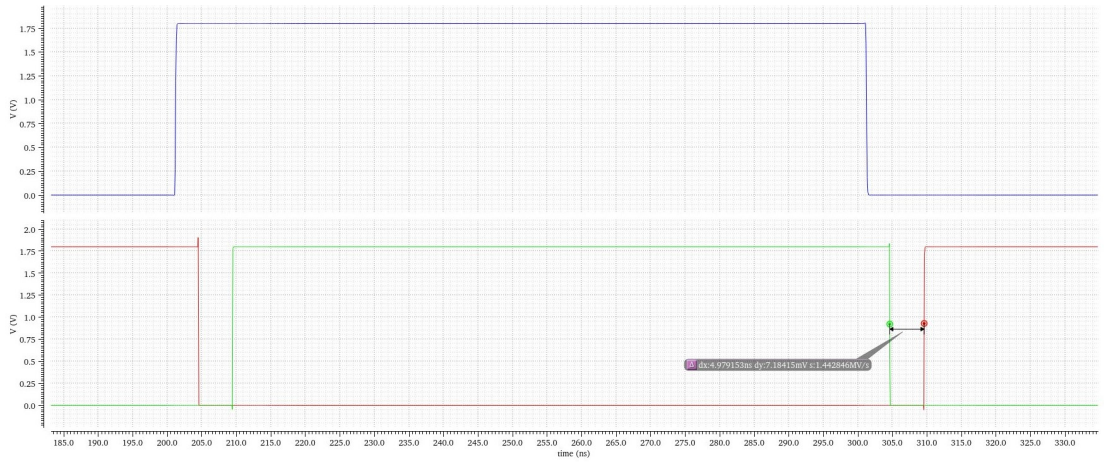

Figure 4.11: Input (PWM, blue curve) and output (gate-HS, green curve, and gate-LS, red curve) signals of the delay generator; the dead-time between the falling edge of gate-HS and the rising edge of gate-LS is highlighted as well. These plots were obtained in the nominal corner.

4.2.1 Radiation corners

Before implementing the final delay generator, all the delay blocks, biased with the optimal current required to achieve the target delay, were simulated in 288 radiation corners, as those one presented in chapter 3. The obtained results are displayed in table 4.3; it is important to underline that the 4ns delay block displayed in this table refers to the tunable delay block that, as explained in section 4.1.3, was initially sized to introduce 4ns delay with a biasing current of 10 µA. Analysing these results, it is clear that, for each block, the delay can increase at most by the 50% of its nominal value in some radiation corners (mainly those characterized by a TID of 200Mrad); meanwhile, the minimum value is just the 25% below the nominal one. This situation is only favorable to the final purpose of the delay generator: indeed, the fact that the delays can be doubled in some radiation corners just guarantees that the final dead-time can be higher than expected, which makes cross-conduction even more unlikely; meanwhile, a reduction of the expected delays could be detrimental in the purpose of avoiding cross-conduction, reason for which it will be important to take into account a 25% degradation when choosing the value of the external resistance that tunes the delay.

	Results for rising edges			Results for falling edges		
Target delay	Nominal value	Min value	Max value	Nominal value	Min value	Max value
0.5ns	505.9ps	378ps	1.058ps	503.1ps	375.9ps	1.015ns
1.7ns	1.741ns	1.357ns	2.863ns	1.706ns	1.322ns	2.808ns
3ns	3.044ns	2.258ns	6.835ns	3.015ns	2.237ns	6.817ns
4ns	4.01ns	3.009ns	8.753ns	4.01ns	3.004ns	8.766ns
5ns	5.052ns	3.899ns	8.279ns	5.047ns	3.893ns	8.271ns

Table 4.3: Simulation results for the fixed-delay blocks of 0.5ns, 1.7ns, 3ns and 5ns measured in all radiation corners; columns named "max value" refer to the maximum delay reached in radiation corners and, similarly, columns titled "min value" refers to the minimum delay found among all the radiation corners.

4.2.2 Current sweeps

In order to assess the optimal biasing point for the fundamental delay lines, current sweeps were performed. In figure 4.12, it is possible to see the resulting plots of the delay as a function of the biasing current, sampled in 100 points between 1 µA and 50 µA. As rising and falling delays are perfectly balanced, the two curves are superimposed for both delay lines. Furthermore, the two plots clearly show the same hyperbolic behaviour of the delay as a function of the biasing current: for

low currents 1 µA, both delays are quite high (2.2ns for delay line D1 and 5.4ns for delay line D2); as the current is increased, the delays decrease quite fast, saturating for very high currents (above 30 µA).

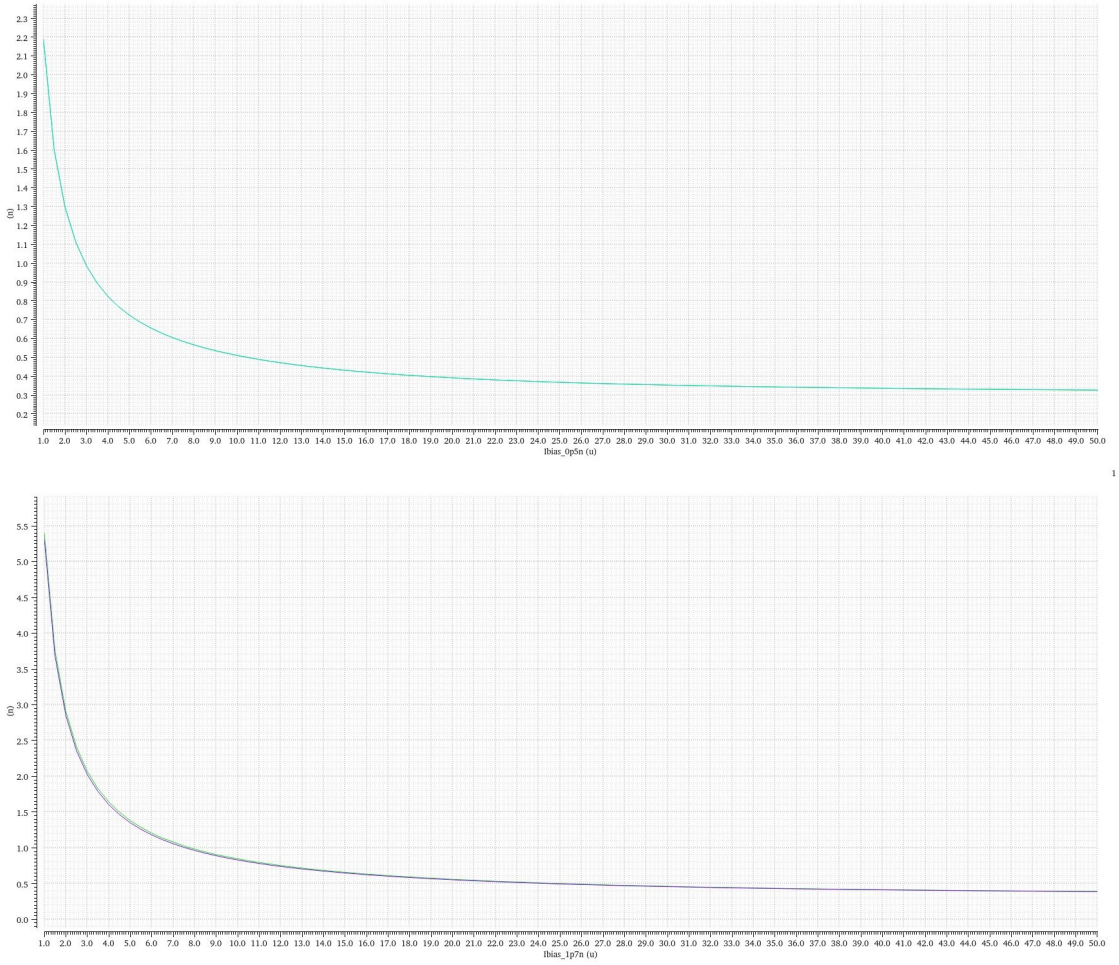

Figure 4.12: Delay vs biasing current for the 0.5ns delay line (figure on top) and for the 1.7ns delay line(bottom figure).

Since the two delay lines were designed to achieve target delays of 0.5ns and 1.7ns, it was necessary to determine the optimal biasing current to reach such delays. From table 4.4, it is possible to analyse some relevant points extracted from the plots in figure 4.12. In particular, this table shows the maximum and minimum delays reached in the performed sweeps, together with the target delays and the currents required to achieve such values. This discussion allows to conclude that to properly bias the designed delay lines, in the attempt of reaching the two targets delay of 0.5ns and 1.7ns, currents of, respectively, 10 µA and 4 µa are needed. Knowing the optimal biasing currents for the fundamental delay block is sufficient to know how to bias the compound delay blocks, as they are just a repetition of delay lines D1 or D2.

Delay line D1		Delay line D2	
Target delay 500ps	Biasing current 10 µA	Target delay 1.7ns	Biasing current 4 µA
Max delay 2.2ns	Biasing current 1 µA	Max delay 5.4 ns	Biasing current 1 µA
Min delay 326ps	Biasing current 50 µA	Min delay 390ps	Biasing current 50 µA

Table 4.4: Optimal biasing current and achieved delays for each designed delay line.

Chapter 5

Level shifters

Level shifters are extensively used electronic circuits, in particular when dealing with different voltage domains and, more specifically, when it is required to go from a lower-voltage domain to an higher one. Indeed, while going from higher voltages to lower ones can be accomplished with a buffer circuit, shifting a signal to a higher voltage is more difficult and requires the implementation of level shifters [20]. In the context of this thesis work, it was necessary to design two level shifters: first, a level shifter allowing to go from the 1.8V voltage domain to the 3.3V one was designed; then, a second one had to be realized to shift the reference of the high-side signal from node V_{SS} to node *Phase*, so that a V_{gs} of at least 3.3V can be always guaranteed to drive the gate of the high-side switch. Indeed, the high-side signal can not be fed as it is to the latter gate, as the source of the high-side transistor is not at V_{SS}, but at node *Phase* that varies between 0V and 20V. Therefore, the main issue is to ensure that at least 3.3V are kept between the gate and the source of the high-side switch, even when the phase node is at $V_{in} = 20V$. To achieve such result, a level shifter was designed able to shift the high-side signal from the 0V-3.3V voltage domain, to the [*Phase*, *Phase* + 3.3V] one.

5.1 1.8V - 3.3V Level shifter

This section will focus on the design of the level shifter allowing the transition from the 1.8V voltage domain, to the 3.3V one. Initially, the discussion will be devoted to present the two different analysed topologies: the first one, described in paragraph 5.1.1, consists of the most standard implementation for a level shifter; the second one, in section , represents a variation with respect to the previous one, that allows to reach better results, both in terms of radiation-hardness and speed of the circuit. For this reason, it was chosen as the final design and its layout was realized, together with post-layout simulations based on parasitic extraction, as

described in the last paragraph of this chapter 5.1.4.

5.1.1 Standard low-voltage level shifter with biasing current

In figure 5.1 it is possible to see the first implementation for the 1.8V-3.3V level shifter. It consists of a differential pair as input stage (transistor M2 and M3), receiving the signal in the 1.8V domain, a pair of cross-coupled transistors in the 3.3V domain (M4, M5) and current mirrors (M10-M11, M7-M8, M12-M13), required in this specific case to differentiate the two reference voltages V_{SS_C} (clean ground) and V_{SS_D} (dirty ground). Indeed, the purpose of shifting the input voltage from 1.8V to 3.3V can be achieved simply with transistors M2-M5, but it is preferable to separate the clean ground, the one corresponding to the digital domain, to the dirty one, which instead corresponds to the higher voltage domain and, for this reason, is more affected by external disturbances. Finally, transistor M1 is part of the biasing circuit that includes transistors M15-M17, and provides the required current to achieve sufficient speed. The working principle is the following: suppose that an input transition is witnessed, such that $V_{in}- = 0V$ and $V_{in}+ = 1.8V$; this means that transistor M2 will be on, pulling its drain to 0V, while transistor M3 will be off. As a consequence, transistor M4 will be ON, being its gate at 0V, and will pull the gate of transistor M3 to 3.3V, turning it off. This means that the left side current mirrors in figure 5.1 will be off, while the right side mirror is on and transistor M8 will pull the output node to 3.3V, ensuring the necessary voltage shift. Similarly, when $V_{in}- = 1.8V$ and $V_{in}+ = 0V$, the left mirror will be on, copying the current from transistor M5 to the diode-connected transistor (M12) that ensures the proper gate voltage for transistor M13, which then pulls the output node to ground. In table 5.1 one can see the chosen sizes for transistors in figure 5.1. The main guideline in sizing these transistors was to ensure enough speed, without consuming too much current, and balance between rising and falling delays of the output signal with respect to the input. For this reason, lengths are all close to the minimum allowed by the exploited technologies and, in particular, for all the NMOS the dimensions were chosen equal to the minimum sizes allowed by ELT design, both in the case of 1.8V (W = 2.01 µm and L = 0.18 µm) and 3.3V (W = 2.3 µm and L = 0.34 µm) devices. It is important to underline that only the input differential pair and the biasing circuit were realized with low-voltage transistors that can withstand only 1.8V; all the other transistors, both N and P type, can withstand gate voltages up to 3.3V.

Device	Width	Length
M1, M15	6 µm	2 µm
M2, M3	2.01 µm	0.18 µm
M4, M5	0.5 µm	0.5 µm
M6, M9, M14	1 µm	0.3 µm
M10, M11, M7, M8	8 µm	0.5 µm
M12, M13	2.3 µm	0.34 µm
M16	3 µm	2 µm
M17	3 µm x 14	2 µm

Table 5.1: Sizing choices for the level shifter in figure 5.1.

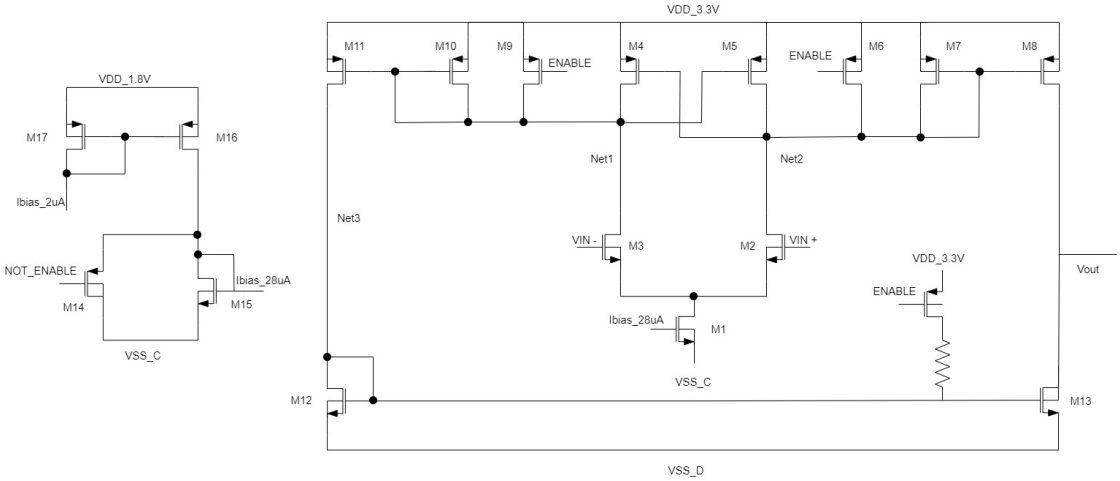

Figure 5.1: Schematic of a standard level shifter with its biasing circuit.

5.1.2 Cross-coupled level shifter with positive feedback and zero static consumption

As it will be shown in the next paragraph, the previously described level shifter is quite slow and power consuming. For this reasons, new solutions to speed up the voltage conversion were sought. This led to design the circuit in figure 5.2, which has no need for biasing, thanks to the introduction of the second pair of cross-coupled transistors (M13 and M14), that allows to shift the voltage at very high speed, while guaranteeing zero static consumption. Instead, in the previous implementation, the presence of the diode connected transistor (M12 in figure 5.1) causes some leakage current even when there is no switching at the input. The working principle is the following: when $V_{in}+$ is at 1.8V and $V_{in}-$ is at 0V, the gate of M4 is pulled to ground, while the gate of transistor M5 will be risen to 3.3V, opening M5. Therefore, the left side current mirrors are off and the right side, instead, is on: this means that the drain of M14 will be risen to 3.3V, having

$V_{out}+ = 3.3V$, and at the mean time, the gate of M13 is at 3.3V, pulling $V_{out}-$ to 0V. Clearly, this circuit has also the advantage of having two outputs, avoiding the use of inverters to create signal $V_{out}-$. In table 5.2 are reported the sizing choices for this level shifter; the same guidelines adopted before were exploited, with the main exception that, this time, it was necessary to oversize even more the differential pair with respect to the cross-coupled transistors (M3, M4). The reason for that is to further boost the drive strength of M1 and M2, while reducing the speed at which the gates of M3 and M4 can be pulled to ground.

Device	Width	Length
M1, M2	2.5 µm x6	0.34 µm
M3, M4	1 µm	0.3 µm
M5, M6	4 µm x6	0.3 µm
M7, M8, M9, M10	4 µm x6	0.3 µm
M11, M12	2.3 µm x4	0.34 µm
M13, M14	2.3 µm	0.34 µm

Table 5.2: Sizing choices for the level shifter in figure 5.1.

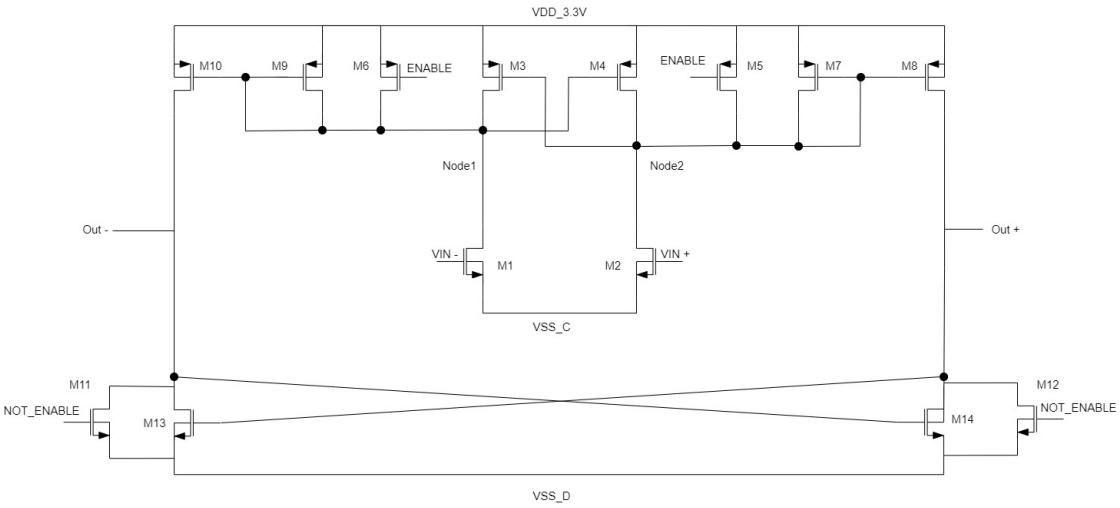

Figure 5.2: Schematic of the Cross-coupled level shifter with positive feedback and zero static consumption.

5.1.3 Simulation results

The final implementation of the level shifter was chosen analysing simulation results in radiation corners, with particular attention to the delay and, above all, circuit response to Single Event Effects (SEE). Indeed, to ensure radiation hardness of both circuits, some critical nodes were tested by injecting and withdrawing

charges corresponding to a Linear Energy Transfer (LET) of 40 $\frac{meV \cdot cm^2}{g}$. This strategy has to verify if charge injection at certain nodes can lead to the creation of a memory element, hence to the verification of Single Event Latch-Up, described in section 1.3. First of all, in figures 5.3 and 5.4, one can see the output of each circuit (for simplicity, only $V_{out}+$ was plotted for the level shifter described in section 5.1.2) evaluated in 865 radiation corners, which take into account a ±10% variation of the core power supply of 1.8V and of the high-voltage domain supply of 3.3V. These plots show that the correct voltage shifting is achieved in every corner and also it is possible to see clearly the distinction between the different values of power supplies; both the input and the output signals are split into three main values, corresponding to 1.62V, 1.8V and 1.98V for the input signal, and 2.97V, 3.3V and 3.63V for the output one. Furthermore, comparing the two outputs, it is evident that the circuit in figure 5.4 has faster rising and falling edges than the first analysed circuit in figure 5.3. To have a more accurate idea of this difference, the delays, on both rising and falling edges, between the input and output signals of the two circuits were evaluated in all the radiation corners, leading to the results summarized in table 5.3. These results highlight the superiority, in terms of speed, of the second circuit, described in section 5.1.2, with respect to the more standard topology presented in figure 5.1, justifying the choice of the former implementation against the latter.

	Standard level shifter			Final level shifter		
Delay	Nominal corner	Max value	Min value	Nominal corner	Max value	Min value
Rising edge	984.6ps	2.06ns	819.4ps	178.7ps	1.085ns	108.5ps
Falling edge	1.047ns	2.151ns	900ps	203.9ps	1.108ns	137.3ps

Table 5.3: Delays between the input and the output signals of circuits in figures 5.1 and 5.2; the displayed results correspond to the maximum and minimum values reached in radiation corners, and the results for the nominal one.

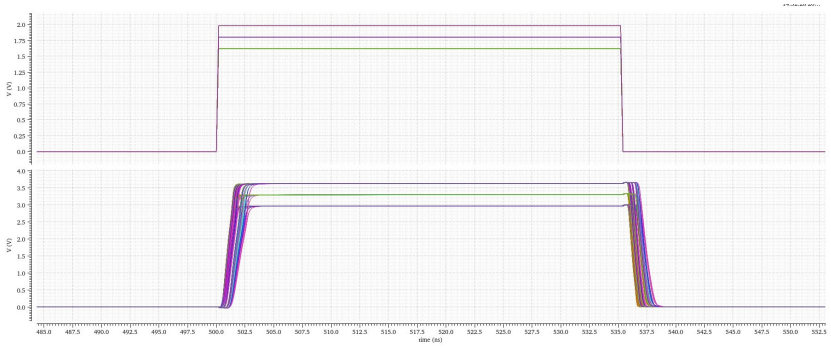

Figure 5.3: Input (waveform on top) and output (waveform below) of the standard level shifter.

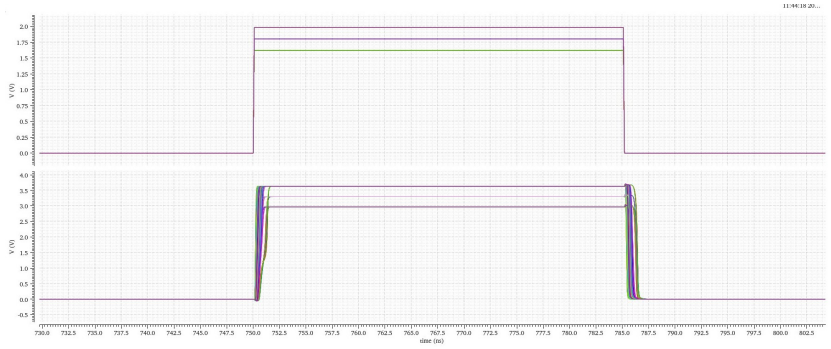

Figure 5.4: Input (waveform on top) and output (waveform below) of the final level shifter.

To complete the analysis and ensure radiation hardness, simulation were performed to assess if, injecting or withdrawing a current equivalent to a LET of 40 $meV \cdot cm^2/g$ in some nodes, the two circuits could behave as a memory. The most critical nodes are Node1, Node2 and the two output nodes in figure 5.2 and Net1, Net2, Net3 and the output node of circuit 5.1. The reason why these nodes had to be checked is that charge injection/withdrawal in those nets could lead to a change in the output voltage, either from high-to-low or low-to-high; if the circuit is not able to quickly restore the correct value, a memory element could be generated, as the output voltage will not change anymore. To simulate a LET of 40 $\frac{meV \cdot cm^2}{g}$, current pulses of 4mA were first injected and then withdrawn in different time intervals, corresponding to different values of the net under analysis: for each net, pulses were injected when the voltage at that node was at V_DD, at zero, at $\frac{V_{DD}}{2}$ on the rising edge and $\frac{V_{DD}}{2}$ on the falling edge. Furthermore, these pulses were generated so that the peak of 4mA would be reached in 50 ps and then it would go back to 0A after 200ps. For the sake of simplicity, here only the plots of the response of the two circuits when injecting and withdrawing charge on the output node will be displayed, as it is the most critical one. From the plots in figures 5.5 and 5.6, it is possible to see that the effect of these currents causes the output node

to switch from low-to-high when current is withdrawn, and from high-to-low when current is injected. This results in the presence of unexpected peaks in the two output functions. Despite the presence of these peaks, no real memory element is generated, as the output waveform goes back to the correct value quite easily. However, the time required to recover the right output voltage is quite different for the two circuits; indeed, the pulses evinced in the output characteristics of the standard implementation have a duration of 1.08ns, meanwhile the second depicted circuit is able to recover the original value in less than 250ps. The reason for this difference can be attributed to the absence of a biasing voltage in the final level shifter in figure 5.2, that will not limit the speed at which the circuit can get rid of the excess charge or re-gain the necessary charge. Concluding, not only the final implementation is intrinsically faster than the standard one, but it is also more robust against radiation effects.

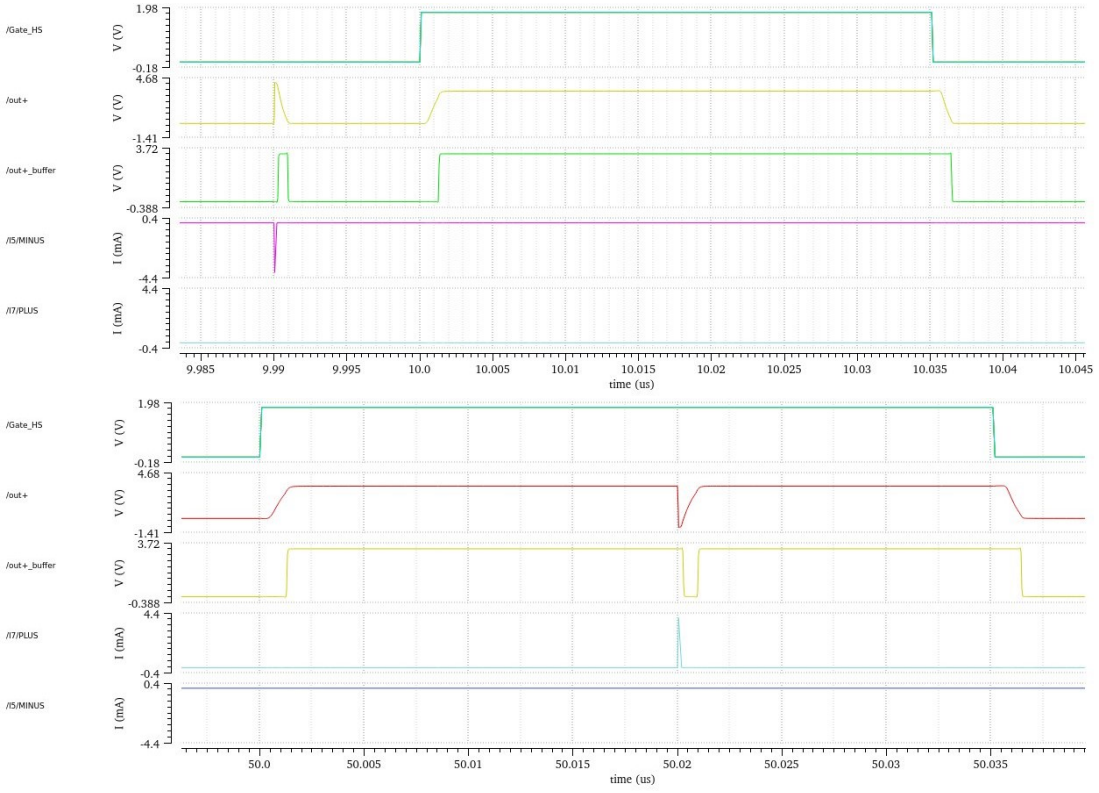

Figure 5.5: Response of the standard level shifter to the withdrawal (figure on top) and injection (figure on the bottom) of 4mA (LET = 40 $meV \cdot cm^2/g$) from the output node.

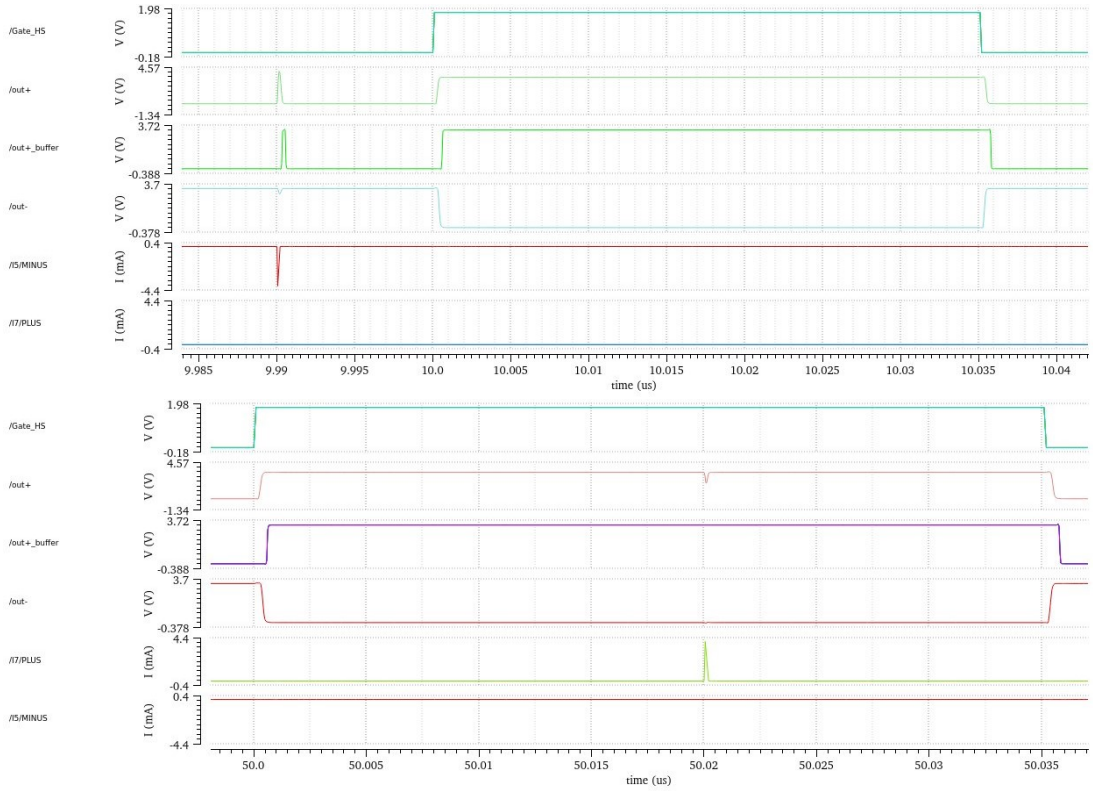

Figure 5.6: Response of the final level shifter to the withdrawal (figure on top) and injection (figure on the bottom) of 4mA (LET = 40 $^{meV \cdot cm^2}/_{g}$) from the output node.

5.1.4 Layout and parasitic extraction

The circuit depicted in figure 5.2 was chosen as the final implementation for the 1.8V-3.3V level shifter and, therefore, its layout was carried out and it is shown in figure 5.7.

Once the layout was concluded, its feasibility was verified performing parasitic extraction and post-layout simulations. The main purpose of this last simulation was to assess how the introduction of parasitic resistances and capacitances would affect the performances of the circuit in terms of speed and, in particular, if it would still correctly shift the input voltage in every radiation corner.

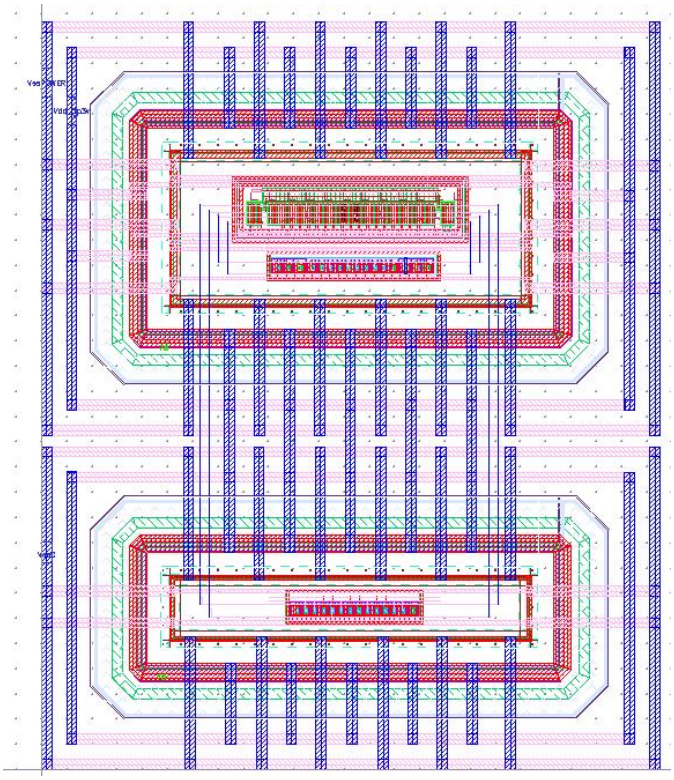

Figure 5.7: Layout of the 1.8V-3.3V level shifter.

As it is possible to see from table 5.4 and image 5.8, both analysis led to positive results. Indeed, the output voltage has the correct behaviour in every radiation corner and the delay is only affected by an increase of the 20% with respect to the values obtained in pre-layout simulations.

Delay	Nominal Corner	Max value	Min value
Rising	226.2ps	1.491ns	138.7ps
Falling	335.5ps	1.631ns	231.2ps

Table 5.4: Summary of radiation corners simulation for the final level shifter after parasitic extraction.

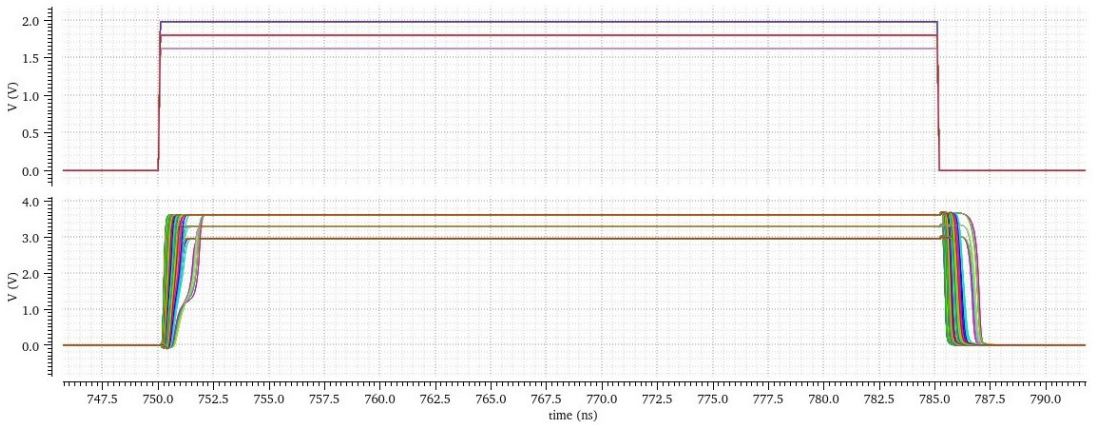

Figure 5.8: Input (waveform on top) and output (bottom waveform) for the final level shifter; results are obtained post parasitic extraction and for each radiation corner.

5.2 High-Voltage Level Shifter

In chapter 2, the general scheme for the control circuit of a DC-DC converter was presented and depicted in figure 2.4. From this picture, it is possible to see that the driving signal for the high-side switch goes through the high-voltage level shifter (or Bootstrap circuit), before being fed to the power stage. As already explained in the introduction of this chapter, this is necessary to shift the high-side signal from the [0V, 3.3V] domain to the [*Phase*, *Phase* + 3.3V] one. Indeed, assuming to have a simple buck converter in the power stage, as the one described in 2.1, then to drive properly the top switch, it is necessary to provide a V_{gs} that can be at least 3.3V above the potential of the source of such transistor. However, this task is not easy, as this source is at the node "*Phase*", which floats between 0V and 20V, depending on whether the switch is "on" or "off". For this reason, the high-voltage level shifter or bootstrap circuit, described in this section, will be introduced. After discussing different possible implementation, the final designed bootstrap circuit, whose general scheme is depicted in figure 5.9, consists of two main blocks: an RC divider and a comparator. In the context of this thesis work, only the RC divider was treated and will be presented in the next paragraph.

5.2.1 Design of the RC divider

In general, an RC divider or RC filter is an electrical circuit that divides the voltage between two points in a circuit using a resistor (R) and a capacitor (C). It's a fundamental circuit used in analog electronics, particularly in signal processing for tasks such as filtering, timing, and shaping waveform. In this thesis work, to design the high-voltage level shifter an analog block made of four RC filters was realized

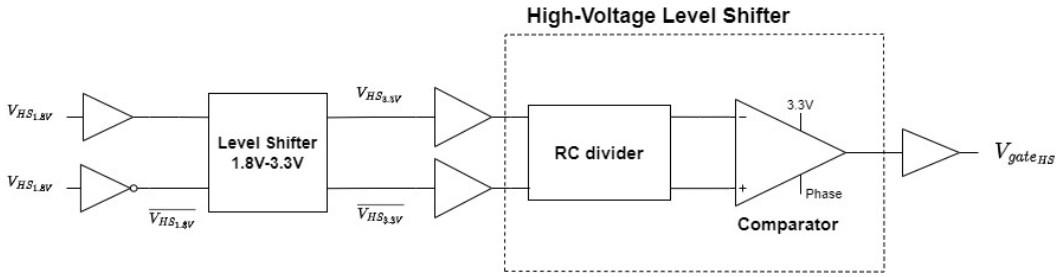

Figure 5.9: Circuit implementation to shift the reference voltage of the high-side signal for the power stage from V_{SS} to *Phase*.

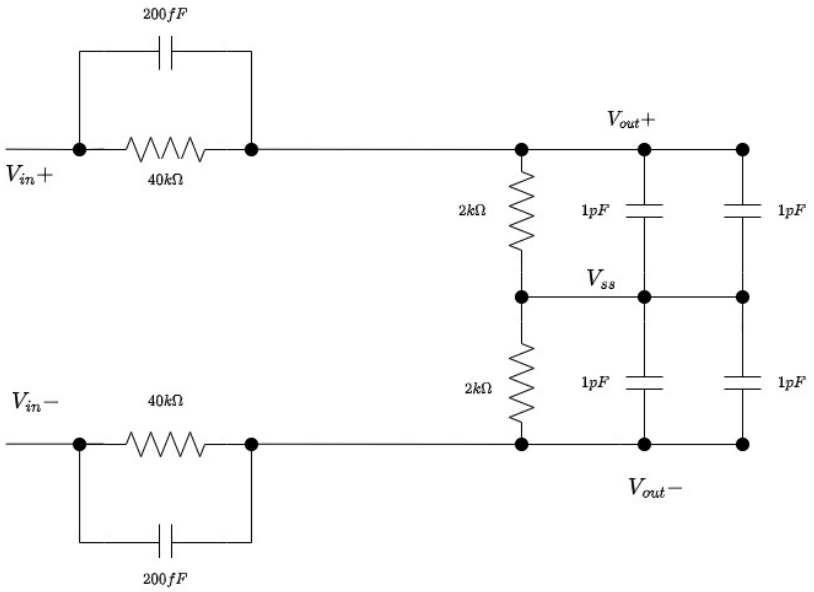

Figure 5.10: Schematic of the RC-divider designed for the High-Voltage level shifter.

and, from now on, improperly called "RC divider". The final implementation of this circuit can be seen in figure 5.10. The purpose of this RC divider is to shift the two input voltages from 3.3V to the voltage domain $[Phase, Phase+\delta V]$, where δV is a small value of voltage above *Phase* that depends on the sizing of resistors in the RC divider. Indeed, in figure 5.10, it is displayed the Vss node of such circuit, which is actually the *Phase* node plus a fixed voltage of 2V: $V_{SS} = Phase+2V$. By properly tuning the value of resistors, one can decide how greater than the *Phase* node can the two output voltages be. The working principle of this circuit is the following: the input voltage $V_{in}+$ is synchronized with the *Phase* node, so it goes at 3.3V when the *Phase* node reaches 20V; in these conditions, $V_{in}-$ is at zero and the two output voltages are simply:

$$V_{out}+ = (22V - 3.3V) \cdot \frac{40k\Omega}{40k\Omega + 2k\Omega} \tag{5.1}$$

$$V_{out}- = 22V \cdot \frac{40k\Omega}{40k\Omega + 2k\Omega} \tag{5.2}$$

It is clear that to have the two output voltages above 20V, the two resistances must be unbalanced, reason for which it was chosen to have the resistances on the left in figure 5.10 equal to $40k\Omega$ and those on the right equal to $2k\Omega$. Similar reasoning can be made when the *Phase* node is low.
In order to size all the resistors and capacitors in the schematic depicted in 5.10, some guidelines were followed, fundamental to ensure the functioning of the comparator, placed at the output of the RC divider. First of all, the comparator has a differential input, meaning that its voltage gain at the output is proportional to the difference $V_{out+} - V_{out-}$. To ensure proper behavior of the comparator, this difference should always be the highest possible, while keeping the difference between each output of the RC circuit and Vss (equal to the *Phase* node) always above the threshold voltage of the input transistors of the comparator, equal to 800mV; if this condition is not met, the two input transistors can not turn on and the comparator will not work. Once the values of the resistors were fixed, the values of the capacitors had to be chosen. In this case, the main idea was to find a suitable time constant for each pair of RC filters. Figure 5.11 displays the outcome of the whole bootstrap circuit simulated in the nominal corner. The red curve represents the difference $V_{out+} - V_{out-}$ between the two outputs of the level shifter, which exhibits transient peaks of |575|mV, and steady-state values of $\pm 82mV$. These results confirmed that the chosen dimensions for every RC pair were optimal to guarantee fast triggering of the output comparator; this statement is further confirmed analysing the two differences $V_{out+} - Phase$ and $V_{out-} - Phase$ (respectively, the yellow and green curves in figure 5.11). These two voltages, which coincides with the V_{gs} of the input transistors in the comparator, are always positive and can rapidly reach values beyond 800mV, ensuring fast turning-on of the comparator. Finally, the blue curve in figure 5.11 represents the output of the comparator (referred to the *Phase* signal) and it is clear that there is a good synchronization between the RC circuit and the comparator: as soon as the differences between the RC circuit's outputs and the *Phase* node reach suitable values, the comparator is triggered, rising the output to 3.3V above the *Phase* node or lowering it at 0V with respect to *Phase*. This means that for what concerns the nominal corner, the circuit is capable of providing the required driving voltage for the high-side switch in the power stage, as the designed bootstrap circuit is able to generate an output voltage that varies between $[Phase, Phase + 3.3V]$.

To achieve these final results, the values of the capacitors were chosen to balance the two time constants of the left and right RC filters. Having the right resistances higher the left ones, clearly the capacitances on the right needed to be smaller than

the left ones. In this way the two time constants have the same order of magnitude:

$$\tau_{left} = R_{left} \cdot C_{left} = 8 \cdot 10^{-9} s \tag{5.3}$$

$$\tau_{rigth} = R_{rigth} \cdot C_{right} = 2 \cdot 10^{-9} s \tag{5.4}$$

In the end, it was chosen to have $\tau_{left} = 4 \cdot \tau_{rigth}$ to generate the peaks of $|574\text{mV}|$ in the plot of $V_{out+} - V_{out-}$, that can be seen in figure 5.11. Indeed, having two perfectly equal time constants was not very efficient in terms of speed: the difference $V_{out+} - V_{out-}$ would reach at most $|100\text{mV}|$ in this conditions, causing the comparator to be very slow. Therefore, the final choice was to have slightly different time constants, to speed up the response of the comparator.

Accordingly to the procedure already depicted in the other chapters, once the achieved results in the nominal corner (typical process conditions, with a temperature of $27°C$ and nominal values for the supply) were satisfying, simulations in several different corners were launched to evaluate the circuit behavior under irradiation condition, process, temperature and power supply variations. The results of such simulations will be depicted in the next paragraph.

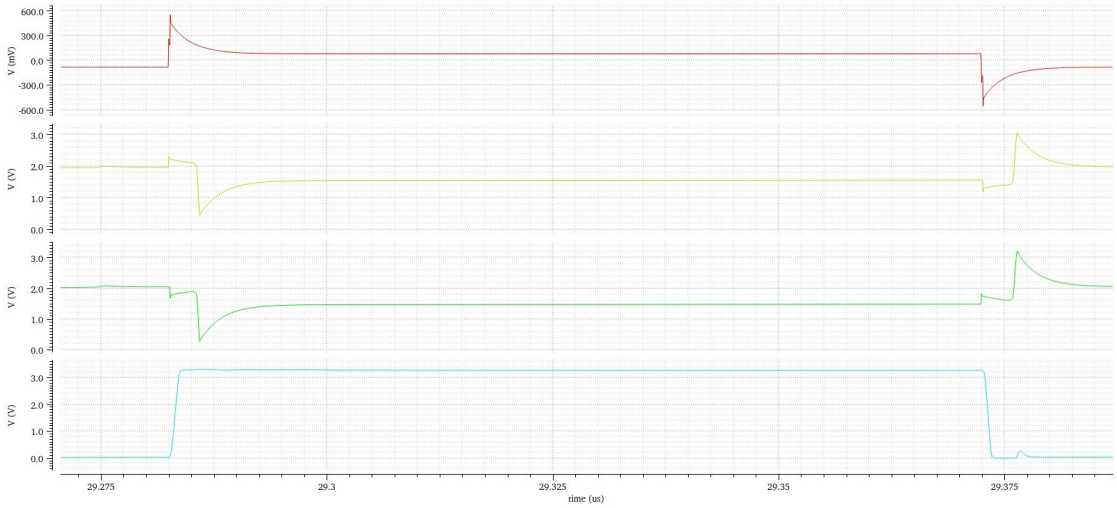

Figure 5.11: Output characteristic in the nominal corner for the circuit in figure 5.10. The red curve represents the difference $V_{out+} - V_{out-}$; the yellow and green waves are, respectively, $V_{out+} - Phase$ and $V_{out-} - Phase$; finally, the blue curve represents the output of the whole bootstrap circuit referred to *Phase*, hence the difference between output of the comparator and the *Phase* node.

5.2.2 Simulation results

The final design was simulated in the radiation corners described in chapter 3 to verify radiation-hardness and ensure that the proper circuit response is achieved under high-levels of irradiation (up to 200MRad) and extreme temperatures (-30°C and 100°C). Analysing the top plot in figure 5.12, it is possible to conclude that the RC circuit for the Bootstrap block correctly works in each radiation corner, as the difference $V_{out+} - V_{out-}$ maintains the proper shape in all the simulated points, with transient peaks ranging between |389|mV and |755|mV. More importantly, the difference between the two outputs of the block under analysis and the *Phase* node is always positive, guaranteeing fast turning-on of the output comparator regardless of process, temperature and power supply variations and irradiation conditions. Finally, the bottom plot in figure 5.12 displays the output of the overall high-voltage level shifter evaluated in each radiation corner; more precisely, this plot represents the difference between the comparator output and the voltage of the *Phase* node. Analysing these curves, it is clear that the level shifter correctly works in all radiation corners, as the output voltage, minus the *Phase* one, varies between 0V and 3.3V (accepting a ±10% variation of $V_{DD} = 3.3V$). Concluding, the RC circuit previously depicted allows to shift and control the voltage necessary to drive the comparator, whose output finally gives the driving signal for the high-side switch in the power stage.

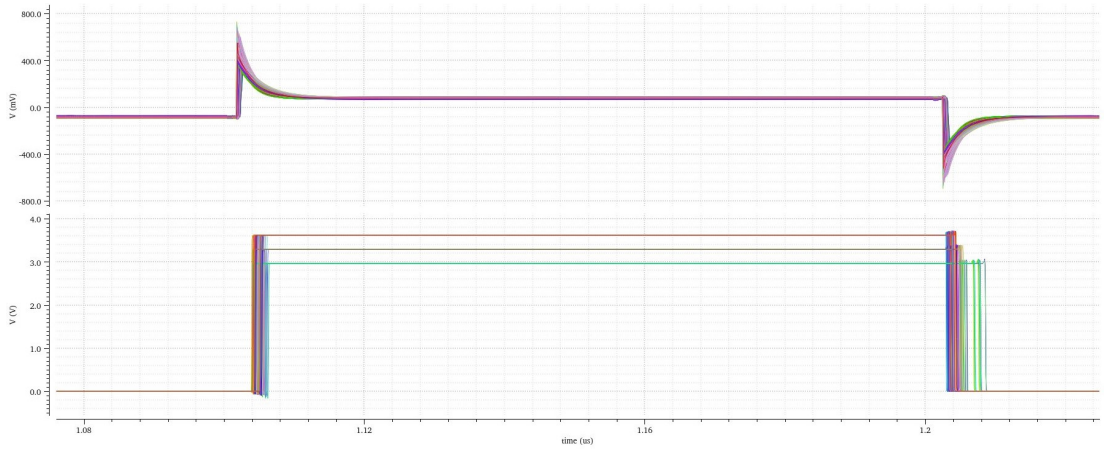

Figure 5.12: Top plot represents the difference between the two outputs of the RC divider evaluated in all radiation corners. The bottom waveform coincides with the output of the comparator, referred to the *Phase* node for all the simulated corners.

5.2.3 Layout and post-PEX simulations

The achieved results depicted in the previous paragraph allowed to pursue the realization of the layout for the RC divider of the Bootstrap circuit. This procedure required the introduction of some modifications to the circuit depicted in figure 5.10, in particular in terms of multiplicity of the exploited capacitors and resistors. The overall values were not modified but each single element was replaced by multiple parallel components with a nominal value close to the one indicated in the device catalog to reach minimal mismatch, with the proper multiplicity to always have the final resistance and capacitance presented in section 5.2.1. Indeed, it was proven that the device was extremely sensible to unbalances between the resistance of the upper and lower branches, as well as the capacitance: the correct behavior of the block is strictly linked to the perfect symmetry between upper and lower values of both resistance and capacitance, so that the time constants of the two branches are always the same. If this symmetry was not preserved in some time intervals the difference $V_{out+} - V_{out-}$ could reach values dangerously close to 0V, causing the comparator to not work properly. Therefore, strategies were sought to improve the mismatch, leading to the final choice of dividing each component in many sub-components of lower nominal capacitance/resistance, with a proper multiplicity to maintain the overall values equal to those displayed in figure 5.10. The final layout is shown in figure 5.13, were it is possible to see that each component is actually made of the repetition of several capacitors/resistors.

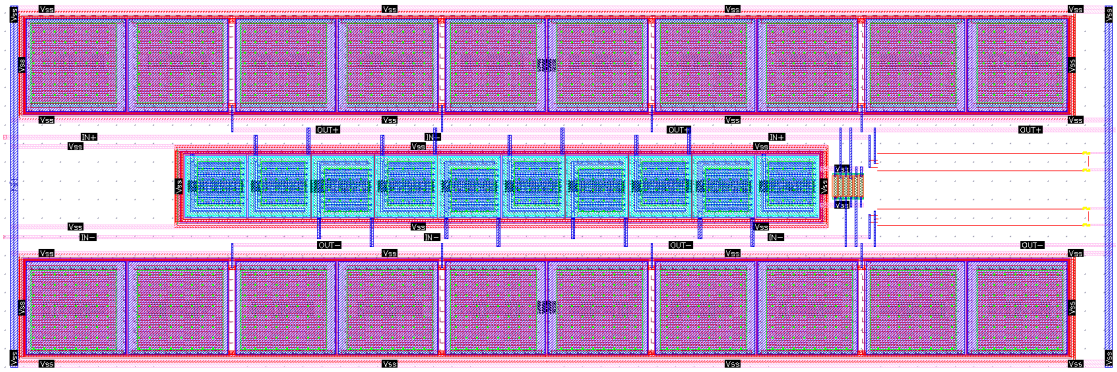

Figure 5.13: Layout of the designed high-voltage level shifter for the Bootstrap circuit.

Once parasitic capacitances and resistances were extracted, the circuit was again simulated in radiation corners and, furthermore, this time also mismatch analysis through Monte Carlo simulations was realized, to ensure that the introduction of parasitic elements does not affect significantly the symmetry of the structure. The former simulation results can be analysed in figure **??**. The difference $V_{out+} - V_{out-}$ (bottom plot) has still the correct shape and the transient peaks have values almost equal to those reached in the pre-layout simulation. The output

of the comparator reaches the correct value in each corner and, furthermore, the comparator is still triggered sufficiently fast, as it is possible to see from this plot, being the two signals well synchronized (in spite of a negligible but unavoidable delay). The same plots were evaluated performing a Monte Carlo simulation, considering only mismatch variations in 300 different points. The achieved plots do not differ significantly from the results obtained in the post-parasitic extraction nominal corner, hence for the sake of simplicity will not be displayed.

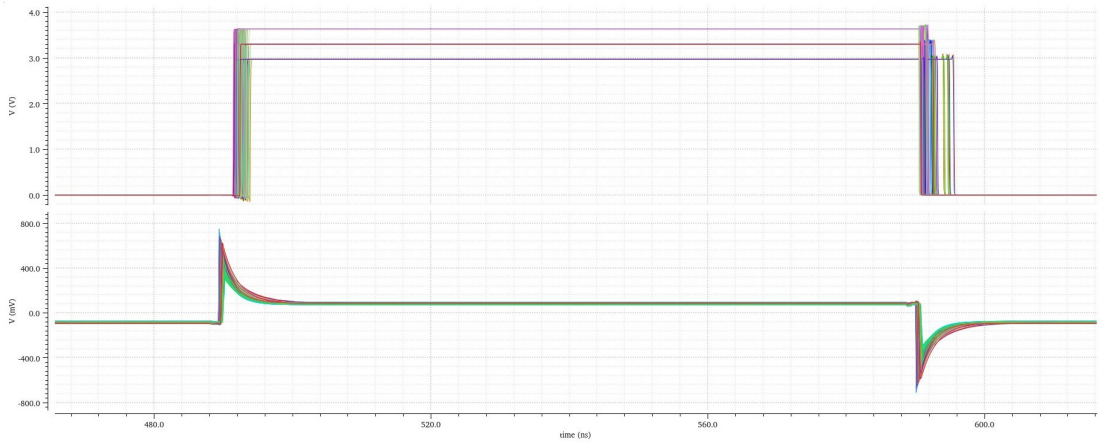

Figure 5.14: Post-layout simulation results in 289 radiation corners. The top waveform represents the difference $V_{out+} - V_{out-}$, while the bottom plot is the output of the comparator evaluated in the cited corners.

Chapter 6

Conclusions

Powering particle detectors for High-Energy Physics (HEP) experiments at CERN poses many significant challenges. For this reason, a dedicated team works on the development of DC/DC converters based on ASICs, whose purpose is to provide all the required voltages to power analog and digital front-end circuits, as well as optoelectronic circuits. This task requires significant engineering efforts, due to the necessity of placing such electronic devices in close proximity to experiments' collision sites, where the high levels of radiations reached and the extreme magnetic fields make commercial electronics not suitable for this purpose. The work presented in this thesis contributes to the development of custom radiation-hardened electronics for HEP experiments at CERN, particularly in the prospect of the future High-Luminosity LHC upgrade, exploiting a commercial 180nm high-voltage technology. The primary objective was to design the control circuit for a fully-integrated DC-DC converter, capable of withstanding the harsh environment of CERN collision chambers. Such converter will be designed to provide an output voltage of 2.5V starting from a 20V input voltage and its output must be stable under extreme temperatures (from $-30°C$ to $100°C$), high levels of TID (200Mrad) and high magnetic fields (up to 4T).

To ensure high reliability and robustness against radiation effects, the design process involved the application of radiation-hardening techniques at both simulation and layout levels. All the developed analog blocks were therefore optimized performing extensive simulations under several radiation corners, reproducing the worst conditions of operation for electronic devices in the depicted harsh environments. The achieved results demonstrated that the proposed designs meet the strict requirements set forth by the HL-LHC upgrade and opened the path for the realization of the layout for each block.

Among the different topologies analysed for the development of the error amplifier, the final choice relied on the two-stage folded cascode with Miller compensation network, as simulations proved its superiority against other architectures

both in speed, stability and power consumption, especially under the effects of a TID of 200Mrad.

Optimization of transistors dimensions and calibration of compensation elements led to a final design capable of reaching a gain-bandwidth product of 97.79MHz in the nominal corner and a minimum of 59MHz simulating in radiation corners, always guaranteeing very high stability (between $63.64°C$ and $97.93°C$). This amplifier is also characterized by a very high DC gain in all radiation corners (between 83dB and 113.2dB) and mismatch analysis through Monte Carlo simulations showed an input offset ranging between -1.815mV and 1.558mV, meeting target specification. To achieve such ambitious results under a TID of 200Mrad, especially in terms of speed, the current consumption reached by this block is equal to $300\mu A$. The search for less current consuming solutions led to design two additional amplifiers, working at lower frequency ranges (40MHz and 20MHz in the nominal corner), but suitable for very low-power applications: the first one works with $130\mu A$ and the second one with only $58\mu A$.

Regarding the 80MHz error amplifier, after validating its design through extensive simulations, its layout was realized. Due to the complexity of the block, several efforts were made to optimize the design in terms of layout and especially the routing approach, in the attempt of reducing parasitic capacitances and resistances. Indeed, the first post-layout simulations proved a significant loss of performances, caused by the effect of layout-induced parasitic components. Though performance worsening is inevitable with the introduction of parasitic elements, it was possible to earn significant improvements, especially in terms of stability, that was in the end guaranteed in every radiation corners. Routing optimization through study of parasitic effects is still undergoing to improve the GBW, that is currently ranging between 47.22MHz and 135.7MHz.

Concerning the delay lines designed for the delay generator, simulations of the whole control loop proved the effectiveness of such blocks in ensuring no cross-conduction between the switching transistors of the power stage. Furthermore, the design of the starved inverter, fundamental element of these delay lines, was proven to be high reliable and easy to control through an external current. In the end, two delay lines were designed, targeting two delays of 0.5ns and 1.7ns; these blocks were then used to generate 3ns, 4ns, and 5ns delay cells, exploited within the dead-time manager to accomplish the introduction of two dead-times between the high-side and low-side gate signals driving the power stage. Once again, extensive simulations proved the solidity of the implemented circuits and the following step will be the realization of the layout of each block.

Two level shifters were designed in the context of this thesis work, allowing the transition between different voltage domains: the first implemented level shifter has to rise the voltage from 1.8V to 3.3V, while the second (Bootstrap circuit)

shifts the voltage from the [0V, 3.3V] range to the [*Phase*, *Phase* + 3.3V] domain. Regarding the low-voltage level shifter, two circuit implementations were explored, a more standard topology and a variation of the latter presenting two pairs of cross-coupled transistors and zero static consumption. In the end, the second implementation was chosen as it proved to be faster, less power consuming and more resistant to SEE, especially to *Single Event Latch-Up*. The layout of the final circuit was then realized and post-layout simulations proved its feasibility, showing correct voltage shifting in all the radiation corners, with a slight decrease of response speed.

Ultimately, the RC divider for the Bootstrap circuit was realized: several efforts were made to optimize the value of the time constants for each RC filter in the final architecture. This optimization was aimed at increasing the difference between V_{out+} and V_{out-}, to ensure a faster triggering of the output comparator. In the end, sufficient speed was reached and the designed level shifter was capable of providing the correct gate voltage to drive the high-side switch.

Simulating the whole control circuit, while exploiting a simple buck converter for the power stage, it was proved that each designed block was working correctly: the high-side and low-side switches were never cross-conducting, even under irradiation conditions, while always ensuring the targeted output voltage of 2.5V. For completeness, in figure 6.1 it is possible to see an example of what is expected to be the functioning of the developed control loop, exploiting a buck converter in the power stage. The output signal V_{out} is correctly reaching 2.5V (as it is possible to see, it is still around 2.46V, but the transient simulation was computationally very heavy and hence it was stopped before the output could reach exactly 2.5V). The *Phase* node has the correct behaviour, moving between -0.7V and 20V, as expected; the output of the error amplifier (V_{EA}) coincides perfectly with the reference voltage V_{ref} and, finally, the two driving signals of the switches in the power stage have the correct timing, exhibiting the proper dead-times and guaranteeing no cross-conduction.

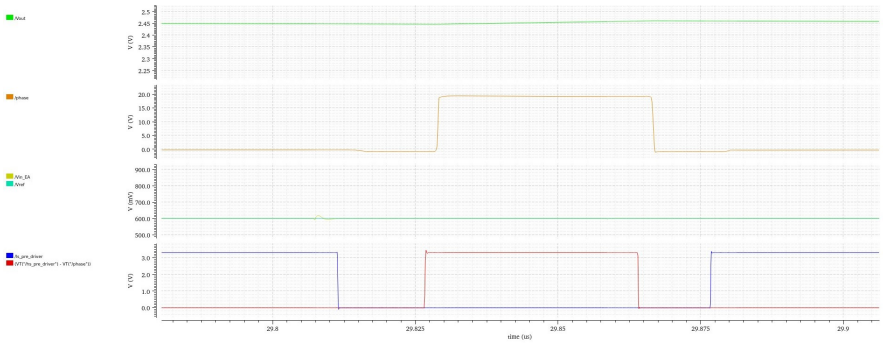

Figure 6.1: Main signals characterizing the proper functioning of the developed 20V-2.5V DC/DC converter.

Bibliography

[1] Giacomo Ripamonti. *Enhanced-performance integrated Resonant Switched-Capacitor and Buck DC-DC converters for application in extreme radiation and magnetic fiedl environments.* PhD thesis, Ecole Polytechnique Fédérale de Lausanne, 2020.

[2] URL: https://home.cern/about/who-we-are/our-history.

[3] URL: https://cds.cern.ch/record/2809109/files/CERN-Brochure-2021-004-Eng.pdf.

[4] URL: https://power-distribution.web.cern.ch/PowerDistribution/.

[5] Giovanni Maria Anelli. *Conception et caractérisation de circuits intégrés résistants aux radiations pour les détecteurs de particules du lhc en technologies cmos submicroniques profondes.* PhD thesis, Institute National Polytechnique de Grenoble, 2000.

[6] G. Borghello. *Ionizing radiation effects in nanoscale CMOS technologies exposed to ultra-high doses.* PhD thesis, University of Udine, 2019.

[7] Hanh-Phuc Le, Seth R. Sanders, and Elad Alon. "Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters". In: *IEEE Journal of Solid-State Circuits* 46.9 (2011), pp. 2120–2131. DOI: 10.1109/JSSC.2011.2159054.

[8] Maksimovic D. Erickson R. *Fundamentals of Power Electronics.* 2020. Chap. 9.

[9] Shuai Jiang et al. "Switched Tank Converters". In: *IEEE Transactions on Power Electronics* 34.6 (2019), pp. 5048–5062. DOI: 10.1109/TPEL.2018.2868447.

[10] Kenichiro Sano and Hideaki Fujita. "Performance of a High-Efficiency Switched-Capacitor-Based Resonant Converter With Phase-Shift Control". In: *IEEE Transactions on Power Electronics* 26.2 (2011), pp. 344–354. DOI: 10.1109/TPEL.2010.2062537.

[11] Willy M. C. Sansen. *Analog Design Essentials.* 2006. Chap. 2.

[12] Willy M. C. Sansen. *Analog Design Essentials.* 2006. Chap. 5.

[13] Davide Bucci. *The EKV transistor model for hand calculations in analog circuits*. 2021.

[14] Christian C. Enz Eric A. Vittoz. *Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design*. 2006. Chap. 5.

[15] Chemning Hu. *Modern Semiconductor Devices for integrated circuits*. Pearson, 2010.

[16] P. E. Allen. *Analog Integrated Circuit Design II*. Available on line. 2002. URL: https://pallen.ece.gatech.edu/Academic/ECE_6412/Spring_2003/L130-OpAmpCompII(2UP).pdf.

[17] *Analog Devices Glossary*. Available on line. URL: https://www.analog.com/en/resources/glossary/psrr.html.

[18] Arvind K. Sharma et al. "Common-Centroid Layouts for Analog Circuits: Advantages and Limitations". In: *2021 Design, Automation Test in Europe Conference Exhibition (DATE)*. 2021, pp. 1224–1229. DOI: 10.23919/DATE51398.2021.9474244.

[19] Yongsam Moon et al. "An all-analog multiphase delay-locked loop using a replica delay line for wide-range operation and low-jitter performance". In: *IEEE Journal of Solid-State Circuits* 35.3 (2000), pp. 377–384. DOI: 10.1109/4.826820.

[20] Yongfu Li et al. "A Comprehensive Study on the Design Methodology of Level Shifter Circuits". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 70.1 (2023), pp. 302–314. DOI: 10.1109/TCSI.2022.3213981.