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**in Electronic Engineering**

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# Process Simulations and Compact Modeling for a NS-GAAFET

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# Summary

In the most recent years, semiconductor-based devices and technologies have experienced fast improvements, resulting in important advancements. To enhance their performances, semiconductor devices have been scaled in geometrical dimensions and voltages, following Gordon Moore's laws.
However, scaling has led to the emergence of detrimental effects, such as short-channel effects and substrate leakage currents (respectively summarized in the DIBL and SS parameters) forcing designers to seek novel devices and technologies with improved electrostatic control and reasonable drive current and speed. In recent times, an important transition occurred with the introduction of 3D devices such as FinFETs. However, FinFETs have also become inadequate for the technological nodes of today due to some limitations. In this framework, stacked NanoSheet (NS) GAAFETs (Gate-All-Around Field-Effect Transistors) have been considered the most promising candidates for the replacement of FinFETs for sub-7-nm technological nodes.
The aim of this work is, starting from the experimental process, to obtain a matching between the aspects of the NS-GAAFET that have been analyzed. A compact model that is more closely related to the actual physical behavior of the device is missing.
Firstly, a comparison has been carried out between a numerical simulation of the technological process of the NS-GAAFET device and an experimental one. Process simulations have been compared with experimental data to highlight the main differences between the numerical simulations and the actual technological process, in particular regarding the process steps peculiar to the NS-GAAFET device itself. Electrical simulations have been, then, carried out to investigate the DC characteristics of the fabricated devices.
In the second part, a matching of the physics-based model with the BSIM-CMG-NS compact model has been done. Modifications in the Verilog-A code of the BSIM-CMG-NS were introduced to make the compact model match the physics-based simulator results.
In the last part, AC simulations have been done at the device level to investigate the impact of inner and main spacers in the time-varying regime. The choice of a low-k dielectric as the main and inner spacer turns out to be important for NS-GAAFET small-signal AC behavior, due to a reduced capacitance, which is peculiar to the NS-GAAFET device itself. Similar results have been obtained in circuit-level simulations, where the oscillation frequency of a Ring Oscillator of 5 ports has been retrieved for different main and inner spacer materials.

*Something old*
*Something new*
*Something borrowed*
*Something blue.*
*(... and a silver sixpence in the shoe...)*
[ Duke Ellington's music definition,
from an old English rhyme ]

# Acknowledgements

I would firstly like to express my gratitude to all my supervisors, Prof. Piccinini, PhD Dr. Mo, and PhD Dr. Spano, for allowing me to delve into this very exciting field of study, and for their patient support and guidance throughout the work.

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# List of Acronyms

**ALD** Atomic Layer Deposition.

**BTBT** Band To Band Tunneling.

**CMG** Common Multi Gate.

**CMOS** Complementary Metal Oxide Semiconductor.

**CMP** Chemical Mechanical Polishing.

**CPP** Contact Poly Pitch.

**CSA** Charge Sheet Approximation.

**CVD** Chemical Vapour Deposition.

**CY-FET** Cylindrical Gate FET.

**DG-FET** Double Gate FET.

**DIBL** Drain Induced Barrier Lowering.

**EDA** Electronic Design Automation.

**FET** Field Effect Transistor.

**FOM** Figure Of Merit.

**FP** Fin Pitch.

**GAA** Gate All Around.

**GCA** Gradual Channel Approximation.

**GIDL** Gate Induced Drain Leakage.

**IL** Interfacial Layer.

**IRDS** International Roadmap for Devices and Systems.

**LER** Line Edge Roughness.

**LKMC** Lattice Kinetic Monte Carlo.

**MIG** Metal Interdiffusion Gate.

**NS** Nano Sheet.

**PDE** Partial Differential Equation.

**PSG** Phospo-Silicate Glass.

**PTSL** Punch Trough Stop Layer.

**QC** Quantum Confinement.

**QG-FET** Quadruple Gate FET.

**QME** Quantum Mechanical Effects.

**SAC** Self Aligned Contact.

**SCE** Short Channel Effects.

**SIT** Sidewall Image Transfer.

**SOI** Substrate On Insulator.

**SPE** Surface Potential Equation.

**SPICE** Simulator Program with Integrated Circuit Emphasis.

**STI** Shallow Trench Insulator.

**TCAD** Technology Computer Aided Design.

**TEOS** Tetra Ethyl Orto Silicate.

**TG-FET** Triple Gate FET.

**VLSI** Very Large Scale Integration.

# Chapter 1

# Introduction

## 1.1 Multi-Gate FETs, GAA-FETs, and Stacked FETs

During these last years, society has deeply experienced in first person the progressive integration of CMOS technology. The term integration means that the number of the basic building blocks of the Integrated Circuits (ICs, or chips) the transistor, is increasing over the years.
This was predicted in 1975 by Robert Moore in his famous Moore laws, which concern the number of transistors per unit area (their density), which is increasing as a function of time and die size, while the gate length of those devices is decreasing in time (during the years). Starting from 1971, superseding the so-called TTL technology based on BJT devices, the MOS system has been, due to various features, the fundamental paradigm that designers had utilized to comply with the scaling principles until recent days.
Today MOS technology is, in fact, a well-established and well-known process, due to the number of studies and research done on it over a quite long time. [1]
Nevertheless, during the scaling process, technologists have encountered several non-ideal effects such as the Subthreshold Currents and the Short Channel Effects (SCEs) which have worsened the electrical behavior of the device, making the gate lose control of the channel. Some of the intrinsic parameters of the device, such as the threshold voltage $V_{th}$ do not scale and therefore are difficult to control. Hence, to combat those spurious effects, new devices have been introduced and proposed over the years. In particular, the classical 2D MOS (also called planar) process for MOSFETs was abandoned by the main foundries in 2014 (in the 14-nm technological node) in favor of a 3D process, allowing for a new device called FinFET, since the silicon was modeled in a fin shape. This novel 3D technology was tried to be as compatible as possible with the previous planar process to save money and equipment. [2]

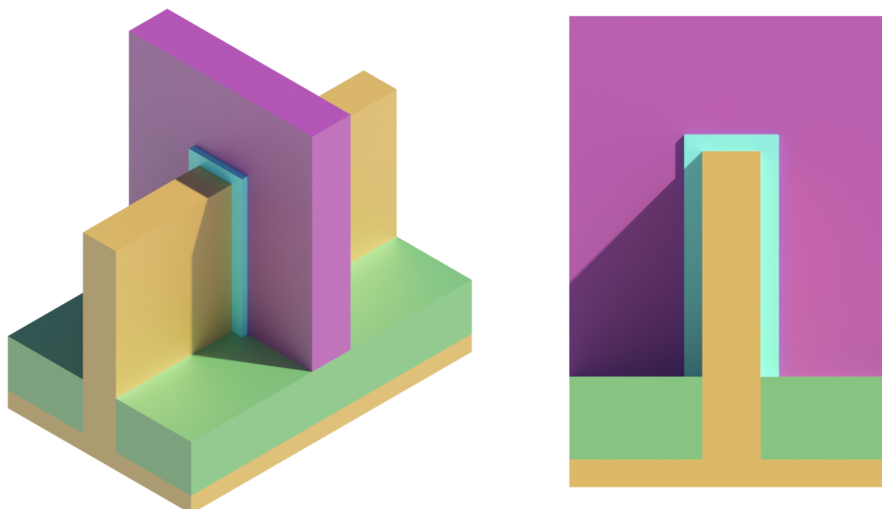

Figure 1.1. Fin-FET device, bird's eye, and cross-section views.

FinFET 3D technology is used nowadays at the industrial level but an evolution of the device is needed to proceed with integration, scaling more aggressively while maintaining the control of the channel by the gate as the dimensions (and eventually the supply voltage) of the devices shrink.
This paradigm is often referred to as the More Moore paradigm since the fundamental idea is to go on with scaling the MOS system, but to overcome leakages and Short-Channel effects, using different geometrical arrangements of the devices, exploiting the space as much as possible with the final aim of having gate and fin pitches (and hence logic cells) as small as possible.
In particular, the International Roadmap for Devices and Systems (IRDS) [3] has tried to predict the future trends of the MOS technology, where the CMOS basic idea is still present but it is further developed to comply with the continuous shrinking of the device dimensions (and voltages, depending on the used type of scaling). There are mainly two key ideas reported for the More-Moore paradigm:

- to wrap the silicon with the gate structure, switching from Multi-Gate FETs to Gate-All-Around (GAA) FETs.
- to proceed in the vertical direction, stacking more and more MOS systems.

Regarding the first point, Multi-Gate structures were the object of several studies. 3D processes enable, in fact, the possibility of having structures presenting multiple gates, giving the device several benefits: fewer subthreshold currents are present because only the amount of Silicon needed is used, leading to thin Silicon substrates. Multigate devices also offer an increased ON current, due to the presence of multiple channels and reduced dimension. However, in particular, those devices present reduced SCEs as a result of more

strong electrostatic control by the gates. Those devices can have a single gate electrode that controls multiple channels (common multigate) or more than one gate electrode that controls them separately.
FinFET devices were, in fact, the first example of Multi-Gate devices, having a Double-Gate (DG) structure at the beginning and, subsequently, a Triple-Gate (TG) structure, exploiting the top sidewall to create an additional channel, albeit with a 45° rotated crystal orientation, which presents different mobility and, hence, different transport properties.[4]
In the FinFET technological nodes, the possibilities to improve speed were limited only to the increase of the height of the fins $H_{fin}$ (leading to technological problems since a high aspect ratio $AR_{fin}$ is unfeasible from the technological standpoint) or otherwise to increase the number of fins $N_{fin}$, making also bigger, hence the device area(footprint). For these reasons, researchers have tried new geometries.[5]

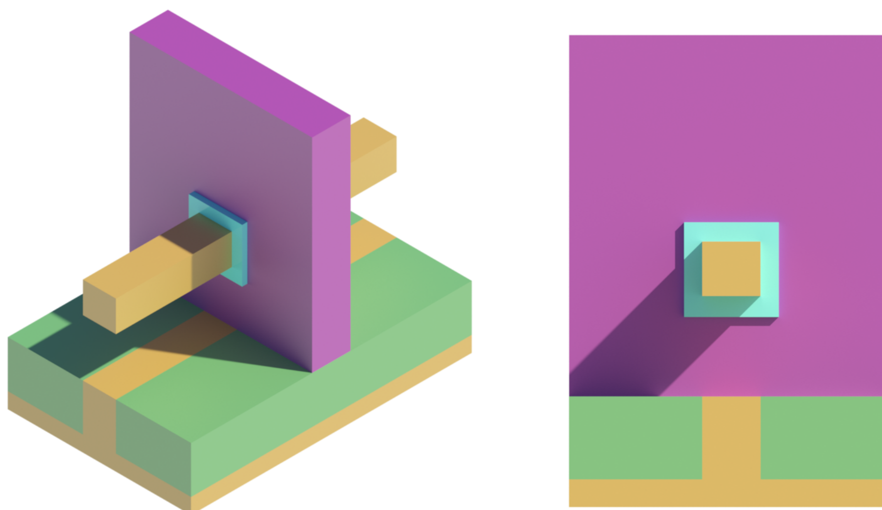

Figure 1.2. NanoWire FET with rectangular cross-section, Fin-FET device, bird's eye and cross-section views.

Starting from the Double-Gate Fin-FET and, then, with the Triple Gate Fin-FET idea of wrapping the silicon has been further extended to all the silicon faces, obtaining the previously mentioned GAAFETs, where the Silicon semiconductor is completely wrapped by the gate structure. GAA-FETs, in particular, may have two different shapes: the Cylindrical FET (CY-FET) which presents a cylindrical shape, and the Quadruple Gate FET (QG-FET), which instead has a rectangular section. Firstly, cylindrical cross-section structures have been tried, but it has been demonstrated that this particular geometrical configuration presents poorer electrical performances that have worse ON and subthreshold behavior compared to rectangular cross-section structures[6]. Rounded corners (hence a more "cylindrical" behavior) are considered a demerit figure in the rectangular cross-section stacked GAA-FET, degrading the device performance. [7]

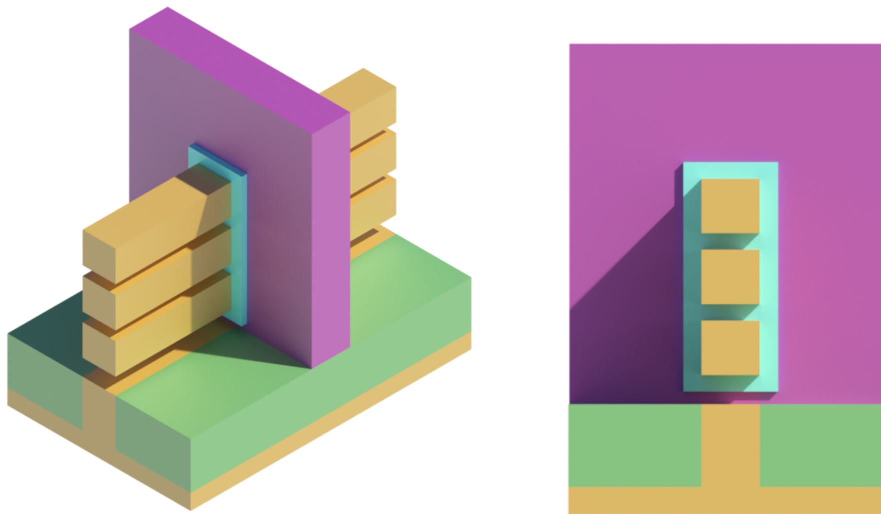

Figure 1.3. Stacked NanoWire FETs with rectangular cross-section, stacking of 4 Quadruple Gate (QG) devices

Regarding the second point, the idea of using the vertical direction was already started to be done in the FinFET nodes, by switching from planar devices to 3D ones. Nowadays this idea can be, in fact, further extended to comply with the Moore law by continuing to exploit the vertical direction by vertically stacking MOS structures using, for example, self-aligned processes, to minimize the gate pitch and scale the logic cells dimensions[8] and the interconnects lengths, resulting in reduced signal delays, increasing the devices speed and performance and the density of the devices for the same footprint. In this framework, novel devices have been presented but have not yet been studied in depth by researchers, such as Forksheet or Complementary FET devices (CFETs). [9]

## 1.2 NS-GAAFETs

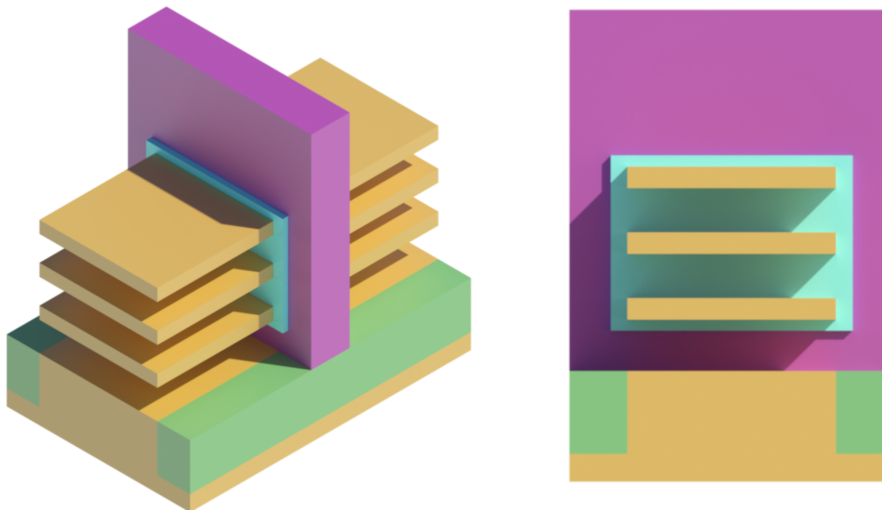

Figure 1.4. NanoSheet(NS) GAA-FET, bird's eye and cross-section views.

Issues regarding speed and performance have been tried to be solved, at this point, by keeping the rectangular cross-section but, this time, increasing the width $W_{NS}$ of the Silicon rectangular wires forming, hence, a stacking of NanoSheets which are wider sheets of silicon (Stacked NanoSheet FET) instead of the narrower wires, to increase the ON current, as it is possible to see in figure 1.5, where a comparison of the previous FinFET with the novel GAA geometries has been done.[10]
Moreover, the process steps for the NS-GAAFET are quite similar to the previous technological nodes, allowing compatibility of the new node with the previous ones. Only a few different process steps for the NS-GAAFET are, in fact, different or modified to the previous MOS devices.
The NS-GAAFET presents, anyway, a slightly worse OFF-state behavior, but this can be accepted by the increasing of the ON current due to this novel geometry with increased width, and hence an increase of the operating speed (and frequency) of the device is obtained, as it is possible to observe in table 1.2. [10]

This trade-off between the speed (ON current) and the power consumption (OFF current) of the device is a key point at design time. However, compared to its predecessors ( such as FinFETs), NS-GAAFET allows for more design flexibility, having additional degrees of freedom that can be exploited in device design, such as the width of the NanoSheet $W_{NS}$ or $T_{NS}$. As an example, by decreasing the thickness of the NanoSheets a better subthreshold behavior can be found, albeit with a slight reduction of the ON current and, most importantly, the appearance of quantum effects since for very low thicknesses

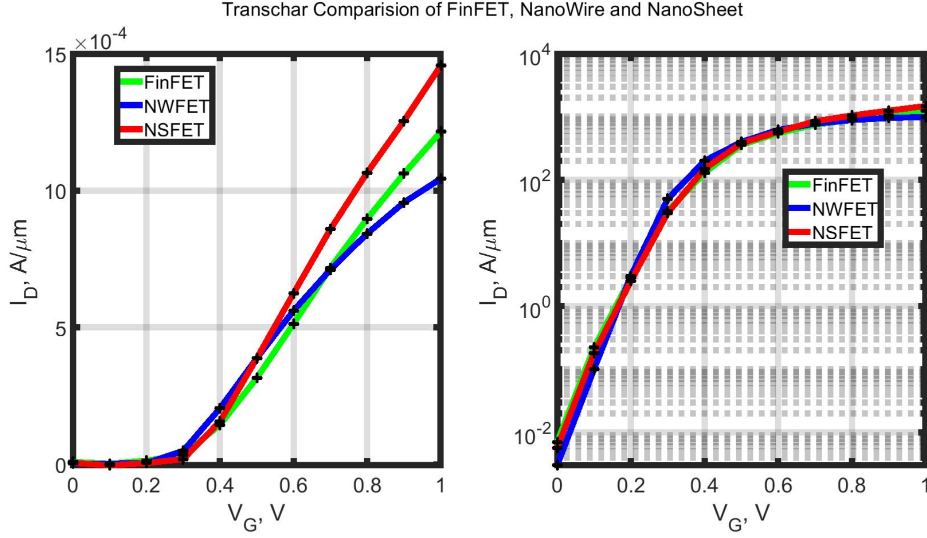


Figure 1.5. Comparison of the trans-characteristic of a single FinFET, NW-FET, and NS-FET, adapted from [10].

the NanoSheet may start behaving as a Quantum Well, causing unwanted effects such as threshold voltage shift and equivalent oxide thickness increase due to the charge centroid shift. [7]
Another parameter that gives an additional degree of freedom that can be designed is the number of nanosheets $N_{NS}$. For an increasing number of NanoSheets, the resistance decreases but the rate of decrease becomes slower since the carrier paths of the bottom NanoSheets become longer, making it necessary for the designer to find an optimal value of $N_{NS}$, which usually stands on around 3 (or even 2) stacked NanoSheets [11]. Moreover, even if the subthreshold behavior is worse than in more narrow devices the NS-GAAFET is more robust to SCE since its subthreshold behavior is less sensitive to gate length $L_G$ scaling. [12]

| Comparison of FinFET, single Nanowire, and Nanosheet devices, adapted from [10] | | | |
|---|---|---|---|
| FoM | FinFET | NWFET | NSFET |
| $V_{th}[V]$ | 0.158 | 0.164 | 0.176 |
| $SS[\frac{mV}{dec}]$ | 77 | 66 | 74 |
| $I_{OFF}[\frac{nA}{\mu m}]$ | 7 | 3 | 5.7 |
| $I_{ON}^{<110>}[\frac{\mu A}{\mu m}]$ | 612 | 568 | 699 |
| $I_{ratio}$ | $8.743 \cdot 10^4$ | $1.89 \cdot 10^5$ | $1.22 \cdot 10^5$ |

It is possible to notice that the ON current refers to the *<110>* direction since this particular crystal direction is the usually preferred channel direction, due to its more favorable properties if compared to other possible orientations of the Silicon lattice. [13]

## 1.3 Thesis Objectives

The main objective of the thesis is to match the physics-based simulations of a device obtained after a simulation of the process fabrication with a compact model based on the BSIM-CMG 110.00. The accurate details of the physical behavior should be caught as much as possible by the compact model, to make the latter as much as possible consistent with the higher level one, but the model should also be fast enough to be run by a SPICE simulator considering the device model in a circuital environment, having hence multiple devices connected one to another in different ways to be simulated at the same time. An open-source model for circuit simulation that is fast enough but also compliant with the higher physical levels simulations, such as the TCAD-based ones or even the Atomistic-based ones, is missing. The BSIM-CMG 110.0 model was originally conceived, in fact, only for Quadruple Gate (QG) FETs, while the cited version can also model a stacking of QG-FETs can be seen as a stacking of wide QG-FETs. A slightly different version of the original model [14], the BSIM-CMG-NS has been used, a variation of the original model that provides modifications to take into account the different geometry of the stacked NS-GAAFET [15]. Validations from higher-level simulators are needed to more accurately take into account the physical effects.
Moreover, AC simulations were performed to analyze the frequency behavior of the device and to investigate the impact of the choice of different materials for both main and inner spacers. Both device-level and circuit-level simulations have been done, analyzing the behavior of the cut-off frequency of the single device and the oscillation frequency of a ring oscillator topology.

## 1.4 Thesis Structure

This work has been structured as follows.
In this first chapter, an introduction to the topic studied in this thesis is given.
In the second chapter, an overview of the BSIM-CMG compact model and on Cadence Virtuoso suite has been provided.
In the third chapter, an overview of the Synopsis Sentaurus platform and the used tools have been provided.
In the fourth chapter, a process simulation has been performed using the Sentaurus SProcess tool, simulating the process fabrication of an n-type NS-GAAFET and a p-type NS-GAAFET using retrieved parameters from an actual experimental process. Subsequently, device-level simulations have been performed, comparing the derived electrical FOMs with the real process.
In the fifth chapter, matching the device-level simulations with the BSIM-CMG-NS model has been done by modifying the original BSIM-CMG-NS compact model.
In the sixth chapter, AC simulations have been performed in both simulators, analyzing the cut-off frequency
In the seventh chapter, final considerations and conclusions have been made.
Moreover, in the appendix at the bottom it is possible to find the Sentaurus scripts used in the thesis work and the modified compact model ones.

# Chapter 2

# BSIM-CMG Compact Model Overview

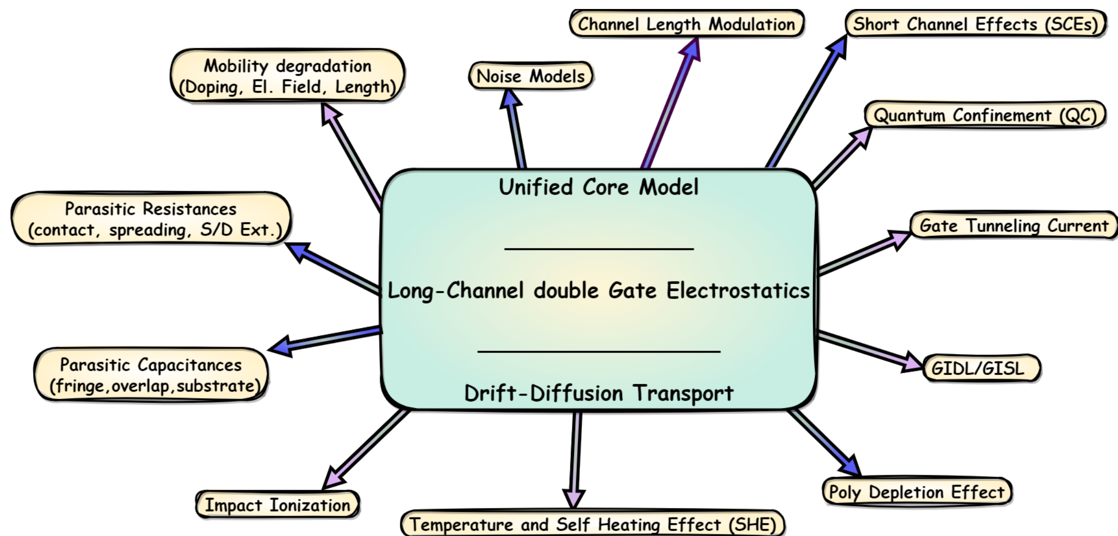


Figure 2.1. BSIM Core Model and Submodels

Electronic Design Automation (EDA) programs like, for example, SPICE (Simulator Program with Integrated Circuits Emphasis) based circuit simulators rely on the so-called compact (or behavioral) models of devices to be inserted in the circuit schematic entries. Compact models are mathematical models describing the behavior of a device (usually a transistor or another nonlinear device) in a way as concise as possible to be run by the simulator without too much computational burden and convergence issues, but achieving a certain amount of precision, at the same time, to be compliant with the evolution and to the increasing complexity of the device's physics due to scaling. Compact models are

usually implemented in a programming or description language such as C or Verilog-A.
A more deep and detailed analysis of the physical behavior of the device can be done by using physics-based models or atomic ones, which are, anyway, more computationally expensive, hence a trade-off between the two models, between the accuracy of the physical effects modeling and the computational speed, is needed.
The Berkeley Short-Channel IGFET (Insulated Gate FET) BSIM Model is a well-established model done by the Berkeley University of California, written in Verilog-A. It is one of the first models to be considered an industry standard by the CMC (Compact Model Council), even if many other device-behavior models such as the PSP, the Hi-Sim, the MEXTRAM, or the EKV-EPFL exist. The first BSIM compact model was created in 1980, and it was initially tailored for the available 2D technology but, then, it was uploaded several times due to the changing of the technology .
One of the latest releases of this model was the so-called BSIM Common Multi-Gate (BSIM-CMG, started in 2006), which is tailored for new Multi Gate devices such as the Double Gate (DG), Triple Gate (TG), and Quadruple Gate (QG) Field Effect Transistors. BSIM-CMG consists of a core model that solves the Surface Potential Equation (SPE), the equation that provides a link between the inner potential of the channel, the surface potential $V_s$, and the outer potential of the channel, the gate potential (which is usually called the bulk in the 2D system, while multiple gates have a source-referred system).
The solution by the core model of the SPE relies on the Gradual Channel Approximation (also called Long Channel Approximation) to solve the quasi-electrostatic Poisson equation, while the transport modeling is done with the well-known Drift-Diffusion model, using the Boltzmann statistics for the inversion charge and considering only the majority carriers for each n-type or p-type device, neglecting the minority ones [16] [17].
The Gradual Channel Approximation, in particular, considers only the transversal component of the Electric field (the component across the channel), neglecting the longitudinal one, the component along the channel). This approximation has led to the insurgence of the previously mentioned Short Channel Effects, which were observed empirically during scaling, in particular the reduction of the gate length $L_g$, and which were not into the equations' account.

The core model of the BSIM-CMG can be augmented by adding other sub-models describing various phenomena to provide a better estimation of the device behavior in a circuit, in particular for shorter gate-length devices. Effects that were secondary for previous nodes' devices (having bigger dimensions) become, in fact, more relevant with scaling; hence corrections have to be included in the BSIM model, and this was done by using the sub-models. It is possible to add, for example:

- SCEs (DIBL, Vth roll-off)
- Quantum Mechanical Effects (QMEs) such as Quantum Confinement or Gate tunneling Current.
- Poly-Depletion Effects (change in threshold voltage due to an additional depletion region in the Poly-Si).
- Parasitic resistances (contact, spreading, extension).
- Parasitic capacitances (friction, overlap, substrate).
- Mobility degradation at low and high Electric Fields.
- Temperature and Self-Heating Effect (SHE).
- Impact Ionization.
- Channel Length Modulation ($\lambda$).
- GIDL/GISL (a parasitic channel due to Band-to-Band tunneling )
- Noise models (thermal, shot, flicker).

## 2.1 BSIM-CMG Core Model

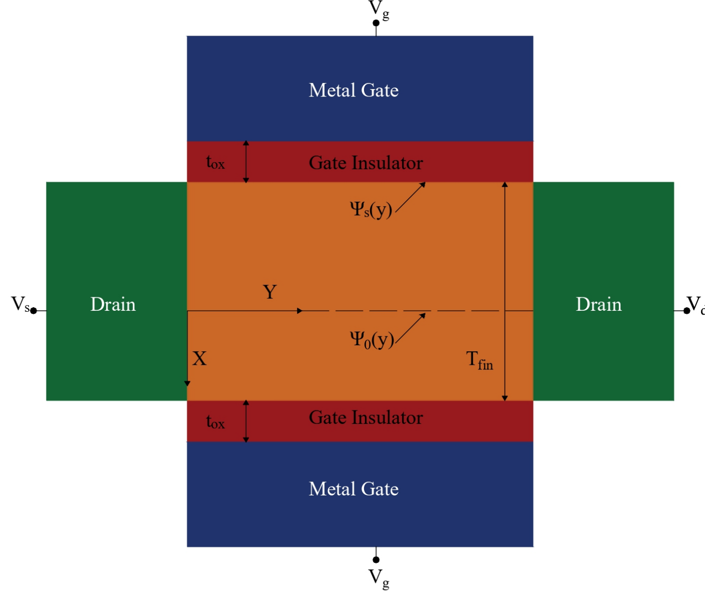


Figure 2.2. Double Gate (DG) FET Schematic Cross Section, adapted from [18]

The core model used in the BSIM-CMG is based on a solution of the 2D Poisson Equation for a Double Gate Structure 2.3.
The unknown of the Poisson equation is the electrostatic potential, which is proportional to the Energy of the Energy Bands diagram, The net charge density causes, in fact, a bending in the Energy Bands diagram, leading to a variation in the curvature (second derivative) of the potential.
It is possible to solve the 2D Poisson equation both in cartesian and cylindrical coordinates, by considering as invariant the third dimension and, hence, solving for the cross-section. Moreover, by using the Gradual (or Long) Channel Approximation (GCA) it is possible to neglect the contribution of the longitudinal electric field, considering only the transverse component: [17]

$$\frac{\partial^2 \varphi(x,y)}{\partial x^2} = \mathcal{E}_x >> \mathcal{E}_y = \frac{\partial^2 \varphi(x,y)}{\partial y^2}$$

We get:

$$\frac{\partial^2 \varphi}{\partial x^2} = \frac{q}{\epsilon_{ch}} \left( n_i e^{\frac{\varphi(x,y)-\varphi_B-\varphi_{ch}(y)}{Vt}} + N_{ch} \right)$$

Where $\varphi(x,y)$ is the electrostatic potential, $\varphi_{ch}(x,y)$ is the channel potential, representing the overall inner voltage drop from source to drain, $\varphi_B(x,y) = V_t \cdot ln\left(\frac{N_A}{n_i}\right)$ is the bulk potential and $N_{ch}$ is the channel doping, $V_t = \frac{k_B T}{q}$ the thermal voltage at $300K$, $n_i$ the

intrinsic carrier density in undoped Silicon, $N_A$ the doping of the substrate ( for an n-type device, opposite for the complementary one).

A peculiar feature of the BSIM-CMG model is that the electrostatic potential can be written using a perturbational approach, decoupling the effect of the mobile inversion carriers and the ionized dopants in a linear superposition effect, neglecting the mutual dependence. The channel doping acts, hence, as a perturbation on the electrostatic potential .[18]
It is therefore possible to separate these two components into two different equations:

$$\varphi(x,y) = \varphi_{inv}(x,y) + \varphi_{dop}(x,y)$$

$$\frac{\partial^2 \varphi_{inv}(x,y)}{\partial x^2} = \frac{qn_i}{\epsilon_{ch}} e^{\frac{\varphi(x,y)-\varphi_B-\varphi_{ch}(y)}{V_t}}$$

$$\frac{\partial^2 \varphi_{dop}(x,y)}{\partial x^2} = \frac{qN_{ch}}{\epsilon_{ch}}$$

It is also possible to exploit the geometrical symmetry of a DG-FET since the vertical component of the electric field is null ($\mathcal{E}_x(x=0)=0$) at the mid-fin position ( $x = 0$ ). By integrating the two components of the electrostatic potential we obtain:

$$\varphi_{inv}(x,y) = \varphi_0(y) - 2V_t ln \left[ cos \left( \sqrt{\frac{q}{2\varepsilon_{ch} V_t} \frac{ni^2}{N_{ch}} e^{\frac{\varphi_0(y)-\varphi_{ch}(y)}{V_t}}} \frac{x}{2} \right) \right]$$

$$\varphi_{dop}(x,y) = \frac{qN_{ch}}{\epsilon_{ch}} \frac{x^2}{2}$$

We can consider at this point the surface potential; hence:

$$V_s(y) = \varphi_{inv}(-T_{fin}/2, y) + \varphi_{dop}(-T_{fin}/2, y)$$

By integrating the Poisson equation we can retrieve the transversal surface electric field, in the vertical direction (across the channel):

$$\mathcal{E}_{xs} = \sqrt{\frac{2qn_i}{\varepsilon_{ch}} \left[ V_t \left( e^{\frac{V_s(y)}{V_t}} - e^{\frac{\varphi_0(y)}{V_t}} \right) e^{\frac{-\varphi_B-\varphi_{ch}(y)}{V_t}} + e^{\frac{\varphi_B}{V_t}} \left( V_s(y) - \varphi_0(y) \right) \right]}$$

Poisson equation is not manageable for full integration, since the electrostatic potential $\varphi(x, y)$ (referred to as the intrinsic Fermi energy $E_{Fi}$) and the electron concentration $n(x, y)$ have mutual dependencies, thus they need to be solved self-consistently.
Hence, using Gauss's law and applying Boundary Conditions (BC) at the interface, it is possible to derive the SPE, $Q_S = \mp\epsilon_{ch}\mathcal{E}_{xs}$ to obtain the variation of the mobile charge relative to the gate voltage (charge control law): [18]

$$V_g - V_{fb} = V_s(y) + V_{ins} = V_s + \frac{Q_S}{C_{ins}} = V_s(y) - \frac{\epsilon_{ch}\mathcal{E}_{xs}}{C_{ins}}$$

Where $V_g$ is the gate potential, $V_{fb}$ is the flat-band potential, $V_s$ is the surface potential, $\epsilon_{ch}$ is the channel dielectric constant.
Applying a change of variable:

$$\beta = \sqrt{\frac{q}{2\epsilon_{ch}V_t}\frac{n_i^2}{N_{ch}}e^{\frac{\varphi_0-\varphi_{ch}}{V_t}}}\left(\frac{T_{fin}}{2}\right)$$

It is possible, then, to obtain the compact form for the SPE valid for the Double Gate structure: [18]

$$f(\beta) = ln(\beta) - ln(cos(\beta)) - \frac{Vg - V_{fb} - \varphi_{ch}}{2V_t} + ln\left(\frac{2}{T_{fin}}\sqrt{\frac{2\epsilon_{ch}V_tN_{ch}}{qn_i^2}}\right) +$$

$$\frac{2\epsilon_{ch}}{T_{fin}C_{ins}}\sqrt{\beta^2\left(\frac{e^{\frac{\varphi_{dop}\left(x=\frac{T_{fin}}{2}\right)}{V_t}}}{cos^2(\beta)} - 1\right) + \frac{\varphi_{dop}\left(x = \frac{T_{fin}}{2}\right)}{V_t^2}\left[\varphi_{dop}\left(x = \frac{T_{fin}}{2}\right) - 2V_tln\left(cos(\beta)\right)\right]}$$

The final aim of a generic MOS system analysis is the calculation of the drain to source current. We need, hence, to include two transport equations for the two complementary mobile carriers, electrons and holes.
The most simple transport model is the Drift-Diffusion model (DD model), for which: [18]

$$J_n = -q\mu_n(T)n\frac{\partial\varphi_{ch}}{\partial y}$$

$$J_p = q\mu_p(T)p\frac{\partial\varphi_{ch}}{\partial y}$$

For an n-type FET (opposite sign yields for complementary device):

$$I_d(y) = \oint_{xz} J_n\, d\Sigma = -q\mu(T)\frac{\partial\varphi_{ch}}{\partial y}\int_0^W \int n(x)\partial z = \mu(T)WQ_{inv}$$

Where $\mu_n$ is the low field mobility and the total inversion charge is:

$$Q_{inv} = -\int_0^{+\infty} n(x)\partial x$$

Integrating the current along the channel to eliminate the longitudinal dependence we get the following: [18]

$$\int_0^L I_d(y)dy = I_d L = \mu(T)W \int_0^L Q_{inv}(\varphi_{ch}) \frac{\partial \varphi_{ch}}{\partial y} \partial y$$

$$I_d = \frac{W}{L}\mu(T) \int_{\varphi_{ch,S}}^{\varphi_{ch,D}} Q_{inv}(\varphi_{ch}) \partial \varphi_{ch}$$

By differentiating:

$$I_d = \frac{W}{L}\mu(T) \int_{Q_{inv,d}}^{Q_{inv,s}} Q_{inv} \left( \frac{d\varphi_{ch}}{dQ_{inv}} \right) dQ_{inv}$$

Where the inversion charges $Q_{inv,d}$ and $Q_{inv,s}$ at source and drain are derived by solving the 2D SPE in the auxiliary variable $\beta$, finding the surface potentials both at the source and at the drain end:

$$V_{S,source} = V_s(y = 0)$$

$$V_{S,drain} = V_s(y = L)$$

$$Q_{inv,d} = C_{ox} \left( V_g - V_{fb} - V_S, d \right) - Q_{dop}$$

$$Q_{inv,s} = C_{ox} \left( V_g - V_{fb} - V_S, s \right) - Q_{dop}$$

By approximating the inversion charge with:

$$Q_{inv}(y) \cong \sqrt{2qn_i \varepsilon_{ch} V_t} e^{\frac{\varphi_s(y) - \varphi_B - V_{ch}(y)}{2V_t}} \sqrt{\frac{Q_{inv}(y)}{Q_{inv}(y) + Q_0}}$$

Where $Q_0 = Q_{bulk} + 5\frac{\epsilon_{fin}}{T_{fin}}$.
We obtain the final drain current:

$$I_d = \frac{W}{L}\mu(T) \cdot \left[ \frac{Q_{inv,s}^2 - Q_{inv,d}^2}{2C_{ox}} + 2V_t \left( Q_{inv,s} - Q_{inv,d} \right) - V_t Q_0 \, ln \left( \frac{Q_0 + Q_{inv,s}}{Q_0 + Q_{inv,d}} \right) \right]$$

The core model of the BSIM-CMG model can solve the SPE for two different cross sections: the rectangular and the cylindrical one, corresponding to solving the SPE in cartesian and cylindrical coordinates but, afterward, a unified charge model has been proposed to have a model which is independent on the cross-section of the device [18] by generalizing the SPE to this Unified FinFET charge control relation :

$$v_g - v_0 - v_{ch} = -ln\left(-q_m\right) + ln\left(\frac{q_t^2}{e^{q_t} - q_t - 1}\right) - q_m$$

It is possible to observe that the first logarithmic term is relevant in depletion, the second logarithmic term is important in weak inversion and the last linear term is relevant in strong inversion.
Here voltages are normalized concerning the thermal one and charges are normalized concerning thermal voltage and insulator capacitance. In particular, $v_g$ is the normalized gate potential, $q_m$ is the normalized inversion charge and $q_t$ is the normalized total semiconductor charge:

$$q_t = \left(q_m + q_{depl}\right)\frac{A_{fin}C_{ins}}{\epsilon_{ch}W^2} = \left(q_m + q_{depl}\right)r_N$$

Which is the sum of the mobile inversion charge $q_m$ and the depletion charge contribution $q_{depl}$. The constant term is, instead, depending on the doping of the channel $N_{ch}$, the flat band potential, the channel area $A_{ch}$, and the normalized depletion charge $q_{depl}$ :

$$v_0 = v_{fb} - q_{depl} + ln\left(\frac{2qn_i^2A_{ch}}{V_tC_{ins}N_{ch}}\right)$$

It is possible to obtain the drain current $i_d$ by employing the Charge Sheet Approximation (CSA). CSA is a further approximation employed in most of the Surface Potential based compact model, in particular in this approximation the inversion charge is considered a delta Dirac distribution, a very thin sheet of charge having an infinitesimal thickness at the Si / $SiO_2$, hence neglecting its potential drop while considering only the depletion region one. The drain current can finally be obtained by difference:

$$i_d = \left[\frac{q_m^2}{2} - 2q_m - q_H \cdot ln\left(1 - \frac{q_m}{q_H}\right)\right]\Bigg|_{Q_{ms}}^{Q_{md}}$$

Where $q_H = \frac{1}{r_N} - q_{depl}$ and where $i_d$ is normalized to the gate length, the low field mobility, and the insulator capacitance. It is possible to notice that the first term is important in the saturation conditions (quadratic function of the inversion charge), the second term is important in the triode conditions (linear) and the last term is important in sub-threshold (logarithmic).
It is important to notice that if the inversion channel charge $q_m$ has a thickness comparable to the one of the depletion $q_{depl}$ the CSA is not valid anymore since the potential drop can be no more negligible. Moreover, the Quantum Confinement effect enlarges the effective thickness of the inversion layer (charge centroid) worsening the approximation.

## 2.2 BSIM-CMG Submodule for Quantum Confinement

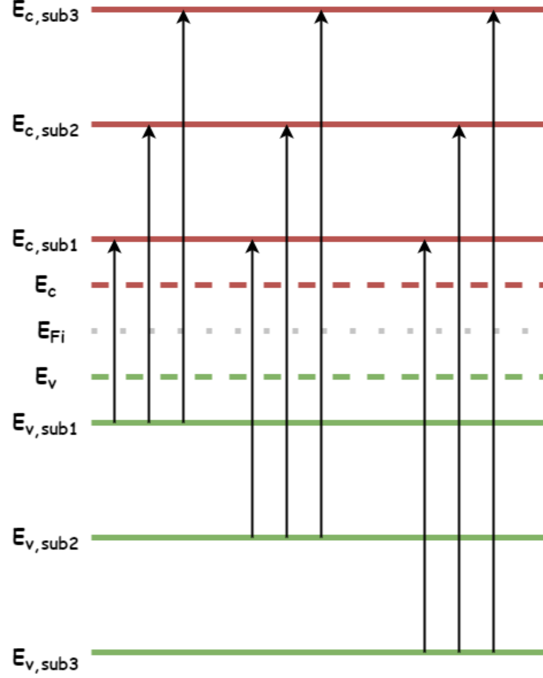


Figure 2.3. Energy subbands $E_{sub,i}$ formation due to Geometrical Confinement causing the threshold voltage shift $\Delta V_{th}$, adapted from [19]

Multigate FETs which are scaled in the nanometric dimensions may present several Quantum Mechanical Effects (QMEs) such as Quantum Confinement, Gate Tunneling, or Band-to-Band Tunneling (BTBT).
The Quantum Confinement (QC) effect, in particular, refers to the phenomenon where some properties of the free carriers change if they are confined to a very small space. In particular, this effect can be found if carriers are confined into a material having a thickness on a scale comparable to the electron wavelength weighted, in the Silicon lattice, by the effective mass (considering an average one since Silicon is an anisotropic material). This particular wavelength is called De Broglie wavelength, which roughly is:

$$\lambda_B = \sqrt{\frac{4\pi^2\hbar}{3m_{eff}k_BT}} \simeq 10\,\text{nm}$$

Thus, for devices having one or more geometrical parameters (such as the width or the thickness) below the De Broglie wavelength, it is possible to have non-negligible quantum effects such as the QC phenomenon.

Quantum confined carriers have quantized energies, behaving, for example, like electromagnetic waves confined in a waveguide, in which continuous values of energies are forbidden since their characteristic wave constant can only assume integer values. To have a complete solution to the QC problem we need to know the exact position, in the Energy domain, of the Subband Energies $E_i$, which can be solved rigorously by the Schrödinger equation by retrieving the bound states of the system, but the solution can be cumbersome and computationally expensive, hence in usual behavioral models as in the physical ones corrections in the model are applied to take into account the quantum effects.

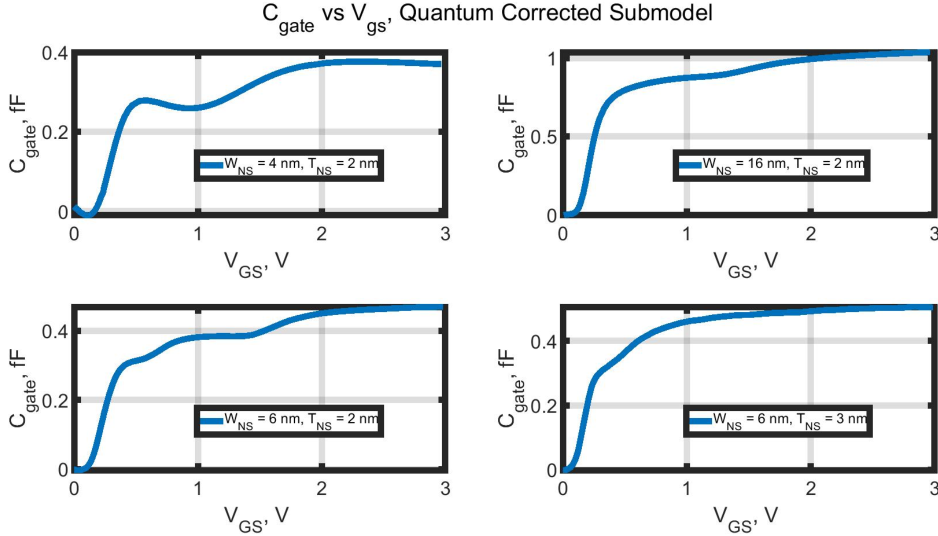


Figure 2.4. Gate Capacitance $C_{GATE}$ versus Gate Voltage $V_{GS}$ with quantum confinement model, $T_{NS}$ and $W_{NS}$ sweep, adapted from [7]. It is possible to notice the formation of secondary peaks due to the formation of subband energies for decreasing geometric values.

It is possible to have, in particular, two different forms of QC: geometrical confinement and electrical confinement. Geometrical confinement is not dependent on bias but on the structure: for a very thin thickness of the fin or of the Nanosheets it is possible to notice an upper threshold voltage shift. Decreasing the thickness of the Fin or Nanosheet $T_{NS}$, the Energy value of the subband energies increases $E_i$ and, consequently, the threshold voltage shift increases: due to QC more band bending and, hence, higher surface potential is required to have the same inversion charge density as in the deterministic model.

In the BSIM-CMG model, a correction on the surface potential is done to take into account the QC-induced $\Delta V_{th}$. The first two subband energies are taken into account and two different effective masses are considered:

$$E_0 = \frac{\hbar\pi^2}{2m_{eff} \cdot TFIN^2}$$
$$E_1 = 4E_0$$

Where the effective masses used are the standard values of longitudinal and transverse ones for Si:

$$m_l = 0.916 \cdot m_e$$
$$m_t = 0.190 \cdot m_e$$

Where the electron mass is:

$$m_e = 9.1 \cdot 10^{-31} Kg$$

By considering a factor:

$$\gamma = 1 + e^{\frac{E_0 - E_1}{k_B T}} + \frac{g' m_d'}{g m_d} \cdot \left[ e^{\frac{E_0 - E_0'}{k_B T}} + e^{\frac{E_0 - E_1'}{k_B T}} \right]$$

Where $g = 2$ and $g = 4$ are prefactor constants taking into account the 2 and 4-fold valley degeneracy. The corrective factor for the threshold voltage shift is:

$$\Delta V_{th,QM} = QMFACTOR_i \cdot \left[ \frac{E_0}{q} - \frac{k_B T}{q} ln\left( \frac{g \cdot m_d}{\pi\hbar^2 N_c} \cdot \frac{k_B T}{TFIN}\gamma \right) \right]$$

Where the parameter $QMFACTOR_i$ is a prefactor/switch to activate the correction. It is possible to observe that the subband energies depend on the inverse square of the thickness of the fin.[20]

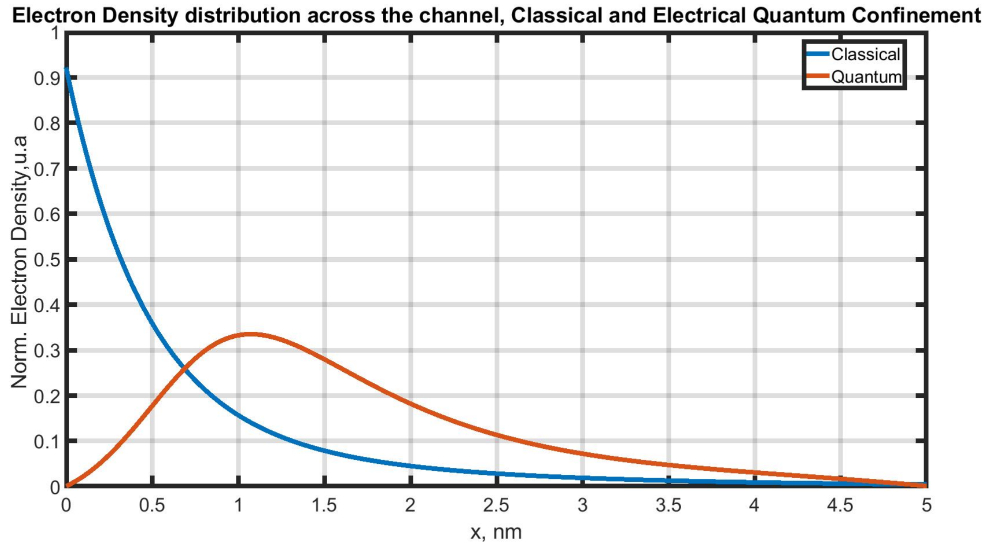


Figure 2.5. Electron density distribution on the vertical direction, electrical confinement causes electrons to be far away from the interface, planar MOS device.

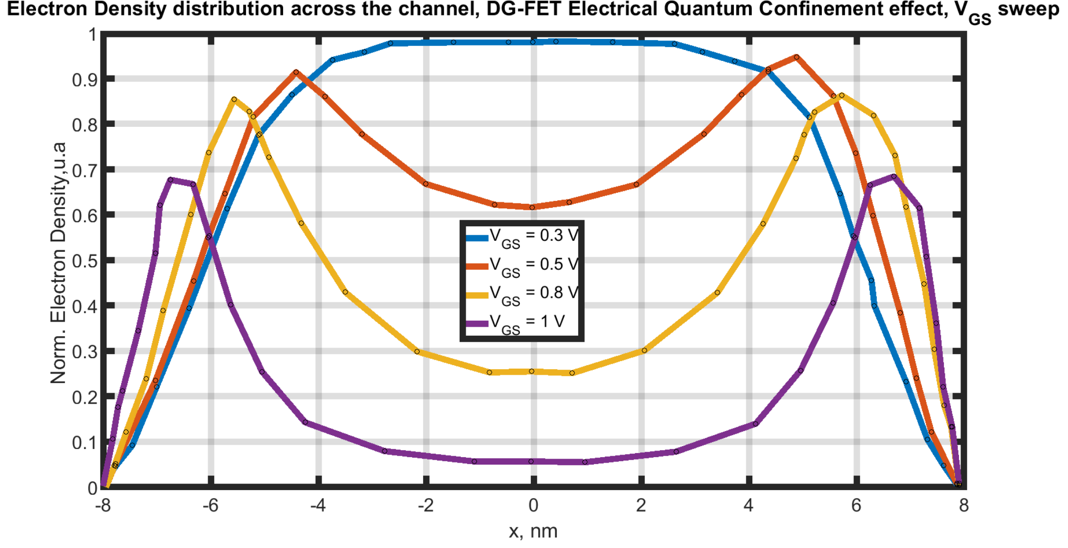


Figure 2.6. Electron density distribution in the vertical direction for a DG-FET, gate voltage sweep, adapted from [21]

The electrical confinement, instead, is a bias-dependent phenomenon due to QC, stemming from the inversion caused by the applied gate voltage, which in turn causes band bending. Electrical confinement causes a shift of the centroid charge depending on the applied gate voltage. Due to this effect, the mobile carrier population gets distant from the Silicon/Insulator interface due to the wavefunction distribution of allowed states, making the inversion charge more difficult to control. The inversion charge can, hence, be almost null at the interface for high gate voltages or for very thin Fins/Nanosheets, hence the charge could be located almost at the mid fin, enabling the so-called bulk inversion effect.[22]. Anyway, as the gate voltage increases the carrier density tends to move towards the Si / $SiO_2$ interface [21]. In the BSIM-CMG the electrical confinement is taken into account by a bias-dependent charge centroid shift parameter $T_{cen}$

$$T_{cen} = \frac{T_{cen0}}{1 + \frac{q_{ia} + ETAQM \cdot q_{ba}}{QMO}}$$

where $ETAQM$ is the body-charge coefficient for charge centroid shift and $QMO$ is a normalization parameter for charge centroid shift in inversion. It is possible to observe that the bias dependence in the centroid thickness shift is present due to a link with average inversion and bulk normalized charges computed by solving the SPE at Source and Drain and, subsequently averaging the two:

$$q_{ia} = \frac{q_{is} + q_{id}}{2}$$

$$q_{ba} = q_{bs} = q \cdot NBODY_i \frac{ACH}{CINS}$$

Moreover, Quantum Confinement causes a reduction of the effective width of the Multigate device. This effect is controlled by the $QMTCENIVi$ and the $QMTCENCVi$ quasi-switch parameters respectively for the I-V and the C-V characteristics. In particular, for the QG-FET the effective width is modified as follows:

$$W_{eff} = W_{eff0} - 8\, QMTCENIVi \cdot T_{cen}$$

$$W_{eff,CV} = W_{eff0,CV} - 8\, QMTCENCVi \cdot T_{cen}$$

Where the multiplicative factor 8 is due to the presence of four channels in the effective width.
Moreover, the centroid charge shift by QC operates a modification of the effective oxide capacitance $C_{ox}$ of the device, for $V_g > Vfb$:

$$C_{ox,eff,QM} = \frac{3.9\epsilon_0}{TOXP\frac{3.9}{EPSROX} + T_{cen} \cdot \frac{QMTCENCVi}{\epsilon_r atio}}$$

Where $TOXP$ is the thickness of the physical oxide, $EPSROX$ is the relative dielectric constant of the gate insulator and the parameters of the BSIM-CMG model. It is possible to observe that the effective capacitance may have an increased thickness depending on the centroid thickness parameter if activated by the $QMTCENCVi$ switch parameter. Quantum Confinement effects are revisable in the gate capacitance plots 2.4 where the subband energies can be observed as different bumps at different voltages in the $C_g(V_g)$ characteristic.

## 2.3 BSIM-CMG Submodule for Direct Gate Tunneling Current

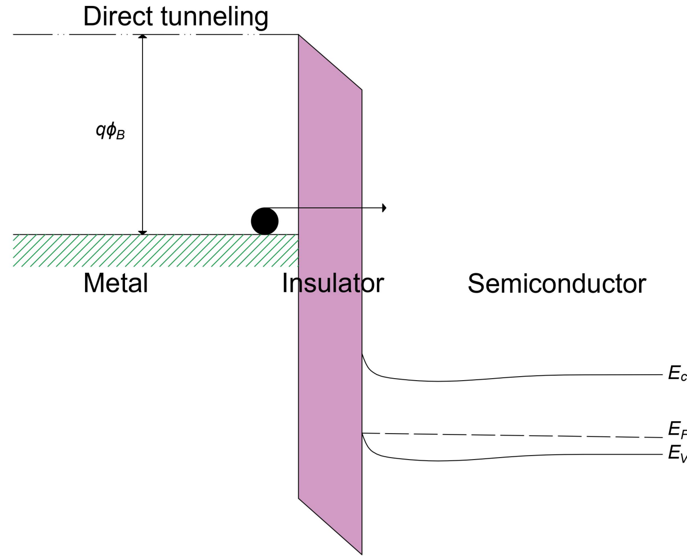


Figure 2.7. Gate Tunneling,

The BSIM-CMG model allows us to consider another relevant Quantum Effect, which is the Gate Tunneling or gate leakage current. In modern devices the gate dielectric stack has reached atomistic dimensions of few atomic lattices, causing a leakage effect attributable to the direct tunneling of carriers from the metal to the channel.
In direct tunneling carriers have insufficient energy to overcome a potential energy barrier classically (thermionic effect) but in quantum mechanics, the carriers present wave-like properties allowing them to tunnel through the barrier. The probability of tunneling depends exponentially on both the width and height of the barrier, and the impinging energy of the electrons. This effect macroscopically consists of an unwanted flow of electrons through the gate insulator layers of the device, due to the small thicknesses of the insulator materials themselves. Hence the gate current $I_g$ becomes non-zero, while usually MOS-based devices exhibit a null $I_g$, impacting in particular the subthreshold behavior increasing, hence, the OFF state current and the power dissipation and lowering the threshold voltage.
BSIM-CMG, in particular, makes a distinction in gate tunneling current modeling equations between the bulk and the SOI case: in the bulk case, the gate current flows from the gate to the substrate, while for SOI devices the gate current flows mostly into the source

since it has lower potential.

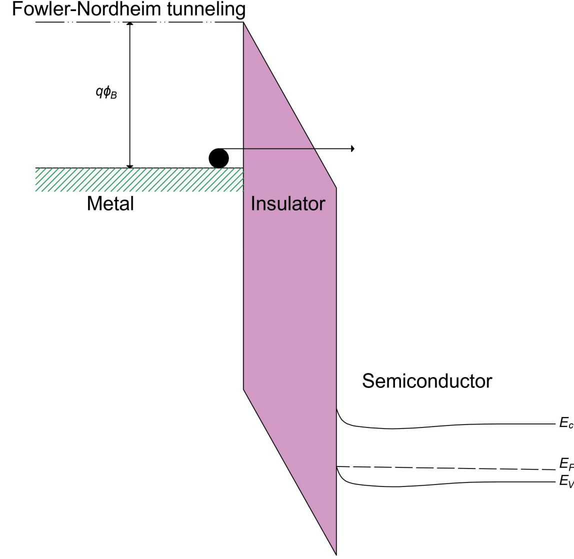


Figure 2.8. Fowler-Nordheim Gate Tunneling, direct tunneling is induced by a strong band banding (applied electric field).

The BSIM-CMG model uses the same model employed for the BSIM-4 one, which is based on a Fowler-Nordheim tunneling model, which is a direct tunneling that is enabled by high Electric Fields instead of the insulator thickness. [18]
Moreover, it uses a reference nominal gate oxide thickness for the gate tunneling model equal to $TOXREF = 1.2\,\text{nm}$ and uses the relative oxide thickness ratio normalized to the latter reference parameter:

$$T_{ox,ratio} = \frac{1}{TOXG^2} \cdot \left(\frac{TOXREF}{TOXG}\right)^{NTOX_i}$$

For a bulk substrate in inversion, the gate to substrate-current is:

$$I_{gb,inv} = W_{eff0} L_{eff} T_{ox,ratio} V_{ge} V_{aux,igbinv} \cdot I_{gtemp} \cdot NFIN_{tot} \cdot \\ e^{-B \cdot TOXG \cdot (AIGBINV(T) - BIGBINV_i \cdot q_{ia}) \cdot (1 + CIGBINV_i \cdot q_{ia})}$$

Where $A$,$B$, $AIGBINV$ and $BIGBINV$ are constant parameters, $V_{ge}$ is the gate to the substrate voltage, $V_{aux,igbinv}$ is an auxiliary voltage:

$$V_{aux,igbinv} = NIGBINV_i \cdot V_t \cdot ln\left(1 + e^{\left(\frac{q_{ta} - EIGBINV}{NIGBINV \cdot Vt}\right)}\right)$$

## 2.4 BSIM-CMG Submodule for GIDL/GISL and Impact Ionization

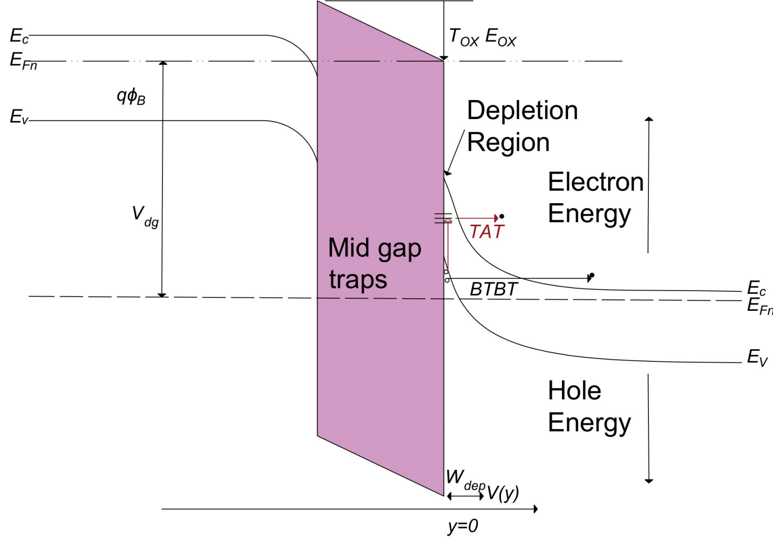


Figure 2.9. Band diagram showing BTBT and TAT phenomena causing GIDL/GIDL effect [23]

Another effect taken into account by an independent submodel of BSIM-CMG and which can be ascribed to Quantum Mechanical phenomena is the Gate Induced Drain Leakage (GIDL), or similarly the Gate Induced Source Leakage (GISL). This spurious effect consists of a parasitic current flow from the drain to the source caused by quantum mechanical phenomena, in particular, the Trap-Assisted Tunneling (TAT) and the Band-To-Band Tunneling (BTBT) effects occurring in the overlap region between the Drain and Source regions with the Gate, due to the unwanted lateral diffusion of dopants in this particular region. This parasitic current is particularly harmful to the OFF-state current, causing a dramatic increase in the leakage OFF-state current. BTB tunneling, in particular, is a Quantum Mechanical process where carriers can gain enough energy to tunnel the valence band $E_v$ being promoted to the conduction band $E_c$, or vice versa. In TAT, also called phonon-assisted BTB tunnel, carriers can tunnel by exploiting spurious trap levels $E_{trap}$ which can be present due to defects impurities, or other imperfections due to the fabrication process. Trap Assisted Tunneling, in particular, is the main actor in the GIDL/GISL phenomena at low electric fields (and hence for low power devices) [23].
The GIDL/GISL phenomena are very significant at high drain voltages $V_{ds}$, smaller gate lengths (can be considered SCEs), and thinner gate oxide, since the electric field increases.

Moreover, it is more relevant for decreasing temperature, since the generation rate increases The model implemented in the BSIM-CMG for GIDL adds a further component to the subthreshold current:

$$I_{GIDL} = T0 \cdot \frac{V_{se}^3}{CGIDL_i + V_{se}^3}$$

$$T0 = AGDL_i \cdot W_{eff0} \cdot \left( \frac{Vds - Vgs - EGIDL_i + V_{fbsd}}{\epsilon_{ratio} \cdot EOT} \right)^{PIGDL_i} \cdot e^{-\frac{\epsilon_{ratio} \cdot EOT \cdot BGIDL(T)}{V_{ds} - V_{gs} - EGIDL_i + V_{fbsd}}} \cdot NFIN_{total}$$

Where $AGIDL$ is the pre-exponential coefficient for GIDL, $BGIDL$ is the exponential coefficient for GIDL, $CGIDL$ is the parameter for body bias effect for GIDL, $EGIDL$ is the band bending parameter for GIDL The same calculations and considerations, albeit with different parameters, apply to GISL.

Impact ionization can be considered a Coulomb scattering phenomenon where, due to an applied electric field, carriers gain sufficient kinetic energy to impact violently the atoms of the lattice and ionize them, generating additional electron-hole pairs.[24]

BSIM-CMG model utilizes two models to emulate the impact ionization model, one for the bulk and one for the SOI substrate-based devices. [24] In particular for a bulk substrate:

$$I_{ii} = \frac{ALPHA0(T) + ALPHA1(T) \cdot L_{eff}}{L_{eff}} \left( V_{ds} - V_{ds,eff} \right) \cdot e^{\frac{BETA0(T)}{V_{ds} - V_{ds,eff}}} \cdot I_{ds}$$

Where $ALPHA1$ is a scaling length-dependent term, $BETA0$ is a Vds-dependent parameter of Iii and $V_{ds}$ is the effective drain-source voltage.

## 2.5 BSIM-CMG Submodule for Mobility Degradation and Velocity Saturation

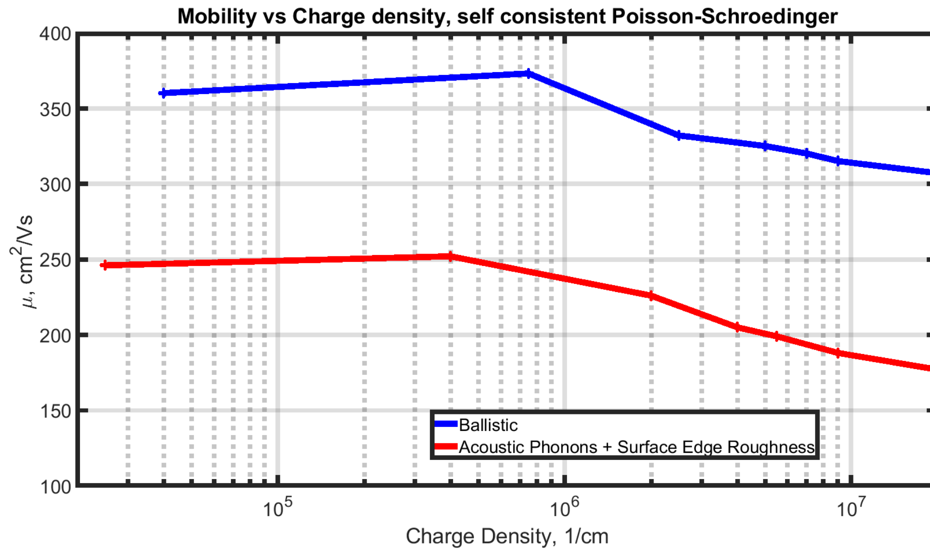


Figure 2.10. Influence of Acoustical Phonons and Surface Roughness Scattering on Mobility, adapted from [25]

Degradation of carrier mobility in the Multigate FETs can be divided into two main parts: low-field and high-field, having two separate submodels taking into account their effects. In particular, at low field, we have three main scattering events, which depend on the transverse component of the Electric field and the Surface potential (hence the region of operation): Coulomb scattering at weak inversion, Acoustical Phonon scattering at mid-inversion, and Surface Roughness scattering (SRS) at strong inversion. These three scattering phenomena are taken into account by the "Low field mobility degradation" submodel of BSIM-CMG, which modifies the effective mobility $\mu_{eff}$ parameter, introducing a degradation term. [26]

In particular, Coulomb scattering is a phenomenon related to the interaction between free carriers due to electromagnetic mutual interactions that cause deflections in the particle trajectories. Remote Coulomb scattering, in particular, it's an interaction of the free carriers on the channel with the trapped charge at the $SiO_2$/Hi-K material interface which limits the low field mobility, due to the presence of additional dipoles and charged defects at this interface due to the different chemical properties of the two amorphous materials.[27]

Acoustic Phonon scattering is a phenomenon related to the motion of the atoms in the crystal lattice, depending on the translational symmetry of the crystal, associated with the propagation of mechanical wa2es (such as sound pressure waves) and the propagation of heat (it is related to thermal conductivity). Since the amount of energy of the intravalley

acoustical phonon is relatively low, this scattering is considered elastic, hence the energy and the momentum are conserved.
Surface Roughness scattering is a phenomenon related to the imperfections and defects in the $Si/SiO_2$ interface causing particles to deviate trajectories. Fluctuation and uncertainty in this interface are considered anyway, in the process variations such as Line Edge Roughness (LER). Due to this, the mobility near the interface is, in fact, lower than the bulk mobility. [28]

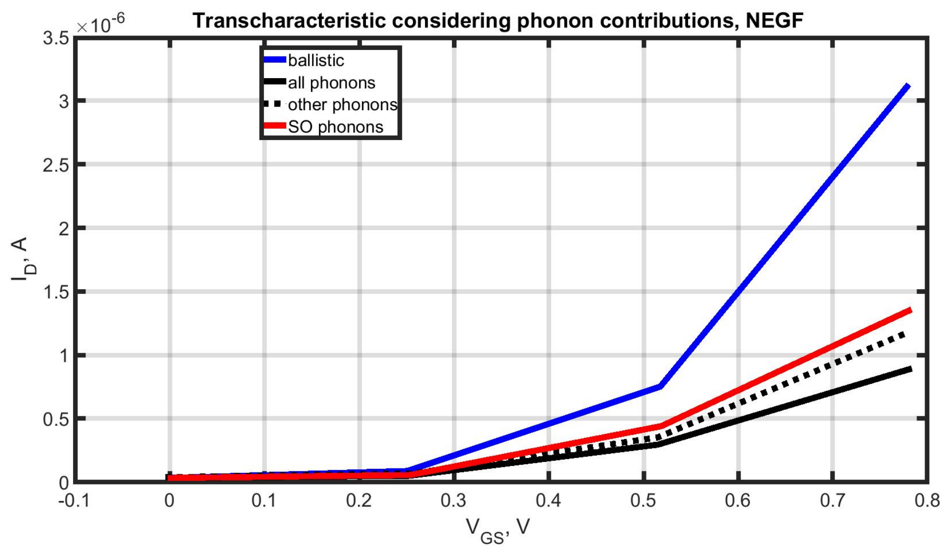


Figure 2.11. Influence of Optical Phonons in the trans-characteristic of a single NS-FET, adapted from [29]

Otherwise, at a high lateral field, the field dependence on the longitudinal component of the field and the dependence on the gate length becomes relevant. High-field effects can be considered SCEs since they depend on the channel length.
The main scattering mechanism acting is the Optical Phonon Scattering, which presents a higher energy than the previous ones, causing the velocity of the carriers to saturate. In this case, the BSIM-CMG submodel taking into account this effect degrades directly the drain-to-source current $I_{ds}$. Optical Phonon Scattering is an interaction between free carriers and high-frequency lattice vibrations in crystalline materials, mostly inelastic processes. The mobility degradation is described in the BSIM-CMG environment, for

bulk devices, as:

$$D_{mob} = 1 + (UA(T) + UC(T) \cdot V_{eseff}) \cdot (E_{effa})^{EU} + \frac{UD(T)}{\left(\frac{1}{2} \cdot \left(1 + \frac{q_i s}{E - \frac{2}{C_{ox}}}\right)\right)^{UCS(T)}}$$

Where $E_{effa}$ is the Source-Drain average effective Electric field:

$$E_{effa} = 10^{-8} \cdot \left(\frac{q_{ba} + \eta q_{ia}}{\epsilon_{ratio} EOT}\right)$$

The parameter $U0$ is the low field mobility, the parameters $UA$ and $EU$ are acoustical phonon/surface roughness scattering parameters, $UCS$ is the columbic scattering parameter, and $UC$ is the bulk coefficient for mobility.

For high field mobility instead, having velocity saturation, the degradation is in terms of current:

$$E_{sat} = \frac{2VSAT1_a \cdot D_{mob}}{\mu_0(T)}$$

$$D_{vsat} = \frac{1 + \left(\delta_{vsat} + \left(\frac{\Delta q_i}{E_{sat} L_{eff}}\right)^{PSAT(L)}\right)^{\frac{1}{PSAT(L)}}}{1 + (\delta_{vsat})^{\frac{1}{PSAT(L)}}} + \frac{1}{2} \cdot PTWG_a \cdot q_{ia} \cdot \Delta q_i$$

A similar calculation has been done also to take into account mobility degradation in the capacitance model. Some devices present a mild velocity saturation effect, hence some empirical parameters have been introduced in the BSIM-CMG model to fit this physical effect:

$$D_{vsat,NON} = D_{vsat} \cdot N_{sat} = D_{vsat} \frac{1 + \sqrt{1 + T0}}{2}$$

Where:

$$T0 = max\left[\left(A1(T) + \frac{A2(T)}{q_{ia} + 2nV_t}\right) \cdot \Delta q_i^2 - 1\right]$$

Where $A1$ and $A2$ are fitting parameters to be tuned.

## 2.6 Cadence Virtuoso Suite

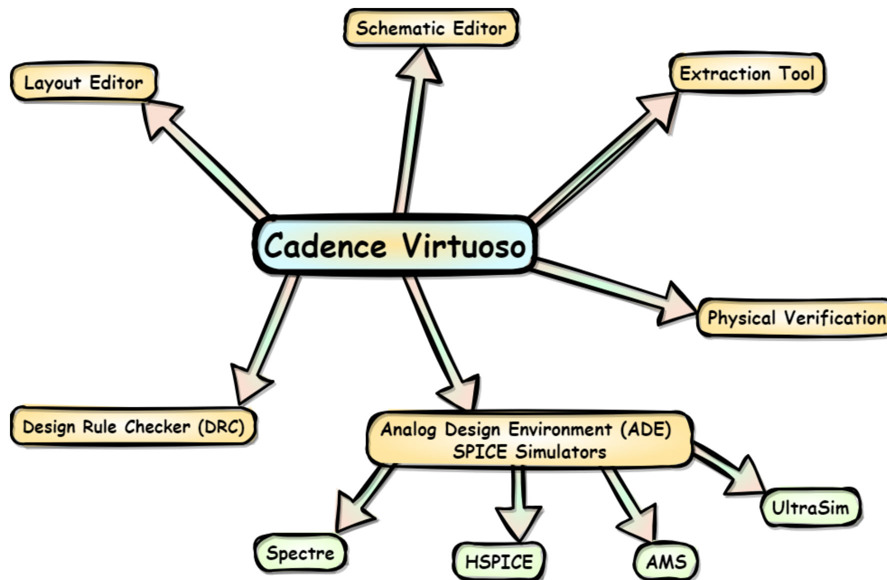


Figure 2.12. Basic scheme of Cadence Virtuoso suite

Cadence Virtuoso is an EDA (Electronic Design Automation) suite, and it is used for the design and verification of semiconductor devices and integrated circuits. Analog, digital, and mixed-mode simulations can be performed on it. It contains several tools (common in many SPICE-like EDAs) such as the Schematic Editor, which is a graphical interface used to draw circuit schematics, and the Layout Editor, which instead, allows the design of the physical layout of the IC (place and route), a Design Rule Checker (DRC), which ensures that there are no inconsistencies between the schematic entries and the physical design coming from the layout, the Physical Verification tool to consider process variations and an Extraction tool to extract parasitic elements from a circuit or a layout.
The main tool for circuit analysis which is usually employed in Cadence Virtuoso is the Simulation Environment called Analog Design Environment (ADE, also called Analog Artist) which has a collection of optimized circuit simulators (SPICE-based) used to analyze and validate previously built circuits, where Simulation Program with Integrated Circuit Emphasis (SPICE) simulators are a particular class of general-purpose circuit simulators created by Berkeley University and used to model the behavior of electronic circuits before the physical implementation.
In SPICE simulations some inputs need to be provided, such as the netlist, which is a textual description of an electronic circuit that defines the circuit topology, the initial conditions, a stimulus to the system, if needed by the simulation, and the models that synthesize the behavior of the various devices and components present in the circuit, allowing DC (static), AC (phase/frequency domain), and transient (time domain) analysis of circuits. In particular, there are two main types of components in circuit simulations,

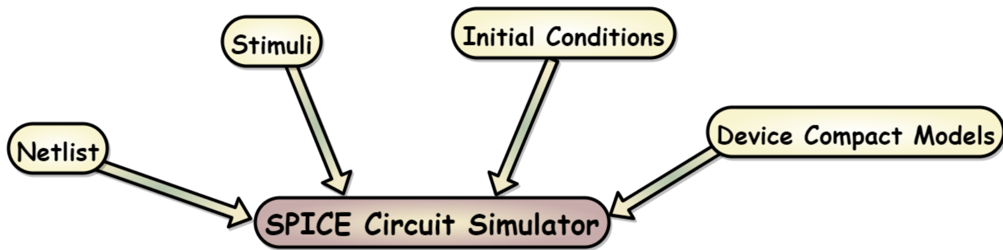


Figure 2.13. Inputs in a SPICE circuit simulator

passive devices (resistors, capacitors) which behave linearly, and active devices (transistors, diodes), which require a specific model to mimic their behavior, the compact model, which should be designed taking into account both the accuracy and complexity of the device physics but also the further complexity that the latter adds to the simulation. Moreover, in active device models, some user-definable parameters are added to be swept to check their impact on the overall system.
SPICE simulators, usually, solve equations based on the Kirchoff Current Law (KCL) for each node of the circuit and the Kirchoff Voltage Law (KVL) for each loop of the circuit by using matrix-based approaches and numerical methods like, for example, the Newton-Rhapson one. The KCL is solved by the algorithm by introducing a voltage variable (measured to a reference one) and identifying the nodes. Non-reference nodes have a fixed potential, such as ground. Subsequently, the nodal equations are transferred into a matrix formulation, solved by using numerical techniques such as the LU factorization and the Newton-Rhapson method, which are necessary if nonlinear devices (such as transistors, diodes, and so on) are present as components of the circuit. Then, once the nodal voltages are known, the SPICE simulator calculates the respective branch currents. For passive elements, SPICE uses the voltages obtained from nodal analysis and checks if the voltages across elements satisfy KVL when summed around the loops in the circuit, while for active elements SPICE utilizes their respective models and equations to ensure KVL holds in the branches involving these components. [30]
In the ADE environment, several optimized SPICE simulators are present, such as UltraSim, Orcad PSpice, AMS, Synopsis HSpice, and the Cadence Spectre simulator. Cadence Spectre, in particular (which is the one used in the circuital simulations of this thesis) is an optimized SPICE circuit simulator with ameliorated convergence and speed by acting on some parameters of the SPICE algorithm itself [31]. But, most importantly, the Spectre simulator allows the use of compact models written in Verilog-A (or C language) as inputs to mimic and simulate non-linear devices (such as the NS-GAAFET transistor) and circuits made with those devices as building blocks.

# Chapter 3

# Sentaurus TCAD Platform Overview

## 3.1 SProcess Tool

The TCAD simulators (Technology Computer-Aided Design) are EDA ( Electronic Design Automation) software that are used in the physics-based analysis and the design of electronic devices, such as Synopsis Sentaurus, Silvaco, or Global TCAD Solutions (GTS). Those simulators are employed to simulate and model several aspects of various devices, such as the fabrication processes or the electrical performances.
In particular, regarding the device fabrication, Sentaurus SProcess is a Sentaurus Tool that is specifically focused on process simulations, providing models or methods to mimic the various fabrication steps, allowing the simulation and optimization of technological process steps such as epitaxy, annealing, ion implantation, thermal oxidation, etching, deposition, and many others, and it can be used both for planar and 3D fabrication process steps. In summary, SProcess can be used to study how different process parameters affect the final characteristics and FOM of a device, using various mathematical models or algorithms to simulate the fabrication steps.

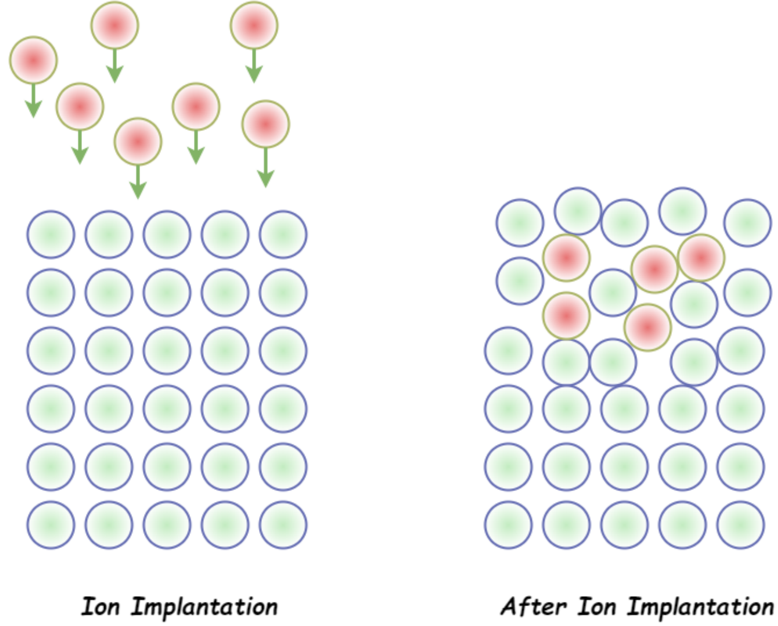


Figure 3.1. Ion Implantation process

As an example, ion implantation is a process step where impurities are accelerated and launched to be inserted into semiconductors. The dopant distribution due to the implantations and the damage they cause to the semiconductor lattice can be treated by SProcess with analytic functions or a Monte Carlo (MC) method. In the analytical models, a distribution function is chosen to simulate the spatial distribution of the ions depending on the ionic element, the energy of the implantation, dose, tilt, and rotation angles. The distribution function used, such as the Gaussian one, is described by statistical moments, where the first is the projected range (an expectation value of the arrival of the impurities): [32]

$$R_p = \int_{-\infty}^{\infty} x \cdot f(x) \cdot dx$$

The higher-order statistical moments such as variance, skewness, and kurtosis are calculated as:

$$m_i = \int_{-\infty}^{\infty} (x - R_p)^i \cdot f(x) \cdot dx$$

Hence, a simple Gaussian distribution can be used:

$$f_{gauss}(x) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(x-Rp)}{2\sigma^2}}$$

More advanced distribution functions for the ion implantation such as the Pearson functions can be used, but also atomistic simulations such as the Kinetic Monte Carlo (KMC), which employs the binary collision approximation (a heuristic model assuming elastic collisions) and which could be used to improve the simulation accuracy. Furthermore, to

calculate damages in the lattice structure, the Hobler model is used, relying on a basic Gaussian distribution corrected with exponential tails which depend on the lightness or the heaviness of the implanted ion. [33]

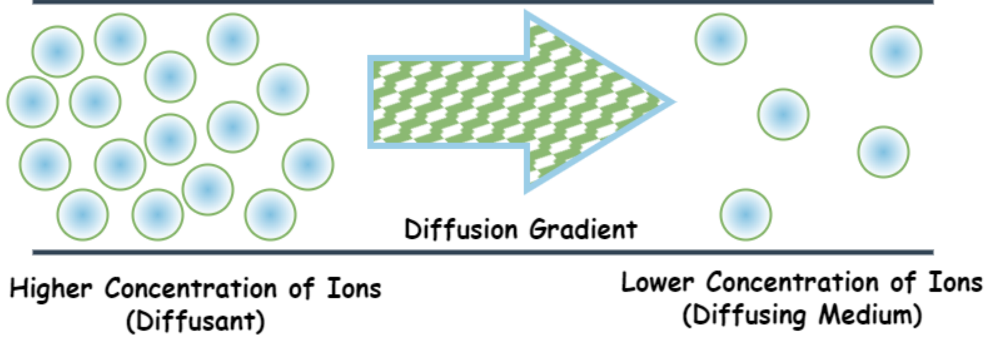


Figure 3.2. Diffusion process

The diffusion process, instead, is a thermal process used to activate and redistribute dopants or to recrystallize a damaged lattice in Solid Phase Epitaxial Regrowth (SPER). Moreover, in Sprocess, the diffuse command is also used to simulate material growth processes such as epitaxial growth or oxidizing growth such as dry or wet oxidation processes. Diffusion could be modeled generally as a system of PDE describing the transport of dopants and the conservation of the dose (continuous diffusion).
In particular, the diffusion current density with its continuity equation reads:

$$\frac{\partial A^c}{\partial t} = -\nabla \cdot J_{A^c} + R^{trans}_{A^c} + R^{react}_{A^c}$$

$$J_{A^c} = -d_{A^c}\left(\frac{n}{n_i}\right)^{-c} \nabla \left(A^c \left(\frac{n}{n_i}\right)^c\right)$$

Where $A^c$ is the specie of charge $c$, $d$ the diffusivity, $R^{trans}_{A^c}$ is a recombination term which can be tuned by choosing a specific transport model and $R^{trans}_{A^c}$ is a chemical reaction term which transforms a specie into another one.
For very small dopant doses or device dimensions, it is also possible to use an atomistic or quasi-atomistic process model such as the Kinetic Monte Carlo (KMC) instead of the continuum diffusion, which is also a more spontaneous way of considering process variability since it considers the atomical interaction of dopants leading to defects and impurities using more accurate statistical approaches.
KMC is considered, anyway, a quasi-atomistic model since it ignores the lattice atoms, which are, instead, considered in the Lattice Kinetic Monte Carlo (LKMC), which is a fully atomistic Monte Carlo modeling of diffusion, epitaxial growth, or SPER. LKMC may also be used for epitaxial deposition simulations, instead of standard epitaxy, and considers, in fact, the interaction of Silane $SiH_4$ gas atoms with the Si lattice atoms of the substrate.

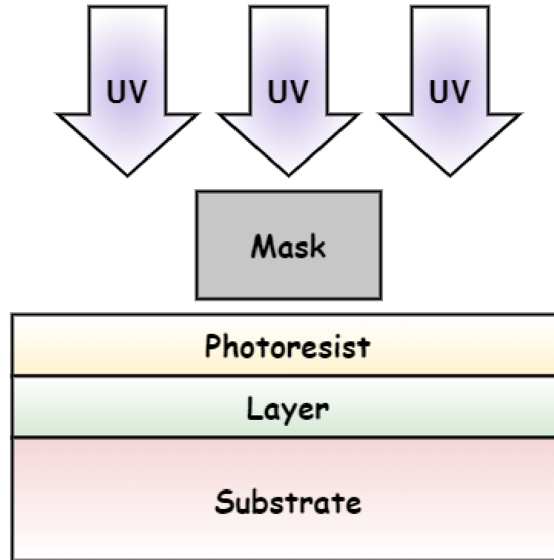


Figure 3.3. Generic Photo-Lithographic process

To define the device's geometric structure etching and deposition processes are simulated by SProcess. It is possible in fact to mimic photolithographic processes by defining masks and photoresist layers (negative and positive ones) allowing to limit the deposition or etching process to a specific spatial window of the device.
Various types of etching and deposition could be used. Regarding etching, the ones used in this thesis are isotropic, anisotropic (along the vertical direction, as in reactive ion etching), and Chemical-Mechanical Polishing (CMP), etching a specified material up to a vertical coordinate). Moreover, for those materials that are directly exposed to the ambient at that current process step, it is possible to remove them using the strip command, which removes the selected material. Similar types exist for the deposition: isotropic, anisotropic (has a preferential direction), and fill (fills the structure with a specified material up to a vertical coordinate).
It is also possible to mimic the Line Edge Roughness (LER), which is a statistical fluctuation in photo-lithographic processes, can be modeled as a random noise from the power of a Gaussian, having a standard deviation $\Delta$ and a correlation length $\Lambda$:

$$Autocorrelation\,(f_{random}) = \Delta^2\sqrt{\pi}\Lambda e^{\frac{-x^2}{\Lambda^2}}$$

## 3.2 NS-GAAFET process steps

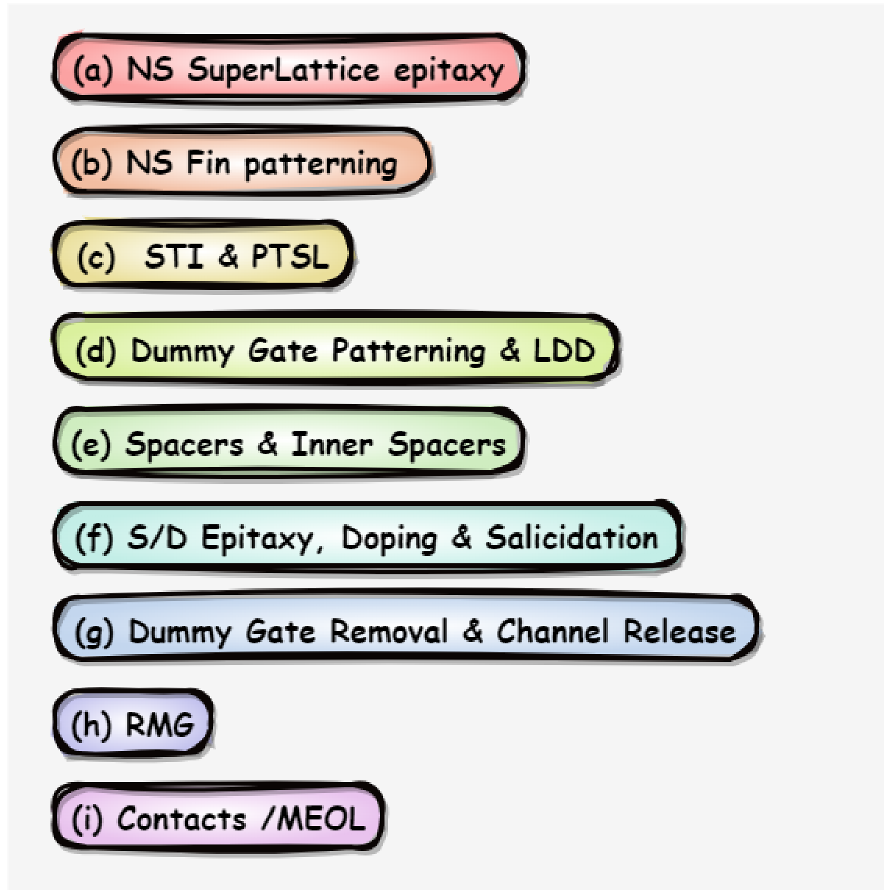


Figure 3.4. Main process steps for the fabrication of a stacked NS-GAAFET, as described in [34].

The technological process for the NS-GAAFETs presents several nodes that are similar to the previous 3D technological nodes, the FinFET ones. This aspect is very useful since allows process compatibility between these two devices. Nevertheless, some of the process steps are peculiar to the NS-GAAFET fabrication itself.
In particular, the considered process flow is the following (taking as reference the steps from [34] and depicted in the TEM photographs):

(a) As a first step the Si/SiGe Superlattice growth is done. An epitaxial growth of a Si/SiGe SuperLattice on a Silicon substrate, involving the growth of alternating layers of Silicon (Si) and Germanium (Ge), avoiding the presence of lattice defects (point or dislocations) and controlling the thickness of the layers and their composition (molar fraction). During the epitaxial growth, it is possible to choose, in fact, the thickness of the Si layers and hence the NanoSheet one $T_{NS}$, and the thickness of

the SiGe epitaxial layers, which is instead the spacing $T_{sp}$ between the NanoSheets. The molar fraction of the $Si_{1-x}Ge_x$ sacrificial layers has been chosen to optimize the stress along the channel, increasing the mobility, to an optimal value of $x_{mol} = 0.3$, growing hence a $Si_{0.7}Ge_{0.3}$ SuperLattice.[35] The most used orientation for the main surface of the NanoSheet superlattice is the one parallel to the substrate, the *(100)* orientation with the sidewall channels on *(110)*, since it shows better electrical properties [36], albeit causing a considerable mobility mismatch between the complementary devices. In the Fin-FET case, instead, Silicon fins were oriented perpendicularly to the substrate orientation, hence on the (110) plane. In the (100) case it happens that the mobility of the electrons is larger if compared to the mobility of the holes, thus obtaining a higher current for n-type devices, but the sensitivity of the hole mobility $\frac{\partial \mu_p}{\partial \epsilon_{strain}}$ relatively to the strain is increased [37]. The transport direction remained, instead, unchanged to the *<110>* one from the FinFet to the NS-GAAFET devices. [38] Moreover, in real processes, the probability of the presence of defects in the periodicity of the lattice, such as point defects (1D), dislocations, and grains (2D) or volume defects (3D) in the lattice structure is non-null. Point defects can be of various types, such as vacancies, self-interstitial, substitutions(like doping), or interstitial. In particular, in the growth of a SuperLattice, the diffusion of different atoms ( Ge in the Si layer or vice versa) causes interstitial or substitutional defects.

(b) The main Fin,made of the stacked Si layers and the sacrificial SiGe ones, the Sidewall Image Transfer process step is used ( as in the FinFET process): dry thermal oxidation is firstly done upon the stacked epitaxial Superlattice to form an oxide layer, then a thick layer of Silicon Nitride $Si_3N_4$ (hard mask) and a thick layer of Amorphous Silicon (mandrel), are deposited using a Chemical Vapour Deposition (CVD). Then an anisotropic etching is performed on the mandrel using a negative photoresist mask, to allow for the creation using the hard mask as an etch stop layer. Subsequently, the oxide spacers are fabricated on top of the hard mask and the side of the mandrel using the classical spacer fabrication method: a CVD of the spacer oxide, then an anisotropic etching, and, lastly, an isotropic over-etch to eliminate the residuals on top of the mandrel.

(c) Afterwards, the mandrel layer is etched, being at this point of no use. Subsequently, the hard mask and the bottom oxide are etched, allowing the patterning of the SuperLattice fin with an additional anisotropic etching of the SuperLattice Si/SiGe. During this process step the width of the NanoSheets $W_{NS}$ can be chosen by modulating the width of the spacer itself. The latter can be changed by a different deposition of the Spacer Oxide or by a different anisotropic etching, which causes a different thickness of the spacer which patterns the stacked fin. At this point, to provide isolation to neighboring devices and avoid parasitic channels the Shallow Trench Isolation (STI) technique is done: as a first step, a shallow etching is done to create the wanted trenches, which are subsequently filled by a CVD of TetraEthyl OrthoSilicate (TEOS) material, an organic insulator with properties similar to the ones of $SiO_2$. Lastly, an anisotropic etching to remove unwanted TEOS is done, and a CMP to planarize the structure ( create a planar surface at the top of the device). The design of the TEOS layers determines, in particular, the Fin Pitch $FP$, which

is the spacing between two different Si / SiGe superlattices.
For bulk devices, additional implantations are needed to avoid parasitic channels at the bottom of the device by creating an additional energy barrier to block the extension of the depletion regions. This implantation is called the Punch-Through Stop Layer (PTSL), located on the Silicon below the stacked channels and between two insulating trenches. This additional implantation is not needed for SOI substrates, which are fabricated to provide isolation to the substrate, but instead are more technologically expensive than bulk ones.

(d) At this point, the Dummy Gate fabrication is done, which is a placeholder structure for the actual gate made of High-K dielectric and metal gate stacks: a CVD of PolySilicon is performed, and then the unnecessary one is etched by using a negative mask and a photoresist layer. Then, the Source/Drain Extensions (or Lightly Doped Drain, LDD) implantation is done. Those implantations are located beyond the source and drain regions of the transistor, close to the channel region. The S/D Extensions allow to limit the longitudinal electric field and hence the influence of the junctions to the channel, reducing SCEs. Moreover, the device gains in reliability, since S/D extensions prevent hot carrier injection from the channel into the oxide layer, forming a trapped charge which modifies the threshold voltage. After the S/D extension implantation, to activate the dopants and smoothen the doping profile, thermal diffusion is done.

(e) To protect the S/D extensions implants from the successive ones and provide isolation to the gate contact from the Source/Drain ones the oxide walls and the spacers, are respectively fabricated: a masked anisotropic etching of the oxide layer deposited on the dummy gate and a partial etch back of the SiGe "dummy" sheets is performed to create the inner spacers, which are additional spacers (peculiar of the NS-GAAFET structure) inserted to prevent short circuits between the Source/Drain and the metals of the gate stack. Subsequently, an oxide layer is deposited to fill the void and form the oxide walls, and then a CMP is performed to planarize the device. The same step, although with a different mask, is done with a different material, silicon nitride $Si_3N_4$ to form the main and inner spacers. Then, for gate protection purposes, a deposition on it of SiOCN is done using a mask and anisotropically etching the unused part. Subsequently, an etching of the exposed Silicon sheets is done to substitute them with the new Source and Drain.

(f) At this point is possible to grow new Source/Drain structures with Silicon or by using a different material that acts as a stressor, introducing longitudinal strain in the channel to boost the mobility, improving the overall speed of the device. In this process, simulation stressors are used, in particular, Silicon Carbide SiC for n-type devices that provide tensile stress because the SiC lattice constant is lower than the Si constant $d_{SiC} = 0.534nm$ and silicon germanium for the p-type that provides compressive stress since the SiGe lattice constant is greater than the Si constant $d_{SiGe} = 0.566nm$. Moreover, the Source and Drain are raised (Raised S/D), as in standard 2D and 3D technology, being taller than the substrate to avoid as much as possible the formation of a pn junction of S/D structures with the channel, which

has opposite doping, albeit low.
The Source Drain epitaxy can be modeled by the simulator by employing a Lattice Kinetic Monte Carlo (LKMC), which is an algorithm emulating the epitaxial growth in an atomistic and statistical way, taking into account the presence of lattice defects or other imperfections and considering the atomistic interaction between the Silane gas molecules ($SiH_4$) and the Silicon lattice. [32] After their epitaxy doping is provided to the novel Source / Drain structures. In particular, the S/D are doped with a masked Ion Implantation and, subsequently, the SAlicitation (Self Aligned Silicidation) technique is applied: a layer of Titanium Ti is deposited only in the Source/Drain regions, and then a chemical reaction is activated through a high-temperature annealing process to favor the formation of the Silicon-Titanium compound, Titanium SilicideTiSi. [39].
The first Inter-Layer Dielectric 0 (ILD 0) of the fabrication is done at this point to planarize the device: a CVD of PhosphoSilicate Glass (PSG) (a fluid amorphous silicate) and a successive CMP planarization is performed. Moreover, the interlayer dielectric allows the separation of the Front End of the Line (FEOL) to the Middle End of the Line (MEOL), in particular the first metal layer M0 interconnections.

(g) The Dummy Gate removal and the Selective etching of SiGe (Channel Release) process steps are done at this point: an etching of the PolySilicon dummy gate is performed to allow the High-k Metal Gate technological steps (HKMG) and, subsequently, an etching of the dummy gate oxide is done to expose the Si/SiGe Superlattice. The remaining part of the SiGe which was not etched during the partial etch back done before is now completely etched by using different chemical or mechanical methods. The latte process should have a high selectivity, avoiding consuming the pure Silicon NanoSheets, that could be rounded or damaged. The more the molar fraction and, hence, the percentage of Germanium in the dummy sheets, the faster and more selective this process step is. [40]

(h) At this point the $SiO_2$ Interfacial Layer (IL) is fabricated: a thin buffer layer made of Oxide is deposited to smooth down the lattice mismatch of the silicon sheet and the high-k insulator to reduce defects in the lattice and mechanical stresses. A successive etching is done using the negative gate mask.
After the Interfacial Layer the High-k dielectric layer is then deposited: an atomic layer deposition (ALD) is performed to have a very thin layer of $HfO_2$, which has a very high relative permittivity to increase the control of the channel by the gate. The use of high-k dielectrics allows for a thicker physical dielectric layer while maintaining the same channel control (gate capacitance) value instead of a thinner standard gate dielectric made in $SiO_2$. This is done to limit the direct Gate tunneling phenomena which may happen due to the thin layer of the dielectric stack but also due to the high electric field (Fowler-Nordheim).
After high K deposition, the metal stack follows, with the Metal Interdiffusion Gate (MIG) technology, which is a series of thin layer depositions to have the right threshold tuning for both p-type and n-type devices, since the flat band voltage $V_{FB}$ depends on the metal work function $q\Phi_M$ respectively, needing a low gap metal such as titanium and a high gap metal such as Nickel or Aluminum. Firstly a deposition

of a thin TiN Titanium nitride (TiN) is applied to n- and p-type devices to modify the threshold voltage, and then a deposition of TaN Tantalum Nitride was used to be used as an Etch Stop Layer, to avoid the diffusion of the Aluminum, which will be further deposited. At this point another layer of TiN is done for the threshold tuning of the p-type device, hence the layer is etched by using a mask on the n-type device. Then deposition of TiAl is done for the adjustment of the threshold of the n-type device: the Aluminum will diffuse until the Hi-K dielectric in the n-type device, while in the p-type it will be blocked by the TaN layer. Afterward, the deposition of the contact metal, Tungsten (which is a midgap metal), follows: the void that has been caused by the dummy gate etching is filled with Tungsten material W, which is a very low resistivity material, providing good gate contact and hence low contact resistivity).

(i) To avoid short circuits between the Gate and the S/D contacts the Self Aligned Contact (SAC) technology is performed at this point [41]: a partial etch back of the tungsten filler is done to have a slight recess of the gate and a successive deposition of Silicon Nitride $Si_3N_4$ on the contact is done to protect the gate and etched using CMP to create the usual planar surface. Subsequently, the Source and Drain contacts are fabricated by an anisotropic etching using a mask that removes the PSG only in the region of interest and, then, a filler deposition of the tungsten contact with a successive CMP to planarize. This process step is crucial for yield enhancement, and it was a key enabling process step for many ICs.
Lastly, all the contacts have been defined to run the Physical Simulator of the TCAD. After having done the FEOL, hence the transistor itself, successive layers of Inter-Layer Dielectric (ILD) and metal layers can be deposited to form the circuits (cells) and the various routings that are present to connect the various cells and blocks of the IC, using various techniques such as the Lift-Off or the Damascene ones. This part is not strictly related to the device fabrication.

## 3.3 SDevice Tool

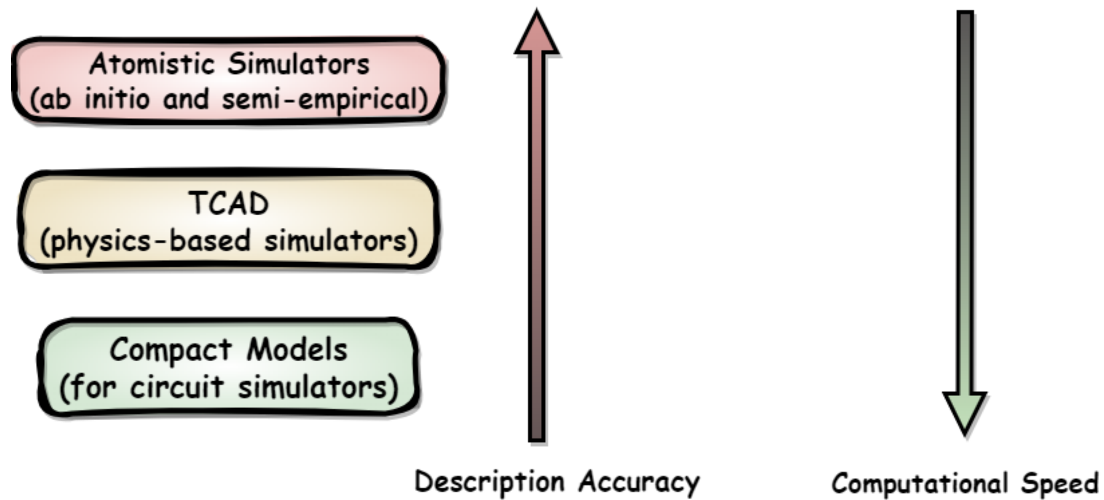


Figure 3.5. Atomistic, Physics-based and Compact Models overview

TCAD simulators allow the simulation of several devices by employing physics-based simulations, which are representations based on quite accurate and complex mathematical models, describing in detail the intrinsic behavior of the device physics. Only atomistic models, based on a more rigorous quantum-mechanical treatment, may reach a further degree of precision in the physical description. Atomistic simulators may employ ab initio methods, which rely only on quantum mechanics-based equations without using experimental data or parameters, hence predicting the properties of the given material from scratch. An example of an ab initio method is the Density Functional Theory (DFT), which can be used with different basis sets, such as the Linear Combination of Atomic Orbitals (LCAO) basis or the Plane Wave one.
Nevertheless, the computational burden of the ab initio methods could be unacceptable especially for bigger and more complex structures having many atoms, hence simpler atomistic simulators may employ different algorithms such as semi-empirical models or force field-based ones, which, instead, are less general since they employ different approximation such as the deterministic Newtonian physics ones.

Physics-based models, such as Sentaurus Sdevice, solve electrostatic and transport properties to analyze the static distribution of potential and electric field in a device being at thermal equilibrium, and the motion of the carriers if an external force is applied, outside of equilibrium. In particular, the electrostatic problem is solved by Maxwell's equation, which in the quasi-static (slow varying) approximation becomes the Poisson equation which, starting from a net charge distribution $\rho$ finds the electrostatic potential $\phi$. The transport problem instead provides the current at the terminal of the device. The most used model used for transport is the Drift-Diffusion (DD) set of equations, which consists of two continuity equations and the Poisson equation:

$$\begin{cases} \dfrac{\partial n}{\partial t} = \dfrac{1}{q}\dfrac{\partial J_n}{\partial x} - U_n \\ \dfrac{\partial p}{\partial t} = -\dfrac{1}{q}\dfrac{\partial J_p}{\partial x} - U_p \\ Jn = n\mu_n \dfrac{\partial E_{Fn}}{\partial x} \\ Jp = p\mu_p \dfrac{\partial E_{Fp}}{\partial x} \\ \nabla^2 \varphi = \dfrac{\rho}{\epsilon} \end{cases}$$

Other simulators may employ more accurate (albeit computationally heavier) transport models, called semiclassical, usually based on the Boltzmann Transport Equation (BTE). BTE, in particular, is an energy conservation PDE that describes the statistical behavior of one or a system of particles outside of equilibrium, giving the probability of finding a particle having a certain velocity in a given spatial position, but still using Newton's deterministic mechanics. The BTE can be solved directly by using various ways such as Monte Carlo simulations, or it can have an approximate solution expanding the solution into statistical moments (such as mean or variance) which give further information such as carrier distribution, current density or average energy (Method of the Moments). Moreover, by truncating the expansion up to a certain moment it is possible to select the desired accuracy of the model. This is a more general framework since the Drift Diffusion model itself can be seen, in fact, as a Method of the Moments of order 0, while transport models employing higher order moments are usually referred to as the Hydrodynamic Model (HD) and the Energy Balance (EB) one, allowing to incorporate more abrupt changes in the potential and other features.

To solve the Poisson equation, which is a Partial Differential Equation (PDE), TCAD solvers such as Sentaurus SDevice provide firstly a discretization of the domain to be simulated, for example using the Finite Element Method (FEM). In particular, the FEM classical formulation uses a set of basis functions such as Lagrange Interpolant Polynomials (of order 0) allowing the transformation of the differential equations, in which the unknowns are functions, into an algebraic problem in which, instead, the unknowns are coefficients:

$$\{r\} = [E]\{\varphi\} - [M]\{\rho\}$$

Where the matrices $E$ and $M$ are assembled depending on two adjacent nodes and the mesh length, and $r$ is the vector of the residuals. Subsequently, to solve the nonlinear problem it is possible to employ the classical or the generalized Newton-Rhapson method or similar methods derived from the Newton-Rhapson one (such as the Bank-Rose algorithm) to solve numerically one or a system nonlinear equations $f(x) = 0$, by using an initial guess and then a first-order Taylor expansion to linearize the system around the initial guess. After having solved the first linearized version of the problem the solution is updated and re-linearized. The size of the system depends on the number of mesh nodes employed in the simulation domain, except for the two points at the edges, which are the Boundary Conditions points and in which the potential should be fixed ( null at thermal equilibrium), which are solved with the standard 1D Newton method.

$$\begin{bmatrix} 1 & 0 & \cdots & \cdots & \cdots & 0 \\ \frac{\partial r_1}{\partial \phi_1} & \frac{\partial r_1}{\partial \phi_2} & \frac{\partial r_2}{\partial \phi_3} & \cdots & \cdots & 0 \\ 0 & \frac{\partial r_2}{\partial \phi_1} & \frac{\partial r_2}{\partial \phi_2} & \frac{\partial r_2}{\partial \phi_3} & \cdots & 0 \\ 0 & 0 & \ddots & \ddots & \ddots & 0 \\ 0 & 0 & 0 & 0 & \cdots & 1 \end{bmatrix} \begin{bmatrix} \Delta\varphi_1^{k+1} \\ \Delta\varphi_2^{k+1} \\ \Delta\varphi_3^{k+1} \\ \vdots \\ \Delta\varphi_N^{k+1} \end{bmatrix} = \begin{bmatrix} 0 \\ r_2^{k+1} \\ r_3^{k+1} \\ \vdots \\ 0 \end{bmatrix}$$

At each step of the Jacobian, the matrix containing the partial derivatives (a tridiagonal matrix since the basis set is not orthogonal) is evaluated, subsequently, the correction in the solution $\Delta x$ is calculated and, then, the solution is updated for a new iteration, which could be done if the norm of the residual vector is higher than a used define a threshold, otherwise, the algorithm considers the convergence reached and stops.

Moreover, due to the reaching of very small dimensions Quantum Mechanical effects are starting to appear in large-scale devices, hence, for this reason, the TCAD solvers allow the insertion of quantum corrections in the numerical solution of the equation. This could be done by using different models, such as the density gradient [42]. The Density Gradient (DG) is, in fact, a more general transport model concerning the classical drift-diffusion implemented in standard Physical simulators since it allows the incorporation of lowest-order quantum effects such as quantum confinement, direct gate tunneling (gate current phenomena), and band-to-band tunneling (BTBT) and it is usually coupled with the Poisson equation solver. The density gradient occupies an intermediate position between the heuristic quantum corrections (done for fitting purposes) and full descriptions of the quantum mechanical behavior ( fully solving Schroedinger equation), and it consists of adding a further dependence of the state equations of electrons and holes on the gradients

of their densities, not only on the densities (as in the drift-diffusion). [43] [44]

$$n = N_c F_{1/2}\left(\frac{E_{fn} - Ec - V_n^{DG}}{k_B T}\right)$$

$$p = N_v F_{-1/2}\left(\frac{E_{fp} - Ev - V_p^{DG}}{k_B T}\right)$$

where the effective Bohm-Wigner quantum potentials are, in the Boltzmann approximation: [45]

$$V_n^{DG} = -\frac{\hbar^2}{8m_{eff,n}}\nabla^2 ln\left(\frac{n}{n_{ref}}\right)$$

$$V_p^{DG} = \frac{\hbar^2}{8m_{eff,p}}\nabla^2 ln\left(\frac{p}{p_{ref}}\right)$$

## 3.4 Derived FOM

From the device-level simulations, it is possible to retrieve the Drain Current and hence the output and the trans-characteristic of the device, from which it is possible to directly derive the $I_{ON}$ the $I_{OFF}$ values (and their ratio) and to compute indirectly the most used device FOM such as the sub-threshold swing $SS$, the threshold voltage $V_{th}$ and the Drain Induced Barrier Lowering $DIBL$ parameter. In particular the $SS$ has been evaluated as the difference of two $V_{GS}$ distant by 2 decades in the sub-threshold regime:

$$SS = \frac{V_{GS,sub1} - V_{GS,sub2}}{2\ \ decades}$$

the threshold voltage has been evaluated using the double derivative method, being the maximum of the trans-conductance derivative concerning the gate voltage:

$$V_{th} = max\left(\frac{\partial gm}{\partial V_{GS}}\right) = max\left(\frac{\partial^2 I_D}{\partial V_{GS}^2}\right)$$

Lastly, the DIBL parameter has been evaluated by running an additional simulation, but this time for a low $V_{D,low} = 0.05V = 50mV$, computing the threshold voltage for the latter simulation and by computing the difference of the two obtained threshold voltages:

$$DIBL = \frac{V_{th}^{V_{DD}} - V_{th}^{V_{D,low}}}{V_{DD} - V_{D,low}}$$

# Chapter 4

# Process and Device-level Simulations

## 4.1 Process Simulation of the NS-GAAFET

In this section, a process simulation of an NS-GAAFET of both n-type and p-type has been done by using Synopsis SProcess. An actual experimental process has been tried to be emulated with the process simulation, to highlight the differences between the two. The relevant parameters of the NS-GAAFET reported in 4.1, are taken or retrieved from an experimental article [34] from IBM®, which is a report of one of the first experimental demonstrations of the fabrication of actual NS-GAAFET devices.
In the following, the differences between the process simulation and the actual experimental process have been highlighted and the NS-GAAFET process differences from the FinFET one are also mentioned. Both n and p-type stacked NanoSheet-GAAFET fabrication processes have been simulated. The complementary p-type fabrication is, in fact, very similar to the n-type one but has opposite doping in the various implantations and different channel stressors for the growth of the Source/Drain structures.

| Parameters of fabricated NS-GAAFET device | | |
|---|---|---|
| Parameter | Description | Value |
| $N_{NS}$ | Number of NanoSheets | 3 |
| $W_{NS}$ | NanoSheets Width | 30 nm |
| $T_{NS}$ | NanoSheets Thickness | 5 nm |
| $T_{SP}$ | Spacing between NanoSheets | 10 nm |
| $L_{ch}$ | Channel length | 12 nm |
| $L_{S/D}$ | Source/Drain Length | 12 nm |
| $L_{sp}$ | Spacer Length | 6 nm |
| $CPP$ | Contact Poly Pitch | 48 nm |
| $L_{STI}$ | STI Lenght | 30 nm |
| $H_{STI}$ | STI Height | 20 nm |
| $FP$ | Fin Pitch | 60 nm |
| $T_{IL}$ | Interfacial Layer Thickness | 1.8 nm |
| $T_{HfO2}$ | Hi-K dielectric Thickness | 2.56 nm |
| $EOT$ | Equivalent Oxide Thickness | 0.4 nm |
| $T_{TiN}$ | Thickness of the TiN layers | 0.7nm |
| $T_{TaN}$ | Thickness of the TaN layer | 0.7nm |
| $T_{TiAl}$ | Thickness of the TiAl layer | 2nm |
| $N_{SDE}$ | Doping of S/D Extensions | $10^{17}$ |
| $N_{PTSL}$ | Doping of PTS Layer | $10^{17}$ |
| $N_{SD}$ | Doping of Source/Drain | $10^{20}$ |
| $N_{ch}$ | Doping of the channel | $10^{16}$ |

The reference parameters are reported in table 4.1, where the Contact Poly Pitch ( CPP) is the sum of the channel length $L_{CH}$ and two times the S/D length $L_{SD}$ and the spacer length $L_{Spacer}$, while the Fin Pitch (FP) is the sum of the NanoSheet Width $W_{NS}$ and the Shallow Trench Insulator width $W_{STI}$.
Moreover, the doping values are taken from classical simulations, since they were not reported in the article [34].

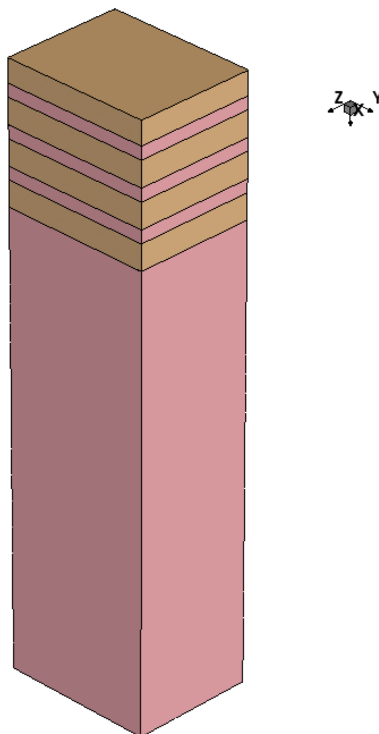


Figure 4.1. Si /SiGe SuperLattice growth.

The SuperLattice growth has been modeled in the TCAD as a deposition (in figure 4.1) and results match with the TEM photograph (a) of [34] even if experimental processes consist of a Molecular Beam Epitaxy (MBE) or a Low-Pressure Chemical Vapour deposition (LP-CVD). In real processes, the probability of the presence of defects in the periodicity of the lattice, such as point defects (1D), dislocations, and grains (2D) or volume defects (3D) in the lattice structure, is non-null.
Point defects can be of various types, such as vacancies, interstitial, self-interstitial, or substitutional. In particular, in the growth of a SuperLattice, a diffusion of the different atoms may happen (Ge in the Si layer or vice versa) causing interstitial or substitutional defects. All those phenomena could be taken into account by a proper atomistic simulator which can also provide a more accurate computation of the strain due to the lattice mismatch of the two layers.[46]

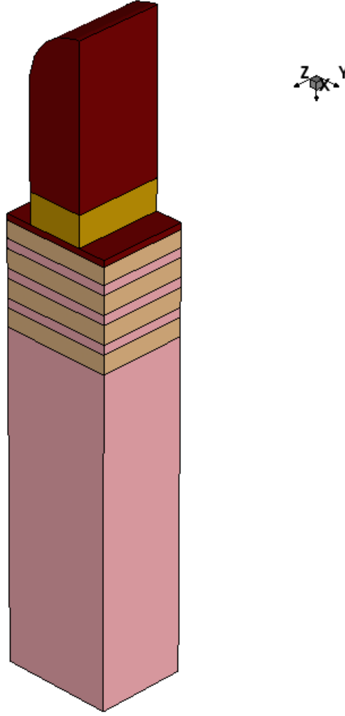


Figure 4.2. Superlattice Fin patterning by Sidewall Image Transfer(SIT)

The Fin Formation using the SIT (Sidewall Image Transfer), also called Self Aligned Double Patterning (SADP), has been done subsequently. It is possible to see that the process simulation (in figure 4.2) matches the experimental process visible in the (b) figure of [34], where a series of anisotropic etching steps have been done to pattern the SuperLattice to have a fin shape with alternate layers of Si and SiGe. However, the process simulation models the result as a rectangular fin cross-section, while in the experimental process, the actual etching step may cause the fin to have a trapezoidal cross-section, scalloping the exposed top part of the fin, causing a dependence on the fin height in the effective width $W_{eff}$ of the device.

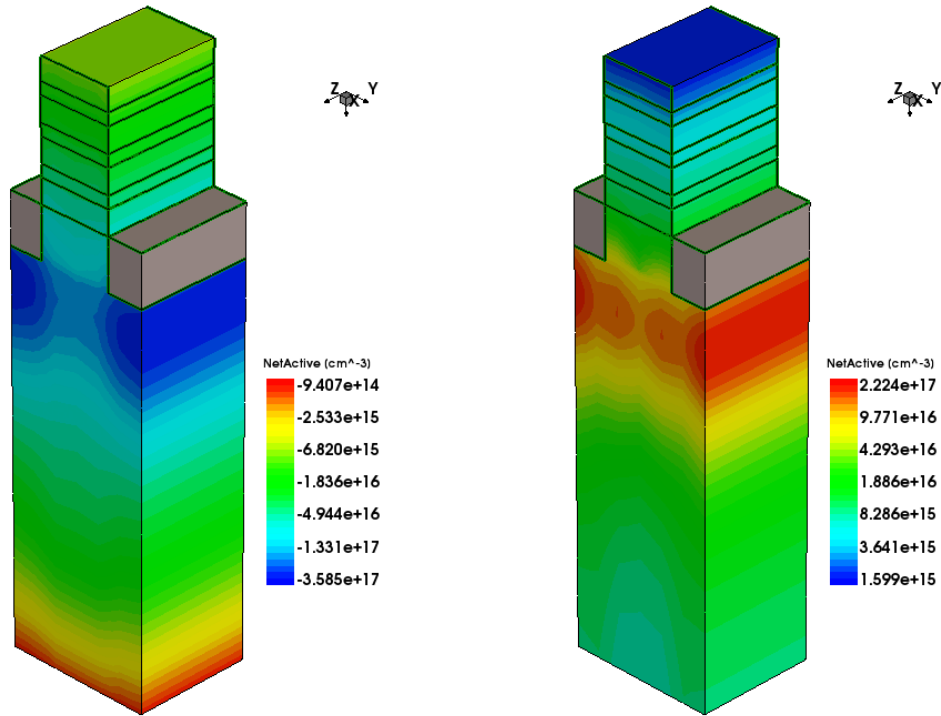


Figure 4.3. STI fabrication and PTSL implantation

At this point, the Shallow Trench Insulation (STI) step has been done (figure 4.3). It is possible to observe that both the process simulation and the experimental process in the TEM photograph (c) of [34] have similar results, even if in the experimental TEM photograph the trenches are deeper in the substrate due to an excessive etching step. Being a bulk device the Punch Through Stop Layer (PTSL) doping has been also done in the process simulation, while this step is not visible in the TEM photograph of the experimental process. Moreover, in the simulation, the PTSL implantations have been done deeply into the substrate since diffusion steps cause the dopants to rise into the channels, which should be as intrinsic as possible to avoid channel mobility degradation. In particular, the Punch Through Stop layer has n-type implantations doped with donors (Phosphorus) while the Source/Drain Extensions (LDD) and the epitaxially grown Source/Drain doping are p-type implantations (Boron). Moreover, the diffusivity constants for donors and acceptors are different, hence the process steps involving thermal processes such as diffusion or annealing need to be re-calibrated to give acceptable results.

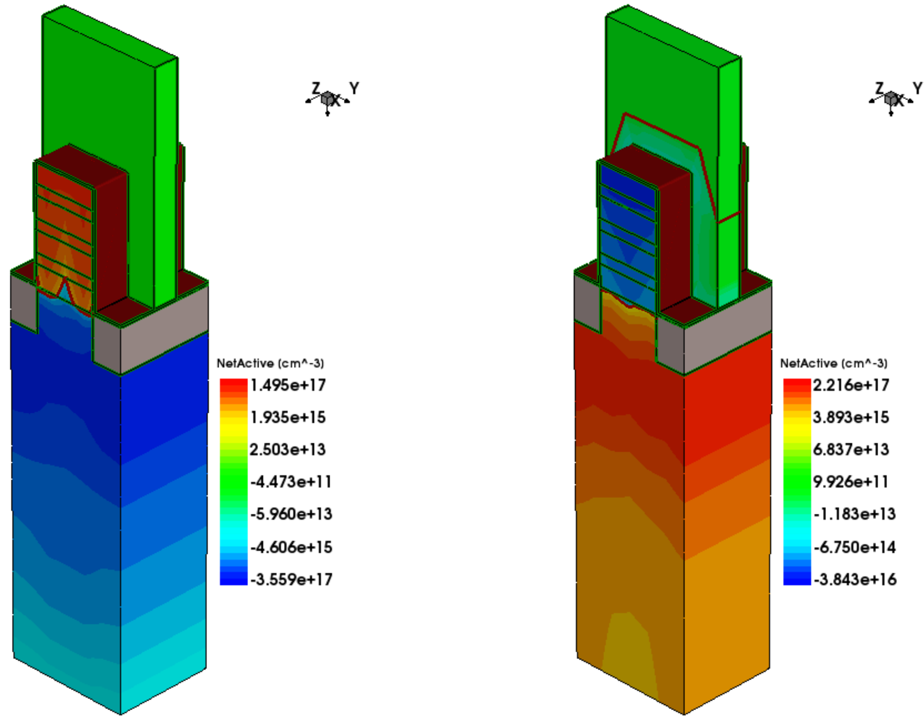


Figure 4.4. Dummy gate fabrication and Source/Drain extensions

The Dummy Gate has been fabricated at this stage, followed by the implantation of the Source/ Drain (S/D) Extensions. It is possible to see that both the process simulation (in figure 4.4) and the experimental process in [34] (TEM photograph (d) ) have analogous results. The dummy gate is fabricated with a deposition and etching of Polysilicon, as in the experiment. The S/D Extensions implantation is, instead, more cumbersome for both the simulation and the experimental process since the doping of the silicon channels is not uniform in both cases since , in fact, the dopant density variability is high and, moreover, increases for taller superlattices. Moreover, for bulk devices, the S/D extension implantation should not reach the bottom of the substrate to avoid the formation of spurious junctions causing leakages.

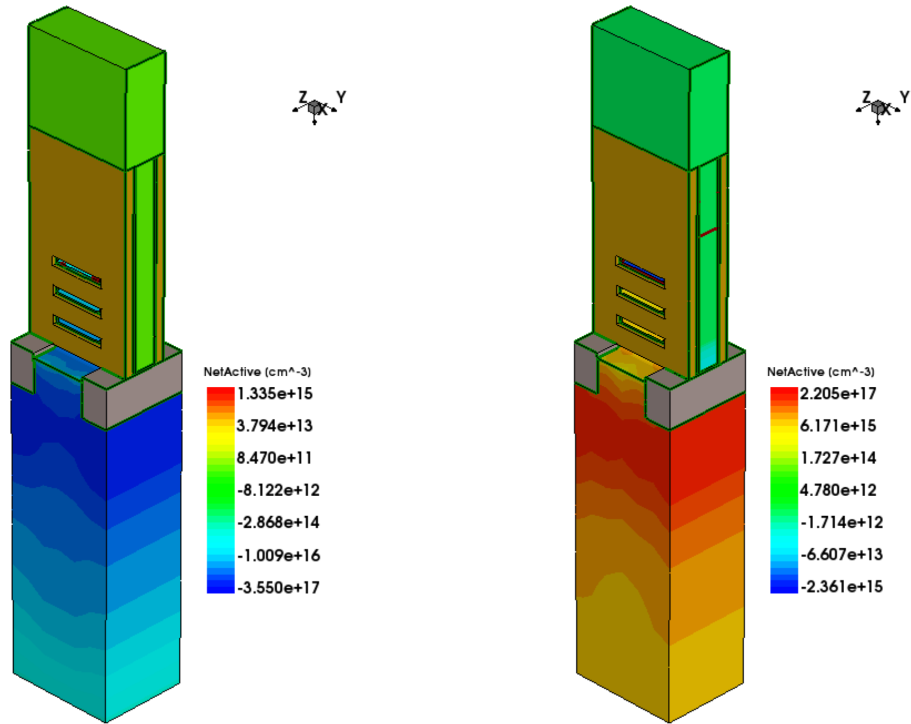


Figure 4.5. Spacer fabrication and S/D etching

The fabrication of the main spacers and the inner spacers (between the sheets) is done at this point (figure 4.5). To form inner spacers, which prevent short circuits between the S / D and the gate stack, a partial etching of the SiGe layers is done; furthermore, it is possible to see from the TEM photograph (e) of [34] the presence of a SiOCN capping to protect the gate. While in the process simulation, the recess of the SiGe layers is done with an etching having an ideal behavior, in the experimental process in [34] (TEM photograph (e) ) it is possible to see an interaction of the etchant medium with the Si channels too, which are slightly recessed and rounded where the etchant has been applied. In the actual process, the selective etching(which can be wet or dry) should be as chemically selective as possible, avoiding the interaction with the silicon layers.[40]. Moreover, in the experiment, the etching step is not perfectly anisotropic, causing the inner spacers to be not ideally squared and all identical to each other, but, instead, presenting concave or convex inner faces.

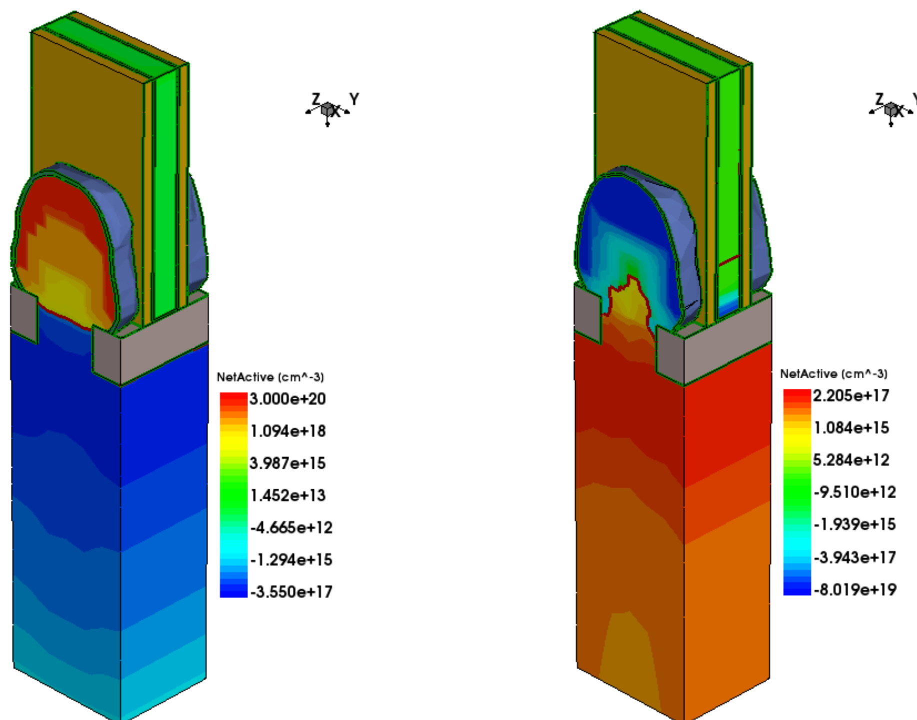


Figure 4.6. Source/Drain epitaxy, doping, and Silicidation

The growth of new Source and Drain structures has been done at this point (figure 4.6). In the process simulation, an atomistic simulation of the process has been performed using lattice kinetic Monte Carlo (LKMC), as previously discussed, by doing an epitaxial growth of Silicon Carbide SiC as a channel stressor for the n-type and thermal diffusion to crystallize the system. The result of the LKMC has a shape that may resemble the one obtained in the experimental process in TEM photograph (f) of [34], which has a diamond shape, as is possible from the TEM photograph (f) and Figure 16 of [34]. Then, silicidation was done, and in particular, in both the simulation and experiment, the silicide layer was wrapped around the grown Source and Drain to reduce the contact resistance, instead of being present only on the top surface of the source/drain (wrap-around contact).

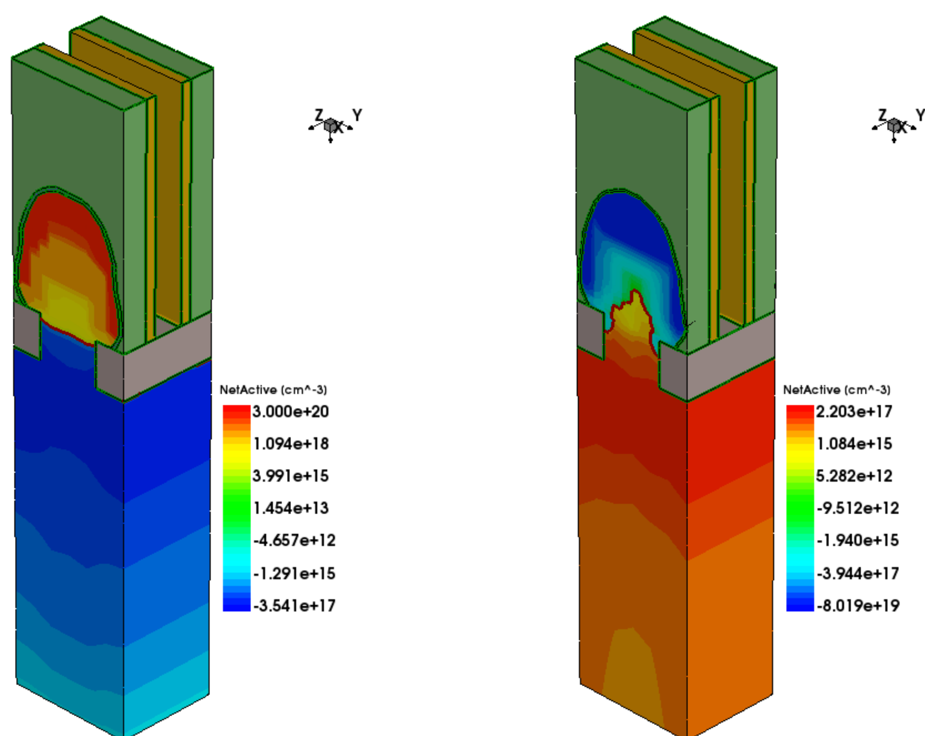


Figure 4.7. Etching of the SiGe sacrificial layers

The successive process step is the channel release, which is actuated by removing the dummy gate and by doing a selective etching of the sacrificial SiGe layers (figure 4.7). In the process simulation, this step is modeled by doing an etching of the dummy gate and by stripping off the sacrificial layers, while in the experimental process visible in TEM photograph (g) of [34], a selective wet or dry etching is done, similarly to in the partial etch back of the sacrificial layers done for the inner space creation, but this time with an increased dose to completely remove the SiGe. The etchants used for this purpose may, anyway, interact with the channels, causing an unwanted over-etching of Silicon, rounding the NanoSheets. [40]

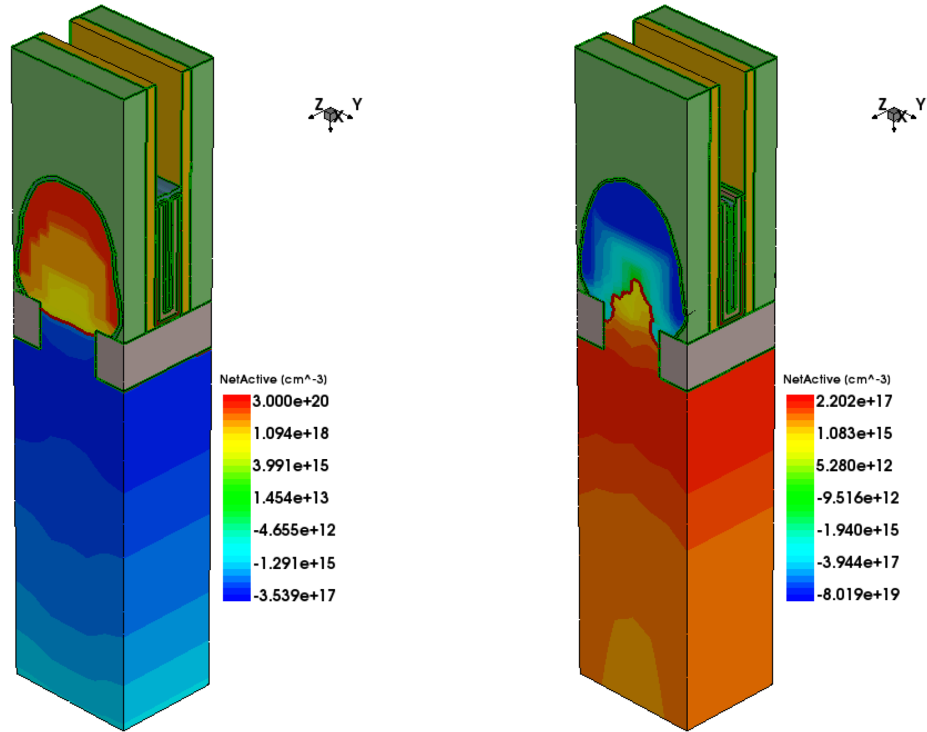


Figure 4.8. Replaced Metal Gate (RMG). Interfacial layer, Hi-K dielectric, and MIG depositions.

At this point, the Replaced Metal Gate (RMG) series of process steps is done (figure 4.8). In the process simulation, the deposition of the interfacial layer ( the oxide buffer layer of the gate), the Hi-K dielectric, and the MIG process have been done. In the experimental process (TEM photograph (h) of [34]) instead, the deposition of very thin layers on the atomic scale has been done using a different technique, Atomic Layer Deposition (ALD), which uses specific chemical processes and reactions to control the precision on the nanometric scale. Moreover, in the experimental process only two metals have been used, one for the n-type device threshold tuning and the other one for the p-metal threshold tuning, as it is possible to see in figure (h) of the article [34].

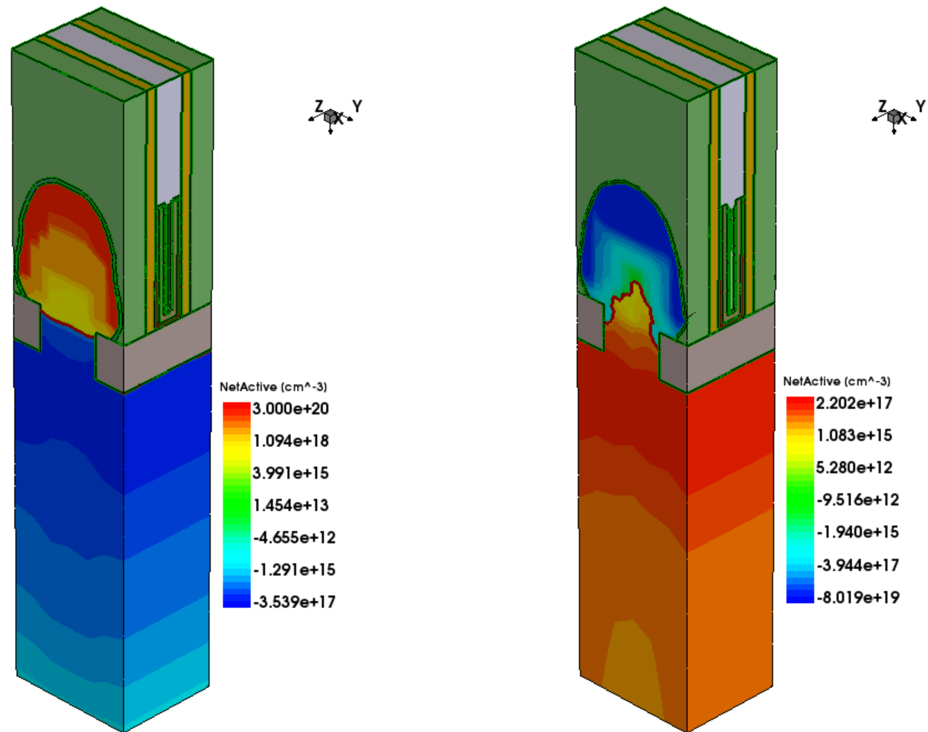


Figure 4.9. Metal filling and Self-Aligned Contact

Then the void left by the Metal Gate Last technology has been filled with a metal with low resistivity such as Tungsten to form the contact and planarize the device ( figure 4.9). Then the Self-Aligned Contact (SAC) technology has been applied to avoid short circuits between the gate contact and the Source/Drain ones. In the experimental process, in TEM photograph (i) of [34], a similar result has been obtained.

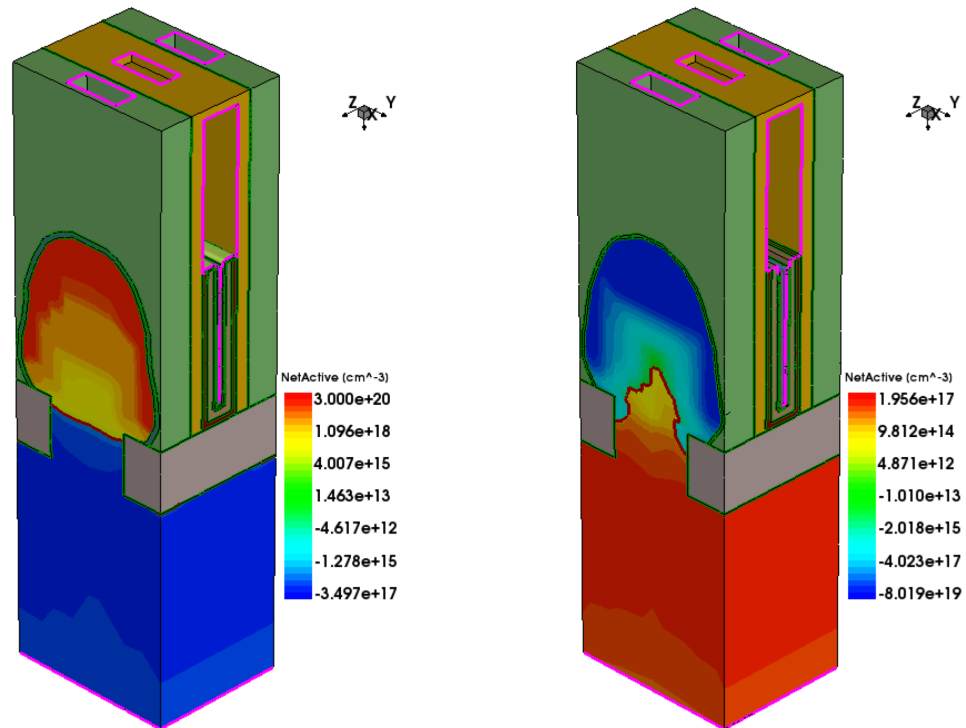


Figure 4.10. Contact definition for the simulations

Lastly, in the process simulation, a sharper mesh (for the successive electrical simulations) has been created and contacts have been defined (figure 4.10). The bottom part of the substrate has been neglected by cutting off it to reduce the computational burden of the device-level simulations.

## 4.2 Physics-Based Simulations

### 4.2.1 DC Trans-characteristic

After having simulated the fabrication process, physics-based device simulations have been done by using the Synopsis Sdevice tool to simulate the electrical characteristics of the fabricated devices and to observe the inner physical quantities inside the device.
Some FOM have been, then, retrieved from the simulations and have been compared with the ones presented by the experimental article [34], in particular the ON/OFF current ratio (or Current Extinction Ratio), the Subthreshold Swing (SS) and the Drain Induced Barrier Lowering (DIBL) parameters. The trans-characteristics obtained for the n-type are shown in figure 4.11.

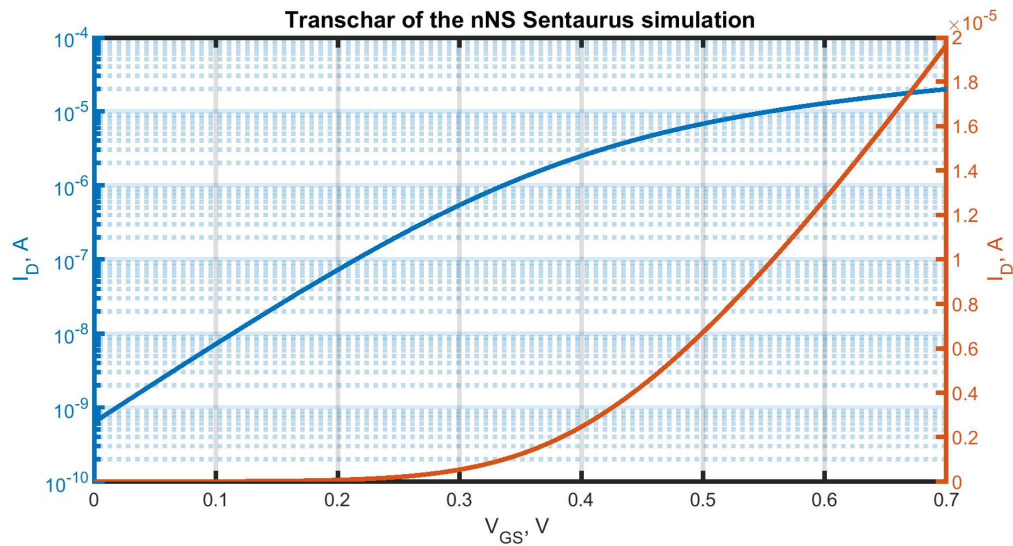


Figure 4.11. Fabricated n-type NS-GAAFET trans-characteristic, linear and logarithmic scale

Moreover, the exact value of the current for the trans-characteristic of the experimental process was not available (for commercial reasons), hence a comparison between the two was done with the normalized trans-characteristic. In particular, the normalization value was chosen to be the ON current, as done by the experimental simulations in the article [34].

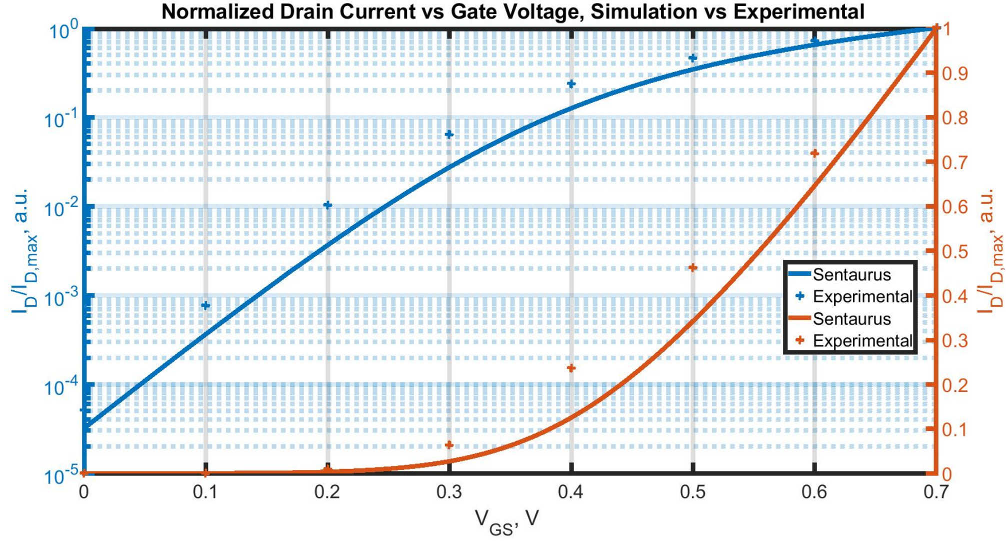


Figure 4.12. Comparison of the trans-characteristic of n-type NS-GAAFET (normalized to the ON current) of the experimental process [34] and the Sentaurus process simulation.

From figure 4.12 it can be visible that there is a slight mismatch between the two, due to the various effects present in the real process which have been discussed in the previous section. Results of the simulation and main FOMs are reported in table 4.13. The FOMs have been compared with the ones declared in the article [34].

| | $I_{ON}$ | $I_{OFF}$ | $I_{ON/OFF}$ | $SS$ | Vth | DIBL |
|---|---|---|---|---|---|---|
| Simulation | $1.965 \cdot 10^{-5}A$ | $6.263 \cdot 10^{-10}A$ | $3.137 \cdot 10^4$ | $84.2\frac{mV}{dec}$ | $0.405V$ | $38.4\frac{mV}{V}$ |
| Experimental | NDR | NDR | $1.95 \cdot 10^4$ | $83\frac{mV}{dec}$ | $0.4V$ | $30\frac{mV}{V}$ |

Table 4.1. n-type NS-GAAFET electrical parameters and FOM, simulation vs experiment

It is possible to observe that the value of the $I_{ON}$ and $I_{OFF}$ ratio obtained with the process simulation is similar to the one obtained in the experimental process, albeit the one in the simulation is slightly better. Also, the Sub-threshold swing obtained in the process simulation is similar to the one obtained in the experimental process. The overall process simulation FOMs are, hence, slightly better than the experimental ones since the latter presents many non-idealities and variations. The only parameter that has a more relevant variation is the DIBL parameter which differs in the two cases. This may depend on the choice of the Source/drain extension doping, which has been arbitrarily chosen in the process simulation since no experimental parameter was given regarding it.

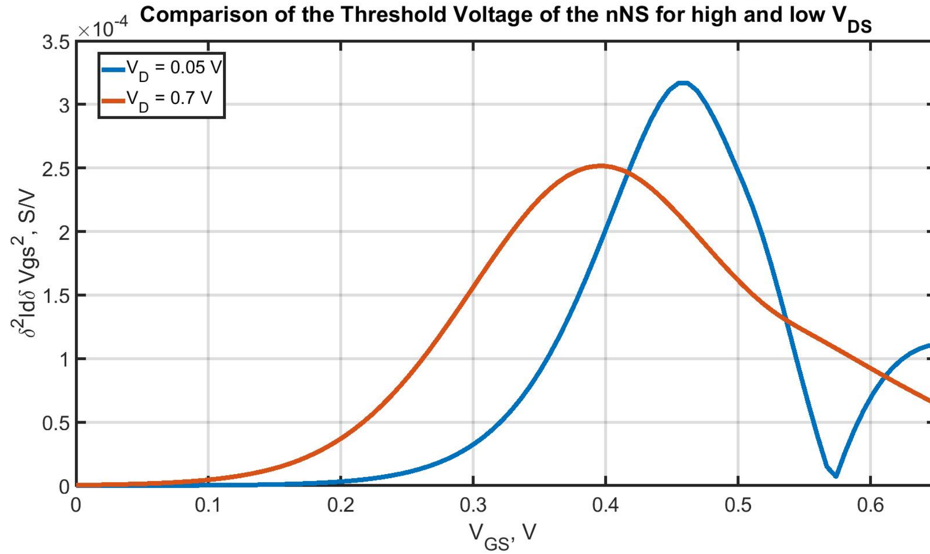


Figure 4.13. Threshold voltage retrieving of the n-type NS-GAAFET for high and low drain voltage $V_{DS}$ using double derivative method

A similar methodology has been used for the p-type device. The device-level simulation of the p-type NS-GAAFET is shown in figure 4.14 and the comparison with the experimental data of the article for the p-type has been reported in figure 4.15. .

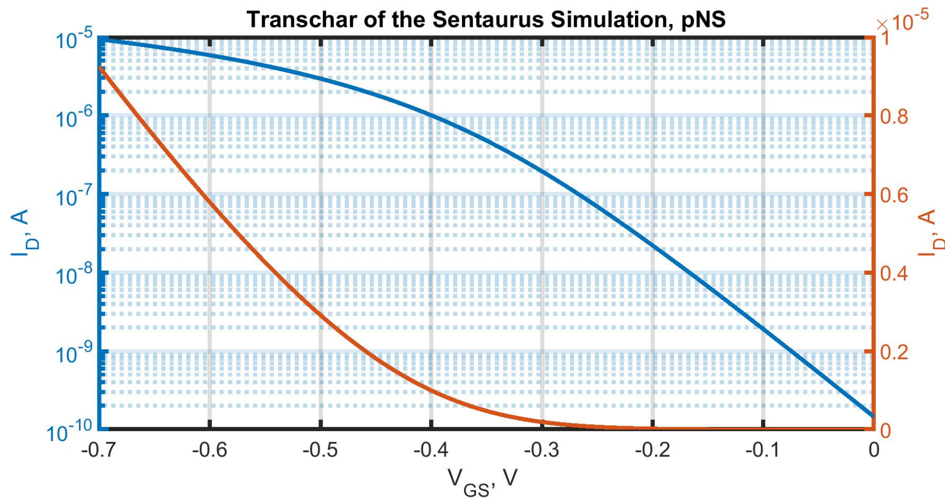


Figure 4.14. Fabricated p-type NS-GAAFET trans-characteristic, linear and logarithmic scale

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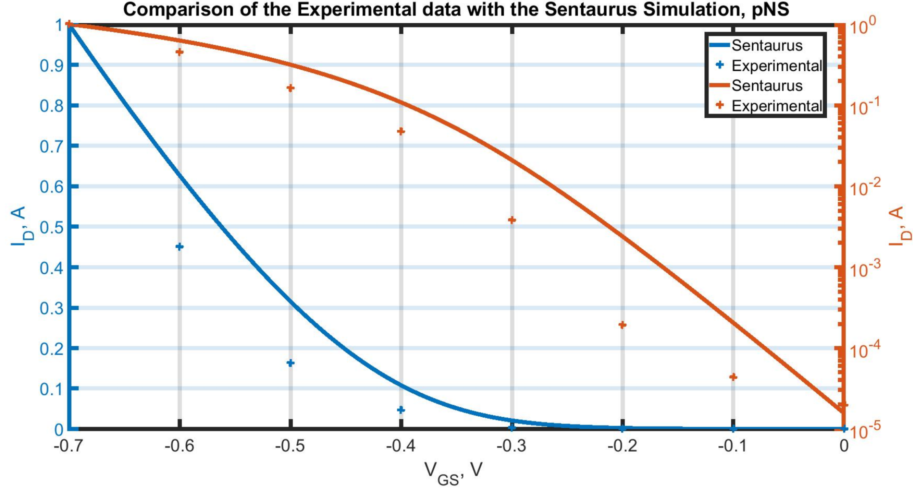



Figure 4.15. Fabricated p-type NS-GAAFET trans-characteristics, logarithmic scale

.

As it is possible to see from figure 4.15 the simulation curve is similar to the experimental data, albeit differing especially around the threshold. The results of the simulation and main FOMs for the p-type NSGAAFET are reported in table 4.2. The FOMs of the p-type NSGAAFET have been also compared with the ones of article [34].

| | $I_{ON}$ | $I_{OFF}$ | $I_{ON/OFF}$ | $SS$ | $Vth$ | $DIBL$ |
|---|---|---|---|---|---|---|
| Simulation | $1.965 \cdot 10^{-5}A$ | $6.263 \cdot 10^{-10}A$ | $6.391 \cdot 10^4$ | $91\frac{mV}{dec}$ | $-0.413V$ | $27.15\frac{mV}{V}$ |
| Experiment | NDR | NDR | $5.02 \cdot 10^4$ | $94\frac{mV}{dec}$ | $-0.4V$ | $29\frac{mV}{V}$ |

Table 4.2. p-type NS-GAAFET electrical parameters and FOM, simulation vs experiment

It is possible to observe from table 4.2 that for the p-type device the value of the $I_{ON}$ and $I_{OFF}$ ratio obtained with the process simulation is similar to the one obtained in the experimental process. Moreover, the value of the Sub-Threshold Swing is similar to the one obtained in the experimental process. Moreover, for the p-type case, the value of the DIBL parameter is similar to the one obtained in the experimental process. It is also observable that the DIBL parameter of the p-type device is smaller than the complementary one. This effect could be due to the mobility difference between the free carriers, the holes being slower in the (100) oriented silicon lattice and, hence, the overall current being lower.

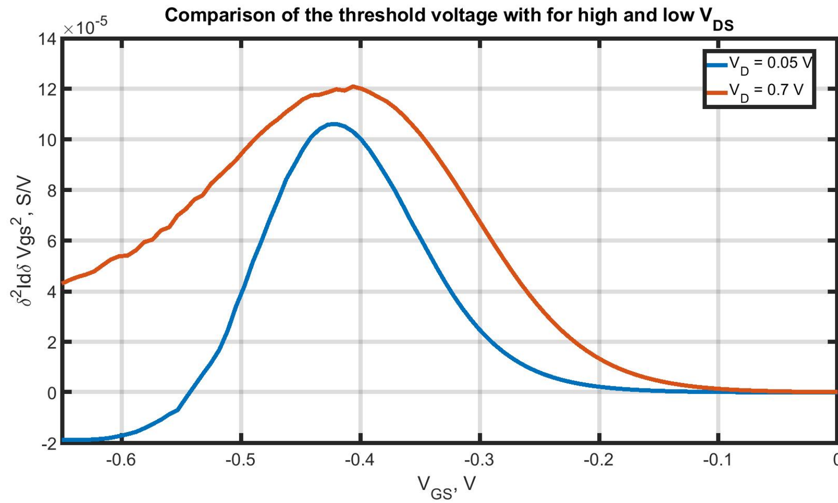



Figure 4.16. Threshold voltage retrieving of the p-type NS-GAAFET for high and low drain voltage $V_{DS}$ using double derivative method

### 4.2.2 Gate Current

Subsequently, a tunneling model through the Si / $SiO_2$ interface has been inserted into the physics section of the simulator to estimate the value of the gate current caused by the direct tunneling phenomenon. In particular, the Schenk tunneling model was used. The direct tunneling phenomenon causes a non-null gate current $I_G$, which can be visible in the following graphs reported 4.17. .

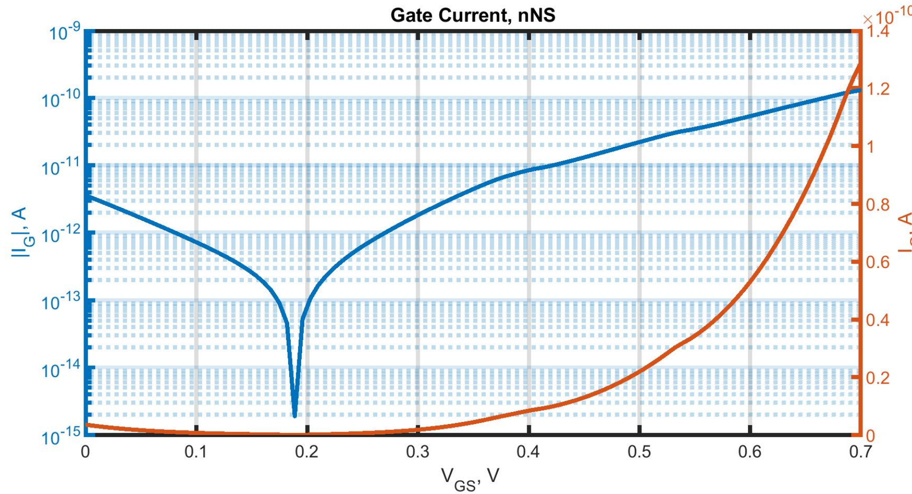



Figure 4.17. Fabricated n-type NS-GAAFET gate current considering Direct tunneling

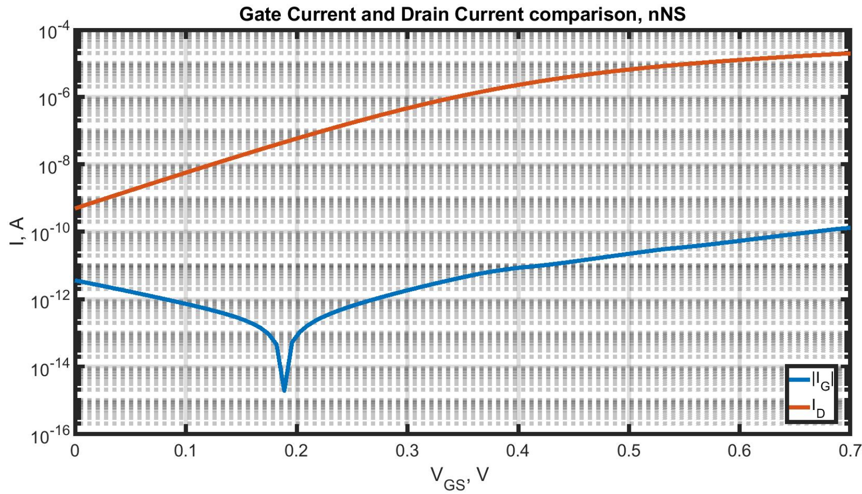



Figure 4.18. Comparison between the drain and the gate current characteristics, n-type NS-GAAFET

As it is possible to observe from figure 4.18 the gate current can be negligible for the ON behavior since the difference in magnitude between the two is significant, but can play a role in the OFF behavior, even if also in this case the gate current can still be negligible ( roughly 3 orders of magnitude) if compared to the drain current. A Gate Current FOM can be considered in 4.19, the ratio between the gate current and the drain current.

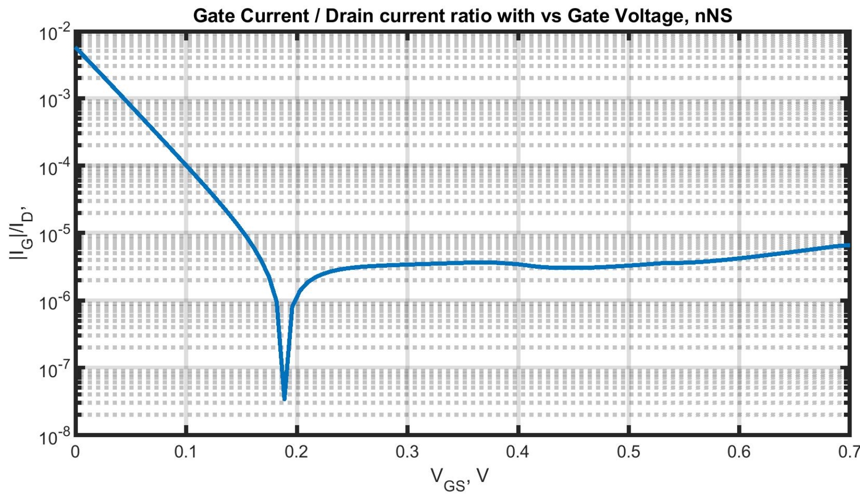



Figure 4.19. Gate current and Drain current ratio, n-type NS-GAAFET

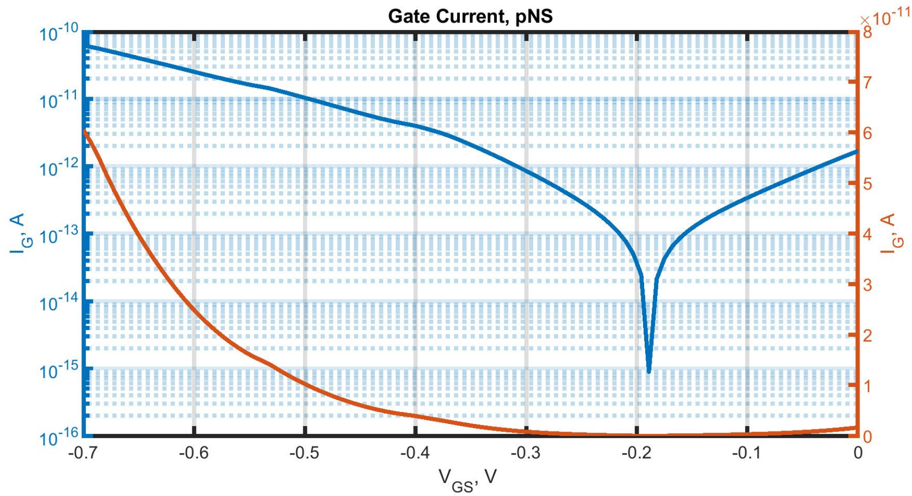



Figure 4.20. Fabricated p-type NS-GAAFET gate current considering Direct tunneling

Similar considerations can be done for the complementary p-type device, as it can be observable in figure 4.20, while in figure 4.21 the comparison between the gate and the drain current is reported. The gate current and drain current ratio is reported instead in 4.22.

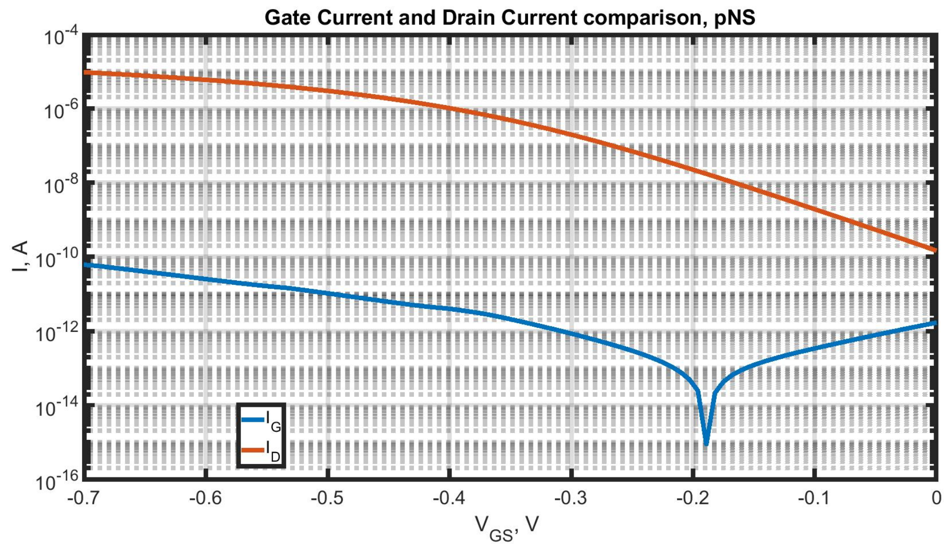



Figure 4.21. Comparison between the drain and the gate current characteristics, p-type NS-GAAFET

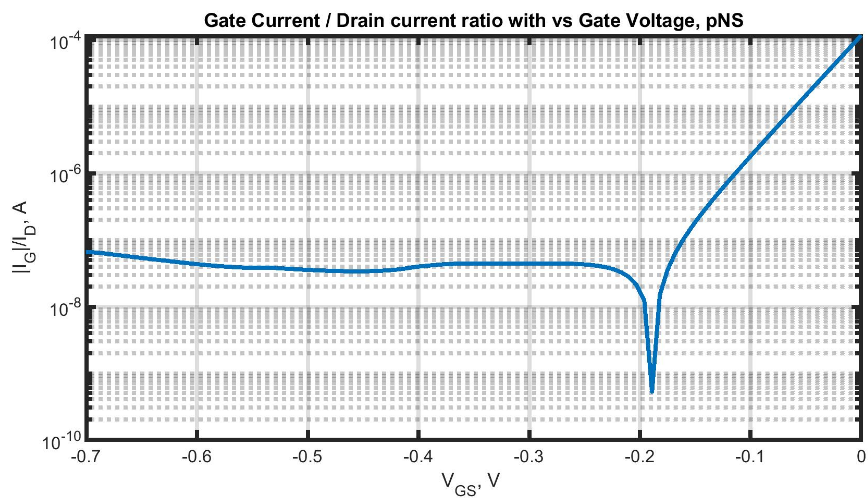



Figure 4.22. Gate current and Drain current ratio, p-type NS-GAAFET

# Chapter 5

# Matching Compact Models with Physical Models

## 5.1 BSIM-CMG modifications

This section aims to have a match between the physics-based model (used in the previous section) that gives a precise insight into the device physics by solving the Drift-Diffusion set of equations (with proper quantum corrections) with a compact model which was initially conceived for single Multi-Gate devices (BSIM-CMG, by Berkeley University) and then having a first adaptation to the NS-GAAFET FET ( BSIM-CMG-NS compact model). The BSIM-CMG-NS compact models were simulated by using the Cadence Virtuoso environment, a SPICE-like simulator tailored for IC design, in particular by using the native Cadence Spectre simulator. The original BSIM-CMG-NS model simulation was, initially, not compliant with the physics-based simulation obtained, having different results, hence some modifications in the code have been done in this part to get close to the higher description model. Having a more accurate compact model can allow for a more precise knowledge of the device's characteristics and also an improved accuracy of the analysis of circuital and topological implementations, such as logical ports or memory cells.

Firstly, the mobility parameter $U0$ of the BSIM-CMG-NS has been modified by inserting an average mobility parameter. Mobility is a local property that changes at each point of the mesh; hence an average value of it along the channel has been computed for each NanoSheet in the mean mobility parameter $U0$ of the compact model. Cuts along the NanoSheet channels have been made, as shown in Figure 5.3, and then a further cut was made at the center of it, and subsequently, the mobility along each channel has been averaged into a single value for each sheet.

$$U0_{AV} = \frac{U0_{top} + U0_{mid} + U0_{bottom}}{3} \tag{5.1}$$

Where $U0_{top}$, $U0_{mid}$, and $U0_{top}$ are the average mobilities for each Nanosheet that have been retrieved from the physics-based simulator results.

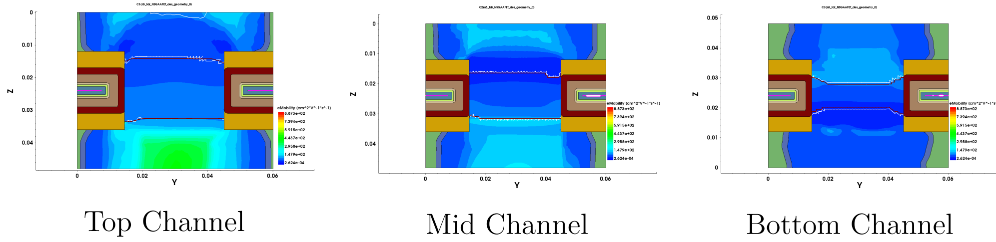



Figure 5.1. Electron mobility cuts along the n-type NanoSheet Channels

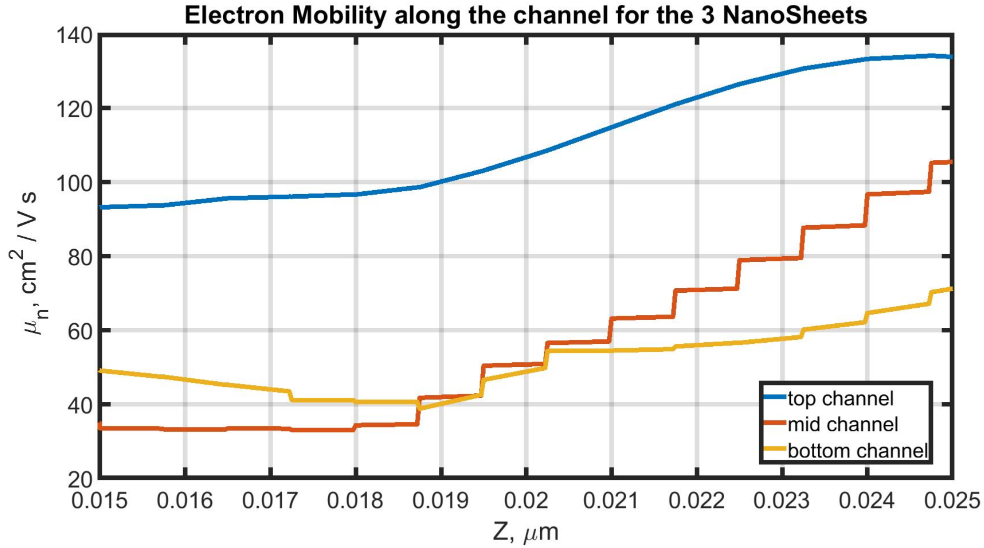
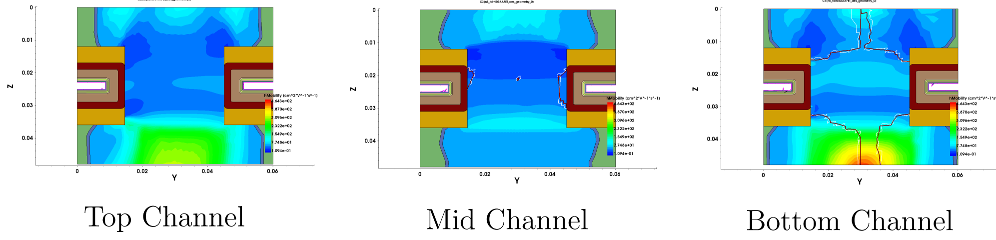



Figure 5.2. Electron mobility along each of the n-type NS-GAAFET channels, cut along the channel

From figure 5.2 it is possible to observe that the bottom channel is the one that presents less mobility, this is due to the doping dependence of this value, since scattering with

ionized impurities lowers the mobility values. Doping can decrease the value of the contact resistances but its diffusion may cause a reduction in current due to scattering mechanisms.



Top Channel Mid Channel Bottom Channel

Figure 5.3. Hole mobility cuts along the p-type NanoSheet Channels

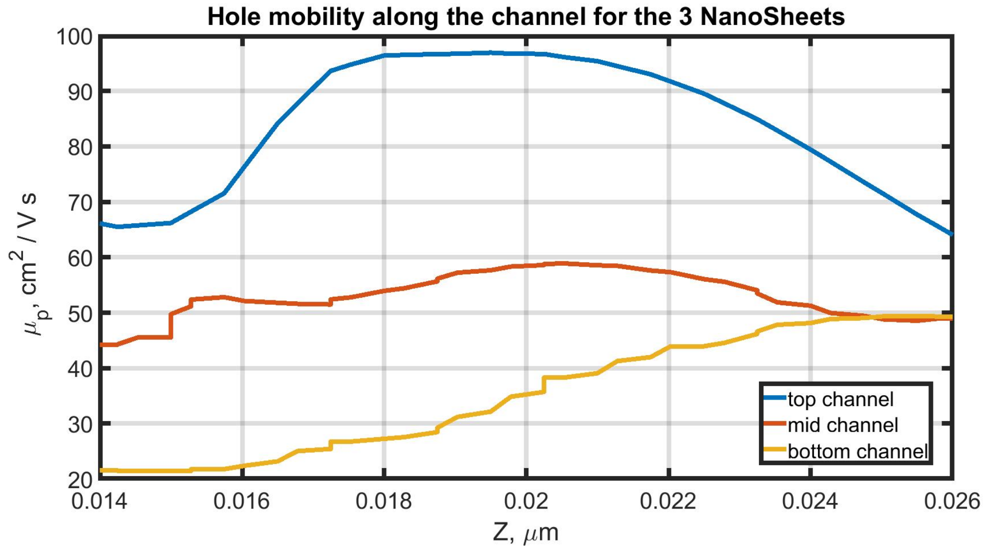



Figure 5.4. Hole mobility along each of the p-type NS-GAAFET channels, cut along the channel

A similar process has been done for p-type devices. Cuts have been made along the NanoSheets and a mean mobility along the channel has been found for each Nanosheet, which has been averaged to a single parameter $U0_{AV}$, which is a mean of the mobilities for each Nanosheet. Moreover, it is possible to notice from the physical simulations that the mobility is lower for holes since we are using (100) oriented Silicon crystals and not (110) as in FinFETs, where the hole mobility was, instead, larger. Then a new equivalent dielectric permittivity constant $EPSEQ$ has been inserted, to take into account the influence of the actual thickness of both the interfacial layer (made of silicon oxide) and the dielectric Hi-K layer, which was previously considered in terms of EOT (Equivalent Oxide thickness) and not in actual thickness, giving a more realistic estimation of the equivalent width $WEFF$.

$$EPSEQ = \frac{EPS0 \cdot EPSOX \cdot TIL + EPS0 \cdot EPSHK \cdot THK}{THK + TIL} \tag{5.2}$$

This parameter is inserted into the $Cins$ one, the insulator capacitance, which reads:

$$Cins = \frac{WEFF \cdot EPSEQ}{THK + TIL} \tag{5.3}$$

Moreover, the $FECH$ (Factor for Channel End ) parameter was inserted into the computation. This parameter was declared but not used in the BSIM-CMG original code and it considers it is used to consider the effective difference between the (100) oriented bottom and top gates and the (110) side gates, by modifying as a pre-factor the effective width of the device.

$$WEFF_UFCM = Nsh \cdot (2 \cdot WFIN + 2 \cdot FECH \cdot HFIN) \tag{5.4}$$

It is also possible to notice that, for 3D devices in particular, channel doping is not constant, especially in the vertical direction, as it is possible to observe in figure 5.5 and 5.6. To consider this effect values of the doping of the channel in the physical simulator have been retrieved by doing cuts along the channel, the values have been, then, averaged and plugged into the compact model by using the following formulation:

$$NBODY_AV = \frac{NBODY_TOP + NBODY_MID + NBODY_BOTTOM}{Nsh} \tag{5.5}$$

It can be observed that the parameter NBODY is the perturbation parameter in the BSIM-CMG, hence it is usually a rather small quantity. The channel doping should be, in fact, as small as possible to avoid ionized impurities scattering mechanisms that result in a reduction of the carriers' mobility.

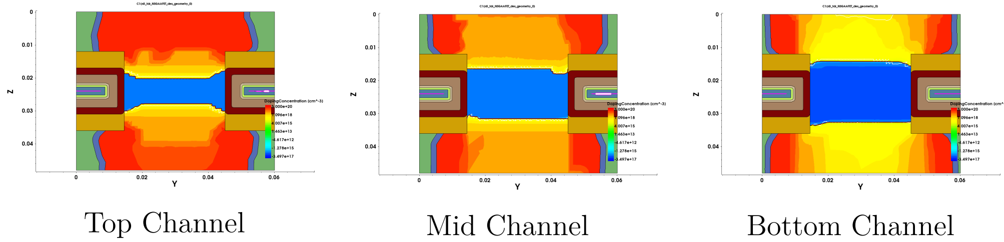



Figure 5.5. Net doping cuts along the n-type NanoSheet Channels

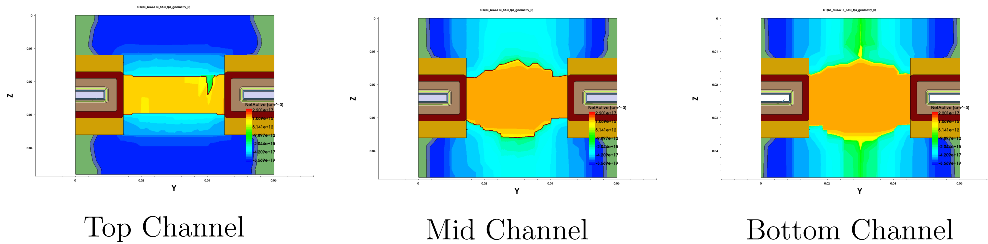



Figure 5.6. Net doping cuts along the p-type NanoSheet Channels

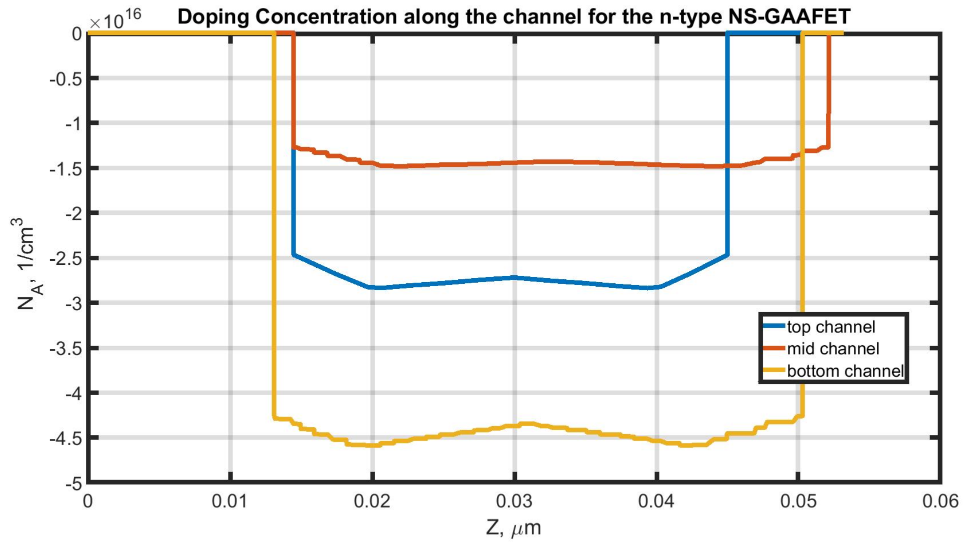



Figure 5.7. Doping of the channel along each NanoSheet channel for n-type NS-GAAFET

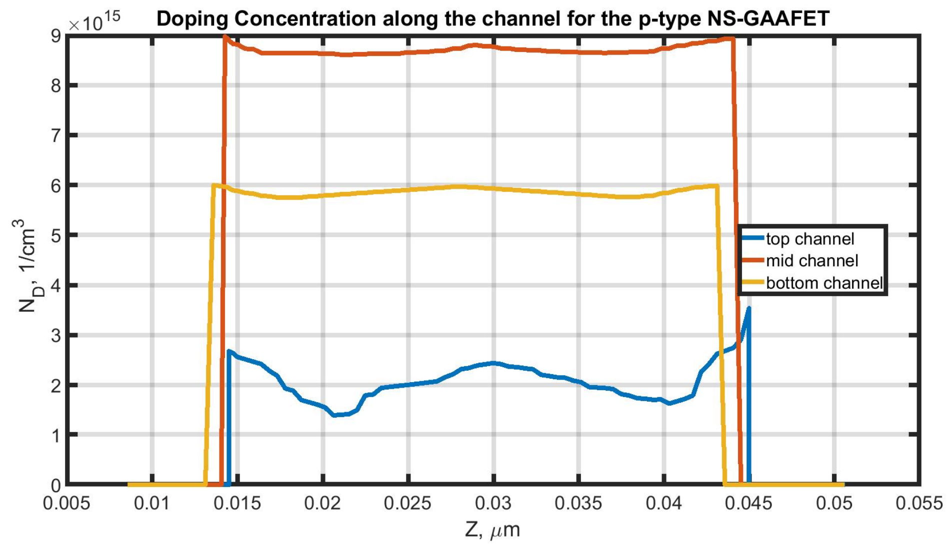



Figure 5.8. Doping of the channel along each NanoSheet channel for p-type NS-GAAFET

The doping of the Source/Drain is also not constant but varies in the vertical direction, due to process variations or misalignments in the implantation steps. In Figure 5.9 and 5.10 it is possible to observe cuts in the vertical direction in the S/D regions. To consider this effect, a mean value of the doping value for each NanoSheet has been considered in $NSD_AV$. Cuts inside the SD regions of each NanoSheet have been done and an average value has been calculated for each sheet. Then a further average parameter $N_{SD,av}$ has been inserted in the compact model.

$$NSD_AV = \frac{NSD_TOP + NSD_MID + NSD_BOTTOM}{3} \tag{5.6}$$

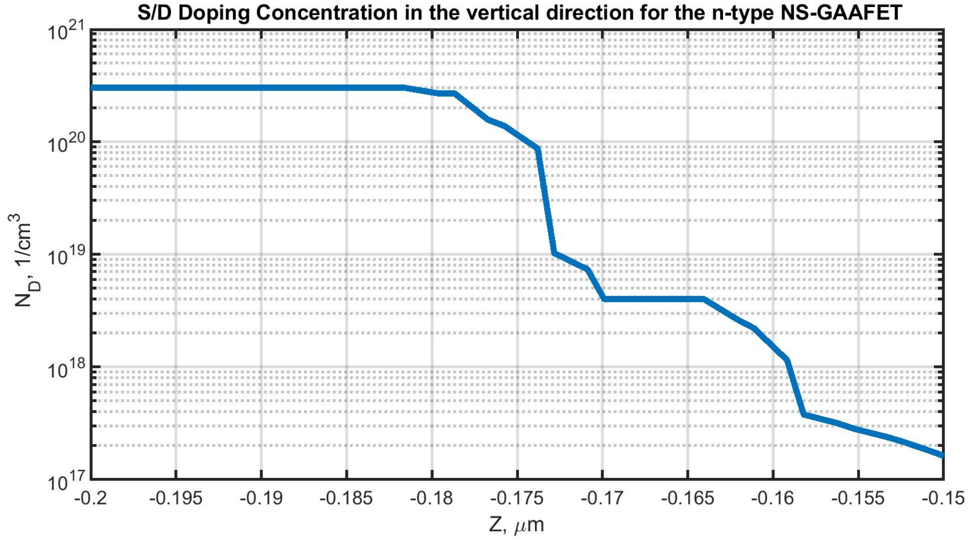



Figure 5.9. Source/Drain doping in the vertical direction, n-type NS-GAAFET

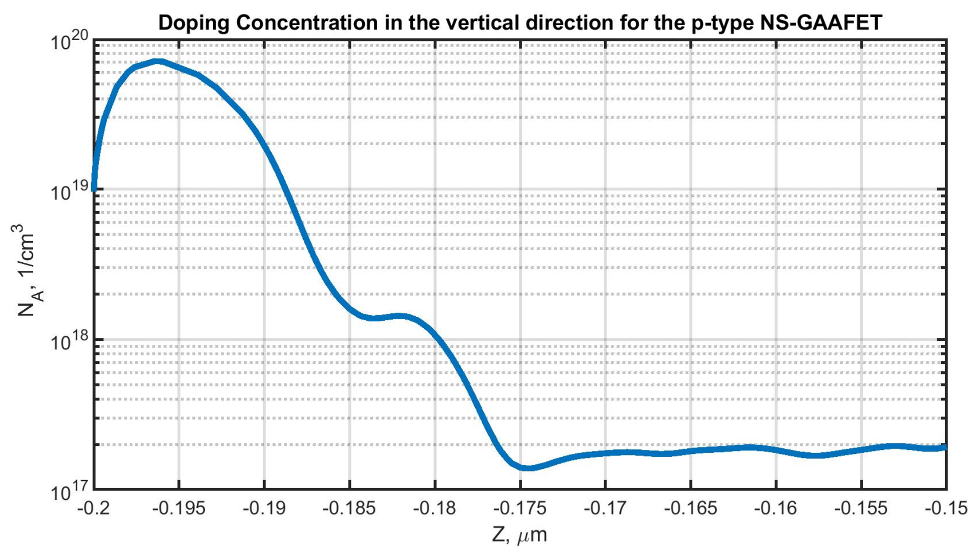



Figure 5.10. Source/Drain doping in the vertical direction, p-type NS-GAAFET

## 5.2 DC Trans-Characterstics

After model modifications, DC simulations were run inside the SPICE simulator to verify compatibility with device-level simulations. The result can be seen in figure 5.11.

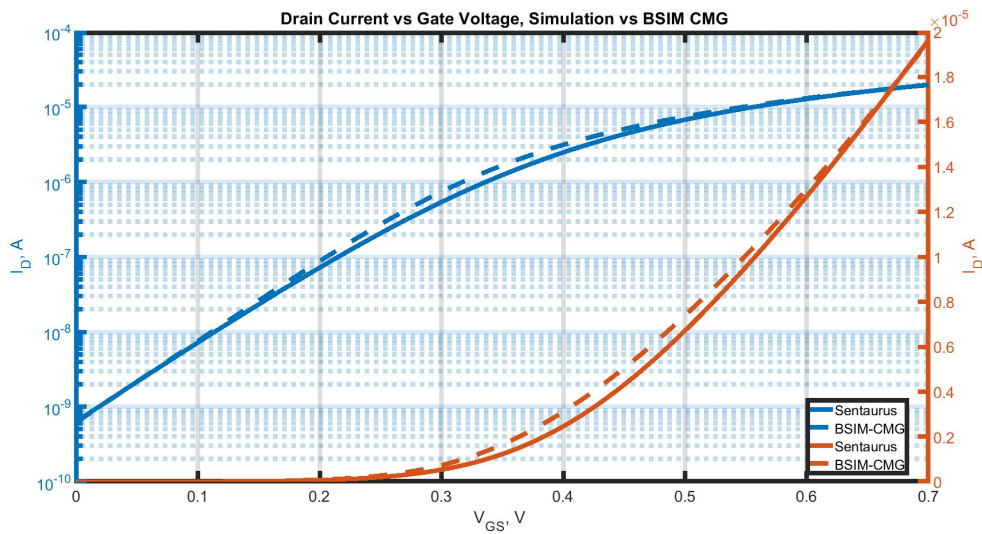



Figure 5.11. Trans-Characteristic of the physics-based model and the modified BSIM-CMG model, n-type NS-GAAFET

As it is possible to observe in figure 5.11, the trans-characteristic matches closely the ON and OFF currents, being useful especially for digital applications, where the two states are codified with the ON and OFF current. The model presents a little uncertainty, anyway, at the middle of the trans-characteristic, especially in the threshold region. Moreover, the absolute and the relative errors between the physics-based simulations and the modified compact model ones have been evaluated, as it is possible to observe in figure 5.12 and figure 5.13.

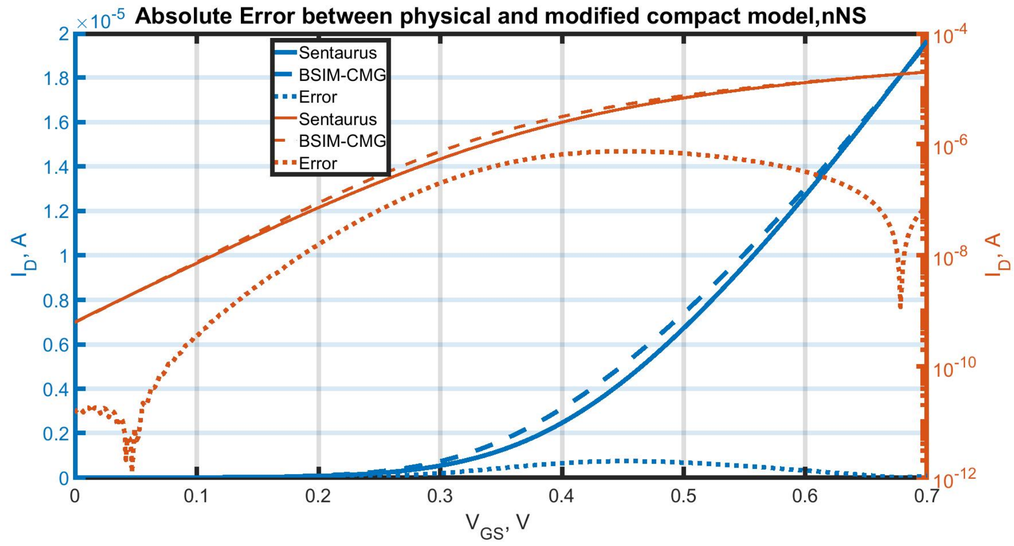



Figure 5.12. Absolute error, compact model trans-characteristic and physical model trans-characteristic in linear and log scale for n-type NS-GAAFET

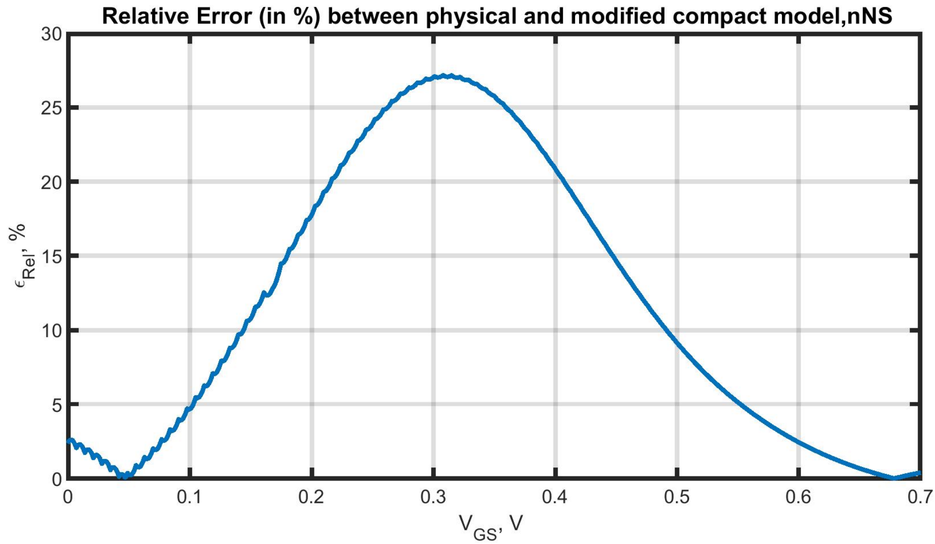



Figure 5.13. Relative error in % between the compact model and physical model

It is possible to observe from 5.13 that the maximum relative difference between the two models is near the threshold, amounting to nearly 30 %.

A similar approach regarding the trans-characteristics has been done for the p-type device after the model modifications. As it is possible to observe in figure 5.14 the model matches closely around the ON and OFF state, but it gets a little weaker in the middle of the trans-characteristic.

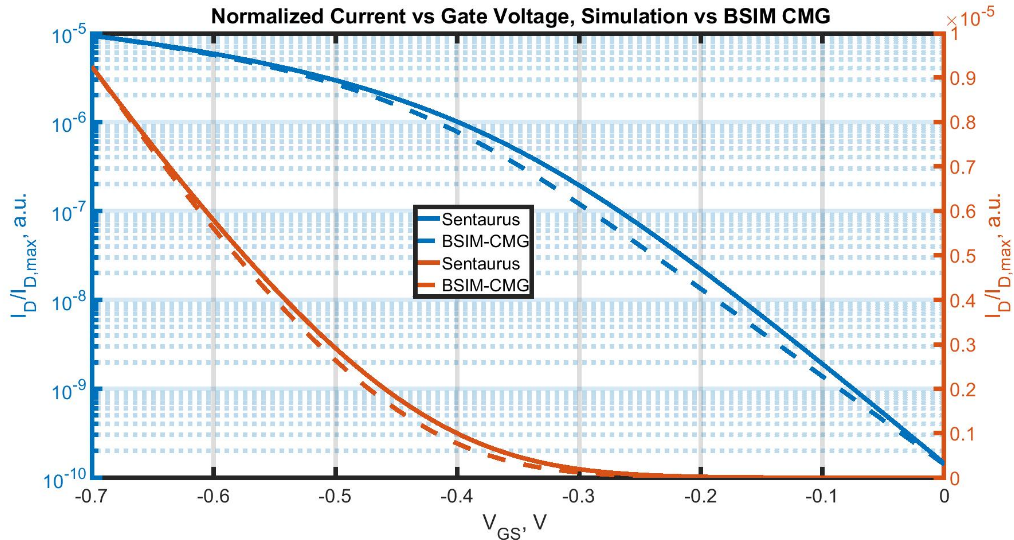



Figure 5.14. Trans-Characteristic of the physics-based model and the modified BSIM-CMG model, p-type NS-GAAFET

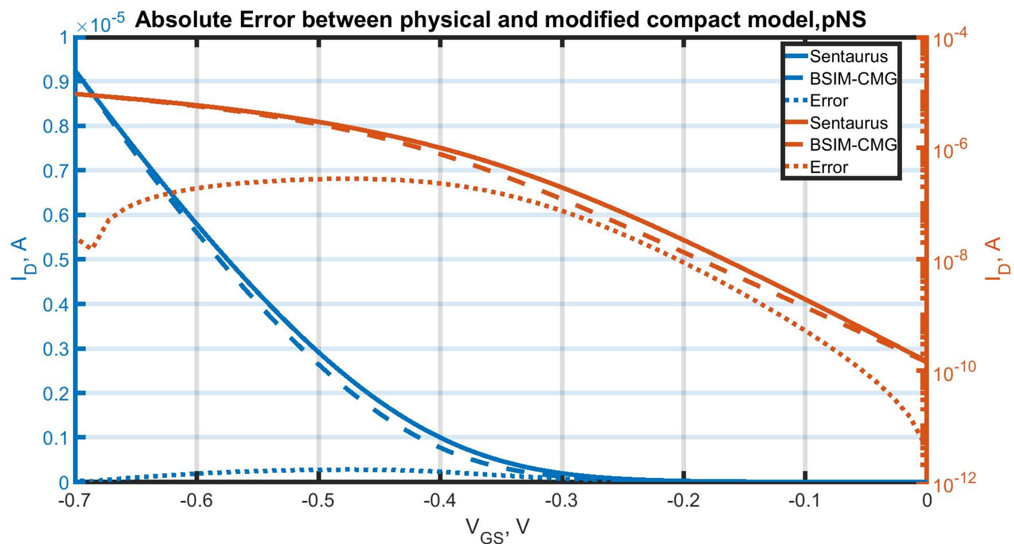



Figure 5.15. Absolute error, compact model trans-characteristic and physical model trans-characteristic in linear and log scale, p-type NS-GAAFET

The absolute and relative errors have been computed similarly for the p-type NS-GAAFET. As it is possible to observe in figures 5.15 and 5.16 also, in this case, the error is less than 40%, being worse, especially near the threshold voltage values.

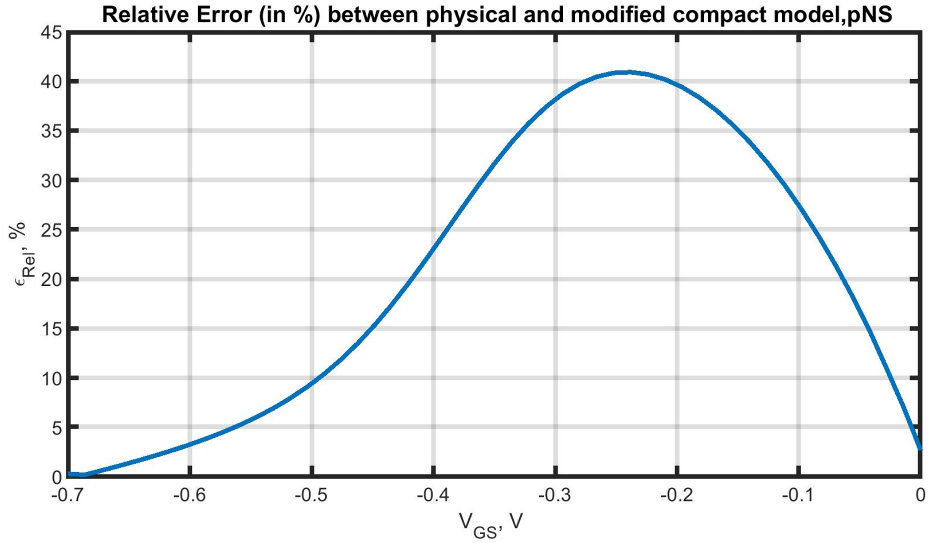



Figure 5.16. Relative error between the compact model and physical model

## 5.3 Gate current

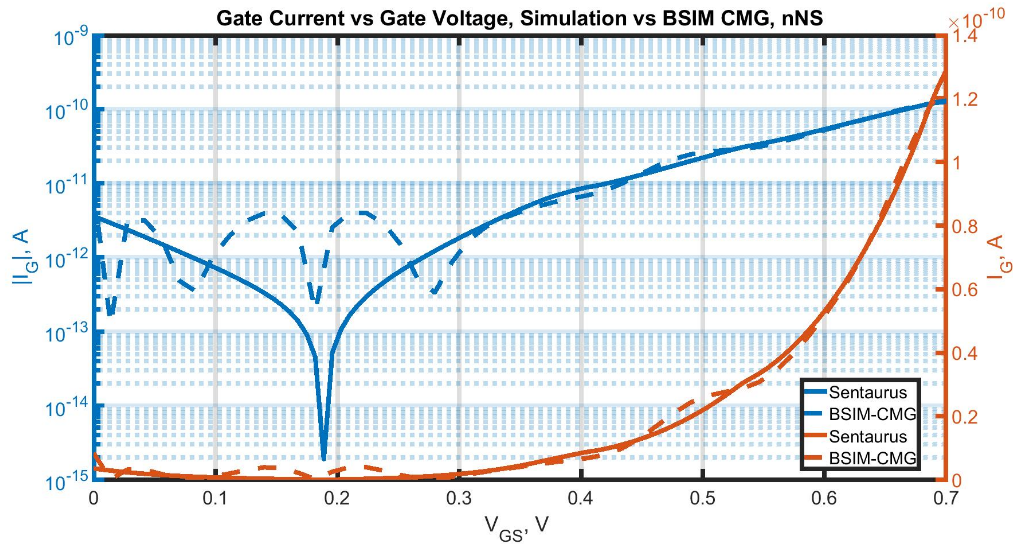



Figure 5.17. Matching of the Gate Current, n-type NS-GAAFET

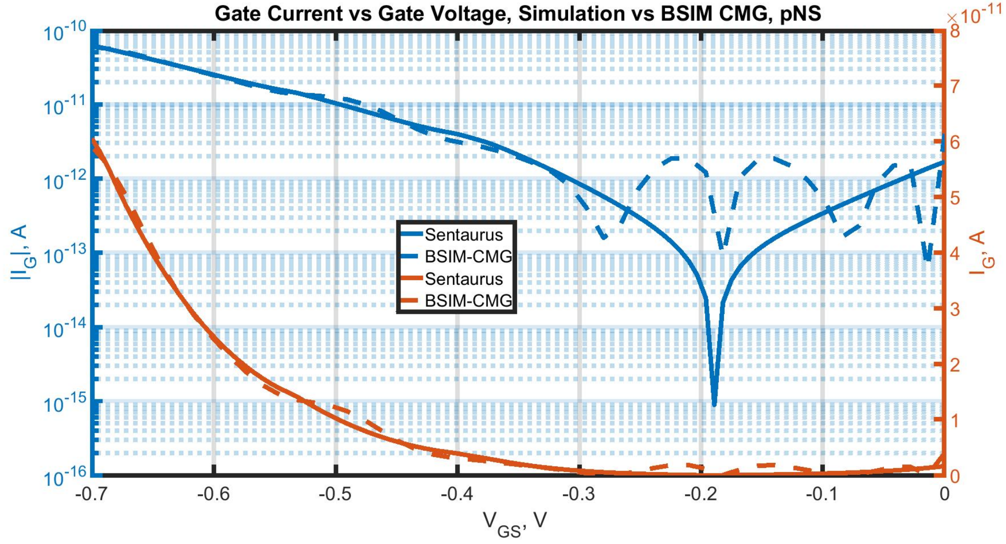



Figure 5.18. Matching of the Gate Current, p-type NS-GAAFET

Afterward, a matching of the Gate current due to the direct gate tunneling has been also tried. As stated in the previous section, the gate current in bulk devices flows mainly from the gate to the bulk, whereas in SOI devices the gate current due to the direct tunneling flows mainly from the gate to the source contact, which presents the lower potential.
The previous modeling for the gate currents relied, in fact, on a model based on the old BSIM-4 expression, having some differences from the physical simulations, and was based on a compound logarithmic and exponential function.
To be more compliant with the simulation obtained by the physics-based simulator a different model based on a compound sinusoidal expression has been used for both the n and p-type devices model, as shown in the following.

$$Ig = c1 \cdot sin(a1 \cdot V_{GS} + b1) + c2 \cdot sin(a2 \cdot V_{GS} + b2) + ...$$

As it is possible to observe from figures 5.17 and 5.18 a slight ambipolar behavior of the gate current is present which was not considered in the previous model is better represented, albeit with little precision.

# Chapter 6

# AC Simulations

## 6.1 Device-Level AC Simulations

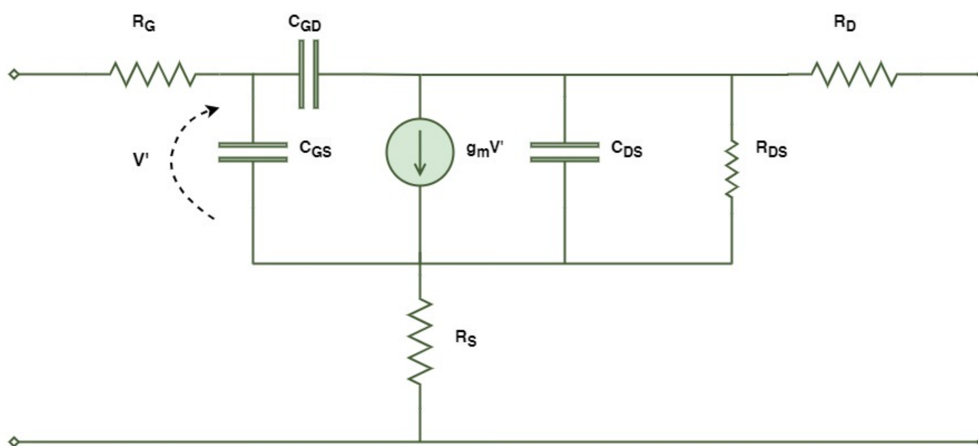



Figure 6.1. Basic High Frequency equivalent Small Signal circuit for a FET

This section aims to verify the fabricated device's frequency behavior by performing AC simulations inside the physics-based simulator to analyze how the various reactive elements present in the device can hamper its performance. The device's frequency response can be computed through the Small Signal AC Extraction feature of the SDevice simulator, which calculates the admittance (Y) parameters for each frequency step. A basic High-Frequency equivalent Small Signal circuit is shown in Figure 6.1.

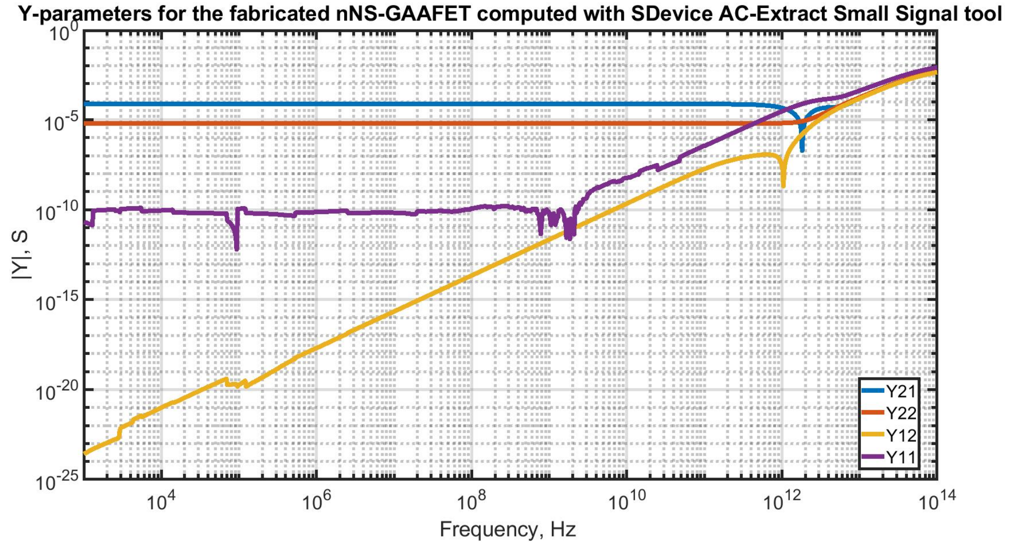



Figure 6.2. Admittance (Y) parameters frequency response for the fabricated n-type NS-GAAFET

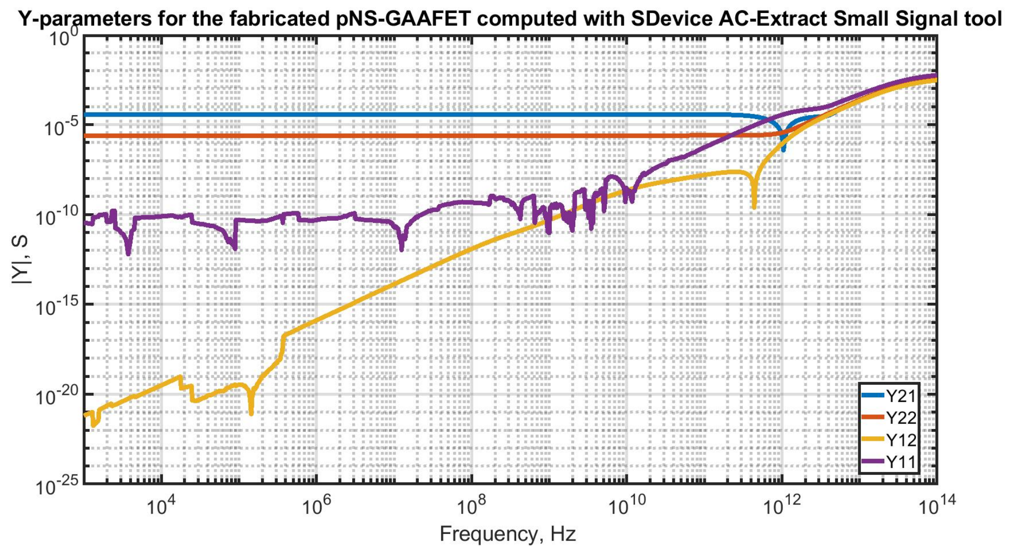



Figure 6.3. Admittance (Y) parameters frequency response for the fabricated p-type NS-GAAFET

The admittance representation has been used since, starting from it, it can be possible to derive the hybrid (H) parameters, from which it is possible to compute the cut-off frequency of the device. The cut-off frequency of the device is the frequency for which the current transfer function $H_{21} = \frac{I_D}{I_G} = \frac{Y_{21}}{Y_{11}}$ parameter has unitary modulus $H_{21} = 1$, hence the device has a unitary gain. Out of the 4 ports of the device, the useful ones for the computation of the frequency behavior of the device are just the drain (output) and the gate (input) ports, thus 2x2 Admittance matrices have been calculated at each given frequency step by the Small Signal AC simulator embedded in the device-level CAD. It is possible to observe the frequency behavior of the admittance parameters computed by the TCAD, in figures 6.2 and 6.3.
At low frequencies the admittance parameter $Y_{21}$ is constant, meaning that the device is working as a controlled current generator (transistor effect) hence the gate is keeping control of the channel. The output admittance $Y_{22}$ is, instead, due to the output resistance, which presents a constant value at low frequencies, while at higher ones capacitive effects start to be considerable, increasing the admittance value. Similar behavior is reported for the complementary device (p-type) in Figure 6.5.
Moreover, it can be noticeable that, at low frequencies, the $Y_{12}$ admittance modulus tends to a very small value, behaving as an open circuit since the parasitic capacitors behave as open circuits at low frequencies. At high frequencies, instead, the admittances tend to a large value (infinity) since the reactive elements dominate over the memoryless ones. Similar results hold for the complementary p-type device AC small signal analysis in figure 6.3.
The frequency dependence of the hybrid parameter $H_{21(}f)$ is reported in Figures 6.4 and 6.5.

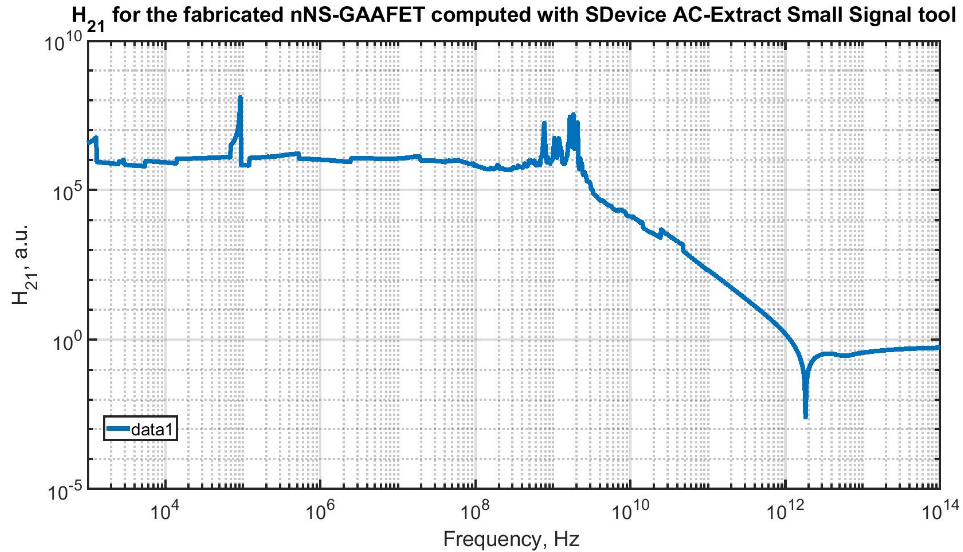



Figure 6.4. $H_{21}$ hybrid parameter frequency response for the fabricated n-type NS-GAAFET

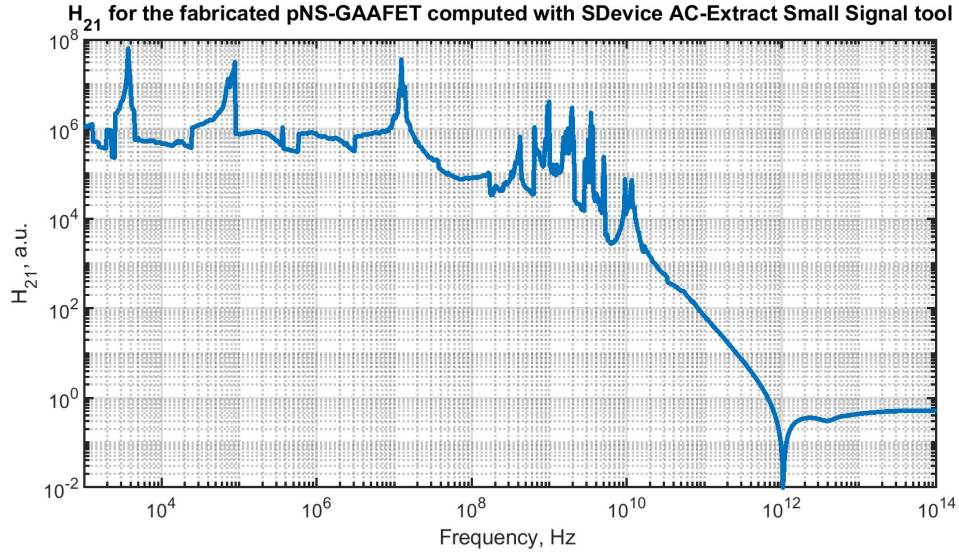



Figure 6.5. $H_{21}$ hybrid parameter frequency response for the fabricated p-type NS-GAAFET

As discussed in the previous sections, for the NS-GAAFET device the additional capacitance contribution due to the presence of the inner spacers can play a certain role, hence it should be reduced to increase the AC performance of the device. For this reason, dielectric permittivities of different materials have been tried to be employed as both inner and main spacers to increase the cutoff frequency, such as the already used $SiO_2$ and $HfO_2$ (for comparison), but also a commonly used dielectric material such as Alumina $Al_2O_3$ and an organic one such as PTFE. In particular, the choice of PTFE (polytetrafluoroethylene, commercially known as Teflon) as the spacer material has been retrieved from [47].
A sweep in the AC simulations at the device level has been carried out to investigate the cut-off frequency sensitivity to the spacers material, as it is possible to observe in figure 6.6 for the n-type device and in figure 6.8 for the complementary one. Moreover, the DC simulations for each device with a different spacer material are almost coincident since only reactive elements are involved, hence the static characteristic of the device remains unvaried.

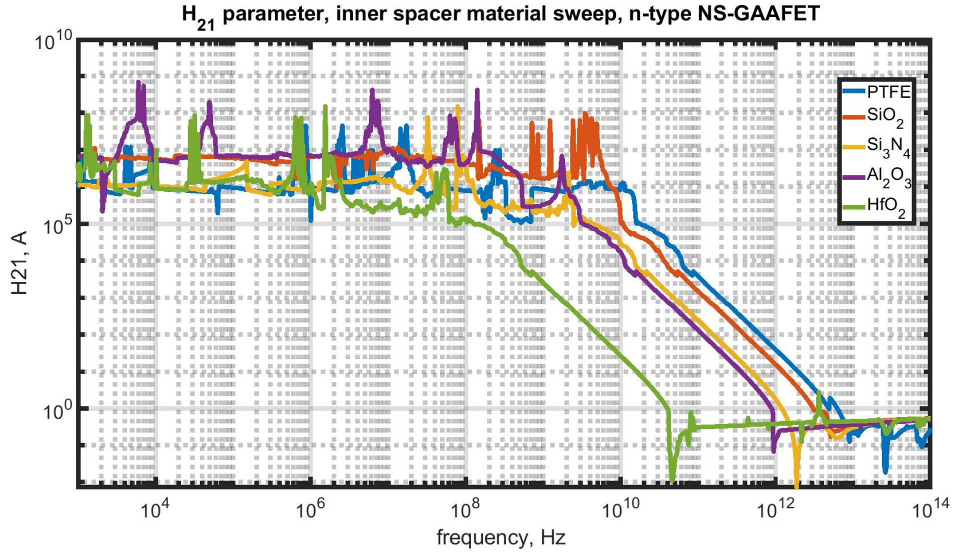



Figure 6.6. $H_{21}$ hybrid parameter frequency response for the fabricated p-type NS-GAAFET

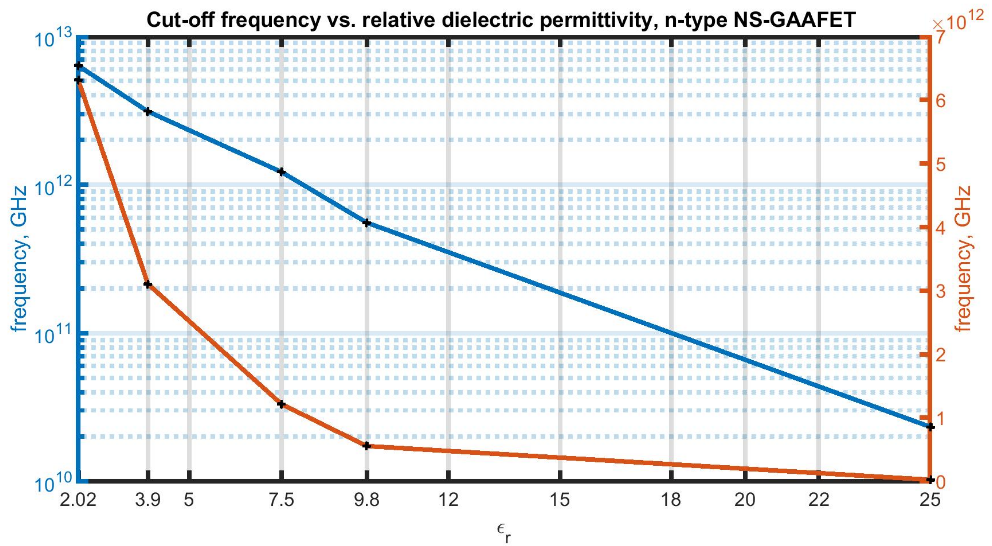



Figure 6.7. $H_{21}$ hybrid parameter frequency response for the fabricated n-type NS-GAAFET

| Cutoff Frequencies for different spacers material, n-type NS-GAAFET | | |
|---|---|---|
| Material | $\epsilon_r$ | $f_{cut}$ $[GHz]$ |
| PTFE | 2 | 6037 |
| $SiO_2$ | 3.9 | 3011 |
| $Si_3N_4$ | 7.5 | 1213 |
| $Al_2O_3$ | 9.8 | 553 |
| $HfO_2$ | 25 | 23 |

Table 6.1. Cutoff Frequencies for different spacers material, n-type NS-GAAFET

As it is possible to observe in figures 6.8 6.7 and in table 6.3, where respectively the frequency behavior of the hybrid parameter $H_{21}$ and the cut-off frequency versus the relative dielectric permittivity has been represented, the cut-off frequency of the n-type device decreases for increasing values of $\epsilon_r$ with a resembling exponential behavior.

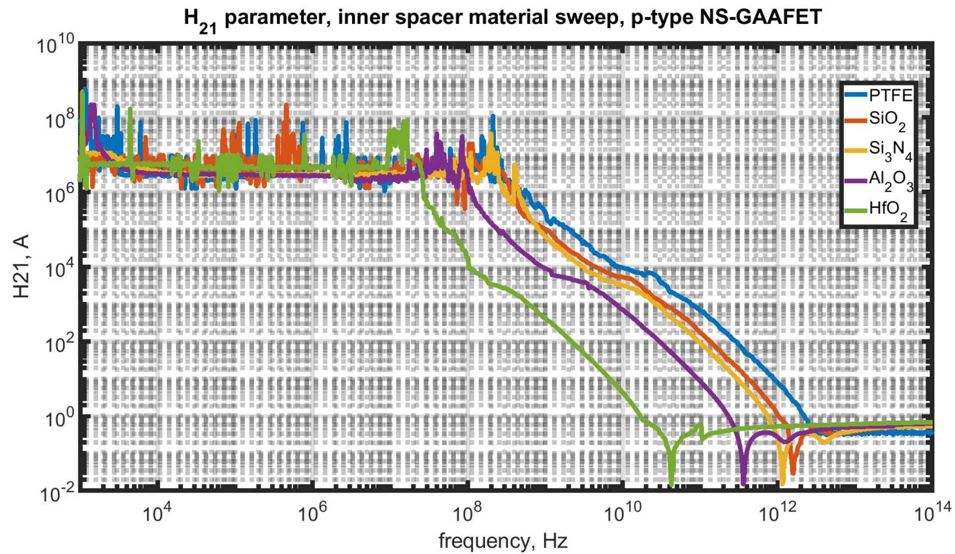



Figure 6.8. Cut-off frequency of the p-type NS-GAAFET versus the relative dielectric permittivity

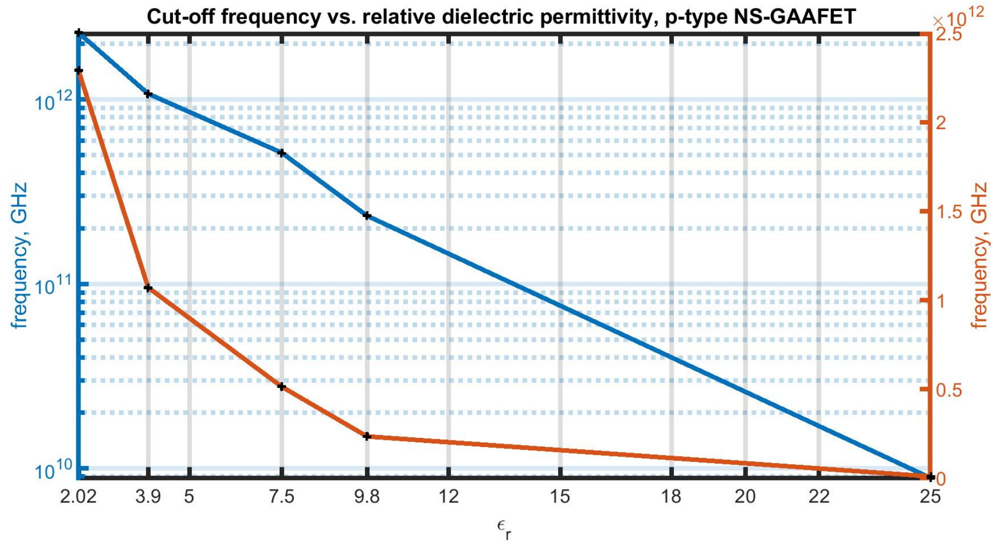



Figure 6.9. $H_{21}$ hybrid parameter frequency response for the fabricated p-type NS-GAAFET

| Cutoff Frequencies for different spacers material, p-type NS-GAAFET | | |
|---|---|---|
| Material | $\epsilon_r$ | $f_{cut}$ $[GHz]$ |
| PTFE | 2 | 2287 |
| $SiO_2$ | 3.9 | 1070 |
| $Si_3N_4$ | 7.5 | 512 |
| $Al_2O_3$ | 9.8 | 233 |
| $HfO_2$ | 25 | 89 |

Table 6.2. Cutoff Frequencies for different spacers material, p-type NS-GAAFET

A similar sensitivity of the cut-off frequency versus the spacers material can be observable in figure 6.8, in figure 6.9 and table 6.2. The behavior of this frequency versus the relative dielectric permittivity of the p-type device can be seen in Figure 6.9. Moreover, it is possible to observe the cut-off frequency of the p-type device is lower if compared to the complementary n-type device, due to the lower mobility and, hence, lower speed of the p-type devices.

## 6.2 Circuit-Level AC Simulations

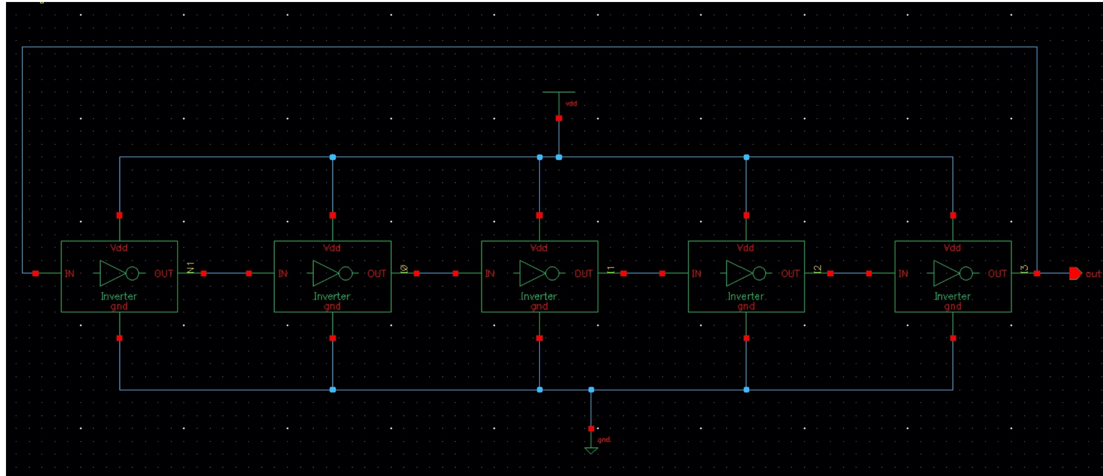



Figure 6.10. Schematic capture of the 5 ports Ring Oscillator.

The impact of inner and main spacer material in a time-varying regime can be observed not only at device-level simulations but also in circuital ones. For example, it is possible to analyze how the oscillation frequency of a ring oscillator changes if the spacer material is modified. This oscillator is often used as a test bench for the verification of new devices. The ring oscillator, in particular, is a topology made of an odd number of inverters connected in series and a feedback connection from the output of the last inverter towards the input. The basic equation for a generic $N_{port}$ ring oscillator is the following.

$$f_{osc} = \frac{1}{2N_{port} \cdot \tau_{inv}}$$

Where $N_{port}$ is the odd number of inverters used and $\tau_{inv}$ is the propagation delay of the inverters, which are supposed to be identical. The factor of 2 has been inserted since a complete cycle of the ring oscillator includes both the high-to-low and low-to-high transitions. In particular $N_{ports} = 3, 5$ have been used, since a larger number of ports results in much slower frequencies. A sweep of the inner spacer material has been done, as is possible to observe in figure 6.11.

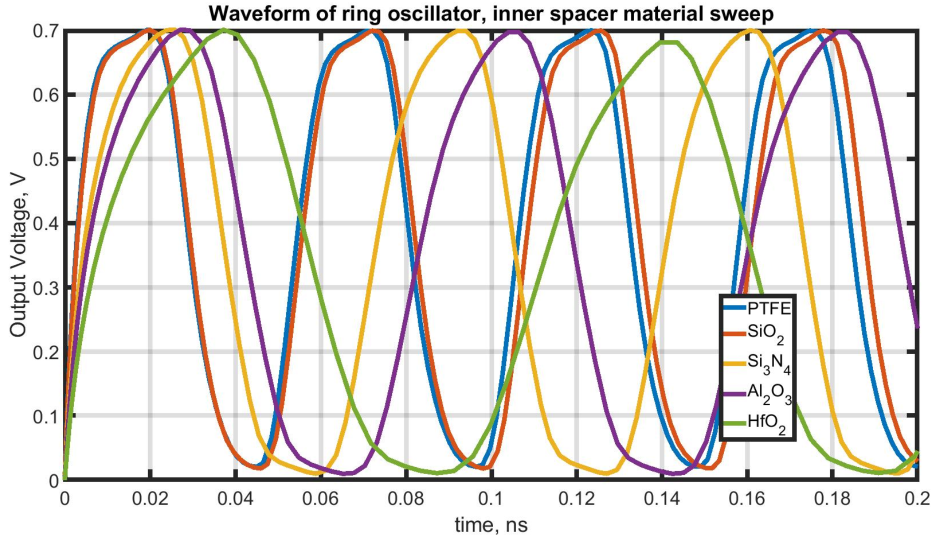



Figure 6.11. Waveform of the output of a 5-port Ring Oscillator, relative dielectric permittivity sweep

From the waveforms in figure 6.11 it can be observable that the spacer having a lower dielectric permittivity material such as the PTFE or the Silicon Oxide provides a higher oscillation frequency since the additional coupling capacitance of the inner spacers is reduced, as it can be seen in figure 6.12.

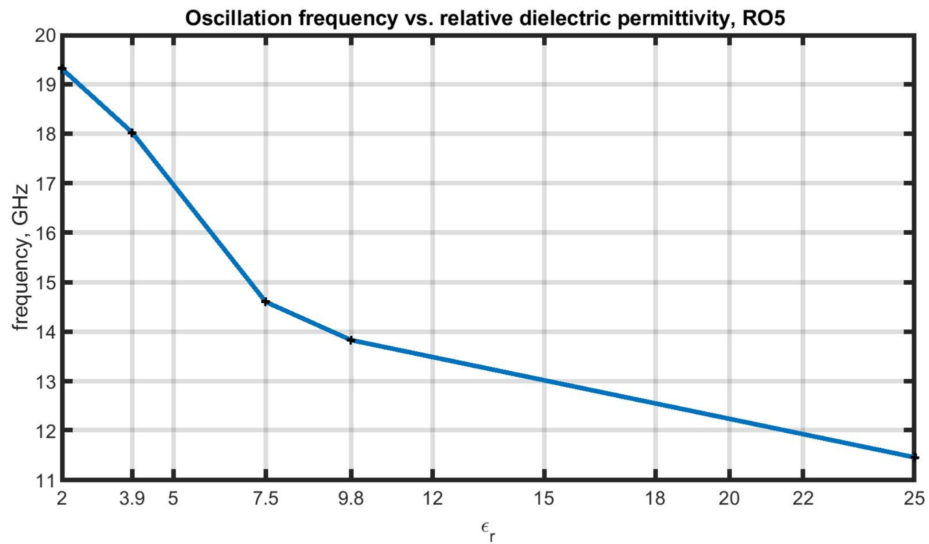



Figure 6.12. Oscillation frequency of the RO5 versus the relative dielectric permittivity

| Oscillation Frequencies for different spacers material, RO5 | | |
|---|---|---|
| Material | $\epsilon_r$ | $f_{cut}$ $[GHz]$ |
| PTFE | 2 | 19.308 |
| $SiO_2$ | 3.9 | 18.016 |
| $Si_3N_4$ | 7.5 | 14.596 |
| $Al_2O_3$ | 9.8 | 13.825 |
| $HfO_2$ | 25 | 11.456 |

Table 6.3. Oscillation Frequencies for different spacers material, RO5

# Chapter 7

# Conclusions and Future Perspectives

This thesis work was focused on the study of the process simulation of novel devices which are main candidates for the current semiconductor electronics devices, the NanoSheet Gate-All-Around FETs, on the modeling of their behavior in a circuit-level environment (compact modeling) and interactions between the two.
In Chapter 4 a comparison is made between the simulation of the NS-GAAFET TCAD process and actual experimental processes, highlighting the main differences between the two, in particular concerning the steps that are peculiar to the fabrication of NS-GAAFET, such as SiGe recess for the definition of the inner spacers and the selective etching of SiGe sacrificial layers. DC simulations have been, then, carried out in the TCAD to obtain the FOMs and compare the results with the experimental measurements and the derived FOMs.
In Chapter 5 a matching of the physics-based simulations results with a Surface Potential compact model such as the BSIM-CMG-NS and on the frequency response of the device, in particular with different materials acting as spacers. The BSIM-CMG-NS model was augmented to grasp a more detailed behavior of the NS-GAAFET device, focusing on mobility, the HKMG stack, and doping nonuniformities.
In Chapter 6 AC simulations have been carried out to investigate the impact of new process steps on the frequency behavior of the NS-GAAFET. In both Device-level and circuit-level AC simulations have been done, the inner spacer material plays a crucial role in reducing the additional capacitance, peculiar to the device, through the use of low-k dielectrics.
For further development of the device process and electrical simulations, more in-depth simulations such as atomistic ones can be employed, such as DFT or Force-Field simulators, which are computationally more expensive but able to provide a much higher degree of accuracy. In particular for devices at nanometric levels, where quantum effects become further relevant, requiring a full solution of the quantum problem through the use of the Schroedinger equation since the corrective terms that are usually plugged into classical or semi-classical solvers (such as BTE ones) may not provide a sufficiently accurate solution.

A second type of development could be done in a circuital direction, both in the digital (time) and analog (frequency) domains, by analyzing the behavior and the response of more complex circuits or cells ( such as memory ones) and the impact of the device features on the circuital FOMs.

# Chapter 8

# Appendix

## 8.1 Sentaurus scripts

### 8.1.1 SProcess n-type NS-GAAFET script

```

math coord.ucs

math numThreads=4
AdvancedCalibration 2017.09


pdbSet Mechanics StressRelaxFactor 1

# Solver Enhancement
pdbSet Math diffuse 3D ILS.hpc.mode 4
# turn off stress relaxation after depo/etch
pdbSet Mechanics EtchDepoRelax 0

# meshing parameters
mgoals resolution= 1.0/3.0 accuracy= 1e-6
pdbSet Grid SnMesh max.box.angle.3d 175
grid set.min.normal.size= 0.005/1.0 \
 set.normal.growth.ratio.3d= 2.0 \
 set.min.edge= 1e-7 set.max.points= 1000000 \
 set.max.neighbor.ratio= 1e6


#-----------------------------------------------------
# Structure parameters, [um]
set STI      0.015                        ;# STI length
set H_STI    0.02                            ;# STI height
set Tns             0.005                                   ;# Thickness nanosheet
set Spacing  0.01                                     ;# Space between nanosheet (SiGe)
set H        [expr 4*$Spacing + 3*$Tns + $H_STI]        ;# Fin exposure
set Hfin     [expr ($H - $STI)]                                ;# Fin height
```

```
set Lg       0.012                 ;# Gate length
set HalfLg   [expr $Lg*0.5]           ;# Half gate length
set Tox      0.0025                          ;# Total thickness of gate insulator
set LSpacer  0.006                           ;# Length Spacer
set Lsd      0.012        ;# Length of S/D
# 12 lg + 6*2 spacer + 12*2 lsd
set CPP                [expr $Lg + 2*$LSpacer + 2*$Lsd] ;#Contact Pitch
set Wns                0.03                        ;#Width of NS
set FP [expr 2*$STI + $Wns] ;#Contact Pitch
set Tiox     0.001               ;#Gate dummy ox


# Doping parameters, [/cm3]

set Nsub     1.0e5                 ;#Substrate doping
set Nsd      1.0e13                 ;#SD doping [/cm2]
set Next     2e10                    ;#S/D extension doping [/cm2]
set Nstop    3.0e11                 ;#channel stop doping [/cm2]


line x location= -70.0<nm> spacing=10.0<nm> tag= SiTop
line x location= 20.0<nm> spacing= 10.0<nm>
line x location= 30.0<nm> spacing= 15.0<nm> tag= SiBottom

line y location= 0.0 spacing= 10.0<nm> tag= Left
line y location= $FP spacing= 10.0<nm> tag= Right

line z location= 0.0 spacing= 15.0<nm> tag= Back
line z location= $CPP spacing= 15.0<nm> tag= Front

#substrate
region Silicon xlo= SiTop xhi= SiBottom
ylo= Left yhi= Right zlo= Back zhi= Front substrate

init concentration=$Nsub<cm-3> field=Boron wafer.orient= {0 0 1} flat.orient= {1 1 0}
!DelayFullD


refinebox name= nw min= {-0.12 0 0.0} max= {0 0.38 0.45} xrefine= 5<nm> yrefine= 10<nm>
zrefine= 15<nm>
grid remesh

#--Epi layer with known doping concentration (well)

deposit material= {Silicon} type=isotropic time=1 rate= {$H}



deposit material= {SiliconGermanium} type=isotropic time=1 rate= {$Spacing}

deposit material= {Silicon} type=isotropic time=1 rate= {$Tns}

deposit material= {SiliconGermanium} type=isotropic time=1 rate= {$Spacing}
```

```
85
86  deposit material= {Silicon} type=isotropic time=1 rate= {$Tns}
87
88  deposit material= {SiliconGermanium} type=isotropic time=1 rate= {$Spacing}
89
90  deposit material= {Silicon} type=isotropic time=1 rate= {$Tns}
91
92  deposit material= {SiliconGermanium} type=isotropic time=1 rate= {$Spacing}
93
94
95
96  #----Sidewall Image Transfer (SIT)
97
98  #dry oxidation
99  diffuse temperature= 900<C> time= 4.0<min> O2
100
101 struct tdr= n@node@_pGAA3 ;#deposit SiO2, hardmask, mandrel
102
103 deposit material= {Nitride} type= isotropic time= 1<min> rate= {0.0165}
104 deposit material= {AmorphousSilicon} type= isotropic time= 1<min> rate= {0.1}
105
106 struct tdr= n@node@_pGAA3b ;#deposit SiO2, hardmask, mandrel
107
108 mask name= fin left= 0<nm> right= [expr $STI + $Wns] back= -1 front= 0.17<um> negative
109
110 etch material= {AmorphousSilicon} type= anisotropic time= 1<min> rate= {0.1} mask= fin
111
112 deposit material= {Oxide} type= isotropic time= 1 rate= {0.035}
113 etch material= {Oxide} type= anisotropic time= 1 rate= {0.045} isotropic.overetch= 0.1
114
115 struct tdr= n@node@_pGAA3c ;
116
117 etch material= {AmorphousSilicon} type= anisotropic time=1<min> rate= {0.3}
118 etch material= {Nitride} type=anisotropic time= 1<min> rate= {0.02}
119
120 struct tdr= n@node@_pGAA3d_etchAM;
121 #etch oxide on top of superlattice
122 etch material= {Oxide} type= anisotropic time=1 rate= {0.035}
123 etch material= {Silicon SiliconGermanium} type=anisotropic time=1<min> rate= {$H}
124
125 struct tdr= n@node@_pGAA3d_finForm;
126
127 #TEOS STI  $H+0.0165
128 mater add name=TEOS new.like=oxide
129 deposit material= {TEOS} type= isotropic time= 1<min> rate= {$H}
130
131 etch material= {TEOS} type=cmp etchstop= {Nitride} etchstop.overetch=0.0001
132 struct tdr= n@node@_pGAA3e_TEOS ;
133
134 #-etch spacers 4 fin
135 etch material= {Oxide} type= anisotropic time=1<min> rate= {0.07}
136 etch material= {TEOS} type=isotropic time=1 rate= {($H-$H_STI+0.02-0.001+0.00009)}
137
```

```
138 etch material= {Nitride} type=anisotropic time=1 rate= {0.02}
139
140 etch material= {Oxide} type= anisotropic time=1<min> rate= {0.035}
141
142 struct tdr= n@node@_pGAA3f_etchMasks ;
143
144
145 #Punch through stop layer
146
147 refinebox name= etchstop min= {-0.13 0 0.0} max= {-0.04 0.040 0.045}
148 xrefine= 4<nm> yrefine= 10<nm> zrefine= 10<nm>
149 grid remesh
150
151
152 implant Boron dose= $Nstop<cm-2> energy=8<keV> tilt=0 rotation=90
153 implant Boron dose= $Nstop<cm-2> energy=8<keV> tilt=0 rotation=270
154
155
156 SetPlxList {PTotal}
157 WritePlx n@node@_PMOS_etchstoplayer.plx y=0.03 z=0.0 Silicon
158
159
160 implant Boron dose= $Nstop<cm-2> energy=9<keV> tilt=0 rotation=90
161 implant Boron dose= $Nstop<cm-2> energy=9<keV> tilt=0 rotation=270
162
163 SetPlxList {PTotal}
164 WritePlx n@node@_PMOS_etchstoplayer.plx y=0.03 z=0.0 Silicon
165
166 implant Boron dose= $Nstop<cm-2> energy=10<keV> tilt=0 rotation=90
167 implant Boron dose= $Nstop<cm-2> energy=10<keV> tilt=0 rotation=270
168
169
170 SetPlxList {PTotal}
171 WritePlx n@node@_PMOS_etchstoplayer.plx y=0.03 z=0.0 Silicon
172
173 diffuse temperature=300<C> time=0.0001<s>
174
175 struct tdr= n@node@_pGAA4_PTSLdiff
176
177
178 #Dummy gate
179 deposit material= {Oxide} type= isotropic time=1 rate= {$Tiox}
180
181 deposit material= {Polysilicon} type= fill coord= -0.25
182 struct tdr= n@node@_nGAA4_dummygatepre
183 mask name= gate back= ($Lsd+$LSpacer)<um> front= ($CPP-$Lsd-$LSpacer)<um>
184 etch material= {Polysilicon} type= anisotropic time=1 rate= {0.2} mask= gate
185
186 struct tdr= n@node@_pGAA4_dummygate
187
188
189 #S/D extension LDD
190
```

```
191 mask name= gate_neg back= ($Lsd)<um> front= ($CPP-$Lsd)<um> negative
192 photo thickness= 5<um> mask= gate_neg
193
194
195 implant Phosphorus dose= $Next<cm-2> energy=1.8<keV>
196 tilt=-70<degree> rotation=-90<degree>
197 implant Phosphorus dose= $Next<cm-2> energy=1.8<keV>
198 tilt=-70<degree> rotation=-270<degree>
199 implant Phosphorus dose= $Next<cm-2> energy=1.8<keV>
200 tilt=-70<degree> rotation=-90<degree>
201 implant Phosphorus dose= $Next<cm-2> energy=1.8<keV>
202 tilt=-70<degree> rotation=-270<degree>
203
204
205 SetPlxList {BTotal BoronImplant}
206
207 WritePlx n@node@_NMOS_sdext.plx y=0.03 z=0.0 Silicon
208 SetPlxList {PTotal BTotal}
209 WritePlx n@node@_PMOS_sdext2X.plx y=0.03 z=0.0 Silicon
210
211 SetPlxList {PTotal BTotal}
212 WritePlx n@node@_PMOS_sdext2Y.plx x=-0.12 z=0.0 Silicon
213 strip Photoresist
214 struct tdr= n@node@_pGAA4_LDD;
215
216 strip Photoresist
217
218 #diffuse LDD RTA
219 diffuse temperature=300<C> time=0.00001<s>
220
221
222 struct tdr= n@node@_pGAA4_LDDdiff;
223
224 #spacer fabrication
225 mask name= inner_neg back= ($Lsd+$LSpacer)<um> front=($CPP-$Lsd+$LSpacer)<um> negative
226
227 etch material= {Oxide} type=anisotropic time=1 rate=1.0
228
229 etch material= {SiliconGermanium} type= anisotropic time=1 rate= {0.18} mask= gate
230
231 struct tdr= n@node@_pGAA6_anisoetch ;
232
233 deposit material= {Oxide} type= isotropic time=1<min>
234 rate= {$Tiox} selective.materials= {PolySilicon}
235
236 etch material= {Oxide} type=cmp etchstop= {PolySilicon} etchstop.overetch=0.001
237
238
239 struct tdr= n@node@_pGAA7_sidewall ;
240
241
242 mask name= spacer_neg back= ($Lsd)<um> front= ($CPP-$Lsd)<um> negative
243
```

```
244
245 deposit material= {Nitride} type= anisotropic time=1<min> rate= {0.2} mask=spacer_neg
246
247 etch material= {Nitride} type=cmp etchstop= {PolySilicon} etchstop.overetch=0.001
248
249 struct tdr= n@node@_pGAA8_spacerfab ;
250
251 # SiOCN protection
252 mask name= spacer_neg back= ($Lsd)<um> front= ($CPP-$Lsd)<um> negative
253
254 mater add name=SiCN new.like= Nitride
255 deposit material= {SiCN} type=anisotropic time=1 rate= {0.05} mask= spacer_neg
256
257 struct tdr= n@node@_pGAA9_SiOCNprot ;
258
259 #Etch Silicon for SD epi
260 etch material= {Silicon} type= isotropic rate= {0.01} time= 15<s>
261 struct tdr= n@node@_pGAA9_SietchSD ;
262
263
264 #---EPI OF SD
265
266 #To activate stress in SiC pocket for nFinFET#
267 pdbSetDoubleArray Silicon Germanium Conc.Strain {0 0 1 -0.0425}
268 pdbSetDouble Carbon Mechanics TopRelaxedNodeCoord 0.05e-4
269
270 # Diamond-shaped Si/SiGe Pocket using Lattice Kinetic Monte Carlo (LKMC)
271
272 pdbSet Grid KMC UseLines 1
273 pdbSet KMC  Epitaxy true
274 pdbSetBoolean LKMC PeriodicBC false
275 pdbSet LKMC Epitaxy.Model Coordinations.Planes
276
277
278 set EpiDoping_init  "Carbon= 1.5e21"
279 set EpiDoping_final "Carbon= 1.5e21"
280
281 temp_ramp name= epi temperature= 500<C> t.final= 550<C> time= 2<min>
282 Epi epi.doping= $EpiDoping_init
283 epi.doping.final= #$EpiDoping_final
284 epi.model= 1 epi.thickness= 0.055<um>
285
286 diffuse temp_ramp= epi lkmc
287
288 #false to model doping non-atomistically
289 pdbSet KMC Epitaxy false
290
291 struct tdr= n@node@_pGAA10_SiGe_SD_epi ;
292
293 #gate refine silicon
294 refinebox name= gate min= {-0.0125 0.0 0.012} max= {-0.18 0.040 0.0} xrefine=2.0<nm>
295 yrefine= 2.0<nm> zrefine= 2.0<nm>
296
```

```
297 #source refine silicon
298 refinebox name= source min= {-0.010 0.0 0.036} max= {-0.18 0.040 0.45}
299 xrefine= 5.0<nm> yrefine= 7.0<nm> zrefine= 10.0<nm>
300 
301 #drain refine silicon
302 refinebox name= drain min= {-0.010 0.0 0.0} max= {-0.2 0.040 0.0085}
303 xrefine= 5.0<nm>yrefine= 7.0<nm> zrefine= 10.0<nm>
304 
305 struct tdr= n@node@_nGAA10_SD_refine ;
306 
307 # S/D Implantation
308 
309 #original 1
310 implant Phosphorus dose= $Nsd<cm-2> energy=1<keV> tilt=-0 rotation=90
311 implant Phosphorus dose= $Nsd<cm-2> energy=1<keV> tilt=-0 rotation=270
312 
313 implant Phosphorus dose= $Nsd<cm-2> energy=1<keV> tilt=-0 rotation=90
314 implant Phosphorus dose= $Nsd<cm-2> energy=1<keV> tilt=-0 rotation=270
315 
316 implant Phosphorus dose= $Nsd<cm-2> energy=1<keV> tilt=-0 rotation=90
317 implant Phosphorus dose= $Nsd<cm-2> energy=1<keV> tilt=-0 rotation=270
318 
319 implant Phosphorus dose= $Nsd<cm-2> energy=1<keV> tilt=-0 rotation=90
320 implant Phosphorus dose= $Nsd<cm-2> energy=1<keV> tilt=-0 rotation=270
321 
322 SetPlxList {Phosporus Boron_Implant}
323 WritePlx n@node@_NMOS_sdimp.plx y=0.03 z=0.0 Silicon
324 
325 #etch SiOCN
326 mater add name=SiCN new.like= Nitride
327 etch material= {SiCN} type=isotropic rate=1.0 time=1
328 
329 diffuse temperature=500<C> time=0.1<s>
330 
331 WritePlx n@node@_NMOS_sddiff.plx y=0.03 z=0.0 Silicon
332 
333 struct tdr= n@node@_nGAA10_SDdoping ;
334 
335 
336 #--Silicidation
337 
338 deposit material= {TiSilicide} type= isotropic rate= 0.03*$Hfin time= 1.0
339 temperature= 500 selective.materials= {Silicon}
340 
341 struct tdr= n@node@_nGAA10_Silicides ;
342 
343 #PSG ILD0
344 mater add name= PSG
345 ambient name=Silane react add
346 reaction name= PSGreaction mat.l= Phosphorus
347 mat.r= Oxide mat.new= PSG new.like= Oxide ambient.name= {Silane}
348 diffusing.species= {Silane}
349 deposit material= {PSG} type= isotropic time=1 rate= {0.2}
```

```
350 etch material= {PSG} type=cmp etchstop= {Nitride} etchstop.overetch=0.01
351
352 # Dummy gate etching
353
354 strip Polysilicon
355 strip Oxide
356
357 #---SELECTIVE ETCHING OF SIGE
358 etch material= {SiliconGermanium} type=isotropic time=1 rate= {0.1}
359
360 struct tdr= n@node@_nGAA11_etchDummySiGe;
361
362
363
364 #----RMG
365
366 #buffer oxide
367 #no used etchstop.overetch=0.01
368 deposit material= {Oxide} type= isotropic time=1 rate= {$Tiox}
369 etch material= {Oxide} type=cmp etchstop= {Silicon}
370 struct tdr= n@node@_nGAA12_newOxide;
371
372 #Hfo2
373 deposit material= {HfO2} type= isotropic time=1
374 rate= {$Tihfo2} selective.materials= {Oxide}
375
376 etch material= {HfO2} type=cmp etchstop= {Silicon}
377 struct tdr= n@node@_nGAA12_HfO2;
378
379 #refinebox name= MIG min= {-0.014 0.0 0.0} max= {-0.2 0.048 0.06}
380 xrefine=2.0<nm> yrefine= 2.0<nm> zrefine= 2.0<nm>
381
382
383 mask name= gate_neg back= ($Lsd)<um> front= ($CPP-$Lsd)<um> negative
384
385 #TiN metal stack
386
387
388
389 deposit material= {TiN} type= isotropic time=1 rate= {$TiN_rate}  mask = gate_neg
390 selective.materials= {HfO2}
391 etch material= {TiN} type=cmp etchstop =  {PSG}
392
393
394 mater add name=TaN new.like= TiN
395
396 deposit material= {TaN} type= isotropic time=1 rate= {$TaN_rate}  mask = gate_neg
397 selective.materials= {TiN}
398 etch material= {TaN} type=cmp  etchstop =  {PSG}
399
400 struct tdr= n@node@_nGAA12_TaN;
401
402 mater add name=TiAl new.like= Aluminium
```

```
403
404 deposit material= {TiAl} type=isotropic time=1 rate = {$TiAl_rate}
405 selective.materials= {TaN}
406
407 etch material= {TiAl} type=cmp coord = -0.197064 etchstop.overetch=2
408 deposit material= {TiAl} type=isotropic time=0.2 rate = {$TiAl_rate}
409 selective.materials= {TaN}
410 etch material= {TiAl} type=isotropic thickness = 0.00035
411
412 diffuse temp=250<C> time=1.0e-6<s> stress.relax
413 ambient clear
414 struct tdr= n@node@_nGAA12_TiAl;
415
416
417 # Tungsten contact
418 deposit material= {Tungsten} type=fill coord= -0.25
419 etch material= {Tungsten} type=cmp etchstop= {PSG} etchstop.overetch=0.01
420
421 struct tdr= n@node@_nGAA12_Tungsten;
422
423 #---SAC
424
425 #deposit nitride
426 mater add name= PSG
427 etch material= {Tungsten} type=isotropic time=1 rate= {0.003}
428 deposit material= {Nitride} type=fill coord=-0.25
429 etch material= {Nitride} type=cmp etchstop= {PSG} etchstop.overetch=0.1
430
431
432 mask name=s left=20<nm> right=40<nm> back=2<nm> front=10<nm> negative
433 mask name=d left=20<nm> right=40<nm> back=38<nm> front=46<nm> negative
434 mask name=g left=20<nm> right=40<nm> back=20<nm> front=28<nm> negative
435
436 #SD tungsten
437 etch material= {PSG} type=anisotropic  time=1 rate= {0.9} mask=s
438 etch material= {PSG} type=anisotropic  time=1 rate= {0.9} mask=d
439
440 #etch SAC nitride
441 etch material= {Nitride} type=anisotropic  time=1 rate= {0.2} mask=g
442 deposit material= {Tungsten} type=fill coord=-0.25
443
444 etch material= {Tungsten} type=cmp etchstop= {Nitride} etchstop.overetch=0.05
445
446 struct tdr= n@node@_nGAA13_SAC;
447
448 transform cut location= -0.05 down
449
450 # clear the process simulation mesh
451 refinebox clear
452 refinebox !keep.lines
453 line clear
454
455
```

```
456 # reset default settings for adaptive meshing
457 pdbSet Grid AdaptiveField Refine.Abs.Error 1e37
458 pdbSet Grid AdaptiveField Refine.Rel.Error 1e10
459 pdbSet Grid AdaptiveField Refine.Target.Length 100.0
460
461
462 # Set high quality Delaunay meshes
463 pdbSet Grid sMesh 1
464 pdbSet Grid Adaptive 1
465 pdbSet Grid SnMesh DelaunayType boxmethod
466 pdbSet Grid SnMesh DelaunayTolerance 5.0e-2
467 pdbSet Grid SnMesh CoplanarityAngle 179
468 pdbSet Grid SnMesh MaxPoints 2000000
469 pdbSet Grid SnMesh max.box.angle.3d 179
470
471 #gate refine silicon
472 refinebox name= gatefinal min= {-0.25 0.0 0.12} max= {-0.12 0.06 0.036}
473 xrefine=2.0<nm> yrefine= 2.0<nm> zrefine= 5.0<nm> materials= {Silicon}
474
475 #source refine silicon
476 refinebox name= sourcefinal min= {-0.25 0.0 0.036} max= {-0.12 0.06 0.48}
477 xrefine= 5.0<nm> yrefine= 5.0<nm> zrefine= 5.0<nm> materials= {Silicon}
478
479 #drain refine silicon
480 refinebox name= drainfinal min= {-0.25 0.0 0.0} max= {-0.12 0.060 0.0012}
481 xrefine= 5.0<nm> yrefine= 5.0<nm> zrefine= 5.0<nm> materials= {Silicon}
482
483 #channel refine silicon
484 refinebox name= channelfinal min= {-0.19 0.014 0.01} max= {-0.145 0.046 0.04}
485 xrefine=1.5<nm> yrefine= 1.5<nm> zrefine= 1.5<nm> materials= {Silicon}
486
487 #silicide refines
488 refinebox name= Tisource min= {-0.25 0.0 0.0} max= {-0.12 0.04 0.45}
489 xrefine= 1.5<nm> yrefine= 2.0<nm> zrefine= 3.0<nm> materials= {TiSilicide}
490
491 refinebox name= Tidrain min= {-0.25 0.0 0.0} max= {-0.12 0.04 0.0085}
492 xrefine= 1.5<nm> yrefine= 2.0<nm> zrefine= 3.0<nm> materials= {TiSilicide}
493
494 grid remesh
495
496 struct tdr= n@node@_nGAA_remesh ;
497
498 contact bottom name= bulk Silicon
499
500 contact name= gate x= -0.248 y= 0.03 z= 0.024 Tungsten
501
502 contact name= source x= -0.248 y= 0.03 z= 0.042 Tungsten
503
504 contact name= drain x= -0.248 y= 0.03 z= 0.006 Tungsten
505
506 struct tdr= n@node@_nGAAfinal_presim !Gas
507
508 exit
```

### 8.1.2 SProcess p-type NS-GAAFET script

```

math coord.ucs

math numThreads=4
AdvancedCalibration 2017.09


pdbSet Mechanics StressRelaxFactor 1

# Solver Enhancement
pdbSet Math diffuse 3D ILS.hpc.mode 4
# turn off stress relaxation after depo/etch
pdbSet Mechanics EtchDepoRelax 0

# meshing parameters
mgoals resolution= 1.0/3.0 accuracy= 1e-6
pdbSet Grid SnMesh max.box.angle.3d 175
grid set.min.normal.size= 0.005/1.0 \
 set.normal.growth.ratio.3d= 2.0 \
 set.min.edge= 1e-7 set.max.points= 1000000 \
 set.max.neighbor.ratio= 1e6


#-------------------------------------------------------
# Structure parameters, [um]
set STI      0.015                        ;# STI length
set H_STI    0.02                            ;# STI height
set Tns             0.005                                       ;# Thickness nanosheet
set Spacing  0.01                                       ;# Space between nanosheet (SiGe)
set H        [expr 4*$Spacing + 3*$Tns + $H_STI]        ;# Fin exposure
set Hfin     [expr ($H - $STI)]                               ;# Fin height
set Lg       0.012                    ;# Gate length
set HalfLg   [expr $Lg*0.5]              ;# Half gate length
set Tox      0.0025                           ;# Total thickness of gate insulator
set LSpacer  0.006                            ;# Length Spacer
set Lsd      0.012          ;# Length of S/D
# 12 lg + 6*2 spacer + 12*2 lsd
set CPP                [expr $Lg + 2*$LSpacer + 2*$Lsd] ;#Contact Pitch
set Wns                0.03                            ;#Width of NS
set FP [expr 2*$STI + $Wns] ;#Contact Pitch
set Tiox     0.001                ;#Gate dummy ox


# Doping parameters, [/cm3]

set Nsub     1.0e5                    ;#Substrate doping
set Nsd      1.0e13                    ;#SD doping [/cm2]
```

```
48  set Next     1.4e10                     ;#S/D extension doping [/cm2]
49  set Nstop    2.0e11                  ;#channel stop doping [/cm2]
50  #1.5 ext
51
52  line x location= -70.0<nm> spacing=10.0<nm> tag= SiTop
53  line x location= 20.0<nm> spacing= 10.0<nm>
54  line x location= 30.0<nm> spacing= 15.0<nm> tag= SiBottom
55
56  line y location= 0.0 spacing= 10.0<nm> tag= Left
57  line y location= $FP spacing= 10.0<nm> tag= Right
58
59  line z location= 0.0 spacing= 15.0<nm> tag= Back
60  line z location= $CPP spacing= 15.0<nm> tag= Front
61
62  #substrate
63  region Silicon xlo= SiTop xhi= SiBottom
64  ylo= Left yhi= Right zlo= Back zhi= Front substrate
65
66  init concentration=$Nsub<cm-3> field=Boron wafer.orient= {0 0 1}
67  flat.orient= {1 1 0} !DelayFullD
68
69
70  refinebox name= nw min= {-0.12 0 0.0} max= {0 0.38 0.45} xrefine= 5<nm>
71  yrefine= 10<nm> zrefine= 15<nm>
72  grid remesh
73
74  #--Epi layer with known doping concentration (well)
75
76  deposit material= {Silicon} type=isotropic time=1 rate= {$H}
77
78
79
80  deposit material= {SiliconGermanium} type=isotropic time=1 rate= {$Spacing}
81
82  deposit material= {Silicon} type=isotropic time=1 rate= {$Tns}
83
84  deposit material= {SiliconGermanium} type=isotropic time=1 rate= {$Spacing}
85
86  deposit material= {Silicon} type=isotropic time=1 rate= {$Tns}
87
88  deposit material= {SiliconGermanium} type=isotropic time=1 rate= {$Spacing}
89
90  deposit material= {Silicon} type=isotropic time=1 rate= {$Tns}
91
92  deposit material= {SiliconGermanium} type=isotropic time=1 rate= {$Spacing}
93
94
95
96  #----Sidewall Image Transfer (SIT)
97
98  #dry oxidation
99  diffuse temperature= 900<C> time= 4.0<min> O2
100
```

```
101 struct tdr= n@node@_pGAA3 ;#deposit SiO2, hardmask, mandrel
102
103 deposit material= {Nitride} type= isotropic time= 1<min> rate= {0.0165}
104 deposit material= {AmorphousSilicon} type= isotropic time= 1<min> rate= {0.1}
105
106 struct tdr= n@node@_pGAA3b ;#deposit SiO2, hardmask, mandrel
107
108 mask name= fin left= 0<nm> right= [expr $STI + $Wns] back= -1 front= 0.17<um> negative
109
110 etch material= {AmorphousSilicon} type= anisotropic time= 1<min> rate= {0.1} mask= fin
111
112 deposit material= {Oxide} type= isotropic time= 1 rate= {0.035}
113 etch material= {Oxide} type= anisotropic time= 1 rate= {0.045} isotropic.overetch= 0.1
114
115 struct tdr= n@node@_pGAA3c ;
116
117 etch material= {AmorphousSilicon} type= anisotropic time=1<min> rate= {0.3}
118 etch material= {Nitride} type=anisotropic time= 1<min> rate= {0.02}
119
120 struct tdr= n@node@_pGAA3d_etchAM;
121 #etch oxide on top of superlattice
122 etch material= {Oxide} type= anisotropic time=1 rate= {0.035}
123 etch material= {Silicon SiliconGermanium} type=anisotropic time=1<min> rate= {$H}
124
125 struct tdr= n@node@_pGAA3d_finForm;
126
127 #TEOS STI  $H+0.0165
128 mater add name=TEOS new.like=oxide
129 deposit material= {TEOS} type= isotropic time= 1<min> rate= {$H}
130
131 etch material= {TEOS} type=cmp etchstop= {Nitride} etchstop.overetch=0.0001
132 struct tdr= n@node@_pGAA3e_TEOS ;
133
134 #-etch spacers 4 fin
135 etch material= {Oxide} type= anisotropic time=1<min> rate= {0.07}
136 etch material= {TEOS} type=isotropic time=1 rate= {($H-$H_STI+0.02-0.0009)}
137
138 etch material= {Nitride} type=anisotropic time=1 rate= {0.02}
139
140 etch material= {Oxide} type= anisotropic time=1<min> rate= {0.035}
141
142 struct tdr= n@node@_pGAA3f_etchMasks ;
143
144
145 #Punch through stop layer
146
147 refinebox name= etchstop min= {-0.13 0 0.0} max= {-0.04 0.040 0.045}
148 xrefine= 4<nm> yrefine= 10<nm> zrefine= 10<nm>
149 grid remesh
150
151 #gut 20 20 25
152 implant Phosphorus dose= $Nstop<cm-2> energy=30<keV> tilt=0 rotation=90
153 implant Phosphorus dose= $Nstop<cm-2> energy=30<keV> tilt=0 rotation=270
```

```
154
155
156 SetPlxList {PTotal}
157 WritePlx n@node@_PMOS_etchstoplayer.plx y=0.03 z=0.0 Silicon
158
159 implant Phosphorus dose= $Nstop<cm-2> energy=30<keV> tilt=0 rotation=90
160 implant Phosphorus dose= $Nstop<cm-2> energy=30<keV> tilt=0 rotation=270
161
162
163 SetPlxList {PTotal}
164 WritePlx n@node@_PMOS_etchstoplayer.plx y=0.03 z=0.0 Silicon
165
166
167 implant Phosphorus dose= $Nstop<cm-2> energy=30<keV> tilt=0 rotation=90
168 implant Phosphorus dose= $Nstop<cm-2> energy=30<keV> tilt=0 rotation=270
169
170
171
172 SetPlxList {PTotal}
173 WritePlx n@node@_PMOS_etchstoplayer.plx y=0.03 z=0.0 Silicon
174
175 diffuse temperature=300<C> time=0.001<s>
176
177 struct tdr= n@node@_pGAA4_PTSLdiff
178
179
180 #Dummy gate
181 deposit material= {Oxide} type= isotropic time=1 rate= {$Tiox}
182
183 deposit material= {Polysilicon} type= fill coord= -0.25
184 struct tdr= n@node@_nGAA4_dummygatepre
185 mask name= gate back= ($Lsd+$LSpacer)<um> front= ($CPP-$Lsd-$LSpacer)<um>
186 etch material= {Polysilicon} type= anisotropic time=1 rate= {0.2} mask= gate
187
188 struct tdr= n@node@_pGAA4_dummygate
189
190
191 #S/D extension LDD
192
193 mask name= gate_neg back= ($Lsd)<um> front= ($CPP-$Lsd)<um> negative
194 photo thickness= 0.4<um> mask= gate_neg
195
196 # 2 kev -60-10 precedente buono
197 implant Boron dose= $Next<cm-2> energy=1<keV> tilt=-70<degree> rotation=90<degree>
198 implant Boron dose= $Next<cm-2> energy=1<keV> tilt=-70<degree> rotation=270<degree>
199
200 implant Boron dose= $Next<cm-2> energy=1<keV> tilt=-10<degree> rotation=90<degree>
201 implant Boron dose= $Next<cm-2> energy=1<keV> tilt=-10<degree> rotation=270<degree>
202 SetPlxList {BTotal BoronImplant}
203
204 WritePlx n@node@_NMOS_sdext.plx y=0.03 z=0.0 Silicon
205 SetPlxList {PTotal BTotal}
206 WritePlx n@node@_PMOS_sdext2X.plx y=0.03 z=0.0 Silicon
```

```
207
208 SetPlxList {PTotal BTotal}
209 WritePlx n@node@_PMOS_sdext2Y.plx x=-0.12 z=0.0 Silicon
210 strip Photoresist
211 struct tdr= n@node@_pGAA4_LDD;
212
213 strip Photoresist
214
215 #diffuse LDD RTA
216 diffuse temperature=300<C> time=0.00001<s>
217
218
219 struct tdr= n@node@_pGAA4_LDDdiff
220 #spacer fabrication
221 mask name= inner_neg back= ($Lsd+$LSpacer)<um> front=($CPP-$Lsd+$LSpacer)<um> negative
222
223 etch material= {Oxide} type=anisotropic time=1 rate=1.0
224
225 etch material= {SiliconGermanium} type= anisotropic time=1 rate= {0.18} mask= gate
226
227 struct tdr= n@node@_pGAA6_anisoetch ;
228
229 deposit material= {Oxide} type= isotropic time=1<min>
230 rate= {$Tiox} selective.materials= {PolySilicon}
231
232 etch material= {Oxide} type=cmp etchstop= {PolySilicon} etchstop.overetch=0.001
233
234
235 struct tdr= n@node@_pGAA7_sidewall ;
236
237
238 mask name= spacer_neg back= ($Lsd)<um> front= ($CPP-$Lsd)<um> negative
239
240
241 deposit material= {Nitride} type= anisotropic time=1<min> rate= {0.2} mask=spacer_neg
242
243 etch material= {Nitride} type=cmp etchstop= {PolySilicon} etchstop.overetch=0.001
244
245 struct tdr= n@node@_pGAA8_spacerfab ;
246
247 # SiOCN protection
248 mask name= spacer_neg back= ($Lsd)<um> front= ($CPP-$Lsd)<um> negative
249
250 mater add name=SiCN new.like= Nitride
251 deposit material= {SiCN} type=anisotropic time=1 rate= {0.05} mask= spacer_neg
252
253 struct tdr= n@node@_pGAA9_SiOCNprot ;
254
255 #Etch Silicon for SD epi 15 sec
256 etch material= {Silicon} type= isotropic rate= {0.01} time= 15.0<s>
257 struct tdr= n@node@_pGAA9_SietchSD ;
258
259
```

```
260 #---EPI OF SD
261
262 #To activate stress in SiGe pocket for pFinFET#
263 pdbSetDoubleArray Silicon Germanium Conc.Strain {0 0 1 -0.0425}
264 pdbSetDouble Silicon Mechanics TopRelaxedNodeCoord 0.05e-4
265
266 # Diamond shaped Si/SiGe Pocket using Lattice Kinetic Monte Carlo (LKMC)
267
268 pdbSet Grid KMC UseLines 1
269 pdbSet KMC  Epitaxy true
270 pdbSetBoolean LKMC PeriodicBC false
271 pdbSet LKMC Epitaxy.Model Coordinations.Planes
272
273
274 set EpiDoping_init  "Germanium= 1.5e21"
275 set EpiDoping_final "Germanium= 1.5e21"
276
277 temp_ramp name= epi temperature= 500<C> t.final= 550<C> time= 1<min>
278 Epi epi.doping= $EpiDoping_init epi.doping.final= #$EpiDoping_final epi.model= 1
279 epi.thickness= 0.055<um>
280
281
282
283 diffuse temp_ramp= epi lkmc
284
285 #false to model doping non atomistically
286 pdbSet KMC Epitaxy false
287
288 struct tdr= n@node@_pGAA10_SiGe_SD_epi ;
289
290
291 #gate refine silicon
292 refinebox name= gatefinal min= {-0.2 0.0 0.12} max= {-0.12 0.06 0.036}
293 xrefine=5.0<nm>yrefine= 5.0<nm> zrefine= 5.0<nm> materials= {Silicon}
294
295 #source refine silicon
296 refinebox name= sourcefinal min= {-0.25 0.0 0.036} max= {-0.12 0.06 0.48}
297 xrefine= 5.0<nm>yrefine= 5.0<nm> zrefine= 7.0<nm> materials= {Silicon}
298
299 #drain refine silicon
300 refinebox name= drainfinal min= {-0.25 0.0 0.0} max= {-0.12 0.060 0.0012}
301 xrefine= 5.0<nm> yrefine= 5.0<nm> zrefine= 7.0<nm> materials= {Silicon}
302 struct tdr= n@node@_nGAA10_SDdop_mesh ;
303
304 # S/D Implantation
305
306 #original 1
307 implant Boron dose= $Nsd<cm-2> energy=0.19<keV> tilt=-0 rotation=90
308 implant Boron dose= $Nsd<cm-2> energy=0.19<keV> tilt=-0 rotation=270
309
310
311 SetPlxList {BTotal Boron_Implant}
312 WritePlx n@node@_NMOS_sdimp.plx y=0.03 z=0.0 Silicon
```

```
313
314  #etch SiOCN
315  mater add name=SiCN new.like= Nitride
316  etch material= {SiCN} type=isotropic rate=1.0 time=1
317
318  diffuse temperature=700<C> time=1.2<s>
319
320  WritePlx n@node@_NMOS_sddiff.plx y=0.03 z=0.0 Silicon
321
322  struct tdr= n@node@_pGAA10_SDdoping ;
323
324  #--Silicidation
325
326  deposit material= {TiSilicide} type= isotropic rate= 0.025*$Hfin time= 1.0
327  temperature= 500 selective.materials= {Silicon}
328
329  struct tdr= n@node@_pGAA10_Silicides ;
330
331  #PSG ILD0
332  mater add name= PSG
333  ambient name=Silane react add
334  reaction name= PSGreaction mat.l= Phosphorus mat.r= Oxide mat.new= PSG new.like= Oxide
335  ambient.name= {Silane} diffusing.species= {Silane}
336  deposit material= {PSG} type= isotropic time=1 rate= {0.2}
337  etch material= {PSG} type=cmp etchstop= {Nitride} etchstop.overetch=0.01
338
339  # Dummy gate etching
340
341  strip Polysilicon
342  strip Oxide
343
344  #---SELECTIVE ETCHING OF SIGE
345  etch material= {SiliconGermanium} type=isotropic time=1 rate= {0.1}
346
347  struct tdr= n@node@_pGAA11_etchDummySiGe;
348
349
350  #----RMG
351
352  # HKMG refine
353  refinebox name= HKMG min= {-0.18 0.0 0.085} max= {-0.12 0.04 0.0365} xrefine= 1.0<nm>
354  yrefine= 1.0<nm> zrefine= 1.0<nm>
355  #grid remesh
356
357  #buffer oxide
358  #no used etchstop.overetch=0.01
359  deposit material= {Oxide} type= isotropic time=1 rate= {$Tiox}
360  etch material= {Oxide} type=cmp etchstop= {Silicon}
361  struct tdr= n@node@_pGAA12_newOxide;
362
363  #Hfo2
364  deposit material= {HfO2} type= isotropic time=1 rate= {$Tihfo2}
365  selective.materials= {Oxide}
```

```
366 etch material= {HfO2} type=cmp etchstop= {Silicon}
367 struct tdr= n@node@_pGAA12_HfO2;
368
369 # MIG
370
371 #TiN buffer
372
373 deposit material= {TiN} type= isotropic time=1 rate= {$TiN_rate}
374 #selective.materials= {HfO2}
375 etch material= {TiN} type=cmp coord = -0.19501
376
377 mater add name=TaN new.like= TiN
378 deposit material= {TaN} type= isotropic time=1 rate= {$TaN_rate}
379 #selective.materials= {TiN}
380 etch material= {TaN} type=cmp coord = -0.19531
381
382 struct tdr= n@node@_pGAA12_TaN;
383 #TiN main, old ESL is PSG
384
385 deposit material= {TiN} type= isotropic time=1 rate= {$TiN_rate}
386 # selective.materials= {TaN}
387 etch material= {TiN} type=cmp coord = -0.19561
388 struct tdr= n@node@_pGAA12_TiN2;
389
390 #TiAl
391 mater add name=TiAl new.like= Aluminium
392
393 deposit material= {TiAl} type= isotropic time=1 rate= {$TiAl_rate}
394 #selective.materials= {TiN}
395 etch material= {TiAl} type=cmp coord = -0.19591
396
397
398
399 diffuse temp=700<C> time=1.0e-6<s> stress.relax
400 ambient clear
401 struct tdr= n@node@_pGAA12_TiAl;
402
403
404
405
406 # Tungsten contact
407 deposit material= {Tungsten} type=fill coord= -0.25
408 etch material= {Tungsten} type=cmp etchstop= {Nitride} etchstop.overetch=0.01
409
410 struct tdr= n@node@_nGAA12_Tungsten;
411
412 #---SAC
413
414 #deposit nitride
415 etch material= {Tungsten} type=isotropic time=1 rate= {0.003}
416 deposit material= {Nitride} type=fill coord=-0.25
417 etch material= {Nitride} type=cmp etchstop= {PSG} etchstop.overetch=0.1
418
```

```
419
420 mask name=s left=20<nm> right=40<nm> back=2<nm> front=10<nm> negative
421 mask name=d left=20<nm> right=40<nm> back=38<nm> front=46<nm> negative
422 mask name=g left=20<nm> right=40<nm> back=20<nm> front=28<nm> negative
423
424 #SD tungsten
425 etch material= {PSG} type=anisotropic  time=1 rate= {0.9} mask=s
426 etch material= {PSG} type=anisotropic  time=1 rate= {0.9} mask=d
427
428 #etch SAC nitride
429 etch material= {Nitride} type=anisotropic  time=1 rate= {0.2} mask=g
430 deposit material= {Tungsten} type=fill coord=-0.25
431
432 etch material= {Tungsten} type=cmp etchstop= {Nitride} etchstop.overetch=0.05
433
434 struct tdr= n@node@_nGAA13_SAC;
435
436
437 transform cut location= -0.05 down
438
439 # clear the process simulation mesh
440 refinebox clear
441 refinebox !keep.lines
442 line clear
443
444
445 # reset default settings for adaptive meshing
446 pdbSet Grid AdaptiveField Refine.Abs.Error 1e37
447 pdbSet Grid AdaptiveField Refine.Rel.Error 1e10
448 pdbSet Grid AdaptiveField Refine.Target.Length 100.0
449
450
451 # Set high quality Delaunay meshes
452 pdbSet Grid sMesh 1
453 pdbSet Grid Adaptive 1
454 pdbSet Grid SnMesh DelaunayType boxmethod
455 pdbSet Grid SnMesh DelaunayTolerance 5.0e-2
456 pdbSet Grid SnMesh CoplanarityAngle 179
457 pdbSet Grid SnMesh MaxPoints 2000000
458 pdbSet Grid SnMesh max.box.angle.3d 179
459
460 #gate refine silicon
461 refinebox name= gatefinal min= {-0.2 0.0 0.12} max= {-0.12 0.06 0.036}
462 xrefine=2.0<nm> yrefine= 2.0<nm> zrefine= 5.0<nm> materials= {Silicon}
463
464 #source refine silicon
465 refinebox name= sourcefinal min= {-0.25 0.0 0.036} max= {-0.12 0.06 0.48}
466 xrefine= 5.0<nm> yrefine= 5.0<nm> zrefine= 5.0<nm> materials= {Silicon}
467
468 #drain refine silicon
469 refinebox name= drainfinal min= {-0.25 0.0 0.0} max= {-0.12 0.060 0.0012}
470 xrefine= 5.0<nm> yrefine= 5.0<nm> zrefine= 5.0<nm> materials= {Silicon}
471
```

```
#channel refine silicon
refinebox name= channelfinal min= {-0.19 0.014 0.01} max= {-0.145 0.046 0.04}
xrefine=1<nm> yrefine=1<nm> zrefine= 1<nm> materials= {Silicon}

#silicide refines
refinebox name= Tisource min= {-0.25 0.0 0.0} max= {-0.12 0.04 0.45}
xrefine= 2.0<nm> yrefine= 2.0<nm> zrefine= 3.0<nm> materials= {TiSilicide}

refinebox name= Tidrain min= {-0.25 0.0 0.0} max= {-0.12 0.04 0.0085}
xrefine= 2.0<nm> yrefine= 2.0<nm> zrefine= 3.0<nm> materials= {TiSilicide}

grid remesh

struct tdr= n@node@_nGAA_remesh ;

contact bottom name= bulk Silicon

contact name= gate x= -0.248 y= 0.03 z= 0.024 Tungsten

contact name= source x= -0.248 y= 0.03 z= 0.042 Tungsten

contact name= drain x= -0.248 y= 0.03 z= 0.006 Tungsten

struct tdr= n@node@_pGAAfinal_presim !Gas


```

### 8.1.3 SDevice n-type NS-GAAFET script

```

File {
*Input Files
  Grid      = "n4_nGAAfinal_presim_fps.tdr"
  Parameter = "sdevice.par"

*Output Files
  Plot      = "n@node@_tdr_nNS"
  Current   = "n@node@_nNS_transchar_tunnel50"
  Output    = "n@node@_log"

}
Electrode
{
* defines which contacts have to be treated as electrodes; initial bias
* & boundary conditions
{ name="source" Voltage=0.0 }
{ name="drain" Voltage=0.0 }
{ name="gate" Voltage=0.0 }
{ name="bulk" Voltage=0.0 }
}
Physics
```

```
23  {
24  Mobility( DopingDep
25            Enormal( RPS)
26                HighFieldSaturation )
27  EffectiveIntrinsicDensity( BandGapNarrowing( OldSlotBoom ) NoFermi )
28  Recombination ( SRH(DopingDep) Auger Band2Band ( Model = Hurkx ) )
29  }
30  Physics (Material="Silicon")
31  {
32          Aniso(eQuantumPotential(Direction(SimulationSystem)=(0,0,1)))
33  }
34  Physics (MaterialInterface = "Silicon/Oxide"){
35                                                  GateCurrent( DirectTunneling )
36
37  }
38  Plot{
39
40  *--Density and Currents, etc
41     eDensity hDensity
42     ConductionCurrentDensity
43     TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
44     eMobility/Element hMobility/Element
45     eVelocity hVelocity
46     eQuasiFermi hQuasiFermi
47     ElectrostaticPotential
48
49  *--Fields and charges
50     ElectricField/Vector Potential SpaceCharge
51
52  *--Doping Profiles
53     Doping DonorConcentration AcceptorConcentration
54
55  *--Generation/Recombination
56     SRH Band2Band Auger
57     AvalancheGeneration eAvalancheGeneration hAvalancheGeneration
58
59  *--Driving forces
60     eGradQuasiFermi/Vector hGradQuasiFermi/Vector
61     eEparallel hEparallel eENormal hENormal
62
63  *--Band structure/Composition
64     BandGap
65     MetalWorkFunction
66     BandGapNarrowing EffectiveBandGap
67     Affinity ElectronAffinity
68     ConductionBandEnergy ValenceBandEnergy
69     eQuantumPotential hQuantumPotential
70
71  #--Tunneling
72  eSchenkTunnel hSchenkTunnel
73  }
74  Math
75  {
```

```
76  coordinateSystem { UCS }
77  -CheckUndefinedModels
78  GeometricDistances
79  * use previous two solutions (if any) to extrapolate next
80  Extrapolate
81  * use full derivatives in Newton method
82  Derivatives
83  * control on relative and absolute errors
84  -RelErrControl
85  * relative error= 10^(-Digits)
86  Digits=5
87  * absolute error
88  Error(electron)=1e8
89  Error(hole)=1e8
90  * numerical parameter for space-charge regions
91  eDrForceRefDens=1e10
92  hDrForceRefDens=1e10
93  * maximum number of iteration at each step
94  Iterations=10
95  * solver of the linear system
96  Method=Pardiso
97  * display simulation time in 'human' units
98  Wallclock
99  * display max.error information
100 CNormPrint
101 * to avoid convergence problem when simulating defect-assisted tunneling
102 NoSRHperPotential
103 StressMobilityDependence=TensorFactor
104 CheckRhsAfterUpdate
105 RHSmin=1e-12
106 Number_of_Threads = 4
107 }
108 Solve {
109    *- Build-up of initial solution:
110    Coupled { Poisson }
111    Coupled (Iterations=100 LineSearchDamping=1e-4) { Poisson eQuantumPotential }
112    Coupled { Poisson Electron eQuantumPotential }
113    Coupled { Poisson Electron Hole eQuantumPotential }
114     Save ( FilePrefix= "n@node@_init" )
115 
116     NewCurrentPrefix = "n@node@_IdVd1"
117 #-- Ramp drain to VdSat
118   Quasistationary(
119     InitialStep= 0.001 MinStep= 1e-7 MaxStep= 0.025
120     Goal { Name= "drain" Voltage= 0.7 } )
121    { Coupled { Poisson Electron Hole eQuantumPotential }
122 *I-V calculated at regular intervals
123        CurrentPlot(Time=(Range=(0 1) Intervals=100))
124     }
125 
126 NewCurrentPrefix = "n@node@_IdVg1"
127 #-- Vg sweep for Vd=VdSat
128   Quasistationary(
```

```
129     InitialStep= 0.001 MinStep= 1e-7 MaxStep= 0.025
130     Goal { Name= "gate" Voltage= 0.7 } )
131     { Coupled { Poisson Electron Hole eQuantumPotential }
132 *I-V calculated at regular intervals
133        CurrentPlot(Time=(Range=(0 1) Intervals=100))
134     }
135 }
136
```

### 8.1.4 SDevice p-type NS-GAAFET script

```
1
2  File {
3  *Input Files
4    Grid      = "n4_pGAAfinal_presim_fps.tdr"
5    Parameter = "sdevice.par"
6
7
8  *Output Files
9    Plot      = "n@node@_tdrNSGAAFET"
10   Current   = "n@node@_pNSGAAFET_I"
11   Output    = "n@node@_log"
12
13 }
14 Electrode
15 {
16 * defines which contacts have to be treated as electrodes; initial bias
17 * & boundary conditions
18 { name="source" Voltage=0.0 }
19 { name="drain" Voltage=0.0 }
20 { name="gate" Voltage=0.0 }
21 { name="bulk" Voltage=0.0 }
22 }
23 Physics
24 {
25 Mobility( DopingDep
26           Enormal( RPS)
27               HighFieldSaturation )
28 EffectiveIntrinsicDensity( BandGapNarrowing( OldSlotBoom ) NoFermi )
29 Recombination ( SRH(DopingDep) Auger Band2Band ( Model = Hurkx ) )
30 }
31 Physics (Material="Silicon")
32 {
33         Aniso(hQuantumPotential(Direction(SimulationSystem)=(0,0,1)))
34 }
35 Plot{
36 *--Density and Currents, etc
37    eDensity hDensity
38    ConductionCurrentDensity
39    TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
40    eMobility/Element hMobility/Element
```

```
41     eVelocity hVelocity
42     eQuasiFermi hQuasiFermi
43     ElectrostaticPotential
44
45  *--Fields and charges
46     ElectricField/Vector Potential SpaceCharge
47
48  *--Doping Profiles
49     Doping DonorConcentration AcceptorConcentration
50
51  *--Generation/Recombination
52     SRH Band2Band Auger
53     AvalancheGeneration eAvalancheGeneration hAvalancheGeneration
54
55  *--Driving forces
56     eGradQuasiFermi/Vector hGradQuasiFermi/Vector
57     eEparallel hEparallel eENormal hENormal
58
59  *--Band structure/Composition
60     BandGap
61     MetalWorkFunction
62     BandGapNarrowing EffectiveBandGap
63     Affinity ElectronAffinity
64     ConductionBandEnergy ValenceBandEnergy
65     eQuantumPotential hQuantumPotential
66  #--Tunneling
67  eSchenkTunnel hSchenkTunnel
68  }
69  Physics (MaterialInterface = "Silicon/Oxide"){
70                                                  GateCurrent( DirectTunneling )
71
72  }
73  Math
74  {
75  coordinateSystem { UCS }
76  -CheckUndefinedModels
77  GeometricDistances
78  * use previous two solutions (if any) to extrapolate next
79  Extrapolate
80  * use full derivatives in Newton method
81  Derivatives
82  * control on relative and absolute errors
83  -RelErrControl
84  * relative error= 10^(-Digits)
85  Digits=5
86  * absolute error
87  Error(electron)=1e8
88  Error(hole)=1e8
89  * numerical parameter for space-charge regions
90  eDrForceRefDens=1e10
91  hDrForceRefDens=1e10
92  * maximum number of iteration at each step
93  Iterations=10
```

```
* solver of the linear system
Method=Pardiso
* display simulation time in 'human' units
Wallclock
* display max.error information
CNormPrint
* to avoid convergence problem when simulating defect-assisted tunneling
NoSRHperPotential
StressMobilityDependence=TensorFactor
CheckRhsAfterUpdate
RHSmin=1e-8
Number_of_Threads = 4
}
Solve {
   *- Build-up of initial solution:
   Coupled { Poisson }
   Coupled (Iterations=100 LineSearchDamping=1e-4) { Poisson hQuantumPotential }
   Coupled { Poisson Electron hQuantumPotential }
   Coupled { Poisson Electron Hole hQuantumPotential }
    Save ( FilePrefix= "n@node@_init" )

    NewCurrentPrefix = "n@node@_IdVd1"
#-- Ramp drain to VdSat
  Quasistationary(
    InitialStep= 0.001 MinStep= 1e-7 MaxStep= 0.1
    Goal { Name= "drain" Voltage= -2.0 } )
    { Coupled { Poisson Electron Hole hQuantumPotential }
*I-V calculated at regular intervals
       CurrentPlot(Time=(Range=(0 1) Intervals=100))
    }

NewCurrentPrefix = "n@node@_IdVg1"
#-- Vg sweep for Vd=VdSat
  Quasistationary(
    InitialStep= 0.001 MinStep= 1e-7 MaxStep= 0.025
    Goal { Name= "gate" Voltage= -2.0 } )
    { Coupled { Poisson Electron Hole hQuantumPotential }
*I-V calculated at regular intervals
       CurrentPlot(Time=(Range=(0 1) Intervals=100))
    }
}
```

### 8.1.5 SDevice AC-Extract n-type NS-GAAFET script

```

File {
*Input Files
```

```
4    Grid      = "n4_nGAAfinal_presim_fps.tdr"
5    Parameter = "sdevice.par"
6
7  *Output Files
8    Plot      = "n@node@_tdr_NSGAAFET"
9    Current   = "n@node@_nNSGAAFET_I"
10   Output    = "n@node@_log"
11   ACExtract = "ACplot"
12 }
13
14 Device "nNS" {
15
16 Electrode
17 {
18 * defines which contacts have to be treated as electrodes; initial bias
19 * & boundary conditions
20 { name="source" Voltage=0.0 }
21 { name="drain" Voltage=0.0 }
22 { name="gate" Voltage=0.0 }
23 { name="bulk" Voltage=0.0 }
24 }
25 Physics
26 {
27 Mobility( DopingDep
28           Enormal( RPS)
29               HighFieldSaturation )
30 EffectiveIntrinsicDensity( BandGapNarrowing( OldSlotBoom ) NoFermi )
31 Recombination ( SRH(DopingDep) Auger Band2Band ( Model = Hurkx ) )
32 }
33 Physics (Material="Silicon")
34 {
35         Aniso(eQuantumPotential(Direction(SimulationSystem)=(0,0,1)))
36 }
37
38 Plot{
39 *--Density and Currents, etc
40    eDensity hDensity
41    ConductionCurrentDensity
42    TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
43    eMobility/Element hMobility/Element
44    eVelocity hVelocity
45    eQuasiFermi hQuasiFermi
46    ElectrostaticPotential
47
48 *--Fields and charges
49    ElectricField/Vector Potential SpaceCharge
50
51 *--Doping Profiles
52    Doping DonorConcentration AcceptorConcentration
53
54 *--Generation/Recombination
55    SRH Band2Band Auger
56    AvalancheGeneration eAvalancheGeneration hAvalancheGeneration
```

```
57
58 *--Driving forces
59    eGradQuasiFermi/Vector hGradQuasiFermi/Vector
60    eEparallel hEparallel eENormal hENormal
61
62 *--Band structure/Composition
63    BandGap
64    MetalWorkFunction
65    BandGapNarrowing EffectiveBandGap
66    Affinity ElectronAffinity
67    ConductionBandEnergy ValenceBandEnergy
68    eQuantumPotential hQuantumPotential
69 #--Tunneling
70 eSchenkTunnel hSchenkTunnel
71 }
72 }
73 Math
74 {
75 coordinateSystem { UCS }
76 -CheckUndefinedModels
77 GeometricDistances
78 * use previous two solutions (if any) to extrapolate next
79 Extrapolate
80 * use full derivatives in Newton method
81 Derivatives
82 * control on relative and absolute errors
83 -RelErrControl
84 * relative error= 10^(-Digits)
85 Digits=5
86 * absolute error
87 Error(electron)=1e8
88 Error(hole)=1e8
89 * numerical parameter for space-charge regions
90 eDrForceRefDens=1e10
91 hDrForceRefDens=1e10
92 * maximum number of iteration at each step
93 Iterations=10
94 * solver of the linear system
95 Method=Pardiso
96 * display simulation time in 'human' units
97 Wallclock
98 * display max.error information
99 CNormPrint
100 * to avoid convergence problem when simulating defect-assisted tunneling
101 NoSRHperPotential
102 StressMobilityDependence=TensorFactor
103 CheckRhsAfterUpdate
104 RHSmin=1e-12
105 Number_of_Threads = 4
106 }
107 System{
108         nNS "nNS" ("bulk"=nsub "source"=ns "drain"=nd "gate"=ng)
109         Vsource_pset "vg" (ng ref) {dc=0}
```

```
110         Vsource_pset "vd" (nd ref) {dc=0}
111         Vsource_pset "vs" (ns ref) {dc=0}
112         Vsource_pset "vsub" (nsub ref) {dc=0}
113         Set (ref = 0.0)
114 }
115 Solve {
116   # initial equilibrium solution
117         Poisson
118         Coupled { Poisson Electron Hole  }
119         Plot(FilePrefix="equil")
120 
121         NewCurrentPrefix= "IDVD"
122         quasistationary (InitialStep=0.01 MaxStep = 0.5 MinStep=1e-12
123         Goal {Parameter = "vd".dc Voltage = 0.7})
124         {coupled { Poisson Contact Circuit Electron Hole }
125         CurrentPlot ( Time = (range = (0 1) intervals = 50))
126         Plot(FilePrefix = "IDVD" Time=(1.0))}
127 
128         NewCurrentPrefix= "IDVG_"
129         quasistationary (InitialStep=0.001 MaxStep = 0.1 MinStep=1e-12
130         Goal {Parameter= "vg".dc Voltage = 0.7})
131         {coupled { Poisson Contact Circuit Electron Hole }
132         CurrentPlot ( Time = (range = (0 1) intervals = 50))
133         Plot(FilePrefix = "IDVG" Time=(1.0))}
134 
135         # AC ANALYSIS
136         NewCurrentPrefix="fREQ"
137         ACCoupled (
138                 StartFrequency=1e3 EndFrequency=1e14
139                 NumberOfPoints=1000 Decade
140                 Node(nd ns ng nsub) Exclude("vg" "vs" "vd" "vsub")
141                 ACExtract = "@node@freq"
142                 )
143                 { Poisson Contact Circuit Electron Hole }
144 }
145 
146 
```

### 8.1.6 SDevice AC-Extract p-type NS-GAAFET script

```
1 
2 File {
3 *Input Files
4   Grid      = "n4_pGAAfinal_presim_fps.tdr"
5   Parameter = "sdevice.par"
6 
7 
8 *Output Files
9   Plot      = "n@node@_tdr_NSGAAFET"
10  Current   = "n@node@_nNSGAAFET_I"
11  Output    = "n@node@_log"
```

```
12    ACExtract = "ACplot"
13  }
14
15
16  Device "pNS" {
17
18  Electrode
19  {
20  * defines which contacts have to be treated as electrodes; initial bias
21  * & boundary conditions
22  { name="source" Voltage=0.0 }
23  { name="drain" Voltage=0.0 }
24  { name="gate" Voltage=0.0 }
25  { name="bulk" Voltage=0.0 }
26  }
27
28
29  Physics
30  {
31  Mobility( DopingDep
32            Enormal( RPS)
33                HighFieldSaturation )
34  EffectiveIntrinsicDensity( BandGapNarrowing( OldSlotBoom ) NoFermi )
35  Recombination ( SRH(DopingDep) Auger Band2Band ( Model = Hurkx ) )
36  }
37  Physics (Material="Silicon")
38  {
39          Aniso(hQuantumPotential(Direction(SimulationSystem)=(0,0,1)))
40  }
41
42  Plot{
43  *--Density and Currents, etc
44     eDensity hDensity
45     ConductionCurrentDensity
46     TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
47     eMobility/Element hMobility/Element
48     eVelocity hVelocity
49     eQuasiFermi hQuasiFermi
50     ElectrostaticPotential
51
52  *--Fields and charges
53     ElectricField/Vector Potential SpaceCharge
54
55  *--Doping Profiles
56     Doping DonorConcentration AcceptorConcentration
57
58  *--Generation/Recombination
59     SRH Band2Band Auger
60     AvalancheGeneration eAvalancheGeneration hAvalancheGeneration
61
62  *--Driving forces
63     eGradQuasiFermi/Vector hGradQuasiFermi/Vector
64     eEparallel hEparallel eENormal hENormal
```

```
65
66 *--Band structure/Composition
67    BandGap
68    MetalWorkFunction
69    BandGapNarrowing EffectiveBandGap
70    Affinity ElectronAffinity
71    ConductionBandEnergy ValenceBandEnergy
72    eQuantumPotential hQuantumPotential
73 #--Tunneling
74 eSchenkTunnel hSchenkTunnel
75 }
76 }
77
78 Math
79 {
80 coordinateSystem { UCS }
81 -CheckUndefinedModels
82 GeometricDistances
83 * use previous two solutions (if any) to extrapolate next
84 Extrapolate
85 * use full derivatives in Newton method
86 Derivatives
87 * control on relative and absolute errors
88 -RelErrControl
89 * relative error= 10^(-Digits)
90 Digits=5
91 * absolute error
92 Error(electron)=1e8
93 Error(hole)=1e8
94 * numerical parameter for space-charge regions
95 eDrForceRefDens=1e10
96 hDrForceRefDens=1e10
97 * maximum number of iteration at each step
98 Iterations=10
99 * solver of the linear system
100 Method=Pardiso
101 * display simulation time in 'human' units
102 Wallclock
103 * display max.error information
104 CNormPrint
105 * to avoid convergence problem when simulating defect-assisted tunneling
106 NoSRHperPotential
107 StressMobilityDependence=TensorFactor
108 CheckRhsAfterUpdate
109 RHSmin=1e-12
110 Number_of_Threads = 4
111 }
112
113 System{
114         pNS "pNS" ("bulk"=nsub "source"=ns "drain"=nd "gate"=ng)
115         Vsource_pset "vg" (ng ref) {dc=0}
116         Vsource_pset "vd" (nd ref) {dc=0}
117         Vsource_pset "vs" (ns ref) {dc=0}
```

```
118         Vsource_pset "vsub" (nsub ref) {dc=0}
119         Set (ref = 0.0)
120 }
121
122 Solve {
123   # initial equilibrium solution
124         Poisson
125         Coupled { Poisson Electron Hole  }
126         Plot(FilePrefix="equil")
127
128         NewCurrentPrefix= "IDVD"
129         quasistationary (InitialStep=0.01 MaxStep = 0.5 MinStep=1e-12
130         Goal {Parameter = "vd".dc Voltage = -0.7})
131         {coupled { Poisson Contact Circuit Electron Hole }
132         CurrentPlot ( Time = (range = (0 1) intervals = 100))
133         Plot(FilePrefix = "IDVD" Time=(1.0))}
134
135         NewCurrentPrefix= "IDVG_"
136         quasistationary (InitialStep=0.001 MaxStep = 0.1 MinStep=1e-12
137         Goal {Parameter= "vg".dc Voltage = -0.7})
138         {coupled { Poisson Contact Circuit Electron Hole }
139         CurrentPlot ( Time = (range = (0 1) intervals = 100))
140         Plot(FilePrefix = "IDVG" Time=(1.0))}
141
142
143         # AC ANALYSIS
144         NewCurrentPrefix="FREQ"
145         ACCoupled (
146                 StartFrequency=1e3 EndFrequency=1e14
147                 NumberOfPoints=1000 Decade
148                 Node(nd ns ng nsub) Exclude("vg" "vs" "vd" "vsub")
149                 ACExtract = "@node@freq"
150                 )
151                 { Poisson Contact Circuit Electron Hole }
152 }
153
```

## 8.2 Modified BSIM-CMG-NS code

### 8.2.1 BSIM-CMG-NS n-type NS-GAAFET code, body

```

      //DEFINITION PARAMETERS FOR MODIFICATION
       Nsh = 3;
       tsp = 10e-9;//m
       Hstack = Nsh * HFIN + (Nsh)* (tsp);
       Epseq = 0;

      NBODY_AV = (NBODY_top + NBODY_mid +NBODY_bottom) /Nsh;
      NSD_AV = (NSD_top + NSD_mid +NSD_bottom) /Nsh;
      // Constants
      if ( TYPE == ntype ) begin
         devsign  =  1;
      end else begin
         devsign  =  -1;
      end

      epssub     =  EPSRSUB * EPS0;
      epssp      =  EPSRSP * EPS0;
      cbox       =  EPSROX * EPS0 / EOTBOX;
      epsratio   =  EPSRSUB / EPSROX;
//////////////////////////////////////////////////
       2: begin // Quadruple Gate
                if (!$param_given(TFIN_TOP) || !$param_given(TFIN_BASE)) begin
                    Weff_UFCM   = Nsh * (2.0 * HFIN + 2.0 * TFIN*FECH);

                Epseq = ( (TIL * EPSROX * EPS0 ) + (THK * EPSRHK * EPS0 ) ) /(THK+TIL);
                    Cins   =  Weff_UFCM * Epseq / (THK+ TIL);
                    Ach    =  Nsh* HFIN * TFIN;
                    rc     =  (2.0 * Cins / (Weff_UFCM * Weff_UFCM * epssub / Ach));
                    Qdep_ov_Cins   =  -`q * NBODY_i * Ach / Cins;
                end else begin
                    Weff_UFCM   =  2.0 * sqrt(HFIN * HFIN +
                    (TFIN_TOP - TFIN_BASE) * (TFIN_TOP - TFIN_BASE) / 4.0) +
                    TFIN_TOP + TFIN_BASE;
                    Cins   =  Weff_UFCM * EPSROX * `EPS0 / EOT;
                    Ach    =  HFIN * (TFIN_TOP + TFIN_BASE) / 2.0;
                    rc     =  (2.0 * Cins / (Weff_UFCM * Weff_UFCM * epssub / Ach));
                    Qdep_ov_Cins   =  -`q * NBODY_i * Ach / Cins;
                end
            end
      //////////////////////////////////////////////////

      // Vgs Clamping for Inversion Region Calculation in Accumulation
          u0_av = (U0_top + U0_mid +U0_bottom) /Nsh;
      beta0      =  u0_av * cox * Weff0 / Leff;
      T0         =  -(dvch_qm +
      nVtm * lln(2.0 * cox * Imin / (beta0 * nVtm * `q * Nc * TFIN)));
      T1         =  vgsfb + T0 + DELVTRAND;
```

```
      vgsfbeff  =  hypsmooth(T1 , 1.0e-4) - T0;

```

### 8.2.2 BSIM-CMG-NS p-type NS-GAAFET code, body

```

      //DEFINITION PARAMETERS FOR MODIFICATION
       Nsh = 3;
       tsp = 10e-9;//m
       Hstack = Nsh * HFIN + (Nsh)* (tsp);
       Epseq = 0;


      NBODY_AV = (NBODY_top + NBODY_mid +NBODY_bottom) /Nsh;
      NSD_AV = (NSD_top + NSD_mid +NSD_bottom) /Nsh;
      NSDE_AV = (NSDE_top + NSDE_mid +NSDE_bottom) /Nsh;


      // Constants
      if ( TYPE == `ntype ) begin
         devsign  =  1;
      end else begin
         devsign  =  -1;
      end

      epssub     =  EPSRSUB * `EPS0;
      epssp      =  EPSRSP * `EPS0;
      cbox       =  EPSROX * `EPS0 / EOTBOX;
      epsratio   =  EPSRSUB / EPSROX;

////////////////////////////////////
      2: begin // Quadruple Gate
                if (!$param_given(TFIN_TOP) || !$param_given(TFIN_BASE)) begin
                    Weff_UFCM  = Nsh * (2.0 * HFIN + 2.0 * TFIN*FECH);

                Epseq = ( (TIL * EPSROX * `EPS0 ) +
  (THK * EPSRHK *`EPS0 ) ) /(THK+TIL) ;
                    Cins   =   Weff_UFCM * Epseq / (THK+ TIL);

                    Ach   =   Nsh* HFIN * TFIN;
                    rc    =   (2.0 * Cins / (Weff_UFCM * Weff_UFCM * epssub / Ach));
                    Qdep_ov_Cins   =   -`q * NBODY_i * Ach / Cins;
                end
                else begin
          Weff_UFCM  =  2.0 * sqrt(HFIN * HFIN + (TFIN_TOP - TFIN_BASE) *
          (TFIN_TOP - TFIN_BASE) / 4.0) +          TFIN_TOP + TFIN_BASE;
                    Cins   =   Weff_UFCM * EPSROX * `EPS0 / EOT;
                    Ach    =   HFIN * (TFIN_TOP + TFIN_BASE) / 2.0;
                    rc     =   (2.0 * Cins / (Weff_UFCM * Weff_UFCM * epssub / Ach));
                    Qdep_ov_Cins   =   -`q * NBODY_i * Ach / Cins;
                end
```

```
47             end
48 /////////////////////////////////////
49
50      u0_av = (U0_top + U0_mid +U0_bottom) /Nsh;
51       beta0     =  u0_av * cox * Weff0 / Leff;
52       T0        =  -(dvch_qm + nVtm *
53       lln(2.0 * cox * Imin / (beta0 * nVtm * `q * Nc * TFIN)));
54       T1        =  vgsfb + T0 + DELVTRAND;
55       vgsfbeff  =  hypsmooth(T1 , 1.0e-4) - T0;
56
57
58
59
```

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