POLITECNICO DI TORINO

Electronic Engineering

Master thesis

Characterization and design of high frequency SPDT switch working in a 8-14 GHz band

Gabriele Abate

Graduand:
Gabriele Abate

Supervisors:
Marco Pirola
Jesus Grajal de la Fuente

Acknoledgments

I dedicate this work to those who have significantly contributed to my academic and personal development: to my family, who have been by my side the whole time—my mother Letizia, my father Emanuele, and my sister Grace.

Secondly, I'd like to extend my heartfelt thanks to the friends I made during my academic journey. A special mention goes to my dear friend Taus, to Zoe, and to the friends I met during my year abroad in Spain, especially my dear friend Sofia. Their support and companionship made this experience unforgettable.

Lastly, I dedicate this work and give thanks to my supervisor, Jesús Grajal, for his invaluable help and dedication throughout this project. I also extend my gratitude to Marta Ferreras Mayo and all the members of SSR for giving me the opportunity to complete this project.

Contents

Introduction

The following thesis focuses on the redesign and characterization of a high-frequency switch intended for use in a T/R Module. It begins with an existing implementation of a Single-Pole Double-Throw (SPDT) Radio frequency (RF) switch circuit operating in the 6 to 18 GHz frequency band, aiming to enhance all relevant performance metrics at the cost of reducing the operating band to 8-14 GHz. The design integrates Gallium Nitride (GaN) technology on a Silicon Carbide (SiC) substrate, chosen for its superior power-handling capabilities and low substrate leakages. Advanced simulation tools are used to optimize the switch's performance parameters, including insertion loss, isolation, and return loss across the target frequency band. Additionally, Monte Carlo analysis will be crucial in determining the robustness of the system when facing manufacturing uncertainties of the components that are part of the switch. Additionally, the transient analysis of the switch will be performed to determine the maximum switching times possible, and optimization strategies to increase the overall velocity of operation. Finally, to validate the design, measurements of a real RF switch with similar properties will be conducted in a laboratory setting, and the results will be analyzed.

1 High frequency electronics switches

1.1 Introduction

The objective of this presentation is to introduce the reader to the technology currently used for modern day electronics switches for high frequency applications, along with its respective challenges and advantages in the perspective of an implementation in a Transmitter/Receiver RF module. As an example, Figure 1 shows the final T/R module layout of the MUSTANG project developed by the Microwave and Radar Group (GMR) at the Polytechnic University of Madrid [1].

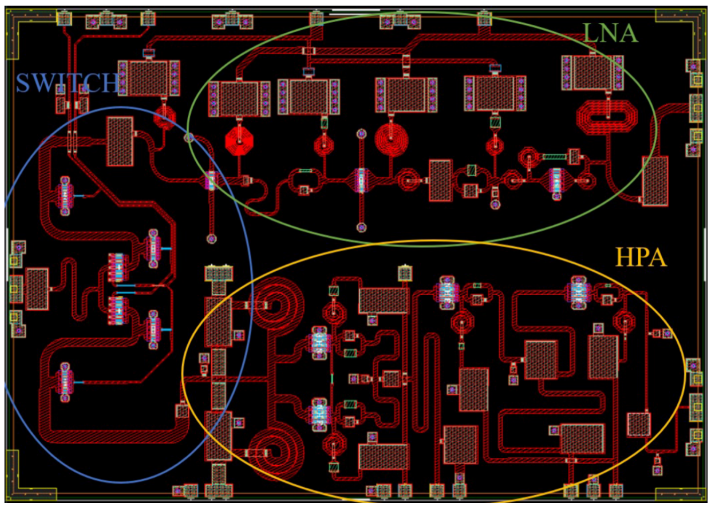


Figure 1: Example of a GaN integrated T/R module

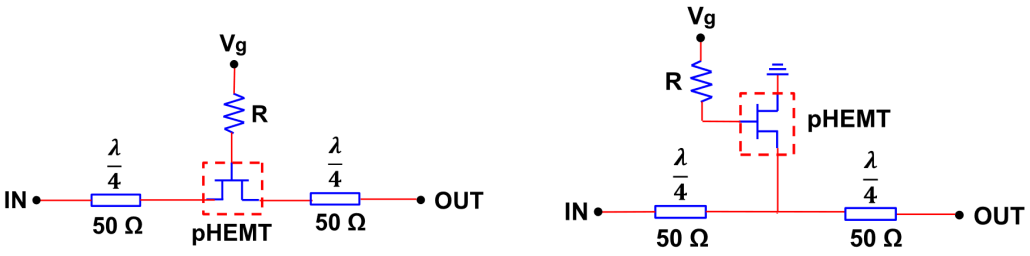
1.2 Operation of high frequency electronics switches

Modern day implementations of high frequency switches are subordinate to the use of MOSFETs, more specifically of pHEMTs, which thanks to their high carrier mobility and low parasitic capacitance, are well-suited for high-frequency applications. A series resistor, R, is normally added to the gate driver of the pHEMT to prevent RF signal leakage, and also to provide isolation between the RF signal path and DC control path[2]. The two basics configurations in use are the one presented in figure 2:

- Series configuration: When the voltage V_g is lower than the threshold voltage of the HEMT V_{th}, the transistor will be in the cut-off region, meaning that it can be modelled as a high value impedance, not allowing any signal to go through the channel(OFF State). When it is indeed higher than V_{th}, the transistor will be in the saturation region, meaning that it will behave like a small variable resistance R_{ON} whose value will depend on the size of the channel[3]. Such short circuit-like behaviour allow any signal to go from the input to the output port(ON State).

- Shunt configuration: When V_g is lower than the threshold voltage V_th the transistor will adopt an open circuit behaviour, making the signal go from the input to the output port indisturbed(ON State). When V_g is higher than V_th it will behave like an

ideal short circuit, allowing a small resistance passage for the signal coming from the input port to the ground node, thus eliminating any communication with the output port(OFF State).



(a) Series configuration

(b) Shunt configuration

Figure 2: Basic configurations for implementation of RF switches

Typically, the series pHEMT switch has higher insertion loss than shunt pHEMT switch over the whole frequency range. This is due to the higher ohmic contact resistance of the pHEMT. Therefore, the shunt pHEMT switch is considered more lenient to high 'ON' state resistance and is suitable to be used in a low-loss switch design. On the other hand, the isolation of series pHEMT switch is better than the shunt one at low-frequency range. However, its isolation was found to decrease at higher frequencies due to higher drain- source capacitance of the pHEMTs[2]. In order to obtain a compromise between both losses and isolation, in the designs that will be presented next, both configurations will be implemented.

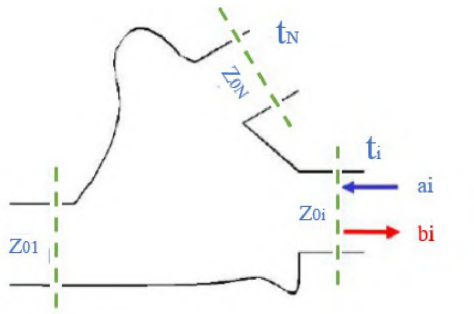
1.3 Parameters of interest

1.3.1 Linearity parameters

Taking as a reference one of the configurations of figure 2 and modelling it as a two ports device, the scattering matrix can be defined. Such matrix relates the incident power wave with the reflected power wave impinging on the ports of a microwave circuit. The S-parameters are used to describe the frequency response in linear or linearized(through small signal models) microwave devices, the linearity is given by the fact that the power is small enough to ensure that the output is directly proportional to the input[4]. They are defined as follow in 1.[4]

$$S_{ij} = \frac{b_i}{a_j} \tag{1}$$

Where a_j is the normalized incident power wave at port j, b_i is the normalized reflected power wave at port i. Furthermore a_i is the only incident power wave in the system, with the other ports all terminated with an impedance Z_{0n}(as in 3a).



(a)

$$\begin{pmatrix} b_1 \\ b_2 \\ b_3 \\ \dots \\ b_n \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} & S_{13} & \dots & S_{1n} \\ S_{21} & S_{22} & S_{23} & \dots & S_{2n} \\ S_{31} & S_{32} & S_{33} & \dots & S_{3n} \\ \dots & \dots & \dots & \dots & \dots \\ S_{n1} & S_{n2} & S_{n3} & \dots & S_{nn} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \\ a_3 \\ \dots \\ a_n \end{pmatrix}$$

(b)

Figure 3: S-Parameters matrix

The term of the scattering matrix can be used to define the important parameters which quantify the performances of the switch:

- The insertion loss(IL) is defined as the ratio between the incident power at port i and the power delivered at a different port j. If the load impedances of each of these ports match the impedance the S-parameter matrix has been defined with, the following relationship is reached:

$$IL_{i\to j}(dB) = 10 \cdot log_{10}(\frac{1}{|S_{ji}^2|}) = -20 \cdot log_{10}(|S_{ji}|) \tag{2}$$

- The return losses (RL) can be defined as the ratio between the incident power at port i and the power delivered at the same port. If the load impedances of each of these ports match the impedance the S-parameter matrix has been defined with, the following relationship is reached:

$$RL_{i\to i}(dB) = 10 \cdot log_{10}(\frac{1}{|S_{ii}^2|}) = -20 \cdot log_{10}(|S_{ii}|) \tag{3}$$

- The Isolation (Iso) is a particular case of insertion losses. It is defined similarly to IL (power injected at port i versus power delivered at port j), but it is measured at a port j, which is not supposed to receive any power.

$$Iso_{i\to j}(dB) = 10 \cdot log_{10}(\frac{1}{|S_{ji}^2|}) = -20 \cdot log_{10}(|S_{ji}|) \tag{4}$$

1.3.2 Non-Linearity parameters

Carrying out a Non-linear analysis means bringing the input power to a high enough power level so that the output is not directly proportional to the input anymore.[4] Two more parameters which help in evaluating the linearity of the switch are the 1 dB compression point(P1db) and the third-order intermodulation distortion (IMD3). The 1dB compression point in a single tone test is defined as the point at the output of the amplifier where the gain has decreased by 1dB compared to the gain in linear operation, which is the ideal behavior under small-signal conditions[5]. The meaning of this definition is illustrated in figure 4. The 1dB compression point will be the input power point (IP_{1dB}) or output power

point (OP_{1dB}) at which the output power has dropped by 1 dB compared to the ideal gain line.
Unlike the P1db, the third-order intermodulation distortion (IMD3), can be defined in the case of a two tones test as the power ratio of the third-order intermodulation component to the fundamental frequency component. Figure 5 provides clarification on such definition.

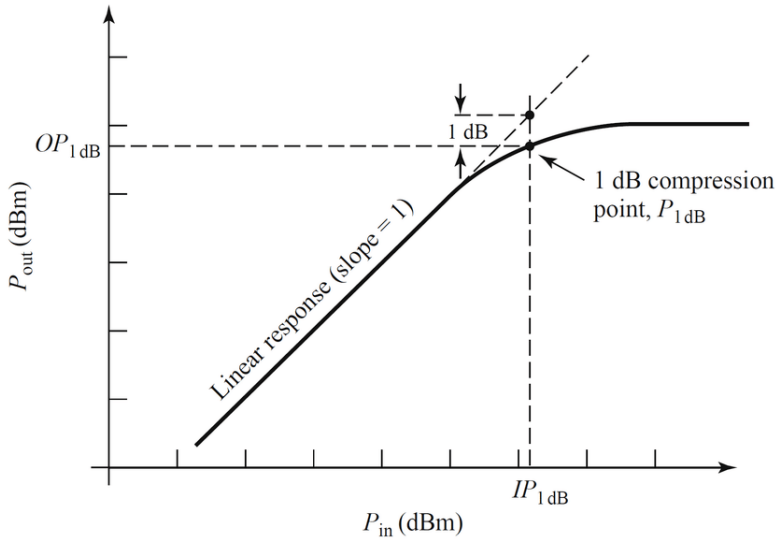


Figure 4: 1 dB compression point

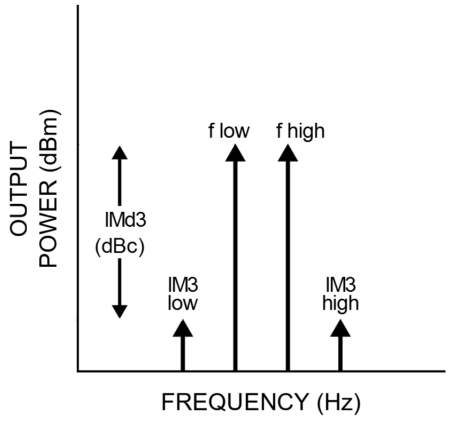
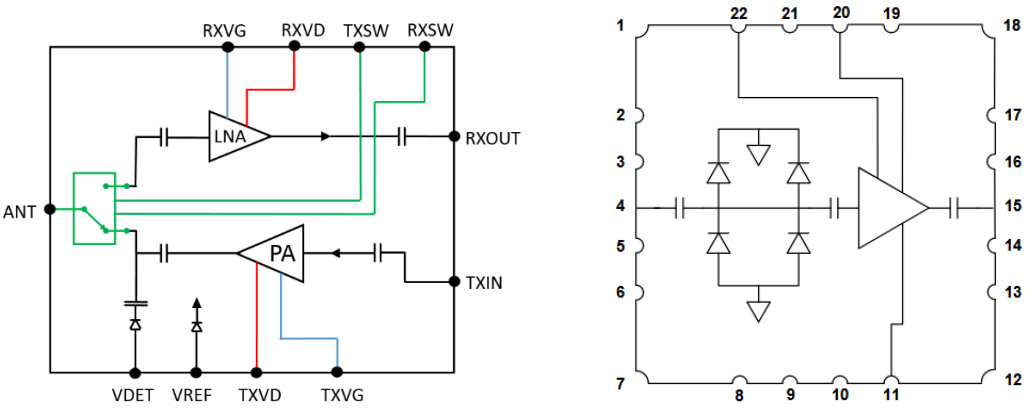


Figure 5: Third-order intermodulation distortion

1.4 Technological features

Working in the microwaves band makes the use of microstrip technology imperative, in particular the switch in question is integrated with Gallium Nitride technology(GaN)[6]. GaN is a semiconductor compound that, in combination with a silicon substrate (GaN-on-Si) or a silicon carbide substrate (GaN-on-SiC), has gained significant relevance in the field of power devices. This is all thanks to its high breakdown voltage which allows a higher value of control voltage V_g and a larger RF input power swing. Furthermore a higher value

of I_{max} allow for a lower channel resistance, thus further reducing channel losses along with an increase of the possible maximum current swing[7]. A reduction of the substrate leakages is also achieved due to the presence of the insulating SiC substrate. The main difference that can be observed when compared to its competitor, the GaAs technology, is unlike how shown in figure 1, the complete omission of the diodes limiter right before the low noise amplifier and after the switch. In 6a can be seen the configuration of a T/R Module in GaN technology of a commercial circuit, as it can be seen the limiter has been removed, whereas in 6b is shown the commercial circuit schematic of a limiter and of a LNA, typical when working with GaAs technology. Thanks to the high breakdown voltage the presence of the limiter which should keep the voltage below the maximum operativity threshold is not required, this comes with the disadvantage of the GaN technology being overall noisier than GaAs, such difference is however insignificant due to the presence in the latter of the limiter, which in the receiving chain, according to the Friis relationship, causes an increase of the noise figure. Finally, it can be stated that GaN offers higher efficiency at high frequencies and power levels, but it does however imply higher overall costs.



(a) GaN typical configuration

(b) GaAs typical configuration

Figure 6: GaN and GaAs configurations comparison

1.5 Optimization techniques

In this section, a simulation was carried out through the Advanced Design System (ADS) tool and the components provided by the manufacturer in its process design kit (PDK). The PDK is a set of tools and models with their respective documentation provided by manufacturers to integrated circuit designers, and that in this instance will be used to model the behaviour of the HEMT transistors used for the switch. The model allows modifying the total gate width (Wt = Wu*Nf) by either adjusting the number Nf of gates (fingers) of the transistor or by adjusting the width Wu of each finger. The topology used for the simulation in question is the one show in figure 7, it is totally symmetric and as it has been anticipated, shunt and series configurations have been placed together in order to have higher degrees of freedom on both the isolation and the insertion losses. By manipulating the gate width of either the shunt or the series branch, the behaviour of the parameters of interest which have been introduced in section 1.3 will be analyzed.

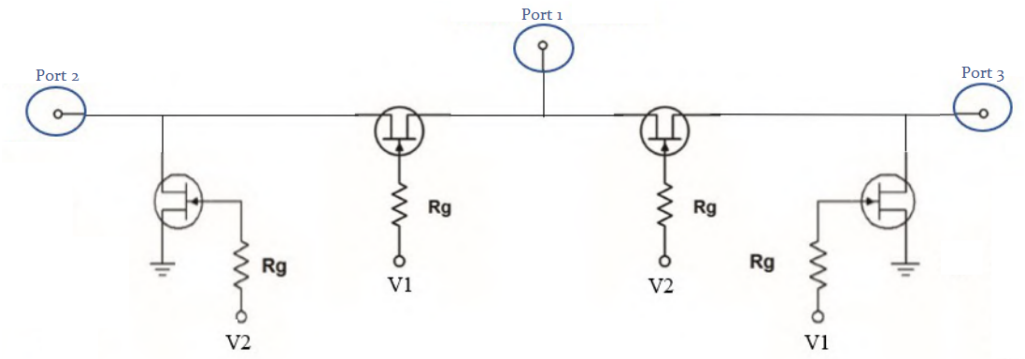
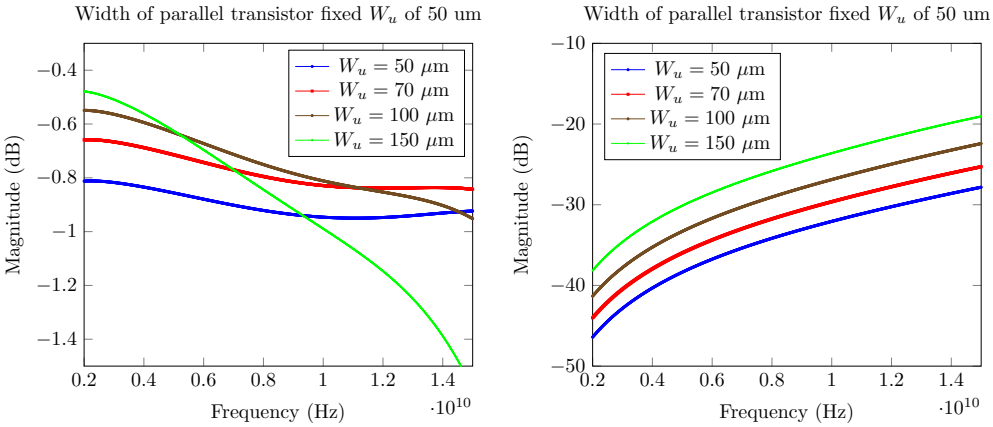


Figure 7: Simulated circuit topology

1.5.1 Linear analysis

In the following part the gate width of the transistors in series is changed in a range going from 50 μm to 150 μm(the parallel transistor size is left at 50 μm), to see how it affects the isolation and the insertion loss. In figure 8a it is evident how increasing the width of the transistor Wu corresponds to better performances in terms of insertion loss, which decreases[8] from 1.8 @$W_u = 20\mu m$ and reaches 0.7 @$W_u = 150\mu m$. This happens as a consequence of the fact that by increasing the width of the series transistor, which is the transistor responsible for most of the insertion losses, also the resistance of the channel decreases, meaning overall less lost power when the information exchange takes place. It must be noted however how the shape of the insertion loss appear to be changing when the width of the transistor changes, this is because the more the width increases the more the parallel parasitic capacitance of the transistor increases[8], thus the frequency response of the system is affected by the presence of this variable dynamic component. One more effect that can be attributed to the increase of the parasitic capaticance is the decrease of the isolation, which as shown in figure 8b(S_{31} and S_{32} are identical due to the symmetry of the circuit) becomes worse the more W_u increases. This is because the capacitance provides a way for the signal to leak to port 3.

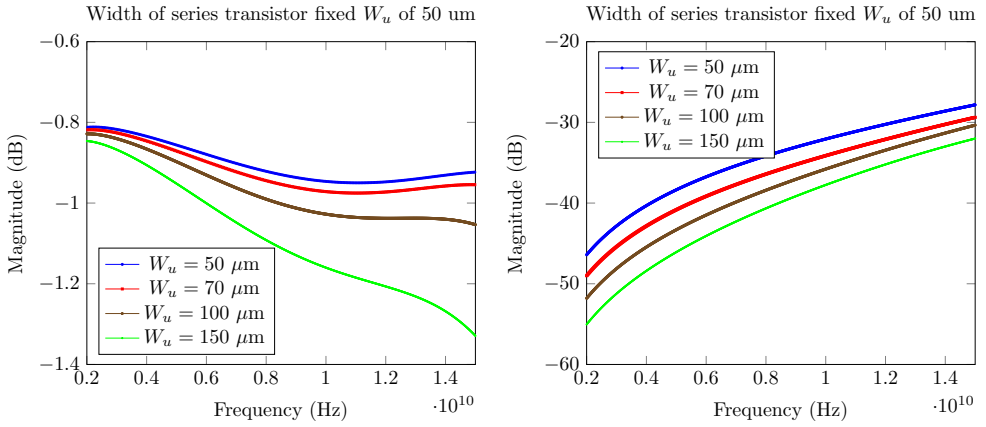


(a) $|S_{21}|$ (Related to insertion loss) (b) $|S_{31}|$ and $|S_{32}|$ (Related to isolation)

Figure 8: Performances tuning of series transistor width with fixed parallel transistor width $W_u = 50\ \mu$m

.

Now, the gate width of the transistors in shunt configuration is changed in a range going from 50 μm to 150 μm(the series transistor size is left at 50 μm), and once again the isolation and insertion loss are analyzed. No big differences can be evaluated for the insertion loss as shown in 9a, It appears however from the isolation scheme of 9b that the isolation increases the more W_u of the parallel transistor increases, this is supposedly due to the reduction of the channel resistance, which in this way facilitate the unwanted signal routing towards the ground. This in the end proves that the parallel transistors are mostly responsible for the isolation performances. Notice however how the bandwidth as shown in the behaviour of the insertion losses decreases with increasing W_u, this is due to the increasing parasitic capacitance. This can be better proved by looking at the low frequency region which doesn't experience any variations as the capacitance doesn't operate at low frequencies.

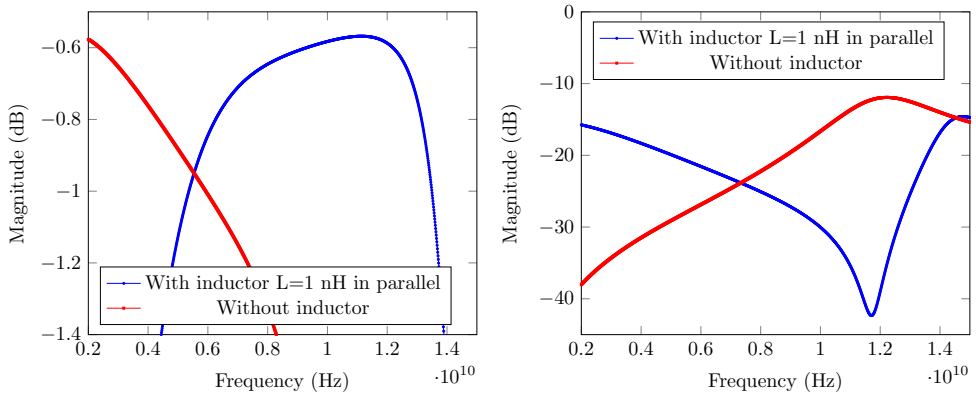


(a) $|S_{21}|$ (Related to insertion loss) (b) $|S_{31}|$ and $|S_{32}|$ (Related to isolation)

Figure 9: Performances tuning of parallel transistor width with fixed series transistor width $W_u = 50\ \mu$m

.

The problems introduced by the increase of the parallel capacitance of the transistor could be tackled by the introduction of a parallel inductance which is supposed to be in parallel with the transistors in series configuration, the inductance value has to be chosen to resonate at the upper side of the frequency band of interest so as to increase the isolation of the switch[9]. Thanks to this addiction, the maximum frequency of operation of the switch is increased. However, this topology is only applicable to pass-band designs, which will align with the design presented in the following chapters.



(a) $|S_{21}|$ (Related to insertion loss)

(b) $|S_{31}|$ and $|S_{32}|$ (Related to isolation)

Figure 10: Comparison with classical topology with series switch width W_u=30 μm, parallel switch width W_u=50 μm and an inductor L=1 nH in parallel to the switch transistor

.

1.5.2 Non-Linear analysis

When trying to move the position of the compression point higher, it appears that changing the width of the transistors in shunt configuration doesn't influence significantly such parameter. A few results collected through tuning the series transistor size W_{u2} in a range going from 50 μm to 150 μm(the parallel transistor size W_{u1} is left at 50 μm) can be observed in the figure below. From the data obtained, the compression point is optimized with a series transistor width as high as possible, it must be however noted that over a certain value of width, the curve seem to stabilize and it eventually reaches saturation. In conclusion such parameter is independent of the shunt transistor width, and can be optimized changing the series transistor width only.

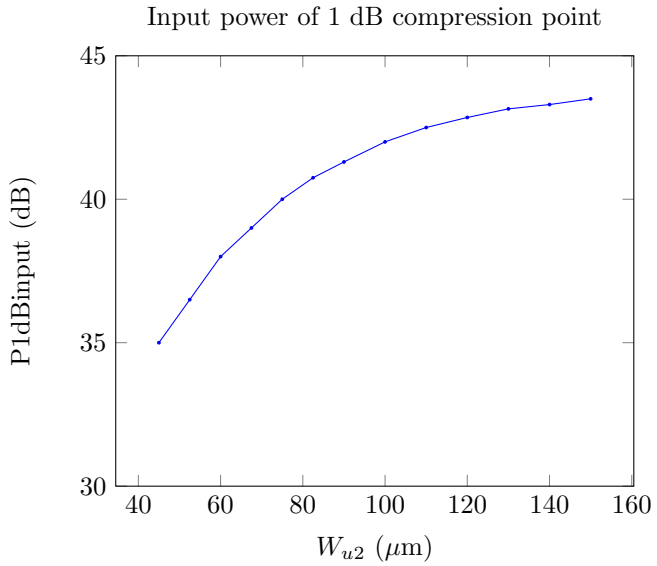


Figure 11: Behaviour of the P1db factor in function of the series switch width (W_{u2})

1.6 Consideration on the asymmetry of the switch

The main goal of the design of the switch is to obtain a viable option for the implementation on a T/R Module, whose ideal schematic can be seen in figure 12. Therefore it is interesting to take into consideration how a non-symmetric design might indeed provide better overall performances. For this purpose let's consider the two branches of the module:

- In the transmission branch, the switch will allow RF signals to pass from the HPA output to the antenna, but not to the LNA input port. Therefore, the switch must operate in a linear regime for the HPA output power, presenting low levels of return and insertion losses, as well as good isolation with respect to the receiver.
- In the reception branch, the switch will allow RF signals to pass from the antenna port to the input of the LNA, but not to the output port of the HPA. The critical parameter will be the small-signal insertion losses, as they will affect the receiver's noise figure.

In light of this, each branch will be designed differently in order to optimize for each branch its own relevant parameters.

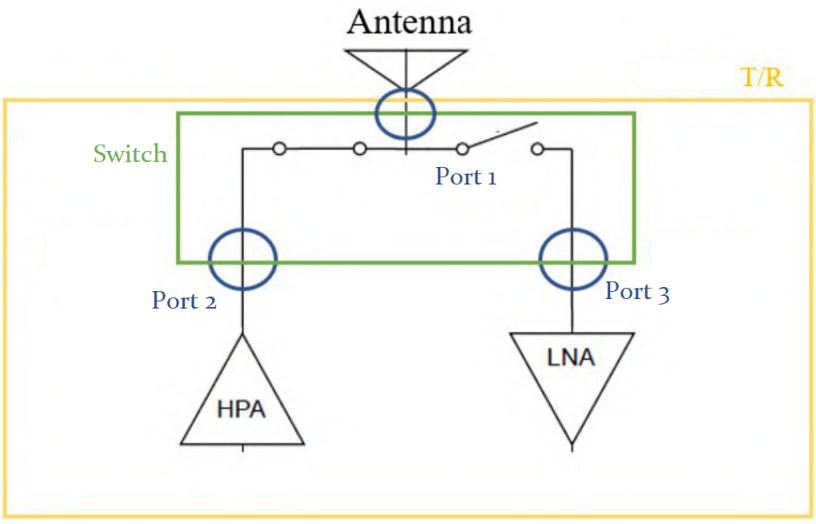


Figure 12: T/R Module branches

2 Radio frequency switch design

2.1 Introduction

This part will be devoted to the redesign of a previously designed high frequency switch satisfying the specifications which are presented in table 2.1. Such switch works with the same technology hereby presented. The goal of the redesign is improving the performances as much as possible of the parameters that have been highlighted in red. This implies achieving a lower insertion loss, a higher isolation, P1db and return losses. Such parameters will be optimized at the cost of the working bandwith, which instead of being 12 GHz wide, will now be shrinked to a 8-14 GHz bandwidth, between band X and band Ku.

Parameter	Initial design
Insertion loss	1.25 dB
Return loss on activated line	12 dB
Isolation	37 dB
1 dB input power compression point	40 dBm
Working bandwidth	6-18 GHz

In order to evaluate the state of art of the technology in use and in this way to evaluate the selected figures of merit to optimize, here will follow a comparison with two commercially available high frequency switch working in the X-Ku band.

Parameter	Typical value
Frequency range	8-12 GHz
Insertion loss	1.18 dB
Input return loss	14 dB
Output return loss	14 dB
Isolation	34 dB
Input Power (P0.1dB)	41.7 dBm

Table 1: QPC2040 commercial SPDT switch[10]

Parameter	Typical value
Frequency range	DC-18 GHz
Insertion loss	1.5 dB
Input return loss	17 dB
Output return loss	17 dB
Isolation	46 dB
Input Power (P1dB)	23 dBm

Table 2: CMD196C3 commercial SPDT switch[11]

As can be seen from the datasheets in 1 and 2. the QPC2040 switch employs the same GaN on SiC technology, therefore the parameters of interest are in line with the values present in table 2.1, the main difference with the CMD196C3 is the lower amount of power it can withstand without compression, which is a positive point that has been highlighted in favour of the GaN technology. As analyzed in the previous section, there is further room of improvement thanks to the introduction of a losses compensating inductor in parallel to the series transistor. As it will be seen with the design, such improvement will be more evident for the insertion loss.

2.2 The design instruments

2.2.1 Harmonic Balance

The harmonic balance (HB) is an iterative circuit-solving technique that combines time-domain and frequency-domain analysis to simulate the effects of nonlinear distortion in

circuits and systems subjected to periodic excitation[12]. Typically, the solving algorithm makes an assumption about the voltages at the circuit nodes, and then the currents of the linear part are analyzed in the frequency domain while the nonlinear currents are resolved in the time domain. By transforming the nonlinear part into the frequency domain using a Fourier transform, it is checked whether the incoming currents to the circuit nodes sum to zero (Kirchhoff's Law). If not, the initial assumption about the voltages at the circuit nodes was incorrect and the initial assumption must be modified, iterating over the process until the error of the Kirchhoff's rule is negligible[12].

In ADS, this technique can be applied using either the Harmonic Balance (HB) controller or the Large-Signal S-Parameter (LSSP) controller. It is important to mention that the analysis is limited by truncation due to using finite Fourier series. Therefore, an important point when using the harmonic balance controller is to choose the number N of harmonics used as a compromise for time-precision compensation of the simulation.[13]

2.2.2 Large signal S-Parameters

In order to carry out a large-signal analysis in the designs of chapters that follow, the usual definition of the S-parameters developed in the previous section will be extended to the realm of large signal. The concept remains the same: relating the reflected/transmitted power to port j with the incident power on port i. However, a different S-parameter matrix will be obtained for each input power excited at port i because it will take into account nonlinear effects such as output power compression. The large-signal S-parameters must be calculated using a large-signal simulation technique such as harmonic balance. In ADS, they will be obtained with the harmonic balance or large-signal S-parameter controllers.

When analyzing the S-parameters in the large-signal realm in the chapters that follow, they will be referenced in the graphs as S_{ij} HB. This way, reference is made to harmonic balance by its initials HB.

2.2.3 Electromagnetic co-simulation

A crucial point in the design of high frequency circuits is the electromagnetic analysis of distributed elements in the circuit, such as transmission lines, inductors, or capacitors. Electromagnetic analysis allows for considering effects that cannot be analytically modeled by components included in ADS libraries and the manufacturer's PDK, as well as identifying parasitic electromagnetic coupling that occurs due to the proximity between nearby elements in space. To perform this analysis, the electromagnetic simulator of planar structures included in the ADS design environment, called ADS Momentum[14], will be used. This simulator uses the method of moments (MoM)[15] and has two operating modes: Momentum RF for efficiently simulating electrically small circuits, and Momentum Microwave for more accurate simulation as frequency increases and effects such as radiation or substrate waves begin to appear. In general, throughout the simulations and optimizations of the chapter that follow, the Momentum Microwave method has been used to achieve greater accuracy.

Electromagnetic analysis should only be performed on passive elements. Therefore, transistors will continue to be simulated from the schematic using PDK models. This joint simulation of electromagnetically simulated elements and circuit elements (e.g., nonlinear

devices) that cannot or are not suitable to be simulated from their layout is known as "electromagnetic co-simulation." In ADS, it is possible to create components for co-simulation using the Momentum electromagnetic option "EM Cosimulation." The procedure to follow to perform this analysis will be as follows:

- Create the "master" schematic of the circuit to be electromagnetically co-simulated, considering the geometric arrangement of components.
- Parameterize all dimensions and variables of the circuit that you want to access later using cell parameters.
- Place pins at the input and output ports of the circuit.
- Generate the parameterized layout and its symbol from the master schematic.
- Configure and create the electromagnetic co-simulation view, choosing which components will be simulated from the layout and which from the circuit in the "partitioning" menu.
- Enable cell parameter interpolation so that ADS can construct electromagnetic solutions of the circuit by interpolating existing solutions when there is a relatively small jump between variables. Interpolation is crucial for optimizing a co-simulated circuit, avoiding computationally expensive electromagnetic simulations for small variations of the circuit.
- Add the component to a schematic, select its co-simulation view (emCosim), and run the desired simulation.

2.2.4 Global and Local Optimization

The procedure for optimizing a radio frequency design involves modifying the parameters that define the behavior of the different elements of the design to meet the circuit specifications. ADS is capable of executing an optimization on the results of any of the usual controllers used to simulate circuits (for example, the S-parameters controller) using different optimization algorithms. The procedure for setting up an optimization in ADS consists of three steps.[16]

- Set up the variables to be optimized, choosing the upper and lower limits within which each parameter can vary. For example, there might be a manufacturing constraint that prevents the lines from having a width less than 20 μm
- Create the error function that needs to be minimized. In ADS, the error function is set up as various "Goals" where different weights can be applied to the goals that are more important to achieve. For example, a goal might be that the S11 parameter is below -10dB between 6GHz and 18GHz.
- Configure the optimization controller by selecting the optimization algorithm to be used and the maximum number of iterations. ADS allows configuring both local and global optimization algorithms:

- Global optimization algorithms such as the "simulated annealing" algorithm focus on finding global maxima and minima, meaning the optimal solution across the entire available search space. This type of algorithm is suitable when the current solution is far from meeting the set objectives. Its main disadvantage is that it needs to evaluate the entire search region, consuming significant processing time (which could be problematic, for example, in co-simulations).

- Local optimization allows finding the solution with the lowest error in a specific region of the search space using search algorithms such as "Quasi-Newton" or "gradient," which aim to approximate the nearest maximum or minimum to the current solution. Local optimization is suitable for quickly refining a result that is close to meeting specifications, meaning a result that is known to be near a local minimum

2.2.5 PDK Elements

In this section, the different elements included in the UMS PDK available for the design of the switch will be analyzed.[17].

- Figure 13 shows the layout corresponding to the resistors that will be used for the development of the switches. Within the PDK, there are two types of resistors with different resistivity. Both are characterized by their width and length. The width of the resistors must be designed so that they do not burn out according to the recommendations imposed by UMS (see Appendix). Similarly, the microstrip lines of MET1 metallization must also be sufficiently wide according to the current passing through them.

- Figures 15 and 16 show an inductance and a capacitance, respectively. Both are characterized by their inductive or capacitive value and the width of their lines. In general, increasing the values of inductance or capacitance implies making the component larger. The maximum current that can pass through an inductor is determined by the thickness of the microstrip line used to construct it. On the other hand, for capacitors, it is important to verify that the maximum voltage difference between their terminals does not exceed the recommendation.

- In Figure 17, the layout of one of the series switching transistors is shown. The gate length depends on the technology used and in this case is fixed at 150 nm. The model allows modifying the total gate width (Wt = Wu * Nf) by adjusting either the number Nf of gates (fingers) of the transistor or by adjusting the width Wu of each finger.

  On the other hand, 18 shows the layout of one of the parallel transistors from the PDK. The main difference between the series transistor and the parallel transistor is that the latter models the interconnections that would connect the source terminal to the ground plane.

Figure 13: Resistance

Figure 14: Transmission lines

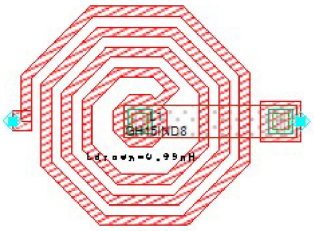


Figure 15: Inductor

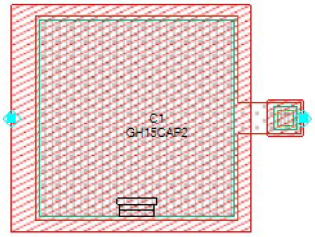


Figure 16: Capacitor

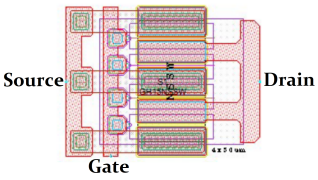


Figure 17: Parallel transistor

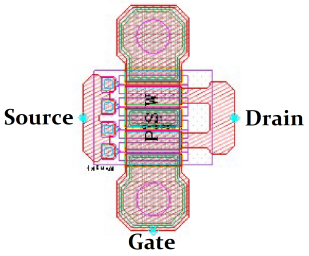


Figure 18: Series transistor

Figure 19: PDK Elements

2.3 Initial steps

Once the analysis of the components included in the PDK provided by UMS has been completed and the objectives set (see the introductory part), this chapter will focus on the design of a RF and symmetrical single-pole double-throw (SPDT) power switch in the 8 GHz to 14 GHz band. The design will be carried out in the Advanced Design System (ADS) design environment. Table 2.1 summarizes the specifications that are supposed to be improved in the redesign. To conduct the analysis, the port nomenclature indicated in Figure (Previous section) will be followed, whereby the antenna is connected to port 1, the transmitter to port 2, and the receiver to port 3. The branch connecting port 2 to port 1 will be referred to in the text as branch 1, and the branch connecting port 3 to port 1 will be referred to as branch 2. Because the design is symmetrical, the behavior in the ON and OFF states of the transmitter and receiver branches can be studied simultaneously. Therefore, during the design process, the transmitter branch (branch 1) will be kept ON (with series transistor voltages at 0V and parallel transistor voltages at -20V), whereas the receiver branch (branch 2) will be in the OFF state (with series transistor voltages at -20V and parallel transistor voltages at 0V). This is because the transistor models for switching included in the UMS PDK are only modeled in this voltage range.[17] The design will be carried out in the Advanced Design System (ADS) design environment using components provided by the manufacturer in their process design kit (PDK). The design development is divided into 7 steps, which will be elaborated upon subsequently:

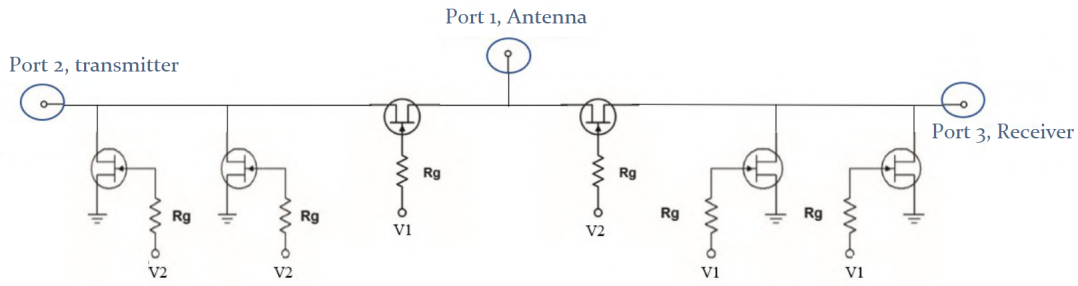


Figure 20: Topology chosen for the design of the RF switch

2.4 Basic circuit design

Among the different switching topologies with varying numbers of stages, a fully symmetrical series-parallel-parallel topology(figure 20) that was used in the previous design has been chosen. Figure 21 shows the schematic obtained after adding the necessary elements to overcome the limits outlined in Table 2.1. As it can be observed, transmission lines have been added between the transistors to achieve the specified broadband matching and isolation with minimal insertion losses possible[8]. Additionally, a DC decoupling capacitor was added at gate 1 (antenna port, see Figure 20). The capacitors required for DC decoupling at gates 2 and 3 will be integrated into the amplifier design. Furthermore two inductor have been introduced to compensate for the capacitive effects of the transistors, they have been placed in parallel to the series configuration transistors, as it was shown previously that the series configuration transistors are mostly responsible for the insertion losses.

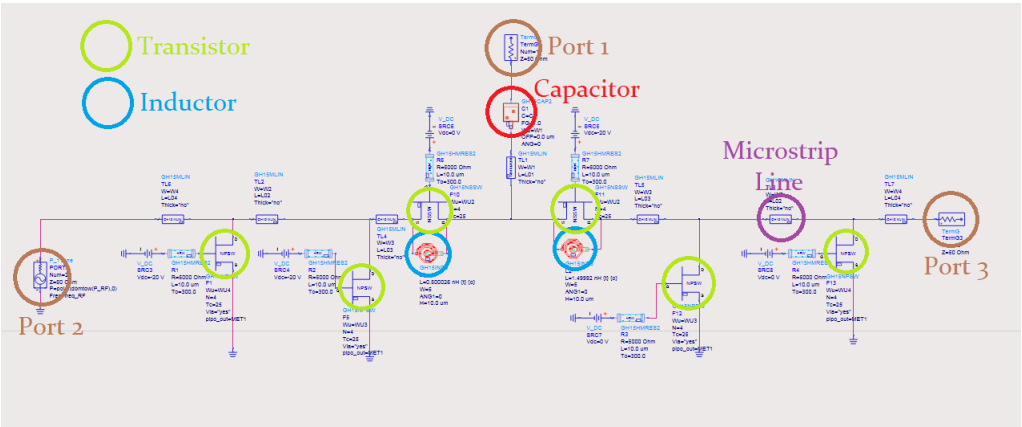
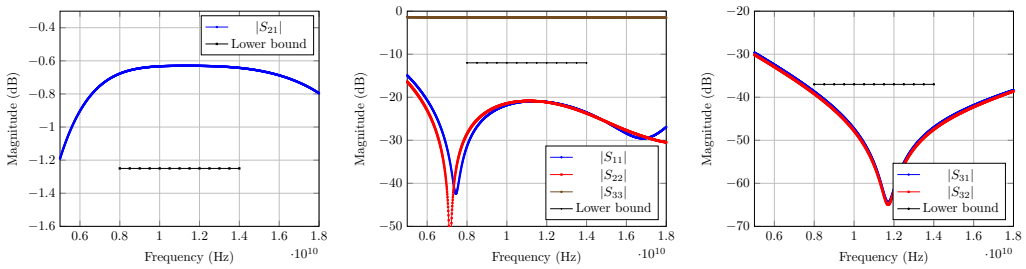


Figure 21: Schematic of the basic circuit design of the radio frequency switch.

The response of the design will be analyzed next after an initial optimization stage, the analysis will be carried out both in small signal and by injecting the estimated power delivered by the HPA into gate 2, over a 50 Ω load, which is supposedly going to be around 40 dBm.

2.4.1 Small signal analysis

The schematic of Figure 21 has been optimized taking into account the limitations of the transistors as established in the previous section, leaving a margin of 0.5dB in the optimization targets for isolation, insertion losses, and return losses with respect to the specifications (see Table 2.1). Figure 22 shows the small-signal S parameters of the optimized design.



(a) S_{21} parameter (b) S_{11},S_{22} and S_{33} parameters (c) S_{31} and S_{32} parameters

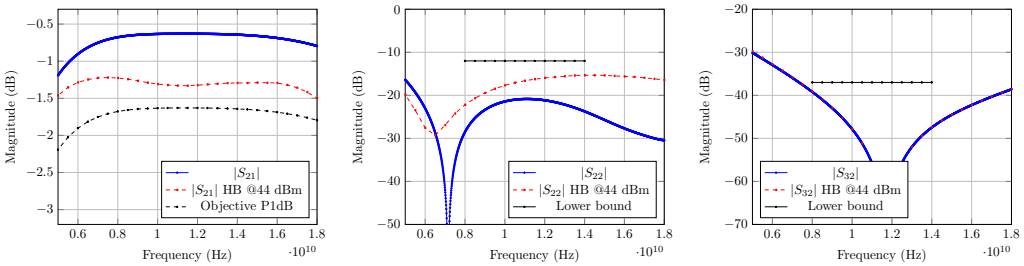
Figure 22: S parameters of the basic radio frequency switch design with branch 1 ON and branch 2 OFF.

.

As observed in Figure 22a, a very good level of insertion loss is achieved, which is lower than 0.7 dB, surpassing the set lower bound (1.5dB). Such big improvement is clearly due to the presence of the inductor. Additionally, notable levels of matching are obtained for the ports of the activated branch (see Figure 22b), maintaining a level below -20 dB across the entire bandwidth, and especially at high frequencies. It is, however, evident how port 3, corresponding to the deactivated branch, is not matched with this switch implementation. This should be taken into account when implementation in a full system is carried out, so that it does not compromise the functioning of the other devices of the chain. Figure 22c) shows that both the transmitter-to-receiver isolation (between gates 2-3) and the antenna-to-deactivated port isolation (between gates 1-3) achieve values above 40dB across the entire working band.

2.4.2 Large signal analysis

After analyzing the small signal S parameters, a power of 44dBm, (40dBm is the IP1dB lower bound) is injected into port 2. Due to numerical analysis issues, providing a higher power levels proved to be problematic, but that doesn't matter as the estimated power delivered by the HPA over a 50 Ω load is about 39 dBm, meaning that if good results are obtained for 44 dBm they will also be suitable for the introduction of the HPA. The following large-signal S parameters are obtained:



(a) S_{21} HB parameter (b) S_{22} HB parameter (c) S_{32} HB parameter

Figure 23: Large signal S parameters simulation of the basic radio frequency switch design with branch 1 ON and branch 2 OFF.

.

In Figure 23, only the S_{12}, S_{22}, and S_{32} parameters are represented because they are the parameters affected by the large power injected into port 2 when the transmitter is activated. The most evident degradation occurs in the insertion loss level (see Figure 23a), obtaining maximum losses of 1.4dB at an injected power of 44dBm. This is because the transistor responsible for transmitting the signal with low insertion losses is the series transistor of branch 1, which is activated in transmission mode and undergoes an inevitable power-dependent compression. Additionally, in Figure 23a, the P1dB target curve is represented in black, and it corresponds to the curve of the small-signal S_{21} parameters minus 1 dB. As in the band it's always lower than the curve for 44 dBm input power, this proves that the P1dB has a value higher than 44 dBm. On the other hand, as observed in Figure 23b, the matching levels remain low just like those obtained in small signal, even though it appears to be facing more degradating, reaching a matching level of about -15 dB. The isolation level represented in Figure 23c and does not appear to change considerably.

2.5 Basic circuit design with geometry

In this section, with the aim of making the design response more realistic and considering space optimization, the following elements will be added:

- MTEE junctions located where there are multiple elements in parallel.
- Step junctions (MSTEP in ADS) and width transition interfaces (MTaper in ADS) where discontinuities in the microstrip line width are present.
- Curved line segments(MCURVE in ADS) where the lengths are extremely long.
- Coupled lines (MCLIN in ADS) in the curved input section to account for the inductive coupling between nearby lines.

Once these elements are added and the design is optimized, the schematic of Figure 24 and the provisional layout of Figure 25 are obtained, ensuring that the elements do not overlap while occupying minimal space. Notice also that the dimensions of the obtained layout will have to satisfy certain size specifications in order to be compatible with the insertion in the T/R Module assigned space.

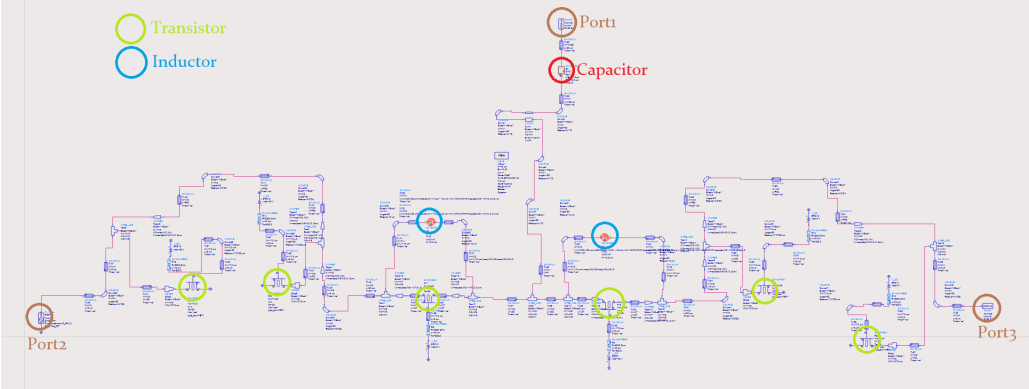


Figure 24: Schematic of the design with geometry of the radio frequency switch.

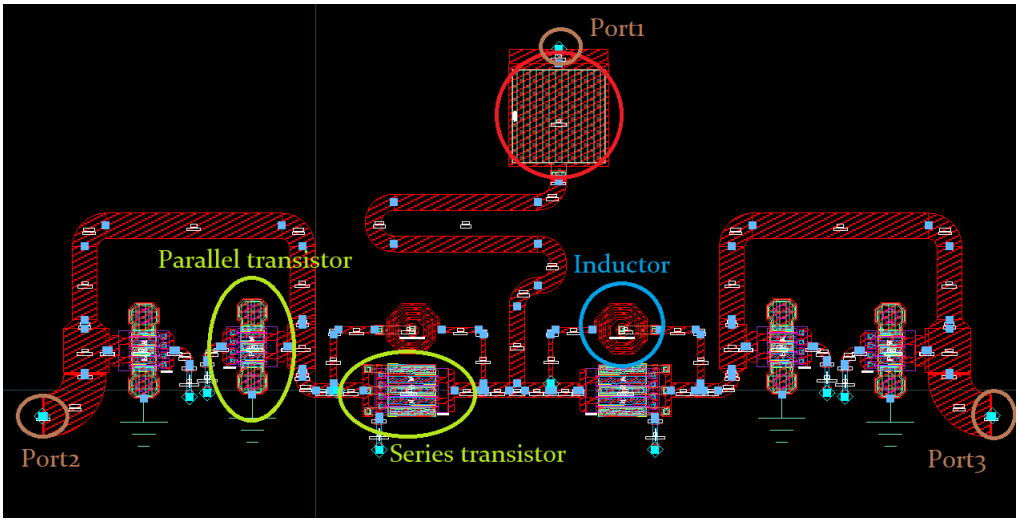
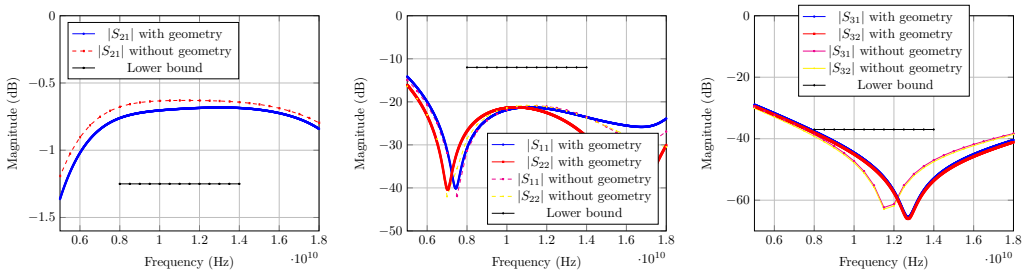


Figure 25: Layout of the design with geometry of the radio frequency switch.

As an optimization bound, the microstriplines sizes have been selected to be at least 5 μm wide and whereas the distance from one another is selected to be about 15 μm, this has been done to avoid coupling between them in the EM cosimulation which would inevitably bring more losses and unexpected behaviours into play. Similarly to the previous section, the small-signal response and the large-signal response will be analyzed by injecting power into gate 2.

2.5.1 Small signal analysis

Here's a comparison of the small-signal results obtained in section 1.3 (circuit 'without geometry') and in the current one (circuit 'with geometry'):



(a) S_{21} parameter (b) S_{11} and S_{22} parameters (c) S_{31} and S_{32} parameters

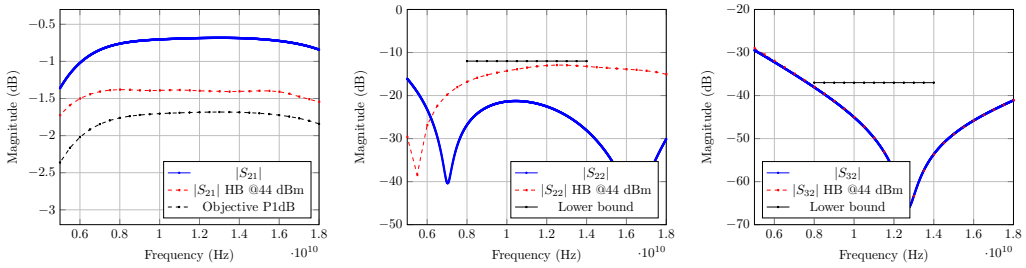
Figure 26: S parameters of the basic radio frequency switch design with geometry with branch 1 ON and branch 2 OFF.

.

Due to the effect of the coupled lines in the input curve section, the new geometry, and the introduction of MTEE/MSTEP/MCURVE elements, more non-idealities seem to appear and are mostly affecting the insertion loss, which as it can be seen in figure 26a is corrupted of about 0.1 dB when compared to the previously obtained insertion loss curve with the ideal schematic, going from 0.7 dB to a 0.8 dB insertion loss. Despite the degradation in terms of insertion loss, the levels reflection parameters shown in Figure 26b do not appear to be changing in a nonnegligeble manner. Regarding the isolation shown in Figure 26c it seems to improve at higher frequencies but to decrease for the lower ones of the band, supposedly due to a shifting of the resonance point caused by the newly introduced geometry. In conclusion, the objectives set in the specification are still met despite the degradation in terms of isolation and insertion.

2.5.2 Large signal analysis

Once again, after injecting the 44 dBm power signal, whose power is higher then the one delivered by the HPA, the following large-signal response is retrieved. It is compared with the small-signal response of the same circuit:



(a) S_{21} HB parameter (b) S_{22} HB parameter (c) S_{32} HB parameter

Figure 27: Large signal S parameters simulation of the basic radio frequency switch design with geometry with branch 1 ON and branch 2 OFF.

.

The behavior is similar to that produced in section 1.3.2. The matching in large signal conditions (see Figure 27b) presents noticeable changes, with a clear degradation with respect to the small-signal response. The isolation (see Figure 27c) do not appear to visibly

change compared to the small-signal analysis, but the lower bounds listed in Table 2.1 are still being overcome. Regarding the insertion losses (see Figure 27a), maximum losses of 1.4 dB are obtained. Gain compression is more significant at the frequencies in the middle, especially at 11 GHz, where it appear to get close to -1.5 dBm.

2.6 Design with electromagnetic co-simulation.

Once a design that overcome the specified lower bounds (see Table 2.1) and has a realistic geometry is obtained, the next step is to electromagnetically simulate the passive elements of the design to verify the effect of electromagnetic couplings in the switch design and in order to obtain a more accurate overall picture of the device performances. To do this, the electromagnetic simulator for planar structures included in ADS, ADS Momentum, is used (see section 2.2.3).

In this section, the passive parts of the layout will be divided into several sections that will be simulated in Momentum separately to speed up optimization. In fact, optimizing the fully co-simulated momentum circuit will prove to be very demanding both in terms of resources and of time, it is more reasonable to plug the values obtained through the optimization of this schematic in the fully co-simulated circuit. To enable optimization from Momentum, it is required to parametrize the most relevant dimensions of the layout of each component. Therefore, in this section, electromagnetic coupling will only be considered internally within each layout component. In the next section, all passive elements will be combined into a single layout to consider the couplings of the entire circuit.

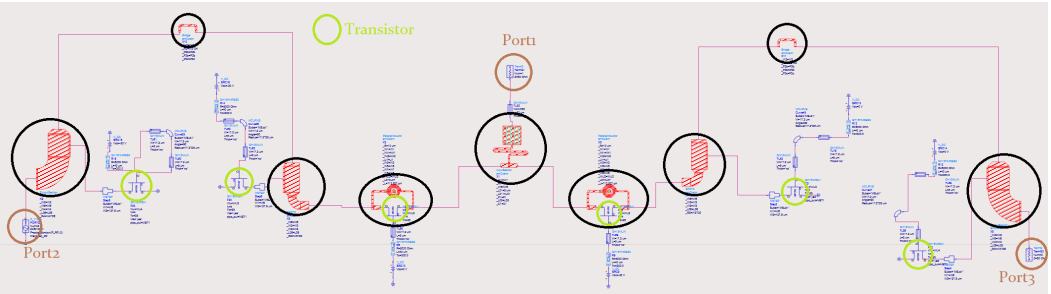
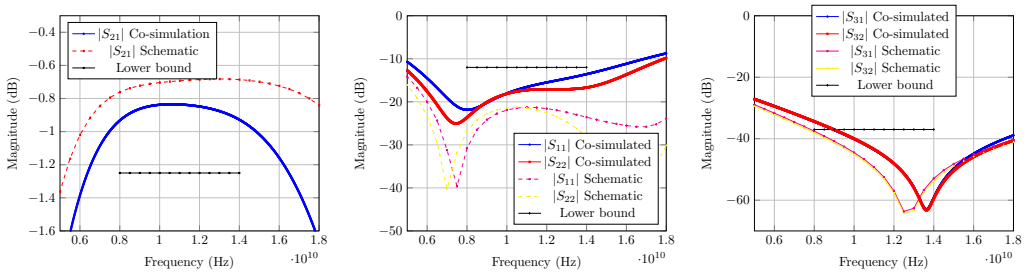


Figure 28: Schematic of the design of the radio frequency switch with electromagnetic co-simulation.

In Figure 28, it can be observed that nine different components have been configured, they will be optimized using their co-simulation view (emCosim). Notice how also the capacitor has been introduced in a layout component, to consider the effect of the coupling between it and the input line section. Once the pieces have been optimized, The analysis can proceed with the small signal and large signal response.

2.6.1 Small signal analysis

Once the schematic is divided into pieces and the design is optimized through co-simulation, Figure 29 shows a comparison between the new S parameters obtained after co-simulation-based optimization and the S parameters of the design from the previous section (see section 2.5).



(a) S_{21} parameter (b) S_{11} and S_{22} parameters (c) S_{31} and S_{32} parameters

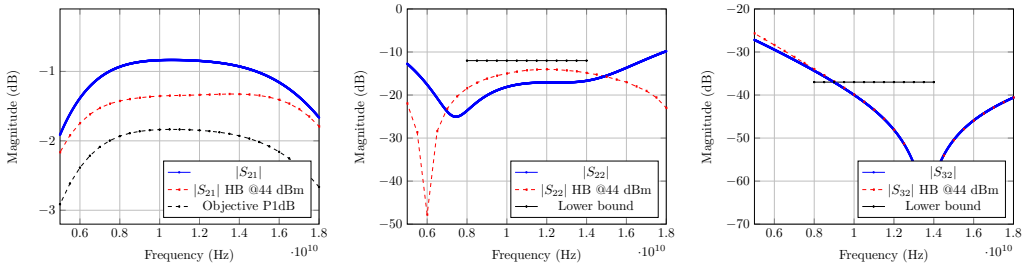
Figure 29: S parameters of the co-simulated radio frequency switch design with branch 1 ON and branch 2 OFF.

.

Figure 29 shows a general degradation of the response compared to the previous section (see section 2.5). The degradation has is more noticeable in the reflection (see Figure 29b), where approximately 7-8 dB have been lost across the entire band. On the other hand, in terms of insertion losses (Figure 29a), 0.2dB have been lost, going from a value of insertion loss of 0.8 dB to 1 dB across the band, there's also a visible reduction of the working bandwith. Regarding the isolation, as it can be seen in figure 29c, the value does not change but it appears that the resonance is slightly shifted towards higher frequencies, therefore for low frequency the lower bounds are exceeded. Despite the degradations compared to the previous stage, all parameters but the isolation still surpass the lower bounds imposed in table 2.1, the isolation will show better results in the stage that follows, since a compensation will take place.

2.6.2 Large signal analysis

After injecting power into gate 2, the following large signal response is obtained



(a) S_{21} HB parameter (b) S_{22} HB parameter (c) S_{32} HB parameter

Figure 30: Large signal S parameters simulation of the co-simulated radio frequency switch design with branch 1 ON and branch 2 OFF.

.

It's evident how the compression suffered by the insertion losses when injecting a power of 44dBm in Figure 30a is still higher than the 1dB compression point objective curve, as was the case in the previous section. In particular, with 44dBm input, maximum insertion losses of 1.5dB are obtained in the working band. On the other hand, Figure 30b shows how the matching in large signal undergoes significant degradation, losing about 3-4 dB in

the overall band. Regarding the isolation shown in Figure 30c, it doesn't appear like the isolation has changed considerably.

2.7 Design with fully electromagnetically co-simulationed layout.

The next step is to electromagnetically simulate the complete layout, to consider the electromagnetic coupling between the layout sections that were simulated independently in the previous section (see section 2.7). As the transistors are active elements, they are still simulated with the schematic view using the PDK circuit models, as active devices are not suitable for the co-simulation through the Momentum tool. Notice how the parameters values initially plugged are the ones obtained through the optimization of the co-simulated circuit in pieces, introduced in section . A small scale optimization procedure is then carried out for the fully co-simulated circuit, but only a few iterations, just to give a final "touch", as the process is very demanding.

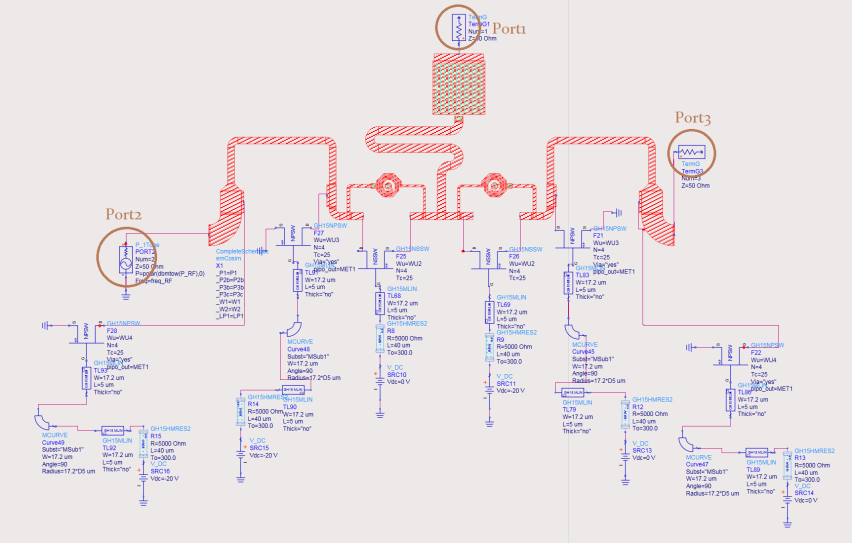
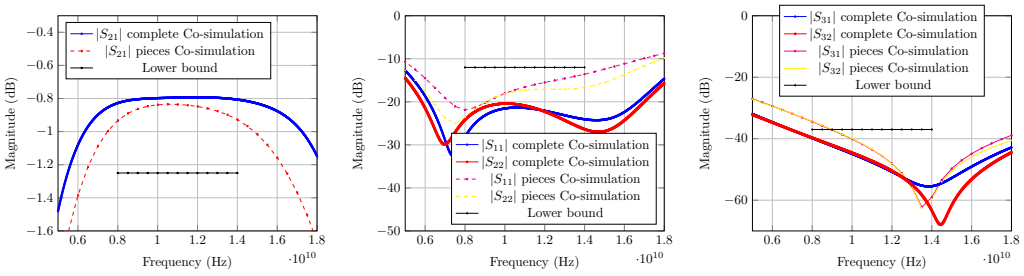


Figure 31: Symbol of the full-layout radio frequency switch design.

Figure 31 shows the symbol of the fully co-simulated layout design that will be used for simulation. This symbol represents a co-simulation component containing all the passive parts of the design merged into a single piece, the transistor are being kept with their respective circuit model.

2.7.1 Small signal analysis

In Figure 32, a comparison is shown between the response of the complete optimized design and the response obtained from the electromagnetic simulation in parts from the previous section (see section 2.7).



(a) S_{21} parameter (b) S_{11} and S_{22} parameters (c) S_{31} and S_{32} parameters

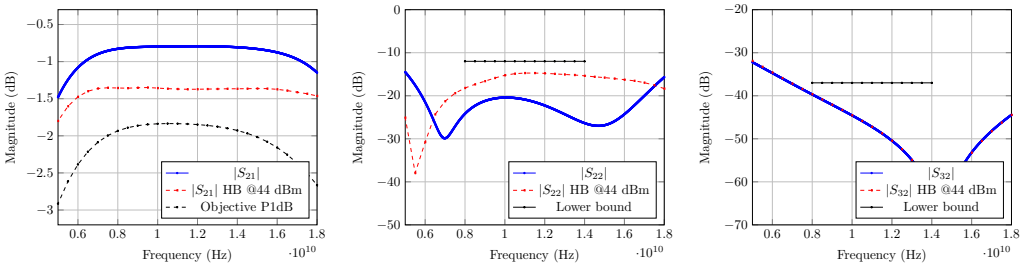
Figure 32: S parameters of the fully co-simulated radio frequency switch design with branch 1 ON and branch 2 OFF.

.

Observing Figure 32b, it can be seen how, thanks to the new couplings taken into account with the complete layout that balance the losses introduced previously, in the pieces simulation, the matching improves significantly, reaching 20 dB across the whole band and surpassing the bounds marked in Table 2.1 of about 10 dB. Furthermore, the insertion losses (see Figure 32a) improve significantly, reaching values above 0.9 dB, also the bandwidth is restored. The isolation become slightly better as shown in figure 32c.

2.7.2 Large signal analysis

Figure 36 shows the results after injecting a power of 44dBm into port number 2.



(a) S_{21} HB parameter (b) S_{22} HB parameter (c) S_{32} HB parameter

Figure 33: Large signal S parameters of the fully co-simulated radio frequency switch design with branch 1 ON and branch 2 OFF.

.

In Figure 33a, maximum insertion loss levels of 1.4dB is obtained in the working band. In this new stage, the gain compression produced when injecting a power of 44dBm in the working band is slightly lower compared to the previous stage (see section 2.7), therefore it still meets the P1dB objective. Regarding the matching (see Figure 33b), the second resonance around 15GHz is apparently again and the reflection is degraded of about 6-7 dB. In terms of isolation (see Figure 33c), no difference is visible, For all parameters there's a significant margin with respect to the values shown in Table 2.1.

2.8 Co-simulated design with full-layout and power supply lines

Once the complete design has been co-simulated and the results have been analyzed in section 3.4, the following changes will be added to inject the necessary DC control voltages to bias each transistor and select the operating mode of the switch once it is integrated into the T/R module.

- 2 control pads (VDC1 and VDC2) connected to the transistors via transmission lines, connected to the bias resistor, whose position has been selected in order to optimize the losses, and a ground pad (GND).
- 50 Ω line sections at ports 2 and 3 where the HPA and LNA will be connected respectively.
- Ground capacitors in each power branch to eliminate potential transient spikes from the power source that could damage the switch transistors.
- Interconnection over a 50 Ω impedance line using bridges in the LNA branch, thus losing its symmetry. This will serve to estimate the effect produced by these elements when the DC lines are brought to one side of the chip to introduce the biasing.

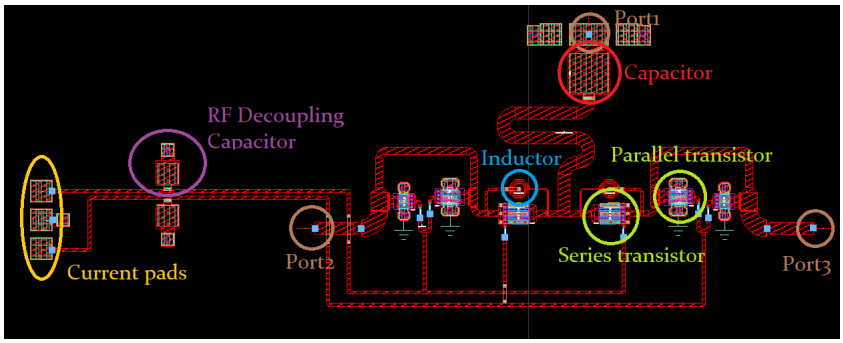
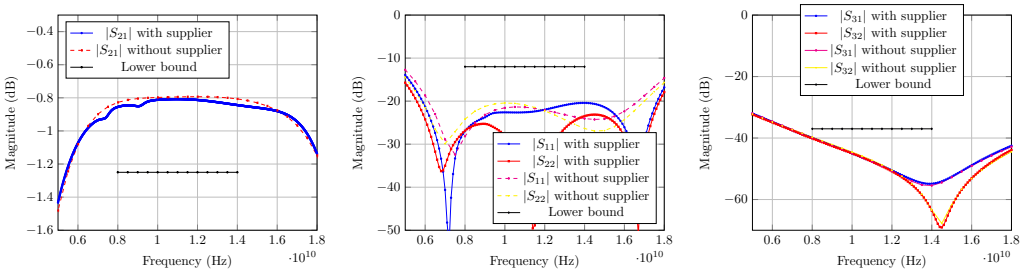


Figure 34: Complete layout of the radio frequency switch with supply lines

2.8.1 Small signal analysis



(a) S_{21} parameter (b) S_{11} and S_{22} parameters (c) S_{31} and S_{32} parameters

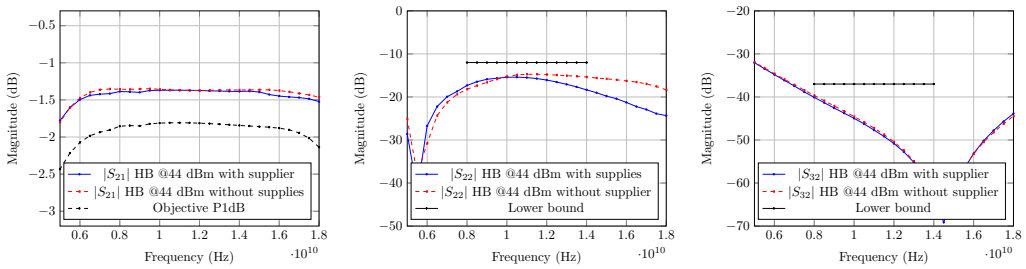
Figure 35: S parameters of the co-simulated radio frequency switch design with supply circuit with branch 1 ON and branch 2 OFF.

.

In Figure 35, it can be observed how the introduction of the supply lines slightly degrades the insertion losses, and how the resonance in matching shifts slightly.

2.8.2 Large signal analysis

After analyzing the small-signal response, the large-signal response of the design is analyzed by injecting power through gate 2.



(a) S_{21} HB parameter (b) S_{22} HB parameter (c) S_{32} HB parameter

Figure 36: Large signal S parameters of the co-simulated radio frequency switch design with supplier with branch 1 ON and branch 2 OFF.

.

Again, in Figure 36, it is observed that the response with the added power supply slightly differs from the response of the previous stage.

2.9 DRC and maximum ratings analysis

Once the design is completed and the power supply has been implemented, the Design Rule Check (DRC) tool provided by the manufacturer is used to verify that the design of section 2.8 complies with all the manufacturing process design rules. Figure 37 shows that there are no errors in the proposed design for the radio frequency switch. Therefore, it would be ready for fabrication.

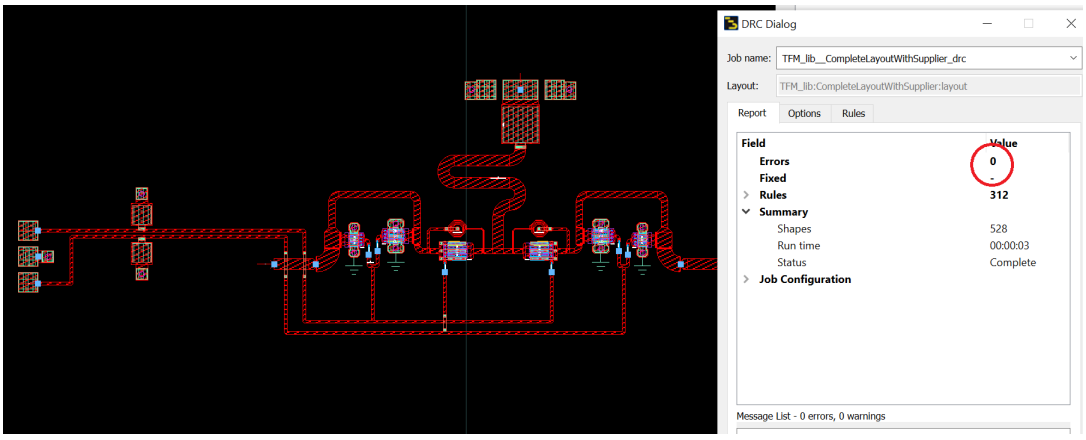


Figure 37: DRC Analysis

On the other hand, the manufacturer UMS provides current, voltage, and temperature

limits that different components manufactured with this technology can withstand to prevent permanent damage to the circuit.[18]

The resistors used to introduce the control bias through the gate terminals of the transistors (see Figure 34) have a width of 17.2 μm. Based on this, Table 2.9 collects the recommended maximum and absolute values of both DC and RMS current that these resistors can withstand without causing permanent damage. Figure 38) shows the nomenclature that will be followed in the resistor analysis.

Current	Recommended	Maximum
DC	1.72 mA	2.23 mA
RMS	6.88 mA	9.12 mA

To perform this analysis, the following expressions will be used for the currents:

$$I_{DC} = \frac{1}{T}\int i(t)dt \tag{5}$$

$$I_{RMS} = \sqrt{\frac{1}{T}\int i(t)^2 dt} \tag{6}$$

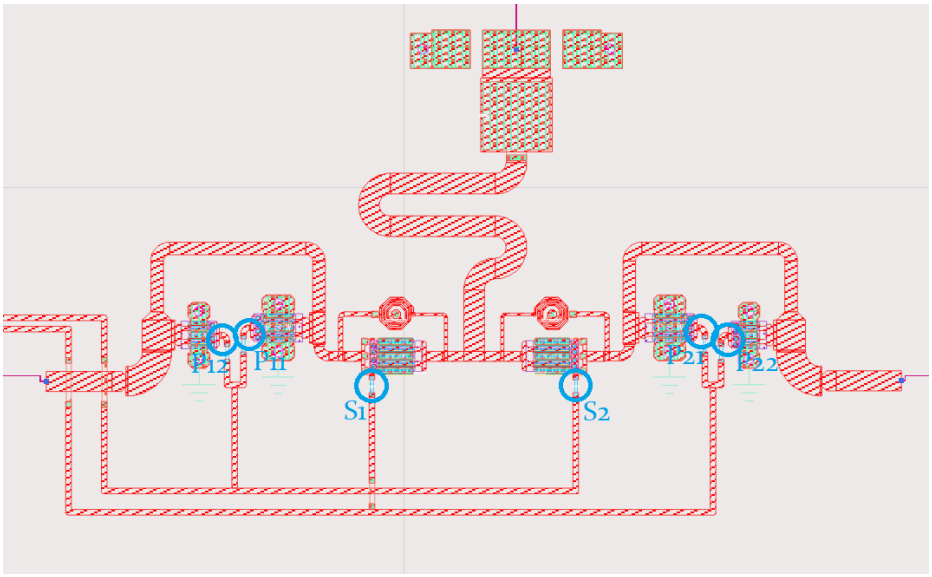
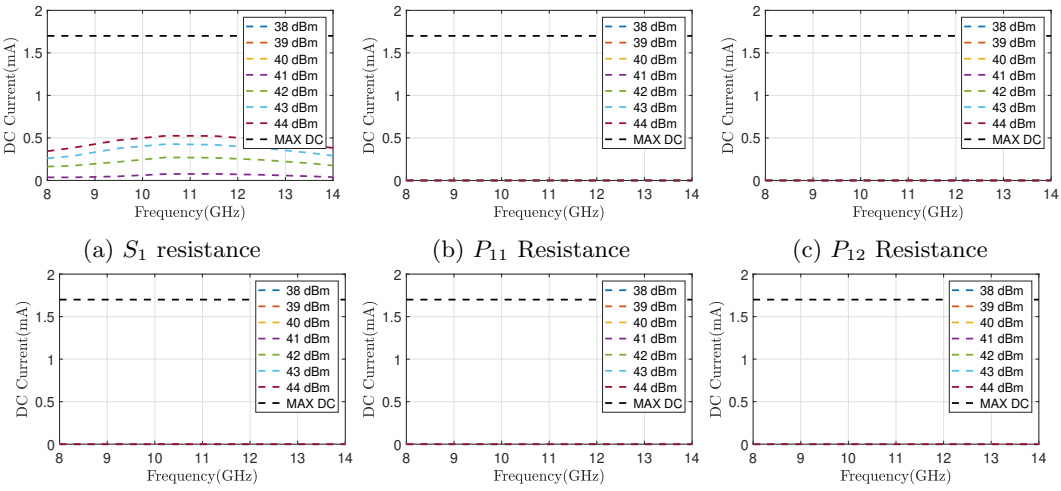


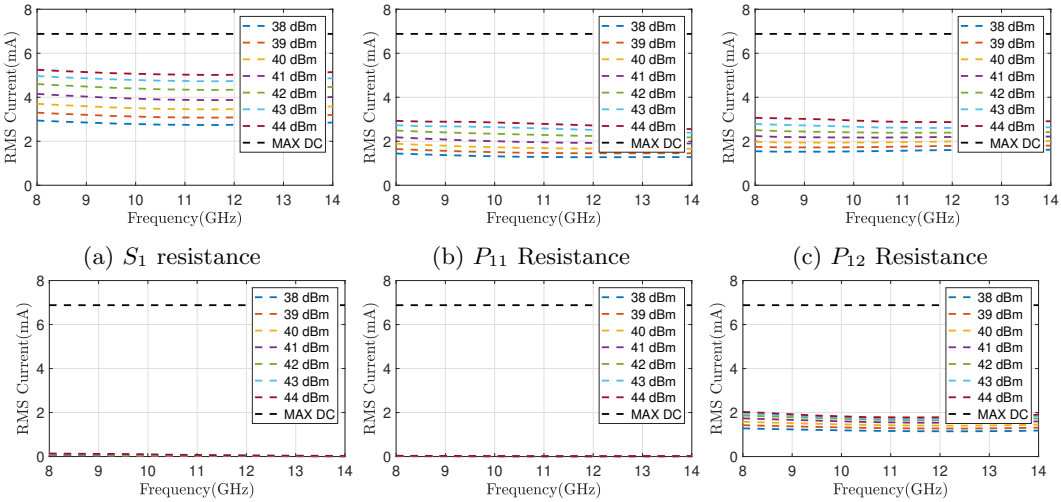
Figure 38: Reference scheme for the maximum ratings



(a) S_1 resistance (b) P_{11} Resistance (c) P_{12} Resistance

(d) P_{21} Resistance (e) P_{22} Resistance (f) S_2 Resistance

Figure 39: DC current flowing through the feed resistors of the radio frequency design



(a) S_1 resistance (b) P_{11} Resistance (c) P_{12} Resistance

(d) P_{21} Resistance (e) P_{22} Resistance (f) S_2 Resistance

Figure 40: RMS current flowing through the feed resistors of the radio frequency design

In Figure 39a, it can be observed that the only resistor that could be critical for the DC current is S_1 (see Figure 38), however the width of the resistor allows the current to be well below the maximum bound. Since Table 2.9 indicates a recommended threshold value of 1.72mA of current, The maximum current corresponding to a power of 44 dBm is below such threshold, therefore no correction is needed. Regarding alternating current (see Table 2.9), the most restrictive resistors are S_1, P_{11} and P_{12} , which are however still below the maximum rating value of 6.88 mA. Since the expected power of the HPA is 39dBm, the width of the resistors can be left to be equal to 17.2µm. The HPA can operate without causing any damage. In the following chapters the dependency of the value of the resistors on the S-Parameters of the device will be analyzed.

2.10 Switch states analysis

Once the design is completed, this section will analyze the different states of the switch that can be achieved by modifying the control voltages VDC1 and VDC2.

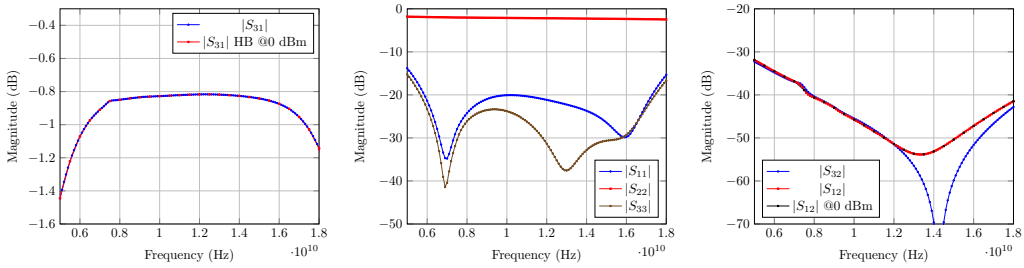
State	Branch 1	Branch 2	VDC1	VDC2
Transmission mode	Open	Short	-20	0 V
Reception mode	Short	Open	0	-20 V
Turned off mode	Open	Open	-20 V	-20 V
Forbidden mode	Short	Short	0 V	0 V

2.10.1 TX Short, RX Open

This state has been the configuration of the radio frequency switch design that has been used for analysis in all stages of the design throughout section 1. The final response is analyzed in 2.8.

2.10.2 TX Open, RX Short

In this state, the switch would operate when the antenna receives a signal that needs to be transmitted to the receiver. According to the specification, the received signal will not exceed 0dBm, and therefore, the switch will operate in small signal mode.



(a) S_{31} parameter (b) S_{11},S_{22} and S_{33} parameters (c) S_{32} and S_{12} parameters

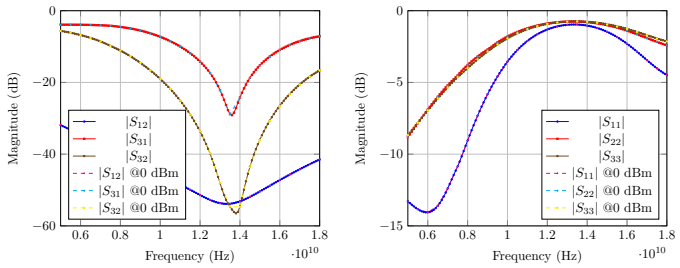
Figure 41: S-parameters of the complete layout of the radio frequency switch with power lines with branch 1 turned OFF and branch 2 turned ON.

.

This section analyzes what happens for a power injected into the antenna port of 0 dBm, as this is the specified IP1dB for the reception mode of the switch. Figure 41 shows a behavior similar to that obtained in the analysis in transmission mode in small signal, as in principle both branches should be symmetric. a similar insertion loss level is obtained, and so is good matching in two of the three ports due to the design of the radio frequency switch (it will be adapted in all three gates in the absorptive switch design), isolation levels are also below 40dB. On the other hand, it is noted that compression is negligible, as could be inferred from the transmission mode analysis.

2.10.3 TX Open, RX Open

This is the state used when the T/R module is idle with HPA and LNA turned off.



(a) S_{12},S_{31} and S_{32} parameters (b) S_{11},S_{22} and S_{33} parameters

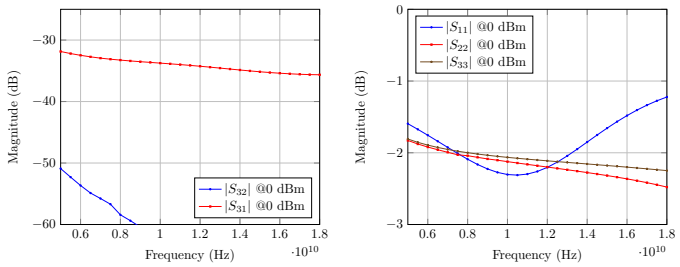
Figure 42: S-parameters of the complete layout of the radio frequency switch with power lines with branch 1 turned OFF and branch 2 turned OFF.

.

The figure 42b shows a high level of reflection losses in all ports. Therefore, in this design, the HPA could not be turned on before opening the branch where it is connected, as unforeseen instability effects could occur during the HPA design.

2.10.4 TX Short, RX Short

In principle, this state is prohibited for the switch.



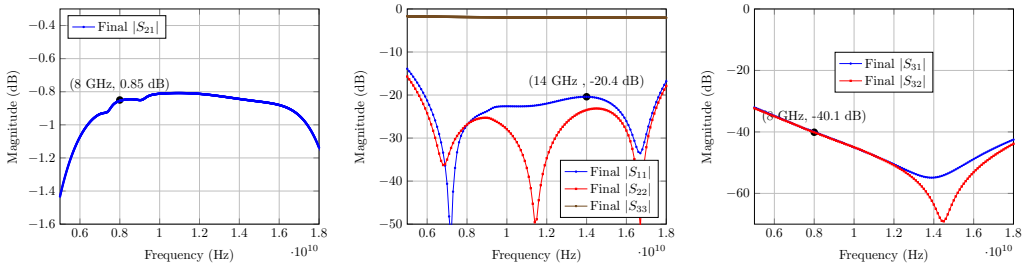
(a) S_{32} and S_{31} (b) S_{11},S_{22} and S_{33} parameters

Figure 43: S-parameters of the complete layout of the radio frequency switch with power lines with branch 1 turned ON and branch 2 turned ON."

.

Figure 43 shows the results obtained with both branches in conduction mode. Figure 43b prooves that the matching at all gates is insufficient. Therefore, this state could not be used in any case as it could damage the transmitter.

2.11 Conclusions



(a) S_{21} parameter (b) S_{11}, S_{22} and S_{33} parameters (c) S_{31} and S_{32} parameters

Figure 44: S parameters of the final radio frequency switch design with branch 1 ON and branch 2 OFF.

.

As it can be seen from figure 3, the final resulting S-Parameters of the design can now be evaluated by considering the most critical points in the bandwidth for each and every parameter of interest, which are marked in the graphs. With the now collected data the final table can be compiled:

Parameter	Objective	Results
Insertion loss	<1.25 dB	0.85 dB
Return loss on activated line	>12 dB	20 dB
Isolation	>37 dB	40 dB
1 dB input power compression point	>40 dBm	>44 dBm
Working bandwidth	8-14 GHz	8-14 GHz

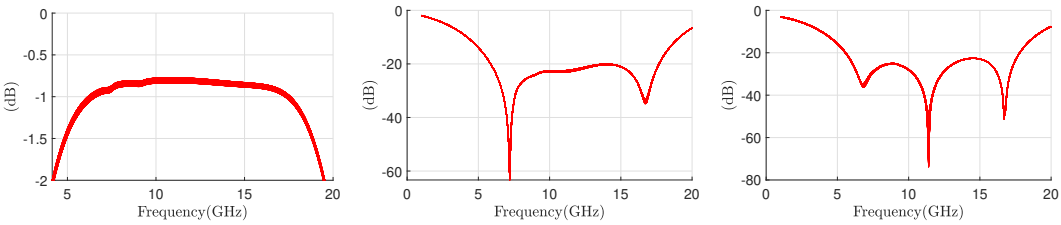
By doing a comparison with the initial table in 2.1 it can be seen how the wanted improvements have been obtained, the insertion loss decreased of about 0.4 dB, the reflection loss of 10 dB, the Isolation increased of 3 dB and the P1dB shifted of more than 4 dB. Furthermore, the complete layout has passed all design rules required by the manufacturer. Therefore, the design would be ready to be integrated into the T/R module and for manufacturing.

3 Radio frequency switch design - Monte Carlo Analysis

The Monte Carlo analysis is a powerful statistical tool used in the analysis and optimization of high-frequency circuits. This method involves running multiple simulations of the circuit, each time using randomly varied parameters within specified tolerances. By performing these numerous simulations, the performance variations of the circuit due to component tolerances, manufacturing imperfections, and environmental factors can be predicted. In high-frequency circuits, where small variations can significantly impact performance, the Monte Carlo method helps in identifying the probability of certain outcomes and the robustness of the circuit design. This approach enables designers to optimize the circuit to ensure reliable operation under a wide range of conditions and consistency with the requirements which have been imposed.
Such method will be applied to the previously designed radio frequency switch, whose schematic can be seen in figure 34, it's important to know that the Monte Carlo analysis average results will be slightly off with respect to the results presented in , as the components whose parameters will be varied will be simulated on a circuital level, as the analysis with the co-simulated components will prove to be unbearable in terms of time and resources.
The most critical components whose parameters will vary according to realistic and specified design tolerances are the inductors, the capacitors, the resistors and the transistors themselves.

3.1 Monte Carlo Analysis - Transistor behaviour

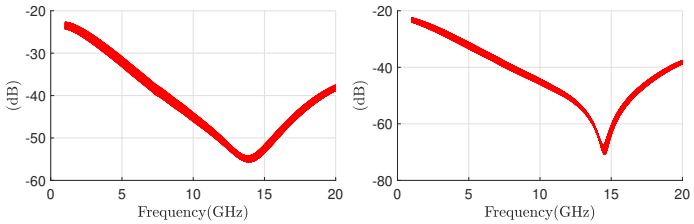
In this section, the Monte Carlo analysis of the circuit is carried out varying the nominal value so far used for the transistors threshold voltage(which now will be in a $\pm$ 0.2 V tolerance range with respect to the nominal value) and the resistance of the active path of the transistor when in "ON" condition, which will now vary in a $\pm 20\%$ range. 500 simulations have been carried out and the results can be seen in 45



(a) $|S_{12}|$ for transistors variation

(b) $|S_{11}|$ for transistors variation

(c) $|S_{22}|$ for transistors variation



(d) $|S_{13}|$ for transistors variation

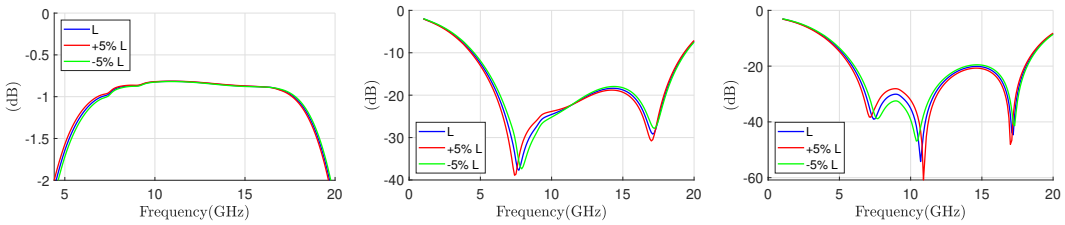
(e) $|S_{23}|$ for transistors variation

Figure 45: Monte Carlo analysis of switch circuit with transistors values

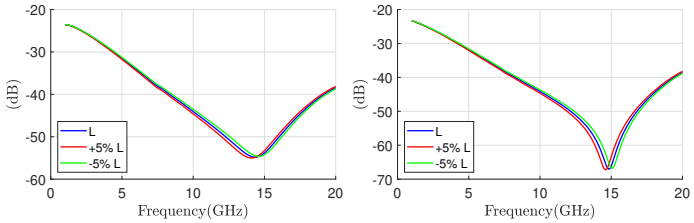
The insertion losses in 45a and the reflection losses in 45b and 45c are only slightly affected and display an uncertainty of about a tenth of 1 dB. Overall, it appears that the transistors parameters variation mildly affect the losses. On the other hand the isolation parameters in 45e and 45d appear to be the ones affected by the largest uncertainty of about 2 dB.

3.2 Monte Carlo Analysis - Inductor behaviour

In this part, the Monte Carlo analysis of the circuit is carried out varying the nominal value so far used for the inductance in a $\pm 5\%$ tolerance range. As anticipated, the inductances are simulated on a circuital level in order for the Monte Carlo analysis not to be too computationally demanding to be carried out, the same will be done later with the others passive components, such as the capacitor and the resistors. In order to get an idea on how the performances are affected in the worst case scenario, the S-Parameters are shown for both the values at the boundaries of the tolerance range and for the nominal values in 46. As it can be seen, the variation appear to be more relevant for the reflection coefficients in 46b and 46c, whereas the insertion loss in 46a does not appear to be changing considerably. It is however interesting to notice that the three curves are slightly shifted: although changing the value of the inductor in the tolerance range does not appear to degrade the overall value insertion loss the bandwidth changes, even if slightly so. That's reasonable, as the inductors have been introduced to fix the bandwidth of the device and increase it, and a variation in their value corresponds to a variation of the parameter.



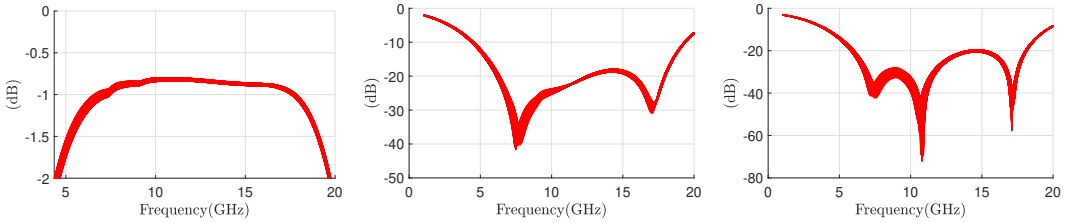
(a) $|S_{12}|$ for inductors variation (b) $|S_{11}|$ for inductors variation (c) $|S_{22}|$ for inductors variation



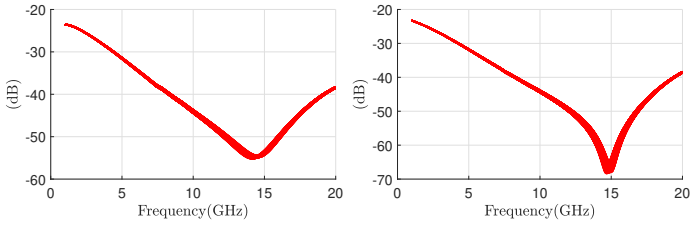
(d) $|S_{13}|$ for inductors variation (e) $|S_{23}|$ for inductors variation

Figure 46: Performance simulation of switch circuit with boundary inductor values

Now, as it has been previously anticipated, a Monte Carlo analysis with 500 simulations is operated for the value L of the inductances, in a $\pm 5\%$ tolerance range following a uniform distribution.



(a) $|S_{12}|$ for inductors variation (b) $|S_{11}|$ for inductors variation (c) $|S_{22}|$ for inductors variation



(d) $|S_{13}|$ for inductors variation (e) $|S_{23}|$ for inductors variation

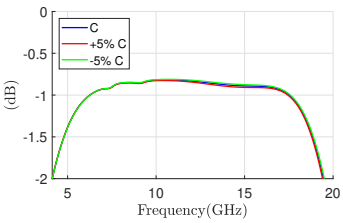
Figure 47: Monte Carlo analysis of switch circuit with inductor values

All of the simulations shown in 47 fall in the range defined by the three curves in 46. As anticipated the degradation mostly influence the reflection parameters, which seem to be affected by a 2 dB uncertainty in the overall frequency range. The isolation parameters in 47d and 47e also appear to be affected by the same uncertainty, whereas the influence on the insertion losses in 47a is minimal.

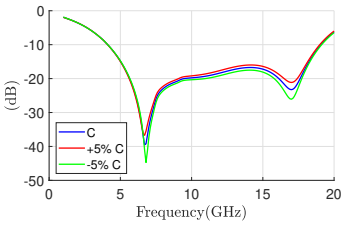
3.3 Monte Carlo Analysis - Capacitor behaviour

Now, the Monte Carlo analysis of the circuit is carried out varying the nominal value so far used for the capacitance right after port 1, it will be subjected to a $\pm 9\%$ variation.

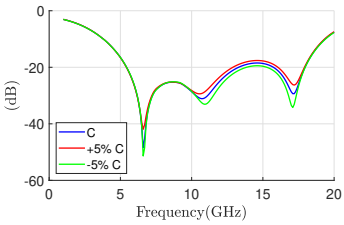
In order to get an idea on how the performances are affected in the worst case scenario, the S-Parameters are shown for the boundaries of the tolerance range and for the nominal values in 48. As can be seen, the variation appears to be more relevant, for the reflection coefficients in 48b and 48c, whereas the insertion loss in 48a does not appear to be changing considerably. The isolation parameters are also overall uneffected, with no variation at all in 48d and 48e.



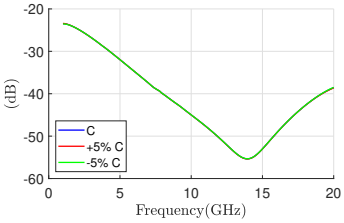
(a) $|S_{12}|$ for capacitor variation



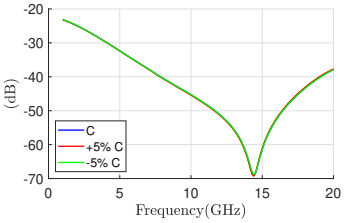
(b) $|S_{11}|$ for capacitor variation



(c) $|S_{22}|$ for capacitor variation



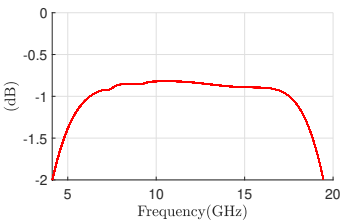
(d) $|S_{13}|$ for capacitor variation



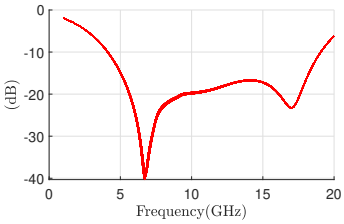
(e) $|S_{23}|$ for capacitor variation

Figure 48: Performance simulation of switch circuit with boundary capacitor values

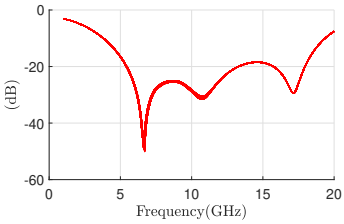
A Monte Carlo analysis with 500 simulations is operated for the value C of the capacitance, in a ±9% tolerance range following a uniform distribution.



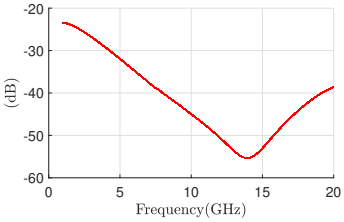
(a) $|S_{12}|$ for capacitor variation



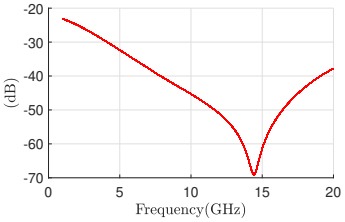
(b) $|S_{11}|$ for capacitor variation



(c) $|S_{22}|$ for capacitor variation



(d) $|S_{13}|$ for capacitor variation



(e) $|S_{23}|$ for capacitor variation

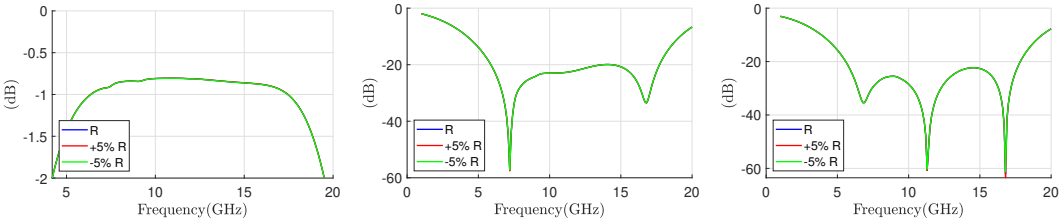
Figure 49: Monte Carlo analysis of switch circuit with capacitance values

The simulations shown in 49 fall in the range defined by the three curves in 48. Although the variations are visible, they can be neglected, in both the reflection curves in 49b and 49c. For the insertion loss in 49a the uncertainty is of about 0.1 dB at most, the same can

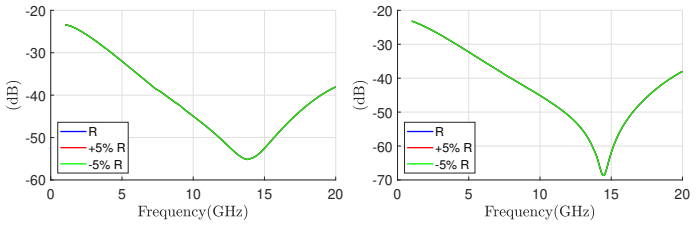
be said about the isolation curves in 49d and 49e. In conclusion, although the capacitor play an important role in defining the bandwidth of the switch, it appears that the performances are not very sensitive to reasonable fluctuations in its value.

3.4 Monte Carlo Analysis - Resistor behaviour

Lastly, a Monte Carlo analysis of the circuit is carried out varying the nominal value of the resistors, it will be subjected to a ±20% variation, with all the resistors having a nominal value of 5000 Ω. In order to get an idea on how the performances are affected in the worst case scenario, the S-Parameters are shown for the boundaries of the tolerance range and for the nominal values in 50. As it can be seen in 50b and 50c, the variation of the reflection parameters is unnoticeable, the same goes for the insertion loss in 50a, this makes sense as they are components used to bias the device and are not directly in the signal path. The isolation parameters in 50d and 50e are also uneffected.



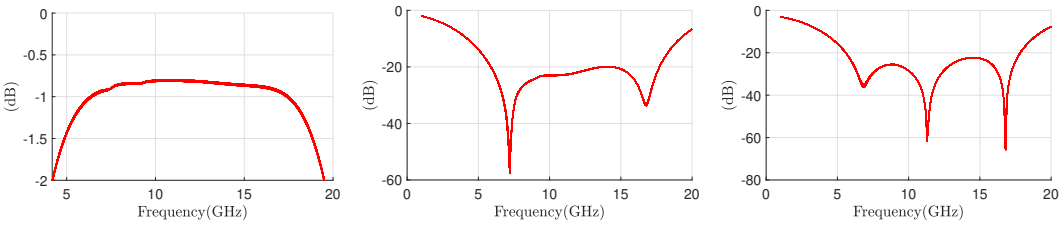
(a) $|S_{12}|$ for resistance variation (b) $|S_{11}|$ for resistance variation (c) $|S_{22}|$ for resistance variation



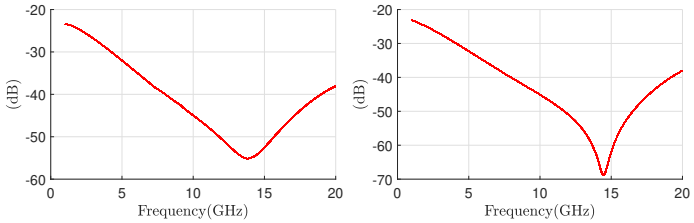
(d) $|S_{13}|$ for resistance variation (e) $|S_{23}|$ for resistance variation

Figure 50: Performance simulation of switch circuit with boundary resistance values

Now, as it has been previously anticipated, a Monte Carlo analysis with 500 simulations is operated for the value R of the resistances, in a ±20% tolerance range following a uniform distribution.



(a) $|S_{12}|$ for resistance variation (b) $|S_{11}|$ for resistance variation (c) $|S_{22}|$ for resistance variation



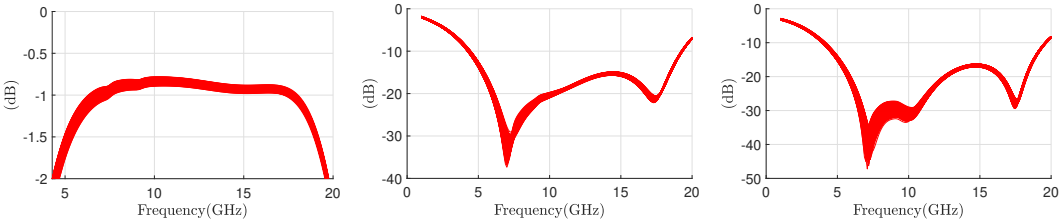
(d) $|S_{13}|$ for resistance variation (e) $|S_{23}|$ for resistance variation

Figure 51: Monte Carlo analysis of switch circuit with resistance values

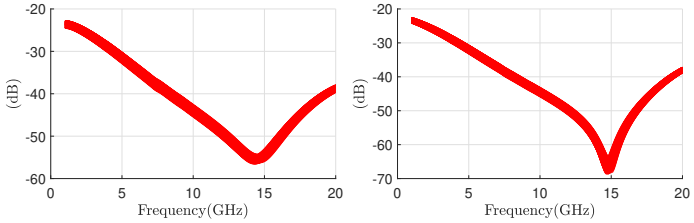
Just like before, in it's clear how the performances are unaffected by the resistors value fluctuations. In conclusion, just like for the capacitor, it appears that the system display a very strong robustness to every variation of the resistor values with respect to the nominal ones.

3.5 Monte Carlo Analysis - Final analysis and conclusions

In the conclusive part, the last 500 simulations are executed, this time by taking into account the variation of all the parameters which were previously made variate only individually. Now the contribution of the capacitor(±9% tolerance range), the inductors(±9% tolerance range), the resistors(±20% tolerance range), the threshold voltages and active path resistances of the transistors are taken into account. The final results are the ones that follow:



(a) $|S_{12}|$ (b) $|S_{11}|$ (c) $|S_{22}|$



(d) $|S_{13}|$ (e) $|S_{23}|$

Figure 52: Monte Carlo analysis of switch circuit considering all the parameters

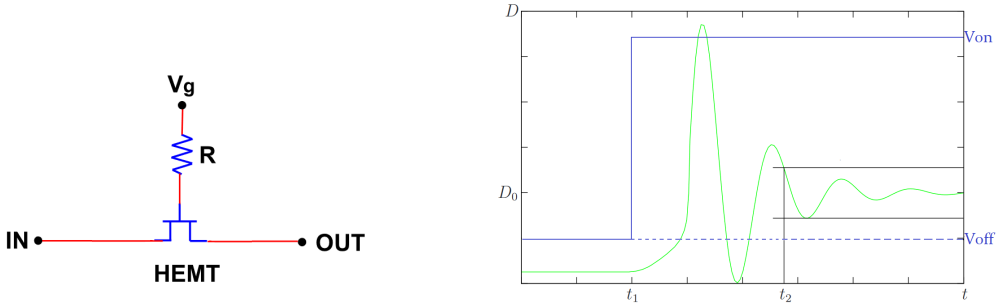
Just as expected, the results display an higher level of uncertainty with respect to the

ones for the Monte Carlo analysis with any of the individual component, due to the fact that now all of them are involved. In conclusion it appears reasonable to prioritize the precision of the parameters of the transistors and of the inductors, as they seem to be the most influential. With the capacitor and resistors uncertainties being the less significant in the degradation of the performances. Overall the sensitivity to variations in both the passive components and the transistors is low. This is therefore a robust design.

4 Radio frequency switch design - Transient analysis

4.1 Introduction

The last part is dedicated to the transient analysis of the switch. To better understand the main time issues of not only the switch in question, but of every switch designed with transistors technology, the example schematic provided in figure 53a should give the idea: let's suppose that a DC voltage signal D_0 is applied at the IN port of the transistor, following that, the transistor is turned on at time t_1(Vg reaches the voltage V_{ON}), in order to let the signal through. Before the signal at the output port OUT reaches the value D_0, a transient takes place as illustrated in figure 53b, and it only starts to settle at time t_2. If before then, the transistor were to be turned off(Vg reaches the voltage V_{OFF}), the transmission of the wave would be incomplete and thus unsuccessful, this implies a limitation in how fast the control voltage can be switched ON and OFF without compromising the performance of the system. It is important to highlight the relevance of such analysis, as the design is mainly focused on the integration of the switch in a T/R Module, the interaction with other components of the system is inevitable. Accurate knowledge of transition times is essential in this regard, as it ensures compatibility with other components and avoids timing conflicts that could lead to signal degradation or system failures. As a rule of thumb, taking into account the compatibility with the rest of the elements of the chain, having a design that ensures faster switching times can enhance the overall efficiency of the system, reducing latency and improving response times in applications such as telecommunications and signal processing.



(a) Basic switch

(b) Out signal in green, control voltage in blue

Figure 53: Transient output signal behaviour of activated HEMT transistor

In order to have some realistic expectations of the transient times and to validate the performance of the previously designed switch, figure 54a and 54b show the switching times of two commercially available RF SPDT switches working in the same band and using the same technology previously introduced. A value that can be expected is therefore a switching time around 10 to 35 ns. As can be seen, in figure 54a, the time to settle varies depending on the state of the transistor, notice how it has been defined as the time that elapses between the moment the control voltage reaches 50% of its new value and the moment the output voltage reaches a value which differs from the input voltage of a margin of either 10 or 90%(depending on rising or falling transition). An example in the case of the falling transition can be seen in figure 55, where t_{phl} is the falling time. Such is the definition that

will be followed in the analysis.

Parameter	Min	Typ
Frequency Range		DC - 18 GHz
Insertion Loss		1.5 dB
Isolation		46 dB
Return Loss - On State		17 dB
Return Loss RF1, RF2 - Off State		17 dB
Input P_{1dB}		23 dBm
Switching Characteristics		
tRISE, tFALL (10/90% RF)		1.8 ns
tON, tOFF (50% CTL to 10/90% RF)		11/4 ns

(a) Switching times of CMD196C3 switch[11]

Isolation (Off-State)	Frequency = 8 GHz	–	35	
	Frequency = 10 GHz	–	36	dB
	Frequency = 12 GHz	–	34	
Output Return Loss Isolated Port	Frequency = 8 GHz	–	4.0	
	Frequency = 10 GHz	–	4.5	dB
	Frequency = 12 GHz	–	4.5	
Input Power ($P_{0.1dB}$)		–	41.7	dBm
Control Voltage		-30	-28	V
Total Supply Current		–	<3	mA
Switching Speed		–	35	ns
Insertion Loss Temperature Coefficient		–	-0.004	dB/°C

(b) Switching times of QPC2040 switch[10]

Figure 54: State of art of commercially available RF switches

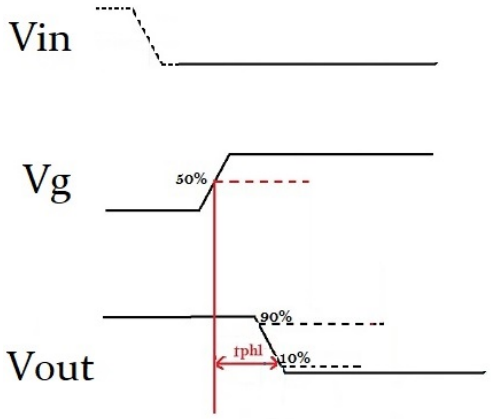


Figure 55: Falling transition example

The next step will be the simulation analysis of the switching times of this switch, and finally, a part devoted to showing how the optimization procedure can be carried out to prioritize this parameter at the expense of others, including the insertion loss, is included.

4.2 Transient time analysis - Scheme and description

In order to keep track of the procedure that will be presented, the schematic of the switch is once again shown in figure 56 where the most important elements have been highlighted:

- Only the behaviour in the branch between port 1 and port 2 is analyzed, a voltage signal of 11 GHz and 10 dBm are applied to port 1, a probe is connected to port 2 to assess the behaviour of the output wave.
- The transistors are the components mainly responsible for the delay in the propagation of the signal.
- As will be seen in the following, the resistors connected at the gates of the transistors can be optimized to increase or reduce the switching times.

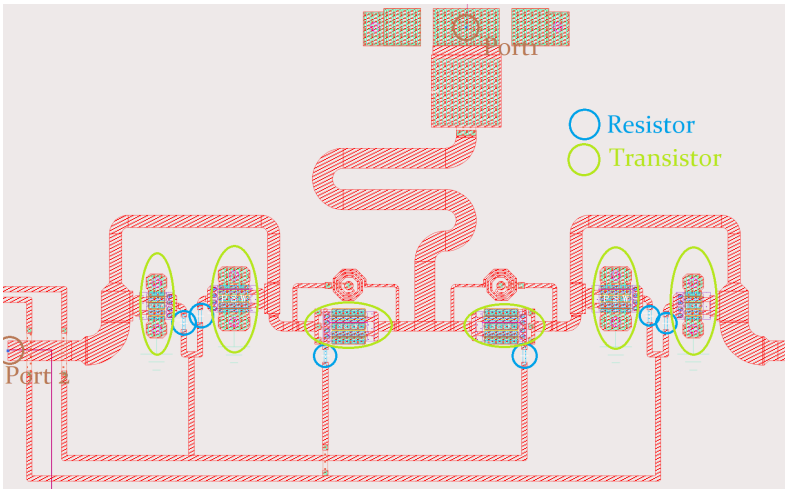
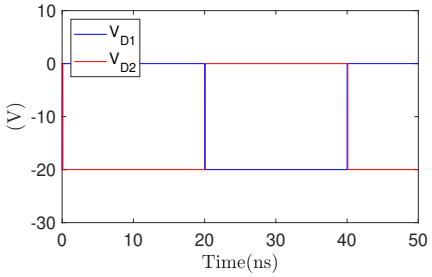


Figure 56: Transient time analysis - Switch scheme

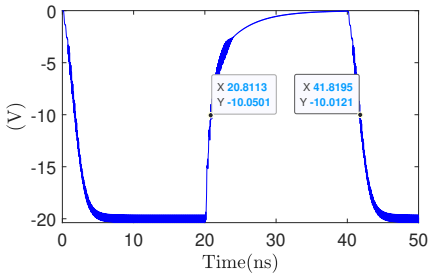
The supply voltage provided to the transistors are two complementary pulse signals, changing value and bringing the switch from transmission state to receiving state of table 5.2 every 20 ns and viceversa.

4.3 Transient time analysis - Simulation results

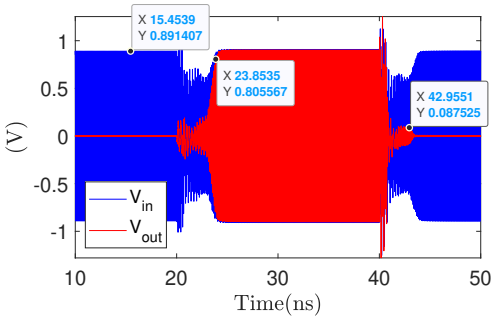
The analysis is carried out as previously illustrated, and the results can be seen in 57.



(a) Supply voltages fed to the transistor lines



(b) Gate voltage of the series transistor of the active branch



(c) Input(Port 1) and output(Port 2) Voltage waves

Figure 57: Results of timing analysis of the RF switch

In order to obtain the transition times, it is considered the time that elapses between the moment the control voltage reaches 50% of its new value and the moment the output voltage reaches a value which differs from the input voltage of either 10 or 90%(depending on rising or falling transition). In figure 57a the supply signals can be seen, using as a reference table 5.2, it is clear how from 0 to 20 ns, the branch analyzed is not active, from 20 to 40 ns it is activated whereas from 40 ns onwards it is deactivated once again. Such behaviour is mimicked by the gate voltage of the series transistor of the branch which can be seen in 57b, the transitions are however not as abrupt as for the supply voltage, in fact, the gate is connected to a resistor, from the point of view of the gate node, the transistor can be modelled with a capacitive behaviour, associated to its parasitic gate capacitance. Because of that, a RC transitory will take place and the signal will take time to settle, such time is related to the time constant τ dependent on the value of resistance and capacitance. Furthermore, again in 57b, the times relative to the 50% transition have been noted in order to later calculate the rising and falling time. Finally in 57c, the behaviour of the input and output signals in PORT 1 and PORT 2 is evaluated: between 0 to 20 ns, as the branch is off, the output signal is visibly close to zero, of course with some residual value due to the final isolation of the switch. After the 20 ns time stamp it can be seen how the output signal slowly catches up to the input signal, with a time stamp annotated at the moment the signal reaches 90% of the input signal. After 40 ns, once the signal branch is turned off, the output signal slowly gets back to a value close to zero, the time where it reaches 10% of the input signal has been annotated. Notice after every transition, the input signal appears to be affected. That is reasonable as changing the control voltage of the transistor also changes the impedance seen at PORT 1, and as such it also changes the S_{11} Parameter. Now that all the time stamps are in place, the rising and falling time can be properly calculated, what is obtained is a value of 3 ns for the rising time and of 1 ns for the falling time. It appears like the two times are different and overall compatible with the values presented in the datasheets of commercially available RF Switches in 54a and 54b, it must be however noted that these values do not take into account the impedances of the drivers connected to the control ports of the circuit. In the part that follows, an attempt to obtain better results for the rising and falling time will be made, a different definition of them will be however used as it is more relevant for the case study. This time instead of using as initial moment of the time lapse the time for the control voltage to reach 50% of its value what will be used is the moment of transition of the supply signal pulse. Meaning that according to this definition, what now will be used for rising and falling time will be, accordingly, 3.85 ns and 3 ns.

4.4 Transient time analysis - Optimization

As previously anticipated, the resistors connected at the gates of the transistors are the main actors in determining the transition times of the switch. This is reasonable, as changing the value of the resistance also changes the time constant $\tau = R \cdot C$ related to the settling time of the gate voltage, this concept should be clearer by looking at the gate voltage curves in 58, where it is clear that the bigger the resistances value the longer the transient time. Having a gate voltage that reaches the intended value faster allows a faster response of the transistor, making the transition times smaller. In order to demonstrate this fact, a

simulation analysis exactly like the one presented in the previous section is carried out, this time, however, instead of having a value for the resistors of 5000 Ω, a value of 2500 Ω is used. The results can be seen in figure 59

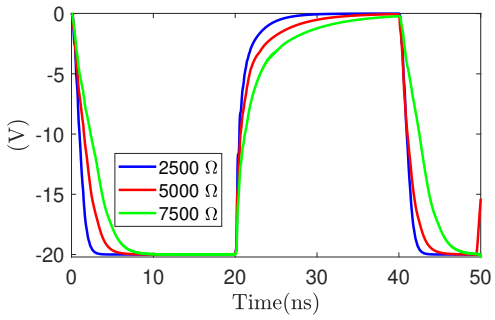
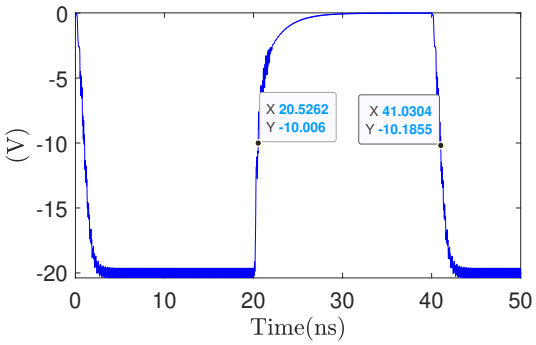
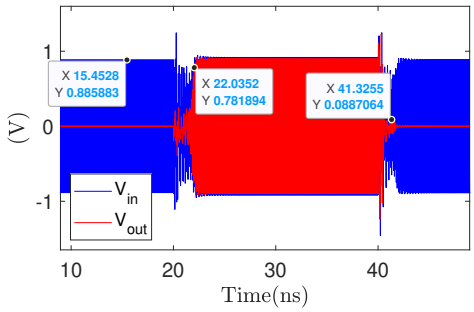


Figure 58: Gate voltage curves as a function of R



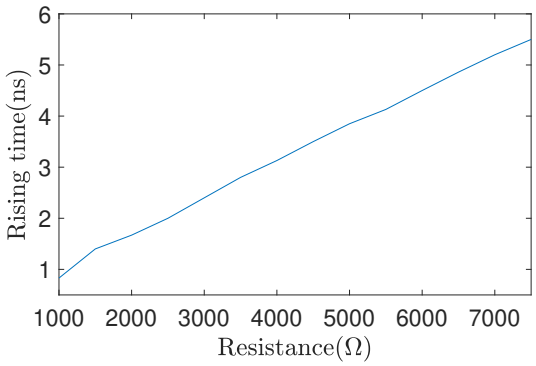
(a) Control voltage of the series transistor of the active branch



(b) Input(Port 1) and output(Port 2) Voltage waves

Figure 59: Results of timing analysis of the RF reflexive switch with resistances 2500 Ω

Taking a quick glimpse at the control voltage at 59a and making a comparison with the control voltage previously obtained for a 5000 Ω resistance in 57a, it appears to be clear that for a lower resistance the signal reaches the 50% threshold faster. Following that, the output e input waves are also analyzed in 59b, with the definition previously introduced for the transition time, the falling and rising times are calculated accordingly: what is obtained is 2 ns for the rising time and 1.32 ns for the falling time.The previous analysis yielded 3.85 ns and 3 ns, therefore a clear improvement has been obtained. In conclusion, lowering the value of the resistance does indeed improve the transition times. The plot in 60a shows how the transition time changes depending on the resistance of the gate. It must be noted that only the rising time is shown, as it is the longest, and as such the one that limits the speed of operation.

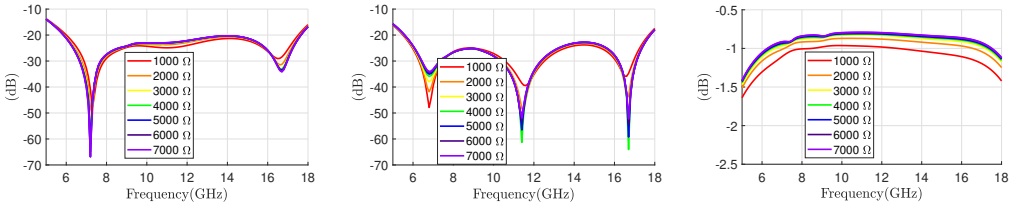


(a) Rising time as a function of the resistance

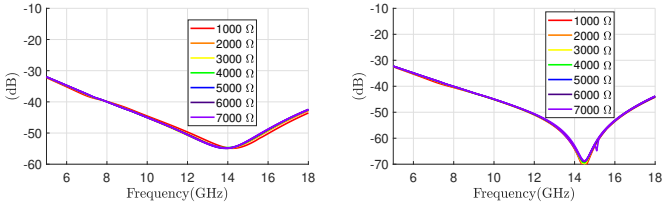
According to the graph, choosing a resistance as low as possible is the ideal choice, however, in the following sections the consequences of choosing a lower resistance is analyzed.

4.5 Transient time analysis - Optimization effects on the other parameters

Once that it has been confirmed that the resistance contributes positively in changing the transition times of the switch, the effect of changing the resistances on the S-Parameters is analyzed in this section. The resistance has now been swept between 1000 Ω and 7000 Ω, for each resistance a curve of each relevant S-Parameter has been plotted in figure 61



(a) $|S_{11}|$ (b) $|S_{22}|$ (c) $|S_{12}|$



(d) $|S_{31}|$ (e) $|S_{32}|$

Figure 61: Comparison estimation of isolation, insertion losses and reflection losses with for different temperatures

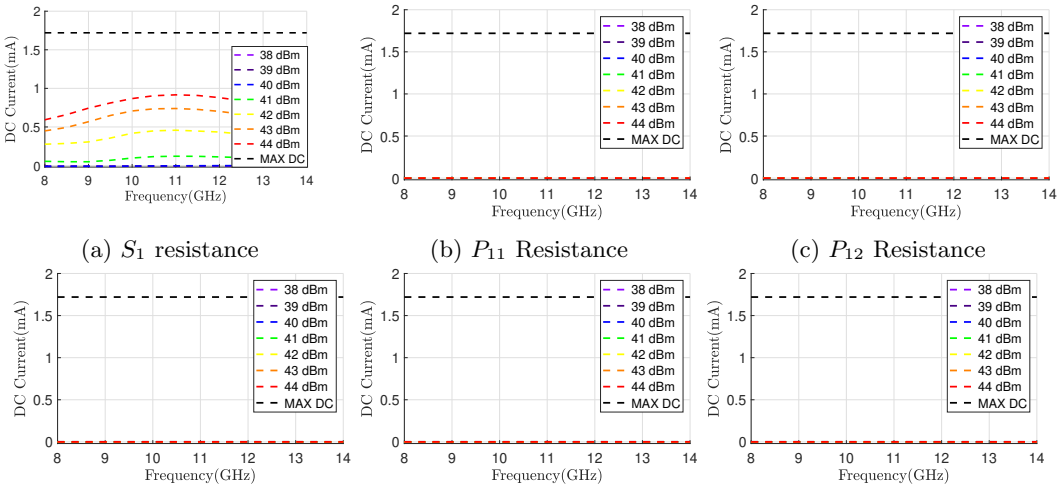
.

The most affected parameter is indeed the S_{12} parameter shown in 61c, the insertion loss experiences considerable degradations, going from the 0.85 dB value in band obtained in the initial analysis to 1 dB for a resistance of 1000 Ω. It is clear how a lower resistance

corresponds to higher insertion losses. It is furthermore noticeable how the gap between the insertion losses for 1000 Ω and 2000 Ω is considerable, meaning that lowering further the resistance will correspond to much higher losses than the ones shown in the graph. The outcome is reasonable, lowering the value of the resistances at the gate, in fact, creates an alternative low resistance path for the signal which now instead of going through the active branch, will be diverted to the supply lines path, causing a higher loss in the signal. Regarding the other parameters, they appear to be overall unaffected, as it can be seen from the reflection losses in 61a and 61b no visible changes can be appreciated, the maximum value in band remains fixed to -20 dB. The same can be said about the isolation parameters, in figure 61d and 61e. The performances are consistent with the conclusive analysis carried out earlier on.

4.6 Transient time analysis - The supply lines current issue

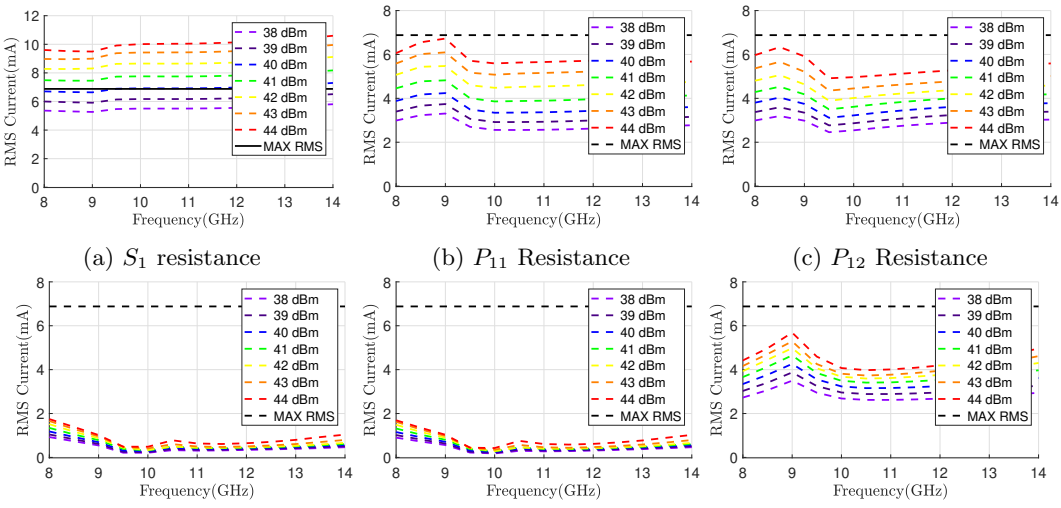
It is clear now how the reduction of the resistance causes an increase of the insertion losses, another unwanted results is also the increase in the current through the supply lines and going through the resistances, an expected outcome considering the Ohm's law. This is problematic, as the size of the resistances does imply a maximum current level for DC and RMS currents(see tab 2.9) that if not respected will compromise the state of the device. In order to better illustrate this issue, the currents going through the resistors are measured for a gate resistances R= 2500 Ω, following the nomenclature of the scheme in 38. Finally, they are plotted in 62 and 63.



(a) S_1 resistance (b) P_{11} Resistance (c) P_{12} Resistance

(d) P_{21} Resistance (e) P_{22} Resistance (f) S_2 Resistance

Figure 62: DC current flowing through the feed resistors of the radio frequency design, with resistances 2500 Ω



(a) S_1 resistance (b) P_{11} Resistance (c) P_{12} Resistance

(d) P_{21} Resistance (e) P_{22} Resistance (f) S_2 Resistance

Figure 63: RMS current flowing through the feed resistors of the radio frequency design, with resistances 2500 Ω

The currents with gate resistances of 2500 Ω are clearly higher in value than the ones shown for the design with gate resistances 5000 Ω in 39 and 40. However, as the widths of the resistances are left untouched, the maximum bound RMS and DC Values for the currents are still the ones illustrated in table 2.9. As can be seen in figure 63a, the RMS current going through the resistance S_1 goes beyond the limit when the power is above 39 dBm, meaning that the device could not even work in the intended implementation, with the HPA working at 40 dBm output power, only by increasing the widths of the resistor can the functionality of the circuit still be ensured. Using the tables present in the appendix 6.2, it is possible to retrieve the recommended width of the transistors for this working point: by increasing the width from 17.2 μm(previous design) to 30 μm, the new recommended RMS current value becomes 11 mA, which allows in this way to respect all of the boundaries.

4.7 Transient time analysis - Possible solutions to the problem

One possible solution to have higher currents bounds and as a consequence not burn out the resistors, is increasing the width of the resistors themselves. This might however introduce ulterior issues which can be made clearer by showing the following schematic in 64: In order to have higher tolerable currents, the widths of the 1000 Ω resistors have been increased, as a consequence the resistors are now very close both to each other and to the transistors, this might end up triggering coupling effects between the two lines and unwanted interaction effects with the transistors, of course the problem might be tackled by simply increasing the distance between transistors, but that implies less degrees of freedom for the optimization. This issue proves hard to be evaluated because the transistors have been simulated only from a circuital point of view, it is therefore impossible to analyze the EM Interaction with the resistors.

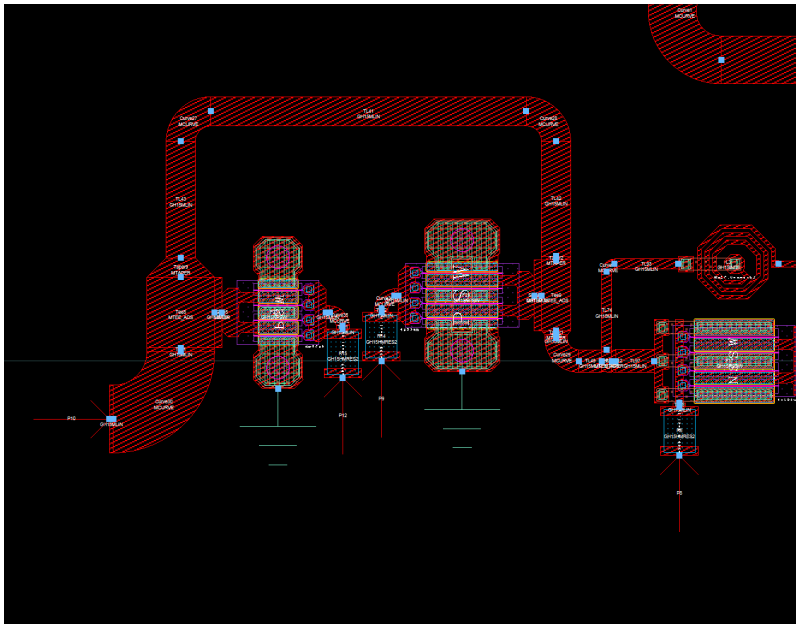


Figure 64: Layout of the switch with increased size, 1000 Ω resistors

4.8 Transient time analysis - Conclusion

The speed and efficiency of the switch, when implemented into a system, strongly depend on its rising and falling times, which must be minimized as much as possible. To achieve this, it has been observed that decreasing the gate resistances allows for faster response times. However, this optimization may lead to unwanted issues such as increased insertion losses and higher currents through the supply lines. Therefore, it must be carried out while ensuring that the design diligently complies with the imposed specifications. The plot down below enables a choice of compromise between insertion losses and transition times. Once a value for the resistance is chosen, the currents are sampled just like it was done in 62 and 63, If they do not exceed the boundaries, the design is considered appropriate; otherwise, the width of the resistances has to be increased until the problem is solved.

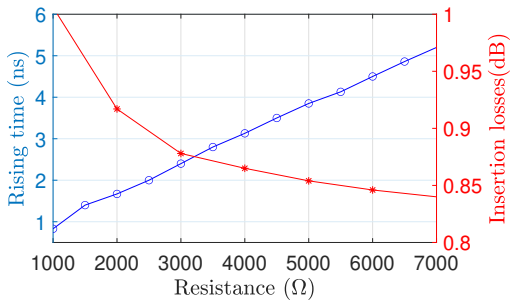


Figure 65: Resistance vs rising time and insertion losses

5 Reflexive switch - Measurement

5.1 Introduction

This section is devoted to the measurement of the RET3_A2_INDRA_V6WBSW high frequency switch circuit working in the 2-26 GHz band and contracted by the spanish company INDRA to the polytechnic university of Madrid(ETSIT). The circuit was manufactured using UMS GH15-10 GaN-on-SiC process and has the internal configuration that can be summerized in the scheme of figure 66. As can be seen, it is a SPDTI(Single Pole, Double Throw) switch, meaning that there will be a node(RF1) where the input signal will be entered. Depending on the two controlling voltages, VD1 and VD2, such signal will be routed towards either the RF2 node or the RF3 node.

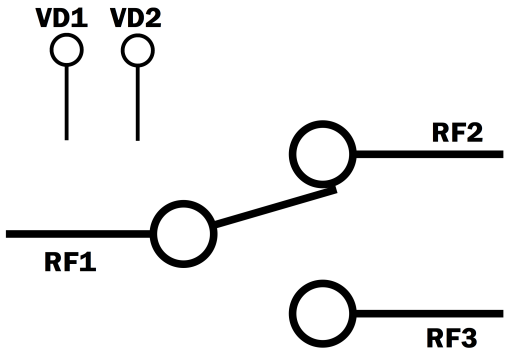


Figure 66: Theoretical schematic of the high frequency switch

5.2 Measurement procedure configuration

For the measurement, two configurations shown in the following table are considered:

SWITCH STATE	VD1	VD2
State 1: RF1 to RF2: ON RF1 to RF3: OFF	0 V	-20 V
State 2: RF1 to RF3: ON RF1 to RF2: OFF	-20 V	0 V

.

As the threshold voltage of the transistors used is around -3 V, 0 V will be the voltage applied to turn on the transistors, whereas the -20 V voltage is used to bring the transistors in cut-off conditions. Such voltage is the one recommended by UMS for switching applications. From the point of view of the system, it would be beneficial to have a value of the cut-off voltage as low as possible. Therefore the performances will also be tested for different cut-off voltages: -15 V, -10 V and -5 V. As can be seen in table 5.2, only two configurations are shown although technically there are four possible configurations. One of the missing configurations is the one with both branches in open state, meaning that VD1= VD2= -20 V. Such polarization will not be analyzed as the device is not designed to operate in the beforementioned conditions. The other configuration, with both branches operating is called

the "prohibited" state. The device is never supposed to operate in this state, as it might compromise the functioning of the device and from a logical point of view it does not make any sense as the signal will never be routed both to port RF2 and to port RF3 at the same time. Since the device under test is a multiport device(three ports) and the vector network analyzer has two connectors, a procedure will be carried out to extract the 3x3 S-parameter matrix, such procedure consists of measurements of the device where two out of the three ports are connected to the VNA and the remaining port is connected to a 50 Ohm load. For each measurement, the ports connected to the VNA are changed. In total 3 measurements are to be carried out to extract the scattering parameters. Considering also the two possible configurations illustrated in the table, this total up to six measurements in the end.

5.3 Measurement 1

In the first measurement, the configuration used is the one shown in figure 67, As can be seen in the illustrative picture 68, the ports of the VNA are connected to the port RF1 and RF2 of the switch, whereas the RF3 port is connected to a 50 Ohm load. In this conditions both the polarization states introduced in table 5.2 will be tested to extract the 2x2 S-Parameter matrix. As previously said, the performances are also tested for polarization voltages: -15 V, -10 V and -5 V.

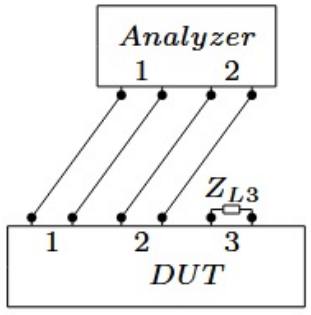


Figure 67: Measurement 1 configuration scheme

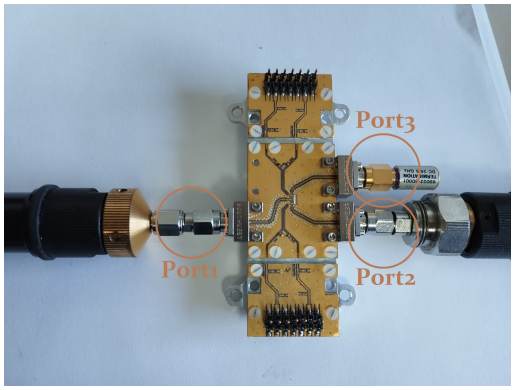


Figure 68: Measurement 1 illustrative picture

In the following part a list of instructions to carry out the measurement in the safest way possible for the device is presented:

1. VNA Calibration Using the SOLT Procedure
2. RF signal is set OFF.
3. RF1, RF2 ports are connected to the VNA. RF3 to the 50 Ohm impedance.
4. VDI1, VD2 ports are connected to the voltage supplier.
5. Voltage supply is set in the off state: VD1 = -20 V and VD2 = -20 V
6. RF1 $\rightarrow$ RF2 (ON state) : VD1 = 0 V
7. RF signal is set ON.

8. Measure → S-Parameters.
9. with VD2 set to -15 V, Measure → S-Parameters.
10. with VD2 set to -10 V, Measure → S-Parameters.
11. with VD2 set to -5 V, Measure → S-Parameters.
12. VD2 is returned to -20 V
13. RF signal is set OFF.
14. Voltage supply is set in the off state: VD1 = -20 V

Now that the S-Parameter have been measured for the ON State, the procedure will be repeated similarly for the OFF State.

1. RF1 → RF2 (OFF state) : VD2 = 0 V
2. RF signal is set ON.
3. Measure → S-Parameters.
4. with VD1 set to -15 V, Measure → S-Parameters.
5. with VD1 set to -10 V, Measure → S-Parameters.
6. with VD1 set to -5 V, Measure → S-Parameters.
7. VD1 is returned to -20 V
8. RF signal is set OFF.
9. Voltage supply is set in the off state: VD2 = -20 V
10. Disconnection

Note that special care should be taken to ensure that the device is always operating in the states for which it has been designed in order to preserve its functionality and performances. Such prohibited states are the ones where both branches are either OFF or ON, and the RF signal is in the ON state.

5.4 Measurement 2

The second measurement is completely analogous to the previous one, only the configuration is changed as shown in figure 69, As can be seen in the illustrative picture 70, the ports of the VNA are connected to the port RF1 and RF3 of the switch, whereas the RF2 port is connected to a 50 Ohm load. In this conditions both the polarization states introduced in table 5.2 will be tested to extract the 2x2 S-Parameter matrix. No initial calibration is necessary, as it has already been performed in the previous measurement procedure. As previously said, the performances are also tested for polarization voltages: -15 V, -10 V and -5 V.

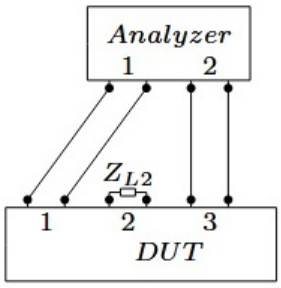


Figure 69: Measurement 2 configuration scheme

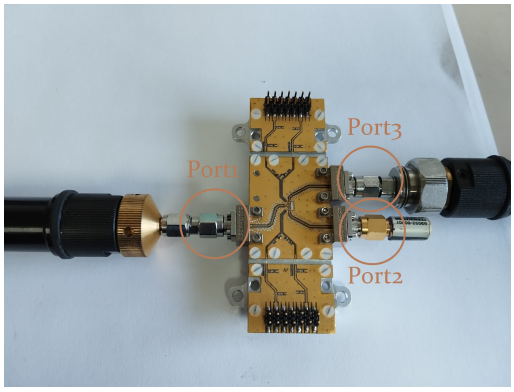


Figure 70: Measurement 2 illustrative picture

In the following part a list of instructions to carry out the measurement in the safest way possible for the device is presented:

1. RF signal is set OFF.
2. RF1, RF3 ports are connected to the VNA. RF2 to the 50 Ohm impedance.
3. VDI1, VD2 ports are connected to the voltage supplier.
4. Voltage supply is set in the off state: VD1 = -20 V and VD2 = -20 V
5. RF1 → RF3 (ON state) : VD2 = 0 V
6. RF signal is set ON.
7. Measure → S-Parameters.
8. with VD1 set to -15 V, Measure → S-Parameters.
9. with VD1 set to -10 V, Measure → S-Parameters.
10. with VD1 set to -5 V, Measure → S-Parameters.
11. VD1 is returned to -20 V
12. RF signal is set OFF.
13. Voltage supply is set in the off state: VD2 = -20 V

Now that the S-Parameter have been measured for the ON State, the procedure will be repeated similarly for the OFF State.

1. RF1 → RF3 (OFF state) : VD1 = 0 V
2. RF signal is set ON.
3. Measure → S-Parameters.
4. with VD2 set to -15 V, Measure → S-Parameters.

5. with VD2 set to -10 V, Measure → S-Parameters.
6. with VD2 set to -5 V, Measure → S-Parameters.
7. VD2 is returned to -20 V
8. RF signal is set OFF.
9. Voltage supply is set in the off state: VD1 = -20 V
10. Disconnection

5.5 Measurement 3

For the third measurement, an interface cable has been connected between the VNA port and the RF3 port, as the big size of the VNA connectors is not suitable for the close distance between port RF2 and RF3 of the device. The configuration used is the one shown in figure 71, As can be seen in the illustrative picture 72, the ports of the VNA are connected to the port RF2 and RF3 of the switch, whereas the RF1 port is connected to a 50 Ohm load. In this conditions both the polarization states introduced in table 5.2 will be tested to extract the 2x2 S-Parameter matrix. As previously said, the performances are also tested for polarization voltages: -15 V, -10 V and -5 V. Initially, re-calibration is carried out in order to nullify the effects of the newly introduced cable in the circuit.

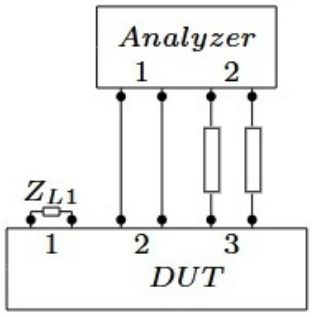


Figure 71: Measurement 3 configuration scheme

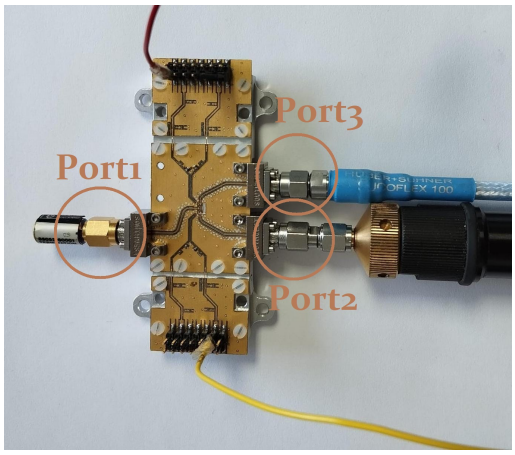


Figure 72: Measurement 3 illustrative picture

In the following part a list of instructions to carry out the measurement in the safest way possible for the device is presented:

1. VNA Re-Calibration Using the SOLT Procedure to eliminate the cable effects.
2. RF signal is set OFF.
3. RF2, RF3(with cable) ports are connected to the VNA. RF1 to the 50 Ohm impedance.
4. VDI1, VD2 ports are connected to the voltage supplier.

5. Voltage supply is set in the off state: VD1 = -20 V and VD2 = -20 V
6. RF2 → RF3 (ON state) : VD1 = 0 V
7. RF signal is set ON.
8. Measure → S-Parameters.
9. with VD2 set to -15 V, Measure → S-Parameters.
10. with VD2 set to -10 V, Measure → S-Parameters.
11. with VD2 set to -5 V, Measure → S-Parameters.
12. with VD2 is returned to -20 V
13. RF signal is set OFF.
14. Voltage supply is set in the off state: VD1 = -20 V

Now that the S-Parameters have been measured for the ON State, the procedure will be repeated similarly for the OFF State.

1. RF2 → RF3 (OFF state) : VD2 = 0 V
2. RF signal is set ON.
3. Measure → S-Parameters.
4. with VD1 set to -15 V, Measure → S-Parameters.
5. with VD1 set to -10 V, Measure → S-Parameters.
6. with VD1 set to -5 V, Measure → S-Parameters.
7. VD1 is returned to -20 V
8. RF signal is set OFF.
9. Voltage supply is set in the off state: VD2 = -20 V
10. Disconnection

5.6 Criticalities of the process

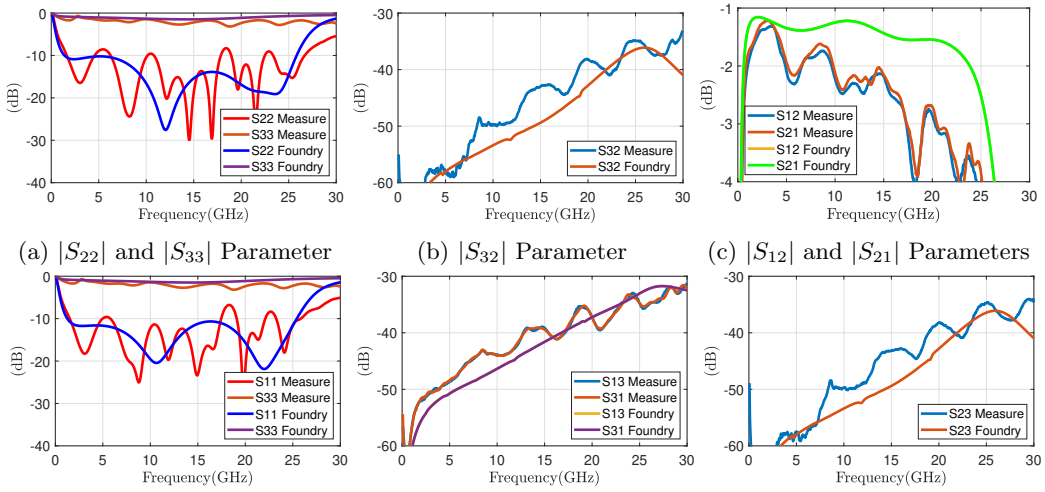
Special care should be ensured when handling the device, as the metal bondings which connect the circuit to the ports are very fragile and even the slightest contact with any object(cables or the hand of the operator) will permanently compromise the functioning of the device. In order for the measurement to be more accurate, the 50 Ohm reference impedance frequency response can be measured and included in the S-Parameters evaluation.

5.7 Conclusion

The results of the six measurements can now be fed to a Matlab script which will extract the S-Parameters of the 3x3 matrix of the switch device. The script can be found at the appendix in 6.3.

5.8 Results - S-Parameters of the (1 → 2) ON configuration comparison

In this section, after the extraction from the measurement of the 3x3 S-Matrix of the switch, a comparison is carried out between the obtained results and the measurements provided by the foundry of the device itself.



(a) $|S_{22}|$ and $|S_{33}|$ Parameter (b) $|S_{32}|$ Parameter (c) $|S_{12}|$ and $|S_{21}|$ Parameters

(d) $|S_{11}|$ and $|S_{33}|$ Parameter (e) $|S_{13}|$ and $|S_{31}|$ Parameters (f) $|S_{23}|$ Parameter

Figure 73: Comparison estimation of isolation, insertion losses and reflection losses between laboratory measurement and foundry measurements

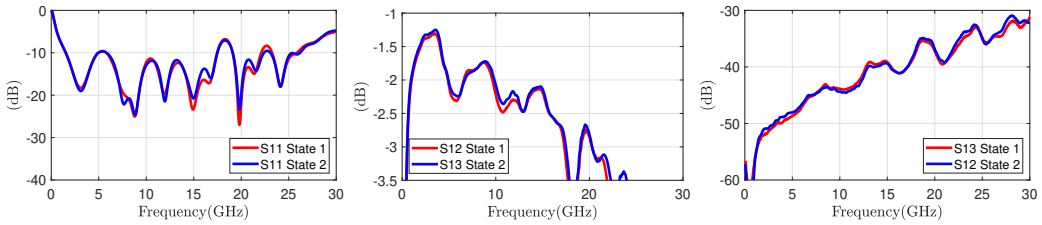
.

It appears like the lab measurements parameters display worse behaviours than the ones of the foundry, the situacion for the insertion loss, As can be seen in figure 73c is particularly remarkable: in the foundry simulated results the insertion loss in band does not go beyond 1.5 dB, whereas the insertion loss in the lab measurement reaches almost 4 dB. The situation for the reflection losses is also concerning, with the S_{11} parameter reaching almost -5 dB in band, as shown in 73a and the S_{22} in 73d going a little over -10 dB. For the isolation, a degradation can be clearly seen in figures 73b and 73e. the measurements at UMS were carried out on-wafer, meaning that the VNA was directly connected to the ports of the RF circuit. This is otherwise not the case for the measurement procedure that has been so far illustrated. The die is now mounted onto an uncalibrated PCB with microstrip lines and connectors which are inevitably contributing to the degradation of the results. So are the uncontrolled effects of the bondings. As a result of this, the difference between the two measurement results is striking, which makes question the efficiency of the procedure. A TRL calibration set has to be developed to account for this microstrip environment. This TRL calibration set is under development in the ETSIT department, and it will allow to

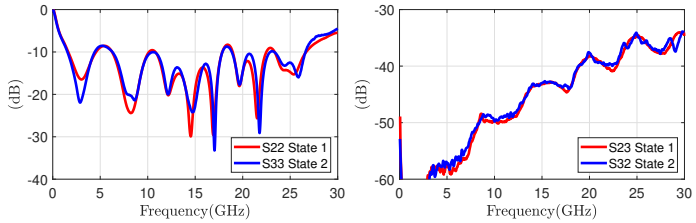
deembed such added elements to the MMIC in the future.

5.9 Results - State 1 - State 2 configurations comparison

Following the comparison with the foundry measurements, it is also interesting to carry out a comparison of the measurements in the State 1 and State 2 configurations(table 5.2 is used as reference). In principle, the results should be the same since both branches of the switch have been designed to be symmetrical. Of course it must be noted that the comparison must take into account the change of the active branch, meaning that it makes sense to compare the S_{12} parameter of the ON configuration and the S_{13} of the OFF configuration, and so forth for the other S-Parameters. The resulting comparison is the one that follows:



(a) $|S_{11}|$ Parameter (b) $|S_{12}|$ and $|S_{13}|$ Parameters (c) $|S_{13}|$ and $|S_{12}|$ Parameters



(d) $|S_{22}|$ and $|S_{33}|$ Parameters (e) $|S_{32}|$ and $|S_{23}|$ Parameters

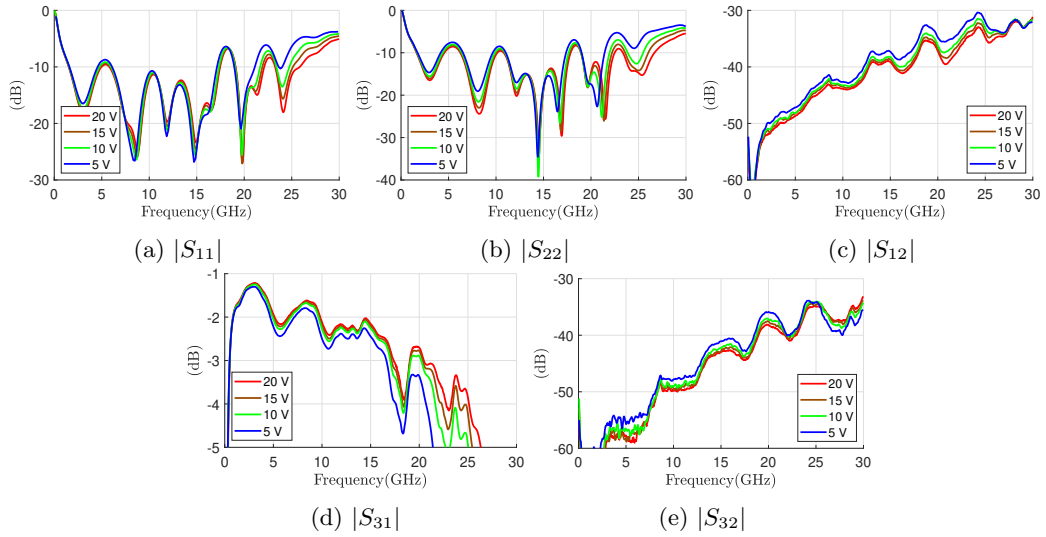
Figure 74: omparison estimation of isolation, insertion losses and reflection losses between laboratory State 1 and State 2 configurations

.

As can be seen the results of the OFF configuration closely mimic the previously illustrated ON configuration results. The differences are however negligible and most likely attributable to mounting asymmetries or measurement errors.

5.10 Results - Polarization variations comparison

it is interesting to see what happens to the performances of the high frequency switch whenever the nominal polarization voltage used to turn off each transistor is increased from -20 V up to -5 V. Using a lower voltage is helpful for the device, however it is important to do this type of analysis to verify that such lowering does not compromise the expected specifications. In the following graphs, all the resulting S-Parameters are shown sweeping the polarization voltage as previously illustrated:



(a) $|S_{11}|$ (b) $|S_{22}|$ (c) $|S_{12}|$

(d) $|S_{31}|$ (e) $|S_{32}|$

Figure 75: Comparison estimation of isolation, insertion losses and reflection losses with different polarization voltages

.

As can be seen from the graphs in 75a and 75b, the reflection performances become worse the higher the voltage, with curves that show visible higher reflections for 5 V polarization. The same can be said about the insertion losses shown in 75c, and the isolation in 75d and 75e. Overall it can be stated that the higher the polarization the worse the performances. This makes sense if the theory illustrated in the first chapter is taken into account. In fact, the higher the voltage, the less efficient is the cut-off behaviour of each turned OFF transistor.

5.11 Temperature analysis

In the wide variety of implementations in which the high frequency switch so far described can be included, it is important to ensure the correct operation of it and the satisfaction of the specifications for temperatures different from the nominal one(usually around 25 C°). This section is devoted to the analysis of the performances of the device for temperatures in a range spanning from 5 C° and 65 C°. In order to bring the device to such temperatures, it will be placed(like in 77) in the commercial VTL4010 technical oven that can be seen in figure 76, where then the measurement will be carried out like previously done with the vector network analyzer, connected to the device with temperature resistent cables going through the side holes of the oven.

Figure 76: Vötsch Industrietechnik VTL4010 Oven

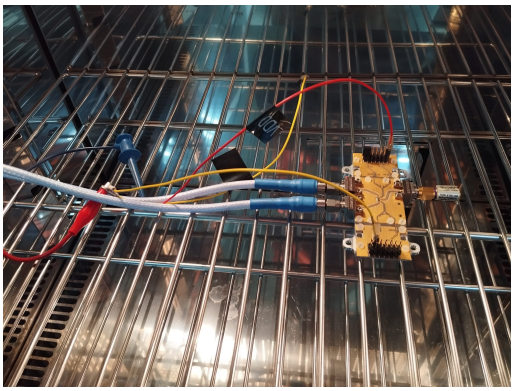


Figure 77: Picture of the measurement setting

5.12 Temperature measurement procedure

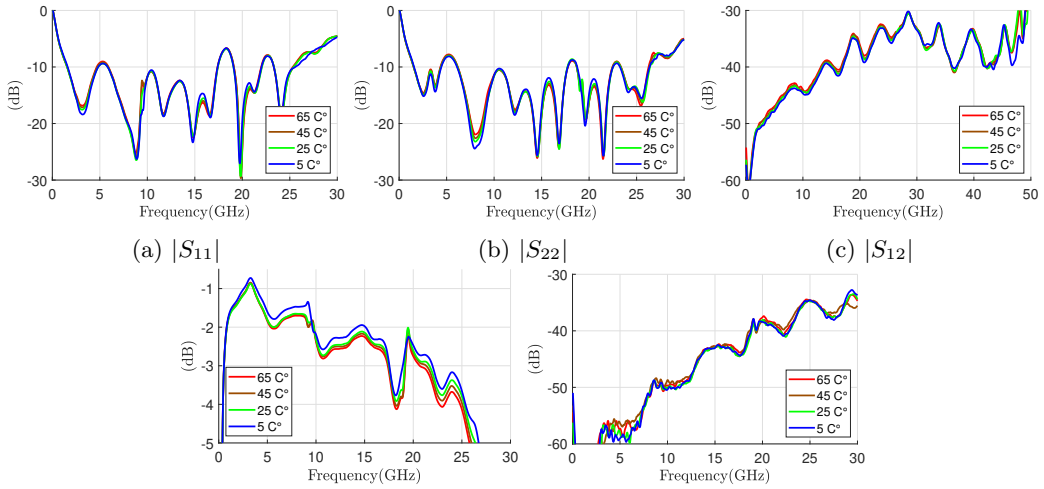
The procedure that follow must be followed carefully in order not to tarnish the measurements and at the same time to not compromise the functioning of the machine by going against the indications imposed in the instructions. Unlike in section 1.2, the measurement will be carried out using only -20 V as "OFF" Polarization, and only the "ON" ($1 \rightarrow 2$) configuration of table 5.2 will be analyzed, as the effect of these two parameters have already been illustrated previously.

1. No contact between the measurement system and direct sunlight is ensured.
2. At least 2.5 m3/kg of refrigerant to the system are being provided
3. temperature limiters set(5 C° lower than the lower bound and 5 C° higher than the upper bound)
4. The circuit to be measured is positioned evenly in the designated space, the cables are connected to the VNA and the voltage supplier through the side holes with both polarization and RF signal turned OFF.
5. VNA Calibration is carried out(Oven turned OFF).
6. The side holes are sealed with sealing plugs.
7. Main switch is turned to 'I'
8. Light switch is turned on
9. The setpoint for the temperature is selected equal to 5°
10. The measurement is carried out following the procedure illustrated in section 1.2. After the measurement the system is set at room temperature, an appropriate time is waited for the temperature to settle
11. The setpoint for the temperature is selected equal to 25°

12. The measurement is carried out following the procedure illustrated in section 1.2. After the measurement the system is set at room temperature, an appropriate time is waited for the temperature to settle
13. The setpoint for the temperature is selected equal to 45°
14. The measurement is carried out following the procedure illustrated in section 1.2. After the measurement the system is set at room temperature, an appropriate time is waited for the temperature to settle
15. The setpoint for the temperature is selected equal to 65°
16. The measurement is carried out following the procedure illustrated in section 1.2. After the measurement the system is set at room temperature, an appropriate time is waited for the temperature to settle
17. The system is put out of operation
18. The circuit and the equipment is withdrawn from the oven.

5.13 Temperature measurement results

As it has been previously said, the measurement is carried out with the $(1 \rightarrow 2)$ branch being turned ON and with -20 V polarization voltage, the results are the ones that follow:



(a) $|S_{11}|$ (b) $|S_{22}|$ (c) $|S_{12}|$

(d) $|S_{31}|$ (e) $|S_{32}|$

Figure 78: Comparison estimation of isolation, insertion losses and reflection losses with for different temperatures

.

As can be seen, the variation of temperature does not appear to affect the performance of the switch considerably. The transmission parameters in 78c seem to be affected the most, although of only about a tenth of a dB. In general, the lower the temperature the lower the insertion losses. No appreciable difference can be seen in the isolation parameters in 78d and 78e. The same can be said about the reflection parameters in 78a and 78b. In conclusion this device has to be tested in a broader temperature range to better account for environments where it could operate.

Conclusions

The complete MMIC circuit design cycle was followed. The design has proven to exceed the imposed expectations. Furthermore, the analysis has been completed by the addition of the Monte Carlo analysis, which allowed to see the influence od manufacturing inaccuracies of the components, and the timing analysis, which allowed to find useful strategies to make the switch faster. Finally, experimental characterization provided insight into how realistic the simulations obtained with the design software are, and the possible variations in the fabricated circuit, due to temperature fluctuations and manufacturing inaccuracies.

6 Appendix

6.1 Appendix A

To express the different dimensions of the various components used in the design of the radio frequency switch, the nomenclature indicated in Figures 79, 80, 81a, 81b, 82, 83, and 84 has been used. In Figures 79 and 80, only a single branch will be shown due to the symmetry of the radio frequency switch.

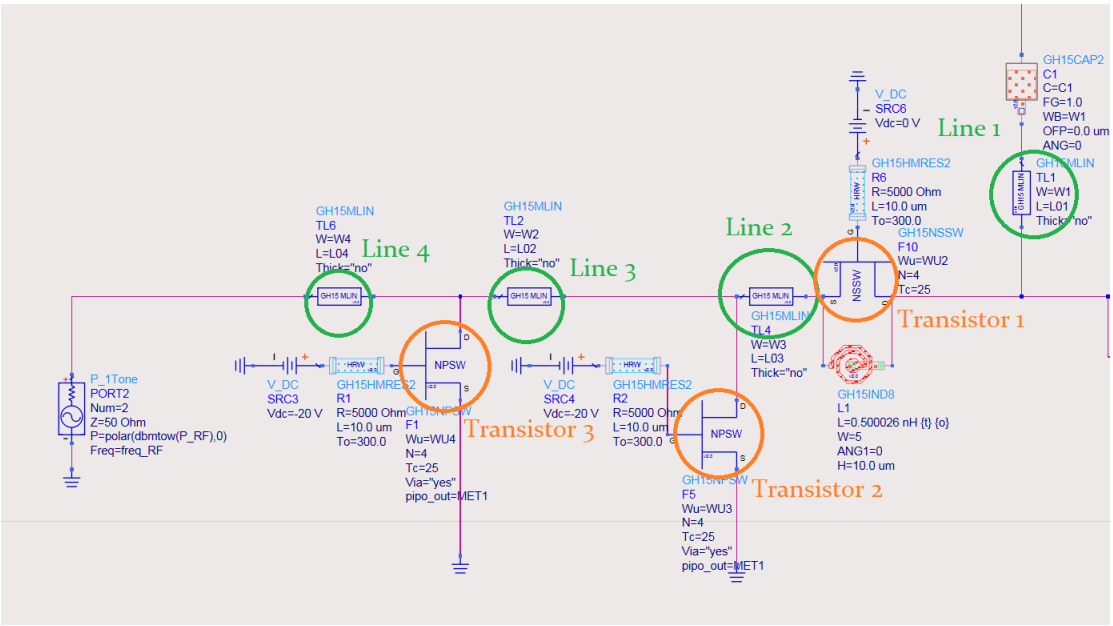


Figure 79: Nomenclature of the components of the radio frequency design for the circuit with no geometry

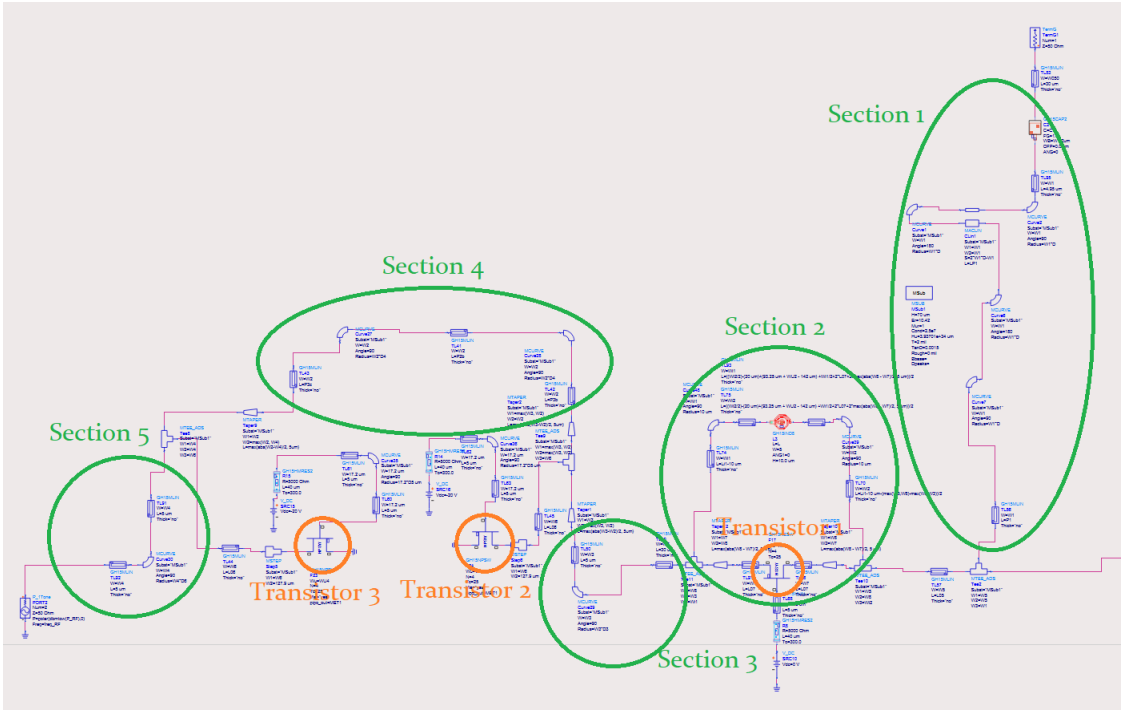
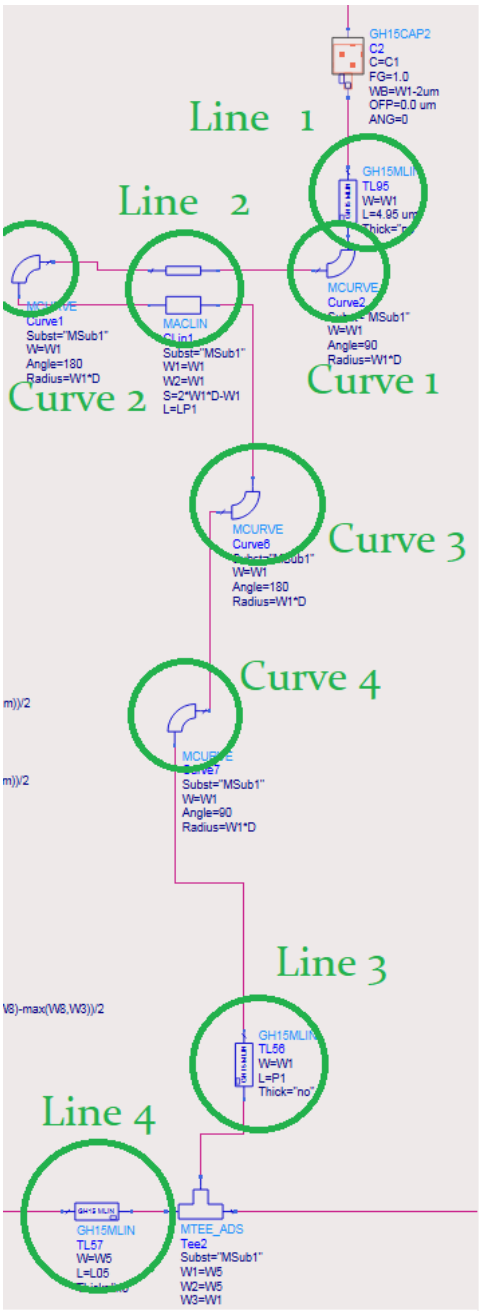
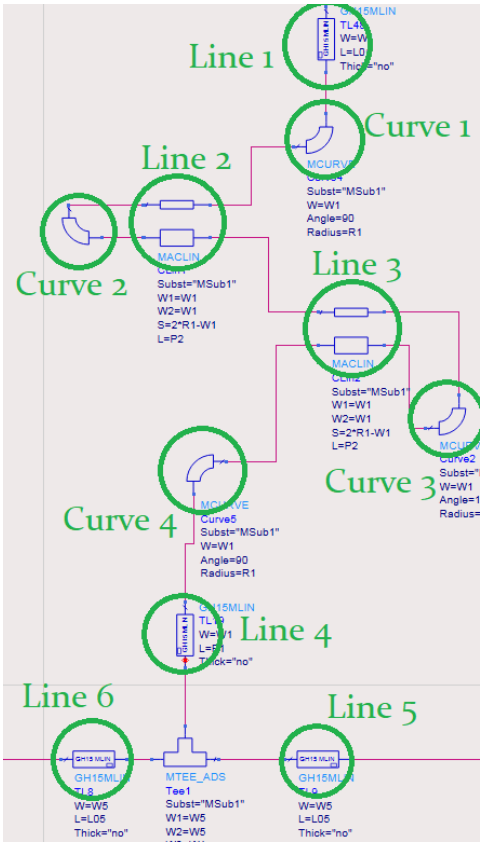


Figure 80: Nomenclature of the components of the radio frequency design for the circuit with no geometry



(a) Section 1 with geometry



(b) Section 1 with EM Cosimulation

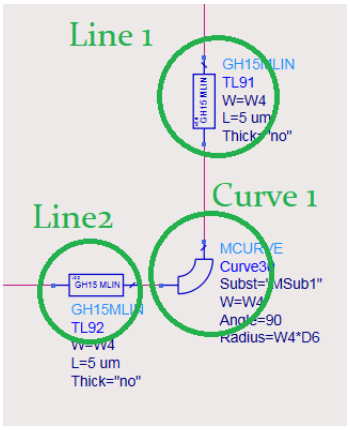


Figure 82: Section 5

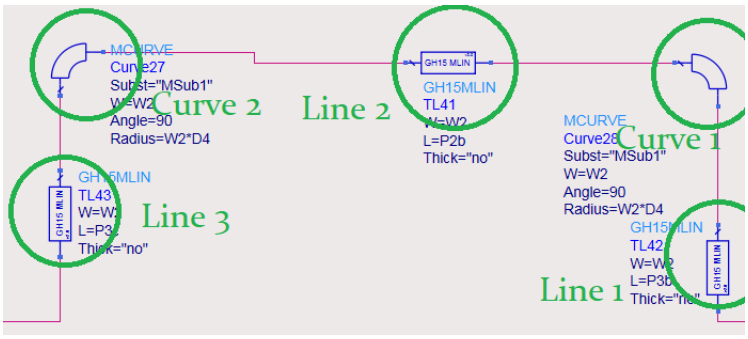


Figure 83: Section 4

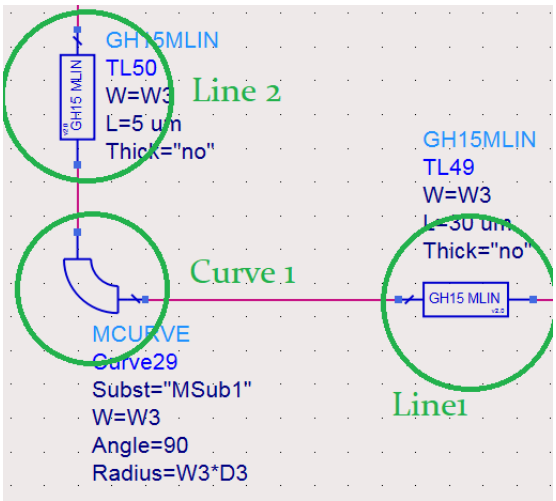


Figure 84: Section 3

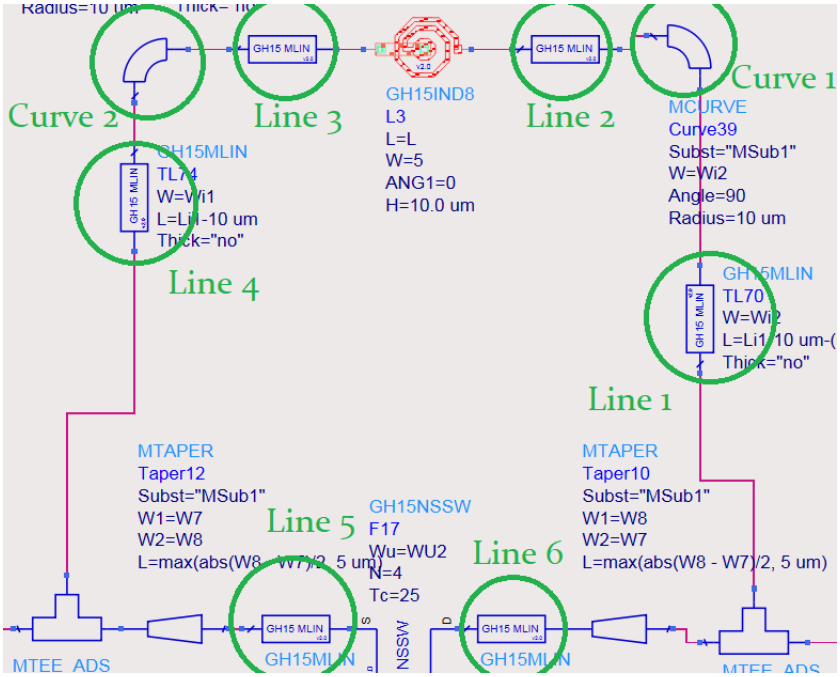


Figure 85: Section 2

6.1.1 Dimensions for the circuit with no geometry

These tables follow the nomenclature developed in Figure 79.

Element	Width (μm)	Number of fingers
Transistor 1	99.9186	4
Transistor 2	35.0426	4
Transistor 3	66.154	4

Element	Width (μm)	Capacity (pF)
Capacitor	40.0898	8.40407

Element	Width (μm)	Inductance (nH)
Inductor	5	0.5

Element	Width (μm)	Length (μm)
Line 1	40.0898	835.81
Line 2	40.8947	781.968
Line 3	28.213	82.7994
Line 4	35.9762	50.9227

Element	Length (μm)	Value (Ω)
Resistance	10	5000

6.1.2 Dimensions for the circuit with geometry

These tables follow the nomenclature developed in Figure 80.

Element	**Width (μm)**	**Number of fingers**
Transistor 1	98.5352	4
Transistor 2	50.7228	4
Transistor 3	51.7047	4

Element section 1	**Width (μm)**	**Length (μm)**
Line 1	33.5122	4.95
Line 2	33.5122	302.352
Line 3	33.5122	161.463
Line 4	30.2942	50.1126

Element section 1	**Width (μm)**	**Radius (μm)**
Curve 1	33.5122	43.46586
Curve 2	33.5122	43.46586
Curve 3	33.5122	43.46586
Curve 4	33.5122	43.46586

Element section 2	**Width (μm)**	**Length (μm)**
Line 1	8.68785	101.781
Line 2	8.68785	76.149
Line 3	13.5312	76.149
Line 4	13.5312	101.781
Line 5	30.2006	50.701
Line 6	30.2006	50.701

Element section 2	**Width (μm)**	**Radius (μm)**
Curve 1	8.68785	10
Curve 2	13.5312	10

Element section 3	**Width (μm)**	**Length (μm)**
Line 1	28.9236	30
Line 2	28.9236	5

Element section 3	**Width (μm)**	**Radius (μm)**
Curve 1	28.9236	28.8368

Element section 4	Width (μm)	Length (μm)
Line 1	52.4564	152.268
Line 2	52.4564	370.099
Line 3	52.4564	153.866

Element section 4	Width (μm)	Radius (μm)
Curve 1	52.4564	43.2311
Curve 2	52.4564	43.2311

Element section 5	Width (μm)	Length (μm)
Line 1	89.2247	5
Line 2	89.2247	5

Element section 5	Width (μm)	Radius (μm)
Curve 1	89.2247	85.5438

Element	Width (μm)	Capacity (pF)
Capacitor	31.5122	6.56682

Element	Width (μm)	Inductance (nH)
Inductor	5	1.02085

Element	Length (μm)	Value (Ω)
Resistance	10	5000

6.1.3 Dimensions for the circuit with individual pieces electromagnetically simulated

These tables follow the nomenclature developed in Figure 80.

Element	Width (μm)	Number of fingers
Transistor 1	104.389	4
Transistor 2	45.6056	4
Transistor 3	51.7047	4

Element section 1	**Width (μm)**	**Length (μm)**
Line 1	35.7657	5
Line 2	35.7657	10
Line 3	35.7657	10
Line 4	35.7657	161.463
Line 5	35.7657	50.1126
Line 6	35.7657	50.1126

Element section 1	**Width (μm)**	**Radius (μm)**
Curve 1	35.7657	36.7005
Curve 2	35.7657	36.7005
Curve 3	35.7657	36.7005
Curve 4	35.7657	36.7005

Element section 2	**Width (μm)**	**Length (μm)**
Line 1	8.66207	102.114
Line 2	8.66207	83.752
Line 3	13.4207	83.752
Line 4	13.4207	102.114
Line 5	30.1995	50.6305
Line 6	30.1995	50.6305

Element section 2	**Width (μm)**	**Radius (μm)**
Curve 1	8.68785	10
Curve 2	13.5312	10

Element section 3	**Width (μm)**	**Length (μm)**
Line 1	29.487	30
Line 2	29.487	5

Element section 3	**Width (μm)**	**Radius (μm)**
Curve 1	29.487	29.9644

Element section 4	**Width (μm)**	**Length (μm)**
Line 1	28.6723	152.268
Line 2	28.6723	370.335
Line 3	28.6723	153.866

Element section 4	Width (μm)	Radius (μm)
Curve 1	28.6723	29.4166
Curve 2	52.4564	29.4166

Element section 5	Width (μm)	Length (μm)
Line 1	88.8875	5
Line 2	88.8875	5

Element section 5	Width (μm)	Radius (μm)
Curve 1	88.8875	88.7141

Element	Width (μm)	Capacity (pF)
Capacitor	33.7657	7.23775

Element	Width (μm)	Inductance (pH)
Inductor	5	713.927

Element	Length (μm)	Value (Ω)
Resistance	10	5000

6.1.4 Dimensions for the circuit with the complete layout

These tables follow the nomenclature developed in Figure 80.

Element	Width (μm)	Number of fingers
Transistor 1	104.386	4
Transistor 2	93.1625	4
Transistor 3	51.7047	4

Element section 1	Width (μm)	Length (μm)
Line 1	62.9354	4.95
Line 2	62.9354	319.879
Line 3	62.9354	187.004
Line 4	62.9354	50.1126

Element section 1	Width (μm)	Radius (μm)
Curve 1	62.9354	64.5531
Curve 2	62.9354	64.5531
Curve 3	62.9354	64.5531
Curve 4	62.9354	64.5531

Element section 2	**Width (μm)**	**Length (μm)**
Line 1	8.66207	102.368
Line 2	8.66207	83.969
Line 3	13.4207	83.969
Line 4	13.4207	102.368
Line 5	30.1995	50.6305
Line 6	30.1995	50.6305

Element section 2	**Width (μm)**	**Radius (μm)**
Curve 1	8.68785	10
Curve 2	13.5312	10

Element section 3	**Width (μm)**	**Length (μm)**
Line 1	29.487	30
Line 2	29.487	5

Element section 3	**Width (μm)**	**Radius (μm)**
Curve 1	29.487	29.9827

Element section 4	**Width (μm)**	**Length (μm)**
Line 1	38.2542	151.294
Line 2	38.2542	415.023
Line 3	38.2542	153.329

Element section 4	**Width (μm)**	**Radius (μm)**
Curve 1	38.2542	39.1910
Curve 2	38.2542	39.1910

Element section 5	**Width (μm)**	**Length (μm)**
Line 1	88.8875	5
Line 2	88.8875	5

Element section 5	**Width (μm)**	**Radius (μm)**
Curve 1	88.8875	88.7141

Element	**Width (μm)**	**Capacity (pF)**
Capacitor	60.9354	7.23775

Element	Width (μm)	Inductance (pH)
Inductor	5	713.927

Element	Length (μm)	Value (Ω)
Resistance	10	5000

6.2 Appendix B

This appendix gathers the maximum and recommended currents, both DC and RMS current, of the lines and resistances provided by UMS in the PDK manual[18].

Component	Measurement Unit	Recommended DC	Max DC
TaN Resistance	mA/μm	0.45	0.5
TiWSi Resistance	mA/μm	0.1	0.13
MET1 Microstrip	mA/μm	11	14.5

Table 3: Recommended and maximum DC current values set by UMS.

Component	Measurement Unit	Recommended RMS	Max RMS
TaN Resistance	mA/μm	2	3.5
TiWSi Resistance	mA/μm	0.4	0.53
MET1 Microstrip	mA/μm	47	62.5

Table 4: Recommended and maximum RMS current values set by UMS.

6.3 Appendix C

In this section of the appendix, the script used to assemble the 3x3 S-parameter matrix using the three two ports measurements illustrated in chapter 5 is presented. The theoretical procedure behind the functioning of the script can be found in the references[19]

```
%reading frequency, first step
table=readtable("Measurement1.txt");
F=table2array(table(:,1));
numsamples=length(F);

%Inizializations




Z0=50;
ZL=zeros(1,numsamples);
U2=[1 0; 0 1];
U3=[1 0 0 ; 0 1 0 ; 0 0 1];
```

```
G2=zeros(2,2);
Gamma2=zeros(2,2);
G3=zeros(3,3);
Gamma3=zeros(3,3);

%Inizializ. of measured matrixes numbered according to the lecture notes

S_one=zeros(2,2,numsamples);
S_two=zeros(2,2,numsamples);
S_three=zeros(2,2,numsamples);

%Final result matrixes

S_one_B=zeros(2,2,numsamples);
S_two_B=zeros(2,2,numsamples);
S_three_B=zeros(2,2,numsamples);


S_Z=zeros(3,3,numsamples);
S_Z0=zeros(3,3,numsamples);

%Variables for the plots
S11_Duplicates=zeros(numsamples,2);
S22_Duplicates=zeros(numsamples,2);
S33_Duplicates=zeros(numsamples,2);

S1=zeros(numsamples,3);
S2=zeros(numsamples,3);
S3=zeros(numsamples,3);

S1p=zeros(numsamples,3);
S2p=zeros(numsamples,3);
S3p=zeros(numsamples,3);

%Data is read from the files
table=readtable("Measurement1.txt");

S_one11=10.^(table2array(table(:,2))/20).*exp(1i*deg2rad(table2array(table(:,3))));
S_one21=10.^(table2array(table(:,4))/20).*exp(1i*deg2rad(table2array(table(:,5))));
S_one12=10.^(table2array(table(:,6))/20).*exp(1i*deg2rad(table2array(table(:,7))));
S_one22=10.^(table2array(table(:,8))/20).*exp(1i*deg2rad(table2array(table(:,9))));

table=readtable("Measurement2.txt");
```

```
S_two11=10.^(table2array(table(:,2))/20).*exp(1i*deg2rad(table2array(table(:,3))));
S_two31=10.^(table2array(table(:,4))/20).*exp(1i*deg2rad(table2array(table(:,5))));
S_two13=10.^(table2array(table(:,6))/20).*exp(1i*deg2rad(table2array(table(:,7))));
S_two33=10.^(table2array(table(:,8))/20).*exp(1i*deg2rad(table2array(table(:,9))));

table=readtable("Measurement3.txt");

S_three22=10.^(table2array(table(:,2))/20).*exp(1i*deg2rad(table2array(table(:,3))))
S_three32=10.^(table2array(table(:,4))/20).*exp(1i*deg2rad(table2array(table(:,5))))
S_three23=10.^(table2array(table(:,6))/20).*exp(1i*deg2rad(table2array(table(:,7))))
S_three33=10.^(table2array(table(:,8))/20).*exp(1i*deg2rad(table2array(table(:,9))))


ReflCoeff=zeros(1,length(F));

for i=1:numsamples

    %Assignment

    ZL(i)=(ReflCoeff(i)+1)*Z0/(1-ReflCoeff(i));


    S_one(1,1,i)=S_one11(i);
    S_one(1,2,i)=S_one12(i);
    S_one(2,1,i)=S_one21(i);
    S_one(2,2,i)=S_one22(i);

    S_two(1,1,i)=S_two11(i);
    S_two(1,2,i)=S_two13(i);
    S_two(2,1,i)=S_two31(i);
    S_two(2,2,i)=S_two33(i);

    S_three(1,1,i)=S_three22(i);
    S_three(1,2,i)=S_three23(i);
    S_three(2,1,i)=S_three32(i);
    S_three(2,2,i)=S_three33(i);
    %End of assignment

    %Conversion of two port matrices
    G2=[sqrt(Z0/ZL(i)) 0; 0 sqrt(Z0/ZL(i))];
    Gamma2=[(ZL(i)-Z0)/(Z0+ZL(i)) 0; 0 (ZL(i)-Z0)/(Z0+ZL(i))];
    S_one_B(:,:,i)=G2*inv(U2-S_one(:,:,i))*(S_one(:,:,i)-Gamma2)* ...
    inv(U2-S_one(:,:,i)*Gamma2)*(U2-S_one(:,:,i))*inv(G2);
```

```
    G2=[sqrt(Z0/ZL(i)) 0; 0 sqrt(Z0/ZL(i))];
    Gamma2=[(ZL(i)-Z0)/(ZL(i)+Z0) 0; 0 (ZL(i)-Z0)/(Z0+ZL(i))];
    S_two_B(:,:,i)=G2*inv(U2-S_two(:,:,i))*(S_two(:,:,i)-Gamma2)* ...
    inv(U2-S_two(:,:,i)*Gamma2)*(U2-S_two(:,:,i))*inv(G2);

    G2=[sqrt(Z0/ZL(i)) 0; 0 sqrt(Z0/ZL(i))];
    Gamma2=[(ZL(i)-Z0)/(Z0+ZL(i)) 0; 0 (ZL(i)-Z0)/(Z0+ZL(i))];
    S_three_B(:,:,i)=G2*inv(U2-S_three(:,:,i))*(S_three(:,:,i)-Gamma2)* ...
    inv(U2-S_three(:,:,i)*Gamma2)*(U2-S_three(:,:,i))*inv(G2);

    %End of two port matrices

    S_Z(:,:,i)=[S_one_B(1,1,i) S_one_B(1,2,i) S_two_B(1,2,i);
          S_one_B(2,1,i) S_one_B(2,2,i) S_three_B(1,2,i);
          S_two_B(2,1,i) S_three_B(2,1,i) S_three_B(2,2,i);
     ];

    %Conversion of three port matrix
    G3=[sqrt(ZL(i)/Z0) 0 0 ; 0 sqrt(ZL(i)/Z0) 0 ; 0 0 sqrt(ZL(i)/Z0)];
    Gamma3=[(Z0-ZL(i))/(Z0+ZL(i)) 0 0 ; 0 (Z0-ZL(i))/(Z0+ZL(i)) 0 ;
    0 0 (Z0-ZL(i))/(Z0+ZL(i))];
    S_Z0(:,:,i)=G3*inv(U3-S_Z(:,:,i))*(S_Z(:,:,i)-Gamma3)* ...
    inv(U3-S_Z(:,:,i)*Gamma3)*(U3-S_Z(:,:,i))*inv(G3);
end

%The 3x3 Matrix has been assembled, and it is stored inside the S_Z0 matrix
```

References

[1] A. Ferreras Estrada, A. Prieto Poyatos, E. Antolinos, M. Ferreras, J. L. Jiménez-Martín, E. Oreja-Gigorro, J. Montero-de-Paz, A. Bódalo-Márquez, V. González-Posadas, J. Grajal and J. J. Sánchez-Martínez. "Diseño de MMICs en GaN para Nuevos Sistemas AESA de Guerra Electrónica". In: (Sept. 2023).

[2] Norshakila Haris et al. "Design and analysis of compact MMIC switches utilising GaAs pHEMTs in 3D multilayer technology". In: *Semiconductor Science and Technology* 32.5 (2017), p. 055014.

[3] Plextek RF Integration. *DC to 20GHz High Linearity GaN SPDT Switch MMIC*. White paper.

[4] David M Pozar. *Microwave engineering: theory and techniques*. John wiley & sons, 2021.

[5] Manuel Sierra Pérez et al. *Electrónica de comunicaciones*. Pearson Educación, 2003.

[6] Pat Hindle. "The state of RF/microwave switches". In: *microwave journal* 53.11 (2010), pp. 20–36.

[7] Charles F Campbell and Deep C Dumka. "Wideband high power GaN on SiC SPDT switch MMICs". In: *2010 IEEE MTT-s International Microwave Symposium*. IEEE. 2010, pp. 145–148.

[8] Bob Y Ma et al. "High power AlGaN/GaN Ku-band MMIC SPDT switch and design consideration". In: *2008 IEEE MTT-S International Microwave Symposium Digest*. IEEE. 2008, pp. 1473–1476.

[9] Vincenzo Alleva et al. "High-power monolithic AlGaN/GaN high electron mobility transistor switches". In: *International Journal of Microwave and Wireless Technologies* 1.4 (2009), pp. 339–345.

[10] Qorvo. *QPC2040 X-Band 10 W GaN SPDT Switch*. Datasheet. `https://www.qorvo.com/products/p/QPC2040`.

[11] Qorvo. *CMD196C3 DC-18 GHz SPDT Non-reflective Switch*. Datasheet. `https://www.qorvo.com/products/p/CMD196C3`.

[12] Stephen A Maas. *Nonlinear microwave and RF circuits*. Artech house, 2003.

[13] Keysight Technologies Inc. *Pathwave Advanced Design System 2021 - Harmonic Balance Simulation*. Keysight Technologies Inc. 2021.

[14] Keysight Technologies Inc. *Pathwave Advanced Design System 2021 - Electromagnetic Simulation*. Keysight Technologies Inc. 2021.

[15] Roger F Harrington. *Field computation by moment methods*. Wiley-IEEE Press, 1993.

[16] Keysight Technologies Inc. *Pathwave Advanced Design System 2021 - Tuning, Optimization and Statistical Design*. Keysight Technologies Inc. Santa Rosa, CA, 2021.

[17] United Monolithic Semiconductor. *UMS_GaN_PDK_for_ADS*. 2009.

[18] United Monolithic Semiconductor. *SP-maximum-Ratings-GH15-1x*. 2022.

[19] J.C. Tippet and R.A. Speciale. “A Rigorous Technique for Measuring the Scattering Matrix of a Multiport Device with a 2-Port Network Analyzer”. In: *IEEE Transactions on Microwave Theory and Techniques* 30.5 (1982), pp. 661–666. DOI: 10.1109/TMTT.1982.1131118.