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FPGA porting and benchmark across different manufacturers

Supervisors

Prof. Mario Roberto CASU

Eng. Riccardo STICCA

Candidate

Maria Pia PIRI

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Abstract

In the dynamic field of avionics systems, the rapid evolution of technology is a constant threat to the longevity of avionics projects. This challenge is particularly evident for key components such as Field Programmable Gate Arrays (FPGAs), which can quickly become obsolete. Specifically, a FPGA is a type of integrated circuit that can be programmed and configured by users to implement any digital circuit.
Recognizing the importance of addressing this challenge, this thesis, conducted in collaboration with **Leonardo Electronics** and based on a real project using two specific FPGAs, aims to identify possible alternatives among those available on the market while keeping the power consumption unchanged. Therefore, the goal of this thesis is to propose a method for the timely replacement of potentially obsolete components with alternative technological solutions, in order to ensure the resilience and longevity of avionics systems. A key consideration includes a benchmark by porting the original code to new potential candidate platforms.
For reasons of confidentiality, the project architecture has not been analyzed in detail in the chapters and is referred to as the "**reference architecture**".
In researching potential alternative FPGAs , it is important to consider the key factors that differentiate one FPGA from another, including the manufacturing process, logic blocks, memory, DSP capabilities and I/O compatibility. These factors play a significant role in determining the performance, capabilities, and suitability of an FPGA for specific applications. In this regard, current FPGAs in use are considered as evaluation baseline. In addition, compliance with the Radio Technical Commission for Aeronautics (RTCA) DO-254 standard is required. This standard ensures the safety and reliability of airborne electronic hardware.
Once the FPGAs were selected, in order to collect the required implementation results, a full design run including synthesis, place and route as well as power simulation was performed using Xilinx VIVADO 2019.1, Microchip LIBERO 2021.3, INTEL QUARTUS 18.0 and Lattice Radiant 2023.1.
In particular, the benchmark process enables the comparison of power consumption and performance among FPGAs. It provides an overview of the impact of technology on power consumption, assuming that performance remains unchanged.

Hence, the results highlight the advantages and disadvantages of all the FPGAs selected and help to evaluate and select the best candidates to replace the FPGAs currently in use.

Acknowledgements

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Chapter 1

Introduction

1.1 Avionics systems: DO-254 standard

The thesis was conducted in collaboration with **Leonardo Electronics** at the Caselle plant. Since 1950 the Caselle Plant is involved into the design and production of Avionics Systems.
Specifically, the **avionics systems** include complex electronic hardware such as **Field Programmable Gate Arrays** (FPGAs). These components need to comply with the Radio Technical Commission for Aeronautics (RTCA) **DO-254 standard**. This standard ensures the safety and reliability of airborne electronic hardware. [1]

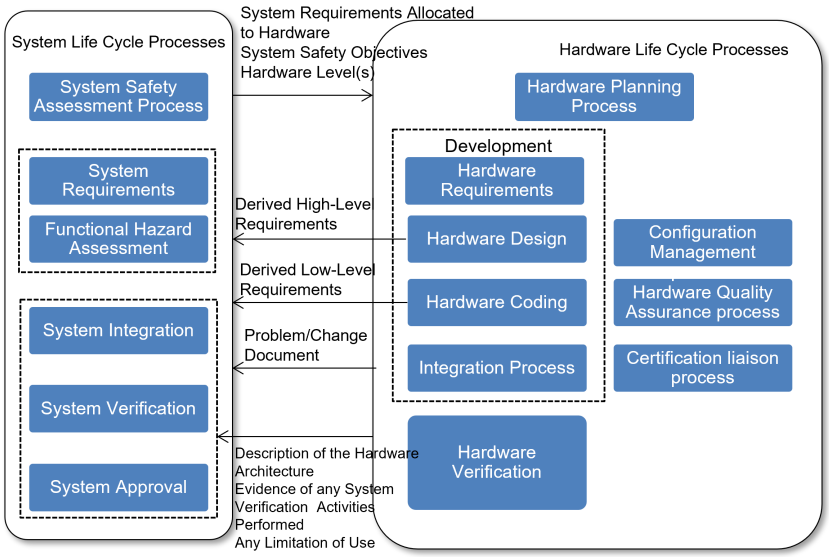

Figure 1.1: Design Assurance Guidance

Looking at Figure 1.1, **Design Assurance Guidance** includes:

- **Planning**: This phase plays a critical role in ensuring that the DO-254 certification process succeeds. Specifically, it involves the development of different planes, such as Plan for Hardware Aspects of Certification, HW Project Plan, HW Verification Plan, HW Configuration Management Plan and HW Quality Assurance Plan. [1]

- **Standards**: The main standards are HW Requirement Standards, HW Design Standards, HW Code Standards, HW Verification Standards, HW Documentation Standards. [1]

- **Development**: This phase consists of the development of the hardware. The hardware is designed according to requirements that have been previously defined. During the development process some high and low requirements can be derived. [1]

- **Verification and validation**: Hardware requirements are verified for compliance, traceability and accuracy at both high and low levels. Source code verification ensures that hardware source code is correct and conforms to standards. Verification activities are performed according to the hardware verification plan. Test coverage is achieved to verify the functionality and safety of the hardware design. [1]

- **Configuration**: The configuration management CM includes baseline management, problem reports, change reviews, traceability to ensure compliance and maintain quality throughout the Hardware Life Cycle Process. [1]

- **Quality**: All processes and activities related to hardware development adhere to standards and best practices to achieve the desired level of safety and reliability. [1]

Looking at Figure 1.2, DO-254 standard categorizes the compliance into five levels based on the potential impact of hardware failure on aircraft operations. Level A represents the highest level of severity, referred to as 'catastrophic', where failure could result in the loss of the aircraft. Conversely, a Level E hardware failure poses no safety risk to the aircraft. Achieving Level A compliance for complex electronic hardware requires significantly more rigorous verification and validation procedures than Level E compliance.[1]

Level	Failure Condition	Effect of Anomaly	Example
A	Catastrophic	Prevent Continued safe flight and landing	Fly-by-wire
B	Hazardous/Severe	Serious or potentially fatal injuries to a small number of occupants	Fuel management
C	Major	Discomfort to occupants, possibly including injuries	Pilot/ATC communication
D	Minor	Some inconvenience to occupants	Flight data recorder
E	Not relevant	No effect on aircraft operational capability or pilot workload	Entertainment system

Figure 1.2: Assurance Levels

1.2 Aim of the thesis

As previously described, avionics systems include complex electronic hardware such as Field Programmable Gate Arrays (FPGAs).
The rapid evolution of technology is a constant threat to the longevity of avionics projects. This challenge is particularly evident for Field Programmable Gate Arrays (FPGAs), which can quickly become obsolete.
Recognizing the importance of addressing this challenge, this thesis, conducted in collaboration with Leonardo Electronics and based on a real project using two specific FPGAs, aims to identify possible alternatives among those available on the market.For reasons of confidentiality, the project architecture has not been analyzed in detail in the chapters and is referred to as the "**reference architecture**".
In exploring potential FPGAs, key considerations include keeping the power footprint unchanged and performing a benchmark by porting the original source code to new potential candidate platforms. In addition, compliance with DO-254 standard is crucial. Therefore, the goal of this thesis is to propose a method for the timely replacement of potentially obsolete components with alternative technologies, in order to ensure the resilience and longevity of avionics systems.

1.3 Thesis outline

The thesis is composed of four main chapters organized as follows:

- **Chapter 1** introduces Field Programmable Gate Arrays (FPGAs) providing an overview of the current state of the art in this field.
- **Chapter 2** describes the methodology employed for identifying potential FPGA alternatives available on the market.

- **Chapter 3** collects a series of results on the suitability, performance and power consumption of the potential FPGA alternatives by implementing the reference architecture. It also provides an overview of the evaluation results, focusing on the advantages and disadvantages of the selected FPGAs in order to identify the best alternatives.
- **Chapter 4** provides a summary of the work described and an explanation of why the evolution of technology is not just a threat but can be an opportunity in this field.

Chapter 2

FPGA: An overview

2.1 Evolution of FPGA Architecture

Xilinx pioneered the field of field-programmable gate arrays (FPGAs) in 1984, although the term "FPGA" was not commonly used until Actel popularized it around 1988 [2]. An FPGA can be configured by the user to implement a digital circuit. Early FPGA architectures were different from those commonly used today. They consisted primarily of a grid array of programmable logic blocks and configurable interconnects. However, their functionality was mainly limited to basic programmable logic operations [3].
Over time, as applications became more complex and demanding, FPGA architectures evolved significantly. One notable development has been the integration of specialized hardware blocks directly onto the FPGA chip, in addition to the programmable logic blocks.
However, also the programmable logic type changed over time. In fact, programmable logic architectures (PLA) have been replaced by k-input look-up tables (LUT-k) to implement any Boolean Function, improving power consumption and timing.
Therefore, modern heterogeneous FPGA architectures include dedicated hardware blocks such as RAMs, DSPs and other hard IP blocks. [3]
RAM blocks have been integrated to provide dedicated memory resources enabling efficient implementation of data storage and buffering. DSP slices, optimized for arithmetic operations commonly used in signal processing applications [3]. In addition, various other hard IP blocks were introduced to address specific functions such as high-speed communications protocols.
In summary, the evolution of FPGA architecture can be represented by a significant shift from early architectures focused primarily on programmable logic blocks to modern heterogeneous architectures incorporating specialized hardware blocks

[3]. This evolution has been driven by both application demand for increased functionality and the opportunities presented by advances in process technology, resulting in more powerful and versatile FPGA devices [2].

2.2 Design flow

To implement the desired design in an FPGA, the design must first be described using a hardware description language such as VHDL or VERILOG. Then it is synthesized, mapped, and placed and routed using specialized design tool provided by the FPGA vendor. Once the design is mapped and placed-and-routed, the final step is to generate the configuration bitstream. This bitstream is a binary file used to configure an FPGA.
Finally, the bitstream can be stored in FLASH or RAM cells within the FPGA. In particular, flash-based FPGAs allow the configuration code to be retained even if the power supply is removed. RAM-based FPGAs, on the other hand, require the bitstream to be reloaded each time the FPGA is powered up.

2.3 Routing architectures

Programmable routing is a critical aspect of FPGA design as it accounts for over 50% of the area and timing of applications [3] . The efficiency of routing is critical as it affects the overall performance of the FPGA. The routing network in FPGAs consists of prefabricated wiring segments and programmable switches, allowing for flexible and configurable interconnections [3].
There are two main types of routing architecture commonly used in FPGAs: ***island-style interconnect architecture*** and ***hierarchical interconnect architecture*** [3]. In an **island-style interconnect architecture**, logic blocks are surrounded by a dense network of routing resources. Each LB is connected to its neighbouring LBs by a network of interconnect wires, typically arranged in a two-dimensional grid pattern. This layout allows signals to be routed horizontally and vertically to connect different LBs. Island interconnect architectures are characterized by their regularity and homogeneous distribution of routing resources, which simplifies routing algorithms [3].
Hierarchical interconnect architectures, on the other hand, organize routing resources into multiple layers or levels, with each layer responsible for connecting different levels of the logic hierarchy. This approach allows more efficient use of routing resources by grouping related signals together and providing dedicated routing paths for high-speed or critical signals. However, hierarchical interconnect architectures can introduce additional complexity into routing algorithms and may require more sophisticated routing algorithms to efficiently exploit the hierarchical

structure [3].
In summary, the main difference between island-style and hierarchical interconnect architectures is how routing resources are organized and distributed within the FPGA. Island-style architectures provide a regular and homogeneous distribution of routing resources, while hierarchical architectures organize routing resources into multiple layers or levels to efficiently connect different levels of the logic hierarchy and optimize the long critical paths [3].

2.4 Package options

Field Programmable Gate Arrays (FPGAs) are available in different package types. These packages facilitate electrical connections between the integrated circuit (IC) and the board while effectively dissipating the heat generated by the device [4]. For example:

1. **Quad Flat Packages (QFP)**: QFP packages are among the earliest forms of packages used for FPGAs. They have pins arranged along all four sides of the package, facilitating easy soldering onto a printed circuit board (PCB). QFP packages are suitable for applications where moderate pin counts and ease of assembly are required.

2. **Ball Grid Arrays (BGA)**: BGA packages feature a grid array of solder balls arranged on the underside of the package [4]. This arrangement allows higher pin densities, improved electrical performance due to reduced susceptibility to electromagnetic interference (EMI) and better heat dissipation compared to QFP packages [4]. BGAs are commonly used in modern high-density FPGAs and are suitable for applications demanding high pin counts and compact form factors [4].

3. **Fine Pitch Ball Grid Arrays (FBGA)**: FBGA packages are a variation of BGAs with smaller pitch between the solder balls.

4. **Chip-Scale Packages (CSP)**: CSPs are ultra-compact packages where the package size closely matches the dimensions of the silicon die. CSPs offer the smallest footprint and are suitable for applications requiring minimal space and low weight, such as portable devices and embedded systems.

Each of these FPGA package types offers several advantages and trade-offs in terms of cost, performance, thermal characteristics, and assembly complexity, allowing designers to select the most appropriate package for their specific application needs.

2.5 Part number

The part number of an FPGA identifies a unique model or variant of the FPGA manufactured by a specific vendor, such as Xilinx, Intel, Microchip or Lattice Semiconductor. The part number typically consists of:

1. **Manufacturer and Family:** The first few characters of the part number usually indicate the manufacturer and the family to which the FPGA belongs.
2. **Model:** The next part of the part number typically identifies the specific model of the FPGA within the family or series.
3. **Package Type:** Some part numbers include information about the package type of the FPGA, such as "FBGA" for a fine-pitch ball grid array. In the package code, lead-free products are distinguished from leaded products by a "G" after the package name and before the pin count. In particular, lead-free products are compliant with RoHS, the Reduction of Hazardous Substances Directive.
4. **Speed Grade:** FPGAs are often available in different speed grades to meet different performance requirements. The part number may indicate the speed grade of the FPGA.
5. **Temperature Range:** In some cases, the part number may also include a letter indicating the temperature range in which the FPGA can operate. For example, "C" indicates commercial temperature range, "I" industrial temperature range, "M" military temperature range and "A" automotive temperature range.

Understanding the part number of an FPGA is important in selecting the right component for a particular application.

2.6 Moore's law

According to Moore's law , the number of transistors in an integrated circuit (IC) doubles about every two years [2].
While process scaling has continued steadily for decades, the impact of Moore's Law on FPGA architecture has been less even. However, advances in technology process played a significant role in enabling the integration of more devices into the FPGA. This integration has resulted in increased functionality, performance and efficiency, making modern FPGAs suitable for a wide range of applications [2].
On the other hand, as transistor size decreases, static power consumption increases

due to Short Channel Effects (SCE) and dynamic power consumption increases due to increased interconnect complexity. In particular, global and intermediate interconnects don't scale with transistor size. These effects are increasingly evident as transistor channel length decreases further, creating a bottleneck in the evolution of the technology. Therefore, while advances in process technology have enabled greater integration and performance in FPGAs, managing power consumption remains a significant challenge [2].
This requires the use of efficient power management techniques such as dynamic voltage, frequency scaling, power gating, clock gating, and so on.

Chapter 3

Methodology for identifying FPGA alternatives

As previously described, this thesis is based on the real project involving two FPGAs and aims to identify FPGA alternatives to replace those initially employed, in order to address as soon as possible the threat of technology evolution to the longevity of the project. For reasons of confidentiality, the project architecture has not been analyzed in detail and is referred to as the "**reference architecture**". Specifically, this chapter aims to analyze the methodology used to identify potential FPGA alternatives available on the market to replace those currently in use.
Operative requirements are initially outlined, followed by a discussion of additional constraints that influence the selection of FPGA alternatives. Subsequently, an analysis of resource consumption in current FPGA implementations is provided, comparing the resource usage between SPARTAN-6 and CYCLONE III FPGAs. The purpose of this analysis is to provide a guideline to identify additional potential FPGAs accurately.

3.1 Operative requirements

The following operative requirements can be noted from the analysis of the defense application under consideration:

- The temperature range must be at least from $-40\,^{\circ}\mathrm{C}$ to $100\,^{\circ}\mathrm{C}$. The maximum ambient temperature of $70\,^{\circ}\mathrm{C}$ required in the technical specification it is a conservative worst case occurring only at ground before flight.
- Regarding the package, soldering of the component is performed using an alloy containing lead. Lead soldering process is necessary in order to grant the reliability performances of the avionic system. Leadless soldering process

induces many physical phenomena that lead to solder joint fragility or short circuits due to whiskers growth. These phenomena can drastically increase the failure rate of the solder joints. For the above reasons lead solder is still allowed for military product [5].

- Regarding dissipated power, it is known that an increase of temperature generates heat. An excessive heat can compromise the performance and lifetime of components, implying effective thermal management. For these reasons, the dissipated power must not exceed 1W under the worst temperature conditions, so when the system operates at 70 °C. In this case, the unit is mounted on a metallic plate providing a path for the heat flow.

These constraints allow to achieve high reliability, long life, safe operation and supportability of aviation electronics in operational environments.

3.2 Other system constraints

Any impact on the current board, where the actual FPGAs are implemented, must be minimized. In terms of the surrounding electronics, it is essential that the pin supply voltage is maintained at 3.3 V.
In addition, the reference architecture has two clock domains:

- **SystemClock** : 40 MHz;
- **PCIClock**: 33 MHz;

3.3 Resource evaluation for current FPGAs

The real project considered satisfies the dissimilarity constraint, which is sometimes necessary to ensure system robustness. For this reason, the project is implemented on two FPGAs from different vendors. Specifically, Xilinx Fpga XQ6SLX150-2FG484Q and Intel Fpga EP3C120F780I7 are the currently used FPGAs. Part number and resource usage reports for both FPGAs are analyzed to provide an order of magnitude of the resources required to implement the reference architecture.

Before proceeding, it is important to take into account key factors that distinguish one FPGA from another:

- Logic blocks
- On-chip memory

- DSP capabilities
- I/O compatibility

The unique characteristics of each FPGA influence significantly performance and resource utilization.

3.3.1 SPARTAN-6Q FAMILY: XQ6SLX150 FPGA

As the part number `XQ6SLX150-2FG484Q` indicates, this FPGA is a part of the Xilinx SPARTAN-6Q family. In particular, this part number consists of:

- `XQ6SLX150`: device type;
- `-2`: speed grade;
- `FG`: Fine-Pitch BGA Package;
- `484`: number of pins;
- `Q`: Expanded temperature range(T_j= −40 °C to 125 °C);

Looking at the table 3.1, which shows the main characteristics of the SPARTAN-6Q LX family, the last row describes the characteristics of the FPGA under consideration. In addition , since the package used is FG484, the occupied area is 23 mm x 23 mm.[6]

Device	Logic Cells	Configurable Logic Blocks (CLBs)			DSP48A1 Slices	Block RAM Blocks		CMTs	Memory Controller Blocks (Max)	Endpoint Blocks for PCI Express	Maximum GTP Transceivers	Total I/O Banks	Max User I/O
		Slices	Flip Flops	Max Distributed RAM (Kb)		18 Kb	Max (Kb)						
XQ6SLX75	74,637	11,662	93,296	692	132	172	3,096	6	2	0	0	4	328
XQ6SLX150	147,443	23,038	184,304	1,355	180	268	4,824	6	2	0	0	4	338
XQ6SLX75T	74,637	11,662	93,296	692	132	172	3,096	6	4	1	8	6	348
XQ6SLX150T	147,443	23,038	184,304	1,355	180	268	4,824	6	4	1	8	6	396

Figure 3.1: Spartan-6Q Device Family Features[6]

Regarding the family overview , it comprises both LX and LXT FPGA variants, with LX designed for optimized logic usage and LXT focusing on high-speed serial connectivity [6]. Overall, the family is engineered for low cost. It incorporates multiple efficient integrated blocks, an optimized selection of I/O standards and high-volume plastic wire-bonded packages [6].

The Spartan-6Q family is characterized by low static and dynamic power consumption, exploiting a 45 nm process optimized for cost and low power [6]. LX FPGAs offer a lower-power 1.0 V core voltage, while LX and LXT FPGAs in -2 and -3 speed grades offer high-performance 1.2 V core voltage [6].
The I/O interface is versatile, supporting multi-voltage, from 3.3V to 1.2V , multi-standard SelectIO interface banks [6].
The Spartan-6Q family includes efficient DSP48A1 slices for high-performance arithmetic and signal processing. They include a fast 18 x 18 multiplier, 48-bit accumulator and pre-adder to assist filter applications [6].
Logic resources are based on efficient 6-input LUTs to improve performance while increasing power. In some cases, the LUTs can be used as distributed RAM and as variable-length shift registers [6].
The family incorporates Block RAM with a wide range of granularity, including fast block RAM with byte write enable. Moreover, it allows 18 Kb blocks to be optionally programmed as two independent 9 Kb RAM blocks.[6]
For efficient clock management, the Spartan-6Q family incorporates Clock Management Tile (CMT) for enhanced performance, providing low noise, flexible clocking. Digital Clock Managers (DCMs) eliminate clock skew and duty cycle distortion, while Phase-Locked Loops (PLLs) ensure low-jitter clocking. [6]
Therefore, SPARTAN-6Q family allows efficiency, low cost and low power consumption. Nowadays, however, the technology used in this family is rather old. Therefore, SPARTAN 6 FPGA needs to be replaced.

Fitting result summary

The reference architecture was synthesized and implemented on XQ6SLX150-2FG484Q using PlanAhead. Both timing and placement constraints were used during the implementation process. Timing constraints in particular are important to ensure that the design meets the required performance. They specify requirements such as clock frequencies, maximum propagation delays and setup/hold times for data signals. At the same time, placement constraints are essential to meet specific I/O standards.
It is important to note that the results shown in the following tables are derived from the reports generated by the PlanAhead CAD flow. These results played a crucial role in evaluating the efficiency of the FPGA under consideration and the resources required to implement the reference architecture.
Focusing on slice utilization, the fitting results are shown in table 3.1. To understand these results, it is necessary to consider the Configurable Logic Blocks (CLBs). The CBLs are the main resources for implementing both sequential and combinatorial circuits [7]. Each CLB contains a pair of slices. Within each slice there are four look-up tables, each with 6 inputs, and eight storage elements. This is

the basic slice and is called SLICEX. In addition to the basic SLICEX, certain slices, known as SLICEL, contain wide multiplexers and an arithmetic carry structure. Another variant, known as SLICEM, extends the functionality by allowing the LUTs to be used as 64-bit distributed RAM and as variable-length shift registers with a maximum length of 32 bits. [7]
Regarding IO utilization, the results are reported in table 3.2.

Number of occupied Slices	15,359 out of 23,038	66%
Number of Slice Registers	34,650 out of 184,304	18%
Number of Slice LUTs:	40,315 out of 92,152	43%
Number used as logic	39,542 out of 92,152	42%
Number used as Memory	35 out of 21,680	1%
Number used exclusively as route-thrus	738	

Table 3.1: XQ6SLX150-2FG484Q: Slice Utilization

Number of bonded IOBs	211 out of 338	62%
Number of LOCed IOBs	211 out of 211	100%

Table 3.2: XQ6SLX150-2FG484Q:IO Utilization

The Spartan-6 FPGAs provide RAM blocks, each with a data storage capacity of up to 18K bits. In addition, each block can be configured in two ways: as two independent 9 Kb RAM blocks or as a single 18Kb RAM block[8]. Each RAM block is then accessible through two ports, although it can also operate as a single-port RAM. To improve pipeline performance, output registers are embedded in the Block RAM resources. These RAM blocks are organized in columns, and the total number of RAM blocks varies depending on the specific size of the Spartan-6 device.[8]
The RAM blocks in Spartan-6, as typically in Xilinx FPGAs, have both write and read operations synchronous [8]. The two ports are symmetrical and operate independently, sharing only the stored data [8]. Each port can be configured with a specific width, which is not dependent on the configuration of the other port. Initialization or clearing of the memory content can be achieved through the configuration bitstream. During a write operation, the memory can be set to maintain the existing data output, reflect the newly written data, or display the data being overwritten.[8]
Thus, block ram library primitives, RAMB16BWER and RAMB8BWER, must be considered in order to understand fitting results about RAM blocks utilization,

reported in Table 3.3 [8]. These are the basic bulding blocks for all block RAM configurations and are shown in Figure 3.2 and Figure 3.3 respectively.

Number of RAMB16BWERs	224 out of 268	83%
Number of RAMB8BWERs	32 out of 536	100%
Number of BUFPLLs	0 out of 8	0%
Number of BUFPLL_MCBs	0 out of 4	0%
Number of DSP48A1s	104 out of 180	57%

Table 3.3: XQ6SLX150-2FG484Q:Specific Feature Utilization

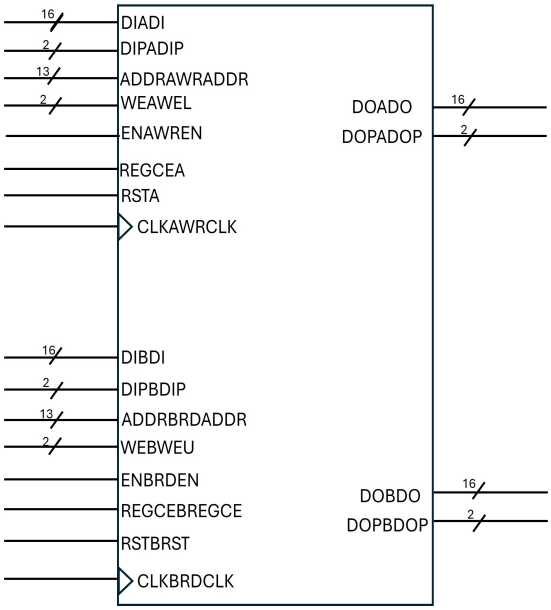

Figure 3.2: RAMB8BWER: The 9 Kb dual-port block RAM primitive [8]

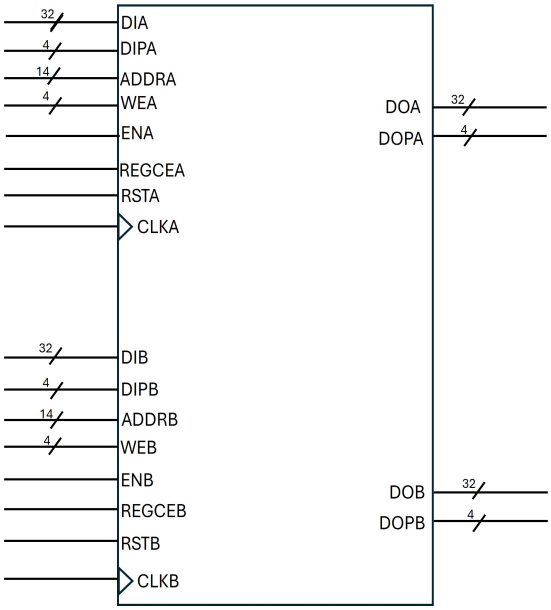

Figure 3.3: RAMB16BWER: The 18 Kb dual-port block RAM primitive [8]

Primitive	**Description**
RAMB8BWER	Supports data widths of x1, x2, x4, x8, x16, x32 (and x9, x18, x36 with parity bits)
RAMB16BWER	Supports data widths of x1, x2, x4, x8, x16, x32 (and x9, x18, x36 with parity bits)

Table 3.4: SPARTAN-6Q family: Block RAM Primitives [8]

The Table 3.3 also reports the number of DSP48A1s in use. Slice DSP48A1, in Figure 3.4, represents the digital signal processing (DSP) component within the Spartan-6q FPGAs.[9]
The reference architecture is implemented by using a lot of DSPs, as can be seen in Table 3.3. This happens when a digital design mainly involves multiplication with addition, so these functions are facilitated by dedicated circuits. Specifically, looking at Figure 3.4, the DSP48A1 slices provide support for a wide range of independent functions, including multiplication, multiplier-accumulator (MACC), pre-adder/subtracter followed by multiply-accumulator, multiplier followed by adder, wide bus multiplexer, magnitude comparator and wide counter [9]. This architecture further enables the interconnection of multiple DSP48A1 slices to create expansive mathematical functions, DSP filters, and complex arithmetic operations [9].

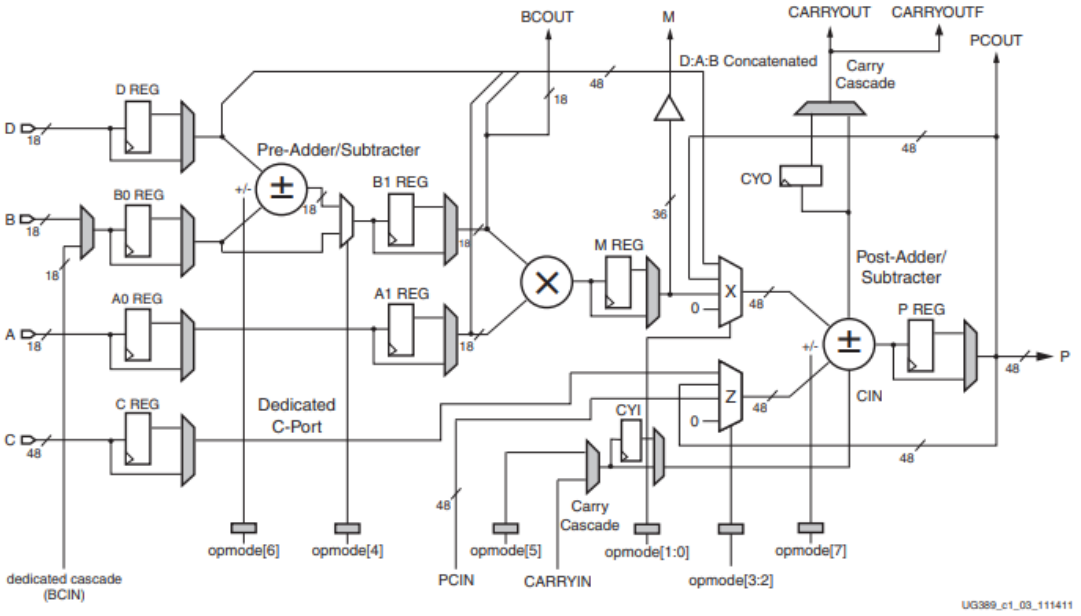

Figure 3.4: DSP48A1 Slice [9]

In reference to the absence of Phase-Locked Loops (PLLs) as indicated in Table 3.3, it shows how easy it is to port the source code of the reference architecture between different FPGAs. This is due to the complete independence of the source code from the specific IP blocks of each FPGA.

3.3.2 CYCLONE III FAMILY: EP3C120 FPGA

As the part number `EP3C120F780I7` indicates, this FPGA belongs to the CYCLONE III family. In particular, the part number `EP3C120F780I7` includes the following details:

- `EP3C`: Family signature, indicating that FPGA is part of CYCLONE III family.
- `120`: Logic elements, approximately 119,088 logic elements.
- `F`: Package type, specifically FineLine Ball-Grid Array (FBGA).
- `780`: Number of pins.
- `I`: Industrial temperature range ($T_j = -40°C$ to $100°C$).
- `7`: Speed grade, providing information about operating frequency and performance characteristics.

For completeness, the main features of the FPGAs in the CYCLONE III family are listed in table 3.5 and in table 3.6.

Family	Device	Logic Elements	Number of M9K Blocks	Total Ram Bits	18x18 Multipliers	PLLs	Global clock Networks	Maximum User I/Os
Cyclone III	EP3C5	5,136	46	423,936	23	2	10	182
	EP3C10	10,320	46	423,936	23	2	10	182
	EP3C16	15,408	56	516,096	56	4	20	346
	EP3C25	24,624	66	608,256	66	4	20	215
	EP3C40	39,600	126	1,161,216	126	4	20	535
	EP3C55	55,856	260	2,396,160	156	4	20	377
	EP3C80	81,264	305	2,810,880	244	4	20	429
	EP3C120	119,088	432	3,981,312	288	4	20	531

Figure 3.5: Cyclone III Device Family Features [10]

This family offers a wide range of logic density, memory, embedded multiplier and I/O options, as can be seen in the Figure 3.5.
As shown in Table 3.6, the package used by the EP3C120**F780**I7 fpga, the F780 package, implies a pitch of 1.0 mm and a nominal area of 841 mm^2.

Family	Package	Pitch (mm)	Nominal Area (mm^2)	Length x Width (mm x mm)	Height (mm)
Cyclone III	E144	0.5	484	22 x22	1.60
	M164	0.5	64	8 x 8	1.40
	P240	0.5	1197	36.64 x 34.64	4.10
	F256	1.0	289	17 x 17	1.55
	U256	0.8	196	14 x 14	2.20
	F324	1.0	361	19 x 19	2.20
	F484	1.0	529	23 x 23	2.60
	U484	0.8	361	19 x 19	2.20
	F780	1.0	841	29 x 29	2.20

Figure 3.6: Cyclone III Device Family Package Sizes [10]

As an overview of the Cyclone III family, it is manufactured using **TSMC's 65nm low-k dielectric process**, which enables low power consumption [10]. It also offers high functionality at low cost. In particular, the Cyclone III family typically operates at a core voltage of 1.2 V to balance performance and power efficiency [10].
In addition, this family provides a high memory-to-logic and multiplier-to-logic ratio, making it ideal for memory-intensive and compute-intensive tasks [10]. In scenarios where user I/O constraints are an issue, it addresses the problem with a high I/O count. The Cyclone III family uses TSMC's 2.5 V transistor technology in the I/O buffers, but despite this the devices are compatible and can be configured with 2.5 V, 3.0 V and 3.3 V configuration voltage standards. [10]
The device offers adjustable I/O slew rates, providing flexibility and helping to improve signal integrity within the system. It supports a wide range of I/O standards, including LVTTL, LVCMOS, SSTL, HSTL, PCI, PCI-X, LVPECL, bus LVDS (BLVDS), LVDS, mini-LVDS, RSDS, and PPDS, ensuring compatibility with various interface specifications.[10]
The inclusion of four phase-locked loops (PLLs) in each device ensures robust clock management and synthesis for multiple applications, including device clock management, external system clock management and I/O interfaces [10]. The dynamically reconfigurable PLLs allow phase shift, frequency multiplication or division and input frequency to be adjusted within the system without the need to reconfigure the device [10].
The device supports remote system upgrades without the need for an external controller, providing convenience and flexibility for system maintenance.[10]
Dedicated Cyclic Redundancy Code checking circuitry is integrated to detect Single

Event Upset (SEU) problems, improving system reliability.[10]
As a result, Cyclone III Fpgas have several key features that make them versatile and suitable for a wide range of applications. Nowadays, however, the technology used in this family is rather old. Therefore, CYCLONE III FPGA needs to be replaced.

Fitting result summary

The reference architecture was synthesized and implemented on EP3C120F780I7 by using Quartus II. During the process, both timing constraints and placement constraints were used. Specifically , timing constraints are needed to ensure that the design meets the required performance specifications. They specify requirements such as clock frequencies, maximum propagation delays, and setup/hold times for data signals. Simultaneously, the placement constraints are essential to meet specific I/O standards.
The Table 3.5 presents the main results derived from the reports generated by the Quartus II CAD flow. It is essential to focus on the fitter results in order to understand the performance and efficiency of an FPGA.

Family	Cyclone III
Device	EP3C120F780I7
Timing Models	Final
Total logic elements	65,676 / 119,088 (55%)
Total combinational functions	48,507 / 119,088 (41%)
Dedicated logic registers	36,946 / 119,088 (31%)
Total pins	211 / 430 (49%)
Total virtual pins	0
M9Ks memory block	293 / 432 (68%)
Embedded Multiplier 9-bit elements	208 / 576 (36%)
Total PLLs	0 / 4 (0%)

Table 3.5: EP3C120F780I7: Fitting Results Summary

Specifically, the overall performance of the FPGA is heavily dependent on the efficiency of the basic building block known as the Logic Element (LE), shown in Figure 3.7. [11]
Each logic element has four inputs and consists of a four-input look-up table (LUT),a carry chain connection, a register and output logic [10]. The four-input LUT is able to implement any Boolean function that involves four variables. In addition, the programmable register within the logic element can be configured as

a D, T, JK or SR flip-flop. This register has inputs for data, clock, clock enable and clear.[10]
In addition, each logic element has multiple outputs. Specifically, two outputs from the logic element are responsible for driving the column, row and direct link routing connections. At the same time, one output from the logic element drives the local interconnect resources.[10]
The configuration, shown in Figure 3.7, enables a concept known as register packing, where the register and LUT can be used for unrelated functions [10]. In practice, this means that the LUT can drive one output while the register drives another. The latter can be used to implement a shift register. This innovative feature improves device utilization by allowing the register and LUT to be used simultaneously for different and unrelated functions.[10]

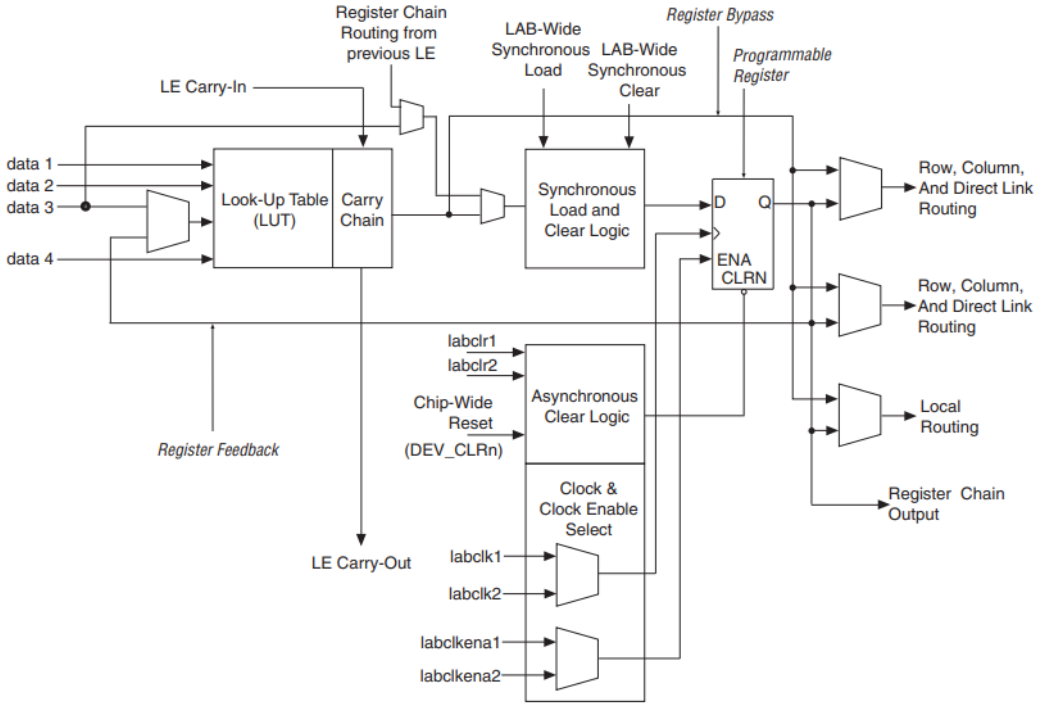

Figure 3.7: Logic Element [10]

The results of using I/O and PLL in the Cyclone III FPGA are the same as for the Spartan 6 FPGA because the implemented architecture is unchanged.
In addition, another result highlighted in Table 3.5 relates to memory blocks. Each M9K memory block, as specified, provides a capacity of 9,216 Kbits [10]. Notably, the maximum data width for each independent block is set to 18 bits. The

embedded memory structure consists of columns of M9K memory blocks that can be configured for different purposes. These can act as random access memory (RAM), first-in-first-out (FIFO) buffers or read-only memory (ROM). This flexibility allows memory usage to be optimized according to specific application requirements [10]. As outlined in Table 3.5, the CYCLONE III FPGA contains up to 576 embedded multipliers, each capable of performing 9 × 9 bit operations. These embedded multipliers are configurable, allowing them to be set up as either a single 18 × 18 bit multiplier or as two independent 9 × 9 bit multipliers. [10] Specifically, each embedded multiplier includes input/output registers and a multiplier stage. Utilizing embedded multipliers from the Cyclone III device family enables the implementation of multiplier adder and multiplier accumulator functions. In these functions, the multiplier part is executed using embedded multipliers, while the adder or accumulator function is carried out in logic elements (LEs). [10]

3.4 Resource Consumption: SPARTAN-6 vs. CYCLONE III FPGAs

A comparative architecture analysis between SPARTAN-6 and CYCLONE III FPGAs aims to understand the order of magnitude of the main resources required to implement the reference architecture, including LUTs, registers, DSP and memory blocks. The most significant difference is the number of inputs for a LUT within the basic logic block. As shown in the previous sections, the SPARTAN-6 FPGA incorporates LUT-6 in the basic logic block, while the CYCLONE III FPGA incorporates LUT-4.
An n-inputs lookup table (LUT) can implement any Boolean function that involves n inputs. In particular, by providing n-inputs to the LUT, a corresponding output value is determined based on the inputs according to the truth table associated with the Boolean function being implemented.
It has been demonstrated that using LUT-4 is advantageous for maximizing efficiency in terms of area with simple functions [11]. However, when dealing with functions with a high number of inputs, employing LUT-4 results in an increase in the number of logic levels compared to LUT-6 [11]. Consequently, performance is compromised as the delay of the critical path increases. To address this issue, LUT-6 is needed to reduce delay and improve system throughput by up to 25%[12]. On the other hand, if the functions are simple, characterized by a number of inputs less than or equal to 4, LUT-6 is underutilized, resulting in inefficiency in terms of area [11].

FPGA	CYCLONE III	SPARTAN-6
TOTAL COMBINATIONAL FUNCTIONS	**LUT-4** 48507/119088	**LUT-6** 40315/92152
REGISTERS	36946/119088	34650/184304
DSP BLOCKS	**9-BIT ELEMENTS** 208/576	**18-BIT ELEMENTS** 104/180
PINS	211/430	211/338
TOTAL MEMORY BITS	1,051,145	1,894,000

Table 3.6: SPARTAN-6 versus CYCLONE III fitting results

The Table 3.6 highlights a comparison between two types of FPGA, the CYCLONE III and the SPARTAN-6, in terms of resource consumption. It is evident that more LUT-4 are required compared to LUT-6, with a ratio of 1.2, as expected for the reasons mentioned before. The SPARTAN-6 also uses fewer registers than the CYCLONE III. However, the SPARTAN-6 needs more memory. The memory is made up of memory blocks and distributed RAM. The memory blocks of the two FPGAs have similar capacities: 9 kbit for the CYCLONE III and 9 kbit or 18 kbit for the SPARTAN-6, so the results are comparable. The differences in the results can therefore be attributed to the design tool used for the implementation process, which may affect the results slightly differently. In addition, the CYCLONE III requires twice as many DSP blocks as the SPARTAN-6, because the CYCLONE III's DSPs handle numbers represented with a maximum of 9 bits, while the SPARTAN-6's DSPs handle numbers represented with up to 18 bits. Finally, as shown in the Table 3.6, the number of pins required is the same for both FPGAs because the architecture implemented does not change.

3.5 FPGA market exploration: resource analysis and constraints as a guideline

Once the requirements in terms of resources, performance, power consumption and package are known, the research for other potential FPGAs that meet these constraints can begin. Major vendors such as XILINX, INTEL, MICROCHIP and LATTICE were considered.
Each manufacturer offers families of FPGAs that differ in application, logic density, technology process, performance, DSP capabilities, and so forth. The aim of this chapter is to identify potential compatible FPGAs in terms of resources, temperature range, package and pin supply voltage. The next chapter analyzes

the power consumption and performance of the selected FPGAs in relation to the current ones.

3.5.1 MICROCHIP

The first vendor to be considered is Microchip. It is one of the main suppliers of FPGAs and offers a range of FPGAs specifically designed for **defense applications**. These FPGAs are designed to ensure the lifetime and reliability required for military applications. This means they meet stringent requirements for operating temperature (-55°C to 125°C) and package type (Pb) [13].
Microchip offer several FPGA families with different fabric resources and **FLASH-based** architectures, as shown in Figure 3.8. According to the resource analysis in section 3.4, 104 DSPs (18x18 multipliers) are required to implement the reference architecture. Among the families listed in the Figure 3.8, SmartFusion, ProASIC3 and Igloo do not include math blocks. As a result, these families are not a suitable option. Microchip offers the Igloo2 and PolarFire families with math blocks optimized for digital signal processing (DSP) applications. Each math block includes a multiplier and adder supporting 18x18 bit operations. [14] [15] Additionally, the PolarFire family includes a pre-adder within the math block architecture.[15] So, the criterion is met by the SmartFusion2, Igloo2 and PolarFire families. These families also fulfil the RAM memory requirement of 2 MB in the worst case, as discussed in section 3.4. These families also incorporate LUT-4 in their basic logic block, similar to INTEL CYCLONE III family. [14] [15] Therefore, the resource consumption of the CYCLONE III FPGA serves as a benchmark for evaluating potential Microchip FPGA families.
As can be seen in the Figure 3.8, FPGA families also differ in the amount of logic elements LEs. Each LE consists of a 4-input look-up table (LUT) with a carry chain and a flip-flop.[14] [15] In the case of the CYCLONE III FPGA, the resource usage analysis indicates that at least 65,676 LEs are required.Consequently, an FPGA candidate must have at least 100,000 LEs, as different design tools used to implement the architecture use different algorithms.

MICROCHIP: PolarFire family

The PolarFire family is designed to reduce costs by providing designers with a mid-range selection of FPGAs [13]. These FPGAs are equipped with DSP resources and logic elements (LEs) ranging from 1K to 500K, making them well suited for a range of high-speed and compute-intensive tasks. They also offer low power consumption and compact form factors to meet stringent design constraints [13].

Features	SmartFusion ProASIC3, IGLOO	SmartFusion 2 IGLOO 2	POLARFIRE
Logic elements	100-30K	5K-150K	25K-480K
Transceiver Rate	-	1-5 Gps	250 Mbps – 12.7 Gbps
I/O Speed	400 Mbps LVDS	667 Mbps DDR3 750 Mbps LVDS	1480
DSP (18X18 Multipliers)	-	240	1480
Max RAM	144 Kb	5 Mb	33 Mb
Processor Option	Hard 100 MHz ARM Cortex-M3	Hard 166 MHz Arm Cortex-M3 Soft RISC-V	Soft RISC-V Hard Crypto Processor
On-Board Flash	Up to 512 KB code store	Up To 512 KB code store	128 KB Code Storage 56 KB secure NVM
Family Type	CPLD Replacements Smallest Packages	Low Density FPGAs with more resources and low power	Mid-Range Density FPGAs Lowest Power, Cost Optimized

Figure 3.8: Microchip: FPGA product table for defense application [13]

The selection of FPGA devices involves a careful evaluation of available resources, package specifications and compliance requirements. In the context of the PolarFire family shown in Figure 3.9 and the corresponding package options shown in Figure 3.10, the constraints outlined in Sections 3.1, 3.2 and 3.4 serve as guide for identifying potential FPGA candidates suitable for implementing the reference architecture.
In terms of available resources such as logic elements (LE), digital signal processors (DSP) and memory, the MPF050 FPGA and MPF100 FPGA are below the resource required limit and are therefore excluded from consideration.
In terms of package requirements, for defense applications it is imperative that the ball composition is lead. However, when selecting the appropriate package, it is essential to ensure that the number of general purpose I/Os (GPIOs) exceeds 211, as specified in section 3.4. Typically, I/Os are divided into High Speed I/O (HSIO) and General Purpose I/O (GPIO), with the former supporting a maximum voltage of 1.8 V and the latter 3.3 V.[16]
Figure 3.10 shows that only FC784 and FC1152 packages for MPF300 and MPF500 FPGAs for defense applications offer packages with more than 211 GPIOs.
However, in order to maintain the current package dimensions of the FPGAs used (29x29 mm and 23x23 mm), the FC1152 package is not considered. The MPF300 and MPF500 FPGAs meet all the requirements, but could be inefficient due to their excessive resources. As there are no compatible packages with appropriate count I/O for the lower logic density MPF200 FPGA for defense applications, automotive

Features		PolarFire FPGA				
		MPF050	**MPF100**	**MPF200**	**MPF300**	**MPF500**
FPGA Fabric	Logic elements (4LUT +DFF)	48K	109K	192K	300K	481K
	Math Blocks (18x18 MACC)	150	336	588	924	1480
	LSRAM Blocks (20Kb)	160	352	616	952	1520
	µSRAM (64x12)	450	1008	1764	2772	4440
	TOTAL RAM (Mb)	3.6	7.6	13.3	20.6	33
	µPROM (Kb)	216	297	297	459	513
	USER DLLs/PLLs	8	8	8	8	8
High-Speed I/O	250 Mbps-12.7Gbps Transceiver Lanes	4	8	16	16	24
	PCI Gen 2 Endpoints/Root Ports	2	2	2	2	2
Total I/O	Total User I/O	176	296	364	512	584

Figure 3.9: PolarFire product table [13]

application packages are considered.

Automotive applications require RoHS compliant packages with lead-free balls and a temperature range of -40°C to 125°C. As shown in Figure 3.10, the largest package for the MPF200 FPGA is FC(V)G, which offers a GPIO count lower than 211.

As a result, while the MPF200 FPGA optimizes resource utilization, it does not meet all requirements. To address the RoHS compliance issue, it is possible to replace the balls with leaded balls through a process known as reballing. In addition, level shifters can be used to adjust pin voltages, but at an increased cost. When selecting an FPGA, it is therefore essential to carefully weigh efficiency against additional cost. However, the MPF300 and MPF200 FPGAs were chosen as a compromise.

Thus, the possible possible candidate part numbers are:

Features	MPF050	MPF100	MPF200	MPF300	MPF500
Extended Commercial and Industrial	**Total User I/O (HSIO/GPIO) GPIO CDRs/XCVRs**				
FCSG325 (11X11, 11X14.5 0.5 mm)	164 (84/80) 6/4	170 (84/86) 8/4	170 (84/86) 8/4		
FCSG536 (16x16, 0.5 mm)			300 (120/180) 15/4	300 (120/180) 15/4	
FCVG484 (19x19, 0.8 mm)	176 (96/92) 7/4	284 (120/164) 14/4	284 (120/164) 14/4	284 (120/164) 14/4	
FCG484 (23x23, 1.0 mm)		244 (96/148) 13/8	244 (96/148) 13/8	244 (96/148) 13/8	
FCG784 (29x29, 1.0 mm)			364 (132/232) 20/16	388 (156/232) 20/16	388 (156/232) 20/16
FCG1152 (35x35, 1.0 mm)				512 (276/236) 24/16	584 (324/260) 24/24
Military 'S' devices only	**Total User I/O (HSIO/GPIO) GPIO CDRs/XCVRs**				
FCS325 (11X11, 11X14.5 0.5 mm)			170 (84/86) 8/4		
FCS536 (16x16,0.5 mm)				300 (120/180) 15/4	
FCV484 (19x19,0.8 mm)				284 (120/164) 14/4	
FC484 (23x23,1.0 mm)				244 (96/148) 13/8	
FC784 (29x29,1.0 mm)				388 (156/232) 20/16	388 (156/232) 20/16
FC1152 (35x35, 1.0 mm)				512 (276/236) 24/16	584 (324/260) 24/24
Automotive 'T2'	**Total User I/O (HSIO/GPIO) GPIO CDRs/XCVRs**				
FCSG325 (11X11, 11X14.5 0.5 mm)	164 (84/80) 6/4	170 (84/86) 8/4	170 (84/86) 8/4		
FCSG536 (16x16, 0.5 mm)			300 (120/180) 15/4	300 (120/180) 15/4	
FCVG484 (19x19, 0.8 mm)	176 (96/92) 7/4	284 (120/164) 14/4	284 (120/164) 14/4	284 (120/164) 14/4	
FCG484 (23x23, 1.0 mm)		244 (96/148) 13/8	244 (96/148) 13/8	244 (96/148) 13/8	
FCG784 (29x29, 1.0 mm)				388 (156/232) 20/16	

Figure 3.10: PolarFire packaging [13]

- **MPF300TS-FC784M**
- **MPF200T-1FC(V)G484T2**

MICROCHIP: Igloo2 family

IGLOO2 FPGAs provide a flexible solution for a wide range of applications[13]. In particular, the selection of appropriate FPGAs from those listed in Figure 3.11, to implement the reference architecture, is based on an analysis of available resources, package specifications and compliance requirements. Figure 3.12 shows the package alternatives for the Igloo2 family for defense applications.
In terms of fabric resources such as logic elements (LE), digital signal processors

(DSP) and memory, only the M2GL150 FPGA provides the necessary resources compared to Cyclone III FPGA currently in use. Additionally, meeting package and I/O requirements is crucial, as in the previous case. The M2GL150 FPGA is available in both the FC(G)536 and FC(G)1152 packages, but only the latter offers a number of I/Os that support 3.3 V higher than 211.
Therefore, the potential candidate part number is:**M2GL150(T/TS)-1FC1152M**.

Peripherals	Features	M2GL005 (S)	M2GL010 (S/T/TS)	M2GL025 (T/TS)	M2GL050 (T/TS)	M2GL060 (T/TS)	M2GL090 (T/TS)	M2GL150 (T/TS)
Logic/DSP	Maximum Logic Elements (4LUT+DFF)	6,060	12,084	27,696	56,340	56,520	86,184	146,124
	Math Blocks (18x18)	11	22	34	72	72	84	240
	PLLs and CCCs	2	2	6	6	6	6	8
	SPI/HPDMA/PDMA	1 each	1 each	1 each	1 each	1 each	1 each	1 each
	Fabric Interface Controllers	1	1	1	2	1	1	2
	Data Security	AES256, SHA256, and RNG	AES256, SHA256, and RNG	AES256, SHA256, and RNG	AES256, SHA256, and RNG	AES256, SHA256, RNG, ECC, and PUF	AES256, SHA256, RNG, ECC, and PUF	AES25, SHA256, RNG, ECC, and PUF
Memory	eNVM (K Bytes)	128	256	256	256	256	512	512
	LSRAM 18K Blocks	10	21	31	69	69	109	236
	µSRAM 1K Blocks	11	22	34	72	72	112	240
	eSRAM (K Bytes)	64	64	64	64	64	64	64
	Total Ram (K)	703	912	1104	1826	1826	2586	5000
High Speed	DDR Controllers	1 x 18	1 x 18	1 x 18	2 x 36	1 x 18	1 x 18	2 x 36
	SerDes Lanes (T)	0	4	4	8	4	4	16
	PCIe End Points	0	1	1	2	2	2	4
User I/Os	MSIO (3.3 V)	115	123	157	139	271	309	292
	MSIOD (2.5 V)	28	40	40	62	40	40	106
	DDRIO (2.5 V)	66	70	70	176	76	76	176
	Total User I/O	209	233	267	377	387	425	574
Grades	Commercial (C), Industrial (I), Military (M), and Automotive (T1/T2)	C, I, T1 and T2	C, I, M, T1 and T2	C, I, M, T1 and T2	C, I, M, T1 and T2	C, I, M, T1 and T2	C, I, M, T1 and T2	C, I and M

Figure 3.11: Igloo2 product table [13]

Package	Devices	MSIO (3.3 V max)	MSIOD (2.5 V max)	DDRIO (2.5 V max)	Total User I/O
FG(G)484	M2GL005 (S)	115	28	66	209
	M2GL010 (S/T/TS)	123	40	70	233
	M2GL025 (T/TS)	157	40	70	267
	M2GL050 (T/TS)	105	40	122	267
	M2GL060 (T/TS)	157	40	70	267
	M2GL090 (T/TS)	157	40	70	267
FC(G)536	M2GL150 (T/S)	151	16	126	293
FC(G)676	M2GL060 (T/S)	271	40	76	387
	M2GL090 (T/S)	309	40	76	425
FG(G)896	M2GL050 (T/S)	139	62	176	377
FC(G)1152	M2GL150 (T/S)	292	106	176	574

Figure 3.12: Igloo2 packaging [13]

3.5.2 INTEL

The second FPGA vendor to be considered is Intel. Its portfolio consists of 5 families of FPGAs: Agilex family, Stratix family, Arria family, Cyclone family and MAX family. They differ in terms of application, available resources and technology process [17]. Among these families, the INTEL CYCLONE 10 family was considered the best in terms of available resources, packaging options and temperature range for the reference architecture to implement. It represents a subsequent iteration to the Cyclone III family. Consequently, the resource utilization data of the Cyclone III FPGA, reported in section 3.4, was used to evaluate potential Cyclone 10 FPGAs.
However, other suitable FPGAs from other families, such as ARRIA 5 family, were not considered. They are either obsolete or comparable to current FPGAs.

INTEL: CYCLONE 10 LP FAMILY

The Intel Cyclone 10 LP devices shown in the Figure 3.13 offer low static power and cost-optimized features.[17]
In terms of resources such as logic elements (LE), digital signal processors (DSP) and memory, only the 10CL120 FPGA provides the required resources compared to Cyclone III FPGA currently in use. As in the previous cases, the package and I/O requirements are crucial. The 10CL120 FPGA is available in both F484 and F780 packages, both of which provide more than 211 GPIOs, as shown in Figure 3.14. The former was chosen for the analysis, but the latter is also suitable. However, this FPGA does not support the military temperature range. The maximum available

temperature range is the extended industrial range, which spans from -40°C to 125°C.[18] In addition, the available packages are RoHS compliant[18]. Therefore, a reballing process is required to replace the balls with leaded balls. Thus, the potential candidate part number is **10CL120YF484I7G**.

Resource		Device							
		10CL006	10CL010	10CL016	10CL025	10CL040	10CL055	10CL080	10CL0120
Logic Elements (LE)		6,272	10,320	15,408	24,624	39,600	55,856	81,264	119,088
M9K Memory	Block	30	46	56	66	126	260	305	432
	Capacity (Kb)	270	414	504	594	1,134	2,234	2,745	3,888
18 x 18 Multiplier		15	23	56	66	126	156	244	288
PLL		2	2	4	4	4	4	4	4
Clock		20	20	20	20	20	20	20	20
Maximum I/O		176	176	340	150	325	321	423	525
Maximum LVDS		65	65	137	52	124	132	178	230

Figure 3.13: CYCLONE 10 LP product table [18]

Device	Package												
	Type	M164 164- pin MBGA		U256 256- pin UBGA		U484 484- pin UBGA		E144 144- pin EQFP		F484 484- pin FBGA		F780 780- pin FBGA	
	Size	8 mm x 8 mm		14 mm x 14 mm		19 mm x 19 mm		22 mm x 22 mm		23 mm x 23 mm		29 mm x 29 mm	
	Ball Pitch	0.5 mm		0.8 mm		0.8 mm		0.5 mm		1.0 mm		1.0 mm	
	I/O Type	GPIO	LVDS	GPIO	LVDS	GPIO	LVDS	GPIO	LVDS	GPIO	LVDS	GPIO	LVDS
10CL006				176	65			88	22				
10CL010		101	26	176	65			88	22				
10CL016		87	22	162	53	340	137	78	19	340	137		
10CL025				150	52			76	18				
10CL040						325	124			325	124		
10CL055						321	132			321	132		
10CL080						289	110			289	110	423	178
10CL120										277	103	525	230

Figure 3.14: CYCLONE 10 LP packaging [18]

3.5.3 XILINX

The third FPGA vendor to be considered is Xilinx. It offers its defense-grade XQ architecture portfolio, which includes families of FPGAs with leaded packages that can support military temperature range, from -55°C to 125°C [19].

These FPGAs ensure long-term availability and incorporate anti-tamper technology[19]. FPGA families that meet these stringent requirements are [19]:

- XQ KINTEX ULTRASCALE+;
- XQ VIRTEX ULTRASCALE+;
- XQ VIRTEX 7;
- XQ KINTEX 7;
- XQ ARTIX 7;

The first two variants are manufactured in 16nm FinFET technology, while subsequent variants are manufactured in 28nm technology [20]. In particular, the Virtex 7 and Kintex 7 have abundant resources in logic cells, DSP and memory blocks, making them oversized for the reference architecture [19]. On the other hand, the Artix 7 fulfils the requirements for both available resources and I/Os that support 3.3 V, so a thorough analysis is required to select the most suitable FPGAs to implement the reference architecture.[19]

XILINX: ARTIX-7Q FAMILY

The ARTIX-7Q family has been strategically designed to offer the lowest cost and lowest power consumption in a compact form factor for high volume applications [21] . Like the current SPARTAN-6Q FPGA in use, the logic resources are based on efficient 6-input LUTs [21]. In some cases, the LUTs can be used as distributed RAM and variable-length shift registers. The family also includes Ram Blocks and DSP48E1 Slices [21].
Several notable features of the Block RAM are:

- 36 Kb dual-port Block RAM that supports port widths of up to 72;
- Programmable FIFO logic;
- Optional integrated error correction circuitry;

Finally, each DSP slice contains a pre-adder, a 25x18 multiplier, an adder and an accumulator. [21]
The architecture of the ARTIX-7Q FAMILY is therefore very similar to that of the SPARTAN-6Q FAMILY. Consequently, the resource consumption data of the SPARTAN-6Q FPGA, reported in section 3.4, was used to evaluate potential ARTIX-7Q FPGAs, which are listed in Figure 3.15 .

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices	Block RAM Blocks			CMTs	PCIe	GTPs	Analog Mixed Signal (AMS)	Total I/O Banks	Max User I/O
		Slices	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)						
XQ7A50T	52,160	8,150	600	120	150	75	2,700	5	1	4	1	5	250
XQ7A100T	101,440	15,850	1,188	240	270	135	4,860	6	1	4	1	6	285
XQ7A200T	215,360	33,650	2,888	740	730	365	13,140	10	1	8	1	8	400

Figure 3.15: ARTIX 7 product table [21]

Package	CS324		CS325		RS484		FG484		RB484		RB676	
Size (mm)	15 x 15		15 x 15		19 x 19		23 x 23		23 x 23		27 x 27	
Ball Pitch (mm)	0.8		0.8		0.8		1.0		1.0		1.0	
Device	GTP	I/O HR (3.3 V max)	GTP	I/O HR (3.3 V max)	GTP	I/O HR (3.3 V max)	GTP	I/O HR (3.3 V max)	GTP	I/O HR (3.3 V max)	GTP	I/O HR (3.3 V max)
XQ7A50T			4	150			4	250				
XQ7A100T	0	210					4	285				
XQ7A200T					4	285			4	285	8	400

Figure 3.16: ARTIX 7 packaging [21]

It is important to note that Xilinx guarantees an extended life cycle for the ARTIX 7 FAMILY until at least 2035.[20]
In terms of resources such as logic elements (LE), digital signal processors (DSP) and memory, the XQ7A100T FPGA and XQ7A200T FPGA provide the required resources compared to SPARTAN-6 FPGA currently in use. In addition, as in the previous case, the package and I/O requirements must be met. For the FPGAs selected, only the FG484 and RB484 packages offer a HR I/O count higher than 211, as shown in Figure 3.16. Therefore, the potential candidate part numbers are: **XQ7A100T-1FG484M** and **XQ7A200T-1RB484M** .

3.5.4 LATTICE

Lattice is the last vendor to be considered. It offers a portfolio of military-grade architectures designed to meet the stringent requirements of mission-critical systems. These FPGA families differ in the technological node , the resources available such as LUTs, DSPs and memory blocks, and the types of packages offered.

However, the latest FPGAs, like CROSSLINK-NX , do not offer sufficient resources compared to those currently in use. As a result, it is necessary to look beyond optimized military FPGAs. Among the alternatives, the FPGA families

based on 28nm FD-SOI technology stand out for their low power consumption and high reliability: the MACHXO5 family and the CERTUSPRO-NX family.

However, these families have RoHS-compliant packages and a number of I/Os that support a voltage of 3.3 V lower than 211. So, it is necessary to reball the packages in order to adapt them to military applications where the system is subjected to high mechanical and thermal stresses. In addition, it is necessary to use level shifters that are designed to adapt the voltage to the one that is required on the respective pins.

LATTICE: MachXO5-NX FAMILY

The MachXO5-NX family is designed primarily for commercial and industrial applications. This FPGA family offers devices with up to 96,000 logic cells, 156 18x18 multipliers and 7.3 megabits (Mb) of embedded memory including EBR and LRAM blocks [22].
The MachXO5-NX FPGA offers robust security features such as bitstream encryption, authentication mechanisms and password protection to ensure the integrity of user designs.[22]
Each logic cell in the MachXO5-NX family corresponds to a LUT-4x1.2[22]. For this reason, the resource consumption data for the CYCLONE III FPGA reported in Section 3.4 is used to select potential FPGAs for the MachXO5-NX family.
As shown in Figure 3.17, only the LFMX05-100T device meets all the resource requirements, including memory, logic cells and DSP resources. However, it is only available in a 400BBG package configuration, which offers a lower GPIO count than the required 211 and is RoHS compliant. This requires reballing and the integration of level shifters. Finally, the industrial temperature range (-40°C to 100°C) is the maximum available range within which these FPGAs can operate.
So the potential candidate part number is **LFMX05-100T-7BBG400I**.

LATTICE: CERTUSPRO-NX FAMILY

The CERTUSPRO-NX FPGA family can be used in a wide range of applications. This family offers FPGAs for commercial, industrial and automotive temperature grades[23]. In particular, these FPGAs can provide up to 100,000 logic cells, 156 multipliers (18×18) for efficient digital signal processing [23].This family also offers FPGAs with up to 7.3 megabits (Mb) of embedded memory, including both EBR and LRAM blocks [23]. Finally, the package options are RoHS compliant and offer both high performance I/Os and wide range I/Os, ensuring compatibility and flexibility for various applications [23].
In the CERTUSPRO-NX family, each logic cell corresponds to a LUT-4x1.2 [23]. For this reason, the resource consumption data for the CYCLONE III FPGA, as described in Section 3.4, is used to identify potential FPGAs for this family.

Device	LFMX05-25	LFMX05-55T	LFMX05-100T
Logic Cells	27k	53k	96k
Embedded Memory (EBR) Blocks (18 Kb)	80	166	208
Embedded Memory (EBR) Bits (kb)	1,440	2,998	3,774
Distributed RAM Bits (kb)	184	320	639
Large Memory (LRAM) Blocks	1	5	7
Large Memory (LRAM) Bits (kb)	512	2,560	3,584
18 x 18 Multipliers	20	146	156
ADC Blocks	2	2	2
450 MHz High Frequency Oscillator	1	1	1
128 kHz Low Power Oscillator	1	1	1
GPLL	2	4	4
PCIe Gen2 hard IP	0	1	1
SerDes (Quad/Channels)	0	1/2	1/2
Bitstream Authentication	ECDSA-256	ECDSA-256	ECDSA-256
UFM (kb)	15,360	79,872	79,872
EMIF	DDR3, DDR3L	DDR3, DDR3L, LPDDR4	DDR3, DDR3L, LPDDR4
Packages (Size, Ball Pitch)	SerDes Channels/Ios (Wide Range (WR) GPIOs (Top/Left/Right Banks) + High Performance (HP) GPIOs (Bottom Banks) +ADC dedicated inputs)		
256 BBG (14 mmx14 mm, 0.8 mm)	0/205 (159+40+6)		
400 BBG (17 mm x 17 mm, 0.8 mm)	0/305 (251+48+6)	2/297 (159+132+6)	2/297 (159+132+6)

Figure 3.17: MachXO5-NX product family [22]

As shown in Figure 3.18, only the LFCPNX-100 device meets all resource requirements, including memory, logic cells and DSP resources. It is available in several package configurations that offer a lower GPIO count than the required 211. However, the BBG484 package was chosen because it offers both the maximum available temperature range and the highest number of wide range I/Os. As previously anticipated, the packages are RoHS compliant, so reballing process is mandatory. The integration of level shifters is required to adapt the voltage to that of the high performance pins.
Finally, the automotive temperature range, from -40°C to 125°C, is the maximum available range within which these FPGAs operate.
Thus, the potential candidate part number is **LFCPNX-100-7BBG484A** .

Device	LFCPNX-50	LFCPNX-100
Logic Cells	52k	96k
Embedded Memory (EBR) Blocks (18 Kb)	96	208
Embedded Memory (EBR) Bits (kb)	1,728	3,774
Distributed RAM Bits (kb)	344	639
Large Memory (LRAM) Blocks (512 kb)	4	7
Large Memory (LRAM) Bits (kb)	2,048	3,584
18 x 18 Multipliers	96	156
ADC Blocks	2	2
450 MHz High Frequency Oscillator	1	1
32 kHz Low Power Oscillator	1	1
GPLL	3	4
PCIe Gen3 hard IP	1	1
SerDes (Quad/Channels)	1/4	2/8 or 1/4
Packages (Size, Ball Pitch)	Total I/O (Wide Range, High Performance, ADC)/SERDES Lanes	
ASG256 (9 mmx 9 mm, 0.5 mm)	165 (75,84,6) /4	165 (75,84,6) /4
CBG256 (14 mm x 14 mm, 0.8 mm)	165 (75,84,6) /4	165 (75,84,6) /4
BBG484 (19 mmx 19 mm, 0.8 mm)	269 (167,96,6) / 4	305 (167,132,6) / 8
BFG484 (23 mmx 23 mm, 1 mm)	269 (167,96,6) / 4	305 (167,132,6) / 4
LFG672 (27 mmx 27 mm, 1 mm)		305 (167,132,6) / 8

Figure 3.18: CERTUSPRO-NX product family [23]

Chapter 4

FPGA candidates: a comparative analysis

This chapter discusses the results of implementing the reference architecture on the previously selected FPGAs in terms of power consumption and performance. Finally, the FPGAs currently in use serve as an evaluation baseline to select the best candidates FPGAs.

4.1 FPGA design flow

Each vendor provides its own design tool to implement the reference architecture on a specific FPGA:

- **MICROCHIP**: LIBERO 2021.3
- **XILINX**: VIVADO 2019.1
- **INTEL**: QUARTUS 18.0
- **LATTICE**: RADIANT 2023.1

However, these tools are based on a common flow that is shown in the Figure 4.1 [24]. In fact, each design tool consists of a sequence of complex optimization algorithms that synthesize the reference architecture, described in hardware description language (HDL), into a circuit netlist. The netlist is then used for placement, i.e. placing on the various FPGA blocks. Next, the routing of connections is performed. Finally, the resulting implementation is used to evaluate timing and power consumption [24].

As shown in Figure 4.1, in addition to the HDL files used to describe the architecture, constraint files are important design source files as they are generally used at each level to guide the FPGA tools in meeting the timing requirements of the design [24]. In particular, a timing closure procedure, illustrated in Figure 4.2, is used to achieve the required performance. This involves iterating through the various steps of the flow until the desired performance is achieved, i.e. until acceptable timing is achieved.

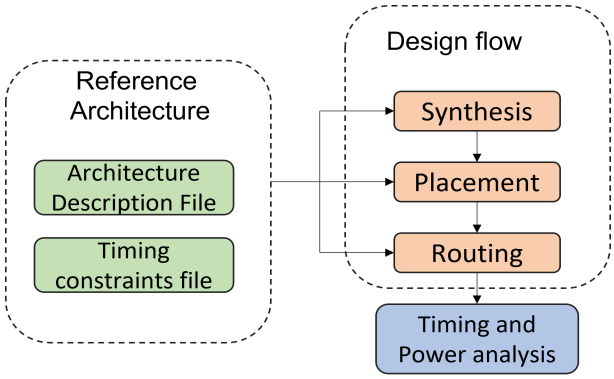

Figure 4.1: FPGA design flow [24]

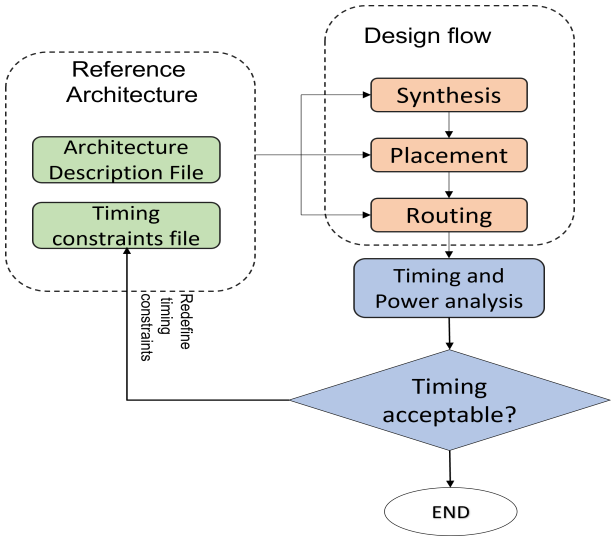

Figure 4.2: Timing closure procedure

Therefore, these design tools were used to collect the required implementation results reported in this chapter.

4.2 FPGA power consumption

Before proceeding, it is important to understand the concept of power. This is necessary in order to be able to analyze the power consumption results collected in this chapter.
First of all, power is measured in watts (W) and is the energy consumed per unit of time. In logic circuits, such as FPGAs, power dissipation can be divided into two main contributions:

- **Dynamic power**: This type of power depends on the operating frequency, supply voltage, switching activity and load capacitance. The latter is influenced by the transistor channel length, i.e. the technological node of the transistor.

$$P_{\text{dynamic}} = C_l \cdot V_{\text{DD}}^2 \cdot f \cdot E_{\text{sw}} \tag{4.1}$$

- **Static power**: This type of power is independent of switching activity. It is mainly caused by the leakage current that flows through transistors when they should be turned off. This in turn depends on the temperature and the technology used to manufacture the device.

$$P_{\text{static}} = V_{\text{DD}} \cdot I_{\text{off}} \tag{4.2}$$

In the context of FPGAs, static power can also be influenced by the architecture used [11]. For example, using LUT-6 instead of LUT-4 in logic blocks can reduce dynamic power due to fewer interconnections, but increase static power due to the larger area occupied [11].
The technology used to manufacture FPGAs is also critical. With transistor size below 100nm, leakage current becomes significant, especially at higher temperatures.
Finally, the type of FPGA configuration memory, whether RAM-based or Flash-based, can affect static power. FPGAs based on SRAM configuration memory consume more power with respect to ones based on FLASH configuration. This is due to the fact that SRAM-based FPGAs must be reconfigured at each power-on cycle.
In addition, SRAM cells require more transistors than flash cells, which increases leakage current. In summary, the **static power consumption** of an FPGA depends on a number of factors, including the operating parameters, the technology used and the specific architecture of the FPGA. In addition, the programmable structure of the FPGA requires highly flexible and configurable interconnects, which contribute significantly to **dynamic power consumption**. In order to evaluate the overall power consumption of an FPGA , it is essential to understand these factors.

4.3 Fitting, performance and power consumption results

MICROCHIP FPGA CANDIDATES

The following Microchip FPGAs have been identified in the previous chapter as potential alternatives to the FPGAs currently in use:

- MPF300TS-FC784M
- MPF200T-1FC(V)G484T2
- M2GL150(T/TS)-1FC1152M

The first two FPGAs are part of the PolarFire family, while the third one is part of the Igloo2 family.
The fitting results, reported in Table 4.1, Table 4.2 and Table 4.3, were obtained using LIBERO 2021.3.

Family	POLARFIRE
Device	MPF300TS-FC784M
4LUT	57578 / 299544 (19.22%)
DFF	51484 / 299544 (17.19%)
User I/O	211 / 338 (54.38%)
μSRAM	4 / 2772 (0.14%)
LSRAM	364 / 952 (38.24%)
Math blocks	106 / 924 (11.47%)
H-Chip Global	4 / 48 (8.33%)
Total PLLs	0 / 8 (0%)

Table 4.1: MPF300TS-FC784M : Fitting Results Summary

Family	POLARFIRE
Device	MPF200T-1FC(V)G484T2
4LUT	57609 / 192408 (29.4%)
DFF	51484 / 192408 (26.76%)
User I/O	211 / 244 (86.48%)
μSRAM	4 / 1764 (0.23%)
LSRAM	364 / 616 (59.09%)
Math blocks	106 / 588 (18%)
H-Chip Global	4 / 48 (8.33%)
Total PLLs	0 / 8 (0%)

Table 4.2: MPF200T-1FC(V)G484T2 : Fitting Results Summary

Family	IGLOO2
Device	M2GL150 (T/TS)-1FC1152M
4LUT	61078 / 146124 (41.80%)
DFF	55041 / 146124 (37.67%)
User I/O	211 / 574 (36.76%)
RAM64X18	213 / 240 (88.75%)
RAM1KX18	228 / 236 (96.61%)
MACC (DSP)	106 / 240 (44.17%)
Chip Globals	4 / 16 (25%)

Table 4.3: M2GL150 (T/TS)-1FC1152M : Fitting Results Summary

As shown in the tables above, the MPF300 has the lowest resource consumption, as expected as it is the largest evaluated Microchip FPGA. On the other hand, the memory consumption of the M2GL150 is significantly higher than the other Microchip FPGAs evaluated. The results also show that it is not possible to opt for a smaller FPGA without modifying the original code due to the high resource usage of the reference architecture.
The results of the place & route stage in the FPGA flow, as depicted in Figure 4.1, are utilized by LIBERO 2021.3 to assess power consumption and performance. Addressing any timing violations is essential. Therefore, the timing closure procedure, outlined in Figure 4.2, is executed iteratively until the timing requirements are met. The timing summaries for the respective FPGAs under evaluation are provided in Table 4.4, Table 4.5, and Table 4.6.

CLOCK DOMAIN	REQUIRED FREQUENCY (MHz)	ACTUAL FREQUENCY (MHz)
SystemClock	40	40.52
PCIClock	33.33	37.88

Table 4.4: MPF300TS-FC784M:Timing Summary

CLOCK DOMAIN	REQUIRED FREQUENCY (MHz)	ACTUAL FREQUENCY (MHz)
SystemClock	40	40.02
PCIClock	33.33	35.82

Table 4.5: MPF200T-1FC(V)G484T2:Timing Summary

CLOCK DOMAIN	REQUIRED FREQUENCY (MHz)	ACTUAL FREQUENCY (MHz)
SystemClock	40	40.63
PCIClock	33.33	37.543

Table 4.6: M2GL150 (T/TS)-1FC1152M:Timing Summary

To compute power consumption, the following conditions are considered:

- Ambient temperature: 70°C
- Toggle rate: 25%

The power consumption summaries are presented in Table 4.7, Table 4.8, and Table 4.9.
All these summaries are derived from the reports generated by LIBERO 2021.3.

FPGA	STATIC POWER (mW)	DINAMIC POWER (mW)	TOTAL POWER (mW)
MPF300TS-FC784M	596.356	330.427	926.783

Table 4.7: MPF300TS-FC784M:Power Summary

FPGA	STATIC POWER (mW)	DINAMIC POWER (mW)	TOTAL POWER (mW)
MPF200T-1FCG484T2	452.848	313.750	1090.235

Table 4.8: MPF200T-1FC(V)G484T2:Power Summary

FPGA	STATIC POWER (mW)	DINAMIC POWER (mW)	TOTAL POWER (mW)
M2GL150(T/TS)-1FC1152M	196.287	893.948	1090.235

Table 4.9: M2GL150 (T/TS)-1FC1152M:Power Summary

As expected, both the MPF200 and MPF300 have similar dynamic power consumption as they use the same amount of fabric resources to implement the reference architecture. However, their static power consumption is slightly different. The MPF300 has a higher static power consumption compared to the MPF200 due to the larger amount of fabric resources.
In addition, while the PolarFire FPGAs evaluated are built in 28nm technology, the M2GL150 FPGA is built in 65nm technology. As a result, the M2GL150 FPGA has a higher dynamic power consumption but a lower leakage current, resulting in lower static power consumption, compared to the other Microchip FPGAs.
Finally, these are FLASH-based FPGAs.

LATTICE FPGA CANDIDATES

In the previous chapter, the following FPGAs were identified for the LATTICE vendor:

- LFCPNX-100-7BBG484A
- LFMX05-100T-7BBG400I

These devices belong to the CERTUSPRO-NX and MACHXO5-NX families, respectively.

The fitting results, reported in Table 4.10 and Table 4.11 , were obtained using RADIANT 2023.1.

Family	CERTUSPRO-NX
Device	LFCPNX-100-7BBG484A
Number of registers	35160 / 80769 (44%)
Number of LUT4s	59217 / 79872 (74%)
Number used as logic LUT4s	32719
Number used as distributed RAM	4152
Number used as ripple logic	22346
Number of Block RAMs	173 / 208 (83%)
Number of LARGE RAMs	0 / 7 (0%)
Number of MULT18	104 / 156 (66%)
I/O	211 / 299

Table 4.10: LFCPNX-100-7BBG484A: Fitting Results Summary

Family	MACHXO5-NX
Device	LFMX05-100T-7BBG400I
Number of registers	35160 / 80745 (44%)
Number of LUT4s	59217 / 79872 (74%)
Number used as logic LUT4s	32719
Number used as distributed RAM	4152
Number used as ripple logic	22346
Number of Block RAMs	173 / 208 (83%)
Number of LARGE RAMs	0 / 7 (0%)
Number of MULT18	104 / 156 (66%)
I/O	211 / 291

Table 4.11: LFMX05-100T-7BBG400I: Fitting Results Summary

The resource utilization between these two FPGAs is the same, as the only difference between the devices is the presence of FLASH memory in the MACHXO5-NX FPGA.
In particular, the FPGA development process consists of several phases, the last one being the Place & Route phase.
Within the RADIANT 2023.1 development environment, the results of this phase are used to perform a detailed analysis of the system in terms of power and timing. It is important to note that although the design was implemented, timing issues may arise if the critical paths do not meet the timing requirements. Timing closure, which involves optimizing critical paths within the circuit, is often required to ensure that timing constraints are met.

Timing summaries for the evaluated FPGAs are provided in Table 4.12 and Table 4.13.

CLOCK DOMAIN	REQUIRED FREQUENCY (MHz)	ACTUAL FREQUENCY (MHz)
SystemClock	40	42.230
PCIClock	33.33	112.549

Table 4.12: LFCPNX-100-7BBG484A:Timing Summary

CLOCK DOMAIN	REQUIRED FREQUENCY (MHz)	ACTUAL FREQUENCY (MHz)
SystemClock	40	44.793
PCIClock	33.33	53.522

Table 4.13: LFMX05-100T-7BBG400I:Timing Summary

To quantify the power consumption, environmental conditions such as a temperature of 70°C and a toggle rate of 25% are taken into account.
Power consumption summaries are presented in Table 4.14 and Table 4.15.

FPGA	STATIC POWER (mW)	DINAMIC POWER (mW)	TOTAL POWER (mW)
LFCPNX-100-7BBG484A	142.954	216	358.882

Table 4.14: LFCPNX-100-7BBG484A:Power Summary

FPGA	STATIC POWER (mW)	DINAMIC POWER (mW)	TOTAL POWER (mW)
LFMX05-100T-7BBG400I	146.441	213.723	360.15

Table 4.15: LFMX05-100T-7BBG400I:Power Summary

Although both the LFCPNX and LFMX05 are SRAM-based FPGAs, their static power consumption is very low compared to the other FPGAs evaluated. This is due to the 28 nm FD-SOI technology used to build these FPGAs, which results in low short channel effects and low leakage current. This technology also offers low parasitics, resulting in low dynamic power consumption.

XILINX FPGA candidates

In the previous chapter, the following Xilinx FPGAs were identified as potential alternatives to the FPGAs currently in use:

- XQ7A100T-1FG484M
- XQ7A200T-1RB484M

They are part of the ARTIX 7 family.

The fitting results, reported in Table 4.16 and Table 4.17 , were obtained using VIVADO 2019.1.

Family	Artix 7
Device	XQ7A100T-1FG484M
SLICE LUTs **LUT as logic** **LUT as memory**	30091 / 63400 (47.46%) 30059 / 63400 (47.41%) 32 / 19000 (0.17%)
SLICE Registers (FF)	35244 / 126800 (27.79%)
Block RAM	125 / 135 (92.96%)
DSP48E1	102 / 240 (42.50%)
I/O	211 / 285 (74.04%)

Table 4.16: XQ7A100T-1FG484M: Fitting Results Summary

Family	Artix 7
Device	XQ7A200T-1RB484M
SLICE LUTs **LUT as logic** **LUT as memory**	30088 / 134600 (22.35%) 30056 / 134600 (22.33%) 32 / 46200 (0.07%)
SLICE Registers (FF)	35234 / 269200 (13.09%)
Block RAM	125 / 365 (34.38%)
DSP48E1	102 / 740 (13.78%)
I/O	211 / 285 (74.04%)

Table 4.17: XQ7A200T-1RB484M: Fitting Results Summary

As expected, both FPGAs require the same amount of fabric resources to implement the reference architecture. However, the memory consumption of the XQ7A100T is so high that a smaller ARTIX 7 FPGA cannot be used.

The implemented design represents the output of Place & Rout and is used within VIVADO 2019.1 to evaluate both power consumption and timing. As in the previous cases, the timing closure procedure was used to meet the timing requirements. The timing summaries for the respective FPGAs under evaluation are provided in Table 4.18 and Table 4.19.

CLOCK DOMAIN	REQUIRED FREQUENCY (MHz)	ACTUAL FREQUENCY (MHz)
SystemClock	40	40.083
PCIClock	33.33	33.40

Table 4.18: XQ7A100T-1FG484M:Timing Summary

CLOCK DOMAIN	REQUIRED FREQUENCY (MHz)	ACTUAL FREQUENCY (MHz)
SystemClock	40	40.06
PCIClock	33.33	33.40

Table 4.19: XQ7A200T-1RB484M:Timing Summary

To compute power consumption, the following conditions are considered:

- Ambient temperature: 70°C
- Toggle rate: 25%

The power consumption summaries are presented in Table 4.20 and Table 4.21.

FPGA	STATIC POWER (mW)	DINAMIC POWER (mW)	TOTAL POWER (mW)
XQ7A100T-1FG484M	258	316	574

Table 4.20: XQ7A100T-1FG484M:Power Summary

FPGA	STATIC POWER (mW)	DINAMIC POWER (mW)	TOTAL POWER (mW)
XQ7A200T-1RB484M	461	317	778

Table 4.21: XQ7A200T-1RB484M:Power Summary

As expected, both the XQ7A100 and XQ7A200 use the same amount of fabric resources, resulting in the same dynamic power consumption. However, there is a difference in static power consumption. The XQ7A200 has a higher static power consumption than the XQ7A100 due to its larger amount of fabric resources. These FPGAs are built in 28 nm technology and are SRAM-based FPGAs.

INTEL FPGA CANDIDATES

As analyzed in the previous chapter, the candidate Intel FPGA is the 10CL120YF484I7G , which is part of the CYCLONE 10 LP family.
The fitting results shown in Table 4.22 were obtained using QUARTUS 18.0.

Family	Cyclone 10 LP
Device	10CL120YF484I7G
Total logic elements **Total combinational functions** **Dedicated logic registers**	76237 / 119088 (64%) 56082 / 119088 (47%) 47817 / 119088 (31%)
Total pins	211 / 278 (76%)
Total memory bits	1041152 / 3981312 (26%)
Embedded Multiplier 9-bit elements	208 / 576 (36%)
Total PLLs	0 / 4 (0%)

Table 4.22: 10CL120YF484I7G: Fitting Results Summary

Similar to the previous scenarios, once the design is implemented, it was possible to evaluate both power consumption and timing. If the timing does not meet the constraints, it is important to perform the timing closure procedure to ensure that the timing requirements are met. The timing summary is provided in Table 4.23.

CLOCK DOMAIN	REQUIRED FREQUENCY (MHz)	ACTUAL FREQUENCY (MHz)
SystemClock	40	46.62
PCIClock	33.33	36.76

Table 4.23: 10CL120YF484I7G:Timing Summary

In order to compute power consumption, the following conditions are considered:

- Ambient temperature: 70°C
- Toggle rate: 25%

The power consumption summary is presented in Table 4.24.

FPGA	STATIC POWER (mW)	DINAMIC POWER (mW)	TOTAL POWER (mW)
10CL120YF484I7G	263.63	850.59	1255.04

Table 4.24: 10CL120YF484I7G:Power Summary

Both summaries are derived from reports generated by QUARTUS 18.0.
As shown in the Table 4.24, the dynamic power consumption of the 10CL120 FPGA is significantly higher than some other evaluated FPGAs, such as the 28 nm XQ7A100T FPGA. This difference is due to the fact that the 10CL120 FPGA is manufactured in 60 nm technology, which results in higher capacitance, i.e. higher dynamic power consumption.
In terms of static power consumption, the technology used is able to manage the leakage current, resulting in an acceptable level of static power consumption.
Finally, it is important to note that this FPGA is an SRAM-based type.

Power consumption: a comparative analysis

The Figure 4.3 provides an overview of the power consumption across different FPGAs used to implement a reference architecture. To quantify the power consumption of each device, operating conditions such as a temperature of 70°C and a switching rate of 25% were taken into account.

Looking at Figure 4.3, it is clear that despite implementing the same architecture across all FPGAs considered, there are variations in total power consumption due to differences in technological node, configuration memory and manufacturing process.
For example, MPF300, MPF200 and M2GL150 store the custom configuration in FLASH-type cells [15] [14] , while LFCPNX ,LFMX05, XQ7A100, XQ7A200 and 10CL120 store the configuration in SRAM-type cells [18] [21] [23] [22]. In addition, FPGAs such as MPF300, MPF200, LFCPNX, LFMX05, XQ7A100 and XQ7A200 are built in 28 nm technology, but with different manufacturing processes [15] [22] [23] [21]. On the other hand, the M2GL150 and 10CL120 FPGAs are built in 65 nm and 60 nm technologies respectively [18] [14].
The MPF200 and XQ7A200 FPGAs have a similar amount of available resources, but the latter has a higher total static power consumption due to its use of SRAM-type configuration. However, the XQ7A200 technology offers lower leakage current due to the use of Hafnium oxide for the gate dielectric, which reduces gate tunneling

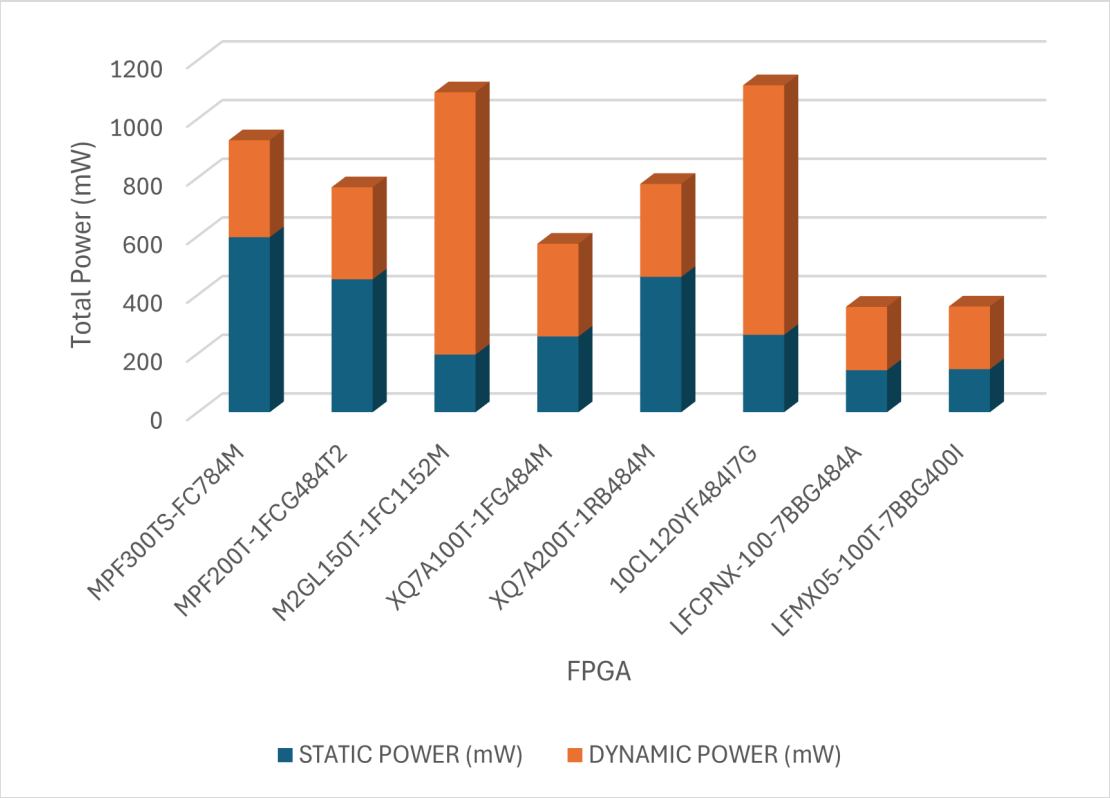

Figure 4.3: Power Consumption vs FPGA

current [25]. This reduction is offset by the configuration type, resulting in higher overall static power consumption.
Also M2GL150, LFCPNX ,LFMX05, XQ7A100 and 10CL120 FPGAs have a similar amount of fabric resources. These are SRAM-based FPGAs.
FPGAs such as LFCPNX and LFMX05, built in 28 nm full-depleted silicon-on-insulator based technology, FD-SOI, offer the lowest static power consumption due to reduced short channel effects and the lowest dynamic power consumption due to reduced parasitics. The FLASH-based M2GL150 built in 65nm technology has lower static power compared to both RAM-based 10CL120 FPGA built in 60 nm technology and RAM-based XQ7A100 FPGA built in 28 nm technology.
MPF300 and MPF200, which belong to the same family, have different static power consumption due to the larger size and higher number of devices of the former. Similarly, the XQ7A200 FPGA has a higher static power consumption than the XQ7A100 due to its larger size.
The dynamic power consumption depends on the resources used. So even if one FPGA is larger than another, the dynamic power remains constant, provided they share the same technology node and implement the same design. For this reason,

the MPF300, MPF200, LFCPNX, LFMX05, XQ7A100 and XQ7A200 FPGAs have similar dynamic power consumption to each other. The M2GL150 and 10CL120 FPGAs also have similar dynamic power consumption to each other.
Reducing the transistor size for the same design implementation allows a reduction in dynamic power for the same performance, as can be seen from Figure 4.3.

4.4 Evaluation of results

Figure Figure 4.4 provides an overview of the power consumption, package specifications and resource consumption of currently used FPGAs. These metrics are used as a baseline for evaluating the selected FPGAs.

Vendor		XILINX	INTEL
Design Tool		PlanAhead	Quartus II
Device		XQ6SLX150-2FG484Q	EP3C120F780I7
Technology		45 nm	65 nm
Logic Utilization		42%	55%
DFF Utilization		18%	31%
Block RAM Utilization		89 %	68%
DSP Utilization		57%	36 %
I/O	Utilization	62%	49%
	Complies with Voltage Constraint (3.3V)	YES	YES
Max Frequency (MHZ)	SystemClock	46.35	47.15
	PCIClock	34.47	36.96
Static Power (mW)		330	423.34
Dynamic Power (mW)		570	995.01
Temperature range		Extended Industrial: -40°C to 125°C	Industrial: -40°C to 100°C
Package	Type	Pb	Pb
	Length x Width (mm x mm)	23 X 23	29 X 29
	Pitch (mm)	1.0	1.0
Configuration memory		SRAM	SRAM

Note: For the simulation of the power consumption, environmental conditions such as a temperature of 70°C and a switching rate of 25% were applied.

Figure 4.4: Current FPGAs in use as evaluation baseline

The results of the evaluation are then summarized and presented in Figure 4.5. Among the evaluated FPGAs, two must be selected to replace the obsolete EP3C120F780I7 and XQ6SLX150-2FG484Q FPGAs. To ensure system robustness, it is necessary to select FPGAs from two different vendors.
The options highlighted in green in Figure 4.5, XQ7A100T-1FG484M, XQ7A200T-1RB484M, M2GL150(T/TS)-1FC1152M and MPF300TS-FC784M, meet all power, performance, package and I/O supply voltage constraints.
When selecting an FPGA, it is important to consider the trade-off between power efficiency and constraints compliance. If FPGAs don't meet the package and I/O supply voltage constraints, this will add cost and time to address these issues.

Therefore, the first FPGA selected to replace one currently in use will be one of those highlighted in green in Figure 4.5. However, XQ7A200T-1RB484M and MPF300TS-FC784M are underused in terms of fabric resources, making them unsuitable replacements. In addition, M2GL150(T/TS)-1FC1152M is not considered due to its large package size and outdated 65nm technology.
The XQ7A100T-1FG484M FPGA is compared to the XQ6SLX150-2FG484Q FPGA, which is used as the evaluation baseline, as both have LUT-6 in their basic logic block. Despite similar resource consumption, with the exception of memory, the XQ7A100T-1FG484M has a lower power consumption as shown in Figure 4.6. This difference is due to the fact that the XQ7A100T-1FG484M is built using more advanced and efficient technology. Therefore, XQ7A100T-1FG484M is chosen as the first alternative FPGA.
Among the other FPGAs, not one of them fully meets all the requirements. For example, 10CL120YF484I7G meets the voltage constraint but not the package type. Similarly, LFCPNX-100-7BBG484A, LFMX05-100T-7BBG400I and MPF200T-1FCG484T2 do not meet the I/O supply voltage and package type constraints.
This means that power consumption represents the key consideration when choosing the second alternative FPGA. So, looking at Figure 4.6, the choice is reduced to LFMX05-100T-7BBG400I and LFCPNX-100-7BBG484A, which differ in the presence of FLASH memory, as they offer the lowest power consumption. The final choice between them depends on cost considerations, which are not discussed here and are left to the experts. However, either LFMX05-100T-7BBG400I or LFCPNX-100-7BBG484A will be chosen as the second alternative FPGA to replace one of the two currently in use.

Vendor		**XILINX**		**INTEL**	**LATTICE**		**MICROCHIP**					
Design Tool		VIVADO 2019.1		QUARTUS 18.0	RADIANT 2023.1		LIBERO 2021.3					
Device		XQ7A100T-1FG484	XQ7A200T-1RB484	10CL120YF 484I7G	LFCPNX-100-7BBG484A	LFMX05-100T-7BBG400I	MPF200T-1FCG484T2		MPF300TS-FC784M		M2GL150 (T/TS)-1FC1152M	
Technology		28 nm-HKMG	28 nm-HKMG	60 nm	28 nm-FD-SOI	28 nm-FD-SOI	28 nm		28 nm		65 nm	
Logic Utilization		47.41%	22.33%	47%	47.21%	47.21%	29.94%		19.22%		41.80%	
DFF Utilization		27.71%	13.09%	40%	44%	44%	26.76%		17.19%		37.67%	
RAM Utilization	**Block Ram**	92.96%	34.38%	35%	83%	83%	LSRAM	59.09 %	LSRAM	38.24%	RAM 1Kx 18	96.61 %
							µSRAM	0.23%	µSRAM	0.14%	RAM 64x 18	88.75 %
	Distributed Ram	0.17%	0.07%	-	5.20%	5.20%	-		-		-	
DSP Utilization		42.50%	13.78%	36%	66%	66%	18%		11.47%		44.17%	
I/O	**Utilization**	74.04%	74.04%	76%	70.57%	72.50%	86.48%		54.38%		36.76%	
	Complies with Voltage Constraint (3.3V)	YES	YES	YES	NO	NO	NO		YES		YES	
Max Frequency (MHZ)	**SystemClock**	40.083	40.06	46.62	42.230	44.793	40.02		40.52		40.63	
	PCIClock	33.40	33.40	36.76	112.549	53.522	35.82		37.88		37.543	
Static Power (mW)		258	461	263.63	142.954	146.44	452.848		596.356		196.287	
Dynamic Power (mW)		316	317	850.59	216	213.723	313.750		330.427		893.948	
Temperature range		M[1]	M[1]	E[1]	A[1]	I[1]	A[1]		M[1]		M[1]	
Package	**Type**	Pb	Pb	Pb-free	Pb-free	Pb-free	Pb-free		Pb		Pb	
	Length x Width (mm x mm)	23 x 23	23 x 23	23 x 23	19 x 19	17 x 17	23 x 23		29 x 29		35 x 35	
	Pitch (mm)	1.0	1.0	1.0	0.8	0.8	1.0		1.0		1.0	
Configuration memory		SRAM	SRAM	SRAM	SRAM	SRAM	FLASH		FLASH		FLASH	

Notes: 1. M=Military temperature range: -55°C to 125°C, A= Automotive temperature range:-40°C to 125°C , I=Industrial temperature range:-40°C to 100°C and E=Extended industrial temperature range:-40°C to 125°C.
For the simulation of the power consumption, environmental conditions such as a temperature of 70°C and a switching rate of 25% were applied.

Figure 4.5: Evaluation results

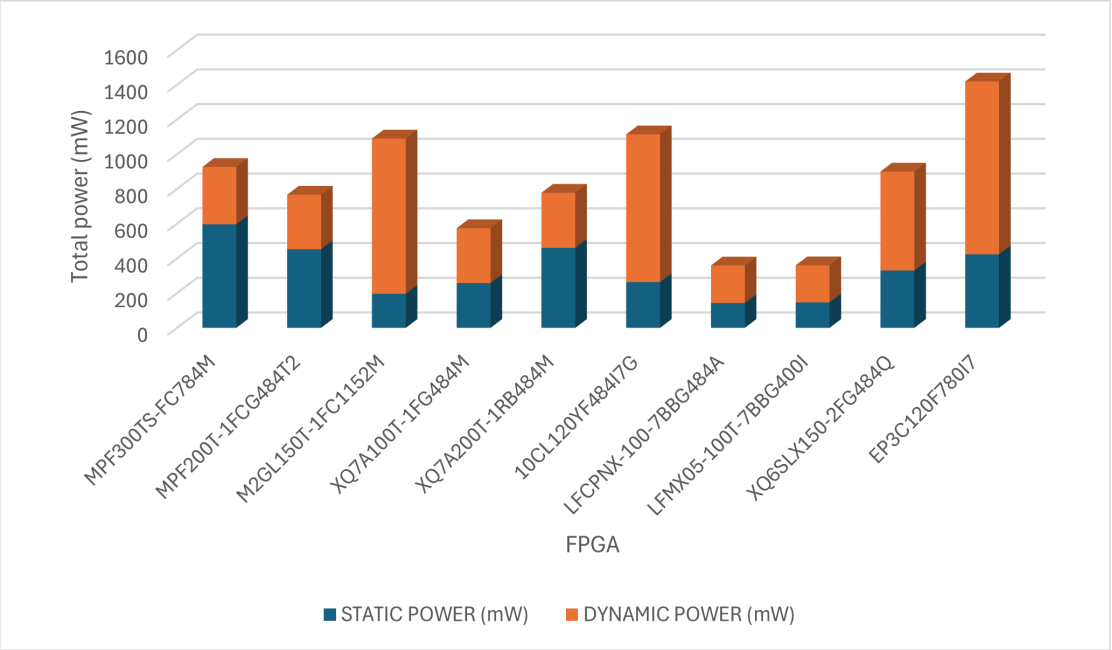

Figure 4.6: An overview about power consumption

Chapter 5

Conclusions

The longevity of avionics projects faces technological evolution. According to Moore's Law, the number of transistors in an integrated circuit (IC) doubles about every two years. Since 1990, this law has encountered a number of obstacles, such as the increasing power consumption of interconnects with scaling, the rise of Short Channel Effects (SCE) leading to an increase in leakage current, and so on. To overcome these problems and sustain Moore's Law, it has been necessary to explore new materials and use new techniques in device manufacturing processes. For example, reducing gate oxide thickness to a few nanometres increases tunneling phenomena, resulting in higher leakage current and static power consumption. To resolve this issue, it was necessary to introduce new gate materials with high dielectric constants, such as hafnium oxide. The reduction in device size thus leads to new challenges in power management, but it makes also possible to have high-density chips with a rather small footprint.
Avionics projects are implemented using complex hardware components such as Field Programmable Gate Arrays (FPGAs). Specifically, a FPGA is a type of integrated circuit that can be programmed and configured by the user to implement any digital circuit.
Due to technological evolution, these FPGAs could quickly become obsolete, threatening the longevity of avionics projects. Recognizing the importance of this issue, this thesis, conducted in collaboration with Leonardo Electronics, proposes a methodology for the timely replacement of potentially obsolete FPGAs used in a real project by proposing suitable alternatives. This real project complies with the dissimilarity constraint that is sometimes necessary to guarantee system robustness. For this reason, this project is implemented on two FPGAs from different vendors. The methodology exploited to replace these two FPGAs with alternative technological solutions is based on one key consideration: FPGA porting and benchmark across different manufacturers.
In order to identify alternative FPGAs to those currently in use, the current FPGA

market has been explored, focusing on the key factors that differentiate one FPGA from another: manufacturing process, logic blocks, memory, DSP capabilities and I/O compatibility. It is important to clarify that the FPGAs selected from those available on the market must meet the fabric resources required to implement the reference architecture, the operative constraints and the DO-254 standard.
To quantify the amount of fabric resources required to implement the reference architecture, the reports from the two FPGAs currently in use were analyzed, which in turn were derived from the design tool used to implement the architecture under consideration. Operative constraints include a temperature range constraint of at least -40°C to 100°C and a total power dissipation of less than 1 W worst case at 70°C. In addition, the FPGA package must be leaded because avionics systems are subject to significant mechanical and thermal stress, making RoHS-compliant packages susceptible to electromigration phenomena. Finally, to minimize the impact on the board on which the two FPGAs are implemented, the I/Os must support a voltage of 3.3 V.
After identifying FPGAs from various vendors that met the previously described constraints, from fabric resources to package type, a full design run was performed using Xilinx Vivado 2019.1, Microchip Libero 2021.3, Intel Quartus 18.0 and Lattice Radiant 2023.1. This full design run includes synthesis, place and route, power simulation and timing analysis.
In this way, it was possible to collect all the results of implementing the reference architecture on each selected FPGA in order to compare the different FPGAs evaluated and identify the best candidates.
This process of FPGA porting and benchmarking among the various selected devices facilitated a comparison of power consumption and performance. Assuming the same target clock frequencies, this process focused attention on the role of technology in power consumption. The results highlighted the advantages and disadvantages of the FPGAs evaluated, providing a valid tool for identifying the best candidates to replace the FPGAs currently in use.
The analysis showed that the XQ7A100T-1FG484M, LFMX05-100T-7BBG400I and LFCPNX-100-7BBG484A FPGAs are the best candidates for various aspects. The first FPGA, XQ7A100T-1FG484M, fulfils all the requirements, so porting the source code to this FPGA is straightforward. The other two do not meet the pin supply voltage and package constraints, requiring the integration of level shifters to adjust the voltage from 3.3 V to that supported by the pins, and the reballing process to replace the balls with leaded balls. However, these FPGAs are built in 28 nm FD-SOI technology, which helps to reduce static power consumption, reducing the challenges of heat dissipation in avionics systems, where the use of heat sinks is sometimes not feasible.
It is well known that total power is the sum of static power and dynamic power. Dynamic power depends on supply voltage, clock frequency, load capacitance and

switching activity. Static power, on the other hand, is mainly due to leakage current, which is exponentially dependent on temperature. Static power also depends on the core supply voltage and the manufacturing process. In particular, a 5% increase in supply voltage leads to a 15% increase in static power.
The other FPGAs evaluated are built in bulk technology, which differs from FD-SOI in the manufacturing process. Compared to bulk technology, FD-SOI reduces parasitics, thus lowering dynamic power consumption assuming performance unchanged, and reduces short-channel effects, thus reducing leakage currents. FD-SOI technology also exhibits greater radiation hardness, reducing the risk of latch-up, which can lead to device destruction due to a high current between the supply voltage and ground.
In conclusion, while technological evolution poses a threat to the longevity of avionics projects, it also provides an opportunity to improve the robustness and resilience of the avionics systems.

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