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Advanced HBT Modeling for High Frequency HBT Power Amplifiers

Master degree in Electrical Engineering

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Contents

CHAPTER 1

Heterojunction Bipolar Transistor

Heterojunction Bipolar Transistors (HBTs) represent an advancement in semiconductor device technology, offering a promising solution to the increasingly demanding requirements of modern electronic systems. Unlike the homojunction inside conventional Bipolar Junction Transistors (BJTs), HBTs utilize a heterojunction structure at the emitter-base interface, where two different semiconductor materials with varying bandgaps are joined. This results in several distinct advantages over traditional BJTs, including enhanced speed, lower power dissipation, lower voltage requirements, and improved high-frequency performance [1]. Nowadays, HBTs have garnered considerable interest and are being used in a variety of applications, including microwave and millimeter-wave amplifiers and high-speed digital circuits. In particular, GaAs HBTs, compared to SiGe counterparts, show higher operating frequencies, hence providing higher gain in the microwave range, higher breakdown voltage and power density and better linearity, at the cost of lower thermal conductivity of the substrate. Also compared to GaAs Field-Effect Transistors (FETs), HBTs show many advantages, such as higher transconductance and power density, at lower supply voltage. Their unique combination of low supply voltage and good high-frequency performance makes HBTs essential components in advanced communication systems, aerospace electronics, and high-performance computing. In this Chapter, the basic characteristics and models for simulating HBTs are discussed together with the thermal challenges that play a fundamental role, especially for power-demanding applications.

1.1 HBT device structure and operating principle

Like Bipolar Junction Transistors, HBTs can be either NPN- or PNP-type transistors (figure 1.1). Thanks to the higher mobility of electrons, leding to an higher cut-off frequency, and a higher input power density, NPN transistor are preferred for high-frequency high-power applications [2]. This thesis focuses on NPN transistor only and in particular uses as reference technoogy the commercial Win Semiconductors' NPN HBT process H02U.

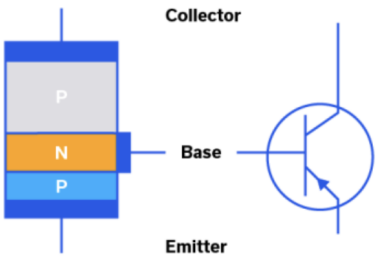

Figure 1.1: NPN Transistors

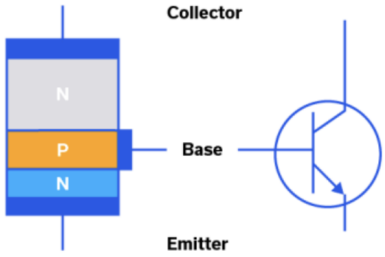

Figure 1.2: PNP Transistors

All bipolar transistors, including HBTs, have four distinct regions of operation, defined by the bias condition of the two junctions:

- **Forward-active region**: The base–emitter junction is forward biased and the base–collector junction is reverse-biased. Most bipolar transistors are designed to afford the greatest common-emitter current gain β_F in forward-active mode.
- **Reverse-active region**: Reversing the biasing conditions of the forward-active region, a bipolar transistor goes into reverse-active mode. In this mode, the emitter and collector regions switch roles.
- **Saturation region**: With both junctions forward biased, a bipolar transistor is in saturation mode and facilitates high current conduction from the collector to the emitter (or the other direction in the case of a PNP device).
- **Cut-off**: When both junctions are reverse biased the device is in cut-off state. There is very little current flowing in the transistor in this region.

For power amplifier applications, HBTs work in the forward-active region, therefore the base-emitter junction is forward-biased and the collector-base junction is reversed-biased. There is a certain current amplification from the base to the collector because of the following physical reason: the equilibrium is disturbed and electrons are injected from the emitter into the base creating a current I_n. Then the electrons diffuse across the base until they reach the edge of the base-collector depletion region and are immediately accelerated across the base-collector junction into the collector where they are majority carriers contributing to the collector current (I_C). The base current (I_B) is due to the holes diffusing from the base into the emitter and there is also a small contribution from electrons that fail to cross the base because they recombine [3]. The various physical currents due to the electrons and holes movement are listed in the table 1.1.

I_n	electron current from emitter to base
I_p	hole current from base to emitter
I_s	current due to electron/hole recombination within forward biased emitter-base space charged layer
I_r	current due to bulk recombination in base

Table 1.1: Physical currents in a bipolar transistor.

All these components contribute to the emitter, collector and base currents as shown in table 1.2.

I_E	emitter current	$I_E = I_n + I_p + I_s$
I_C	collector current	$I_C = I_n - I_r$
I_B	base current	$I_B = I_p + I_r + I_s$

Table 1.2: Currents in the bipolar transistor.

Two figures are used to describe the current gain in a bipolar device. The first is common emitter current gain β_F defined as the ratio of the collector current to the base current in the forward-active region and is given by

$$\beta_F = \frac{I_C}{I_B} = \frac{I_n - I_r}{I_p + I_r + I_s} >> 1 \tag{1.1}$$

The second is the common-base current gain, α_F. The common-base current gain is approximately the gain from the emitter to the collector in the forward-active region.

$$\alpha_F = \frac{I_C}{I_E} = \frac{\beta_F}{1 + \beta_F} \tag{1.2}$$

ans it is also equal to

$$\alpha_F = \gamma b \tag{1.3}$$

where $\gamma < 1$ is the emitter efficiency, $b < 1$ is the base transport factor [4].

HBT improvements compared with conventional BJT

For HBTs, the emitter-base and the base-collector junction are heterojunctions strategically designed to modulate the flow of charge carriers, limiting the injection of holes from the base into the emitter region. This is achieved adopting an emitter semiconductor material with a wider bandgap compared to the base. This make HBTs better suited for power amplification since:

1. HBT uses higher base doping than in homojunction transistors, resulting in decreased base resistance compared with conventional transistors [5].

2. Emitter-base heterojunction provides a high energy barrier for hole injection and a lower energy barrier for electron injection, which results in high emitter injection efficiency compared with conventional transistors [5].

3. Lower emitter doping results in a negligible minority carrier storage, reducing base-emitter capacitance and enabling higher frequency operation with excellent wideband performance [6].

4. High electron mobility and lower electron transit time due to the thinner base result in higher frequency of operation compared with conventional transistors and FETs [3, 6].

To better understand the effect of the heterojunction, consider, as and example, an AlGaAs/GaAs HBT with abrupt emitter-base junction and graded emitter-base junction as constructed in figure 1.4. The band diagram for this HBT is shown in figure 1.3: the potential barrier for hole injection ΔV_p and the potential barrier for electron injection ΔV_n in the emitter-base junction differ by the bandgap difference ΔE_g between the AlGaAs emitter the GaAs base [7].

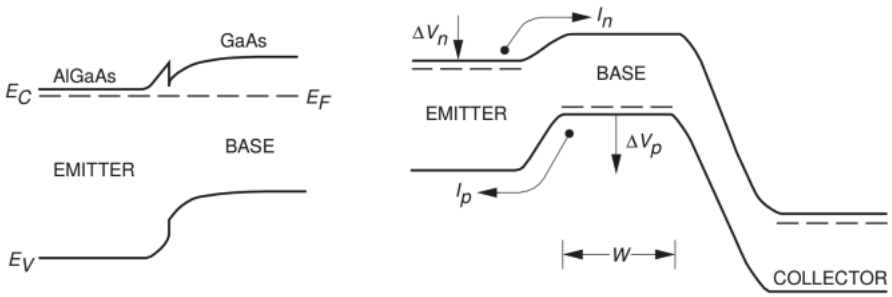

Figure 1.3: Band diagram for the AlGaAs/GaAs HBT

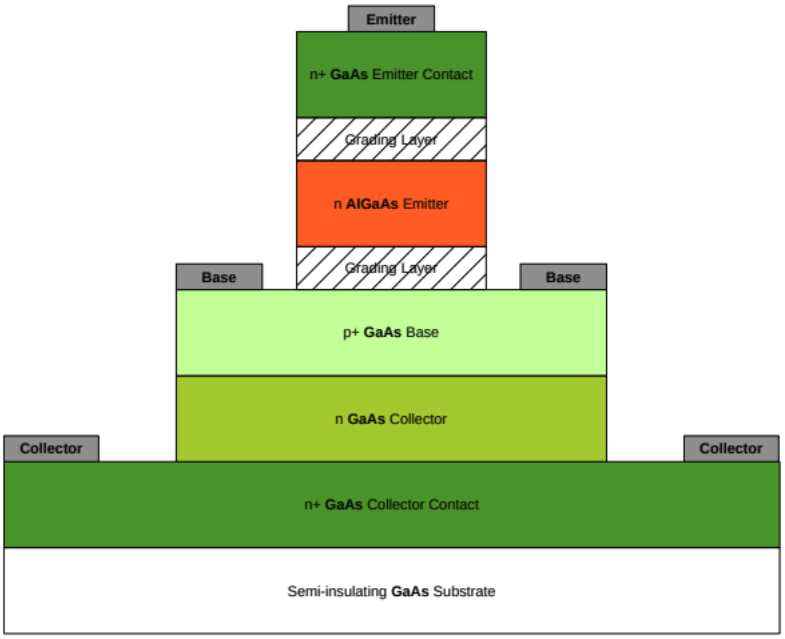

Figure 1.4: Composition of the NPN AlGaAs/GaAs HBT

1.2 Challenges for HBTs working as power amplifiers

Despite the good potential of HBTs for power amplification, the design of HBT power amplifiers poses three main challenges:

- Thermal stabilization or compensation.
- Biasing circuit design.
- Power cell layout.

These challenges are strongly related to each other and to the thermal nonlinear behavior for HBTs: a very critical aspect of this technology compared to FETs. There are two major thermal aspects that can be considered. One is self-heating [8], in fact, whereas in FET devices the effect of self-heating only some performances degradation, in bipolar transistors it can lead to thermal instability, the so-called current hogging, i.e. the uneven current distribution, in multi-finger devices. Both Si- and GaAs-based HBT technologies suffer from this phenomenon but the effect is very different since the current gain (β_F) has the opposite behavior in temperature for those two materials: it increases for Si devices, leading to thermal runaway, while it decreases for GaAs devices, leading to current gain collapse when the thermal instability condition is met [9].

1.2.1 Self-heating

Self-heating is a phenomenon observed in many semiconductor devices: it refers to the increase in the temperature of the device due to the dissipation of power during operation. To observe the effects in simulation, the Win foundry model (including self-heating effects) and an ideal HBT model (without self-heating effects) are used. Details about the foundry model will be given in Chapter 2. In both cases a DC analysis sweeping the base current and collector-emitter voltage has been performed as shown in the schematic of figure 1.5. V_{CE} is varied from 0 V to 8 V with step 0.1 V and DC base current I_{BB} from zero to 1 mA with steps of 100 µA. The results are reported in figure 1.6 and figure 1.7.

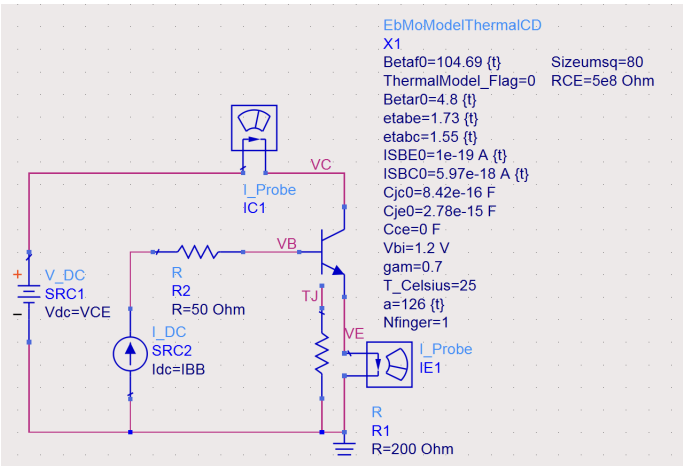

Figure 1.5: DC schematic of an ideal HBT.

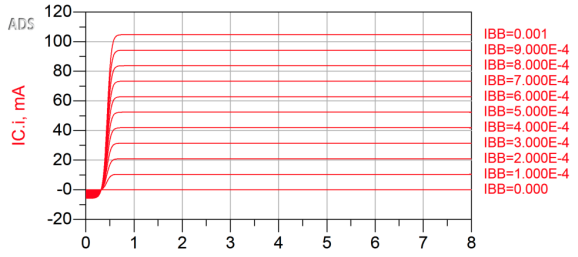

Figure 1.6: DC simulation of an ideal HBT.

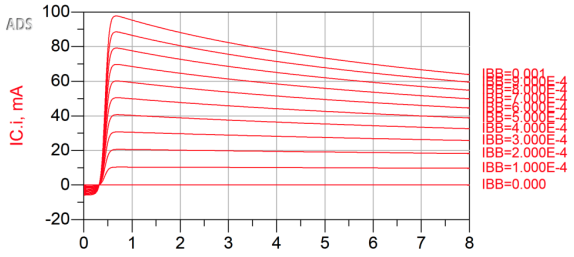

Figure 1.7: DC simulation of a real GaAs HBT.

Due to self-heating, the real HBT does not show a constant collector current in saturation, as is instead the case in the ideal HBT situation. When the collector DC voltage varies, the current gain between the collector current and the base current no longer remains constant; in fact, the collector current decreases as the DC voltage rises. In general, the consequence of self-heating in HBTs are [10]:

- **Increase of Base Current:** The increase in temperature can lead to a rise in the base current of the transistor. This is because the intrinsic carrier concentration in the base region increases with temperature.
- **Reduction in Current Gain:** The temperature rise can also affect the current gain of the transistor. Higher temperatures can decrease the mobility of charge carriers, leading to a reduction in current gain and overall transistor performance.
- **Shift in Operating Characteristics:** The increase in temperature can cause a shift in the operating characteristics of the transistor, such as its threshold voltage and saturation current.
- **Degradation of Device Reliability:** Extended periods of operation at high temperatures resulting from self-heating may cause a rapid deterioration of device reliability. This may manifest as greater leakage currents, decreased breakdown voltages, and possible long-term reliability problems.

1.2.2 Current collapse

The current collapse (or current gain collapse) is a phenomenon observed in multi-finger GaAs HBTs under high-voltage/high-power conditions. It occurs when one particular finger of a multi-finger GaAs HBT suddenly conducts most of the device current (hogging), giving rise to a drastic decrease in the device current gain.

Compared to the single-finger device, the multi-finger device suffers from collector current collapse even though the temperature difference between fingers is pretty small. It has been shown that the collapse of current gain occurs when the thermal instability condition is met [11]. To observe the collector-current-collapse effect in simulation, many single-finger GaAs HBT has been paralleled and connected to generate the equivalent effect of a multi-finger GaAs HBT. The circuit is built in figure 1.8: in this case as an equivalent to a two-finger HBT device. The HBT model adopted in this simulations is again the Win's foundry model adopted in the previous analyses and described in details in Chapter 2.

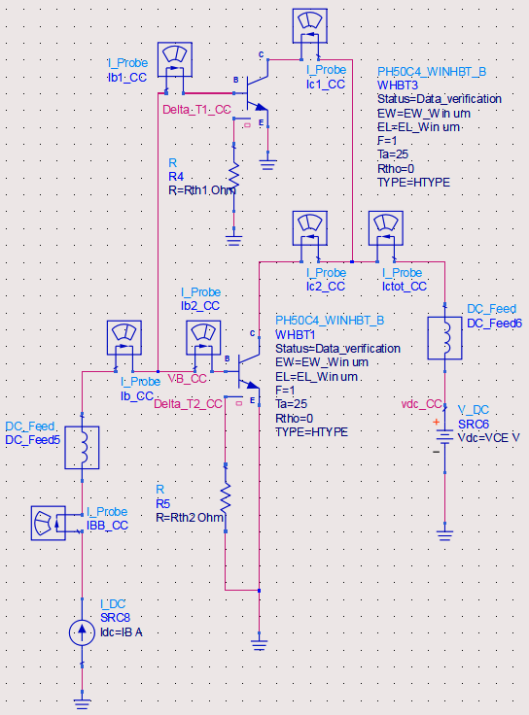

Figure 1.8: Equivalent multi-finger HBT schematic.

The collector-current collapse occurs when a particular finger suddenly draws most of the collector current because of its non-uniform current distribution, leading to a decrease in device current gain. To force this effect to happen, the two single-finger HBTs have been provided a different thermal resistance ($Rth1$ and $Rth2$, details on how the external thermal resistance work in the Win model will be given later on). The DC voltage V_{CE} ranges from 0 V to 15 V with step 0.01 V. The DC base current I_{BB} sweeps from 0 to 1 mA with steps of 100 µA. The final simulation result is shown in figure 1.9 and figure 1.10. If the two fingers' thermal resistances are set to be the same, there is no current collapse effect for multi-finger GaAs HBT, the simulation result is shown in figure 1.11 and figure 1.12.

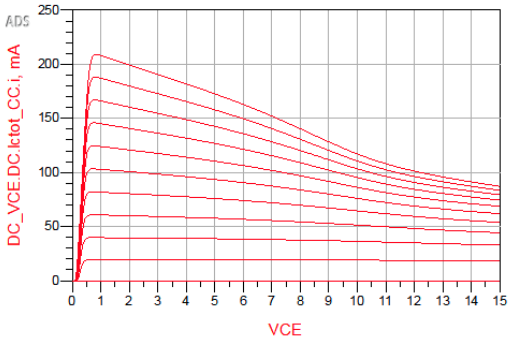

Figure 1.9: Collector current collapse effect.

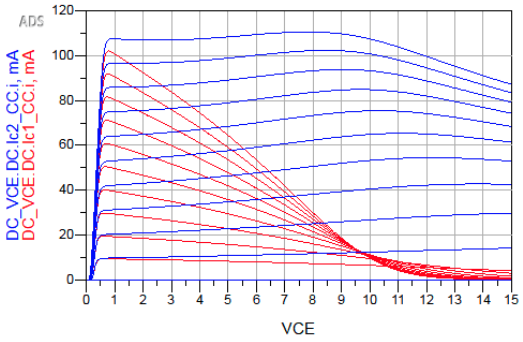

Figure 1.10: Collector current distribution with collapse effect (current hogging).

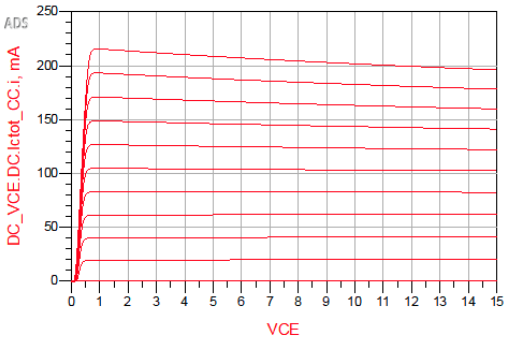

Figure 1.11: Total collector current without collapse effect.

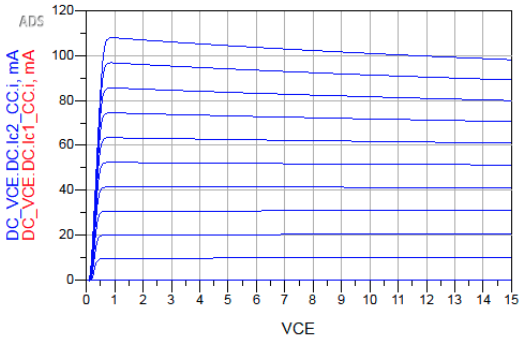

Figure 1.12: Collector current distribution without collapse effect.

The collapse does not cause HBTs to fail immediately, however, it degrades the device performance significantly and should be avoided through the proper design of the ballasting resistor.

1.3 Thermal stabilization of GaAs HBTs

The high power density of GaAs HBTs emphasizes the role of proper thermal design. There are two major solution to be always considered when dealing with thermal effects in HBTs. The first is the use of ballasting resistances to avoid the collapse of current gain caused by internal current unbalance, which will be analyzed in the following section. A second aspect, which can not be underestimated, is the design of bias circuits that enable to keep the device performance as constant as possible in temperature, in order to fully exploit the excellent radio-frequency performance of the GaAs HBT technology [12]. Indeed, bias networks play a crucial role in HBT power amplifiers [13]: both in minimizing performance variation in temperature and in enhancing the gain linearity in the high-power region. Chapters 3 and 4 are dedicated to the study of biasing networks, in particular:

- Chapter 3 focuses on the more classical biasing solutions based on current mirrors: the main drawback of simple resistive bias is in fact operating point temperature stability, which can be sensibly improved by resorting to current mirrors to fix either the base o the collector current.
- Chapter 4 shows instead more advanced active bias solutions which, besides giving the same advantages of the basic current mirrors ones, can also provide a linearization effect on gain. Many active bias

circuits in the literature have been proposed including a linearizer to compensate for bias voltage or current depression. Indeed, as already pointed out, the DC base-emitter voltage decreases with increasing input power densities and this negatively impacts on transconductance thus deteriorating AM/AM distortion [14]. The most widely adopted linearization scheme, introduced in [15] exploits the base-emitter diode of a buffer transistor together with a shunt capacitor (replaced by a reverse-biased diode in [14]). The diode-capacitance pair compensates for the decrease of the bias voltage at high input power by acting on the base-emitter voltage of the biasing HBT.

1.3.1 Ballasting resistances

The use of ballasting resistors is a fundamental technique used in all HBT power amplifiers, to prevent or mitigate current gain collapse. Contrary to Si-based device, both emitter-ballasting and base-ballasting can be adopted in a GaAs HBT, thus both case are analyzed in the following to prove their ability to solve the HBT's thermal instability.

Emitter-ballasting resistance

Emitter ballasting is the most widely adopted method to mitigate current hogging in Silicon HBT, and can be profitably exploited also in GaAs devices, despite the opposite current gain trend in temperature. Starting from the schematic in figure 1.8, individual emitter ballasting resistors R_E have been added as shown in figure 1.13.

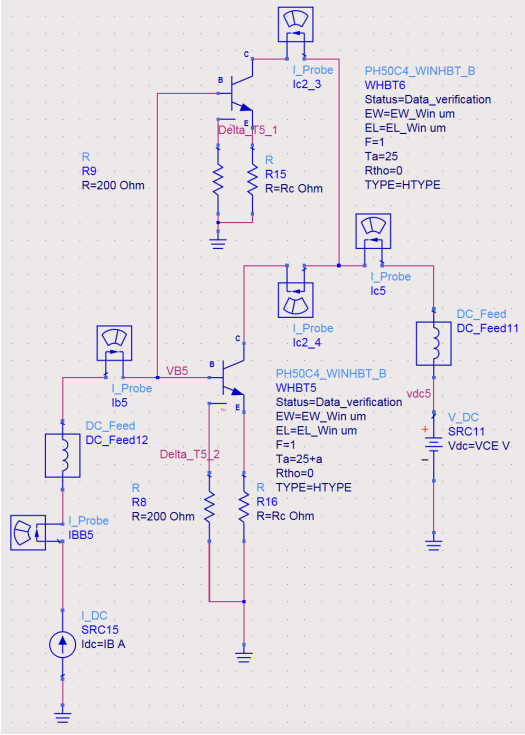

Figure 1.13: Emitter-ballasting schematic.

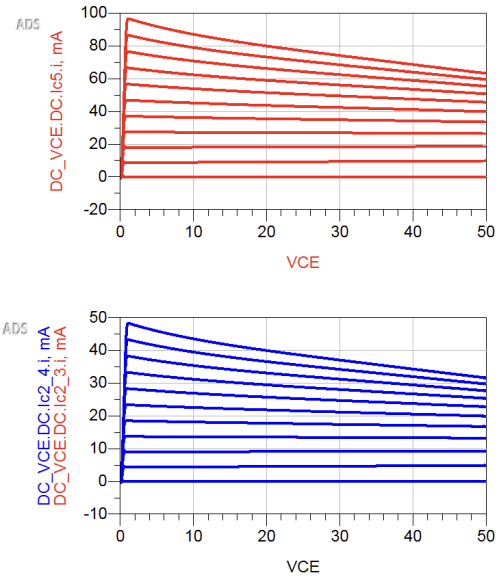

Figure 1.14: Emitter-ballasting simulation results.

The value of the resistances (equal for the two finger) have then been tuned in order to achieve current balance, as demonstrated in figure 1.14. Comparing these results to the current behavior in figure 1.10, it is evident that the emitter ballasting resistance is effective in the elimination of the collector current collapse effect. The value obtained in case of the adopted Win's model is

$$R_E = 4\,\Omega/\text{finger}$$

In some cases ohmic losses in the connection path among fingers can be engineered to provide most of the required ballasting avoiding the need of thin film resistors. Nonetheless, a ballasting resistor which is placed in the collector current path degrades the collector efficiency of the device. Therefore, the actual ballasting emitter resistance value chosen for a practical HBT is often chosen as a compromise between performance and thermal stability in the entire operating region.

Base-ballasting resistance

GaAs-based HBTs can also exploit base ballasting resistance to produce negative feedback with temperature. In fact, as the current amplification factor falls because of self-heating, more base current is needed; as a result, the base-emitter voltage is reduced when a base resistor is introduced because of its voltage drop. With respect to emitter ballasting this ensures much lower (in some cases negligible) efficiency degradation, but, on the other hand it demands for larger chip area to implement the relatively large resistor values required to be effective [16].

Adding individual base ballasting resistor to the same circuit (figure 1.15) and tuning them to achieve even current distribution (figure 1.16), the value of the base-ballasting resistances R_B required for the Win's model to compensate for the thermal instability is:

$$R_B = 230\,\Omega/\text{finger}$$

As expected, the required value is much higher (more than 50 times R_E), due to the current gain between base and emitter.

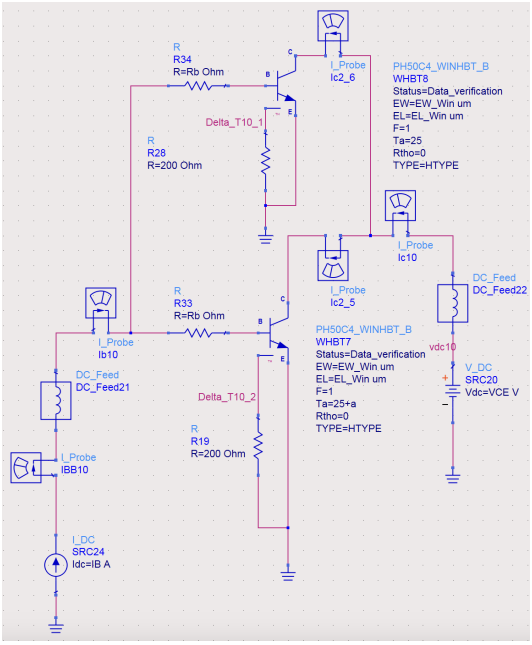

Figure 1.15: Base-ballasting schematic.

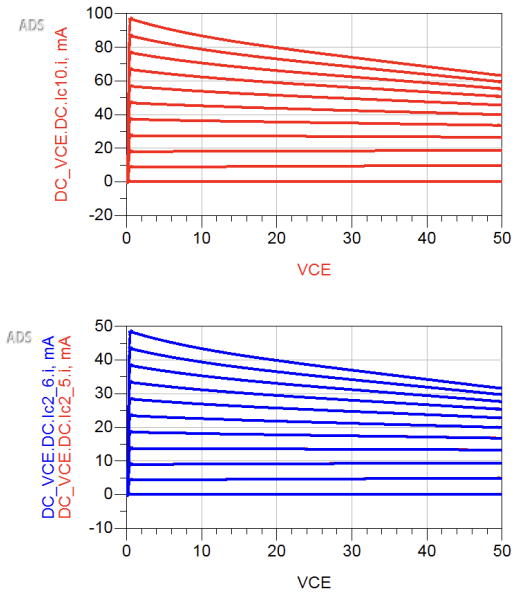

Figure 1.16: Base-ballasting simulation results.

1.4 GaAs HBT modelling

Owing to the complexity of hardware testing, the thesis work relies on CAD software simulations. The adopted software, Keysight Advanced Design System (ADS), is specifically designed for high-frequency analog circuits.

As one of the goal of this thesis is to develop a custom HBT model including temperature effects, a brief introduction to popular HBT models is discussed in the following.
The most widely adopted models for HBTs are the **Ebers-Moll model** and **Gummel-Poon model**:

- The HBT Ebers-Moll model is a relatively simple and compact model that describes the behavior of HBTs in terms of their terminal currents. It is an extension of the Ebers-Moll model originally developed for conventional BJTs. The ideal HBT Ebers-Moll model represents the HBT as a three-terminal device and provides a valuable framework for analyzing and simulating the performance of HBTs in various circuit configurations, enabling the design and optimization of HBT-based electronic systems [17].
- The HBTs Gummel-Poon model is another widely-used compact model. Similar to its counterpart for BJTs, the Gummel-Poon model provides a detailed description of the HBT's terminal current and voltage relationships in terms of its internal transistor parameters. This model is particularly useful for device characterization, parameter extraction, and circuit simulation. By incorporating the heterojunction properties of HBTs, the Gummel-Poon model provides a more comprehensive framework for accurately predicting the behavior of HBTs in practical circuit applications, thus aiding in the development of high-performance HBT-based electronic devices [18].

1.4.1 Ebers-Moll HBT model

The classic mathematical model for the bipolar junction transistor is the Ebers-Moll model formulated by J. J. Ebers and J. L. Moll from Bell Laboratories in early 1954 [17]. The Ebers-Moll model provides an alternative view or representation of the voltage-current equation model including configurationally series resistances, depletion capacitances, and charge carrier effects [19]. The basic Ebers-Moll HBT model is composed of two diodes and two current generators connected like in figure 1.17. In the HBT, the transistor looks like two diode

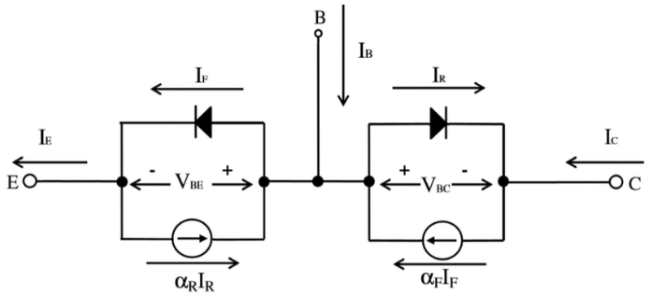

Figure 1.17: The Ebers-Moll Model of an NPN transistor. Two dependent current sources are used to indicate the interaction of the junctions.

junctions, with the collector positive with respect to the emitter, the base-emitter diode forward biased and the base-collector diode reverse biased. Therefore, currents into the collector and emitter are controlled by the current generator and the diode direction in figure 1.17. The DC emitter and collector currents in active mode can be well approximated using the Ebers-Moll model for bipolar junction transistors. Here are the equations 1.4 and 1.5 for the emitter and collector currents in terms of the transistor voltages. These current equations provide a simplified yet effective description of the DC behavior of HBTs in the active mode [19].

$$\text{Emitter Current } (I_E): \quad I_E = I_{ES}\left(e^{\frac{V_{BE}}{V_T}} - 1\right) - \alpha_R I_{CS}\left(e^{\frac{V_{BC}}{V_T}} - 1\right) \tag{1.4}$$

$$\text{Collector Current } (I_C): \quad I_C = \alpha_F I_{ES}\left(e^{\frac{V_{BE}}{V_T}} - 1\right) - I_{CS}\left(e^{\frac{V_{BC}}{V_T}} - 1\right) \tag{1.5}$$

Where:

- I_{ES}, I_{CS}: the reverse saturation currents for the emitter-base and collector-base junctions, respectively.
- V_{BE} and V_{BC}: the voltage across the base-emitter and base-collector junctions, respectively.
- α_F and α_R: the forward and reverse common-base current gains, respectively.
- V_T: the thermal voltage, equal to kT/q, where k is Boltzmann's constant, T is the temperature in Kelvin, and q is the elementary charge.

The equations 1.4 and 1.5 can be further simplified into a popular interpretation of a transistor as a current amplifier, where the collector current is proportional to the base current [20]. The constant of proportionality, β_F, is the common-emitter current gain. The relationship between base and collector currents in this simplified model is shown in equation 1.6.

$$I_C \approx I_E = \beta_F \cdot I_B \tag{1.6}$$

Looking at the transistor as a transconductance device where the collector current is controlled by the base-emitter voltage (V_{BE}), the collector current I_C is described by equation 1.7 which is the simplified version of equation 1.4 and equation 1.5.

$$I_C = I_S \cdot \left(e^{\frac{V_{BE}}{V_T}} - 1 \right) \tag{1.7}$$

Where $I_S = I_{ES}$ is the reverse saturation current.

Conversely, the base-emitter voltage can be described as a function of the collector current.

$$V_{BE} = V_T \cdot ln \left(\frac{I_C}{I_S} + 1 \right) \tag{1.8}$$

In equation 1.7 and equation 1.8, V_T is about 26 mV at room temperature, while I_S is typically in the range of 10^{-15}A. Since $I_C \gg I_S$, the equation 1.7 and equation 1.8 can be simplified into equation 1.9 and equation 1.10.

$$I_C = I_S \cdot e^{\frac{V_{BE}}{V_T}} \tag{1.9}$$

$$V_{BE} = V_T \cdot ln \left(\frac{I_C}{I_S} \right) \tag{1.10}$$

These last equations can be used to construct the simplest possible HBT model.

1.4.2 The Gummel Poon Model for HBT

Even though the modeling process in Chapter 2 does not implement the Gummel-Poon model, further development on the model can be considered in future work resorting to the Gummel-Poon HBT characteristics. This is because the Gummel-Poon model incorporates high injection effects by taking into account an HBT model that shows charge control relation connecting junction voltages, collector current, and base charge. The Gummel-Poon model is built based on the Ebers-Moll model described in equation 1.11 approximately equivalent to equation 1.5 and equation 1.4. However, equation 1.11 proposes a dependence of transistor gains on operating currents compared to the Ebers-Moll model.

$$\begin{bmatrix} I_E \\ I_C \end{bmatrix} = \begin{bmatrix} \frac{I_{ES}}{1-\alpha_F\alpha_R} & -\frac{\alpha_R I_{CS}}{1-\alpha_F\alpha_R} \\ -\frac{\alpha_F I_{ES}}{1-\alpha_F\alpha_R} & \frac{I_{CS}}{1-\alpha_F\alpha_R} \end{bmatrix} \begin{bmatrix} e^{\frac{V_{BE}}{V_T}} - 1 \\ e^{\frac{V_{BC}}{V_T}} - 1 \end{bmatrix} \tag{1.11}$$

This charge control relation permits the dominant current components to be obtained without the use of low-injection approximations and high-injection effects in the base region. The Gummel-Pool model (including parasitic effects) is described in figure 1.18. [21]

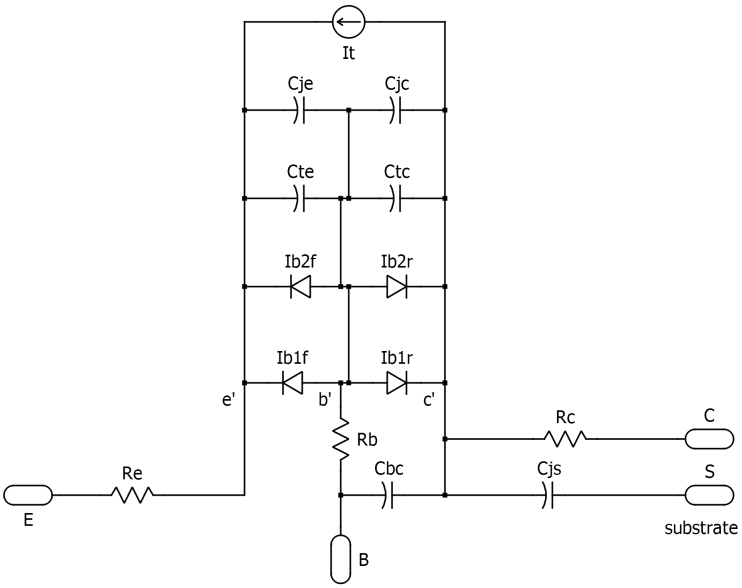

Figure 1.18: Schematic of the Gummel–Poon model of an NPN transistor.

Where:

- $Ib1f$, $Ib1r$ are the ideal diodes in charge of the major current flow.
- $Ib2f$, $Ib2r$ are the leakage diodes whose currents are proportional to the ideal diode current with the setting of the weighing saturation currents.
- $It = (I_{b1r} \cdot \beta_r) - (I_{b1f} \cdot \beta_f)$ where I_{b1r}, I_{b1f} are the currents flows through the ideal diodes, β_r and β_f are the reverse and forward current gain, respectively.

The Gummel–Poon model can be used to describe the basic operation of the transistor as well as to describe non-ideal effects. In the develped model, described in Chapter 2, the only nonlinear effects of the model are the thermal effects and the parasitic effects. Further development on the model, such as the consideration of the Early effect, can be implemented with the help of the Gummel-Poon HBT model.

CHAPTER 2

HBT Modeling with Thermal Variation

This chapter's objective is to present a custom developed HBT model that can take into account thermal effects, namely the current collapse and self-heating effects. The model is based on the Ebers-Moll HBT model with the addition of a thermal port. The Win foundry GaAs HBT model has been considered as a reference to fit the custom model parameters. This model does include thermal effects by itself, however, due to the lack of internal insights into the nonlinear effects in a proprietary model, one of the goals of this thesis was to build a self-designed HBT model that considers significant thermal instability. The model has been developed in Keysight ADS, exploiting an the SDD equation-based component.

2.1 Characteristics of Win's HBT model

The reference technology of this work is Win's H02U HBT process. The foundry Process Design Kit (PDK) for ADS has been adopted to simulate the transistor behavior, as depicted in figure 2.2. The area of the HBT is limited to a certain range of emitter length, emitter width, and finger number as detailed in table 2.1. Only the parameters inside the range would be acceptable for the simulation, as indicated by the verification Status property *"Data_verification"*. This nonlinear model includes the self-heating effect through an internal (default) thermal resistance, but also allows the user to define a custom thermal network thanks to a dedicated thermal pin. According to the device manual, the thermal pin connection modifies the thermal resistance of the GaAs HBT: if the thermal pin is floating, only the internal thermal resistance is considered, while if the thermal pin is connected through a resistance to the ground, this external (thermal) resistance is parallel connected with the internal one, which can be set to a large value if only the external should be considered (parameter $Rtho$). More details will be given in Section 2.2.

Parameter	Numerical value range
Emitter Length	10 µm-40 µm
Emitter Width	2 µm-4 µm
Finger Number	1-4

Table 2.1: Win's Model Parameter Description

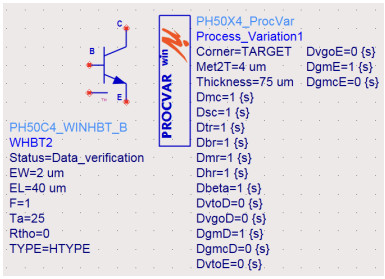

Figure 2.1: Model of Win's HBT

2.1.1 DC simulation

The first simulation aims to find the DC characteristics of the Win's HBTs, to explore the relationship between the collector current and the collector-emitter voltage in figure 2.2. An HBT area of 2 µm·40 µm·1 is selected as case study. With the study of single-finger Win's HBT, the development of a multi-finger model based on the parallel combination of multiple single-finger devices can be realized. An external thermal resistance of 100 Ω has been chosen, as detailed in Section 2.2. Clearly, such a resistance may affect junction temperature, but since the aim of these simulations is to provide data to be fit with the custom model, the effect of the external resistance can be easily taken into account.

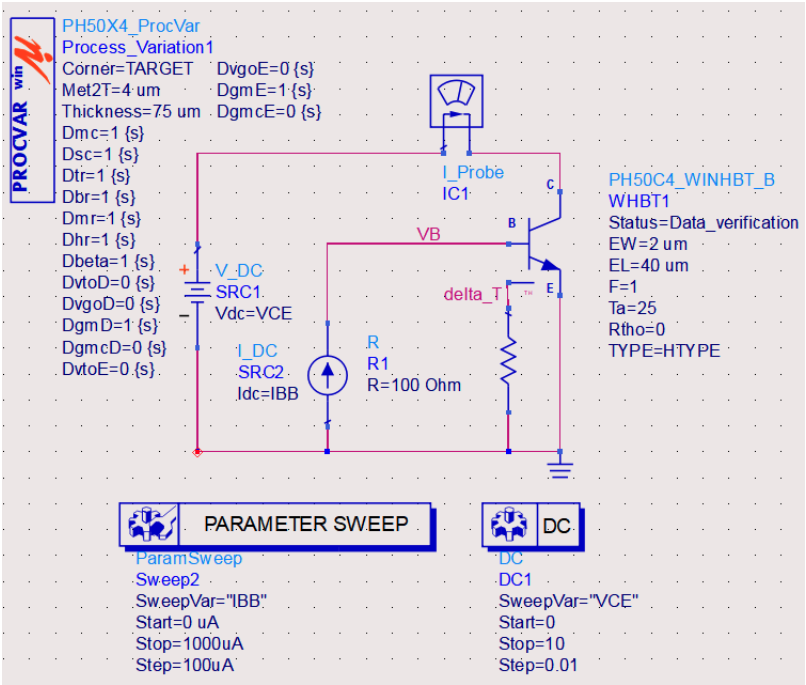

Figure 2.2: DC schematic of Win's HBT.

The base is biased with an ideal current generator and both base and collector DC supplies have been swept as follows:

- the DC voltage V_{CE} from 0 V to 10 V with step 0.01 V.
- the DC current I_{BB} from 0 A to 1 mA with steps of 100 µA.

The DC simulation result is shown in figure 2.3.

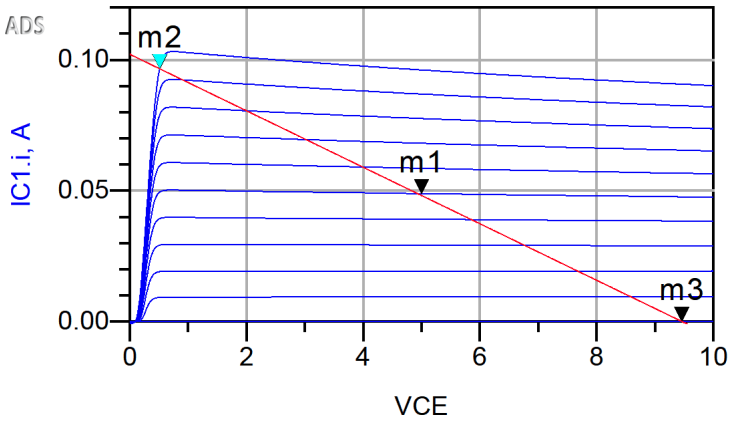

Figure 2.3: DC simulation of Win's HBT.

The breakdown voltage V_{br} is around 14 V, however, the recommended bias for power is 5 V thus the swing to be considered is from 0.5 V (knee voltage, V_{knee}) to 9.5 V. The optimal load for power therefore results in 92.628 Ω. The equation 2.1 is used in the computation.

$$R_{load} = \frac{I_{cmax} - I_{cmin}}{V_{br} - V_{knee}} \tag{2.1}$$

where $I_{cmin} = 0$ and I_{cmax} is the maximum collector current that the transistor can reach.

Marker m1 in figure 2.3 shows the class-A bias point, while equation 2.2 defines the associated quiescent dissipated power $P_{DC,q}$.

$$P_{DC,q} = V_{CE,q} \cdot I_{C,q} \tag{2.2}$$

which is around 250 mW for the selected device.

As expected, due to self-heating the collector current reduces when the collector-emitter voltage increases in the saturation region. According to the DC simulation findings shown in figure 2.3, the collector current in the working zone changes when the collector-emitter voltage increases. The collector current does, however, primarily drop linearly. This is due to the fact that when the collector-emitter voltage rises, the junction temperature rises as well, which alters the mobility of electrons and holes and the junction turn-on voltage.

2.1.2 AC simulation

A biasing point of (V_{CE}=5 V, I_{BB}=500 µA) has been selected based on the definition of a class A power amplifier that operates with a basing point ($V_{CE} = 0.5 \cdot (V_{br} - V_{knee})$, $I_B = 0.5 \cdot (I_{max} - I_{min})$) from figure 2.3. The output port is terminated with the optimum load computed with 2.1, while the input resistance has been tuned to maximize gain and input matching. The AC schematic is shown in figure 2.4. The simulations results include the stability factor (Mu factor) and maximum available gain (MAG) behavior in figure 2.5, and the relationship between the incident and outgoing waves at each of the two gates (S-parameter matrix) in figure 2.6 and figure 2.7.

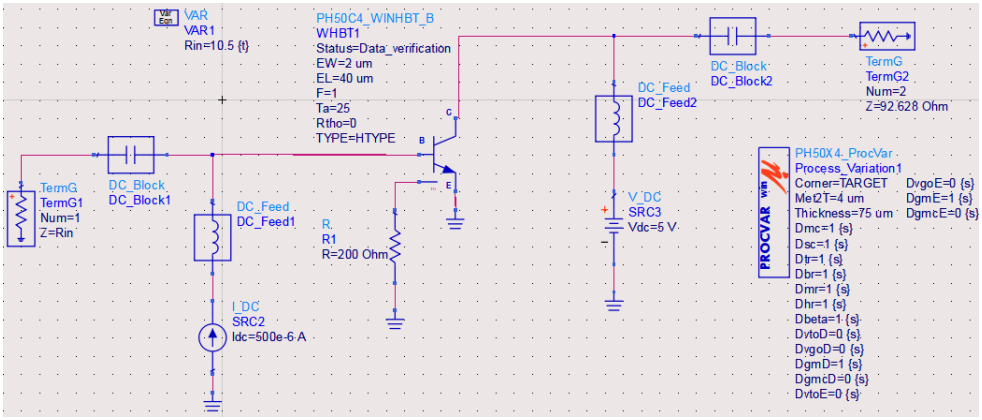

Figure 2.4: AC simulation schematics of Win's HBT.

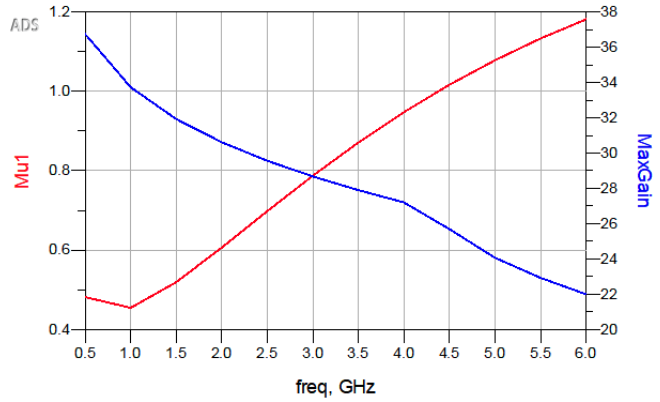

Figure 2.5: Mu factor result and maximum available gain result for Win's HBT.

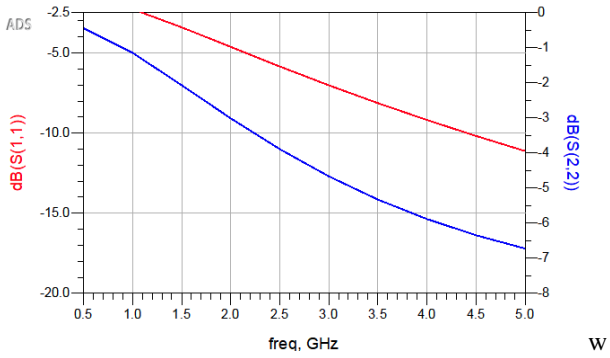

Figure 2.6: S11 and S22 results of Win's HBT.

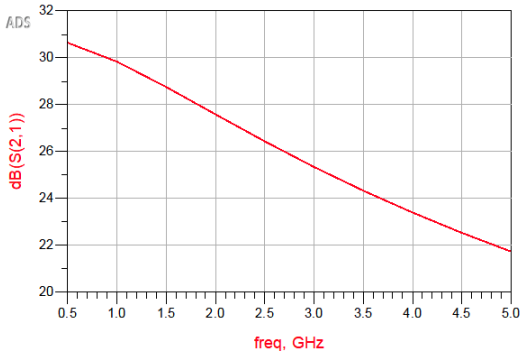

Figure 2.7: S21 result of Win's HBT.

From the results in figure 2.5, the device is not unconditionally stable below 4.4 GHz. The thesis considers a working frequency range around 5 GHz as an interesting frequency for mobile handset applications [22], hence considering the device as unconditionally stable. The inclusion and impact of a stabilization network in the biasing circuit will be considered in future developments.

2.1.3 Harmonic Balance simulation

Analog RF and microwave circuits are typically handled in the frequency domain. A frequency-domain analysis method called Harmonic Balance (HB) is used to simulate nonlinear circuits and systems under large-signal excitation. The HB analysis reported in the following is carried out when the working frequency is 5 GHz, sweeping the input power from -30 dBm to 15 dBm (1 dB step). Figure 2.8 displays the simulation schematic.

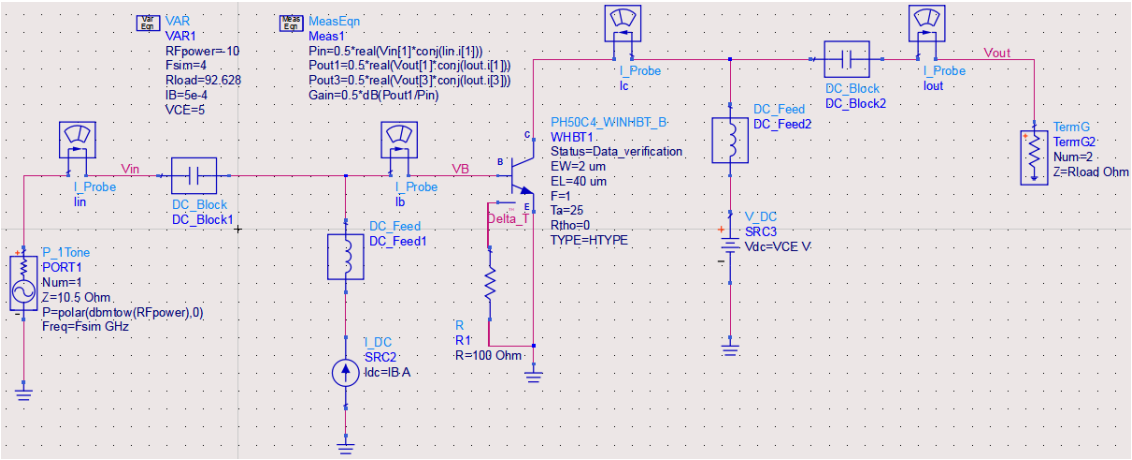

Figure 2.8: HB simulation of Win's HBT.

To the aim of designing a power amplifier the relevant transistor performance to be evaluated are:

- Fundamental output power (P_{out}) and third-order output power in figure 2.9.
- Power gain in figure 2.10.
- HBT junction temperature in figure 2.11.
- DC collector and base currents in figure 2.12.

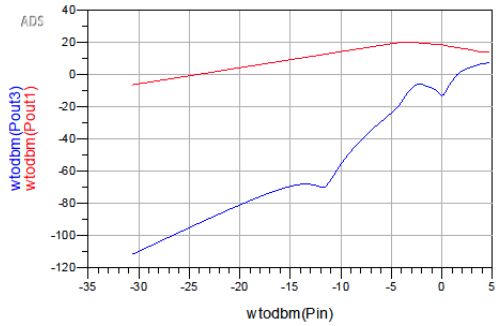

Figure 2.9: Fundamental and third-order output power (dBm) of Win's HBT.

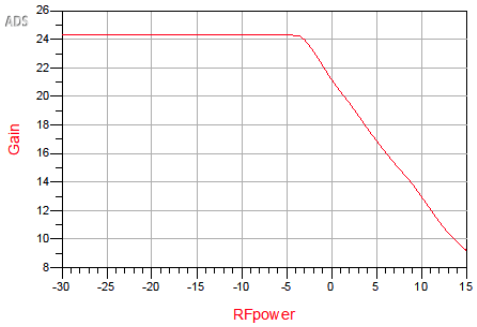

Figure 2.10: Gain (dB) of Win's HBT.

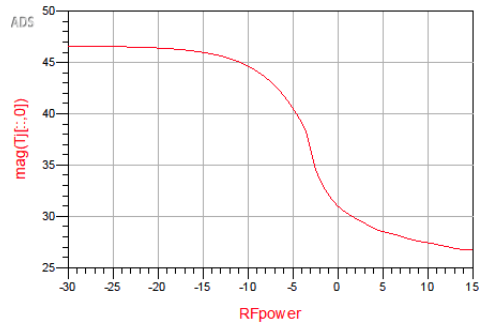

Figure 2.11: Junction temperature (degrees Celsius) of Win's HBT.

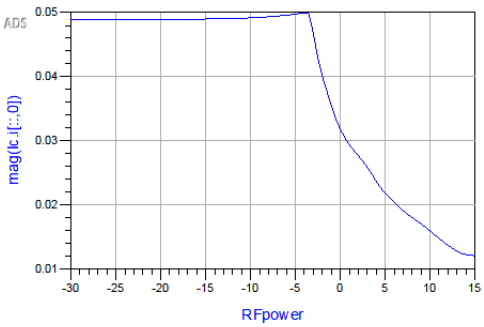

Figure 2.12: Dc currents (A) of Win's HBT

The junction temperature begins to cool down at a certain input power value as expected from a class A power amplifier and the device reaches the expected 20 dBm of output power, but then experiences sudden and sharp compression.

2.2 Thermal pin functionality

To allow the user to define a custom thermal network and/or to monitor the junction temperature, an extra terminal pin (ΔT) is provided. The voltage at the thermal pin is in fact equal to the temperature difference ΔT between the device junction temperature (hot spot) and the ambient temperature (at chip backside), as defined through equation 2.3 and equation 2.4.

$$T_j = T_a + \Delta T \tag{2.3}$$

$$\Delta T = R_{th} \cdot P_{diss} \tag{2.4}$$

Where:

- T_j is the junction temperature inside the transistor.
- T_a is the ambient temperature.
- R_{th} is the thermal resistance.

Internally, the thermal pin can be represented with the circuit in figure 2.13.

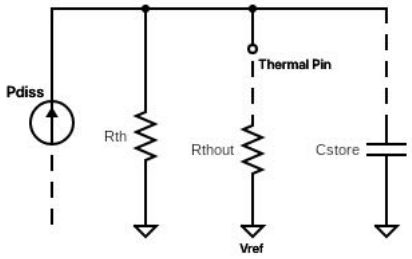

Figure 2.13: Thermal Pin Equivalent Circuit.

- P_{diss} is the dissipated power of the HBT, which is is output as current at the thermal pin if an external resistance is applied.

- R_{th} is the intrinsic (nonlinear) thermal resistance fitted from measurements by the foundry.
- R_{thout} is the extrinsic thermal resistance that the user can add so the total thermal resistance is the parallel of R_{th} and R_{thout}.
- C_{store} is the thermal capacitance, i.e., the element that shows the capability of the device to store a certain amount of heat (energy). The default internal value is zero, thus but it has not been considered in this thesis.
- V_{ref} potential represents the ambient temperature.

Since most of the heat produced at the junction is due to the collector current, in this thesis, the dissipated power P_{diss} is only assumed to be as in equation 2.2.1

$$P_{diss} = V_C I_C \tag{2.5}$$

This is slightly optimistic (best case) since the impact of base current is neglected.

2.2.1 Internal thermal resistance

Investigating how the internal thermal network works in Win's model is an essential step for developing the custom model. First, a diode-connected device with the thermal pin floating as in Figure 2.14 is simulated, to observe the junction temperature variation with bias and ambient temperature.

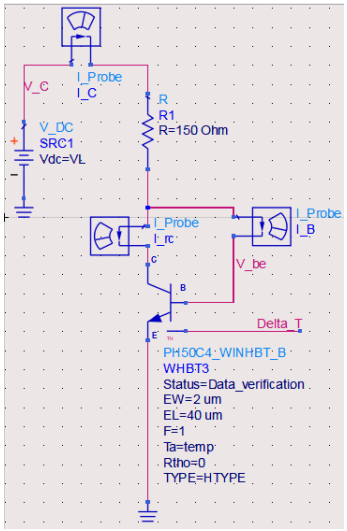

Figure 2.14: Simulation set-up with diode-connected HBT.

With the sweep of the DC supply voltage (V_{DC}) and the ambient temperature (T_a), the results in figure 2.15 and 2.16 are obtained.

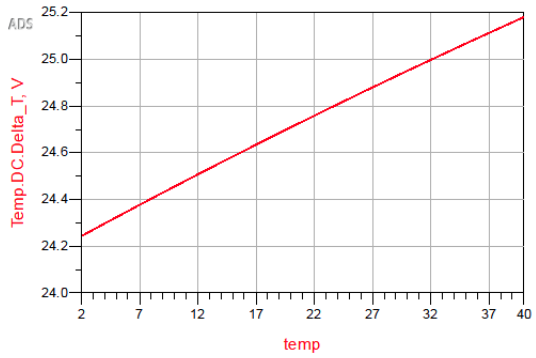

Figure 2.15: Temperature rise ΔT as a function of ambient temperature (V_{DC} =10 V).

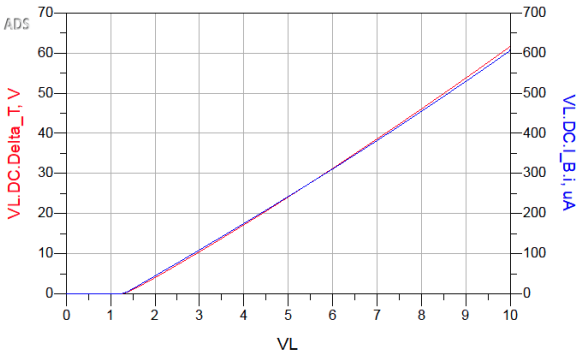

Figure 2.16: Temperature rise ΔT and base current as a function of collector supply voltage (T_a = 20°C).

The result are two aspects according to the different swept parameters:

- Increased ambient temperature: the thermal voltage increases even if the dissipated power stays constant. This can be only due to a relationship between the temperature and the internal thermal resistance, which is therefore not constant.
- Increased DC supply voltage on the collector terminal: the thermal voltage increases quasi-linearly when the DC power supply increases linearly. This proves the proportion relation between the ΔT and the V_{CE} inside equation 2.4 and equation .

In this thesis, a fixed ambient temperature equal to the room temperature has been considered. That is, the relationship between the temperature and the thermal resistance has been neglected but will be the object of future developments. In the next sections, the value of the internal Win's model thermal resistance will be derived from simulations, as well as its relationship with the area of the transistor.

2.2.2 Evaluation of thermal resistance at room temperature

The simulation set-up for the evaluation of the thermal resistance in Win's model, accounts for the following aspects:

- A class A power amplifier is considered as a worst-case from the thermal stand-point.
- The relationship between the temperature and thermal resistance is ignored, therefore, the ambient temperature is set at room temperature 25°C.
- The case study HBT with area 2 µm·40 µm·1 is considered, while the relationship between the HBT area and thermal resistance will be explored later on.
- The dissipated power is calculated through equation 2.2.1.
- The thermal pin should be either floating or connected to a high-valued resistance so that the dominant resistance is the internal one in the parallel-resistance network. In the latter case the dissipated power can be directly evaluated as the current flowing in the external resistance.

The circuits in figure 2.17 and figure 2.18 are being simulated to find out the internal thermal resistance. The DC simulator sweeps the DC supply voltage (V_L in the schematics). In the case of figure 2.17, where the thermal pin is floating, the dissipated power is calculated through the equation 2.2.1. To calculate the thermal resistance for both schematics, equation 2.6 is used.

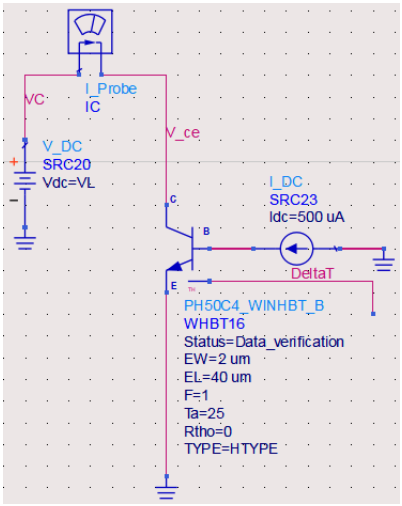

Figure 2.17: Circuit to estimate the internal thermal resistance when the thermal pin is floating

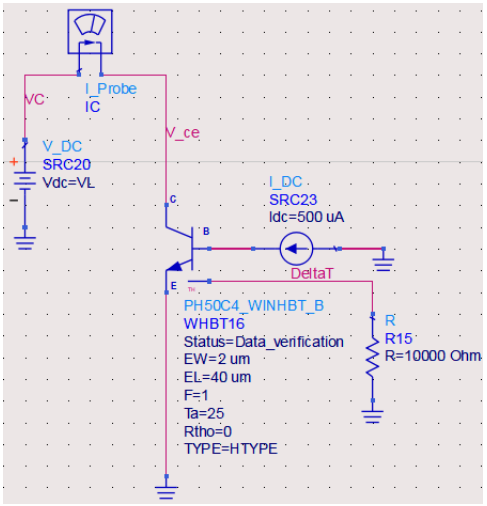

Figure 2.18: Circuit to estimate the internal thermal resistance when a large resistance is connected to the thermal pin

$$R_{thtot} = \frac{DeltaT}{P_{diss}} \tag{2.6}$$

If the schematic with external thermal resistance is used, the internal resistance is calculated through equation 2.7 due to the parallel connection between $R_{th(in)}$ and $R_{th(out)}$.

$$R_{th(in)} = \frac{R_{thtot} R_{th(out)}}{(R_{thtot} + R_{th(out)})} \tag{2.7}$$

The simulation results plot the P_{diss} and $R_{th(in)}$ value shown in figure 2.19. Note that plots of $Rth0$ and $Power\_diss$ shows the result for schematic in figure 2.18 and $Rth1$ and $Power\_diss1$ for floating thermal pin.

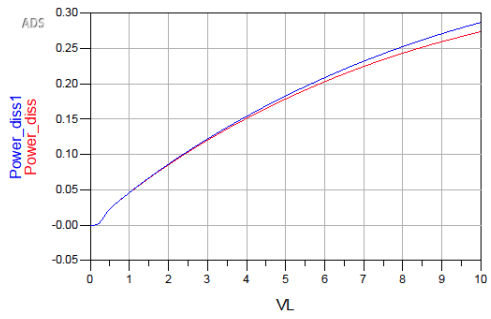

Figure 2.19: Dissipated power versus bias.

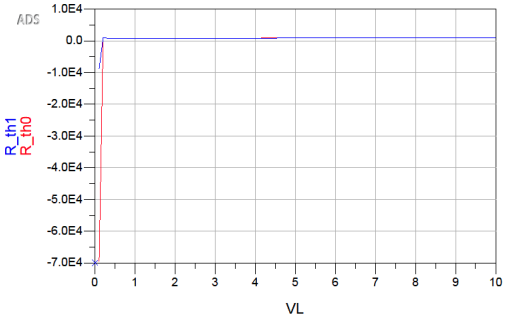

Figure 2.20: Internal thermal resistance versus bias.

The internal thermal resistance for Win's HBT with area=80 μm^2 is

$$R_{th(in)} = 880\,\Omega$$

There is less than 10 Ω difference for thermal resistance results obtained with schematics 2.17 and 2.18, due to the fact that the calculation of the dissipated power from the collector current only (equation 2.2.1) is optimistic.

Relationship between thermal resistance and HBT size

The area of the transistor can be defined in equation 2.8.

$$A_{HBT} = L_E W_E N_f \tag{2.8}$$

where the L_E stands for the length of the emitter, W_E stands for the width of the emitter, N_f stands for the number of fingers. Therefore, the simulations presented above for calculating the thermal resistance for HBT area=80 μm^2 are repeated for different HBT area values, wihtin the allowed values according to table 2.1. The results for the thermal resistance are listed in table 2.2. It is worth noticing that Wins's model gives the same results for different device geometries with the same area (e.g., 2x40x1 μm^2 and 4x20x1 μm^2 HBTs). The

Area (pm^2)	$R_{th(internal)}$	Area (pm^2)	$R_{th(internal)}$	Area (pm^2)	$R_{th(internal)}$	Area (pm^2)	$R_{th(internal)}$
480	414.188	468	419.15	456	424.302	444	429.656
...	...	...	...	...	...	...	...
156	578.572	152	585.68	148	593.067	144	600.752
...	...	...	...	...	...	...	...
360	474.158	348	481.767	3336	489.775	324	498.203
...	...	...	...	...	...	...	...
117	797.088	114	806.878	111	817.0520	108	827.638
...	...	...	...	...	...	...	...
320	414.188	312	419.15	304	424.302	296	429.656
...	...	...	...	...	...	...	...
104	699.889	100	1712.875	96	726.642	92	741.273
...	...	...	...	...	...	...	...
240	571.726	234	578.572	228	585.680	222	593.067
...	...	...	...	...	...	...	...
78	967.724	72	1004.508	66	1046.063	60	1093.537

Table 2.2: Thermal resistance values for different transistor areas.

values of table 2.2 are all imported to the Python code to model the mathematical relationship between the thermal resistance and the area of the transistor: the trend for thermal resistance when the HBT area varies is shown in figure 2.21.

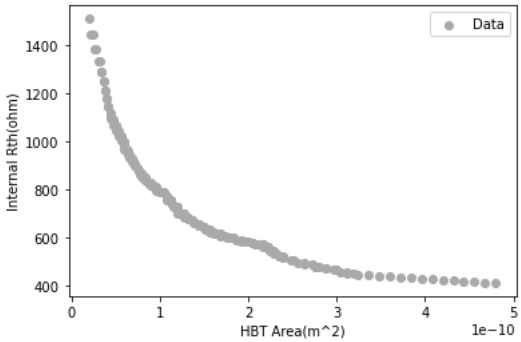

Figure 2.21: Thermal resistance as a function of transistor area.

To model this trend properly in mathematics, four different mathematical functionalities have been tested:

- Exponential fit: $R_{th} = ae^{-bA_{HBT}} + c$
- Logarithmic fit: $R_{th} = d \log A_{HBT} + f$

- Reciprocal fit: $R_{th} = \frac{h}{iA_{HBT}} + j$
- Power law fit: $R_{th} = \frac{m}{A^n_{HBT}}$

As shown in figure 2.22, all these functions show a similar trend to that of the samples with proper choice of fitting coefficients (a, b, c, d, f, h, i, j, m, n).

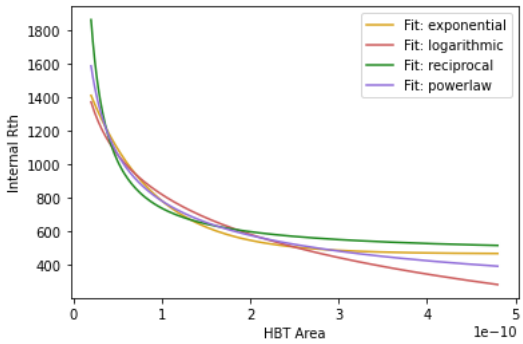

Figure 2.22: The thermal resistance VS transistor area data compared to the candidate mathematical models.

The following Python code has been developed to compute coefficient values:

```
def func(x, a, b, c):
    return a   np.exp(-b   x) + c
params, _ = curve_fit(func, x_data, y_data)
a, b, c= params

def func(x, d, f):
    return d   np.log(x) + f
params, _ = curve_fit(func, x_data, y_data)
d, f = params

def func(x, h, i, j):
    return ( h / (i   x) ) + j
params, _ = curve_fit(func, x_data, y_data)
h, i, j = params

def func(x, m, n):
    return m / np.power(x, n)
params, _ = curve_fit(func, x_data, y_data)
m, n = params

print(f'a= {a}; b= {b}; c={c}')
print('\n'f'd= {d}; f= {f};')
print('\n'f'h= {h}; i= {i}; j= {j};')
print('\n'f'm= {m}; n = {n};''\n')

y_exponential = a   np.exp(-b   x_data) + c
y_logarithmic =   np.log(x_data) + f
y_reciprocal = ( h / (i   x_data) ) + j
y_powerlaw = m / np.power(x_data, n)

# Number set print to see the difference directly
A = np.column_stack((x_data, y_data, y_exponential, y_logarithmic, y_reciprocal, y_powerlaw
    ))
```

The fitting of each function was defined according to the **root-mean-square error**:

```
def rmse(actual, pred):
```

```
    actual, pred = np.array(actual), np.array(pred)
    return np.sqrt(np.square(np.subtract(actual,pred)).mean())

error_expoential = rmse(y_data, y_exponential)
error_logarithmic = rmse(y_data, y_logarithmic)
error_reciprocal = rmse(y_data, y_reciprocal)
error_ppowerlaw = rmse(y_data, y_powerlaw)
```

The best function to describe the relationship between the HBT area and the thermal resistance is the power law equation as shown in figure 2.23.

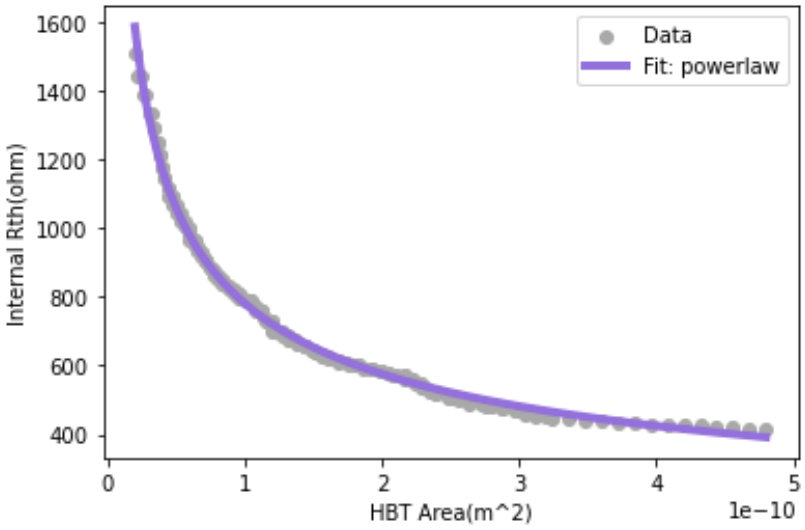

Figure 2.23: Power law fit.

The fitting coefficients are found to be:

$$R_{th(win)} = \frac{0.030954}{A_{HBT}^{0.440182}}$$

2.3 Custom-developed HBT model

Due to the paramount importance of the thermal aspects in HBTs, a self-designed GaAs HBT device model is developed to have detailed insights and control of the nonlinear thermal effects as well as the flexibility to easily switch to an ideal HBT (without self-heating) for fast comparison. The main features of the model are:

- The model follows the Ebers-Moll mathematical relationships representing the behavior of a GaAs HBT.
- The model includes a boolean parameter (flag) to include or exclude the self-heating effect.
- The model is developed for a 1-finger device and includes a thermal pin. In this way the behavior of multi-finger devices, including thermal effects, can be easily obtained with the combination of multiple unit cells.

2.3.1 Symbolically Defined Device (SDD) component in ADS

The symbolically-defined device (SDD) is an equation-based component that enables the user to define custom components. These components are multi-port devices that can be modeled directly on a schematic. The user

defines an SDD by specifying equations that relate port currents, port voltages, and their derivatives. Equations can also reference the current flowing in another device. Once defined, a model can be used with any circuit simulator in ADS. Taking inspiration from Win's model, the most flexible way to include thermal effects is the use of a dedicated thermal pin. Thus the model has the four-port symbol in figure 2.24. The parameter **ThermalModel_Flag** works as the flag to include the thermal effect in the self-designed HBT. The basic HBT behavior is described with the Ebers-Moll (EB) model, as detailed in the following.

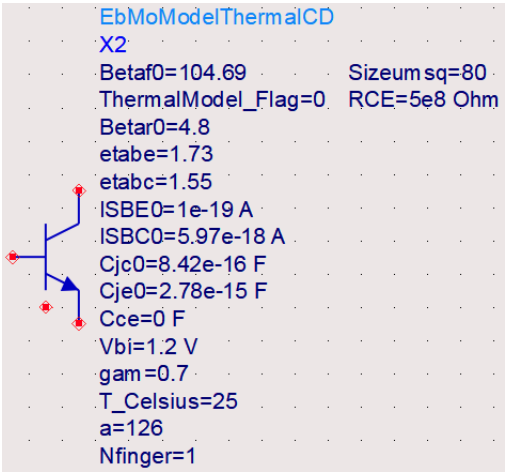

Figure 2.24: Symbol of the custom Ebers-Moll HBT Model.

The procedures for building the model are explained in detail as follows:

1. Implementation of the ideal Ebers-Moll model following equations 1.4 and 1.5.
2. Inclusion of the junction capacitances and output impedance.
3. Inclusion of the breakdown voltage.
4. Inclusion of the thermal behavior.

Implementation of the Ebers-Moll model in SDD As shown in Section 1.3, the EB models separate the parasitic resistance and capacitance from the collector and emitter current generators, which are described within the SDD component by equations 2.9 and 2.10.

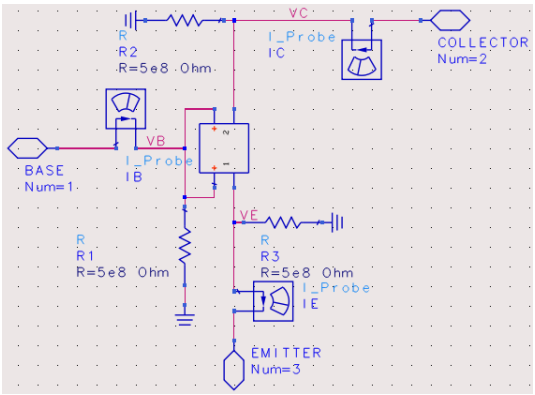

Figure 2.25: Ebers-Moll HBT Model with two-port SDD

$$\_i1 = (Sizeumsq \cdot Nfinger) \cdot \left(I_{SBE} \left(e^{\frac{\_v1}{V_T \cdot etabe}} - 1 \right) - alphar \cdot I_{SBC} \left(e^{\frac{\_v2}{V_T \cdot etabc}} - 1 \right) \right) \tag{2.9}$$

$$\_i2 = (Sizeumsq \cdot Nfinger) \cdot \left(I_{SBC} \left(e^{\frac{\_v2}{V_T \cdot etabc}} - 1 \right) - alphaf \cdot I_{SBE} \left(e^{\frac{\_v1}{V_T \cdot etabe}} - 1 \right) \right) \tag{2.10}$$

Where:

- $\_i1$ and $\_i2$: the base and emitter current, respectively.
- $\_v1$ and $\_v2$: the voltage between the base and the emitter and the voltage between the base and the collector, respectively.
- Sizeumsq is the emitter width (E_W) times the emitter length (E_L), i.e. the area of the emitter. Nfinger is the number of fingers inside the HBT.
- I_{SBE}, I_{SBC}: the saturation current for the base-emitter junction and the base-collector junction, respectively.
- V_T: the thermal voltage, computed as $\frac{25.9e-3 \cdot (T_A + 273.15)}{300.15}$ where T_A is the ambient temperature.
- $betar$ and $betaf$: the forward and reverse common-emitter current gains.
- $alphar$ and $alphaf$: the forward and reverse common-base current gains, that are calculated through $\frac{betar}{betar+1}$ and $\frac{betaf}{betaf+1}$, respectively.
- $etabc$ and $etabe$: diode ideality factors. In equations 1.4 and 1.5, they are equal to 1 (ideal diodes), but in the custom model these parameters have been added to allow for turn-on voltage adjustments.

Inclusion of the junction capacitances and output impedance in SDD The second step is to consider the implementation of parasitic capacitances and resistances inside the HBT that can affect its behavior. The internal capacitances and resistances adopted in compact HBT models are listed in table 2.3.

C_{bc}, C_{be}	The parasitic capacitor due to the transistor junctions
C_{ce}, R_{ce}	The output capacitance and resistance parallel connected

Table 2.3: Internal capacitances and resistances.

Since C_{ce} is constant, it can be directly modeled adding a lumped capacitor in parallel to a lumped resistor R_{ce} between the collector and the emitter in figure. The junction capacitances C_{be} and C_{bc} are instead nonlinear functions of V_{BE} and V_{BC}. Therefore, they have been implemented through the nonlinear equations 2.11 and 2.12.

$$\begin{aligned} if \quad & \_v1 < \gamma_1 V_{bi} \quad then \quad C_{je} = \frac{C_{je0}}{\sqrt{1 - \_v1/V_{bi}}} \\ else \quad & C_{je} = C_{je0} \cdot \left(\frac{1}{\sqrt{1-\gamma_1}} + \left(\frac{1-\gamma_1}{2V_{bi}} \right)^{-1.5} \cdot (\_v1 - \gamma_1 V_{bi}) \right) \end{aligned} \tag{2.11}$$

$$\begin{aligned} if \quad & \_v2 < \gamma_1 V_{bi} \quad then \quad C_{jc} = \frac{C_{jc0}}{\sqrt{1 - \_v2/V_{bi}}} \\ else \quad & C_{jc} = C_{jc0} \cdot \left(\frac{1}{\sqrt{1-\gamma_1}} + \left(\frac{1-\gamma_1}{2V_{bi}} \right)^{-1.5} \cdot (\_v2 - \gamma_1 V_{bi}) \right) \end{aligned} \tag{2.12}$$

Where:

- γ_1 is the fraction of Vbi where starts linear capacitance approximation which should be less than 1.
- V_{bi} is the build-in voltage for capacitance dependency on the voltage which is usually 0.7 V.

- C_{jc0} and C_{je0} are the base-collector junction capacitance and base-emitter junction capacitance under zero voltage.

The junction capacitances contribute to the emitter and base currents in equations 2.9 and 2.10 with a term proportional to the derivatives of the junction voltages (_$v1$ and _$v2$). To compute this derivative, two extra ports defined by equations _$v3 = \dot{_v1}$ and _$v4 = \dot{_v2}$ are introduced in the SDD, along with equations 2.13 and 2.14, obtaining the circuit shown in figure 2.26.

$$\_i1 = (Sizeumsq \cdot N finger) \cdot \left(I_{SBE} \left(e^{\frac{\_v1}{V_T \cdot etabe}} - 1 \right) - alphar \cdot I_{SBC} \left(e^{\frac{\_v2}{V_T \cdot etabc}} - 1 \right) \right) + \\ +(Sizeumsq \cdot N finger) \cdot C_{je} \cdot \dot{\_v3} \tag{2.13}$$

$$\_i1 = (Sizeumsq \cdot N finger) \cdot \left(I_{SBC} \left(e^{\frac{\_v2}{V_T \cdot etabc}} - 1 \right) - alphaf \cdot I_{SBE} \left(e^{\frac{\_v1}{V_T \cdot etabe}} - 1 \right) \right) + \\ +(Sizeumsq \cdot N finger) \cdot C_{jc} \cdot \dot{\_v4} \tag{2.14}$$

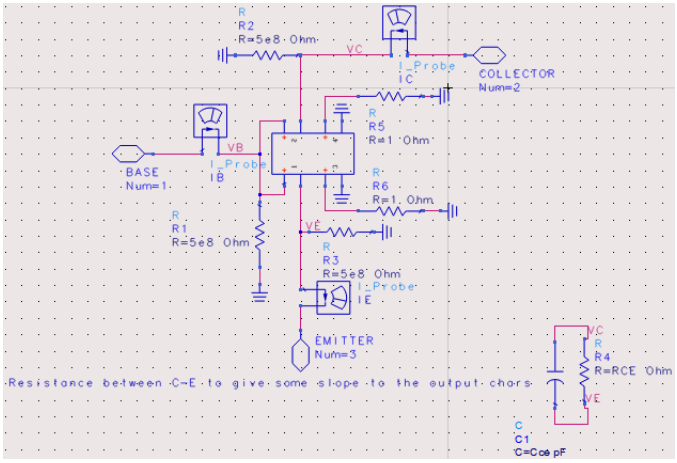

Figure 2.26: Four-port SDD Ebers-Moll HBT model.

Inclusion of the breakdown voltage in SDD The third step is to introduce the breakdown voltage into the model. The transistor behavior can be defined by two different equations depending on the working region. However, the two functions should be continuous at the breakdown voltage. From spice reference [23], the collector and emitter currents can be rewritten as in equation 2.13 and 2.10 where $Area = (Sizeumsq \cdot N finger)$.

$$\_i1 = \begin{cases} Area \cdot \left(I_{SBE} \left(e^{\frac{\_v1}{V_T \cdot etabe}} - 1 \right) - alphar \cdot I_{SBC} \left(e^{\frac{\_v2}{V_T \cdot etabc}} - 1 \right) + C_{je} \cdot \dot{\_v1} \right), & \text{if } V_{CE} \leq V_{BD} \\ Area \cdot \left(I_{SBE} \left(e^{\frac{\_v1}{V_T \cdot etabe}} - 1 \right) - alphar \cdot I_{SBC} \left(e^{\frac{\_v2}{V_T \cdot etabc}} - 1 \right) + C_{je} \cdot \dot{\_v1} \right) \cdot e^{\frac{V_{CE} - V_{BD}}{10^{-3} \cdot \eta_{bc}}}, & \text{if} V_{CE} > V_{BD} \end{cases} \tag{2.15}$$

$$\_i2 = \begin{cases} Area \cdot \left(I_{SBC} \left(e^{\frac{\_v2}{V_T \cdot etabc}} - 1 \right) - alphaf \cdot I_{SBE} \left(e^{\frac{\_v1}{V_T \cdot etabe}} - 1 \right) + C_{jc} \cdot \dot{\_v2} \right), & \text{if } V_{CE} \leq V_{BD} \\ Area \cdot \left(I_{SBC} \left(e^{\frac{\_v2}{V_T \cdot etabc}} - 1 \right) - alphaf \cdot I_{SBE} \left(e^{\frac{\_v1}{V_T \cdot etabe}} - 1 \right) + C_{jc} \cdot \dot{\_v2} \right) \cdot e^{\frac{V_{CE} - V_{BD}}{10^{-3} \cdot \eta_{be}}}, & \text{if} V_{CE} > V_{BD} \end{cases} \tag{2.16}$$

Where V_{CE} is the voltage between the emitter and the collector which can be defined as $V_{BE} - V_{BC} = \_v1 - \_v2$, while V_{BD} is the breakdown voltage. The implementation of the breakdown voltage can be added to the port definition through the equations shown in figure 2.27.

```
F[1,0]=(Sizeumsq*Nfinger)*(ISBE*(exp(_v1/(VT*etabe))-1)-alphar*ISBC*(exp(_v2/(VT*etabc))-1))*(VCE<=VDSS)-_i1
F[1,0]=(Sizeumsq*Nfinger)*(ISBE*(exp(_v1/(VT*etabe))-1)-alphar*ISBC*(exp(_v2/(VT*etabc))-1))*(exp((VCE-VDSS)/(10e-3*etabc)))*(VCE>VDSS)-_i1
F[2,0]=(Sizeumsq*Nfinger)*(ISBC*(exp(_v2/(VT*etabc))-1)-alphaf*ISBE*(exp(_v1/(VT*etabe))-1))*(VCE<=VDSS)-_i2
F[2,0]=(Sizeumsq*Nfinger)*(ISBC*(exp(_v2/(VT*etabc))-1)-alphaf*ISBE*(exp(_v1/(VT*etabe))-1))*(exp((VCE-VDSS)/(10e-3*etabc)))*(VCE>VDSS)-_i2
F[1,0]=(Sizeumsq*Nfinger)*Cje*_v3*(VCE<VDSS)-_i1
F[1,0]=(Sizeumsq*Nfinger)*(Cje*_v3)*(exp((VCE-VDSS)/(10e-3*etabc)))*(VCE>VDSS)-_i1
F[2,0]=(Sizeumsq*Nfinger)*Cjc*_v4*(VCE<VDSS)-_i2
F[2,0]=(Sizeumsq*Nfinger)*(Cjc*_v4)*(exp((VCE-VDSS)/(10e-3*etabc)))*(VCE>VDSS)-_i2
I[3,1]=_v1
I[4,1]=_v2
```

Figure 2.27: HBT model equations considering the breakdown voltage $VDSS$.

Inclusion of thermal effects

To model the nonlinear thermal effect, the parameters that can be affected by the junction temperature, i.e. the thermal voltage, the current gains, and the saturation currents (see table 2.4), have to be modified further.

First recall (see Section 1.4) that in case of base-emitter junction forward biased the collector current can be expressed as in equation 2.17.

$$I_C = I_S \cdot \left(e^{\frac{V_{BE}}{V_T}} - 1 \right) \tag{2.17}$$

Where the saturation current I_S is given by equation 2.18.

$$I_S = \frac{Aq^2 n_i^2 D_n}{Q} \tag{2.18}$$

Where:

- A: the area of the junction.
- q: the electron charge.
- D_n: the electrons diffusion constant (NPN transistor).
- Q: the total charge of uncompensated acceptors per unit area of the base layer.
- n_i: intrinsic carrier density.
- V_γ: the bandgap voltage of the semiconductor for the emitter and base regions.

The intrinsic concentration is proportional to temperature as in equation 2.19.

$$n_i^2 \propto e^{\frac{-V_\gamma}{V_T}} \tag{2.19}$$

Therefore, the collector current is proportional to parameters in equation 2.20

$$I_C \propto \left(e^{\frac{V_{BE}-V_\gamma}{V_T}} - e^{\frac{-V_\gamma}{V_T}} \right) \tag{2.20}$$

Starting from these considerations, the relationship between the saturation current and temperature can be thus found to be as in equation 2.21 [23].

$$I_S(T_J) = I_S(T_0) \left(\frac{T_J}{T_0} \right)^b exp \left(\frac{qE_g}{kT_J} \left(\frac{T_J - T_0}{T_0} \right) \right) \tag{2.21}$$

Where $I_S(T_J)$ is the saturation current at temperature T_J, $I_S(T_0)$ is the saturation current at the reference temperature (usually the room temperature 300 K), k is the Boltzmann constant and q is the elementary charge value. Finally, E_g is the band-gap value in eV, and b is a coefficient that must fit the thermal behavior of a specific device.

The variation of the current gain can be instead expressed as in equation 2.22 [23].

$$\beta(T_J) = \beta(T_0)\left(\frac{T_J}{T_0}\right)^a \tag{2.22}$$

Where $\beta(T_J)$ is the current gain at temperature T_J, $\beta(T_0)$ is the current gain at the reference temperature, and a is a coefficient that must fit the thermal behavior of a specific device.

The saturation currents, current gains, and thermal voltage in the SDD have been thus rewritten as temperature-dependent functions as shown in table 2.4, where T_A (usually as 300 K) and ΔT are in Kelvin.

Parameter	Ideal case without thermal effect	Considering the thermal effect
Thermal Flag	0	1
β_r	$Betar0$	$Betar0 \cdot \left(\frac{T_A+\Delta T}{T_A}\right)^a$
β_f	$Betaf0$	$Betaf0 \cdot \left(\frac{T_A+\Delta T}{T_A}\right)^a$
I_{SBE}	$ISBE0$	$ISBE0 \cdot \left(\frac{T_A+\Delta T}{T_A}\right)^b exp\left(\frac{qE_g}{k(T_A+\Delta T)}\left(\frac{\Delta T}{T_A}\right)\right)$
I_{SBC}	$ISBC0$	$ISBC0 \cdot \left(\frac{T_A+\Delta T}{T_A}\right)^b exp\left(\frac{qE_g}{k(T_A+\Delta T)}\left(\frac{\Delta T}{T_A}\right)\right)$
V_T	$V_T(T_A)$	$\frac{V_T(T_A)\cdot(T_A+\Delta T)}{T_A}$

Table 2.4: Parameters defined with and without thermal effect.

In order to compute the junction temperature increase with respect to ambient temperature ΔT, and to provide an additional thermal pin to model thermal coupling among individual HBTs, the final model is a six-port SDD as depicted in figure 2.28.

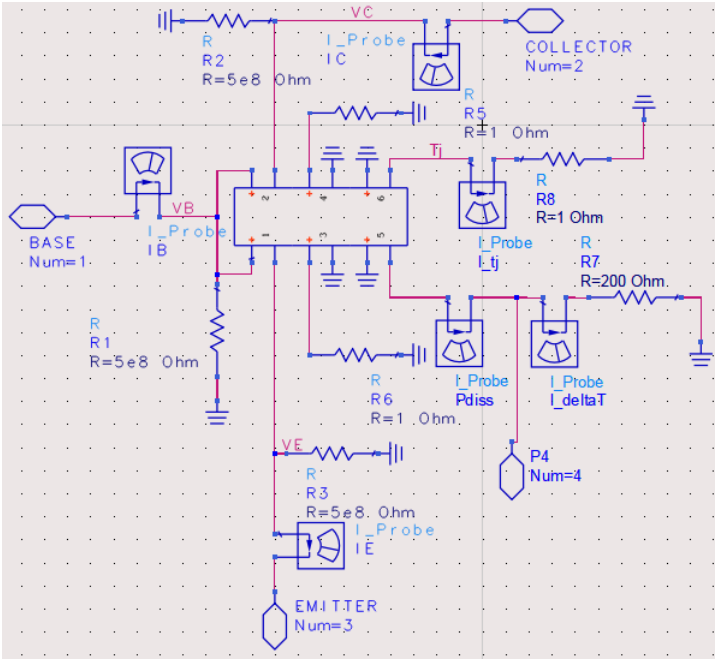

Figure 2.28: Final Ebers-Moll HBT SDD circuit with thermal pin. **Port 1 negative side** and **Port 2 negative side** define the nonlinear emitter and collector currents due to the two junctions. The base terminal is obtained connecting the **Port 1 positive side** and **Port 2 positive side**. **Port 3** and **Port 4** are used to include the nonlinear junction capacitances, while output impedance (not shown here) is a lumped RC network. **Port 5** is used to compute the dissipated power and **Port 6** is the thermal pin.

The current of the first added port the dissipated power, computed according to equation 2.23, and the resistance from this port to ground is the internal thermal resistance. The second added connects in parallel the thermal resistance to the thermal pin ans its voltage represents the junction temperature. The self-heating process is modeled through a low-pass function as shown in equation 2.24.

$$P_{diss} = I_{BC}V_{BC} + I_{BE}V_{BE} = \_v1 \cdot \_i1 + \_v2 \cdot \_i2 \tag{2.23}$$

$$\Delta T = P_{diss} \cdot \frac{1}{1 + j\omega\tau} \cdot R_{th} \tag{2.24}$$

Where the τ is controlled by the cutoff frequency parameter (f_{cutoff}) as described by equation 2.25.

$$\tau = \frac{1}{f_{cutoff} \cdot 2\pi} \tag{2.25}$$

To include the relationship between the area and the thermal resistance found in equation 2.23 equation 2.24 can be modified into equation 2.26.

$$\Delta T = P_{diss} \cdot \frac{0.02165 \cdot (Sizeumsq \cdot Nfinger \cdot 10)^{\frac{-1}{\sqrt{2}}}}{1 + j\omega\tau} \cdot R_{th} \tag{2.26}$$

2.4 Verification of Ebers-Moll model

The custom-made HBT model parameters have been fitted to match the Win's HBT performance. In this section, the consistency between the two model is proved under DC, small-signal and large-signal conditions. The test case single-figner device with area 80 $\mu m^2$is adopted. The thermal resistance is set as 200 Ω both external and internal. The total thermal resistance then, is equal to 100 Ω considered the parallel connection between two thermal resistances, as in the Win's HBT considered in the simulations presented in Section 2.1.

2.4.1 DC simulation

Beyond model fitting to Win's device, DC simulations are also used to demonstrate the functionality of the $Thermal\_Flag$. The same simulation, with V_{CE} swept from 0 V to 10 V with a step of 0.01 V and I_{BB} swept from 0 µA to 1000 µA with a step of 100 µA (see schematic 2.29), is run both with $Thermal\_Flag = 0$ and $Thermal\_Flag = 1$ and for different values of the a and b parameters. The results are shown in figure 2.30, figure 2.31 and figure 2.32. Without self-heating, DC curves are constant above the knee voltage, as in figure 1.6 for an ideal HBT. Accounti for self-heating, instead, the DC current on the collector is no longer constant but it can increase (as in Si HBTs) or decrease (as in GaAs HBTs) according to the sign of the a parameter. In this case, $a = -600$ is the value that best fits the DC curves of the Win's HBT, as proved in in figure 2.33. Calculated through equation 2.1, the optimum load is 86.460 Ω which is also approximately equal to Win's one. The second thermal parameter b has been set to zero in this case, but it can be tuned to further improve models matching.

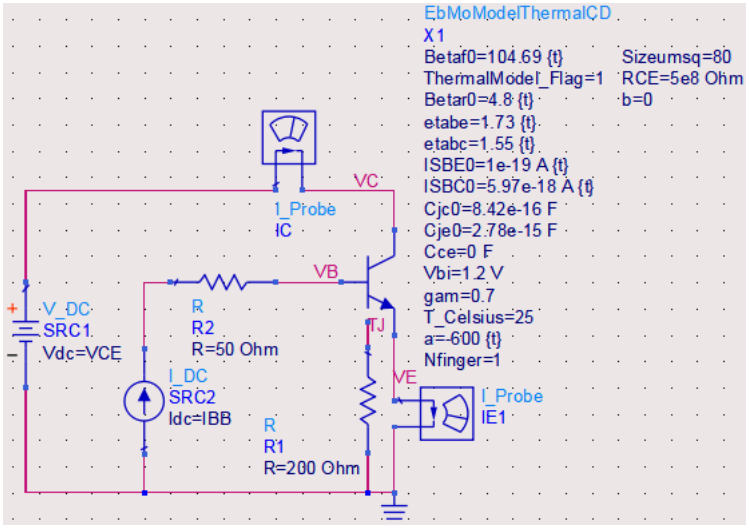

Figure 2.29: Custom-made HBT DC simulation circuit.

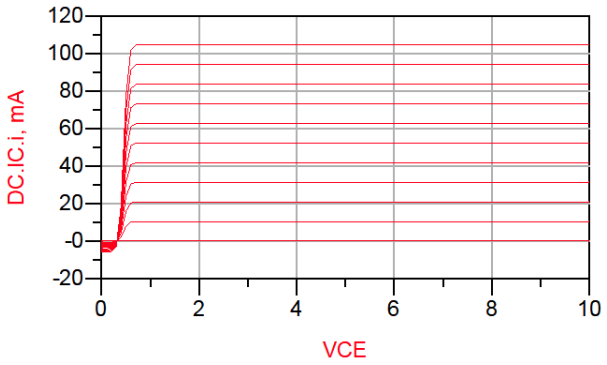

Figure 2.30: Custom-made HBT DC simulation with $Thermal\_Flag = 0$.

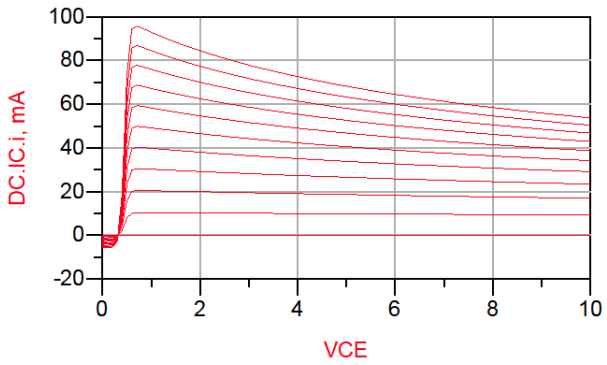

Figure 2.31: Custom-made HBT DC simulation with $Thermal\_Flag = 1$ and negative a value.

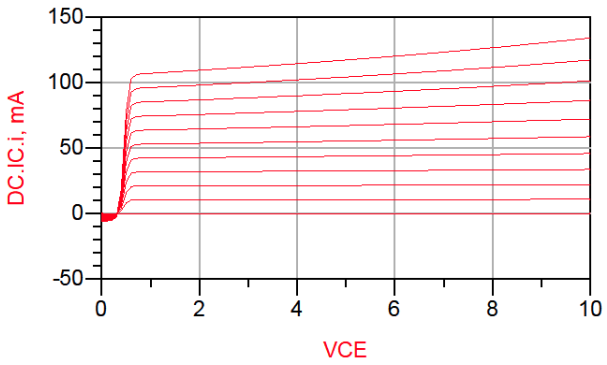

Figure 2.32: Custom-made HBT DC simulation result with $Thermal\_Flag = 1$ and positive a value.

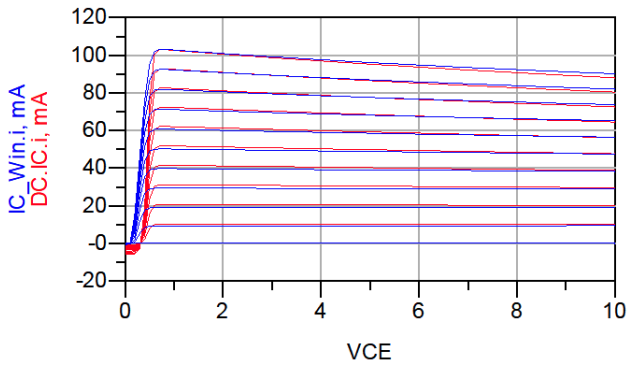

Figure 2.33: DC simulation result for two HBTs models when $a = -600$, where the red curve represents the custom-made model and the blue curve represents Win's

2.4.2 AC simulation

Adopting the same class-A biasing point of V_{CE}=5 V, I_{BB}=500 µA, an AC simulation is used to adjust the values of the parasitic capacitances. With the data from Win's model, the comparison of the custom-made model and Win's model is built in the schematic in figure 2.34. Paramter fitting has been carried out directly in ADS, through the built-in optimizer, with the goal of best the S-parameters approximation. The obtained values for the parameters are summarized in table 2.5.

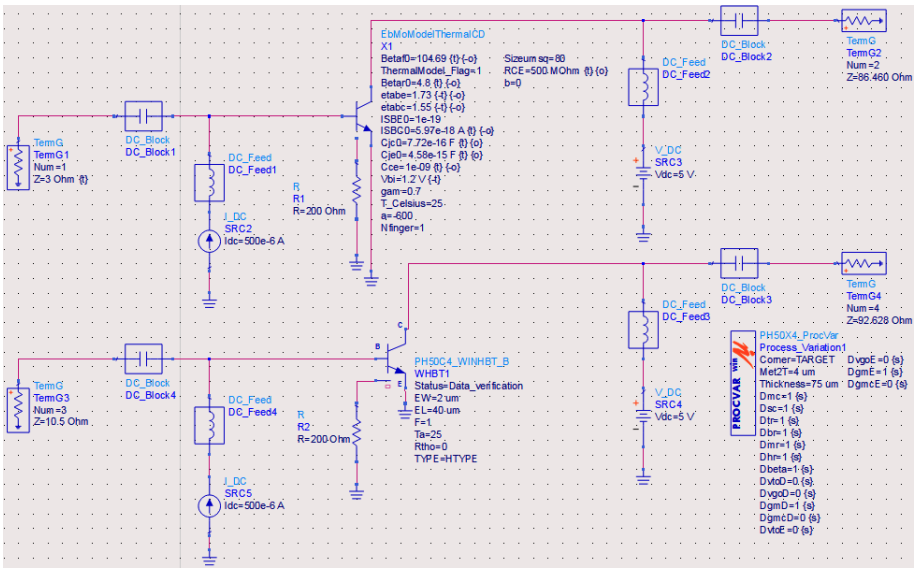

Figure 2.34: Custom-made HBT AC simulation schematic.

Parameter	Value	Parameter	Value
β_{f0}	104.69	β_{r0}	4.8
η_{be}	1.73	η_{bc}	1.55
I_{SBE0}	$10^{-19} A$	I_{SBC0}	$5.97^{-18} A$
C_{jc0}	$8.42^{-16} F$	C_{je0}	$2.78^{-15} F$

Table 2.5: Parameter values after Dc and AC optimization.

2.4.3 Harmonic Balance simulation

Finally the same HB analysis at 5 GHz, sweeping the input power from -35 dBm to 15 dBm (1 dB step) already reported for the Win's model, has been performed with the custom one. Figure 2.35 displays the simulation schematic, while the simulation results reported in the following include:

- Fundamental output power (P_{out}) and third-order output power in figure 2.36.
- Power gain in figure 2.37.
- HBT junction temperature in figure 2.38.
- DC collector and base currents in figure 2.39.

Comparing the results with those reported in Section 2.1.3 for the Win's model demonstrate the good agreement obtained between the to models with the parameters in table 2.5 also in large-signal conditions.

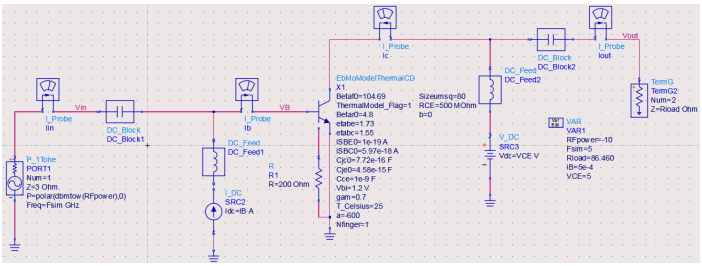

Figure 2.35: Custom-made HBT HB simulation schematic.

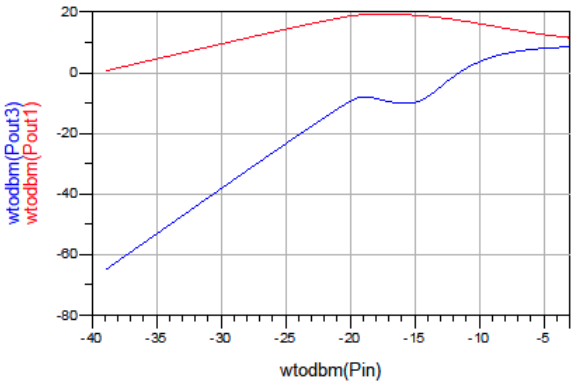

Figure 2.36: Fundamental and third-order output power (dBm) of custom-made HBT model.

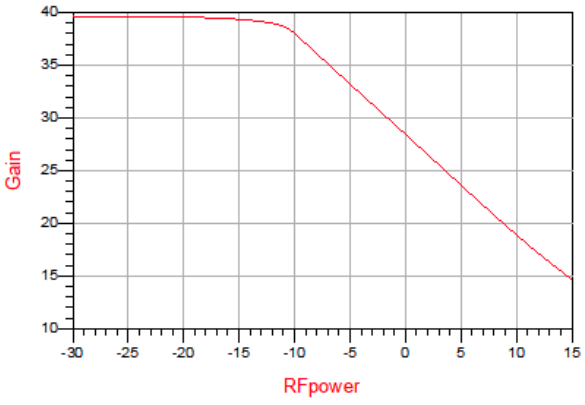

Figure 2.37: Gain (dB) of custom-made HBT model.

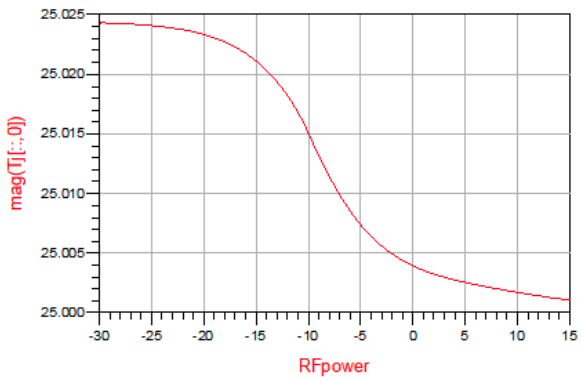

Figure 2.38: Junction temperature (degrees Celsius) of custom-made HBT model.

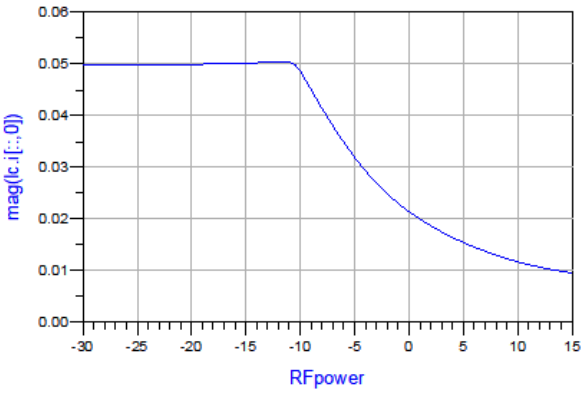

Figure 2.39: Dc currents (A) of custom-made HBT model.

CHAPTER 3

Current mirror biasing circuits

Within the active devices adopted in low-power amplifiers, for example, the operational amplifiers, due to the small size and low dissipation power, the temperature of all the components on the chip is uniform. The increase in the temperature can be ignored. The current mirror is a typical solution to bias the active devices, to set a well-defined DC current. However, considering high current, and high power HBT, the temperature increase effects can not be disregarded. In this chapter, the current mirror biasing networks considering the thermal effect that occurs inside the devices are introduced.

3.1 The biasing networks for HBTs based on the current mirror

3.1.1 Basic current mirror schematics

The current mirror requires two identical HBTs connected in figure 3.1. Based on the fraction operation of collector currents equation in 3.1 and 3.2, the relationship between I_{out} and I_{ref} is shown in equation 3.3.

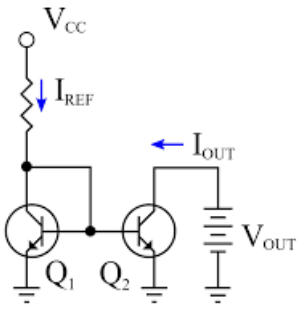

Figure 3.1: Current mirror basic schematics

$$I_{ref} = I_{S1} e^{\frac{V_{be1}}{V_{T1}}} \tag{3.1}$$

$$I_{out} = I_{S2} e^{\frac{V_{be2}}{V_{T2}}} \tag{3.2}$$

$$\frac{I_{ref}}{I_{out}} = \frac{I_{S1}}{I_{S2}} e^{\frac{V_{be1}}{V_{T1}} - \frac{V_{be2}}{V_{T2}}} = \frac{I_{S1}}{I_{S2}} e^{\frac{V_{T2}V_{be1} - V_{T1}V_{be2}}{V_{T1}V_{T2}}} \tag{3.3}$$

Where:

- I_{ref}, I_{out}: I_{ref} is the supplied current, and I_{out} is the mirrored current to be used.
- I_{S1}, I_{S2} are the saturation currents for the two HBTs.
- V_{be1}, V_{be2} are the base-emitter voltages for the two HBTS.
- V_{T1}, V_{T2} are the thermal voltages for the two HBTs, equal to kT/q, where k is Boltzmann's constant, T is the junction temperature in Kelvin, and q is the elementary charge.

In the current mirror schematics, base is connected, so $V_{be1} = V_{be2} = V_{be}$. Therefore, the equation 3.3 can be rewritten as equation 3.4.

$$\frac{I_{ref}}{I_{out}} = \frac{I_{S1}}{I_{S2}} e^{\frac{V_{be}(V_{T2}-V_{T1})}{V_{T1}V_{T2}}} \tag{3.4}$$

When $V_{T1} = V_{T2}$, the junction temperatures of the two HBTs are identically equal. The I_{out} and I_{ref} have a constant ratio that depends only on the ratio between the saturation current in equation 3.5.

$$\frac{I_{ref}}{I_{out}} = \frac{I_{S1}}{I_{S2}} \tag{3.5}$$

However, in the real case, due to the different functionalities of two HBTs in a current mirror, one as the contact DC power supply, and one as the power amplifier transistor, their dissipation powers can be different. In addition, the area of HBTs can be relatively big, so the distances between the two HBTs can not be ignored. The current mirror biasing networks are simulated when all transistors are connected to their individual thermal pin. The transistors can have different temperatures.

3.2 Mathmatical analysis when the temperatures differ

Considering the case when Q1 has junction temperature as T_1 and Q2 has junction temperature as T_2 in figure 3.1, if the temperatures work like the real world case, the condition in equation 3.6 holds.

$$T_1 - T_2 = T_d \tag{3.6}$$

Where T_d is the temperature difference that is not equal to zero. Hence, the ideal case assumes the junction temperature only changes the values of thermal voltage in equation 3.7. The saturation current would not be affected by the junction temperature.

$$V_T = \frac{kT}{q} \tag{3.7}$$

$$V_{Td} = V_{T1} - V_{T2} = \frac{kT_1}{q} - \frac{kT_2}{q} = \frac{kT_d}{q} \tag{3.8}$$

To introduce V_{Td} for the calculation of I_{out}, natural logarithms and reciprocal have been implemented for equation 3.1 and equation 3.2.

$$\frac{1}{\ln \frac{I_{ref}}{I_{S1}}} = \frac{V_{T1}}{V_{be}} \tag{3.9}$$

$$\frac{1}{\ln \frac{I_{out}}{I_{S2}}} = \frac{V_{T2}}{V_{be}} \tag{3.10}$$

Equation 3.9 minus equation 3.10, parameter V_{Td} can be related to I_{out}.

$$\frac{1}{\ln \frac{I_{ref}}{I_{S1}}} - \frac{1}{\ln \frac{I_{out}}{I_{S2}}} = \frac{V_{T1} - V_{T2}}{V_{be}} == \frac{V_{Td}}{V_{be}} \tag{3.11}$$

Due to the logarithm function characteristic $\ln \frac{a}{b} = \ln a - \ln b$.

$$\frac{1}{\ln \frac{I_{ref}}{I_{S1}}} - \frac{1}{\ln \frac{I_{out}}{I_{S2}}} = \frac{\ln_{I_{out}} - \ln I_{ref} + \ln I_{S1} - \ln I_{S2}}{\ln I_{out} \ln_{I_{ref}} + \ln I_{S2} \ln I_{S1} - \ln I_{out} \ln I_{S1} - \ln_{I_{ref}} \ln I_{S2}} \tag{3.12}$$

Considering the case when I_{S1} and I_{S2} are equal.

$$I_{S1} = I_{S2} = I_S \tag{3.13}$$

Equation 3.16 is generated by combination of equation 3.11, 3.12 and 3.13.

$$\frac{V_{Td}}{V_{be}} = \frac{\ln I_{out} - \ln I_{ref}}{\ln I_{out} \ln I_{ref} + \left(\ln I_S\right)^2 - \ln I_{out} \ln I_S - \ln_{I_{ref}} \ln I_S} \tag{3.14}$$

$$\ln I_{out} = \frac{V_{Td} \ln I_S \left(\ln I_{ref} - \ln I_S\right) - V_{be} \ln I_{ref}}{V_{Td} \left(\ln I_{ref} - \ln I_S\right) - V_{be}} \tag{3.15}$$

$$I_{out} = e^{\frac{V_{Td} \ln I_S \left(\ln I_{ref} - \ln I_S\right) - V_{be} \ln I_{ref}}{V_{Td} \left(\ln I_{ref} - \ln I_S\right) - V_{be}}} \tag{3.16}$$

Assume I_{ref} and I_S stay constant when the power amplifier works, two new functions $R(V_{Td})$ and $G(V_{Td})$ are defined to simplify equation 3.16.

$$R(V_{Td}) = V_{Td} \ln I_S \left(\ln I_{ref} - \ln I_S\right) - V_{be} \ln I_{ref} \tag{3.17}$$

$$G(V_{Td}) = V_{Td} \left(\ln I_{ref} - \ln I_S\right) - V_{be} \tag{3.18}$$

Equation 3.15 can be calculated.

$$\frac{\partial \ln I_{out}}{\partial T_d} = \frac{[\ln I_S(\ln I_{ref} - \ln I_S)]G(V_{Td}) - (\ln I_{ref} - \ln I_S)R(V_{Td})}{[V_{Td}(\ln I_{ref} - \ln I_S) - V_{be}]^2} \tag{3.19}$$

If the constants a, b, c are defined in equation 3.20, 3.21 and 3.22.

$$\ln I_{ref} - \ln I_S a \tag{3.20}$$

$$\ln I_S = b \tag{3.21}$$

$$V_{be} = c \tag{3.22}$$

Equation 3.19 can be rewritten as the equation 3.2.

$$\frac{\partial \ln I_{out}}{\partial V_{Td}} = \frac{ab(V_{Td}a - c) - a^2 V_{Td} b + abc - a^2 c}{(V_{Td}a - c)^2} = \frac{-a^2 c}{(V_{Td}a - c)^2} \tag{3.23}$$

The final result is as $\frac{d}{x^2}$ function, where d is a constant. This can be proved through the simulation by changing junction temperature differences for the two HBTs. To simplify the simulation, the thermal pin for two HBTs can connect with a single wire, and ΔT for both HBTs would be the same. Even though it is not realistic, the simulation can now work by setting the different ambient temperatures for two HBTs, as the equivalent way to model the junction temperatures difference when ΔT is the same. The simulation to prove the equation can be further developed for the thesis.

3.3 Current mirror biasing circuit designs

To include the thermal effects for HBTs, two different GaAs HBT models have been used in the following biasing design. They are:

- Win's HBT: considerable thermal effects but lack of the detailed insight view.
- Self-defined HBT in chapter 2: adjustable thermal effects.

Note that in the later schematics, all the simulations are run for both HBTs. But only Self-defined HBT is presented in the figure to show the basing networks' composition. Both models are biased with the same conditions for I_B and V_{CE}. The detailed parameters are listed in table 3.1.

SDD Model		Win's HBT	
I_B	500 µA	I_B	500 µA
I_C	47.97 mA	I_C	48.80 mA
R_{load}	90 Ω	R_{load}	90 Ω
V_{CE}	5.0 V	V_{CE}	5.0 V
$Area(um^2)$	80	$Area(um^2)$	80

Table 3.1: Biasing conditions for SDD HBT and Win's HBT

3.3.1 Resistive biasing circuit as reference

In the schematics 3.2, the simple biasing is constructed using direct DC battery supply (I_B, V_{CE}). This simple biasing network is a comparison to the current mirror biasing networks.

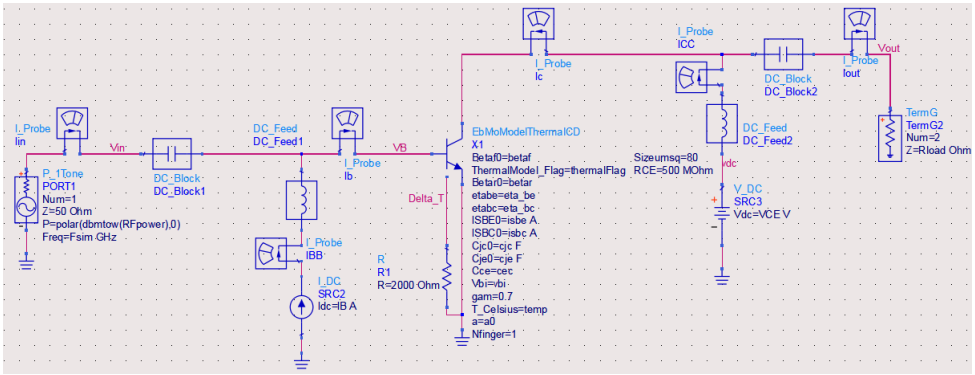

Figure 3.2: Simple resistive biasing circuits for GaAs HBT

The simulations are DC and large signal:

- DC simulation is used to guarantee the same DC working conditions for all biasing networks:
  - DC voltage supply V_{CE} sweeps from 0 V to 10 V with the step of 0.01 V.
  - DC base current supply I_{BB} sweeps from 100 µA to 1000 µA with the step of 100 µA.
  - Ambient temperature for the transistor sweeps from 1° to 40° with the step of 1°.
- Large signal simulation is used to compare the performance of the power amplifier with different biasing networks:
  - Working frequency $F_{sim} = 5$ GHz.

– Harmonic orders $Order$ =5.

– Input radio frequency power RF_{power} sweeps from −30 dBm to 20 dBm with the step of 1 dBm.

There are two different current mirror-biasing networks proposed. The details and the simulation results are listed in the following sections.

3.3.2 Simple current mirror biasing network with base ballasting resistance

As mentioned in Chapter 2, the ballasting resistances are a simple method to avoid current collapse. Based on the basic current mirror in figure 3.1, base ballasting resistors are connected between the two transistors to minimize the current collapse effects for both the HBTs. However, the two collector currents have a ratio related to the saturation currents, which, in the ideal case, is decided by the area of the transistors. With the different areas setting of Q1 and Q2 in figure 3.3, the collector current for Q1 can be mirrored to Q2 with a certain multiplication factor related to the area ratio, thus, the efficiency would be remarkable for the device. In Chapter 2, it is proved that the ballasting resistance value is also related to the area of the transistors. It is essential, therefore, that the resistance numerical values ratio be consistent with the area ratio of the two transistors. Figure 3.3 shows the current mirror schematics with the base ballasting resistances. The two transistors have the area ratio as A and the ballasting resistances ratio is $\frac{1}{A}$. As a result, figure 3.4 has the schematics based on the current mirror biasing circuit with the base ballasting resistances for both of the two transistors. 2

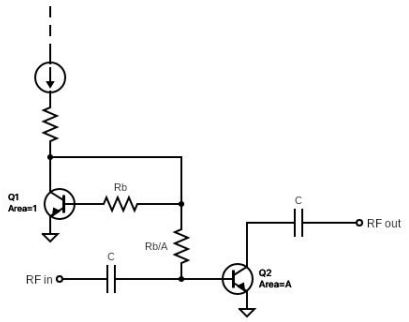

Figure 3.3: Current mirror with base ballasting resistance

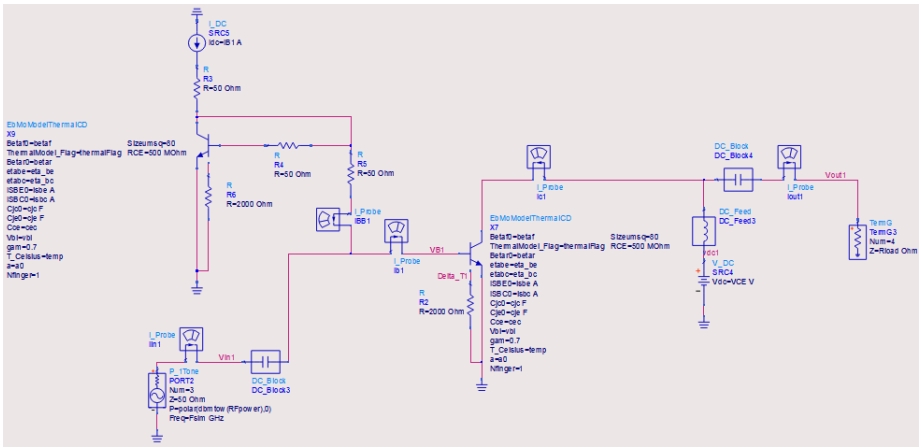

Figure 3.4: Power amplifier biased with current mirror concerning the base ballasting resistance

Compared to the simple resistive biasing network, this power amplifier (Q2) collector current in DC would be related to the collector current on the biasing transistor (Q1). It is hence more stable against variations in temperature. Nonetheless, the two bipolar transistors must be adjacent to one another on the layout domain in order for this biasing circuit to be implemented correctly since they need to be at precisely the same temperature [12]. Additionally, the power amplifier's base's ability to feed current is limited by the ballasting resistance of the base. For a power amplifier that needs a large biasing current, the bias circuit's current driving capacity is particularly crucial.

3.3.3 Advanced current mirror biasing network with current driver transistor

If the high base current should be introduced for the large-size power amplifiers, the additional bipolar transistor working as the base current-driven transistor can be implemented to have an extra base current supply as in figure 3.5. The new biasing network with the current-driven transistor is based on the current mirror biasing network in figure 3.4 and the current mirror connection between the two transistors should be introduced at the base of the current-driven transistor. The schematics are displayed in figure 3.6. The HBT X10 in the schematics 3.6 works as the additional current-driven transistor.

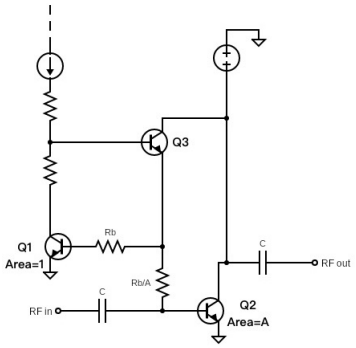

Figure 3.5: Current mirror concerning a current driver transistor

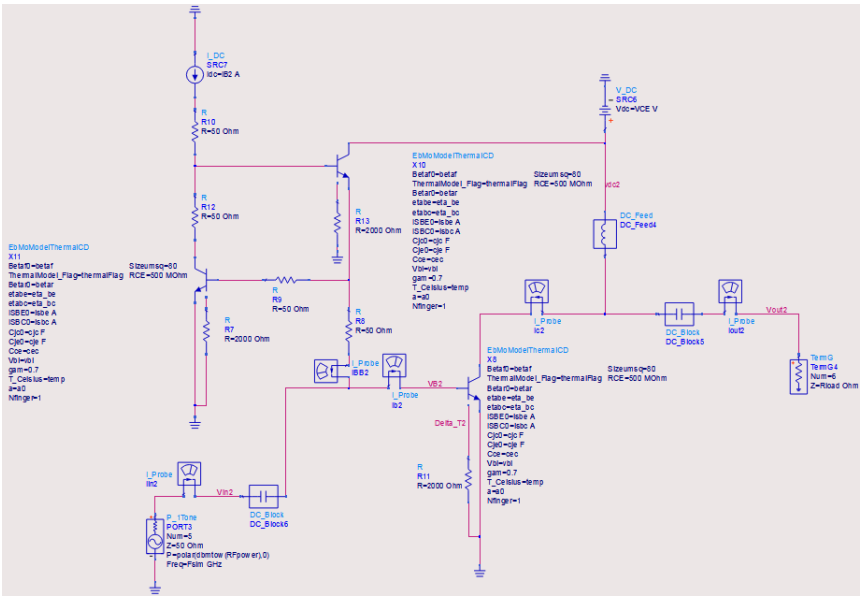

Figure 3.6: Power amplifier biased with current mirror concerning a current driver transistor

The sensitivity between the biasing current and the temperature variation is the same in schematics 3.4 and schematics 3.6. The two biasing networks are both based on the current mirror. However, with the additional transistor, the biasing network in figure 3.6 should have a larger dynamic range for the base biasing current. The biasing network would increase the biasing collector current as temperature increases which compensates the roll-off in dc-beta of the AlGaAs/GaAs HBT.

3.4 Simulation results and analysis

To compare the performance for different biasing circuits, separate DC simulations are carried out for different biasing networks to make the DC components I_B and I_C approximately equal to the values for the resistive biasing network (I_B=500 µA, I_C=48 mA) in figure 3.2. The numerical values for all the DC battery values are set in table 3.2 for all the biasing networks with different models. Note that:

- Label DC is the real DC battery value set directly to voltage sources and current sources in the schematics.
- Label I_C and I_C are the power amplifier transistor DC currents measured by probes with given DC power from the sources.
- Label Win means all the transistors in the circuits are Win's HBTs.
- Label EB means all the transistors in the circuits are custom-made HBTs in Chapter 2.

Schematic 3.4		Schematic 3.6	
$I_{DC(EM)}$	50.15 mA	$I_{DC(EM)}$	72.04 mA
$I_{B(EM)}$	500.50 µA	$I_{B(EM)}$	500.23 µA
$I_{C(EM)}$	48.07 mA	$I_{C(EM)}$	48.89 mA
$I_{DC(WIN)}$	49.50 mA	$I_{DC(WIN)}$	48.82 mA
$I_{B(WIN)}$	500.60 µA	$I_{B(WIN)}$	499.90 µA
$I_{C(WIN)}$	48.07 mA	$I_{C(WIN)}$	48.86 mA

Table 3.2: DC power supply and biasing conditions for proposed the biasing networks.

The simulation results display several parameters:

1. **dB(HB.Gain)** plots the available gain result defined by equation 3.26 when the input radio frequency power varies.
2. **HB.PAE** is the power-added efficiency for all the power amplifiers.
3. **mag(HB.Ib[::,0])** is the DC base voltage when the input power varies which is the base biasing point for the power amplifier.
4. **mag(HB.Ic.i[::,0])** is the DC base-collector current for all the power amplifiers as the collector biasing point.
5. **dBm(HB.Pout)** plots the fundamental output power defined by equation 3.25 for all the power amplifiers with the variation of the input fundamental power.
6. **dBm(HB.Pout3)** shows the third harmonic output power calculated by equation 3.27 for all the power amplifiers with the variation of the input fundamental power.

$$P_{in} = 0.5 \cdot real(V_{in}[1]conj(I_{in}[1])) \tag{3.24}$$

$$P_{out} = 0.5 \cdot real(V_{out}[1]conj(I_{out}[1])) \tag{3.25}$$

$$Gain = 0.5 \cdot \frac{P_{out}}{P_{in}} \tag{3.26}$$

$$P_{out3} = 0.5 \cdot real(V_{out}[3]conj(I_{out}[3])) \tag{3.27}$$

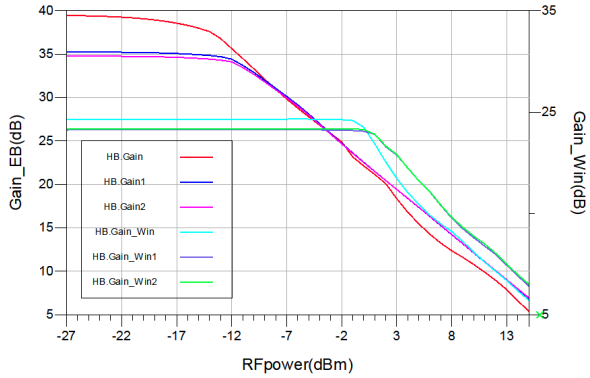

Figure 3.7: Gain results for different biasing networks

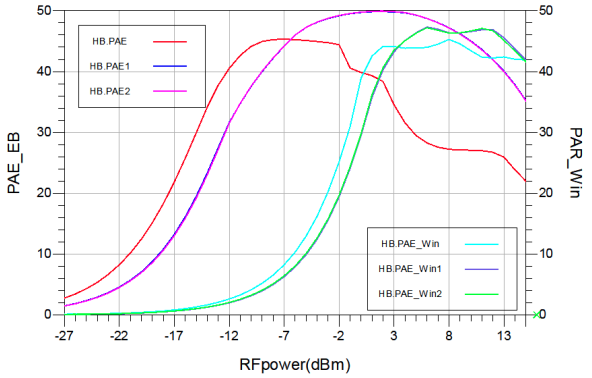

Figure 3.8: Efficiency results (PAE) for different biasing networks

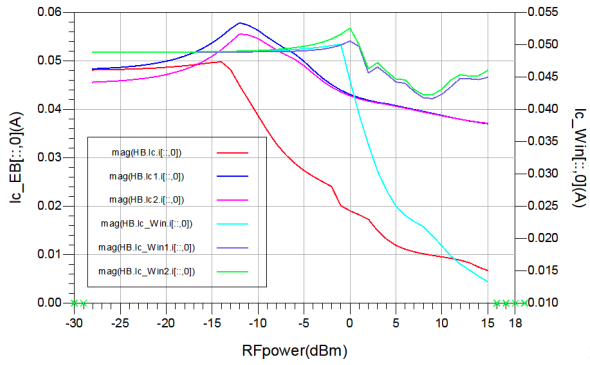

Figure 3.9: DC collector current results for different biasing networks

re

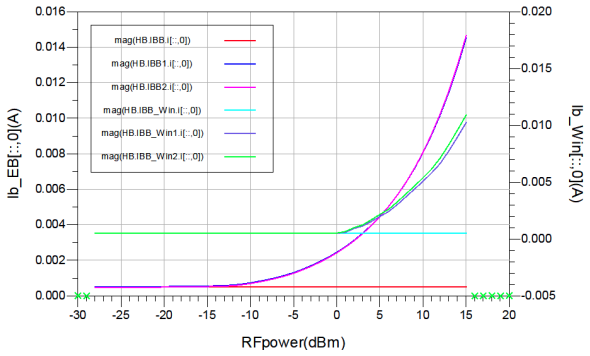

Figure 3.10: DC base current results for different biasing networks

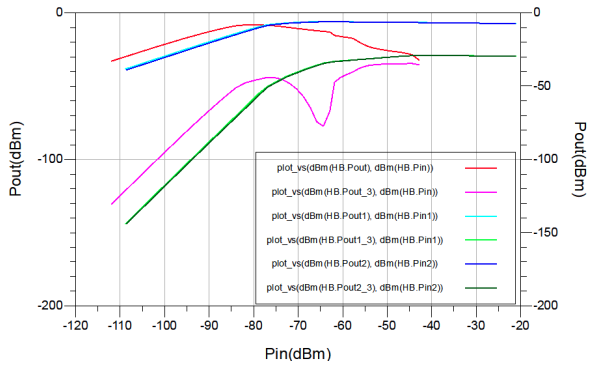

Figure 3.11: Output power results for different biasing networks with self-designed model

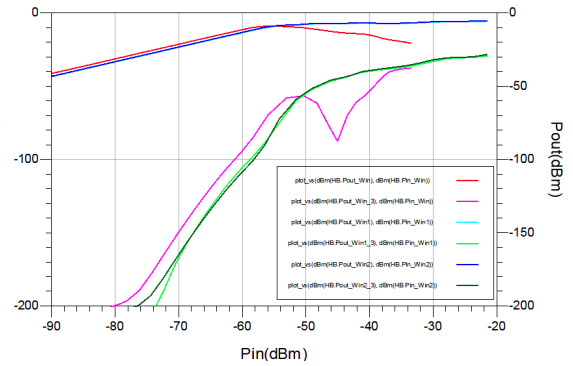

Figure 3.12: Output power results for different biasing networks with Win's model

3.4.1 Comparison of different biasing networks

Only Win's simulation results are considered in this analysis. The comparison is based on the differences in gain, efficiency, and DC components' behavior, together with fundamental output power and the third-order output power.

Gain and PAE comparison Gain_Win(dB) in figure 3.7 and PAE in 3.8:

- Blue curve is the result for resistive biasing in figure 3.7. Compared with the other curves, the gain compression happens at a lower input power level for the resistive biasing circuit in figure 3.2. In fact, to measure the values of gain compression, the plot in figure 3.13 generates the numerical value of gain compression values in dB when the power amplifier reaches the highest PAE.
- Purple curve is the result for the current mirror in figure 3.4. Apparently, compared with the blue curve, the gain compression occurs at a slightly higher input power level. The gain compression value is also smaller according to figure 3.14. Even though the highest PAE is the same for the blue curve and purple curve, the purple curve has a smaller slope when the PAE drops.
- Green curve is the result for the current mirror in figure 3.6. It works equivalently to the purple curve in gain and efficiency behavior.

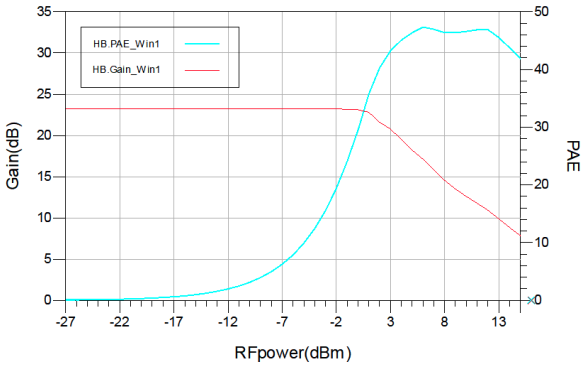

Figure 3.13: Measurement of Gain compression in the resistive biasing network.

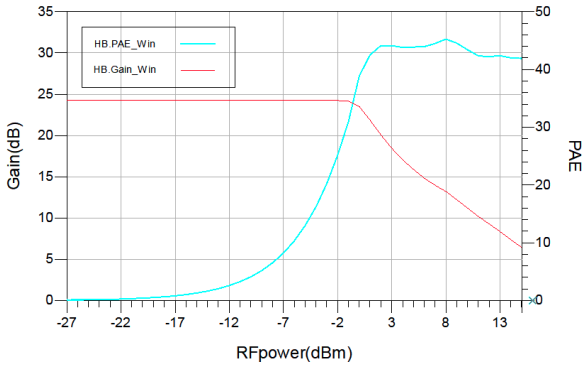

Figure 3.14: Measurement of Gain compression in proposed current mirror biasing network.

Parameter	Resistive biasing in 3.4	Current mirror biasing in 3.4
Maximum PAE	45.269%	47.319%
Gain compression (dB)	11.057	6.108

Table 3.3: Maximum PAE and gain compression value for resistive and current mirror biasing network

DC components comparison Ic_Win(A) in figure 3.9 and Ib_Win(A) in 3.10:

- Blue curve is the result for resistive biasing in figure 3.7. Compared with the other curves, the collector current loses its constant behavior at a low input power level around $RFpower = 3dBm$. The base current stays the same.
- Purple curve is the result for the current mirror in figure 3.4. The collector current, in fact, increases at first and drops around $RFpower = 5dBm$ when the HBT loses its linearity. The base current tends to increase in compensation for the loss of the currents.

- Green curve is the result for the current mirror in figure 3.6. The curve trend behaves similarly to the purple one. In fact, when the DC simulation sweeps the base current for this circuit. The collector current can be huge even though the DC source is small, as shown in figure 3.15.

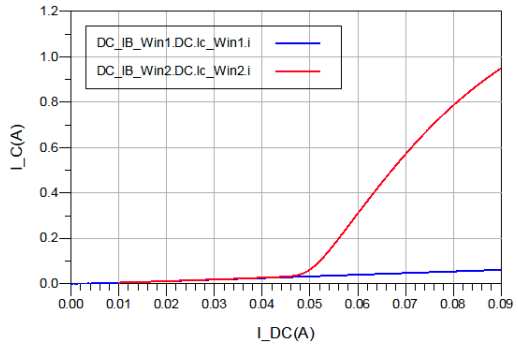

Figure 3.15: Collector current for two different current mirror schematics when the current sources offer the same currents, where the red is the current mirror in figure 3.6 and blue is the current mirror in figure 3.4.

3.4.2 Comparison between Wins's model and custom-made model in the same biasing circuit design

Only the biasing network design in figure 3.4 is considered in this analysis. The thermal flag has been set as 1 in the self-designed HBT model to include the thermal effects. The comparison is based on the performances in gain, as the pink curve and the green curve in figure 3.7. It is obvious that the custom-made model performance on the linearity is much worse compared to Win's HBT. To improve it, the linearizer design is introduced in Chapter 4.

CHAPTER 4

Biasing Circuits with Linearizer

The active devices adopted in power amplifiers internally dissipate power that, considering the classical efficiency values, is comparable to the delivered output power. Therefore, the active regions of the power transistors will raise considerably its temperature in order to transfer to the ambient. The temperature increase has different consequences for FET and HBT.

- For FETs, the increased channel temperature reduces the current mobilities and, therefore, worsens the device's performance.
- In HBT, temperature affects the device currents in a more complex way. In fact, there are effects that decrease the current when the temperature increases, and others with opposite consequences. Therefore, it is possible to compensate for the temperature effects on the device behavior, to increase the overall linearity in large signal conditions. [24].

Linearity, one of the most significant issues for power amplifiers in the transmitter system, has been enhanced by the linearizer network design nowadays. Considering the thermal effects of HBTs, this chapter proposed linearizer designs inside the biasing networks. Unlike the implementation of the current mirror biasing network design in Chapter 3, which concentrates on the well-defined DC current for transistors working for low-power operations, the linearizer focuses on the performance of power amplifiers in large signal conditions.

4.1 The working principle of the linearizer

HBT technology offers high efficiency and high power density at a low operation voltage. The thesis focuses on the design of high efficiency, high frequency, and high linearity power amplifier design. To enhance the linearity without decreasing efficiency, the linearizer design should reach the following requirements:

- effective improvement of the gain compression of the HBT;
- no additional DC current consumption;
- little insertion loss;
- almost no increase in die area.

4.2 Proposed biasing networks based on linearizer capacitance

To include the thermal effects for HBTs, two different GaAs HBT models have been used in the following biasing design. They are:

- Win's HBT: considerable thermal effects but lack of the detailed insight view.
- Self-defined HBT in chapter 2: adjustable thermal effects.

Note that in the later schematics, all the simulations are run for both HBT. But only Self-defined HBT is presented in the figure to show the basing networks' composition. Both models are biased with the same conditions for I_B and V_{CE}. The detailed parameters are listed in table 3.1.

4.2.1 Resistive biasing circuit as reference

In the schematics 3.2, the reference biasing circuit is constructed using simple resistance and a DC battery supply. This simple biasing network works as a comparison to the current mirror biasing networks. The simulations are DC and large signal simulation:

- DC simulation is used for the same DC working conditions for all biasing networks:
  - DC voltage supply V_{CE} sweeps from 0 V to 10 V with the step of 0.01 V.
  - DC base current supply I_{BB} sweeps from 100 µA to 1000 µA with the step of 100 µA.
  - Ambient temperature for the transistor sweeps from 1° to 40° with the step of 1°.
- Large signal simulation is used to compare the performance of the power amplifier with different biasing networks:
  - Working frequency $F_{sim} = 5$ GHz.
  - Harmonic orders $Order$ =5.
  - Input radio frequency power RF_{power} sweeps from −30 dBm to 20 dBm with the step of 1 dBm.

There are three different current mirror-biasing networks proposed. The details and the simulation results are listed in the following sections.

4.2.2 linearizer with a transistor base-collector junction diode.

Figure 4.1 shows the circuit topology of the biasing circuit design based on the linearizer with a transistor base-collector junction diode. The linearizer is composed of the transistor Q2 and the resistance RB. The Q2 HBT base-collector diode is forward-biased, and the resistance connecting the base and emitter of Q2 has no effect on the linearization, therefore there is no current flowing between the base and emitter of Q2. When the input power increases, the rectified DC current of the Q2 base-collector diode increases and the DC voltage across the diode decreases. Therefore, the DC voltage across the amplifier HBT Q1 base-emitter diode (V_{BE}) increases slightly [25]. The schematics that are based on the forward-biased diode linearizer are built in figure 4.2.

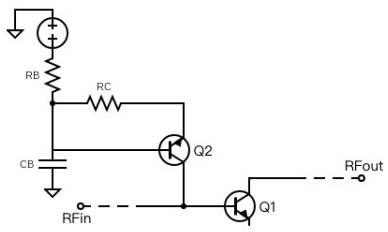

Figure 4.1: Linearizer biasing circuit based on HBT base-collector diode

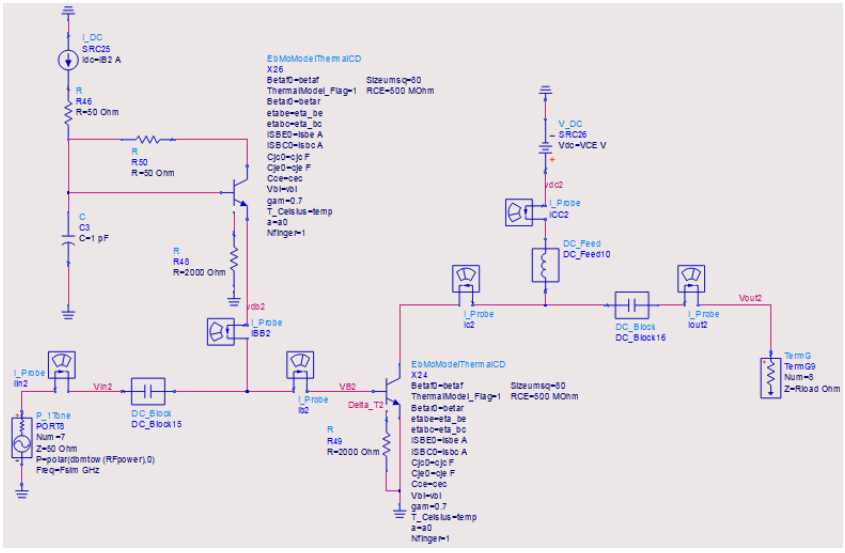

Figure 4.2: Linearizer biasing circuit based on HBT base-collector diode

4.2.3 Linearizing shunt capacitor with a single base-emitter diode

The second linearizer is composed of a transistor base-emitter diode and a shunt capacitor. Figure 4.3 shows the details of the linearizer biasing circuit. Transistors Q3, and Q4 work as two series-connected diodes. The biasing base current of amplifier transistor Q1 is supplied by the linearizer transistor Q2. Q3, Q4, Cb, and Rb provide a DC voltage to the linearizer transistor Q2. Therefore, the schematics for verifying the biasing network have been built in figure 4.4. The biasing collector current for the amplifier transistor Q1 ($I_{C,Q1}$) is determined by its base-emitter voltage ($V_{BE,Q1}$) in equation 4.1. The base-emitter voltage ($V_{BE,Q1}$) for Q1 can be represented in equation 4.2. When the input power increases, due to the current collapse and self-heating, the amplifier requires a higher collector current ($I_{C,Q1}$) to reach larger output power. The current flowing through the resistance RB may increase, therefore, the $V_{BE,Q1}$ may be reduced and then the amplifier HBT Q1 can only provide smaller output power capability [26]. In the linearizer design, voltage (V_P) is controlled by the two diode-connected transistors Q3 and D4 with shunt capacitance C_B during the trend of increasing base current of Q1. V_P would decrease more as higher input powers are induced. Hence, $I_{C,Q1}$ would be limited to a certain level.

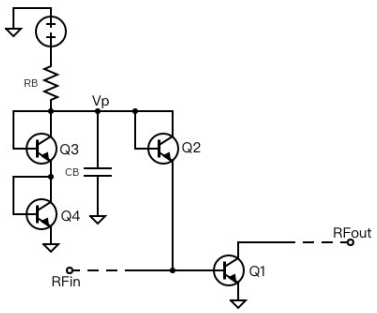

Figure 4.3: Linearizer biasing circuit with shunt capacitance and an HBT base-emitter diode

$$I_{C,Q1} = I_{S,Q1} \cdot e^{\frac{V_{BE,Q1}}{V_T}} \tag{4.1}$$

Where $I_{S,Q1}$ is the saturation current of HBT Q1. V_T is the thermal voltage of the HBT Q1.

$$V_{BE,Q1} = V_{BB} - V_{RB} - V_{BE,Q2} = V_P - V_{BE,Q2} \tag{4.2}$$

V_{BB} is the DC supply voltage from the battery. V_{RB} is the voltage across the resistance RB which is controlled by the current (I_B) flowing through the resistance.

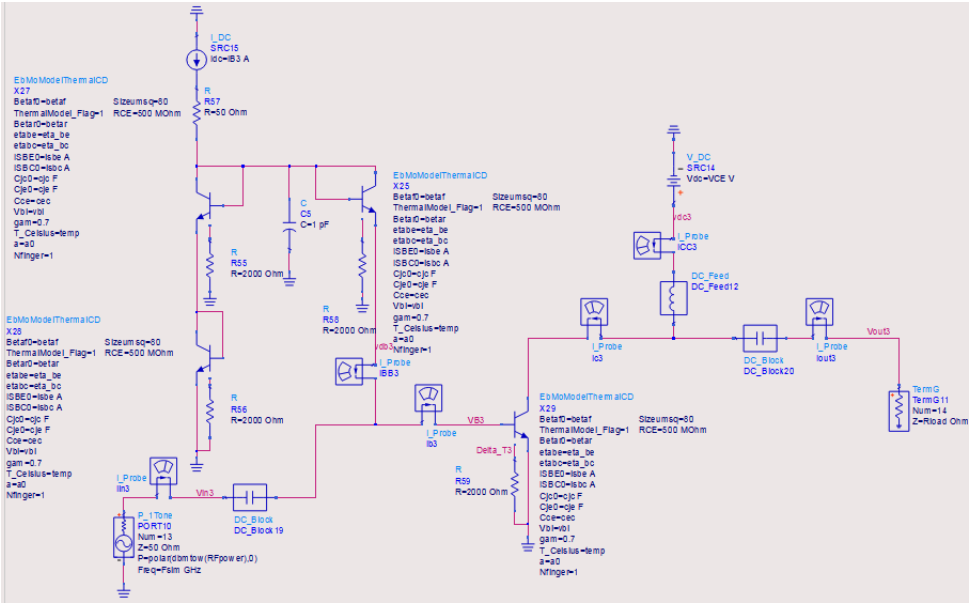

Figure 4.4: Linearizer biasing circuit with shunt capacitance and an HBT base-emitter diode

4.2.4 Linearizing shunt capacitor with an active biased transistor base-emitter diode

The new proposed linearizer is composed of the base-emitter diode of an active bias transistor and a capacitor to provide an RF shot at the base node of the active bias transistor. The linearizer compensates for the decreased base bias voltage of the RF amplifier caused by the increased input power level with the setting of the following procedures:

1. The impedance to the linearizer is decreased by the capacitor CB at the RF frequency.
2. The amount of RF power leak to the linearizer is increased.
3. The rectified DC current to the linearizer makes the voltage drop between the base and emitter of HBT Q2.
4. The voltage drop compensates for the decreased base bias of the amplifier HBT Q1.

The impedance of the parallel connection of a resistor RB and two series diodes Q3 and Q4 is substantially larger than the impedance of the capacitor CB at the RF frequency, all the RF signal at node V_P is routed through the capacitor Cb, resulting in a fixed voltage at V_P. With increasing input power, HBT Q1 requires more collector current, hence the base current of HBT Q1 must be raised. In this scenario, the voltage at V_P remains constant in DC, because the current flowing through the diodes Q3 and Q4 is significantly greater than the base current of HBT Q2. The entire voltage drop between the base and emitter of the HBT Q2 compensates for the HBT Q1 base bias loss [15]. The schematics are shown in figure 4.6.

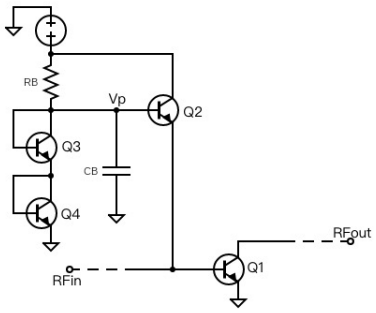

Figure 4.5: Linearizer biasing circuit with shunt capacitance and an active-biased HBT base-emitter diode

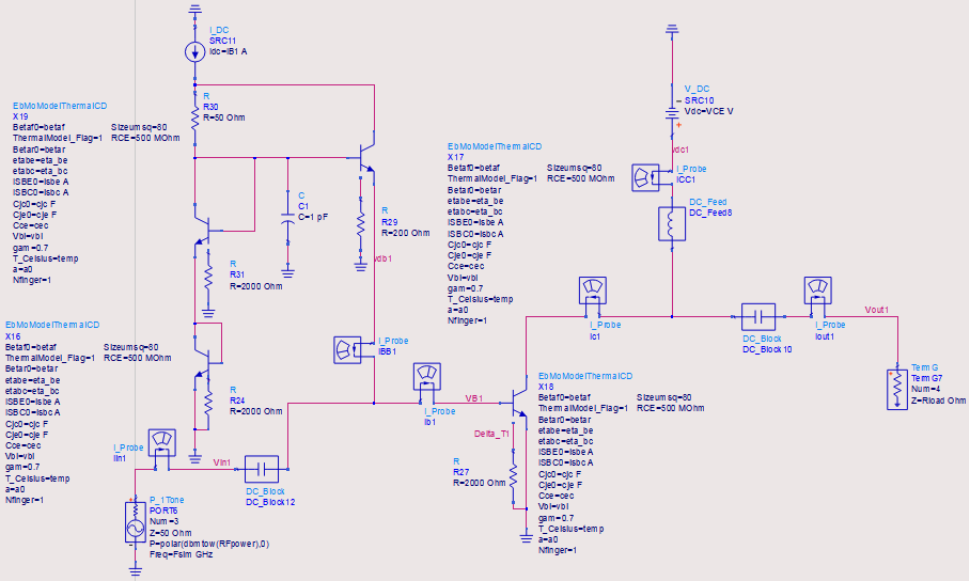

Figure 4.6: Linearizer biasing circuit with shunt capacitance and an active-biased HBT base-emitter diode

4.3 Simulation results and analysis

4.3.1 Simulation results for different biasing networks

To compare the performance for different biasing circuits, separate DC simulations are carried out for different biasing networks to make the DC components I_B and I_C approximately equal to the values for the resistive biasing network (I_B=500 µA, I_C=48 mA) in figure 3.2. The numerical values for all the DC supply values have been set in table 4.1 for all the schematics that have been simulated.

Schematic 4.6		Schematic 4.4		Schematic 4.2	
$I_{DC(EM)}$	5.44 mA	$I_{DC(EM)}$	505.00 µA	$I_{DC(EM)}$	5.44 mA
$I_{B(EM)}$	500.51 µA	$I_{B(EM)}$	505.00 µA	$I_{B(EM)}$	500.16 µA
$I_{C(EM)}$	48.07 mA	$I_{C(EM)}$	48.47 mA	$I_{C(EM)}$	48.04 mA
$I_{DC(WIN)}$	7.68 mA	$I_{DC(WIN)}$	499.40 µA	$I_{DC(WIN)}$	7.68 mA
$I_{B(WIN)}$	500.61 µA	$I_{B(WIN)}$	499.40 µA	$I_{B(WIN)}$	499.88 µA
$I_{C(WIN)}$	48.92 mA	$I_{C(WIN)}$	48.80 mA	$I_{C(WIN)}$	48.85 mA

Table 4.1: Biasing conditions for all the biasing networks

The simulation results display several parameters:

- **dB(HB.Gain)** plots the available gain result defined by equation 3.26 when the input radio frequency power varies. Schematics with self-defined model plots in figure 4.7 and Win's model in figure 4.8.
- **HB.PAE** is the power-added efficiency for all the power amplifiers. Schematics with self-defined model plots in figure 4.9 and Win's model in figure 4.10.
- **mag(HB.Ic.i[::,0])** is the DC base-collector current for all the power amplifiers as the collector biasing point. Schematics with self-defined model plots in figure 4.11 and Win's model in figure 4.12.
- **dBm(HB.Pout)** plots the fundamental output power defined by equation 3.25 for all the power amplifiers with the variation of the input fundamental power.
- **dBm(HB.Pout3)** shows the third harmonic output power calculated by equation 3.27 for all the power amplifiers with the variation of the input fundamental power.

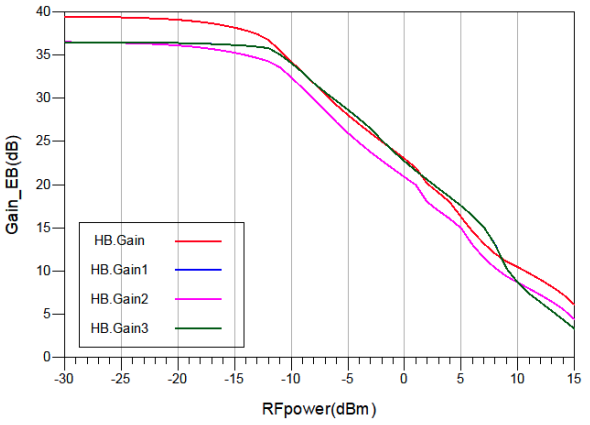

Figure 4.7: Gain results for different biasing networks with self-defined HBT.

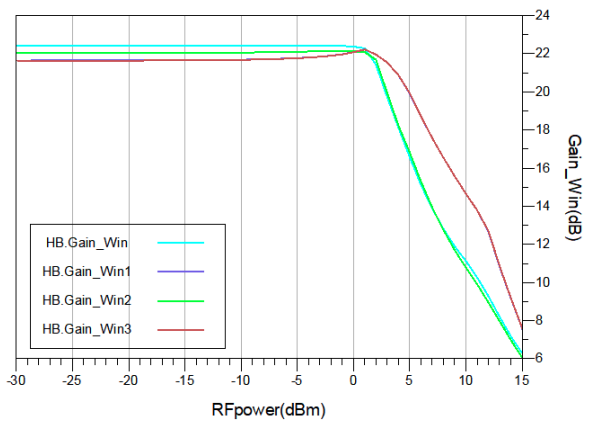

Figure 4.8: Gain results for different biasing networks with Win's HBT.

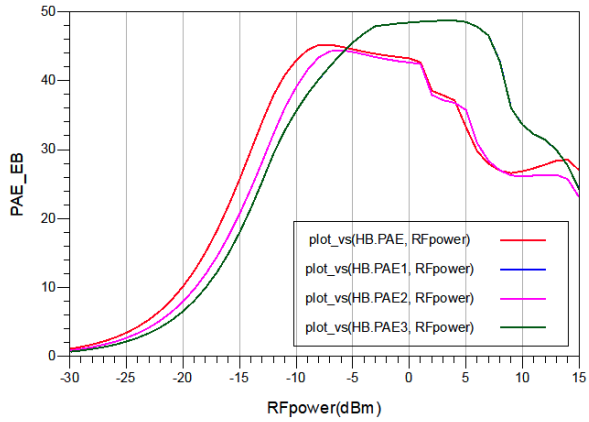

Figure 4.9: PAE results for different biasing networks with self-defined HBT.

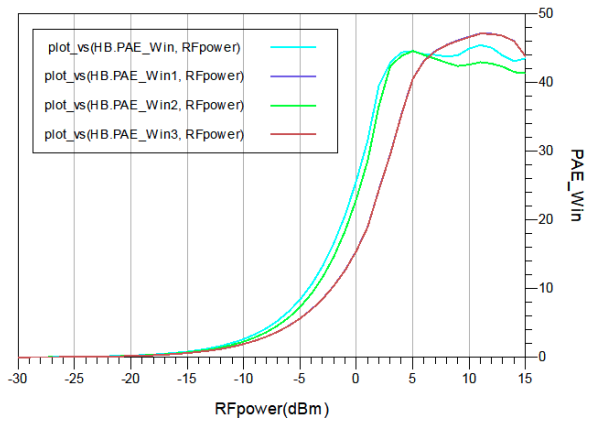

Figure 4.10: PAE results for different biasing networks with Win's HBT.

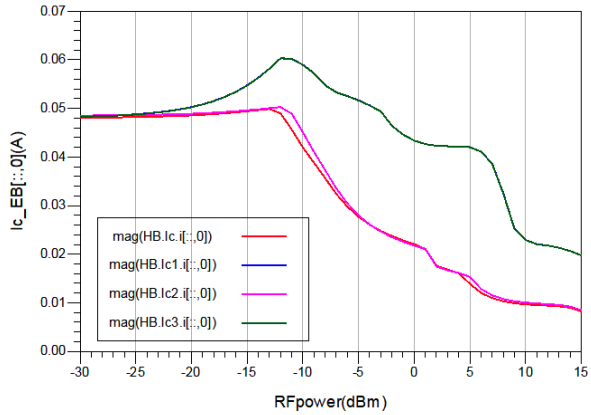

Figure 4.11: DC collector current results for different biasing networks with self-defined HBT.

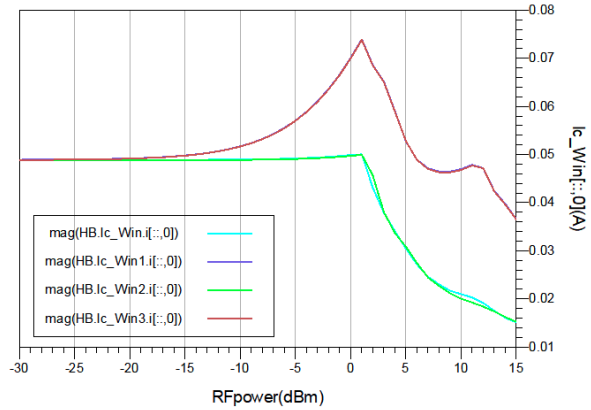

Figure 4.12: DC collector current results for different biasing networks with Win's HBT.

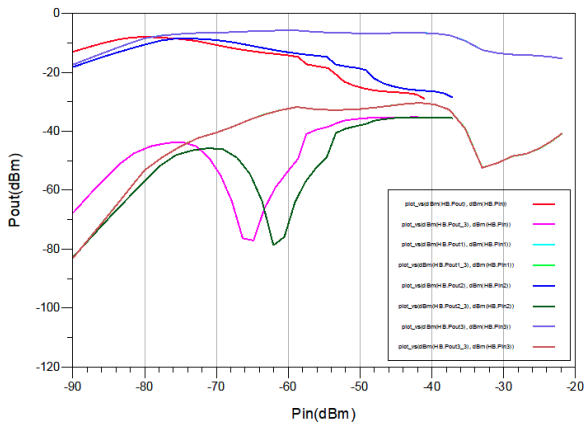

Figure 4.13: Output power results for different biasing networks with self-designed model.

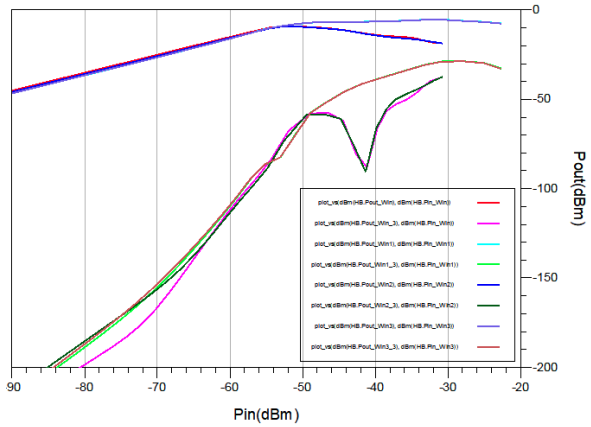

Figure 4.14: Output power results for different biasing networks with Win's model

4.3.2 Analysis and comparison based on the simulation results

Improvement of linearity based on measurement of gain compression

Analysis compared to the current mirror design The current mirror designs in Chapter 3 perform poorly in the linearity domain. Compared to the gain compression result between the current mirror biasing network and the linearizer biasing network, the improvement of linearity by the linearizer is much better. Only the self-defined model is considered in this case. Take the schematics in figure 3.4 and 4.6 as an example, the results of gain compression are generated in table 4.2. In addition, resulting in a decent PAE, the input power level has been extended in linearizer design. The input power level can reach to 8dBm in this design.

Parameter	Current mirror in 3.4	Linearizer in 4.6
Maximum PAE	49.855%	48.610%
Gain compression(dB)	14.812	12.776
Input power level for max PAE(dBm)	2	1

Table 4.2: The linearity compression measurements for current mirror biasing circuit and linearizer biasing circuit.

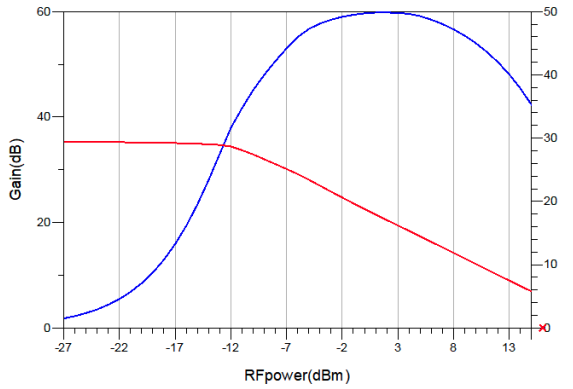

Figure 4.15: Gain vs PAE for the power amplifier with current mirror biasing design.

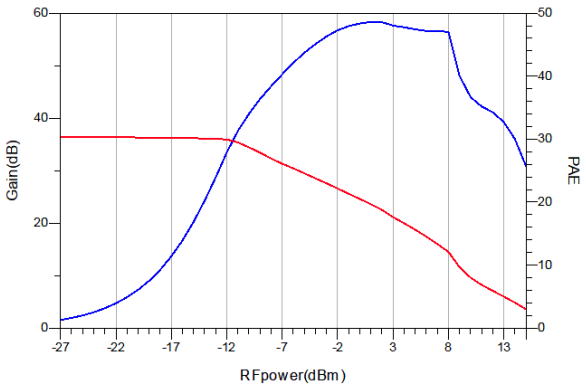

Figure 4.16: Gain vs PAE for the power amplifier with linearizer biasing design.

Analysis among different linearizer designs Only a self-defined model has been considered in the analysis. Combined the gain result in figure 4.7 and the efficiency result in figure 4.9, the numerical gain compression value and the best PAE value are measured in table 4.3, together with the input power level (dBm) that reaches the highest PAE.

Parameter	Linearizer in 4.2	Linearizer in 4.4	Linearizer in 4.6
Maximum PAE	44.403%	48.614%	48.610%
Gain compression(dB)	8.892	12.775	12.776
Input power level for max PAE(dBm)	-6	1	1

Table 4.3: The linearity compression measurements for different linearizer biasing circuits.

Even though the gain compression value is lower when the linearizer is designed as in figure 4.2, its input power level and PAE are also the smallest. However, the linearizers with shunt capacitance on the base in figure 4.4 and 4.6 have a higher input power range. In addition, the efficiency is remarkable.

The result in figure 4.7 is consisted of:

- The red curve is the result of the resistive biasing network in figure 3.2. Even though the small signal gain result is the highest compared with other curves. The linearity is the worst. In addition, PAE reaches the highest value when the input power level is around -7 dBm which is quite low compared to the other curves. The input power range for this amplifier is limited.
- The pink curve is the result for the linearizer circuit in figure 4.2. The linearity improvement is not obvious compared to the green and blue ones. Also, this circuit results in a low-efficiency result.
- The green and blue are the results for the linearizer circuit in figure 4.4 and 4.6. Their performance in gain and efficiency are approximately equivalent, where the gain is more well-defined when the power amplifiers are working. The gain compression occurs when the input power is around -12dBm, which is the highest.

4.3.3 Simulations on the different values of capacitance

The value for the shunt capacitance in figure 4.4 and 4.6 is 6 pF in previous simulations. To explore the functionality of the shunt capacitor, different capacitance values for the biasing network in figure 4.6 have also been a concern during the simulation. The capacitance values used for the simulation are listed in table 4.4.

Simulation Number	Capacitance value
Simulation Schematics 1	1 pF
Simulation Schematics 2	6 pF
Simulation Schematics 3	12 pF

Table 4.4: Different capacitance values for linearizer biasing network

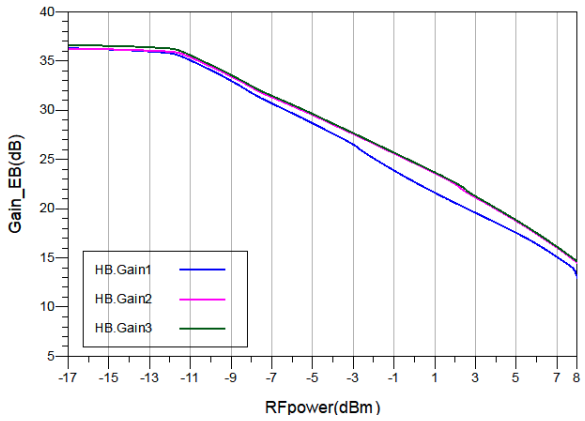

Figure 4.17: Gain results for different biasing networks

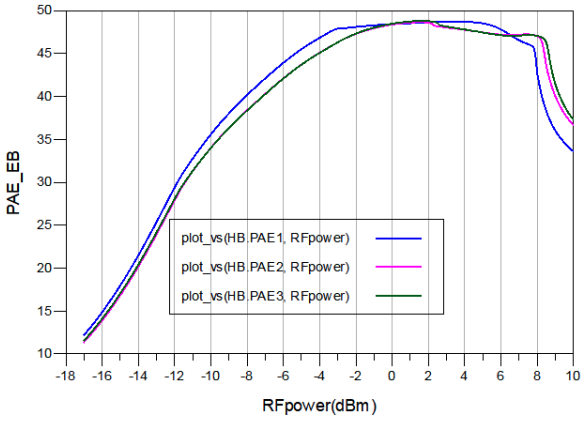

Figure 4.18: Efficiency results (PAE) for different biasing networks

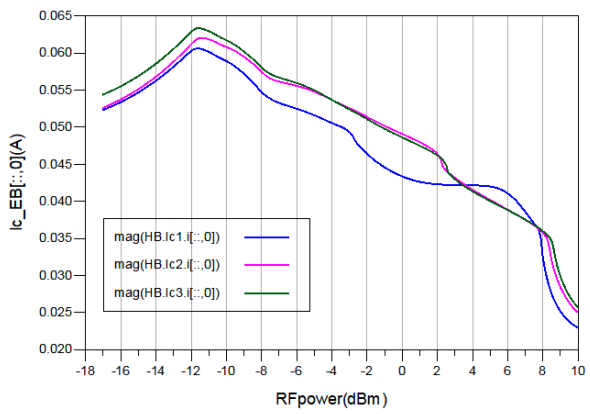

Figure 4.19: DC collector current results for different biasing networks

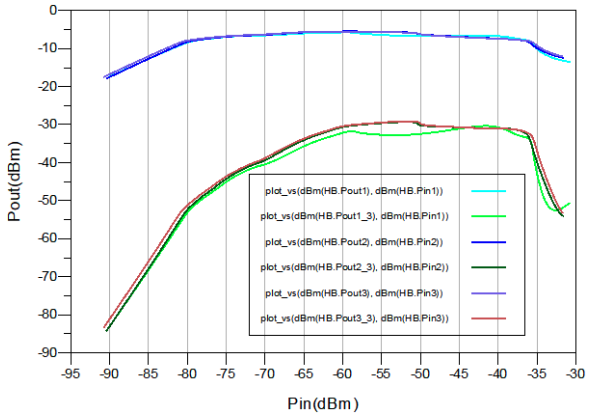

Figure 4.20: DC base current results for different biasing networks

4.3.4 Linearity performance with different capacitance values

The linearity measurement is listed in table 4.5.

Parameter	C=1 pF	C=6 pF	C=12 pF
Maximum PAE	48.712%	48.654%	48.788%
Gain compression(dB)	17.502	13.283	13.799
Input power level to reach the max PAE(dBm)	3.6	1	1.7

Table 4.5: Gain compression measurement for different shunt capacitances

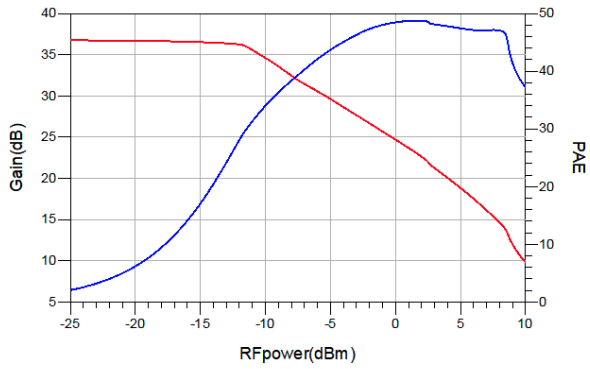

Figure 4.21: Gain vs PAE for the power amplifier when shunt capacitance is 12pF.

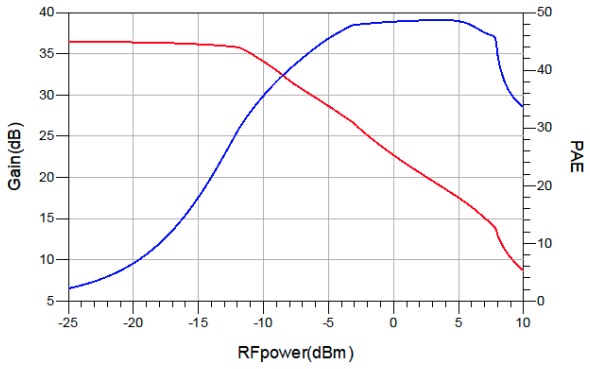

Figure 4.22: Gain vs PAE for the power amplifier when shunt capacitance is 1pF.

The shunt capacitance values affect the linearity improvement nonlinearly. In fact, in figure 4.11, a higher value of shunt capacitance in the biasing provides higher DC current compensation. However, the goal of the biasing circuit is to provide a stable and well-defined DC base current. The proper choice for shunt capacitance is crucial. Further simulations can be carried out to choose the best shunt capacitance value.

CHAPTER 5

Conclusion

This thesis focuses on a comprehensive exploration of advanced Heterojunction Bipolar Transistor (HBT) modeling, considering GaAs HBTs for high-frequency power amplifier applications. Through various investigations and simulations, I have addressed the critical challenges of thermal effects with biasing networks in HBT power amplifiers, offering innovative solutions that enhance performance and reliability, especially the linearity for the power amplifiers.

The development of a custom GaAs HBT model that, considered thermal variations, offers further insights. This model, consistent with the industry-standard Win's HBT model, provides more detailed consequences from the thermal effects impacting HBTs, specifically self-heating and current collapse phenomena. By including a thermal pin functionality and examining the influence of thermal resistance, the model offers valuable insights for designing more efficient biasing networks to minimize thermal instability.

Furthermore, the thesis presented novel biasing circuit designs, emphasizing the use of current mirrors and linearizers. These designs not only address the thermal challenges but also improve the linearity and stability of HBT power amplifiers, for their performance in high-frequency applications. The comparison and analysis of different biasing networks underline the importance of different customized solutions to meet specific design requirements.

Key takeaways and implications in this thesis are:

- Advanced Modeling: The custom HBT model with thermal effects provides a powerful tool for modeling device behavior under various operating conditions in a relative simulation tool ADS, which is essential for the design and optimization of biasing networks.
- Thermal consideration: Effective thermal stabilization techniques, including the use of ballasting resistances and optimized biasing circuits, are crucial for minimizing the effects of self-heating and ensuring device reliability.
- Biasing Strategies: The proposed biasing circuits, particularly those incorporating linearizers, offer a promising approach to enhancing the linearity and efficiency of HBT-based amplifiers, crucial for modern communication systems.
  - Current mirror: can provide stable DC collector current for power amplifiers. However, considering the extra transistor, the requirement, that two transistors should have the same junction temperatures, is hard to reach. Also, the area of the integrated circuit can be relatively big with two transistors, which results in a higher delay. In addition, the current mirror improvement on the linearity is poor.

– Linearizer design: can improve the power amplifier linearity without additional DC current consumption and increase in die area. The thesis finds the linearizer with shunt capacitance and an active-biased HBT base-emitter diode works the best when it comes to the improvement of gain comparison. Nevertheless, the choice of the shunt capacitance affects the performance of the linearizer.

The findings of this thesis provide various directions for future investigation. Further exploration into the ambient temperature's impact on thermal resistance, together with the integration of other nonlinear effects into the model could provide deeper insights into HBT behavior. Additionally, the practical implementation of the proposed biasing circuits in real-world applications can be done to validate their performance and adaptability. Ultimately, the continuous advancement in HBT modeling and design strategies will play a crucial role in the development of next-generation high-frequency electronic devices.

In conclusion, this thesis contributes to the foundational understanding and advancement of HBT technology, particularly in addressing the thermal effects inherent in high-frequency, high-power, and high-linearity power amplification. HBTs development can be crucial for communication systems, up to 5 and 6 GHz nowadays. The consideration of thermal effects is crucial for modern transistors to extend their lifetime. Further development on this thesis is necessary for developing high frequency, high linearity power amplifiers based on HBTs.

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