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Advanced current sensing for power modules based on WBG transistors

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to my family

Aknowledgements

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Abstract

A wide variety of applications require information about the current flow. Current sensing applications have different performance requirements in terms of cost, isolation, precision, measurement range, bandwidth, size. Several current sensing techniques are used, depending of the application type. Sensing techniques can be classified based upon the physical principle they rely on, the main classes being:

- Ohm's law based sensors
- Faraday's law based sensors
- Magnetic field sensors
- Faraday effect based sensors

Ohm's law based sensors are the most used ones because of the low cost and good reliability. Besides that, resistors can sense both AC and DC currents. Drawbacks include power dissipation, non-isolation and voltage drop. This method guarantees high frequency operation and bandwidth is typically limited by the measuring circuitry. The problems of power dissipation and voltage drop can be tackled by reducing the resistor value but this causes the voltage across the resistor to decrease, hence the bandwidth of the system decreases.

Faraday's law based sensors provide electrical isolation. The most used ones are the Rogowski coil and the current transformer. A Rogowski coil provides a voltage which is proportional to the time derivative of the current flowing in the wire. Drawbacks are that it only works for alternated currents and the sensitivity is not large since the core material is non magnetic. A current transformer is also based on the Faraday's law. It consists of one primary turn and several secondary turns and it

has a core made of high permeability material. The difference with the Rogowski coil is that there is a sense resistor on the secondary side of the current transformer. The resulting voltage is proportional to the current flowing in the primary winding. Like the Rogowski coil, this solution is only suitable for AC currents. Advantages of this method are the isolation, low losses and that the output voltage does not require amplification.

Magnetic field sensors can sense both static and dynamic magnetic fields. Among the magnetic field sensors, the most common are the Hall effect sensor and the Fluxgate sensor. Hall effect sensor is very popular because of its compact size. It provides an output voltage proportional to the sensed magnetic field. One drawback is that magnetic field also penetrates the area enclosed by the sense wires, leading to a bandwidth limitation. Fluxgate sensor is one of the most accurate. It provides an alternating voltage whose peak value is proportional to the external magnetic field. Fluxgate is more accurate than other solutions due to its high sensitivity and temperature stability. Drawback is the bandwidth which is not very large.

Faraday effect based current sensors are extremely complex and high-cost so they are not employed in low current measurements.

This thesis' aim is to design an acquisition chain for the measurement of the current flowing in a power switch. Accurate current sensing in power devices is important in order to optimize the performance of such devices, the final goal being that of designing more efficient energy conversion systems. A shunt resistor has been chosen as current transducer due to its ability to sense both AC and DC currents and to its large bandwidth, as well as the simplicity and low cost. The main challenges are the large dynamic range (86 dB) covered by the current and the relatively wide required bandwidth. The higher switching frequency of last generation power devices, using new technologies such as GaN and SiC, implies a reduction of the available time for performing the measurement hence posing strict specifications in terms of the bandwidth of the sensing circuitry. The proposed acquisition chain has to tackle bandwidth reduction and limited resolution problems which affect conventional current sensing systems. The proposed system is based on nonuniform quantization which allows a quantization step proportional to the input signal. Nonuniform quantization is achieved by means of signal compression followed by uniform quantization.

A description of the system is provided and a temperature-compensated logarithmic amplifier, performing signal compression, is presented. The conditioning circuit presents minimum bandwidth of about 1 MHz and shows a worst case accuracy of 9% at minimum input current.

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CHAPTER 1

State of the art

The development of an integrated systems approach, in recent years, has caused an increase in the need for current sensors suitable for packaging into power electronic modules. Current sensing is necessary for control, protection and monitoring in power electronics systems. The specifications of the current sensing system are determined by the application since the performance of control systems strongly depends on the accuracy and efficiency of its sensors.

There are several current sensing techniques and they differ from one another in terms of cost, isolation, bandwidth, precision, measurement range, size, complexity. The different techniques can be classified depending on the physical principle they are based upon. The following classification is provided in [1]:

- Ohm's law of resistance based sensors
- Faraday's law of induction based sensors
- Magnetic field sensors
- Faraday effect based sensors

In case of very specific requirements, different techniques can be combined.

1.1 Ohm's law of resistance

Ohm's law is a simplification of Lorentz's law that states

$$\vec{J} = \sigma(\vec{E} + \vec{v} \times \vec{B}). \tag{1.1}$$

In most cases the velocity of the charges is sufficiently small so that the second term can be neglected, yielding the most familiar

$$\vec{J} = \sigma\vec{E}. \tag{1.2}$$

This is known as the Ohm's law of resistance and states that a flowing current inside a resistor is proportional to the developed voltage across the resistor. This simple relationship suggests that a resistor can be used to sense a current, by measuring the resulting voltage across it.

1.1.1 Shunt resistor

Shunt resistors are largely employed in current sensing applications due to their low cost, simple working principle and reliability. The current to be measured flows through the shunt resistor and the voltage across it is measured. This technique is suitable for both AC and DC currents. Shunts must be inserted in the main current path, and therefore decrease efficiency, particularly in high current low voltage applications. The main drawbacks are the voltage drop in the branch where the shunt is inserted and the power loss due to Joule effect. Both these problems can be tackled by reducing the value of the shunt resistor. A smaller resistor causes smaller voltage drop and less power dissipation but it also implies an increased gain for the conditioning circuitry, which can be responsible for the bandwidth limitation of the measurement. The power loss usually limits the use of shunt resistors for large currents measurement. In order to improve accuracy, often, shunts have low temperature coefficient of resistance and use Kelvin terminals (fig. 1.1).

Shunt resistors can be used to measure large current variations with fast transition times. In those applications the frequency behavior of the shunt resistor is very important. Practical shunt resistors have a series parasitic inductance (fig. 1.2a).

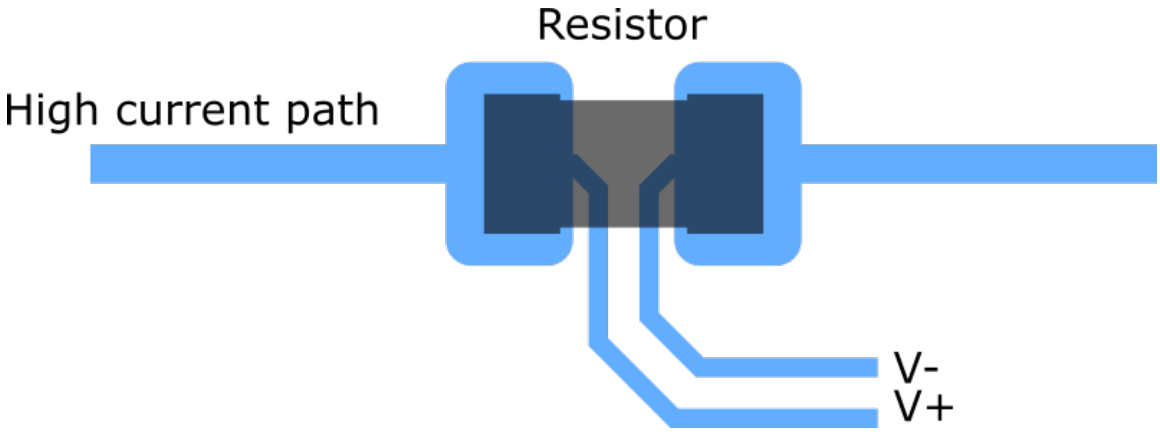

Figure 1.1: Kelvin connection for improved accuracy.

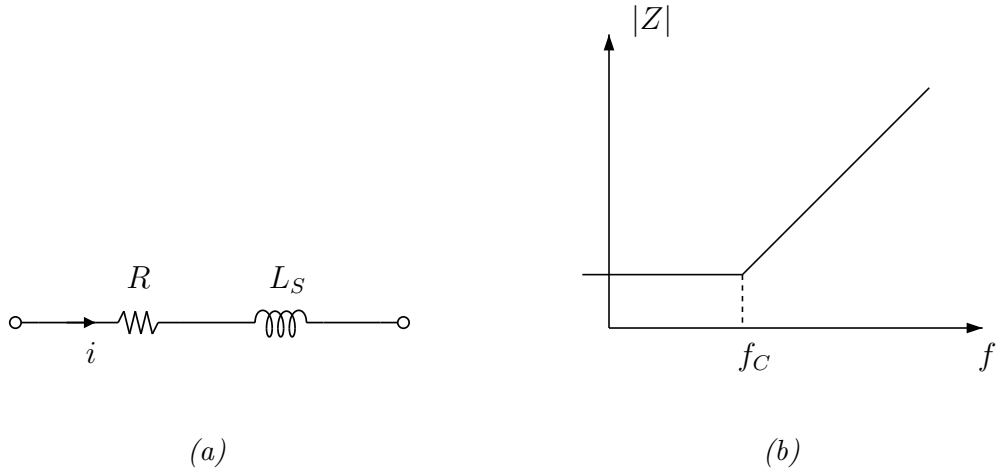

Figure 1.2: High frequency shunt: (a) Circuit model. (b) Frequency response.

Its impedance starts increasing from a certain frequency on as shown in fig. 1.2b: the induced voltage across the parasitic inductance becomes comparable with the resistive voltage hence the accuracy of the measurement at higher frequencies decreases. It is interesting to notice that the series inductance present in the circuital model is not only due to the self inductance of the shunt; in fact, it is mainly due to the mutual inductance between the loop formed by the sensing wires and the loop formed by the main current[2]. For a good measurement, the area enclosed by the loop must be minimized. Different geometries were found to reduce the inductive effect, such as coaxial shunts [3]. In that case the bandwidth limitation is caused by the skin effect [4].

Coaxial shunts, due to their large physical dimensions, are not optimal for being used in highly integrated devices. For that purpose, a thick film shunt resistor is more suitable since it is more compact. The smaller physical dimensions make the skin effect of secondary importance and the bandwidth limitation is caused by the parasitic series inductance.

Sensing resistors can be inserted either in the forward or in the return path. A low side shunt resistor has a voltage drop that is referred to ground which can typically be easily amplified. On the other hand, a voltage drop is caused in the ground path and this might cause problems to some analog circuits. In addition, a short circuit to ground can bypass the shunt resistor and go undetected. A high side shunt resistor is able to detect these kind of faults and eliminates the problem of the voltage drop on the ground path. On the other hand, the conditioning circuit becomes more complicated since the voltage to be measured might have a high common mode.

1.1.2 Trace sensing

An alternative solution to the dedicated shunt resistor is the use, for the current measurement, of the trace that carries the current. This allows for a low cost solution without introducing any additional power loss. This method cannot be used to measure small currents because of the very small intrinsic resistance of the trace. It is not recommended to use this method in those applications where good accuracy is required; in fact, the resistance of the trace has a large thermal drift [5]. The temperature error can be compensated by employing a temperature compensation scheme (obviously, a temperature measurement system is needed in that case).

Ohm's law based sensors represent the simplest way to measure currents. They have the drawback of causing a voltage drop in the branch where they are inserted and of introducing a power loss. Resistive sensors do not provide isolation but, on the other hand, they allow for sensing of both direct and alternated currents.

1.2 Faraday's law based current sensors

These kind of sensors provide inherent isolation and allow for the measurement of a floating voltage that may have a large common-mode, while the output voltage can

be easily referred to ground. The working principle of these kind of sensors is based on the Faraday's law of induction.

1.2.1 Rogowski coil

Rogowski coil is a classic example of an isolated current sensing technique; it is shown in fig. 1.3.

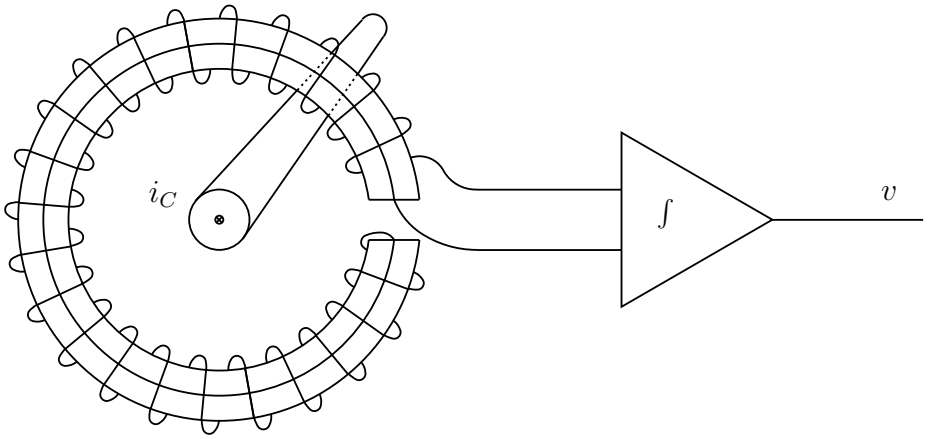

Figure 1.3: Rogowski coil configuration.

The operation can be explained by starting with Ampere's law

$$\oint_C \vec{B} \cdot \mathrm{d}\vec{l} = \mu_0 i_C. \tag{1.3}$$

The analysis makes use of the assumption that the coil diameter is much smaller than its radius. This way the magnetic flux density can be expressed by

$$B = \frac{\mu_0 i_C}{2\pi r}. \tag{1.4}$$

The induced voltage into the coil can be determined by using Faraday's law of induction

$$v = -N\frac{\mathrm{d}\phi}{\mathrm{d}t} = -nA\frac{\mathrm{d}B}{\mathrm{d}t} = -NA\frac{\mu_0}{2\pi r}\frac{\mathrm{d}i_C}{\mathrm{d}t}. \tag{1.5}$$

It can be seen from eq. (1.5) that the induced voltage is proportional to the time derivative of the current flowing in the wire. In order to get the current value, an

integration operation is needed. By using an integrator with a constant k, a voltage proportional to the flowing current can be obtained

$$v_{OUT} = -NA\left(\frac{\mu_0}{2\pi r}\right) k \int_t \frac{\mathrm{d}i_C}{\mathrm{d}t}\,\mathrm{d}t + v_{OUT}(0) = -k\left(\frac{NA\mu_0}{2\pi r}\right) i_C + v_{OUT}(0). \quad (1.6)$$

The expression in eq. (1.6) would suggest that the coil can be used for measuring direct currents. However, the working principle is based on a flux change so this technique is only suitable for measuring alternated currents. It is possible to combine the Rogowski coil with a magnetic field sensor to extend its operating frequency range down to the DC. The accuracy of the measurement performed by means of the Rogowski coil could be deteriorated if the conductor is not perfectly centered inside the coil. The Rogowski coil has the advantages of having large bandwidth, being capable of measuring large currents, isolation and non-intrusive measurement. Furthermore, the absence of magnetic material avoids the problems of saturation and non-linearity. The sensitivity of the Rogowski coil is small compared to current transformers since it is air wound and so it cannot exploit the large permeability of the magnetic core material. The use of passive or active integration is dictated by a trade-off between maximum rise time (can be limited for active integration) and gain (low for passive integration). The sensitivity can be improved by increasing the number of windings or by increasing the gain of the integrator. Increasing the number of turns causes the self-capacitance of the coil to increase while a larger k factor requires a higher performance amplifier.

1.2.2 Current transformer

The current transformer is similar to the Rogowski coil in that it is based on the same physical principle. Typically, construction requires a single primary turn and several secondary turns. Differently from the Rogowski coil, it has a magnetic material core; the high permeability of the magnetic core material allows for an increased sensitivity. Another difference with respect to the Rogowski coil is the fact that the secondary of the CT is loaded with a sense resistor R_S and the voltage across it is proportional to the current flowing in the primary winding. A simple circuital model is shown in fig. 1.4.

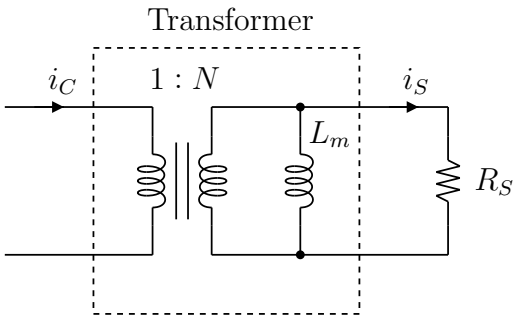

Figure 1.4: Circuit model of the current transformer.

The secondary current is given by

$$i_S = \frac{i_C}{N} - \frac{1}{L_m} \int_t v_S \, \mathrm{d}t \tag{1.7}$$

where i_C is the primary current i.e. the current to be measured, L_m is the magnetizing inductance, v_S is the secondary voltage. If the circuit is properly designed the secondary voltage has a zero average, otherwise the transformer saturates. This makes impossible for the current transformer to measure direct currents. The most important advantages of the current transformer are the isolated measurement and the fact that, being the output voltage proportional to the sensed current, there is no need for an integrator that would cause an accuracy degradation due to its offset drift. By choosing the number of secondary turns and the sense resistor value, the losses can be largely reduced and the output voltage can be made large enough so that it can easily be acquired by means of an A/D converter. The magnetizing current can cause an error in the measurement since it does not contribute to the secondary current flowing through the shunt resistor R_S. This effect can be minimized by either using a core with high permeability or by reducing the value of the sense resistor.

In some applications, like Peak Current Mode Converters, it is possible to use the Current Transformer to measure currents having a DC component. This is possible due to the fact that only the rising part of the current is interesting for the application, while during the descending part the core can be demagnetized. Current transformers are very popular in power conversion applications because of their low-cost and their ability to provide an output voltage that does not need further amplification.

1.3 Magnetic field sensors

Magnetic field sensors are able to sense both static and varying magnetic fields. They can be used in an open loop or closed loop fashion.

The open loop configuration represents a simple method for measuring currents. A sensor of this type is usually packaged as an SMD IC and it is placed close to the trace which carries the current. The working principle is based on the fact that the magnetic field around a conductor at a certain distance is proportional to the flowing current. This solution has the advantages of being low-cost, simple and compact. Some of the drawbacks are related to the fact that it is difficult to achieve good accuracy without performing a calibration. The most important limitation, however, is the susceptibility to external magnetic fields. External fields add to the wanted field and reduce the measurement accuracy. A magnetic core can be placed around the current carrying conductor for the purposes of both reducing the effect of unwanted magnetic fields as well as increasing the sensitivity of the sensor thanks to the high permeability of the magnetic material the core is made of. Core losses typically limit the measurement bandwidth below the maximum frequency of the magnetic field sensor.

In a closed loop configuration, the output voltage of the sensor is used to compensate for the core residual magnetization. This is done by forcing a current through a secondary winding, wound around the magnetic core as shown in fig. 1.5. This secondary current is proportional to the current flowing in the main conductor and it is forced through a sensing resistor, giving rise to an output voltage that is proportional to the sensed current. At high frequencies the secondary can work as a current transformer thus increasing the measurement bandwidth. In closed-loop configuration, since the magnetization is theoretically zero, there are no eddy currents or hysteresis losses.

Sensors belonging to this class have worse accuracy and bandwidth characteristics with respect to the Faraday effect based sensors. A Hall effect sensor and a current transformer can be combined to improve performances. This combination has lead to the active current probes. They are able to achieve an accuracy of about 2% and bandwidth in the order of 100 MHz [1] but on the other hand they present an

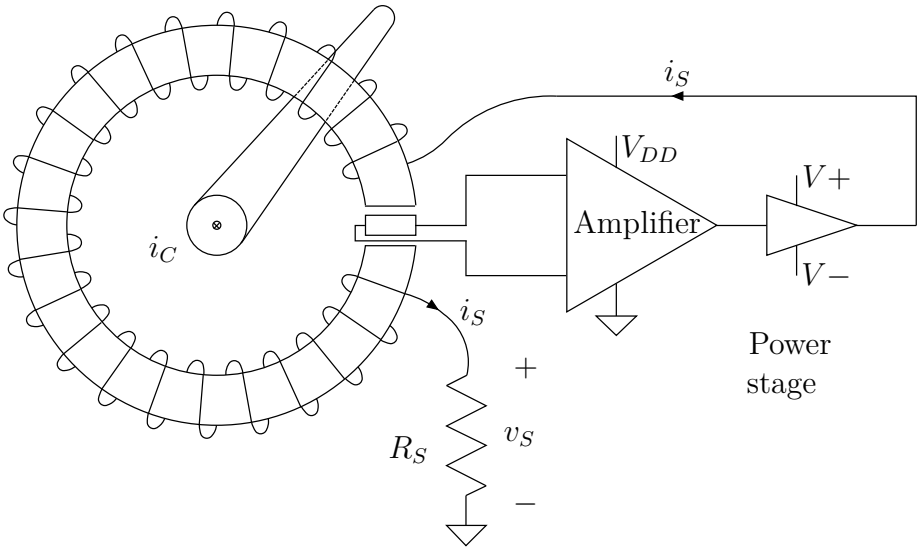

Figure 1.5: Closed-loop magnetic sensor.

increased complexity, size and cost.

1.3.1 Hall-effect sensor

Hall-effect sensor is one of the most popular magnetic field sensors. It is based on the Hall effect so it provides at the output a voltage that is proportional to the external magnetic field that is, in turn, proportional to the current that generates it

$$V_H = \frac{IB}{nqd} \tag{1.8}$$

where I is the bias current, B is the external magnetic field, n is the carrier concentration, q is the elementary charge and d is the thickness of the material. The material properties are usually enclosed in the coefficient R_H

$$R_H = \frac{1}{nq}. \tag{1.9}$$

The material thickness d is a trade-off between sensitivity and resistance (losses). One problem is that the magnetic field also penetrates the area enclosed by the sensing wires and the induced voltage reduces the measurement accuracy. A simple trick to solve this problem consists in building a second loop with the same area but opposite polarity so that the two induced voltages cancel out. Additional circuitry is required to use the Hall-effect sensor as a current sensor because of an offset which is present at the output when the input is at zero. The accuracy is medium (5% [1]) when used in open loop and it is high (0.5% [1]) when used in closed loop. Hall effect sensors are very popular because of the low cost and compact size. Furthermore, they can be fabricated using a conventional CMOS technology. Hall effect sensors usually operate in closed loop in order to achieve good accuracy and large measurement range (up to kA [1]).

A current sensor that exploits the Hall effect is based on the MagFET [6]. The MagFET is a Field Effect Transistor having the drain region split in two parts. In the absence of external magnetic field the drain current equally splits between the two regions. However, if a magnetic field is present close to the device, the two currents become unbalanced due to Hall effect and their difference is proportional to the external field. Typically, the trace carrying the current to be measured is placed close to the MagFET and the differential drain current is amplified by means of a transresistance amplifier (fig. 1.6). This amplifier is able to achieve a good immunity

to external disturbances.

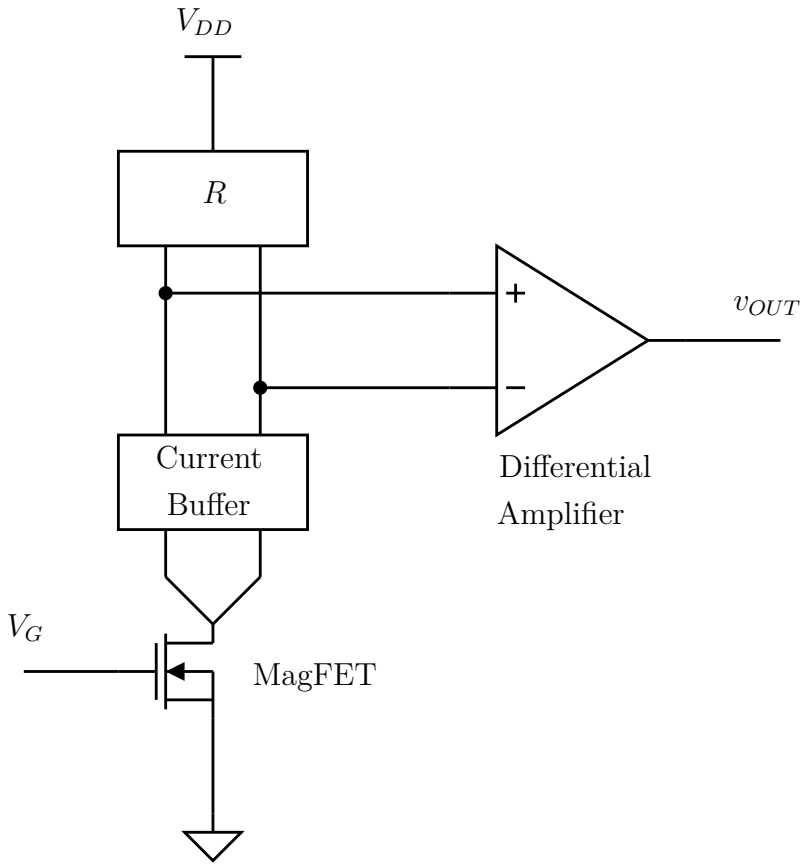

Figure 1.6: MagFET sensor conceptual scheme.

1.3.2 Fluxgate sensor

Sensors based on fluxgate technology are among the most accurate magnetic field sensors available today. Its basic working principle exploits the nonlinear relationship between the magnetic field H and magnetic flux density B inside a magnetic material. An excitation current is forced through a winding and as a result a magnetic field H_0 is generated (fig. 1.7). The excitation magnetic field is in opposite direction in the two rods so the pickup winding does not see the magnetic field generated by the excitation winding. A voltage v_S is induced in the pickup winding and it is proportional to the

difference between the time derivative of the flux in the two rods

$$v_S = -2NA\left(\frac{\mathrm{d}B_1}{\mathrm{d}t} + \frac{\mathrm{d}B_2}{\mathrm{d}t}\right). \tag{1.10}$$

If a sinusoidal current is used to drive the exciting winding, the time dependent rate of change in each core can be written in terms of the permeability μ

$$\mu = \frac{\mathrm{d}B_{H_{ext}\pm H_0}}{\mathrm{d}\left(H_{ext} \pm H_0\right)}. \tag{1.11}$$

The permeability is a function of the electric field. Combining 1.10 and 1.11 yields

$$v_S = -2NA\left(\mu_1\frac{\mathrm{d}\left(H_{ext} + H_0\right)}{\mathrm{d}t} + \mu_2\frac{\mathrm{d}\left(H_{ext} - H_0\right)}{\mathrm{d}t}\right) \tag{1.12}$$

and if the external field is static, 1.12 becomes

$$v_S = -2NA\frac{\mathrm{d}H_0}{\mathrm{d}t}\left(\mu_1 - \mu_2\right) = -2NA\frac{\mathrm{d}H_0}{\mathrm{d}t}\mu_d \tag{1.13}$$

where $\mu_d = \mu_1 - \mu_2$ is the differential permeability. Provided that the external field is small with respect to the excitation field, the output voltage has a peak value proportional to the magnitude of the external field. Sensitivity can be improved by increasing the frequency of the input current, increasing the number of turns or by using a magnetic material with a rectangular B-H characteristic. The bandwidth of the measurement is limited by the time needed to drive the magnetic core from negative to positive saturation and vice-versa. In order to increase the bandwidth, a current transformer can be used in combination with the fluxgate sensor.

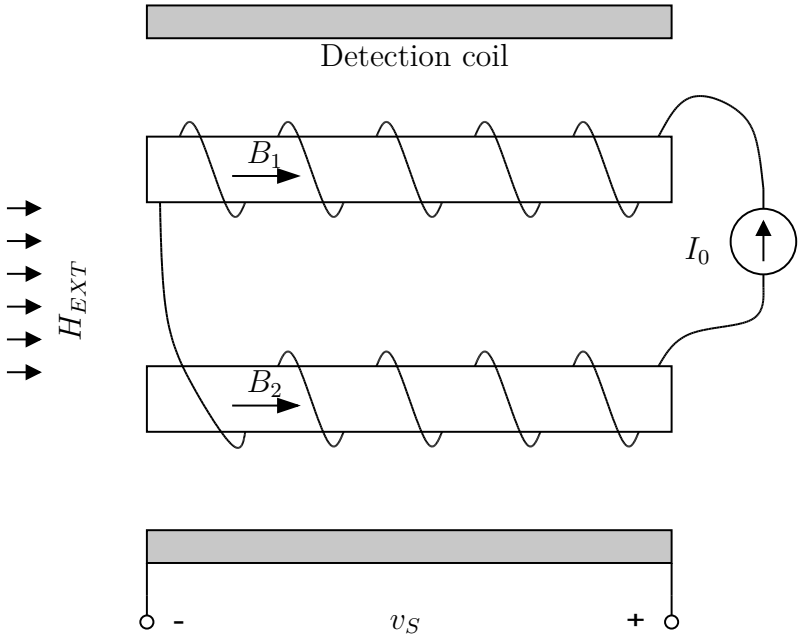

Figure 1.7: Current sensor structure based on Vacquier fluxgate principle.

1.3.3 Magneto Resistance effect

Magneto Resistance effect sensors are structures in which the electrical resistance varies as a function of a magnetic field. This makes them suitable to be used as magnetic field sensors hence as current sensing devices. There are several types of MR effect sensors and they have advantages such as the possibility of integration in ICs but their main drawbacks are the non linearity and the thermal drift. Anisotropic Magneto Resistance (AMR) sensors are based on the dependence of the resistance encountered by a current, on the angle between current direction and magnetization direction [7]. The external magnetic field is applied perpendicular to the initial magnetization direction and this causes the resulting magnetization to vary its direction fig. 1.8. The variation of the angle between the direction of the current and the resulting magnetization gives rise to a resistance variation. AMR sensors have low sensitivity ($\frac{\Delta R}{R} \approx 2\% - 4\%$) [8], high thermal drift and high non-linearity. Giant Magneto Resistance (GMR) offer an improvement in the sensitivity ($\frac{\Delta R}{R}$ up to 12.8%) [8], allowing for the sensing of weaker magnetic fields with respect to the AMR sensors. A GMR sensor is, in its simplest form, a four layer structure that is made of two thin ferromagnets separated by a sheet of conductor material (fig. 1.9). The fourth

layer is made of antiferromagnetic material and one of the ferromagnetic layers has its magnetization pinned to it. The magnetization of the free ferromagnetic layer, instead, is oriented by the external magnetic field. The resistance of the structure depends on the orientation of the two magnetizations with respect to one another, so it varies with the external magnetic field. Although GMR sensors improve sensitivity, they suffer from the same problems of non-linear behaviour and high thermal drift as AMR sensors. This has limited their use, in the past years, to digital applications such as the reading operations in magnetic recording. At present, GMR current sensors are typically placed in a Wheatstone bridge topology to improve the sensitivity and minimize the temperature dependent effects. The physical structure of GMR sensors makes them suitable for integration in ICs.

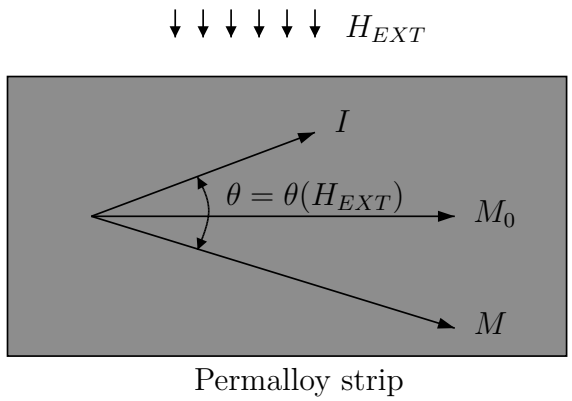

Figure 1.8: AMR structure.

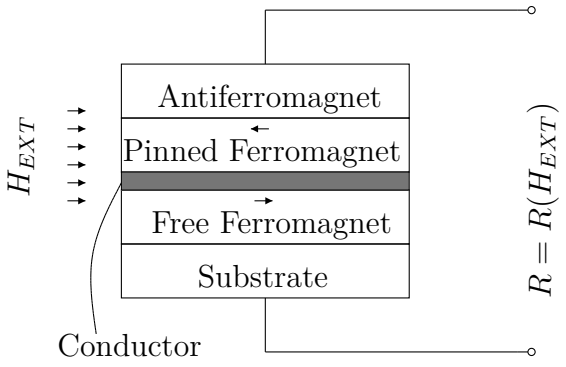

Figure 1.9: GMR structure.

1.4 Faraday effect

Faraday effect sensors working principle is based upon the ability of birefringent materials to change the polarization of light propagating through them. Circular birefringence materials change the polarization of linear polarized light and maintain the polarization of circular polarized light while linear birefringence materials behave in the opposite way [9]. Faraday discovered that a magnetic field applied parallel to the light propagation direction, can induce circular birefringence. If linearly polarized light is sent through a material having small intrinsic circular birefringence, the rotation plane of the polarization of the light is proportional to the line integral of the magnetic field

$$\theta = V \int \vec{H} \cdot \mathrm{d}\vec{s} \tag{1.14}$$

where V is the Verdet constant which is a property of the medium and it indicates the strength of the Faraday effect. The rotation θ can be measured with the polarimeter detection method or by using the interferometer detection method. The basic scheme of the polarimeter detection measurement setup is shown in fig. 1.10. The wire carrying the main current is sent through a fiber-optic coil with N turns and linearly polarized light is fed into the coil. The intensity of the light at the output is measured and it is related to the input light intensity by

$$I_d = \frac{I_0}{2}\left(1 + \sin 2\theta\right) \tag{1.15}$$

where θ is directly proportional to the current flowing in the wire and it can be evaluated by using Ampere's law

$$\theta = VNi_C. \tag{1.16}$$

An alternative measurement technique is the interferometer detection method; the setup is shown in fig. 1.11. Two circular polarized waves are fed into the either end of the fiber-optic coil that encloses the main current conductor. The two waves are converted back to linearly polarized light at exiting the coil and they are processed by the Sagnac interferometer [10]. The differential phase shift between the two waves

is given by [11]

$$\Delta\theta = VN \oint_C \vec{H} \cdot \mathrm{d}\vec{s} = 2VNi_C. \tag{1.17}$$

The detected intensity resulting after interference is

$$I_d = \frac{I_0}{2}\left(1 + \cos\Delta\theta\right) \tag{1.18}$$

where I_d is the intensity of the input light [11].

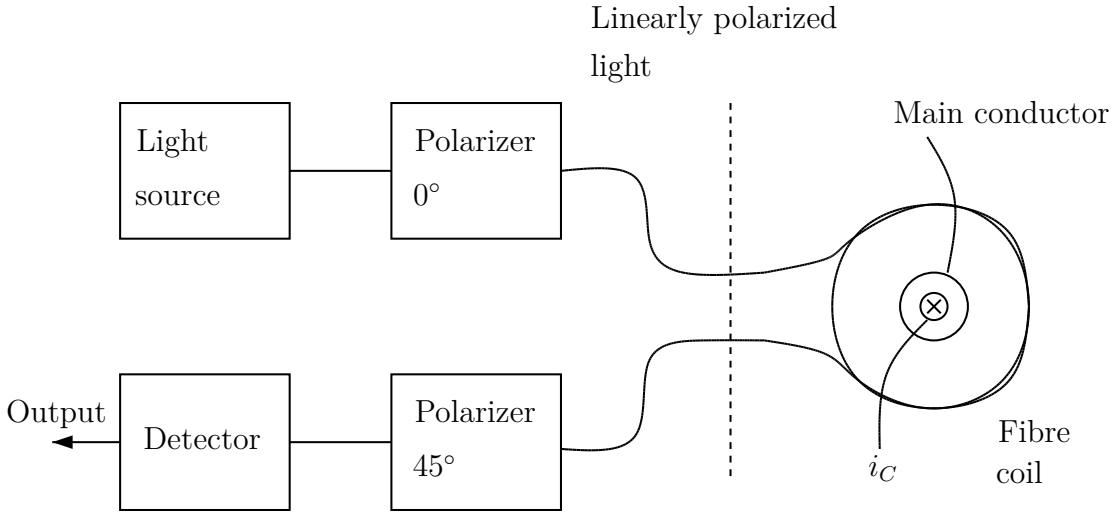

Figure 1.10: Polarimeter detector.

In order to avoid stress on the fiber optic cable (which would cause variations in the Verdet constant), the cable must be packaged in a way such that it is protected from mechanical stress. Fiber optic current sensors are a good alternative to traditional current transformers and Hall effect sensors in power distribution applications, where isolation is a critical parameter. They greatly reduce power consumption and physical dimensions compared to alternative technologies for similar current ratings. However, due to large cost and complexity these sensors are not used for low current measurements.

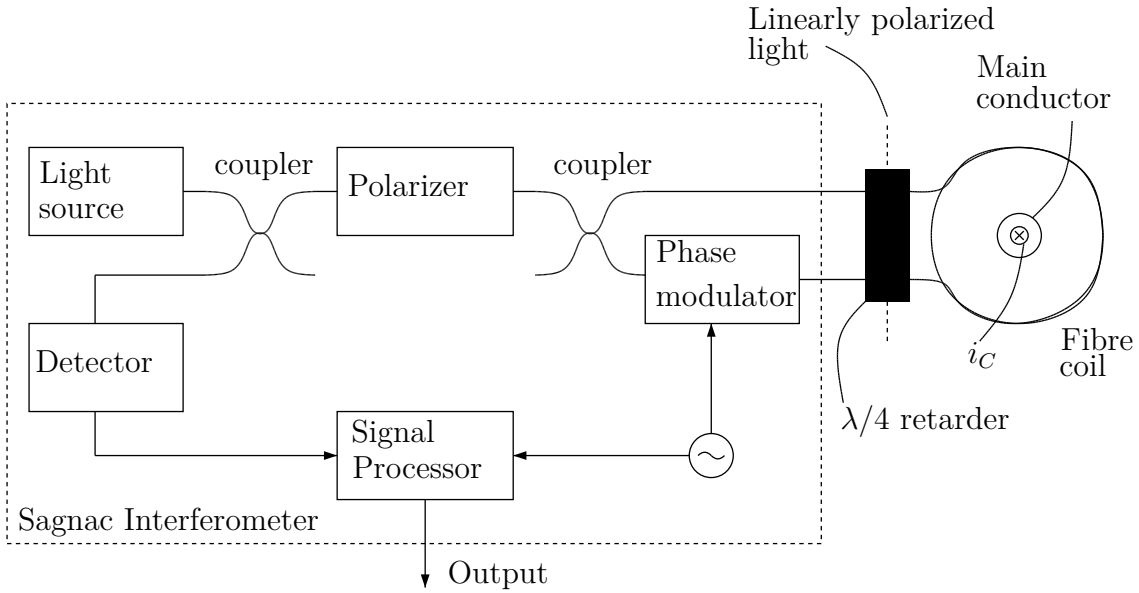

Figure 1.11: Interferometer detector.

1.5 Comparison

A comparison between the different current sensing techniques shows that for large bandwidth measurements ($\sim$ MHz) possible solutions can be the shunt resistor, current transformer, Rogowski coil, Faraday effect current sensors. Shunt resistors become troublesome for high current measurements due to power loss. Hall effect sensors provide an alternative with low power losses and galvanic isolation but at a much higher price. For higher performance, closed-loop AMR-based current sensors or Rogowski coils can be used but due to their high price are only suitable for specific applications. Current transformers and Rogowski coils are very popular in power electronics systems. These techniques provide galvanic isolation and good accuracy. The most suitable for being integrated in power modules are the shunt, Rogowski coil and the MGR sensors.

CHAPTER 2

Resistive shunt current sensing

Resistor based current sensing systems are very common. They have advantages such as simplicity and the ability to measure both AC and DC currents. One important aspect of these kind of systems is the fact that the sensing resistor can be integrated in a traditional CMOS process. In fact, shunt resistors have been reportedly realized [12] by paralleling several metal layers. Many aspects are important when designing the integrated resistor such as the physical dimensions, the material properties and the connection to the measurement circuitry. A low TCR metal has to be used and the shunt must be able to carry the maximal current. A 4 terminals Kelvin connection is needed in order to achieve a good accuracy. An entirely integrated measurement chain allows for more compact solutions and also is less susceptible to external disturbances. These kind of circuits typically comprise a conditioning amplifier and an analog to digital converter.

2.1 Design choices

For the current work, a shunt resistor is chosen due to its simple operating principle, low cost, large bandwidth as well as the ability to sense both direct and alternated currents. The acquisition chain is designed to comply with specifications on the measurement bandwidth and resolution. Conditioning a large dynamic range signal is a challenging task in that an acceptable accuracy must be guaranteed on the whole measurement range; the other issue is related to the amplitude of the smallest signal to be amplified which can be comparable to the offset of the amplifier and it can

easily be covered by noise. The current to be measured is bipolar with maximum value 20 A and bandwidth equal to 1 MHz. The available supply voltage is 3 V and the signal is to be digitized on 12 bits. Near the zero crossing, currents down to 1 mA have to be measured.

2.2 Conventional current sensing circuit

A standard solution is the one shown in fig. 2.1, used for high side current sensing.

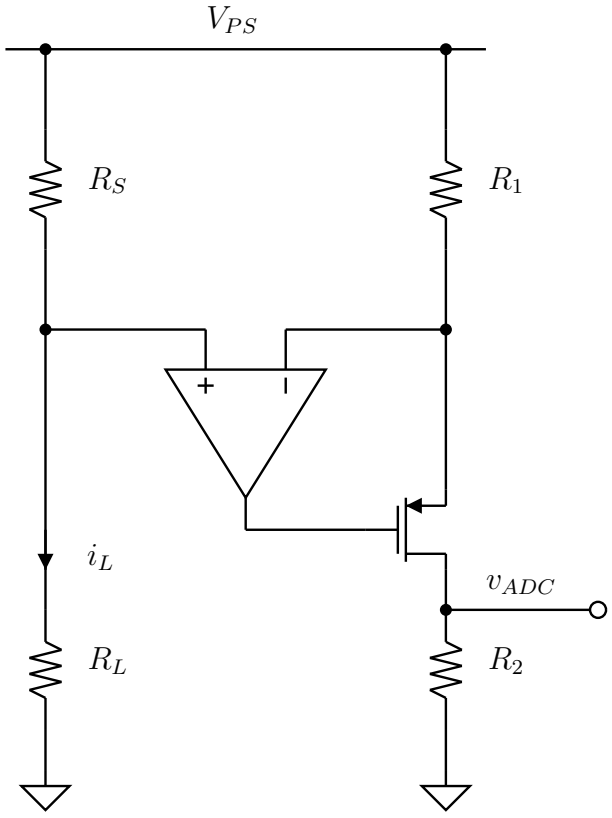

Figure 2.1: High side current sensing.

The circuit operation is as follows: the current to be measured flows in the load R_L and in the sensing resistor R_S. All considerations discussed above about the choice of R_S are valid. The resulting voltage

$$v_S = R_S i_L \tag{2.1}$$

is forced across R_1 by the operational amplifier hence the current flowing through the pMOS is

$$i_1 = i_L \frac{R_S}{R_L} \tag{2.2}$$

so the range of the current i_1 is determined by the ratio of the two resistors. Current i_1 is then forced through resistor R_2 giving rise to the voltage

$$v_{ADC} = i_L R_S \frac{R_2}{R_1}. \tag{2.3}$$

This voltage is digitized by an ADC converter.

2.3 Design

In order to analyze the limitations of this topology, components have been sized to comply with the requirements of the current project. R_S is fixed at $10\,\mathrm{m\Omega}$ and the load current (unipolar) in the range $(0, 20\,\mathrm{A})$ is to be digitized on 11 bits. For a bipolar current two circuits are needed, one for each polarity.

Assuming that the load current can be scaled by a factor 10^4, the value of R_1 is extracted by the following relation.

$$\frac{R_1}{R_S} = 10^4 \Rightarrow R_1 = 10^4 \cdot R_S = 100\,\Omega. \tag{2.4}$$

If the ADC range is $(0, 3\,\mathrm{V})$, the value of R_2 is calculated so that the SNR_q is maximal, which means that the resulting voltage covers the whole range of the ADC

$$R_2 = \frac{3\,\mathrm{V}}{20\,\mathrm{A}} 10^4 = 1.5\,\mathrm{k\Omega}. \tag{2.5}$$

2.3.1 Resolution

The system resolution is limited by the quantization step amplitude

$$i_{Lq} = \frac{i_{L,max}}{2^{11}} = 9.77\,\mathrm{mA}, \tag{2.6}$$

hence the system in exam is not suitable for the measurement of wide dynamic signals. There are different possible solutions to the problem of wide range signal

measurement. One possible solution would be that of using two sense resistors in series. At large current one of the resistors is shorted while at low current both resistors are in the main path so that the sensed voltage increases. The alternative solution is to perform a gain change in the current sensing amplifier. This could lead to the use of a PGA controlled by a μC or to a nonlinear gain characteristic amplifier.

2.3.2 Frequency limitation

The effects of the operational amplifier bandwidth limitation are analyzed in the following. In table 2.1the parameters used for the operational amplifier are shown

A_{d0}	10^5
GBW	10 MHz

Table 2.1: OA parameters.

and the frequency response is assumed to be a first order one as shown in fig. 2.2.

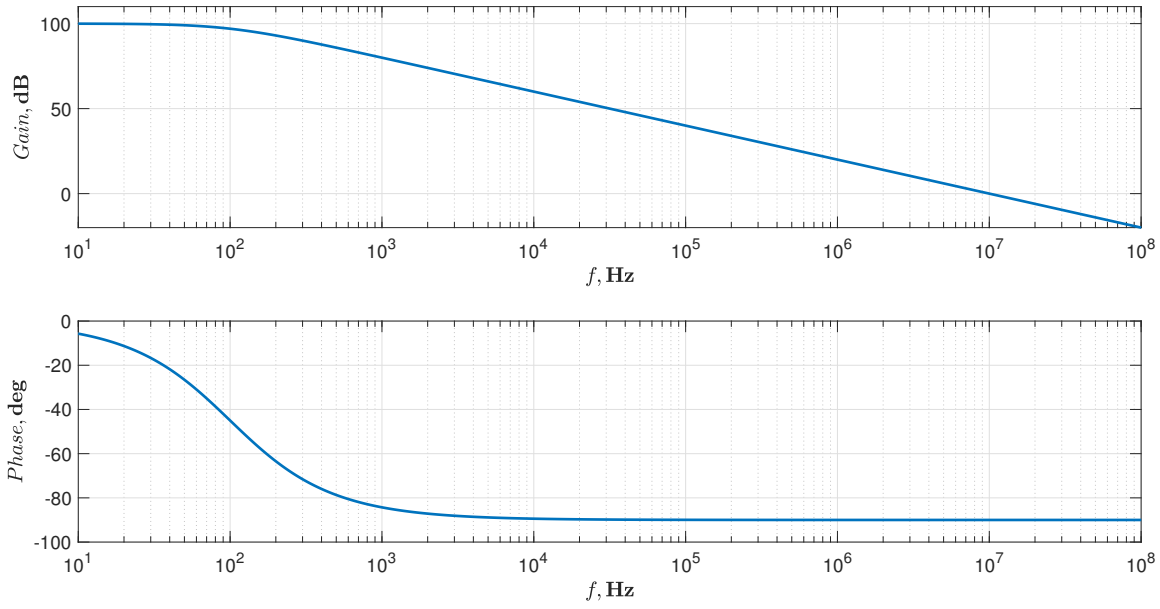

Figure 2.2: Single pole frequency response.

The system bandwidth is first evaluated by hand, in a simplified manner and afterwards simulated with SPICE. For the frequency response evaluation the contribution of the pMOS capacitances is neglected. This is equivalent to saying that

the only frequency limitation of the system is due to the low pass behavior of the operational amplifier open loop gain.

The small signal equivalent circuit is shown in fig. 2.3.

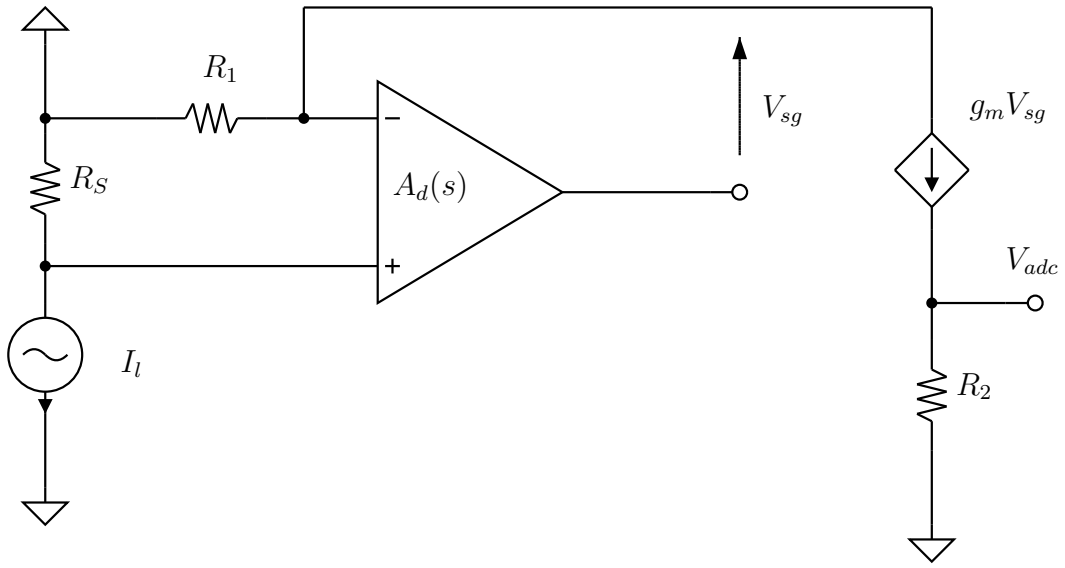

Figure 2.3: Small signal equivalent circuit.

where

$$A_d(s) = \frac{A_{d0}}{1 + \frac{s}{s_{p0}}} \tag{2.7}$$

and s_{p0} is the complex frequency of the pole. The closed loop amplification can be calculated by means of the Rosenstark's [13] formula

$$A_F(s) = \frac{V_{adc}}{I_l} = \frac{A_\infty(s)T(s) + A_0(s)}{1 + T(s)}. \tag{2.8}$$

$A_\infty(s)$ and $A_0(s)$ are given by

$$A_\infty(s) = R_S \frac{R_2}{R_1} \left(\frac{A_d(s)}{1 + A_d(s)} \right) \tag{2.9}$$

$$A_0 = 0 \tag{2.10}$$

while the return ratio is evaluated from the circuit shown in fig. 2.4

$$T = -\frac{g_m V_{sg}}{I_p} = g_m R_1 (1 + A_d(s)). \tag{2.11}$$

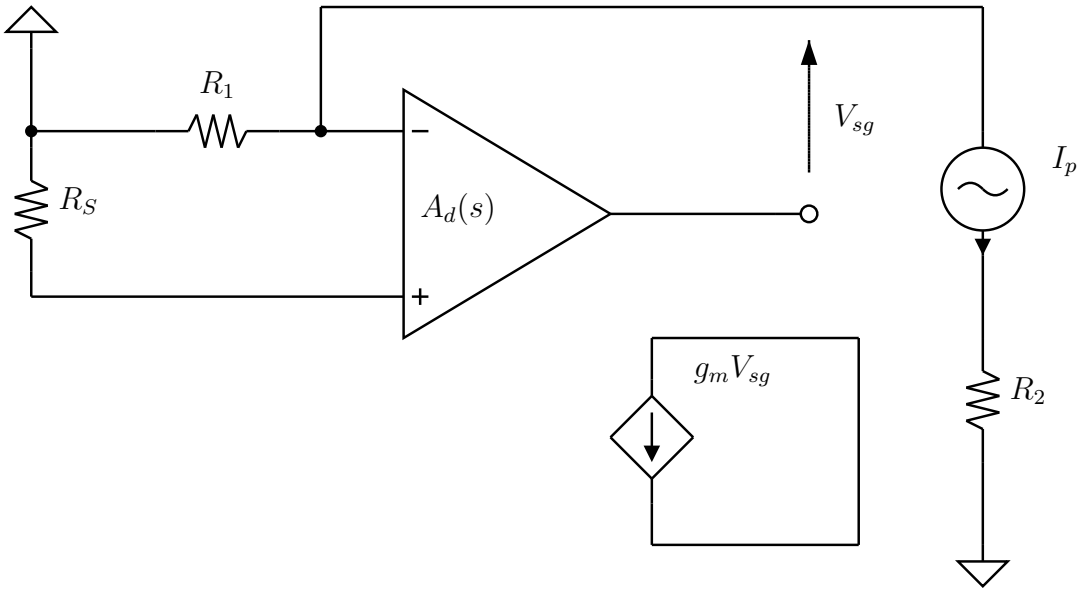

Figure 2.4: Small signal equivalent circuit for the evaluation of the return ratio.

The closed loop gain is then given by

$$A_F(s) = \frac{V_{adc}}{I_l} = R_S \frac{R_2}{R_1} \left(\frac{A_d(s)}{1 + A_d(s)} \right) \left(\frac{T(s)}{1 + T(s)} \right). \tag{2.12}$$

In order to carry out the simulations a MOSFET with the following parameters (table 2.2) was used

V_{Tp}	$-0.7\,\mathrm{V}$
$\mu_p C_{OX}$	$50\,\mu\mathrm{A/V^2}$
$\frac{W}{L}$	20

Table 2.2: pMOS parameters.

Using the strong inversion relation for the MOSFET, the transconductance is

given by

$$g_m = \sqrt{2\mu_p C_{OX} \frac{W}{L} i_D} \tag{2.13}$$

where μ_p is the mobility of the holes, C_{OX} is the specific gate capacitance, $\frac{W}{L}$ is the transistor aspect ratio and the drain current is the same as the current flowing through R_1.

In fig. 2.5 the return ratio, calculated in eq. (2.11), is shown at 4 different load currents. It can be noticed that the loop gain decreases as the load current decreases. This is due to the decrease of the MOSFET transconductance. In fig. 2.6 the closed loop gain is plotted for the same load current values. The effect of the loop gain decreasing with the load current is a shifting of the pole to lower frequencies hence a bandwidth reduction.

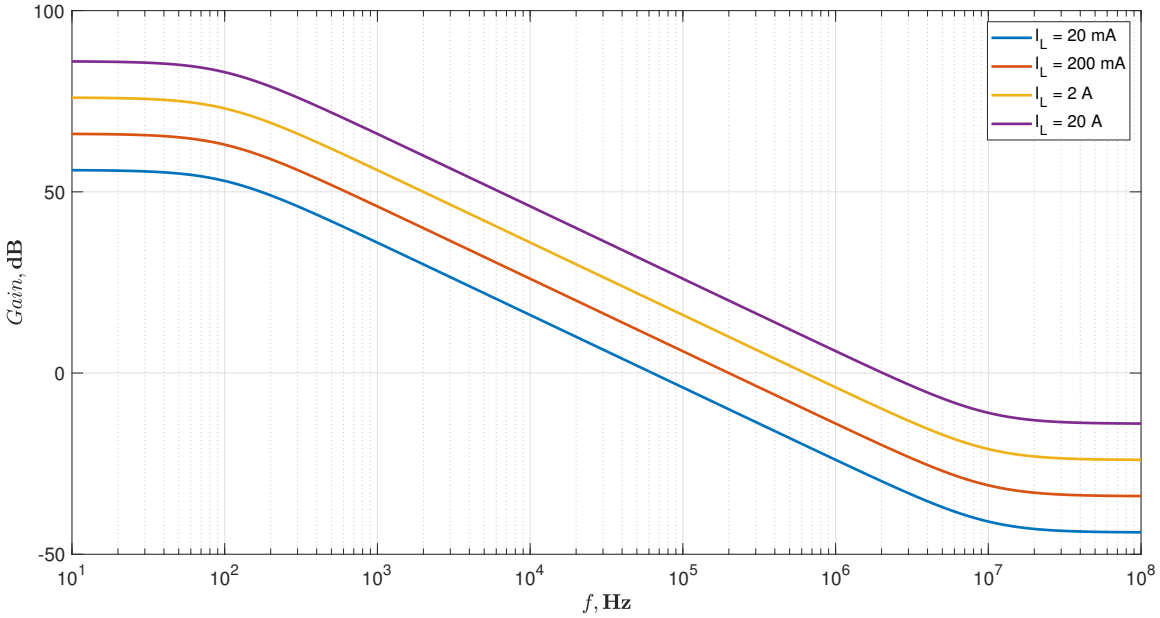

Figure 2.5: Calculated loop gain at different load currents.

This result is verified through a SPICE simulation of the circuit shown in fig. 2.7. The graph in fig. 2.8 shows the frequency response of the closed loop gain at different load currents and the bandwidth reduction as the load current decreases is obvious.

These simple calculations show the limitations of this current sensing system; both resolution and frequency limitation strongly depend on the dynamic range of the signal to be measured. In fact, employing uniform quantization with a fixed

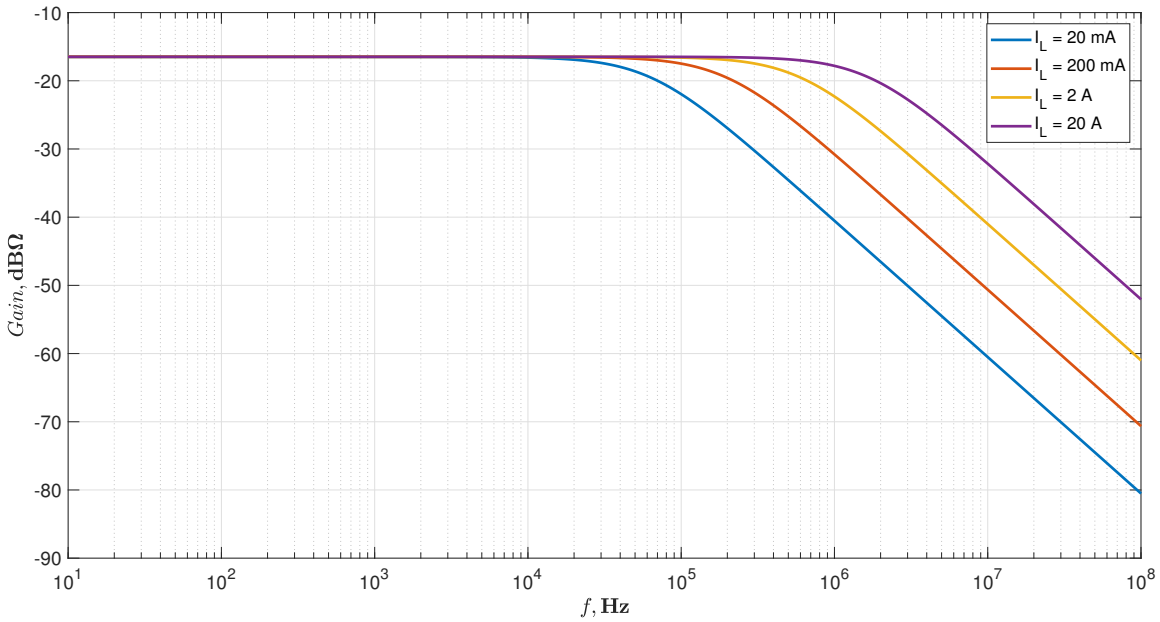

Figure 2.6: Closed loop gain at different load currents.

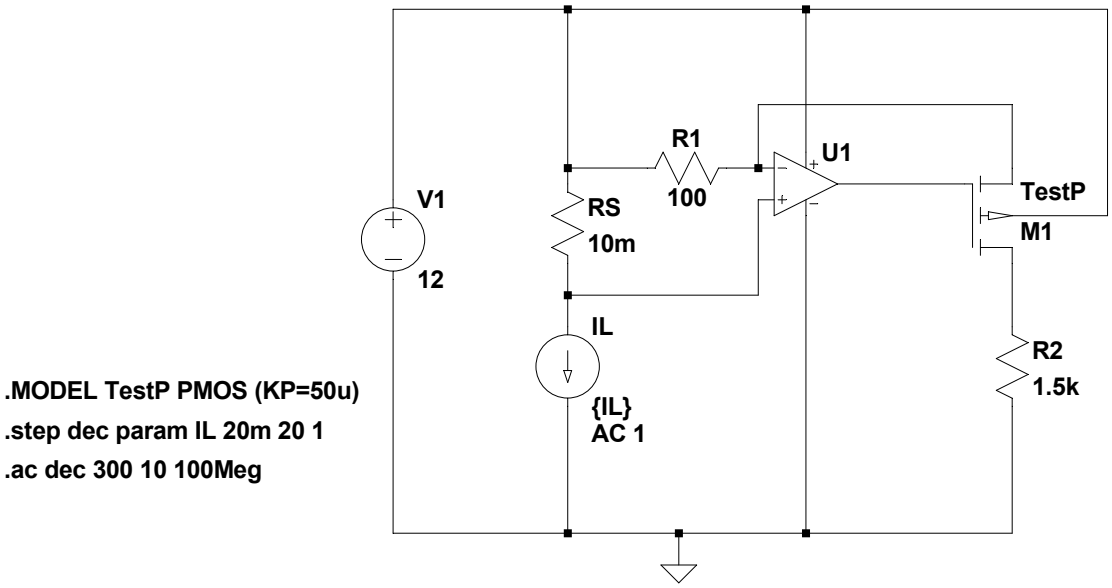

Figure 2.7: LT SPICE circuit.

number of bits leads to a fixed quantization step size and small amplitude signals are measured with a poor accuracy or cannot be measured at all. In turn, also the frequency limitation is related to the signal dynamic range: the larger the range to

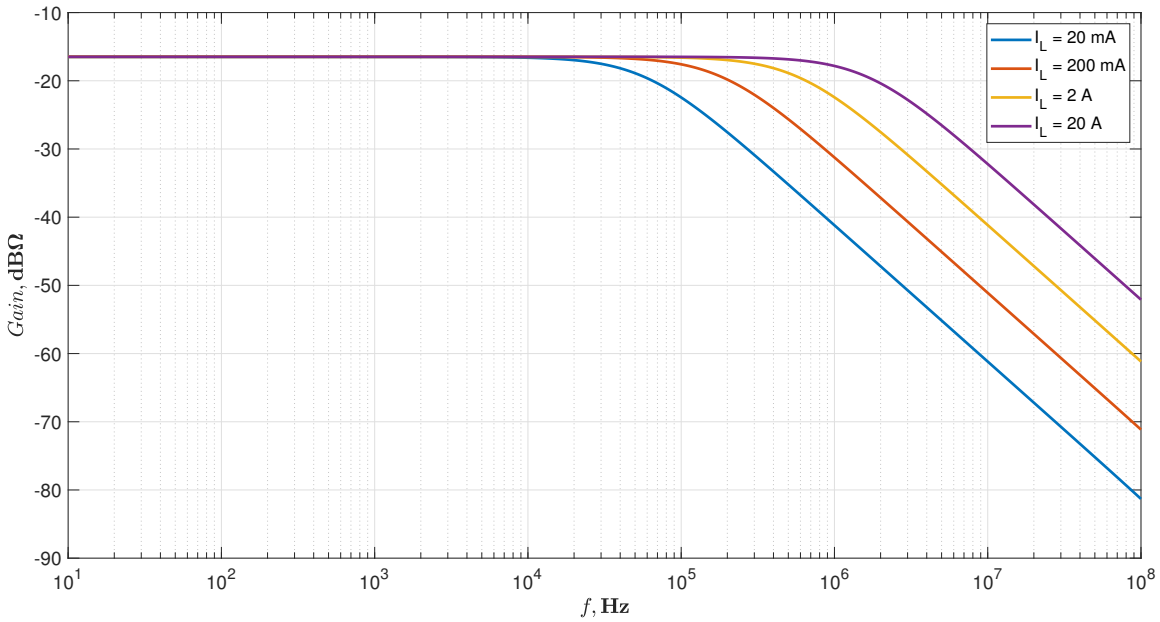

Figure 2.8: Frequency response of fig. 2.7 simulated with LT SPICE

be covered the larger the loop gain variation (it is due to the g_m variation which depends on the input signal) and so also the bandwidth reduction increases. In the next chapter these two problems will be addressed by the introduction of a nonuniform quantization scheme which allows for variable quantization step size and a compressed range of variation of the input signal that translates in a smaller bandwidth variation.

CHAPTER 3

System description

In the previous chapter it was pointed out that uniform quantization leads to resolution and bandwidth limitations when wide dynamic range signals are to be acquired. Nonuniform quantization can be employed in these cases. Nonuniform quantization is useful to overcome the resolution limitation which is related to the number of bits of the converter and, at the same time, compress the range in which the signal varies hence allowing for bandwidth limitation improvement. Indeed, the bandwidth limitation in a gain varying system can be a problem, specially when the gain of the amplifier must vary in a very large range. One way to achieve nonuniform quantization is to compress the signal with a nonlinear conditioning amplifier followed by a uniform quantizer; the required steps for nonuniform quantization will be described further on.

The block scheme of the proposed system is shown in fig. 3.1. The load current flows through the sense resistor and the resulting voltage is processed by the analog circuitry. The analog to digital conversion is implemented by means of a pulse counting scheme. A gating signal with duration proportional to the voltage to be converted is used to enable a counter which counts the pulses of a fixed frequency clock signal. At the end of each conversion cycle, the counter value is latched into an output register. The output code is composed by appending to the counter value (in the MSB position, acting as a sign bit) the output of a comparator placed at the input which acts as a polarity detector. The advantage of such a system is given by the fact that the output data is already in digital form hence a dedicated A/D

converter is not needed. This means that the data could also be used for on-chip processing. The various blocks will be presented in the following.

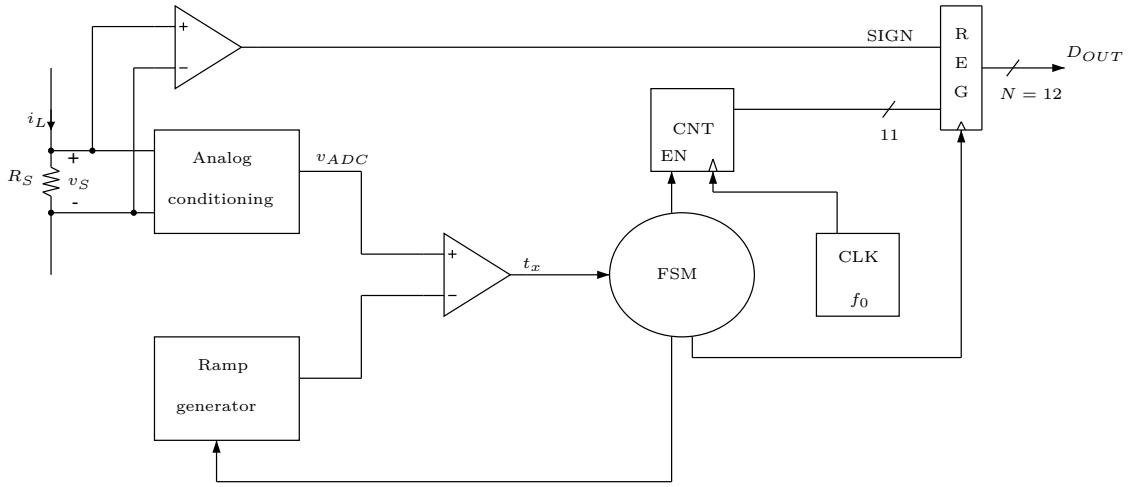

Figure 3.1: Block scheme of the system.

3.1 Nonuniform quantization

Signal conversion in a data acquisition system implies quantization in both time and amplitude. Both these operations tend to cause the accuracy of the system to deteriorate. Quantization in amplitude causes a loss of information in the analog to digital conversion process. This is due to the fact that a finite number of digits has to be used to represent a sampled variable. The characteristic of a uniform quantizer is shown in fig. 3.2.

It can be expressed as

$$x_q = nq, \quad (n - \frac{1}{2})q \leq x < (n + \frac{1}{2})q \tag{3.1}$$

where x is the input quantity, x_q is the output and q is the quantization step. Uniform quantization results in small relative errors when large amplitude signals are converted. However, in the conversion of small amplitude signals only few quantization levels are used hence large relative errors are introduced. If a large dynamic range signal is to be converted with a small number of bits, nonuniform quantization can be employed. The need for nonuniform quantization arises in those cases where

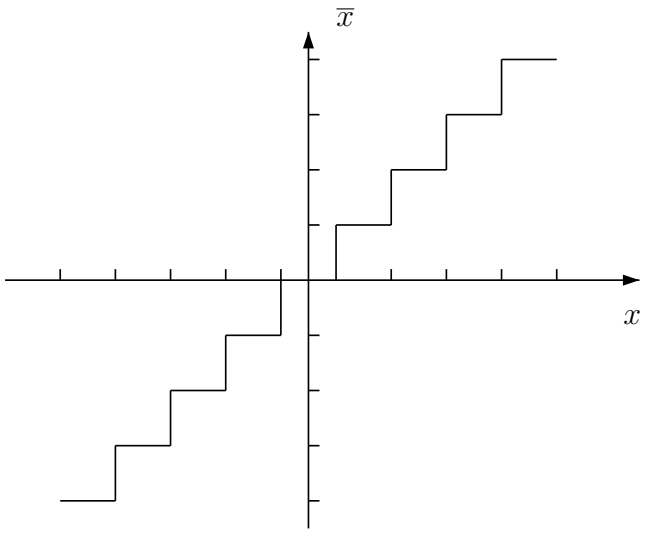

Figure 3.2: Uniform quantization

the range of the signal to be acquired is very large and the smallest signal to be measured is not able to excite a single quantization interval. Nonuniform quantization can provide fine quantization of the weak signals and coarse quantization of the strong signals ([14], [15], [16]). Thus, in the case of nonuniform quantization, quantization noise can be made proportional to signal size.

There are several ways to achieve nonuniform quantization of a signal. The most straightforward is the one based on the nonlinear conditioning of the input signal (compression). For small magnitude signals, the compression characteristic has a much steeper slope than the slope for large magnitude signals. Thus, a given signal change at small magnitudes will carry the uniform quantizer through more steps than the same change at large magnitudes. After compression, the distorted signal is used as an input to a uniform quantizer. The non uniformly spaced levels are obtained after applying the inverse compression characteristic (expansion); this operation is typically done in software. The required steps for nonuniform quantization are qualitatively illustrated in the following fig. 3.3 and fig. 3.4.

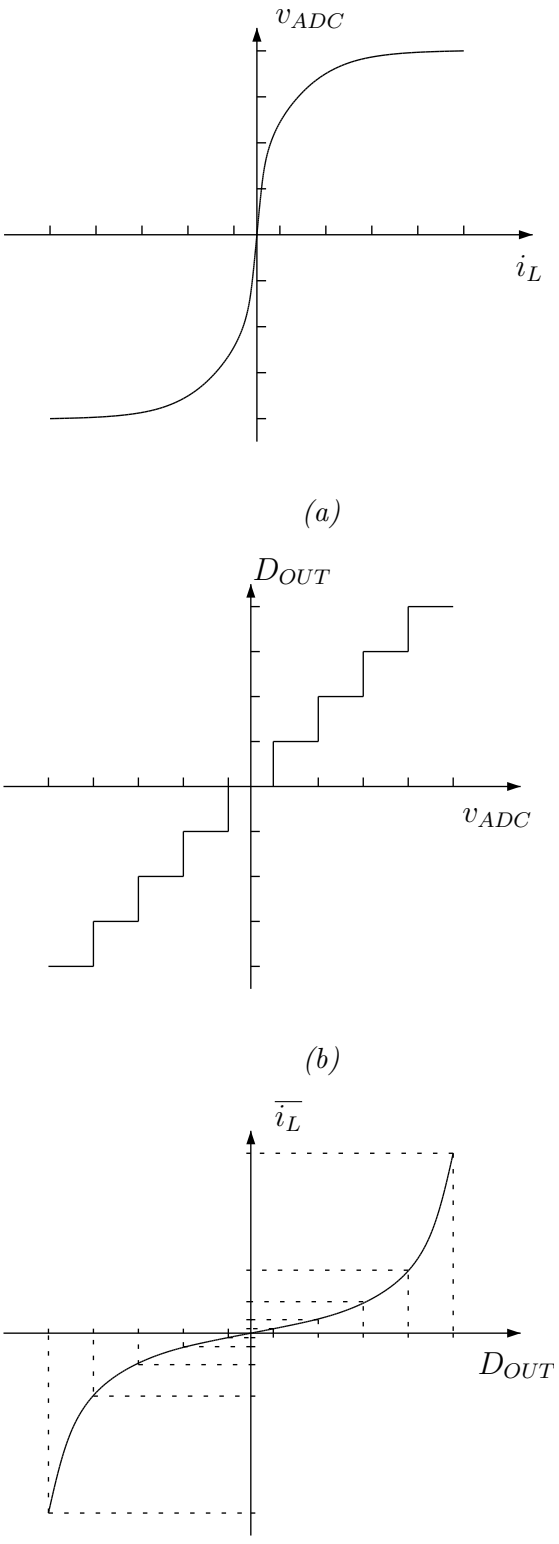

Figure 3.3: Nonuniform quantization: (a) compression, (b) uniform quantization, (c) expansion.

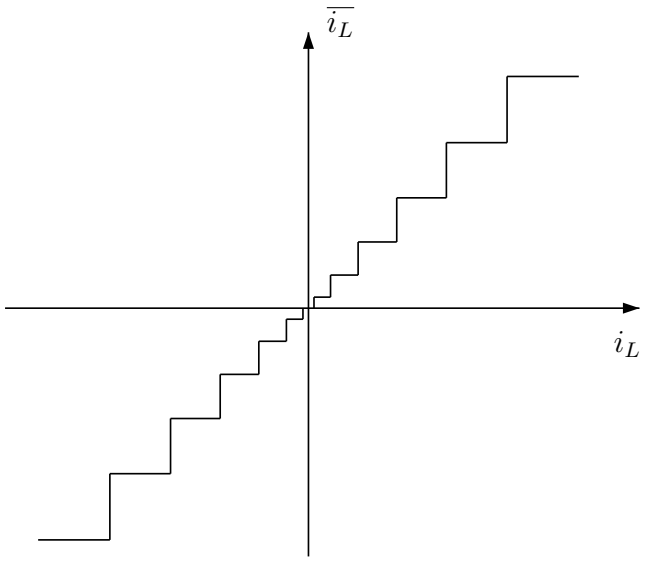

Figure 3.4: Nonuniform quantization.

3.2 Analog conditioning circuitry

The analog conditioning circuit (block scheme shown in fig. 3.5) is made of two blocks: a first block used to rectify the input signal and a second block performing signal compression. The first block is needed since the input signal is bipolar and the same nonlinear characteristic has to be applied to both positive and negative signals. For this reason a comparator is placed at the input in order to detect the polarity of the input signal and feed this information directly to the output register. The logarithmic amplifier is used to compress the signal dynamic thus allowing for nonuniform quantization.

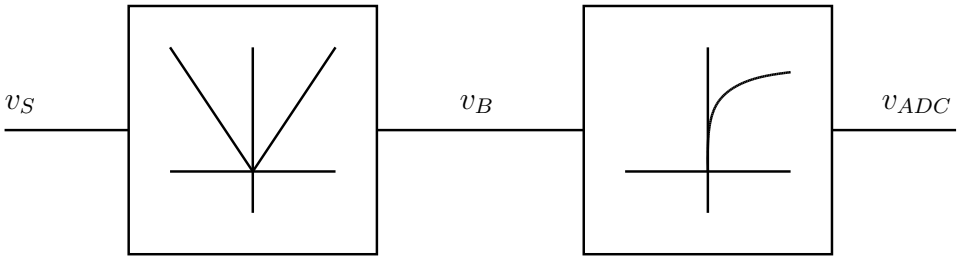

Figure 3.5: Analog conditioning circuit - block scheme.

The load current is translated into a voltage by means of the shunt resistor R_S. $R_S = 10\,\mathrm{m\Omega}$ provides a maximum voltage of 200 mV at maximum load current $i_L = 20\,\mathrm{A}$(fig. 3.6). A functional level (operational amplifiers) schematic of the rectifier is shown in fig. 3.7. It's output acts as an input to the logarithmic amplifier which is shown in fig. 3.8. The complete circuit is shown is fig. 3.9. This circuit has been used for the spectre simulations in order to define the requirements for the operational amplifiers.

AC simulations show the huge impact that the GBP (Gain-Bandwidth product) of I_4 has on the overall frequency response. This is due to the fact that I_4 operates as an inverting amplifier with a variable gain since a nonlinear element is present in its feedback loop (fig. 3.10). This means that the feedback impedance is not constant and it is given by the dynamic impedance of the diode

$$Z_{diode} = \frac{\partial v_D}{\partial i_D} = \frac{V_T}{i_D}. \tag{3.2}$$

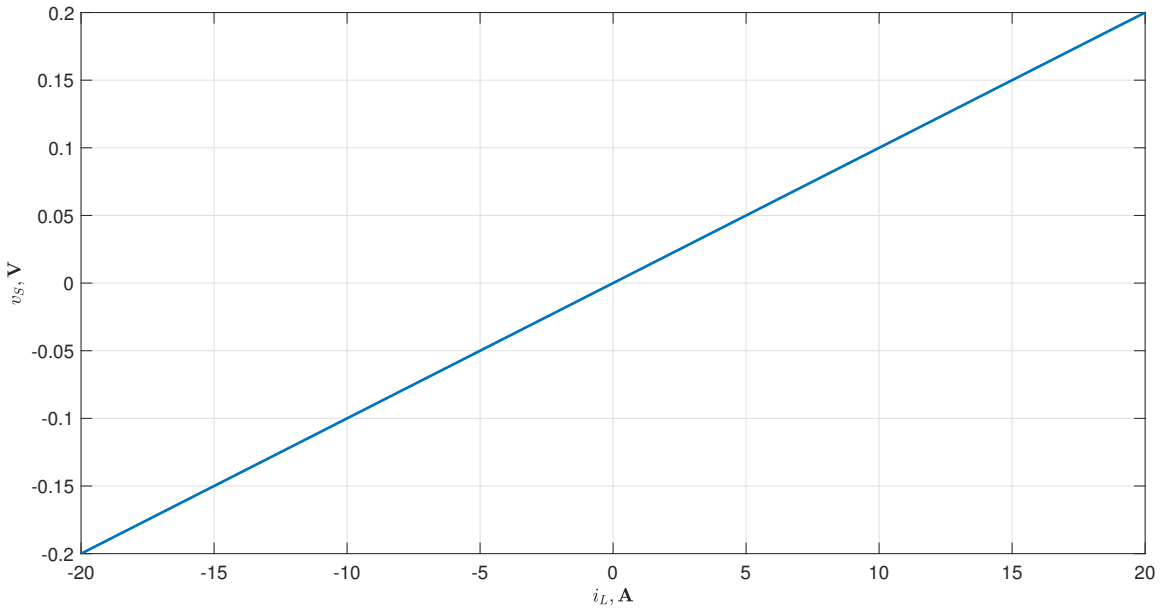

Figure 3.6: Sense resistor characteristic.

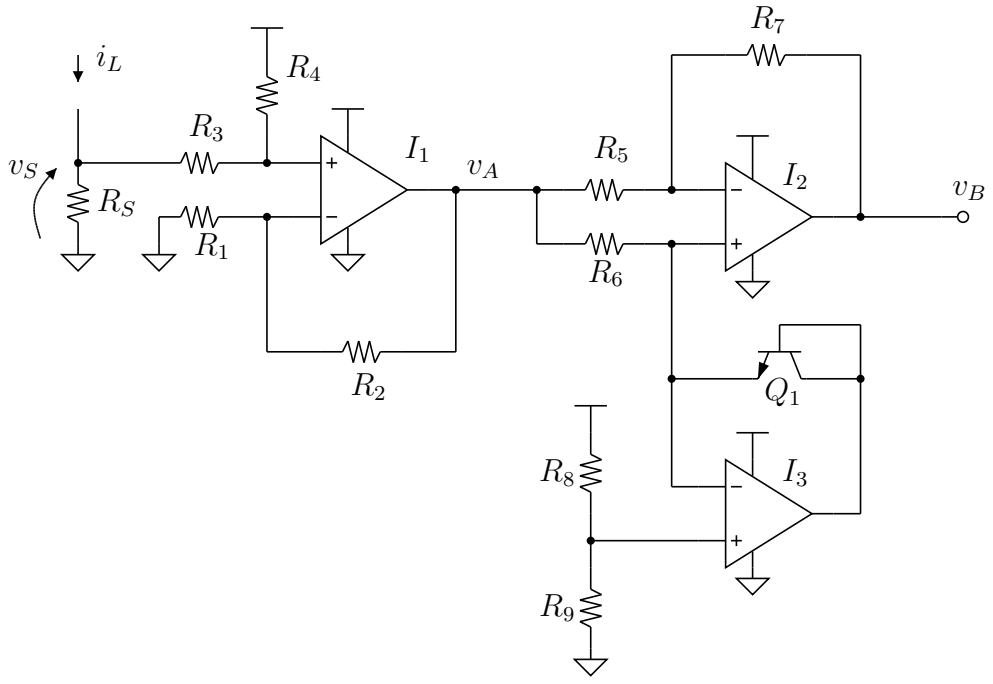

Figure 3.7: Amplification and absolute value circuit.

From eq. (3.2) it can be seen that the feedback factor is inversely proportional to the input signal. An input signal covering a dynamic range of 86 dB causes the feedback factor and, as a consequence, the closed loop gain to vary over a range

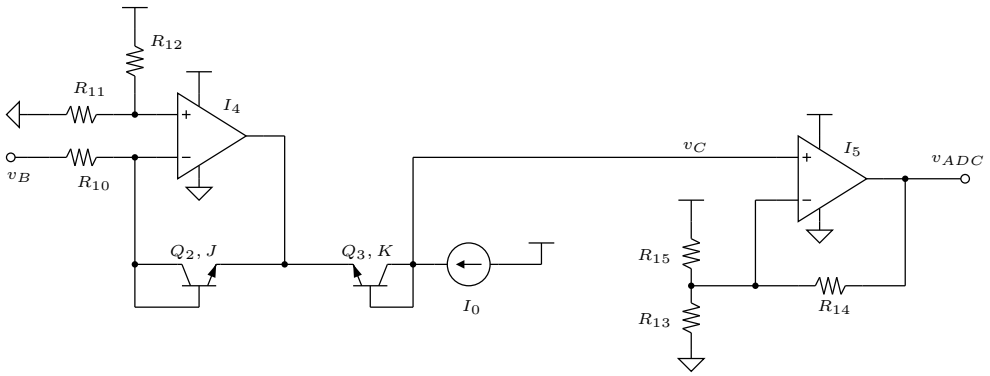

Figure 3.8: Logarithmic amplifier.

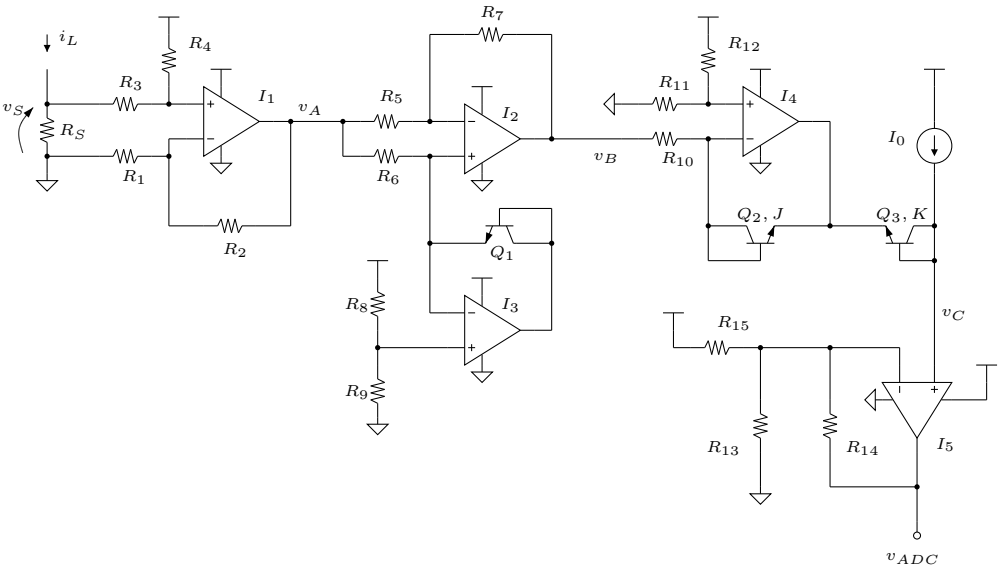

Figure 3.9: Complete amplifier.

larger than 4 decades. In constant gain-bandwidth amplifiers, this leads to severe bandwidth limitation as shown in fig. 3.11, where a $GBP = 10\,\mathrm{MHz}$ was used for the operational amplifier. At small current values the circuit operates in the steep region of the characteristic, thus I_4 works with a fairly large closed loop gain hence its bandwidth reduces and limits the bandwidth of the whole chain. In fig. 3.12 it is shown that, in order to achieve a 1 MHz minimal bandwidth, a GBP of 1 GHz is needed.

Because of this limitation a change in the topology is necessary. Since the logarithmic amplifier relies on the amplification of the difference between two diode voltages,

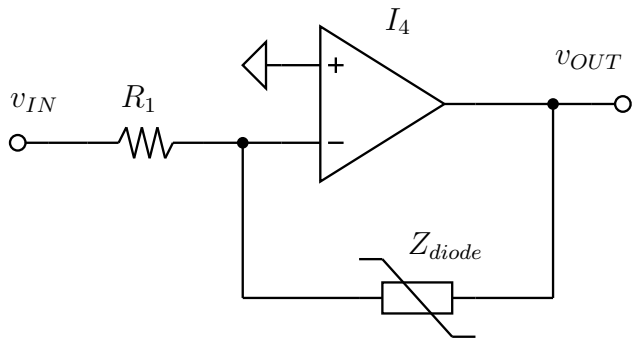

Figure 3.10: Inverting amplifier with varying feedback impedance.

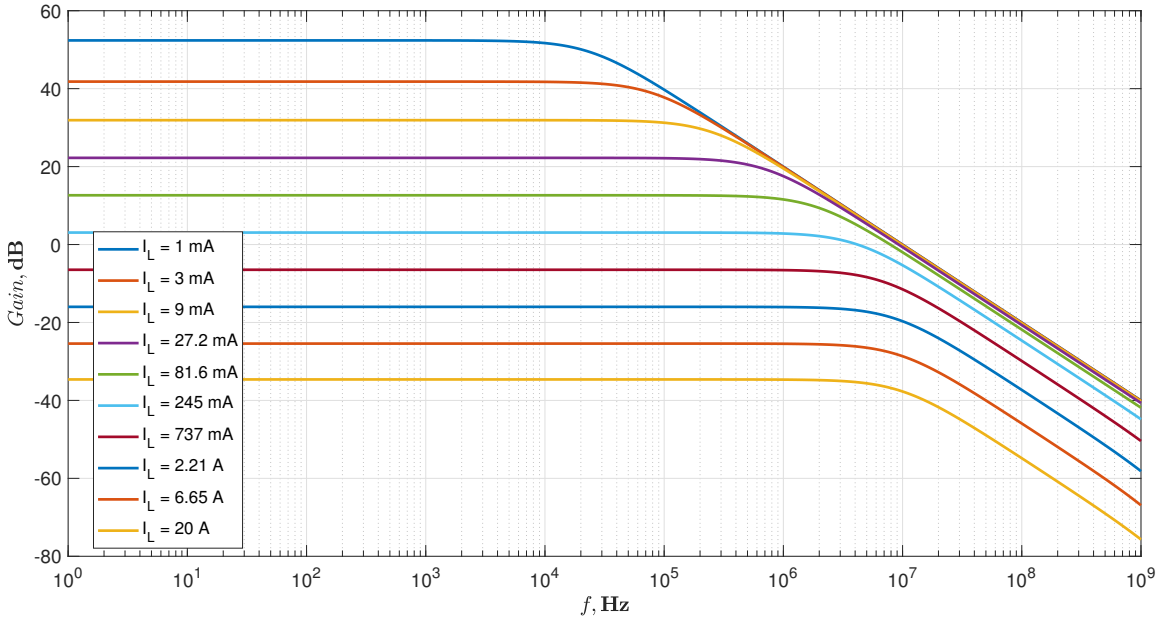

Figure 3.11: Logarithmic amplifier bandwidth limitation.

a solution to the problem can be that of using the schematic shown in fig. 3.13. It is the well known instrumentation amplifier which is able to amplify and shift a differential voltage.

The dependent current source i_{IN} represents the current output rectifier which can be represented by the schematic in fig. 3.14

The in-out relation of the rectifier is

$$i_{IN} = GR_S|i_L| \tag{3.3}$$

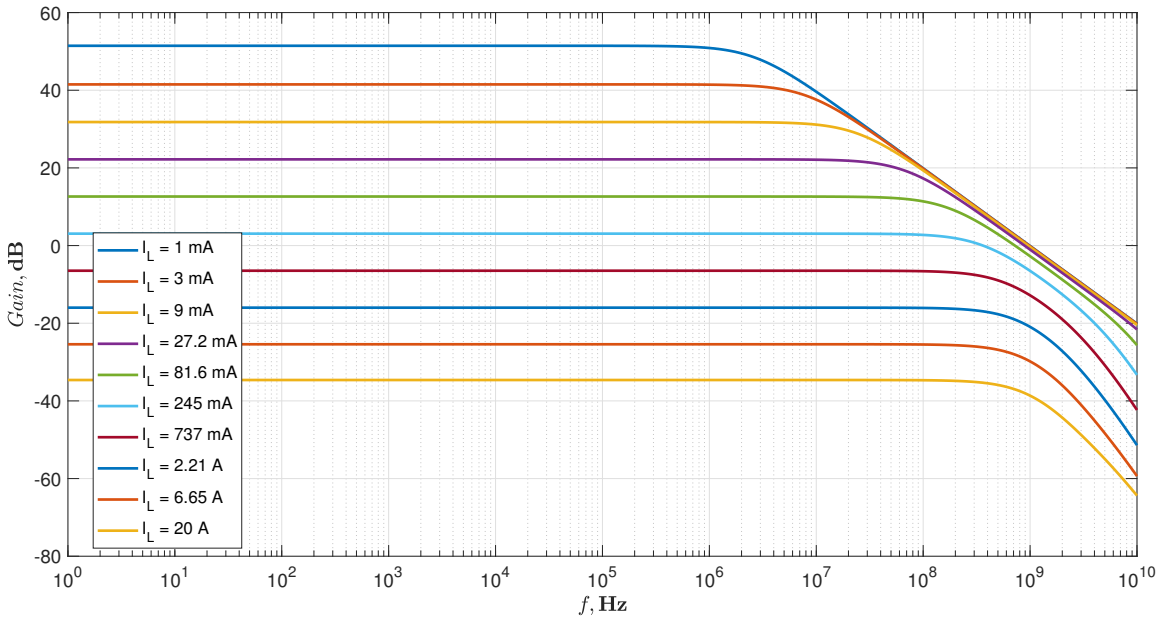

Figure 3.12: Logarithmic amplifier gain-bandwidth requirement.

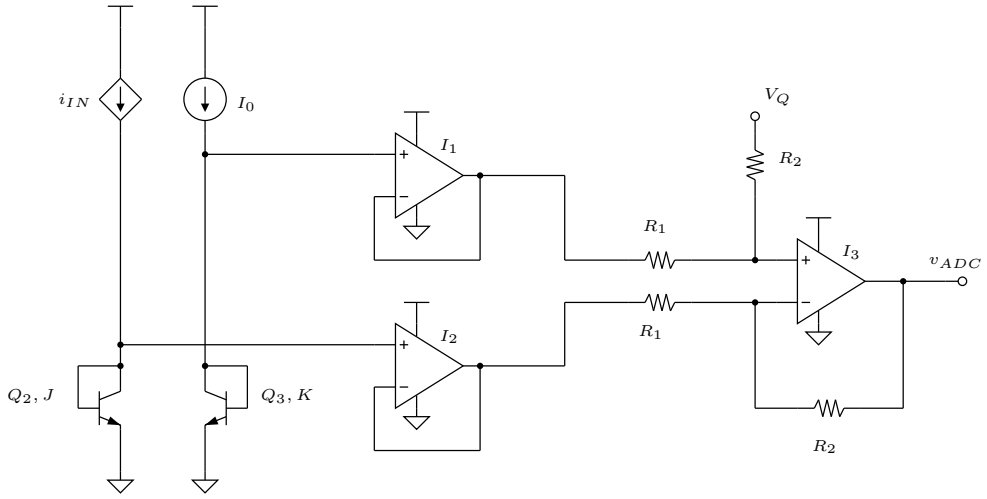

Figure 3.13: Logarithmic amplifier exploiting an instrumentation amplifier.

and it is plotted in fig. 3.15. The choice of G is dictated by the chosen range for i_{IN}which is fixed as $i_{IN} \in (10\,\text{nA}, 200\,\mu\text{A})$. It is clear that this current has to cover a dynamic range that is equal to the one covered by the load current since all stages before this one are linear. The extreme values of the chosen interval are related to the characteristics of real bipolar transistors such as finite current gain and series resistance, which limit the range in which the logarithmic relation is followed by the

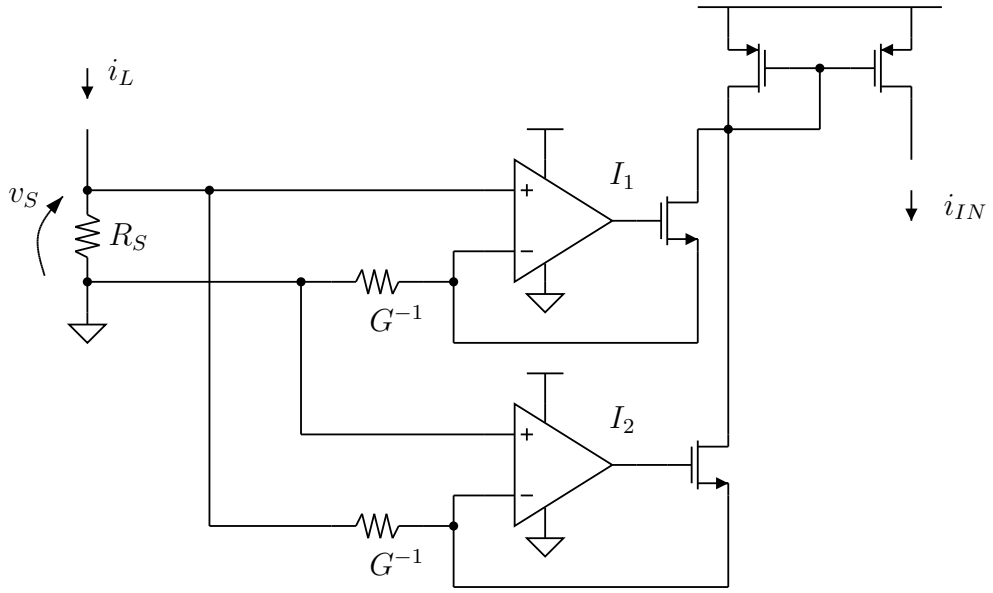

Figure 3.14: Current output rectifier.

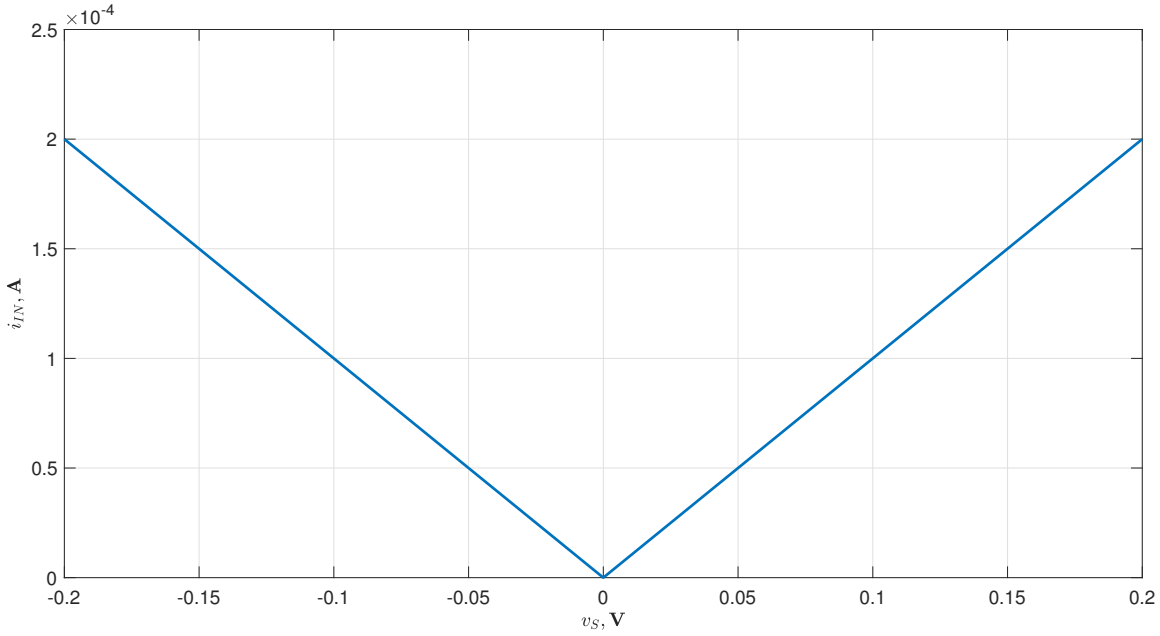

Figure 3.15: Rectifier characteristic.

pn junction; this choice will be further explained in the next chapter.

The in-out characteristic of the logarithmic amplifier can be written as

$$v_{ADC} = V_Q + V_K \ln\left(\frac{K}{J} \cdot \frac{|i_{IN}|}{I_0}\right) \tag{3.4}$$

where K and J represent the emitter areas of Q_2 and Q_3 respectively. The current I_0 is fixed at 10 µA. This choice affects the zero thermal drift point but it is not important for the measurement range. In fact, chosen I_0, the characteristic can be shifted by means of V_Q so that the desired range is covered. V_K is typically indicated as measured in V/decade. This notation is related to the fact that V_K fixes the range of the input signal that can be covered with a certain output voltage range. In the specific case the input signal covers a range of $2 \cdot 10^4$ or, equivalently, 4.3 decades. Hence V_K must be chosen so that it allows the measurement of a signal covering this range. If the available output voltage range is indicated with OR then the angular coefficient is given by

$$V_K = \frac{OR}{\#decades} \log_{10} e. \tag{3.5}$$

From this relation it appears that the smaller V_K, the better, since this would imply a larger input range. However, V_K is also related to the sensitivity of the inverse compression relation with respect to v_{ADC}. Indeed, when the i_L current is evaluated from the v_{ADC} voltage, its relative sensitivity is

$$S_{v_{ADC}}^{i_L} = \frac{\partial i_L}{\partial v_{ADC}} \frac{v_{ADC}}{i_L} = \frac{v_{ADC}}{V_K}. \tag{3.6}$$

As a trade-off between input dynamic range and reduced i_L sensitivity, V_K is chosen for a 5 decades input range which is slightly larger than the range covered by the desired signal (4.3 decades). Assuming an output range of $OR = 2.8\,\mathrm{V}$, which is reasonable for a rail-to-rail amplifier, the angular coefficient is

$$V_K = \log_{10} e \cdot \frac{2.8\,\mathrm{V}}{5\,\mathrm{dec}} = 0.243\,\mathrm{V/dec}. \tag{3.7}$$

This choice of V_K yields a maximum sensitivity of

$$S_{v_{ADC}}^{i_L} = \frac{2.8\,\mathrm{V}}{0.243\,\mathrm{V}} = 11.5 \tag{3.8}$$

at maximum input signal. This can be interpreted as follows: when calculating i_L starting from the measured v_{ADC} (errors related to the A/D conversion are not considered for now), an error of 1% in the measurement of v_{ADC} gives rise to an error of 11.5% in the calculation of i_L, at full range. This sensitivity is not constant and it

is proportional to the input quantity amplitude. This is the price to pay for increased resolution at small input signal levels. So both the quantization error and the error due to the analog circuitry are minimal at minimum input signal and increase as the signal amplitude increases. V_Q vertically shifts the characteristic and it is calculated so that at full range the output voltage is $v_{ADC}(20\,\mathrm{A}) = 2.8\,\mathrm{V}$.

In fig. 3.16 the characteristic of the logarithmic amplifier is shown while in fig. 3.17 the characteristic of the complete conditioning circuit (including the shunt resistor) is plotted.

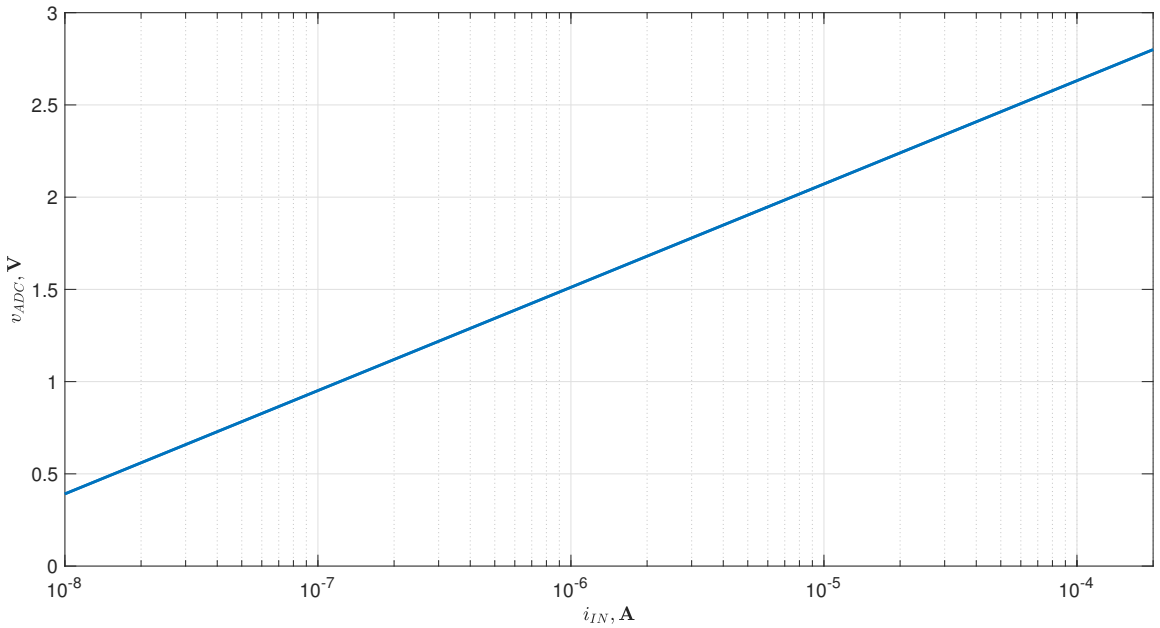

Figure 3.16: Logarithmic amplifier characteristic.

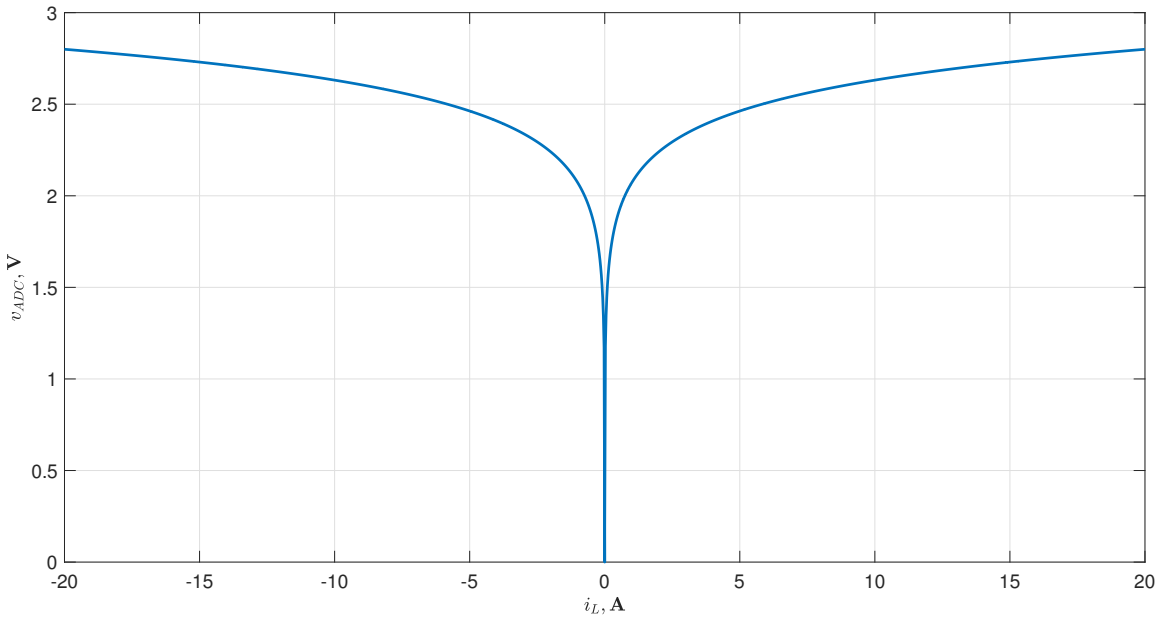

Figure 3.17: Complete acquisition channel characteristic; the correct sign is found by looking at the bit carried by the input comparator.

3.3 Time-based analog to digital conversion

Voltage to time conversion can be used to implement a form of low-cost analog to digital conversion. Circuit is shown in fig. 3.18 while the waveforms are shown in fig. 3.19.

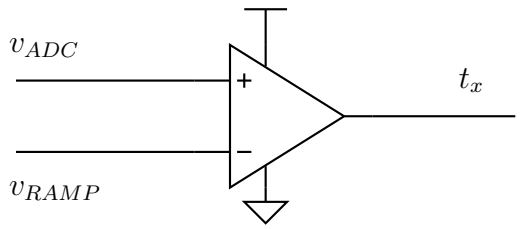

Figure 3.18: Voltage to time conversion.

The voltage to be converted is compared with a linearly rising voltage. The comparator output is a voltage pulse whose duration is proportional to v_{ADC}. This pulse is used as a gating signal for a counter and so a numeric value proportional to the input voltage is obtained. This value is latched into an output register after each

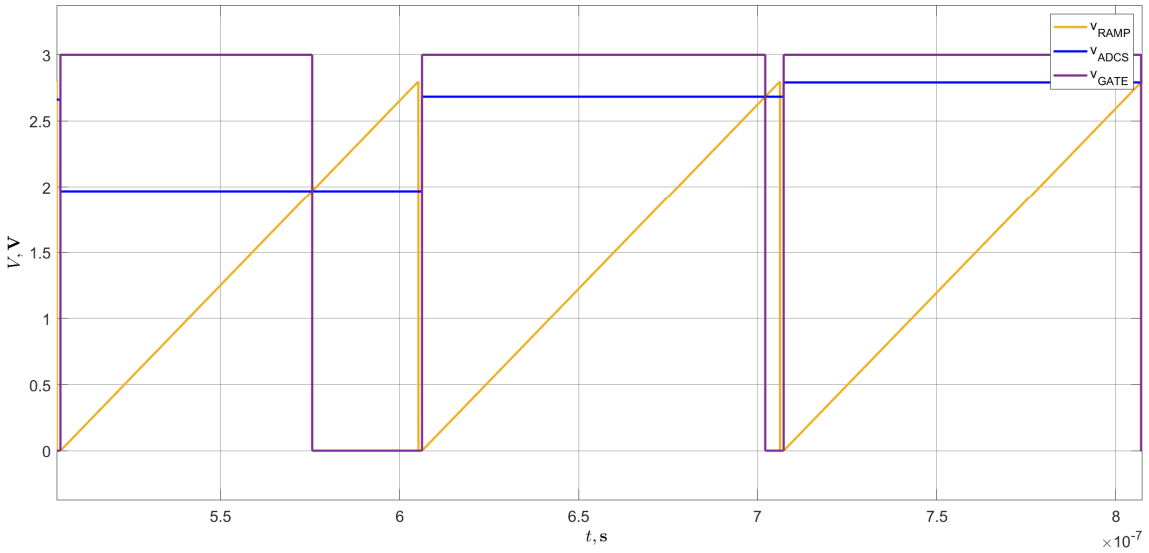

Figure 3.19: Voltage to time conversion - waveforms.

conversion interval T_S. The operation of the whole digital part is timed by a finite state machine which operates in three basic phases (fig. 3.20)

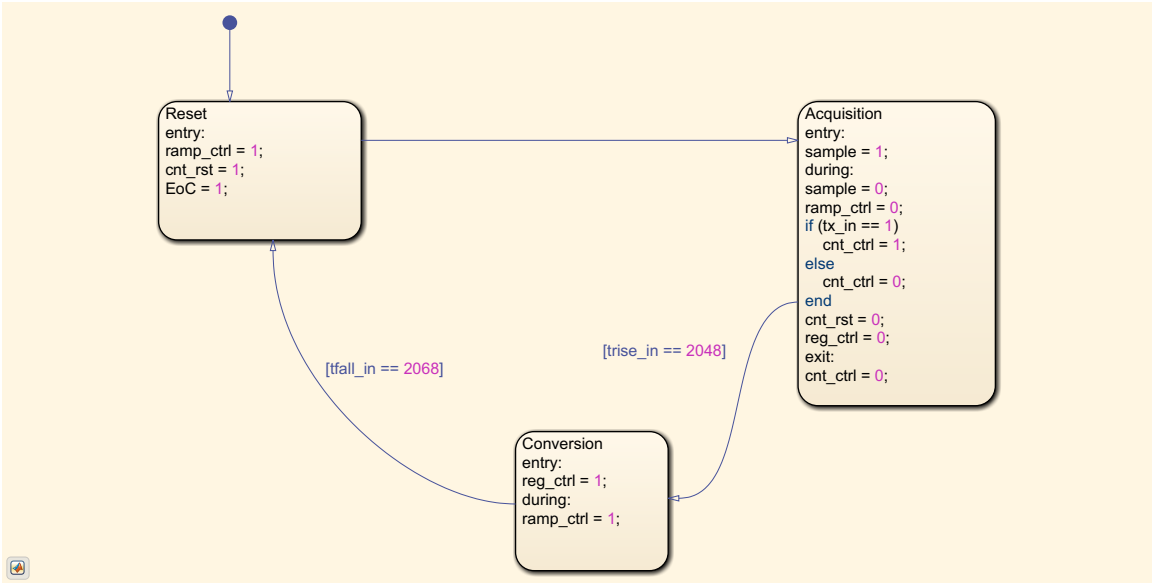

Figure 3.20: FSM state diagram.

In the acquisition state the gating signal is high and the counter increases its value at each clock pulse (fig. 3.21). Once the ramp voltage reaches v_{ADC} the gating signal goes low and the counter output is latched into the register. At the end of the cycle the counter is reset and the process can start over. The cycle duration is T_S and it

is fixed depending on the required sampling frequency. Since the desired bandwidth is $BW = 1\,\text{MHz}$ a sampling frequency of $f_S = 10\,\text{MHz}$ can be assumed. This gives a conversion time $T_S = 100\,\text{ns}$. In order to compute the required clock frequency it can be noticed that v_{ADC} is to be converted on 11 bits (since 12 bits are required and one bit is reserved to the sign). Hence the max count in T_S is

$$N_{MAX} = 2^{11} - 1 = 2047. \tag{3.9}$$

The clock frequency can be computed as

$$f_0 = 2047 \cdot f_S = 20.47\,\text{GHz} \tag{3.10}$$

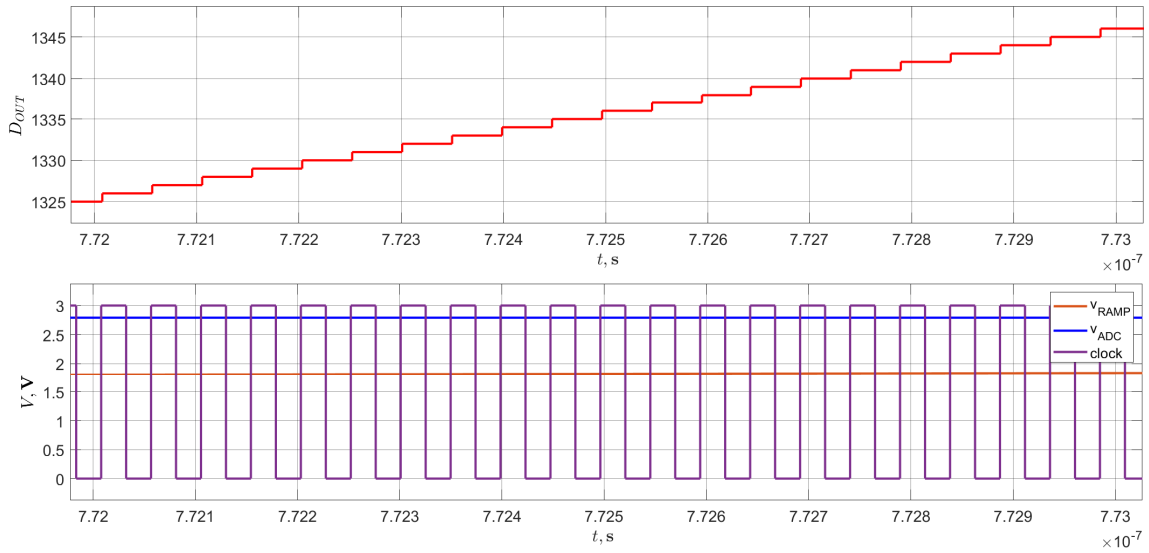

Figure 3.21: Pulse counting.

Another parameter to be specified is the slope of the ramping voltage. Since it has to sweep $OR = 2.8\,\text{V}$ in $T_S = 100\,\text{ns}$, its slope will be

$$k_T = \frac{OR}{T_S} = 28\,\text{V/µs} \tag{3.11}$$

The input-output relation of the voltage to time converter is given by

$$t_x = \frac{v_{ADC}}{k_T} \tag{3.12}$$

and it plotted in fig. 3.22

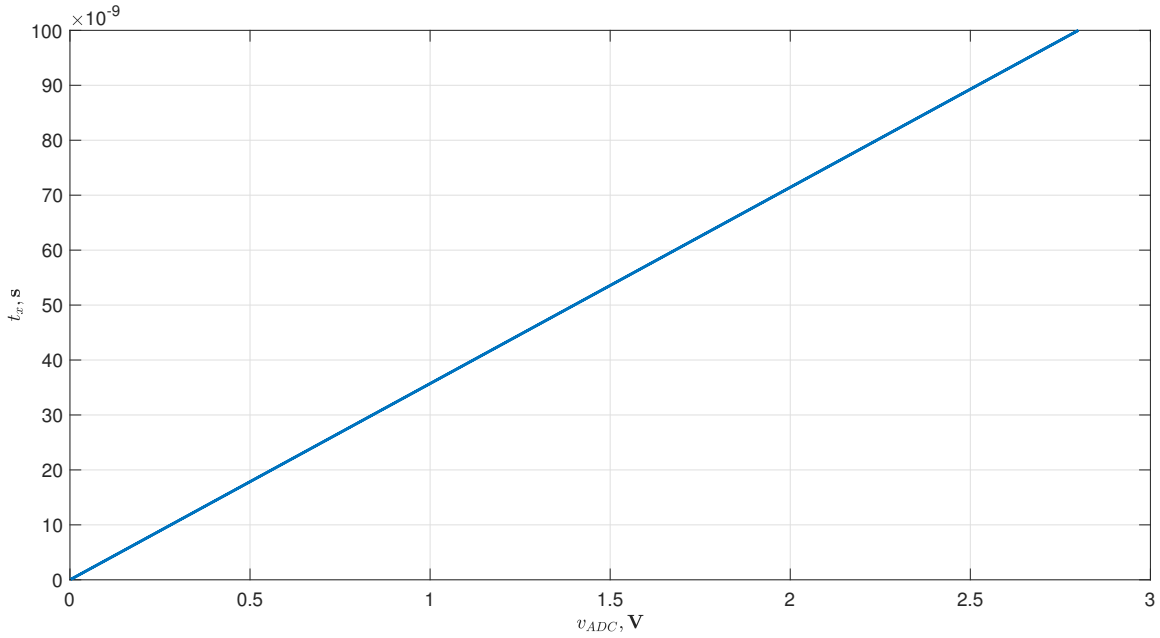

Figure 3.22: Voltage to time characteristic.

In order to obtain the in-out characteristic, the number of pulses (m_x) counted at the end of each sampling interval can be computed as

$$m_x = \lfloor t_x f_0 \rfloor = \left\lfloor \frac{v_{ADC}}{k_T} f_0 \right\rfloor . \tag{3.13}$$

The input-output relation of the counter is shown in fig. 3.23. The output code D_{OUT} is a 12-bit signed representation of the input current where the amplitude (given by the 11 LSB) is calculated as

$$m_x = \left\lfloor \frac{f_0}{k_T} \left(V_Q + V_K \ln \left(\frac{G R_S |i_L|}{I_0} \right) \right) \right\rfloor . \tag{3.14}$$

The inverse compression relation is applied in order to obtain the amplitude of the sensed current, while the correct polarity is given by the MSB

$$\left| \overline{i_L} \right| = \frac{I_0}{G R_S} \exp \left(\frac{\frac{m_x k_T}{f_0} - V_Q}{V_K} \right). \tag{3.15}$$

The quantization step can be derived from eq. (3.15) as (characteristic is symmetric so sign is not important for quantization step size)

$$i_{Lq} = \frac{\partial \overline{i_L}}{\partial m_x} = \frac{\overline{i_L} \cdot OR}{V_K \cdot 2^{N-1}}. \tag{3.16}$$

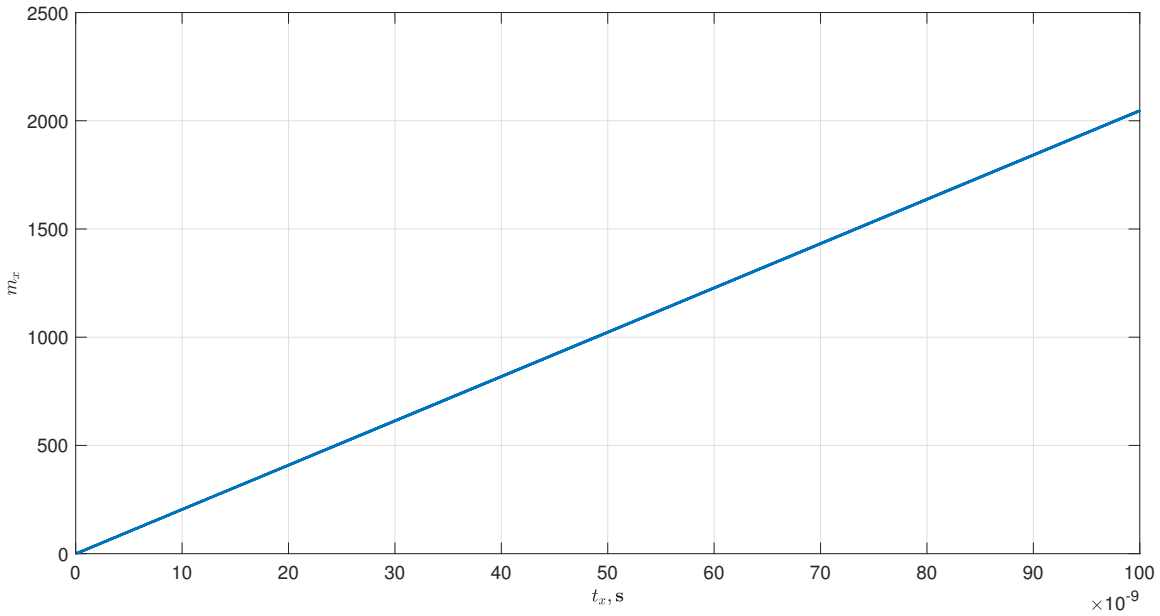

Figure 3.23: Time to code characteristic.

In the following two images (fig. 3.24, fig. 3.25 the quantization step size is shown for uniform and nonuniform quantization. From the second one it can be seen that the relative quantization error is constant for nonuniform quantization.

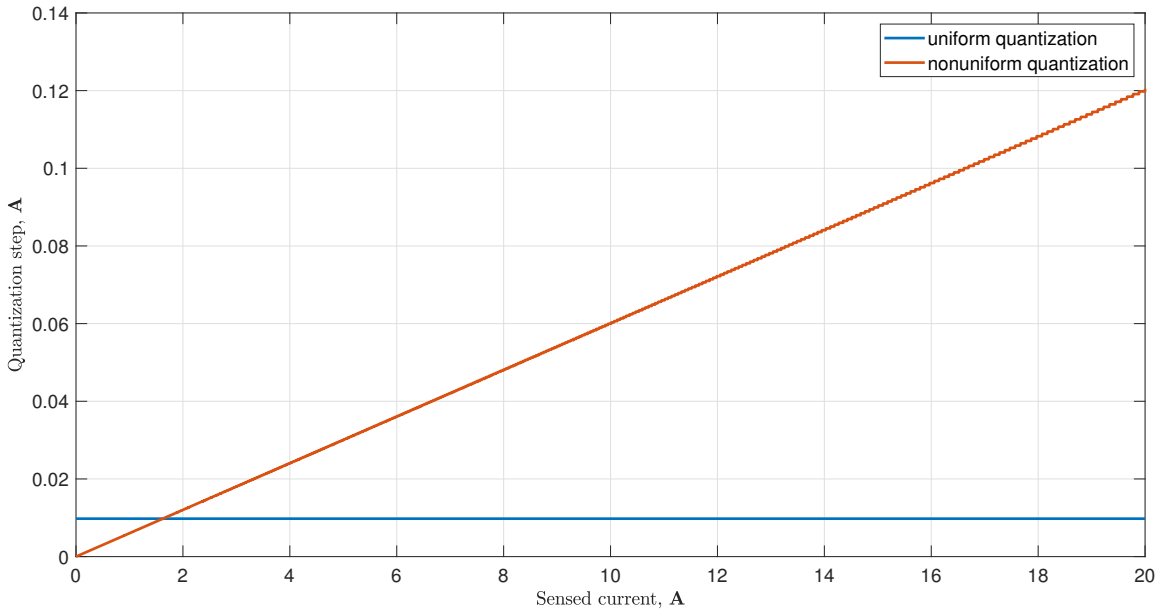

Figure 3.24: Quantization step.

In the following (fig. 3.26, fig. 3.27), some time domain simulations, carried out by means of Simulink, are shown. The test signal is a sinusoidal current with amplitude

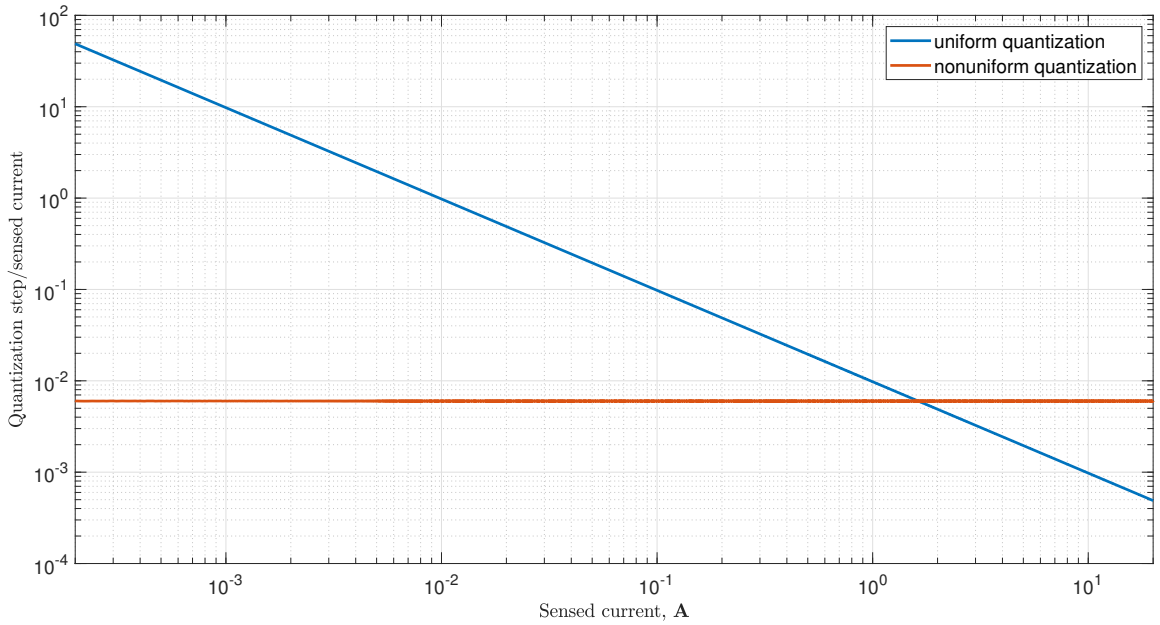

Figure 3.25: Quantization step relative to the signal amplitude.

$i_{L,peak} = 20\,\text{A}$ and frequency $f = 1\,\text{MHz}$. Since the signal goes through a nonlinear conditioning block, the v_{ADC} voltage is strongly distorted hence an increase in the bandwidth occupation is to be expected. In fig. 3.26 the voltage to be converted and the sampled one are shown; this simulation highlights one of the drawbacks of the proposed system that is, sampling frequency must be much higher than the required bandwidth which, in turn, would require the frequency of the oscillator to increase. In fig. 3.27 the input current and the reconstructed one, after applying the expansion relation to the acquired voltage are shown. The reconstructed current could be smoothed by the use of digital filtering but this, again, would cause a reduction in the bandwidth of the system.

In the following chapter the design of the logarithmic amplifier is presented.

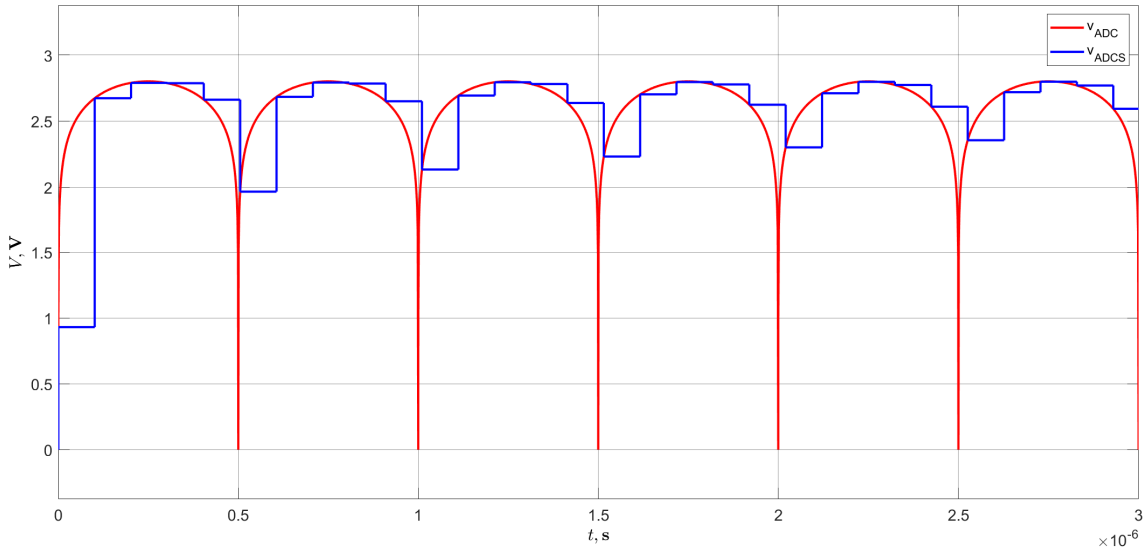

Figure 3.26: Time domain simulation performed on the block scheme.

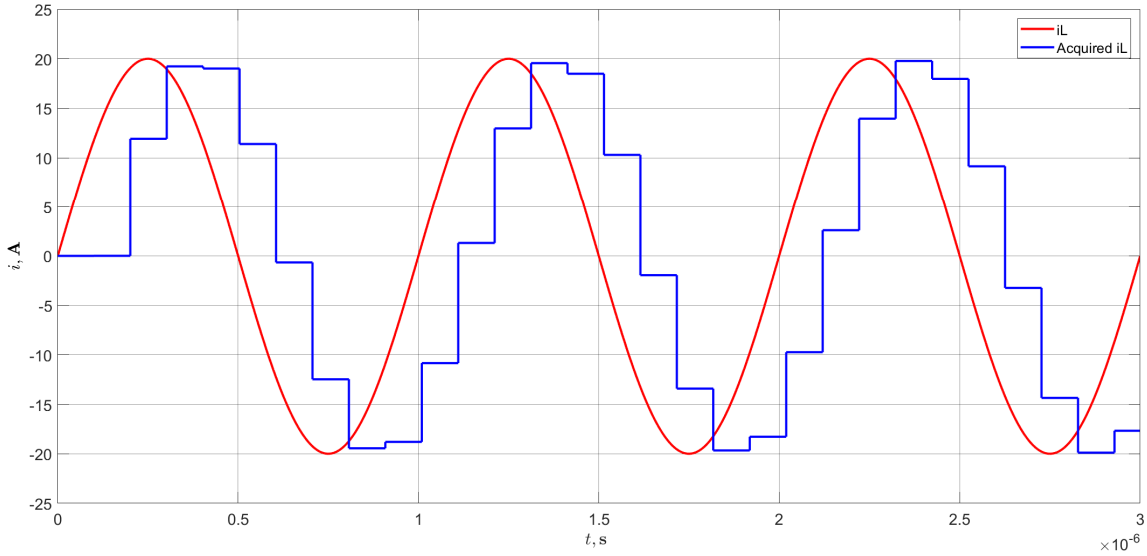

Figure 3.27: Time domain simulation performed on the block scheme.

CHAPTER 4

Analog conditioning circuitry

The analog blocks that were designed and simulated are presented in this chapter.

4.1 Log amplifier review

As seen previously, the logarithmic amplifier can be built by using two diode connected transistors and an instrumentation amplifier (fig. 4.1).

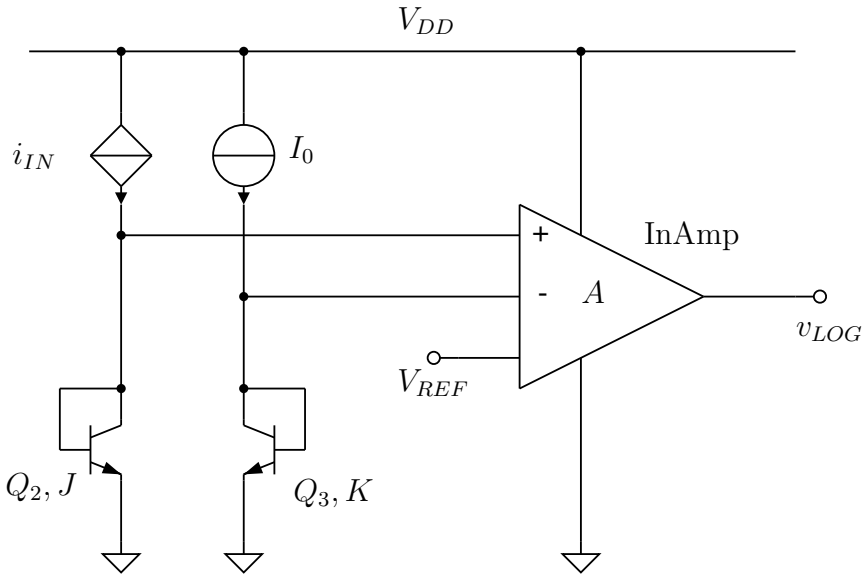

Figure 4.1: Logarithmic amplifier with instrumentation amplifier.

Q_3 is biased at fixed current while Q_2 is driven by the input current. The instru-

mentation amplifier performs the following operation

$$v_{LOG} = A(V_{REF} + v_+ - v_-). \tag{4.1}$$

The difference $v_+ - v_-$ is equal to $v_{BE2} - v_{BE3}$ and it is proportional to the natural logarithm of the input current. So the output voltage is related to the input current by

$$v_{LOG} = A\left(V_{REF} + V_T \ln\left(\frac{i_{IN}}{I_0}\right)\right). \tag{4.2}$$

4.2 BJT characterization

Logarithmic amplification is based on the voltage-current curve of a pn junction having exponential behavior (fig. 4.2)

$$i_D = I_S \exp\left(\frac{v_D}{\eta V_T} - 1\right). \tag{4.3}$$

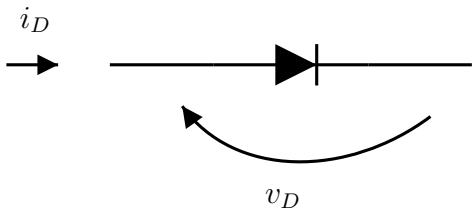

Figure 4.2: Diode voltage and current convention.

The unitary term can be safely neglected for any v_D a few times larger than the thermal voltage. In eq. (4.3) there are several parameters that depend on technology or other factors such as temperature. The parameter η is technology dependent while the reverse saturation current depends on doping levels and on temperature. In order to remove η a BJT with its base tied to its collector can be used instead of a diode.

In fact, in the BJT formula the ideality factor is not present (from Ebers-Moll model)

$$i_C = I_S \left(\exp\left(\frac{v_{BE}}{V_T} \right) - 1 \right). \tag{4.4}$$

In a diode connected transistor the collector current depends exponentially on v_{BE} while the current that can be forced from the outside is the emitter current. For this reason the approximation $i_E \simeq i_C$ is introduced which can be reasonable when the current gain is much larger than unity. The current gain is dependent, among other things, on the collector current so it is important to take this into account when choosing the current range in which the BJTs are to be used. The reverse saturation current value also cannot be controlled by the designer so its effect has to be removed from the characteristic. The traditional solution to this problem is the use of a second BJT, matched to the first one so that the I_S can be assumed to be the same; the difference between the two v_{BE}, thanks to the properties of the logarithm, is not dependent on I_S. Besides finite current gain, there is another problem with real bipolars related to the nonzero series resistance which at large current can have an important effect and make the diode characteristic differ from the expected logarithmic one.

In order to select the best range in which the bipolars can be used, the available vertical BJTs were characterized through simulations. The following testbench was used (fig. 4.3)

Emitter current of diode connected BJTs was swept from 1 nA to 500 µA, covering a range which is larger than the required one. Also the temperature was changed in steps and the current gain and series resistance were extracted. The current gain curves are shown in fig. 4.5 as a function of emitter current and at different junction temperatures. It can be seen that below 1 nA the current gain keeps decreasing so the approximation $i_E \simeq i_C$ would not be reasonable anymore. As to the large current values, the extracted series resistance value is around 100 Ω. The effect of the series resistance can be seen from the logarithmic v_{BE} - i_E plot (fig. 4.6). This plot shows that the measured v_{BE} departs from the theoretical one at large emitter current. The curve labeled v_{BE} is the one extracted from the simulation. The curves labeled as v_{BEE} and v_{BEC} were calculated as

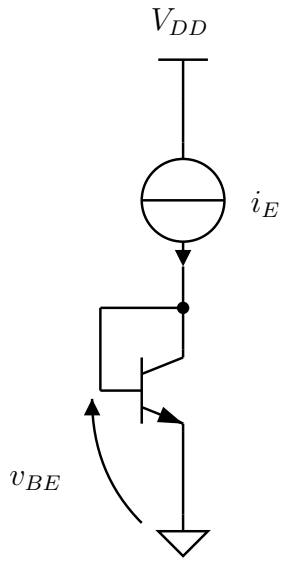

Figure 4.3: BJT characterization.

$$v_{BEE} = V_T \ln\left(\frac{i_E}{I_S} + 1\right) \tag{4.5}$$

$$v_{BEC} = V_T \ln\left(\frac{i_C}{I_S} + 1\right) \tag{4.6}$$

where I_S is the inverse saturation current and it was calculated from the simulated curve. It can be seen that these two curves are virtually overlapped which shows that the effect of the finite current gain is not important in the chosen range. The curve labeled v_{BER} is calculated by assuming the model shown in fig. 4.4 for the diode connected BJT

$$v_{BER} = V_T \ln\left(\frac{i_E}{I_S} + 1\right) + R_S i_E. \tag{4.7}$$

From the curves in fig. 4.6 it can be seen that the best current range for the usage of the BJTs is the one from 1 nA to 20 µA. Since a current of 1 nA is not easy to work with, it is better to increase the area of the transistors so as to be able to work with larger current values. The BJT is made of 10 unit transistors so that the input current range is 10 nA to 200 µA. In order to have a good matching the two transistors have the same emitter area. Choice of the current I_0 affects the point

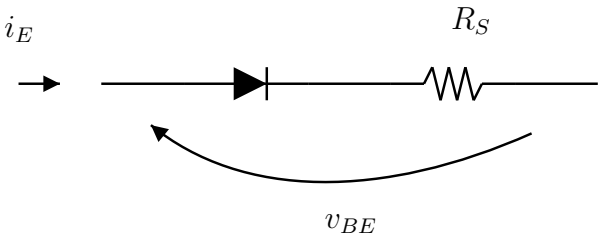

Figure 4.4: Diode connected BJT - series resistance.

at which the logarithm is zero. It is typically placed near the center of the input range (geometrical mean) because this minimizes the temperature dependence of the characteristics. In fact the zero point has zero thermal drift. In this case the center of the input range is around 3 µA. I_0 can be fixed at 10 µA which is easy to generate and will be used for other tasks as well (bias current for the analog blocks).

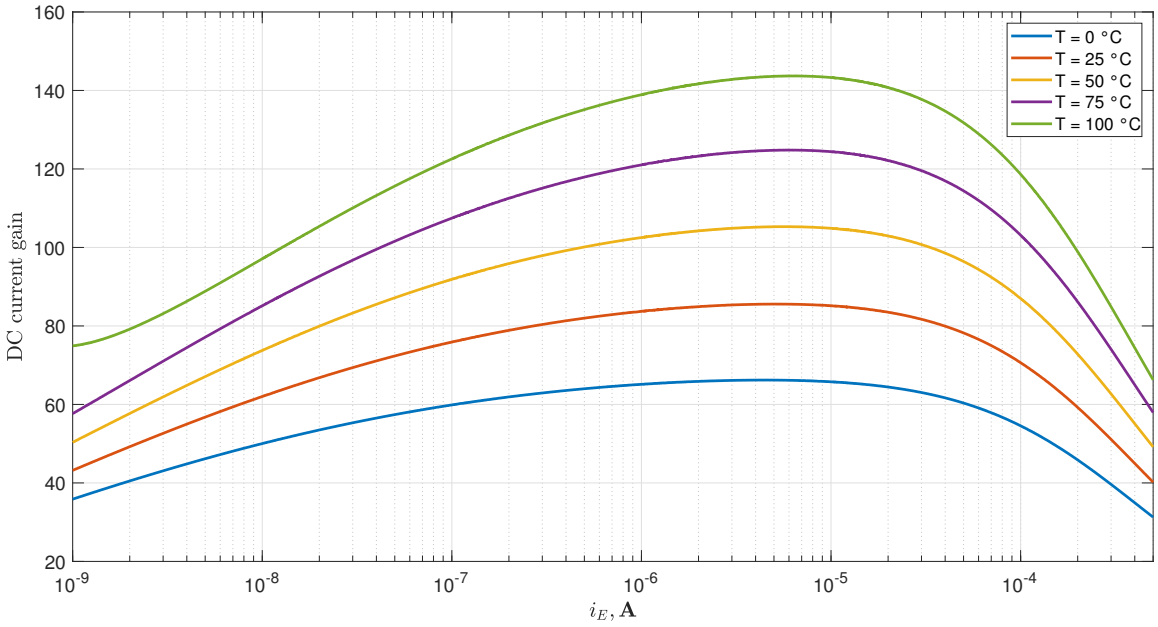

Figure 4.5: Vertical NPN transistors' current gain curves.

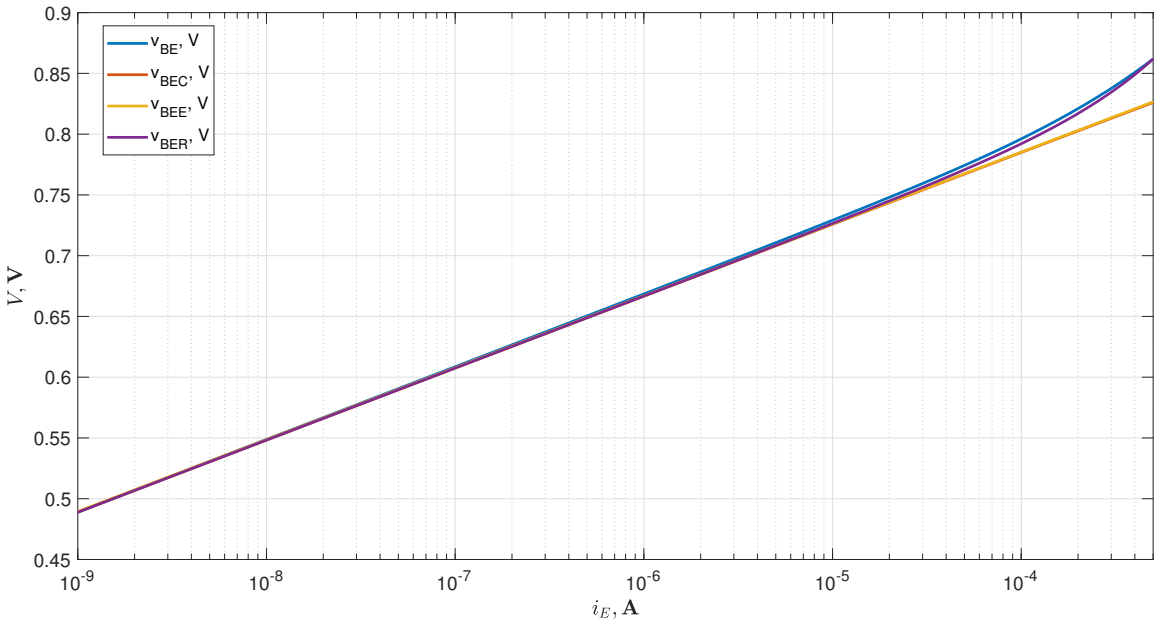

Figure 4.6: Vertical NPN transistors' v_{BE} - i_E curve.

4.3 DDA

Traditional instrumentation amplifiers require the use of three operational amplifiers and several resistors. The schematic is shown is fig. 4.7. The main advantages are the possibility of amplifying a differential signal with also the possibility to apply a vertical shift to the resulting signal. 3 OA INAs offer very large input impedance and good common mode rejection ratio (it is related to the matching of the resistors). The characteristic of the circuit is the following

$$v_{OUT} = V_{REF} + \frac{R_2}{R_1}\left(2 + \frac{R_G}{R}\right)(v_+ - v_-). \tag{4.8}$$

However, for CMOS integrated circuit design the instrumentation amplifier can be realized as a single block. It goes by the name of Differential Difference Amplifier ([17]) and its block scheme is shown in fig. 4.8. The input output relation is

$$v_{OUT} = G_{m1}Rv_{D1} - G_{m2}Rv_{D2} \tag{4.9}$$

and, assuming $G_{m1} = G_{m2} = G_m$

$$v_{OUT} = G_mR(v_{D1} - v_{D2}) \tag{4.10}$$

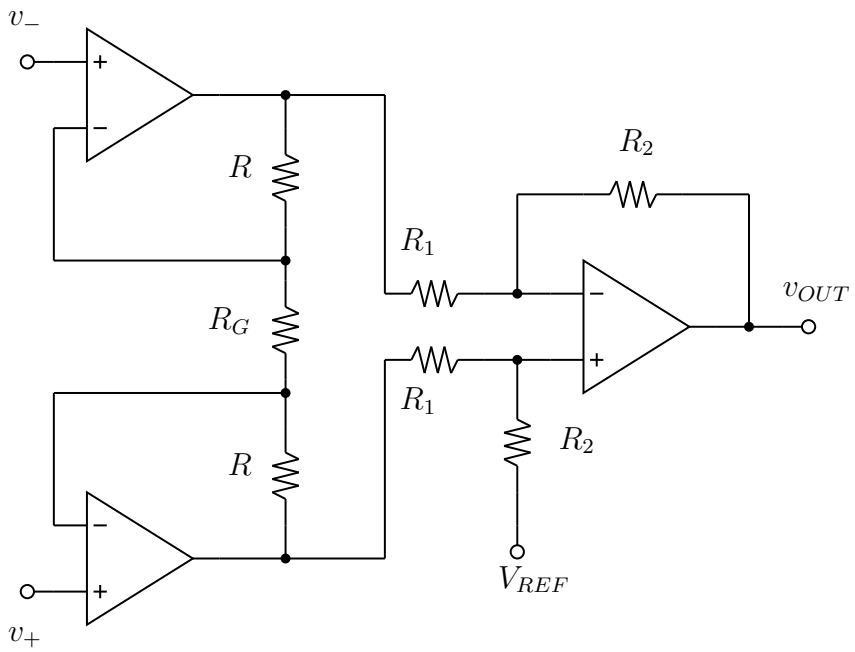

Figure 4.7: 3 OpAmp instrumentation Amplifier.

The difference between the output currents is forced through a load resistor. If connected with a resistive feedback (fig. 4.9), provided that the open loop gain ($G_m R$) is large enough, the output voltage can be written as

$$v_{OUT} = (V_{REF} + (v_+ - v_-)) \left(1 + \frac{R_2}{R_1}\right) \frac{G_{m2}}{G_{m1}}. \tag{4.11}$$

The transconductance elements can be simple differential pairs (fig. 4.10). If the differential input signal is not small, like in the current case, some local feedback is needed in order to improve linearity and increase the input differential range of each pair (fig. 4.11, it is usually drawn as in fig. 4.12, the small signal operation is the same for both circuits).

The differential output current is given by

$$i_D = i_{D1} - i_{D2} = gm(v_+ - v_-) \tag{4.12}$$

where g_m is the transconductance of each transistor. For the source degenerated

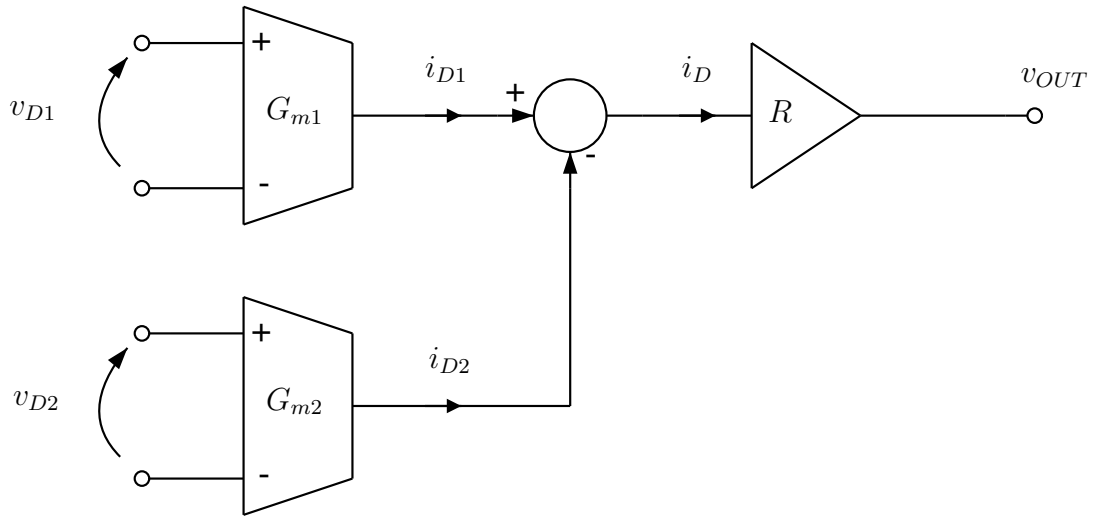

Figure 4.8: Differential Difference Amplifier.

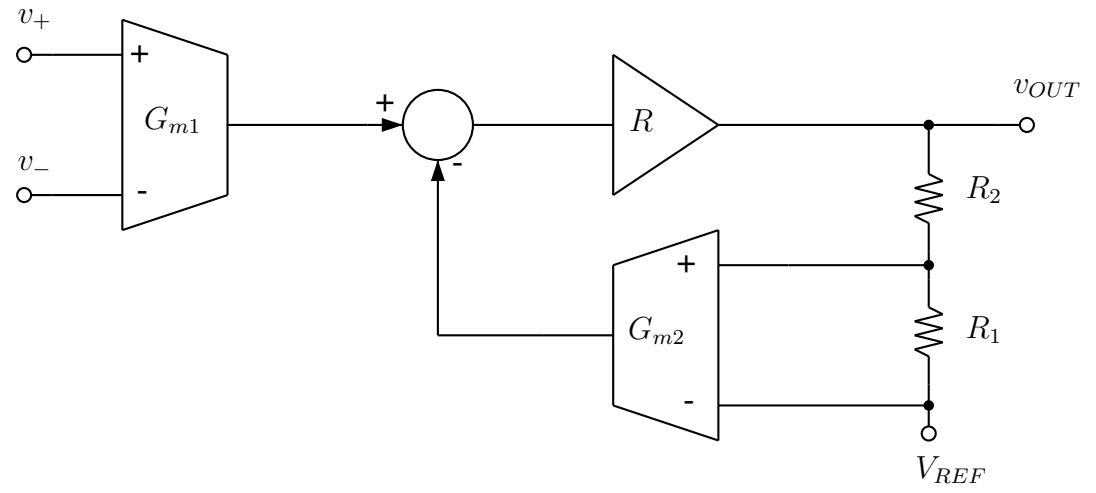

Figure 4.9: Feedback connected Differential Difference Amplifier.

differential pair the transconductance is fixed through the source resistor

$$G_m = \frac{g_m}{1 + g_m R_S}. \tag{4.13}$$

If $g_m R_S \gg 1$ the transconductance is roughly independent of the parameters of the

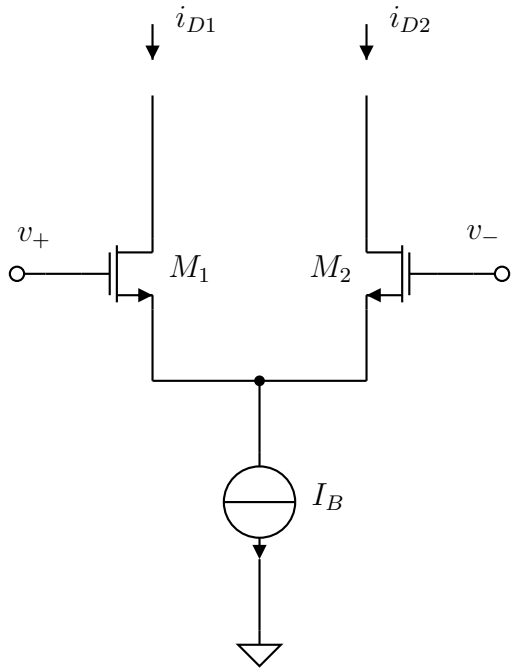

Figure 4.10: Differential pair.

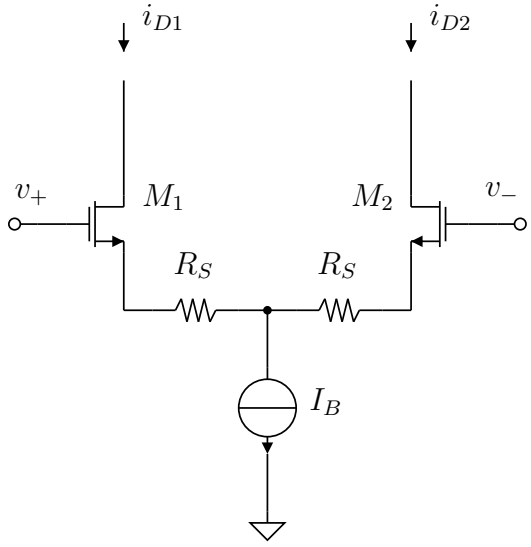

Figure 4.11: Differential pair with local feedback.

transistor and is given by

$$G_m \simeq \frac{1}{R_S}. \tag{4.14}$$

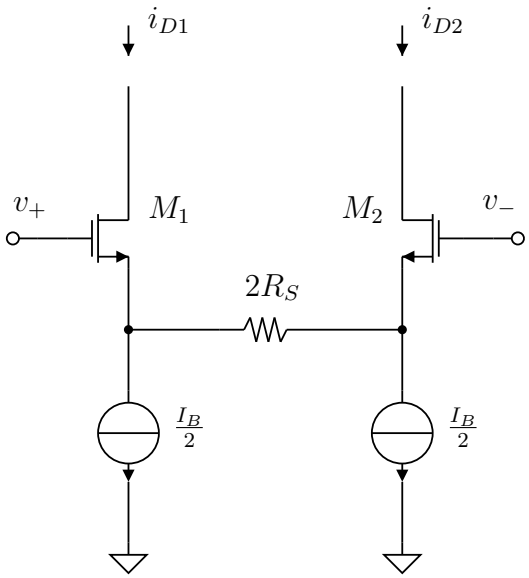

Figure 4.12: Differential pair with local feedback, alternative representation.

R_S is chosen in order to increase the differential voltage swing according to the maximum Δv_{BE} (fig. 4.13).

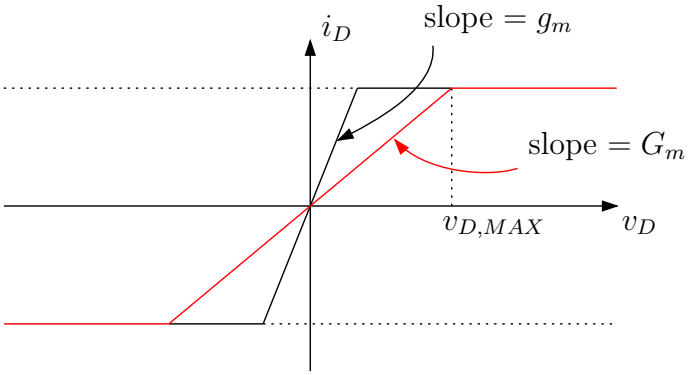

Figure 4.13: Differential pair with local feedback, input swing.

Since the input voltages are smaller than 1 V, the differential pairs are built with p type MOSFETS which present a common mode input range that includes the reference voltage. The difference between the differential currents is performed by a cascode load whose output impedance acts as a current to voltage converter. Adding a second stage to the amplifier allows to increase the low frequency gain and, by

proper frequency compensation, also the unity-gain frequency. Furthermore, the cascode load has a relatively small output swing so adding an n-type common source output stage allows to achieve an output swing that can virtually reach the negative supply rail. Since the amplifier does not have to drive resistive loads (as shown in fig. 4.24), a low output impedance buffer stage is not needed.

In order to study the frequency response of the amplifier, the circuit shown in fig. 4.14 is analyzed, where resistance and capacitance for each node towards ground have been highlighted. The pole associated to node 1 is typically not considered since the impedance of that node towards ground is low ($R_1 \approx \frac{1}{g_{mK5}}$). Resistance and capacitance associated to nodes 2 and 3 can be approximated as

$$R_2 \approx (r_{oK4} g_{mK4} r_{oK2}) \parallel (r_{oK6} g_{mK6} (r_{oK8} \parallel r_{oP1} \parallel r_{oP3})) \tag{4.15}$$

$$C_2 \approx C_{gdK6} + C_{dbK6} + C_{gdK4} + C_{dbK4} + C_{gs6} \tag{4.16}$$

$$R_3 \approx r_{o,6} \parallel r_{o,7} \tag{4.17}$$

$$C_3 \approx C_{gd6} + C_{db6} + C_{gd7} + C_{db7} + C_L. \tag{4.18}$$

The MOSFET parasitic capacitances can be calculated as

$$C_{gs} = \frac{2}{3} C'_{OX} + C_{gs,O} W \tag{4.19}$$

$$C_{gd} = C_{gd,O} W \tag{4.20}$$

$$C_{gb} = C_{gb,O} L \tag{4.21}$$

$$C_{sb} = C'_{j0} A_S + C'_{jSW0} P_S \tag{4.22}$$

$$C_{db} = C'_{j0} A_D + C'_{jSW0} P_D \tag{4.23}$$

where the typical ([18]) technological parameters shown in table 4.1 were used.

A frequently used compensation technique is the Miller compensation, shown in fig. 4.15. This technique allows for pole splitting between the first two poles which are approximately given by ([18])

$$f_{p1} \approx \frac{1}{2\pi g_{m6} R_1 R_2 C_C} \tag{4.24}$$

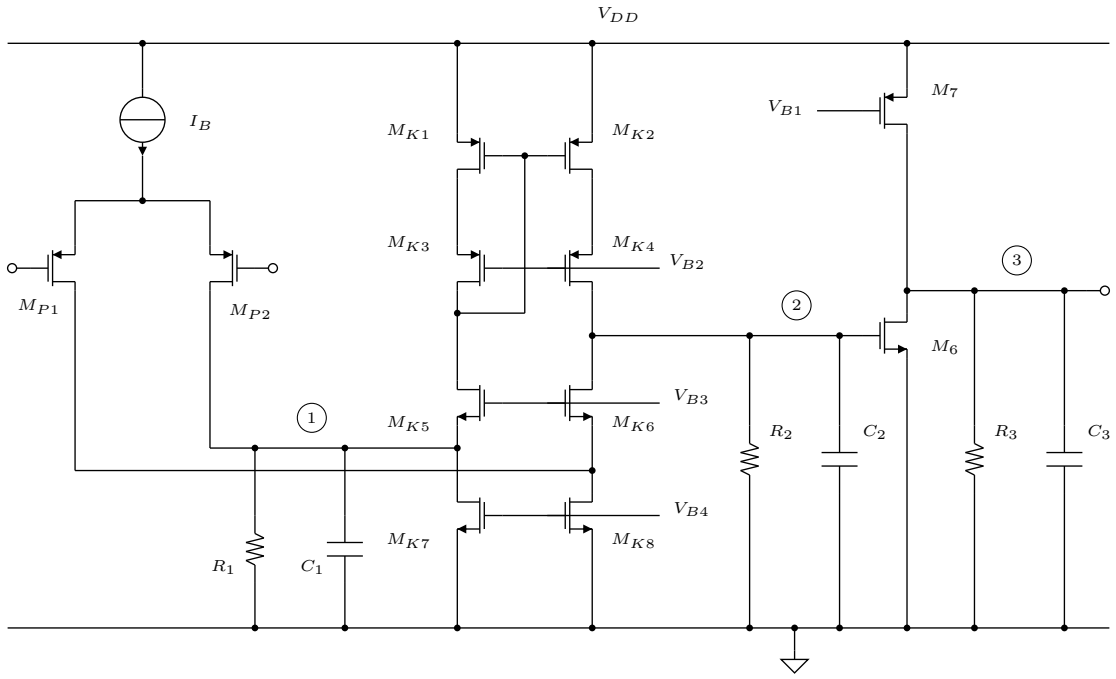

Figure 4.14: Two stage amplifier, circuit for the frequency response evaluation.

C'_{OX}	$1.75\,\mathrm{fF/\mu m^2}$
$C_{gs,O}$	$0.2\,\mathrm{fF/\mu m}$
$C_{gd,O}$	$0.2\,\mathrm{fF/\mu m}$
$C_{gb,O}$	$0.1\,\mathrm{fF/\mu m}$
C'_{j0}	$0.4\,\mathrm{fF/\mu m^2}$
C'_{jSW0}	$0.1\,\mathrm{fF/\mu m}$

Table 4.1: Capacitance technology parameters.

$$f_{p2} \approx \frac{g_{m6}C_C}{2\pi(C_C C_1 + C_1 C_2 + C_C C_2)}. \tag{4.25}$$

Miller compensation also yields a RHP zero at

$$f_z = \frac{g_{m6}}{2\pi C_C} \tag{4.26}$$

which causes the phase to decrease hence reduces phase margin. There are several ways to tackle the RHP zero problem; since the zero arises because of the bypass path around M_6, one way of avoiding it is that of feeding back the current indirectly

([18]) as can bee seen in the complete circuit shown in fig. 4.16.

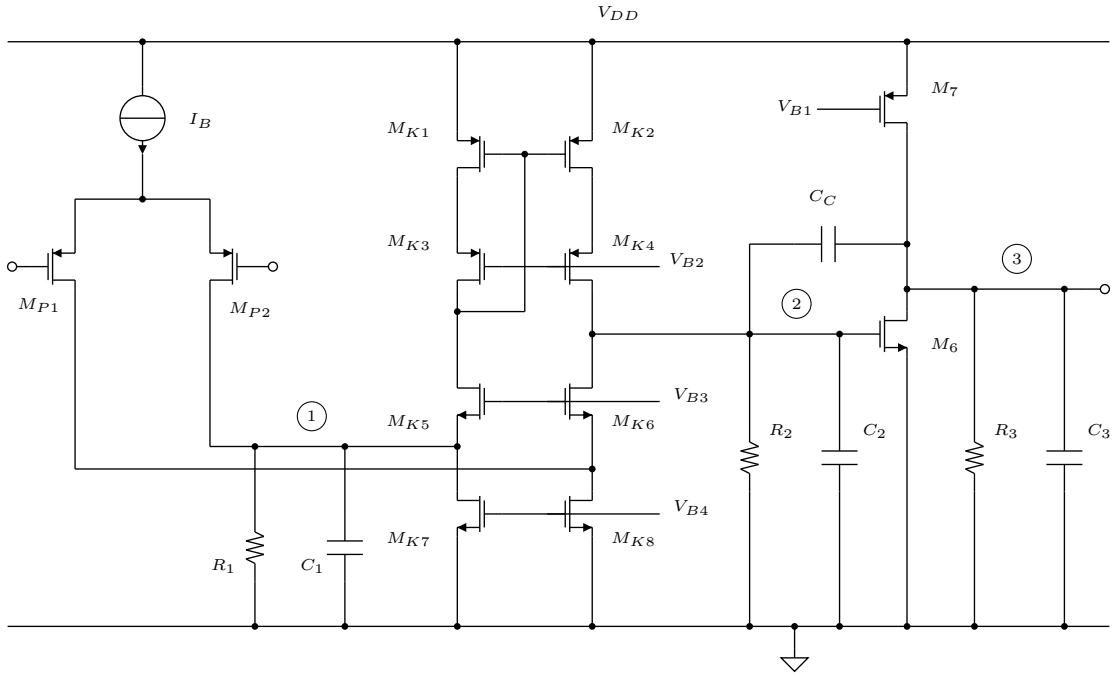

Figure 4.15: Two stage amplifier with Miller compensation.

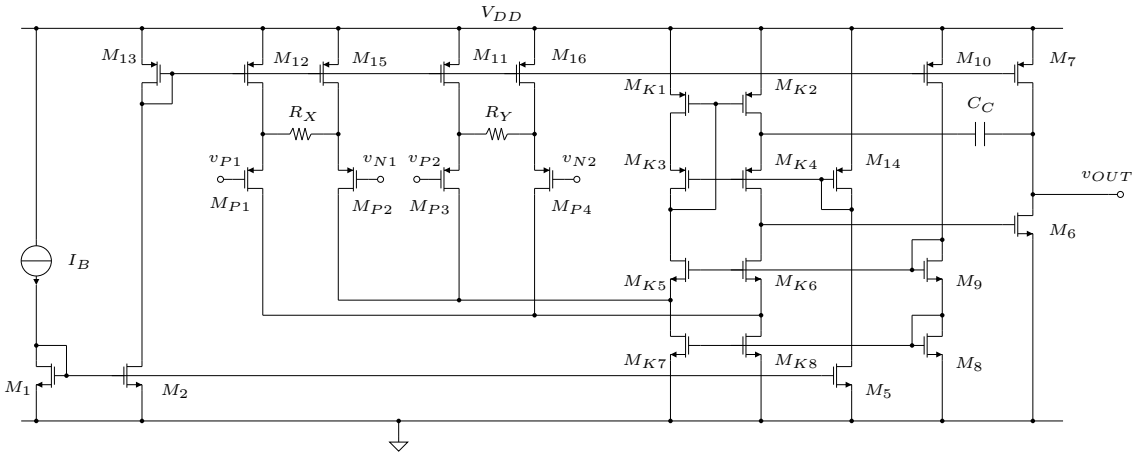

Figure 4.16: Differential difference amplifier. All nMOS have the body connected to ground and all pMOS have the body connected to V_{DD}.

Resistances R_X and R_Y have the same value of 40 kΩ, calculated so that the maximum differential signal at the input of the pairs does not cause the input transistors to turn off.

The symbol used for the DDA is shown in fig. 4.17.

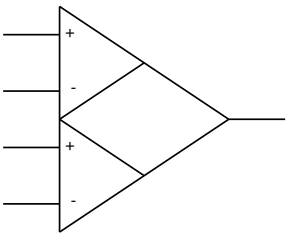

Figure 4.17: Differential difference amplifier, symbol.

The extracted parameters for the MOSFETs, obtained as average values for different polarization conditions, are shown in table 4.2. The indicated threshold voltages assume no body effect; in case of body effect a slightly higher threshold voltage is used.

Type	V_{TH}	λ	μC_{OX}
n	$0.51\,\mathrm{V}$	$0.024\,\mathrm{V}^{-1}$	$100\,\mu\mathrm{A/V}^2$
p	$-0.75\,\mathrm{V}$	$0.026\,\mathrm{V}^{-1}$	$46\,\mu\mathrm{A/V}^2$

Table 4.2: Extracted MOSFET parameters.

Since there are no particular constraints on the transconductance of M_6, its aspect ratio is chosen so that it can be correctly driven by the cascode stage. The aspect ratios of the transistors are shown in table 4.3.

The open loop gain of the DDA is simulated by using the testbench shown in fig. 4.18. The frequency response is plotted in fig. 4.19. The AC simulation shows a DC open loop gain of $\approx 100\,\mathrm{dB}$ and

$$GBW \simeq 20\,\mathrm{MHz} \tag{4.27}$$

$$PM \simeq 75°. \tag{4.28}$$

Since the capacitance values used to estimate the frequency response are typical values, the frequency response was simulated also for variations of the load capacitance and the compensation capacitance. The load capacitance is represented by the gate capacitance of M_A (fig. 4.24) and it is estimated to be $\approx 15\,\mathrm{fF}$. However, this is

Device	AR
M_1, M_2, M_5	6/1.2
M_6	1.2/1
M_8	4.3/1.2
M_9	27.6/1.2
M_{10}	13/1.2
M_7, M_{11}, M_{12}, M_{13}, M_{15}, M_{16}	10.8/1
M_{14}	0.84/1.2
M_{P1}, M_{P2}, M_{P3}, M_{P4}	154/1
M_{K1}, M_{K2}	5.4/0.7
M_{K3}, M_{K4}	49/1
M_{K5}, M_{K6}	23/1
M_{K3}, M_{K4}	7.5/0.7

Table 4.3: DDA transistor sizes.

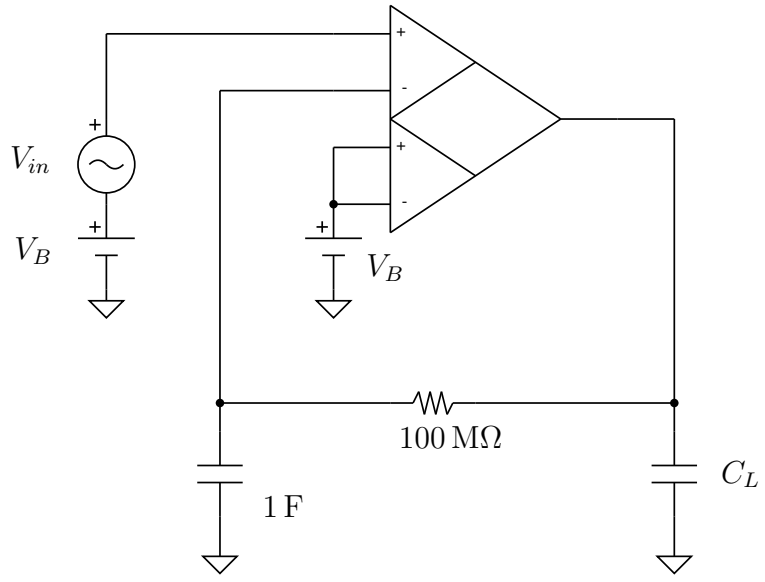

Figure 4.18: DDA AC simulation testbench.

a typical value and it does not account for layout parasitic capacitances so the open loop response was simulated for $C_{L1} = 30\,\text{fF}$ and $C_{L1} = 100\,\text{fF}$. The results plotted

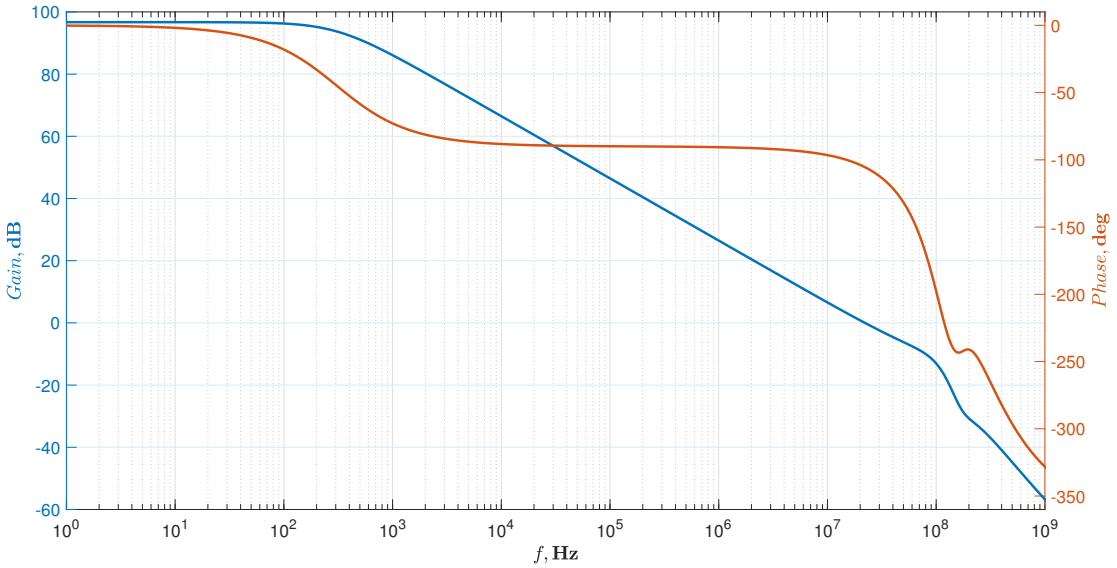

Figure 4.19: Open loop gain of DDA.

in fig. 4.20 show that both the GBW and the PM do not change much, thanks to the fact that C_C is much larger than both C_1 and C_2.

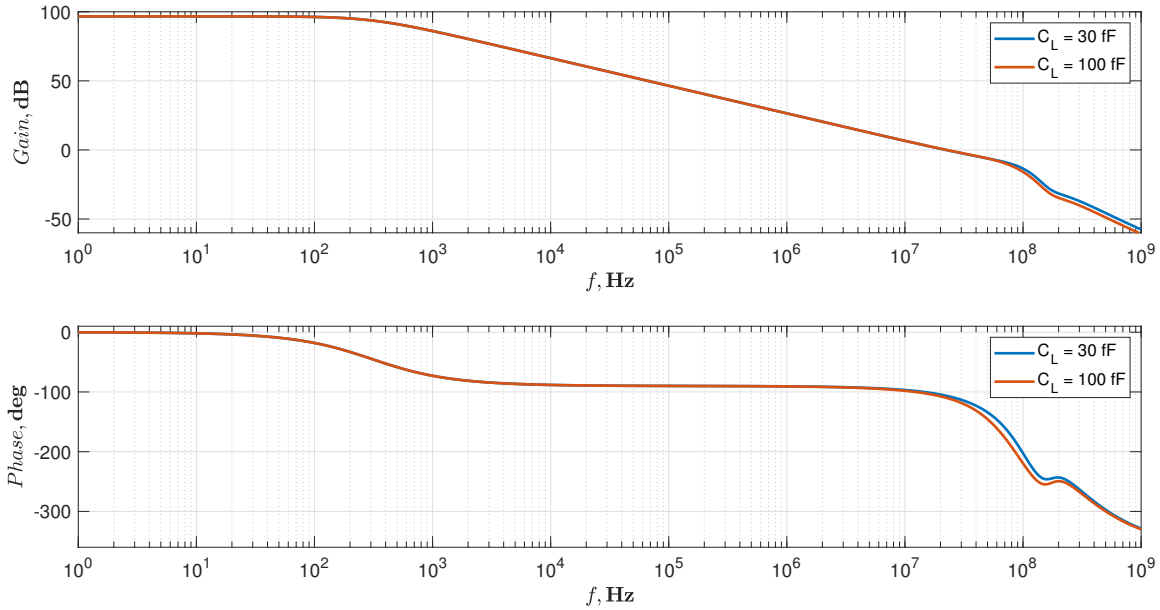

Figure 4.20: Open loop gain of DDA for different load capacitances.

The open loop response has also been simulated for a ±20% variation of the compensation capacitor value. The results are shown in fig. 4.21.

Finally, the output swing was simulated by using the testbench shown in fig. 4.22.

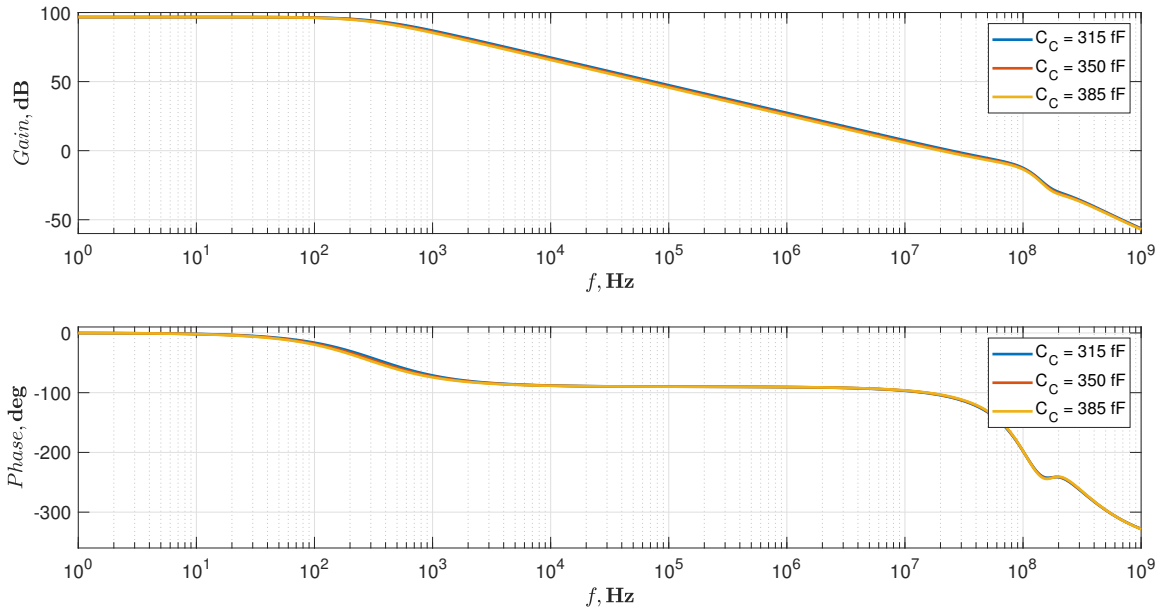

Figure 4.21: Open loop gain of DDA for ±20% compensation capacitance variation.

From the results plotted in fig. 4.23 it can be seen that the output can virtually drop down to zero hence the amplifier is able to correctly drive M_A even at the minimum input signal value.

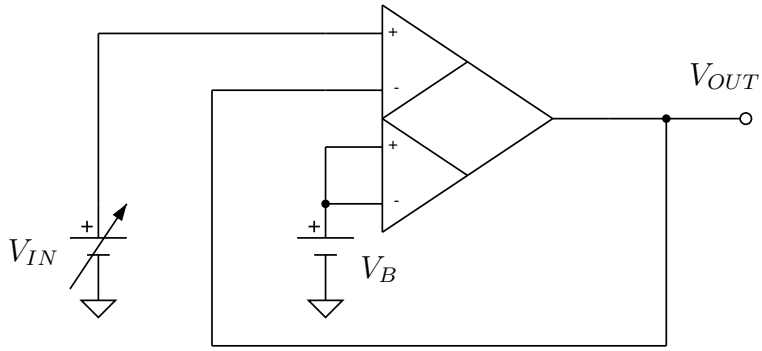

Figure 4.22: DDA DC simulation testbench.

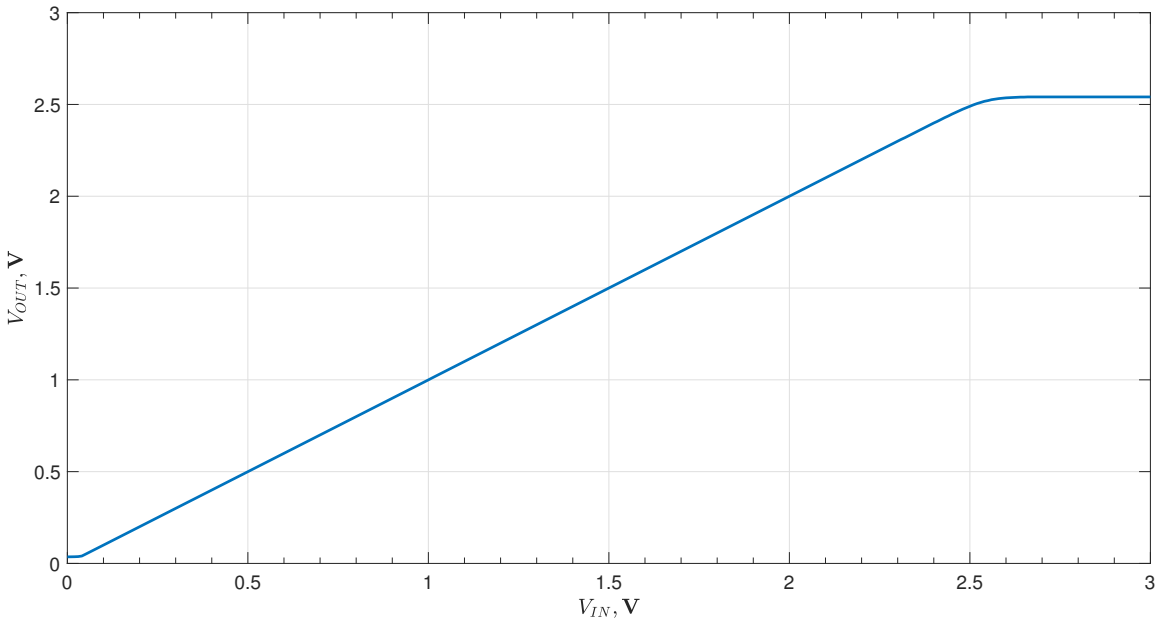

Figure 4.23: Output voltage swing of DDA.

4.4 Temperature dependence

The logarithmic characteristic has been compensated for the temperature variations by removing the I_S from the expression. However, there is still a temperature dependence which is represented by the thermal voltage V_T. The voltage across a diode is directly proportional to the absolute temperature. This temperature dependence can be theoretically removed by using an amplifier having a CTAT gain. Indeed, assuming that an amplifier with a gain $A = \frac{K}{V_T}$ is available, the output voltage would be independent of temperature variations. In discrete realizations the solution was that of using a temperature dependent resistor to set the gain of an operational amplifier. This is not possible in integrated circuits since, although integrated resistors with different temperature coefficients are available, it is not possible to realize a precise ratio of resistors built in different process steps. One possible solution is that of using a current multiplier/divider circuit. A current output is required so the logarithmic amplifier is modified in the following way (fig. 4.24).

The output current is given by

$$i_{LOG} = \frac{v_{LOG}}{R_1} = \frac{1}{R_1}\left(V_{REF} + V_T \ln\left(\frac{i_{IN}}{I_0}\right)\right). \tag{4.29}$$

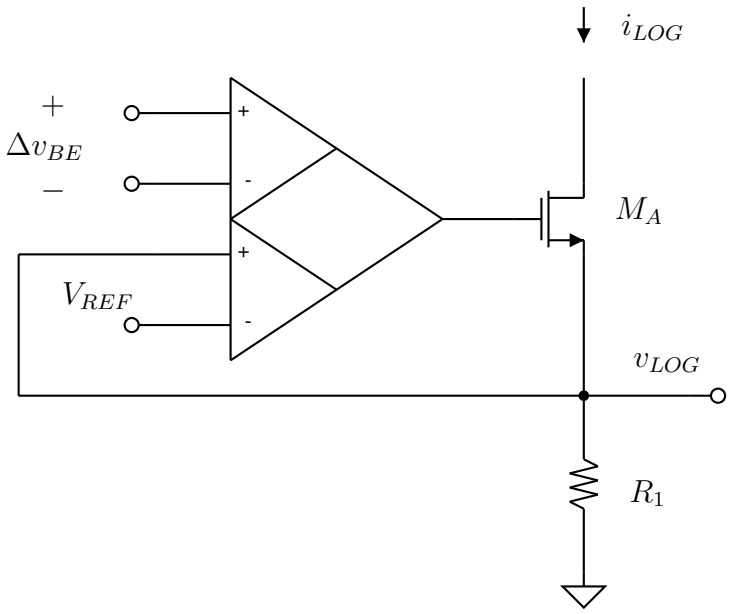

Figure 4.24: Differential difference amplifier, current output.

R_1 is chosen to be 29.8 kΩ so that the maximum current is $i_{LOG,max} = 10\,\mu A$. The i_{LOG} current, as written in eq. (4.29), has a PTAT (proportional to absolute temperature) component and a constant component related to V_{REF}. If V_{REF} is made PTAT, the output current is then exactly PTAT as well. The temperature dependence is removed by dividing i_{LOG} by a PTAT current and multiplying it by a temperature independent reference current, as shown in fig. 4.25

$$i_{ADC} = \frac{i_{LOG}}{I_{PTAT}} I_{REF}. \tag{4.30}$$

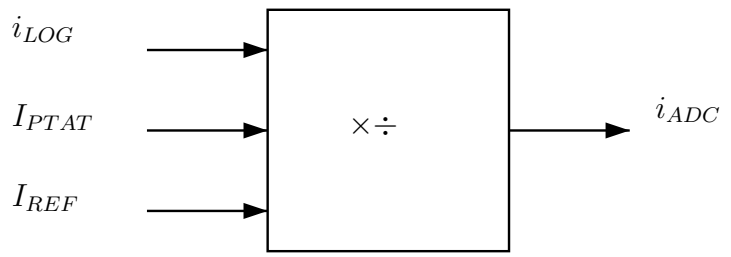

Figure 4.25: Current multiplier/divider block.

4.4.1 Current multiplier/divider

A current multiplier/divider presented in the literature [19] is based on a translinear loop (shown in fig. 4.26). The circuit operation can be analyzed in a simple way by neglecting the base currents (this implies large enough current gain). Transistors Q_A, Q_B, Q_C are current driven by I_1, I_2, I_3 respectively. The 4 v_{BE} voltages form a translinear loop and the base-emitter voltage of Q_D is given by

$$v_{BE,D} = v_{BE,A} + v_{BE,B} - v_{BE,C}. \tag{4.31}$$

Since each v_{BE} voltage is a logarithmic function of the collector current, the output current is given by

$$i_4 = \frac{i_1 \cdot i_2}{i_3}. \tag{4.32}$$

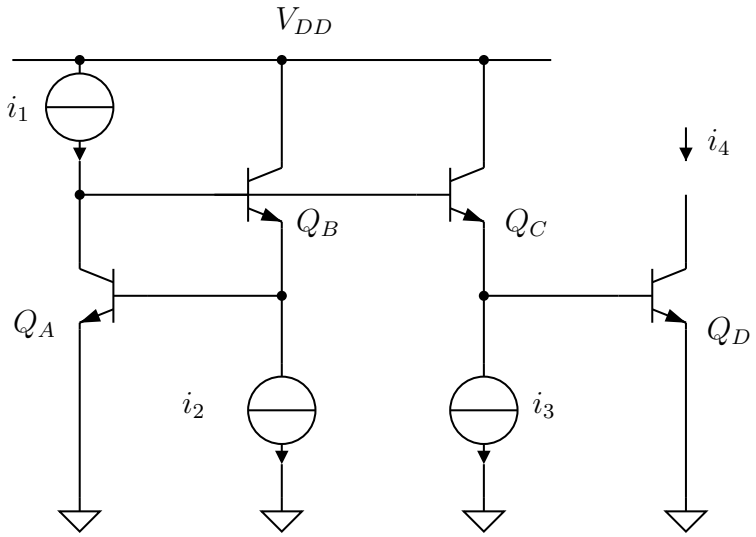

Figure 4.26: Current multiplier/divider.

A modified version of this circuit has been presented [20] that allows to reduce the error due to the finite current gain of the transistors (fig. 4.27).

Two DC simulations of the multiplier/divider are shown in fig. 4.28 (division by 1) and in fig. 4.29 (division by 2).

The AC response is shown in fig. 4.30 (divider by one) and in fig. 4.31 (divider by two). It can be seen that the $-3\,\mathrm{dB}$ bandwidth extends well beyond $10\,\mathrm{MHz}$.

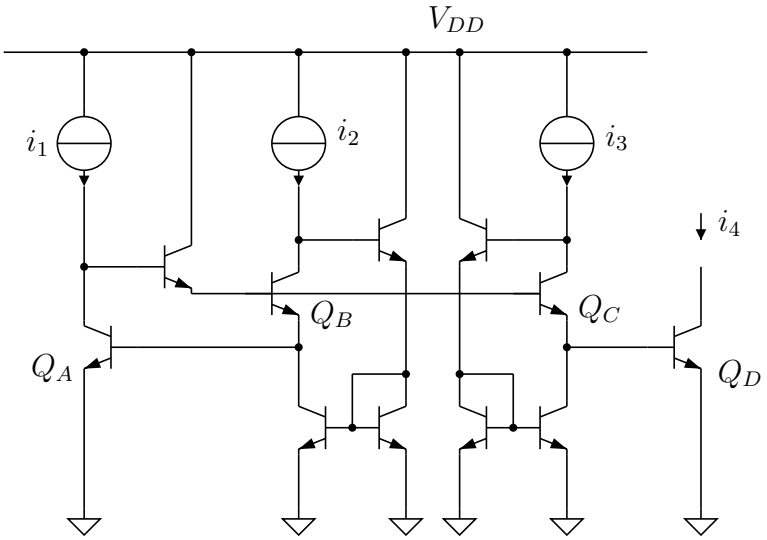

Figure 4.27: Improved current multiplier/divider.

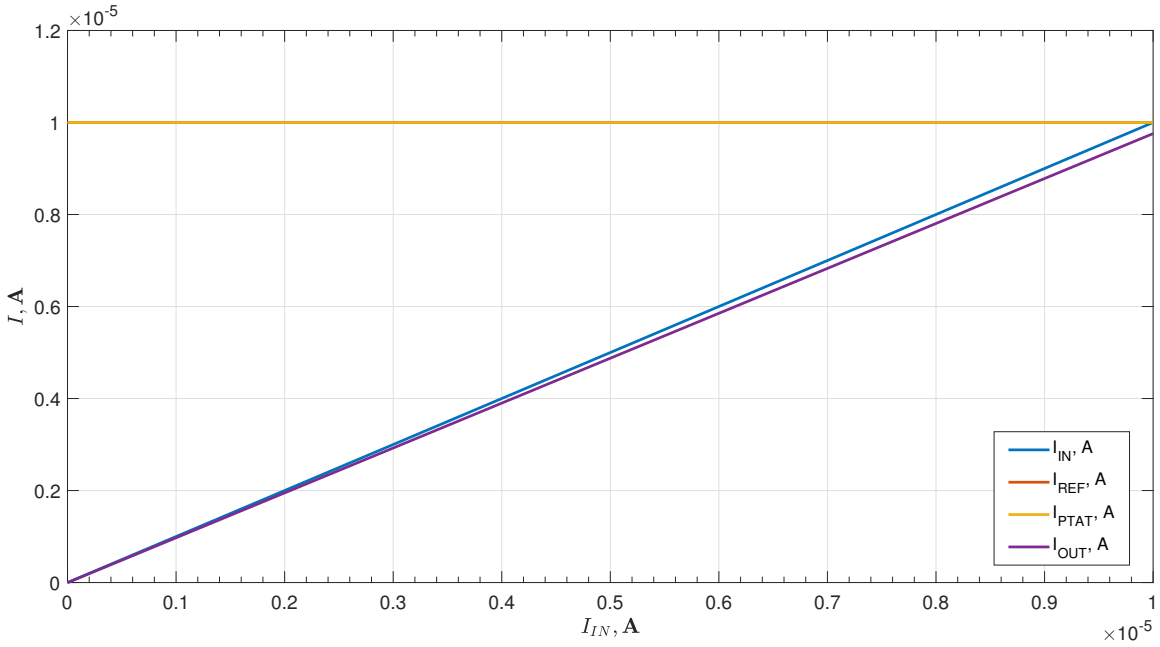

Figure 4.28: DC sweep of divider by one.

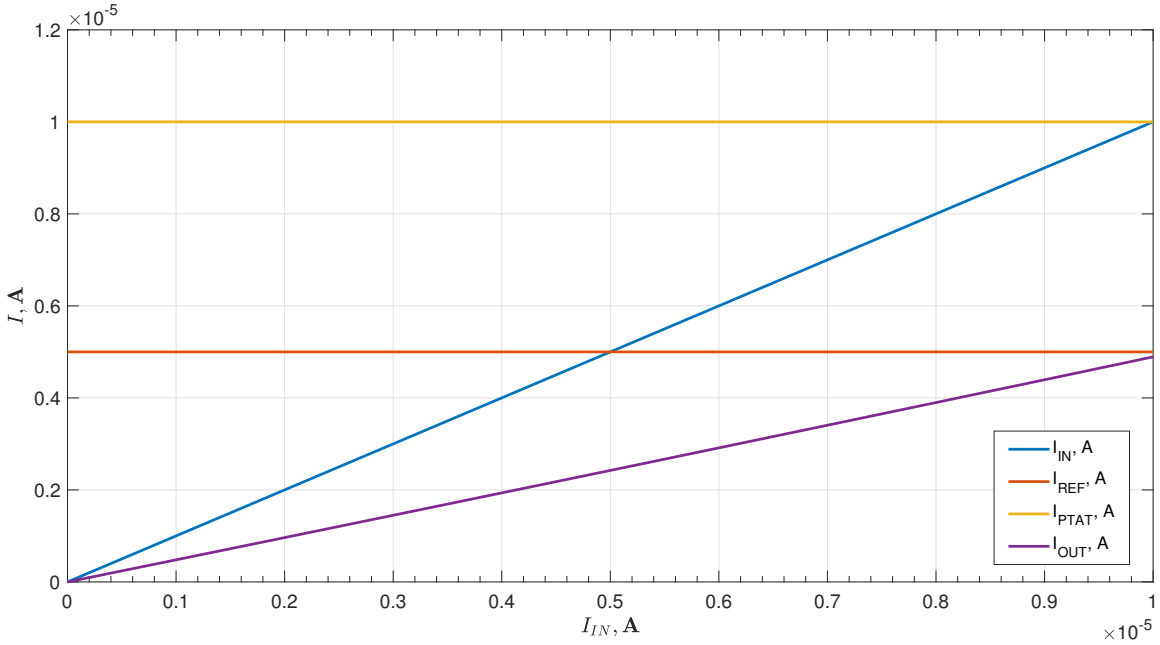

Figure 4.29: DC sweep of divider by two.

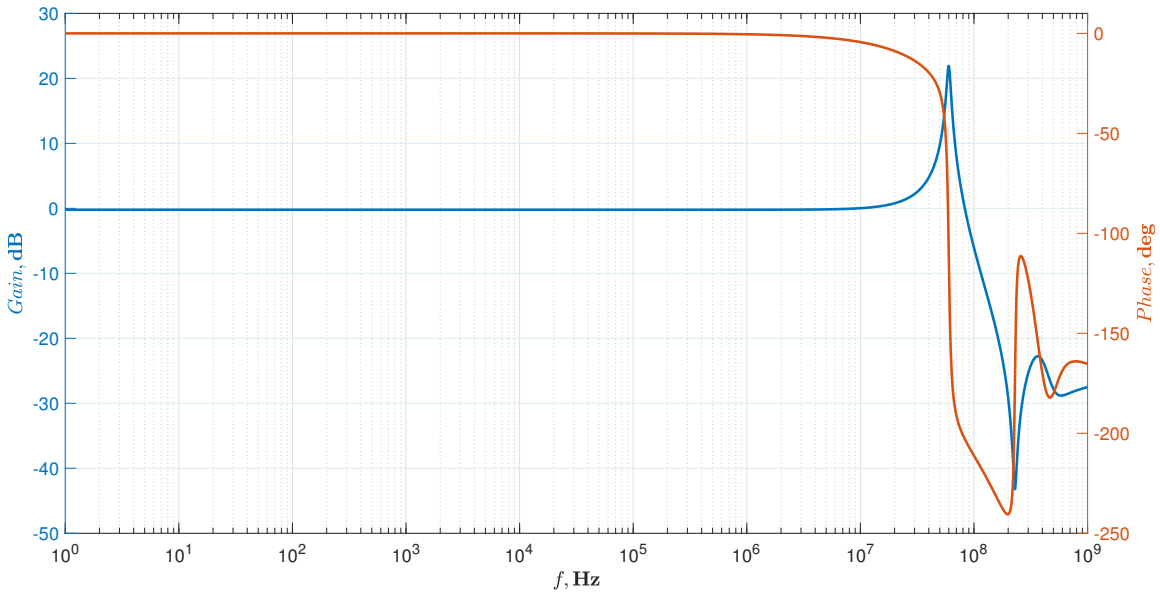

Figure 4.30: AC response of divider by one.

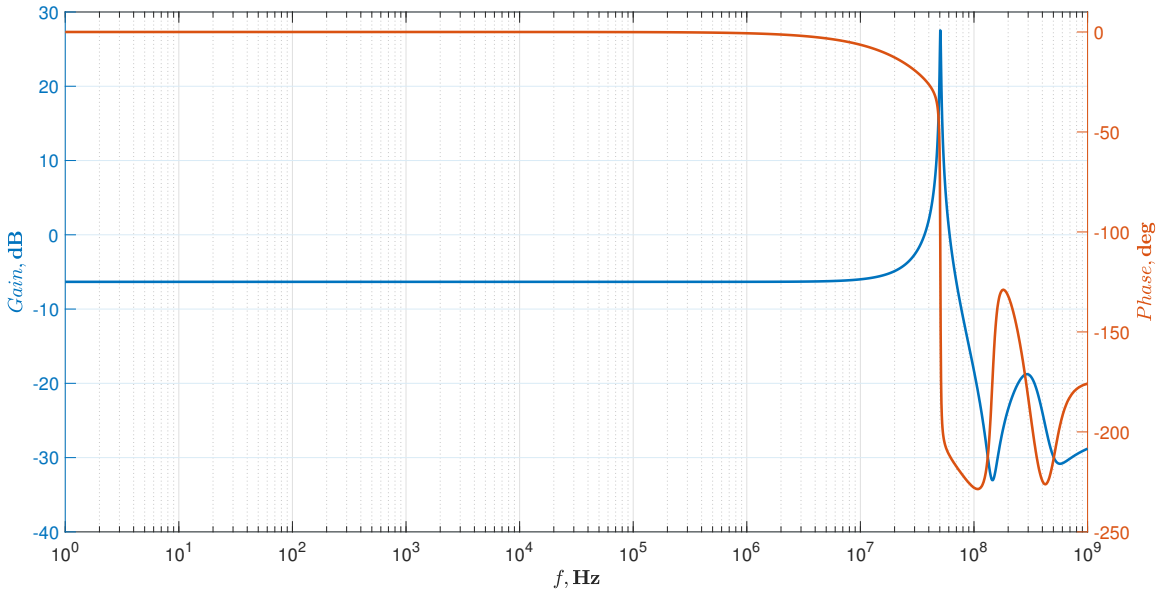

Figure 4.31: AC response of divider by two.

4.4.2 PTAT references

In order for i_{LOG} to be truly PTAT, the reference voltage used to shift the Δv_{BE} should also be PTAT. The schematic of a PTAT current reference [18] is shown in fig. 4.32. It is composed of the startup circuit whose task is to make the zero current equilibrium point an unstable one and the two back-to-back cascode mirrors that force the same current through the two bipolar transistors. The two BJTs have different emitter areas so as to generate a PTAT voltage drop across the resistor R. The current through R is given by

$$I_{PTAT} = \frac{V_T}{R} \ln L. \tag{4.33}$$

A PTAT voltage can be obtained by simply forcing the PTAT current through a resistor.

$$V_{PTAT} = MV_T \ln L. \tag{4.34}$$

Simulations of the circuit show the operation in a temperature range from $-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$. The current and the voltage are plotted in fig. 4.33 and fig. 4.34 respectively.

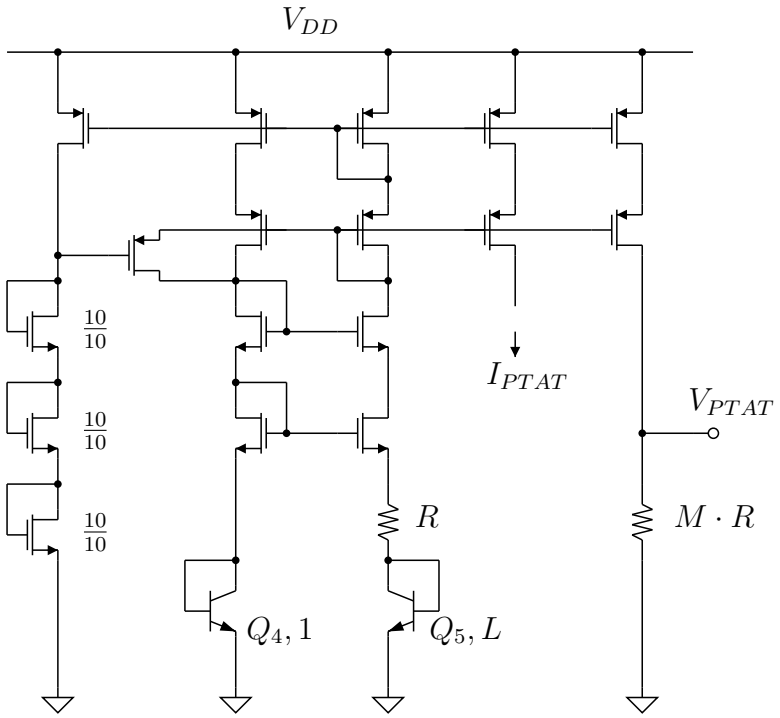

Figure 4.32: PTAT current and voltage references. All unlabeled pMOS are $\frac{30}{1}$ and all unlabeled nMOS are $\frac{10}{1}$. nMOS have the body connected to ground while pMOS have the body connected to V_{DD}.

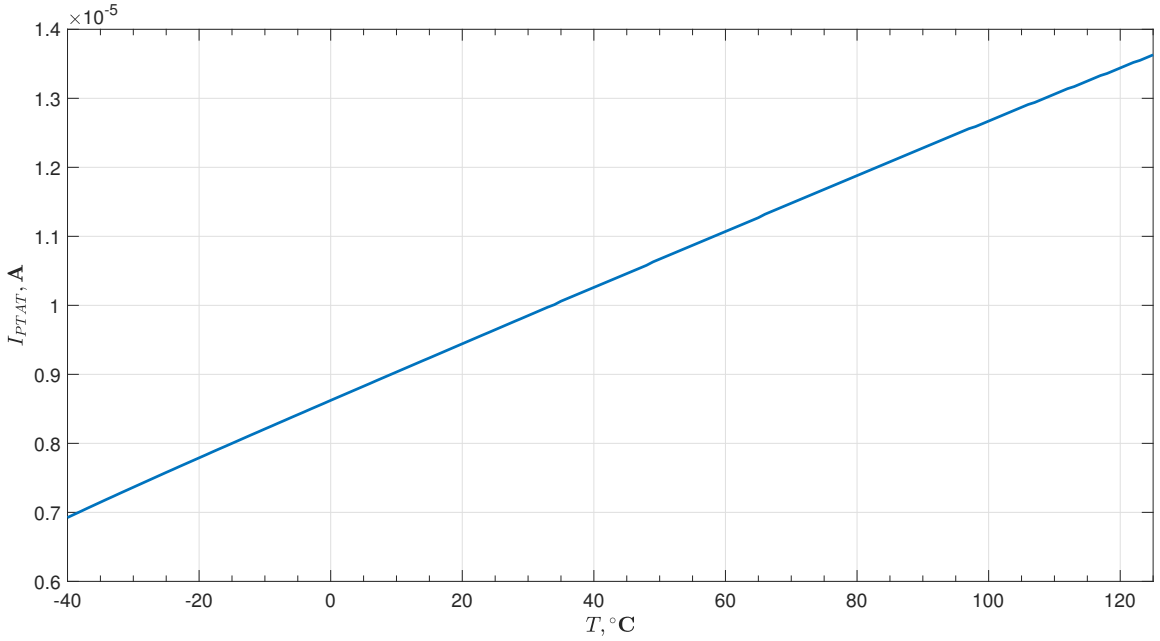

Figure 4.33: PTAT current.

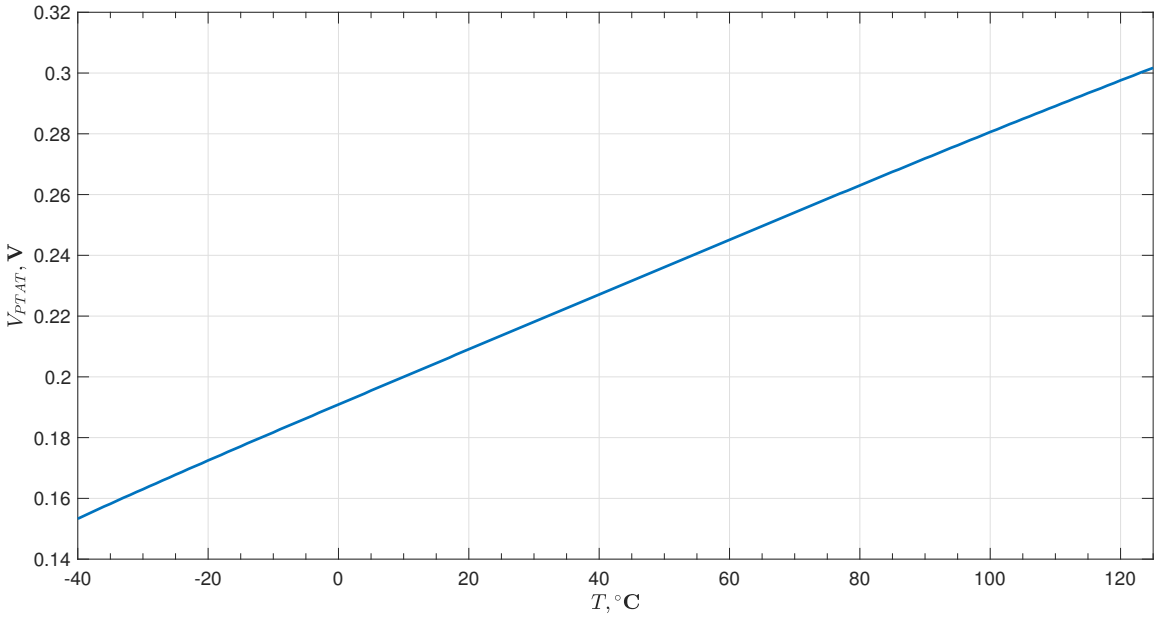

Figure 4.34: PTAT voltage.

4.4.3 High compliance current mirror

The current at the output of the translinear circuit is (approximately) not dependent on the temperature. It can now be converted into a voltage by forcing it through a resistor. The output voltage should be referred to ground so a current mirror can copy the current sinked by the temperature compensation circuitry into an output resistor. In order to have a high output impedance and a good voltage swing, an improved p type current mirror is used. The circuit has been presented in [21] and it allows for an accurate mirroring over a wide range of output voltage. Regulated cascode structures M_1-M_4 and M_5-M_8 behave like MOS transistors with higher output resistance. N type MOSFETs M_4 and M_8 are employed to push M_1 and M_5 at the border of the saturation region hence the output voltage compliance improves.

DC simulation (fig. 4.36) shows excellent matching between in and out currents up to 10 µA with the output node voltage up to 2.8 V (280 kΩ resistor connected at the output node). AC simulation (fig. 4.37) shows that the −3 dB bandwidth goes up to around 10 MHz. The transistor sizes are given in table 4.4.

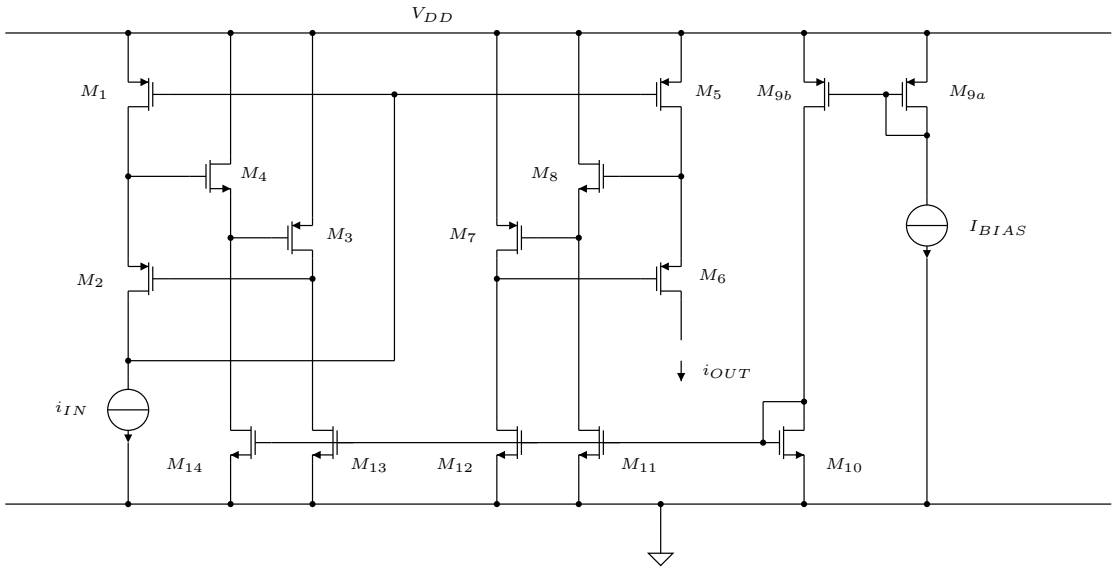

Figure 4.35: High compliance current mirror. nMOS have the body connected to ground while pMOS have the body connected to V_{DD}.

Device	AR
M_1, M_2, M_5, M_6	30/0.5
M_3, M_7	0.5/0.5
M_4, M_8	0.5/0.5
M_{9a}	15/0.5
M_{9b}, M_{10}, M_{11}, M_{14}	1.5/0.5
M_{12}, M_{13}	1.5/0.5

Table 4.4: Current Mirror MOSFET sizes.

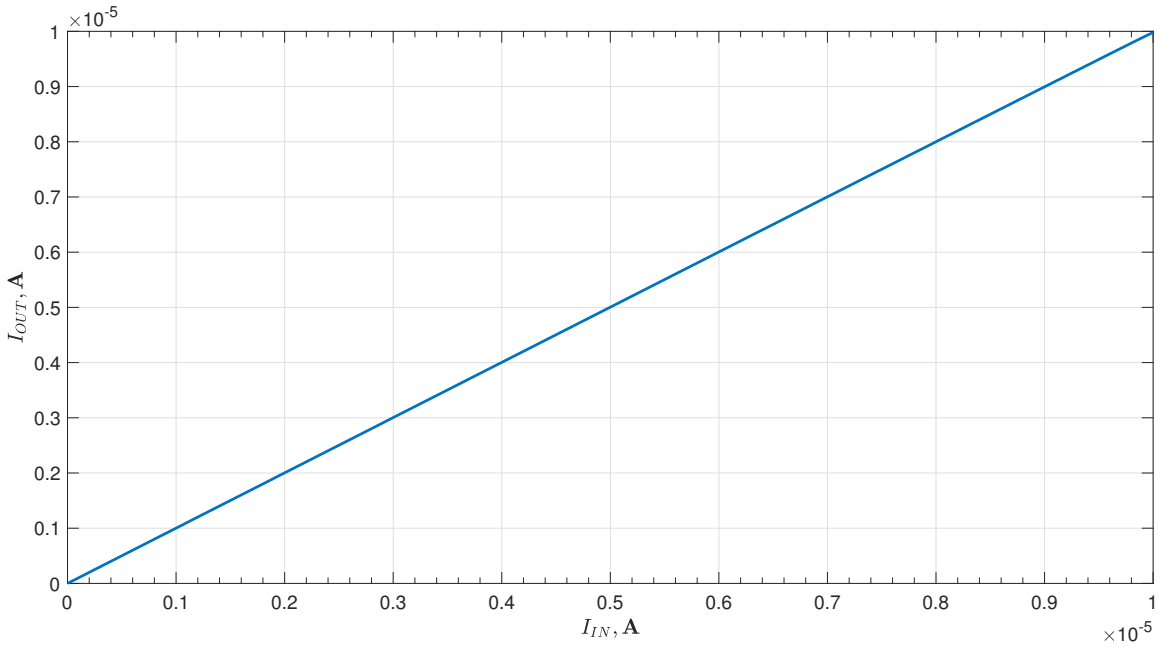

Figure 4.36: Output current mirror characteristic.

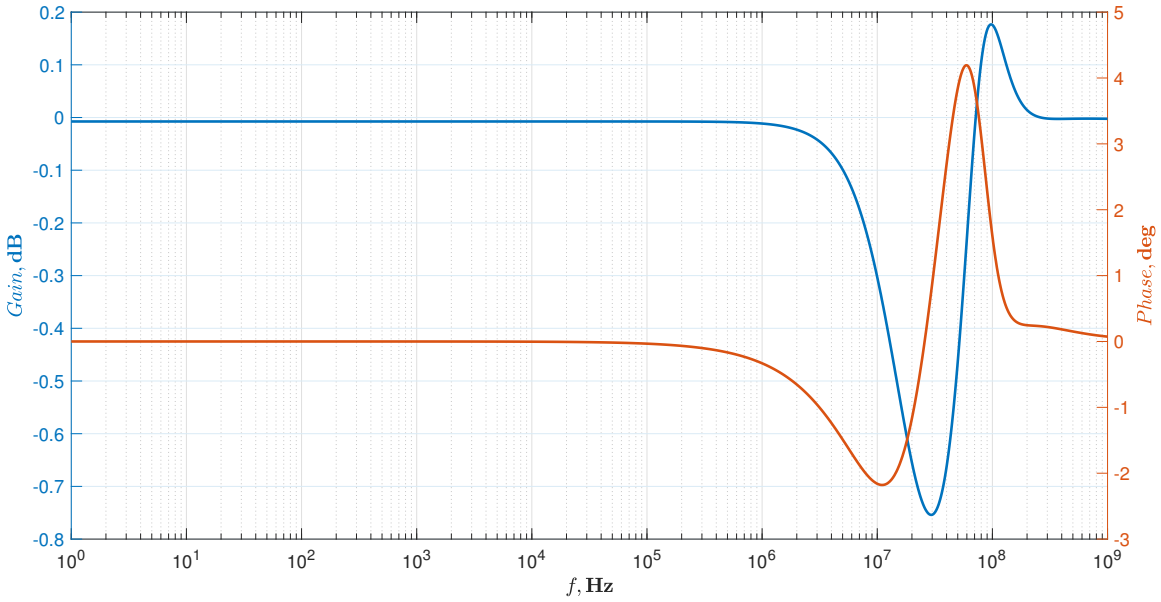

Figure 4.37: Output current mirror AC response.

4.5 Simulations

The complete logarithmic amplifier is shown in fig. 4.38.

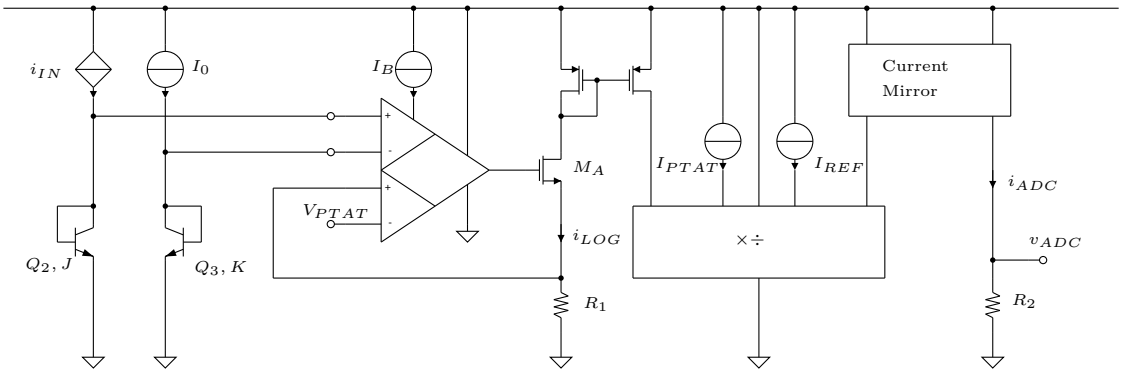

Figure 4.38: Temperature compensated logarithmic amplifier.

By combining the characteristics of all sub-blocks the input-output relation of the logarithmic amplifier is obtained as

$$v_{ADC} = V_Q + V_K \ln\left(\frac{i_{IN}}{I_0}\right) = \frac{R_2}{R_1}\left(I_{REF}RM + \frac{I_{REF}R}{\ln L}\ln\left(\frac{i_{IN}}{I_0}\right)\right). \tag{4.35}$$

It can be seen that this expression depends on the ratio of two resistors and on two fixed constants (L, M) which is desirable for reducing the technology dependent uncertainty. The product $I_{REF}R$ can also be made relatively technology independent since the current I_{REF} can be obtained by means of a resistor which is matched to R.

Simulated DC characteristic and the theoretical one are plotted in fig. 4.39 while in fig. 4.40 the input and output currents of the multiplier/divider circuit are shown.

Simulations at varying T were carried out in order to verify the reduced temperature dependence. The current at the input of the multiplier is plotted in fig. 4.41 for temperature varying between 0 °C and 100 °C while fig. 4.42 shows the current at the output of the multiplier in the same temperature range. The output voltage is shown in fig. 4.43.

AC simulation for input current from 10 nA to 200 µA is shown in fig. 4.44.

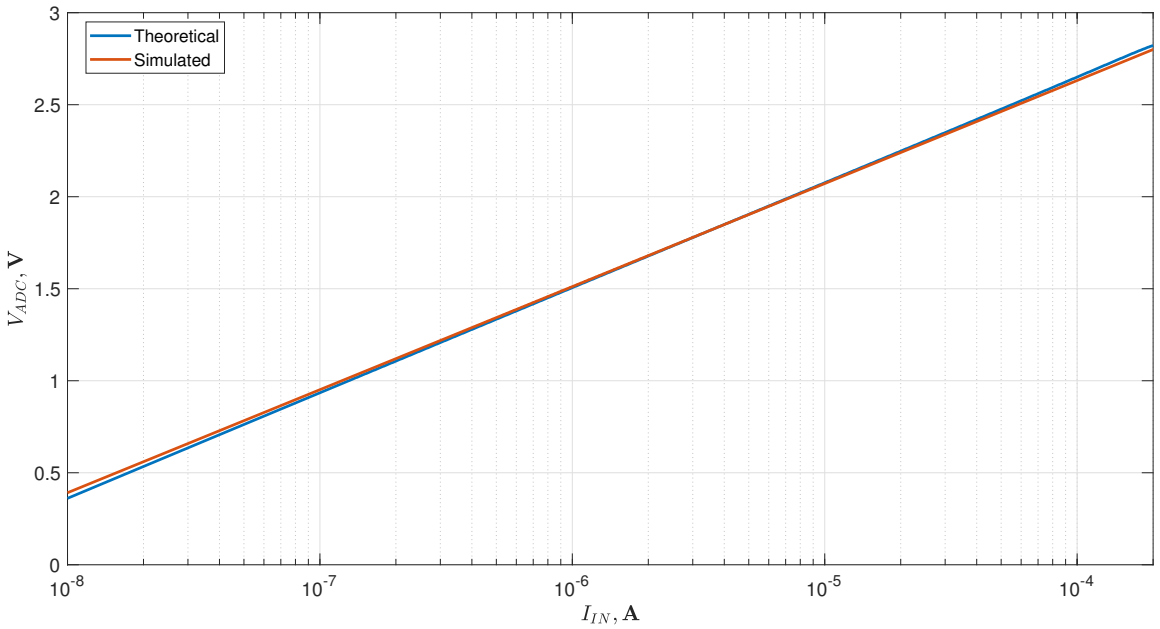

Figure 4.39: DC simulation, $V_{ADC}(I_{IN})$.

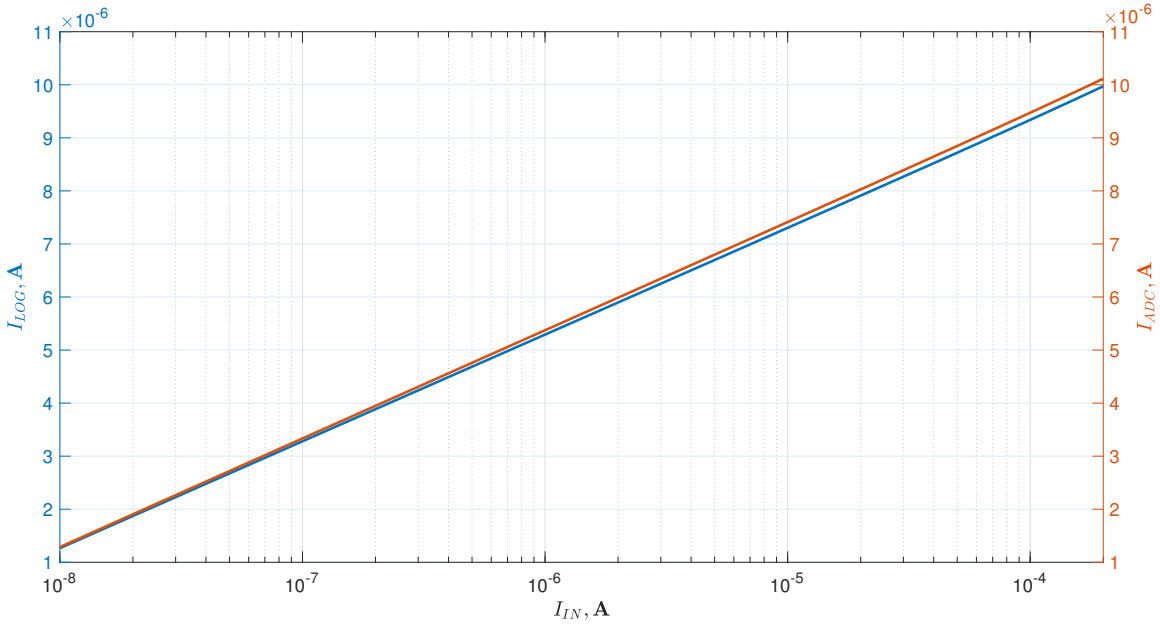

Figure 4.40: DC simulation, input and output currents of the multiplier/divider circuit.

The DC simulations show a good linearity and a good compensation of the temperature effects. The relative error of the simulated output voltage with respect to the ideal one is plotted in fig. 4.45. It shows a relative error of about 9% at minimum

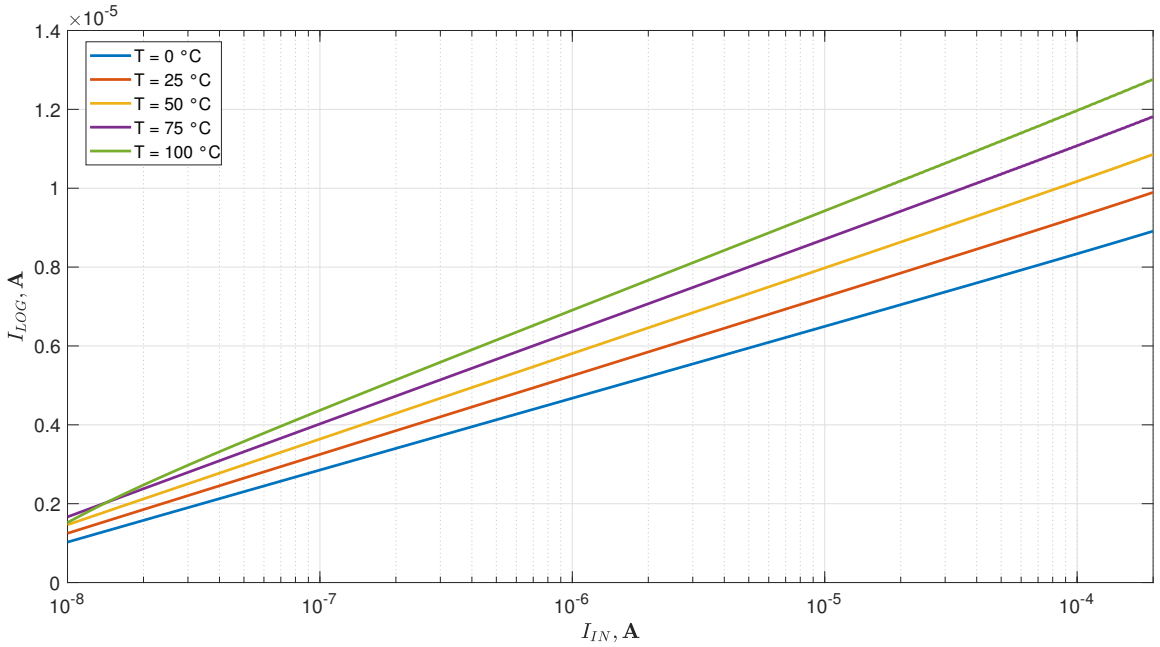

Figure 4.41: DC simulation with varying T, multiplier input current.

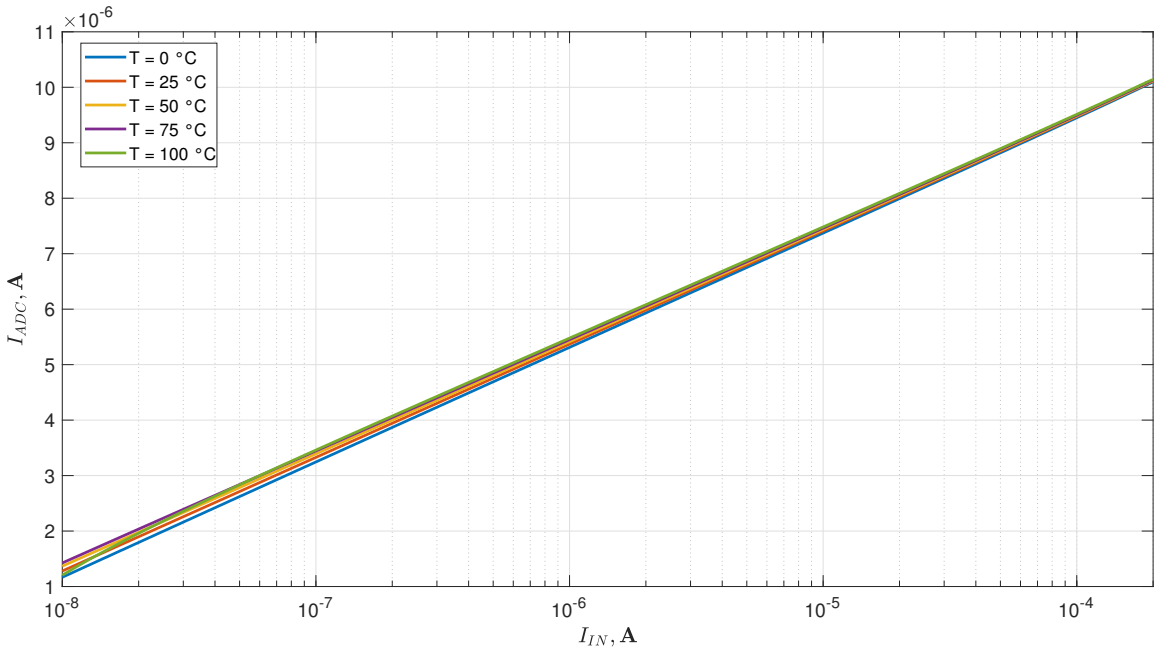

Figure 4.42: DC simulation with varying T, multiplier output current.

current down to about 1% at maximum current. From the AC simulation it can be seen that the $-3\,\mathrm{dB}$ bandwidth at minimum input current is slightly lower than the target. This is due to the fact that the employed circuit still comprises a voltage to current amplifier as fig. 2.1, hence the transconductance of transistor M_A decreases

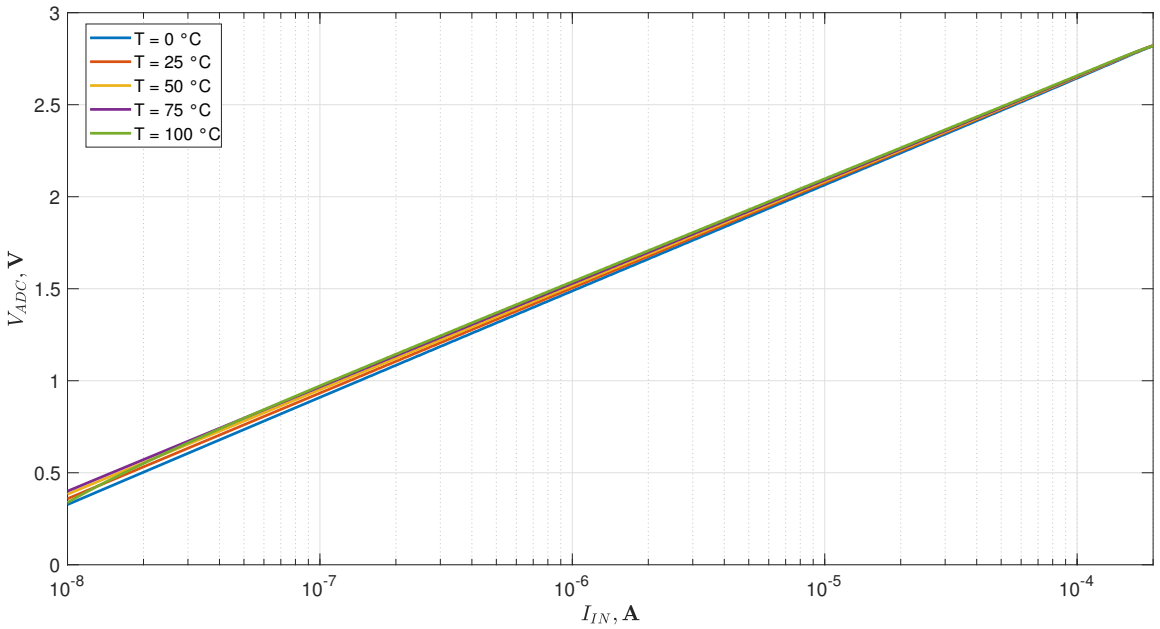

Figure 4.43: DC simulation with varying T, output voltage.

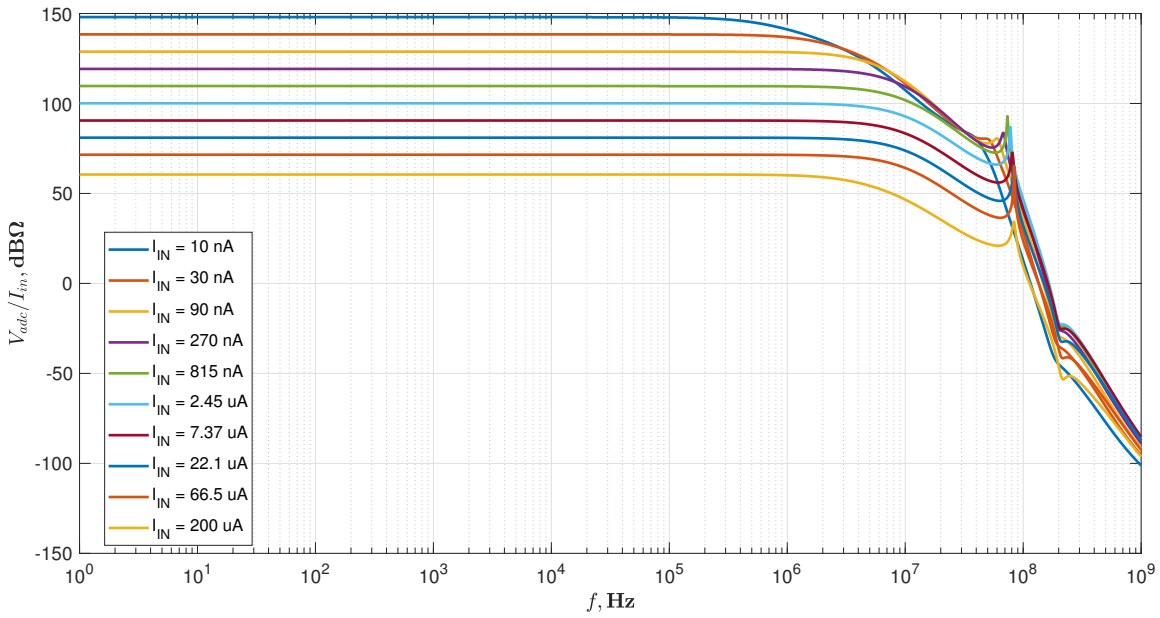

Figure 4.44: AC simulation, Gain = $\frac{V_{adc}}{I_{in}}$.

with the input signal. However, the improvement in terms of bandwidth with respect to fig. 2.1 is clear; indeed, the signal variation range has been compressed from 4.3 decades to 1 decade, hence the system bandwidth limitation is reduced.

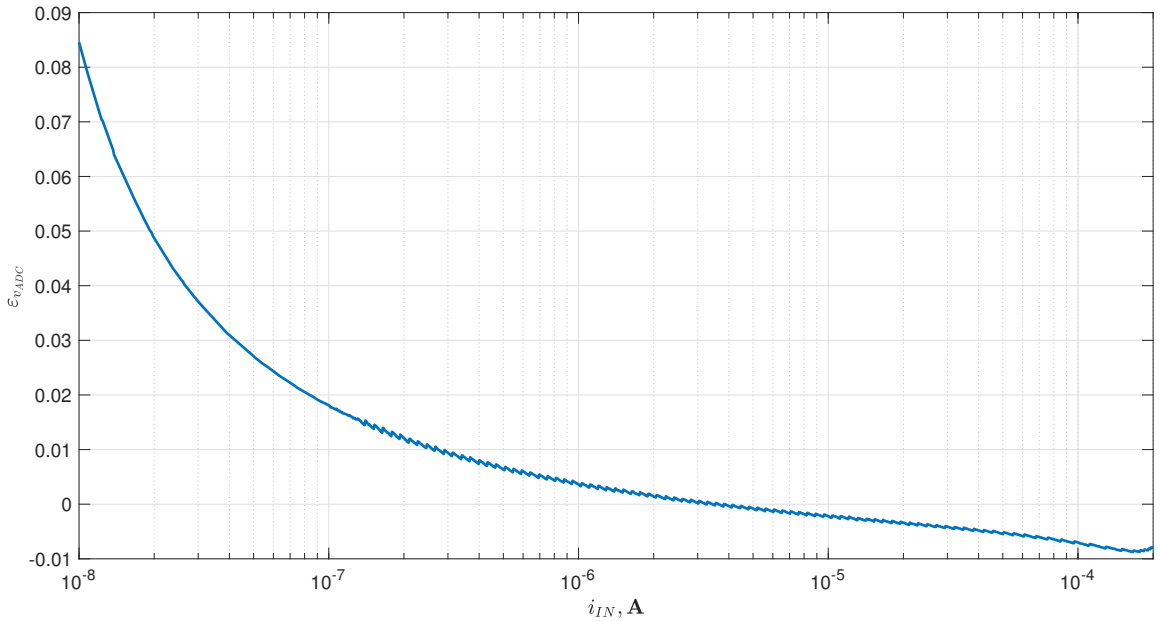

Figure 4.45: v_{ADC} relative error over the whole input current range.

CHAPTER 5

Conclusions and future work

A current sensing system based on nonuniform quantization is presented. As shown in the previous chapters, nonuniform quantization yields constant relative quantization error hence allowing for the measurement of weak signals. The system bandwidth is weakly dependent on signal amplitude since the variation range has been compressed through a logarithmic amplification. This relaxes the requirements on the gain-bandwidth product of the operational amplifier. Also, temperature dependence has been compensated for. Time domain simulations at system level show that the resolution, although the analog conditioning would allow to overcome this problem, can be deteriorated by the not sufficiently high sampling frequency. Circuit level simulation results show that the DC accuracy of the circuit ranges is around 9% at minimum input signal. The minimum bandwidth is about 1 MHz in the worst case conditions (minimum input current).

Following issues could be considered for future work:

- An accurate study of the optimal sampling frequency for nonlinear conditioning circuits.
- The issue of signal rectification remains open. It is necessary to overcome bandwidth limitations encountered in conventional schemes such as the one presented in chapter 2.

Bibliography

[1] S. Ziegler, R. C. Woodward, H. H. Iu, and L. J. Borle, "Current sensing techniques: A review", *IEEE Sensors Journal*, vol. 9, no. 4, pp. 354–376, Apr. 2009, ISSN: 1530-437X. DOI: 10.1109/JSEN.2009.2013914.

[2] F. Grover and I. S. of America, *Inductance Calculations: Working Formulas and Tables*, ser. Dover books on engineering and engineering physics. Instrument Society of America, 1946, ISBN: 9780876645574. [Online]. Available: https://books.google.it/books?id=rqceAQAAIAAJ.

[3] J. A. Ferreira, W. A. Cronje, and W. A. Relihan, "Integration of high frequency current shunts in power electronic circuits", *IEEE Transactions on Power Electronics*, vol. 10, no. 1, pp. 32–37, Jan. 1995, ISSN: 0885-8993. DOI: 10.1109/63.368463.

[4] R. Malewski, C. T. Nguyen, K. Feser, and N. Hylten-Cavallius, "Elimination of the skin effect error in heavy-current shunts", *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-100, no. 3, pp. 1333–1340, Mar. 1981, ISSN: 0018-9510. DOI: 10.1109/TPAS.1981.316606.

[5] L. Spaziani, "Using copper pcb etch for low vakue resistance", *Texas Instruments*, 1997. [Online]. Available: http://www.ti.com/lit/an/slua236/slua236.pdf.

[6] O. Aiello and F. Fiori, "A new current sensor based on MagFET highly immune to EMI", in *2009 International Conference on Electromagnetics in Advanced Applications*, Sep. 2009, pp. 784–787. DOI: 10.1109/ICEAA.2009.5297310.

[7] H. Mason, "Basic introduction to the use of magnetoresistive sensors", *Zetex*, 2003. [Online]. Available: https://www.diodes.com/diodes-part-files/SZ/ZR431/Application%20Notes/an37.pdf.

[8] J. Lenz and S. Edelstein, "Magnetic sensors and their applications", *IEEE Sensors Journal*, vol. 6, no. 3, pp. 631–649, Jun. 2006, ISSN: 1530-437X. DOI: 10.1109/JSEN.2006.874493.

[9] E. Udd and W. Spillman, *Fiber Optic Sensors: An Introduction for Engineers and Scientists: Second Edition*. Jul. 2011. DOI: 10.1002/9781118014103.

[10] P. A. Nicati and P. Robert, "Stabilised current sensor using sagnac interferometer", *Journal of Physics E: Scientific Instruments*, vol. 21, no. 8, pp. 791–796, Aug. 1988. DOI: 10.1088/0022-3735/21/8/010. [Online]. Available: https://doi.org/10.1088%2F0022-3735%2F21%2F8%2F010.

[11] K. Bohnert, P. Gabus, J. Nehring, and H. Brandle, "Temperature and vibration insensitive fiber-optic current sensor", *Journal of Lightwave Technology*, vol. 20, no. 2, pp. 267–276, Feb. 2002, ISSN: 0733-8724. DOI: 10.1109/50.983241.

[12] S. Heidary Shalmany, D. Draxelmayr, and K. A. A. Makinwa, "A ±36-A Integrated Current-Sensing System With a 0.3% Gain Error and a 400 µA Offset From −55 °C to 85 °C", *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 1034–1043, Apr. 2017. DOI: 10.1109/JSSC.2016.2639535.

[13] G. Palumbo and S. Pennisi, *Feedback amplifiers: Theory and design*. Springer US, 2007, ISBN: 9780306480423. [Online]. Available: https://books.google.it/books?id=w4jqBwAAQBAJ.

[14] P. F. Panter and W. Dite, "Quantization distortion in pulse-count modulation with nonuniform spacing of levels", *Proceedings of the IRE*, vol. 39, no. 1, pp. 44–48, Jan. 1951, ISSN: 0096-8390. DOI: 10.1109/JRPROC.1951.230419.

[15] B. Smith, "Instantaneous companding of quantized signals", *The Bell System Technical Journal*, vol. 36, no. 3, pp. 653–710, May 1957, ISSN: 0005-8580. DOI: 10.1002/j.1538-7305.1957.tb03858.x.

[16] R. Edwards and J. Durkin, "Application of non-uniform quantization to closed-loop digital systems", *Journal of Physics E: Scientific Instruments*, vol. 2, no. 4, pp. 321–326, Apr. 1969. DOI: 10.1088/0022-3735/2/4/305. [Online]. Available: https://doi.org/10.1088%2F0022-3735%2F2%2F4%2F305.

[17] R. Sotner, N. Herencsar, V. Kledrowetz, A. Kartci, and J. Jerabek, "New Low-Voltage CMOS Differential Difference Amplifier (DDA) and an Application Example", in *2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2018, pp. 133–136. DOI: 10.1109/MWSCAS.2018.8623866.

[18] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation, Second Edition*. Wiley-IEEE Press, 2004, ISBN: 047170055X.

[19] K. Koli and K. A. I. Halonen, *CMOS Current Amplifiers: Speed Versus Nonlinearity*, 1st. Springer Publishing Company, Incorporated, 2010, ISBN: 9781441952806.

[20] N. Tadic, "A β-error elimination in the translinear reduction of the "log-antilog" multiplier/divider", vol. 1, Feb. 1999, 525–530 vol.1, ISBN: 0-7803-5276-9. DOI: 10.1109/IMTC.1999.776806.

[21] S. S. Rajput, P. Vajpayee, and G. K. Sharma, "1V high performance current mirror for low voltage analog and mixed signal applications in submicron regime", in *TENCON 2009 - 2009 IEEE Region 10 Conference*, Jan. 2009, pp. 1–4. DOI: 10.1109/TENCON.2009.5396113.