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UAPDIFF machine: upgrade and improvement for functional tests on residual current circuit breakers

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Abstract

The UAPDIFF is a machine located in the smart buildings and electrification laboratories of ABB S.P.A (Vittuone). The purpose of this machine is the automation of tests on the tripping current and tripping times of residual current circuit breakers. These tests are currently carried out by hand by operators, as the machine has limitations and malfunctions, it also has no documentation, no operating instructions, and the manufacturer is now bankrupt.

The presented thesis is a continuation of another one, more focused on explaining the functions, the hardware and software structure and the operating state of the machine. This work, instead, involves improving some of the machine's functions, such as generating clearer and more readable reports at the end of the tests, and correcting, as far as possible, the malfunctions of one component of the machine, the linear amplifier (DANA). The previous work had in fact shown how some of the tests were falsified by anomalies generated by the amplifier: unwanted peaks and offsets.

The thesis begins with an overview of how residual current circuit breakers work and what standards govern the tests performed by the machine, a description of how the machine is constituted at the hardware and software level, and finally some information on how the tests are currently carried out in the laboratory. It will later continue with a description of the first real task of this thesis, which is to improve the current report generation, and then conclude with the work done to eliminate the unwanted peak generated by the amplifier, by using contactors and FPGA.

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Chapter 1

1 Background

1.1 Residual current circuit breakers

The earth leakage circuit breaker is a device that performs the function of electrical protection by automatically interrupting the power supply; it is, therefore, an amperometric device that cuts off the power supply when the circuits and electrical appliances on the line present an earth leakage current. (Claudio Amadori, 2008)

The earth leakage circuit breaker protects against direct and indirect contact live parts and contributes to fire prevention.

Let us consider for simplicity a single-phase line, as shown in the following figure, where I_L represents the current flowing in the phase conductor, while I_N represents the current flowing in the neutral. In normal operation, due to Kirchoff's first principle,

 $I_L = I_N$, however, in the presence of a fault, $I_L \neq I_N$, a differential current I_Δ (either fault or earth fault): $I_\Delta = I_L - I_N$ is created.

This fault current can flow to earth not only via the earthtermination system (PE), but also via any other pathway that represents a 'de facto earth' such as the body of a person getting electrocuted.

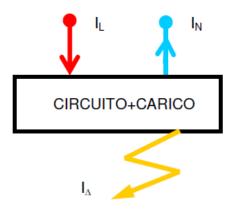


Figure 1:simple basic functional diagram of earth leakage circuit breakers (Claudio Amadori, 2008)

Therefore, irrespective of the number of phases, the main function of the residual current circuit breaker is to carry out, at any time, a vector sum of the currents flowing in the active conductors of the line; if this sum is zero or remains below a certain threshold, the circuit breaker continues to supply the load, otherwise it suspends the supply. It is important to note that there will always be a small physiological leakage current to earth, even in the absence of a fault, which must be tolerated, to avoid the risk of a trip in the absence of a fault or danger (untimely tripping), which could lead to inconvenience and not insignificant risks.

In conclusion, there are three main functions of the earth leakage circuit breaker:

- The *detection* of leakage current.
- The *evaluation* of it against predetermined values (in terms of both intensity and duration).
- If necessary, the *interruption* of the power supply. (Claudio Amadori, 2008)

1.1.1 Operating principle

Considering a two-pole residual current circuit breaker, its operating scheme can be represented as follows:

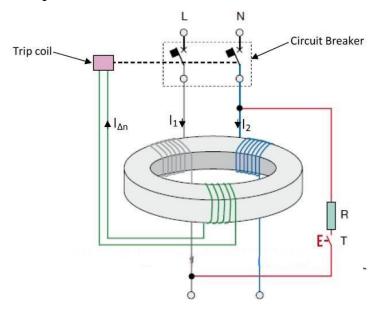


Figure 2:schematic diagram of the operating system and components of the earth leakage circuit breaker

A residual current circuit breaker (RCCB) consists of three constituent blocks:

- The toroidal transformer;
- The tripping actuator;
- The opening mechanism;

The current sensor is usually a transformer consisting of a toroidal core made of magnetic material, a primary winding, and a secondary winding. (Claudio Amadori, 2008)

The primary winding consists of several windings, created by winding the line conductors onto the core. In the absence of a fault, the vector sum

of the currents in the conductors is zero and the corresponding contributions to the magnetic flux in the toroid cancel each other out. Conversely, in the presence of a fault, the magnetic flux generated corresponds to the vector sum of the currents in each conductor and induces a voltage on the secondary winding. Consequently, the current flowing at the primary winding is simply the fault current to Earth I_{Δ} and it is this which, depending on what values it assumes, must make open or not the switch. The switch actuator is usually represented by polarized demagnetization relays since the latter does not need a lot of power to operate and therefore can be powered by the simple fault current.

1.1.2 Classification

Residual current circuit breakers can be classified according to several parameters:

- <u>The tripping sensitivity</u>

The tripping sensitivity is the nominal current of intervention $(I_{\Delta n})$, that is the minimum current beyond which the differential switch must intervene, respecting the times established by the standards.

Switches are therefore divided into:

- High sensitivity: 6 mA, 10 mA, 30 mA, the last two are the most used.
- Low sensitivity: 100 mA, 300 mA, 500 mA, 1 A, 2 A
- <u>The tripping time and selectivity</u>

The rules define not only the time limit within which to intervene for the sake of safety, but also the maximum time within which not to intervene, therefore delays (no intervention time), to ensure the continuity of the power supply. Based on this delay the switches are divided into:

- Generic (or not delayed): are the only ones who do not have upper limits, that is, they must not respect a delay before intervening.
- **Selective** (or type S) The Austrian standard also provides:
- Slightly delayed type G, as subtype of generics

- **M-retarded** (only as pure differential).

We can then represent this last classification graphically as follows:

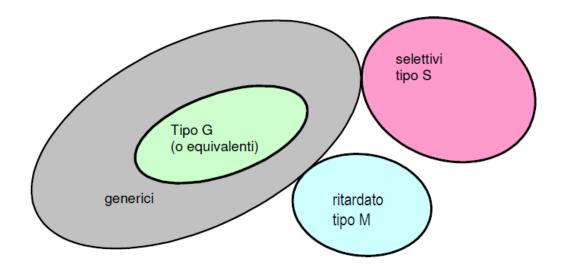


Figure 3:division of switches on the basis of tripping delays (Claudio Amadori, 2008)

- The waveform of the fault current

The earth leakage circuit breakers covered by the standards are designed for use on 50Hz or 60Hz sinusoidal alternating voltage networks, however, the earth leakage current may not necessarily be sinusoidal alternating, as there may be the presence of non-linear semiconductor electronics, this gives rise to the need for differential circuit breakers that are also sensitive to different waveforms.

The earth leakage circuit breakers can be classified into:

- AC: open the circuit only for alternating differential currents sinusoidal currents applied suddenly or slowly increasing.
- A: open the circuit for the same currents as the AC type, for unidirectional pulsating differential currents with or without

phase angle control, and for unidirectional pulsating differential currents superimposed on a continuous current without ripple of 6 mA, in all these cases independent of polarity, applied suddenly or slowly increasing.

The following figure shows all possible angles of delay at which partial fault currents are generated according to the Reference Standards.

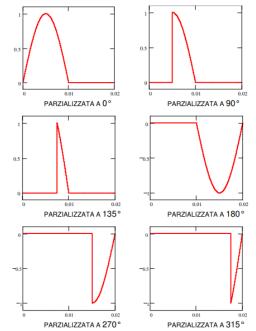


Figure 4: six possible delay angles provided by CEI EN 61008 for unidirectional pulsating waves of the tests prescribed for type A differential switches (Claudio Amadori, 2008)

- F: open the circuit for the same currents as the A type, for differential currents comprising multi-frequency components generated by variable frequency drives, for one-way pulsating differential currents superimposed on a continuous current without ripples of 10 mA, in all these cases independent of polarity, applied suddenly or slowly increasing.
- **B**: open the circuit for the same currents as the F type, and furthermore for sinusoidal alternating differential currents up to 1000 Hz, for sinusoidal alternating differential currents superimposed on a direct current without ripples of 0.4 times

the rated differential current $(I_{\Delta n})$ or 10 mA whichever is higher, for unidirectional pulsating differential currents superimposed on a direct current without ripples of 0.4 times the rated differential current $(I_{\Delta n})$ or 10 mA whichever is higher, for unidirectionally rectified pulsating differential currents resulting from two or more phases, for continuous differential currents without ripple, in all these cases independent of polarity, applied suddenly or slowly increasing.

We can then represent this last classification graphically as follows:

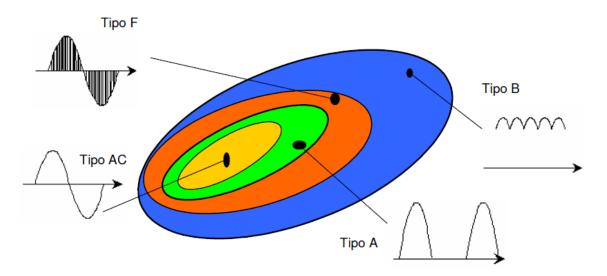


Figure 5: Graphical representation of the classification based on the waveform of the fault current. (Claudio Amadori, 2008)

There are still two other important classifications for differential switches, first, they can be distinguished into:

- Voltage-dependent (VD): which uses the energy from the electricity grid on which they are mounted.

- Voltage-independent (VI): which uses only the fault energy provided by the differential sensor itself to operate the release mechanism.

Finally, the earth leakage circuit breakers are divided into:

- **RCBO:** They perform the function of either an earth leakage circuit breakers or a magnetothermic switch, where the latter is defined as a device to protect against overcurrents, overloads or short circuits.
- **RCCB:** They are not equipped with magnetothermic protection and intervene only in case of failure with dispersion of differential current towards the ground.

1.1.3 Standards

Standards play a very important role in all areas, and here we will look into the standards applied to electrical installations.

Standards are a collection of rules to define the object of interest in accordance with the states of art.

The standards also have, however, a deeper meaning, as they guarantee the safety of those who use the product.

The reference bodies responsible for developing standards are:

- The IEC, International Electrotechnical Commission for International Standards;
- **CENELEC**, Comité Européen de Normalisation Electrotechnique for European standards;
- The **CEI**, Italian Electrotechnical Committee for national standards.

Therefore, the purpose of the standards is to establish the minimum construction requirements that must be met for safety, as well as the electromechanical characteristics, nominal values, prescriptions and specific function tests for each type of differential, whether individual or routine.

The Publication IEC/TR 60755, General requirements for residual current operated protective devices, defines the basic characteristics of all

residual current operated devices, and is the reference for all the numerous IEC, CENELEC and IEC product standards for such devices.

In particular, since the devices of interest here are earth leakage circuit breakers (for domestic and similar use up to 400 V and 125 A), the standards of greatest interest are as follows:

- CEI EN 61008, for the pure A and AC type switches.
- CEI EN 61009, for the A-type and AC thermal-magnetic circuit breakers.
- CEI EN 62423, for the F and B type switches.

However, only the CEI EN 61008 standard will be dealt with in more detail here, as it is the reference standard for all earth leakage circuit breakers that were tested during the UAPDIFF study.

1.1.3.1 CEI EN 61008 Standard

CEI EN 61008 applies to earth leakage circuit breakers with voltagedependent or voltage-independent operation, type A and AC, without built-in overcurrent protection (RCCB), for rated voltages not exceeding 440 V alternating current - at rated frequencies of 50 Hz, 60 Hz and 50/60 Hz - and rated currents not exceeding 125 A. (Residual current operated circuit-breakers without integral overcurrent protection for household and similar uses (RCCBs))

Before going into the details of the standard, it is important to give an overview of the electrical quantities involved in the test instructions:

- The rated differential tripping current $(I_{\Delta n})$, which, as anticipated before, is the minimum current beyond which the differential switch must intervene, respecting the times established by the standards.
- The rated differential non-strike current $(I_{\Delta no})$, which is the maximum value of the differential current below which the circuit breaker must not trip. The standard stipulates its value to be 0.5 $I_{\Delta n}$.
- The nominal current (I_n) , which is a current value assigned by the manufacturer which corresponds to the current value

of the main circuit which the circuit-breaker can conduct under predetermined continuous service conditions. The Standard establishes the values 10-13-16-20-25-32-40-63-80-100-125 A for this parameter.

- **The number of poles**, based on this parameter, switches are subdivided into two-pole, three-pole or four-pole.
- The nominal operating voltage U_e , is the value of the nominal voltage assigned by the manufacturer to which the performance of the device is referred.
- The nominal frequency, referring to the mains voltage.

The standard tells us in detail how to test these two parameters, which parameters to use, which waves, the test conditions, etc.

Various tests are listed and described within the standard itself, but the tests carried out by UAPDIFF are those listed in Chapter 9.9, dedicated to the verification of the intervention characteristic.

The tripping characteristics are represented by the **tripping current** and the **tripping time**, these are, therefore, the two parameters we are going to test, also, regarding times, in the case of S-type switches, we also check the non-tripping times.

More precisely, the **maximum duration of a residual current circuit breaker** is defined as the maximum duration of the time interval between the instant in which the fault current flows through the toroid and the instant in which it is completely extinguished at all poles of the circuit breaker.

On the other hand, the **minimum non-trip duration** is defined as the minimum guaranteed delay for which the circuit breaker does not trip when its toroid is traversed by a fault differential current greater than the non-trip differential current (Pennati).

As mentioned above, the standard also contains general descriptions of the conditions under which tests must be carried out, in fact, the standard prescribes that the residual current circuit breaker under test be kept in the closed position and installed as for normal use at the reference temperature of 20 ± 5 °C with a maximum relative humidity of 50 % at 40 °C, at an altitude of not more than 2000 m, according to the circuit

diagram shown in the following figure. However, in practice, ad hoc apparatuses are used for tests such as Hytron, which will be discussed in the next chapter.

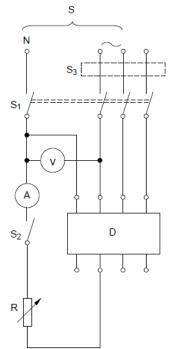


Figure 6:circuit diagram for the intervention characteristics verification tests. The test switch is designated with D, V and A being a voltmeter and an ammeter respectively. Switches S1, S2 and S3 refer to all poles, a single pole, and all but one phase, respectively. R is a variable resistor (Residual current operated circuit-breakers without integral overcurrent protection for household and similar uses (RCCBs))

In addition, all tests are carried out on a random pole and the test is repeated five times.

The first step is to measure the switching current of the switch under test: with the switches S1, S2 and S3 closed, a sinusoidal differential current shall be fed to the switch in the closed position, starting from a value not exceeding $0,2I_{\Delta n}$, increases steadily to the value of $I_{\Delta n}$ over a period of 30 s.

To pass the test, five measurements shall be all between $I_{\Delta no}$ and $I_{\Delta n}$. Then the next tests are the ones of a general nature of verification of the intervention time according to two modalities:

- Close-Open mode (CO): these tests are tests on failure, so starting with the switch open, a sinusoidal current equal to the sensitivity of the device is passed, then the switch is closed and it is measured how long it takes to reopen. The values to be respected are those shown in Table 1.
- Open mode (O): foresees to measure the switching time when the switch is closed, with S2 closed, suddenly administering a fault sinusoidal current by closing S1, whose amplitude values are calibrated according to Table 1. In this mode the correct operation of the switches is verified even in case of sudden appearance of high currents, randomly choosing an amplitude for the fault current a value between the following: 5 A, 10 A, 20 A, 50 A, 100 A, 200 A.

There are other types of additional tests for type A and higher switches, in which the current administered is not a pure sine wave but a onedimensional pulsed fault current with six possible delay angles, as shown above (figure 6).

The tests are performed with reference to the circuit diagram in the following figure, with all the switches in the closed position:

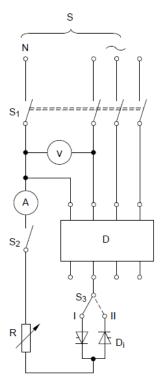


Figure 7:circuit diagram to verify the correct operation of RCCB switches in case of unidirectional pulsed fault current. S3 is a bidirectional switch connected to the thyristor Di, which together with the variable resistance is responsible for generating the desired waveform by changing the delay angle α (Residual current operated circuit-breakers without integral overcurrent protection for household and similar uses (RCCBs)).

For the limits of the intervention current values in this case, table 3 is used. The switch under test will be tested with each of the partialized waves shown in Figure 7, but this time only two measurements are taken for each test. Again, the current amplitude increases linearly within the ranges specified in Table 3, within 30 s.

Regarding the intervention currents, the Standard provides that the differential intervention current is also measured in the presence of partial fault currents at 0 and 180. Refer to Table 3 for limits of validity.

As for the intervention times, on the other hand, for type A switches, two measurements of the intervention time are made at the sudden application of a pulse current unidirectional at a delay angle equal to 0, the possible amplitudes of which are specified in Table 2, which also shows the limits for intervention time. The Standard reports the time/current characteristics in tabular form, depending on the type of switch, in particular, three tables are used:

Table 1:Limit values of break time and non-actuating time for alternating residual (Residual current operated circuit-breakers without integral overcurrent protection for household and similar uses (RCCBs))

			Limit values of break time and non-actuating time (s) for type AC and A RCCB in event of alternating residual currents (r.m.s. values) equal to						
Туре	I _n A	I _{∆n} A	I∆n	2 / _{4n}	5 <i>I</i> ∆n	5 I _{∆n} or 0,25 Aª	5 A - 200 A ^b	500 A	
		< 0,03	0,3	0,15		0,04	0,04	0,04	
General	Any	0,03	0,3	0,15		0,04	0,04	0,04	Maximum break times
		> 0,03	0,3	0,15	0,04		0,04	0,04	
		> 0,03	0,5	0,2	0, 1 5		0,15	0,15	
S	≥ 25	> 0,03	0,13	0,06	0,05		0,04	0,04	Minimum non- actuating times
a Value to be decided by the manufacturer for this test.									
^b The tests are only made during the verification of the correct operation as mentioned in 9.9.2.4.									

Table 2:Maximum values of break time for half-wave pulsating residual currents (Residual current operated circuit-breakers without integral overcurrent protection for household and similar uses (RCCBs))

			Maximum values of break time(s) for type A RCCB in event of half-wave pulsating residual currents (rms values) equal to							
Туре	I _n A	I _{∆n} A	1,4 <i>I</i> ∆n	2 / _{4n}	2,8 <i>I</i> ∆n	4 <i>I</i> ∆n	7 I _{∆n}	0,35 A	0,5 A	350 A
		< 0,03		0,3		0,15			0,04	0,04
General	Any	0,03	0,3		0,15			0,04		0,04
		> 0,03	0,3		0,15		0,04			0,04
S	≥ 25	> 0,03	0,5		0,2		0,15			0,15

Table 3:Switching current ranges for Type A differential switches (Residual current operated circuit-breakers without integral overcurrent protection for household and similar uses (RCCBs))

Angolo, α	Corrente d'intervento A					
0	Limite inferiore $I_{\Delta n}$	Limite superiore $I_{\Delta n}$				
0	0,35	J				
90	0,25	1,4 o 2 (5.3.12)				
135	0,11)				

Since the RCCBs are **safeguard devices** and they preserve human life, they need to be fully functioning when used by the customers.

It is crucial, then, to **respect** the numerous requirements before releasing a new residual current circuit breaker onto the market.

Chapter 2

2 State of the art UAPDIFF machine and previous work

As introduce before, this thesis is the continuation of another thesis, focused on the study of the machine's composition at both hardware and software level, drawing up an analysis of all the machine's limitations and problems, and concluding with an initial approach to troubleshooting the machine.

Both my work and the previous one have been conducted in the almost total absence of documentation of every type, including electrical diagrams or workflow of the logic that regulates the behaviour of the machine itself: the only document received was in fact a guide to the use of the graphical interface for the test setup, therefore in both cases it was almost a reverse engineering work.

As mentioned before, UPADIFF is a machine designed to automate the tests listed above, which are currently carried out by hand operators.

2.1 Hardware description of UAPDIFF

The following figure shows the UAPDIFF machine that can be divided into 4 functional building blocks.



Figure 8: UAPDIFF machine (Di Pippo)

- **Block 1**: consists of a rack containing all the instruments used for measuring, acquiring and processing test signals, together with those for supplying the supply voltage to the devices under test.
- **Block 2**: includes the three stations where the residual current circuit breakers are housed and tested, the mechanical arms responsible for resetting and closing the switches, and the solenoid valves below which in turn determine the movement of the mechanical arms.
- **Block 3**: constitutes the communication part between block 1 and block 2: it contains terminal blocks that articulate the I/O communication signals coming from area 1 and convey them through a relay system to the test stations above, making the operating controls of the mechanical arms and the delivery of test currents and continuity; each relay corresponds to a virtual channel in the software and a physical channel on the I/O interface.

- **Block 4**: represents the user interface with the machine and peripherals associated with the PC.

Then disassembling the rack, to make a more in-depth analysis, one can see the presence of other elements such as:

- NI PXI 1033, a chassis manufactured by National Instruments for remote control applications. In two of the six available slots, it houses respectively a reconfigurable multifunction I/O module (NI PXI-7841) containing a LabViewprogrammable FPGA (slot 2), and a 32-channel digital I/O module (NI PXI-6514, slot 6), the latter being used for communication with test stations.
- A relay connecting the emergency reset button to the TTL port of the Chroma.
- A high voltage differential probe.
- An AC/DC converter and a voltage stabilizer (Siemens SITOP 6EP1333-3BA00) providing 24 V DC voltage from the 230 V AC supplied by the Chroma.
- A current transducer (Seneca T201 DCH) that receives the output current of the linear amplifier as input and translates it into a voltage signal.
- A 68-pin terminal board (NI CB-68LPR) for connecting signals to the DAQ associated with the FPGA and for direct communication between the latter and certain peripherals.
- A terminal board for connecting all the above-mentioned parts.

The following picture shows a block diagram illustrating the machine components and the communication interfaces between them. We note that the interfaces described are the results of a reverse engineering process, as the machine documentation was not available.

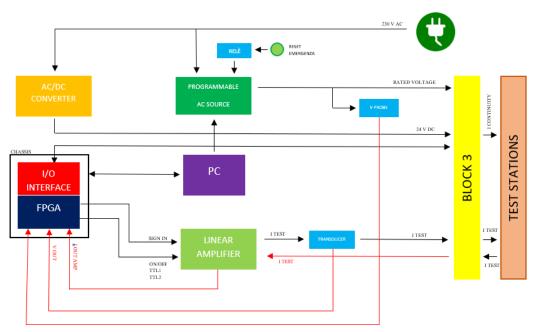


Figure 9: Principle diagram of the internal connections of block 2 and the connection between it and the other two blocks. Non-established connections are shown in red. (Di Pippo)

The relevant component here is the FPGA; it communicates both with the linear amplifier, via port D15, supplying the signal to be amplified as input, and, probably, with the differential voltage probe, although this connection has not been ascertained.

2.2 Software description of UAPDIFF

The operation of the UAPDIFF is regulated by an application written in the labVIEW development environment, consisting of an executable called ABB-Main and hundreds of VI and subVI associated with it.

In the following figure, the machine's VI hierarchy is depicted to give an idea of the vastness of the machine's logic.

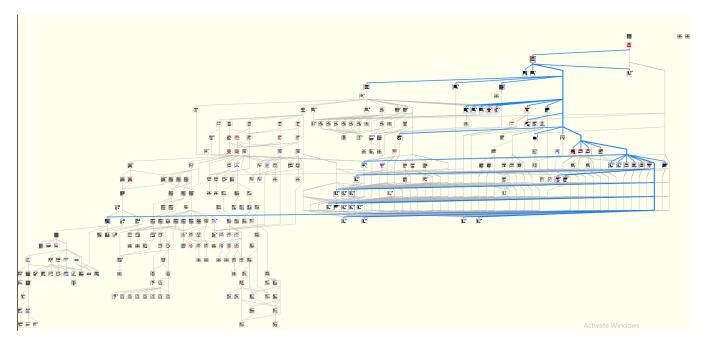


Figure 10: Overall hierarchy of VI of UAPDIFF

Given the breadth of the programme, only the VIs most important for this thesis work will be described.

When the executable is started, an initial dialogue tab opens, called UUTDataDialog.vi, where you are asked to enter the data of the unit under test (UUT), such as:

- Rated current I_n
- Type
- Rated voltage U_n
- Pole number
- Sensitivity $I_{\Delta n}$
- Frequency
- PS frequency

Then we can also choose whether the switch is of the RCCB/RCBO type, if it is type S, whether to use the $1.1 * U_n$ or $0.85 * U_n$ mains voltage, whether to use the Australian and New Zealand standard (AS/NZS), and

finally we have the fault management, i.e. in case of test failure, currently disabled.

Type S Rated Current In Type		ensitivity Idn Frequency		
ý) 40 A ý) A	(f) 230 V (f) 2 (f)	30 mA 🕤 50 Hz	50 Hz	0
lormative Tests	Tables	N	Colored N	
Test Type	Test Name	Noramtive Paragraph	Selected Num	1,1 Un 0,85 Un
CORRENTE DI INTERVENTO	Rampa 30 mA AC 230 V 50 Hz	CEI EN 61008-1.9.9.2.1	NO	0 0
CHIUSURA SU GUASTO	Tempi CO 30 mA AC 230 V 50 Hz	CEI EN 61008-1.9.9.2.2	NO	
TEMPO DI INTERVENTO	Tempi O 30 mA AC 230 V 50 Hz	CEI EN 61008-1.9.9.2.3	NO	AS/NZS
TEMPO DI INTERVENTO	Tempi O 60 mA AC 230 V 50 Hz	CEI EN 61008-1.9.9.2.3	NO	
TEMPO DI INTERVENTO	Tempi O 150 mA AC 230 V 50 Hz	CEI EN 61008-1.9.9.2.4	NO	
CORRENTE DI INTERVENTO	Rampa 42 mA parzializzata 0° 230 V 50 I		NO	
CORRENTE DI INTERVENTO	Rampa 42 mA parzializzata 90° 230 V 50		NO	Continuity Test
CORRENTE DI INTERVENTO	Rampa 42 mA parzializzata 135° 230 V 5		NO	Failure Reaction
CORRENTE DI INTERVENTO	Rampa 42 mA parzializzata 180° 230 V 5		NO	CD FAULUDE
CORRENTE DI INTERVENTO	Rampa 42 mA parzializzata 270° 230 V 5	CEI EN 61008-1.9.21.1.1	NO	CB FAILURE
CORRENTE DI INTERVENTO	Rampa 42 mA parzializzata 315° 230 V 5	CEI EN 61008-1.9.21.1.1	NO	() NONE
CORRENTE DI INTERVENTO	Rampa 42 mA parzializzata 0° + offset	CEI EN 61008-1.9.21.1.4	NO	
CORRENTE DI INTERVENTO	Rampa 42 mA parzializzata 0° + offset	CEI EN 61008-1.9.21.1.4	NO	TEST FAILURE
CORRENTE DI INTERVENTO	Rampa 42 mA parzializzata 180° + offse	CEI EN 61008-1.9.21.1.4	NO	() NONE
CORRENTE DI INTERVENTO	Rampa 42 mA parzializzata 180° + offse	CEI EN 61008-1.9.21.1.4	NO	() NOTICE
TEMPO DI INTERVENTO	Tempi O 84 mA parzializzata 0° 230 V 50	CEI EN 61008-1.9.21.1.2	NO	
TEMPO DI INTERVENTO	Tempi O 84 mA parzializzata 180° 230 V	CEI EN 61008-1.9.21.1.2	NO	Select All
TEMPO DI INTERVENTO	Tempi O 42 mA parzializzata 0° 230 V 50	CEI EN 61008-1.9.21.1.2	NO	Deselect All
TEMPO DI INTERVENTO	Tempi O 42 mA parzializzata 180° 230 V	CEI EN 61008-1.9.21.1.2	NO	Descreter All
TEMPO DI INTERVENTO	Tempi O 350 mA parzializzata 0° 230 V 5	CEI EN 61008-1.9.21.1.2	NO	
TEMPO DI INTERVENTO	Tempi O 350 mA parzializzata 180° 230		NO	
			_	
	6			
			2 5	
				Next
		5 -	2 2 2	
				💥 Cancel

Figure 11: UUTDataDialog.vi's front panel

At this point, by opening the main screen, is possible to manage the machine through the buttons "run-stop-pause-step-clear" and is possible to follow the main steps running through a log window.

Through this interface is also possible to choose the name to be given to the generated report at the end of the test, the names of the UUT, which are subject to the test, and choose the number of cycles to which to submit the differentials. At this point, the test begins by carrying out a continuity test before and after the current supply, where we check whether the switch was correctly armed before the test and whether it actually opened after the test. During the test we can watch the waveform generated by the screen shown in the following figure and, from the log screen, we can already appreciate the tripping current/tripping time measurements, however, to get a true analysis of the test we will need to open the generated report.

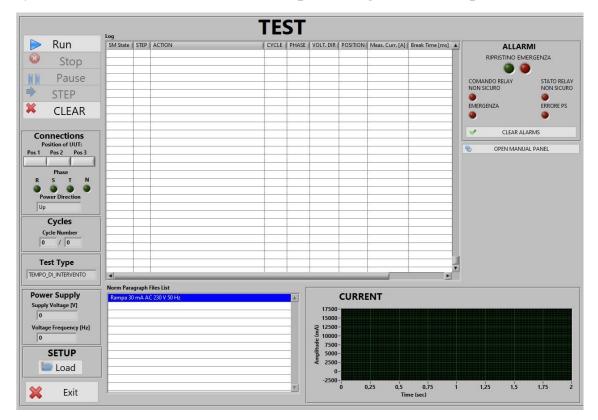


Figure 12: ABB_main.vi's front panel

As mentioned before, the logical structure of the UAPDIFF is very complex and only a few VIs will be analysed, such as:

- **ABB_main**: is the most 'general' VI, where within it are all the other VIs with specific functions, it basically handles the screen of the previous image.

Prova_SM: Inside there is a large case structure, where are managed all the five states in which the machine can be found: "Paused", "Running", "Stopped", "Init", "Delnit". The transitions between these states depend on which button we click in the user interface screen shown above, as shown in the following figure.

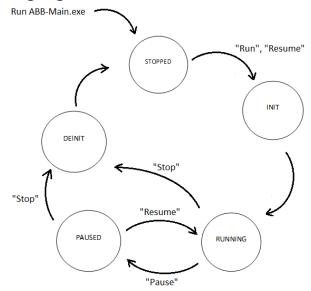


Figure 13: Diagram of machine state transition conditions (Di Pippo)

As shown in the diagram, at the start of the test the machine is in the "Stopped" state, when we click on "Run", we start all the dialogue screens mentioned above where we are asked for information about the type of test, switch, etc...

In the "Init" state, on the other hand, all the variables are initialized with the values obtained previously, and the reports are created and the folders where they are stored, but are not yet compiled.

Finally, in the "Running" state, the actual test is performed.

- **ExecuteStep2:** Here we have a large case structure where the tests are managed, via the following steps:

1) EV_C_on, EV_C_off, EV_A_on, EV_A_off, EV_B_on, EV_D_on, EV_D_ff, EV_B_off.

2)Set_circuit_test_cont,Set_circuit_meas,Set_circuit_PS,

Set_circuit_WF, Set_WF, Set_Power, Set_Current.

3)Start_test_cont_before,Start_test_cont_before,

Start_meas_current,Start_meas_time,Wait_meas_time,

Wait_meas_current.

4) Reset_power, Reset Circuit.

In step one, all commands to the solenoid valves for a particular location are explained so that all mechanical arms are lowered or raised.

In step two, all information provided by the operator to perform the test is set, such as waveform type, limits, frequency values and the supply of current and voltage is enabled.

In step three, the machine communicates with the FPGA to obtain information on the measurements of the generated wave and the values of interest (tripping current or tripping time) and then transcribes them into reports.

In step four, all previously initialized values are reset.

- WriteMeasureRecord: In this VI we construct a string where we write the information of the type of test, i.e. the name of the test and its reference on the standard, the pole we are testing the results of the continuity test, the result and the outcome of the test. In particular, the result is obtained from the interaction with the FPGA.
- WriteMeasureRecordonfile: here, simply the string created by the previous VI is taken and transcribed into the report.

2.3 Previous Activities

After this machine composition analysis, in the previous work the computer's operating system was upgraded from Windows XP to Windows 11 and labVIEW from labVIEW 2013 to labVIEW 2023 Q3.

It was then carried out an initial quality analysis of the tests performed by UAPDIFF, noticing that the machine performed poorly in the tests by reporting values far from those measured by hand.

These results were influenced by either larger or smaller current spikes before or after the test sinusoid and/or a larger current peak at the instant the circuit breaker trips, or current steps just before the test sinusoid.

These problems originated in the poor sizing of the low-pass filter which, being too selective, also distorted the shape of the wave, therefore it was necessary to resize the filter and also to lower the trigger threshold as much as possible so that the interval identified by the algorithm tended towards the true duration of the test signal. In addition to the low-pass filter, a new sub-VI had to be added to remove larger peaks which generally occur at the trigger of the switches, which receive as input the test signal and its nominal amplitude expressed in mA and discriminates all samples whose amplitude is above the nominal amplitude of the sine wave and sets them to zero.

In order to eliminate the presence of the above-mentioned current steps, it was necessary to add another VI, which identifies and resets to zero all signal samples that are simultaneously negative and of modulus not exceeding 200, a value established empirically.

It was also changed the way of selecting tests, which previously involved the use of configuration files external to the application and dependence on paths, whether absolute or relative. Operating, therefore, on UUTDataDialog.vi, the selection of proofs was parameterized, so that the machine would be able to autonomously generate proofs relating to a given model whenever the user enters data relating to it via the interface.

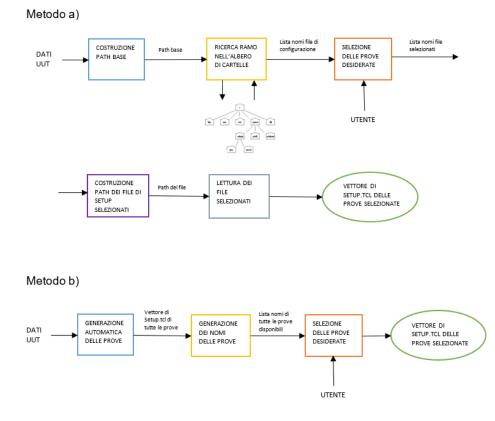


Figure 14:Comparison of the old test selection method (metodo a) and the new one (metodo b) (Di Pippo)

Finally, in order to eliminate the presence of the high amplitude current peaks that caused the switch to trip prematurely, since the origin of these peaks lies in the linear amplifier, the time during which the amplifier remained active was shortened, activating it only when the test actually began. In this way, the peaks still occur, but of a much smaller magnitude, so that they no longer trip the switch.

At the beginning of the thesis, in spite of all the earlier work, the machine still presented the following flaws and limits:

- Anomalies: at the moment, the machine does not manage the case in which the test should fail, that is, in case of failure the machine does nothing, since the management of these cases has been disabled, because once activated the tests are no longer properly executed.

- **Reporting**: the machine produces reports in ".txt" files, unclear and unreadable.
- **Managing amplifier faults:** there are still problems with generating tests for switches A and AC, as the amplifier generates unwanted peaks and offsets that falsify the test.
- Expand the types of tests performed: once the tests on types A and AC have been completed, it is necessary to add all the cases related to types B and F which are not currently taken into account by the machine.
- Add voltage-independent circuit breakers: the machine will always power the UUTs, but as mentioned before there are some independent voltage differential switches, which do not need to be powered and therefore cannot be tested by the UAPDIFF. (Di Pippo)

Chapter 3

3 Manual tests on earth leakage circuit breakers

In order to understand the deep meaning of the discussed tests, I was able to carry out these tests together with experienced operators.

As mentioned before, testing earth leakage circuit breakers is a crucial step because it is important that these devices are flawless when they are put on the market, as they are life-saving devices, so responsible for people's safety.

Tests were carried out on the following bipolar switches:

- F202 A 25A/10mA
- F202 A 40A/30mA

Consider the first switch of those listed above, as the steps to be followed are the same only change.

3.1 Current test

In order to test the tripping currents, the following instrumentation was used:

- Oscilloscope
- Multimeter (Keithley 2001), which is only used as an auxiliary instrument to see the current increase.
- Hytron F1, which is a precision current generator, up until 5 A of current, after this value we need to use another setup.

All of the three devices are put in series.

In order to test the current, it is needed to generate ramps of the duration of 30 seconds, using the Hytron, the minimum and maximum values of these ramps are given from the standards.

The Hytron also allows to generate unidirectional pulsing signals at each of the phase angles required by the standard itself, with or without superimposing a continuous current of 6 mA.

During ramping, the Keithley instantaneously measures the current flowing in the designated pole as it is set to always send the maximum value to the screen: when the switch is triggered, the last value stored by the Keithley is always the maximum, as well as the value of the switch trip current.

The following photo shows a representation of the setup used with all the instruments used:

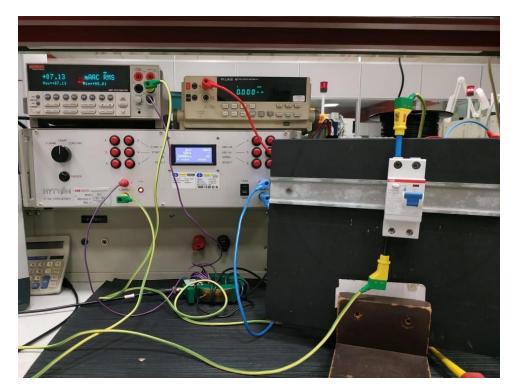


Figure 15:Setup test measuring the tripping current on a differential switch with a sensitivity of 10 mA. Shown are the Keithley 2001 in the top left, the Hytron in the bottom. All instruments are connected in series to the switch under test, which receives the f ault current via pole R. The Hytron is set in AC ramp mode, so that it generates a sine wave of amplitude equal to the sensitivity of the instrument. (Di Pippo)

3.2 Time test

In order to test the timing, the following instruments are used:

- Hytron F1, for "open" type tests.
- Eltec D-Box, for "closed-open" type tests.

The Eltec functions as a current generator of waveforms that can be set between sine, 0° , 90° and 135° positive or negative pulsing, and $0^{\circ} + DC$ pulsing; the operating frequency can also be selected between 50 Hz or 60 Hz. It can be used in both of the previously described tripping current ramp tests as well as in both of the previously described tripping time tests; it can therefore deliver fault current despite the switch being open, unlike the Hytron. Another function of the Eltec is to be able to enter test parameters into preset programs which can then be called up as required by entering the corresponding code.

A pure sinusoidal current of constant amplitude was thus set equal to the sensitivity of the device under test, i.e. in this case 10 mA, the setup of this test is shown in the following picture:

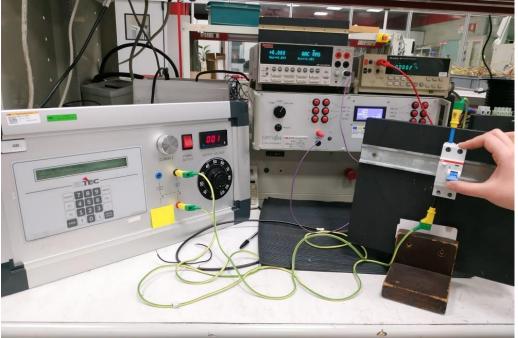


Figure 16:Failure test setup. On the left is visible the Eltec, which generates a sine wave of amplitude equal to the sensitivity of the switch under test, again 10 mA. The switch must be reset while the current flows through the circuit, the tripping time being measured by Eltec itself. Switch and instrument are connected in series. (Di Pippo)

In order to carry out the tests for the sudden administration of a differential fault current prescribed by the standard, the Hytron was set to CONSTANT mode, so as to administer a wave of constant amplitude. Three tests were carried out with pure sinusoidal currents with amplitudes of $I_{\Delta n}$, 2 $I_{\Delta n}$ and 5 $I_{\Delta n}$ respectively, in accordance with Table 1 in the previous chapter. As far as the tests with biases are concerned, the standard prescribes the following amplitude values for a sensitivity of 10 mA: 2 $I_{\Delta n}$, 4 $I_{\Delta n}$, 0.5 A.

The test setup in this case is entirely analogous to that described in the previous section, and reference is made to it.

Chapter 4

4 Reports Generation

For the first half of my thesis, they couldn't be performed any measurement tests, but qualitative tests, since an important element of the machine (the linear amplified) was being repaired. These months were very useful in understanding the operation of the interface and becoming more confident with the machine. The focus was on the problem of test generation and the improvement of the file report.

As mentioned before, the report files generated are .txt files, which are difficult to understand, like the one shown in the next picture.

1									_						
postazione2_202	23_07_04_15_4	4_44 - Notepad												- 0	Х
File Edit Format	View Help														
ID POLO	NORMA	PARAGRAFO	TIPO TEST	TIPO MISURA	MISURA	LIMITE SUP/	CONT PRIMA	LIMITE	INFERIO	RE/CONT	DOPO	TENSIONE DI	ALIMENTAZIONE	ESITO TIMESTA	MP
Rampa 30 mA AC	C 230 V 50) Hz													
postazione2	R	CEI EN 61009-1	9.9.1.2.a	CORRENTE DI	INTERVENTO	CONTINUITA'	PRIMA	SI	SI	NO	230 V	PASSATO	martedì 4 lu	glio 2023 15:44:54	
postazione2	R	CEI EN 61009-1	9.9.1.2.a	CORRENTE DI	INTERVENTO	CORRENTE (m	A) 21,272	2384	30,00	0000	15,000	1000 230	V PASSATO	martedì 4 lugli	0 2023
postazione2	R	CEI EN 61009-1	9.9.1.2.a	CORRENTE DI	INTERVENTO	CONTINUITA'	DOPO	NO	SI	NO	230 V	PASSATO	martedì 4 lu	glio 2023 15:45:22	
postazione2	R	CEI EN 61009-1	9.9.1.2.a	CORRENTE DI	INTERVENTO	CONTINUITA'	PRIMA	SI	SI	NO	230 V	PASSATO	martedì 4 lu	glio 2023 15:45:33	
postazione2	R	CEI EN 61009-1	9.9.1.2.a	CORRENTE DI	INTERVENTO	CORRENTE (m	A) 21,416	5131	30,00	0000	15,000	000 230	V PASSATO	martedì 4 lugli	0 2023
postazione2	R	CEI EN 61009-1	9.9.1.2.a	CORRENTE DI	INTERVENTO	CONTINUITA'	DOPO	NO	SI	NO	230 V	PASSATO	martedì 4 lu	glio 2023 15:46:02	
postazione2	R	CEI EN 61009-1	9.9.1.2.a	CORRENTE DI	INTERVENTO	CONTINUITA'	PRIMA	SI	SI	NO	230 V	PASSATO	martedì 4 lu	glio 2023 15:46:12	
postazione2	R	CEI EN 61009-1	9.9.1.2.a	CORRENTE DI	INTERVENTO	CORRENTE (m	NA) 20,966	5549	30,00	0000	15,000	000 230	V PASSATO	martedì 4 lugli	0 2023
postazione2	R	CEI EN 61009-1	9.9.1.2.a	CORRENTE DI	INTERVENTO	CONTINUITA'	DOPO	NO	SI	NO	230 V	PASSATO	martedì 4 lu	glio 2023 15:46:40	
postazione2	R	CEI EN 61009-1	9.9.1.2.a	CORRENTE DI	INTERVENTO	CONTINUITA'	PRIMA	SI	SI	NO	230 V	PASSATO	martedì 4 lu	glio 2023 15:46:50	
postazione2	R	CEI EN 61009-1	9.9.1.2.a	CORRENTE DI				0603	30,00	0000	15,000	000 230		martedì 4 lugli	0 2023
postazione2	R	CEI EN 61009-1	9.9.1.2.a	CORRENTE DI	INTERVENTO	CONTINUITA'	DOPO	NO	SI	NO	230 V	PASSATO	martedì 4 lu	glio 2023 15:47:19	
Tempi CO 30 m4	A AC 230 V	/ 50 Hz													
ID POLO	NORMA	PARAGRAFO	TIPO TEST	TIPO MISURA	MISURA	LIMITE SUP/	CONT PRIMA	LIMITE	INFERIO	RE/CONT	DOPO	TENSIONE DI	ALIMENTAZIONE	ESITO TIMESTA	MP
postazione2	R	CEI EN 61009-1	9.9.1.2.b	CHIUSURA SU G		TEMPO (ms)	42,925	5000	300,0	00000	1,0000	100 230	V PASSATO	martedì 4 lugli	
postazione2	R	CEI EN 61009-1		CHIUSURA SU G		TEMPO (ms)	36,225		300,0	00000	1,0000			martedì 4 lugli	
postazione2	R	CEI EN 61009-1	9.9.1.2.b	CHIUSURA SU G	UASTO	TEMPO (ms)	27,000		300,0	00000	1,0000	00 230	V PASSATO	martedì 4 lugli	
postazione2	R	CEI EN 61009-1	9.9.1.2.b	CHIUSURA SU G	UASTO	TEMPO (ms)	39,429	5000	300,0	80000	1,0000	00 230	V PASSATO	martedì 4 lugli	0 2023
Tempi O 30 mA															
ID POLO	Norma	PARAGRAFO	TIPO TEST	TIPO MISURA	MISURA	LIMITE SUP/	CONT PRIMA	LIMITE	INFERIO	RE/CONT	DOPO	TENSIONE DI	ALIMENTAZIONE	ESITO TIMESTA	MP
postazione2	R	CEI EN 61009-1	9.9.1.2.c	TEMPO DI INTE		CONTINUITA'	PRIMA	SI	SI	NO	230 V	PASSATO		glio 2023 15:48:26	
postazione2	R	CEI EN 61009-1		TEMPO DI INTE		TEMPO (ms)	30,750		300,0		1,0000			martedì 4 lugli	0 2023
postazione2	R	CEI EN 61009-1		TEMPO DI INTE		CONTINUITA'		NO	SI	NO	230 V	PASSATO		glio 2023 15:48:33	
postazione2	R	CEI EN 61009-1		TEMPO DI INTE		CONTINUITA'		SI	SI	NO	230 V	PASSATO		glio 2023 15:48:44	
postazione2	R	CEI EN 61009-1		TEMPO DI INTE		TEMPO (ms)	30,800		300,0		1,0000			martedì 4 lugli	0 202:
postazione2	R	CEI EN 61009-1		TEMPO DI INTE		CONTINUITA'		NO	SI	NO	230 V	PASSATO		glio 2023 15:48:51	
postazione2	R	CEI EN 61009-1		TEMPO DI INTE		CONTINUITA'		SI	SI	NO	230 V	PASSATO		glio 2023 15:49:02	
postazione2	R	CEI EN 61009-1		TEMPO DI INTE		TEMPO (ms)	30,775		300,0		1,0000			martedì 4 lugli	0 2023
postazione2	R	CEI EN 61009-1		TEMPO DI INTE		CONTINUITA'		NO	SI	NO	230 V	PASSATO		glio 2023 15:49:09	
postazione2	R	CEI EN 61009-1		TEMPO DI INTE		CONTINUITA'		SI	SI	NO	230 V	PASSATO		glio 2023 15:49:20	
postazione2	R	CEI EN 61009-1		TEMPO DI INTE		TEMPO (ms)	30,750		300,0		1,0000			martedì 4 lugli	0 2023
postazione2	R	CEI EN 61009-1	9.9.1.2.c	TEMPO DI INTE	RVENTO	CONTINUITA'	DOPO	NO	SI	NO	230 V	PASSATO	martedì 4 lu	glio 2023 15:49:27	
1															

Figure 17: report initially generated by the machine.

As can be seen from the picture, the information is not provided in a proper table, in fact it is not well aligned and makes it difficult to read the report, furthermore the .txt format is not a useful format for the company. Instead, the goal was a file of the following type:

4	А	в	С	D	E	F	G	н	1	J	к	L
	Date:		20/07/2023				-			_		_
2	Name Opera	ator:	Maria									
3												
1												
5	Rampa 30 m	A AC 230	V 50 Hz	CEI EN 61	009-1	9.9.1.2.a	R	21.272.384	21.416.131	20.966.549	21.500.603	
5	Tempi CO 3	0 mA AC 2	230 V 50 Hz	CEI EN 61	009-1	9.9.1.2.b	R	42.925.000	36.225.000	27.000	39.425.000	
7	Tempi CO 3	0 mA AC 2	230 V 50 Hz	CEI EN 61	009-1	9.9.1.2.c	R	30.750.000	30.800.000	30.775.000	3.075.000	
3												
9												
0												
1												
2												
3												
4												
5												
6												
7												
8												
9												
20												
21												
22 23												
23 24	-											
24 25												
26 26												
27												
28	-											
29	-											
30	-											
31	-											
32												
33												
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36												
37												
8												
9												
10												
1												
2												
2		_										

Figure 18: final report we wish to obtain

The goal was to create a report in Excel format, composed of three pages, one for each UUT. In fact:

- Page number 1: reports the information and results about the first unit under test, therefore the name of this page is the same name given by the user to the UUT in the interface shown in fig.22
- Page number 2: reports the information and results about the second unit under test, therefore the name of this page is the same name given by the user to the UUT in the interface shown in fig.22
- Page number 3: reports the information and results about the third unit under test, therefore the name of this page is the

same name given by the user to the UUT in the interface shown in fig.22

Each page then had to have the same layout, i.e. the date and the name of the operator at the top left and after that the actual table with the names of the tests, exactly as they appear when you select them from the user interface, the chapter and paragraph references on the standards, the name of the pole being are tested and finally the measured result (there will be as many results as the number of cycles selected).

As shown earlier by the VI hierarchy, the UAPDIFF has a very broad and complex logic where it is impossible to expound it in its entirety. It is therefore necessary to identify only the VIs that are useful for this cause and understand how they fit in with the rest of the logic.

The real difficulty in this part is in fact managing to modify a certain part of the code, without disrupting the entire logic, and thus managing not to generate a cascade effect whereby we have to modify all the VIs.

4.1 Initial phase

The software with which the machine is built, labVIEW, has a purposebuilt library for generating reports in Word, Excel and HTLM.

Consequently, the initial phase of the approach was focused on working on machine-independent VIs to familiarise with this library and to try to obtain files as close as possible to those wanted (fig. 18).

After several iterations, it was created a VI called **'Report_Generetion_2'**, shown in the next figure:

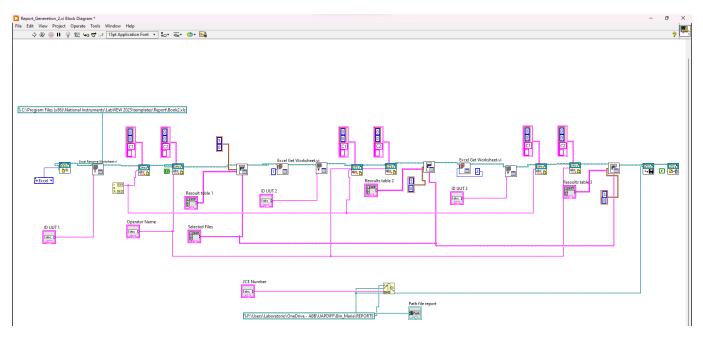


Figure 19: LabVIEW block diagram of Report_Generation_2

As can be seen from the previous picture, in this VI there are fields that will then be filled in by the user, which are:

- **ID UUT1, ID UUT2, ID UUT3,** which represent the names to be given to the tested devices and which will name the three excel sheets.

- Operator Name

- **2CE Number**, which is the name to be given to the report.

In particular, on the left side of the VI a report is created in an excel file, using a template specifically made for this purpose, called **"Book2"**, then the next blocks will be repeated twice more as the three sheets must have the same layout:

- a sheet is created with the name given by the user
- the date on which the test is carried out is entered
- the name of the operator is entered

- finally, a table called "Results table" is inserted, the first column contains the list of selected tests obtained from "Selected Files", the

second column represents the reference of the selected test on the standards, the third column represents the pole under test and finally, the last column represents the actual results of the test, obtained from the calculations performed by the machine.

Finally, the report is saved under the name given by the user and is saved in the 'REPORTS' folder and the file is then closed.

This VI generates a report of the following type:

AutoSave 🔟 🗄		- ∓ Repo	rt 20092023 - C	ompatibility Mc	ode 🗸																Lab Vittu	one 🐽	(ii	- 0	
e Home Insert																							Comme		Share
Gut ↓ Cut Garage Copy → aste ♂ Format Painter	Calibri B I L		⊸ A* A* <u>∧</u>	===		🐉 Wrap Text	Center ~	General		Conditiona Formatting	I Format as	Normal Neutral	B	ad alculation	Good	k Cell		ert Delete	Format	∑ AutoSum III ~	1 ° Â∑√ Sort& Filter •	Find 82	Analyze Data		
Clipboard 5					Alignm	ent		Numbe		- Connaccing	- 18L/IC -		Styles					Cells			Editing		Analysis		
▼ : × ✓																									
A B		D	E F	G	н		1	K L	м	N	0	Р	Q	R	S	т	U	v	w	×	Y	z	AA	AB	A
ata:	20/09/2023																								
lome operatore:	Maria																								
mps 30 mAAC 230 V 50 I mpl 0 30 mAAC 230 V 50																									
mpi O 30 mA AC 230 V 50 mpa 42 mA parzializzata																									
ringes viz min per crellizzete	C C21 EN 0100		1.0071104																						
																					Activat				
																					Go to Set	ings to ac	tivate Wir	ndows.	
> Posizion	Posizic	one2 Posi	zione3																_						

Figure 20: Report generated by Report_Generation_2

4.2 Integration into the UAPDIFF code

Consequently, it was needed to identify all the VIs of greatest interest for this purpose, which are as follows:

- WriteMeausureRecord
- WriteMeausureRecordOnFile
- ProvaSM

- ExecutionStep2

At this point, the user interface, called "TestParamsDialog" was edited, updating the name to be given to the report and adding the "operator name" field, the changes are reported in the following pictures:

LSP	Position of UUT:		Norm Paragraph Files List (Single Cycle Number)	
Pos 1	Pos 2	Pos 3	Rampa 30 mA AC 230 V 50 Hz	0
Pos 1 ID	Pos 2 ID	Pos 3 ID		
· · · · · · · · · · · · · · · · · · ·				-
				_
	Phase			
	R S T N			
		Current		
	R S T N			
		Voltage		_
	Power Direction			
	() Up			_
	NEXT 🗱 EX	т	All Cycle Number	

Figure 21: Initial interface

2CE Number	Operator Name	
	Position of UUT:	Norm Paragraph Files List (Single Cycle Number)
Pos 1	Pos 2 Pos 3	Rampa 30 mA AC 230 V 50 Hz 0
Pos 1 ID	Pos 2 ID Pos 3 ID	
	Phase	
	R S T N O O O Current	
	R S T N	
	Power Direction	
	Up NEXT X EXIT	All Cycle Number

Figure 22: Interface after the changes

Moreover, it was desirable to basically leave the logic unchanged, just adapt what was previously created in the independent VI, to the preexisting code. Furthermore, within the VI called "PROVA_SM", in the case structure "init", all initial setups were made, including the report file to be compiled later and the folder where the reports were placed.

Hence all of that logic was deleted and replaced with the subVI "Report_Generetion_2", here the excel report is created and the fields "UUT ID 1", "UUT ID 2", "UUT ID 3", "Name Operator" and "2CE Number" are filled in.

The changes are shown in the following picture:

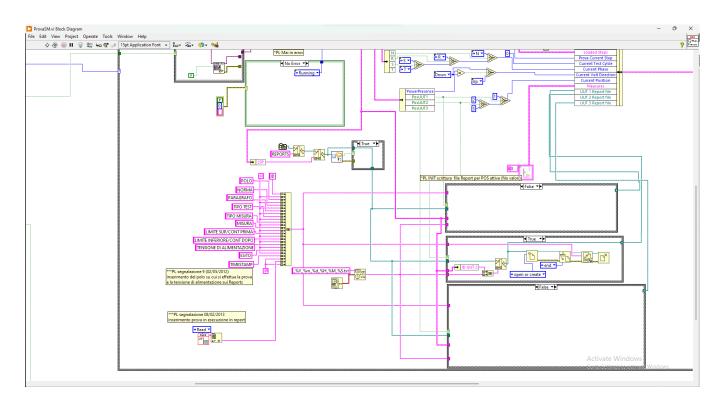


Figure 23:Original VI

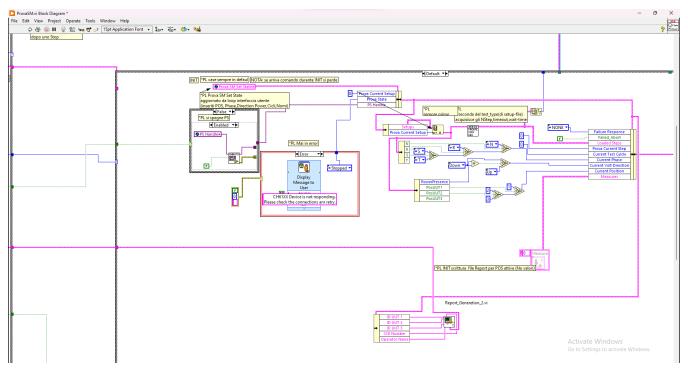


Figure 24: VI after the changes

In particular the creation of the report needs to be placed here because, at this moment the test is not yet started e so the time "lost" to create the file report will not affect the measurements. Instead, if the report is created where in the subVI listen below, so where the measurements are actually saved, it will falsify the tests, since the machine will lose more time during the test.

Then the "ExecutionStep2" VI was modified, in particular the following subVIs:

- WriteMeausureRecord

Where there are five case structure: "Continuity before","Continuity after","Volatge","Current" and "Time", managing the types of measurements the machine can do. In particular all these structure are all the same, the only thing that changes is the value that is measured.

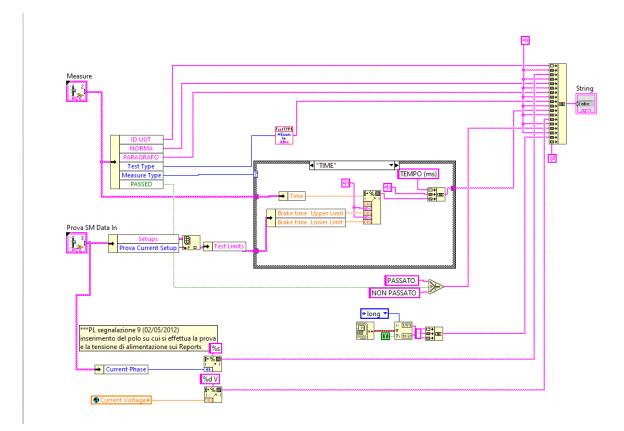


Figure 25: Original VI

As shown in the previous picture, the aim of this subVI is to build a string where it's written in sequence: the name of the UUT, the reference of the test on the norm, the type of test, the date, the value measured and finally if the test is successful or not.

In the following picture, instead, it's possible to see the new adaptations:

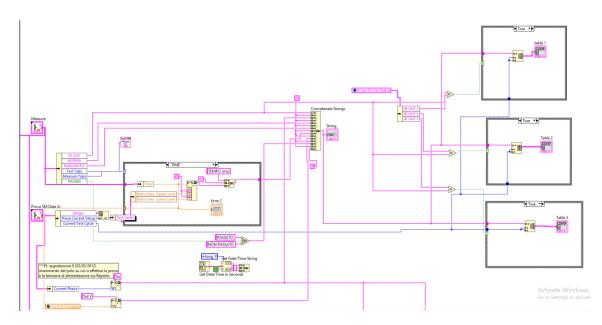


Figure 26: VI after changes

As shown, the logic of this VI didn't change, the aim is always to build a string with some less information of the previous case, in fact the date is not written every time for each line, but it's written only once at the beginning of the file report. The big difference is that in this case there is a comparison between the name of the UUT and the name given to the UUT in position one, two and three, in order to place the string in the right table, which will be then place in the right page of the excel report.

- WriteMeausureRecordOnFile

In this other subVI the string previously built is placed inside the report file created in the "PROVA_SM.VI", in particular at the end, as shown in the following picture.

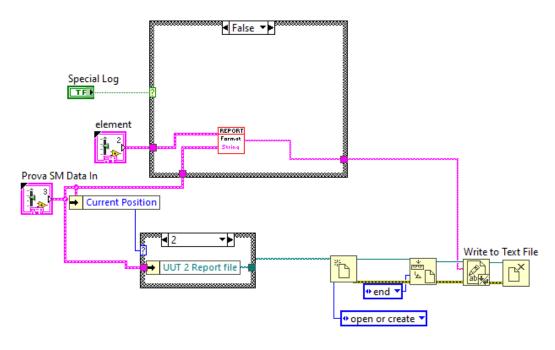


Figure 27: Original VI

In the following picture, instead, it's possible to see the new adaptations:

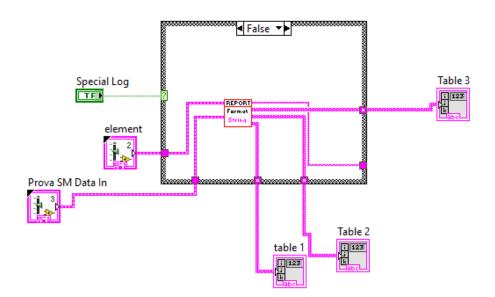


Figure 28:VI after changes

In this case, the storage of the results and measurements happens in three tables:

- Table 1 collects the data for the first UUT, so this table should be placed on the first page of the Excel file.
- Table 2 collects the data for the second UUT, so this table should be placed on the second page of the Excel file.
- Table 3 collects the data for the third UUT, so this table should be placed on the third page of the Excel file.

The aim of this is, once the table are fully filled, to then insert these tables inside the report previously created and complete it.

This task was unfortunately not completed as, due to lack of time, it was decided to give higher priority to the task to be shown later. Nevertheless, in the following picture can be seen the report that the machine produces at the moment:

File Home	Inserisci	Disegno	Layout di	pagina	Formule	Dati	Revisione	Visualizz	a Automa	ate Com	ponenti ago	jiuntivi G	iuida			🖓 Con	nmenti 🛛 🖻	Condivid
	Calibri G C	-)[1 <u>s</u> - <u>-</u> -	1 ~ A^	A* =	= = =	°⁄~ ≖ ≖	e₽ ₩ ~	Generale	000		ttazione For	matta come tabella ~	Stili cella ¥	 Inserisci Inserisci Elimina Formato 	Σ ~ 	AZY Prdina e Trova e filtra ~ seleziona	Ado	l-ins
Appunti 🕞		Carattere		F5	Allinea		F3		meri	15		tilli		Celle		Modifica	Compone	nti aggi
14 ~	: × ~	fx																
A	В	с	D	E	F	G	н	1	J	к	L	м	N	0	P	Q R	S	т
Data:		20/09/2023																
Nome operate	ore:	Maria																
Rampa 30 mA A	C 230 V 50 I	Hz																
Tempi O 30 mA	AC 230 V 50	Hz																
Rampa 42 mA p	 arzializzata	0° 230 V 50 H	z															

Figure 29: Updated report that the machine produces now

As it is shown, the report meets already some of the requirements that were discussed before:

- For instance, the report is produced in Excel, a format much more useful to the company then.txt, in addition to that, the information shown are all clear and easily readable.
- The name of the report is the one that the user can insert from the field called "2CE number", shown in fig. 22
- The name of the tree sheets are the ones inserted by the user in the fields called respectively "Pos 1 ID", "Pos 2 ID", "Pos 3 ID", shown in fig. 22 and each of these sheets reports the information of the corresponding UUT.
- As required, the date is given as well as the name of the operator, which is inserted by the user in the interface shown in fig. 22
- Finally, they are shown also the type of test that the user has selected from the dynamic list shown in fig. 11

The only step missing is the insertion of the table build in fig 26 and in fig 27 in the currently report.

Chapter 5

5 Managing amplifier faults

The work done before this one had shown that the linear amplifier was probably the cause of the irregularities in the generated signal, because while the signal did not show any irregularities at the amplifier's input, it showed undesirable peaks and offsets at the output. Thus, to overcome this problem, the linear amplifier was sent for repair for two months.

Once it was back and connected, we proceeded to an analysis of the device's status in order to verify that it had indeed been fixed.

All tests and verifications were carried out on a trio of earth leakage circuit breakers of the following type:

F202 A 40A/30mA

And the workstation used to carry out the measurements was the central one.

5.1 Amplifier defects

In order to evaluate the performances of the amplifier was used:

- Oscilloscope: PicoScope 6824E/YOKOGAWA DL9140
- Voltage probe: LeCroy: AP032 DIFFERENTIAL PROBE

- Current probe: FLUKE i2000 FLEX

with which it was measured the current and voltage across the switch, the input and output voltage of the linear amplifier.

The following figure shows the setup used:



Figure 30: photo of the probe setup for measuring the voltage between poles R and N and the current at pole R

In carrying out initial checks, it was noticed that, despite the two months in repair, the amplifier's problems had remained unchanged, in particular the signal irregularities were two:

- A very intense peak of varying amplitude

- A negative offset

In the following image it can be seen these two anomalies mentioned above:

- The yellow signal, the most important one, represents the **current** flowing through the switch.
- The pink signal represents the **voltage** at the input of the amplifier.

- The blue signal represents the output **current** from the amplifier, proportional to the current flowing through the switch.



Figure 31:in the image, the current through the switch is acquired by oscilloscope, where we can see the presence of the peak and the negative offset. The test selected was a timing test with a 0-degree bias

It is easy to see how, in particular, the spike can pose a threat to the tests, as it occurs with varying intensity and, especially for even more sensitive switches, could be dangerous as it could cause the switch to trip prematurely and cause the test to fail.

As can be seen from the picture, the peak always occurs slightly earlier than the negative offset, and the latter always 'compensates' before the actual test, so it is a problem that can be ignored for the time being, as the peak is more dangerous. Both the peak and the offset occur when the amplifier is switched on, after the continuity test, which is represented by the positive offset in the yellow signal.

With the help of my tutors, we invited a technician from the former 'DANA' company that manufactured the amplifier, the same one who had repaired the instrument a couple of months earlier. From this on-site analysis, it emerged that the amplifier is not exactly broken, but rather the spike is a production bug. The technician explained that the sudden change of OFF-ON state generates a rush current that can be controlled by the amplifier's voltage potentiometer. Basically, this potentiometer limits the current and the programmed voltage at the output of the amplifier, so the higher the potentiometer, the higher the output current, and the higher the amplitude of the peak we see on the oscilloscope. By setting the potentiometer to the minimum, therefore having a very small programmed current, the peak no longer occurs at the output. As shown in the following image:

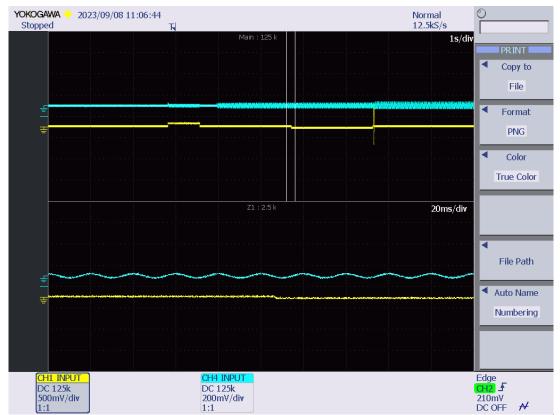


Figure 32:photo of the test with potentiometer at idle where the peak is not present.

Although this solution is formally correct, it cannot actually be used, as the operator would have to position the potentiometer knob and periodically check it.

However, since the aim of this project is to build a machine capable of testing independently, so without any interaction with humans during the test, it is not a very feasible solution.

Therefore, other solutions were evaluated to solve this peaking problem. These solutions involve the use of contactors and FPGAs, which are introduced in the following paragraphs.

The initial idea was to bypass the peak somehow, and that is where the contactors come in.

5.2 Contactors

A contactor is an electronic device that belongs to the relay category, however, compared to relays, contactors are used with very high current carrying capacities.

The purpose of a contactor is precisely to open and close a circuit via its power contacts and consists of three main components:

- **The coil**: is the most significant component, which allows the power contacts to be opened or closed when energized.
- **The contacts**: are the components of the device that carry the energy through the circuit being switched and there are different types of them.
- The contactor body: is used to isolate the contacts and the bushing in order to protect users from accidental contact with live parts and to protect internal parts from environmental hazards.

The operating principle of an electric contactor is simple. When a current flows through the electromagnetic coil, a magnetic field is created. This causes the armature inside the contactor to move in a certain way with respect to the electrical contacts.

(https://it.rs-online.com/web/content/discovery-blog/idee-

suggerimenti/guida-contattori, s.d.).

There are two types of contactors:

- The normally open (NO): when the contactor is energized it becomes a closed switch and lets the current flow, whereas when the contactor is de-energized becomes an open switch.
- The normally close (NC): when the contactor is energized it becomes a open switch and lets the current flow, whereas when the contactor is de-energized becomes an closed switch.

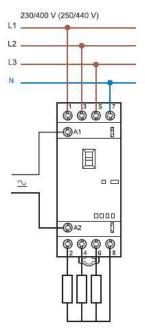


Figure 33: wiring diagram of a four-pole contactor

5.3 First solution: One contactor

Since both the peak and the offset are present at the output of the linear amplifier, but not at the input, it's quite clear that the problem is inside this component.

As mentioned earlier, the aim is to try to improve the quality of the signal output to the amplifier, so the first approach to a solution was to insert a normally open contactor in series with the amplifier output, identified as C_1 , which, depending on the position of the coil, allows or does not allow the connection between the amplifier and the UAPDIFF machine.

This contactor then acts as a switch between the output of the amplifier and the rest of the machine, in particular:

- When the switch is closed, the amplifier is connected to the machine and everything works normally.
- Conversely, when the switch is open, the amplifier is disconnected from the rest of the machine.

The contactor needs something to drive it and actually tell it when to open or close the contacts, so for this first stage, where it was needed to just try the operation of the logic, a simple latch was used to control the contactor. Therefore, since the peak was very sharp and short, the first solution was for the contactor to disconnect the amplifier from the UAPDIFF at the peak and reconnect it later once the peak had occurred, before the start of the test.

The new logical flow to be followed for the conduct of the test is as follows:

- 1) C_1 is closed and everything is working normally.
- 2) The continuity test before the actual test is conducted.
- 3) C_1 is open and the amplifier is disconnected from the UAPDIFF.
- 4) The peak occurs.
- 5) C_1 is closed.
- 6) Delivery of the actual test.
- 7) The continuity test after the actual test is conducted.
- 8) Go to 1) all over again.

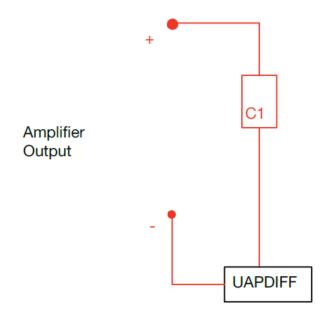


Figure 34:Connection diagram between UAPDIFF and Contactors C1

In order to make the experiment possible, it was introduced a delay of 1600ms into the code between when the amplifier is switched on and when the test is actually delivered, in order to manually allow the circuit to be closed after the peak but before the start of the test.

Next, it was necessary to calculate when the amplifier is switched on (and thus when the peak occurs), or rather, it was necessary to calculate the

time interval between the start of the continuity test and the start of the peak, in order to know the exact moment when to manually open the circuit. Using the sliders, this value was 2890ms, so from the start of the continuity test, just count about 3s and close the circuit.



Figure 35: distance in ms between continuity test and peak

Several tests were carried out, but the solution still proved to be unsuccessful, because every time the circuit was closed, the peak presented itself with the opposite amplitude to the previous one, so every time the amplifier was connected to the UAPDIFF, the peak still presented itself, as it is shown in the following picture:

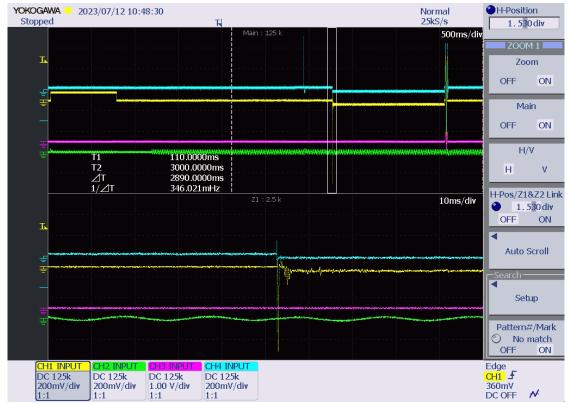


Figure 36: photo of the test using the new setup, including the contactor between amplifier and UAPDIFF

5.4 Second solution: Two contactors

The next iteration was to add another contactor. In fact, the problem arose when the contactor was connected to the machine, so the idea was to, instead of disconnecting the amplifier at the peak, short-circuit it so that the peak would be discharged to this new branch and not to the machine. The new circuit diagram is as follows:

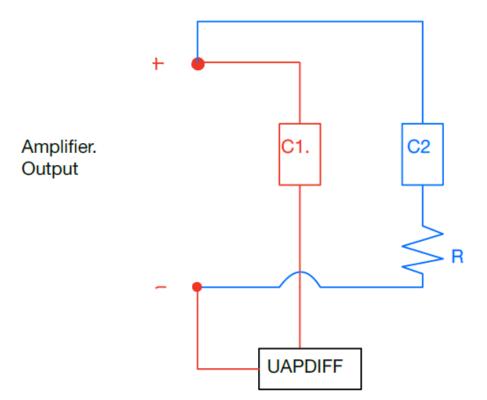


Figure 37:Connection diagram between UAPDIFF and Contactors C1 and C2

This new contactor is also a normally open contactor, identified as C_2 , which, depending on the position of the coil, connects or disconnects the amplifier to a short circuit:

- When the switch is closed, the output of the amplifier is connected to a short-circuit.
- Conversely, when the switch is open, the amplifier is disconnected from the short-circuit.

Afterwards, for safety reasons, a small 1Ω resistor was putted in series with the output of the amplifier in order to not close it on a short-circuit.

Also in this case, the contactor was driven by a simple latch and, since now there are two latches to manually press, the interval of time between the amplifier is switched on and when the test is actually delivered was extended to 1900ms.

The new logical flow to be followed for the conduct of the test is as follows:

1) C_1 is closed, C_2 is open and everything is working normally.

- 2) The continuity test before the actual test is conducted.
- 3) C_1 is open and C_2 is closed, therefore the amplifier is disconnected form the UAPDIFF, but connected to the resistor (short-circuit).
- 4) The peak occurs.
- 5) C_1 is closed and C_2 is open, therefore the amplifier is disconnected form the resistor, but connected to the UAPDIFF, everything is working properly.
- 6) Delivery of the actual test.
- 7) The continuity test after the actual test is conducted.
- 8) Go to 1) all over again.

The tests were carried out very similarly to the ones of the first solution, therefore, also in this case, it was needed to know the exact moment to perform point 3) of the previous list of steps.

Thus, as before, using the sliders, the time interval between the start of the continuity test and the start of the peak was evaluate, in order to know the exact moment when to manually perform point 3).

Many tests were performed on different tests and many time and all of them showed a big improvement of the quality of the signal generated, as shown in the following pictures, where the signal of our interest is the yellow one:



Figure 38:photo test after the introduction of the second contactor

It's important to say that the peak is not completely removed, but it's much more reduced than before, in a way that it doesn't represent a threat anymore.

In order to ensure that, in this case, the peak discharged on the short circuit, a current probe was used and placed it on the branch of interest, so that it could be observed its behaviour on the oscilloscope.

Since all channels on the oscilloscope were occupied, the one of least interest was replaced, i.e. the channel representing the voltage across the switch, with this new channel representing the current through this shortcircuited branch, as shown in the following picture, where the signal in yellow represents the current across the switch and the signal in green represents the current on the new branch:

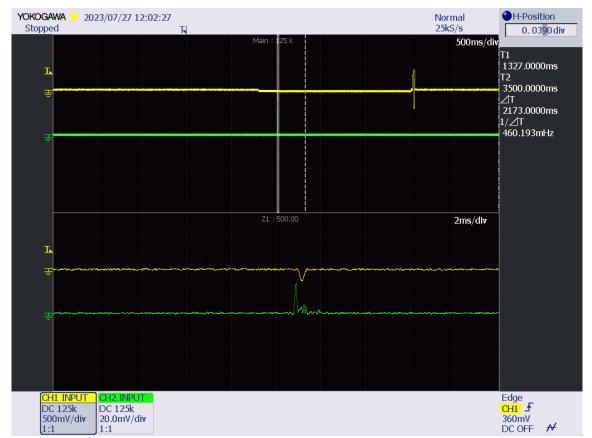


Figure 39: picture of a test where the current through the switch and the new ramp introduced with a 1Ω resistor is shown.

As shown in the figure above, the peak is as if it was splitting and most of its intensity is concentrated on the branch with the lower resistance, i.e. the one with the 1Ω resistance, however it is strange to see the peak split over the two branches, when in theory the two branches should never be closed at the same time, so the peak, i.e. the current, should only occur in one of the two. A very plausible explanation is that this irregularity is due to the human error factor during the manual opening and closing of the two contactors and the correct timing with which to open or close them, so once the solution is automated, it should further improve performance.

5.5 Solution automation

Since this time the solution was successful, the next step was to automate it.

Considering that on the machine was already available a FPGA module, it was convenient to use it, in order to drive the contactor.

For instance, the two contactors were replaced with a single contactor, having both normally open and normally closed contacts:

- The **normally closed** contact to the contactor named with C_1 , which is located between the amplifier and the machine.
- The normally open contact to the contactor designated with C_2 , which short-circuits the amplifier.

In this way when the coil is energised, C_1 opens and C_2 closes.

The idea was to create a kind of virtual switch, which would either power the contactor or not via FPGA.

As you can see in the following diagram:

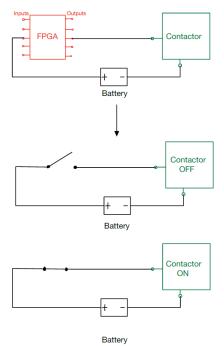


Figure 40:Connection diagram between FPGA and Contactor and visual explanation of the concept of virtual switch

The FPGA board can energize the contactor through its output pin, in particular:

- If we want to energise the contactor, we must output the power supply that the FPGA is capable of producing.
- If we want to switch it off, on the other hand, we must output zero.

5.5.1 FPGA

FPGAs (*Field Programmable Gate Array*) are programmable

semi-conductors devices, which allow customised integrated circuits.

The operation of FPGAs is based on the programming, using the hardware description language (VHDL), of the logic gates (AND, OR, XOR and NOT) with which they are equipped.

These devices are therefore composed of a matrix of configurable blocks, **CLB**, connected to each other by a configurable network, which also manage input and output signals.

What makes them even more interesting to use is also the fact that they are equipped with **registers**, namely devices that store data. They allow quick access and allow to change the information stored with a new one.

Compared to the ASICs, FPGAs are more flexible and cost effective, since they allowed to be newly programmed and used for new purposes, very easily.

On the other hand, ASICs are integrated circuits composed of electrical component such as, transistor, capacitor, resistor etc. Moreover, they are compact, fast but highly specific, therefore it's very difficult to change the logic of a small part of the circuit.

In addiction to that, FPGAs are highly boastful because they allow to program in parallel, so they allow to do many actions all at once instead of the one action that ASICs and similar allow.

Here the FPGA available was the PXI-7841R of National Instruments. (Brand)

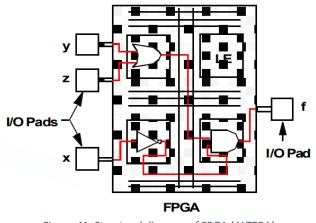


Figure 41: Structural diagram of FPGA (ALTERA)

5.5.2 Implementation: First attempt

The new contactor (Schneider LC1D066M7) needs as power supply 6V DC, obtained from the FPGA board as it is capable of generating, as said before, a voltage of \pm -10V DC, which is very convenient, since there is no need for external power supply, therefore that's why we switched to this new solution.

Again, labVIEW is equipped with a library for controlling the FPGA, in particular, it is possible to create FPGA VIs to be placed within a project and run on the target, PXI 7841R in this case.

The target can only run the top-level VI, so it is important not to overwrite the new logic, but to integrate it with the old one so that the machine continues to do what it did before without any problems.

Therefore, first the project on which the UAPDIFF works, called "ABB-**Diff project**", was identified, and then the VI top level that is executed on the target of interest was identified, called "ABB-Diff MainFPGA".

As mentioned before, one of the great advantages of the FPGA is the fact that it can be programmed in parallel so that it can perform several functions simultaneously.

Hence the new logic was introduced in parallel to the old one, in the following way:

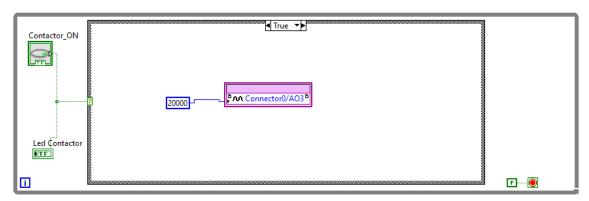


Figure 42: Contactor logic on LabVIEW FPGA project.

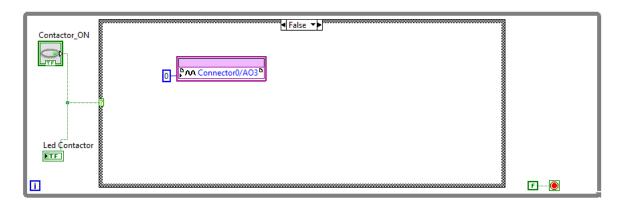


Figure 43: Contactor logic on LabVIEW FPGA project.

As can be seen from the pictures, there is a while loop with the output condition always set to false, so that it will always run as long as we don't interrupt the VI.

Inside this while loop, there is a case structure controlled by a Boolean called "**Contactor_ON**", so as can be guessed from the name:

- When it is set to **true**, the case structure manages the **switching on** of the contactor, by setting the output to 20000, thus allowing the power to reach the contactor and activate it, just as was said before.
- When it is set to **false**, the case structure manages the **switching off** of the contactor, by setting the output to 0.

There is actually a conversion factor between the value of the voltage of the output pin and the input code mapping, this factor was taken from the

data sheet of the hardware I am using (PXI-7841R), as shown in the following picture:

Analog Output

The bipolar output range of the NI 783xR/784xR/785xR AO channels is fixed at ±10 V. Some applications require that the AO channels power on to known voltage levels. To set the power-on levels, you can configure the NI 783xR/784xR/785xR to load and run a VI when the system powers on. The VI can set the AO channels to the desired voltage levels. The VI interprets data written to the DAC in two's complement format. Table 2-3 shows the ideal AO voltage generated for a given input code.

Output Description	AO Voltage	Input Code (Hex) (Two's Complement)
Full-scale range -1 LSB	9.999695	7FFF
Full-scale range -2 LSB	9.999390	7FFE
Midscale	0.000000	0000
Negative full-scale range, +1 LSB	-9.999695	8001
Negative full-scale range	-10.000000	8000
Any output voltage		$\frac{AO \ Voltage}{10.0 \ V} \times 32,768$

Table 2-3. Ideal Output Voltage and Input Code Mapping



Note If your VI does not set the output value for an AO channel, then the AO channel voltage output will be undefined.

Figure 44:data sheet of the PXI 7841R (PXI 7841R Datasheet)

Therefore, in order to have 6V as output we need:

Input Code =
$$\frac{6000 * 32,768}{10,0} = 19660 \sim 20000$$

Furthermore, the Boolean, "Contactor_ON", has been made global variables that can be called in the code to enter or not enter these case structures.

Since the amplifier technician established that the problem occurred whenever the amplifier was switched on, the logic of the contactor has to be managed at where in the code the amplifier is switched on.

Consequently, within the VI "ExecuteStep2", there are two case structure "START_MEAS_CURRENT" and "START_MEAS_TIME" which manage the tests for tripping current and tripping time respectively.

For both of the above-mentioned case structures, the logic implemented was the same as shown in the following pictures:

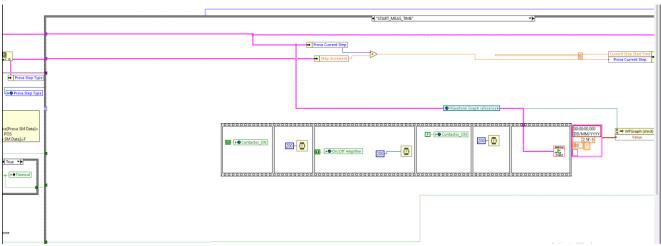


Figure 45: FPGA logic inside UAPDIFF's logic

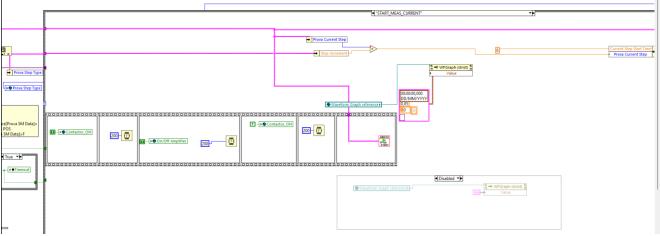


Figure 46: FPGA logic inside UAPDIFF's logic

In practice, the contactor is switched on 200ms before the amplifier is switched on, setting the variable "Contactor_ON" to true, and then switched off 200ms after switching on the amplifier and 200ms before delivering the waveform for the actual test, setting the variable "Contactor_ON" to false.

The next step was the testing phase of the algorithm.

Therefore, a multimeter (FLUKE 175 true RMS multimeter) was used in order to measure the voltage produced by the output pin of the FPGA board and its corresponding ground.

The idea is to stick the two multimeter leads between the output pin of the FPGA board and the corresponding ground, in this way, when the Boolean 'Contactor_ON' is set to true, and thus the contactor is energized, the multimeter should reads 6V.

The algorithm has actually shown itself successful, in fact when the Boolean contactor_ON is set to true, output read by the multimeter was read 6V, instead when contactor_ON was set to false, the output read by the multimeter was 0V, confirming also the absence of spurious or unwanted currents when the output signal is set to 0V.

Despite that, the contactor seems to not change the state at that point the same multimeter was used as before, but in continuity mode, that is a mode whereby the multimeter itself delivers a small current and emits a sound when recording a current passage.

Furthermore, when the contactor is switched off:

- The normally closed contact allows the passage of current, so when the multimeter's tips are connected, it should emit the sound that confirms the continuity.
- The normally open contact doesn't allow the flow of current, so when we the multimeter's tips are connected, it should not emit any sound.

This actually happens, but when the contactor is energised the normally open contact and the normally closed contact should switch, therefore:

- The normally closed contact should open, thus when the multimeter is connected, it shouldn't emit any sound.
- The normally open contact should close, thus when the multimeter is connected, it should emit the sound to confirm the continuity.

But this doesn't happen, so the contactor doesn't actually switch state. This is because a deeper analysis revealed that there was a typo on the site where the new contactor was bought. In fact, while on the website the contactor appeared to be energizable via a voltage of 6V DC, in the data sheet of the device this was absolutely not possible, since the required voltage was 220V AC at 50/60Hz.

5.5.3 Implementation: Second attempt

The next step was to search for a new contactor to be controlled with the voltage generated by the FPGA (+/- 10V), however, the search proved inconclusive, as there were no contactors existing or available in short time that could be controlled with such low voltages.

It was decided to use at least the contactors that were already inside the company, in order to not waste any other time, so the two contactors that were used at the beginning were picked, but both of them are driven by 24DC voltage, that the FPGA is unable to produce.

Thus, the project proceeded by adding a voltage regulator (LM317T STMicroeletronics), that gives as output 24V DC, between the FPGA and the contactors.

In that way, the VI logic would not have been disrupted, thus the VI logic in the **ABB-Diff MainFPGA.VI** was changed in the following way:

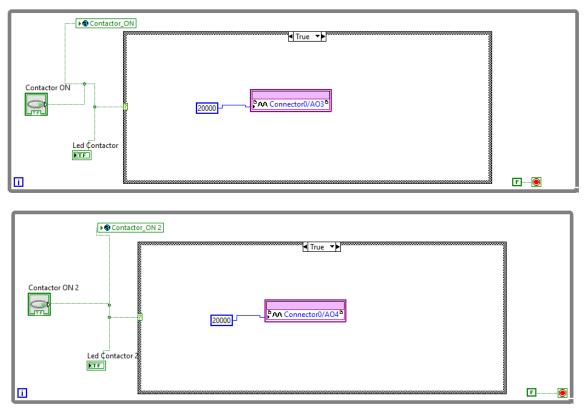


Figure 47: FPGA logic

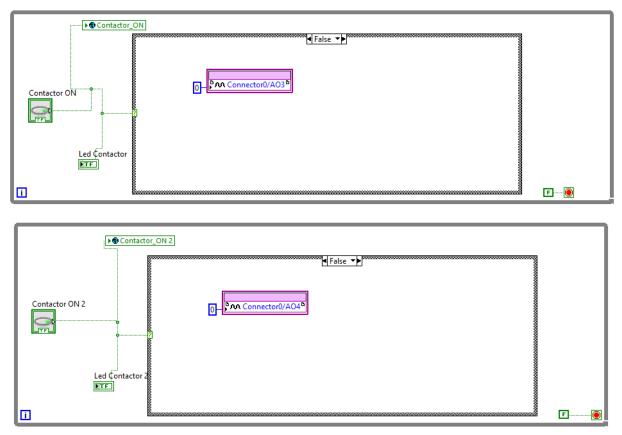


Figure 48:FPGA logic

Since the two contactors are both NO, the Boolean that controls the contactor C1 need to have a default value true, because it needs to be closed for almost the entire duration of the test.

Once this VI was compiled, so the FPGA board actually received the new instructions, the actual machine logic was changed in the following way:

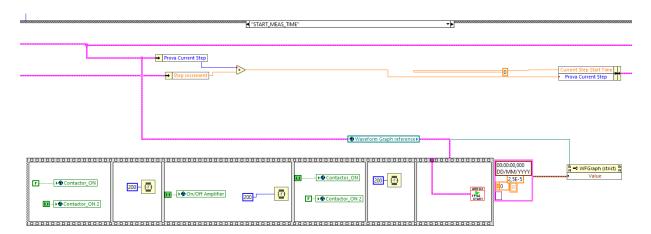


Figure 49:FPGA logic inside UAPDIFF's logic updated.

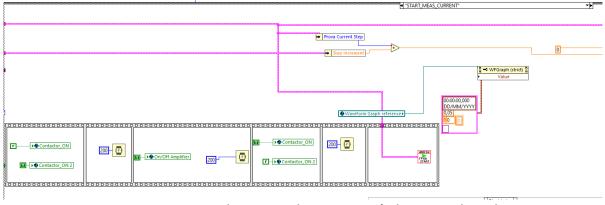


Figure 50:FPGA logic inside UAPDIFF's logic updated.

At this point, the voltage regulator can produce a variable voltage from 1.2V to 37V, therefore the voltage in output depends on a resistive load, as shown in the following picture:

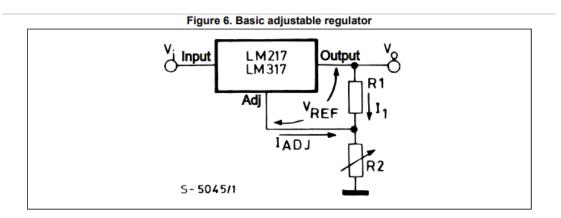


Figure 51: Adjustable regulator diagram (LM217, LM317 : 1.2 V to 37 V adjustable voltage regulators's Datasheet)

From the picture, it can be seen that the output voltage depends on the other parameters shown in the following way:

$$V_O = V_{REF} * \left(1 + \frac{R_2}{R_1}\right) + I_{ADJ} * R_2$$

From the datasheet of the regulator it's known that the second term $(I_{ADJ} * R_2)$ can be neglected, since I_{ADJ} is very small (~100 µA at most) by design.

Since the datasheet also says that $V_{REF} = 1.25V$, as a consequence, the following equation is obtained:

$$24 = 1.25 * \left(1 + \frac{R_2}{R_1}\right)$$
$$\downarrow$$
$$\frac{R_2}{R_1} = 18.2$$

Therefore, by fixing: $R_1 = 1.2 \text{ k}\Omega$ R_2 can be obtain as a consequence: $R_2 = 21.84 \text{ k}\Omega$

those are the ideal values of the resistors, as real values, they can be set as:

 $R_1 = 1.2 \text{ k}\Omega$ $R_2 = 22 \text{ k}\Omega$ Thus, it is obtained $V_0 \sim 24.16 \text{ V}$

This simple circuit was built on bread board, so that if this solution actually worked, it could be welded, as it is shown in the following figure:

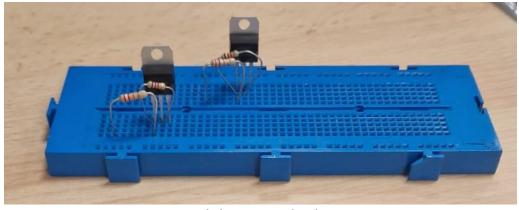


Figure 52: laboratory-built circuit

However, once this solution was tested, again, it was not successful, since the voltage produced by the voltage regulator was not enough to turn on the contactors.

5.5.4 Implementation: Third attempt

This last implementation was the **successful one**.

The aim was still to automate the solution, using laboratory resources and changing as little as possible the software logic.

Therefore, the two contactors were again substituted with one single contactor with both normally closed contacts and normally open contacts, in particular, as before:

- The **normally closed** contact to the contactor named with C_1 , which is located between the amplifier and the machine.

- The normally open contact to the contactor designated with C_2 , which short-circuits the amplifier.

In this way when the coil is energised, C_1 opens and C_2 closes.

This new contactor (ABB B6-30-01) works with 24V AC (50 Hz/60 Hz), therefore it was used an external power supply, capable of producing the required voltage, that would energise the contactor.

This external power supply was driven by a relay, which worked with 24V DC, despite this, it was noted that the coil actually changed state as early as 20V DC.

Thus, the relay was the new component to be controlled through FPGA, furthermore the FPGA was now required to produce 20 V DC.

As said before, the output pins of the FPGA are capable of producing a range of voltage that goes from -10V DC to +10V DC, the idea was then to use two pins:

- One capable of producing 10V DC.

- One other capable of producing -10V DC.

In this way the difference between the two outputs pin is 20V high enough to drive the relay.

Therefore, the FPGA logic was changed in the following way:

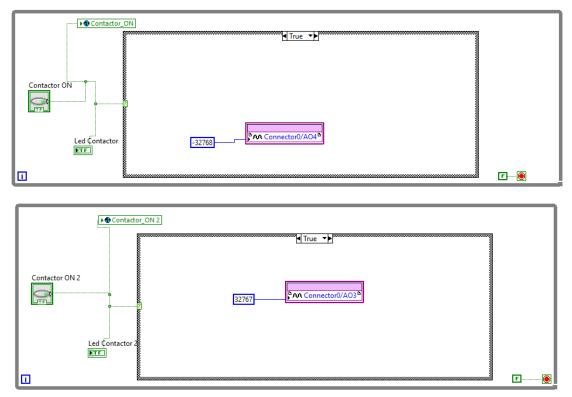


Figure 53: FPGA true logic updated.

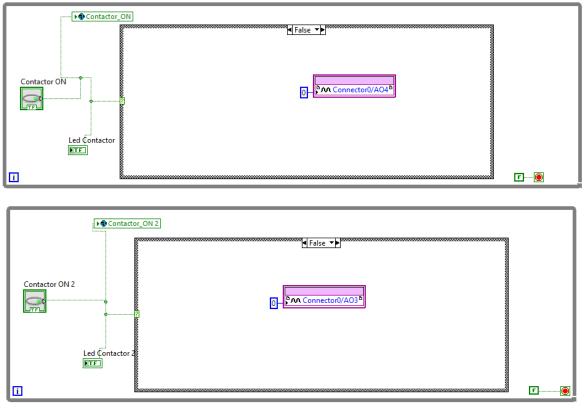


Figure 54: FPGA false logic updated.

As it can be see from the pictures above, there are now two output pins used:

- AO4 is used to provide -10V and it is driven by the Boolean "Contactor_ON", which was made global variable.
- AO3 is used to provide 10V and it is driven by the Boolean "Contactor_ON2", which was made global variable.

As said before, it is not written directly 10 on the logic but 32768, because of the conversion factor between the output voltage and its value in 16-bit resolution.

Very similarly to before, when the two Booleans are switched to true then the relay is energised, instead when they are switched to false then the relay is turned off.

In the same way as the first and second iterations, the two global variables are called inside the UAPDIFF logic, in order to activate the contactor thew milliseconds before the peak and turn it of thew milliseconds after, as it is shown in the following pictures:

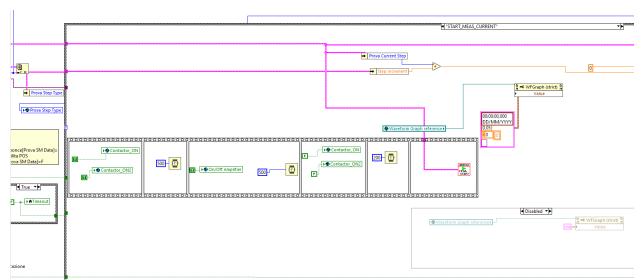


Figure 55:UAPDIFF integrated logic for current

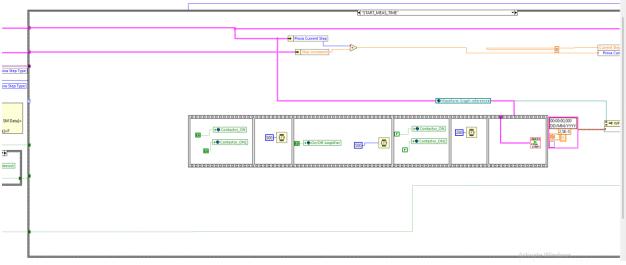


Figure 56: UAPDIFF integrated logic for time

In this way it was possible to control the relay, which controlled the contactor.

Actually, once the relay was connected to the outputs of the FPGA, the output voltage decreased from 20V to 17V, since the relay absorbed some energy, therefore it was added an external voltage generator, put in series to the output of the FPGA, which produced approximately 3V, that were enough to activate the relay.

The final setup is shown in the following picture:



Figure 57: Final setup of the automated solution

5.6 Results and validation

Once the setup was ready, it was performed some testing in order to make sure that also after the automation the peak wasn't showing off. Therefore, the testing was performed for both functional characteristics:

- The tripping current:

During this test an increasing sinusoidal ramp is generated at 50 Hz and the RCCB has to open before the ramp reaches an amplitude of 30 mA. The following picture represents an oscillogram taken during the testing, where the signal of major interest is the yellow one, which represents the current through the residual current circuit breaker:

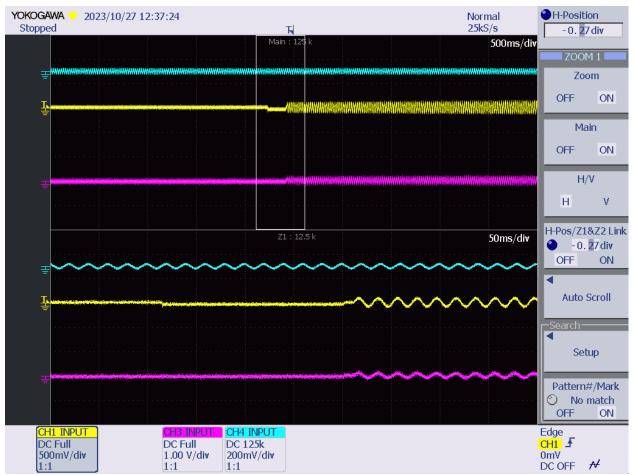


Figure 58: Oscillogram of the tripping current testing after the automation

As it can be seen, the peak that before was present at the beginning of the negative offset now it's not there anymore.

- The tripping time

During this test a sine wave with an amplitude of 30 mA at 50 Hz is generated, in which case the RCCB must be triggered within the time frame set by the standard.

The following picture shows an oscillogram taken during the testing of the tripping time, as before, the signal of major interest is the yellow one:

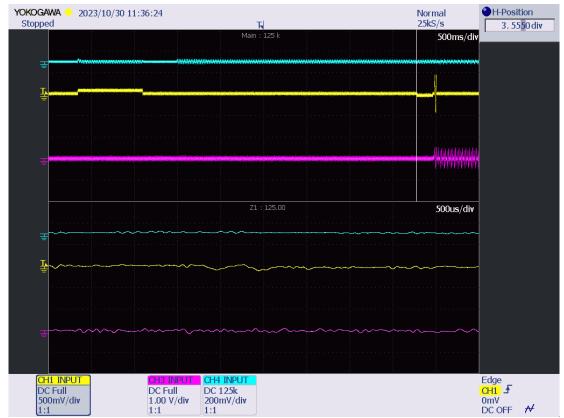


Figure 59: Oscillogram of the tripping time testing after the automation.

As it can be seen, also in this case the peak is not present anymore, therefore it can be concluded that the problem was solved and the solution was successful.

At this point, the last thing to do was to validate the solution, making sure that the measures taken by the UAPDIFF were reasonable and trustworthy compared to the ones taken by hand by the operators. Therefore, they were taken some results for both the testing of the tripping current and the tripping time, to be compared with the ones taken by hand.

As shown in the following tables, the results taken during the tripping current test are:

	Campione1	Campione2	Campione3
Ciclo1	24	21,4	22,6
Ciclo2	22,9	21,6	20,8
Ciclo3	22,4	21,8	20,6
Ciclo4	22	21,7	21,2
Ciclo5	22,3	22,1	20,4

Figure 60: measurements taken by hand

	Campione1	Campione2	Campione3
Ciclo 1	24,6547	20,26485	21,32504
Ciclo 2	25,32607	20,65016	21,31268
Ciclo 3	24,11714	20,72488	21,45211
Ciclo 4	24,07485	20,97634	21,11818
Ciclo 5	23,85743	20,90158	21,38677

Figure 61: measurements taken by the UAPDIFF machine

The following bar plot shows the measure of the tripping current, comparing the results taken by hand and the results taken by the UAPDIFF:

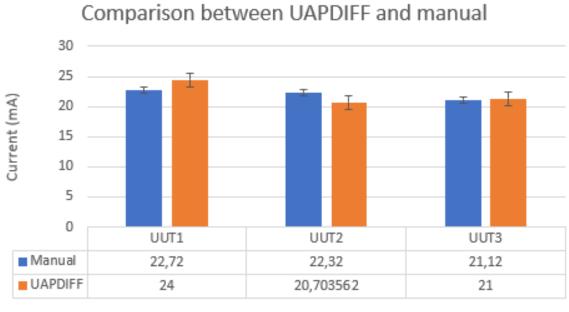




Figure 62: comparison between the UAPDIFF and manual measurements during the same tripping current test

As it can be seen from the plot, the results taken by the UAPDIFF are really close to the ones taken by hand, which means that they are actually trustworthy results.

As shown in the following tables, the results taken during the tripping time test are:

	Campione1	Campione2	Campione3
Ciclo1	45	26	35
Ciclo2	45	26	35
Ciclo3	45	26	35
Ciclo4	45	26	35
Ciclo5	45	26	36

Figure 63: measurements taken by hand

	Posizione 1	Posizione2	Posizione3
Ciclo1	45,6	26	35
Ciclo2	46	26	36
Ciclo3	45	26	36
Ciclo4	45	26	36
Ciclo5	45	26	37

Figure 64: measurement taken by the UAPDIFF machine

Below the plot are shown the data, each value represents the mean of five results taken by the tests performed.

Whereas, the following bar plot shows the measure of the tripping time, comparing the results taken by hand and the results taken by the UAPDIFF:

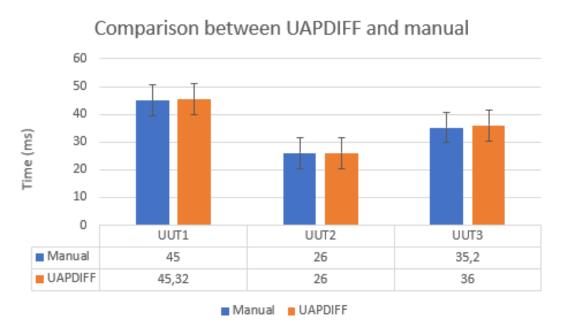


Figure 65 :comparison between the UAPDIFF and manual measurements during the same tripping time test

Also in this case, the results are close to each other, validating this solution once again, even for the tripping current measurements. As before, below the plot are shown the data, each value represents the mean of five results taken by the tests performed.

In conclusion, the above solution is already a good solution, however for future developments of this project, one could consider using a simple linear amplifier to amplify the output voltage of the FPGA, without having to add an external voltage generator.

Chapter 6

6 Conclusions and future developments

In this thesis, we have extensively discussed the activities carried out on the UAPDIFF machine, located in the electrification and smart buildings labs of ABB S.p.A in Vittuone (MI).

The UAPDIFF machine performs functional tests on the tripping current and tripping time of residual current circuit breakers, in compliance with the standard CEI EN 61008.

The aim of this thesis was to adjust the UAPDIFF machine to perform accurate and reliable tests and improve the reports generated at the end of the tests.

At the beginning of the activities, the machine produced a signal for testing residual current circuit breakers characterized by an unwanted peak of variable intensity capable of jeopardizing the test outcome. The machine also generated a test report in .txt format, not suitable for easy interpretation.

The desired outcome at the end of the thesis was a machine capable of producing a clean signal without unwanted peaks and a test report in Excel easily readable, this task, however, was not completed due to time constraints, resulting in partially completed information in the reports.

At the conclusion of the activities, we successfully obtained a peak-free signal by integrating a contactor capable of discharging the peak onto an alternative circuit. This solution was then automated using an FPGA module already present on the machine.

In conclusion, this was a highly extensive and complex project, significantly influenced by factors as the lack of information about the machine (electrical diagrams, logical schemes, etc.), lengthy waits for the delivery of certain components, and poor compatibility between the new software and hardware. Even though not all activities have been completed, the thesis goal was achieved: a machine capable of automatically conducting functional tests, and generating validated and reliable results is now available.

Furthermore, this work lays the foundation for future developments as: completing the information reported in the test report and expanding the machine's application to include B-type, F-type, and voltage-independent switches could be pursued.

7 Bibliography

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