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Low Efficiency Injection Anode Diode

for future LEIA RC-IGBT

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Ai miei genitori, perchè hanno creduto in me sin dal primo giorno.

A Pasquale, perché ha saputo rendere speciali questi anni.

A me stessa, perché ho saputo rialzarmi anche quando pensavo di non farcela.

"Alis propriis volat"

Abstract

The demand to improve technologies, to make them smaller and more integrated, clashes with the difficulties of developing new processes that can improve devices and make them more competitive in the world scenario.

The devices that were studied in this thesis work are PIN diodes with low anode doping and were realized in collaboration with STMicroelectronics. They have been called LEIA (Low Efficiency Injection Anode) diodes. The realization of these diodes is preparatory to the realization of the future LEIA RC-IGBT (Reverse Contacting IGBT). The latter will be a device integrating the IGBT (Insulate Gate Bipolar Transistor) and the freewheeling diode in the same die. The field of application for this device is motor-control, so it will be placed inside the power modules of three-phase motors. This type of application requires fast switching, hence the need for a fast diode. Typically, to make a diode fast, lifetime killing techniques are used, like diffusion (platinum or gold), irradiation (β or γ) and implantation (α or proton). However, these techniques deteriorate the performance of the IGBT, as they increase conduction losses, making it a problem since, in the RC-IGBT, the diode and IGBT are on the same die. Using the LEIA technique, the diodes were speeded up by lowering the body (anode) dose and using a lifetime killing technique with low doses, so β electron irradiation was chosen. It was decided to use it because it did not have a negative temperature coefficient, as it would lead to a decrease in conduction losses as temperature increases, which would be a problem in the case of devices connected in parallel, as the devices would be thermally coupled. This would be sufficient to cause the device with the lowest forward-voltage to go into thermal runaway.

The objective of this work is the comparison of diode prototypes with high

irradiation doses (10Mrad and 15Mrad) with LEIA diodes (low irradiation doses, 5Mrad, 2Mrad and 0.5Mrad). An important blocking point is the anode contact, because in the standard contact of an IGBT there is a TiTiN barrier, which is not compatible with the low doped anode because it forms a Schottky barrier. To avoid this, the barrier was removed and the standard AlCu top metal was replaced with AlSi to avoid another problem (aluminum spikes).

To fulfil this task, 25 silicon wafers were reserved for splits in terms of irradiation doses and process flows. Irradiated wafers were split into two flow sequences to achieve two different lifetime profiles. In the first case, the irradiation was done after the laser annealing (which serves to activate the implants on the backside), in the second before, resulting in a non-uniform lifetime profile for the latter, and a uniform profile for the former.

Through the TCAD simulations performed using the Sentaurus, a model was implemented to simulate the defect caused by electron irradiation, performing static and dynamic simulations with different irradiation doses. Simulations of the IGBT characteristic at different irradiation doses were also carried out to estimate the increase in Vcesat caused by these.
This comparison was concluded through the measurements performed on the wafers between non-irradiated LEIA diodes and standard diodes with high irradiation doses (10Mrad and 15Mrad).

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Chapter 1

Introduction

1.1 Motivation

The demand to improve technologies, to make them smaller and more integrated, clashes with the difficulties of developing new processes, that can improve devices and make them more competitive in the world scenario. These observations led to the need to integrate the power transistor (IGBT) with its corresponding diode (freewheeling diode) in the same die. This prompted the creation of a hybrid structure, the RC-IGBT.

The aim of this work is to demonstrate the validity of a new concept. This concept is the LEIA (Low Efficiency Injection Anode), which is based on the idea that by lowering the anode dose of the diode, we can make it faster without resorting excessively to lifetime killing techniques, that can damage the performance of the IGBT [1].
This work is preparatory to the development of a future RC-IGBT (Reverse Conducting Insulate Gate Bipolar Transistor), which will be used for motor control applications.
The IGBT is a power transistor that requires a freewheeling diode for switching, to allow charges to recombine when the device is turned-off. Motor control applications require a fast diode for switching.

Typically, the diode can be speed up using lifetime killing techniques, such as diffusion (platinum or gold), irradiation (β or γ) or implantation (α or

protons) [2]. All these techniques create defects in the lattice, which allow the formation of recombination centres, that permit faster recombination of charges.
These techniques, however, deteriorate the performance of the IGBT, because they increase the $V_{CE_{sat}}$, conduction losses and leakage current of the device.

The goal of this work is to provide a comparison of diode prototypes accelerated using a high dose of electron irradiation β, with diode prototypes, which have been named LEIA diode prototypes, that have a very low dose of electron irradiation β, but with a low doped anode. This would allow us to make devices that integrate a fast diode, with a process which does not deteriorate the performance of the IGBT.

An important blocking point in this process is the anode contact. If we maintained the barrier, the contact would become Schottky, i.e. it would form a Schottky barrier. To avoid this, i.e. to have an ohmic contact, we have to remove the Ti/TiN barrier and we have to use $AlSi$ metal, because the typical $AlCu$ metal would generate aluminium spikes, which can deteriorate the diode [1].

To perform this comparison between diodes with the LEIA process and diodes with the standard process and high irradiation doses, measurements were carried out on prototypes to analyse their static and dynamic performance.

1.2 Thesis structure

This work is organized in these chapters:

- **Chapter 1** → this chapter introduces the motivation of this work;
- **Chapter 2** → this chapter provides an overview of the PIN diode, discussing its physical structure, characteristics and operation. This is important, since the diode on which this thesis work is based is a PIN diode;
- **Chapter 3** → this chapter gives an overview of the lifetime control techniques that allow us to make faster diodes. In particular, it will

talk about diffusion techniques (gold diffusion and platinum diffusion), irradiation techniques (β electron irradiation and γ irradiation) and implantation techniques (helium implantation and proton implantation);

- **Chapter 4** → this chapter gives an overview of some fast PIN diodes;
- **Chapter 5** → this chapter provides an overview of the IGBT device, its physical structure, characteristics and operation. It is important because this work is preparatory to the realisation of the RC-IGBT, the IGBT with integrated diode;
- **Chapter 6** → this chapter explains the concept of the new LEIA RC-IGBT, the proposed structure, the LEIA concept, and the improvement it can provide to the IGBT and diode trade-off;
- **Chapter 7** → this chapter explains the DOEs done on the LEIA diode, comparing them with previous DOEs on accelerated diodes using electron irradiation [1];
- **Chapter 8** → this chapter presents a summary of the conclusions and considerations of the results obtained and new trials to be carried out in the future.

Chapter 2

PIN Diodes

PIN diodes are a kind of diodes, that possess a middle region with a much lower doping concentration than the outer regions p and n. This type of device has the advantage of having the on-resistance R_{on} strongly reduced by high-level injection into the base region. This phenomenon is known as "conductivity modulation".
PIN diodes are widely used in power applications, especially as freewheeling diodes. The "i" in the name stands for intrinsic but is used improperly, because the base middle region is not intrinsic. In order to have an intrinsic semiconductor, the doping should be in the range of $< 10^{10} cm^{-3}$, but achieving the latter is very difficult.
Power PIN diodes usually have a $p^+n^-n^+$ structure, so the so-called "i" region is an n^- region, which is several orders of magnitude lower than the doping of the outer regions.

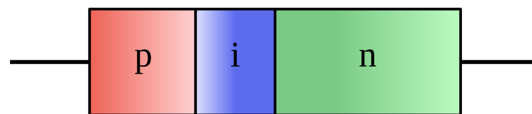

Figure 2.1: PIN diode structure [3]

In terms of applications, PIN power diodes can be distinguished into two main types [4]:

- **Rectifier diode** $\rightarrow$ for applications in which you have a frequency of about $(50-60)Hz$, where there is a high carrier lifetime in the middle

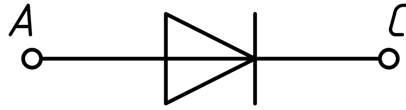

Figure 2.2: PIN diode electronic symbol [3]

region;

- **Fast recovery diodes** $\rightarrow$ (also called Fast recovery rectifier diodes) used as freewheeling diodes for switching devices with frequencies up to $20kHz$ and in switch-mode power supplies from $(50-100)kHz$ and above. In this case, the carrier lifetime in the middle region must be very low.

2.1 PIN diodes structure

Considering the technology and doping profile, PIN diodes can be classified into two types [4]:

- **Epitaxial diode**;
- **Diffused diode**.

The typical structure is $p^+n^-n^+$.
As can be observed in Figure 2.3(a), in the epitaxial diode, we have a very small base width w_B. The n^- layer is deposited by epitaxial growth on a highly doped n^+ substrate. By creating recombination centres, using lifetime killing techniques, such as gold or platinum diffusion, we can realize very fast diodes. Since w_B is very small, the voltage drop across the middle layer is low. For this reason, epitaxial diodes are used in applications requiring medium voltages between $(100-600)V$ [4].
In Figure 2.3(b) we can see the diffused diode, which can be used for high voltage applications of around $1200V$ or more. They are usually manufactured by diffusion. The diffused diode is fabricated from a low-doped n^- wafer, in which the layers p^+ and n^+ are created by diffusion. The thickness of the w_B layer depends on the diffusion profile. In this case, we must have a thick w_B. If we increase the depth of layers p^+ and n^+, we can increase the thickness of the wafer, but deep layers p have disadvantages regarding the reverse recovery behaviour of the diode.

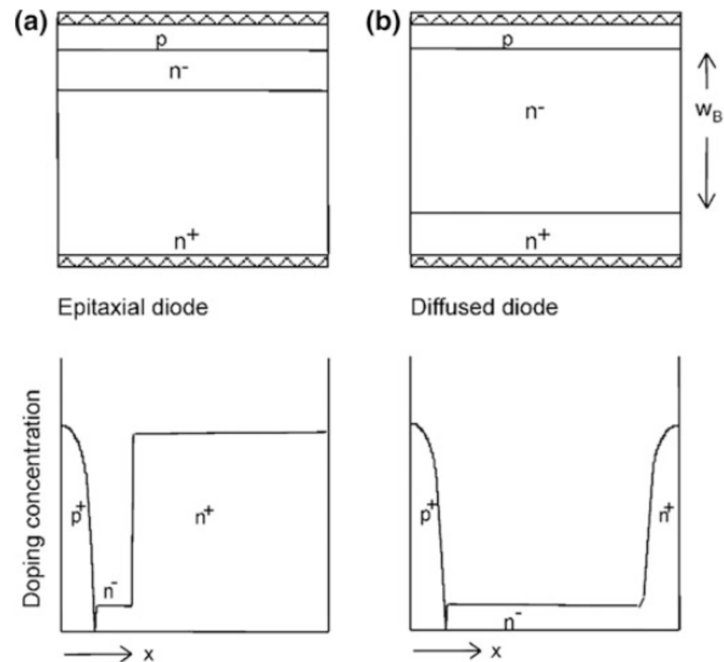

Figure 2.3: Structure of PIN diodes (a)Epitaxial diode (b)Diffused diode [4]

In general, the regions p and n are strongly doped, because we need an ohmic contact. In an ohmic contact, the resistance is negligible, regardless of the polarity of the voltage [4].

2.2 I-V characteristic

The I-V characteristic of a PIN diode is different from the ideal diode (Figure 2.4) [5]. When the diode is forward biased, the equivalent circuit consists of an inductor and a resistor in series (Figure 2.5), while, when it is reverse biased, the equivalent circuit consists of a capacitance and a resistor in parallel (Figure 2.6).

The difference between the PIN diode and the PN diode remains in the series resistance [6]. When we increase the forward bias, the minority carriers increase in the p and n layers. The intrinsic layer is flooded with electrons and holes and this triggers the conductivity modulation phenomenon, i.e. the resistivity of the intrinsic layer becomes dependent on the applied bias.

The thickness of the intrinsic layer also affects the I-V characteristic of the

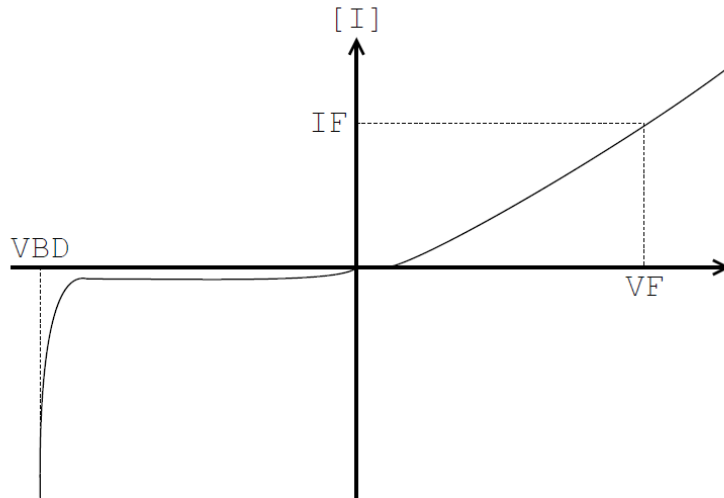

Figure 2.4: Example of I-V curve of a PIN diode, in which V_{BD} is the breakdown voltage and V_F and I_F is the forward voltage and current [5]

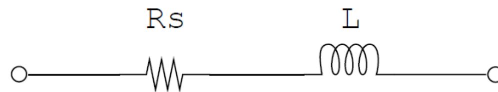

Figure 2.5: PIN diode equivalent structure in forward bias [5]

PIN diode[7]. The parameters that mainly affect the diode characteristic are the density of the minority carrier, the thickness of the intrinsic layer, the minority diffusion length and the generation-recombination current.

As can be seen in Figure 2.7, there is a dependence of the I-V characteristic on the thickness of the intrinsic layer. The higher the thickness, the lower the current at the same voltage. The forward current is inversely proportional to the intrinsic layer thickness [7].

2.3 Physical parameters

The important parameters involved in the conduction of the PIN diode are the forward current I_F, the forward voltage V_F, the breakdown voltage V_{BD}, the junction voltage V_J and the junction capacitance C_J. The main physical parameters for the design of a PIN diode are the resistivity of the intrinsic

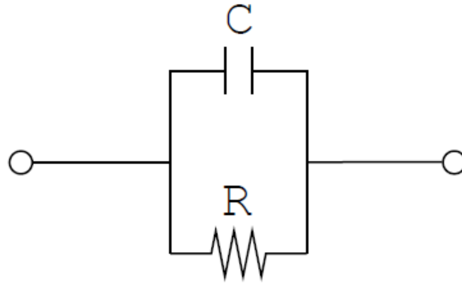

Figure 2.6: PIN diode equivalent structure in reverse bias [5]

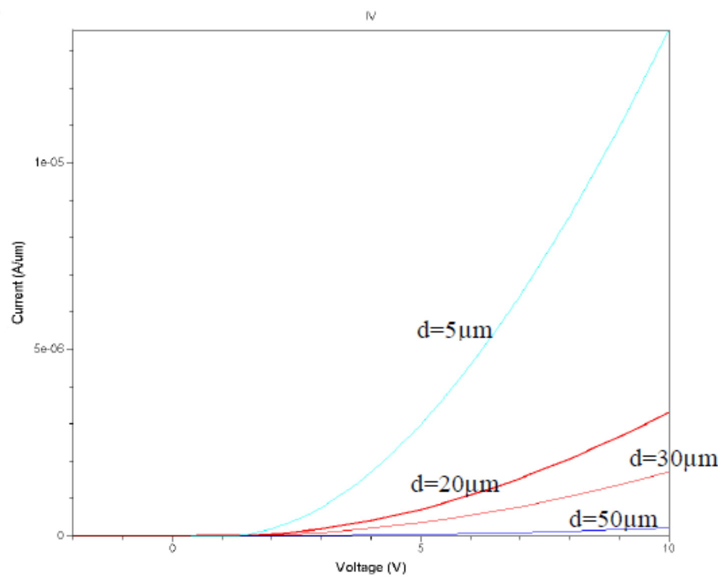

Figure 2.7: I-V characteristic at different intrinsic layer thickness [7]

layer ρ, the width of the intrinsic layer w_B, the junction area A_J and the carrier lifetime τ [5].

2.3.1 Intrinsic layer resistivity

The resistivity of the intrinsic layer depends on the doping concentration. A low resistivity of a heavily doped layer results in a fast diode with a low capacitance, but with some conduction loss. Conversely, if the resistivity is high, the capacitance is large, the conduction loss is lower and the diode is

slower [5].

2.3.2 Intrinsic layer width

This parameter has a significant impact on the behaviour of the diode. A thin intrinsic layer produces low forward resistance with a fast diode. In contrast, thicker intrinsic layers produce slower devices with lower junction capacitance and better power handling capabilities [5].

2.3.3 Junction area

A PIN diode with an intrinsically depleted region is essentially a capacitor. The junction area affects the capacitance of the device. A small junction area produces high-speed devices with low capacitance, high forward resistance, high conduction loss and low power handling capability. Conversely, a larger junction area produces a slower device with higher capacitance, lower forward resistance, lower conduction loss and better power handling capability [5].

2.3.4 Carrier lifetime

The carrier lifetime is the average time it takes for minority carriers to recombine. The carrier lifetime affects the speed of the device. A longer carrier lifetime slows down the switching speed. Conversely, a shorter carrier lifetime produces diodes that are faster [5].

2.4 Forward bias

2.4.1 Carrier density distribution

When a positive voltage is applied to the PIN junction, the intrinsic base region is flooded with carriers injected from the highly doped outer regions p and n. This reduces the forward resistance of the diode, which behaves as a variable resistance.

In the neutrality condition, the spatial charge density is as follows:

$$\rho_s = N_D - N_A + p - n = 0 \tag{2.1}$$

In the region n the concentration of acceptors is zero ($N_A = 0$), and thus:

$$n = p + N_D \tag{2.2}$$

Since the doping in the n^- region is very low, the donor concentration can be neglected ($N_D \approx 0$):

$$n(x) \approx p(x) \tag{2.3}$$

In order to calculate the carrier density distribution, we start from the transport equations [4]. For each carrier, the total current has two contributions, the drift current and the diffusion current:

$$J_p = J_{p_{drift}} + J_{p_{diff}} = q\mu_p p\varepsilon - qD_p\frac{dp}{dx} \tag{2.4}$$

$$J_n = J_{n_{drift}} + J_{n_{diff}} = q\mu_n n\varepsilon + qD_n\frac{dn}{dx} \tag{2.5}$$

The total current density is the follow, considering the approximation due in Equation 2.3:

$$J = J_n + J_p = q(\mu_n + \mu_p)p\varepsilon + q(D_n - D_p)\frac{dp}{dx} \tag{2.6}$$

we can write the electric field in this way:

$$\varepsilon = \frac{\frac{J}{q} - (D_n - D_p)\frac{dp}{dx}}{(\mu_n + \mu_p)p} \tag{2.7}$$

The carrier density current becomes:

$$J_p = \frac{\mu_p}{\mu_n + \mu_p}J - qD_A\frac{dp}{dx} \tag{2.8}$$

$$J_n = \frac{\mu_n}{\mu_n + \mu_p}J + qD_A\frac{dp}{dx} \tag{2.9}$$

where

$$D_A = 2\frac{D_n D_p}{D_n + D_p} \tag{2.10}$$

We start from the continuity equation:

$$\frac{dJ_p}{dx} = -qR = -q\frac{p}{\tau_{SRH}} \tag{2.11}$$

where R is the recombination rate and τ_{SRH} is the SRH lifetime.
According to the Shockley Read-Hall model, the lifetime depends on the level of injection, where in high-level injection the $\tau_{SRH} = \tau_{HL}$ [8].
Thus, defining the ambipolar diffusion length:

$$L_A = \sqrt{D_A \tau_{HL}} \tag{2.12}$$

and after some algebraic calculation, we can obtain the carriers density distribution in the base:

$$p(x) = \frac{p_R \sinh\frac{x}{L_A} + p_L \sinh\frac{w_B - x}{L_A}}{\sinh\frac{w_B}{L_A}} \tag{2.13}$$

where p_R and p_L are the concentrations on the left and right edges of the base region, respectively. The electron carrier density is the same, considering Equation 2.3 [4].

2.4.2 Junction voltage and Drift voltage

PIN devices have two space charge regions in the junction p^+n^- and in the doping step n^-n^+ connected to two different built-in voltages $V_{bi}(p^+n^-)$ and $V_{bi}(n^-n^+)$. When we apply the forward voltage V_F, we reduce the potential steps and increase the carrier density injected into the base region. The forward voltage provides an ohmic voltage drop V_{drift} on the weakly doped base region, which is necessary for current transport. The voltage in the outer parts of the diode is called $V_J(p^+n^-)$ on the p side and $V_J(n^-n^+)$ on the n side. The forward voltage is [4]:

$$V_F = V_J(p^+n^-) + V_{drift} + V_J(n^-n^+) \tag{2.14}$$

According to the Boltzmann equation and the mass action law, the junction voltage is as follows:

$$V_J = V_J(p^+n^-) + V_J(n^-n^+) = \frac{kT}{q} \ln \frac{p_L p_R}{n_i^2} \tag{2.15}$$

Another parameter related to the junction voltage is the junction capacitance, which depends on the electrical and geometrical properties of the device [5], in this way:

$$C_J = \frac{\varepsilon A}{w_B} \tag{2.16}$$

where A is the cross-sectional area.

The drift voltage V_{drift}, i.e. the voltage across the middle region, is calculated by integrating the electric field Equation 2.7 [4]:

$$V_{drift} = \frac{J}{q(\mu_n + \mu_p)} \int_0^{w_B} \frac{dx}{p(x)} \tag{2.17}$$

If $p(x) = const$, the result of the integral is $\frac{w_B}{p}$. For the inhomogeneous case, we can replace p by its average value $\bar{p}$:

$$V_{drift} = \frac{J}{q(\mu_n + \mu_p)} \frac{w_B}{\bar{p}} \tag{2.18}$$

considering the stored charge:

$$Q_F = qAw_B\bar{p} \tag{2.19}$$

the V_{drift} can be rewritten in this way:

$$V_{drift} = \frac{I_F w_B^2}{(\mu_n + \mu_p)Q_F} \tag{2.20}$$

where $I_F = JA$ represents the forward current. Finally, from Equation 2.20, we can find the forward/series resistance:

$$R_F = \frac{w_b^2}{(\mu_n + \mu_p)Q_F} \tag{2.21}$$

and the stored charge:

$$Q_F = \frac{I_F w_B^2}{V_{drift}(\mu_n + \mu_p)} \tag{2.22}$$

2.5 Reverse bias

When the PIN diode is reverse biased, there is almost no free charge in the intrinsic region. In reverse, the PIN diode behaves as an almost constant capacitance, as can be seen in Figure 2.6. In reverse polarisation, an important parameter is the breakdown voltage V_{BD}. The breakdown voltage is defined as the maximum voltage that can be applied to the PIN diode without it failing. Since there is almost no free charge in the intrinsic region, the electric field is constant, and the breakdown voltage is determined by the breakdown field E_{BD} and the width of the intrinsic region w_B in this way [5]:

$$V_{BD} = E_{BD} w_B \tag{2.23}$$

Exceeding the breakdown voltage can cause permanent damage to the intrinsic layer the device.
The breakdown voltage is related to the width of the intrinsic layer w_B and the doping of this region [9].

As we can observe in Figure 2.8, the breakdown increases when the width of the intrinsic layer w_B increases. In fact, by increasing w_B, it is possible to harden the device.

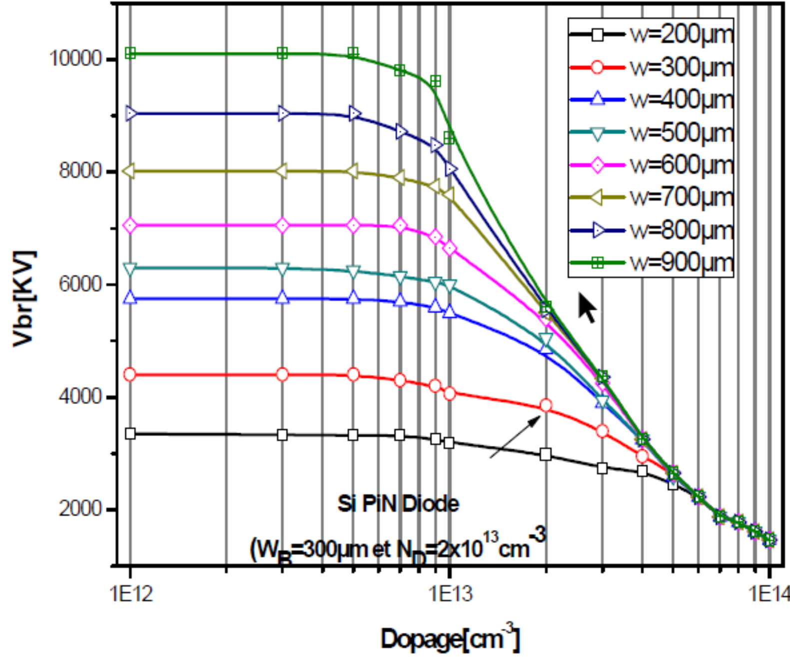

Figure 2.8: Breakdown voltage in function of the doping in silicon PIN diode [9]

2.6 Trade-off curve

The trade-off curve, especially for fast diodes, is very important in terms of stored charge and low forward voltage for fast switching. In Figure 2.10, we can see a typical trade-off curve for a PIN diode, where we have the stored charge Q_F/Q_{RR}, also known as the reverse recovery charge, on the y-axis and the forward voltage V_F on the x-axis.

As we can see, the trade-off curve has a hyperbolic trend. This relation for the trade-off curve is typical for many technologies and is an important evaluation criterion for a specific design. If we consider the Equation 2.22 and the Equation 2.20, w_b of the intrinsic layer has a squared contribution to both Q_F and V_F. Therefore, w_B must be as low as possible if we want to have a fast diode [4].

In order to have a faster device, we must have as small a reverse recovery charge Q_{rr} as possible. This is because, when the PIN diode is to be

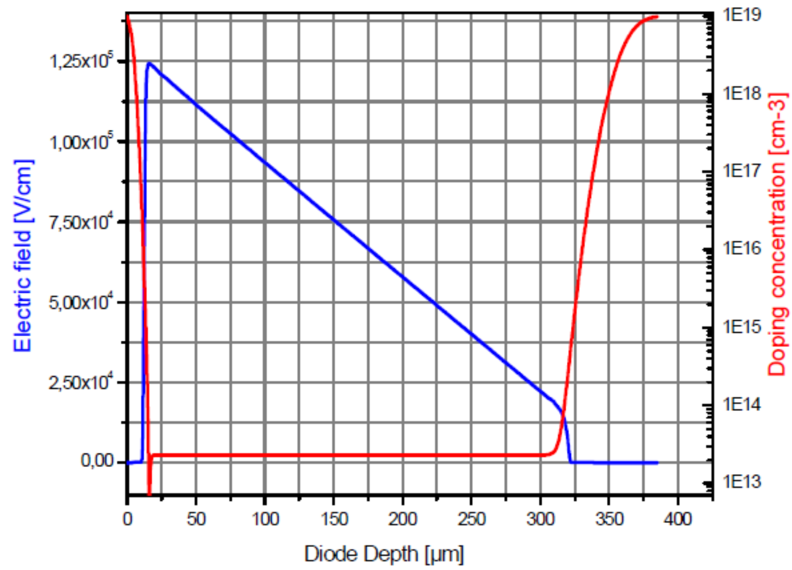

Figure 2.9: Electrical field repartition inside the silicon PIN diode structure corresponding to its breakdown voltage [9]

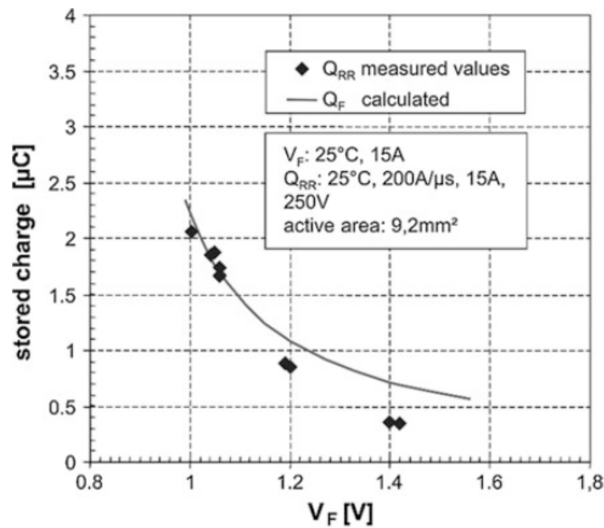

Figure 2.10: Pin diode trade-off curve [4]

used in applications as a freewheeling diode in parallel with an IGBT, the smaller the Q_{rr}, the faster the switching. Clearly, this leads to a higher forward voltage V_F. This is the reason why a good trade-off must be found according to the application of the device.

2.7 Switching behaviour

The switching on and off of power diodes, particularly in terms of reverse recovery, is a topic that requires special attention. The diode is usually used as a freewheeling diode coupled to an IGBT, since when the IGBT turns-off, the diode intervenes to prevent the device from being damaged. During the transition from the blocking state to the conducting state, the diode is accompanied by an anode overvoltage peak, also called forward recovery maximum voltage V_{FRM}. During the transition from the conduction state to the blocking state, the stored charge must be extracted before a high voltage reaches the drift region, which brings a resulting large reverse current, called the reverse recovery current I_{rr} [10]. When a PIN diode switches from conduction state to blocking state, the drift region must extract the free carriers in order to form a depletion region that can withstand high voltages. In the case of an inductive load, the diode current does not immediately drop to zero, but there is a soft-recovery (Figure 2.13).

2.7.1 Turn-on characteristic

In Figure 2.11 we can observe the turn-on characteristic behavior of power diodes.

The voltage first increases to the peak of the turn-on voltage V_{FRM}, before droping down to the forward voltage. In the plot, we can see the turn-on time t_{fr}, which is the sum of t_{rise} (rise time) and t_{fall} (fall time), defined as the time interval between the instant of the forward voltage of 10% and the instant when the voltage has dropped down to 1.1 times the steady-state forward voltage.
The peak forward recovery voltage V_{FRM} is an important parameter for the design of freewheeling diodes. These are used when the IGBT is turn-off. In this case, the diode is turn-on. The dI/dt on turn-off the IGBT creates a voltage peak on the parasitic inductance which is superimposed by V_{FRM}. The sum of both components can lead to a critical voltage peak [4].

In order to obtain a soft recovery behaviour at turn-off, we can design a very wide w_B. Conversely, to obtain a fast recovery diode, w_B must be reduced. If we compare the V_{FRM} of a wide or narrow w_B region, we can see that, in the former case, the V_{FRM} is lower than in the latter case. In fact,

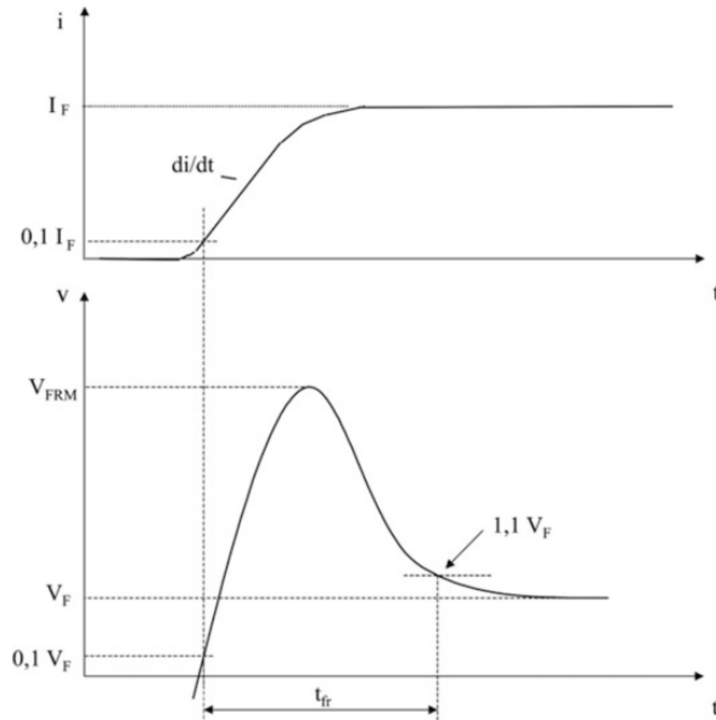

Figure 2.11: Characteristic parameters of the turn-on behavior of the power diodes [4]

analytically, the V_{FRM} has the following form:

$$V_{FRM} = \frac{w_B J}{q \mu_n N_D} \tag{2.24}$$

This equation can be used to design the diode, because to increase the V_{FRM}, we can decrease the doping N_D or/and increase the base width w_B.

2.7.2 Reverse recovery

The process that occurs when the polarisation of a PIN diode is changed from forward to reverse is called "reverse recovery" of the diode. The initial condition is a PIN diode with a forward bias current. In this case, the intrinsic region is filled with a charge proportional to the forward bias current I_F and the carrier lifetime τ. The bias is changed by applying a negative bias voltage to the PIN diode. The negative bias creates a reverse current which depletes the PIN diode of stored charge. At the beginning of this

process there is a lot of free charge in the intrinsic region and the charge is quickly withdrawn. As the charge is removed, the resistance increases and the current decreases. The main parameter for the charge withdrawal process is the carrier lifetime τ, and if it is several microseconds, this can be a problem for high voltage diodes that require fast switching.

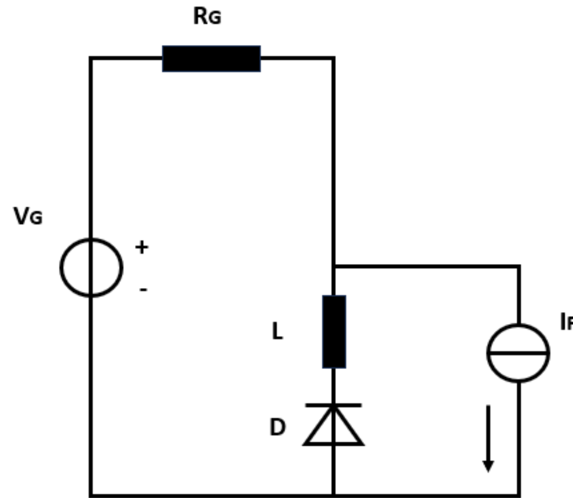

Figure 2.12: Circuit for characterising reverse recovery behavior

The simplest circuit for measuring the reverse recovery of a diode is found in Figure 2.12. It is an ideal circuit, I_F an ideal current source, V_G an ideal voltage source, R_G the generator resistance, L the parasitic inductor and D the diode we have to consider. The progression of current and voltage occurs at the diode and the circuit can be described by the following equation [4]:

$$L\frac{di}{dt} + v(t) = -V_G \tag{2.25}$$

where $v(t)$ is the time dependent voltage on the diode.
In Figure 2.13 we can see the waveforms of the current and voltage during reverse recovery of the diode.

When the current decreases, $v(t)$ can be neglected. In this case, the slope of the current at the time of commutation can be determined by the voltage inductance:

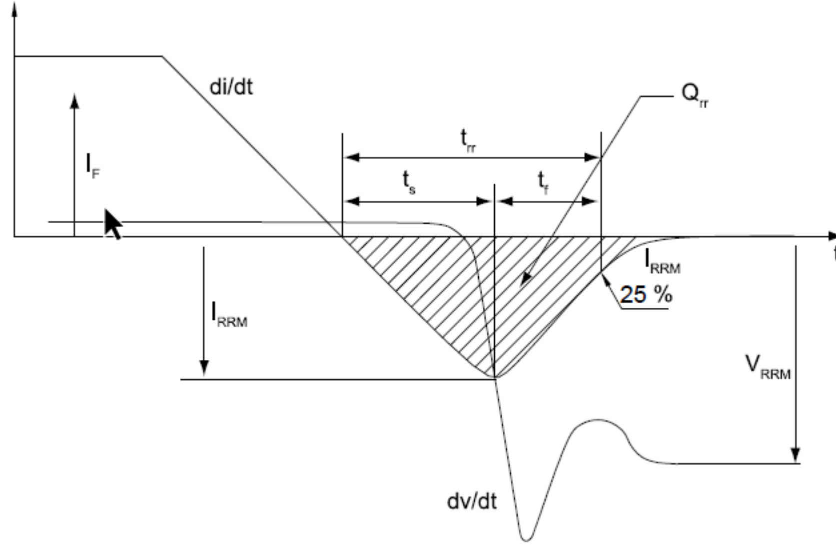

Figure 2.13: Waveforms of current and voltage, for a soft recovery diode, during the reverse recovery process [4]

$$-\frac{di}{dt} = \frac{V_G}{L} \tag{2.26}$$

2.7.3 Turn-off power losses

Another parameter to be taken into account for the reverse recovery is the power loss in terms of turn-off energy E_{off} [4]:

$$E_{off} = \int_{t_s+t_f} v(t)i(t)dt \tag{2.27}$$

where t_s and t_f are the "soaring/rising time" and "falling time", respectively.

We assume that the voltage v is null for the time t_s, until the current crosses zero. During t_f:

$$i_r(t) = I_{RRM} + \frac{I_{RRM}}{t_f}t \tag{2.28}$$

where I_{RRM} is the reverse recovery peak current.

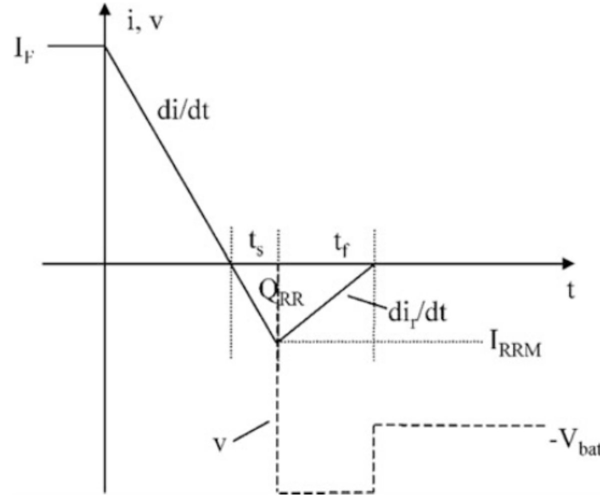

Figure 2.14: Simplified waveform for PIN diode reverse recovery [4]

$$v = -V_G - L\frac{di_r}{dt} = -V_G - L\frac{I_{RRM}}{t_f} = const \tag{2.29}$$

Substituting Equation 2.28 and Equation 2.29 into Equation 2.27 and integrating, we obtain:

$$E_{off} = \frac{1}{2}LI_{RRM}^2 + \frac{1}{2}V_G I_{RRM} t_f \tag{2.30}$$

We can write L in this way:

$$L = -\frac{V_G}{di/dt} = \frac{V_G}{I_{RRM}/t_s} \tag{2.31}$$

and thus,

$$E_{off} = \frac{1}{2}V_G I_{RRM} t_s + \frac{1}{2}V_G I_{RRM} t_f = \frac{1}{2}V_G I_{RRM} t_{rr} = Q_{RR} V_G \tag{2.32}$$

We can see that the turn-off losses are directly proportional to the reverse recovery charge Q_{rr}. This is an important consideration for this work, because it means that, in order to maintain the turn-off losses low, one must have a Q_{rr} as low as possible.

2.8 Softness

The reverse recovery time t_{rr} is defined as the sum of $t_{rr} = t_s + t_f$, the time from t_0 to the point where the current has decayed to 25% of the value of I_{RRM}. Linked to the reverse recovery time, we can define an important parameter called "Softness" in this way:

$$s = \frac{t_f}{t_s} \tag{2.33}$$

the ratio between the fall time and the rise time. If we want to define better the softness factor, we can use the following definition [4]:

$$s = \left| \frac{-\frac{di}{dt}\big|_{i=0}}{\frac{di_r}{dt}\big|_{max}} \right| \tag{2.34}$$

If the softness factor is less than unity $s < 1$, it is called a soft-recovery diode, while if $s > 1$, it is called a fast-recovery or snappy-recovery diode. This parameter helps us in the design of the diode. If we have to make a soft diode, we have to maintain s low; on the contrary, we have to raise it as high as possible. For this work, it is important to achieve a high softness factor, because for the applications in which our diode will be inserted, it is important that it switches as fast as possible.

Chapter 3

Lifetime Killing for Fast Commutation

In applications requiring a fast commutation, such as motor control, we need to speed up our devices. During the reverse recovery process, the charge stored within the device is removed, and in order to speed up devices, we can follow two ways: to lower the injection efficiency of the device or to use a lifetime killing technique. There are several lifetime killing techniques. The concept is to generate defects in the crystal lattice, for creating recombination centres that allow faster charge recombination during switching.
In this work, it is important to know the different lifetime killing techniques for speeding up PIN diodes. The main techniques are:

- gold and platinum diffusion;
- β^- and γ irradiation;
- α and H^+ implantation.

These techniques allow for lifetime control, but have a negative impact on the devices, as they increase device conduction losses and leakage current. Before going into the specifics of these techniques some background is necessary. In particular, it is necessary to talk about lifetime. The concept of lifetime is linked to the concepts of generation and recombination rate. When the device is at equilibrium, carriers are continuously generated thermally. There is a generation rate that is equal to the recombination rate.

During operation, there is non-equilibrium. A state of non-equilibrium tends to restore equilibrium. The time it takes for carriers to recombine is called the "Lifetime". The total lifetime is the combination of several recombination mechanisms.

3.1 Lifetime and recombination centres position

The expression of the carrier lifetime is different according on the position of the recombination centres [11]. It is possible to divide them into four typologies:

- **Shockley-Read-Hall lifetime** (τ_{SRH}) $\rightarrow$ obtained from deep level recombination. It is expressed by the Shockley-Read-Hall statistic;

- **Low-level lifetime** (τ_{LL}) $\rightarrow$ in the case of low-level injection, this is the simplification of the Shockley-Read-Hall lifetime;

- **High-level lifetime** (τ_{HL}) $\rightarrow$ as in the case of the PIN diode, when there is a high-level of injection. The high-level lifetime does not depend directly on the position of the recombination centres, but on the traps concentration and the capture coefficient. As we will see in the following chapters, this will be useful in the model developed for our diode;

- **Space charge lifetime** (τ_{SC}) $\rightarrow$ this parameter depends on the fact that the position of the recombination centres also influences the lifetime in the space charge regions.

The position of the recombination centres has a strong influence on the carrier lifetime. It also depends on the temperature. If we call, in n-type semiconductor, the position of the recombination centre n_1, its expression becomes:

$$n_1 = n_i e^{\frac{E_T - E_I}{k_B T}} \tag{3.1}$$

3.2 Radiative and non-radiative recombination

Recombination mechanisms can be

- Radiative;
- Non-radiative.

3.2.1 Radiative recombination

Band-to-band radiative recombination is a direct recombination of an electron and a hole. Direct band-to-band recombination is only possible in materials with extremely low defect concentrations, because the strain field in the crystal structure alters the distance and strength of interatomic interactions [12]. In radiative recombination there is a release of energy in the form of photons. In simple statistics, the net rate of recombination is [4]:

$$R = B(np - n_i^2) \tag{3.2}$$

In which the B is the recombination probability.

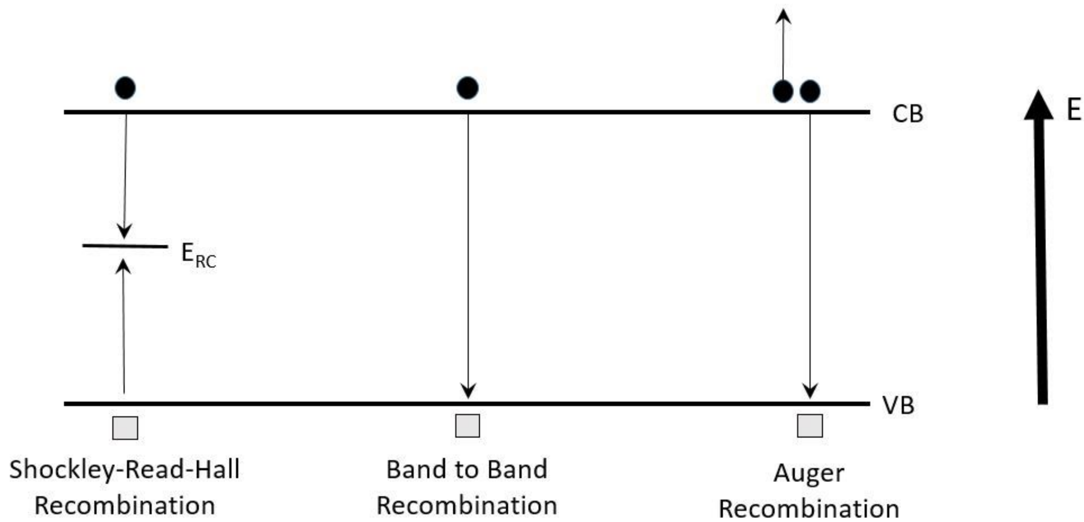

Figure 3.1: Recombination mechanisms [12]

3.2.2 Non-radiative recombination

In this case, the two main recombination mechanisms are Shockley-Read-Hall (SRH) and Auger recombination. SRH recombination occurs when intermediate energy levels are introduced into the band gap of a material, through defects in the crystal structure. When an electron or hole is trapped in an energy level close the conduction or valence band, respectively, the carrier is said to be trapped. In an electron trap, the energy required for an electron to occupy its energy level is significantly higher than the probability of a hole occupying that level, and vice versa. Trapped carriers cannot recombine and eventually return to their initial state. High carrier trap concentrations reduce carrier mobility, which in turn reduces the recombination rate. If the energy level is in the middle of the band gap, this energy level allows SRH recombination, also known as defect-level recombination. As a result, the energy difference between the initial and final electron energies is smaller, resulting in less energy being released during recombination. This energy is often in the form of thermal oscillations known as phonons, and heating occurs when these phonons are absorbed by the material. This heating occurs at defect sites within the material and can be extremely detrimental to the device efficiency, because the phonon concentration reduces electron mobility and the thermal energy increases the strain regions within the material [12].

Another recombination mechanism is Auger recombination. In this case, the energy released during recombination is not transferred to a third electron or hole carriers [12]. The recombination probability B can be replaced by a term proportional to the carriers concentration. The following equation represents the Auger recombination rate [4]:

$$R_A = (c_{A,n}n + c_{A,p}p)(np - n_i^2) \tag{3.3}$$

The two coefficients $c_{A,n}$ and $c_{A,p}$ determine the recombination rate for electrons and holes, respectively. In particular, Auger recombination is important in highly doped regions.

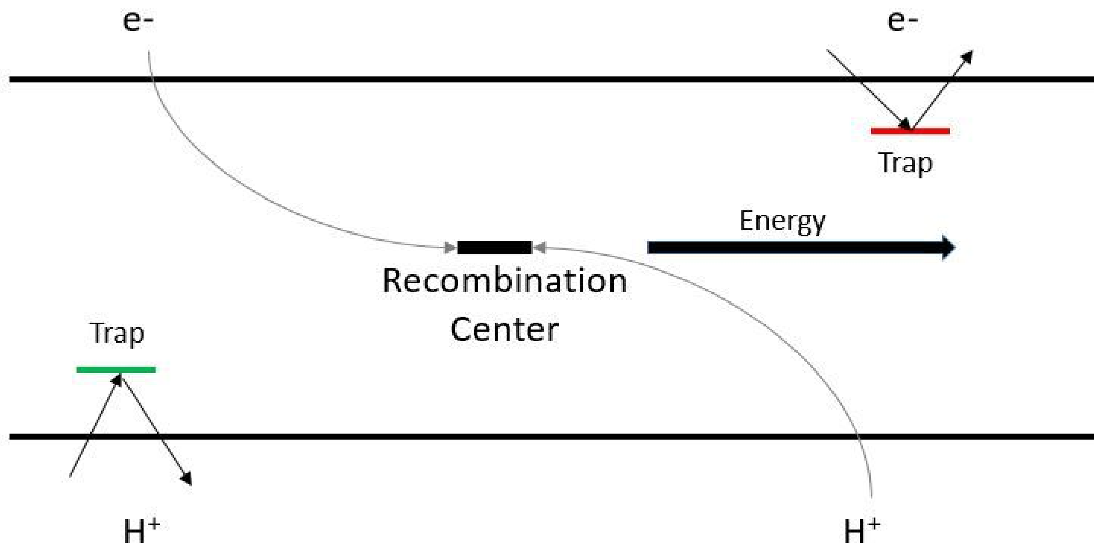

Figure 3.2: SRH recombination [12]

3.3 Gold & Platinum diffusion

The reduction of the carrier lifetime can be achieved by diffusing metallic impurities such as gold and platinum. These techniques permit local control of the lifetime over an extended area. The techniques used are thin film deposition with subsequent diffusion or implantation for both materials. These techniques introduce deep levels into the band gap that act as recombination centres, which allows for a reduction in the reverse recovery time t_{rr}, the turn-off time during which minority carriers escape from the n^- region. This occurs because the reverse recovery charge Q_{rr} is reduced. Q_{rr} is the integral of the reverse current flowing inside the diode in a time equal to t_{rr}. Considering the trade-off curve, a reduction in the reverse recovery charge corresponds to an increase in the on-resistance R_{on} and, if an IGBT is considered, an increase in $V_{CE_{sat}}$ [13]. For this reason, it is important to find a compromise.

3.3.1 Gold diffusion

The diffusion of gold into silicon introduces acceptor and donor levels into the band gap. The temperature dependencies of these gold levels are well known

from the literature [11]. The acceptor and donor energy levels are 0.54eV and 0.35eV, respectively. The acceptor level is very close to the intrinsic energy level and acts as a very effective generating centre but causes high leakage currents. Gold diffusion in freewheeling diodes generates high voltage peaks during turn-on. The gold profile after diffusion has a U-shape because gold has a higher solubility in areas of higher doping concentration [11].
Gold atoms can diffuse via interstitial lattice sites according to the following reaction, and occupy the vacancy [14]:

$$Au_i + V \leftrightarrow Au_s \tag{3.4}$$

Only the atoms on the substitutional lattice sites Au_s are electrically active and can be detected by spreading resistance measurements. This is called substitutional diffusion (Equation 3.4). This is not the only possible process, but self-interstitial diffusion (Equation 3.5) is also possible:

$$Au_i \leftrightarrow Au_s + I \tag{3.5}$$

The two models are reciprocal, but there are differences. The diffusion of A_i is faster than A_s.

The techniques used for the gold diffusion are the following: gold-plate and gold ion-implanted. The former consists of the deposition of a thin film of gold on the back-side of the wafer, before the metallisation step [13]. Typically, diffusion takes place in a dry nitrogen environment, in the temperature range $(850 - 900)°C$ for Au-plated samples and $970°C$ for implanted samples. The parameter that is modified is the R_{on}. The R_{on} is the sum of several terms:

$$R_{on} = R_{ch} + R_{acc} + R_J + R_{epy} \tag{3.6}$$

where R_{ch} is the channel resistance, R_{acc} is the resistance due to the excess negative charge accumulated in the n^- region below the gate, R_J is the junction resistance and R_{epy} is the resistance of the epitaxial layer. In the case of a high-voltage device, R_{epy} is approximately $75\% R_{on}$, and thus the other terms are negligible. The introduction of gold into the epitaxial layer

produces an increase in the resistivity of this layer due to compensation effects. The static characteristics worsen, but the reverse recovery charge Q_{rr} improves. The Q_{rr} depends mainly on the concentration of the recombination centres in the epitaxial layer and the R_{on} on the resistivity profile in the epitaxial layer [13].

There is a difference between the sample with gold-plate (thin film deposition) and the sample ion-implanted with gold. For the gold-plated sample, there is a strong depth dependence, and at the surface, the concentration is higher. This is because the surface concentration for an infinite source is fixed by the solubility of gold at the diffusion temperature. In order to avoid high compensation, we must maintain the temperature below $900°C$, because, at this temperature, there is a low diffusion coefficient that does not allow complete reconstruction.
For ion-implantation samples with gold, there is an uniform concentration profile of approximately $1.2x10^{14} atoms/cm^3$ calculated in this way [13]:

$$concentration = \frac{\phi}{d} \tag{3.7}$$

Where ϕ is the implanted fluence and d the wafer thickness. In this case, it is possible to perform high temperature diffusion process because you have a completely different implanted profile, but there is the same amount of gold in the epitaxial layer that permits to have the same Q_{rr} [13].
It is convenient to have a uniform concentration, because a higher concentration on the surface causes a large increase in resistivity.

As can be seen in Figure 3.3, the silicon resistivity remains constant for a low gold concentration and becomes abruptly high above certain values for gold-plate samples [13]. In gold-implanted devices, the resistivity value is constant along the thickness of the epitaxial layer and, in this case, the increase in R_{on} corresponds to the increase in R_{epy}. In gold-plate devices, the increase in R_{on} corresponds to the increase in both R_{epy} and R_{JF} [13].

3.3.2 Platinum diffusion

Platinum diffusion is more widely used than gold diffusion, considering a series of benefits. Platinum diffusion generates a pair of two defects, donor and acceptor, which act as effective recombination centres [11]. This is only

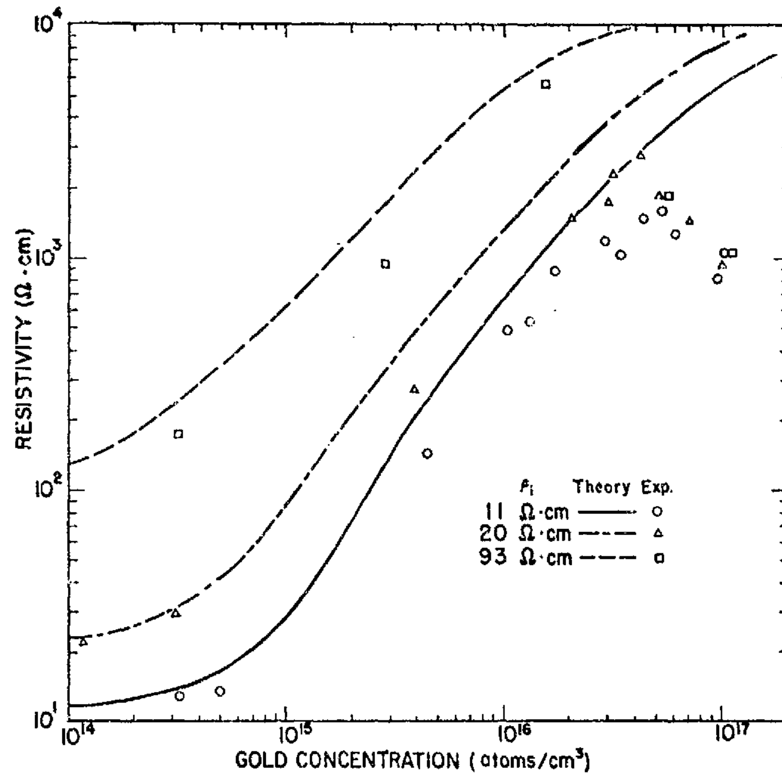

Figure 3.3: Silicon resistivity vs impurity concentration curves for gold in silicon at different substrate resistivity for gold-plate samples [15]

possible with high injection because, with low injection, platinum forms a small amount of recombination centres.
The advantages of using platinum include that: at a high diffusion temperature, platinum generates a low leakage current in the device, generates a lower device R_{on} than that generated by gold, and has a low peak voltage during the turn-on. One disadvantage, however, is that it generates devices with a negative temperature coefficient. This behaviour is very unfavourable for diodes connected in parallel because the parallel connection leads to attract more current to the diode with a lower voltage drop. Consequently, the temperature of the device would increase. This would further reduce the forward voltage, so that this diode would attract a further percentage of current, and so on. Therefore, a strong negative temperature dependence can lead to a thermal runaway of the diode [4].

The diffusion mechanisms are the same as for gold diffusion [16]:

$$Pt_i + V \leftrightarrow Pt_s \tag{3.8}$$

$$Pt_i \leftrightarrow Pt_s + I \tag{3.9}$$

$$I + V \leftrightarrow O \tag{3.10}$$

Pt_i stands for interstitial platinum, Pt_s for substitutional platinum, I for self-interstitial silicon, V for silicon vacancy and O for undistributed lattice silicon, respectively. To better explain these diffusion mechanisms, according to Equation 3.8 interstitial platinum goes to occupy vacancies in the lattice and generates substitutional platinum. According to Equation 3.9, substitutional platinum goes to occupy interstitial sites and generates interstitial platinum. The difference is that the vacancies are voids in the lattice and, instead, the interstitial sites are the sites in the lattice where impurity atoms can enter. The Figure 3.4 explains the concepts.

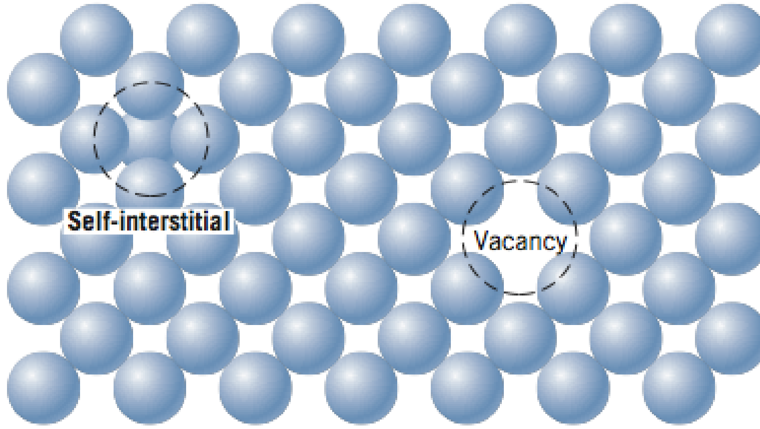

Figure 3.4: Vacancies and self-interstial sites

Platinum diffusion can be described by four partial differential equations [17]:

$$(1)\ \frac{\delta C_s}{\delta t} = k_{FT\rightarrow} C_i C_V - k_{FT\leftarrow} C_s + k_{KO\rightarrow} C_i - k_{KO\leftarrow} C_s C_I \tag{3.11}$$

$$(2)\ \frac{\delta C_i}{\delta t} = div(D_i grad C_i) - k_{FT\rightarrow} C_i C_V + k_{FT\leftarrow} C_s - k_{KO\rightarrow} C_i + k_{KO\leftarrow} C_s C_I \quad (3.12)$$

$$(3)\ \frac{\delta C_I}{\delta t} = div(D_I grad C_I) + k_{KO\rightarrow} C_i - k_{KO\leftarrow} C_s C_I - k_{IV\rightarrow} C_I C_V + k_{IV\leftarrow} \quad (3.13)$$

$$(4)\ \frac{\delta C_V}{\delta t} = div(D_V grad C_V) - k_{FT\rightarrow} C_i C_V + k_{FT\leftarrow} C_s - k_{IV\rightarrow} C_I C_V + k_{IV\leftarrow} \quad (3.14)$$

Parameters k are the reaction constants and FT indicates the Frank-Turnbull mechanism and KO the kick-out mechanism, while parameters C and D are used to indicate the concentrations and diffusion coefficients.
These differential equations are also valid for the diffusion of gold.

Interstitial platinum diffuses faster than substitutional platinum. The continuous exchange mechanism described in Equation 3.8 is called the Frank-Turnbull mechanism (an atom of impurity travels rapidly through the interstitial sites before reacting with a vacancy) and in Equation 3.9 it is the kick-out mechanism (atoms of interstitial impurities move rather fast by a direct interstitial mechanism, until they eventually displace a lattice atom) [16].
The typical temperature range for platinum diffusion is from $700°C$ to $950°C$. The Frank-Turnebull mechanism dominates below $850°C$ and the kick-out mechanism above $900°C$.
There are two possibilities: platinum can be implanted, or platinum silicide can be formed. The two processes are as follows (Figure 3.5).

If we consider the process of platinum diffusion on a PIN diode, for platinum implanted devices, the first step is to implant the platinum through the anode side and then perform a subsequent annealing to allow the platinum to diffuse. For platinum silicide, the platinum must be deposited on the anode side, using, for example, magnetron sputtering with argon. Then the wafer is sintered at $400°C$ for $60min$ and a layer of $PtSi$ is formed. The subsequent steps are the same. Usually, the device is annealed at $700°C$.

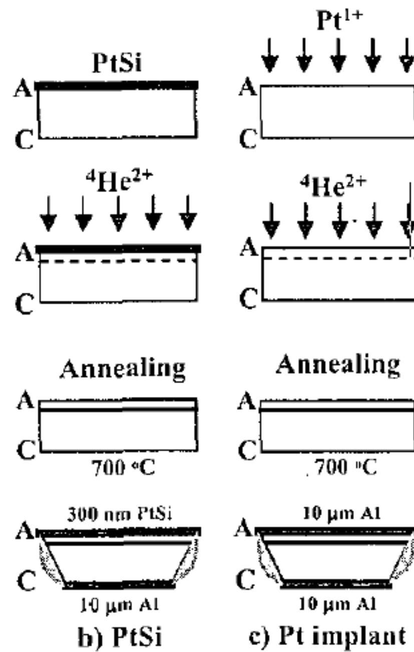

Figure 3.5: Platinum implantation vs platinum silicide [18]

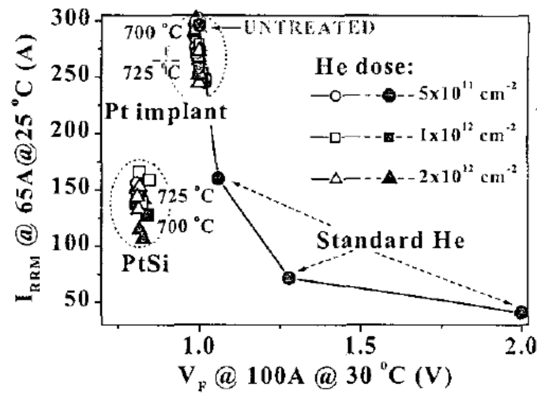

Figure 3.6: Trade-off between the forward voltage and current for PtSi and Pt implant [18]

As we can see in Figure 3.6, there is a better trade-off for platinum silicide. This is due to the thin anode contact *PtSi* formed with to respect to the standard aluminium contact, which allows us to have a more ohmic contact and lower conduction losses in the device.
In the Figure 3.5 and Figure 3.6, the platinum diffusion process is also

improved by using alpha implantation. This shows us that the techniques we will discuss in this work can be combined with each other.

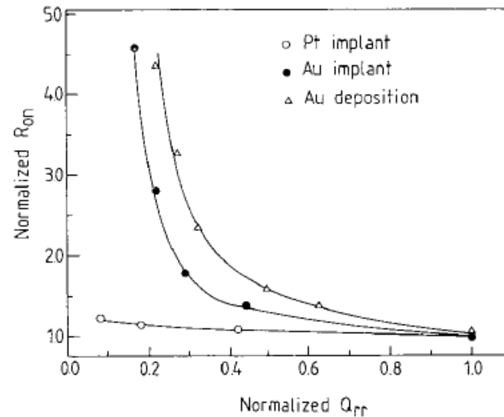

Figure 3.7: Comparison between Platinum and gold diffusion [13]

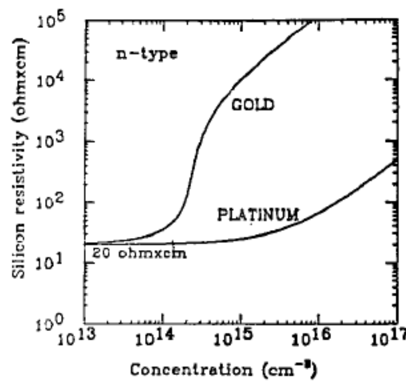

Figure 3.8: Silicon resistivity vs impurity concentration for gold and platinum diffusion [13]

The standard platinum diffusion process can be improved by using a lower doping level in the anode side [19]. We will use this concept in the LEIA diode, combining a low doped anode with electron irradiation [1].

A comparison of the two diffusion techniques treated is shown in Figure 3.7. The best compromise in platinum diffusion is visible. In platinum devices, it is possible to reduce Q_{rr} by a factor of 10 with a limited increase in R_{on}. This happens because the Q_{rr} depends on the concentration of the recombination centres in the epitaxial layer and the R_{on} on the resistivity profile,

which we can see in Figure 3.8.

3.4 β^- electron & γ irradiation

β^- electron irradiation and γ irradiation are other methods of generating recombination centres to speed up devices. The irradiation process is characterised by high precision and reproducibility. In addition, the irradiation technique offers the possibility of controlling the carrier lifetime at the end of the fabrication process, after the device has been metallised and passivated [4].

The β^- and γ irradiations generate Frenkel defects in the lattice. These consist of moving an atom in the lattice for creating a vacancy and, with the same atom, creating an interstitial defect Figure 3.9.

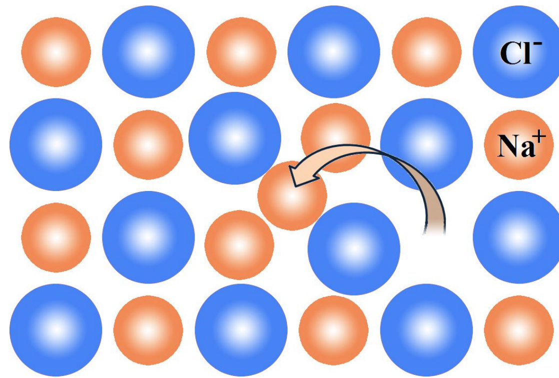

Figure 3.9: Frenkel defects

3.4.1 β^- electron irradiation

The β^- irradiation creates a homogeneous distribution of defects. This technique has an advantage in the constant distribution of the recombination centre with to respect the diffusion technique [4]. It does not allow localised lifetime control [2]. Irradiation increases the forward voltage drop [20]. The vacancy and interstitial atoms created by the collisions diffuse and form stable complexes with each other and with impurity atoms such as carbon, oxygen and phosphorus, which are also present in high-purity silicon. The irradiation process is followed by a mild annealing process to remove the thermally unstable centres and ensure the long-term stability

of the device's characteristics. The annealing process is also necessary to reduce the effects of further processing steps, such as soldering, that can alter the characteristics of the defects.
The possible sources of β^- irradiation are the two isotopes Pm-147 or Kr-85 [21]. These are radiative isotopes that release beta particles when they decay. When the promethium isotope decays, it forms a samarium atom and a beta particle, while when the krypton isotope decays, it forms a rubidium atom and a beta particle.
The beta spectrum of Pm-147 is characterised by a half-life of 2.62 years, a maximum particle energy of 230 keV and an average beta energy of 62.5 keV [21]. Only a small fraction of the emitted beta particles enter silicon with energies exceeding the irradiation damage threshold E_{th}. The beta spectrum of Kr-85 is characterised by a half-life of 10.756 years, a maximum particle energy of 670 keV and an average beta energy of 250 keV [21]. In this case, a much larger fraction of the spectrum is able to damage the silicon. The energy absorbed is so small that cooling is not necessary.

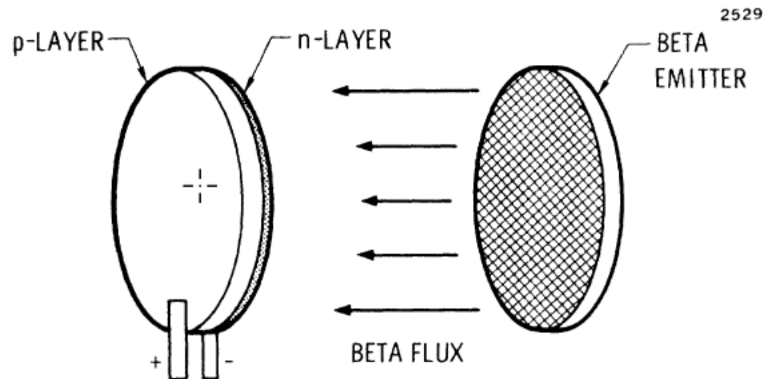

Figure 3.10: Beta irradiation setup with use of Pm-147 [21]

In Figure 3.10 we can see a typical configuration for beta irradiation with Pm-147. It consists of a Pm_2O_3 vapour deposited on tantalum substrates and subsequently, using the Faraday cup technique, in the generation of a beta flux on the device [21].
The Kr-85 system consists of beta gas sources coupled to silicon cells and assembled in one-inch lead-walled fixtures Figure 3.11.

In Figure 3.12 we can see that the absorption of beta particles produces electron-hole pairs.

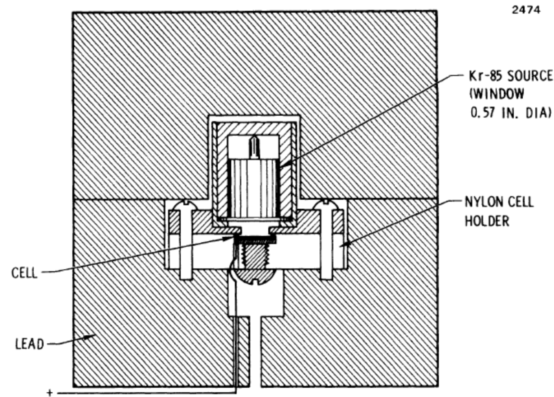

Figure 3.11: Beta irradiation setup with use of Kr-85 [21]

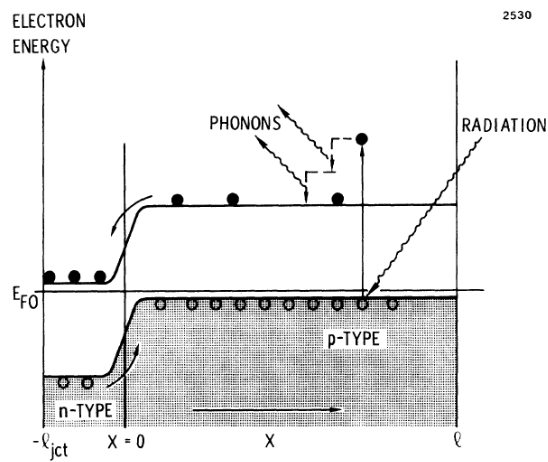

Figure 3.12: Beta irradiation [21]

Beta irradiation can be performed at room temperature or at higher temperature [20]. A device irradiated at elevated temperature shows a lower forward voltage drop than a device irradiated at room temperature. The energy levels introduced by electron irradiation cause an increase in the recombination rate and, as a result, the lifetime becomes [20]:

$$\frac{1}{\tau} = \frac{1}{\tau_0} + KD \tag{3.15}$$

where K is the irradiation efficiency factor and D is the irradiation dose.

3.4.2 γ irradiation

A typical source for γ irradiation is the Co-60 isotope [22]. It has a half-life of 5.27 years and an average energy of 1.33 MeV. It decays in nickel [23].
γ rays can be produced by atomic nuclei that, after emitting β rays, remain in an excited state that decays to the fundamental state. Another method of producing γ beams is by electron capture or the particle accelerator [24].

3.5 α & H^+ implantation

Another method used for lifetime control is the implantation of ionic species, such as hydrogen (proton implantation) and helium (alpha implantation) [25]. Ion implantation produces defects in the lattice that create recombination centres.

3.5.1 α implantation

The irradiated ions create damage that will be localised at the end of the projected range, which is determined by the chosen irradiation energy. The choice of irradiation dose is determined by the defect introduction rate. This increases with the size of the particle used. The implantation of alpha particles provides only vacancy-related defects, as opposed to protons [26].
This technique allows for localised lifetime control and stability until temperature of $T = 1200°$. This permits this technique to be used at any phase of the process [2].
Proton injection produces voids near the projected area. A subsequent thermal process evaporates the helium, forming an extremely stable microcavity. This introduces two levels into the silicon gap near the centre of the band, which act as recombination centres.
Helium is a noble gas. The solubility of noble gases in silicon is lower ($< 10^{16} atoms/cm^3$). If the ions exceed a specific value, they form voids. This value depends on the implantation energy, because it increases as the energy increases.
After thermal treatments, the helium is not stable and the trapped helium escapes from the surface. The formed microcavity can be considered as an individual particle that can collide with each other when in motion and collapse into a bigger microcavity [2].

3.5.2 Proton implantation

Proton irradiation has a large depth of penetration into silicon with a relatively small acceleration energy [27].

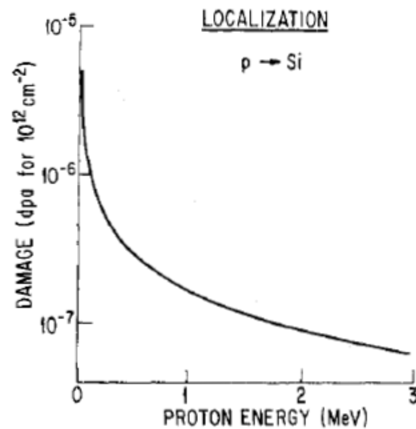

Figure 3.13: Damage curve for protons implanted into silicon [28]

As in the case of the helium implant, we do not have a homogeneous damage profile. A typical profile can be observed in Figure 3.13.
The concept is the same as for the helium implant, it is based on the creation of voids, but the main difference is that the proton implant can be used as a donor for silicon, because hydrogen ions can be bound in the voids. We must have a specific dose to create voids that act as recombination centres.

3.6 Other lifetime killing techniques

There are other lifetime killing techniques that permit the device to be speed up. For example, palladium diffusion or indium implantation. High temperature palladium diffusion to control the carrier lifetime in power devices was initially studied to find deeper levels with a lower leakage current than gold and easier process control than gold or platinum [29]. This method has been shown to provide very low leakage currents and very good durability of fast recovery high power diodes.

Finally, We can do a comparison between the discussed techniques in Table 3.1:

Gold diffusion/implantation	High increase of the leakage current R_{on} increase Localized lifetime control in extended area
Platinum diffusion/implantation	Low increase of the leakage current Low R_{on} increase Localized lifetime control in extended areas
β/γ irradiation	Low increase of the leakage current Low R_{on} increase Instability in the V_{th} Homogeneous lifetime control
Helium and proton implantation	Negligible increase of leakage current Negligible increase of R_{on} Localized lifetime control in restricted areas

Table 3.1: Lifetime killing techniques

Chapter 4

Some Optimized PIN Diodes for Fast Reverse Recovery

4.1 MPS: Merged PIN Schottky

The merged PIN Schottky diode is a diode typically realized in SiC, implemented to improve the surge current capability [30, 31].
When we refer to power diodes, we can consider two big classes [32]:

- **Schottky diodes** → which offer extremely high switching speed but suffer from high leakage current;
- **PIN rectifier diodes** → which offer low leakage current but show reverse recovery charge during switching and have a large junction voltage drop.

The solution may be the MPS diode, because it offers low voltage drop in the on-state, fast switching characteristics and good high temperature characteristics like a Schottky diode, and low leakage in the off-state like a PIN diode [32].
Hereafter, we can see a Schottky diode ((a) Figure 4.1) and two types of MPS diodes ((b) Figure 4.1 and (c) Figure 4.1) [4]:

- the classical Schottky diode contains a p-zone on the edge of the active

area for field termination ((a) Figure 4.1);

- in the second type, highly p-doped regions are implemented, which act as a p-emitter and inject carriers when the forward voltage drop exceeds the junction voltage of the PIN diode ((b) Figure 4.1);
- the last solution is the implementation of p-layers in the PIN diode ((c) Figure 4.1).

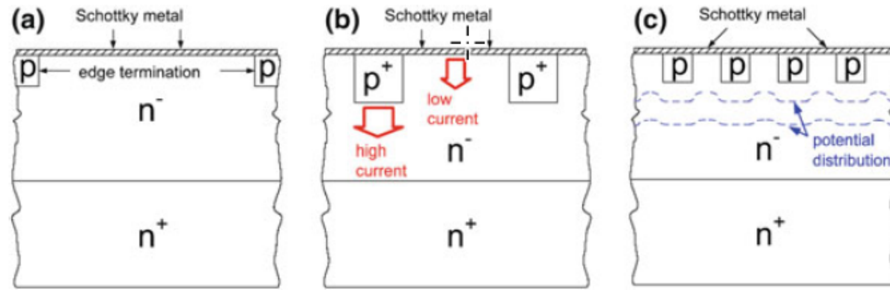

Figure 4.1: (a) Conventional Schottky diode (b) MPS diode structure with p^+ regions (c) MPS diode structure with p regions to shield the Schottky junction from high electric fields [4]

If we consider the structure in (c) Figure 4.1, the MPS is a sequence of p-layers and Schottky regions. The distance between the p-layers was chosen to be small enough so that, at blocking voltage, the Schottky junction is shielded from the electric field and only a low field strength is generated at that location. At low current, the MPS diode is similar to the Schottky diode characteristic, but at high current, it has a higher voltage due to the loss of area in the p-emitter region [4].
The on-state voltage drop of the MPS diode is determined by the resistance of the drift region, the height of the Schottky metal barrier, and the relative areas of the Schottky region and the doped p-region [32].

$$V_{MPS}(Low) = V_{FR} + \phi_B + \frac{k_B T}{q} ln \frac{J_F}{AT^2} \tag{4.1}$$

$$V_{MPS}(High) = V_{FR} + \phi_B + \frac{k_B T}{q} ln \frac{J_F}{AT^2} + V_{end} \tag{4.2}$$

where V_{FR} is the forward voltage, ϕ_B is the barrier height, J_F is the forward current density [33].

4.2 EMCON: Emitter Controlled

The emitter controlled is the precursor of the LEIA diode concept. The EMCON diode uses a p-emitter with low emitter efficiency [4].
Two principles can dominate the distribution of carrier concentration in the middle region of a diode [34]:

- **Hall principle** → if all recombination occurs in the middle region of the diode and the lifetime is dominant;
- **Kleinmann principle** → whether recombination exists only in the regions p^- or n^- or occurs at the contact of the metal with these regions, if a transparent emitter exists. In this case, the emitter efficiency in the boundary regions controls the carrier concentration.

EMCOM combines Kleinmann's principle with the control lifetime of the emitter. We can express this using the emitter parameter h_p:

$$h_p = \frac{D_n}{G_n} \tag{4.3}$$

where D_n is the diffusion coefficient and G_n is the Gummel number, the number of doping atoms per area [4]. To reduce the emitter efficiency, h_p must have a high value, so the Gummel number G_n must be low. A high h_p means that a significant portion of the total recombination occurs inside or on the surface of the p-emitter. As for the cathode side of the diode, it must have a high plasma density. Plasma concentrations can be controlled from very high to rather low values by the gate. However, extremely low values cannot be achieved because the required Gummel number must be low [35]. During commutation, the hole current flows to the anode of the negative electrode and the electron current flows to the cathode of the positive electrode.

As we can observe in Figure 4.2, the removal of the stored charge occurs for instants t_1, t_2, t_3 and t_4. The maximum reverse current occurs at instant t_2. The low p-emitter efficiency of EMCON diodes has the disadvantage of reducing the peak current capability.

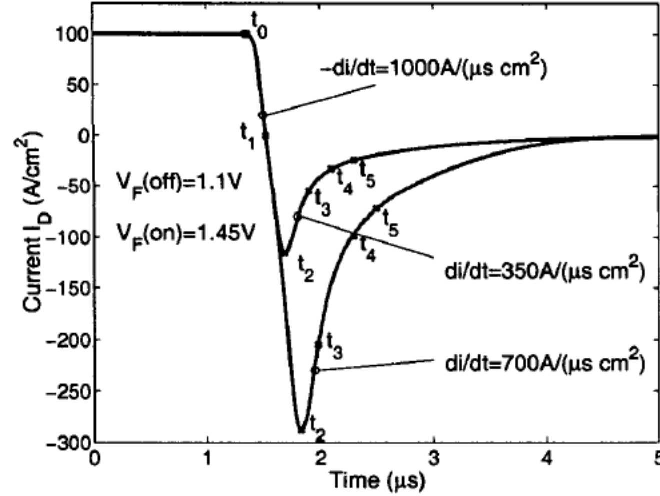

Figure 4.2: Current density during reverse recovery [35]

4.3 CAL: Controlled Axial Lifetime

The controlled axial lifetime diode is a diode that uses ion irradiation to make the diode faster [36]. This lifetime control is based on structuring the axial lifetime using single-energy mask ion irradiation (e.g. helium irradiation). The purpose of the non-contact single mask inserted in the beam line between the ion source and the device is to alter the energy distribution of the incident ions on the target and thus the axial defect profile of the device. The resulting axial defect, and hence the lifetime profile, is given by the density of the mask and its lateral/axial structure [36]. The implant depth can be controlled by the implant energy and its peak density by the dose. Three degrees of freedom, the depth of the recombination centre peak, its height and the base recombination centre density, are available to adjust the reverse recovery behaviour. It is better to locate the recombination centre peak near the pn junction. The main requirement is a low reverse recovery current peak I_{RRM}. This requires that there are no carriers in the pn junction at the beginning of the reverse recovery period. The relationship between the forward voltage V_F and I_{RRM} is better the closer the peak of the recombination centre is to the pn junction. In CAL diodes, the radiation induced recombination centre peak is located in the p layer near the pn junction. Consequently, most of the vacancy lies outside the space charge

and this arrangement results in a low leakage current [4].

4.4 FCE: Field Charge Extraction

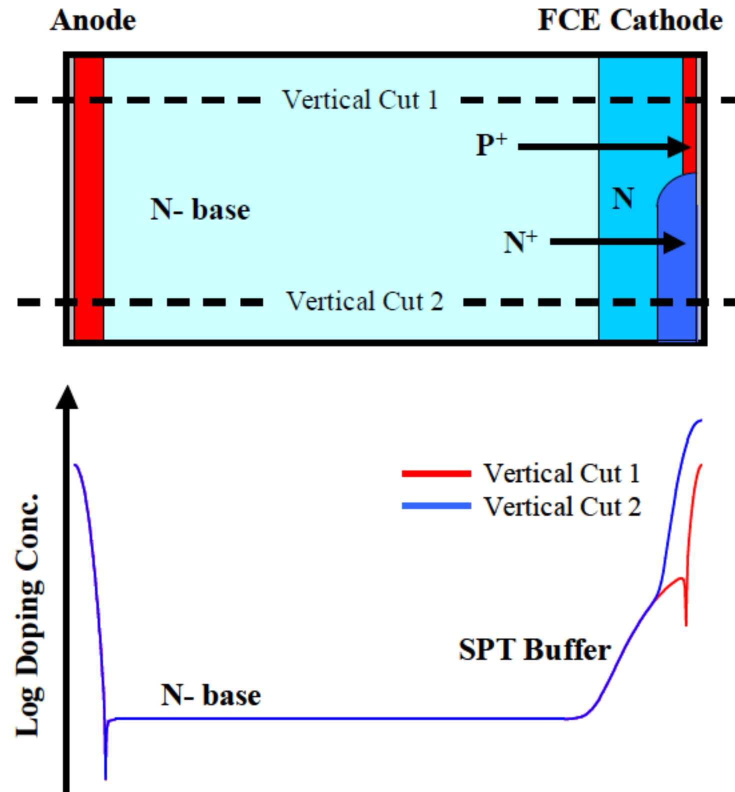

Figure 4.3: Cross-section of the FCE diode structure [37]

In Figure 4.3 we can observe the cross-section of the field charge extraction diode, with the respective doping concentration. This structure has a highly doped p^+ emitter, in which the emitter efficiency is governed by the local lifetime control by means of helium irradiation. The lifetime of the base n, on the other hand, is regulated by electron irradiation [37]. In the FCE diode, the cathode is a combination of p^+ and n^+ electrical connected by a metal, as can be seen in Figure 4.3. The cathode side n^+ is a PIN diode and the cathode side p^+ is a bipolar transistor *pnp*. We have a hybrid structure consisting of a PIN diode in parallel with a bipolar transistor *pnp* [37].

During forward conduction in a conventional PIN diode, the base n is flooded

with excess carriers. Their concentration depends on the emitter efficiency of the anode and cathode. In the FCE diode, current can only flow in the n^+ contact region of the FCE cathode. Therefore, the average concentration of excess carriers on the cathode side of the FCE diode is reduced, and thus, the on-state voltage drop is higher than in a standard diode. However, the overall trade-off between on-state and reverse recovery loss is better in the FCE diode. The on-state voltage of the FCE diode depends on the concentration of n-buffer and the area ratio of the p^+ region to the n^+ cathode region [37].
During the reverse recovery phase, electrons initially stored in the n base flow towards the FCE cathode, thus preferentially passing through the n^+ region to the cathode contact. At the end of the reverse recovery phase, when the electric field begins to close the cathode, the gain of the internal bipolar transistor increases, inducing the injection of holes from the p^+ region. This hole current is in addition to the reverse recovery current derived from the stored excess carriers and further delays the depletion of the excess carriers under the p^+ region of the FCE cathode. In conventional diode structures, as the electric field propagates towards the cathode, the stored charge eventually becomes too small to support the continuously decreasing reverse current and the current snaps-off. In the cathode FCE, the current of the stored charge is injected by the emitter p^+. The average concentration of excess carriers increases from the anode side to the cathode side of the diode, which is important for the reverse recovery characteristics of the FCE diode. This is to prevent space charge regions from accumulating on the cathode side in the early stages of reverse recovery. This inevitably leads to undesirable reverse recovery characteristics, with a large peak reverse recovery current I_{RR} [37].

4.5 RED: Radiation Enhanced Diffusion

Another fast diode is the radiation enhanced diffusion diode (RED). Typically, this diode is speed up using a diffusion technique, such as gold and platinum diffusion [38] or palladium diffusion [39].

The Figure 4.5 is the profile of the RED anode. The RED diode has a uniform, low doped p layer attached to the anode junction pn [40]. The role of this layer is to flatten the electric field peak under reverse bias, thus providing a higher breakdown voltage and reduced dynamic avalanche

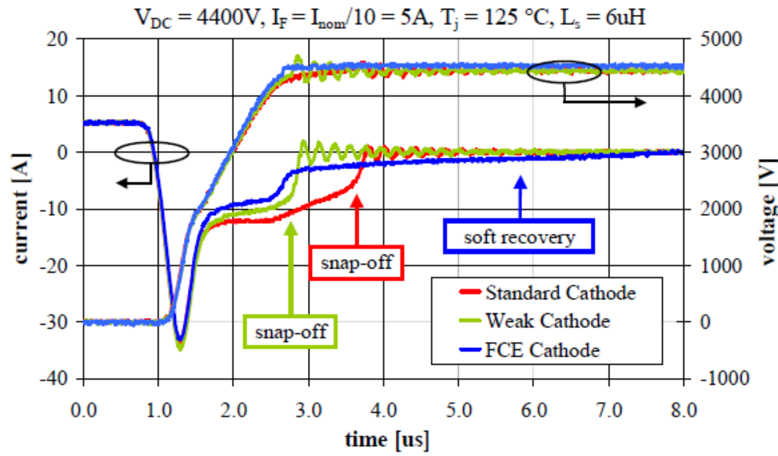

Figure 4.4: Reverse recovery FCE diode [37]

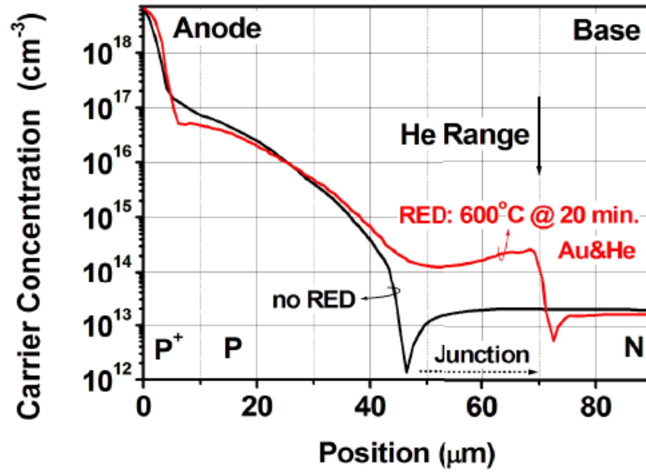

Figure 4.5: Anode doping profile with e without RED of gold

during fast reverse recovery. This layer locally decreases the lifetime of excess carriers and increases the concentration of on-state carriers. As a result, the distribution of on-state carriers is reduced and the leakage current increases negligibly [40].

4.6 Other fast recovery diode

Other fast recovery diodes exist:

- **MOS controlled diode (MCD)** → in which the properties of the diode are to be improved by introducing a third electrode, a MOS gate [4];
- **Controlled injection of backside holes (CIBH) diode** → in which the back-side p-layers inject additional holes and dampen possible oscillations [4];
- **Ultra small reverse recovery charge (USQ) diode** → has a thin p-layer anode with low concentrations of impurities, p+ strip anodes and lifetime control by irradiation of helium ions [41];
- **Ultra soft and fast recovery diode (USFD)** → has shallow p-type Schottky junctions and deep pn junctions [42];
- **Junction charge extraction (JCE) diode** → is based on the integration of low and high lifetime regions into a single structure, using masked helium irradiation [43].

All of these diodes have one common characteristic, they are speeded up with a lifetime killing technique.

Chapter 5

IGBT

The IGBT stands for "Insulate Gate Bipolar Transistor". The first IGBT was developed around 1980, in the USA, by F. Wheatley and H. Becke [44]. This technology combines the concept of a bipolar transistor with the possibility to control the transistor in voltage, as occurs in power MOSFET technology [4].
The IGBT allows mixed, unipolar and bipolar conduction. This results in low output resistance, high current flow rate and good SOA (Safe Operating Area). The key point is the trade-off between switch-off commutation velocity and conduction losses. If we make the IGBT faster, we increase conduction losses and vice versa.

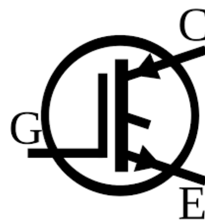

Figure 5.1: IGBT symbol [45]

5.1 IGBT overview

The IGBT is a transistor with three terminal: *Emitter*, *Collector* and *Gate*. The manufacturing process is similar to that of a power MOSFET, with

regard to the elementary cell [2]. The main difference is the presence of a p^+ layer on the bottom side of the structure. The mere introduction of this layer profoundly changes the equivalent circuit and the operating principle. The resulting structure has a bipolar transistor *pnp* and a parasitic transistor *npn*.
The presence of the *pnp* is fundamental to the operation of the device, because in the ON phase, the equivalent circuit consists of a power MOSFET and a bipolar *pnp* transistor, and both cooperate to determine the characteristics of the device [2].

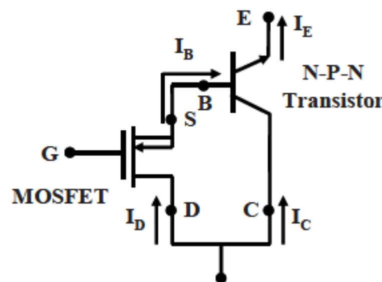

Figure 5.2: IGBT equivalent circuit [44]

The function of the n^+ layer is to control the gain of the *pnp* transistor and to prevent the electric field, when the device is inversely polarised, from reaching the p^+ layer, producing a "punch-through" effect.

5.1.1 IGBT structure

The basic structure of the IGBT consists of an n-channel. In Figure 5.3 we can see two kinds of IGBT structures: *Planar* and *Trench*. The latter will be analysed in detail in the following sections.

The structure of the IGBT is formed using four alternating semiconductor layers (N-P-N-P). We can name the different layers:

- P^+ on the backside is the EMITTER;
- N^+ on the backside is the FIELD-STOPPER;
- N^- is the DRIFT LAYER;
- P on the front-side is the BODY;

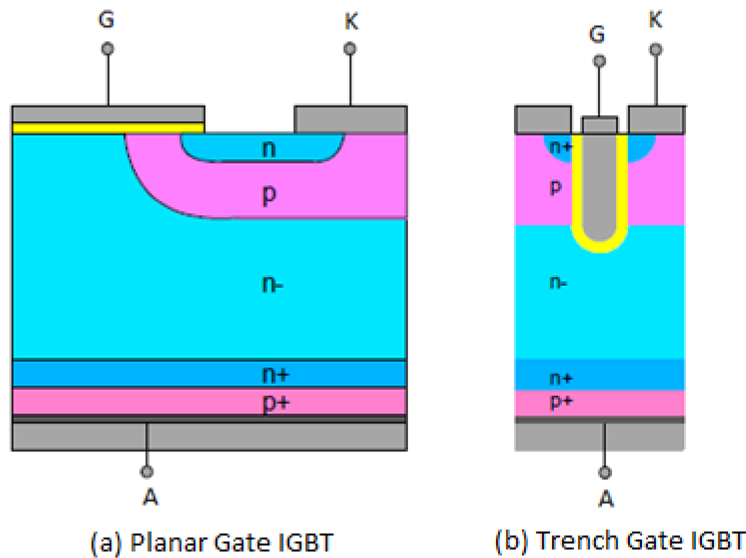

Figure 5.3: (a)IGBT planar structure (b)IGBT trench structure [46]

- N^+ on the front-side is the SOURCE.

It presents three contacts:

- GATE;
- EMITTER;
- COLLECTOR.

The power IGBT essentially consists of a repetitive array of dozens of elementary unit cells arranged in a topological layout with a wide aspect ratio between width and length.
The first kind of IGBT, which was developed, is the *Planar*. This structure differs from the others in that it lacks the trench structure. The motivation for using the trench structure is the interest in reducing the on-state voltage drop. Another motivation is the observation of an increased concentration of carriers in the proximity of the trench-gate region, called the "injection enhancement effect" [44]. Today, the most widely used technology is the *Trench* IGBT structure.

5.1.2 Operating principles

The IGBT device operates in mixed conduction (minority and majority carriers). The device is in the on state when we apply a positive gate voltage V_G, which is higher than the threshold voltage V_{Th}, and the positive voltage V_{CE} between emitter and collector is higher than the turn-on diode voltage V_J (typically $\sim 0.6V$) of the *pn* junction at the back-side. A hole current I_{CE} is injected from the collector and an electron current I_{MOS} passes into the channel of the PowerMOSFET. A part of I_{CE} is collected in the emitter and a part recombines in the drift layer. The I_{MOS} recombines with the hole current from the emitter [2]. The simplified equations are as follows:

$$I_{CE} = I_C + I_{MOS} \tag{5.1}$$

$$I_C = \beta I_{MOS} \tag{5.2}$$

$$I_{CE} = (1+\beta) I_{MOS} = \frac{I_{MOS}}{1-\alpha} \tag{5.3}$$

An important conduction phase parameter for the IGBT is the $V_{CE_{sat}}$ (Equation 5.4):

$$V_{CE_{sat}} = V_{BE} + I_{MOS} R_{on} \tag{5.4}$$

where R_{on} is the resistance of layer n. The heart of the IGBT's operation is the *pnp* transistor, for the static characteristic but also for the dynamic characteristic [2].
Turn-off of the IGBT requires special attention. It will be discussed in the following sections.

5.2 PT IGBT & NPT IGBT

There are three kinds of IGBTs, punch-through (PT), non-punch-through (NPT) and trench field stopper (TFS). The latter will be discussed in a separate section.

With regard to PT IGBTs and NPT IGBTs, their choice is related to applications [2]. Static and dynamic characteristics and robustness are impacted by this.
The IGBT NPT can be considered a symmetrical structure because it has the same forward and reverse breakdown voltage [46].
PT IGBTs, also known as asymmetric IGBTs, have an n-type buffer layer that performs two functions. Firstly, it provides electrons that recombine with holes. This reduces the device's turn-off time and speeds up switching. Secondly, it reduces the width of the n-drift region, resulting in a reduction of the breakdown voltage that the device can support [46].

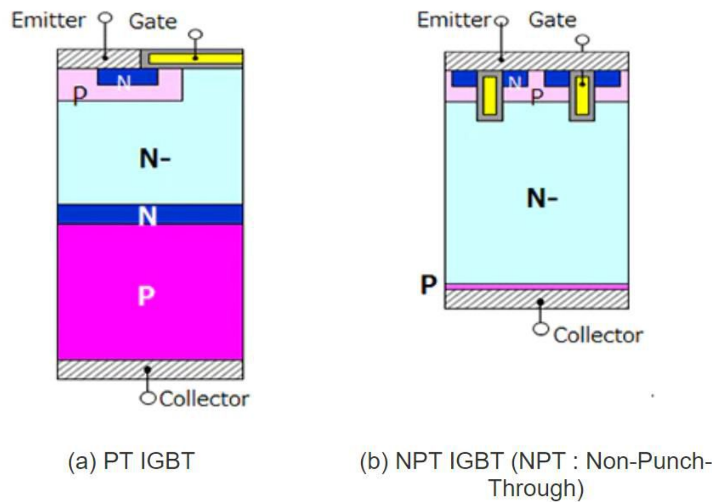

Figure 5.4: Section (a)IGBT-PT (b)IGBT-NPT

In the very first IGBT structure, the N^+ substrate of the MOSFET was replaced by a P^+ substrate. These structures, unfortunately, were very sensitive to latch-up. The behaviour was improved by the addition of a medium-doped N layer, called the "Buffer layer", as seen in Figure 5.4(a). The electric field can penetrate the buffer layer, which can give a trapezoidal shape to the electric field [2].

This is the case of the punch-through IGBT. In this case, during the off-state, the depletion region extends over the entire N^- region, until it reaches the buffer layer, which rapidly drops the electric field, preventing it from reaching the P^+ substrate. The charge Q_N that we have in the buffer layer must be sufficient to drop the electric field to zero and to satisfy the condition

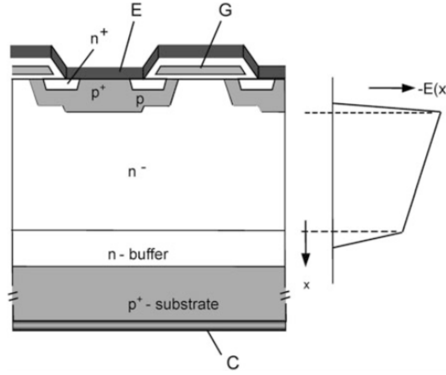

Figure 5.5: IGBT punch-through (PT) [4]

[2]:

$$Q_N = X_{N^+}N^+ \geq \frac{\epsilon}{q}E = 1.3 * 10^{12}cm^{-2} \tag{5.5}$$

where E is the electric field at the $N - N^+$ interface and X_{N^+} and N^+ are the thickness and concentration of the buffer layer, respectively. In theory, it is possible to decrease the thickness and increase the doping concentration to compensate, but there is an upper limit for the doping concentration of the buffer layer, because too high a concentration can degrade the performance of the device in forward conduction. Due to the buffer layer, the IGBT PT has a thinner N^- layer and a lower $V_{CE_{sat}}$ than the NPT IGBT, at the same Breakdown voltage. When the PT IGBT is in the conduction state, more holes are injected due to the higher doping concentration of the substrate P^+. This results in a reduction of $V_{CE_{sat}}$ and a longer turn-off time. In order to solve this problem, lifetime killing techniques can be used [2].

In the NPT IGBT, the N^- layer is thick enough to reset to zero the electric field before it reaches the substrate, and the substrate concentration P is lower without the lifetime killing techniques. As can be seen in Figure 5.6, the electric field is triangular; the N^+ buffer layer is removed because the electric field is negligible in its proximity; the N^- layer must be larger than the depletion region at the breakdown voltage [2]:

$$X_{N^-} > \sqrt{\frac{2\epsilon BV}{qN^-}} \tag{5.6}$$

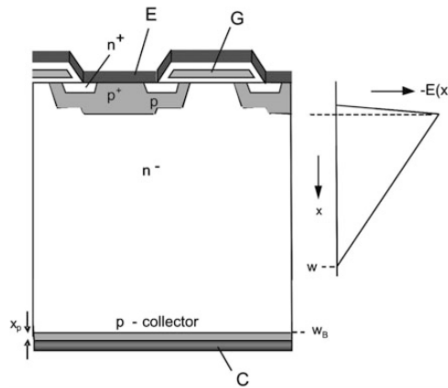

Figure 5.6: IGBT not-punch-through (NPT) [4]

Both structures present problems: the PT IGBT has a highly doped substrate, which results in a higher injection of holes, forcing the use of lifetime killing techniques to speed up the device; the NPT IGBT does not require lifetime killing techniques, but for the same breakdown voltage, the drift layer becomes thicker and $V_{CE_{sat}}$ increases [2].

5.3 EI TFS IGBT

In order to overcome the limitations of the structures described above, a structure called IGBT emitter implant trench field stopper was realised. This is a hybrid approach that combines the advantages of PT and NPT structures. This new structure presents a better compromise between static and dynamic characteristics. The field stop layer concept is a compromise between the trapezoidal shape of the electric field in a PT device and the low injection/low doping emitter together with the high carrier lifetime of an NPT device [47].

The P^+ collector layer and the N^+ layer at the back-side are realised by ion implantation. By controlling the amount of charge Q_E in the P^+ layer, it is possible to decrease and control the injection of holes to realise a faster device, without using lifetime killing techniques. The N^+ layer is called the "field-stop" layer, realised by implanting it at a higher energy than P^+ and with a dose that has very little effect on the *pnp* emitter efficiency and that drops the electric field to zero. Its concentration is an order of magnitude lower than the concentration of the N^+ layer of the PT IGBT [2]. The

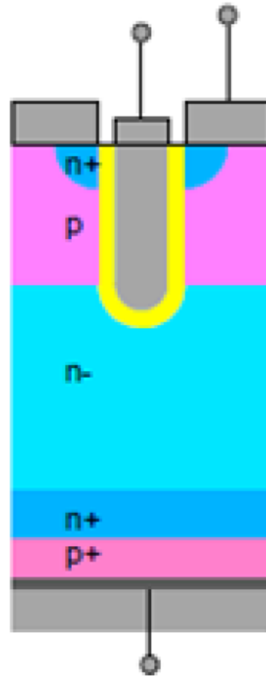

Figure 5.7: Emitter Implant Trench Field Stopper IGBT

function of the N^+ layer is to drop the electric field and allow the thickness of the drift layer to decrease. We can see the differences between PT IGBT, NPT IGBT and EI FS IGBT in Table 5.1 and in Figure 5.8:

	PT IGBT	NPT IGBT	EI FS IGBT
Emitter charge	High	Low	Low
Thickness N^-	Thin	Thick	Thin
Buffer layer N^+	Needed to reduce the emitter efficiency and to drop the electric field	No needed	Need to drop the electric field
Lifetime killing	Needed	No needed	No needed

Table 5.1: IGBT technologies

FS technology requires thin wafer processing capability because the FS layer and emitter are implanted after the front-side fabrication and wafer thinning

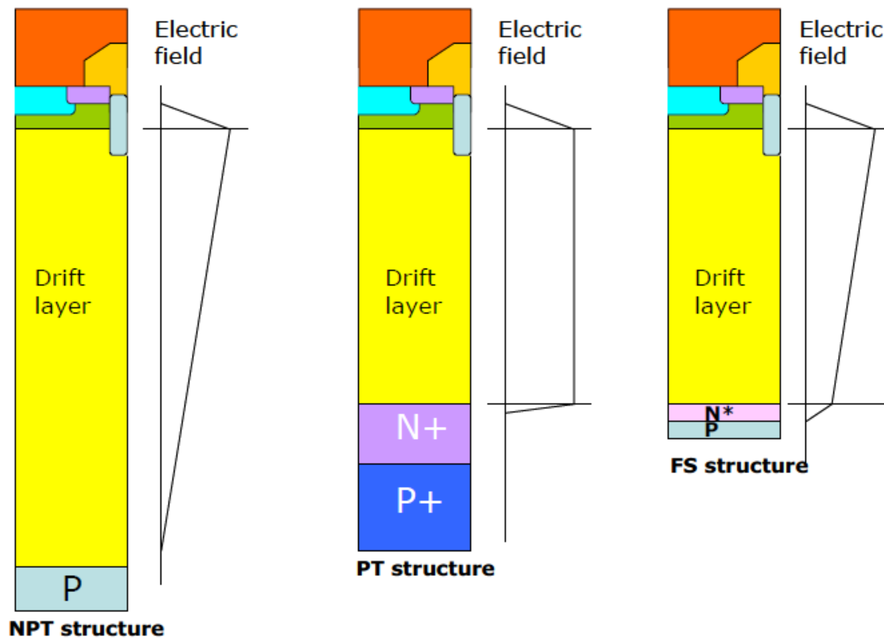

Figure 5.8: Three different IGBT structure [48]

[48].
This technology is characterised by low emitter efficiency, low concentration of the N^+ buffer layer and the absence of lifetime killing techniques. The substrate thickness is reduced before to ion implantation of the P^+ and N^+ layers. This leads to two issues:

- the processing of thin wafers;
- the doping activation in the P^+ and N^+ layers.

With regard to the processing of thin wafers, a technique called "Taiko" is used to prevent the wafer from bending. Concerning doping activation in the P^+ and N^+ layers we have two possibilities:

- the furnace annealing;
- laser annealing.

5.3.1 Taiko process

The Taiko process is named after the physicist who invented it. The Taiko process is a back grinding method. In Figure 5.9 we can see the differences between the conventional back grinding technique and the Taiko back grinding [49].

Figure 5.9: On the right the thinning of the silicon wafer with the conventional back grinding technique and on the left the thinning of the silicon wafer with the Taiko process [49]

When back grinding is performed using the Taiko method, a ring edge of approximately 3 mm is left on the outermost edge of the wafer and only the inner edge is thinly ground. This method reduces the risk when handling thin wafers and reduces warpage aging.

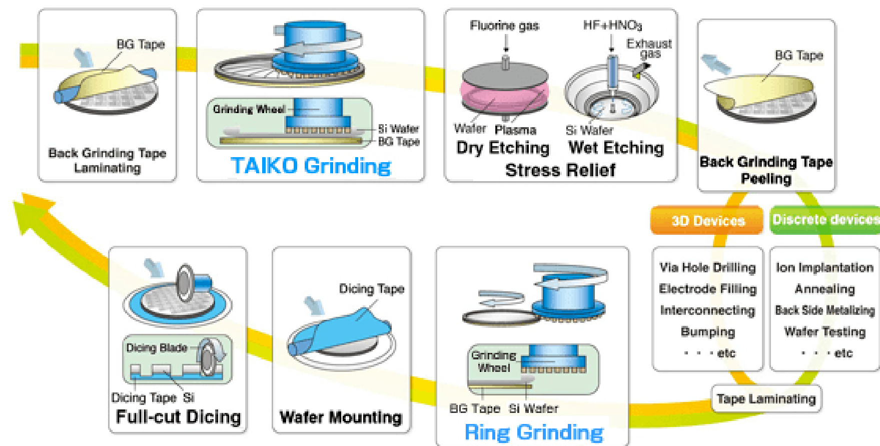

Figure 5.10: Taiko flow [49]

In Figure 5.10 we can see the Taiko process flow. The first step consists of gluing the tape to prevent the wafer from slipping during grinding. The

second step consists of grinding through the Taiko process, leaving the edge. Then the lapping processes are performed on the wafer and, finally, the detape is performed [49].

5.3.2 Furnace annealing

One process used to activate the dopant is furnace annealing, which only activates a fraction of the implanted dose. We have a limit in the implanted dose, because a high dose can produce a high defectiveness, which cannot be recovered because it requires treatment at too high a temperature. The high defectiveness worsens the $V_{CE_{sat}}$. The $V_{CE_{sat}}$ decreases when we increase the doping dose, but it reaches a minimum value and then increases again, because we have a high defectiveness [2]. Due to the impossibility of obtaining a good $V_{CE_{sat}}$, the furnace annealing can only be used in low-frequency applications, e.g. PFC, microwave oven, etc... For high-frequency applications, e.g. motor control, traction inverter, etc., laser annealing is used.

5.3.3 Laser annealing

To overcome the constraint of furnace annealing, we can use laser annealing, which allows a higher temperature in order to be reached for complete activation. We can activate higher doses.
If we want to make devices with very low $V_{CE_{sat}}$, the way forward is to use laser annealing to activate the doping [2].

5.4 Trade-off curve

An important concept in defining the characteristic of the IGBT is the trade-off curve $V_{CE_{sat}}$ vs E_{off}. This is important in device design, because the design must be functional for the application. An example of this curve can be seen in Figure 5.11.

If we want a faster device, we have to decrease the E_{off} (turn-off energy), but, in this case, we increase the $V_{CE_{sat}}$ and the conduction losses; conversely, if we have an application that requires lower conduction losses, we have to move to the left side of the trade-off curve. In order to make a device with low conduction losses, we have to use laser doping activation, because with

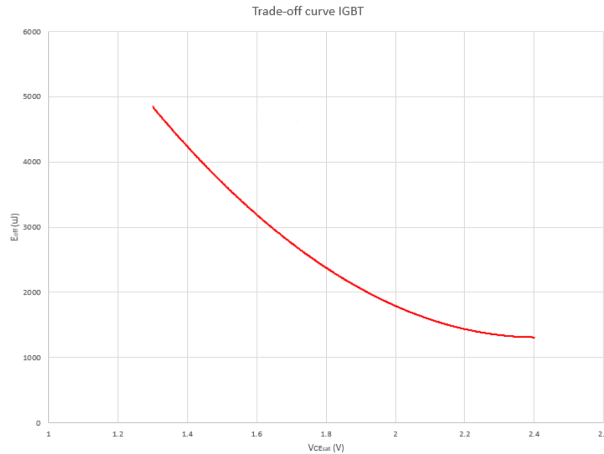

Figure 5.11: IGBT trade-off curve

the laser we recover almost all defects and the conduction loss in this case is lower than when we use furnace annealing, because with the furnace process the defects are partially recovered [2].

5.5 I-V characteristic

In Figure 5.12 we have an example of an I-V characteristic for the IGBT. This characteristic is very similar to that of a MOSFET. The channel is open when the gate voltage is higher than the threshold voltage. In particular, the IGBT differs from the MOSFET in the pn-junction voltage on the collector side. Like a MOSFET, the IGBT operates in the saturation region [46].

In Figure 5.13 we can see the comparison between IGBTs and bipolar transistors. The difference is pronounced. The IGBT can also be designed for higher voltages than the MOSFET or BJT.

5.6 Switching operations

To determine the switching behaviour of the IGBT, we must have a circuit with an inductive load, diode and gate resistance, such as Figure 5.14 [4].

The inductive load is important because we have to use a specific coil to determine the switching time. The formula is as follows:

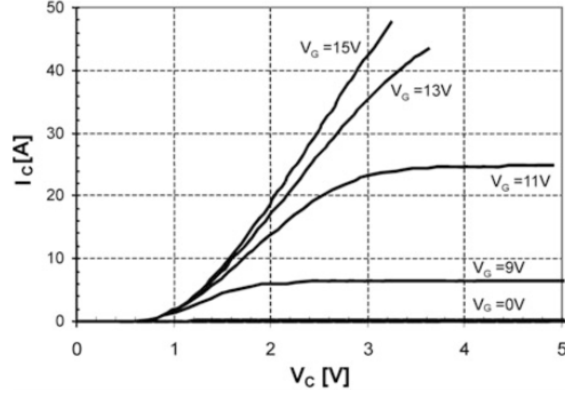

Figure 5.12: I-V characteristic [4]

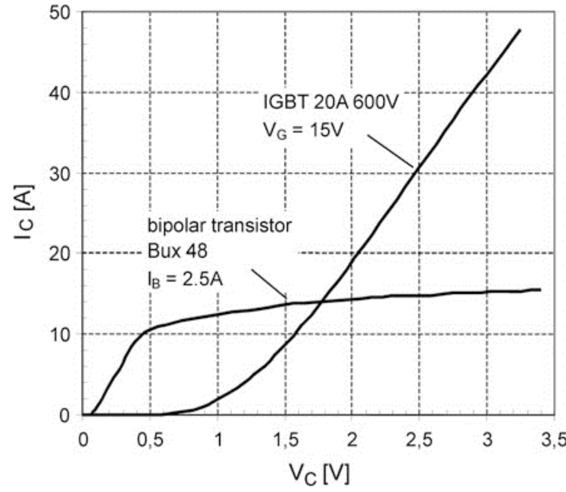

Figure 5.13: I-V characteristic comparison with a bipolar transistor [4]

$$t = \frac{I_C L_{load}}{V_{cc}} \tag{5.7}$$

where I_C is the nominal current and V_{cc} is the battery voltage and t is the commutation time. To turn-off the IGBT, the positive gate voltages are switched to zero or to a negative value. An important parameter for turn-off is the E_{off} (switch-off energy). It can be calculated from the following formula [4]:

$$E_{off} = \frac{1}{2} V_{cc} I_C t_{rise} + \frac{1}{2}(V_{cc} + \Delta V I_C) t_{fall} + \frac{1}{2} V_{cc} I_{tail} t_{tail} \tag{5.8}$$

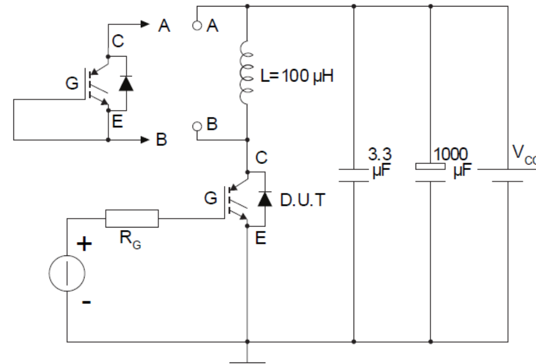

Figure 5.14: Circuit for the IGBT turn-off

In this formula, the first term regards the part where the collector voltage increases until it reaches the peak, the second term regards the part where the voltage decreases until it reaches V_{cc} and the third term regards the tail. We can see this in Figure 5.15.

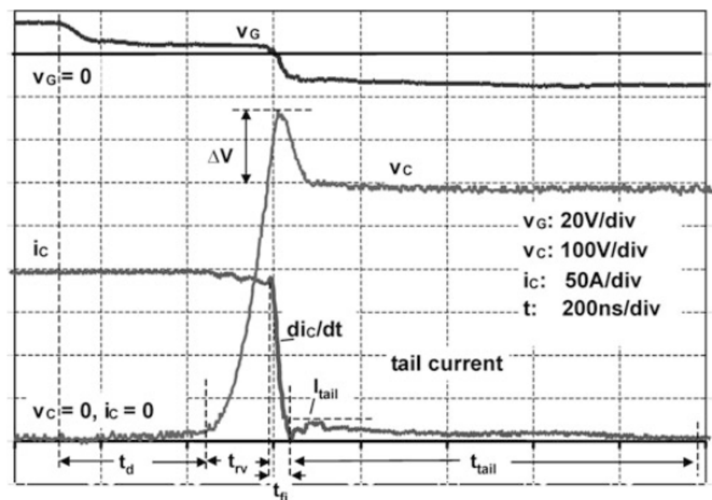

Figure 5.15: Waveform of IGBT turn-off [4]

The turn-off principle is very similar to that of MOSFETs. The main difference is the tail current. The current drops slowly during the time interval t_{tail} to the value I_{tail}. This time is determined by the recombination of the charge carriers remaining in the device. The voltage is high during the tail current period and the losses occurring during this time are not negligible [4].

5.7 Use of IGBT with anti-parallel diode

The anti-parallel diode is required for switching the IGBT. This diode is a freewheeling diode. During the activity of the IGBT, an amount of charge accumulates in the *pn* junction at the back-side. When an IGBT is turned off, the voltage across it changes rapidly. This can cause a reverse current to flow through the IGBT, which can damage the device.
The freewheeling diode provides a path for this current to flow, which protects the IGBT from damage. MOSFETs have the diode structure integrated. For the IGBT, this is not the same. We have to have the correct freewheeling diode. This depends on the application. For example, if we have to use the IGBT in an application for hard switching, we need to have a fast diode, whereas if the application is for example for induction heating, the diode does not have to be necessary fast. The freewheeling diode in an IGBT module is typically chosen according to the maximum current and voltage rating of the IGBT. It is important to select a diode with a rating higher than the maximum current and voltage that the IGBT will experience.
Overall, the freewheeling diode in an IGBT module plays an important role in protecting the IGBT from damage and ensuring the reliable operation of the circuit.
The diode used must be a PIN rectifier diode.

5.8 RCIGBT concept

An evolution of the IGBT is the RC-IGBT. This device solves the freewheeling diode problem. RC-IGBT stands for "Reverse Conducting Insulated Gate Bipolar Transistor". The diode is integrated in the IGBT. This is very convenient because in one die, we have both the diode and the IGBT.
The first difference of the RC-IGBT is the possibility of bidirectional commutation, it can manage current in both directions. Part of the P region in the collector electrode is replaced by an N region to form a PIN diode. This PIN diode is connected anti-parallel to the IGBT, like the freewheeling diode. The process steps are the same as for the standard IGBT. The difference in the process lies in the final phototechnique on the back-side. This step allows the doping to be inverted in a specific region, where a PIN diode region is created, that permits reverse conduction.

This kind of device, when forward biased, works like a simple IGBT, but with a small difference in the I-V characteristic. For small voltages, the characteristic has a resistive behaviour due to the parassitic MOSFET integrated in the RC-IGBT structure. When a positive voltage is applied to the on-state of the transistor, i.e. at the anode (collector) with respect to the cathode (emitter), a unipolar current due to electrons flows, as in a MOSFET from the N side of the cathode through the the n-buffer [50]. When the junction voltage V_J is reached, bipolar conduction is triggered. This phenomenon can lead to the snapback effect, which is undesirable.
When the device is reverse biased, the integrated PIN diode starts working. The RC-IGBT concept it is very effective cost solution with good performance.

Chapter 6

LEIA RC-IGBT as New Hybrid Concept

6.1 Proposed structure and flow

The LEIA RC-IGBT structure is a novel hybrid concept introduced in the patent application "Reverse-Conducting IGBT device and manufacturing method thereof, inverter stage" [1]. This structure integrates the power transistor (IGBT) and the diode within the same die, and it is intended for use in motor control. A fast diode is necessary for this application, because the power transistors, inserted in the modules, must carry current to the three-phase motor [23].
Three-phase motors are AC motors, in which the rotor current, that is required to generate the torque, is produced by electromagnetic induction, from the stator winding's magnetic field. As an asynchronous motor, it must alternate the current to produce the rotation and generate three phase-shifted waves. Fast switching is essential to generate the three phase-shifted waves, as the transistors must alternate between turning on and off quickly.

In this section, we will illustrate a hybrid structure utilizing the LEIA concept. Further elaboration on the LEIA concept will be provided in the subsequent section.

In Figure 6.1 we can see the possible final cross-section of this structure,

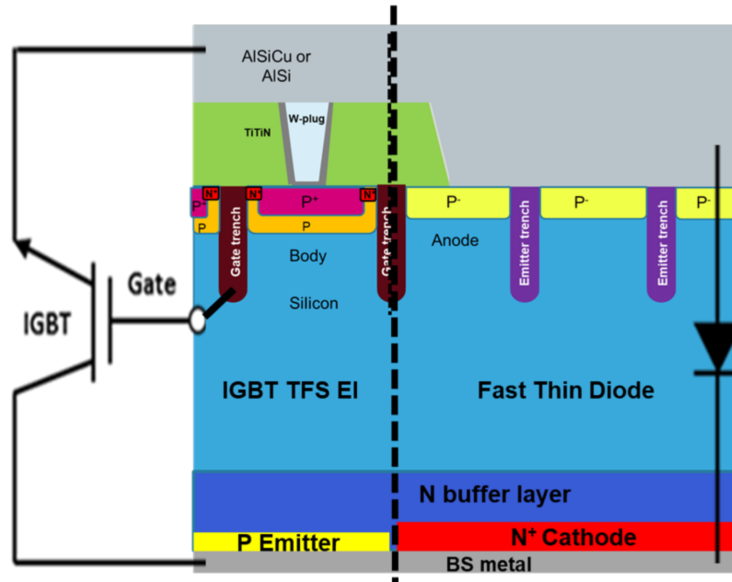

Figure 6.1: LEIA RCIGBT structure

with the IGBT on the left and the diode on the right.
The flow sequence is very similar to that of the standard IGBT, but differs, mainly in terms of the dose between the IGBT body and the diode anode, for the source and deep body implants skipped on the diode side, for the top contact and for the cathode implant on the back-side.
We summarised the main steps of the flow in the following subsection [1].

IGBT Body implantation

We start from a silicon wafer and we perform the preliminary processes in the fabrication of an IGBT. This includes the ring implantation and subsequent diffusion, and the photolithography technique use for the body implantation. The wafer is coated with a photoresist and, subsequently, exposed through a mask. Afterward, the IGBT side has the body implanted with a standard boron dose. It is necessary to differentiate between the IGBT's body and the diode's anode, because the p dopant dose must vary (see Figure 6.2) [1].

Diode Anode implantation

The subsequent step involves the implantation of the anode on the diode side. This step mirrors the procedure for implanting the body on the IGBT

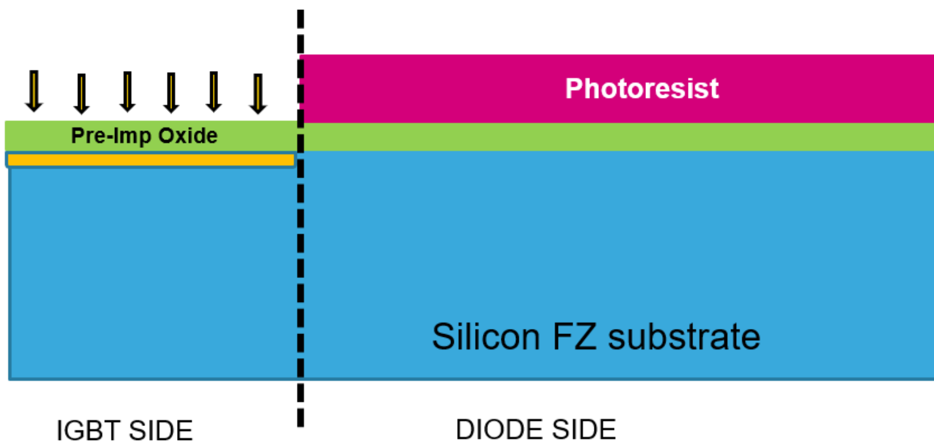

Figure 6.2: IGBT Body implantation

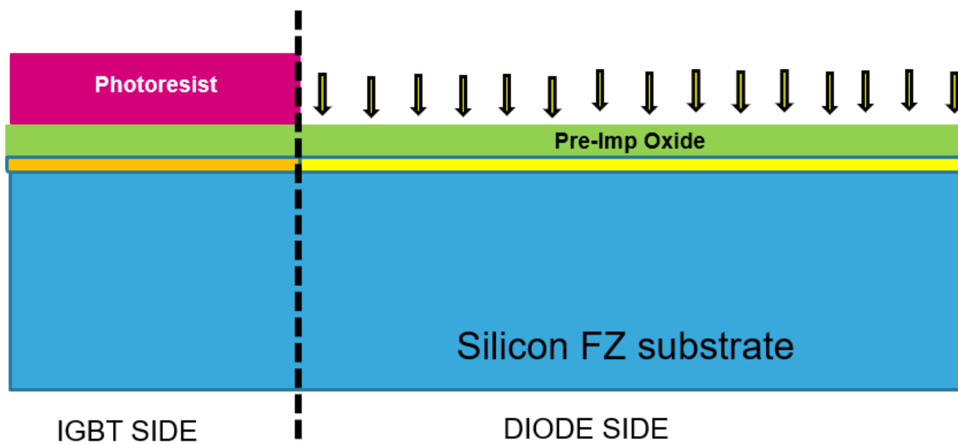

Figure 6.3: Diode Anode implantation

side, except for a lower dose of p dopant used. This reduction of the dose is the key to the LEIA process (see Figure 6.3) [1].

IGBT Body and Diode Anode diffusion

Following implantation, activation of the dopants requires thermal annealing diffusion in a furnace. During implantation, the dopant atom penetrates the crystal lattice, with penetration depending on factors, such as dopant concentration and implantation energy. As the dopant travels through the

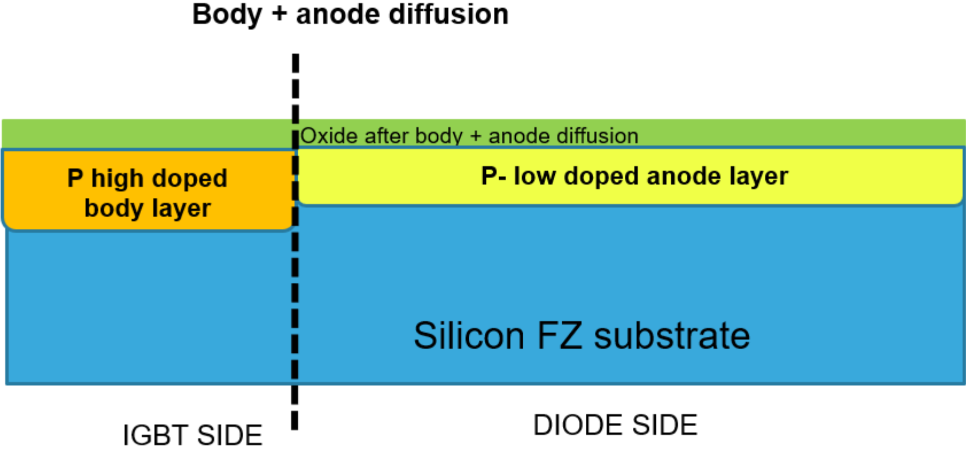

Figure 6.4: IGBT Body and Diode Anode diffusion

lattice, it loses energy due to a series of scatterings, that damage the lattice, until it eventually comes to a stop. After the process of annealing, there is a reconstruction of the crystal lattice and the dopants are activated (see Figure 6.4) [45] [1].

Deep Body implantation

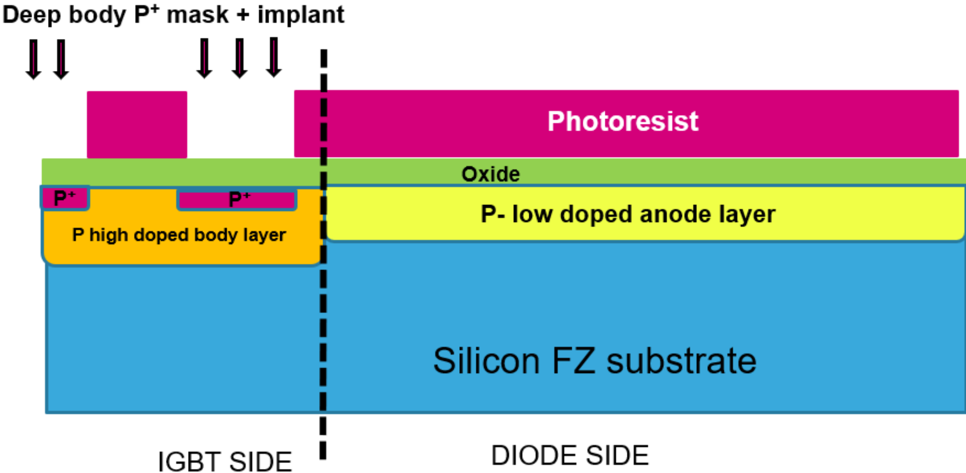

Figure 6.5: Deep Body implantation

The fourth step involves the P^+ implant into the IGBT side and then annealing. We have chosen to implant the P^+ only in the part of the IGBT, because in the part of the diode, as we will explain in more detail in the section on "Metal-semiconductor ohmic contacts", we will implant the BF^2 to enrich the contact, which will allow us to maintain the advantages of the low injection efficiency, given by the use of the LEIA technique, and to generate an ohmic contact. The implantation of BF^2 compared to the standard implantation of P^+, allows us to have a shallow enrichment, which will therefore only enrich near the metal-semiconductor junction. Aided by the TCAD simulations (see Table 6.1), we observe that by removing P^+ from the diode side, and adding BF^2, the V_{fec} of the device improves (see Figure 6.5) [1].

V_{fec} (15A) with P^+	V_{fec} (15A) without P^+	V_{fec} (15A) without P^+ & with BF^2
1.4090 V	2.2847 V	1.1201 V

Table 6.1: P^+ implant skipped in diode side

Source implantation

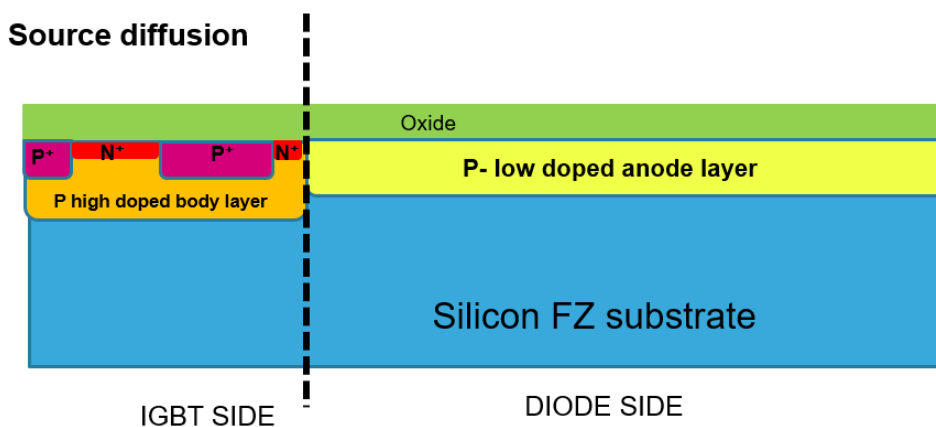

Figure 6.6: Source implantation

Next, we performed source implantation solely on the IGBT side. Results from TCAD simulations indicate that elimination of the source implantation on the diode side, led to an improvement in the V_{fec} of the diode (see

Table 6.2) (see Figure 6.6) [1].

V_{fec} (15A) with source	V_{fec} (15A) without source
1.5134 V	1.4090 V

Table 6.2: Source implant skipped in diode side

Source diffusion

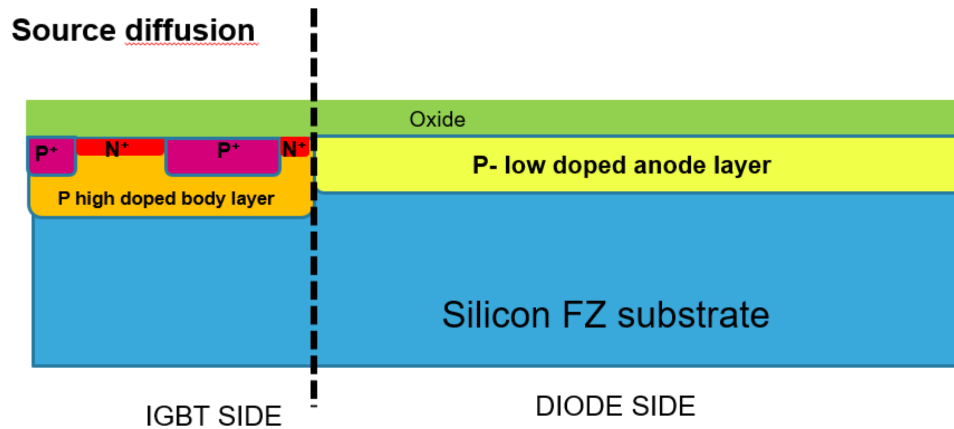

Figure 6.7: Source diffusion

After implantation, dopants are activated through diffusion (see Figure 6.7) [1].

Trench formation

The seventh step involves an anisotropic and isotropic etching process, that creates a trench to be filled with polysilicon. Subsequently, the dielectric layer is deposited (see Figure 6.8) [1].

IGBT contact opening

Following the deposition of the dielectric layer, an opening is created for the IGBT contact on the IGBT body, by etching into the dielectric layer, using a photolithographic mask that covers the diode side. This opening is located on the IGBT body (see Figure 6.9) [1].

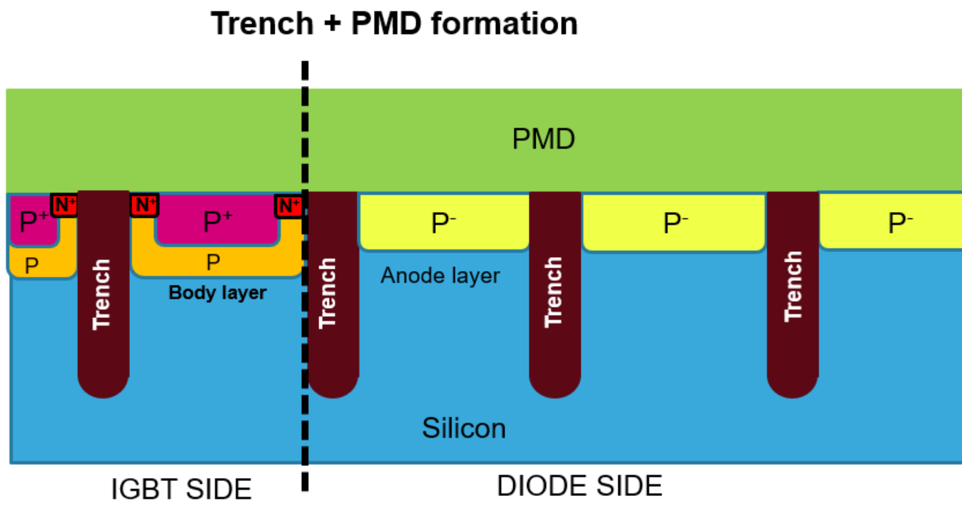

Figure 6.8: Trench formation

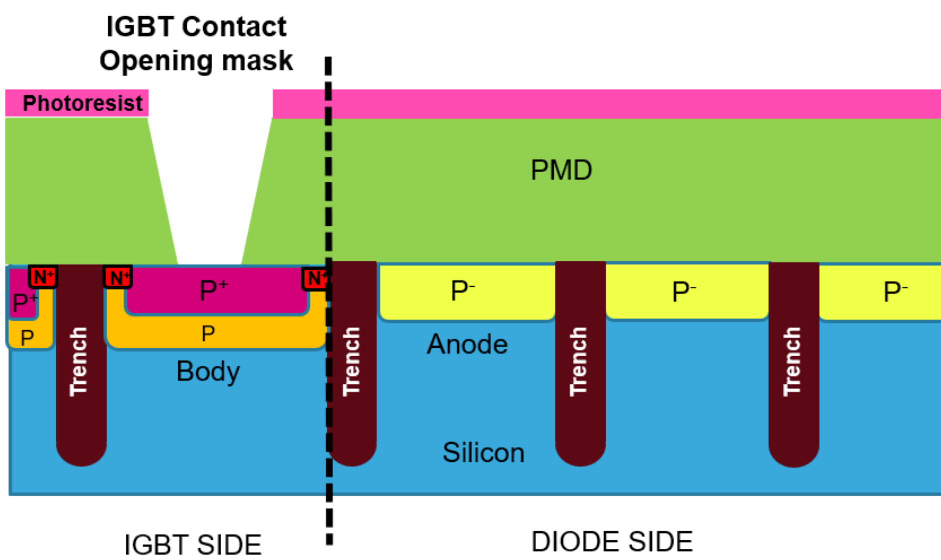

Figure 6.9: IGBT contact opening

TiTiN barrier deposition

The ninth step involves depositing the TiTiN barrier onto the top of the device (see Figure 6.10) [1].

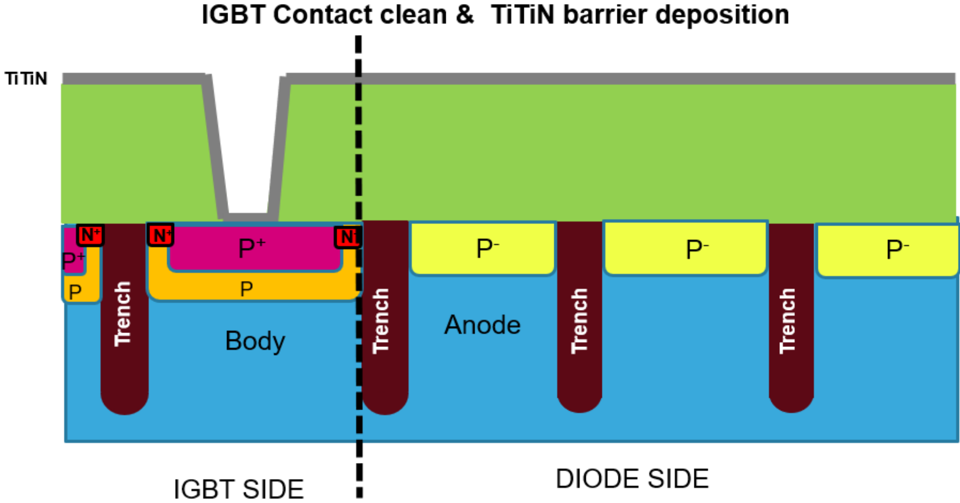

Figure 6.10: TiTiN barrier deposition

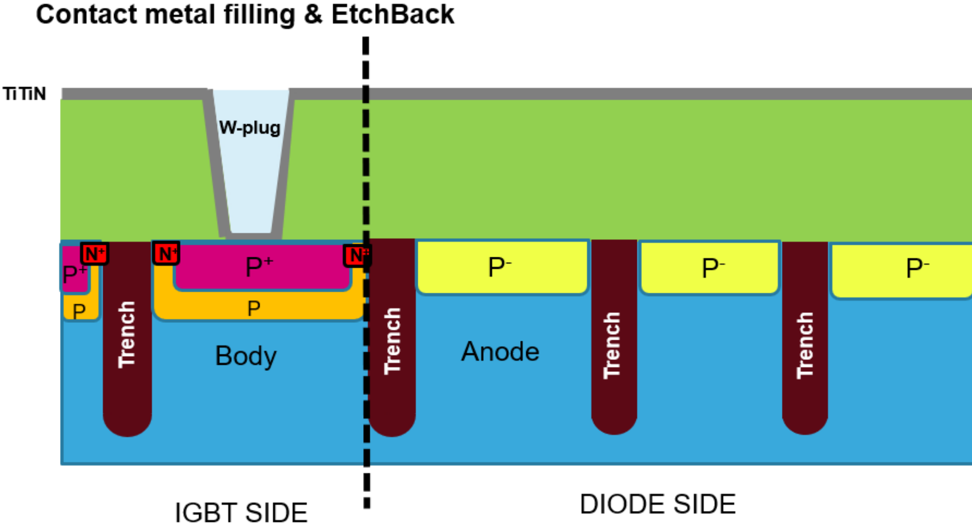

Figure 6.11: Contact metal filling

Contact metal filling

After the TiTiN barrier has been deposited, the contact must be filled with a tungsten plug, as the standard top metals (such as AlCu, AlSi or AlCuSi) do not provide adequate filling of the contact when the contact is very narrow (see Figure 6.11) [1].

TiTiN barrier stripping

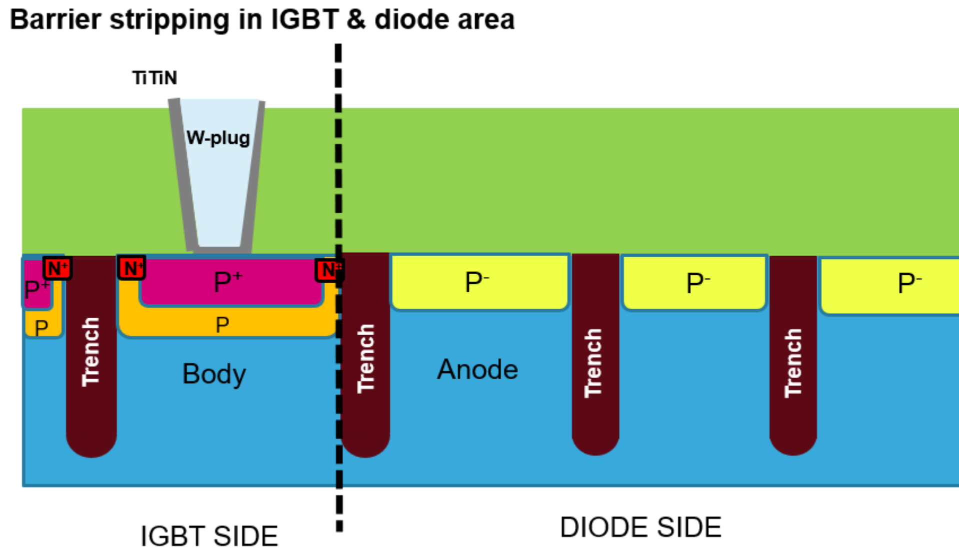

Figure 6.12: TiTiN barrier stripping

After filling with the tungsten plug, it is necessary to eliminate the TiTiN barrier from the dielectric layer (see Figure 6.12) [1].

Diode contact opening

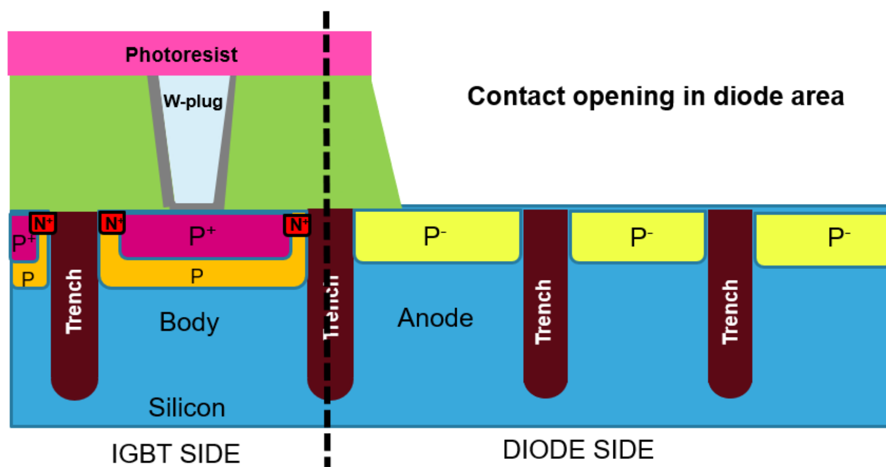

Figure 6.13: Diode contact opening

Subsequent to depositing the photoresist on the IGBT side, we remove the dielectric layer on the diode side, to expose the contact side and permit direct deposition of AlSi onto the silicon surface (see Figure 6.13) [1].

Contact enrichment implantation

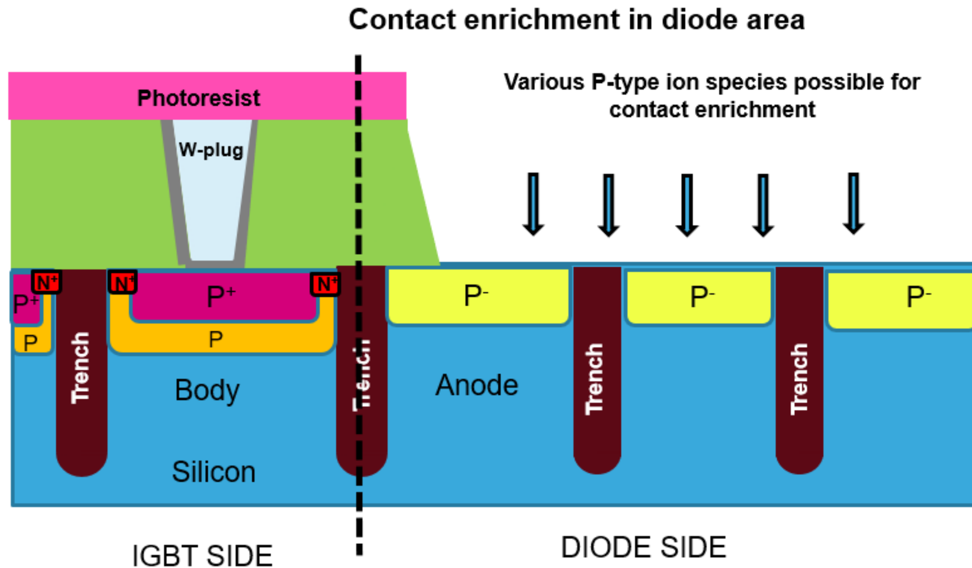

Figure 6.14: Contact enrichment implantation

The thirteenth step involves BF_2 implant. As we will see in the following section, this enrichment aids in creating a more ohmic contact on the diode side, since the anode, which is lowly doped, produces a Schottky contact (see Figure 6.14) [1].

Metal deposition

The fourteenth step is to deposit the AlSi metal on the top-side. On the diode side we will have a full contact, in which the trenches are floating because in the diode we have only two connections, the anode on the top-side and the cathode on the back-side. The trench is also maintained in the diode part to ensure a structural continuity and uniform modulation of the electric field throughout the active area (see Figure 6.15) [1].

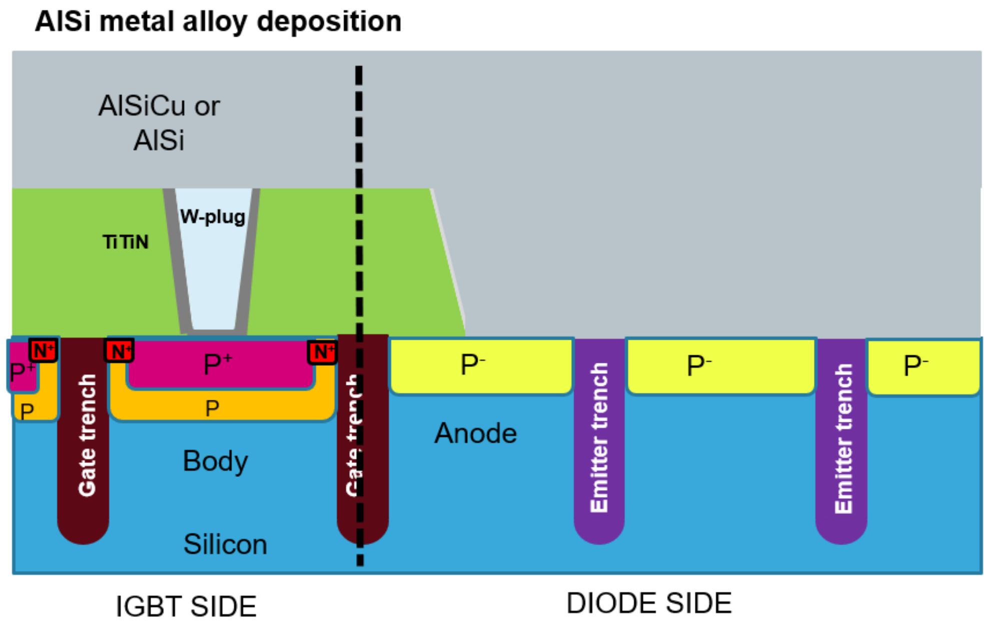

Figure 6.15: Metal deposition

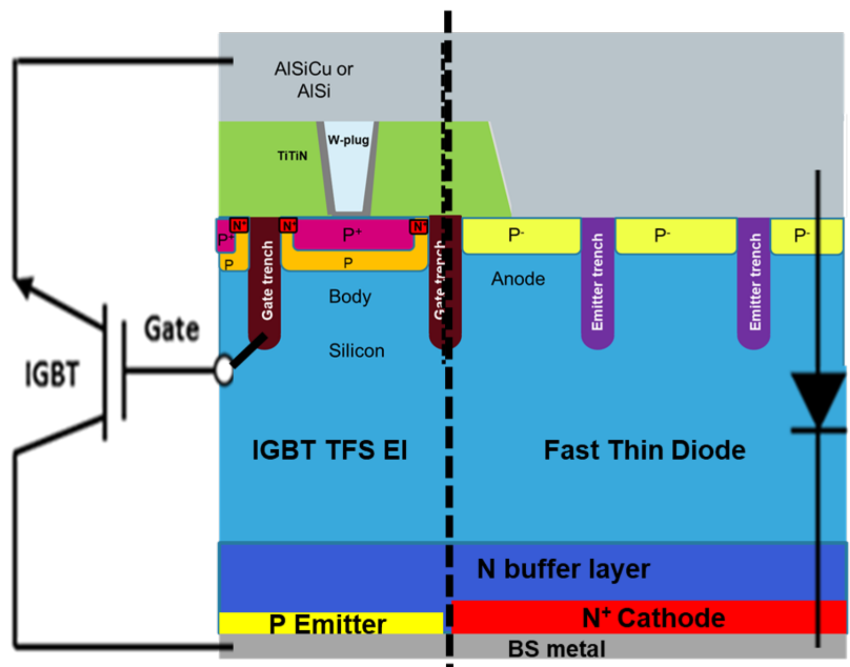

Figure 6.16: Final structure

Back-end finishing

The final steps are the back-side processes. The field stop, emitter and cathode are implanted and activated by laser. To make the cathode of the diode, we should make a photolithographic step in the backside to invert the doping. Finally, we will deposit the back metal [1]. The final structure can be seen in Figure 6.16.

6.2 Low Efficiency Injection Anode enabling low dose lifetime killing techniques

The aim of this Master's thesis is to demonstrate that diodes realised using the LEIA concept perform better than diodes realised using high electron irradiation dose as a lifetime killing technique. The LEIA concept is based on two fundamental points: the differentiation of the body of the IGBT from the anode of the diode, in which we reduce the injection efficiency, making a low doped anode, and the use of a lifetime killing technique with low doses and intensities. In this work, we decided to use electron irradiation as the lifetime killing technique, because devices irradiated with electrons do not show a negative temperature coefficient. It has been seen in the literature, that when a lifetime killing technique, such as platinum diffusion, is used, the forward voltage has a temperature dependence that decreases with increasing temperature, and therefore, has a negative temperature coefficient (see Figure 6.17). This is advantageous in terms of conduction losses, but this temperature behaviour is very unfavourable for diodes parallel connected. Within a power module, the different diodes may have a different forward voltage. In this case, the parallel connection led to attract more current to the diode with a lower voltage drop. As a result, the temperature of the device would rise. This would further reduce the forward voltage, so that this diode would attract a further percentage of current, and so on. Therefore, a strong negative temperature dependence can lead to thermal runaway of the diode [4].

In this work, a comparison will be provided between samples using electron irradiation at high dose as a lifetime killing technique, and samples using the LEIA concept and low electron irradiation dose.
By reducing the anode dose, we reduce the injection efficiency of the anode,

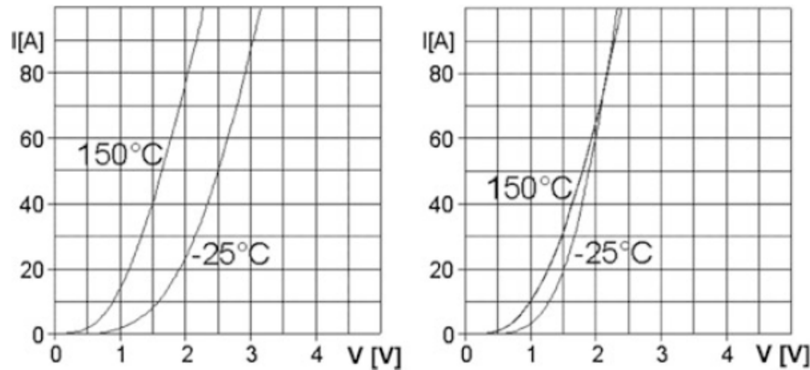

Figure 6.17: Forward characteristics of fast diodes and its temperature dependency. Left: platinum diffused diode. Right: Diode with electron irradiation [4]

so we have fewer charges to recombine during reverse recovery of the diode. This allows a faster recovery, keeping the value of V_{fec} not too high and reducing the reverse recovery charge Q_{rr}, the charge that has to recombine when the diode is turned-off [1].

6.3 Metal-semiconductor ohmic contacts

There are two types of metal-semiconductor contacts:

- **rectifying** (Figure 6.18);
- **ohmic** (Figure 6.19).

The Fermi level of two solids in contact must be equal at thermal equilibrium. The difference between the Fermi level and the vacuum level is called the work function. The work function is the minimum thermodynamic work required to remove an electron from a solid to a point in the vacuum, just outside the surface of the solid. A metal and a semiconductor in contact can have different work functions, ϕ_M and ϕ_S, respectively. When two materials are brought into contact, electrons flow from the material with the lower work function to the Fermi level at equilibrium. As a result, the material with the lower work function takes on a slightly positive charge and the material with the higher work function takes on a slightly negative charge.

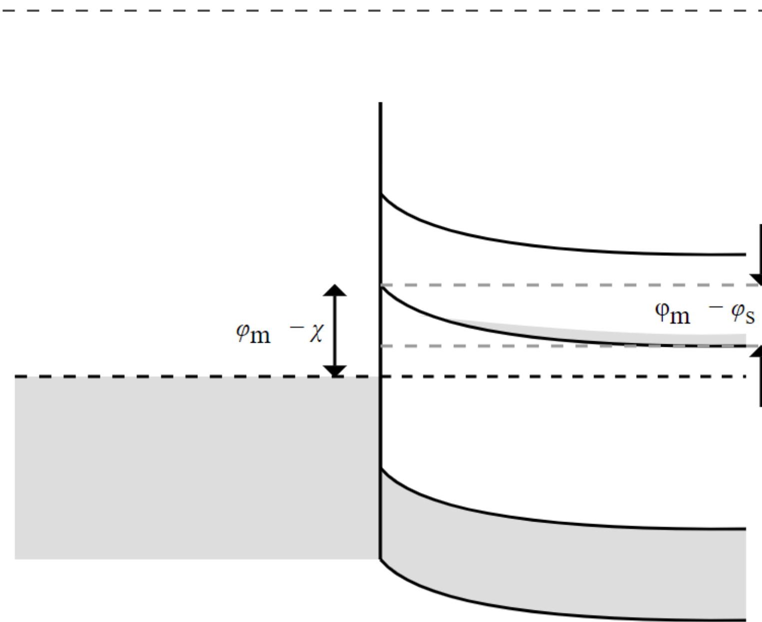

Figure 6.18: Metal-semiconductor rectifying junction

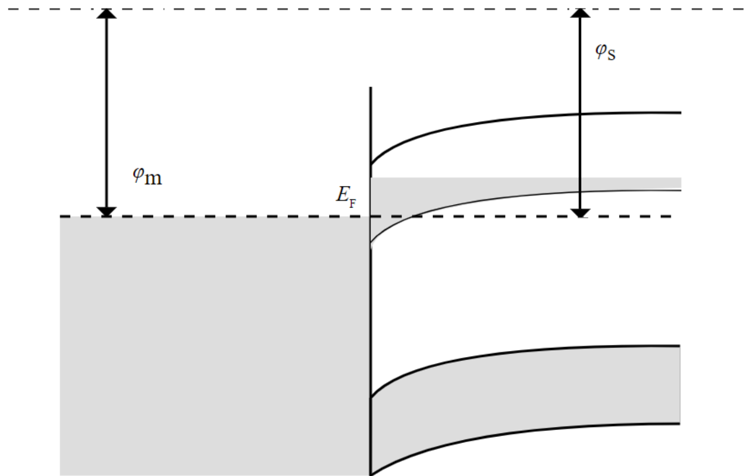

Figure 6.19: Metal-semiconductor ohmic junction

The resulting electrostatic potential is called the built-in potential V_{bi}. This built-in potential is responsible for band bending in semiconductors near the junction. In metals, the shielding length is so short that the electric field extends only a short distance from the interface, so no significant band

bending occurs [51]. To overcome the barrier, the charge carriers in the semiconductor must gain enough energy to jump from the Fermi level to the top of the bent conduction band. The energy required to overcome the barrier ϕ_B is the sum of the built-in potential V_{bi} and the offset between the Fermi level and the conduction band; for n-type semiconductors $\phi_B = \phi_M - \phi_S$, where ϕ_S is the electronic affinity of the semiconductor, i.e. the difference between the vacuum level and the conduction band (CB) level, and for p-type semiconductors $\phi_B = E_g - \phi_M + \phi_S$.
In order to minimise the on-state voltage drop and power dissipation during current conduction, it is important to have an ohmic contact in the n and p region, as the contact resistance must be as low as possible [44]. This can be achieved by using a metal-semiconductor contact with a low barrier height and a high doping concentration in the semiconductor, to promote tunnelling current through the contact. The most important property of ohmic contacts is their contact resistance R_c. For contacts with a high doping level, the contact resistance depends on the barrier height ϕ_B and the doping concentration N_D [44]:

$$R_c = e^{\frac{2\sqrt{\epsilon_S m^*}\phi_B}{h\sqrt{N_D}}} \tag{6.1}$$

where ϵ_S is the dielectric constant and m^* is the effective mass.

In Figure 6.20 we can see the dependence of the contact resistance R_c on the doping concentration and the barrier height ϕ_B.

In general, a metal contact on a low-doped semiconductor produces a rectifying contact [52]. This is because the more we dope the semiconductor, the more metallic the semiconductor behaves, so its work function approaches that of the metal, and this allows a more ohmic contact with low contact resistance.
In the proposed LEIA structure, the presence of the low-doped p anode can be a problem. We cannot use the standard IGBT contact because the TiTiN barrier on the low-doped silicon creates a very high contact resistance, forming a Schottky rectifying contact. This is because we have a gap between the work function of TiN (about 4.1eV) and the work function of the low-doped silicon p, which is similar to the work function of intrinsic silicon (about 4.6eV). This gap creates a high potential barrier that makes it difficult to extract electrons. To avoid this problem, we need to eliminate the IGBT

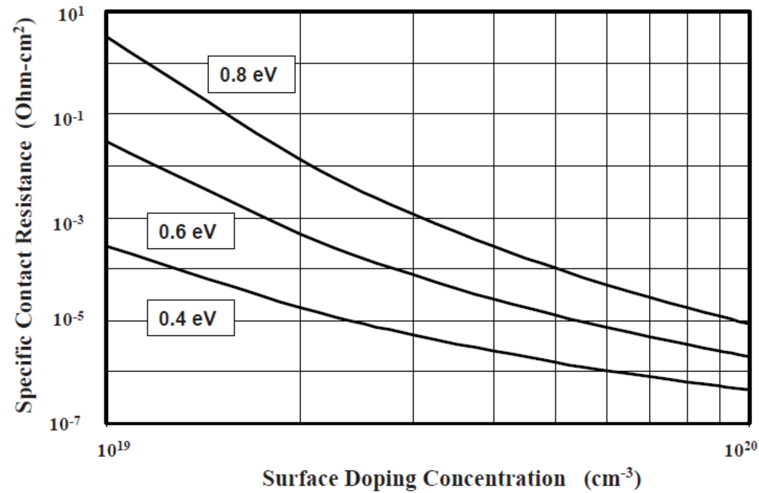

Figure 6.20: Specific resistance at metal-semiconductor contacts

contact with the TiTiN barrier and tungsten plug under the AlCu metal layer, and use an AlSi metal directly on the silicon surface.
We have to replace AlCu with AlSi because removing the TiTiN barrier can cause aluminium spikes in the silicon. The best solution in this case is to use AlSi or AlCuSi, aluminium with a certain percentage of silicon. This also makes the contact more ohmic by bringing the two work functions closer together.

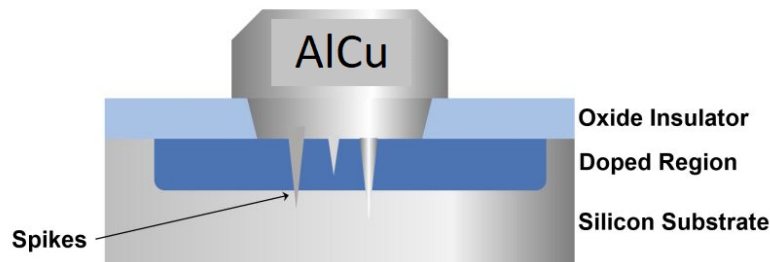

Figure 6.21: Aluminum spikes [53]

The use of pure aluminium or an alloy of aluminium and copper causes the silicon to diffuse into the metal. The semiconductor reacts with metallisation at only $(200-250)°C$. This diffusion of silicon creates cavities at the interface between the two materials, which are filled by the aluminium. This creates peaks, which can cause a short circuit if they pass through the

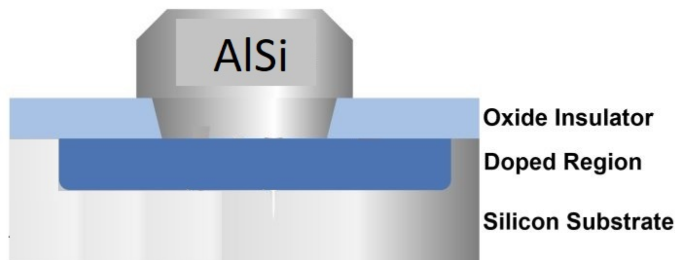

Figure 6.22: Contact without aluminum spikes [53]

doped region and reach the underlying silicon crystal. The size of this peak depends on the temperature at which the aluminium was deposited on the wafer [54].
This phenomenon can lead to the degradation of device performance, because it creates an undesirable path. By using a percentage of silicon in the metal, the aluminium spike can be avoided, because it reduces the solubility of aluminium in silicon.
In our device, we used aluminium-silicon alloy (AlSi) as the top metal, combined with a BF_2 enrichment implant to make the contact more ohmic. We decided to use a BF_2 enrichment implant because it allows the formation of a shallow enrichment, that reduces the contact resistance, but does not reduce the advantages of using the LEIA structure, because this enrichment is very superficial, but on the surface, it increases the value of the doping concentration. We were able to see this through TCAD simulations; in particular, we saw an improvement in the V_{fec} of the diode when we added the BF_2 enrichment implant to the simulated structure:

V_{fec} (15A) without BF_2	V_{fec} (15A) with BF_2
2.2847 V	1.1201 V

Table 6.3: BF_2 enrichment improvement

As we see in Table 6.3, we have a high improvement of V_{fec} (approximately half) because, in this way, the contact resistance becomes lower.

6.4 IGBT trade-off (no negative impact on the IGBT $V_{CE_{sat}}$)

In this thesis work, a comparison is made between diode samples speed up through the use of electron irradiation, compared to diode samples speed up using the LEIA concept. In the latter case, electron irradiation will be used, but with much lower doses than with irradiated samples.
The LEIA concept is used because we have to consider the fact that this structure will be integrated into the future RC-IGBT, and when we perform electron irradiation, this process is not selective. This means that we also irradiate the IGBT side in the RC-IGBT structure. The irradiation generates defects in the crystal lattice. These defects are partially recovered after annealing. This generates a deterioration of the $V_{CE_{sat}}$ of the IGBT, and thus an increase in conduction losses and an increase in leakage current. These problems deteriorate the performance of the device, so it is necessary to reduce the irradiation dose to avoid this and obtain a better compromise between the $V_{CE_{sat}}$ of the IGBT and the switching speed of the diode.
To demonstrate this, we decided to test the performance of diodes made with high doses of electron irradiation and diodes using the LEIA concept. In the next chapter, we will explain in more detail the tests we have carried out, both through simulations and measurements made on the samples.

Chapter 7

LEIA Diode as Propedeutic Structure

7.1 Proposed structure and flow

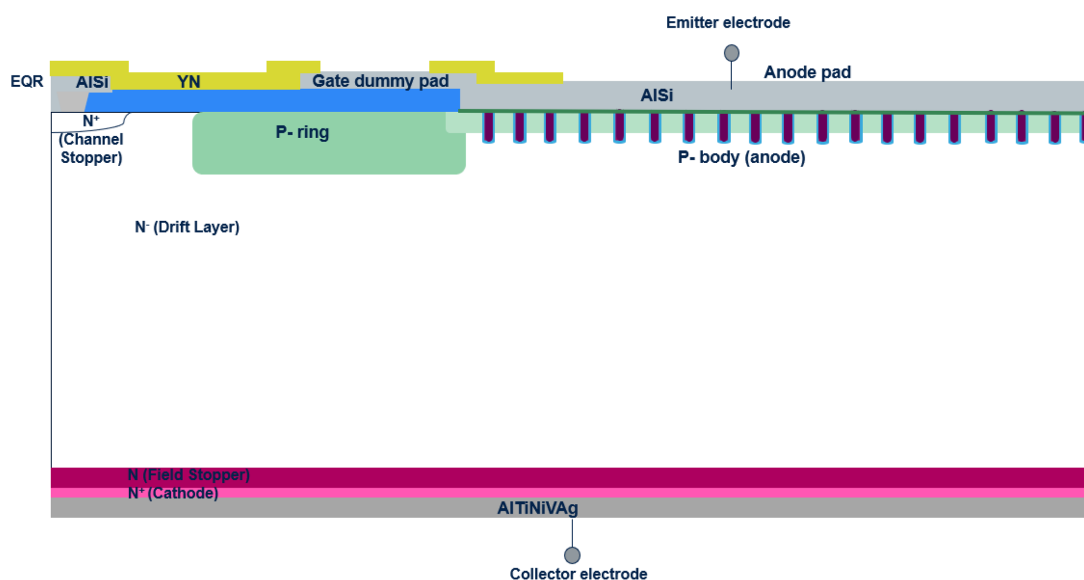

Figure 7.1: LEIA diode cross-section

The proposed structure, which we have realised for this thesis work, is a fast recovery diode. We can observe the cross-section of the device in Figure 7.1.

The structure is very similar to the standard IGBT. We have the trenches in the active area, like a standard IGBT, and the edge termination is the same. We decided to keep the trenches in the structure because this work is propaedeutic to the realisation of the RC-IGBT, where we will also keep the trenches in the diode side, to allow a structural continuity on the device, to have a constant modulation of the electric field and to reproduce exactly the part of the diode that will be integrated in the RC-IGBT. The main difference is the low doped anode, the absence of the p^+ source implants, the blanket contact and the presence of the cathode implant on the back, because after the standard processes we perform a cathode implant to invert the doping and obtain a diode to have a *pin* junction. In the edge termination we keep the ring dose p^- and the standard EQR implant.
To better describe the process steps that were performed to realise these diodes, let us consider the sequence of masks. We needed 11 mask levels. In Figure 7.2 we can see the alignment tree for these masks.

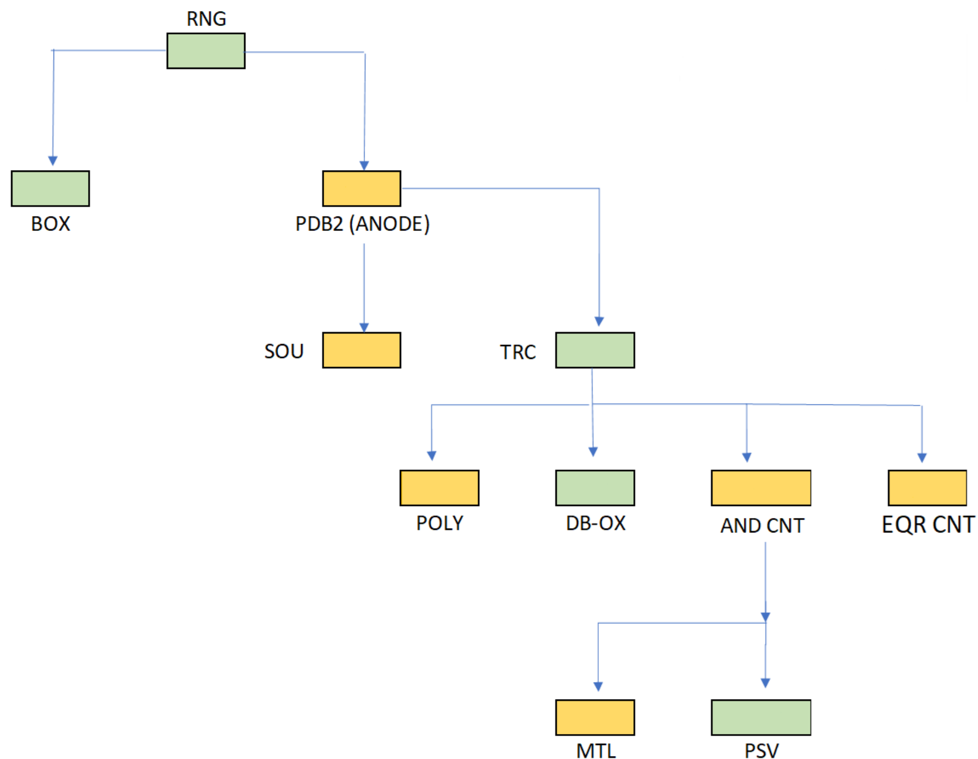

Figure 7.2: Alignment tree

In green we can see the masks that have remained unchanged from those of the standard IGBT, and in yellow the masks that we have modified. Below we will list the masks used and their function:

- **RING mask** → this is the first mask, used for implanting the ring in the edge termination. This mask is the same as the standard IGBT and leaves the alignment marks for subsequent masks;
- **BOX mask** → this second mask is the same in the standard IGBT. It is used for generating the BOX oxide. It aligns with the RING mask;
- **ANODE mask** → this third mask in a new mask. It is used for the Body/Anode implant and aligns with the RING mask;
- **SOURCE mask** → mask is different from the standard SOURCE mask in IGBTs, because it is not used for source implantation, but only for channel stopper implantation, as we do not have source implantation in the active area of the diode. It aligns with the ANODE mask;
- **TRENCH mask** → this fifth mask is the same in the standard IGBT. It is used for creating the trenches that will fill with the poly-silicon to form the gate. It aligns with ANODE mask;
- **OXIDE mask** → this mask is used to remove some of the oxide inside the trench for filling with poly-silicon. This mask is the same as the standard IGBT and aligns with the TRENCH mask;
- **POLY mask** → this seventh mask is different from the standard IGBT mask because the poly-silicon in this structure is only found inside the trenches. It aligns with the TRENCH mask;
- **ANODE CONTACT mask** → this contact mask is separate from the EQR CONTACT mask because we decided to perform two different types of etching, as the anode contact is a large aperture and requires wet etching compared to a small aperture in EQR. It aligns with the TRENCH mask;
- **EQR CONTACT mask** → this ninth mask is another contact mask. In this case we have to ecth in a small area. It aligns with the TRENCH mask;
- **METAL mask** → this mask is different from the standard IGBT mask, because we have a different type of etching. It aligns with the ANODE

CONTACT mask;

- **PASSIVATION mask** → this mask remains the same as the standard IGBT. It aligns with the ANODE CONTACT mask.

7.2 DOEs on silicon

For this thesis work, 25 silicon wafers were reserved for different splits in terms of irradiation doses and process flows.
Three wafers were sacrificed for testing the new process, in particular for verifying the contact etching, because in this new flow, compared to the standard IGBT flow, we have a blanket contact.
Three non-irradiated wafers were used for testing the possibility of activating BF_2 enrichment at a lower temperature. One wafer did a standard RTA (rapid thermal annealing) and two wafers a lower temperature RTA. This verification is important for the future RC-IGBT, because on the IGBT side we will use the TiTiN barrier, which is not compatible with high temperatures because it could be damaged.
The remaining wafers were divided into three groups. Seven wafers were not irradiated, in order to speed up the process, and thus to have preliminary data on this new concept. This is because electron irradiation is a process that is done in service, and therefore would have taken another 4 weeks in the flow timeline. These seven wafers are the wafers we tested to have a comparison with wafers that do not use the LEIA concept, and therefore treated with higher irradiation doses.
The remaining wafers are divided into two flow sequences. Six wafers will perform the irradiation after the back-side implants (field-stop, emitter and cathode implant) and after the activation with the laser annealing and six wafers before the back-side implants activation. This can generate two different lifetime profiles in the devices. Devices with irradiation after laser activation of the back-side implants will have a uniform lifetime profile in the entire device, because the beta irradiation creates a uniform defectness profile; as the electrons penetrate the entire thickness of the device, they displace the lattice atoms, creating defect centres that decrease the lifetime of the carriers (Figure 7.4). In the second case, when we perform laser annealing to activate the back-side implants after irradiation, we recover part of the defects created by the irradiation. In this case, we expect that the

lifetime profile is not uniform, but that there is a higher lifetime in the back-side and a lower lifetime in the bottom-side of the device, because the laser can generate defect recovery in the first microns of the device (Figure 7.3).

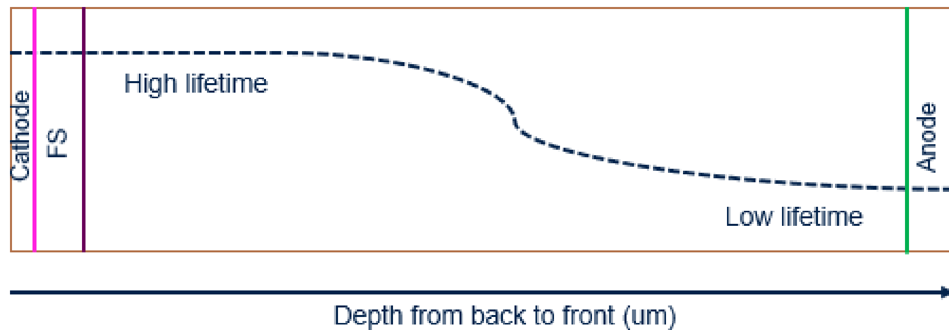

Figure 7.3: Irradiation before the back-side implantations

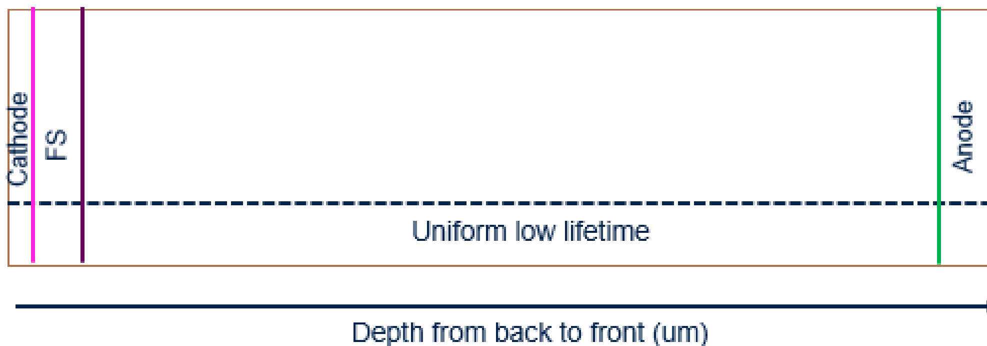

Figure 7.4: Irradiation after the back-side implantations

In Figure 7.3 we can see a non-uniform defectness profile, because in the proximity of the anode junction, the final lifetime will be determined (controlled) only by the beta electron irradiation, since the effect of the laser thermal wave is greatly reduced in this region.
With regard to the 12 wafers that will be processed by electron irradiation, we decided to perform three different irradiation doses:

- 2+2 wafers $\rightarrow$ 0.5Mrad;

- 2+2 wafers → 2Mrad;
- 2+2 wafers → 5Mrad.

For us, it is important to have as much information as possible on the effect of different irradiation doses on the device, as this will enable us to build a more accurate model of irradiation dose-related defects, to be implemented in the simulator, which will help us in the development of new technologies. Returning to the different irradiation doses, for the 5Mrad split we decided to perform one wafer with RTA at a lower temperature and one at a higher temperature to test the possibility of activating the BF_2 at a lower temperature.

In the Table 7.1 and Table 7.2 we can see the split matrix realised for this batch of silicon. In the first table (Table 7.1) we can see the different dose and RTA splits, and in the second (Table 7.2) the splits of the three different flows: non-irradiated, irradiated before laser activation and irradiated after. Another important thing to emphasise is that we have decided to maintain the emitter implant in the flow, even though we are making a diode, because this work is preparatory for future RC-IGBT in which we will not have a photolithography mask, as far as the emitter implant is concerned, but will solely have the cathode mask, and thus we will have a blanket emitter implant.
The measurements we carried out to demonstrate the improvement due to the new LEIA concept, were performed on wafers not irradiated by the accelerated flow. These measurements were compared with the measurements made on the old diode wafers with standard anode dose and accelerated with high irradiation doses (10Mard and 15Mard). This work will, of course, be continued and concluded as soon as we also have wafers with LEIA diodes with irradiation.

7.3 TCAD simulation for preliminary data

The simulations were performed using Sentaurus. Sentaurus is a TCAD simulator developed by Synopsys. TCAD stands for Technology Computer-Aided Design and refers to the use of computer simulations to develop and optimise semiconductor process technologies and devices.
Sentaurus consists of several tools. For this thesis work, we used the following tools in particular:

Wafer	NI	0.5Mrad	2 Mrad	5 Mrad	RTA standard	RTA lower
1	X				X	
2	X				X	
3	-	-	-	-	-	-
4	X					X
5	X					X
6	-	-	-	-	-	-
7		X			X	
8		X			X	
9	X				X	
10	X				X	
11			X		X	
12			X		X	
13	-	-	-	-	-	-
14	X				X	
15				X	X	
16				X		X
17		X			X	
18		X			X	
19	X				X	
20	X				X	
21			X		X	
22			X		X	
23	X				X	
24				X	X	
25				X		X

Table 7.1: Split matrix 1

- Sprocess;
- Sdevice;
- Svisual;
- Sde;
- Inspect.

Wafer	Irradiation after	Irradiation before	NI
1	-	-	-
2			X
3	-	-	-
4	-	-	-
5	-	-	-
6	-	-	-
7	X		
8	X		
9			X
10			X
11	X		
12	X		
13	-	-	-
14			X
15	X		
16	X		
17		X	
18		X	
19			X
20			X
21		X	
22		X	
23			X
24		X	
25		X	

Table 7.2: Split matrix 2

With Sentaurus Process (Sprocess), we simulated the processes and integrated them into a complete front-end process flow. We performed oxidations, diffusions, implantations, depositions, thermal annealing and combined them with robust mesh generation. For our simulations, we preferred to run 2D simulations, because the computational cost of running 3D simulations is onerous. We observed that the results obtained from 2D simulations are accurate enough, that 3D simulations are not required.
Sentaurus Device (Sdevice) is a device simulator capable of simulating the

electrical, thermal and optical characteristics of silicon-based and compound semiconductor devices. In particular, we performed static and dynamic simulations with this tool, running a mixed-mode simulation.
With Svisual, we observed simulation results with regard to structure, doping, electric field, current distribution and other electrical and process characteristics.
Sde allowed us to modify the mesh grid for the device simulation, after the process simulations and to define the lifetime in different regions of the device.
Finally, with Inspect we extracted the curves and values from the curves simulated by Sdevice.

7.3.1 Process simulation

The first step in the simulation of the process is to define the simulation grid mesh. In this work, we considered an elementary cell of $4\mu m$. We started by constructing the upper half of the device ($2\mu m$) and defining the wafer resistivity:

```
line y loc=0.0   tag=Mid         spac=0.1
line y loc=2.0   tag=Right       spac=0.1

line x loc=0.0    tag=SiTop       spacing=0.05
line x loc=2.0                    spacing=0.05
line x loc=6.0                    spacing=0.08
line x loc=10.0   tag=SiBottom    spacing=1.0

region silicon xlo=SiTop xhi=SiBottom ylo=Mid yhi=Right

init resistivity=@res_sub@ field=Phosphorus wafer.orient=100
```

Then we ran the whole process, defining the recipe used in the actual process. The main commands used were:

```
implant boron dose=@BodyDose@ energy=@BodyEnergy@ tilt=7
rotation=22 #for implantation

diffuse temp=700 time=60 ramprate=5.0<C/min> flowN2=8.0
flowO2=0.08 #for diffusion
```

```
deposit poly thickness=0.3 type=isotropic #for deposition

mask name=m_source left=0.0 right=1.2 #for mask definition

etch oxide anisotropic thickness=0.15 mask=m_source #for ecthing
```

We continued until the trench was filled with polysilicon, after which we reflect the structure over to obtain the entire elementary cell (see Figure 7.5):

```
transform reflect right
```

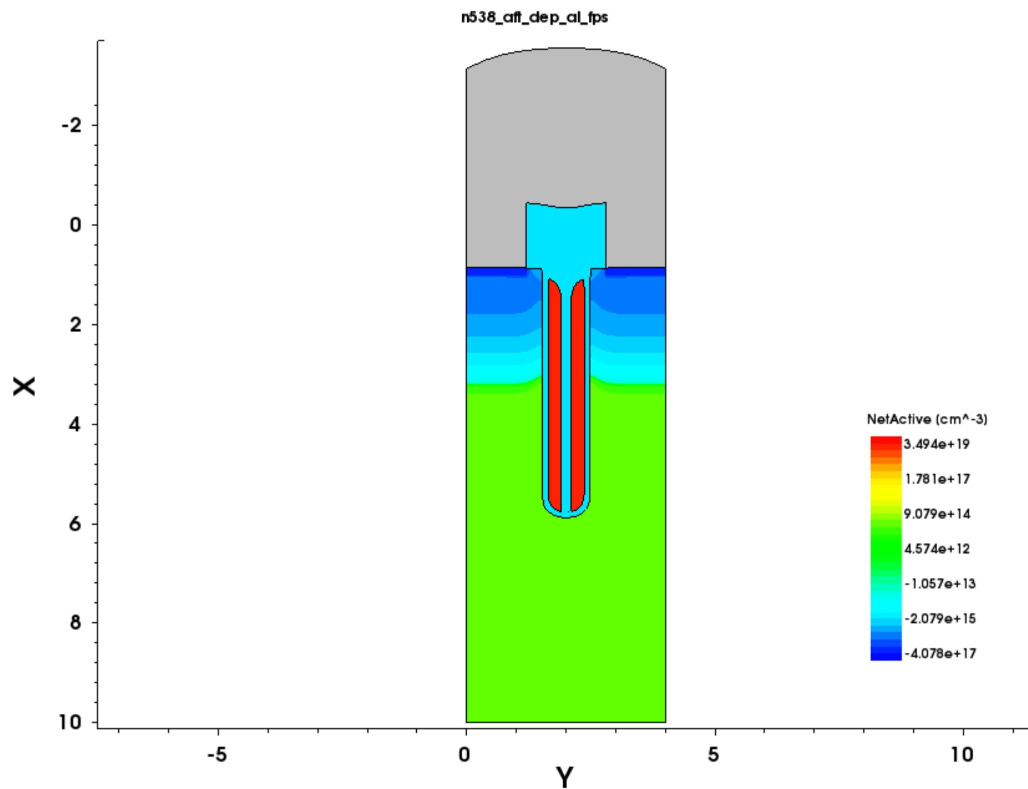

Figure 7.5: Upper side LEIA diode from Sentaurus Svisual

In Figure 7.6 we can observe the two structures compared. In the structure on the left, we can clearly see that the anode has a much lower doping.

After that, the structure was stretched and the back-side implants were performed:

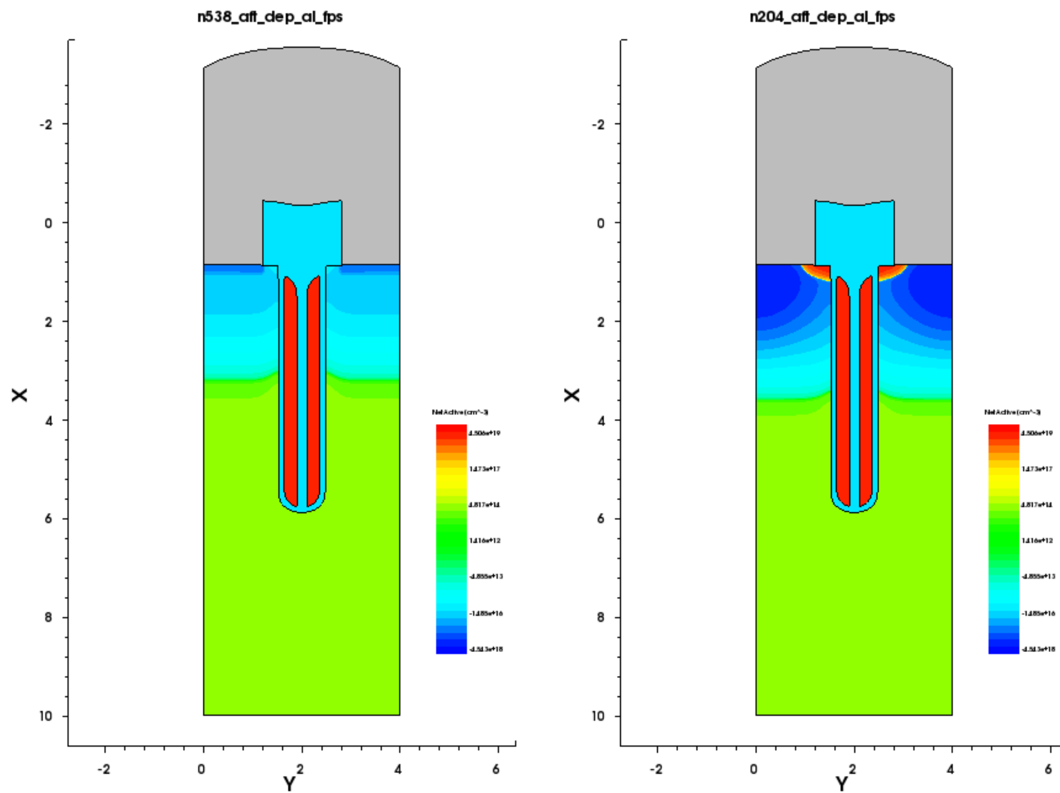

Figure 7.6: Left: LEIA diode top structure; Right: Standard diode top structure from Sentaurus Svisual

```
transform stretch location=10.0 length=@length_str@ down

implant phosphorus dose=@FSDose@ energy=@FSEnerg@ tilt=0 rotation=0

implant boron dose=@EmiDose@ energy=@EmiEnerg@ tilt=0 rotation=0

profile infile=ProfilocatodolaserUV.txt silicon name=Phosphorus
```

The field stop implant and the emitter implant were simulated by implanting them from the process. The cathode profile, on the other hand, was extracted from a profile from the spreading analysis and loaded via a .txt file.
The last step in the process simulation is the definition of the contacts, which will then be used for device simulations (see Figure 7.7):

```
contact name=anode  point x=-2.0  y=2.0  replace

contact name=gate  box xlo=1.0  ylo=1.6  xhi=6.0  yhi=2.4
PolySilicon

contact name=catode  point x=75.05  y=0.0  replace
```

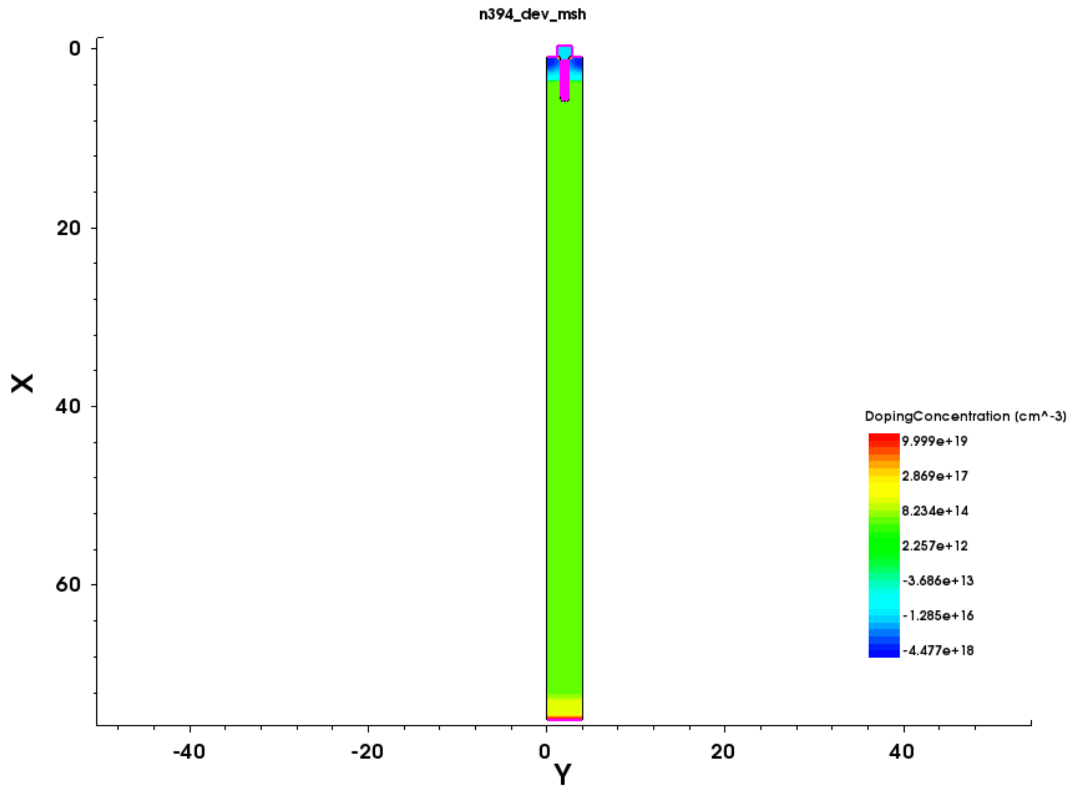

Figure 7.7: Final Sprocess structure from Sentaurus Svisual

This structure is a 3-terminal structure because it is based on the layout of an IGBT, but from an electrical point of view, during device simulations the anode and gate will be placed at the same potential.

It should be emphasised that the real structure of this diode is a structure formed by many elementary cells, all equal to each other, forming an array of elementary cells. In device simulations, therefore, a parameter called 'Area factor' (Af) has been introduced, which allows us to simulate the real area of the device.

Finally, after the process simulation, using SDE we went on to define the grid mesh for the device simulations. In the middle part of the substrate, we left a looser grid and went to refine the top (important for the formation of the channel, which would affect the threshold voltage) and the bottom where the back-side implants were made.
After that, we defined the lifetime profile for the electrons and holes in the device, differentiating the top of the device from the bottom. In the top we have introduced a higher lifetime than in the bottom, as we imagine that in the back, due to the processes carried out, the lifetime is lower.
In Figure 7.8 we can see the mesh grid generated by Sentaurus SDE.

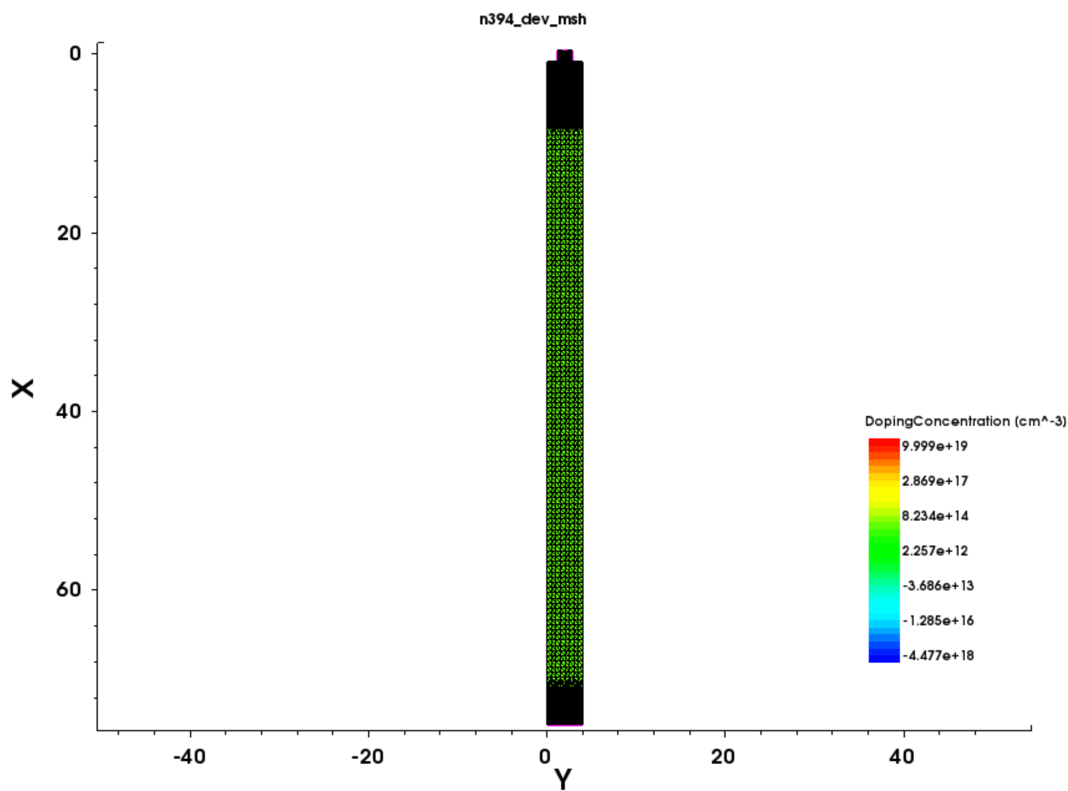

Figure 7.8: Sentaurus SDE mesh grid

7.3.2 Device simulation

We can divide the device simulations that have been performed in two categories:

- **static simulations**;
- **dynamic (mixed-mode) simulations**.

We started from static simulations in order to extract the V_{fec} values of the diodes.
In order to be able to simulate the formation of trap levels for acceptors and donors, due to electron irradiation, a model was included in the "Physics" section of Sdevice:

```
Traps(Acceptor Level Conc=@conc@ EnergyMid=0.27 fromValBand
      eGfactor=1 hGfactor=1 eXsection=8e-13 hXsection=9.5e-15)

Traps(Donor Level Conc=@conc@ EnergyMid=0.16 fromCondBand
      eGfactor=1 hGfactor=1 eXsection=2e-15 hXsection=2e-15)
```

The energy levels and capture sections were deduced from the literature [55]. The density of donors and acceptors was derived by means of a fitting we made from experimental measurements of irradiated 15Mrad and 10Mrad devices. The best fitting was found with a density of $1.5e13cm^{-3}$ for the 15Mrad dose and $1e13cm^{-3}$ for the 10Mrad dose. Using these results, by a linear fitting, we derived the possible densities of the simulated irradiation doses. In the future, when we have the results on the diodes irradiated with the other irradiation doses, we will be able to further improve this model, which will allow us to make very accurate estimates, and thus, allow us to better choose the most appropriate irradiation dose for the device to be designed.
The introduction of trap levels is a way of modifying the lifetime of the device. The lifetime has a dependency on the irradiation dose [55]:

$$\frac{1}{\tau_f} = \frac{1}{\tau_i} + K\phi \tag{7.1}$$

where τ_i and τ_f represent the lifetime of the minority carriers before and after irradiation, K is the radiation damage coefficient and ϕ the electron radiation dose.

Mixed-mode simulations consist of simulating the dynamic behaviour of the device. The device is inserted into a circuit and switched on and off via a series of pulses. The circuit used in the simulations is as follows (see Figure 7.9).

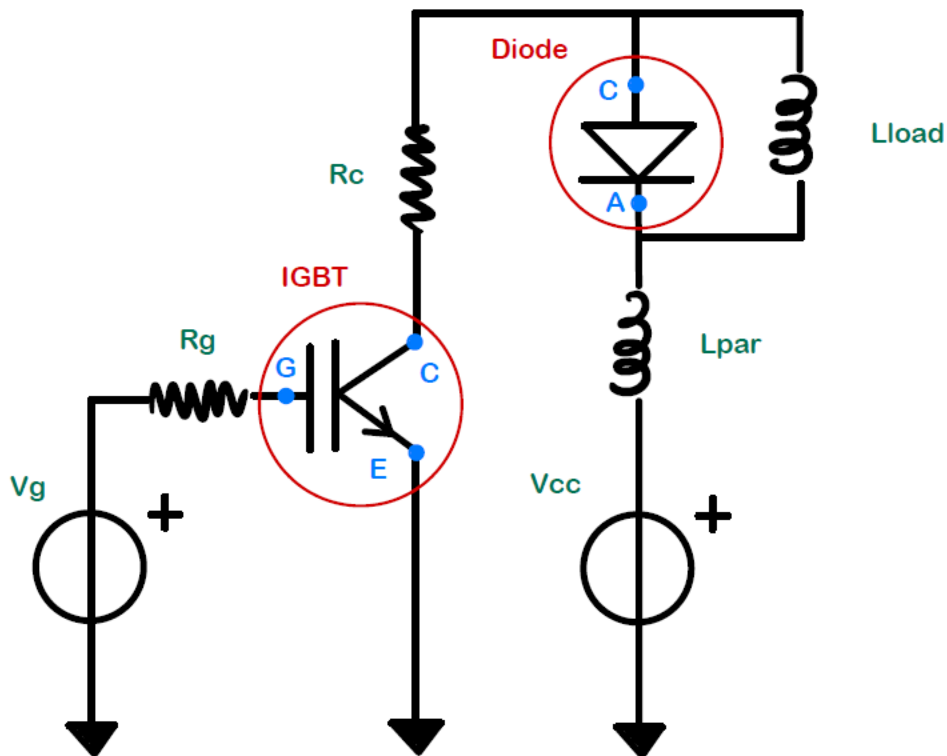

Figure 7.9: Simulation circuit

It is a circuit that simulates the application of the diode. In the low side we find the IGBT and in the high side the diode. The diode switches on an inductive load, which in our simulation is represented by the inductance L_{load}. The parasitic inductance of the circuit is represented by the inductance L_{par}.
The structures included in our simulations are process simulated structures.

7.3.3 Simulation results

We simulated the following cases:

- LEIA diode without irradadiation (NI);
- LEIA diode with 0.5Mrad dose;
- LEIA diode with 2Mrad dose;
- LEIA diode with 5Mrad dose;
- Diode with 10Mrad dose;
- Diode with 15Mrad dose;
- IGBT NI;
- IGBT with 0.5Mard dose;
- IGBT with 2Mard dose;
- IGBT with 5Mard dose;
- IGBT with 10Mard dose;
- IGBT with 15Mard dose;

In order to simulate electron irradiation, we set up the following concentrations at the trap levels (see Table 7.3):

Dose (Mrad)	Concentration (cm^-3)
NI	0
0.5	5e11
2	2e12
5	5e12
10	1e13
15	1.5e13

Table 7.3: Trap levels concentration

With regard to simulations of devices without the LEIA concept, with the 10Mrad and 15Mard irradiation doses, we performed 2 types of simulation. This is because the samples in our possession do not have an optimised contact resistance, and therefore have a particularly high V_{fec}. Consequently,

we simulated both the case in which the contact resistance was not optimised (see Figure 7.10) and the case in which it was (see Figure 7.11).

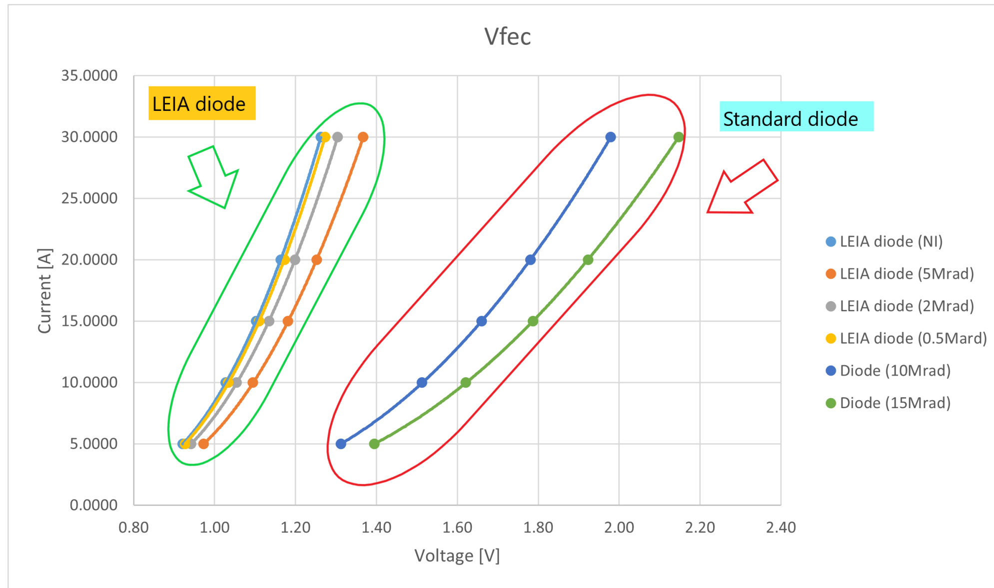

Figure 7.10: V_{fec}

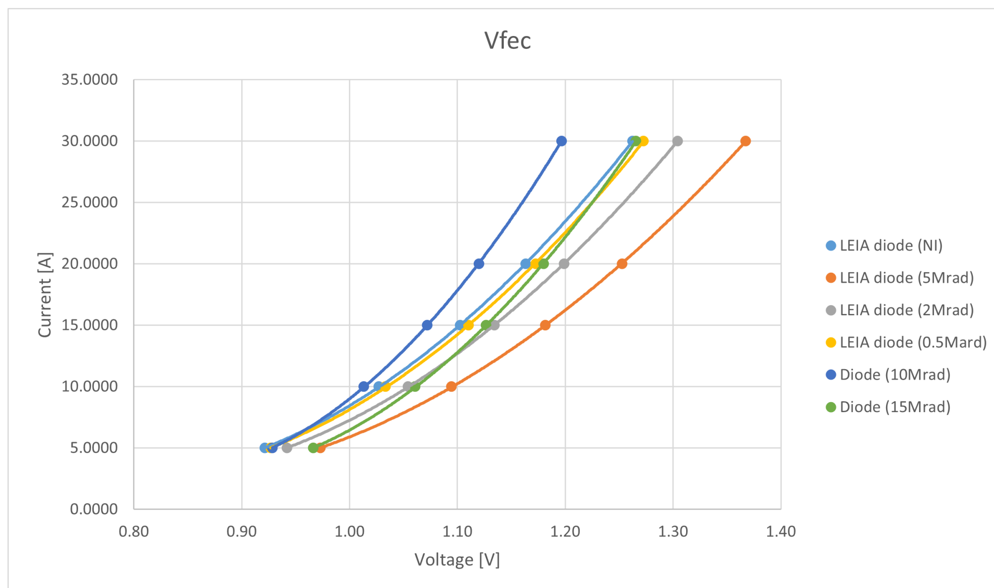

Figure 7.11: V_{fec} optimised

We can observe that the non-irradiated LEIA diodes and the LEIA diodes

with 0.5Mrad dose have a very close V_{fec}, as we expected. It is clear from the Figure 7.11, that at low currents the V_{fec} of the 15Mrad is very close to the non-irradiated LEIA case and at higher currents the latter is closer to the 10Mard.
The simulated values are shown in tables at the end of the section.
To better understand the benefits of the LEIA structure, we simulated the trade-off curves, in which the value of V_{fec} at 15A is shown on the x-axis and the value of Q_{rr} on the y-axis (see Figure 7.12 and Figure 7.13).

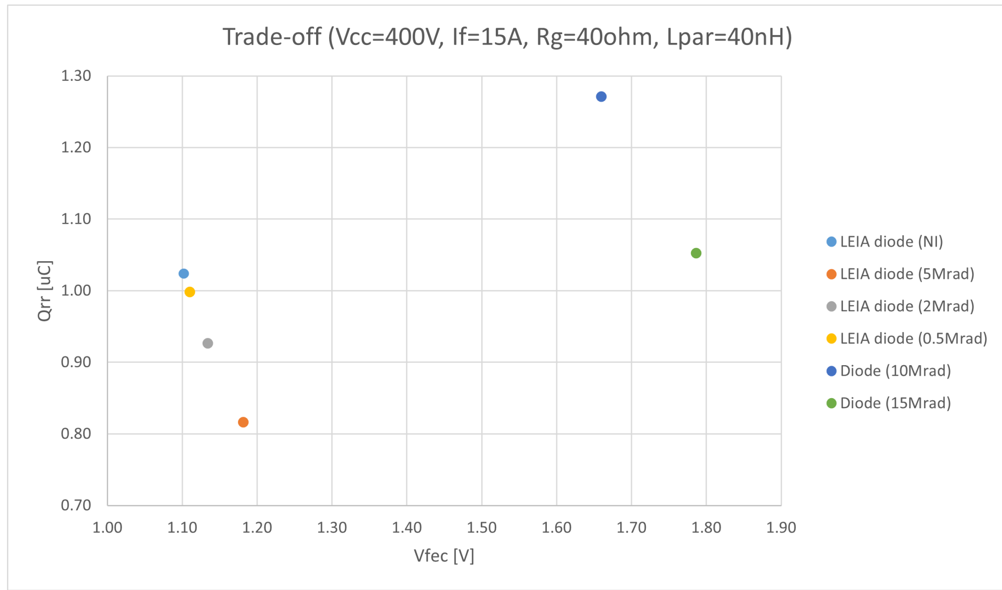

Figure 7.12: Trade-off diode (V_{cc}=400V, I_F=15, R_g=40ohm and L_{par}=40nH)

In this simulation, measurement conditions were set for a V_{cc} of 400V, a diode switch-off current I_F of 15A, an input resistance R_g of 40ohm and finally, a parasitic inductance L_{par} of 40nH to obtain a dI/dt of approximately $1210A/\mu s$ was set.
It is important to emphasise that to modify the dI/dt of the diode during switch-off, the parameter to be adjusted is the input resistance R_g. The parasitic inductance L_{par} plays a fundamental role on the softness parameter s of the diode.
As we can see from the Figure 7.13, the trade-off curve of LEIA diodes is shifted lower than those made with the standard process. This allows us to have a lower V_{fec} for the same Q_{rr}. It should also be noted that the

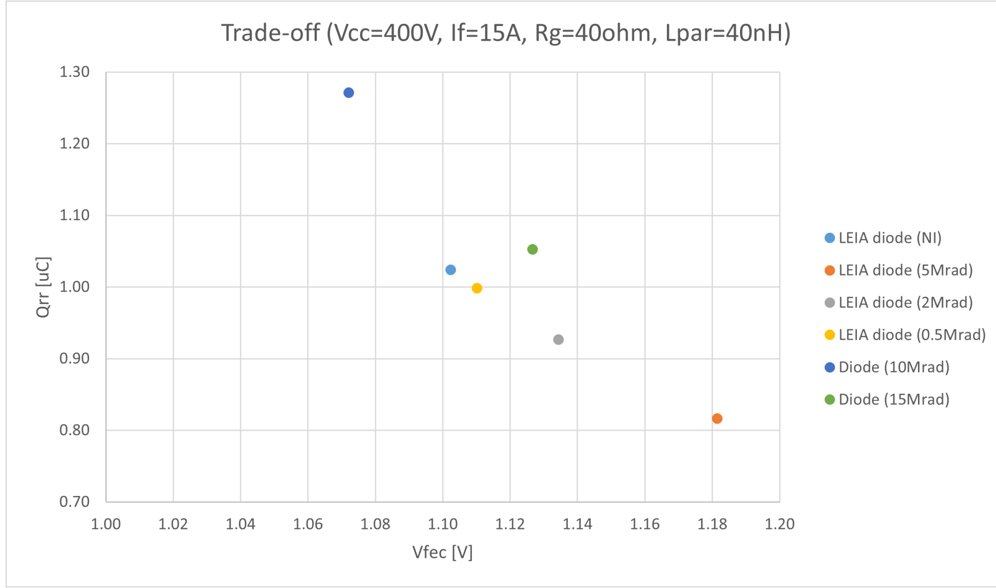

Figure 7.13: Trade-off diode with V_{fec} optimised (V_{cc}=400V, I_F=15, R_g=40ohm and L_{par}=40nH)

value of Q_{rr} of the non-irradiated LEIA diode is close to the value of the diode with the standard process irradiated 15Mrad. This is an important result because it means that we can achieve very similar diode performance by lowering the irradiation dose by quite a bit. This is a very good result in terms of the $V_{CE_{sat}}$ of the IGBT, in which the diode is integrated, and therefore in terms of conductivity loss and current leakage.

As expected, from the Figure 7.14 we can observe an increase in the $V_{CE_{sat}}$ of the IGBT as the irradiation dose increases. This is because the irradiation process is not a selective process, and therefore when we irradiate the device, we impact the performance of the IGBT.

Considering the measurement conditions, these simulations were repeated. In this case, the measurement conditions were, V_{cc} of 100V, I_F of 5A, R_g of 250ohm with a dI/dt of $40A/\mu s$ and a L_{par} of $2\mu H$ (see Figure 7.15 and Figure 7.16).

From the Figure 7.16 we can see that at 15Mrad we are close in Q_{rr} to the LEIA 2Mrad case. This allows us to maintain low irradiation doses and still have devices that are fast.

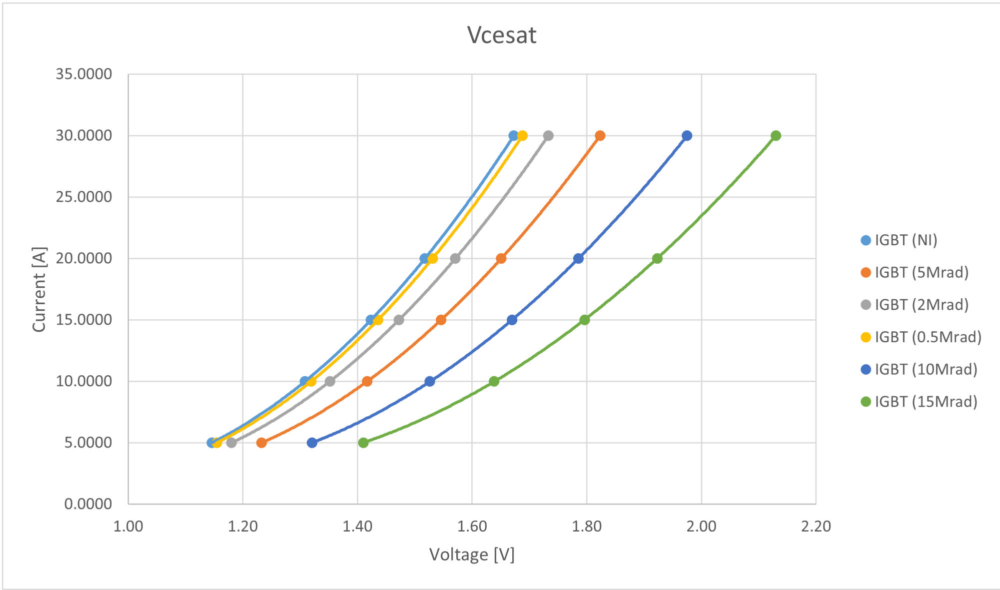

Figure 7.14: $V_{CE_{sat}}$

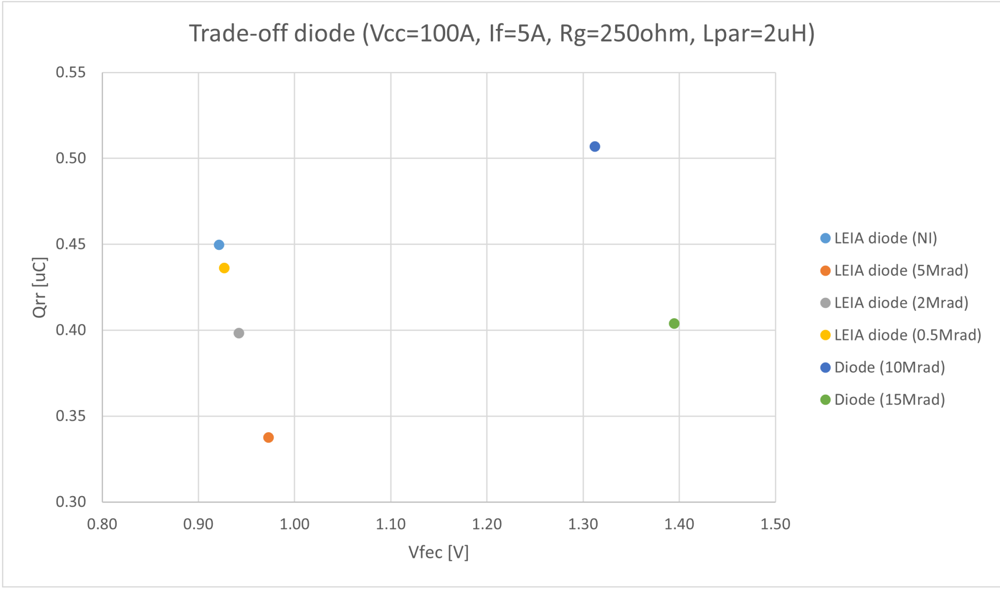

Figure 7.15: Trade-off diode (V_{cc}=100V, I_F=5, R_g=250ohm and $L_{par}=2\mu H$)

Another important term of comparison is the trade-off curve of the IGBT (see Figure 7.17). The point circled in red corresponds to the standard IGBT. It can be seen that if we maintain low irradiation doses (0.5Mrad,

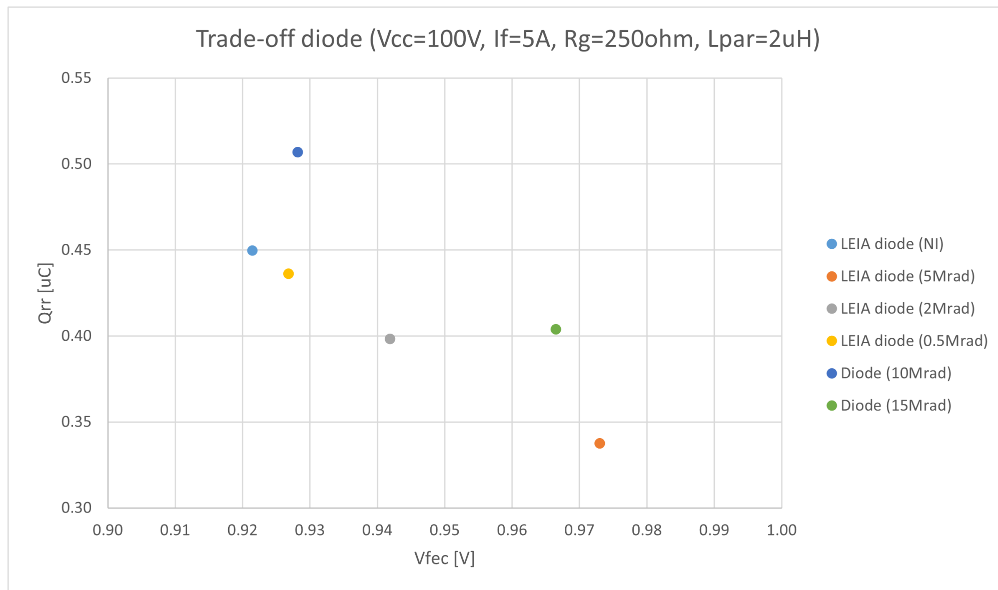

Figure 7.16: Trade-off diode with V_{fec} optimised (V_{cc}=100V, I_F=5, R_g=250ohm and $L_{par}=2\mu H$)

2Mrad, etc.), the performance of the IGBT does not change abruptly.

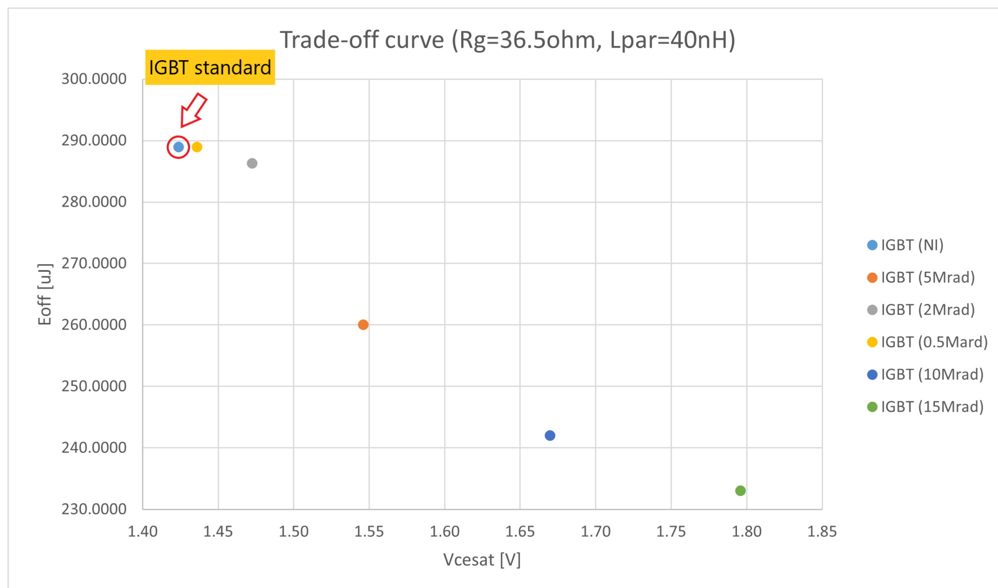

Figure 7.17: Trade-off IGBT

Finally, in the Figure 7.18 we can see the diode switching simulated at

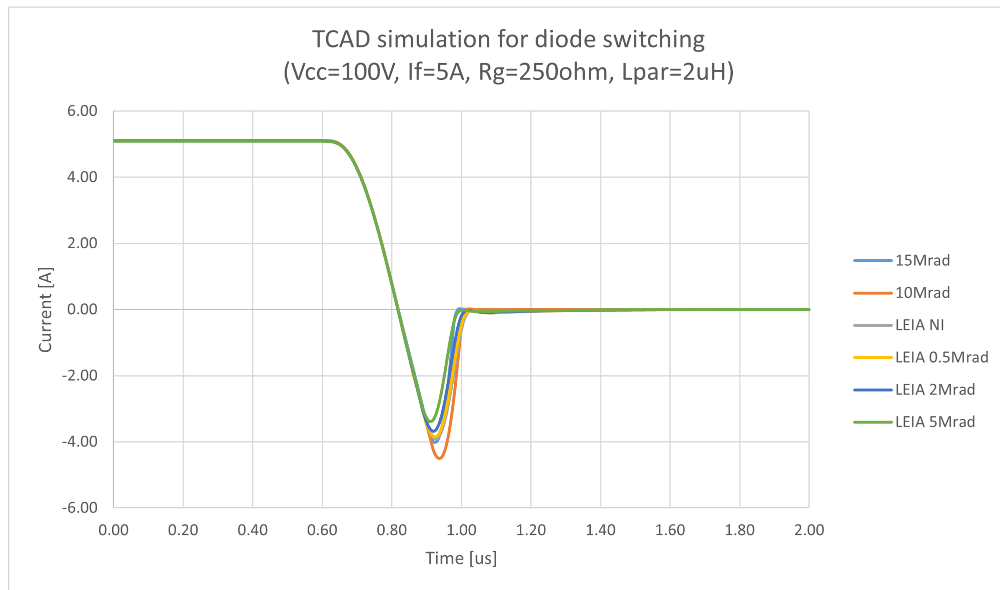

Figure 7.18: Switching behaviour of the diode, simulated at measurement conditions

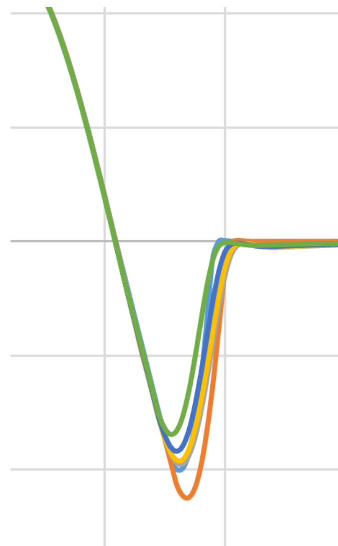

Figure 7.19: Zoom Figure 7.18

measurement conditions. This aspect will be discussed in more detail in the following sections.
At the end of this chapter are the tables with the simulated data.

7.4 Measurement equipment

Equipment used for measurements:

- MPI TS2000-DP prober station;
- Keysight B1505A Curve Tracer;
- Tektronix DPO7054 Digital Phosphor Oscilloscope;
- Tektronik AFG3022B Dual Channel Arbitrary/Function generator;
- 2 Power Supplies;
- Tektronix TCP0030 Current Probe;
- 3 Voltage probe;
- Measurement Circuit;

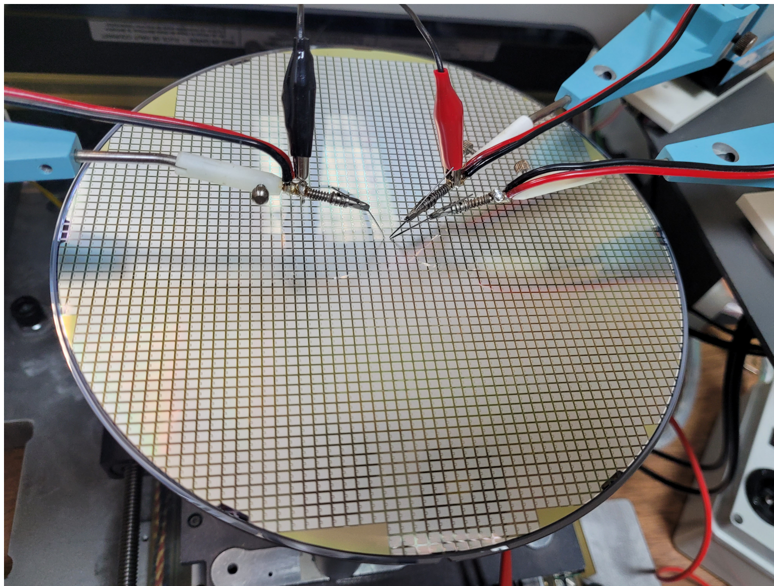

Figure 7.20: Wafers under testing

Static measurements of V_{fec} and leakage current were performed using the MPI prober station and the Keysight Curve Tracer. We dropped three tips on the die, as we can see in the Figure 7.20, two of them on the anode and one on the gate pad, as each of these tips can tolerate up to 10A. We wrote a program which, via Keysight, extracted the V_{fec} values at the currents we

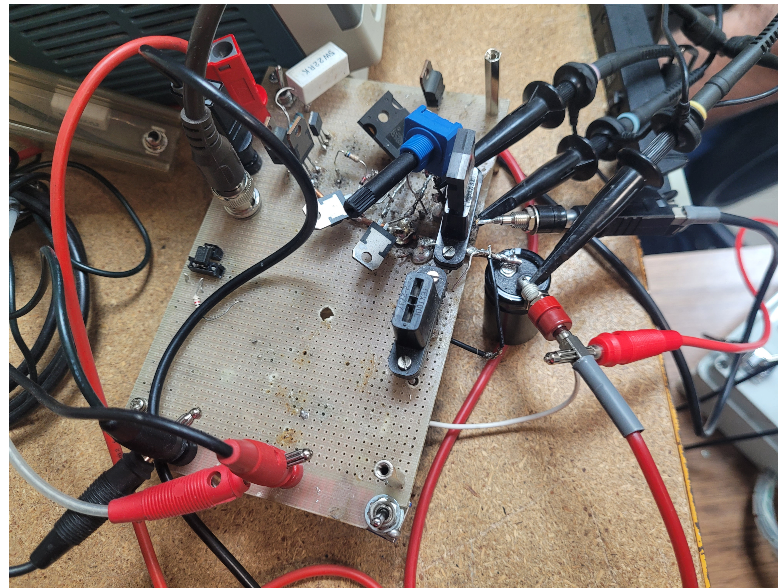

Figure 7.21: Circuit used for diode switching

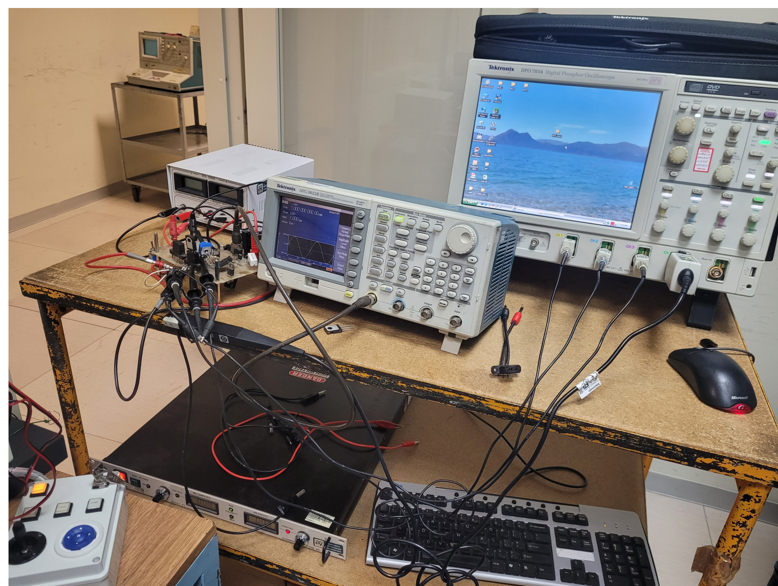

Figure 7.22: Dynamic measurement equipment

wanted and the leakage current values at 480V and 600V (80% and 100% of the nominal voltage of the device, which is 600V).
Anode and gate were at the same potential.

For the dynamic switching measurements of the diode, we used the circuit in the Figure 7.21. Via a power supply we provided power to the low-side device (an IGBT was used), and via a second power supply we provided V_{cc} to our diode. The on/off pulse was given via a function generator. Using four probes connected to the oscilloscope we went to capture the voltage at the anode, cathode and gate of the device, and with the current probe we went to capture the forward current of the diode.
In Figure 7.22 we can see the dynamic measurement equipment.

7.5 Static characterization

We performed measurements of V_{fec} on three wafers:

- LEIA diode non-irradiated;
- Standard diode 10Mrad;
- Standard diode 15Mard.

The extrapolated values are shown in the Table 7.10. They refer to average values, as we sampled several wafer dies with MPI prober station.

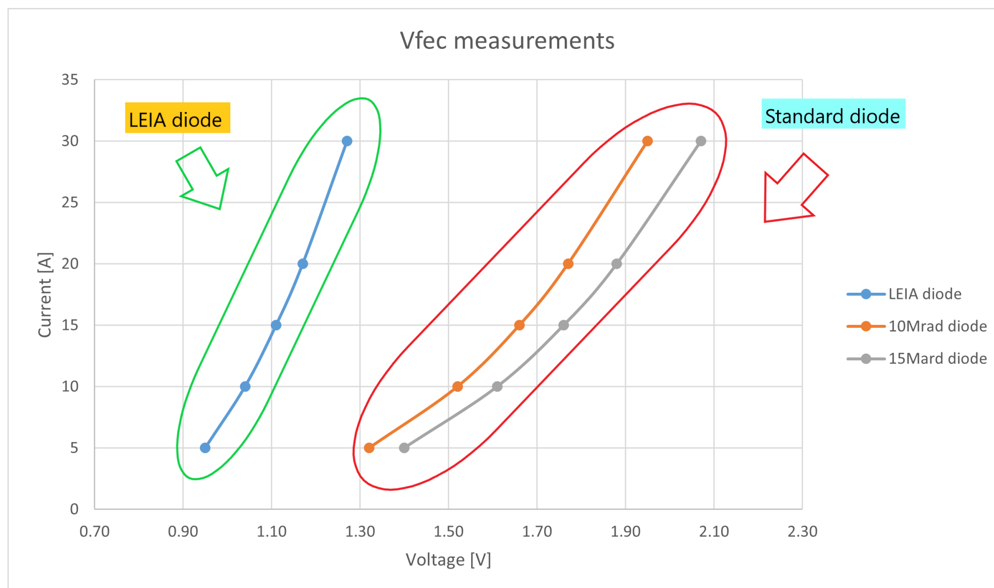

Figure 7.23: V_{fec} measurements

The measurements showed what we expected from the simulations. The

non-irradiated LEIA diode has a much lower V_{fec} than the other 2 diodes. The high value of V_{fec} in the 10Mrad and 15Mrad samples is mainly due to the presence of high contact resistance. In the LEIA diode, BF_2 was introduced to enrich the contact and make it more ohmic. From the Figure 7.23, it can be seen that the BF_2 implant contributed to improving the contact resistance.

After that, leakage current measurements were performed (see Table 7.4):

	LEIA diode NI	10Mrad	15Mrad
$I_{leakage}$ (480V) [nA]	7	32	50
$I_{leakage}$ (600V) [nA]	15	40	65

Table 7.4: Leakage current measurements

As we expected, irradiation has an impact on the device's leakage current. In the non-irradiated LEIA device, we have a lower leakage current.

7.6 Dynamic characterization

The circuit used in the measurements (see Figure 7.21) has a potentiometer to vary the input resistance, in order to obtain the desired dI/dt, which in our case was adjusted to 40 $A/\mu s$, considering that these measures had to be made on the wafer and not on the assembled sample. An inductive load of 1mH was used for this measurement. It was decided to recirculate a current of I_F of 5A in the diode and to supply it at a V_{cc} of 100V, in order not to flow too much current through the tips positioned on the wafer.
The on/off pulse was provided by a function generator. The function used was a square wave with a duty cycle of 50% and a period of 100μs.

The dynamic measurement circuit was initially tested using assembled diodes. Only the 10Mrad and 15Mard diodes are assembled, as it was not possible to assemble the wafers with the LEIA diode due to time constraints.

In the Figure 7.24 and Figure 7.25 we can observe the consistency of the measurements made on the wafer. The only difference lies in a higher parasitic inductance due to the presence of the long wires used to connect the tips, which results in the more pronounced oscillations after the rise time t_s.

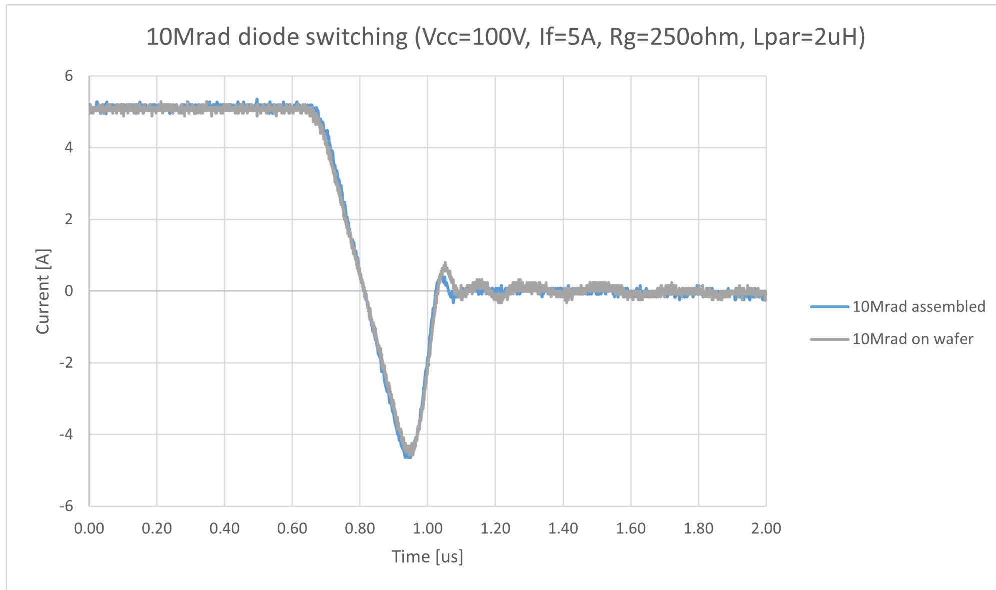

Figure 7.24: 10Mrad standard diode measurement on assembled sample vs measurement on wafer

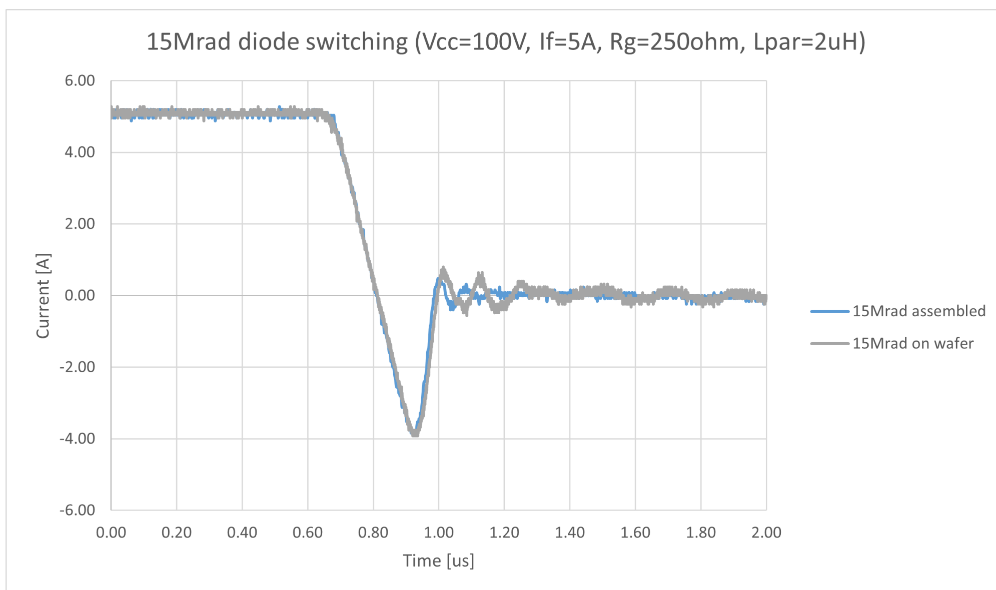

Figure 7.25: 15Mrad standard diode measurement on assembled sample vs measurement on wafer

We decided to test the centre of our wafers and four dies that were located

at the four cardinal points. This allowed the measurements to be averaged and to observe whether there was any difference due to the processes in the various areas of the wafer.

	LEIA	10Mrad	15Mrad
Q_{rr} [nC]	435.15	517.28	417.85
I_{rrm} [A]	-3.84	-4.58	-3.99
t_{rr} [ns]	187.28	215.12	184.40
t_s [ns]	110.64	131.04	112.16
t_f [ns]	76.64	84.08	72.24
s	0.70	0.64	0.65

Table 7.5: Average dynamic measurements

As we can see from the Table 7.5, the values extracted by using the oscilloscope were the Q_{rr} (integral of the curve subtended from zero to zero), the peak current I_{rrm}, the diode recovery time t_{rr} (calculated from zero to zero of the curve), the t_f (calculated from zero to peak current), the t_s (calculated from peak current to zero of the curve) and the diode softness s (t_s/t_f).

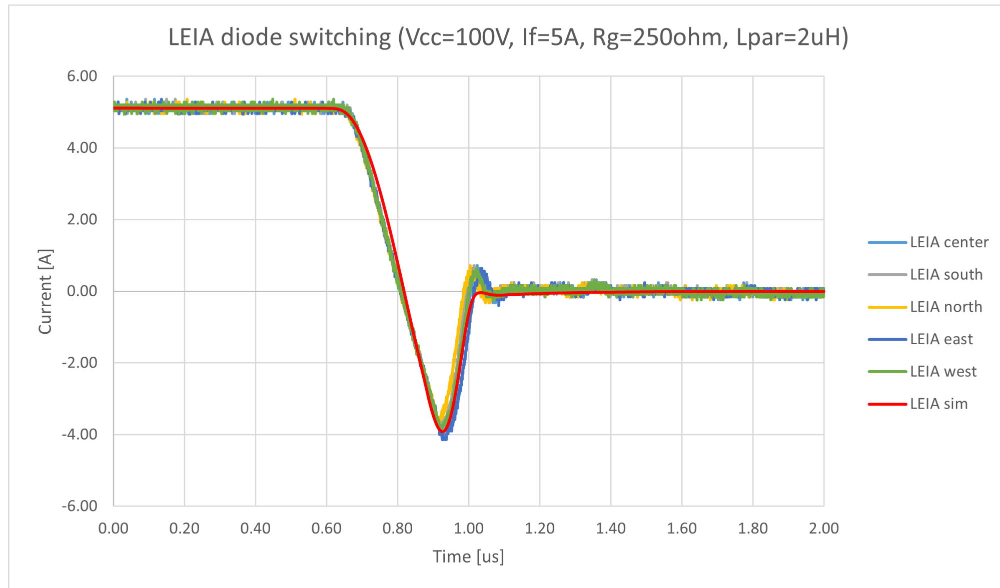

Figure 7.26: LEIA diode switching

In the Figure 7.26, Figure 7.27 and Figure 7.28 you can see the curves of the measurements made on the wafer, on assembled and simulated samples.

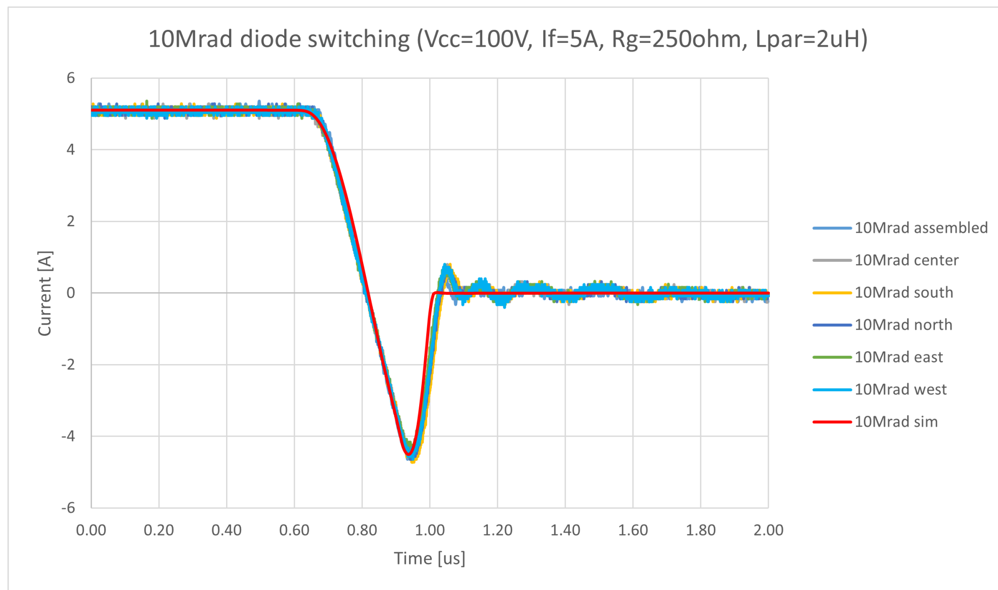

Figure 7.27: 10Mrad standard diode switching

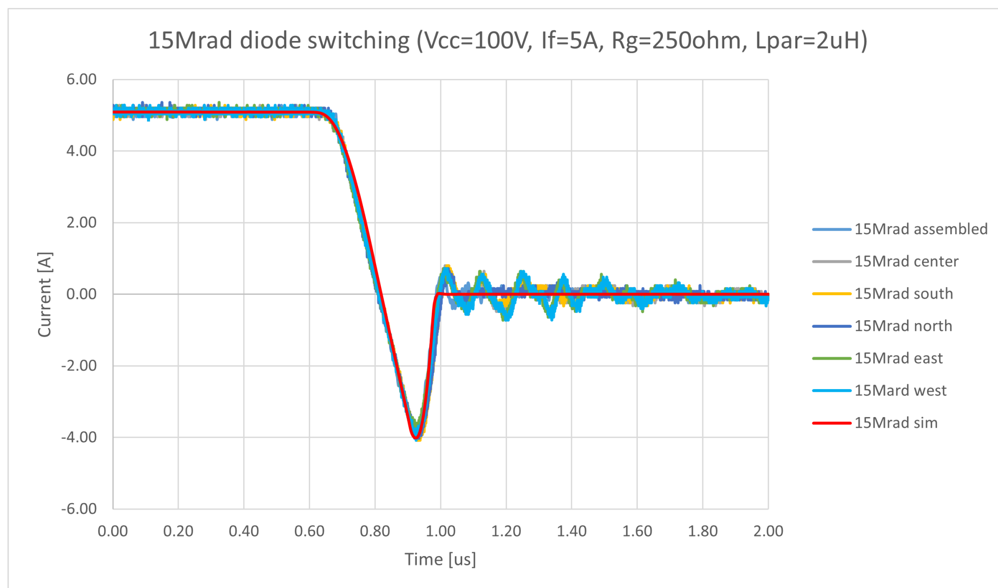

Figure 7.28: 15Mrad standard diode switching

Using a fit, we were able to find the value of R_g to include in the simulations (250 ohms) which would allow us to have a dI/dt of $40A/\mu s$ and the value of L_{par} of $2\mu H$ which would allow us to have a comparable softness value of the diode.

The value of softness is important for estimating the type of diode switching; the higher the softness, the faster the switching. From the Table 7.5 we can see that, as we expected, the LEIA diode has a higher softness. The measured values are however very low, this is related to the presence of a high parasitic inductance of the measurement circuit. If we could make measurements on the assembled sample, what we would expect would be a much higher softness. This can be seen in simulations made under standard diode operating conditions (see Table 7.6).

	LEIA	10Mrad	15Mrad
s	2.49	1.90	1.40

Table 7.6: Softness at V_{cc}=400V, I_F=15A, R_g=40ohm and L_{par}=40nH

From the Figure 7.26, Figure 7.27 and Figure 7.28 we can see a good fitting between the measurements and the simulations. The result obtained with non-irradiated LEIA diodes is really good. As we can see from the Table 7.14, the average value of Q_{rr} obtained is even lower than that expected from the simulations. As we can observe from the Figure 7.29, the behaviour of our LEIA diode is close to the behaviour of the standard 15Mrad device.

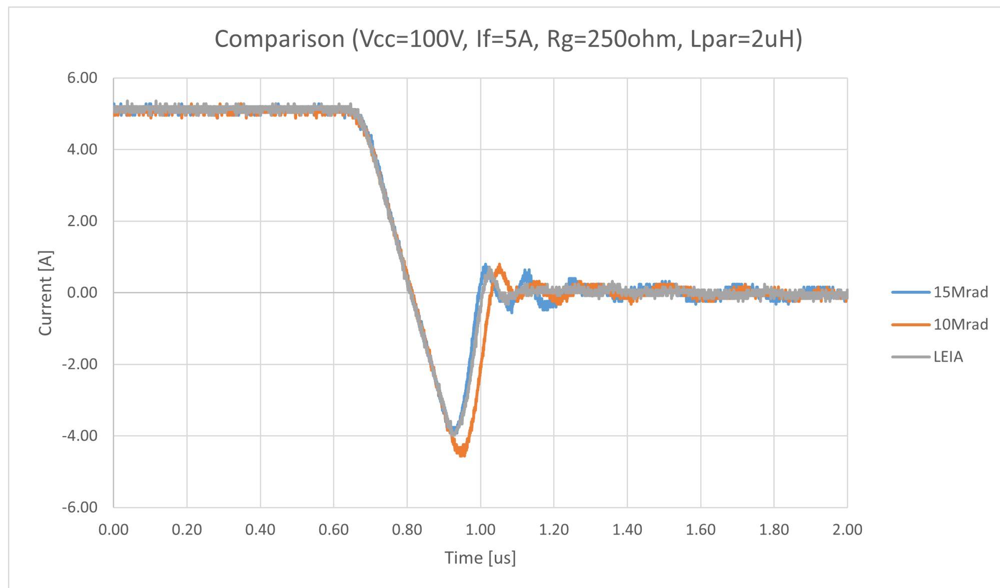

Figure 7.29: Comparison central dies diode switching

7.7 Results tables

	NI	0.5Mrad	2Mrad	5Mrad	10Mrad	15Mrad
$V_{CE_{sat}}$ (5A) [V]	1.1457	1.1543	1.1804	1.2327	1.3207	1.41
$V_{CE_{sat}}$ (10A) [V]	1.3085	1.3192	1.3517	1.4167	1.5263	1.638
$V_{CE_{sat}}$ (15A) [V]	1.4237	1.4359	1.4725	1.546	1.6698	1.796
$V_{CE_{sat}}$ (20A) [V]	1.5176	1.5309	1.5708	1.6508	1.7856	1.923
$V_{CE_{sat}}$ (30A) [V]	1.6727	1.6877	1.7328	1.8231	1.9751	2.1298
E_{off} (15A) [μJ]	288.96	288.94	286.27	260.05	241.98	233.02

Table 7.7: IGBT simulations

	NI	0.5Mrad	2Mrad	5Mrad
V_{fec} (5A) [V]	0.9215	0.9268	0.9419	0.973
V_{fec} (10A) [V]	1.0269	1.0334	1.0541	1.0945
V_{fec} (15A) [V]	1.1024	1.1101	1.1343	1.1815
V_{fec} (20A) [V]	1.1634	1.1726	1.1988	1.2526
V_{fec} (30A) [V]	1.2623	1.2726	1.3041	1.3673
$Q_{rr}{}^{*}$ [μC]	1.0241	0.9985	0.9265	0.8164
$Q_{rr}{}^{**}$ [μC]	0.4496	0.4361	0.3983	0.3376

Table 7.8: LEIA diode simulations

(*) V_{cc}=400V, I_F=15A, R_g=40ohm, L_{par}=40nH
(**) V_{cc}=100V, I_F=5A, R_g=250ohm, $L_{par}=2\mu H$
(***) V_{fec} improvement

	10Mrad	15Mrad	10Mrad***	15Mrad***
V_{fec} (5A) [V]	1.3121	1.3949	0.9282	0.9665
V_{fec} (10A) [V]	1.5125	1.6207	1.0133	1.0609
V_{fec} (15A) [V]	1.6599	1.7865	1.0721	1.1266
V_{fec} (20A) [V]	1.7807	1.9228	1.1198	1.1801
V_{fec} (30A) [V]	1.979	2.1466	1.1964	1.2655
Q_{rr}* [μC]	1.2714	1.0526	1.2714	1.0526
Q_{rr}** [μC]	0.5069	0.4038	0.5069	0.4038

Table 7.9: Standard diode simulations

	LEIA diode NI	10Mrad	15Mrad
V_{fec} (5A) [V]	0.95	1.32	1.4
V_{fec} (10A) [V]	1.04	1.52	1.61
V_{fec} (15A) [V]	1.11	1.66	1.76
V_{fec} (20A) [V]	1.17	1.77	1.88
V_{fec} (30A) [V]	1.27	1.95	2.07
$I_{leakage}$ (150V) [nA]	7	19	22
$I_{leakage}$ (480V) [nA]	15	41	44

Table 7.10: Static diode measurements

	center	south	north	east	west
Q_{rr}** [nC]	457.08	411.92	406.50	484.60	436.37
I_{rrm}** [A]	-3.98	-3.82	-3.75	-4.00	-3.82
t_{rr}** [ns]	192.00	176.40	176.80	204.80	189.20
t_s** [ns]	116.40	103.60	106.40	126.40	108.40
t_f** [ns]	75.60	72.80	70.40	78.40	80.80
s**	0.65	0.70	0.66	0.62	0.75

Table 7.11: LEIA diode non-irradiate measurements on wafer

	center	south	north	east	west
Q_{rr}** [nC]	517.48	552.70	534.47	489.64	522.41
I_{rrm}** [A]	-4.56	-4.72	-4.64	-4.40	-4.64
t_{rr}** [ns]	216.00	223.60	219.60	211.20	214.40
t_s** [ns]	130.80	139.20	130.80	123.20	135.20
t_f** [ns]	85.20	84.40	88.80	88.00	79.20
s**	0.65	0.61	0.68	0.71	0.59

Table 7.12: 10 Mrad diode measurements on wafer

	center	south	north	east	west
Q_{rr}** [nC]	406.72	437.60	435.92	390.99	418.02
I_{rrm}** [A]	-3.92	-4.08	-4.02	-3.84	-4.08
t_{rr}** [ns]	182.00	190.00	192.00	177.60	180.40
t_s** [ns]	114.40	118.40	115.20	104.00	108.80
t_f** [ns]	67.60	71.60	76.80	73.60	71.60
s**	0.59	0.60	0.67	0.71	0.66

Table 7.13: 15 Mrad diode measurements on wafer

	average on wafer	simulation
Q_{rr}** [nC]	435.15	449.60
I_{rrm}** [A]	-3.84	-3.99
t_{rr}** [ns]	187.28	200.35
t_s** [ns]	110.64	112.14
t_f** [ns]	76.64	88.21
s**	0.70	0.79

Table 7.14: LEIA diode non-irradiate measurements

	average on wafer	assembled	simulation
Q_{rr}** [nC]	517.28	512.20	506.90
I_{rrm}** [A]	-4.58	-4.64	-4.59
t_{rr}** [ns]	215.12	210.00	190.07
t_s** [ns]	131.04	128.00	122.21
t_f** [ns]	84.08	82.00	67.86
s**	0.64	0.64	0.56

Table 7.15: 10Mrad diode measurements

	average on wafer	assembled	simulation
Q_{rr}** [nC]	417.85	394.96	403.80
I_{rrm}** [A]	-3.99	-3.92	-4.10
t_{rr}** [ns]	184.40	176.00	167.88
t_s** [ns]	112.16	116.00	102.60
t_f** [ns]	72.24	60.00	65.28
s**	0.65	0.64	0.52

Table 7.16: 15Mrad diode measurements

	NI	0.5Mrad	2Mrad	5Mrad
Q_{rr}** [μC]	0.4496	0.4361	0.3983	0.3376
I_{rrm}** [A]	-3.993	-3.929	-3.770	-3.480
t_{rr}** [ns]	200.35	197.39	187.98	171.32
t_s** [ns]	112.14	102.19	102.35	92.66
t_f** [ns]	88.21	95.19	85.63	78.67
s**	0.7866	0.9315	0.8366	0.8490

Table 7.17: Dynamic LEIA diode simulations

Chapter 8

Conclusion and Future Perspectives

The aim of this thesis work was to demonstrate the validity of the LEIA concept. This concept is based on two assumptions, speeding up the diode by lowering the injection efficiency (realising a low doped anode) and using a low dose lifetime killing technique, in order not to impact the IGBT part, when this structure will be integrated into the RC-IGBT [1].
LEIA diode samples without electron irradiation were compared with standard diode samples with 15Mrad and 10Mrad irradiation. Unfortunately, it was also not possible to make this comparison on the LEIA diode samples with irradiation, because these samples are still being processed.
The results obtained from our measurements show that the behaviour of the non-irradiated LEIA diode is very close to that of the standard 15Mrad diode. This shows us that it is truly possible to speed up our diode, without to use high doses of irradiation.
The result will allow us to integrate the LEIA structure into RC-IGBTs for motor control. The low irradiation doses makes it a process compatible with RC-IGBTs, as the impact on the IGBT part as shown by the simulations would be very low.

Figure 8.1 and Figure 8.3 show the improvement that could be achieved in terms of diode switching speed. It can be observed that as the irradiation dose increases, the Q_{rr} of the diode decreases and its softness increases. Furthermore, low irradiation doses don't increase the V_{fec} too much.

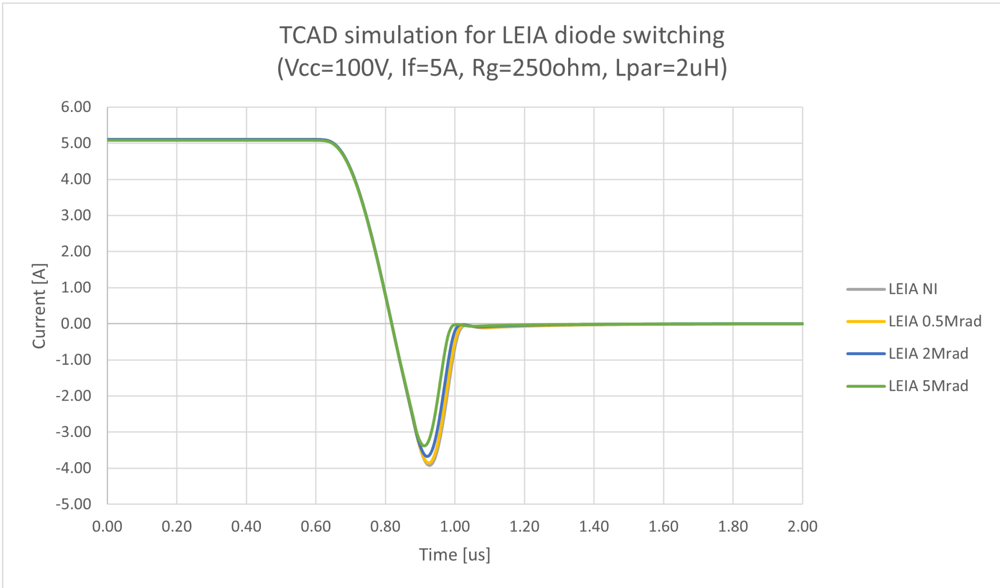

Figure 8.1: TCAD simulations for LEIA diode switching at different irradiation doses

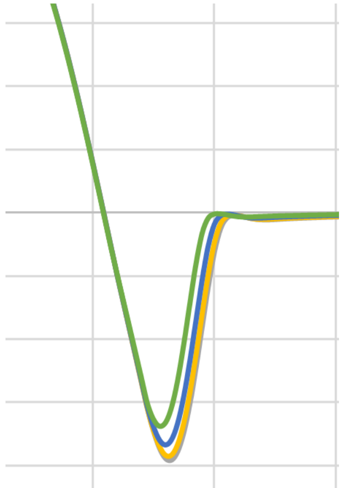

Figure 8.2: Zoom Figure 8.1

As soon as the LEIA samples with 0.5Mrad, 2Mrad and 5Mrad irradiation doses are available, analogous measurements performed on the non-irradiated LEIA diode will be carried out on them.

Our goal in the future will be to integrate a fast LEIA diode into the IGBT

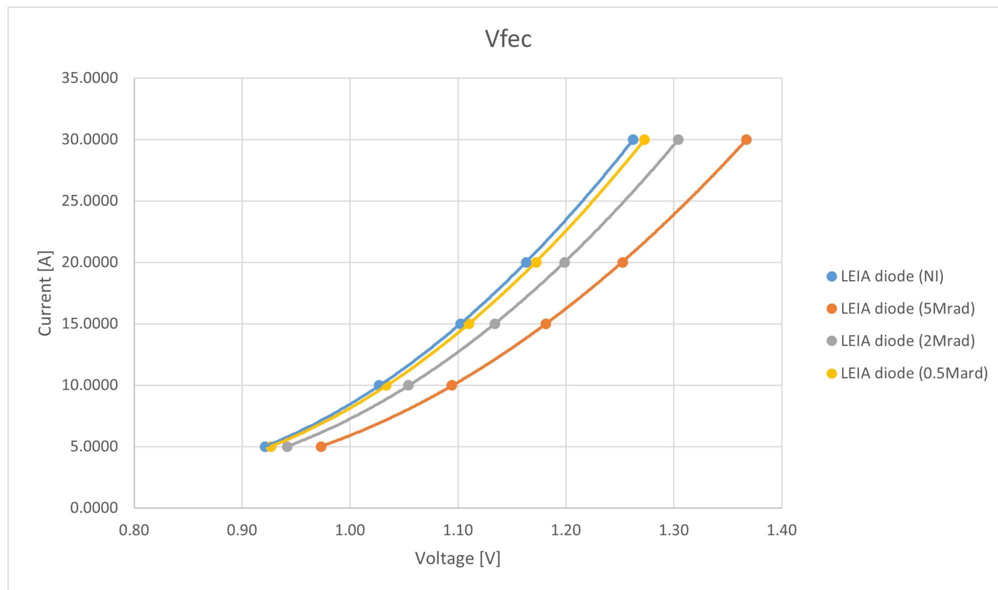

Figure 8.3: LEIA diode V_{fec} at different irradiation doses

structure, which utilises low-dose electron irradiation and thus enables us to further lower the Q_{rr} and make the diode faster. This will allow us to realise a competitive device, an RC-IGBT that combines excellent performance of the IGBT with a diode that has a high switching speed.

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