POLITECNICO DI TORINO

Master's Degree in Nanotechnologies for the ICTs

Master's Degree Thesis

Realization of a novel 3D magnetic sensor

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Summary

The topic of this thesis is the realization of a novel type of Hall sensor (PYRAMID), able to detect the off-plane and in-plane magnetic field.
The device is a three dimensional (inverted) pyramid-shaped device, engraved into Silicon. Eight contacts are patterned at the corners and at the middle of its sides, playing the role of biasing and sensing contacts.
The device is realized through anisotropic TMAH etching of silicon <100>, with a characteristic angle of 54.74°. The three components of the magnetic field can be detected by choosing a proper biasing/sensing contact configuration.
The novelty of the device stands in its ability to measure the three components of the magnetic field within a single compact structure. What is more, the sensor can be intrinsically made CMOS-compatible.

A theoretical model was successfully extracted, and validated by means of simulations with both COMSOL and SENTAURUS.
Additionally, different working modes were discovered and studied: B_{plane} and $B_{z1/z2/z3}$. These four modes detect respectively the in-plane and out-of-plane magnetic fields.
Several sweepings were performed, and these simulations proved to be in good agreement with the theoretical results. Quite interestingly, other studies highlighted a dependence of the sensitivity on the PYRAMID size and contact dimensions, not predicted by the theoretical model.

After these analyses, a process flow to produce the devices was conceived and successfully performed. An unconventional coating technique, i.e. spray coating, was adopted and optimized to pattern the device after the TMAH etching.

Two devices with PYRAMID side 25 µm and net n-doping $5 \cdot 10^{16}\ cm^{-3}$ were lastly wirebonded and characterized.
All the modes were tested, and their current-related sensitivities and cross-sensitivities were extracted. Each mode proved to be sensitive to the component of the magnetic field it was supposed to detect.

The sensitivities discovered were quite high, between 74 $\frac{V}{AT}$ and 220 $\frac{V}{AT}$. However, the devices were found to be more noisy than expected and presented a very high offset.

Solutions to these problems are yet to be found, but further research, alternative fabrication processing/materials and noise/offset reduction techniques might be able to improve the performances of the PYRAMID devices

Acknowledgements

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Table of Contents

List of Tables

List of Figures

Acronyms

BiCMOS
Bipolar Complementary Metal Oxide Semiconductor (transistor)

CMOS
Complementary Metal Oxide Semiconductor (transistor)

EKL
Else Kooi Labs

IMC
Integrated Magneto-Concentrators

JFET
Junction Field Effect Transistor

LPCVD
Low Pressure Chemical Vapor Deposition

MEMS
Micro Electro Mechanical Systems

MOSCAP
Metal Oxide Semiconductor CAPacitor

PCB
Printed Circuit Board

PSD
Power Spectral Density

RIE

Reactive Ion Etching

SEM

Scanning Electron Microscope

TLM

Transfer Lenght Method

TMAH

TetraMethylAmmonium Hydroxide

USD

USA Dollars

VHT

Vertical Hall Technology

Chapter 1

Introduction

1.1 Motivation and Objectives

Magnetic sensors are some of the most diffused sensors that are produced today. Each year, hundreds of millions of magnetic sensors are produced and sold, with a market size value of over USD 4 billion estimated in 2021[1].
These sensors are adopted in many different fields and currently used in a widespread range of applications such as current sensing, power measurement, position and motion sensing, automotive ignition and fuel injection, wheel rotation sensing, industrial application and spacecraft propulsion.
There are many types of magnetic sensors, but within the scope of micro technology we can distinguish three main categories: Micro Electro Mechanical Systems (MEMS), Magnetoresistance and Hall effect.
MEMS devices exhibit good performances, but they present fragile movable parts that require complex microfabrication and reduce their reliability.
Magnetoresistance sensors are extremely promising, however they require the deposition of non-conventional stacks of materials that have yet to be co-integrated with the CMOS line.
Lastly, Hall devices and Hall effect sensors cover by far the largest part of the magnetic sensor market. Their main advantage is that they can be easily manufactured with standard BiCMOS processes, so they can be co-integrated with their CMOS readout circuit in a straightforward way. Additionally, they have no movable parts, which implies a very high reliability.
Currently, there are two categories of Hall devices: horizontal and vertical. Horizontal Hall devices, also called Hall plates, detect magnetic fields perpendicular to the surface. Vertical Hall devices, instead, detect one component of the planar magnetic field. State of the art 3D Hall device co-integrate, on the same platform, a Hall plate with two vertical Hall devices. The performance of these devices

are limited by the vertical Hall devices, which require deep n-wells to reach good sensitivities. However, modern CMOS technologies guarantee active regions that are too shallow to ensure proper operation of vertical Hall devices.
To overcome this problem, many Hall sensors' producers adopt integrated magneto-concentrators (IMC). [2] An IMC is a ferromagnetic disc, deposited on top of a horizontal Hall device, that changes the direction of the magnetic field from in-plane to vertical. This solution reaches good sensitivities, but it requires post-processing and it has a limited measurement range due to the saturation of the ferromagnetic disc. [3] What is more, the presence of a ferromagnetic material limits the maximum operation temperature at which the device can properly operate.

The objective of this thesis is the realization of a novel type of Hall sensor, able to detect the out-of-plane and in-plane magnetic field without the need for expensive post-processing. The device is a three dimensional (inverted) pyramid-shaped device, engraved into Silicon. Eight contacts are patterned at the corners and at the middle of its sides, playing respectively the role of biasing and sensing contacts. The device is realized through anisotropic TMAH etching of silicon <100> with a characteristic angle of 54.74°, combining micro-fabrication techniques proper of the MEMS industry with common CMOS processes.
The novelty of the device stands in its ability to measure the three components of the magnetic field within a single compact structure, reducing the footprint and enabling a higher level of integration. The device presents the same structure and geometry of vertical Hall devices but "folded". However, the physics of the sensor follows the same working principles of horizontal Hall plates. This means that it requires shallower active regions to operate with an immediate boost of in-plane sensitivity.

1.2 Thesis overview

This work is structured as follows.

Chapter 2 overviews the general background that is necessary to grasp the physics behind Hall devices. Additionally, it reviews the state of the art of Hall magnetic sensors.

Chapter 3 collects the modelling and simulations of PYRAMID, performed on COMSOL and SENTAURUS. The effects of geometry have been investigated, as well as the consequences of different dopings and biasing.

Chapter 4 describes the fabrication of the Hall sensor in the Else Koi Lab

cleanroom facility of TU Delft. The process flow is explained, with particular emphasis on the most critical process steps.

Chapter 5 shows the results of the characterization of the PYRAMID sensor.

Lastly, **Chapter 6** encloses the general conclusions of the work, as well as the outlook for the future works.

Chapter 2

Background and state of the art

This chapter covers the main technical background information that is necessary to better understand the next chapters.
It begins with an overview of the Hall effect. Then the main performance parameters, sensitivity and offset, are explained and extracted for a 1D Hall plate device. Lastly, a brief review of the state of the art for integrated Hall sensors is presented.

2.1 The Hall Effect

2.1.1 Overview of the Hall Effect

The Hall Effect was discovered by Edwin Hall in 1879.[4] It describes how electrical currents and charges behave in the presence of magnetic fields.
In the most common and easy formulation, the Hall effect is the production of a voltage at the opposite sides of a conducting material subject to an electric current. This voltage difference can be measured at the sides transverse to both the current and the magnetic field.
Generally speaking, the name "Hall Effect" relates not to a single but to a series of physical phenomena, distinguished by the dimension and context in which they are analyzed.[5]
The most common one, the Ordinary Hall Effect, can be explained starting from Lorentz force:

$$\boldsymbol{F} = -q\boldsymbol{E} - q(\boldsymbol{v} \times \boldsymbol{B}) \tag{2.1}$$

where q is the elementary charge and **v** is the velocity of the electron.
Under the assumptions of no space charge, no generation-recombination of carriers, low field frequencies and negligible carrier density gradients the current density can be written as [3]:

$$\boldsymbol{J} = \sigma \boldsymbol{E} + \mu_H (\boldsymbol{J} \times \boldsymbol{B}) \tag{2.2}$$

where σ is the conductivity of the material and μ_H and Hall mobility. This result can be either obtained by an approximate classical approach, or a more exact kinetic approach.[6]
The Hall mobility can be expressed as:

$$\mu_H = r_H \mu \tag{2.3}$$

where μ is the drift mobility and r_H is called the Hall scattering coefficient.
The Hall scattering coefficient is typically close to 1 and depends on the scattering phenomena in the semiconductor/conductor, the temperature and the value of the magnetic field (second order dependence).

Solving the equation for **J**, we obtain Equation 2.4:

$$\boldsymbol{J} = \sigma_B [\boldsymbol{E} + \mu_H (\boldsymbol{E} \times \boldsymbol{B}) + {\mu_H}^2 \boldsymbol{B} (\boldsymbol{E} \cdot \boldsymbol{B})] \tag{2.4}$$

with:

$$\sigma_B = \frac{\sigma}{(1 + \mu_H B)^2} \tag{2.5}$$

This is the equation mostly used by semiconductor CAD such as SENTAURUS to simulate the galvanic effect, eventually rewritten to facilitate the numerical resolution of the differential equations.
Additionally, it is the equation that was used to extract the coefficients of the conductivity tensor that were adopted in the COMSOL simulations (see chapter 3, section 3.2 for more details).

Solving Equation 2.2 for $\boldsymbol{E}$, instead, gives:

$$\boldsymbol{E} = \rho_B \boldsymbol{J} - R_H [\boldsymbol{J} \times \boldsymbol{B}] + P_H (\boldsymbol{J} \cdot \boldsymbol{B}) \boldsymbol{B} \tag{2.6}$$

where ρ_B is the (intrinsic) magneto-resistivity, R_H is the Hall coefficient and P_H is the planar Hall coefficient.
An explicit expression for the magneto-resistivity and the planar Hall coefficient is neither easy to obtain nor interesting to the scope of this review. However, for relatively small magnetic fields, $\rho_B \approx \rho$ (the zero-field resistivity) and $P_H \approx 0$.
The Hall coefficient, instead, is given by:

$$R_H = \frac{r_H}{qn} \tag{2.7}$$

where n is the carrier density of the device.

If the magnetic and electric fields are perpendicular, Equation 2.4 and Equation 2.6 reduce to:

$$\boldsymbol{J} = \sigma_B[\boldsymbol{E} + \mu_H(\boldsymbol{E} \times \boldsymbol{B})] \tag{2.8}$$

$$\boldsymbol{E} = \rho_B \boldsymbol{J} - R_H[\boldsymbol{J} \times \boldsymbol{B}] \tag{2.9}$$

This is the case of many practical applications, such as Hall plates and vertical Hall devices.
From these simplified relations, it is very easy to observe the two main physical manifestations of the Hall effect. In fact, looking at Equation 2.8, we can see that the term:

$$\boldsymbol{E_t} = \mu_H(\boldsymbol{E} \times \boldsymbol{B}) \tag{2.10}$$

has the dimensions of an electric field and it is orthogonal both to the magnetic and electric field. This extra term can be seen as an additional electric field that deflects the current of a certain angle called Hall angle:

$$\theta_H = \frac{|\boldsymbol{E_t}|}{|\boldsymbol{E}|} = arctan(\mu_H B) \tag{2.11}$$

The current deflection is indeed the reason for which a magnetic field determines a modulation of the sample conductivity, as reported in Equation 2.5.

The second effect is the appearance of an electric field that opposes the current deflection caused by the Lorentz force. Looking at Equation 2.9, we can see that this electric field has the form:

$$\boldsymbol{E_H} = -R_H(\boldsymbol{E} \times \boldsymbol{B}) \tag{2.12}$$

This is nothing but the electric field that induces the appearance of the Hall voltage.

2.1.2 Sensitivity of a Hall plate

Now, the sensitivity of a simple Hall device will be extracted and investigated.
An example of Hall plate is represented in Figure 2.1: it is a conductive/semiconductive layer with carrier density n, length l, width w and thickness t.

On the plate there are four contacts in total: two bias contacts C1 and C2 and two sense contacts S1 and S2.
The external electric field is generated applying a voltage V between C1 and C2, or alternatively forcing a current I to flow between the two biasing contacts.
Of course, the application of a voltage makes a current flow in the material, and a current causes a potential drop between the two contacts. Current bias and voltage bias are intrinsically related by Ohm's law.
The Hall voltage readout is performed measuring the voltage difference between S1 and S2, and we assume for now that $V_{out} = V_H$.
The external magnetic field is supposed to be homogeneous and it is applied perpendicular to the plate surface, which means that $\mathbf{B} = B_z\,\hat{\boldsymbol{k}}$. The goal is to find the relation between V_{out} and B.

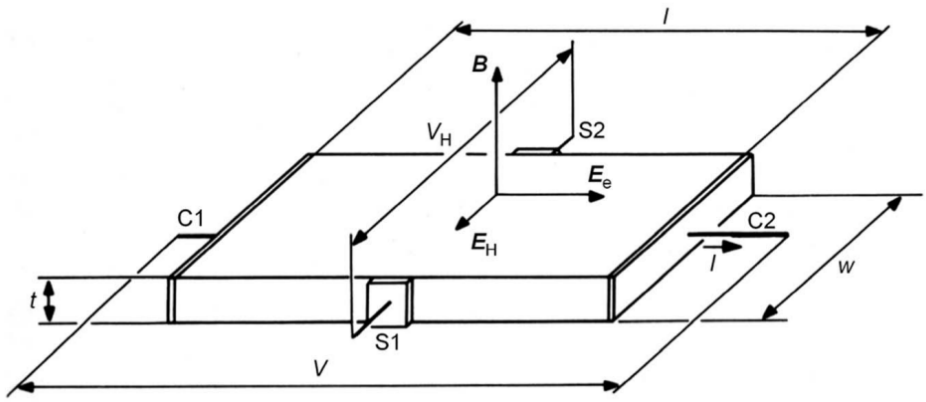

Figure 2.1: Example of Hall plate [7]

To this scope, let us consider a very long Hall plate, i.e. $\frac{l}{w} >> 1$.
What happens inside the device is that the current, which flows straight from C1 to C2, is deflected by the Lorentz force. As a consequence, there is an accumulation of carriers on one sense contact and a depletion on the other one.
This generates a potential difference, the Hall voltage, that at equilibrium produces an electric force that perfectly compensate the effects of Lorentz force.

Since the sample is infinitely long, the insulating boundary condition on the long sides of the plate (i.e. the ones on which the sense contacts are placed) implies that the current is confined to flow on the x direction. This means that the current density can be written as:

$$\boldsymbol{J} = J_x\,\hat{\boldsymbol{i}} = \frac{I}{tW}\,\hat{\boldsymbol{i}} \tag{2.13}$$

It is interesting to point out that, in the case of a very long plate, no current deflection is present.

The Hall voltage V_H for this ideal device can be obtained by integrating the Hall electric field on a path that joins the two sense contacts.
Recalling that the Hall electric field is given by Equation 2.12, we obtain:

$$V_H = \int_{S2}^{S1} \boldsymbol{E_H}\, d\boldsymbol{y} = -R_H \int_{S2}^{S1} (\boldsymbol{E} \times \boldsymbol{B}) \tag{2.14}$$

Now, let us solve the cross product exploiting Equation 2.13 and remembering that $\mathbf{B} = B_z\, \hat{\boldsymbol{k}}$. In addition, let us substitute R_H by means of Equation 2.7:

$$V_H = R_H J_x B_z \int_{S2}^{S1} dy = I \frac{r_H}{qnt} B_z \tag{2.15}$$

Note that this result is only valid for long plates. In the case of short plates ($\frac{w}{l} << 1$) no Hall voltage can form since the electric field is forced to stay confined in the x direction, and the electric field has the form:

$$\boldsymbol{E} = E_y \hat{\boldsymbol{i}} = \frac{V}{l} \hat{\boldsymbol{i}} \tag{2.16}$$

This is true because the continuity boundary condition must always be fulfilled on the bias contacts, and since the device is infinitely small this condition is automatically extended to the whole structure.
In this case, however, the current is deflected by an angle θ_H given by Equation 2.11.

Any other case, between the limiting cases of long and short plate, will present both a current deflection and a Hall voltage.
As a consequence, Equation 2.15 should be modified to include a correction factor (of magnetoresistance) G_H that takes into consideration the finite geometry of real devices: [8]

$$V_H = I G_H \frac{r_H}{qnt} B_z \tag{2.17}$$

The geometrical correction factor is always between 0 and 1, where $G_H = 0$ in the case of a short plate while $G_H = 1$ in the case of a long plate.

If the Hall plate is biased with voltage instead of current, Equation 2.17 becomes:

$$V_H = V \mu_H G_H \frac{w}{l} B_z \tag{2.18}$$

This expression can be obtained relating V and I with Ohm law:

$$V = RI \quad with\ R = \frac{1}{q\mu n} \frac{l}{wt} \tag{2.19}$$

Finally, recalling the definition of sensitivity of a device, we can write the absolute sensitivity of a real Hall plate as:

$$S_A = \frac{\delta V_{out}}{\delta B} = V \mu_H G_H \frac{w}{l} = I G_H \frac{r_H}{qnt} \tag{2.20}$$

From this result we can see that increasing the biasing voltage or current there is a linear increase of the sensitivity.
To better characterize the intrinsic performance of a Hall device, the voltage-related and current-related sensitivities are introduced:

$$S_V = \frac{S_A}{V} = \mu_H G_H \frac{w}{l} \tag{2.21}$$

$$S_I = \frac{S_A}{I} = G_H \frac{r_H}{qnt} \tag{2.22}$$

From these two equations we can see that the voltage-related sensitivity is proportional to the mobility of the sample, while the current-related sensitivity is inversely proportional to the density of carriers. This explains the reason why low-doped semiconductors are generally used as materials for Hall sensors. In fact, a low doping decreases the carrier density and improves the mobility, which steadily goes down starting from $10^{16}\ cm^{-3}$ on.
Additionally, we can see that the current-referred sensitivity is inversely proportional to the thickness of the material. This is one of the reasons why Hall plates are easily integrated in CMOS processes. In integrated horizontal Hall sensors, in fact, the thickness of the device is defined by the junction depth of the n-doped layer. This active layer is generally created during the same implantation step that defines the low doped N-well regions. This allows to perfectly co-integrate both readout circuit and sensor at the same time.
Typically n-well regions are not deeper than 3 μm, and they are getting shallower and shallower as technology progresses. This means that excellent performances can be achieved that, together with extremely simple processing, makes Hall plates the most popular type of integrated magnetometer.

2.1.3 Non-idealities in Hall plates: offset and noise

The previous analysis involved a perfect and isolated Hall device. Now, we will consider the case of a real device. The full output voltage of a real Hall plate can be written as follows:

$$v_{out} = V_H + V_{off} + v_N(t) \tag{2.23}$$

where V_{off} is the offset voltage and v_N is the output noise.
In every application V_H is the useful signal while V_{off} and v_N are nothing but disturbances that should be minimized.

The offset voltage V_{off} determines a reading different from zero at zero field applied. If the offset voltage is not exactly known, as is frequently the case, the precision with which we can determine the Hall voltage is limited.
The major causes of offset are imperfections in the fabrication process, such as misalignment and asymmetries during the lithography phase or local non-uniformities in the materials' thickness and resistivity.

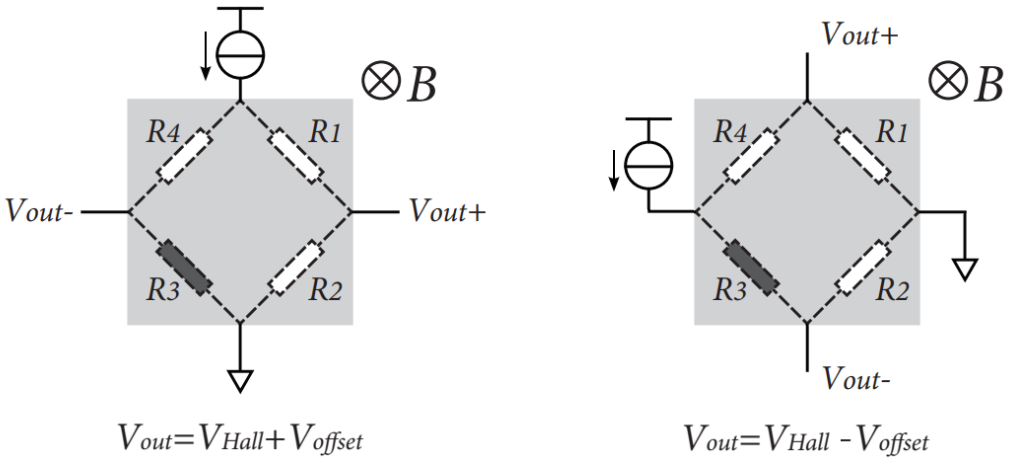

Figure 2.2: Wheatstone model of a Hall device. Each resistor represents the path that joins each contact to the closest ones. [9]

Now, let us consider a Hall plate that is current biased. Offset can be easily represented with a Wheatstone bridge circuital model, as reported in Figure 2.2. The offset voltage is given by [9]:

$$V_{off} = I\frac{R_1R_3 - R_2R_4}{R_1 + R_2 + R_3 + R_4} \tag{2.24}$$

where $R_1 - R_4$ are the resistances of the four branches, that connect the biasing contacts to the sensing contacts. Of course, if the structure is perfectly symmetric, the resistances are equal and $V_{off} = 0$.
It is also very interesting to notice that, inverting biasing and sensing contact (i.e. rotating the contacts configuration of 90°, see Figure 2.2), we get that the offset voltage becomes:

$$V_{off}^{'} = I\frac{R_2R_4 - R_1R_3}{R_1 + R_2 + R_3 + R_4} = -V_{off} \tag{2.25}$$

At the same time, the measured Hall voltage does not change polarity. This means that, averaging the two measurements, we can obtain a result that is virtually independent from the offset voltage. This technique is called current spinning and it allows an offset voltage reduction of more than 3 orders of magnitude. In most of the cases more than two phases can be used to have an even higher reduction of the offset voltage.
Despite the application of current spinning, however, there is always a relatively small residual offset. The main causes of this residual offset are both external (packaging and stray field in the measurement system) and internal (thermal gradients from self-heating [10] and non-uniform depleted region distributions).

For what concerns the noise, it is a stochastic disturbance that ultimately limits the precision with which we can measure both offset and Hall voltage.
It is typically expressed in terms of power spectral density, which can be related to the root mean square noise voltage by means of Equation 2.26 [11][12]:

$$v_N = (\int_{f_1}^{f_2} S_{NV}(f)\, df^{\frac{1}{2}}) \tag{2.26}$$

There are several sources of noise inside semiconductors, but the main ones for our analysis are thermal noise and flicker noise:

$$S_{NV} = S_{VT} + S_{V_\alpha}(f) \tag{2.27}$$

Thermal noise, also known as Johnson–Nyquist noise or white noise, is caused by the thermal motion of carriers. It is a uniform contribution that cannot be removed:

$$S_{VT} = 4k_bTR \tag{2.28}$$

Flicker noise, or pink noise, is known to empirically exist but its physical origins are still under dispute. It can be written as:

$$S_{V_\alpha} = V^2 \frac{\alpha_H}{N} \frac{1}{f^\gamma} \tag{2.29}$$

where N is the total number of carriers, γ is the logarithmic slope of the $1/f$ portion of the PSD graph (Figure 2.3) and α_H is a dimensionless parameter called the Hooge parameter. Initially, the Hooge parameter was believed to be a constant of value $2 \cdot 10^{-3}$ for all semiconductors, but later it was discovered that it has a dependence on the material.

Figure 2.3 shows the typical semilogaritmic graph of the power spectral density of a Hall device. There is a low frequency domain that is dominated by the flicker noise, while at higher frequencies the PSD becomes constant and it reduces

to the thermal noise. The point that crosses these two regimes is called corner frequency.
The main concern from an electronic point of view is the flicker noise, which can be reduced with commonly used techniques such as chopping and averaging. [13] It can be shown that current spinning, with a frequency higher than the corner frequency, can also help remove the flicker noise component. [11]

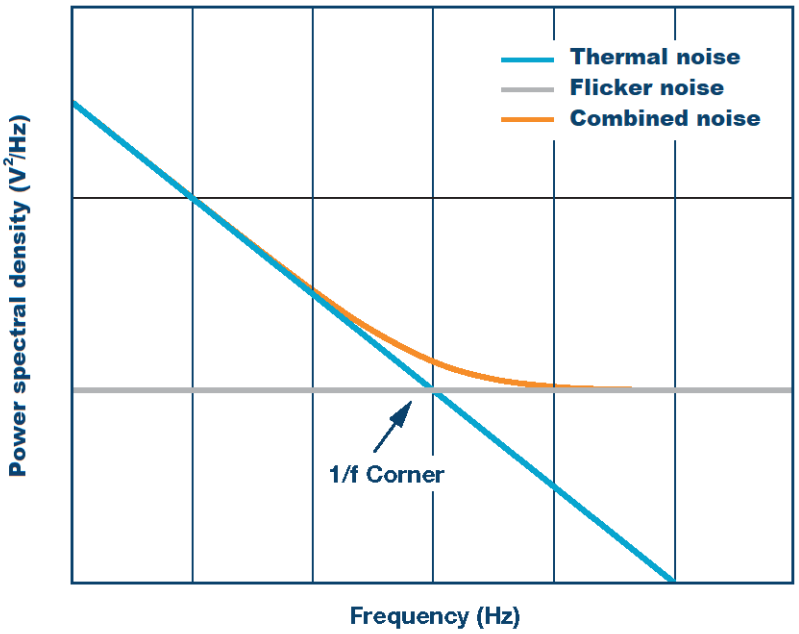

Figure 2.3: Power spectral density of a semiconductor. [14]

2.1.4 Vertical Hall devices

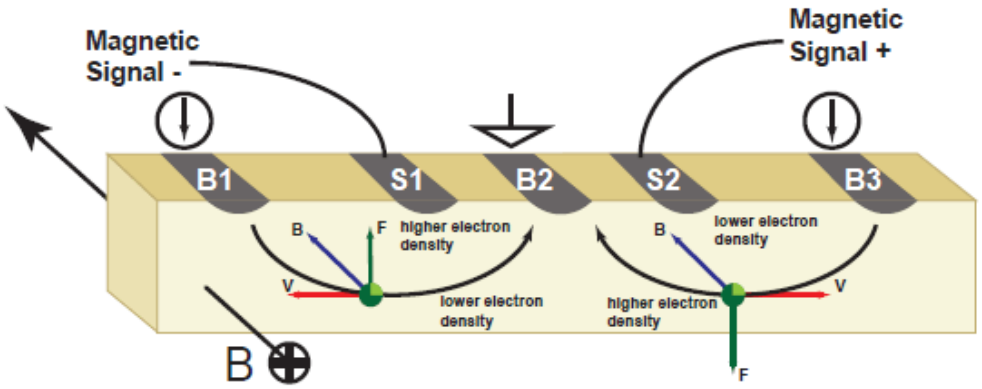

Figure 2.4: A vertical Hall device [15]

As previously mentioned and explained, Hall plates allow the measurement of magnetic fields that are orthogonal to the device surface.
To measure magnetic fields that are in-plane, the concept of vertical Hall devices was developed by Popovich in 1984.[16]
The simplest vertical Hall device is a 5-contact device in which the contacts are placed in a straight line on top of the semiconducting material (see Figure 2.4).
Moving from left to right the first contact B1, the third contact B2 and the fifth contact B3 are biasing contacts. The second contact S1 and the fourth contact S2 are instead sensing contacts. Therefore, biasing contacts and sensing contacts are alternated.
The working principle is quite simple: a positive voltage is applied between B1 and B2, while a negative voltage is applied between B2 and B3. As a consequence,two currents are produced in the device that flow in opposite directions.
Now, let us apply a magnetic field that is in-plane, but orthogonal to the currents. Lorentz force acts on the two currents and bends them. However, since these currents flow in opposite directions, they are bent in directions that are exactly the opposite. In particular, one current points towards the substrate while the other points towards the surface.
This means that we will have an accumulation of carriers on one sensing contact and a depletion of carriers on the other contact. Thus, a voltage difference will form between S1 and S2 that is linearly proportional to the magnetic field.

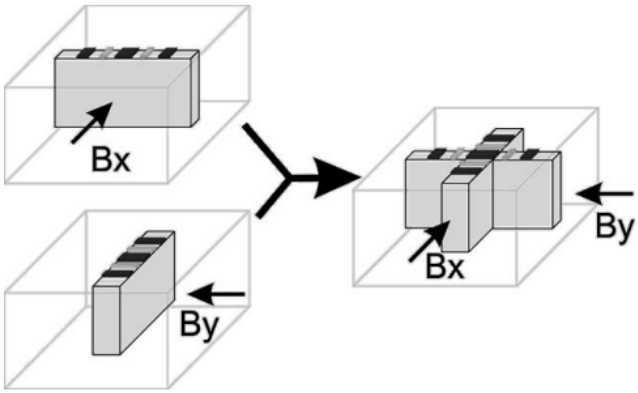

Figure 2.5: Vertical Hall structure to measure both the components of the in-plane magnetic field. [17]

Of course, only one in-plane direction is sensed by the vertical device. To detect the whole in-plane magnetic field at least two vertical devices with orthogonal active regions are needed (shown in Figure 2.5).
A vertical Hall device is strongly related to a horizontal Hall plate. It can be rigorously proved that a 5-contacts Hall device can be traced back to a Hall plate by means of the conformal mapping method. [8]
In a more intuitive way, a vertical Hall device can also be seen as a buried Hall plate in which the sense contacts have been "stretched" to reach the surface, as shown in Figure 2.6. Therefore, all the results obtained in subsection 2.1.2 are still valid, but only if we keep into account the "stretch" operation.
In particular, this transformation maps the length l of the Hall plate to the horizontal extension of the vertical Hall device. At the same time, the width is translated into the relative distance between the contacts of the vertical device.
Additionally, the active region should be cylindrical to exactly reproduce the mathematical mapping. However, it can be proven that a box-shaped active region produces the same results if its junction (i.e. thickness) is sufficiently deep. From a more intuitive point of view, this would cause the currents to flow deep into the material, allowing the formation of a reasonable voltage difference. A too thin junction depth necessarily implies a very low sensitivity, which is actually the main reason why vertical Hall devices cannot be integrated with CMOS processing.

What is more, vertical Hall devices suffer from high offset due to their two-fold symmetry, which limits the application of current spinning. The main cause of the offset is, again, asymmetries due to fabrication errors and misalignments. Other reasons, however, play also a relevant role. The Junction Field Effect (or JFET

effect) is the most noticeable example. The presence of a p-n junction between the substrate and the active region determines the appearance of a depleted region. When the bias is applied, the region closer to the high potential depletes more than the one at ground. This determines a further asymmetry which increases the offset and cannot be removed by means of current spinning.
A Wheatstone bridge-like model can be adopted again to model the offset of a vertical Hall device.[18] In this case, however, the JFET effect results more relevant than for horizontal Hall plates and cannot be neglected. Therefore, non-linear resistors are used in the electrical model.

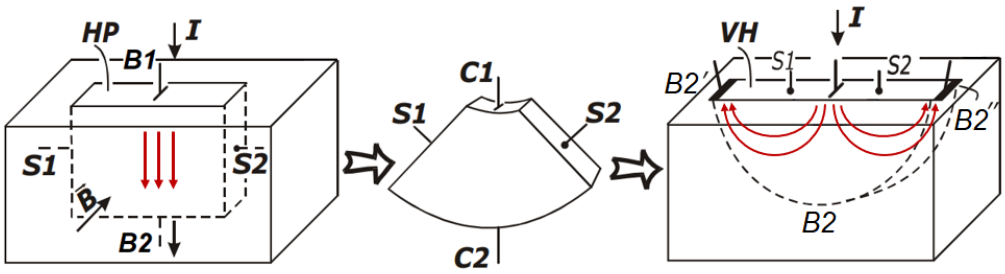

Figure 2.6: From Hall plates to vertical Hall devices: the bias and sense contacts are "stretched" to reach the exposed surface of the semiconductor. [16]

2.2 State of the art

2.2.1 State of the art of 1D devices

Horizontal Hall devices are the most common type of integrated magnetic sensor. They can be easily integrated in standard CMOS processes, where the active region is defined by means of a shallow N-well implantation. Their footprint is in the range of 10 μm, and they are not made smaller to prevent increasing unwanted disturbances (offset and noise). As technology progresses the junction depth becomes even more shallow, effectively enhancing the performances of Hall plates.
These sensors can present different shapes (Figure 2.7), but the most common ones present a 4-fold symmetry. In this way current spinning can be applied in an extremely effective way, reducing offset and noise of the device. The state of the art of these devices present a current-scaled sensitivity of $100 - 400\ \frac{V}{AT}$, and a voltage-scaled sensitivity of $30 - 70\ \frac{mV}{VT}$. [11] [19] [20]
Regarding vertical Hall devices, the ones developed by Popovich exhibit quite high current-scaled sensitivities (around $400\frac{V}{AT}$) and good stability.[16] However, they are realized in a custom technology called VHT with very low N-well dopings and deep junction depth (open N-well).[3] Therefore, the process is not CMOS-compatible.

Vertical Hall devices realized in standard CMOS processes exhibit poor performances and high noise. For example, Vertical Hall devices realized in the GLOBALFOUNDRIES 0.18 μm BCDlite technology reach a sensitivity of 5.56 V/AT, which is two orders of magnitude lower than horizontal Hall devices. [21]
To further improve the performances, expensive pre-processing has to be done. This is the case of the trench Hall-technology, which reaches sensitivities of around 300 $\frac{V}{AT}$. [22]
Alternatively, sensitivities of 130 $\frac{V}{AT}$ were reached by adopting high-voltage technologies and unconventional doping reduction techniques.[23] However, this good result is limited to a particular technology and cannot be extended to others.

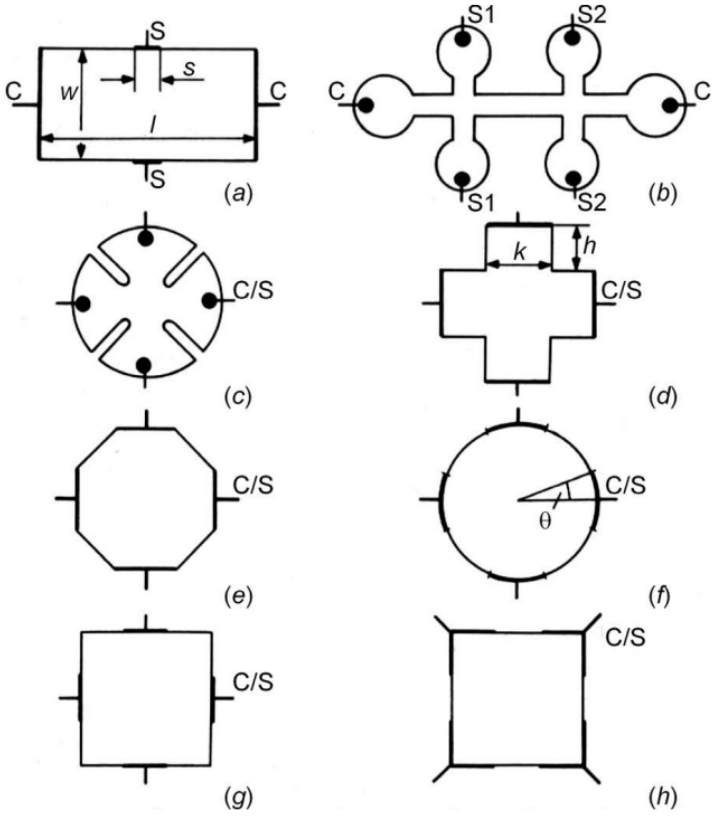

Figure 2.7: Various shapes of horizontal Hall devices [8]

An alternative to vertical Hall devices adopts horizontal Hall devices and magneto-concentrators (IMC). [24] A ferromagnetic disc, placed on top of a Hall plate, converts the magnetic field from in-plane to perpendicular and it is detected by the sensors. Both current-referred and voltage-referred sensitivities are very good, respectively 360 $\frac{V}{AT}$ and 90 $\frac{mV}{VT}$. [3] However, it requires post-processing and

the performances are limited by the saturation of the ferromagnetic disk.

2.2.2 State of the art of 3D devices

The simplest three-dimensional Hall sensor integrates on the same platform one horizontal Hall device and two orthogonal vertical Hall devices. In this way, the three components of the magnetic field are simultaneously detected. However, this approach requires independent optimization of the horizontal and vertical devices which have opposite requisites to properly operate (shallow junctions vs deep junctions). Furthermore, if these devices are realized in standard CMOS processes, their performances are limited by the vertical Hall sensors.
The approach adopted by Melexis, one of the leader companies in integrated magnetometers, makes use Hall plates with IMCs (see Figure 2.8) [2]. This technology is employed in their TriAxis® magnetic sensor, used to create 2D and 3D sensors that sense the linear, rotary and joystick motion as well as magnetometers able to output the individual components of the B field.

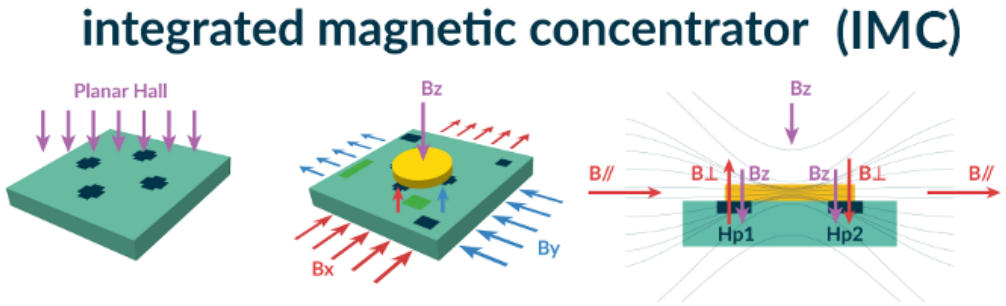

Figure 2.8: The IMC-Hall technology adopted in TriAxis®. Four Hall plates, two per planar direction, are placed below the IMC in a symmetrical way. Each component of the magnetic field can be obtained by linear combination of the Hall voltages detected by the four Hall devices. [2]

Another approach was proposed by Schott in 1999.[25] His device (represented in Figure 2.9) is a squared block of doped silicon with 8 contacts: 4 bias contacts at the corners and 4 sensing contacts placed in the middle of the squared block. The biasing voltage polarities are alternated.
This device can actually be seen as a combination of an 8-contact vertical Hall device and a non plate-like horizontal Hall device: when a magnetic field is applied, each sensing contact exhibits a voltage that is a linear superposition of the Hall voltages generated by the different magnetic field components. Therefore, each

component of the magnetic field can be extracted by doing some simple linear combinations of the sensed voltages.
This is a very simple and elegant solution that reaches quite high sensitivities, low noise and long-term stability. However, it requires again very deep junctions that are not reachable with standard CMOS processes.

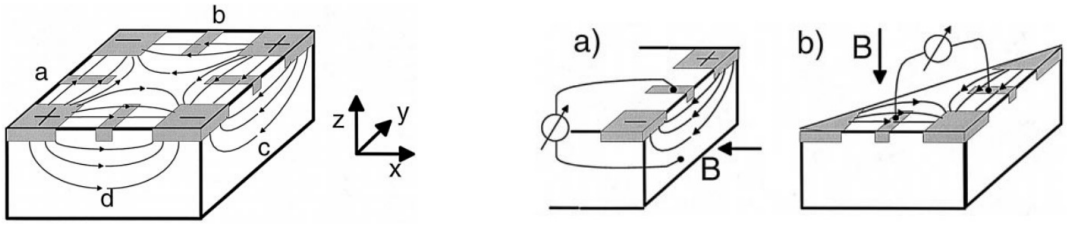

Figure 2.9: The 3D Hall device developed by Schott. [25]

A last alternative solution is the one presented by Sanders and al. in 2015.[26] The sensor is a hexagonal prism with symmetric sets of contacts on the top and bottom of the structure. Applying a bias, three orthogonal identical Hall plates are operated. The three components of the magnetic field can be then extracted after a change of coordinates. This Hall device is extremely isotropic, with voltage-related sensitivities of around 33 $\frac{mV}{VT}$ for each Cartesian axis.

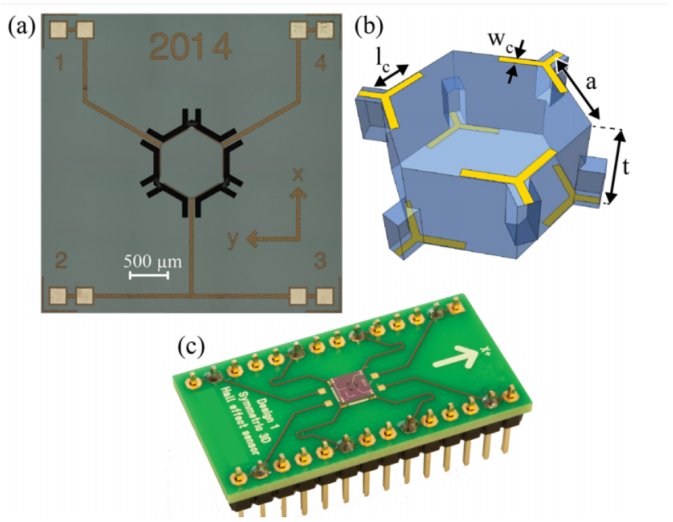

Figure 2.10: The 3D Hall device developed by Sanders.[26]

Chapter 3

Modelling and simulation of PYRAMID

This chapter's topic is the modelling and simulation of the PYRAMID sensor, performed with both COMSOL and SENTAURUS. First of all, the 3D pyramidal Hall sensor is shown and a theoretical model is extracted. Next, an overview of the models adopted by the two simulators is given. Then, the working modes of PYRAMID are shown. After that, the main studies performed are displayed, showing the effect that the main design parameters (such as PYRAMID size, contact size, doping, etc.) have on the sensitivity of the device.
Lastly, the main and most useful results obtained are summarized in a series of design guidelines that should be followed to maximize the performances of the PYRAMID devices.

3.1 A novel 3D magnetometer: PYRAMID

To solve some of the problems exposed in the previous paragraphs in an innovative and alternative way, the PYRAMID Hall sensor was conceived.
The device is represented in Figure 3.2. It is a pyramid-shaped hole, lightly doped, engraved into silicon. This device is technologically realized by means of anisotropic KOH/TMAH etching of silicon, which implies a characteristic angle of 54.74°.
It is an 8-contact device, placed in correspondence of the four corners and in the middle of the four sides.

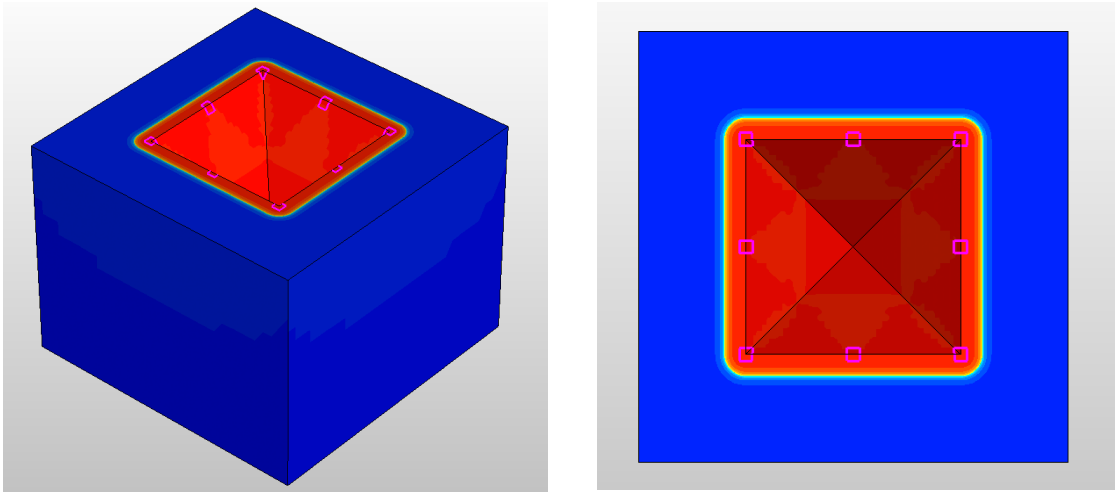

Figure 3.1: The PYRAMID Hall sensor

To better understand the working principle of PYRAMID, let us focus on the simplified case of a V-groove. A V-groove is, as the name suggests, a V-shaped cavity engraved into silicon. Let us consider only the active area, i.e. the lightly N-doped region. Additionally, suppose that two sensing contacts are on top of each sloped side of the V-shaped cavity (see Figure 3.2).
What is more, let us assume that the two sloped sides are identical and perfectly symmetric, which implies that no offset is present.
This device is geometrically characterized by six parameters:

- the thickness: t
- the sloped-side length: W
- the horizontal projection of the sloped side: $L/2$
- the vertical projection of the sloped side, or height: h
- the depth: l

Let us consider a section (Figure 3.3) and suppose that two currents, with the same polarity, flow inside the sloped sides (i.e, perpendicular to the section). If we suppose that the V-groove is infinitely long ($\frac{l}{W} >> 1$), then the current can be written as:

$$\boldsymbol{J} = J_y \hat{\boldsymbol{j}} = \frac{I}{tW} \hat{\boldsymbol{j}} \tag{3.1}$$

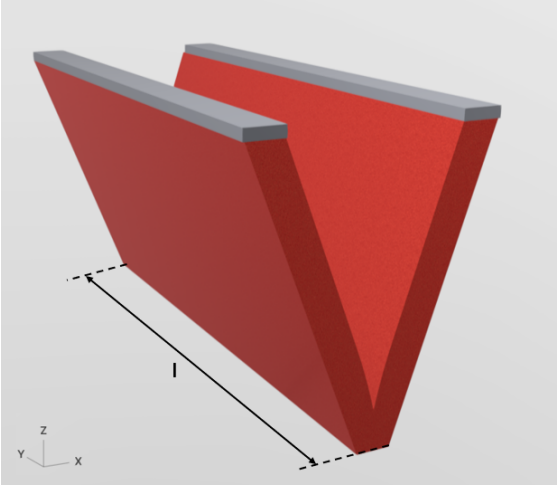

Figure 3.2: Example of a V-groove

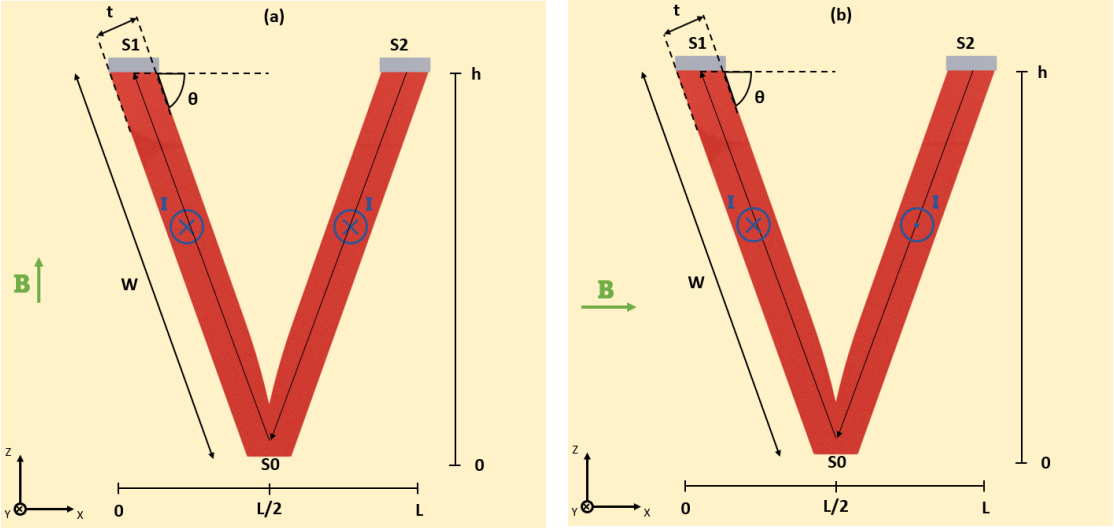

Figure 3.3: The two working modes of a V-groove: (a) Bz mode and (b) Bx mode

Let us apply a three dimensional magnetic field, i.e. $\boldsymbol{B} = B_x\,\hat{\boldsymbol{i}} + B_y\,\hat{\boldsymbol{j}} + B_z\,\hat{\boldsymbol{k}}$. The Hall voltage can be obtained by integrating the Hall electric field in a path that joins the sense contacts. Let us choose a path that follows the V-shaped sides, and let us exploit the properties of integrals to break down this path into two sub paths:

$$V_H = \int_{S2}^{S1} \boldsymbol{E_H}\, d\boldsymbol{l} = \int_{S2}^{S0} \boldsymbol{E_H}\, d\boldsymbol{l} + \int_{S0}^{S1} \boldsymbol{E_H} d\boldsymbol{l} \tag{3.2}$$

Now, let us focus on the first integral. Recalling Equation 2.12 and choosing a path that lies in the section's plane (such that $d\boldsymbol{l} = dx\,\hat{\boldsymbol{i}} + dz\,\hat{\boldsymbol{k}}$), we get:

$$V'_H = -\int_{S2}^{S0} R_H(\boldsymbol{J}\times\boldsymbol{B})\,d\boldsymbol{l} = \int_{S0}^{S2} R_H(\boldsymbol{J}\times\boldsymbol{B})\,(dx\,\hat{\boldsymbol{i}} + dz\,\hat{\boldsymbol{k}}) \tag{3.3}$$

Solving the cross product and remembering that the only component different from zero is J_y, we reach:

$$\boldsymbol{J}\times\boldsymbol{B} = J_y B_z\,\hat{\boldsymbol{i}} - J_y B_x\,\hat{\boldsymbol{k}} \tag{3.4}$$

Substituting this in Equation 3.3, we obtain:

$$V'_H = R_H J_y(B_z\int_{\frac{L}{2}}^{L} dx - B_x\int_0^h dy) = R_H J_y(B_z\frac{L}{2} - B_x h) \tag{3.5}$$

Getting back to the second integral, we notice that the cross product result is exactly the same. The integrals, however, have different upper and lower bounds:

$$V''_H = R_H J_y(B_z\int_0^{\frac{L}{2}} dx - B_x\int_h^0 dy) = R_H J_y(B_z\frac{L}{2} + B_x h) \tag{3.6}$$

Finally, we get that the Hall voltage difference between the two contacts is given by:

$$V_H = V'_H + V''_H = R_H J_y B_z L \tag{3.7}$$

and using Equation 3.1 and Equation 2.7 to substitute J_y and R_H we obtain:

$$V_H = \frac{r_H}{nqt}\frac{L}{W} I B_z = 2\frac{r_H}{nqt} cos\,\theta I B_z \tag{3.8}$$

θ is the etching angle that, in our case, is 54.74°.
Therefore, we have a device that uniquely detects the z component of the magnetic field, whose absolute sensitivity is given by:

$$S_A^z = 2G_H\frac{r_H}{nqt} cos\theta I \tag{3.9}$$

where the geometric correction factor is introduced to take into account the finite dimension of the device.

Now, let us consider again the same section but let us push the two currents in opposite directions. Again, the Hall voltage is given by Equation 3.2 and V''_H can be obtained by means of Equation 3.6.
The only different term is V'_H, which presents a negative sign in front of it:

$$V'_H = -R_H J_y(B_z\frac{L}{2} + B_x h) \tag{3.10}$$

Consequently, the Hall voltage is given by:

$$V_H = V'_H + V''_H = R_H J_y B_x h \tag{3.11}$$

which can be also written as:

$$V_H = 2\frac{r_H}{nqt}\frac{h}{W} I B_x = 2\frac{r_H}{nqt} sin\theta I B_x \tag{3.12}$$

We have obtained a result that depends exclusively on the x component of the magnetic fields. The absolute sensitivity of this mode is given by:

$$S_A^x = 2G_H \frac{r_H}{nqt} sin\theta I \tag{3.13}$$

The current-referred sensitivities of the two working modes are obtained by normalizing the results by the biasing current:

$$S_I^z = 2G_H \frac{r_H}{nqt} cos\theta \tag{3.14}$$

$$S_I^x = 2G_H \frac{r_H}{nqt} sin\theta \tag{3.15}$$

The voltage-referred sensitivities can be obtained, instead, starting from the absolute sensitivity and applying Ohm law:

$$I = \frac{1}{R} V = nq\mu \frac{Wt}{l} V \tag{3.16}$$

which substituted in Equation 3.9 and Equation 3.13 gives the following formulas:

$$S_V^z = 2G_H \mu_H \frac{W}{l} cos\theta \tag{3.17}$$

$$S_V^x = 2G_H \mu_H \frac{W}{l} sin\theta \tag{3.18}$$

It is very interesting to notice that, for $\theta = 0$, the current-related and voltage-related sensitivities of the z- mode (S_I^z and S_V^z) become exactly 2 times the scaled sensitivities of a Hall plate device. At the same time the x- mode sensitivities (i.e. S_I^x and S_V^x) become equal to zero. This actually makes sense, since for $\theta = 0$ the V-groove reduces to two horizontal Hall devices one next to the other.
For $\theta = 90$, instead, S_V^x and S_I^x reach the global maximum while S_V^z and S_I^z instead become equal to zero. This again makes sense, since in this case we would have two Hall plates but 90° degrees rotated, so that their active region is perpendicular to x- component of the magnetic field.

The most intriguing result, however, is the fact that a decrease in the V-groove thickness causes an increase in both the x- and y- sensitivities, as is the case for Hall plates. This implies that, in principle, this device could be made CMOS compatible.

The y-component of the magnetic field can be detected by rotating the V-groove of 90° around the z-axis. Therefore, two orthogonal V-grooves should be realized to detect both x- and y- components of the magnetic field.
PYRAMID can be seen, in a certain sense, as a compact and reproducible way to introduce two V-grooves in a Silicon substrate.
The x- and y- components of the magnetic field can be obtained simultaneously by pushing four currents, one per side, in the device. Each couple of parallel currents must flow in opposite directions.
The z- component, instead, can be obtained by pushing two parallel currents that flow in the same direction. A better insight into the PYRAMID working modes is reported in section 3.3.
Assuming that PYRAMID can be represented as two orthogonal V-grooves, the current-related sensitivities of PYRAMID are the ones extracted in the previous analysis. Regarding the voltage-related sensitivities, we can even go a step further stating that L=l in the case of a PYRAMID sensor. Consequently, the formulas extracted for the V-groove become:

$$S_V^z = G_H \mu_H \tag{3.19}$$

$$S_V^{x/y} = G_H \mu_H tan\theta \tag{3.20}$$

This means that, in principle, the only dependence on geometry is inside the geometrical correction factor. However, this factor typically depends only on the ratio $\frac{W}{l}$ and not on the effective dimensions of the devices. This implies that an exact scaling down of PYRAMID, keeping constant all the ratios, should not degrade the sensitivity.

3.2 The models: COMSOL vs SENTAURUS

To obtain a higher number of results and with the aim of comparing and validating them, the simulations were performed with two different simulators: COMSOL and SENTAURUS.

COMSOL is a multiphysics simulation software that implements models and equations to study many different physics and engineering applications. Despite that, it does not implement modules that efficiently simulate semiconductor-related problems.

Therefore, to simulate PYRAMID with the lowest computational effort, the study was reduced to an electrical conduction problem. This means that the only physics used was "Electric currents". In addition, only the N-doped active region was taken into consideration and modeled.
The device is consequently reduced to a conductive pyramidal "shell", whose side and thickness are parameterised. The thickness of the pyramid is a simple and naive representation of the junction depth (i.e. the point at which the device doping and the substrate doping become equal). However, it does not reproduce accurately a real device since it assumes a constant doping profile and not a Gaussian distribution. The height is fixed to preserve the characteristic angle of KOH/TMAH etching of 54.74°.
8 squared contacts were placed at the middle sides and at the four corners, on which the "Voltage"/"Ground" and "Floating Potential" boundary conditions were applied based on the specific mode simulated.

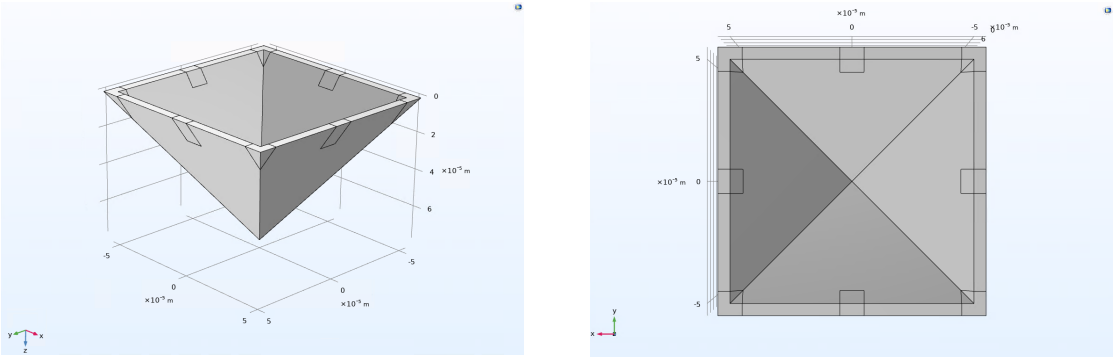

Figure 3.4: The COMSOL model of the PYRAMID sensor

The Hall effect has been introduced only in COMSOL 6.1, while the version used for this work is COMSOL 5.6. Consequently, to reproduce the effect of a magnetic field on the semiconductor, the conductance tensor was explicitly defined inside the "J-E relation" of the boundary condition "Current conservation". The nine tensor coefficients (reported in Equation 3.21) were extracted from Equation 2.4, and the material parameters (see Table 3.1) were specified for a silicon layer doped with Phosphorous, with concentration $1 \cdot 10^{16}\ cm^{-3}$.

$$\sigma = \begin{bmatrix} \sigma_H[1+(\mu_H B_x)^2] & \sigma_H[\mu_H Bz + \mu_H^2 B_x B_y] & \sigma_H[\mu_H^2 B_x B_z - \mu_H B_y] \\ \sigma_H[\mu_H^2 B_x B_y - \mu_H B_z] & \sigma_H[1+(\mu_H B_y)^2] & \sigma_H[\mu_H^2 B_y B_z - \mu_H B_x] \\ \sigma_H[\mu_H^2 B_x B_z - \mu_H B_y] & \sigma_H[\mu_H^2 B_y B_z - \mu_H B_x] & \sigma_H[1+(\mu_H B_z)^2] \end{bmatrix} \tag{3.21}$$

$$\sigma_H = \frac{\sigma_0}{1+(\mu_H B)^2} \tag{3.22}$$

$$\mu_H = r_H \mu \tag{3.23}$$

Parameter	Value	Unit
σ_0	188.54	S/m
μ	0.1177	1/T
r_H	1.03	//

Table 3.1: Material parameters of the COMSOL model

The magnetic field B is nothing more than a parameter defined in the scope of each study, which means that this model works under the assumption of uniform magnetic field.
The result is a very efficient and lightweight model that can perform many different parametric sweeps in a reasonable time. This is the model that was mostly used in the course of this work.

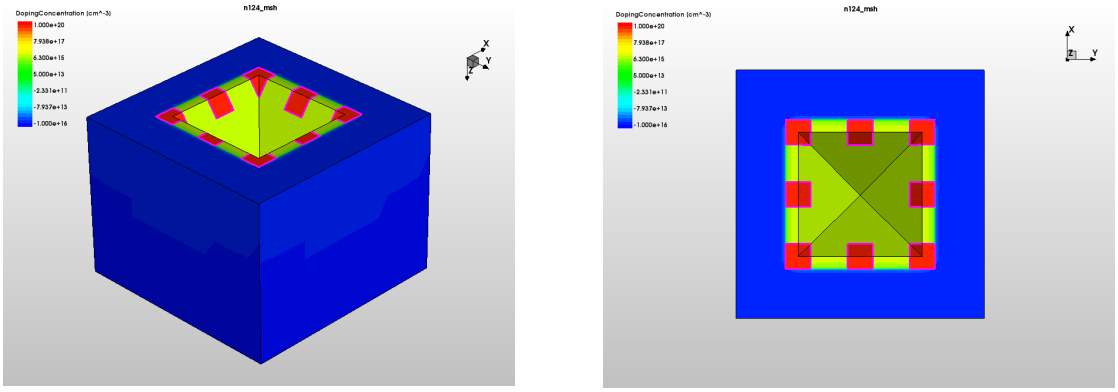

Figure 3.5: The SENTAURUS model of the PYRAMID sensor

SENTAURUS is instead a suite of tools, specialized in the simulation of technological processes and devices realized in semiconductor materials.
The device/model was realized with the 'sde' tool (SENTAURUS Structure Editor): a block of lightly boron-doped silicon (concentration: $1 \cdot 10^{16}\ cm^{-3}$) was instantiated, on which the pyramidal-shaped hole was engraved. The side dimension was parameterised, and the PYRAMID height was fixed to preserve a constant angle of 54.74°. The pyramid shaped hole was then doped with phosphorous. To reproduce the technological processes that concretely produce the device in a more accurate way, the phosphorous dopant distribution was chosen to be a Gaussian with peak at the surface. The peak doping value and the junction depth were both defined as

design parameters.
The 8 contacts were again placed at the corners and in the middle of the four side, but in this case the 20x20 μm squared pads were doped with Arsenic. The dopant distribution was again a Gaussian with peak at the surface, with maximum doping $1 \cdot 10^{20}\ cm^{-3}$ and junction depth 300 nm. The model obtained can be observed in Figure 3.5.

Successively, this model was simulated with the SENTAURUS tool 'sdevice'. 'Sdevice' solves numerically the Poisson equation and the continuity equations both for electrons and holes on each element of the device mesh. The effect of the magnetic field is taken into account by the galvanic transport model, which complements the adopted transport model (by default: drift-diffusion) introducing a series of terms that depend on B [27]:

$$\boldsymbol{J_\alpha} = \mu_\alpha \boldsymbol{g_\alpha} + \mu_\alpha \frac{1}{1 + (\mu^*_\alpha B)^2} [\mu^*_\alpha \boldsymbol{B} \times \boldsymbol{g_\alpha} + \mu^*_\alpha \boldsymbol{B} \times (\mu^*_\alpha \boldsymbol{B} \times \boldsymbol{g_\alpha})] \tag{3.24}$$

with $\alpha = n, p$.
g_α is the current vector without mobility, while μ^*_α is the Hall mobility.
It is interesting to notice that the magnetic-dependent terms of this equation are the same as Equation 2.4, but with a different notation.

This model is, from a fundamental standpoint, more exact and rigorous than the one realized in COMSOL. However, its computational cost is extremely high even for a relatively low number of mesh elements. Therefore, each simulation takes a very high amount of time and cannot be used to perform numerous series of parametric sweeps.

For this reason, the SENTAURUS model was only used to validate the results obtained with COMSOL and to obtain a better insight into more semiconductors physics-oriented problems.

3.3 The PYRAMID modes

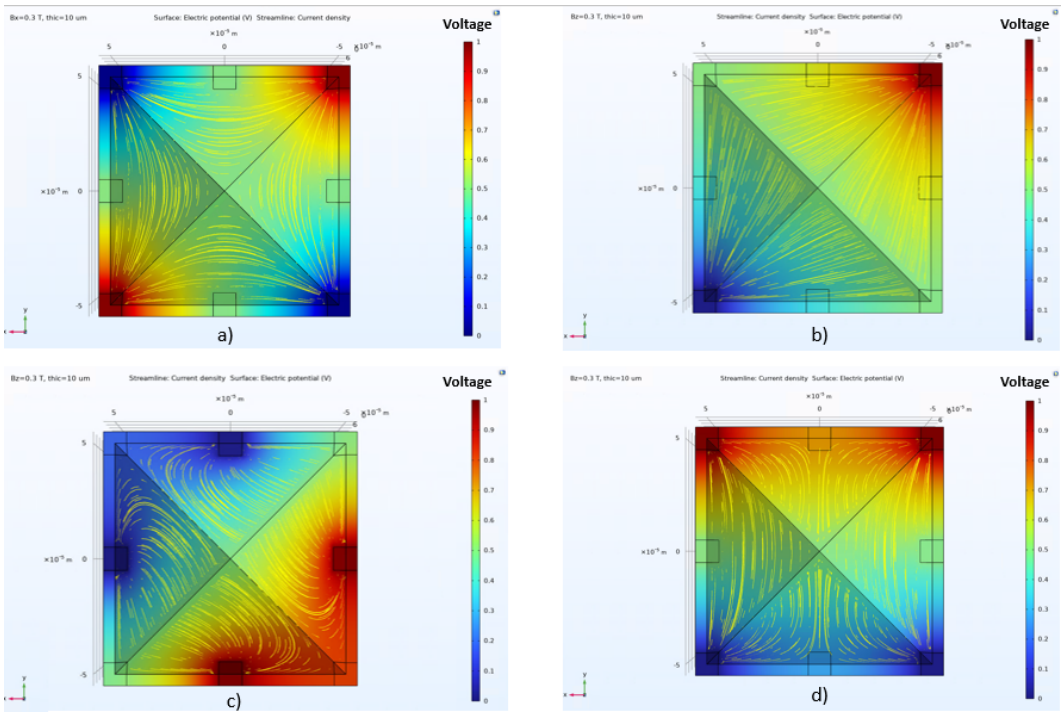

Figure 3.6: The four PYRAMID modes: a) B_{plane}, b) B_{z1}, c) B_{z2}, d) B_{z3},

The PYRAMID device presents 5 different operation modes: one planar mode (B_{plane}), three out-of-plane modes (B_{z1},B_{z2} and B_{z3}) and one 3D mode (B_{3D}). The first four PYRAMID modes are represented in Figure 3.6.
Extracting the theoretical sensitivity of each of these modes is not an easy task (only done for B_{plane} and B_{z3}, see section 3.1). However, the component of the magnetic field sensed by each mode can be easily understood by analyzing the Lorentz force that acts on each current of the device.
For example, let us consider B_{plane}. The B_{plane} mode allows the measurement of the x- and y-components of the magnetic field at the same time. Now, let us consider two out of the four currents that flow in the device. Let us choose, in particular, the two currents that flow parallel to the y-direction, but with opposite verses (see Figure 3.7). When an out-of-plane magnetic field is applied, both currents are bent away from the sense contacts (S1 and S2 in the picture). As a consequence, in stationary conditions the two sense contacts present the same absolute voltage and the Hall voltage difference will be zero. On the other hand, when an in-plane magnetic field is applied (B_x, in this example), one current is "pushed" toward the substrate while the other current is "pulled" toward the surface. However, the

sloped surface of PYRAMID forces the "pulled" electrons to accumulate at the right sense contact, producing a measurable Hall voltage difference.
Repeating the same reasoning with all the other modes, the magnetic field components sensed and the relative sense contacts can be obtained.

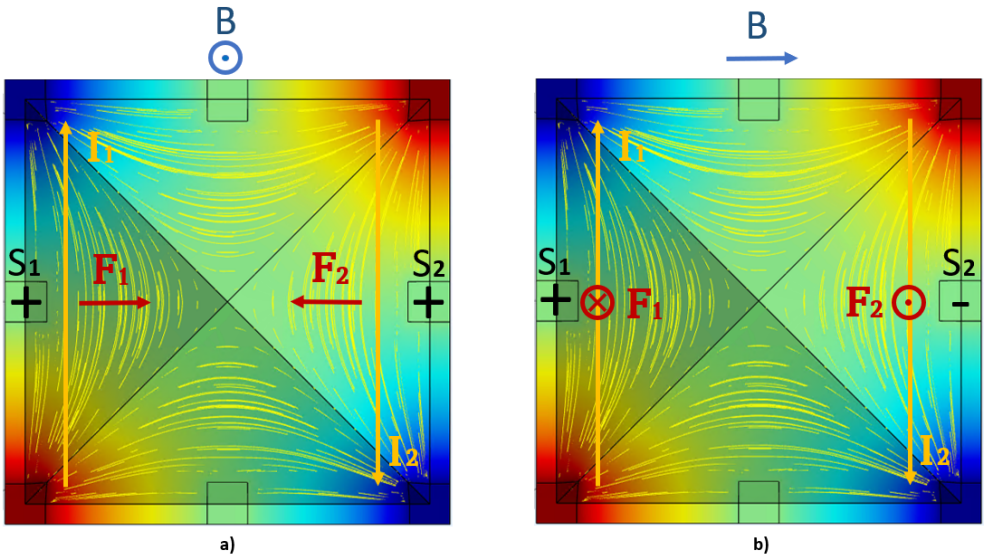

Figure 3.7: B_{plane} mode: a) with an out-of-plane magnetic field applied; b) with an in-plane magnetic field applied

B_{3D} is instead represented in Figure 3.8. This is a peculiar and interesting mode since it allows the measurement of the three components of the magnetic field at the same time. To understand B_{3D} working mechanism, let us suppose that the currents flow in a straight line from the positively-biased contacts toward the negatively-biased contacts (see Figure 3.8). When a magnetic field is applied, each sense contact (i.e. the four contacts at the corners) will manifest a voltage that is a superposition of the Hall voltages generated by each component of the magnetic field:

$$\begin{cases} V_{S_1} = -\frac{V_z}{2} + \frac{V_x}{2} + \frac{V_y}{2} \\ V_{S_2} = +\frac{V_z}{2} + \frac{V_x}{2} - \frac{V_y}{2} \\ V_{S_3} = -\frac{V_z}{2} - \frac{V_x}{2} - \frac{V_y}{2} \\ V_{S_4} = +\frac{V_z}{2} - \frac{V_x}{2} + \frac{V_y}{2} \end{cases} \tag{3.25}$$

Therefore, if we linearly combine the voltages measured at the sense contacts we can extract three quantities that depend exclusively on the x,y and z components

of the magnetic field:

$$\begin{cases} V_z = -\frac{V_{S_1}+V_{S_3}-V_{S_2}-V_{S_4}}{2} \\ V_x = -\frac{V_{S_3}+V_{S_4}-V_{S_1}-V_{S_2}}{2} \\ V_y = -\frac{V_{S_3}+V_{S_2}-V_{S_1}-V_{S_4}}{2} \end{cases} \tag{3.26}$$

The results of the 3D mode simulations are shown in Figure 3.9: we can see a good linearity but also a certain cross-sensitivity for magnetic field components that are not the ones that we want to measure. This is related to the fact that the hypothesis "current flows straight between bias contacts" is not completely true, which introduces a cross-contamination between different signals.
These are the only simulations performed for this mode: despite being quite intriguing, B_{3D} might be particularly difficult to optimise.
This means that a better and more accurate analysis is left for future work.

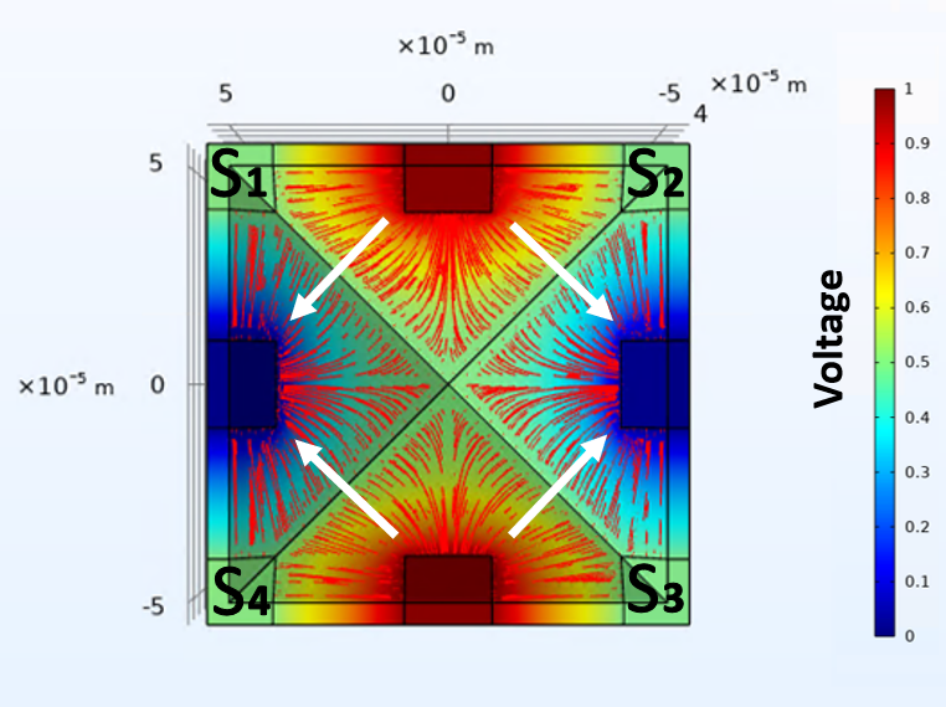

Figure 3.8: The 3D mode: the white arrows represent the simplified current flows adopted in the theoretical analysis.

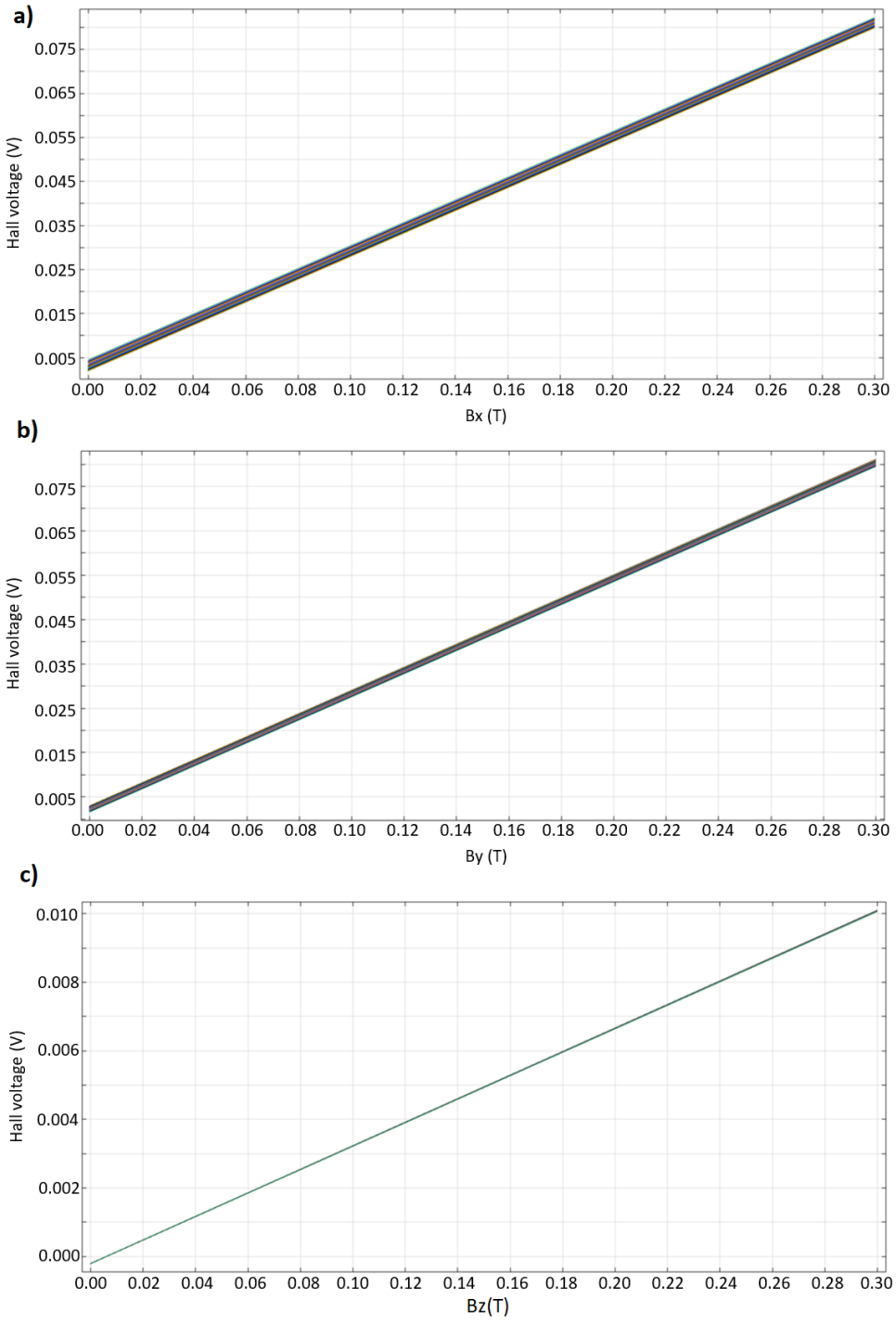

Figure 3.9: The 3D mode simulations: a) V_H vs B_x; b) V_H vs B_y; c) V_H vs B_z

3.4 PYRAMID simulations

3.4.1 Overview and linear range

As previously stated, most of the simulations were performed with COMSOL and validated with SENTAURUS.
If not explicitly specified, the magnetic field was swept from 0 to 0.3 T in at least 30 points. The devices were biased with a constant voltage of 1 V.
The design parameters that were studied and swept are PYRAMID size, contact sizes, junction depth/thickness and doping.
The main performance parameters that were investigated are the voltage- and current-related sensitivities. The current-related sensitivity is simply obtained by normalizing the absolute sensitivity with the current that flows in the biasing contacts.
Noise and offset were not studied and left for future work.

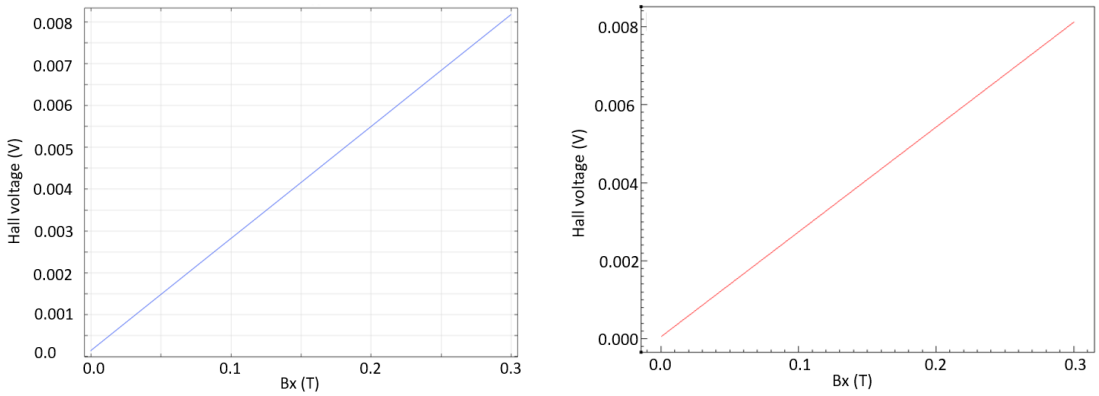

Figure 3.10: Comparison between the COMSOL (left) and SENTAURUS (right) simulations of the B_{plane} mode

Figure 3.10 shows the Hall voltage vs magnetic field curves, simulated for a device of size 100 μm, contact sizes 20 μm, thickness 5 μm and doping $1 \cdot 10^{16}$ cm^{-3}. The mode considered in this simulation is B_{plane}.
This simulation was performed both with COMSOL and SENTAURUS and it gave results that are perfectly compatible, showing the actual reliability of the COMSOL model.
Successively, the magnetic field range was extended to 30 T and the simulation was repeated for both B_{plane} and B_{z3}.
The COMSOL results are represented in Figure 3.11. We can see that PYRAMID presents a non-linear behaviour around 5 T, both for the B_{z3} and B_{plane} modes.

The reason for this divergence stands in the second-order magnetic field dependence of the conductance/resistivity of the Hall device, not considered in the simple model presented in section 3.1.

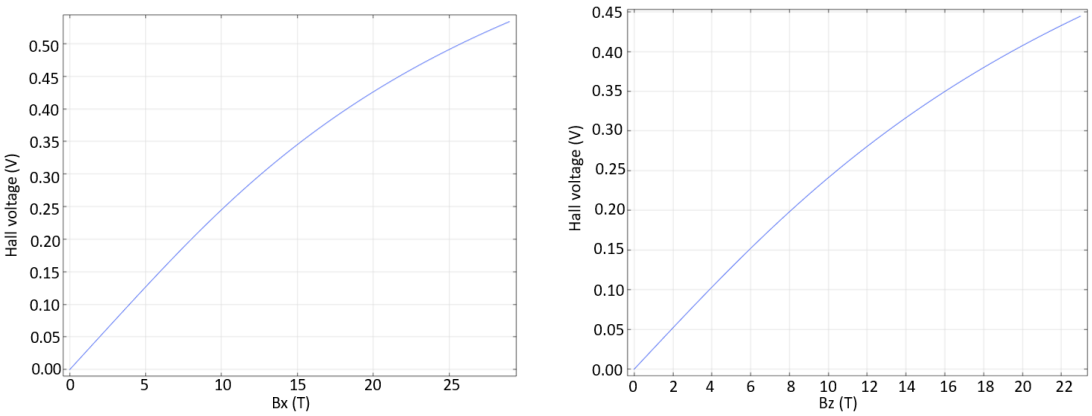

Figure 3.11: Linearity of the B_{plane} and B_{z3} modes

3.4.2 Doping and junction's depth

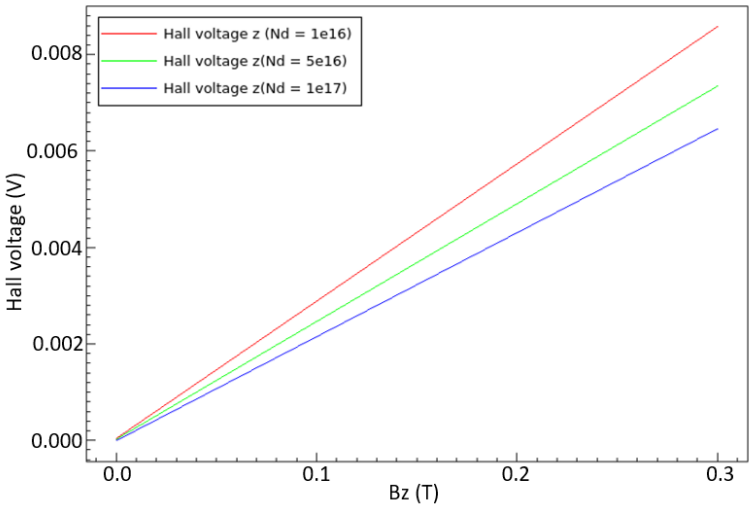

Figure 3.12: Hall voltage vs B_z for three different n-well dopings: $1 \cdot 10^{16}\ cm^{-3}$, $5 \cdot 10^{16}\ cm^{-3}$ and $1 \cdot 10^{17}\ cm^{-3}$

After these preliminary simulations, the effect of doping and junction depth/thickness were investigated. In this case, SENTAURUS was adopted to study the impact

that different dopings have on the device. SENTAURUS was preferred to COMSOL in order to exploit the implemented models that take into account the effect of doping variation on the materials' parameters.
The size of the PYRAMID was again fixed to 100 μm, the contact sizes to 20 μm and the junction depth to 10 μm. This relatively high junction depth was chosen to reduce the dimension and number of the mesh elements, increasing the simulation speed. The doping was swept in three different points: $1 \cdot 10^{16}$ cm^{-3}, $5 \cdot 10^{16}$ cm^{-3} and $1 \cdot 10^{17}$ cm^{-3}. The results can be observed in Table 3.2.

N_D (cm^{-3})	S_V $(\frac{mV}{VT})$	I_{bias} (mA)	S_I $(\frac{V}{AT})$
$1 \cdot 10^{16}$	28.5	0.634	45.0
$5 \cdot 10^{16}$	24.5	2.41	10.2
$1 \cdot 10^{17}$	21.5	3.95	5.4

Table 3.2: Sensitivities for different doping values

As we can see, the absolute/voltage-related sensitivity of the device decreases with increasing doping as a consequence of mobility degradation. Additionally, a higher doping implies a higher current flowing between the biasing contacts, which in turn decreases the current-related sensitivity. The voltage-related and current-related sensitivities, as well as the biasing current measured at the biasing contacts, are reported in Figure 3.12.

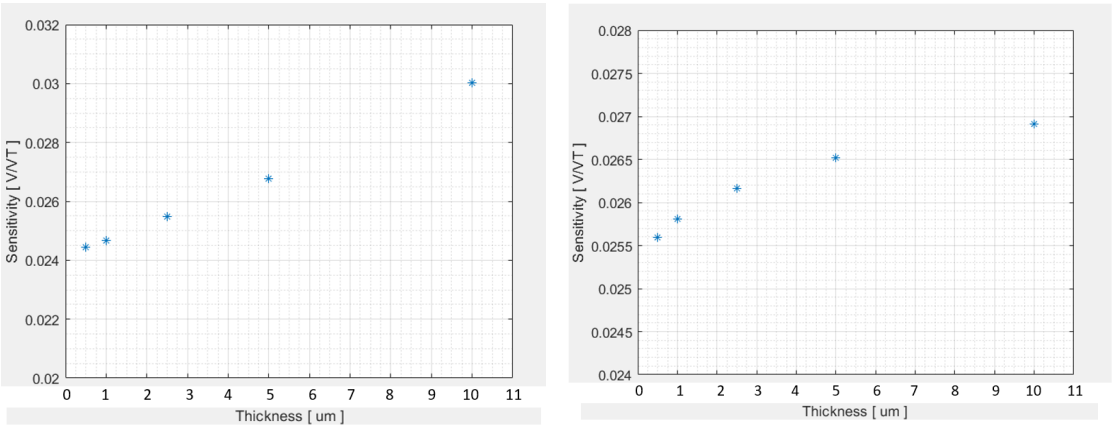

Figure 3.13: Voltage-related sensitivity vs thickness for B_{plane} (left) and B_{z3} (right)

Regarding the thickness, its effect on the device sensitivity was again studied in COMSOL.

The PYRAMID side and the contact sizes were kept respectively to 100 μm and 20 μm, while the doping was fixed to $1 \cdot 10^{16}$ cm^{-3}.
The device was simulated for five different thicknesses: 0.5 μm, 1 μm, 2.5 μm, 5 μm and 10 μm.
The modes studied were, in this case, B_{plane} and B_{z3}. The voltage-related and current-related sensitivity were extracted and plotted.
We can see that for both modes the voltage-referred sensitivity (Figure 3.13) slightly increases with the thickness of the device. However, this dependence is not well understood since, theoretically, the junction depth should not affect the voltage-related sensitivity of these two modes.
For what it concerns the current-referred sensitivity (Figure 3.14), it decreases with the thickness with a $\frac{1}{x}$ trend. This is an extremely good result that is actually in line with the theoretical model shown in section 3.1. It consolidates the fact that a shallow junction depth does not degrade but enhances the current-related sensitivity both for planar and out-of-plane modes.

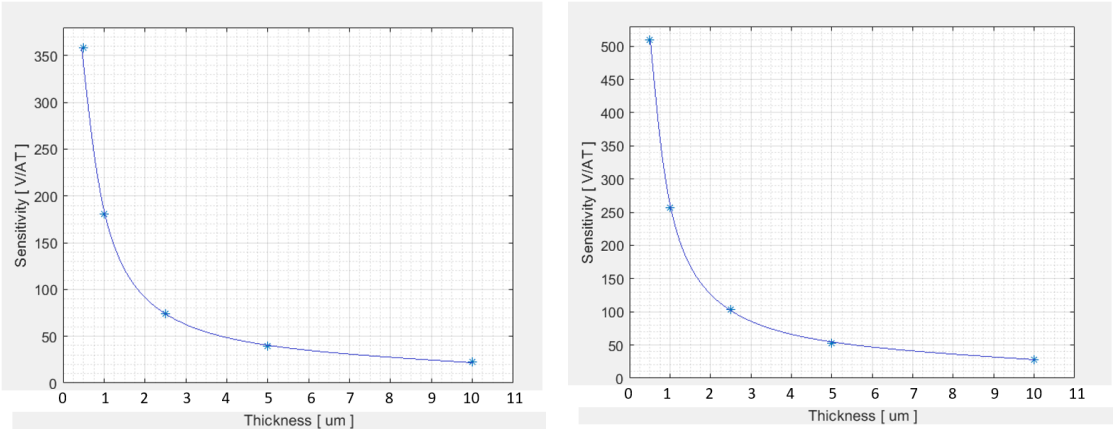

Figure 3.14: Current-related sensitivity vs thickness for B_{plane} (left) and B_{z3} (right)

3.4.3 Geometrical effects: PYRAMID and contact sizes

Successively, the effect of different PYRAMID sizes was extrapolated.
All the simulations reported in this section were done with doping $1 \cdot 10^{16}\ cm^{-3}$ and thickness 2.5 μm.
Theoretically, both voltage-referred and current-referred sensitivities should not depend on the PYRAMID size. However, the simulations proved a different trend.

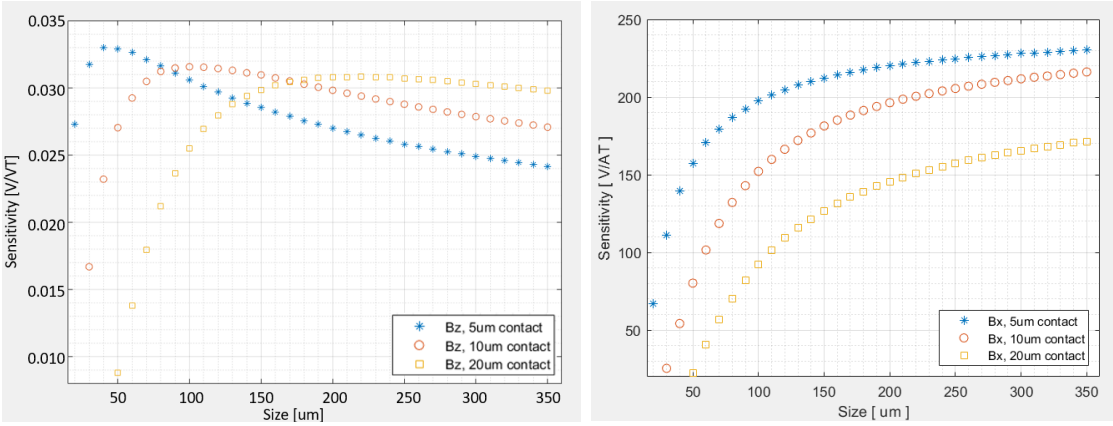

Figure 3.15: Voltage- and current-referred sensitivities vs PYRAMID size for three different contact sizes: 5 μm, 10 μm and 20 μm. The mode simulated is B_x.

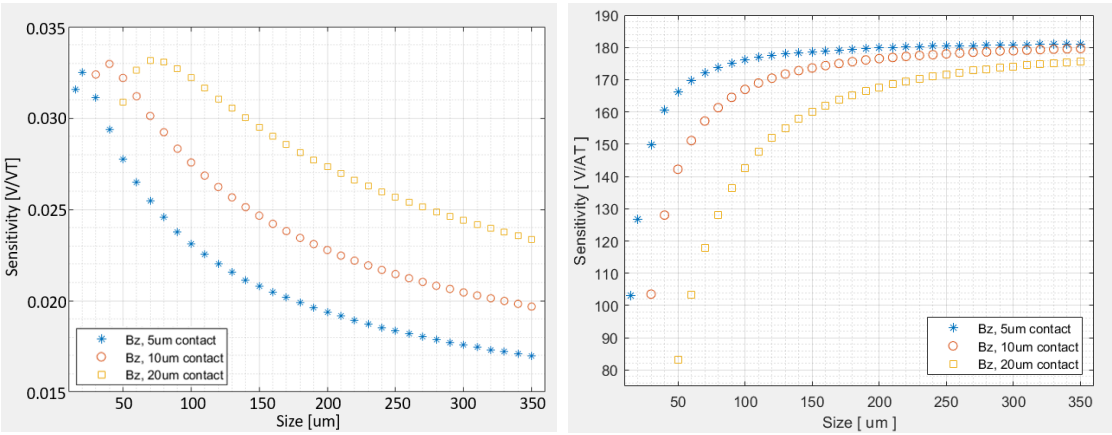

Figure 3.16: Voltage- and current-referred sensitivities vs PYRAMID size for three different contact sizes: 5 μm, 10 μm and 20 μm. The mode simulated is B_{z1}.

Figure 3.15 and Figure 3.16 show the voltage- and current-related sensitivities

for three different contact sizes: 5 μm, 10 μm and 20 μm. The results are reported for B_{plane} and B_{z1}, but other simulations proved that modes B_{z2} and B_{z3} share the same trend of B_{plane}. Figure 3.17 instead shows a comparison between the four modes with contact size fixed to 10 μm.
This unexpected behaviour can be explained by taking into account a parameter that was not considered in the simple theoretical derivation: the finite contact size. Looking at the graphs we can see that, in fact, the contact dimension has an effect on the sensitivity of the device, modifying the trend of the "sensitivity vs PYRAMID size" graphs. Contact dimension and PYRAMID side dependencies are therefore strongly intertwined. This fact suggests that the sensitivities do not depend independently on the value of these two parameters, but rather on the relative dimension of the contacts compared to the PYRAMID size.

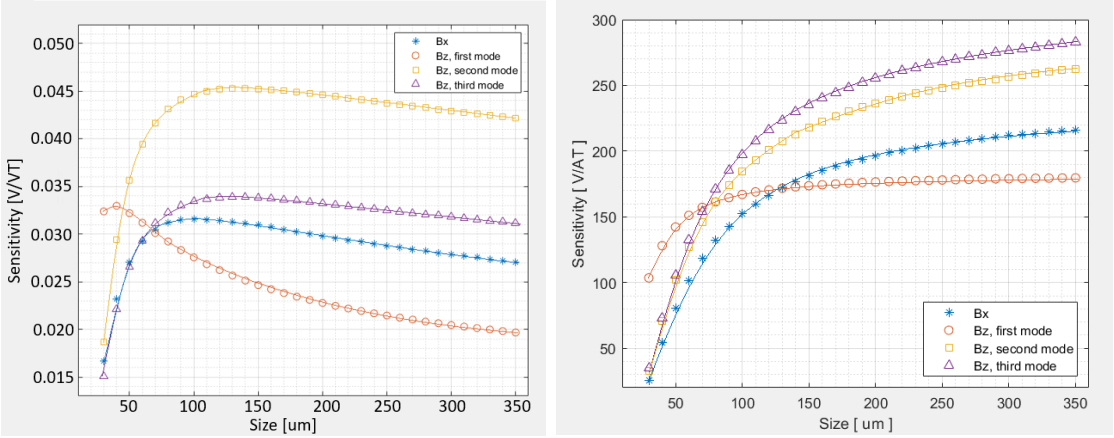

Figure 3.17: Comparison between the different modes. The contact size is fixed to 10 μm.

Assuming that this hypothesis is true, we can therefore suppose that keeping a constant ratio between PYRAMID and contact sizes will produce the same sensitivity, whatever the PYRAMID dimension. The relative effect of the finite contacts would be, in this case, exactly the same whatever the PYRAMID and contact dimension. We can then return to the simple theoretical results obtained in section 3.1 by introducing the side-to-contact ratio dependence in the geometrical correction factor G_H.
This assumption is confirmed by the simulations, reported in Figure 3.18. From these graphs we can see that different device sizes present almost the same current- and voltage-related sensitivities, if the PYRAMID side-to-contact ratio is kept constant. The specific behaviour of these curves depends on the mode taken into consideration.

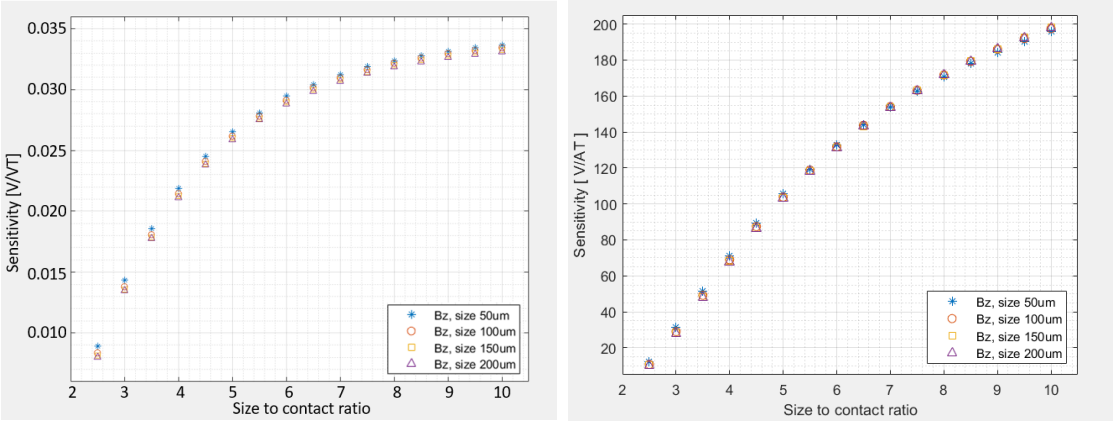

Figure 3.18: Sensitivity vs size-to-contact ratio for different PYRAMID sizes (mode B_{z3}).

Keeping in mind these outcomes, the next step was to vary the dimension of the sense contacts with respect to the bias ones.
The results obtained are reported in Figure 3.19 (only B_{plane} reported). For every mode we can witness an increase in both sensitivities, which is higher or lower depending on the mode considered. For example, B_{plane} shows an 88% increase in voltage-related sensitivity, if we compare a device with the highest ratio studied (4:1) to a device with contact-to-contact ratio 1:1. Mode B_{z2}, on the other hand, shows an increase of only 8 %.

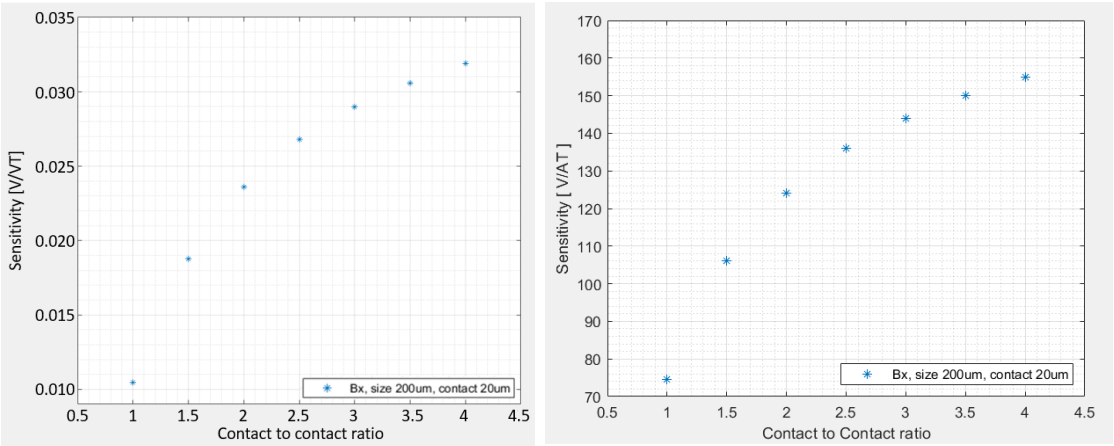

Figure 3.19: Sensitivity vs contact-to-contact ratio (mode B_{plane})

3.4.4 Offset control

The last analysis that was carried out in the course of this work involved the bias voltage. 3 out of 4 modes (B_{plane},B_{z2} and B_{z3}) present 4 instead of 2 biasing contacts, contrarily to what happens in standard Hall devices.
In every analysis performed in the previous paragraphs, the same biasing voltage difference was applied to each couple of electrodes.
For this study, instead, one pair of contacts was biased with 1 V while the other was biased with a different voltage: 2 V for the first simulation and 0.5 V for the second one.
The results can be observed in Figure 3.20. As we can see from this graph, this bias difference determines the appearance of an offset that can be controlled by varying the ratio between the two biases.
The reason behind this effect is that the presence of two different voltages introduces an artificial asymmetry inside the PYRAMID structure, which in turn causes an offset in the response.
The offset control introduces a further degree of freedom inside PYRAMID, not present in other Hall devices. It could be exploited to correct the shift in the output response in a straightforward way, compensating the physical asymmetries of the device by means of an artificially introduced bias asymmetry.

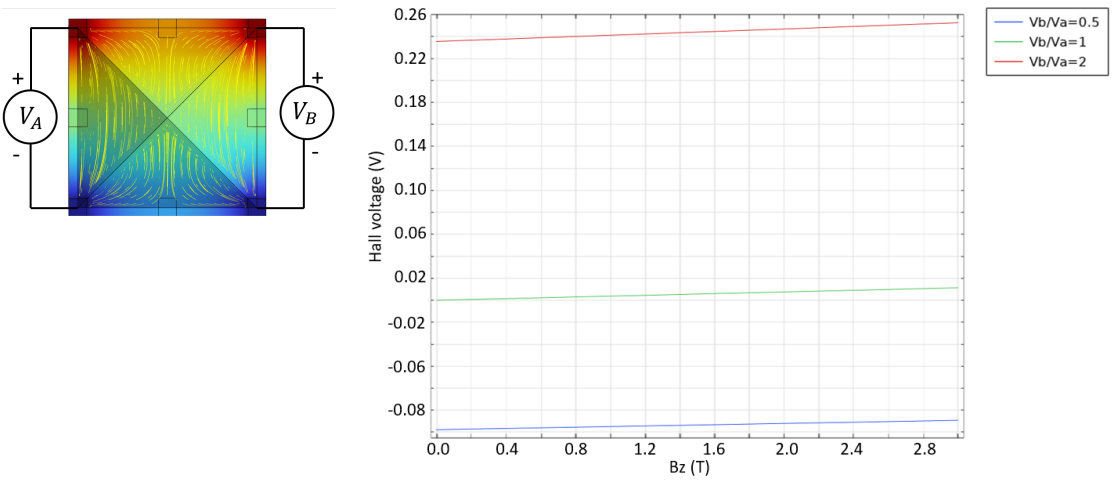

Figure 3.20: Offset control for mode B_{z3}

3.5 Conclusion

To conclude the chapter, this paragraph will summarize all the relevant results that were obtained from the simulations:

- A low doping boosts both current- and voltage- referred sensitivities. To maximize the performances a relatively low doping should be adopted, being aware that the lower the doping the higher the flicker noise.
- A shallow junction depth implies a high current-related sensitivity. Nonetheless, ultra-shallow junctions should be avoided since the p-n junction that the active layer forms with the substrate determines the presence of a depleted region. In the worst case, the application of a voltage could cause a pinch-off of the layer or, eventually, its complete depletion.
- For most modes, small contacts are better than big contacts. Mode B_{z1} is an exception since it is optimized for relatively large pads.
- Keeping the sense contact size smaller than the bias one always determines a boost in both sensitivities. Despite that, it must be noticed that co-optimization of different modes is only possible if they share the same bias and sense contacts. This means that an optimal contact-to-contact ratio for B_{z1} and B_{z2} determines automatically a worsening in the performances of modes B_{plane} and B_{z3}.

From these considerations, an optimal device should have low doping and junction depth, small bias contacts (compared to the PYRAMID side) and even smaller sense contacts.
Since co-optimization of all the modes is not possible, an eventual commercial device should arguably exploit mode B_{z3} to measure the out-of-plane magnetic field. The reason is straightforward: it shows one of the highest current-related sensitivity and has the same bias and sense contacts of B_{plane}. Additionally, this mode presents 4 bias contacts instead of 2, which means that its offset can be controlled.

Chapter 4

Fabrication of PYRAMID

This chapter addresses the main part of the whole project, the fabrication of the PYRAMID device.
The process flow is first displayed in a summarized form, and it is later broken down into steps that are detailed in the subsequent paragraphs. Each main technological processing choice is pondered and the final decisions are carefully justified.
To conclude, the main achievements of this process run are summed up in a short conclusion.

4.1 Fabrication overview

The complete process flow is shown in Figure 4.1.
The p-doped substrate was covered with a silicon nitride layer, deposited with LPCVD, that plays the role of hard mask for the anisotropic etching of silicon.
The features were opened through dry etching of the Si_3N_4, and then the pyramid-shaped holes were created by means of TMAH wet etching of silicon.
Successively, a thin layer of silicon oxide was thermally grown to create a dirt barrier layer, and the pyramids were doped with a low-dose phosphorous implantation.
The sample was later annealed to activate the dopants and diffuse them inside the substrate to obtain the desired junction depth.
The silicon nitride and the dirt barrier were removed by means of wet etching with orthophosphoric acid and a second dirt barrier was thermally grown for the consequent N+ implantation.
To define the N+ doped contact regions, the cavity was covered with spray coated photoresist that was successively patterned. Spin coated photoresist, in fact, does not ensure conformal coverage of the cavities and therefore cannot be used with sloped or high aspect ratio cavities/features.
The open areas were then doped with a low-energy high-dose arsenic implantation.

The photoresist was stripped and the dirt barrier was removed with BHF wet etching.
Next, a silicon oxide passivation layer was deposited by means of LPCVD. The sample was subsequently annealed at a high temperature to increase the oxide density, activate the implanted arsenic dopants and heal the substrate damage at the same time.
The sample was again spray coated with photoresist and patterned to define the contact openings in the silicon oxide, that was later etched by means of BHF wet etching.
Finally, after an HF dip etch that removed the native oxide from the contact surface, a layer of aluminium-silicon was sputtered on the sample. The layer was spray coated and patterned to define the interconnections, and then etched through wet processing.
A polysilicon dip etch and the subsequent alloying in the furnace concluded the process run.

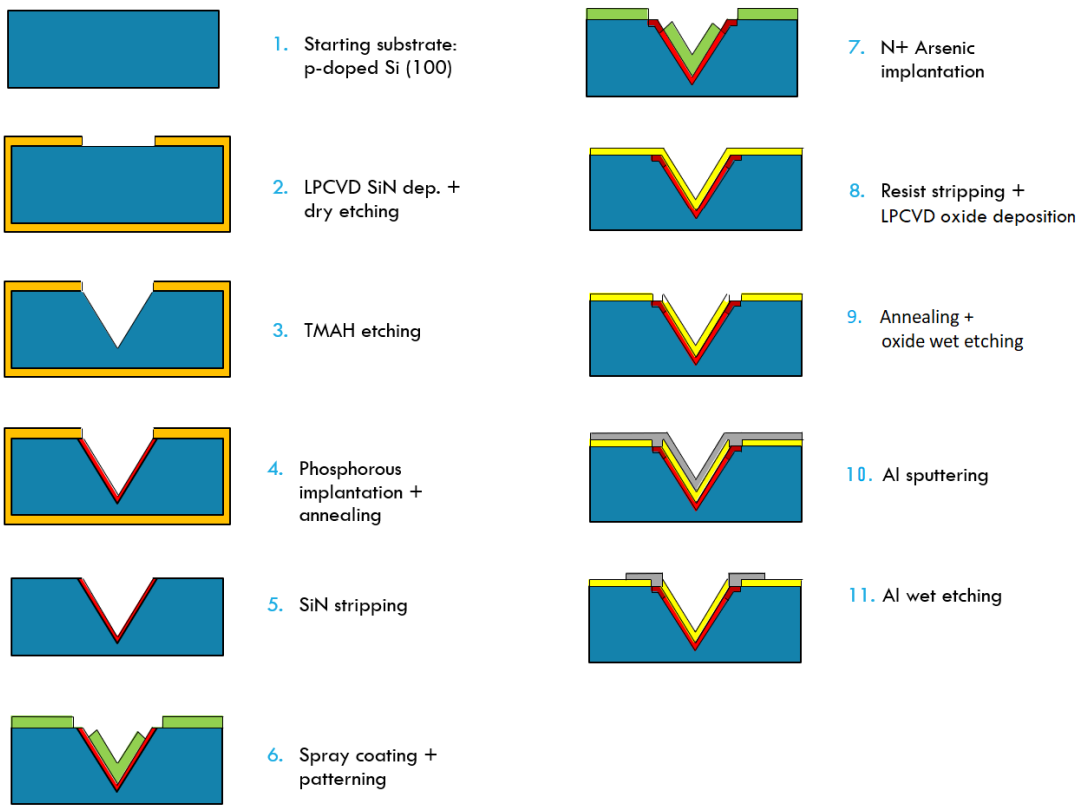

Figure 4.1: The complete process flow

4.2 Detailed process flow

4.2.1 Preliminary information

In this section, each part of the process will be discussed more carefully. Before that, however, some important considerations must be shared.

First of all, the substrates used in this process run were single-side polished boron-doped wafers. The resistivity of these wafers is in the range $1 - 5\ \ \Omega \cdot cm$, which corresponds to a doping range of $3 \cdot 10^{15} - 1.5 \cdot 10^{16}\ cm^{-3}$. This implies that there is an intrinsic variation in the net doping of each processed wafer, based on the starting doping of the substrate. Said that, for the sake of simplicity the starting doping of the substrate will be always considered $1 \cdot 10^{16}\ cm^{-3}$ in future analyses.

Second, the most important part of every micro-technological process is photolithography. In EKL, exposure can be realized either in contact/proximity mode using the SUSS MicroTec MA/BA8 mask aligner, or in projection mode using the ASML PAS 5500/80 waferstepper.
The SUSS contact aligner transfers the pattern of a photo-lithographic mask exposing the whole wafer at the same time. The aerial image is a 1:1 replica of the pattern that is present on the mask. The exposure can be accomplished in hard contact, i.e. pressing the mask against the resist, or in proximity.
The maximum resolution of this tool is around 1 μm, while the alignment of a layer to another one is performed manually. The overlay error is therefore dependent on the ability of the operator.
The ASML PAS 5500/80 wafer stepper instead operates in projection mode: the wafer is exposed die-by-die by means of a set of projection lenses that de-magnify the image on the mask by a 5x factor. This means that the mask shows the pattern of a single die, and after the exposure every single die will present the same identical pattern.
The maximum resolution of this tool is around 500 nm, while the alignment is automatic with an overlay error of around 100 nm.
Comparing the two tools, the wafer stepper has a better resolution, a better overlay error and it is completely automatic, which means that it can process batches of wafers in a much shorter time.
On the other hand, the contact aligner presents a much higher freedom in the design of the masks, which are at the same time much less expensive than the ones for the stepper.
Lastly the wafer stepper, being a projection system, has to define a focus plane before exposure. This is a further parameter that must be optimized for correct pattern transfer, and it is a serious concern in the case of deep cavities and high

aspect ratio features. Features patterned on the sloped sides of cavities, in fact, get progressively out-of-focus moving away from the focal plane. This causes a loss of resolution and a "broadening" of the features.
These problems do not exist with the contact aligner, especially when used in hard contact mode. In this case, the electromagnetic radiation produced by the lamp approximates a planar wave, and every point of the wafer is ideally in focus.
Taking into consideration the pros and cons, the lithography steps of PYRAMID were realized with the wafer stepper. The guarantee of an optimal overlay coupled with a high throughput were the main reasons behind this decision.

Last information, the devices were realized in three PYRAMID side dimensions: 25 μm, 50 μm and 100 μm. Different PYRAMID dimensions were processed on separate wafers. This decision was taken to avoid increasing the undercut on features that are already completely etched (see subsection 4.2.3). Additionally, this choice allowed us to optimize separately the lithographic processes for each feature size.
What is more, each PYRAMID size was doped with two different phosphorous doses to obtain net dopings of $1 \cdot 10^{16}\ cm^{-3}$ and $5 \cdot 10^{16}\ cm^{-3}$.

4.2.2 Lithographic masks

The stepper masks were realized with KLayout, and they can be observed in Figure 4.2. The die size adopted is $10 \times 10\ mm^2$.
There are four layers, one for each lithographic step: KOH, N+, CO and IC. However, the PYRAMID sizes investigated are 3, which implies that the total number of lithographic masks should be 12. To avoid this enormous number of masks, multi-image masks were instead designed. A multi-image presents four quadrants of $10 \times 10\ mm^2$ separated by 1 mm (to block stray light), and each quadrant can host a lithographic image. Before exposure the wafer stepper uses its blanking system, composed of four programmable blades, to block the images that are not used. In this way, more than one image can be stored on the same physical mask, that can be retrieved during the exposure phase.
For this project four multi-image masks were designed, one for lithographic step/layer. Each mask hosts the patterns of four feature sizes: 25 μm, 50 μm, 100 μm and 200 μm (not used in this work).

The mask design includes 9 PYRAMIDs per die, disposed in 3x3 matrixes (see Figure 4.3). Each PYRAMID in the matrix presents different contact sizes, and moving along a row there is an increase of the bias contact size. On the other hand, moving along a column there is an increase in the sense contact size. Increasing the PYRAMID dimension, the contacts are designed to scale up proportionally.

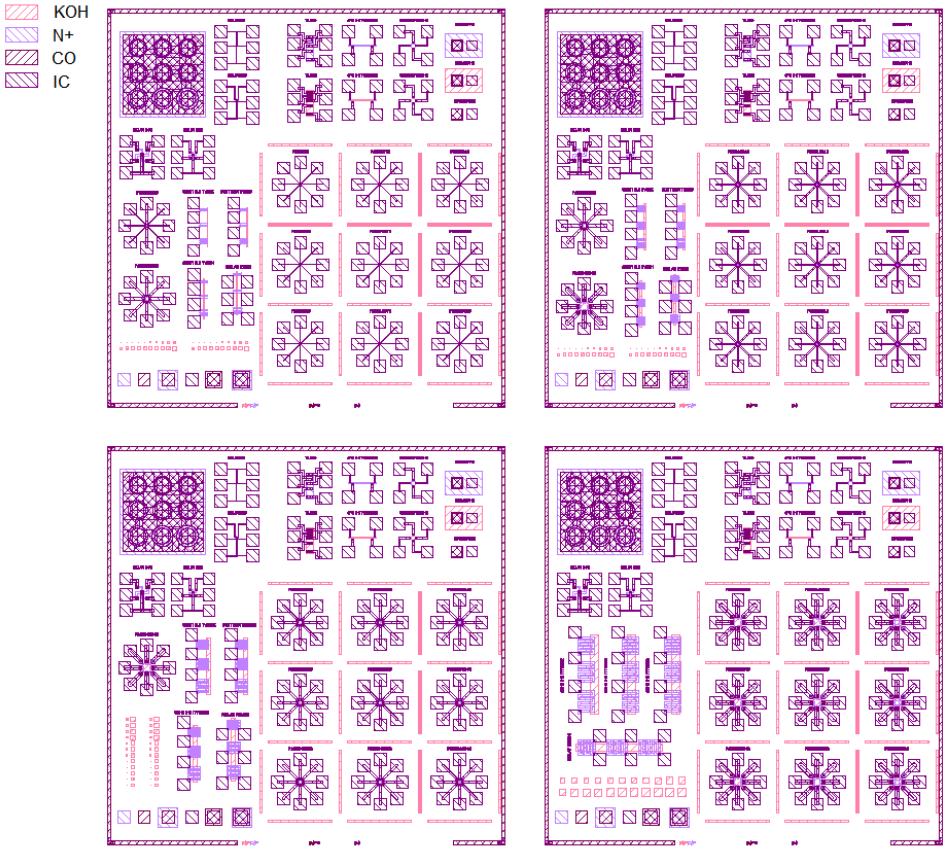

Figure 4.2: The complete mask design

A zoom-in on a single PYRAMID can be seen in Figure 4.3. What is interesting to notice is that the only layer that is patterned on the sloped surface is N+. The other two (CO and IC) lay on the "flat" substrate region. This design choice was made to minimize the number of features patterned on the cavity walls, simplifying considerably the lithographic process optimization.

To fill the remaining space on the die, several testing structures were designed and added: TLMs, 4-probe measurement structures, Kelvin, Van der Pauw and MOSCAPs for both N-well and N+ implantation.
What is more, a MOSCAP for silicon substrate characterization was introduced, as well as some continuity and isolation structures. To check and characterize the TMAH etching, an etching test structure was also added. Lastly, two PYRAMIDs whose side is 2x and 4x times larger than the current design dimension were included, to eventually observe the behaviour of a non-completely etched PYRAMID.

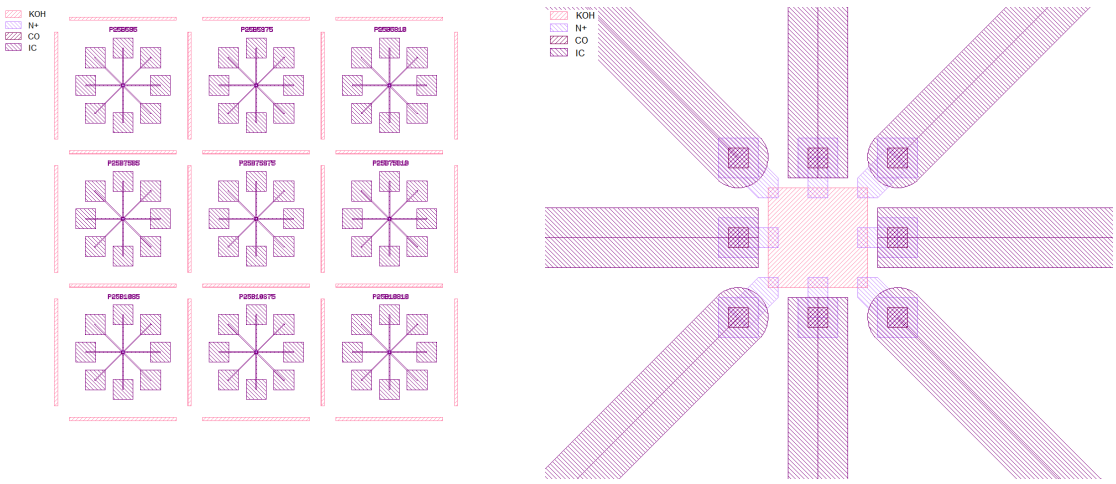

Figure 4.3: PYRAMID mask design

4.2.3 TMAH etching of Silicon

To begin, the zero-layer alignment marks were engraved onto the silicon surface. These 14 marks, located all around the external edge of the wafer, are nothing but diffraction gratings that are exploited by the ASML wafer stepper to align each layer to the next one.
The p-doped substrates were spin coated with a 1.4 μm thick positive resist and patterned. Subsequently, the marks were dry etched by means of Reactive Ion Etching (RIE).
After that, a 500 nm thick stoichiometric silicon nitride layer was deposited using Low Pressure Chemical Vapor Deposition (LPCVD). The deposited Si_3N_4 has a double role:

- **Etching mask**: TMAH and KOH strip photoresist, so a hard mask is required. LPCVD silicon nitride appears to be the best material to fulfill this role, with an etch rate that is virtually zero for both TMAH and KOH. Silicon oxide could have also been used as a good masking material, but silicon nitride was preferred due to its higher chemical resistance. [28]

- **Implantation mask**: the regions that must be implanted are the sloped-walls, which are in correspondence of the areas that have been etched with TMAH/KOH. As a consequence, the hard mask can be reused as an implantation mask. This is very convenient since it allows us to skip a whole lithographic step.
  The thickness of the silicon nitride layer, however, should be enough to guarantee no dopant penetration in the covered areas.

Looking at the graph in Figure 4.4, we can see that a thickness of 300 nm is sufficient to ensure a 99.99% masking effectiveness for energies up to 200 keV.[29] Therefore, a 500 nm thick layer is more than enough to protect the underlying silicon.

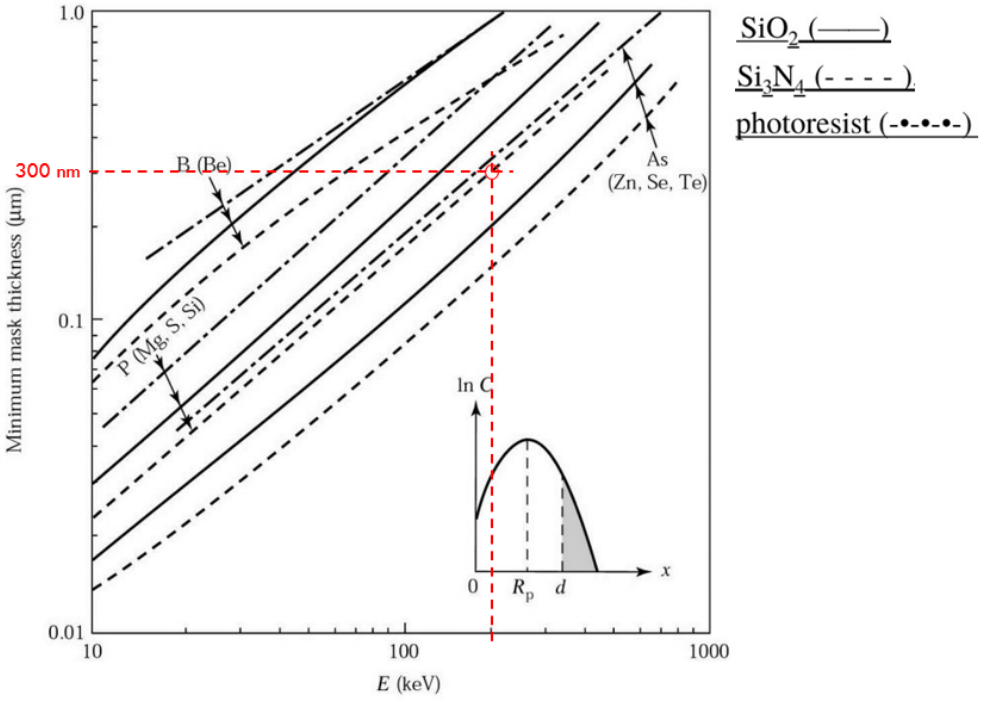

Figure 4.4: Minimum mask thickness to produce a mask effectiveness of 99.99%. [29]

The silicon nitride layer was successively spin-coated with positive photoresist ($1.4\mu m$ thick) and patterned, to be then dry etched by means of RIE.
The resist was stripped with oxygen plasma, and the silicon substrate was etched by means of TMAH.
As already mentioned, TMAH and KOH etch silicon in an anisotropic way: the <100> crystallographic planes are etched much faster than the <111> ones, giving birth to sloped-sided cavities with a characteristic angle of 54.74°.
When all the <100> crystallographic planes are etched away from the cavity, the process is automatically stopped and we obtain a V-groove or a pyramidal hole. In particular, a V-groove is obtained with a rectangular mask opening, while an inverted pyramid is obtained with a squared feature.
Keeping the samples in the chemical bath after the complete formation of the

pyramid/V-groove slowly enlarges the side of the structure, expanding the hole beneath the hard mask.
This is because the <111> etch rate is very small for both KOH and TMAH but different from zero. This means that part of the silicon underneath the hard mask is etched anyway, producing a certain undercut. The anisotropy ratio $\frac{<111>}{<100>}$ is typically used to characterize this phenomenon, which is nothing but the ratio between the <111> planes etch rate and the <100> planes etch rate. The lower the ratio, the lower the undercut.
The etching time to etch completely a squared or rectangular opening is given by Equation 4.1:

$$t = \frac{W}{\sqrt{2}(V_{100} - V_{111})} \tag{4.1}$$

where W is the size of the shortest side of the opening, V_{100} is the etching rate for the <100> crystallographic planes and V_{111} is the etching rate for the <111> ones. Furthermore, the total undercut can be obtained from Equation 4.2:

$$u = \frac{\sqrt{6}}{2} V_{111}\, t_{tot} \tag{4.2}$$

where t_{tot} is the total wet etching time.
As previously explained, both KOH and TMAH can be used to anisotropically etch silicon. However, KOH has in general a higher <100> etching rate, a lower anisotropy ratio $\frac{<111>}{<100>}$ and produces less rough surfaces (for the same concentration and temperature). A comparison between the two chemicals can be found in Figure 4.5. Additionally, KOH is a safer chemical than TMAH.

	TMAH 90°C, 22 wt%	KOH 90°C, 20 wt%
(100) etching rate (μm/min)	1.0	2.5
(110) etching rate (μm/min)	1.4	3.8
Surface roughness (nm)	<100	<100
(111)/(100) etching rate ratio	0.033	2.5×10^{-3}
SiO_2 etching rate (nm/min)	0.23	9.6
Si_3N_4 etching rate (nm/min)	<0.01	<0.01

Figure 4.5: Comparison between KOH and TMAH. [30]

The main problem of KOH is that it is not CMOS-compatible.[28] KOH releases in fact potassium ions that can contaminate MOS gates, worsen passivation layers and break down dielectrics. Additionally, they can out-diffuse if subject to high temperatures, contaminating furnaces and LPCVD tubes. As a consequence,

TMAH was preferred due to its organic nature and total absence of mobile ions. The TMAH etching was performed at 90 °C, with a 25% chemical concentration. A high temperature was employed to increase the <100> etch rate, as well as to reduce the undercut (increasing the $\frac{<100>}{<111>}$ anisotropic ratio). The solution was not further diluted from its starting 25% concentration for the sake of better reproducibility, even though a lower concentration would have increased the <100> etching rate. [31] The final result can be observed in Figure 4.6 and Figure 4.7.

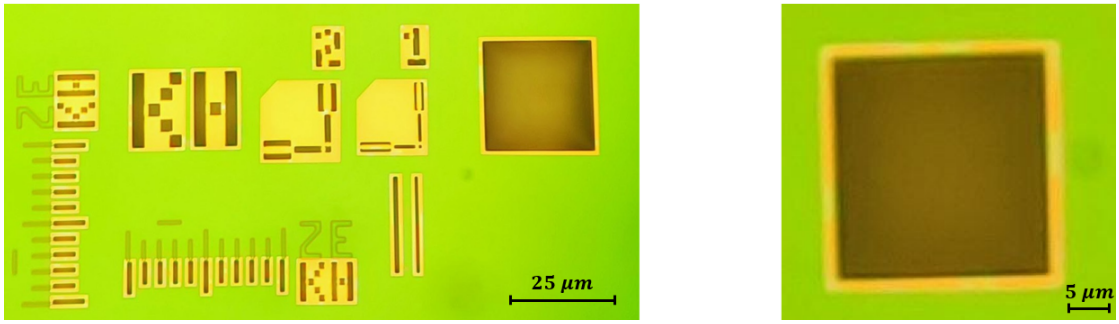

Figure 4.6: Microscope images after TMAH etching, on a 25 μm wafer. The images were taken before removal of the Silicon Nitride layer. Please notice the undercut below the features etched in the masking layer (around 1.3 μm)

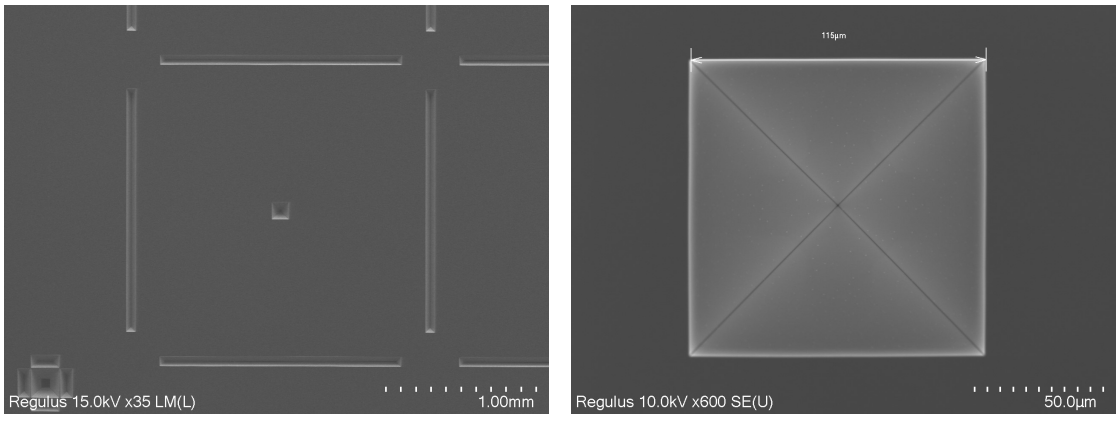

Figure 4.7: SEM images of a 100 μm PYRAMID, after removal of the silicon nitride. The undercut is around 7μm.

4.2.4 N-well implantation

After TMAH etching, the samples were dry oxidized at 950 °C for 35 min to produce a thin silicon oxide layer on top of the sloped walls.

This layer is called dirt barrier and it serves the purpose of blocking mobile ions that are released during ion implantation. These ions could be physisorbed and then they might diffuse inside the silicon, contaminating it. Therefore, this thin silicon oxide layer is grown to block them from reaching the silicon surface. Additionally, since in implantation the doping peak is always hundreds of nanometers away from the surface (especially for higher energies), the dirt barrier partially reduces this distance. Lastly, this layer also helps minimize the channeling effect.
The next step in the process flow is the phosphorous implantation.
As already mentioned, the desired net doping concentrations (at the peak) are $1 \cdot 10^{16}\ cm^{-3}$ and $5 \cdot 10^{16}\ cm^{-3}$. Supposing that the substrate is boron-doped with a concentration of $1 \cdot 10^{16}\ cm^{-3}$, the aimed peak dopings are then $2 \cdot 10^{16}\ cm^{-3}$ and $6 \cdot 10^{16}\ cm^{-3}$.
The desired junction depth is 1 μm, a reasonably shallow junction to obtain a pretty high sensitivity.
With these goals in mind, simulations were performed with SENTAURUS sprocess to get the correct process parameters. In particular, a 1D simulation was performed and the material was selected to be silicon with crystallographic orientation <111>. To avoid shadowing effects and asymmetries in the doping profile, the implantation must be realized with a 0° tilt with respect to the <100> plane. This means that the dopants would hit the <111> surface with an angle of 54.74° degree. Therefore, to ensure that the results obtained from the simulations are correct, an artificial tilting angle of 54.74° was introduced in the model. A thermal oxidation process at 950 °C for 35 min was simulated, followed by the phosphorous implantation and the subsequent annealing. The variable process parameters investigated were the implantation dose, the implantation energy, the annealing temperature and the annealing time.

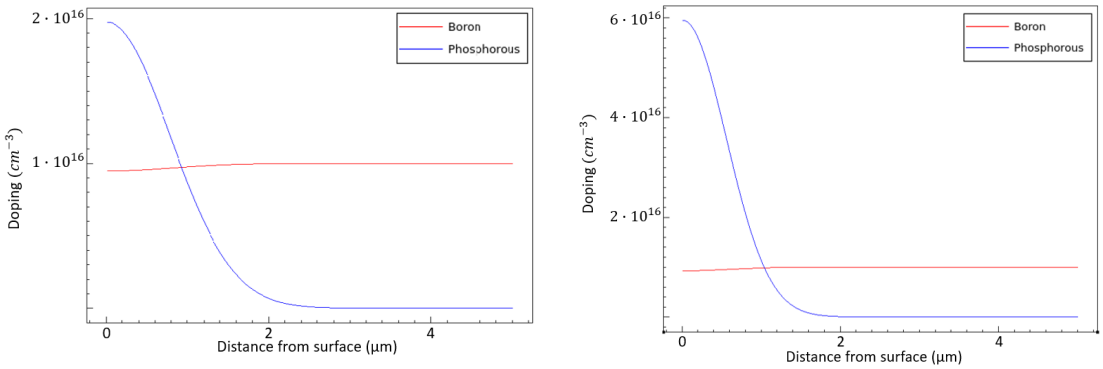

Figure 4.8: N-well doping profiles.

The parameters' values that fulfil the requested specifications are reported in Table 4.1. What is more, Figure 4.8 shows the doping profiles obtained from the simulations.
After the phosphorous implantation, the samples were annealed in an inert atmosphere (N_2). However, the simulated annealing times were reduced respectively to 50 min and 110 min to take into account the ramp-up and ramp-down times of the furnace.
The silicon nitride layer was finally removed by means of wet etching with orthosphoric acid at 157 °C, which stripped both the hard mask and the silicon oxide dirt barrier.

N_D (cm^{-3})	$2 \cdot 10^{16}$	$6 \cdot 10^{16}$
Dose (cm^{-2})	$2 \cdot 10^{16}$	$4.5 \cdot 10^{16}$
Energy (keV)	150	100
Annealing T (°C)	1150	1150
Annealing time (min)	120	60

Table 4.1: Parameters of the n-well implantation

4.2.5 Spraycoating of N+ contact regions

The samples were put again inside the furnace at 950 °C for 35 min to create a dirt barrier layer. This step was followed by the coating of the samples with photoresist and patterning of the N+ contact regions.
Contrarily to the previous lithographic steps, spin coating could not be used to cover the sample.
Spin coating, in fact, coats uniformly the wafer surface exploiting centrifugal force. The photoresist is poured on top of the sample, which is then slowly rotated to distribute the polymer on the whole surface. After that, the speed is increased to reach the desired thickness and create a uniform layer. This technique presents very good uniformity, repeatability and throughput. However, it cannot be adopted for deep cavities and high aspect ratio structures. In fact, the photoresist, due to reflow and the gravitational force, tends to accumulate at the bottom of the cavities leaving the upper edges uncovered.
For this reason, spray coating was adopted instead . During spray coating a diluted photoresist is sprayed on top of a rotating substrate by means of a nozzle. The photoresist is atomized into droplets of some μm thanks to an ultrasonic atomizer, which are then deposited on the sample carried by a pressured nitrogen or air flow. The substrate is placed on a chuck that rotates with a constant velocity, and a mechanical arm moves the nozzle from one side of the wafer to the opposite one with varying velocity. The nozzle arm moves slower in proximity of the edge of

the wafer, and faster toward the center. This is to ensure that each point of the rotating wafer receives more or less the same quantity of resist.
The droplets land randomly on the substrate surface, slowly accumulating until they generate a continuous resist film.
Spray coated resist tends to have a better conformality than spin coating for deep cavities and trenches. On the other hand, the roughness of the resist layer is much higher due to the almost complete absence of resist reflow. What is more, spray coating has a much higher number of deposition parameters that must be re-optimized every single time that a different topography has to be coated. Nozzle pressure, resist dispensed, distance of the nozzle from the surface, chuck rotation, resist viscosity and arm speed profile are only some of these process parameters.

Getting back to PYRAMID processing, positive resist was adopted during this lithographic step. To increase the resist thickness multiple layers were sprayed one on top of the others, with some soft baking steps taken in between the spraying rounds.
Several coating recipes were tried out, but the one adopted was 2 set of 8 layers for 25 μm PYRAMIDs and 3 sets of 8 layers for 50 and 100 μm PYRAMIDs. Each set was followed by a 2 min soft bake at 115 °C, with the exception of the last baking step which was 5 min long. The resist dispensed was 2 mL per set, and the nozzle pressure was 1000 mbar.
The deposited resist was then measured. The resist thickness (measured on the flat area of the substrate) is not uniform: moving from the edge to the center it increases from around 4 to 6 μm on the 25 μm wafers, and from around 6 to 10 μm on the 50 μm ones. This proved to be a serious problem. Different resist thicknesses, in fact, present different doses to clear. This means that, adopting the same exposure dose on the whole wafer, the most external dies are overexposed while the most internal ones are underexposed. The N+ features are quite small and closely spaced, which implies that a too high dose not only broaden but merges close features together. On the other hand, a too low dose does not allow the development of the features.
This problem could be partially solved reducing the thickness of the resist: a reduction in the resist thickness, in fact, improves the aspect ratio and the resolution. However, spray coated resists tend to accumulate at the bottom corner of cavities and thin out on the upper corners, reaching its nominal value only on the planar areas. This means that, to ensure a good corner coverage, the resist on the flat area cannot be made arbitrarily thin.

The coated wafers were then exposed with the wafer stepper. The dose was selected to have the highest possible number of correctly exposed dies. As a consequence, the most central dies were under-exposed and had to be sacrificed.

The wafers were afterward developed in diluted AZ-400K 1:2 with water. The development time was 3-4 min for 25 μm wafers and 7-8 min for 50 and 100 μm wafers. In this way, 47 out of 48 dies were correctly patterned for 25 μm wafers, and 45 out of 48 dies were correctly patterned for 50 μm ones.

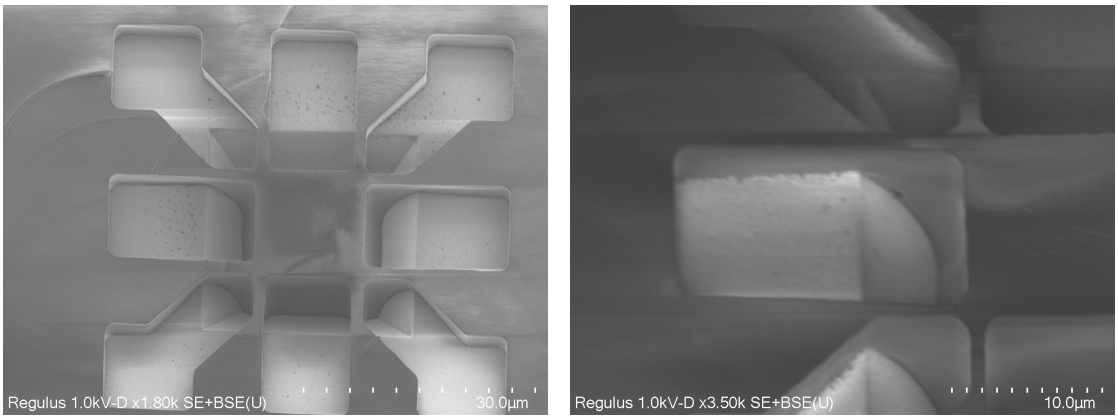

Figure 4.9: The 25 μm patterned PYRAMID.

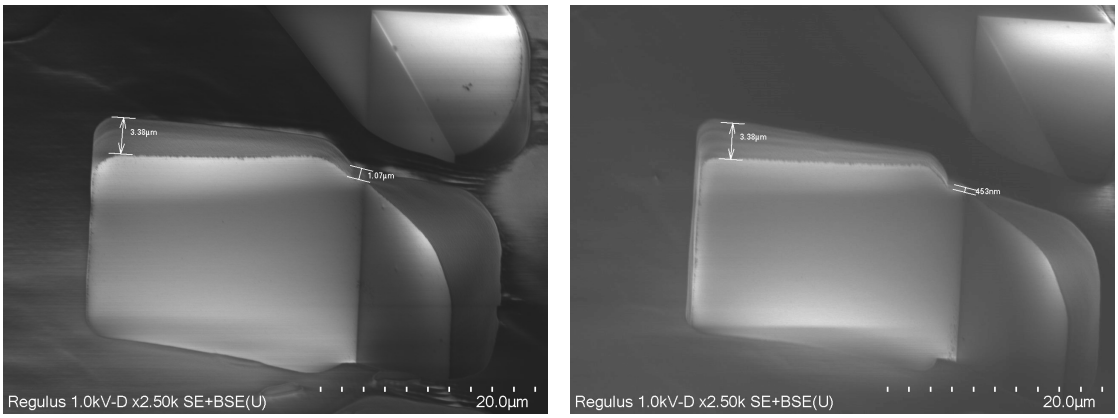

Figure 4.10: Detail of a patterned contact on a 50 μm PYRAMID. The left image was taken on a die closer to the center of the wafer, while the image on the right was taken on a die near to the edge.

The results can be observed in Figure 4.9, Figure 4.10 and Figure 4.11.
We can see that the 25 μm structures present a very thick resist in every point of the structure, even on the upper corners. This is due to the fact that the spray

coated resist managed to almost completely fill the cavities.
50 μm structures instead show instead a die-to-die variation in the corner coverage. In fact, moving from the edge to the center of the wafer the structures show (in general) an increasingly better coverage of the corners.
Additionally, due to the poor aspect ratio of the resist, the features of the PYRAMID with the biggest contacts (3rd row 3rd column on the PYRAMID matrix, see Figure 4.3) merged together. A lower exposure/development time did not help, and actually worsened the situation decreasing the number of correctly patterned dies with no significant improvement. Therefore, this PYRAMID was discarded and considered unfeasible, and we focused on the optimization of the lithographic process for the remaining ones.

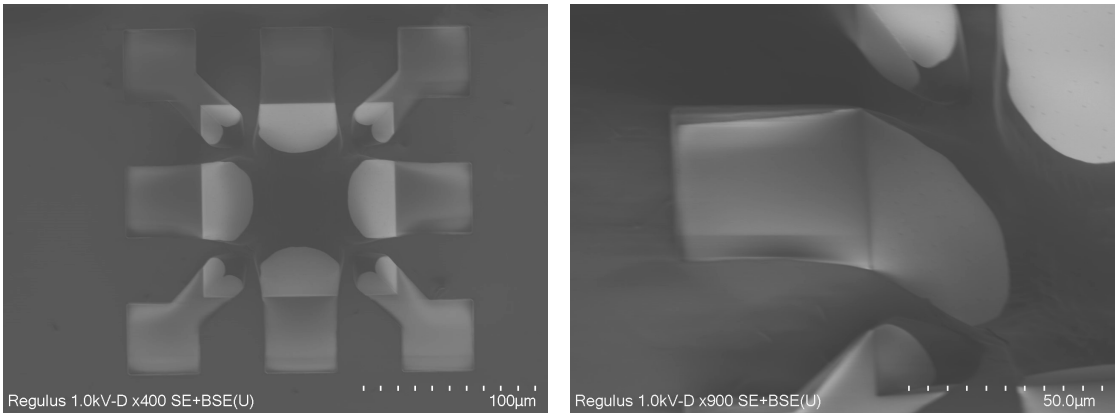

Figure 4.11: The 100 μm patterned PYRAMID.

Lastly, 100 μm structures presented a very thin resist at the corners even with 3 sets of 8 layers. In addition, the patterns were exposed in a slightly "distorted" way moving closer to the bottom of the pyramidal hole. This is due to the fact that, in this case, the featured extends much more deeply in the cavity. As a consequence, the exposing radiation becomes progressively out of focus, enlarging and broadening the contact pads. These facts showed that the 100 μm PYRAMIDs needed more optimization than expected. Therefore, these wafers were dropped and left for eventual future work.
Another interesting thing to notice is that, for both 25 μm and 50 μm structures, the contacts progressively "extend" less in the cavity (see Figure 4.12) moving from the external edge to the center of the wafer. This effect can be related (as well as the die-to-die variation seen in the 25 μm wafers) to the radial thickness gradient produced during spray coating.

The minimum resist thickness necessary to have a good masking can be obtained

from Figure 4.4. Considering a 40 keV arsenic implantation, the minimum thickness required is 90 nm. This value is however referred to standard commercial resists. Spray coated resists are more diluted and typically less dense than spin coated photoresists. Therefore, it is reasonable to assume that their stopping power is slightly lower. On the other hand, this theoretical value is at least 5 times smaller than the minimum resist thickness measured at the SEM. Consequently, we can reasonably assume that this coating is more than enough to efficiently mask the Arsenic dopants during implantation. To conclude, the resist was hard baked in the oven for 10 min at 100 °C to increase its adhesion and improve its stopping power.

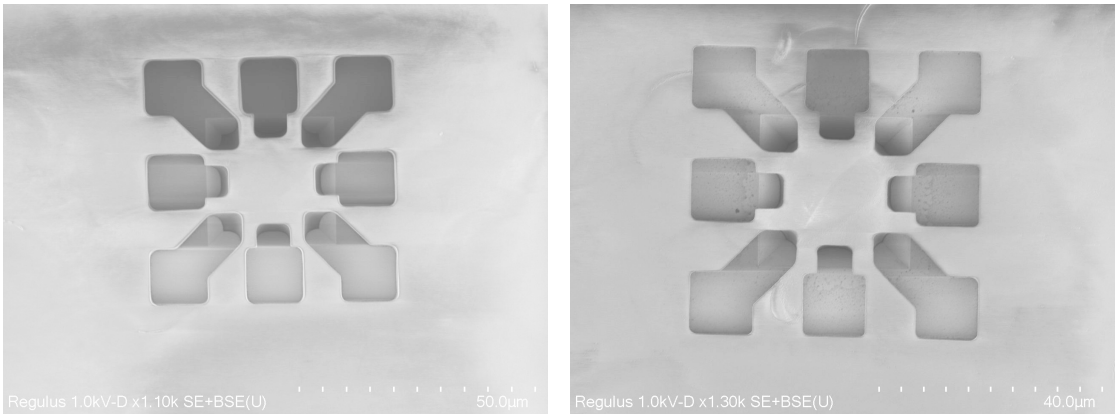

Figure 4.12: Two 25 μm patterned PYRAMIDs. The one on the left is closer to the center of the wafer, while the one on the right is closer to the edge.

4.2.6 N+ contacts implantation

The wafers were then implanted with Arsenic.
Highly doped N+ regions are in fact necessary to ensure a good ohmic/tunneling contact. The dose and energy adopted were respectively $5 \cdot 10^{16} cm^{-2}$ and 40 keV. These are pretty standard values for N+ arsenic implantation, also adopted in the EKL 1 μm BiCMOS technology. [32] The tilting angle was, however, set to 0° and not to the standard 7°. This choice was made to prevent the short-circuiting of adjacent contacts due to tilted implantation over the very thick resist. The negative side of this decision is that the absence of a tilting angle leaves the <100> crystallographic planes subject to ion channeling. In fact, when an ion beam is aligned with a crystallographic axis of a crystalline material the dopant distribution is not completely stochastic anymore. The usual Gaussian profile is superposed to an exponential tail that produces a substantial increase in the junction depth.
Simulations with SENTAURUS sprocess, however, proved that the samples are not subject to this phenomenon. The 22 nm silicon oxide layer, in fact, successfully

prevents the arsenic ions from channeling through the silicon lattice. Additionally, the high dose produces an amorphization of the silicon surface, introducing a second amorphous layer that further reduces the channeling of ions. SENTAURUS sprocess was also used to check the activation of dopants after the annealing step. The total and activated arsenic distribution for both <100> and <111> can be observed in Figure 4.13. We can see that, for the <100> planes, the value at the surface is $3 \cdot 10^{20}\ cm^{-3}$. This value is more than enough to guarantee an ohmic/tunneling metal-semiconductor junction between silicon and aluminium-silicon.

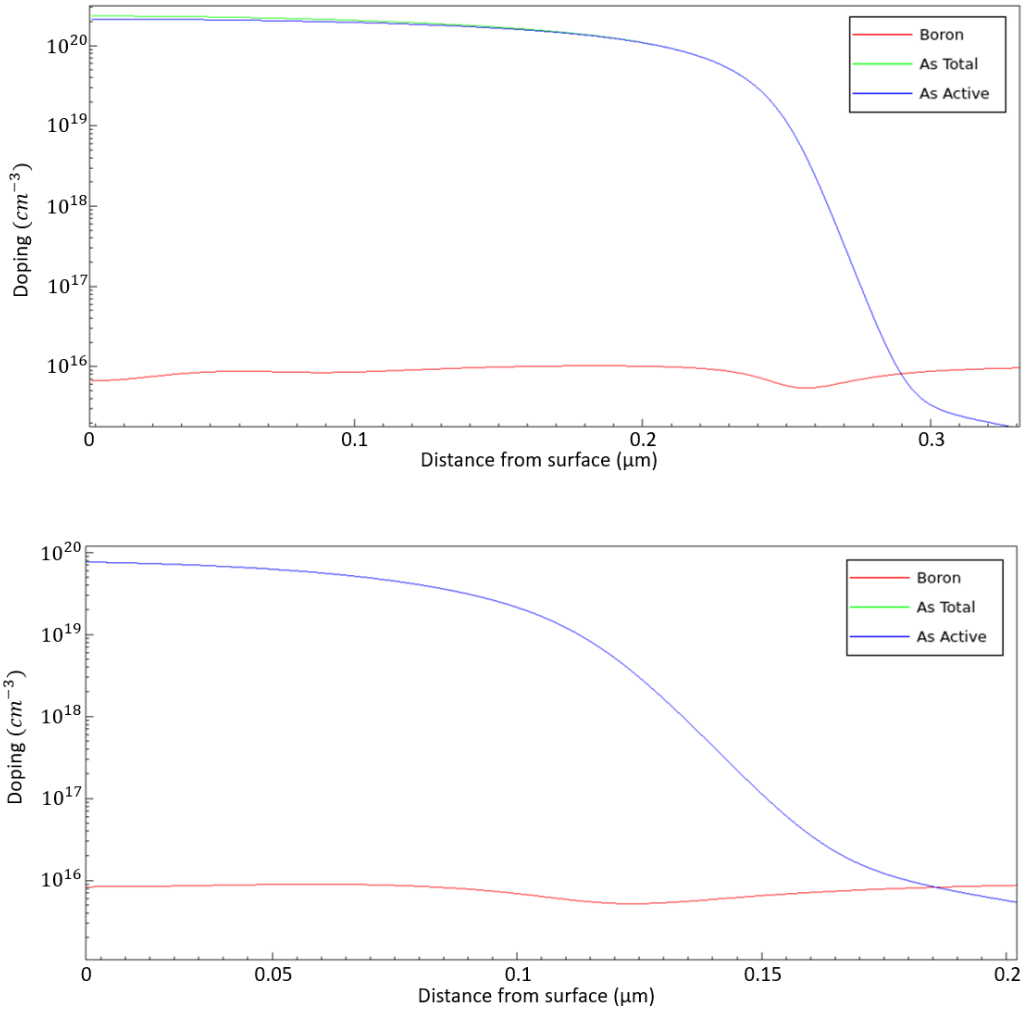

Figure 4.13: N+ doping profiles after annealing, for <100> (up) and <111> (down) planes.

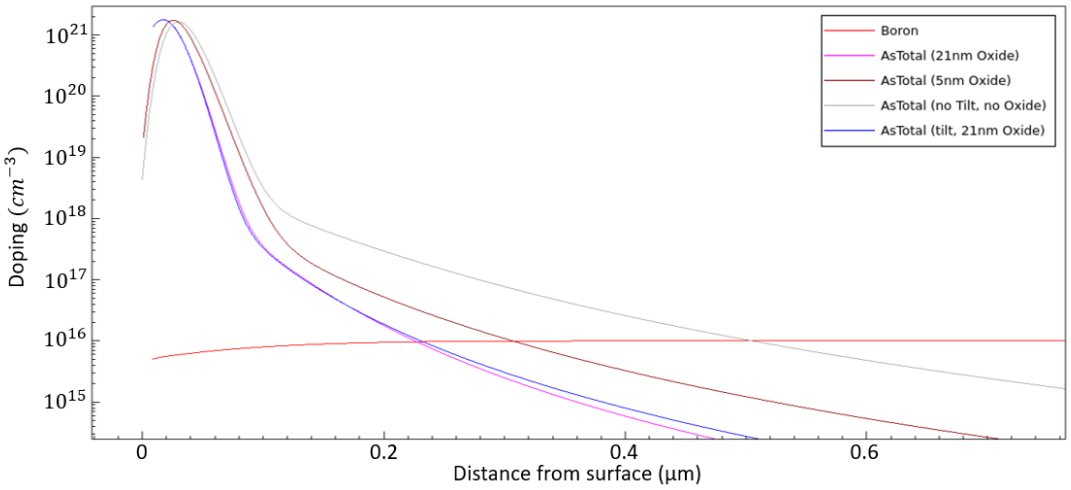

Figure 4.14: Doping profiles after implantation, for different tilts and oxide layer thicknesses. Please notice the absence of channeling for 22 nm of oxide, opposed to 8 nm or no oxide at all.

4.2.7 Passivation of the silicon surface

The next step was the deposition of a 300 nm thick silicon oxide layer. This layer was deposited by means of LPCVD at 750 °C for 43 min, using tetraethoxysilane (TEOS) as precursor. Then, the samples were annealed in the furnace at 1000 °C for 30 min in an inert atmosphere. The annealing step has several roles:

- **Activate the dopants:** Arsenic ions must be driven, after implantation, from their random interstitial position to the crystal lattice sites, where they behave as substitutional impurities.
- **Repair the implantation damage:** as explained, high-dose implantations induce an amorphization of the silicon surface. A thermal treatment is necessary to restore the monocrystalline structure.
- **Densify the LPCVD silicon oxide:** the LPCVD silicon oxide deposited has a good quality but presents a relatively low density. This implies a quite low chemical resistance. A low chemical resistance leads, in turn, to a significant thickness reduction during the next etching steps. The silicon oxide layer is therefore subjected to a thermal treatment to improve its density and etching resistance, at the same time improving the dielectric properties.

Additionally, the annealing was performed after the deposition of silicon oxide so the passivation layer could act as a cap layer, blocking eventual arsenic ions

from out-diffusing from the silicon surface. Despite that, part of the dopants is lost anyway because of the inter-layer diffusion from the silicon substrate to the oxide layer. The diffused arsenic ions partially modify the silicon oxide structure, changing the optical properties only in correspondence of the N+ doped silicon regions. An "image" of the N+ contact area is therefore impressed in the silicon oxide layer, allowing the visual inspection of the implanted areas (see Figure 4.15).

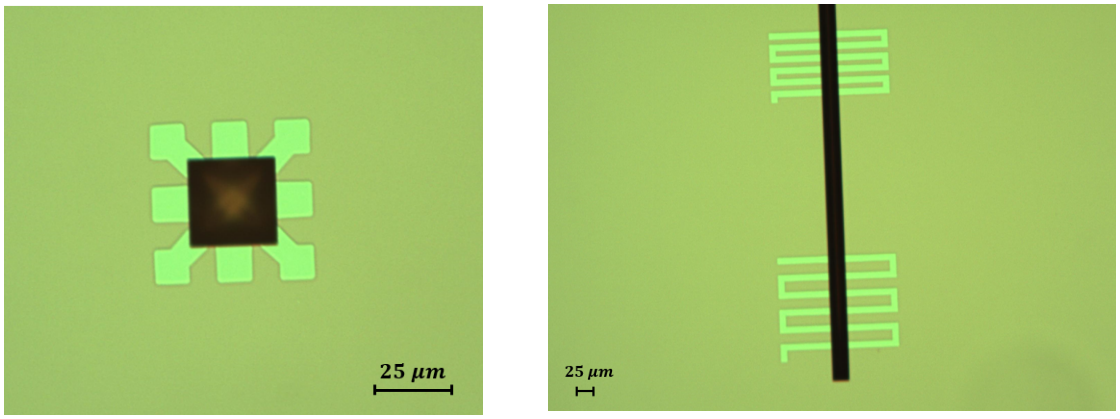

Figure 4.15: A PYRAMID device and a test structure after the annealing. The N+ doped region are perfectly observable on the oxide layer.

Later, the samples were spray coated with positive photoresist. In this case, both 25 μm and 50 μm were coated with 2 steps of 8 layers, with a 2 min and 5 min soft bake at 115 °C after each step.
The samples were exposed with a dose high enough to correctly develop every single die, even the most central ones. The CO features, in fact, are much more spaced than the N+ ones. This means that the most external dies can be overexposed with no problems aside from a slight loss of resolution.
Both the 25 μm and 50 μm were then developed in AZ-400K diluted 1:2 with water. The patterned silicon oxide was later wet etched with BHF diluted with 7 parts of water. Wet etching was preferred to dry etching to avoid the physical bombardment of the resist. The non-selective physical etching, in fact, would have completely removed the resist from the less covered upper corners, partially etching the silicon oxide.
Wet etching, instead, proved to be extremely selective to oxide against spray coated photoresist. On the other hand, the isotropic etching caused a further enlargement of the features. The resist was finally stripped with a 40 °C acetone bath.

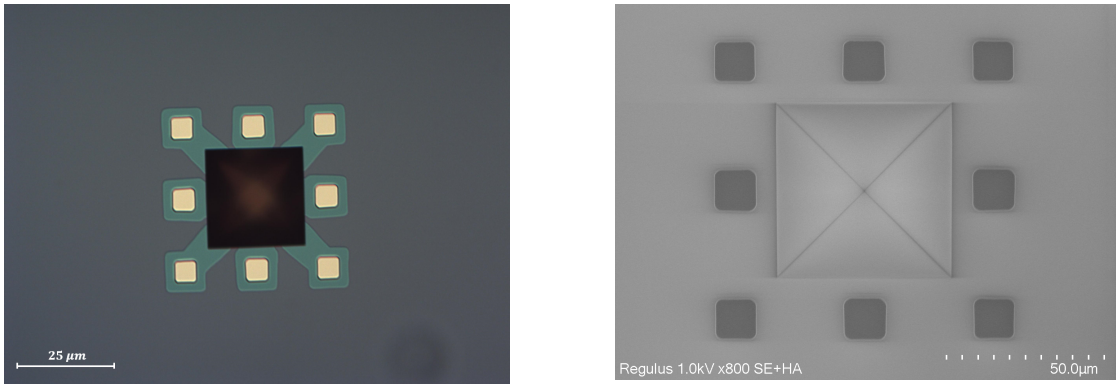

Figure 4.16: Optical and SEM images of a 50 μm PYRAMID after wet etching.

4.2.8 Metal interconnections

After that, the native oxide was removed from the contact openings by means of a 4 minutes dip etch in HF 0.55%. This step was necessary to ensure good contact between the metal layer and the bare silicon surface.
The samples were then sputtered with aluminium mixed with 1% of silicon. Silicon, in fact, is soluble in aluminium. When pure aluminium is deposited, silicon tends to dissolve inside the aluminium leaving voids behind that are filled by the metal. This is a problem because aluminium could contact the n-layer directly, "spiking" into the N+ doped layer and giving rise to bad ohmic contacts. This issue is solved by using aluminium which is already saturated with silicon.
The metal layer is then spray coated with negative photoresist. Negative photoresist was in this case employed because, as mentioned before, the metal interconnections lay completely on a planar area. The use of negative resist allows the stepper to expose features that are on the same focal plane. At the same time, the sloped walls of the cavities are not exposed at all avoiding useless and unpredictable reflections of the UV light.
In this case, the samples were spray coated with 2 sets of 4 layers. Soft baking steps of 1 min and 5 min at 100 °C were taken after each set.
The samples were then exposed, baked at 110 °C for 90 s and developed with MF-322. The post-exposure bake is necessary because the negative resist used (AZ-Nlof-2070) is a chemically amplified resist that requires a thermal treatment to start the cross-linking reaction.
The patterned aluminium layer was then wet etched with PES, a mixture of phosphoric acid, nitric acid, acetic acid and water. Wet etching was preferred to dry etching to avoid any physical bombardment, but also to ensure that the aluminium is completely removed from the bottom of the cavities. Again, the main

disadvantage stands in the isotropic etching mechanism, which decreases the lateral dimension of the metal lines.
After the metal etching, a 30 sec poly-silicon dip etch was made. PES, in fact, etches the aluminium but not the silicon dissolved. The latter deposits under the form of polysilicon grains, that must be removed by wet etching in a solution of HF and HNO_3. The resist was then stripped in acetone and the samples were alloyed in a furnace at 400 °C in a reducing atmosphere (N_2 and H_2), to decrease the contact resistance.

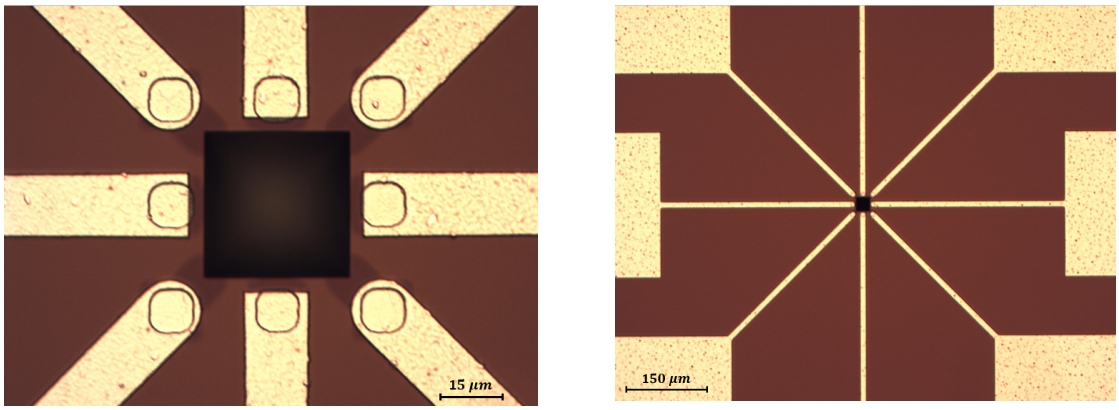

Figure 4.17: Optical image of a 25 μm PYRAMID device.

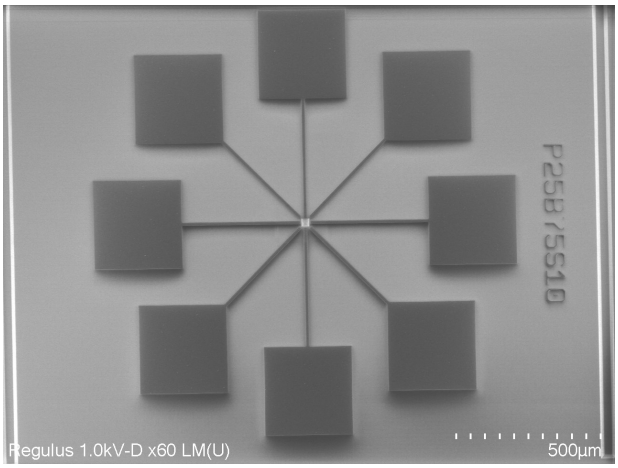

Figure 4.18: Low magnification SEM image of a 25 μm PYRAMID device.

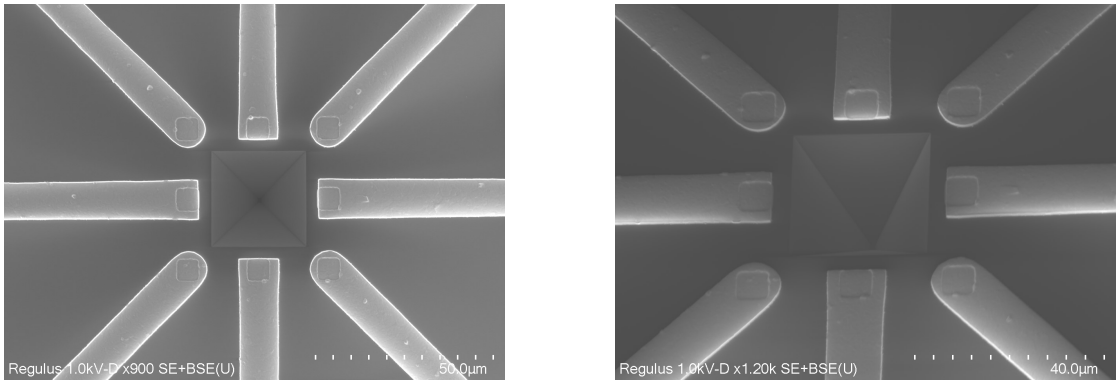

Figure 4.19: SEM images of a 25 μm PYRAMID device.

4.3 Conclusion

To sum up the results obtained, the 25 μm and 50 μm wafers were successfully fabricated. 47 out of 48 dies were correctly patterned for the 25 μm wafers, while 45 out of 48 dies were correctly patterned for the 50 μm wafers.
Further optimization of the spray-coating recipe might be required to obtain a more uniform layer, further improving the yield. Additionally, some fine tuning of the second lithographic step might be required to reduce the critical distance between close features.
The 100 μm wafers were dropped due to the extra optimization required to obtain a correctly patterned N+ layer. Eventually, these wafers will be completed in future work.
More refined techniques, such as multi-focal exposure [32], might be adopted to ensure a correct patterning of the whole cavity.

Chapter 5

Characterization of PYRAMID

This last chapter covers the characterization of the highly doped 25 μm PYRAMID devices. First of all, the back-end of line processing of the 3D Hall sensors is presented. Then, the experimental setup is displayed. Successively, the main results obtained are carefully analyzed and discussed. Lastly, the main results are summarised in a short conclusion.

5.1 Back-end of line

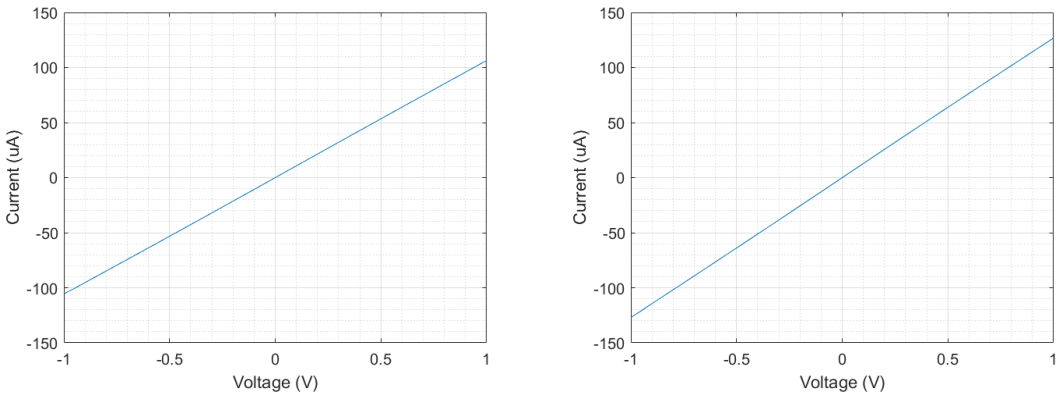

Figure 5.1: IV curves of a 25 μm PYRAMID with net doping $5 \cdot 10^{16}$ cm^{-3}, taken on the diagonal (left) and on the full side (right) of the device. The resistances are respectively 9.4 $k\Omega$ and 7.9 $k\Omega$.

After the alloying step, the 25 μm wafers were characterized on a probe station. The wafer scale testing showed that good ohmic contacts and no short circuits were successfully generated. Figure 5.1 displays the IV curves for a 25 μm device, with theoretical net doping $5 \cdot 10^{16}$ cm^{-3}.
After that, the 25 μm wafer with net doping $5 \cdot 10^{16}$ was covered with 4 μm thick photoresist and diced. The single dies were then cleaned with acetone, isopropanol and water.
No other wafers were diced and subject to back-end of line processes due to lack of time. Therefore, the characterization was performed only for one device size with one doping. The single dies were then glued to a PCB and wire bonded.

Each PCB presents 16 pads, which means that a maximum of two PYRAMID devices can be wired and tested per die. Despite that, we decided to bond only one PYRAMID per PCB to prevent too much wire crowding.
In conclusion, the wired and tested devices were two: the (1,1) and (2,2) elements in the PYRAMID matrix. Each of them was glued and wire bonded on a different PCB. For the sake of simplicity, from now on the (1,1) element will be called Device 1 while the (2,2) element will be called Device 2, as shown in Figure 5.2.

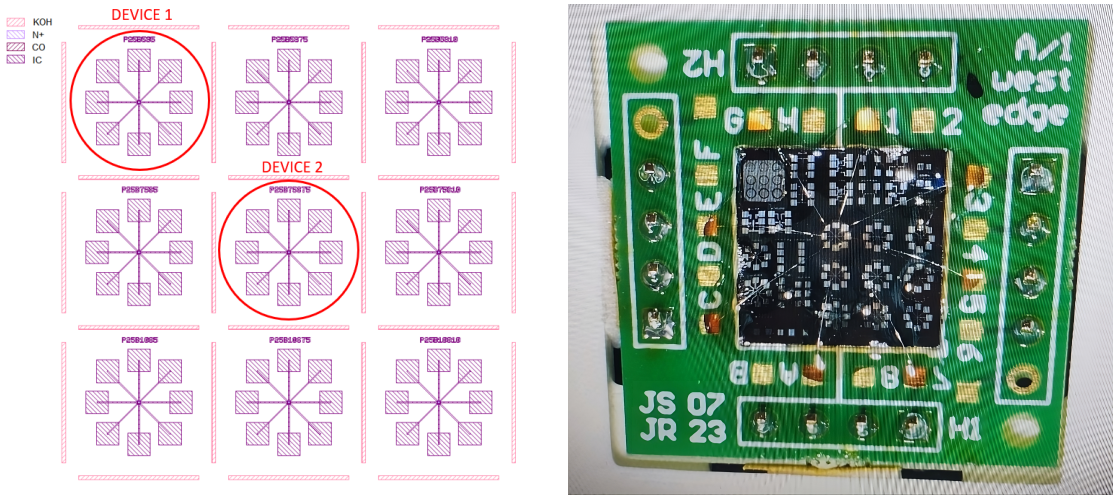

Figure 5.2: On the left, the devices wire-bonded are shown on the mask design. On the right, a photograph of Device 1.

5.2 Experimental setup

The experimental setup is displayed in Figure 5.3. The magnetic field is generated by means of an electromagnetic coil: a current is pushed into the coil and a constant

magnetic field, orthogonal to the spires of the coil, is generated. The current is provided by a TENMA programmable DC power supply. This instrument can reach a voltage of up to 12 V, which corresponds to a maximum magnetic field of about 2 mT. The response of the coil to a variation in the input current/voltage was characterized prior to the experiments, and it showed a linear response. Converting the input voltage/current to the equivalent magnetic field generated is therefore straightforward.
To perform a measurement, the sample is locked in a sample holder placed exactly in the middle of the coil. The sample can be either placed perpendicular or parallel to the magnetic field. The magnetic field was measured at different points in the coil and it proved to be quite homogeneous in the proximity of the sample holder. Additionally, the PCB is covered by a black container to avoid direct illumination of the device. The devices, in fact, proved to be quite light-sensitive. The biasing voltage/current is provided by a Keithley 2400 sourcemeter, and the Hall voltage is measured by an Agilent 34401A multimeter.

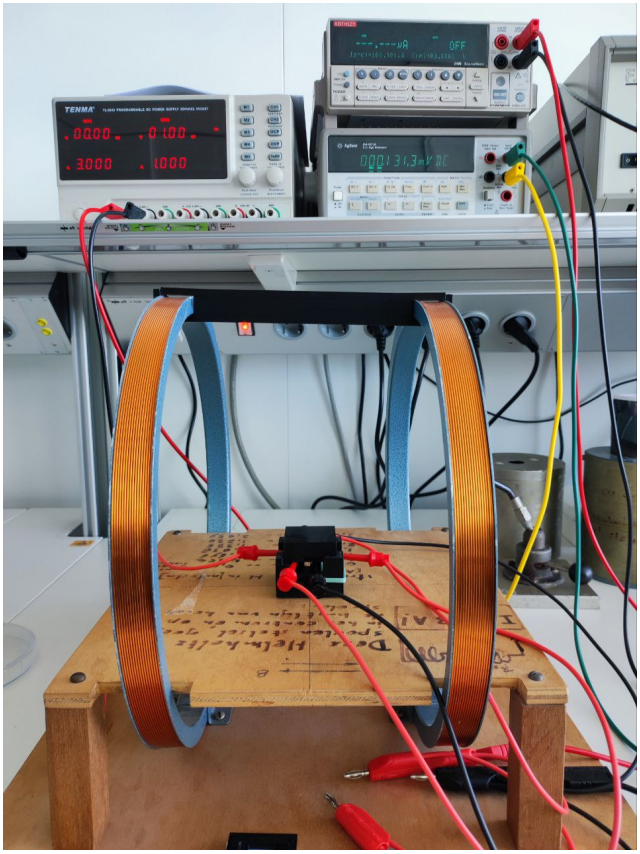

Figure 5.3: The experimental setup.

5.3 Characterization results

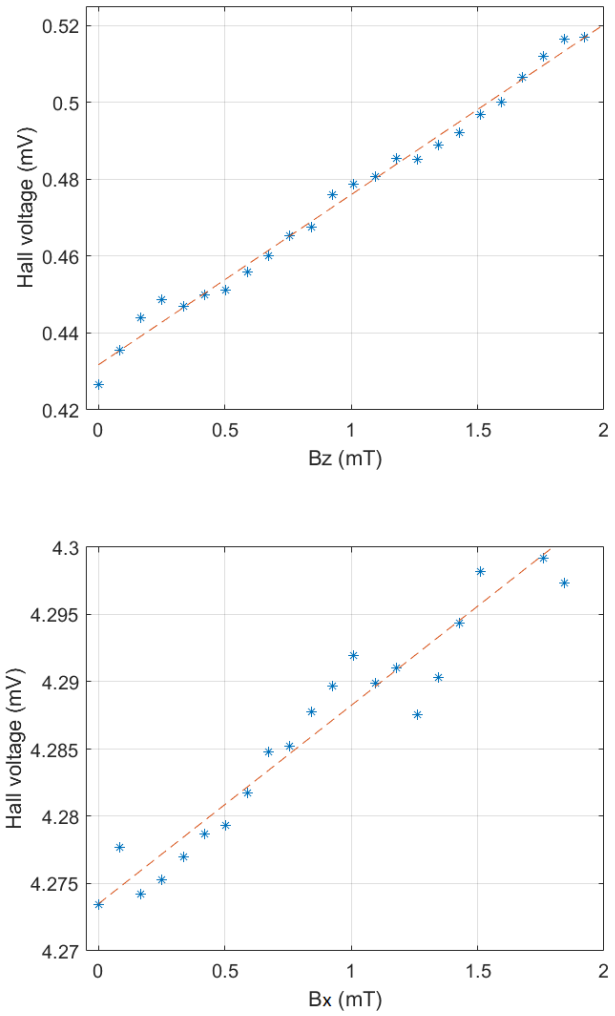

Figure 5.4: The "Hall voltage vs magnetic field" curves of the B_{z1} (up) and B_{plane} (down) modes of Device 2. The red curves represent the linear regression performed on the experimental data.

For all these measurements the devices were biased in current. The two samples were subject to a constant bias current of 200 μA, distributed in one or two ports based on the number of input terminals. This means that all the modes with more than two biasing contacts had a 100 μA current flowing between each couple of electrodes.

This causes an ambiguity in the definition of current-based sensitivity. In fact, the absolute sensitivity could be normalized either by the total current provided, or the "real" current that flows between each couple of contacts. In this case, the normalization operation was performed adopting the total current convention. As a consequence, the current-related sensitivity for the B_{z1} mode appears to be around two times the sensitivity of the other modes. However, this is not related to any physical reason but rather to the convention adopted (which is different from the one used in the simulations). The magnetic field was swept in 25 points, and 7 measurements of the Hall voltage were taken per magnetic field step. All 4 modes, illustrated in chapter 3, were tested. In particular, both sensitivity and cross sensitivity measurements were taken. Some of the "V_{Hall} vs B" curves can be observed in Figure 5.4. Additionally, Figure 5.5 shows a table with all the sensitivities, cross-sensitivities and offsets extracted from linear regression.

Sample 1

Field	Sensitivity ($\frac{V}{AT}$)			
	X	Z1	Z2	Z3
X	**120.46**	26.19	24.27	56.62
Y	31.26			
Z	22.44	**197.46**	**106.67**	**102.43**
offset in mV	0.10	8.00	10.24	6.41

Sample 2

Field	Sensitivity ($\frac{V}{AT}$)			
	X	Z1	Z2	Z3
X	**73.72**	14.43	32.27	17.67
Y	0.86		0.84	37.48
Z	10.42	**221.33**	**89.50**	**103.54**
offset in mV	4.28	0.57	2.26	3.64

Figure 5.5: The current-related sensitivities and offset of each mode, taken for every component of the magnetic field. Please note that these values are taken in absolute value.

As explained in chapter 2, the causes of the offset are likely related to asymmetries generated during fabrication. Additionally, some more intrinsic reasons might play a role, such as the "JFET effect". As already explained in chapter 2, when a bias voltage/current is applied the part of the n-layer subject to high voltage depletes more than the part closer to the ground terminal. This creates a further asymmetry

that becomes a source of additional offset. Other effects, such as packaging stress and heating distributions may also affect the overall zero-field response. A good current spinning strategy might be able to reduce the offset component due to the asymmetries, but not the one due to the JFET effect.

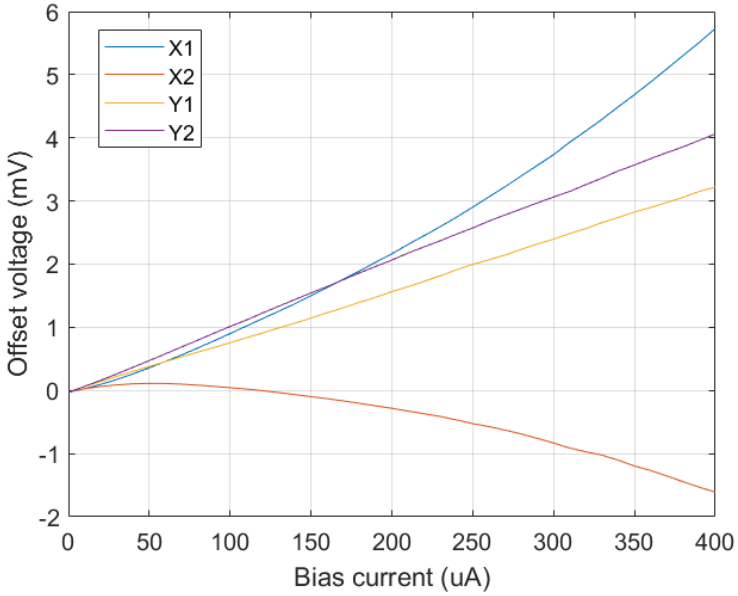

Figure 5.6: Offset in function of the biasing current for different phases (B_{plane} mode). The quadratic behaviour of the X1 and X2 curves is still under discussion, but it is arguably related to the "JFET effect". [27][18]

Current (μA)	Sensitivity ($\frac{V}{AT}$)
50	-10.97
100	5.97
150	15.39
200	-20.85
250	-8.49
300	26.60

Table 5.1: "Cross-sensitivities" extracted measuring the y- component of the magnetic field with the B_{z3} mode, for different bias currents.

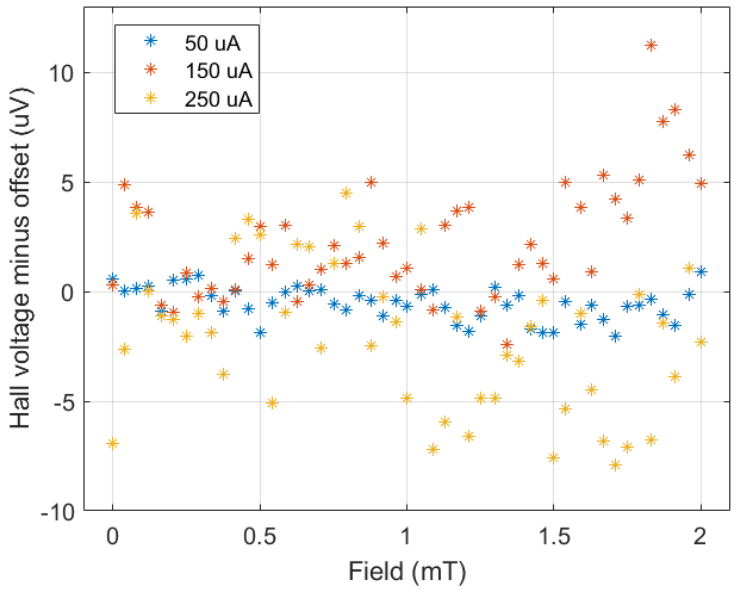

Figure 5.7: The Hall voltage measurements during the cross-sensitivity tests. Only 3 sets out of 6 have been reported.

Additionally, the measurements proved to be very noisy. The linearity of the output response, in fact, is strongly affected by the very strong noise. Again, the noise is dependent on the mode and the bias.
Thanks to further measurements, we managed to discover that the noise level is so high that it completely covers the output signal of the cross-sensitivity measurements. Table 5.1 shows how the linear regression of a cross-sensitivity measurement changes value and sign as we repeat the measurement with different bias currents. The only explanation for this behaviour is that the cross-sensitivity of this mode is completely masked by the noise.
Therefore, the cross-sensitivity values reported in Figure 5.5 cannot be trusted.

The reasons behind the very high noise level are yet to be discovered. The predominant component is believed to be flicker noise, but other sources of noise such as generation-recombination cannot be excluded. A noise spectral density analysis should be performed to better understand the origins and dynamics of this disturbance.

5.4 Conclusion

The characterization of the high-doping 25 μm wafers proved that each mode is indeed sensitive to the component of the magnetic field that they are supposed to detect. The sensitivities discovered were quite high, between 74 $\frac{V}{AT}$ and 220 $\frac{V}{AT}$. However, the devices were found to be more noisy than expected and presented a very high offset.
Solutions to these problems are yet to be found. A good current spinning strategy might be able to lower the offset level. Regarding the noise, an analysis of its origins is essential to discover a method to reduce it. Therefore, a noise spectral density analysis might be required to get a better insight into the causes of this undesired effect.

Chapter 6

Conclusion and future work

6.1 Results of this thesis

The main results of this thesis can be summarized as follows:

- The PYRAMID device was presented, and a theoretical model for both current-related and voltage-related sensitivities was extracted. This model can be seen as a starting point toward the comprehension and optimization of this novel Hall device. Additionally, it showed how both the z- and planar modes sensitivities do not degrade reducing the junction depth of the n-layer. Therefore, this simple analysis confirmed that PYRAMID can be made CMOS compatible.
- Simulation with both COMSOL and SENTAURUS confirmed and complemented the theoretical model. In particular, the simulations showed the effect that the finite contact sizes have on the sensitivities of the device.
- Different working modes were discovered and analyzed. One mode detects in-plane magnetic fields, three modes detect out-of-plane magnetic fields and the last mode detects all the components of the magnetic field at the same time.
- The PYRAMID device was successfully fabricated for two sizes and two different dopings. The lithographic masks were designed and the process flow was carefully conceived. Additionally, the spray coating and exposure steps were optimized to properly pattern the specific topography of the PYRAMID devices.
- The samples were lastly characterized. Despite having some problems of offset and noise, each mode worked correctly and presented good current referred sensitivities.

6.2 Outlook on future works

This thesis managed to successfully show the concept of PYRAMID. However, more work is necessary to exploit the full potentiality of this promising device and eventually obtain a commercially competitive product. To be specific:

- More simulations and better models might be required. In particular, a simulation adopting the geometrical and doping parameters of the fabricated PYRAMID devices should be performed. In this way, the models can be compared and validated with the characterization results.
  What is more, some additional simulations should be performed to better comprehend the quantitative correlation between design asymmetries and offset.

- A current spinning strategy should be defined for each mode, if possible. Current spinning is by far the most effective method that can be used to reduce the offset.

- Some alternative n-doping techniques might be considered, such as diffusion and epitaxial deposition. One of the causes of the very high offset, in fact, might be doping inhomogeneity due to implantation. To verify this some simulations and spectroscopic analysis should be performed.

- Some other coating and patterning techniques could be considered instead of spray coating. Spray coating, in fact, is not broadly spread in industry and might be a problem from a CMOS integration perspective.

- If other techniques cannot be adopted, spray coating should at least be optimized to have a more uniform layer on the whole wafer. In this way, the wafer can be better exposed and a higher yield can be achieved.

- A technique to correctly pattern deeper cavities should be elaborated to successfully fabricate 100 μm and larger PYRAMIDs.

- The sources of noise should be identified and removed/reduced. A spectral density analysis might be the best method to diagnose the causes of this disturbance.

- The characterization of the other 25 μm devices, as well as the 50 and planar μm ones, must be performed. A comparison between different devices with different sizes and doping is indeed extremely interesting. Additionally, it could give a better insight into the probable causes of offset and noise.

- Lastly, the PYRAMID structure might be integrated with novel materials to achieve harsh environment operation or to get maximum performance. Some examples are graphene, diamond and gallium nitride.

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