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Auto calibration of RF reconfigurable circuits in FD-SOI CMOS

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Auto calibration of RF reconfigurable circuits in FD-SOI CMOS

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Keywords

Multiphase Reception Radio Frequency (MR-RF) circuits; N-path Mixer (NPM); N-path Filter (NPF); Harmonic Rejection N-path Mixer (HR-NPM); Reconfigurability; Calibration; Receiver; low noise amplifier (LNA); Harmonics rejection; Stray signal attenuation.

Abstract

In an era marked by the proliferation of connected devices, the imperative to minimize ecological impact has become paramount. Novel solutions are required to make circuits reconfigurable while also prioritizing energy efficiency. This work delves into one such solution: the design of circuits capable of self reconfiguration based on contextual cues. The study centers on Multiphase Reception Radio Frequency (MR-RF) circuits, specifically investigating their integration with embedded test strategies. Central to this work is the N-path mixer, a cornerstone in modern multiphase receivers. Harnessing the N-path mixer's unique attributes, this study explores its versatility and configurable potential, positioning it not only as an independent testing entity but also a calibration tool. The study introduces an innovative approach that utilizes the N-path mixer both as a conventional mixer and an oscillator for calibration, streamlining testing processes and resource utilization in RF circuit evaluation. Through meticulous examination, this work unveils the reconfigurability of the harmonic rejection N-path mixer, demonstrating its adaptability within RF receivers. The study's findings underscore the versatility of the circuit and the criticality of maintaining signal quality while minimizing mismatches for optimal performance.

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Acronyms

FSK frequency-shift keying.

HR-NPM harmonic rejection N-path mixer.

IoE Internet of Everything.

IoT Internet of Things.

LNA low noise amplifier.

LO Local Oscillator.

MR-RF Multiphase reception radio frequency.

NF noise figure.

NPM N-path Mixer.

PSK phase-shift keying.

QAM quadrature amplitude modulation.

RF radio frequency.

SNR signal-to-noise ratio.

1 Introduction

With the increasing number of connected objects on the planet, it is crucial to minimize their ecological footprint. For this, new solution must be found to make circuits reconfigurable (one circuit for multiple application) and energy efficient. In this work, one of this solution will be explored which consist in designing circuits able to reconfigure itself according to the context.
Multiphase reception radio frequency (MR-RF) circuits in *Figure 1* and embedded test strategies will serve as an object of study for this work, with the objective of ensuring the reduction of stray signals while minimizing the circuit consumption.

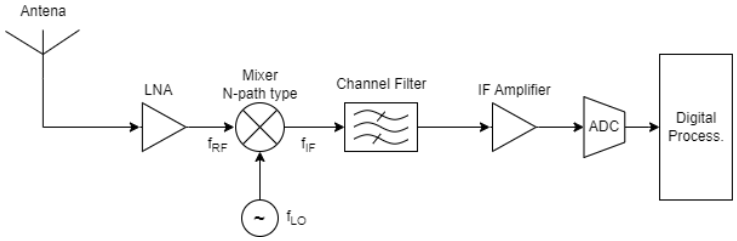


Figure 1: RF LNA-first receiver block diagram

The architecture reported in *Figure 1* is the typical one of an LNA-First receiver. Since the first stage of the receiver controls its performance and noise as demonstrated by the Friis formula in [19], this configuration is the most suited to minimize the overall noise figure of the receiver. Moreover, this architecture enhances the receiver's sensitivity allowing better reception of low signals.
Alternatively, the use of the LNA in the previous schematic could be avoided resulting in a Mixer-First receiver architecture which allows saving energy while improving the image rejection and selectivity.

Whatever the used architecture is, the design of circuits in microelectronic technologies is characterized by the need to address the concept of variability. Components available in integrated technologies suffer from tolerances, especially when comparing devices on different wafers. These variations in component parameters inevitably lead to variations in circuit performance.
While performance variability has historically been managed by incorporating design margins, that is, by over designing, this approach is no longer acceptable due to resulting wastage of energy and silicon area, leading to reduced product competitiveness.
The conventional approach to deal with the issue of variability involves providing adjustment mechanisms for circuits (such as bias current of a transistor) to position each circuit precisely at the specified level.

In the realm of radio frequency (RF) and wireless communications, the design and implementation of high-performance receivers are essential for reliable signal reception and processing. A key component employed in the architecture of modern multiphase receivers is the N-path mixer. This advanced mixer configuration offers numerous benefits, including improved performance, enhanced linearity, and exceptional versatility.

N-path mixers stand out from conventional mixers due to their utilization of multiple parallel signal paths operating simultaneously. The 'N' in N-path represents the number of signal paths employed in the mixer design, which can vary depending on specific application requirements. These mixers are typically implemented using a combination of active devices such as transistors and passive components like capacitors and inductors.

In this study, the N-path mixer will be employed as a test vehicle to comprehensively investigate its versatility and configurable capabilities. By harnessing the unique attributes of the N-path mixer, we aim to showcase its potential as not only an independent testing entity but also as a valuable tool for calibration purposes. Specifically, we aim to exploit the built-in characteristics of the N-path mixer to perform dual roles; serving as both a conventional N-path mixer and an oscillator that can be employed as calibration reference for the mixer. This innovative approach presents an interesting advantage of making the testing and calibration process more efficient, resulting in a reduction in the number of required devices. Through this dual-functionality of the N-path mixer, we aspire to establish a novel methodology that enhances the efficiency and effectiveness of testing and calibration procedures in RF circuit evaluation.

This master's thesis begins by providing a concise outline of the goals and timetable in Chapter 2. It is then followed by an elucidation in Chapter 3 regarding the collaborating entities, namely ST Microelectronics and the TIMA laboratory, which have played a pivotal role in facilitating the successful completion of this work. Chapter 4 delves into the current state of the art concerning the subject under investigation, while Chapter 5 elaborates on the fundamental principles of the studied circuit and elucidates the rationale behind its consideration. The culmination of this master's thesis are Chapters 6 and 7 which delve into the exploration of the two operational modes in which the circuit can operate. This master's thesis concludes in Chapter 8, where the findings are summarized, and the potential future directions of this research are outlined.

2 Objective and Schedule

The primary objective of this project centers around a thorough investigation into the reconfigurability of RF circuits, coupled with the exploration of potential calibration methods to optimize their performance.

The focal point of analysis in this study is the radio frequency receiver, with particular emphasis on the behavior of its mixer circuit component. This study delves into the reconfigurability of the mentioned circuit, examining its functionalities both in the generation mode, that is, reconfigured as an oscillator and the conventional mixing mode, as illustrated in the Gantt diagram depicted in *Figure 2*. This comprehensive approach enables an exploration of the circuit's operational dynamics under various conditions.

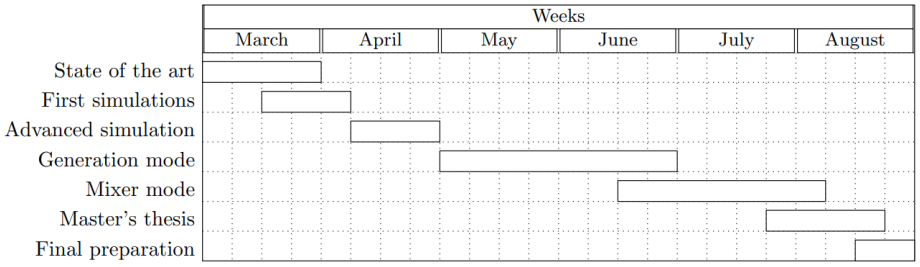


Figure 2: Internship schedule

To achieve the intended goal, a combination of specialized circuit simulation software like Cadence and computational tools like Matlab were employed. The utilization of these software platforms allowed for a comprehensive and multi-faceted approach to the project's objectives. Throughout the 6-month duration of this project, conducted as part of the internship, regular weekly meetings were held to discuss progress, and comprehensive reports and presentations were prepared and presented.

The key tasks to be achieved during this time frame encompass a comprehensive and methodical exploration of the existing literature, aimed at grasping pivotal milestones and emerging innovations within the field. Furthermore, mastering the simulation software allows for in-depth exploration and analysis of complex systems. This proficiency will facilitate a thorough understanding of the intricacies involved. Lastly, the design of advanced systems was a crucial aspect that received dedicated attention throughout the designated period.

3 Company and laboratory presentation

This master's thesis was undertaken within the context of an internship program co-supervised by STMicroelectronics and TIMA laboratory.

3.1 TIMA laboratory

TIMA is a collaborative research laboratory, jointly established by CNRS, Grenoble-INP, and UGA (Shared Research Unit #5159). It boasts an international team, comprised of members and interns hailing from various corners of the globe. A substantial portion of TIMA's research endeavors are conducted within the framework of cooperative ventures alongside industrial and academic partners. These initiatives receive support from regional, national, and European funding sources.

The focal points of TIMA's research encompass a wide array of aspects including the specification, design, verification, testing, CAD tools, and design methodologies for integrated systems. Encompassing both analog and digital components at one end of the spectrum, and multiprocessor Systems-on-Chip alongside their fundamental operating systems at the other, TIMA's research terrain is diverse and comprehensive.
The key research topics of the laboratory are:

- Robustness, reliability and test
- Hardware/Software co-design
- Simulation and verification
- Low power design
- Hardware security and embedded trust
- Asynchronous design
- New sampling and data processing techniques
- MEMS, Smart Sensors and Actuators
- Design of AMS/RF/mmW devices, circuits and systems
- Modeling, control and calibration of AMS/RF devices, circuits and systems
- New hardware computing and digital design

3.2 STMicroelectronics

STMicroelectronics, founded in 1987 as a collaborative effort between SGS Microelettronica and Thomson Semiconducteurs, has rapidly evolved into a global leader in semiconductor technology. Its rich history, unwavering commitment to innovation, and far-reaching impact make it a prominent player in the industry. The company's origins trace back to the fusion of Italian and French semiconductor giants, an alliance that set the stage for groundbreaking achievements. Over the years, STMicroelectronics has expanded its presence and influence, consistently pushing the boundaries of technological possibilities.

With innovation at its core, STMicroelectronics consistently strives to redefine what's achievable. This driving force has propelled the company to the forefront of semiconductor advancements, shaping everything from consumer electronics to industrial solutions.

Boasting a vast international presence, STMicroelectronics operates across a global network of offices, research centers, and manufacturing facilities. Its 14 primary manufacturing sites attest to its commitment to delivering top-quality solutions. The company's expansive footprint spans 80 offices in 35 countries, enabling it to serve over 200,000 customers worldwide.
STMicroelectronics' reach extends beyond technological prowess. Its semiconductor solutions power billions of electronic devices, revolutionizing the way people interact with technology. From smartphones to smart appliances and automotive innovations, its contributions touch countless aspects of modern life.

The company's vision is encapsulated in "life.augmented," a commitment to enhancing human experiences through technology. This philosophy is a driving force behind its constant pursuit of innovation and its dedication to enabling individuals to fully embrace the potential of technology.

Beyond technology, STMicroelectronics is a champion of sustainability and ethical business practices. As a signatory of the United Nations Global Compact (UNGC) and a member of the Responsible Business Alliance (RBA), the company is committed to minimizing its environmental impact and upholding ethical standards.

The partnership between STMicroelectronics and the TIMA laboratory for this master's thesis underscores the company's interest in fostering a symbiotic relationship between academia and industry. The shared knowledge and expertise have paved the way for innovative solutions and cutting-edge research.

4 State of the art

In the realm of signal reception the mixer assumes a fundamental role for frequency translation and signal processing, making it a key component that determine the receiver's overall performance. Consequently, an in-depth analysis of the mixer's capabilities lays the foundation for designing RF receivers that meet the evolving demands of wireless communication systems. N-path Mixer are an emerging field of study due to their versatility and reconfigurability. These mixers, characterized by multiple parallel signal paths, offer a range of advantages over traditional mixers. In this state-of-the-art overview, we will explore the current advancements and key research findings related to N-Path mixers, highlighting the advancement in linearity improvement, noise performance optimisation, versatility and their potential applications. Despite the remarkable progress made, there remain bottlenecks and challenges that need to be addressed to further advance N-Path mixer design and practical implementation.

4.1 N-Path Mixer Architecture

Figure 3 shows the conceptual schematic of a basic N-path mixer. In 2006, Abidi's work introduced an 800 MHz/6 GHz software-defined wireless receiver [1], demonstrating the potential of using mixers with N-path in wide band applications. The article discusses the selection, characteristics, and optimization of mixers, with a focus on achieving low noise and distortion while maintaining harmonic rejection and addressing challenges related to second-order non linearity. The mixer's role in the receiver's performance and the importance of specific topologies and design considerations are key themes in the discussion. N-Path mixers employ a distinctive architecture (*Figure 3*) consisting of multiple parallel signal paths which characteristics allows for receiver's performance improvements.

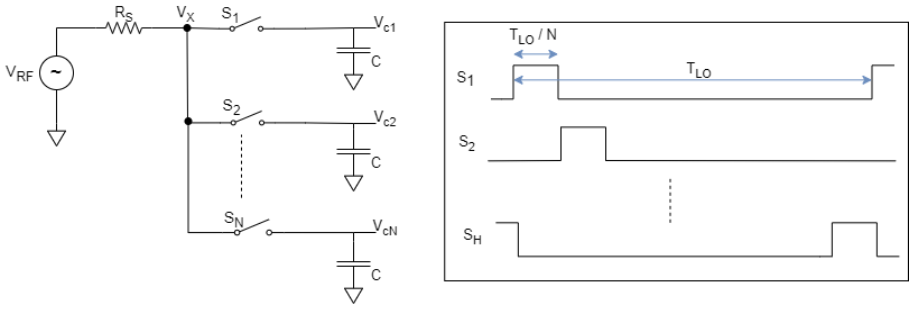


Figure 3: N-path Mixer

As demonstrated in Appendix A, this structure allows to avoid additional filtering due to its inherent filtering at node V_X, however considering the mixer output, it is affected by all the harmonics. To consider an even harmonics rejection structure, a differential configuration could be implemented as in *Figure 4*. In this configuration, the charging of the capacitors is faster and it could be observed that doubling the input frequency the output will be null. Therefore, if a perfectly symmetrical structure is considered, the even harmonics will be rejected.

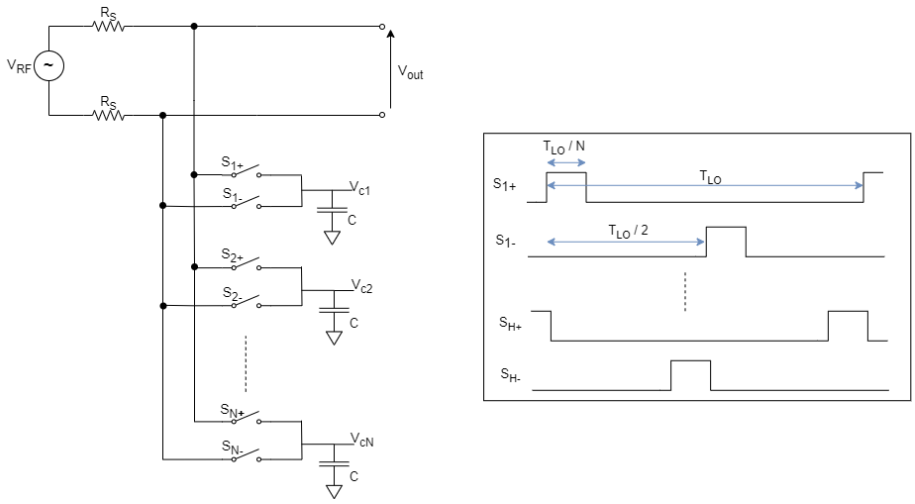


Figure 4: Differential N-path Mixer

Ongoing research aims to enhance the N-path mixer architecture, with the objective of achieving more effective rejection of harmonics. Advanced architecture such as the harmonic rejection N-path mixer (HR-NPM), that will be introduced in the next chapter, has been developed to reject up to the N-1 (N being the number of paths) harmonic.
The following subsections explore different solutions that have been proposed in the literature for the implementation of high performance mixers.

4.2 Linearity Enhancement Techniques

The importance of N-path mixers lies in their ability to face several challenges encountered in traditional mixer designs. One of their primary advantages is their improved linearity performance. Linearity refers to the ability of a mixer to accurately preserve the original information contained in the input signals

while performing frequency translation. N-path mixers achieve high linearity by employing cancellation techniques that effectively suppress undesired harmonics and intermodulation products.

Achieving high linearity in N-Path mixers has been a subject of intensive study. In 2011, Nauta explored techniques to improve the selectivity of N-path structure introducing a high-Q 4-Path band-pass filter [2]. The proposed architecture have a differential configuration which allows clock-leakage reduction and suppress selectivity around even harmonics. The linearity in this structure is highly increased using high-quality switches.
Moreover, Nauta's research focused on enhancing linearity and reducing noise in mixer-first receivers. In his studies he firstly proposed an innovative solution based on complex pole pairs with capacitive positive feedback [3] which allows increasing linearity as well as decreasing the noise figure. Subsequently, the author proposed a linearity improvement technique [4] by using a double N-path stage filtering with passive mixing.
More recently, Bourdel et al. proposed linearity improvements [5], [6] based on the study of HR-NPM's switch control signals and of the gains of the amplifiers stage.

4.3 Noise Performance Optimization

Achieving reliable signal reception in RF receivers significantly relies on the optimization of noise performance. By utilizing parallel signal paths, N-path mixers exploit noise-shaping techniques to suppress noise contributions from individual paths, enhancing then the overall signal-to-noise ratio (SNR). This results in increased sensitivity and improved reception of weak signals.
Researchers have been focused on improving noise performance in N-Path mixers. The study done in [7] delves into the impact of baseband trans-impedance amplifiers on linearity and noise figure in N-path mixer-first receivers. This article highlight the trade-off between linearity and noise in N-path mixers, providing some perspective for design optimization. In a related work [8], the analysis extends to passive mixer-first receivers which imply N-path structures. The study shows the impact of higher harmonics on impedance and noise figure highlighting that with appropriate baseband design, the limit on noise figure is set by this shunting or re-radiation effect.
Afterwards, Weinreich and Murmann in 2023 [9] introduced a fully-integrated N-path harmonic-rejection transformer-mixer which allows achieving high linearity and very low noise figure (NF) in the range of (3.4 - 4.8)dB.
These pioneering studies contribute to minimizing noise contributions and enhancing the overall receiver sensitivity, making N-Path mixers interesting candidates for robust and reliable RF receivers.

4.4 Versatility and Modulation Flexibility

The versatility of N-Path mixers is a key feature that makes them suitable for a wide range of applications. Their flexible architecture allows for the implementation of various modulation schemes, making them suitable for a wide range of applications. Whether it involves frequency-shift keying (FSK), phase-shift keying (PSK), quadrature amplitude modulation (QAM), or other complex modulation formats, N-path mixers can elaborate different types of signal and provide efficient frequency conversion. Moreover, the versatility of N-path mixers extends to their compatibility with emerging wireless communication standards and technologies. As new standards such as 5G and beyond continue to evolve, as discussed in [10] N-path mixers offer the necessary adaptability to meet the increasing demands for higher data rates, wider bandwidths, and improved spectral efficiency.
Molnar et al.'s research in 2015 showcased optimized designs for N-Path mixer-first receivers operating in wideband operation [11]. Their work emphasized the mixers' ability to handle diverse modulation schemes, ranging from narrowband to wideband, and the potential for achieving high linearity and selectivity across these schemes.
Furthermore, it could be notice that the harmonic cancellation principle exploited in [12], [13] and [14] to design a signal generator is similar to the working principle of a harmonic rejection N-path mixer. One of the idea behind this work is to exploit the versatility of N-path mixers to envision a reconfiguration possibility for implementing a signal generator.

4.5 Emerging Applications

N-Path mixers have the potential to revolutionize emerging wireless communication technologies. Some example of emerging application are:

- Millimeter-Wave and mmWave-Radar: N-Path mixers, with their superior performance at high frequencies, are well-suited for mmWave-radar receivers [15]. Their ability to handle wide bandwidths and support different modulation improve the capabilities of these radar systems.
- Internet of Things (IoT): The increasing number of IoT devices requires also compact and low-power components. N-Path mixers, with their low power consumption [16], [17] and their adaptability to different standard communication, are ideal for IoT devices. Furthermore, as discussed in [9], N-path mixer are well suited also for Internet of Everything (IoE) applications.

- 5G applications: As 5G networks continue to expand, N-Path mixers are expected to play an important role in supporting high data rates and diverse modulation schemes in advanced communication networks. The N-path mixers potentiality in this field was discussed in [10] analyzing the balance of wide input range tunability, noise, gain, and linearity performance.
- Biomedical and Healthcare Devices: Hum noise, such as the interference caused by power line noise, stands as a significant challenge in the realm of biomedical signal processing. Studies [18] have demonstrated the capability of N-path structure used as Notch filter to reject those unwanted signals.

4.6 Bottlenecks and challenges

N-Path mixers show promise in diverse communication applications, but they also encounter specific bottlenecks and challenges that researchers are actively working to solve. The main challenges are:

- Out-of-Band Interference Susceptibility: External signals or noise outside the desired frequency range can negatively impact the mixer's performance, leading to signal degradation and reduced overall receiver sensitivity. Designing efficient rejection techniques for these interference is important to improve the mixer's robustness.
- Linearity Limitations: Non-linearities in the mixer can lead to unwanted intermodulation products and harmonics, degrading the receiver's overall performance. As investigated previously, numerous advancements were made in this branch. However, developing techniques to enhance the linearity of N-Path mixers is still an area of active research.
- Power Consumption: While N-Path mixers generally offer advantages in terms of low power consumption compared to active mixers, power optimization remains a challenge, especially for battery-powered devices and energy-efficient systems. Moreover, it is important to reduce the power consumption without compromising the performance.
- Clock Leakage and Feedthrough: Proper isolation between the Local Oscillator (LO) and radio frequency (RF) paths is essential to prevent clock leakage and feed-through, which can result in unwanted mixing products and degrade performance.

- Mismatch and Calibration: The N-path architecture is sensitive to component mismatches, requiring careful calibration techniques to mitigate their effects and maintain consistent performance across different paths.

In conclusion, N-path mixers play a very important role in the design of multiphase receivers for RF and wireless communication systems. Their importance lies in their ability to have a high linearity, enhanced noise performance, and a very wide versatility. With their unique architecture and advantages, N-path mixers enable the realization of high-performance receivers capable of handling complex modulation schemes and adapting to the evolving communication standards.

5 HR-NPM

In this chapter we will investigate the HR N-path mixer principle and the need of having harmonics rejection to avoid signal degradation.

5.1 Frequency transposition issue

Frequency transposition, a fundamental function of mixers, involves translating a signal's frequency from one frequency band to another. This process is essential for a wide range of applications, including signal conversion in both receivers and transmitters. However, several significant challenges arise during frequency transposition, impacting the overall performance of the mixer and the quality of the transposed signal. When an input signal is mixed with a local oscillator (LO) signal in a nonlinear mixer, spurious signals can emerge at various frequencies other than the desired output. These spurious signals can lead to interference and degradation of signal quality. Moreover, intermodulation distortion occurs when the mixer's non-linearity generates additional frequencies that were not present in the original input signals, resulting in signal distortion and the creation of unwanted spectral components.

Furthermore, phase noise introduced by the LO signal can mix with the input

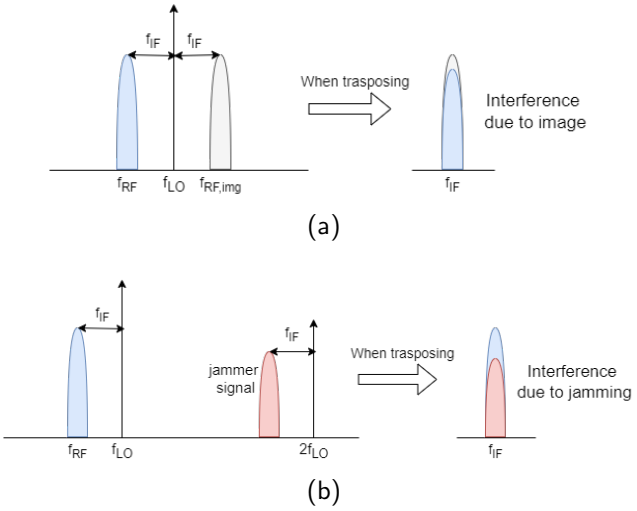


Figure 5: Transposition interference due to image (a) and jamming (b) signals

signal and produce undesirable sidebands, affecting the overall spectral purity of the output signal. Additionally, LO leakage refers to a portion of the LO signal leaking into the output signal, leading to spurious components and interfering with the intended transposition. Managing phase noise and LO leakage is

vital to achieving high-quality frequency translation. Moreover, mixer circuits are vulnerable to harmonic distortion, where harmonics of the input signal mix with LO harmonics to produce undesired output frequencies. In the presence of jamming signals (*Figure 5b*), these harmonic components could interact with the jamming frequencies, complicating the signal separation. Image frequencies are mirror frequencies on the other side of the LO frequency that can also appear in the output due to the mixer's nonlinear behavior as shown in *Figure 5a*. Managing harmonic and image rejection is crucial to ensuring accurate and clean frequency transposition.
While solutions like anti-imaging filters can alleviate image interference concerns, addressing issues associated with harmonics requires dedicated techniques for harmonic rejection.

5.2 HR-NPM principle

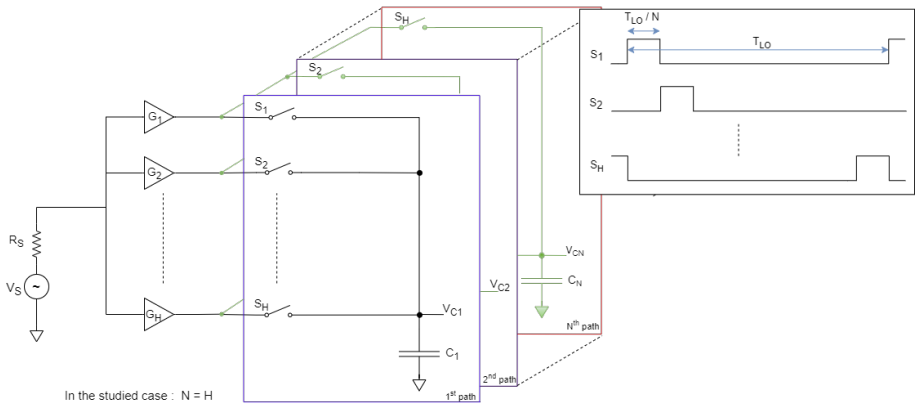


Figure 6: Harmonic rejection N-path mixer

Figure 6 represents the general structure of an harmonic rejection N-path mixer. From this representation, a general form of the effective LO that drives the switches for the HR-NPM architecture can be derived in its frequency domain enabling to evaluate the theoretical HR band. The representation of Figure 6 consists of N paths and H branches per path, where $H = N$ is the most common choice. Along each path, H switches, respectively driven by signal $S_i(t)$, sample the RF input signal through H gain stages G_h, represented by LNAs resulting in a LNA-first architecture. Their computation has been studied in the literature with several methodologies. In this work, we consider that the effective LO applied to the mixer ($eflo(t)$) is based on a sine wave sampled at a frequency $F_s = H \cdot F_{LO}$, which maximizes the number of zero coefficients, each coefficient corresponding to a dedicated gain during sampling. Hence, the value of the gain coefficients G_h have to be carefully controlled to reach the targeted harmonic rejection. The G_h are given by the following series defined

for $0 \leq h \leq H-1$:

$$G_{h+1} = \frac{sin\left(\frac{2\pi}{H}h\right)}{sin\left(\frac{2\pi}{H}\right)} \tag{1}$$

Moreover, the effective LO can be represented as:

$$eflo(t) = \sum_{h=-\infty}^{+\infty} G_h \cdot \delta(t - hT_s) * g(t) \tag{2}$$

Where $g(t)$ is the gate function of width $T_s = \frac{T_{LO}}{H}$. Doing the Fourier transform of the previous signal:

$$|E_{FLO}(f)| = \frac{A}{2} \cdot \text{sinc}\left(\pi \cdot T_s \cdot f\right) \sum_{n=0}^{+\infty} \delta\left(f - n \cdot F_s \pm F_{LO}\right) \tag{3}$$

Which is graphically represented by:

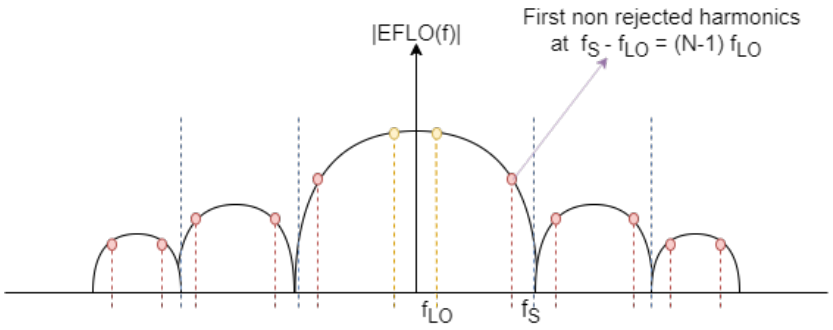


Figure 7: Effective LO frequency response

All the harmonics occur at frequencies of $f_{hi} = n \cdot f_s \pm f_{LO}$, which simultaneously represent the folded harmonics. This general description demonstrates that the harmonic rejection band of the HR-NPM is associated with H, the number of branches in the schematic shown in Figure 6, and with the number of samples of the sine wave. However, it is not dependent on N, the number of paths.
Considering an $H = N = 8$ structure, the gain values associated to each path are reported in the table below.

G_1	G_2	G_3	G_4	G_5	G_6	G_7	G_8
0	1	$\sqrt{2}$	1	0	-1	$-\sqrt{2}$	-1

Table 1: Theoretical gain values

Harmonic rejection depends on the interplay between these gain values rather than their specific nominal values. This means that multiplying these values by a constant factor won't affect the rejection quality and the aforementioned principle.

6 Generation mode

In this master's thesis, we studied for the first time the reconfiguration of an HR-NPM circuit as a sinusoidal signal generator. Within the framework of the generation mode configuration, the HR-NPM circuits showcase its remarkable degree of reconfigurability. Particularly, it could be noticed how the response of the HR-NPM varies based on the nature of the applied input. Notably, when a constant input is applied instead of an RF signal, from a theoretical point of view a sinusoidal-like behavior becomes evident in the output observed at each capacitor. By applying a steady input, it becomes then possible to synthesize an RF signal. The distinct advantage of this approach lies in the inherent properties of the HR-NPM, which facilitate notable reduction in harmonic components. As a result, this configuration demonstrates the HR-NPM's ability to efficiently react to different inputs type and to be adapted to different application.

The interest in this configuration mode comes from the generation of a signal with highly attenuated harmonics, which could be used as a test stimulus signal for another block. However, the high linearity of the generated signal is strongly dependent on the non ideality introduced by each component of the HR-NPM circuit which also paved the way to using the generator mode for calibrating the HR-NPM itself. As shown in the previous chapter, the rejection of even harmonics depends on the symmetry of the gain values while the the rejection of odd ones is related to the characteristic of the circuit. In this section, the influence of different HR-NPM circuit's parameters and the mismatches effect introduced by the components on the generated signal quality will be investigated.

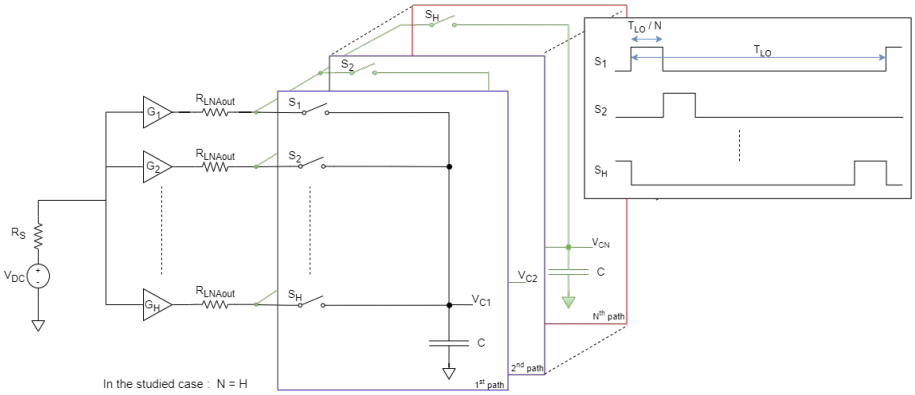


Figure 8: Harmonic rejection N-path generator: simulated schematic

All the results shown in this chapter were obtained through the use of Cadence schematic analysis tools using the configuration reported in *Figure 8*. The used amplifiers are ideal ones and to simulate the output impedance of ad LNA

a resistor R_{LNAout} was added in the schematic. Furthermore, the switches have an equivalent closed resistance ($R_{SW} = 1\Omega$) which could be generally neglected with respect to the output impedance of the LNA stage.

6.1 Impact of different capacitor and LNA's output impedance on the generated signal

Assuming that the employed LNAs have a structure that allows the amplification of DC voltages, the influence of different output resistances and different capacitor loads can be analyzed using the schematic in *Figure 8*. Whatever the respective gains are, the LNA's output impedance was assumed the same for all the amplifiers considering typical values in the range of hundreds of Ohm. Furthermore, a range between $2f$ F and $200p$ F was considered for this analysis.

The voltage across the capacitor at any instant of time during the charging period can be expressed as:

$$V_C = V_0 \left(1 - e^{-t/\tau}\right) + V_{C0} \cdot e^{-t/\tau} \tag{4}$$

Where V_0 is the applied voltage, V_{C0} the initial voltage stored into the capacitor and τ the RC time constant.
Considering then the output in time domain, the effect of different capacitor value *Figure 10* and LNA output impedance *Figure 9* can be easily predicted since those parameters will influence the RC time constant of the circuit.

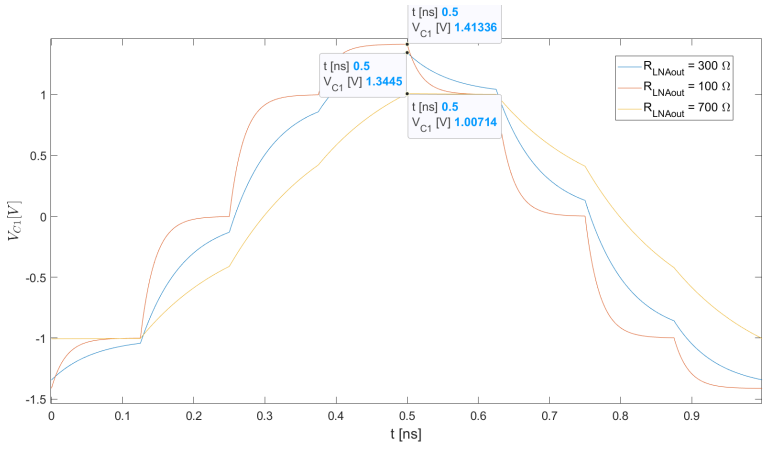


Figure 9: Periodic steady state (pss) analysis of the output of the first branch for $C = 200fF$ and different values of LNA output impedance R_{LNAout}

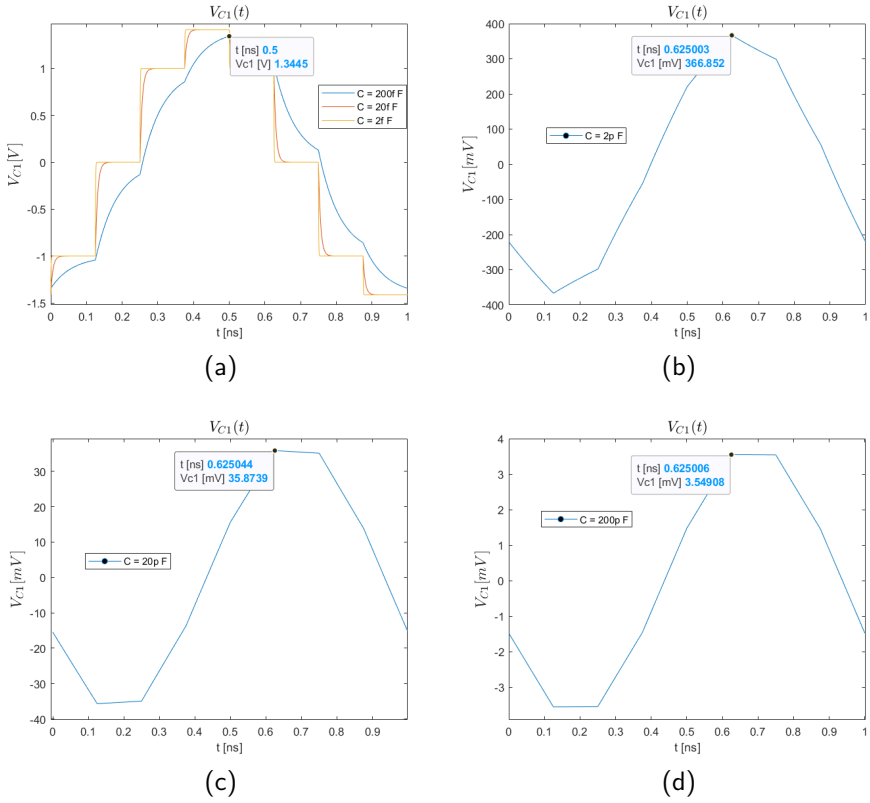


Figure 10: Pss analysis of the output of the first branch for $R_{LNAout} = 300\Omega$ and different values of capacitor

Investigating first the effect of different loading capacitors on a configuration with $R_{LNAout} = 300\Omega$, it is possible to observed in *Table 2* how different loads could affect the linearity of the generated signal.

Capacitors	Fundamental H1 [dBv]	H3 [dBc]	H5 [dBc]	H7 [dBc]	H9 [dBc]
200 pF	-48.77	-51.10	-55.53	-33.80	-38.16
20 pF	-28.77	-57.03	-61.47	-33.80	-38.17
2 pF	-9.06	-62.93	-67.12	-33.52	-37.88
200 fF	2.21	-59.12	-59.05	-25.36	-29.51
20 fF	2.78	-56.16	-56.26	-17.19	-19.55
2 fF	2.79	-41.56	-41.56	-16.90	-19.09

Table 2: Harmonic analysis: effect of different capacitor on an ideal circuit with a 300Ω LNA output impedance

Analyzing the results, the fundamental harmonic amplitude have an inversely proportional dependence with the value of the capacitor. In particular, when the RC time constant is too large with respect to the switching period, the capacitor will not reach the steady state condition applied at its input. This will leads to have a gain in the fundamental attenuation of approximately 20 dBv when dividing by 10 the value of the applied loads. This result could be also verified using the outcomes reported in "N-Path Filtering and Mixing Analysis - A General Approach Based on Fourier Transform" article in which this author will be involved and publication date is after the actual work presentation. In the mentioned article, the relation between the load capacitor and the gain will be demonstrated.
Studying the rejection of harmonics, in *Table 2* only the odd ones are shown due to the fact that the symmetry of the circuit allows to highly reject and consider negligible all the even harmonics. As aforementioned, for a N-path structure the first harmonics that should appear are the (N-1) and (N+1) ones. Therefore, using an 8-path structure particular attention should be payed on the rejection of the 3^{rd} and 5^{th} harmonics when analyzing the effect of different components. Evaluating the results in *Table 2*, the third harmonic rejection is slightly more critical than the fifth one considering the range in pF, while it is almost the same using lower value of capacitors, in the femto Farad range.
The same analysis could be done changing the LNA's output resistance as in *Table 3* and *Table 4*, investigating then also the effect of these parameter on the harmonics rejection.

Capacitors	Fundamental H1 [dB]	H3 [dBc]	H5 [dBc]	H7 [dBc]	H9 [dBc]
200 pF	-39.28	-51.11	-55.54	-33.80	-38.17
20 pF	-19.31	-59.85	-64.28	-33.78	-38.14
2 pF	-1.38	-63.64	-67.89	-31.76	-36.11
200 fF	2.72	-56.63	-57.52	-19.36	-22.65
20 fF	2.79	-41.56	-41.56	-16.94	-19.14
2 fF	2.79	-41.56	-41.56	-16.90	-19.08

Table 3: Harmonic analysis: effect of different capacitor on an ideal circuit with a 100Ω LNA output impedance

Capacitors	Fundamental H1 [dB]	H3[dBc]	H5 [dBc]	H7 [dBc]	H9 [dBc]
200 pF	-56.11	-51.09	-55.49	-33.80	-38.16
20 pF	-36.11	-51.10	-55.54	-33.80	-38.16
2 pF	-16.17	-60.84	-65.27	-33.75	-38.11
200 fF	0.29	-62.38	-66.45	-30.32	-34.64
20 fF	2.75	-56.37	-56.84	-18.27	-21.17
2 fF	2.79	-41.57	-41.57	-16.92	-19.11

Table 4: Harmonic analysis: effect of different capacitor on an ideal circuit with a 700Ω LNA output impedance

Comparing the three tables before, the fundamental harmonic's amplitude is inversely proportional to the R_{LNAout} as well. This fact, as aforementioned is related to the change of the RC time constant.
Changing the output resistance of the LNA the impact on the harmonics rejection of the capacitor will differ, maintaining however an high attenuation in the range between $200fF - 20pF$. Investigating further, it is possible to retrieve the optimal condition for which the higher harmonics rejection could be reached for a specific LNA's output resistance.
The optimal values of capacitors for each considered configuration are summarized in *Table 5* where it is possible to witness a substantial reduction in the magnitude of odd harmonics compared to the fundamental frequency, reaching attenuation levels of several orders of magnitude. The effect of those optimal values on the generated signal shape is reported in *Figure 11*.

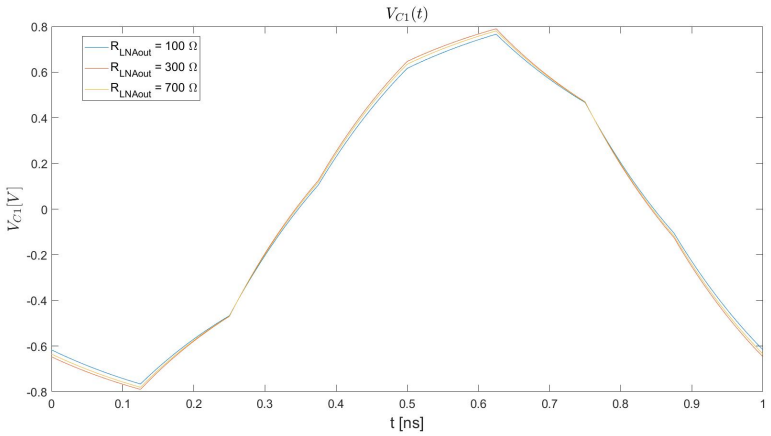


Figure 11: Periodic steady state: analysis optimal capacitor value for different LNA output impedance

R_{LNAout}	Optimal Capacitor	H1 [dBv]	H3 [dBc]	H5 [dBc]	H7 [dBc]	H9 [dBc]
100 Ω	2.5 pF	-2.68	-63.85	-68.21	-32.39	-36.74
300 Ω	800 fF	-2.39	-63.95	-68.24	-32.27	-36.62
700 Ω	350 fF	-2.50	-64.26	-68.11	-32.32	-36.67

Table 5: Harmonic analysis: optimal capacitor value for different LNA output impedance

By examining the data and graph before mentioned, it can be determined that there exists an optimal RC time constant for which, under the given operating conditions, maximum harmonic rejection is achieved. The calculated τ should be around 2 times the pulse width used for the switches ($T_{ON} = 125ps$). However, from the implementation point of view particular attention should be payed on the values of the used capacitors. Capacitor that are too small (in the order of some hundreds of femto Farad) can be highly affected by Process, Volt-

age, and Temperature (PVT) variations, leading to changes in its capacitance value. These variations can cause shifts in circuit parameters such as frequency response, bandwidth, and overall signal integrity. Therefore, to manage for PVT variations lower capacitor values should be excluded from the analysis.
Moreover, high capacitor value will affect the miniaturization and the scaling down of the overall circuit. Since a typical metal capacitance density can be for example $5fF \cdot \mu m^2$, to realize a 20 pF a $4000\mu m^2$ capacitor area should be considered. For all the aforementioned reasons, a standard 2 pF capacitor value is taken for the analysis performed in the next subsections.

6.2 Impact of components mismatch on the generated signal quality

The discussions presented in the preceding chapters were centered around the conceptual ideal circuit configuration, devoid of any introduction of component mismatches or deviations. These deliberations provided a foundational understanding of the circuit's behavior under ideal typical conditions, laying the groundwork for a comprehensive exploration of its performance characteristics and responses. By initially examining the circuit's ideal state, we established a baseline understanding from which we can then delve into the complex dynamics that arise due to real-world variations and mismatches in the components. This approach enables us to identify how the circuit's behavior may be influenced and how it may deviate from its theoretically perfect behavior when subjected to the variations that occur in real-world scenarios. In this section we will investigate the different types of non idealities and their effect on the generated signal in an harmonic rejection N-path circuit using Monte Carlo simulations on Cadence environment.

Monte Carlo simulation is a computational technique used to model and analyze the behavior of complex systems through random sampling. In our study, we employed Monte Carlo simulation to assess the robustness and reliability of our circuit design in the presence of parameter variations. This technique involves generating a large number of random input values for the circuit's key parameters, incorporating statistical distributions that represent their variability due to manufacturing tolerances or environmental factors.
By simulating a significant number of scenarios, we gain insights into the range of possible outcomes and the likelihood of specific events occurring. Monte Carlo simulation provides a comprehensive view of how parameter variations affect the overall performance metrics of the circuit, allowing us to identify potential weaknesses and design improvements that can enhance the circuit's reliability under real-world conditions. The results of the simulation guide our design decisions and contribute to a more robust and dependable final product.

Incorporating Monte Carlo simulation into our design process helps us account for uncertainties and provides a quantitative assessment of the circuit's performance in a realistic operating environment, contributing to more conscious design choices and higher-quality outcomes.

6.2.1 LNA gain mismatch

In the preceding section, we delved into the examination of various output impedance configurations for the Low-Noise Amplifier. However, in the context of practical LNA design, achieving precise and targeted amplification levels presents a formidable challenge. The effects of manufacturing variabilities and environmental factors can contribute to deviations from the ideal amplification goals. As a consequence, it becomes essential to not only consider the theoretical analyses but also account for the nuances of real-world scenarios when designing LNAs for optimal performance.
In the studied analysis a ground noise in the same order of the LNA gains tolerances was considered for the branches which actually should be not connected to any LNA as in the theoretical investigation in the previous chapter.

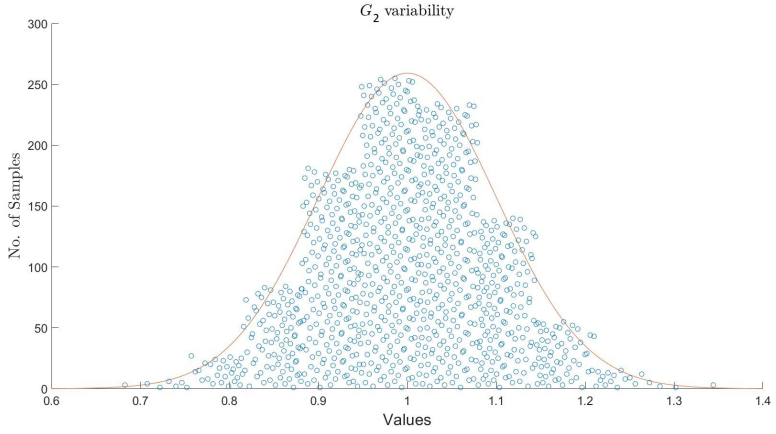


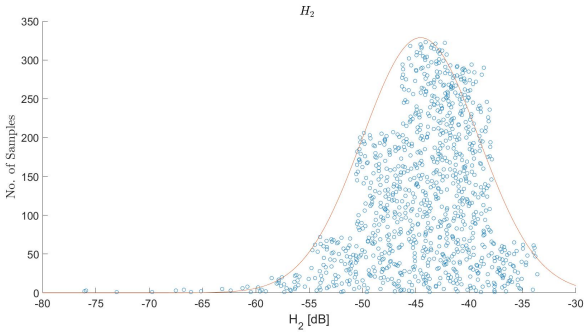
Figure 12: Gain mismatch in the G_2 LNA value

The Monte Carlo analysis was performed by the use of n = 1000 samples considering Gaussian distributions as the one in *Figure 12* and targeting an arbitrary 0.1 standard deviation for all the amplifications value.
The resulting mean values and the corresponding standard deviation deriving from the simulation are reported in *Table 6*, where the real mean value differs from the ideal ones only due to the fact that the simulation was performed considering a non infinite number of samples.

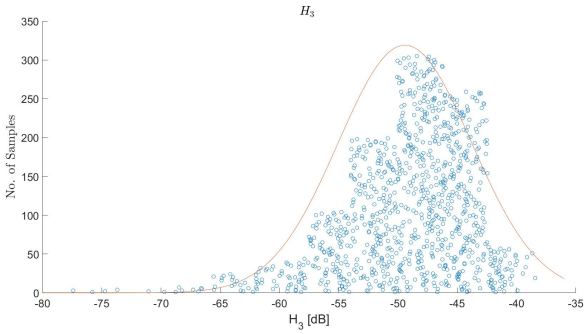
Gain	Ideal value	Real mean value	std deviation
G_1	0	-116.513μ	99.9659m
G_2	1	1.00044	99.9525m
G_3	$\sqrt{2}$	1.41397	100.051m
G_4	1	999.573m	99.9367m
G_5	0	111.311μ	99.882m
G_6	-1	-999.851m	100.057m
G_7	-$\sqrt{2}$	-1.4142	100.215m
G_8	-1	-1.00049	100.117m

Table 6: LNA gaussian distribution gains

The impact of non-ideal amplification values was explored through analysis of *Figure 13* where some of the harmonic amplitudes are shown. Analysing the trends of the results, the derivation of a pseudo-Gaussian distribution could be retrieved.



(a)



(b)

Figure 13: Pss analysis of the output of the first branch for $R_{LNAout} = 300\Omega$ and different values of capacitor

These distributions elucidate the implications stemming from the existence of non-perfectly symmetrical LNA gain values, leading to the emergence of even harmonics. This occurrence also leads to a deterioration in the average rejection of the odd harmonics, as evidenced by the data presented in *Table 7*. The table highlights the mean values of the Gaussian distribution for the harmonics, corresponding to the average scenario.
Moreover, upon comparing these findings with those presented in *Table 2*, it becomes evident that the discrepancies introduced in the gain values will not have an important impact on the fundamental harmonic. As previously analyzed, this amplitude is principally determined by the RC time constant.

H1 [dBv]	H2 [dBc]	H3 [dBc]	H4 [dBc]	H5 [dBc]	H6 [dBc]	H7 [dBc]	H9 [dBc]
-9.08	-35.48	-40.34	-47.54	-49.11	-54.46	-33.5	-40.87

Table 7: Harmonic analysis: effect of Gaussian distribution for 300Ω LNA output impedance

However, the information reported in the previous table gives only some remarks on the overall mean harmonics attenuation considering the all sets of value in the variability system. This means that these attenuation levels are referred to the mean case for a bench of circuits which components have the same variability. To completely investigate the effect of a defined gains configuration on a specific harmonic, the analysis reported in *Figure 14* should be considered. The chart represents the third harmonic as a function of different inputs combination represented by each iteration.

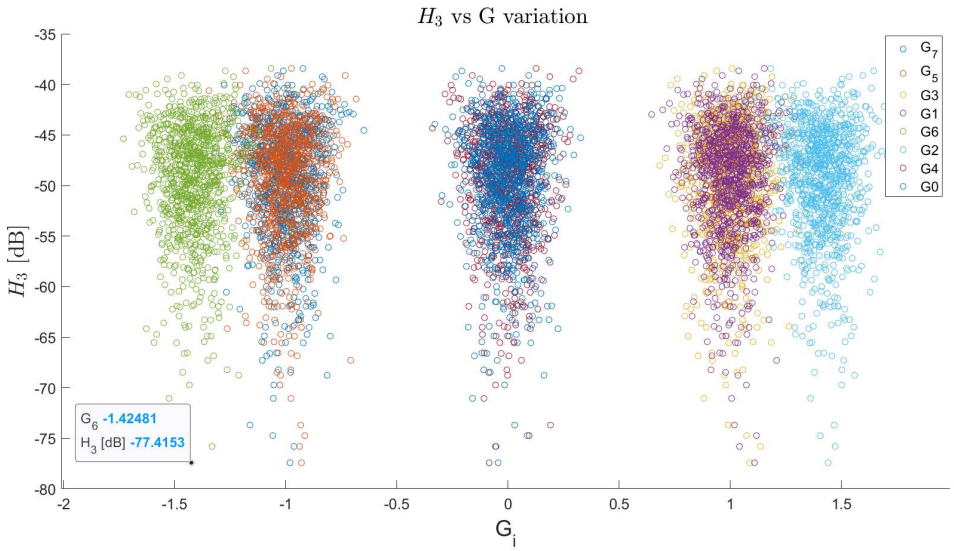


Figure 14: Gains mismatch effect on the third harmonic amplitude

From *Figure 14*, it is possible to identify a set of LNA gains that allows reaching a third harmonic rejection which is even higher than the one analyzed in *Table 2* where the ideal case was shown. This means that a combination of LNA's gain values in *Table 8* different from the theoretical ones could be implemented in order to maximize the rejection of some specific harmonics.

G_1	G_2	G_3	G_4	G_5	G_6	G_7	G_8
-44.65 m	1.11	1.29	1.09	-84.68 m	-930.00 m	-1.42	-980.59 m

Table 8: LNA possible gains for improving the H3 rejection for a 300Ω LNA output impedance implementation

H1 [dBv]	H2 [dBc]	H3 [dBc]	H4 [dBc]	H5 [dBc]	H6 [dBc]	H7 [dBc]	H9 [dBc]
-9.00	-34.95	-68.41	-40.68	-61.54	-54.01	33.49	37.87

Table 9: Harmonic analysis: effect of specific LNA gains value for improving H3 rejection for a 300 Ω LNA output impedance implementation

The impact of this specific set of values on the rejection of all harmonics is detailed in Table 9. A comparison of these results with the reference values in Table 7 reveals an enhancement in the rejection of odd harmonics in contrast to the average case, although there is a decline in the rejection of even harmonics. Nevertheless, when compared to the ideal scenario presented in Table 2, only the third harmonic demonstrates improvement.

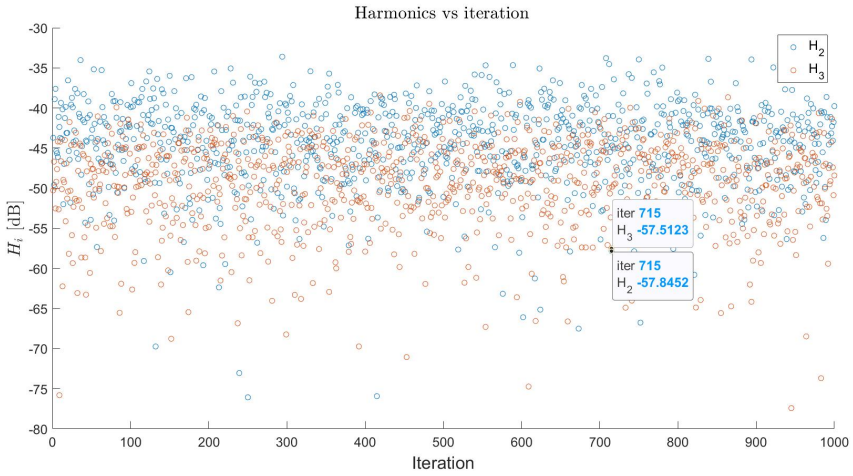


Figure 15: Second and third harmonics Vs iteration

Another valuable method employed to delve into the complexities of harmonics rejection across each iteration configuration executed through the Monte Carlo simulation is through the examination of harmonic amplitudes against iteration counts, as depicted in *Figure 15*. By collectively analyzing various harmonics, this approach enables the identification of a shared rejection target ($> -45dB$ in the example) that remains consistent across each harmonic. Consequently, this technique facilitates the discovery of a corresponding configuration that optimally achieves the desired level of rejection across all harmonics of interest. This process provides a deeper understanding of the interplay between configuration parameters and harmonics rejection, offering insights that can contribute to the refinement and enhancement of the overall circuit performance.

6.2.2 Clock signal mismatches

Generating a stable and accurate clock signal in a circuit, such as the one illustrated in *Figure 8*, can introduce a range of complexities and challenges. Mismatch-related discrepancies in the clock signal can arise from various factors, including process variations, temperature fluctuations, and voltage supply inconsistencies. These disparities can result in variations in the clock signal's frequency, amplitude, and phase, all of which are critical parameters for the proper operation of the circuit.
Furthermore, mismatches can impact the duty cycle and rise/fall times of the clock signal, leading to variations in the switching behavior of the associated transistors. Inaccurate switching characteristics can give rise to undesirable inter-modulation products and a decline in the rejection of harmonics. These concerns become particularly relevant in applications where precise signal timing and control are essential.
Effectively managing these challenges related to clock signal generation requires a well-thought-out design approach and meticulous implementation. Strategies like calibration, signal conditioning, and the use of specialized clock generation circuits can help mitigate the effects of mismatches and ensure the reliable performance of the circuit. By delving into these clock-related complexities, we can enhance the overall robustness and efficiency of the circuit's operation.
In this section we will investigate the different types of mismatch related to the clock signal generation and their effect on the generated output signal linearity.

6.2.2.1 Delay

In the structure of *Figure 8* the clock signals (S_i) are non overlapped and have all a pulse width equal to T_{LO}/N, where N is the number of used path. In real cases, a clock signal may be affected by phase accuracy (t_{js}) which introduce an unintended variations in the timing or phase of a signal's edges or transitions. Moreover, variations in timing and phase can occur due to factors like

propagation delays, impedance mismatches, and component mismatches. These variations can lead to timing misalignment between different parts of the circuit, affecting the overall performance.

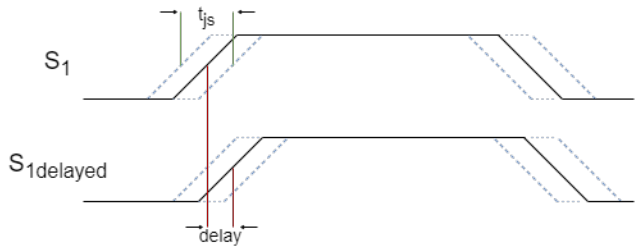


Figure 16: Clock's mismatch

As seen in *Figure 16*, both phase accuracy and variations in timing can collectively contribute to mismatches in the timing at which the pulse width is allocated to the corresponding switch. Naming D_i the instant of time the pulse width is given to a specific switch S_i for commutation, to simulate its mismatch with respect to the ideal case a Monte Carlo analysis could be performed even for this case. For these simulations, a standard deviation of 10 ps was utilized, representing a common scenario accounting for approximately 1% of the clock's period. The outcomes of the analysis, encompassing the delay distributions examined, are graphically presented in the figure provided below.

Gain	Ideal value [ps]	Real mean value [ps]
D_1	0	0.01494
D_2	125	124.951
D_3	250	250.044
D_4	375	374.957
D_5	500	500.001
D_6	625	624.975
D_7	750	749.988
D_8	875	875.011

Table 10: Delay mean values for Gaussian distribution

All the analysis performed in the previous section regarding the rejection of the harmonics and the arrangements we can adopt for improving them could be repeated considering only the mismatches of the delay. By investigating the effect of these distribution on the average harmonics rejection (*Table 11*) it could be noticed that the overall attenuation is deteriorated with respect to the ideal case analyzed previously.

H1 [dBv]	H2 [dBc]	H3 [dBc]	H4 [dBc]	H5 [dBc]	H6 [dBc]	H7 [dBc]	H9 [dBc]
-11.00	-16.5	-19.42	-24.04	-24.07	-26.22	-20.31	-25.37

Table 11: Harmonic analysis: effect of phase noise

The decline in the attenuation of all harmonics can be anticipated by examining the system's behavior. For instance, if one or more branch are delayed in responding to the applied DC input, it can result in an uneven distribution of current or voltage among the branches. This, in turn, can disrupt the balance of the circuit and introduce unexpected voltage drops or current flows. Furthermore, if there are phase differences between the branches due to mismatch or delay, they might not sum up as expected. This can lead to unwanted cancellations or amplifications of certain signal components, potentially causing unexpected variations in the output.

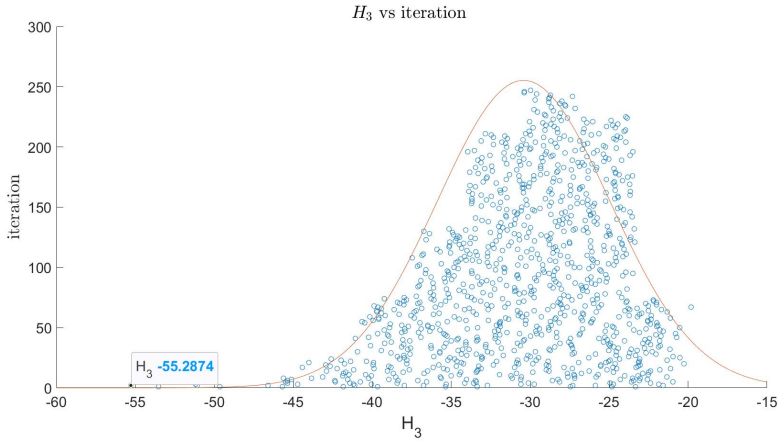


Figure 17: Effect of clock's delay on the third harmonic

The effect of the delays mismatch on the third harmonic is shown in *Figure 17* a maximal rejection of $-45.12dB$ represented by the marker in the figure can be reached. This results highly differ from the ideal one in which a rejection of $-62.93dB$ was achieved. This notable distinction arises from the fact that any simulated configuration introducing delays in the signal driving the switch, deviating from the ideal setup, leads to a decline in the harmonic rejection. Additionally, upon simulating n=1000 samples, the ideal configuration enabling higher attenuation could not be replicated.
Furthermore, the fundamental harmonic experiences attenuation because, in some of the analyzed delay scenarios, the clock signals overlap. This overlapping compromises the output signal quality as cross-conduction occurs between multiple branches within the same path.

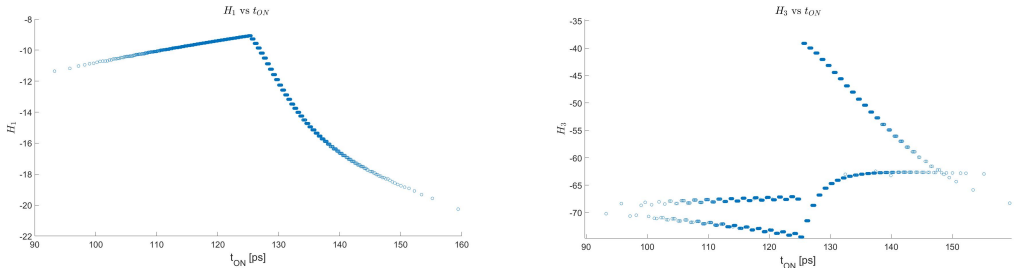
6.2.2.2 Duty Cycle

Variations in the duty cycle of a clock signal can significantly impact the performance of electronic circuits. The duty cycle represents the ratio of the signal's active state (t_{ON}) to its inactive state within one period. A precisely controlled duty cycle is important for ensuring accurate timing synchronization and reliable system operation. One of the factors contributing to duty cycle variations is phase accuracy, as illustrated in *Figure 16* which introduces unintended fluctuations in the signal's timing or phase. Similarly, a Monte Carlo simulation was employed to simulate Duty Cycle mismatch, revealing the average harmonic rejections as depicted in *Table 12*. The simulation was performed considering the same duty cycle for each clock signal and assuming a Gaussian distribution with standard deviation of 1% of the clock's period.

H1 [dBv]	H2 [dBc]	H3 [dBc]	H4 [dBc]	H5 [dBc]	H6 [dBc]	H7 [dBc]	H9 [dBc]
-11.43	-231.69	-51.96	-232.9	-58.07	-233.02	-23.31	-31.9

Table 12: Harmonic analysis: effect of a different duty cycle

As depicted in the table, the even harmonics rejection are not influenced by the duration of each pulse width since the symmetry between branches is not affected. Moreover, the attenuation of odd harmonics deviates from the ideal scenario due to instances where certain duty cycle values lead to cross-conduction between different branches. As a result, the rejection of odd harmonics becomes less effective compared to the ideal case.



(a) (b)

Figure 18: Fundamental and third harmonic as a function of the duty cycle

The *Figure 18* represent the behaviour of the fundamental and the third harmonic introducing the mismatch in the active period of the clock signal and so in its duty cycle. As shown, the biggest influence will be present when the clocks of different branches will overlap as mentioned above.

6.2.3 Mismatch Results analysis

Summarizing the conclusions drawn from the preceding sections, it becomes evident that the introduction of mismatches leads to a deterioration in the circuit's overall performance. Nevertheless, potential calibration procedures could be explored to attain a targeted condition that maximizes the attenuation of specific harmonics. Furthermore, our analysis revealed that the primary influence on the harmonic rejection level arises from the delays in the clock signals. Indeed, a variation of 1% in the clock's delay is impacting more the performances than a variation of 10% of the LNA gain values. These delays can result in uneven voltage distribution and cross-conduction between different branches, exerting a significant impact on the circuit's harmonic rejection characteristics.
A more complete analysis can be performed considering both the mismatches introduced by the LNA gain values and the one of the clock signal. Conducting this investigation, we are able to derive the average outcomes presented in *Table 13*. Comparing these results with the outcomes in *Table 11* it could effectively noticed that the circuit's overall performance is predominantly shaped by the discrepancies in delay timings. This underscores the critical role that delay mismatching plays in influencing the operational characteristics of the circuit.

H1 [dBv]	H2 [dBc]	H3 [dBc]	H4 [dBc]	H5 [dBc]	H6 [dBc]	H7 [dBc]	H9 [dBc]
-11.69	-18.56	-20.75	-25.12	-25.42	-28.31	-20.24	-36.75

Table 13: Harmonic analysis: effect of the combination of different mismatches

Focusing on the rejection of the third harmonic improvement, performing the analysis as in the previous sections, the outcomes in *Table 14* can be extracted.

H1 [dBv]	H2 [dBc]	H3 [dBc]	H4 [dBc]	H5 [dBc]	H6 [dBc]	H7 [dBc]	H9 [dBc]
-9.765	-36.50	-48.80	-41.14	-30.44	-44.82	-26.98	-49.05
G_1	G_2	G_3	G_4	G_5	G_6	G_7	G_8
-27.29 m	1.1217	1.5904	870.93 m	140.73 m	-1.16	-1.5016	-833.46 m
D_1 [ps]	D_2 [ps]	D_3 [ps]	D_4 [ps]	D_5 [ps]	D_6 [ps]	D_7 [ps]	D_8 [ps]
0.35	115.99	253.7	367.44	502.43	620.24	756	883.9

Table 14: Harmonic analysis: Improvement of harmonics rejection through specific mismatches combination

Moreover, the resulting pulse width of the clock for this configuration to improve the third harmonic rejection was $t_{ON} = 108.55ps$ which results in having a 10.86% duty cycle. As highlighted by this outcomes, it is possible to find a configuration that compensates for the lacks in harmonics rejection introduced by the delays of clock by tuning other components value as the LNA gain values.

7 Receiver mode

When working in receiver mode, the circuit on *Figure 6* could be considered, where the input signal of interest takes the form of an RF sinusoid. As expounded upon in Chapter 5, this configuration engages the N-path structure in a mixing mode, thereby facilitating the rejection of harmonics.
However, the successful implementation of this setup necessitates an LNA configuration that facilitates the transition from a single-ended to a differential arrangement, ensuring the synthesis of the required differential gain values for the HR-NPM structure. A plausible approach involves the utilization of a common gate common source (CG-CS) amplifier. Notably, this type of amplifier can accommodate single-ended input signals, simplifying the integration of such signals and allowing for enhanced voltage gain due to the series connection of a common gate stage followed by a common source stage. Nevertheless, it is important to acknowledge that this arrangement might introduce more noise compared to a fully differential amplifier, stemming from the cascaded architecture of the two distinct stages. Additionally, this structure might exhibit a limited bandwidth and present higher design complexity.
To streamline the analysis, our study assumes a differential input derived from a passive balun. This choice facilitates the examination of the circuit using a fully differential amplifier. In *Figure 19* the configuration of the HR-NPM coupled with the differential LNAs can be observed.

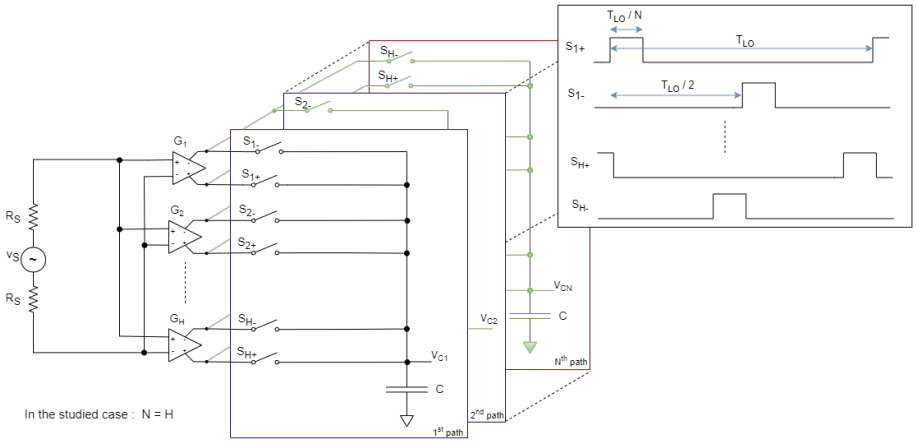


Figure 19: HR-NPM structure with differential input

Within this section, our inquiry will delve into the practical implementation aspects of the differential LNA. Subsequently, we shall present the outcomes of the mixing process, shedding light on the generated output results.

7.1 LNA implementation

As previously indicated, the selected amplifiers for our circuit are the differential transconductance amplifiers, the detailed analysis and corresponding equations of which can be found in Appendix B. By referencing the supplementary materials in Appendix B, we aim to offer readers a more in-depth insight into the intricacies and mathematical foundations of the selected differential transconductance amplifiers. The final schematic of the used amplifiers is reported in the figure below.

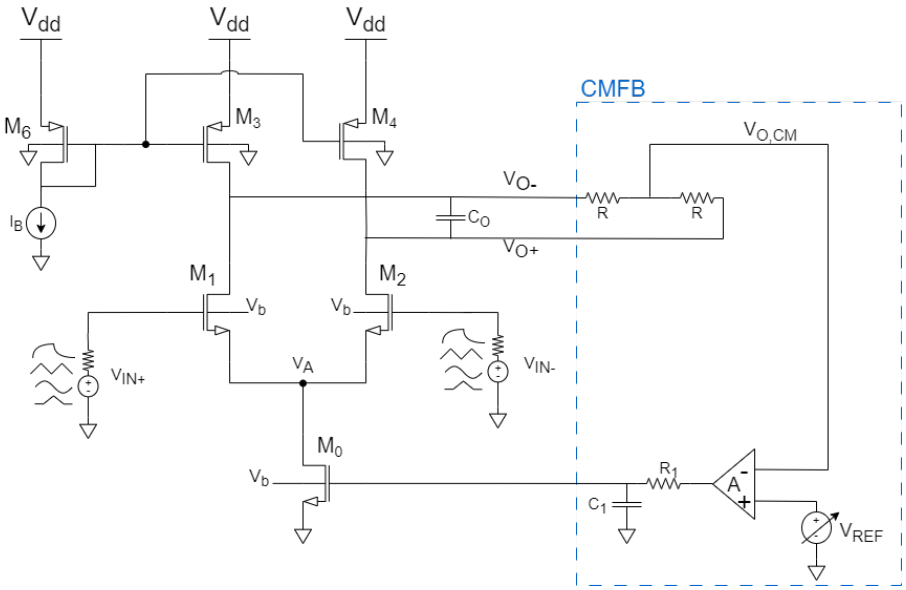


Figure 20: Used amplifier in the HR-NPM analysis

The schematic in *Figure 20* represent the first stage of a complete LNA in which a final stage should be considered. During the design procedure, a body biasing equal to $V_b = 1.5V$ was considered for all the used nMOS which allows reducing the threshold voltages. This choice make easier the polarization of the used nMOS lowering the minimum value for the CMIR as reported in Appendix B. An ideal Common-Mode Feedback Circuit, labelled CMFB in *Figure 20*, has been employed in this preliminary validation. The used resistor are in the order of $T\Omega$ so that they will not influence the frequency response and the common mode output voltage could be extracted and a gain A equal to 1000.
As analyzed in the previous chapter when explaining the principle of the harmonic rejection, the interrelation of amplification values holds significance, with their absolute values being less relevant. In essence, when aiming for a specific value of G_2, the corresponding G_3 amplification need only to be $\sqrt{2}$ times the value of G_2.

Moreover, considering the structure presented above, the common mode output voltage cannot be null for polarizing the pMOS side. Taking then the single ended output to have the positive and negative amplification for the system in *Figure 19*, the two signals will have a DC value different from zero. This implies that in order to achieve accurate harmonic rejection, all amplifiers should have uniform DC values and exhibit specific correlations among them as stipulated by the theoretical investigation.

Two amplifiers were designed in FD-SOI 28nm technology to simulate respectively the theoretical gain of 1 and the one equal to $\sqrt{2}$. For both amplifiers the same nMOS sizing was used, having $L_1 = L_2 = 70nm$, $L_0 = 100nm$, $W_1 = W_2 = 70\mu m$ and $W_0 = 10\mu m$. Then, the applied input biasing voltage to have all the nMOS in saturation region is equal to $V_{CM} = 324.35mV$ while using a biasing current of $I_B = 100\mu A$.
To have the two different gains, the pMOS sides of the amplifiers will be different as reported in the *Table 15*, where the M_3 and M_4 are considered equal and all the length of the pMos are equal to $L = 100n$.

Amplifier	Ideal gain	Real gain	$(W)_{M_3}$	$(W)_{M_6}$	$V_{O,CM}$
A	1	12.44	25 μm	2.5 μm	464.84 mV
B	$\sqrt{2}$	18.02	19.9 μm	1.99 μm	506.03 mV

Table 15: LNAs results

Furthermore, the table report the value of $V_{O,CM}$, showing that for the two circuit the common mode output voltages differs. As observed earlier, considering the influence of amplification correlation on harmonic rejection, any disparity in the DC output values of the two amplifiers will compromise the effectiveness of harmonic rejection. To address the issue stemming from distinct $V_{O,CM}$ values, a biasing voltage was introduced to the outputs, thereby aligning them to a uniform value of 500 mV.

Moreover, the $R_1 = 100K\Omega$ $C_1 = 1pF$ network was introduced to insert a low frequency pole and avoid the instability of the common mode feedback loop. Additionally, the dissimilar pMOS characteristics in the two amplifiers lead to distinct parasitic capacitance and, consequently, varying frequency responses in their outputs. This discrepancy introduces a phase shift between the amplified signals of the two amplifiers. To address this phase shifting issue, a capacitor C_O was introduced. For the amplifiers outlined in *Table 15*, specific values of these capacitors were set: $C_{O,A} = 1fF$ and $C_{O,B} = 12fF$, corresponding to their respective amplifiers.
The output waveform of the amplifiers are reported in *Figure 21*, where also the exact trend of the ideal signal multiplied by the $\sqrt{2}$ factor is reported.

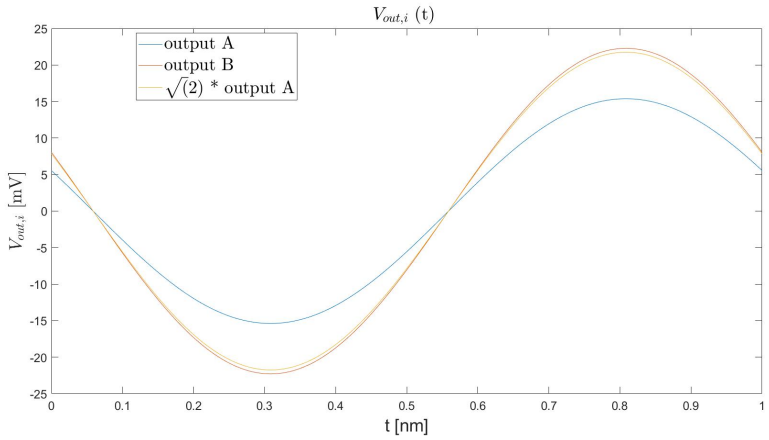


Figure 21: Differential output for the designed amplifiers

From the figure above and the *Table 15*, it could be noticed that the B's amplification has exactly the correlation seen in the theoretical analysis. This occurrence is aligned with the investigation carried out earlier concerning the disparities in the amplification values of the LNAs in the generation mode section. Subsequently, the noise figure of the designed amplifiers could be retrieved starting from the definition of Noise Factor:

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{P_{signal,in}}{P_{noise,in}} \cdot \frac{P_{noise,out}}{P_{signal,out}} \tag{5}$$

$$F = \frac{P_{signal,in} \cdot Gain}{P_{noise,in} \cdot Gain} \cdot \frac{P_{noise,out}}{P_{signal,out}} = \frac{P_{noise,out}}{P_{noise,in} \cdot Gain} \tag{6}$$

Observing that the term $P_{noise,in} \cdot Gain$ represent the noise contribution of the input signal at the output ($P_{outNoise,in}$), the previews equation could be rewrite as:

$$F = \frac{P_{noise,out}}{P_{outNoise,in}} \tag{7}$$

Performing then a noise simulation with Cadence software, the noise contribution of one port on the total output noise is the 22.43%. Considering then the differential input and so the contribution of both input ports, the result below is obtained.

$$F = \frac{P_{noise,out}}{44.86\% \cdot P_{noise,out}} = \frac{1}{44.86\%} \tag{8}$$

The correlated noise figure is computed as $NF = 10\log(F) = 3.48dB$. In comparison with the prevailing values found in literature, the noise figure of

the achieved LNA slightly exceeds the norm. Modern LNAs usually maintain a noise figure below 3 dB. Enhancing the noise figure of the designed amplifier could involve employing specialized techniques such as input impedance matching. This approach might encompass the utilization of input inductors with precisely designed values to emulate a 50Ω resistor, thus achieving compatibility with the input ports.
Furthermore, it is imperative to refine the design of these amplifiers to ensure that the DC input value can be consistently amplified with the same predetermined correlation established during the theoretical analysis to make them suited for the generation mode. A plausible avenue for this refinement could involve fine-tuning the body bias voltages of the pMOS sides of the amplifiers or potentially integrating two additional pMOS transistors in parallel with M_3 and M_4, respectively. These supplementary MOSFETs would need to operate in the saturation region during the generation mode and in the OFF state when in the mixer mode. However, it should be noted that these solutions might introduce secondary effects, necessitating further investigation.

In conclusion, the optimization of the employed amplifiers must extend to factors such as noise figures, feedback loop characteristics and value of $V_{O,CM}$, and DC amplification. Although these amplifiers have been subjected to testing, the subsequent section delves into an exploration of the results from the output mixing mode.

7.1.1 Mixer output

An ideal mixer facilitates the conversion of modulation centered around a specific carrier frequency to a different frequency. Within a receiver context, this transformation typically occurs from a higher Radio Frequency (RF) frequency to a lower Intermediate Frequency (IF) frequency. Conversely, in the case of a transmitter, the process is reversed.
In the studied case of a receiver, the RF and LO inputs signal can be considered as:

$$v_{RF}(t) = A(t)cos(w_0 t + \phi(t)) \tag{9}$$

$$v_{LO}(t) = A_{LO}cos(w_{LO} t) \tag{10}$$

Therefore, applying the trigonometric properties:

$$\begin{aligned} v_{out}(t) &= v_{RF}(t) \cdot v_{LO}(t) \\ &= \frac{A(t)A_{LO}}{2} \cdot \{cos(\phi)\,[cos(w_{LO} + w_0)t + cos(w_{LO} - w_0)t] + \\ &- sin(\phi)\,[sin(w_{LO} + w_0)t + sin(w_{LO} - w_0)t]\} \end{aligned} \tag{11}$$

Resulting in:

$$v_{out}(t) = \frac{A(t)A_{LO}}{2} \cdot \{cos[(w_{LO} + w_0)t + \phi(t)] + cos[(w_{LO} - w_0)t + \phi(t)]\} \tag{12}$$

As a result, the modulation is effectively translated to two distinct frequencies: $f_1 = f_{LO} + f_{RF}$ and $f_2 = f_{LO} - f_{RF}$. Typically, we opt for either the upper or lower sideband by employing filtering on the mixer's output. Considering the N-path structure in *Figure 19*, to reject the unwanted frequencies specific combination between the signal at the output of the paths *Figure 22* could be adopted.

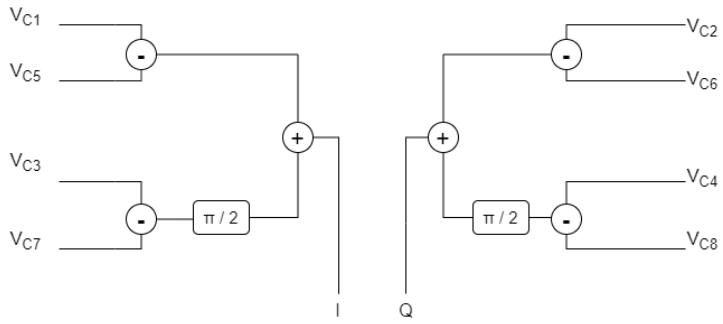


Figure 22: Output signal branch combination for IQ modulation

In the reported scenario, the first subtraction stage is used to reject the even harmonics and the DC part, so the harmonic 0 as shown in *Figure 23*.

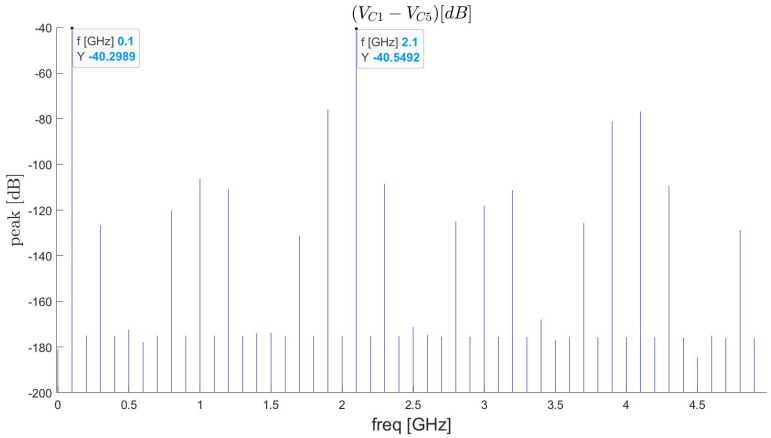


Figure 23: Spectral analysis for the combination of V_{C1} and V_{C2} considering $f_{LO} = 1GHz$ and $f_{RF,2} = 1.1GHz$

The $\pi/2$ phase shifter and the final summation is used for the elimination of the unwanted f_1 or f_2 as represented in *Figure 24* and *Figure 25*.

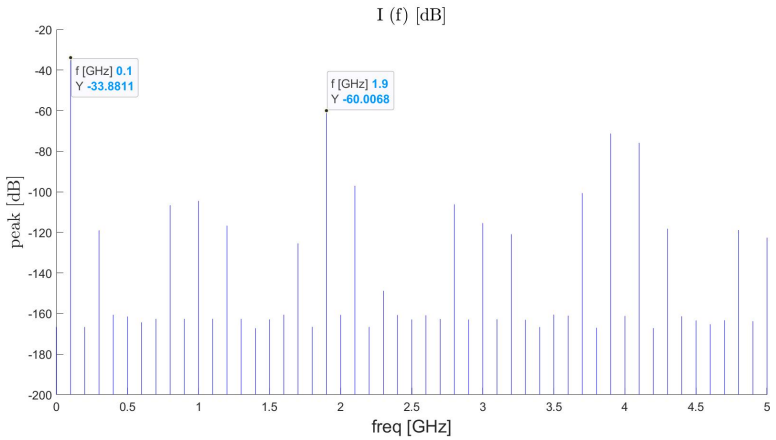


Figure 24: Spectral analysis for the in-phase output considering a $f_{RF} = 0.9GHz$

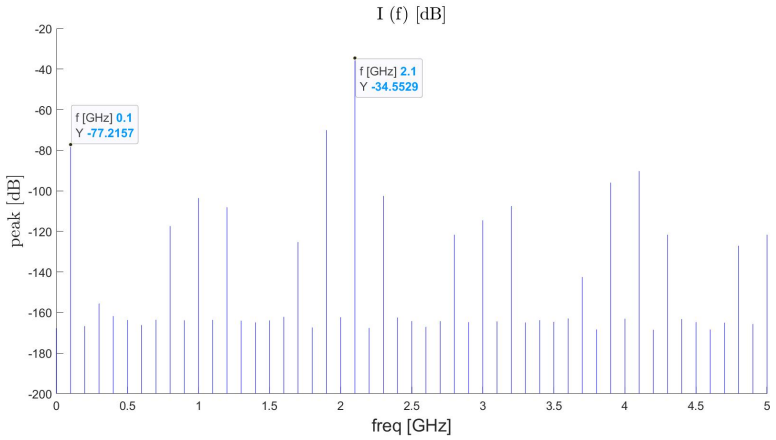


Figure 25: Spectral analysis for the in-phase output considering a $f_{RF} = 1.1GHz$

The two figures above show that considering a local oscillator with frequency $f_{LO} = 1GHz$, if a radio frequency signal with lower frequency $f_{RF,1} = 0.9GHz$ is applied at the input of the mixer, the frequency $f_1 = f_{LO} + f_{RF,1}$ will be attenuated. Contrarily, applying $f_{RF,2} = 1.1GHz$ the mixing frequency $f_1 = f_{LO} - f_{RF,2}$ is attenuated. Finally, the outputs of this combinations will be two sinewave signal, one in-phase (I) and one in quadrature (Q).

8 Conclusions

This study undertook a thorough exploration of the properties of the harmonic rejection N-path mixer, with the primary objective of showcasing the potential reconfigurability and adaptability of one of the primary blocks within a radiofrequency receiver. The HR N-path structure was evaluated in two operational modes: generation mode and mixer mode.

The generation mode involves working with a DC input signal to synthesize a sinusoidal signal. This synthesized signal can serve for calibrating other components or the N-path structure itself. For instance, it could be used to calibrate the delay in the local oscillator by adjusting the frequency. The scrutiny of this operational mode provided insights into the impact of real-world components on the quality of the generated signal. The key finding indicated that maintaining the quality of the LO signal, and consequently minimizing mismatches in duty cycle and particularly in delays, is crucial to prevent degradation of harmonic rejection. Furthermore, specific mismatch conditions that deteriorate signal integrity led to the identification of component values that could be adjusted to enhance the rejection of specific harmonics. An illustrative instance is the Chapter 6 where a set of values was presented to improve the third harmonic rejection while accounting for the influence of all circuit mismatches.

In the receiver mode, the foundational mathematical principles of the mixer were presented, including a possible LNA implementation design and the combination of N-path outputs to achieve optimal harmonic rejection. Furthermore, given that all the components used in the two operational modes are identical, all the considerations made in the generation mode can also be applied to the receiver mode. Consequently, calibrating the circuit in generator mode will enable calibration in receiver mode as well.

Nevertheless, despite these comprehensive analyses, several challenges remain unresolved, such as devising an LNA capable of amplifying both DC and RF voltages. The discussions presented in this work have laid a solid foundation for future implementations and explorations of reconfigurable circuits and calibration methodologies. This subject will be further delved into by the author in an upcoming Ph.D. research with the topic "Design of self-adjusting radio frequency circuits to optimize the energy efficiency of applications."

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A Appendix - N path structure

The N-path structure in *Figure 3*, could act either as a band-pass filter if the output is taken considering V_x node or as a mixer if the output is taken at the capacitor end. To better understand the behaviour of this structure, *Figure 26* from [20] could be analysed.

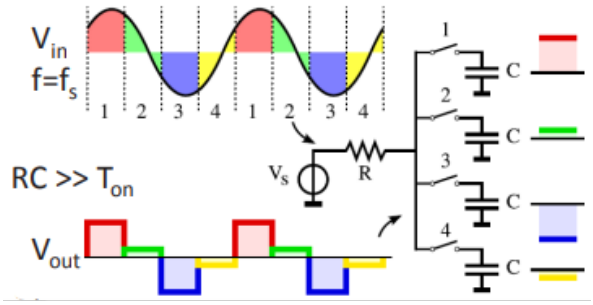

Figure 26: N-Path filtering principle [20]

The depicted diagram illustrates that when $f_{in} = f_{SW}$, within the duration of t_{ON} when a switch conducts, the capacitor undergoes charging with a corresponding segment of the input sinewave. Subsequently, the capacitor accumulates the DC value of the sampled portion of the sinewave. It's worth noting that due to the typically much larger RC time constant compared to t_{ON}, multiple periods must transpire before this stored value stabilizes.

In the case of $f_{in} \neq f_{SW}$, the sampled section of the sinewave will inevitably vary throughout the t_{ON} period of a particular branch. This variation results in a zero value being stored within the capacitor and subsequently yielding a zero V_{OUT}, highlighting the band pass filtering behaviour.
The N path filter operates intrinsically as a passive mixer due to the multiplication of the clock signal and the sine wave within each path. This operation inevitably results in a frequency-transposed signal, which can either represent a baseband signal when the switching period T_{SW}, aligns with that of the RF sine wave input or an intermediate frequency when the LO frequency deviates from the RF frequency.

From these considerations it results that the N-path structure acts both as a filter and as a mixer, avoiding the use of additional antecedent filters in receivers with mixer first structure.

However, as shown in *Figure 3*, the local oscillator signals are not pure sine waves but periodic pulse impulse which will then carry numerous harmonics. With this structure all the harmonics are present with exception for the N^{th} one, affecting then the quality of the output signal.

Considering the structure in *Figure 4* instead, each path consists of two branches that process a differential input signal. This input signal is switched using a LO control signal based on π delay. Using this setup, every path act as a basic mixer controlled by two LO signals which actually constitute an effective LO eflo(t) signal. With this structure, the even harmonics are suppressed in the eflo(f) having then the first harmonic folding for the 3^{rd} RF harmonic.

Numerous designs proposed in literature focus on generating the appropriate effective LO signal in the simplest and most efficient manner possible. The analysis in this work is performed through the use of the HR-NPM which structure is depth investigated in Chapter 5

B Appendix - Differential Amplifier

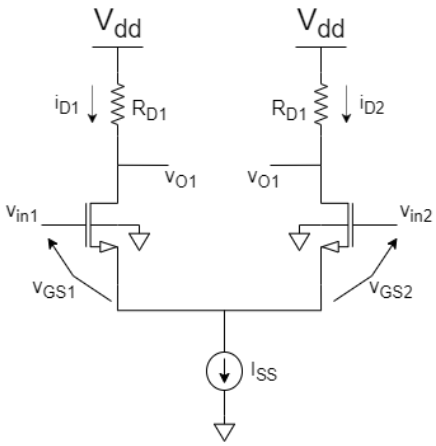

Figure 27: Differential amp schematic

The figure above presents the conceptual differential amplifier schematic, where the two inputs are equal to:

$$v_{in1} = V_{cm} + v_d/2 \tag{13}$$

$$v_{in2} = V_{cm} - v_d/2 \tag{14}$$

From the Kirchhoff law:

$$v_{in1} - v_{gs1} + v_{gs2} - v_{in2} = 0 \tag{15}$$

$$v_d = v_{gs1} - v_{gs2} = V_{th1} + v_{od1} - V_{th2} - v_{od2} = v_{od1} - v_{od2} \tag{16}$$

Furthermore, considering the overdrive voltage:

$$v_{od} = \left[\frac{i_{D,Q}}{\beta_n \left(\frac{W}{L}\right)}\right]^{1/2} \tag{17}$$

The previous equation can be rewritten as:

$$v_{od} = \left[\frac{1}{\beta_n \left(\frac{W}{L}\right)}\right]^{1/2} \left(\sqrt{i_{D1}} - \sqrt{i_{D2}}\right) \tag{18}$$

Moreover using also the equation

$$i_{D1} + i_{D2} = I_{SS} \tag{19}$$

It is possible to find out that the two drain currents are equal to:

$$\begin{cases} i_{D1} = \dfrac{I_{SS}}{2} + \dfrac{1}{2}\left[\beta_n \left(\dfrac{W}{L}\right) v_d \left(\dfrac{2I_{SS}}{\beta_n \left(\frac{W}{L}\right)} - v_d^2\right)^{1/2}\right] \\ i_{D2} = \dfrac{I_{SS}}{2} - \dfrac{1}{2}\left[\beta_n \left(\dfrac{W}{L}\right) v_d \left(\dfrac{2I_{SS}}{\beta_n \left(\frac{W}{L}\right)} - v_d^2\right)^{1/2}\right] \end{cases} \tag{20}$$

Which graphically translates into:

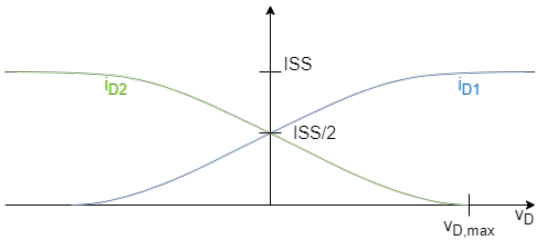

Figure 28: i_D vs v_d

The maximal differential voltage to apply at the input in order to have both branches of the differential pair active should be lower than:

$$v_{d,max} = \left[\frac{I_{SS}}{\beta_n \left(\frac{W}{L}\right)}\right]^{1/2} \tag{21}$$

In order to improve linearity, a lower range ($v_{d,max}/2$) is typically used. Therefore, the output voltage will be equal to:

$$\begin{gathered} v_O = v_{O1} - v_{O2} = V_{DD} - R_{D1} i_{D1} - (V_{DD} - R_{D2} i_{D2}) \\ v_O = R_{D2} i_{D2} - R_{D1} i_{D1} \end{gathered} \tag{22}$$

Considering a null differential input:

$$v_{O,CM} = (R_{D2} - R_{D1}) \frac{I_{SS}}{2} \tag{23}$$

This means that the common mode propagates to the output due to the mismatch between the two resistors.

Differential amplifier with active components

With the prospective of miniaturization, active component could be considered, resulting in the schematic reported below. Tho further investigate this structure

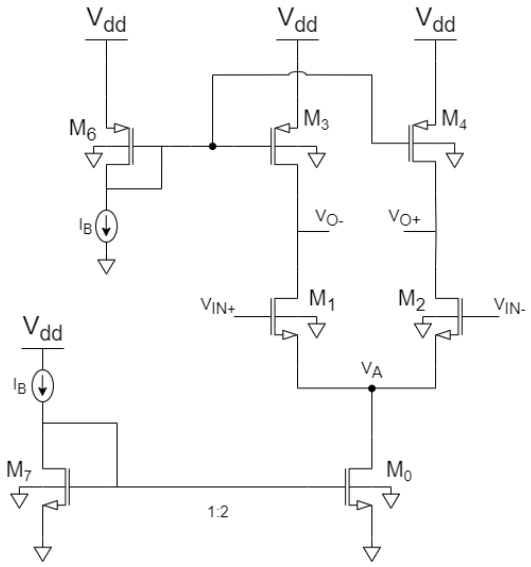

Figure 29: Differential amplifier with active load

properties different analysis could be performed.

CMIR (Common Mode Input Range)

The CMIR of that circuit could be found considering a null differential input and analyzing the input common mode voltage range that allow the correct behaviour of the circuit.
As previously mentioned, with a null differential input:

$$i_{D1} = i_{D2} = I_{SS}/2 \tag{24}$$

Moreover:

$$v_{O1} = v_{O2} = V_{dd} - v_{SD3} \tag{25}$$

For the circuit to function as an amplifier, certain conditions need to be met. Firstly, both transistors M_1 and M_2 should be operating in saturation. This requirement establishes the upper limit of the operational range. Secondly, transistor M_0 also needs to be in saturation. This condition sets the lower limit for proper amplifier functionality. The CMIR will then results in:

$$V_{th,n} + v_{OD1} + v_{OD0} \leq V_{CM} \leq V_{dd} - v_{SD3} + v_{th,n} \tag{26}$$

DMOR (Differential Mode Output Range)

The voltage at one of the output is maximum when no current flows in the

respective branch and then it reach the V_{dd} value. For the lower limit instead, the saturation of the input MOS have to be considered:

$$v_{DS1} \geq v_{OD1} \tag{27}$$

$$v_{O2} - V_A = v_{O1} - (V_{CM} - v_{gs1}) \geq v_{OD1} \tag{28}$$

Therefore, the DMOR results to be:

$$V_{CM} - V_{th,n} \leq v_{O2} \leq V_{dd} \tag{29}$$

Differential gain

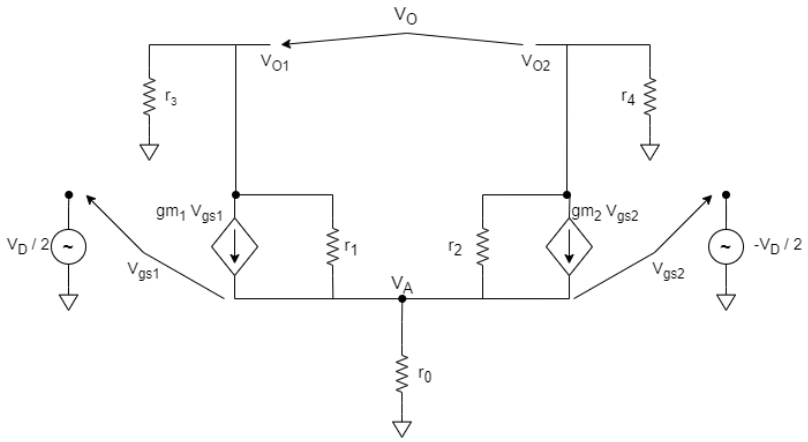

Figure 30: Small signal: differential input

Considering the equivalent small signal circuit it is possible to find the output relation as follow:

$$v_O = v_{O1} - V_{O2} = -g_{m1}(r_1//r_3)\left(\frac{v_D}{2}\right) - \left(-g_{m2}(r_2//r_4)\left(-\frac{v_D}{2}\right)\right) \tag{30}$$

At $g_{m1} = g_{m2} = g_m$ and $r_1//r_3 = r_2//r_4$:

$$A_d = -g_m(r_1//r_3) \tag{31}$$

Common Mode gain

Considering the small signal configuration, the influence of the input common mode on the output can be analyzed.

Defining the parallel resistor of the branches as:

$$\begin{aligned} R_{D1} &= (r_1 + 2r_0)//r_3 \\ R_{D2} &= (r_2 + 2r_0)//r_4 \end{aligned} \tag{32}$$

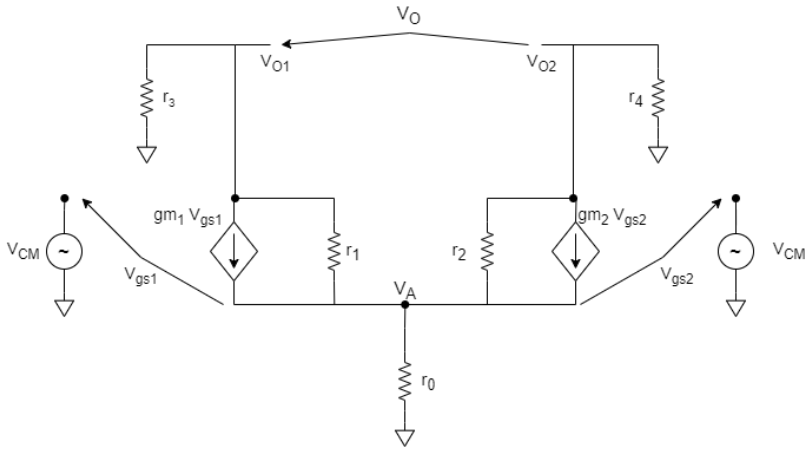

Figure 31: Small signal: common mode input

The two output nodes will have a voltage equal to:

$$\begin{aligned} v_{o1} &= -g_{m1}R_{D1}(V_{CM} - V_A) \\ v_{o2} &= -g_{m2}R_{D2}(V_{CM} - V_A) \end{aligned} \tag{33}$$

Where the voltage at node A is given by:

$$V_A = r_0(i_{D1} + i_{D2}) = r_0(g_{m1} + g_{m2})(V_{CM} - V_A) \tag{34}$$

$$V_A = \frac{r_0(g_{m1} + g_{m2})}{1 + r_0(g_{m1} + g_{m2})} V_{CM} \tag{35}$$

Replacing it in the previous equations, the output due to a common mode input can be founded.

$$V_o = V_{o1} - V_{o2} = -\frac{g_{m1}R_{D1} - g_{m2}R_{D2}}{1 + r_0(g_{m1} + g_{m2})} V_{CM} \tag{36}$$

Furthermore defining the variations and the mean values:

$$\Delta g_m = g_{m1} + g_{m2} \qquad \Delta R_d = R_{d1} - R_{d2} \tag{37}$$

$$\overline{g_m} = \frac{1}{2}(g_{m1} + g_{m2}) \qquad \overline{R_d} = \frac{1}{2}(R_{d1} + R_{d2}) \tag{38}$$

The common mode amplification will be:

$$A_{CM} = \frac{\overline{gm}\Delta R_d + \overline{R_d}\Delta g_m}{1 + 2r_0\overline{g_m}} \tag{39}$$

Finally, the Common Mode Reject Ratio is given by:

$$CMRR = \left| \frac{A_d}{A_{CM}} \right| = \frac{1}{\frac{\Delta R_d}{R_d} + \frac{\Delta g_m}{g_m}} (1 + 2r_0 \overline{g_m}) \tag{40}$$

Current mirror

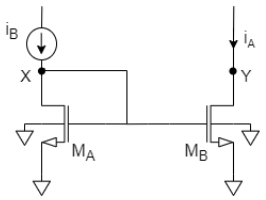

Figure 32: Current mirror

Considering the simple current mirror circuit, the ratio between the currents can be expressed as:

$$\frac{i_A}{i_B} = \frac{\mu_n \frac{C_{OX}}{2} \left(\frac{W}{L}\right)_B (V_X - V_{th,B})^2 (1 + \lambda_B V_Y)}{\mu_n \frac{C_{OX}}{2} \left(\frac{W}{L}\right)_A (V_X - V_{th,A})^2 (1 + \lambda_B V_X)} \tag{41}$$

$$\frac{i_A}{i_B} = \frac{\left(\frac{W}{L}\right)_B (1 + \lambda_B V_Y)}{\left(\frac{W}{L}\right)_A (1 + \lambda_B V_X)} \tag{42}$$

To avoid mirroring error $V_X = V_Y$ should be guaranteed. To do that a possible solution is to implement the following circuit:

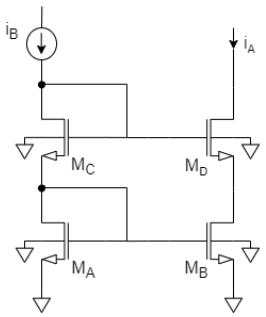

Figure 33: Improved current mirror

By guaranteeing $v_{GS,C} = v_{GS,D}$ the mirroring error will be cancelled. However this configuration could suffer for output swing limitation. In our case, we opt for a configuration involving a common mode output feedback which allows avoiding these type of current mirrors.

CM control at the output of the differential amplifier

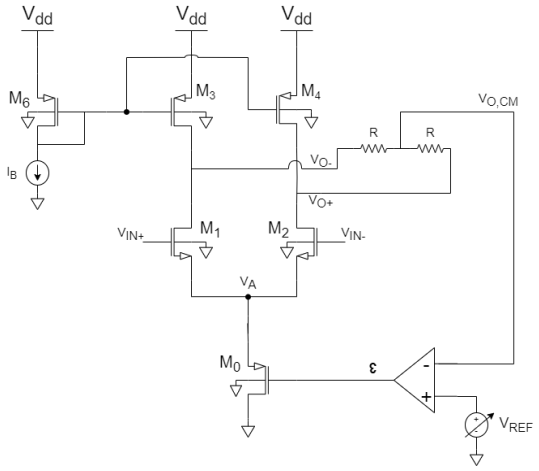

Figure 34: Common mode feedback theoretical circuit

With this configuration, through tuning the value of the V_{REF} is possible to control the common mode voltage at the output. The error ϵ allow the regulation of the I_{SS} value.

$$v_{O,CM} = V_{O-}\frac{R}{2R} + V_{O+}\frac{R}{2R} = \frac{V_{O-} + V_{O+}}{2} \tag{43}$$

A possible solution to implement the theoretical schematic is reported in figure 35.

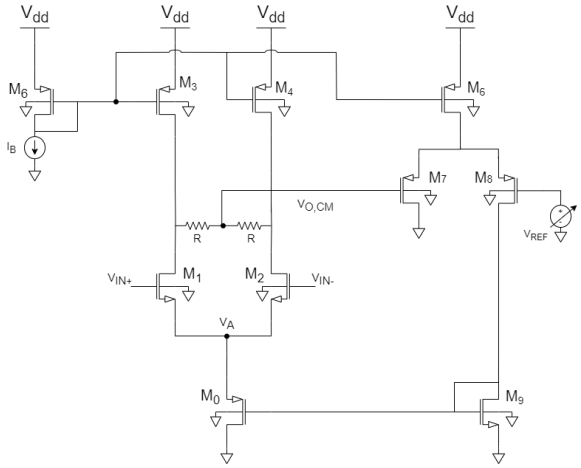

Figure 35: Common mode feedback circuit