Politecnico Di Torino

A.a 2022/2023

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Design and Optimization of a Digital-Based Operational Transconductance Amplifier

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Abstract

The spreading of IoT (Internet of Things) devices has posed a great challenge to the world of integrated circuit design. Systems need to be smaller and consume less energy, as they are sometimes powered by small batteries or in combination with energy harvesting devices. Technology scaling has allowed digital circuits to benefit from it. Analog subsystems, on the other hand, represent the bottleneck in terms of power dissipation and occupied area.

Operational transconductance amplifiers are essential in analog subsystems such as filters, front-end signal conditioning circuitry or inter-stage amplificatior for ADCs. To be included in the construction of IoT devices, they must meet the conditions of low power dissipation and small occupied area.

Over the years, to reduce the performance gap between analog and digital subsystems, various analog functions have been rethought in digital terms to leverage the technological advancements and digital design flow benefits.

For this reason, the concept of DIGOTA (Digital-based Operational Transconductance Amplifier) has been explored. Several research studies and prototypes have demonstrated its compatibility with the specific requirements in the field of IoT (Internet of Things).

The objective of this thesis work is to optimize this particular topology by proposing a new input stage based on Floating Inverters (FI). This new stage adds a preamplification and provides the ability to control the common mode at the input without using resistive components.

The performance of the circuit has been evaluated after the layout was im-

plemented and parasitic extraction was carried out. Subsequently, Monte Carlo simulations have been conducted to assess the circuit's sensitivity to process variations. The results have then been compared with the state of the art.

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Chapter 1

Introduction

1.1 IoT

The Internet of Things (IoT) is the concept according to which there exists a vast network of interconnected devices and systems equipped with computing units and sensors. The IoT world has revolutionized the way we approach the world.

Figure 1.1: IoT network

Market forecast

Research and innovation are also driven by an economic reason that justifies the interest of industries in producing devices for this sector. Some studies predict that a significant portion of the market will be dominated by this industry.

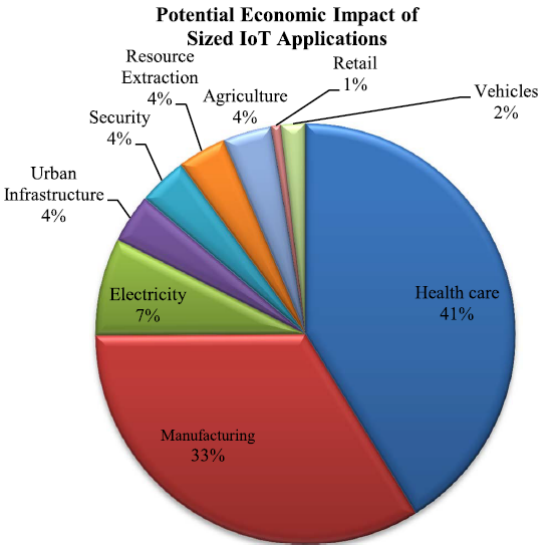


Figure 1.2: Projection of market share of IoT applications [1]

According to the forecasts of the McKinsey Global Institute, there has been a remarkable growth in interconnected machines, as well as in the traffic monitoring of cellular networks. The economic growth for IoT devices related to healthcare and manufacturing is expected to have a greater impact: healthcare because it is increasingly common to have services related to prevention and diagnosis through electronic tools, and the manufacturing world because automation is becoming more predominant, and the need to monitor and control the factory remotely is becoming increasingly necessary. [1].

Nonetheless, these statistics indicate the possibility of substantial and rapid IoT growth in the near future, encompassing associated industries and services. This trend presents a distinctive chance for conventional equipment and appliance manufacturers to adapt their products into "smart devices".

The shift toward greater portability and wearability in healthcare screening devices has prompted the development and production of microelectronic devices for biomedical signal processing. These biomedical devices have demanded high processing speed, low power consumption, and robust equipment.

The aim has been to create low-voltage, implantable, and portable biomedical electronic devices for diagnosing health issues. [5]

Technical challenge and analog world as bottlneck

IoT nodes perform the function of sensing any real-world parameter (such as sound, image, biometric data, biomarkers sensors). The sensing chain is always followed by a signal conditioning chain before ADC conversion and the digital domain processing. Afterward, it is transmitted to other IoT nodes through the transmission chain, as depicted in the Figure 1.3.

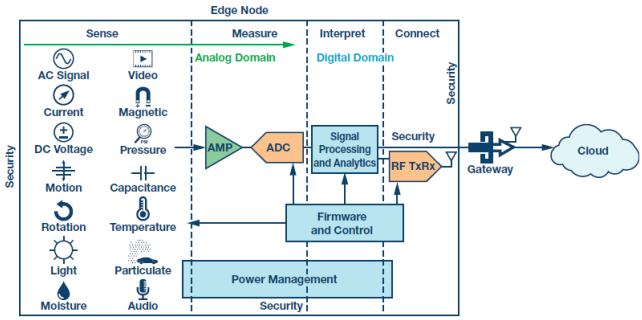


Figure 1.3: IoT Node [2]

The technological scaling described in Figure 1.4 demonstrates how the increase in circuit density and complexity has allowed integrated systems to operate at a lower voltage. This improvement is primarily attributed to the benefits gained by digital subsystems.[4]

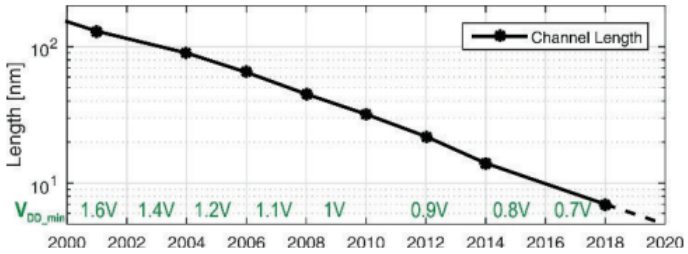


Figure 1.4: Moore' law [3]

However, as Figure 1.5 illustrates, fundamental analog blocks such as the operational transconductance amplifier (OTA) have not taken advantage from this technological trend.

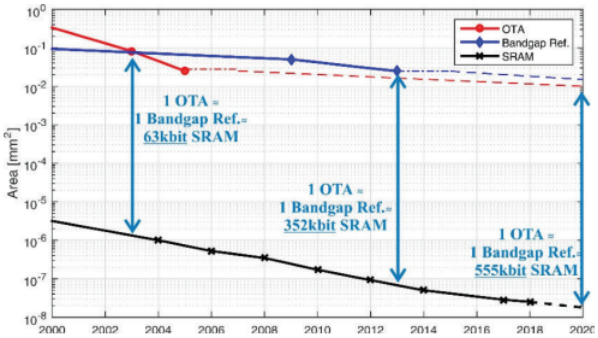


Figure 1.5: Analog vs Digital scaling [4]

The main reason is that often what leads to better performance for digital subsystems is in contrast with the desired performance in the analog world. This can include factors such as signal swing, the need for good matching, and the intrinsic characteristics of transistors when working with smaller dimensions.

1.2 This work

This work addresses the design in 180nm CMOS technology of a digital-based operational transconductance amplifier (DIGOTA), a specific type of amplifier that meets the performance standards of IoT applications. This amplifier features an input stage that allows innovative common-mode control through a structure called Floating Inverters (FI).

1.3 Thesis organization

In the first introductory chapter, the concept of the Internet of Things (IoT) has been explained, the market trend in this sector and the bottleneck caused by the analog subsystems are highlighted.

In the second chapter, a theoretical overview of operational amplifiers is provided, along with some applications in the IoT domain. Finally, the performance characteristics that qualify them and the main figures of merit are described.

In chapter three, traditional approaches for implementing low-power analog structures are described. Subsequently, digital-based solutions for analog circuits are discussed, referring to existing literature and explored solutions in the field.

In chapter four, the structure of the floating inverter is described using a behavioral model, highlighting how it is utilized to enable the operation of the DIGOTA. Subsequently, the design in CMOS 180nm technology is presented. Schematic simulations are shown, followed by post-layout simulations and Monte Carlo analyses.

In chapter five, a comparison of the novel DIGOTA with the state-of-the-art is presented, based on the performance obtained through simulations. Finally, conclusions are drawn, and potential ideas for future work are discussed.

Chapter 2

Overview on operational amplifiers

This chapter presents a review of the operational amplifier and explains why this building block is used for IoT applications. Finally, there is an overview of performance specifications used in the later chapters for the description of the circuit object of this work.

2.1 Operational amplifier

From [6], an operational amplifier is an electronic device that boosts and manipulates analog signals. It is a small integrated circuit with the ability to greatly amplify signals and perform various operations on them. These devices have two input terminals (inverting and non-inverting) and one output terminal.

The ideal behaviour of the amplifier is described by the equations [2.1] and [2.2], where A_d is defined as the differential amplification of the signal v_d.

$$v_d = v_+ - v_- \tag{2.1}$$

$$v_{out} = A_d v_d \tag{2.2}$$

In the realization of a real op-amp the parameter A_d can not be designed accurately due to the non-idealities of the process of fabrication. But it can be designed to be rather large (1 to 1000000).

This is the reason why operational amplifiers are always used in negative feedback configurations, which allow precise control of the amplifier's gain and other characteristics. Negative feedback is commonly employed also to make the amplifier performance indipendent of process, supply voltage and temperature variations.

A simple description of a negative feedback system can be made with a simple schematic block in figure [2.1].

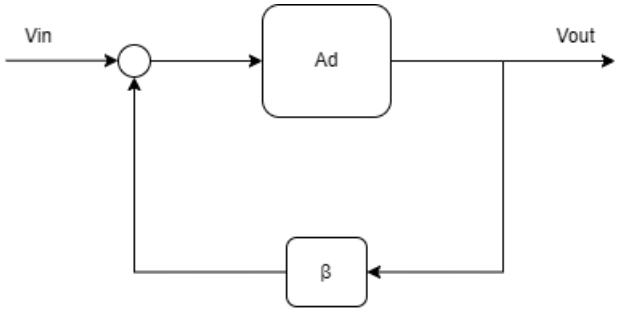


Figure 2.1: Schematic block of amplifier with feedback

It can be shown that:

$$v_{out} = v_{in} \cdot \frac{1}{\beta} \cdot \frac{\beta A_d}{1 + \beta A_d} \tag{2.3}$$

if $\beta A_d \longrightarrow \infty$

$$v_{out} = v_{in} \frac{1}{\beta} \tag{2.4}$$

For this reason the op-amp must guarantee a minimum value of A_d, to ensure the validity of the approximation. The relation [2.4] makes the ratio v_{out}/v_{in} indipendent from the uncertain A_d parameter.

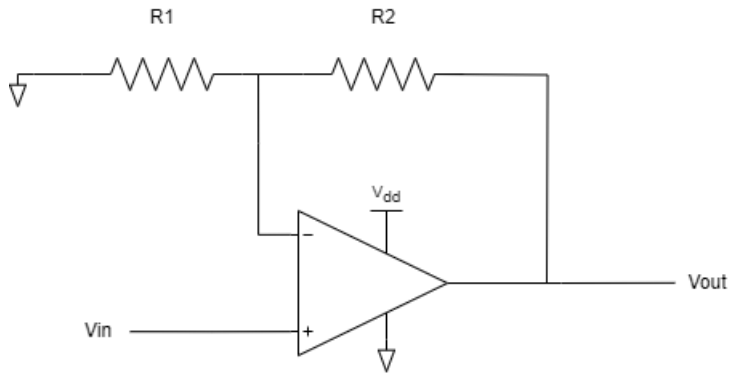


Figure 2.2: Operational amplifier with feedback

Fot the circuit in figure [2.2] it can be shown that:

$$\beta = \frac{R1}{R1 + R2} \tag{2.5}$$

$$A_{cl} = \frac{1}{\beta} = \left(1 + \frac{R2}{R1}\right) \tag{2.6}$$

This example shows that the signal V_{in} can be amplified using a resistor divider and does not depend on the uncertain parameter A_d.

2.2 OTA for IoT applications

Operatioanal amplifiers are essential building blocks for all analog electronic functions, such as filters, front-end signal conditioning circuitry or inter-stage amplificatior for ADCs. The scaling of CMOS technology has facilitated the advancement of low-power electronic systems for IoT nodes.

Some areas of application:

Front-end sensor for biomedical applications The biomedical devices often need to detect low-voltage/low-frequency human physiological signals. The growing demands for these devices has led to the rapid development of low-power analog circuits. In the analog biomedical circuits, OTAs are the most power-hungry sub-blocks, for this reason a low power OTA is suitable for this purpose [7].

Active filter for NB-IoT applications Narrow-band IoT (NB-IoT) is a novel protocol to support narrow-band IoT applications. It plays an important role in mobile communications, such as 5G technology. Low-power/high-preformance analog filters are mandatory modules for NB-IoT receiver blocks. An example is presented in [8].

Inter-stage amplifier for low-power ADCs An essential prerequisite in the design of a pipeline ADC is effective inter-stage amplification. Typically, this amplification is performed by an operational transconductance amplifier (OTA). These OTAs are one of the largest power consumers in the ADC [9].

2.3 Op-amp parameters

In this section, the main parameters of an opamp will be shortly revised. [6]

Open Loop Gain

The open loop gain of an amplifier is the ratio between the differential input and the output.

$$A_d = \frac{v_{out}}{v_d} \tag{2.7}$$

Usually this parameter is evaluated in dB.

$$A_d[dB] = 20log\left(\frac{v_{out}}{v_d}\right) \tag{2.8}$$

Gain bandwidth product

The A_d parameter of a real op-amp is dependent from the frequency, tipically it has a first-order response with one dominant pole. For this reason the gain of a real amplifier has a bandwidth ω_{p1}.

$$A_d(j\omega) = \frac{A_0}{1 + \frac{j\omega}{\omega_{p1}}} \tag{2.9}$$

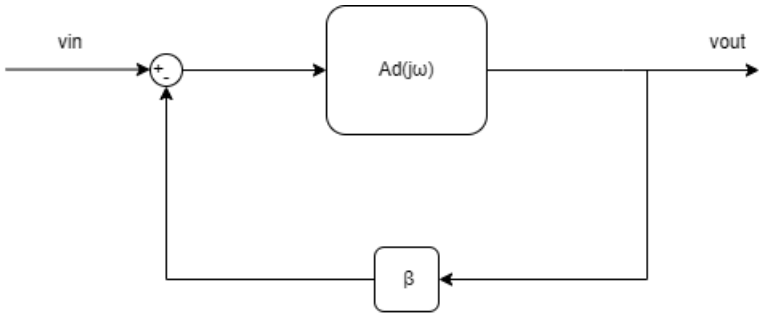


Figure 2.3: Schematic block of amplifier with feedback

The closed loop gain is shown in equation [2.10].

$$A_{cl}(j\omega) = \frac{1}{\beta} \cdot \frac{A_d(j\omega)\beta}{1 + A_d(j\omega)\beta} = \frac{1}{\beta} \cdot \frac{A_0\beta}{1 + A_0\beta} \cdot \frac{1}{1 + \frac{j\omega}{\omega_{p1}(1+A_0\beta)}} \tag{2.10}$$

If $A_0\beta \longrightarrow >> 1$ the equation becomes [2.11].

$$A_{cl}(j\omega) = \frac{1}{\beta} \cdot \frac{1}{1 + \frac{j\omega}{\omega_{p1}(A_0\beta)}} \tag{2.11}$$

The DC closed loop gain is shown in equation[2.12].

$$A_{cl0} = A_{cl}(j\omega \longrightarrow 0) = \frac{1}{\beta} \tag{2.12}$$

The bandwidth of closed loop gain configuration is shown in equation[2.13].

$$\omega_{cl} = \omega_{p1} A_0 \beta \tag{2.13}$$

The product between A_{cl} and the bandwidth ω_{cl} is constant and equal to $\omega_{p1}A_0$. With this consideration the GBW parameters is defined as [2.14].

$$GBW = A_0\omega_{p1} \tag{2.14}$$

It as been shown in equation [2.10] that if $\beta = 1$ (voltage follower configuration) the bandwidth of $A_{cl}(\beta = 1)$ is the GBW.

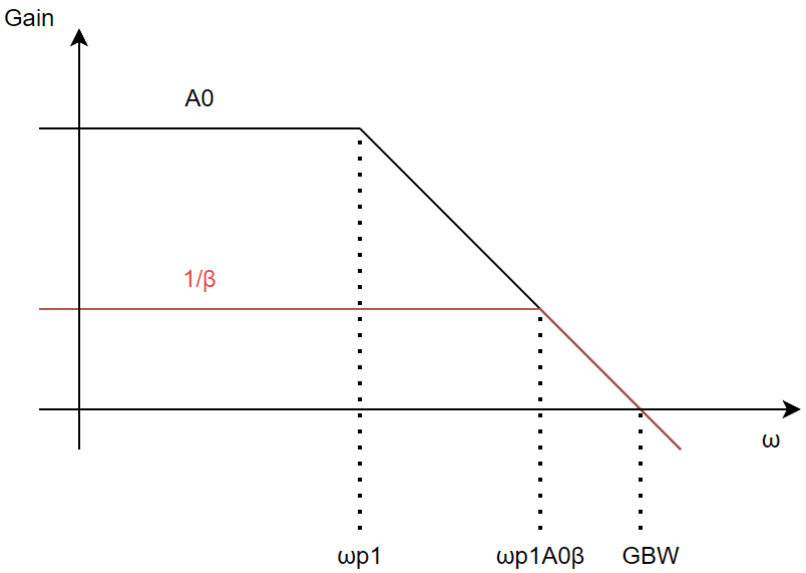


Figure 2.4: Closed-loop and Open-loop gain

PSRR

PSRR stands for Power Supply Rejection Ratio. The parameter quantifies the ability of a device to maintain a stable output in the presence of changes in the power supply voltage. It is typically expressed in decibels (dB) and defines the ratio A_d/A_{ps} where A_{ps} corresponds to the power supply rejection V_{out}/V_{ps} in closed-loop unity-gain configurations. A higher PSRR value indicates stronger rejection of power supply variations, indicating that the device is less affected by changes in the power supply voltage.

CMRR

CMRR stands for Common Mode Rejection Ratio. It measures the ability of an op-amp to attenuate common-mode signals or unwanted noise that appears simultaneously on both input terminals. CMRR is typically expressed in decibels (dB) and represents the ratio of the differential-mode gain to the common-mode gain. A higher CMRR value indicates better rejection of common-mode signals.

$$v_{out} = A_d v_d + A_{CM} v_{CM} \tag{2.15}$$

Where v_{CM} is:

$$v_{CM} = \frac{v_+ + v_-}{2} \tag{2.16}$$

The CMRR is defined as [2.17].

$$CMRR = \frac{A_d}{A_{CM}} \tag{2.17}$$

Slew Rate

The slew rate (SR) is a parameter that describes the rate of change at which the output voltage of an op-amp can change when there is a rapid change in the input signal. Typically measured in volts per microsecond (V/µs) or volts per nanosecond (V/ns), the slew rate represents the maximum slope or steepness of the output voltage waveform. A higher slew rate indicates a faster response of the device to rapid changes in the input signal.

THD

THD stands for Total Harmonic Distortion. It is a metric used to quantify the amount of distortion present in a signal due to the presence of harmonics. Harmonics refer to frequencies that are integer multiples of the fundamental frequency. THD is commonly expressed as a percentage, it represents the ratio of the combined power of all harmonics to the power of the fundamental frequency. A lower THD value indicates lower levels of distortion, while a higher THD value signifies a higher degree of distortion.

$$THD = \frac{\sqrt{v_2^2 + v_3^2 + v_4^2 + \cdots + v_n^2}}{v_1} \tag{2.18}$$

Where v_n are the different harmonic component of the fundamental v_1.

Power consumption

Power consumption in an operational amplifier is generally evaluated by measuring the quiescent current entering in the supply terminal. The average power dissipated is evaluated by this relation [2.19].

$$P_{diss} = I_Q \cdot V_{DD} \tag{2.19}$$

FOM

FOM stands for figure of merit. It is a general term used to describe a parameter that qualifies the design. For comparison purpose different FOM can be defined. In this work [2.21] and [2.20] have been used.

$$FOM_S = \frac{GBW \cdot C_L}{P_{diss}} \tag{2.20}$$

$$FOM_L = \frac{SR \cdot C_L}{P_{diss}} \tag{2.21}$$

Where C_L is the load capacitance on the output node.

Chapter 3

Low-Power amplifiers

This chapter presents an overview of the solutions adopted for the design of low-power OTAs. The first section describes the most frequent approaches to build standard CMOS based OTAs. The second one introduces the novel concept of the digital-based OTA (DIGOTA) [10].

3.1 Traditional topology

This section describes the most common approaches to build a low-power OTA based on popular topology like: conventional differential pair based OTA, two-stage miller OTA and Gilbert cell OTA. Different design strategies can be selected to achieve low supply voltages and therefore less power. The most common: weak inversion (or subthreshold) operation [11] [12], body-driven [13] [14], body-biasing [15] [16], floating-gate approaches [17] [18].

3.1.1 Subthreshold/weak-inversion operation

This approach imply that the V_{gs} applied on each MOS in the circuit is lower than the threshold V_{th}. In this condition the MOS transistors exhibits exponential beahvior, the drain current I_D is exponentially dependent on the V_{gs} (3.1).

An important consideration is that a MOS transistor operated in the subthreshold region has better transconductance efficiency g_m/I_D than a regular biasing. This additionally justify the use of this working region.

The main drawback is the low achievable value of g_m. This causes the dete-

rioration of frequency performances of the device, but sometimes it is not a serious loss for all IoT applications because most of the sensor node applications involve slowly varyng signals (few kHz) [19].

$$I_D = I_S\left(\frac{W}{L}\right)\exp\left(q\frac{V_{GS}-V_{TH}}{nkT}\right)\left[1-\exp\left(-q\frac{V_{DS}}{kT}\right)\right] \tag{3.1}$$

3.1.2 Body-driven devices

The technique consists of the biasing of the MOS transistor with a bias current (I_D) and a fixed V_{gs} to a value slightly above the threshold to create a conducting channel between the drain and source. An example in fig. [3.1].

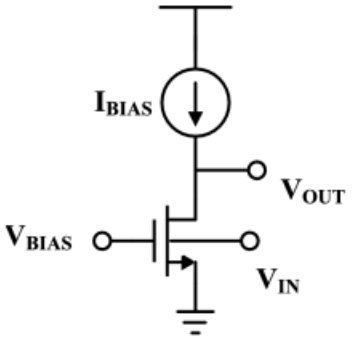


Figure 3.1: Schematic example

The input signal is applied on the body terminal that modulates the conducting channel. In this operation the minimum input voltage is not bounded by the V_{th}, it follows that even rail-to-rail operation is possible.

The main drawback of this solution is that the g_{mb} is about 60-80% lower than the gate-driven operation. This also results in reduced speed and bandwidth.

Another important consideration is the fact that the body terminal of n-MOS transistor is available only if it is technologically realized in triple well [20],[14].

3.2 Floating gate

It is a non-conventional technique that serves to make the threshold of a MOS transistor adjustable. The structure of the FGMOS is the same as a conventional MOS, the difference being that the control gate is electrically isolated from the floating gate but capacitively coupled [3.2].

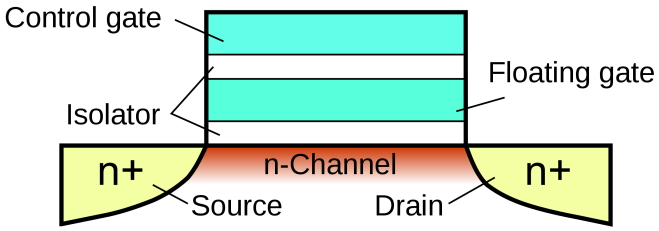


Figure 3.2: Section view of FGMOS

It is possible to vary the threshold voltage of the FGMOS by changing the bias voltage of the control terminal [17].

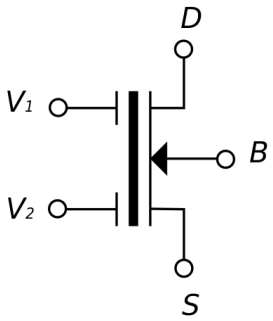


Figure 3.3: FGMOS symbol with two gate control terminal

The main problem with this solution is that it requires models that are often not available in design kits, making it difficult to perform accurate simulations during the design phase. Designing an amplifier with this structure requires a custom and completely non-standardized procedure [19].

3.2.1 Body-biasing

This design method exploits the body of the differential pair as a control terminal to lower the threshold voltage, and to adjust the common-mode of the differential stage. This design technique is used in combinations with the gate-driven technique to take advantage of the higher value of g_m.

The main drawback is the current consumption increase caused by the additional circuitry needed to generate the bias voltage for the body terminals [15] [16].

3.3 Digital-Based Analog Differential Circuit

In this section the working principle of digital-based analog differential circuit is presented, the relationship between input and digital output is derived, and how the common-mode input is rejected in order to guarantee the correct behaviour of the circuit.[10]

3.3.1 Operating principle

In the most general sense, a differential circuit creates a link between the difference of two measured quantities and the output (e.g., voltage, currents). The input-output relation is not necessarily linear. For this reason, two identical buffers can be used to implement such operation.

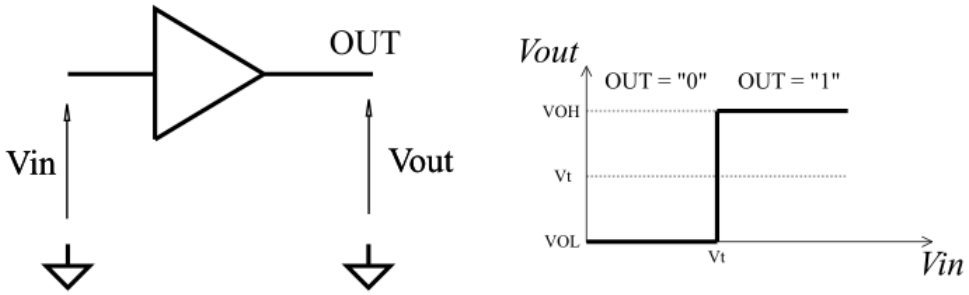


Figure 3.4: Ideal buffer behaviour

An ideal buffer can be interpreted as an one bit Analog to digital converter. The analog input (Vin) is converted into a logical “1” if its value is above the threshold (Vt) and viceversa. The circuit in Fig.[3.5] includes two digital buffers, it receives two analog inputs (V+, V-) and provides two bits digital output (OUT+, OUT-) according to the equations [3.2].

$$\begin{aligned} V+ > Vt &\Longrightarrow OUT+ = 1 \\ V+ < Vt &\Longrightarrow OUT+ = 0 \\ V- > Vt &\Longrightarrow OUT- = 1 \\ V- < Vt &\Longrightarrow OUT- = 0 \end{aligned} \tag{3.2}$$

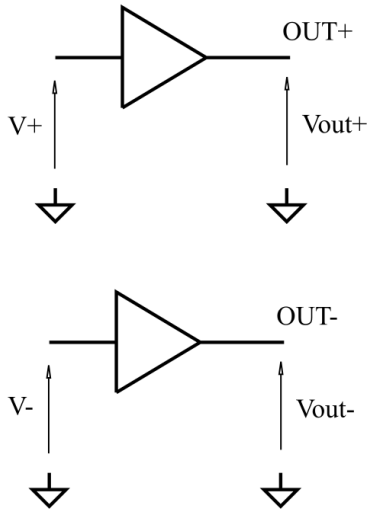


Figure 3.5: A pair of single-ended digital buffers as a digital differential stage

Since

$$V_d = V_+ - V_- \tag{3.3}$$

$$V_{cmd} = \frac{V_+ + V_-}{2} \tag{3.4}$$

$$(OUT+, OUT-) = OUT \tag{3.5}$$

it follows that

$$\begin{aligned} OUT = (1,0) &\Longrightarrow v_d > 0 \\ OUT = (0,1) &\Longrightarrow v_d < 0 \end{aligned} \tag{3.6}$$

$$\begin{aligned} OUT = (1,1) &\Longrightarrow v_{cmd} > V_t \\ OUT = (0,0) &\Longrightarrow v_{cmd} < V_t \end{aligned} \tag{3.7}$$

According to the equations [3.6], the circuit acts as a differential amplifier with a digital output (OUT) if the assertion $(OUT+) \oplus (OUT-)$ is true. Otherwise, the digital output is no related to the Differential mode input voltage, however, it is related to the Common mode input voltage according to the equations [3.7].

The equations [3.7][3.6] can be summarized as shown in Fig.[3.6].

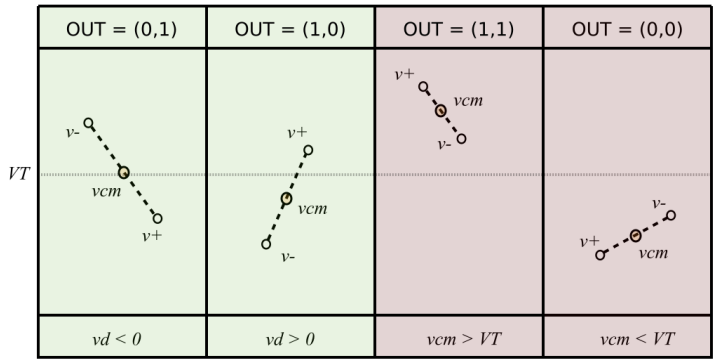


Figure 3.6: Digital output table

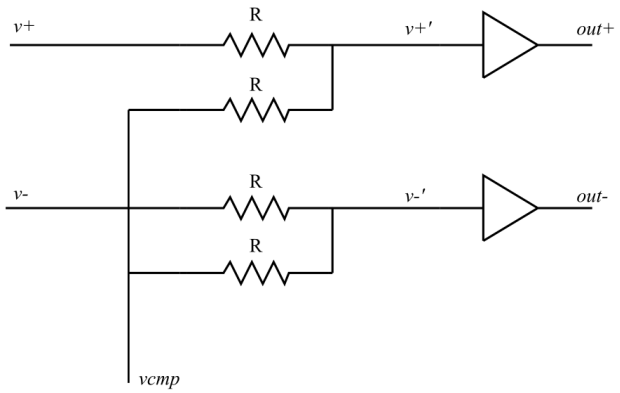


Figure 3.7: Summing network

The circuit can be modified in order to reject the CM input voltage by adding a negative feedback path. The summing network in Fig.[3.7] allows to add a compensation voltage to the external inputs.
It follows that the equation [3.8] can be written.

$$v^{+\prime} = \frac{v^{+} + v_{cmp}}{2} \qquad v^{-\prime} = \frac{v^{-} + v_{cmp}}{2} \tag{3.8}$$

The digital output signal drives two look up tables (Look-up table) called "DM LUT" and "CM LUT". If the CM input voltage value is close to the value of the inverters threshold, the DM LUT drives M3 and M4 according to the differential content of the signals. If the Common mode input voltage value is higher or lower then the threshold, the CM LUT drives M1 and M2 resulting in a negative feedback. For example, if the CM is higher then the threshold, the CM Look-up table turns on M2, causing the discharge of "Ccm" capacitor and the lowering of the CM input voltage of the buffers.

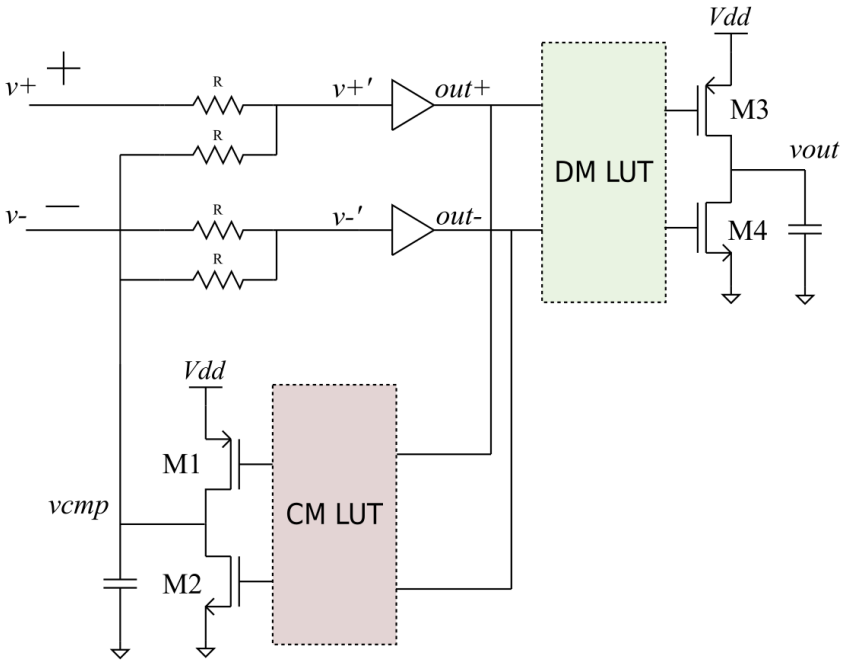


Figure 3.8: Digital differential circuit

The behaviour of the circuit in figure [3.8] can be summarized in the table [3.1]

OUT		CM LUT		DM LUT	
out+	out-	M1	M2	M3	M4
0	0	OFF	ON	OFF	OFF
1	1	ON	OFF	OFF	OFF
1	0	OFF	OFF	ON	OFF
0	1	OFF	OFF	OFF	ON

Table 3.1: Look-up tables behaviour

3.3.2 Behavioural simulation

In this subsection a MATLAB high level simulation is presented to better explain the behaviour of the Digital operational transconductance amplifier. In the first place, buffer and transistor models used for the simulation are de-

scribed. Finally, the open loop and voltage follower behavioural simulations are explained.

Buffers

The buffers are modeled as ideal comparators, the output is equal to $1V$, if the input voltage is greater then the threshold voltage (V_t). Otherwise, the output is $0V$. The following simulations are based on $V_t = 0.5V$.

Transistors

The transistors M1, M2, M3 and M4 in figure [3.8] are modeled as ideal switches providing a constant current in ON state and act as an open circuits in OFF state. Therefore, the output and the compensation voltages increase/decrease linearly in time during the operation.

Open loop operation

The input signals are defined as in equation [3.9] to simulate the open loop behaviour.

$$v^+(t) = 0.4[1 + sin(4\pi t)] \quad [V] \qquad\qquad v^- = 0.6 \quad [V] \tag{3.9}$$

In the figure [3.9] the waveforms are shown. The output voltage is high when the Differential mode input is positive and low when the Differential mode is negative. When the signals $OUT+$ and $OUT-$ are both high or low the compensation signal voltage (v_{cmp}) increase or decrease to compensate the input Common mode. In this particular case the compensation signal assume a quasi-constant value because one of the input is constant.

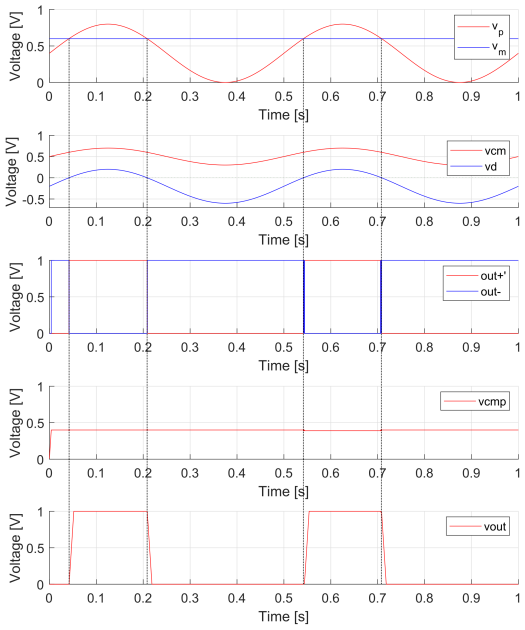


Figure 3.9: Open loop operation

Voltage follower operation

The close loop voltage follower operation is characterised by the fact that the output voltage is the same of the inverting input, this results in an internal oscillating behaviour. This occurs because $v+$ is varying, the voltage v_{cmp} must be modified time by time so the circuit oscillates between the Common mode compensation mode and output driving mode. The submitted results are evaluated according to the equation [3.10].

$$v^+(t) = 0.4[1 + sin(4\pi t)] \quad [V] \qquad\qquad v^-(t) = v_{out}(t) \tag{3.10}$$

In the figure [3.10] the waveforms are shown.

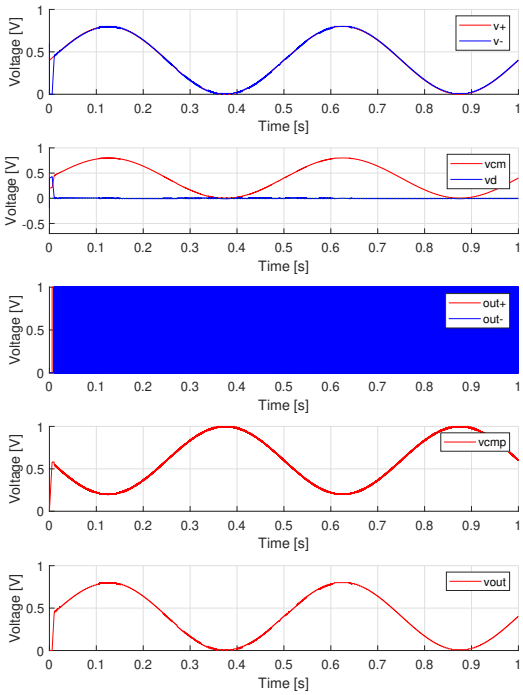


Figure 3.10: Close loop operation

The output voltage correctly follows the input. The signal v_d is the difference between the input and the output, it represent the tracking error that should be ideally null. The compensation signal v_{cmp} results to be the mirrored signal of the Common mode input signal with respect to the threshold voltage.

3.3.3 CMOS implementations

This subsection reviews two implementation of the concept in CMOS technology presented in [21] and [22].

DB-OTA with passive summing network The circuit proposed in [21] has been realized in 180nm CMOS technology. The supply voltage of $V_{dd} = 300mV$ has been selected to be compatible with the Minimum Energy Point (MEP) of the target technology [23]. The output stage has been designed to drive a maximum load of $C_L = 80pF$. The schematic is shown in Fig. [3.11].

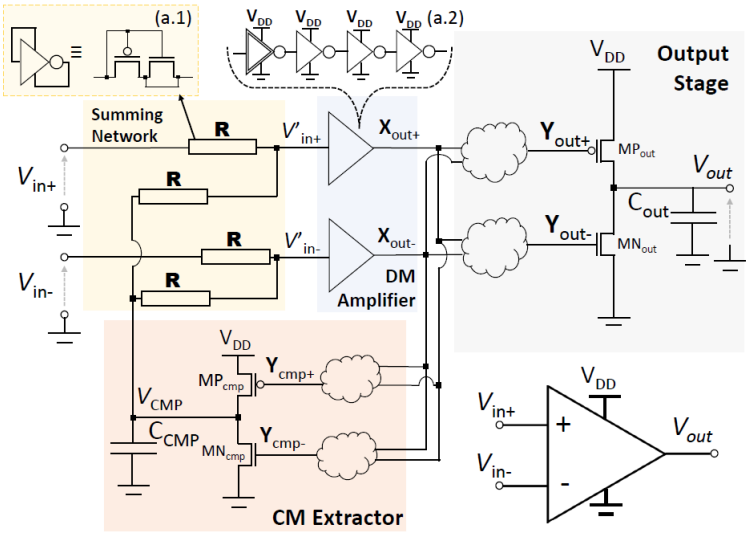


Figure 3.11: DB-OTA schematic

There are two critical parts of the circuit: the summing circuit and the differential mode (DM) amplifier. The summing circuit has been implemented using inverter-based pseudo-resistors, for which large-sized PMOS transistors have been employed to achieve good matching. The DM amplifier has been implemented with a calibration network to reduce VT mismatch and decrease the input offset.

The simulation results are shown in table [3.2]. The performance was obtained from post-layout simulations of the circuit. With this circuit, it has been demonstrated how this topology benefits from technology scaling due to the prevalence of digital elements. However, the main limitations are the presence of a passive summing network and the need for calibration.

DB-OTA based on Muller-C element The proposed schematic in [22] was aimed to replace the passive input network and eliminate the calibration process, which has increased silicon area consumption. The Muller-C logic element has been used to replace the input stage, and to compensate the common-mode effect without requiring any calibration.

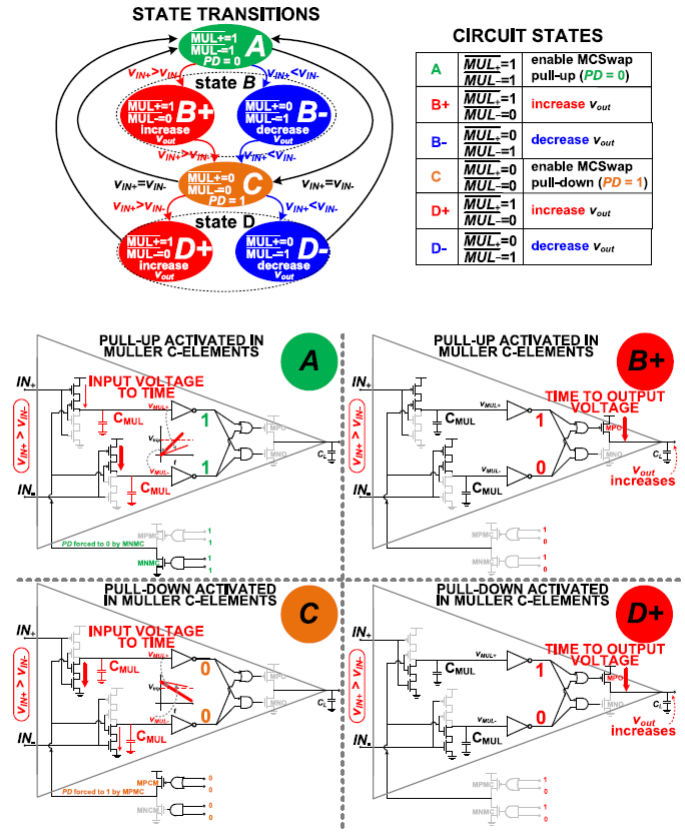


Figure 3.12: State-transition diagram and transistor-level detail for each state

Another advantage is that no-bias currents are needed for the passive elements, ensuring higher efficiency. The schematic in Fig.[3.12] illustrats the circuit diagram and the transition stage diagram. The performance has been evaluated through measurements on a fabricated test chip, and the results are shown in Table [3.2].

Performance	**DB-OTA** [21]	**DB-OTA (Muller-C)** [22]	**Unit**
Technology	180	180	nm
Supply Voltage	0.3	0.3	V
DC Gain	35	30	dB
GBW	0.850	0.250	kHz
Slew Rate	0.5	0.085	V/ms
THD	3	2	%
Phase Margin	76	90	^{O}
C Load	80	150	pF
Power	2	2.4	nW
Area	1426	982	μm^2
FOMs	34	15.6	$\frac{MHz \cdot pF}{\mu W}$
FOMl	20	5.3	$\frac{V \cdot pF}{\mu s \cdot \mu W}$

Table 3.2: Summary of the performances

Chapter 4

Floating-inverter digital OTA

This chapter presents the structure of CMOS Dynamically Biased integration pre-amplifier proposed in the article [24], and how this topology is implemented to control the common mode of DIGOTA.

4.1 DB inverter amplifier structure

The circuit considered in the thesis, is represented in figure [4.1]. It behaves as a differential-mode integrator, with the particularity that the input pair is powered by two tail capacitors.

The structure works in two phases: the reset phase and the integration phase. During the reset phase, the tail capacitors are completely discharged, it follows the integration phase, where the bottom node voltage ($Vs-$) increases. On the contrary, the upper one ($Vs+$) decreases.

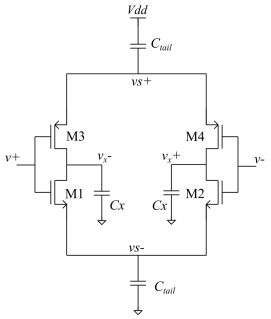


Figure 4.1: CMOS DB Pre-Amplifier

4.1.1 DB inverter amplifier as common mode control circuit

Resistive model of CMOS complementary inverter

To explain how this structure has been used for controlling the common input mode of the DIGOTA, a behavioral model has been created.

First, the behavior of the CMOS inverter has been approximated using two variable resistors. For clarity, this model with its static characteristic is described in Fig. [4.2], [4.3].

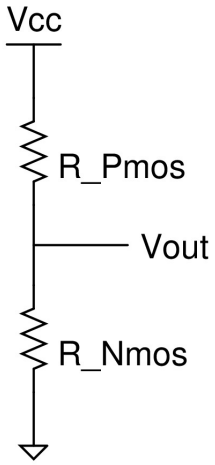


Figure 4.2: Resistive complementary CMOS inverter model

The analytical description has been provided by the Eq.[4.1],[4.2],[4.3].

$$R_{Pmos} = R_{min} + 10^{6(V_{in}-0.5)+3} \tag{4.1}$$

$$R_{Nmos} = R_{min} + 10^{6(0.5-V_{in})+3} \tag{4.2}$$

$$V_{out} = \frac{R_{Nmos}}{R_{Nmos} + R_{Pmos}} V_{cc} \tag{4.3}$$

If $V_{cc} = 1V$:

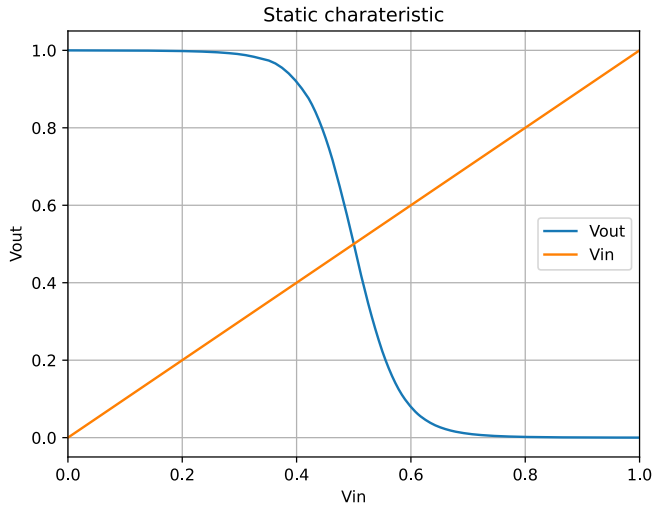


Figure 4.3: Static charateristic of the model

Output resistance is $R_{Pmos}||R_{Nmos}$:

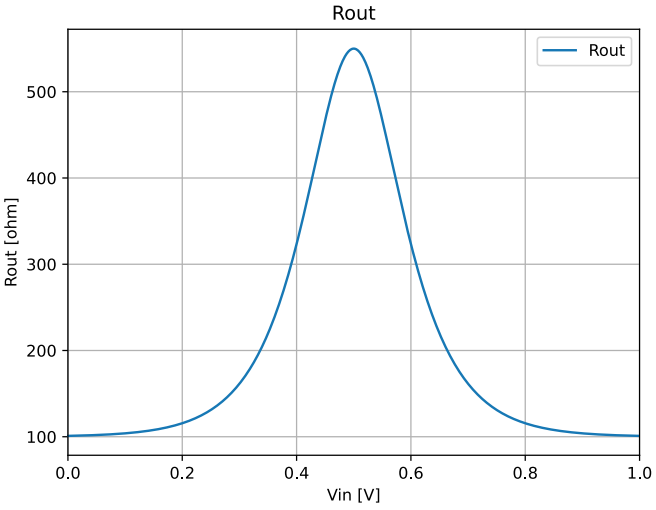


Figure 4.4: Output resistance

Beahvioural model of DIGOTA with FI

The floating inverter structure with resistive model is shown in the Fig.[4.5]. The value of the capacitance has been set to $10pF$ for all the capacitors in the schematic.

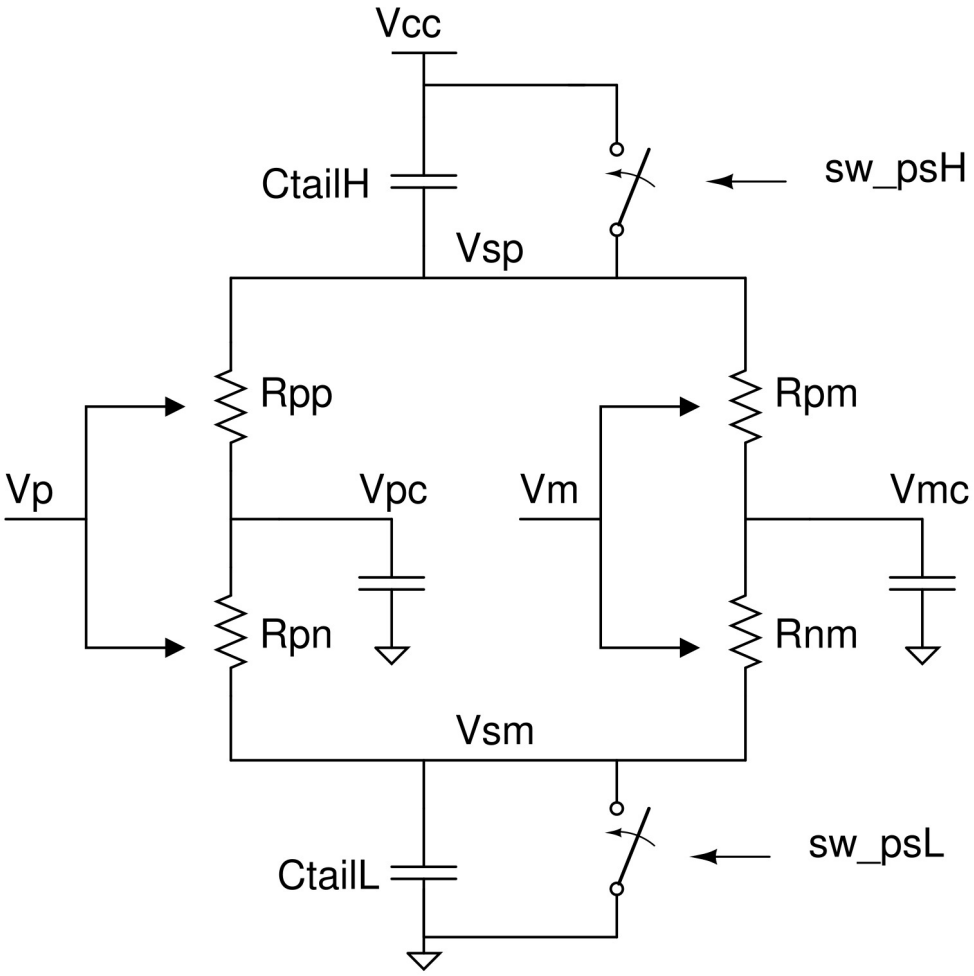


Figure 4.5: Floating inverter with resistive inverter model

The Eq. [4.4], [4.5] represent the input for the DIGOTA structure.

$$VOUT_{diff} = V_{pc} - V_{mc} \tag{4.4}$$

$$VOUT_{cmd} = \frac{V_{pc} + V_{mc}}{2} \tag{4.5}$$

To obtain the behavior of the DIGOTA, its logic has been implemented at a behavioral level, as depicted in Figure [4.6]. The gates represent a logic high value when the voltage is 1V and a logic low value when the voltage is 0V. The threshold voltage (Vth) is 0.5V. To model the logic delay, the output signals "outp" and "outm" are generated with a delay of 4ns relative to the input signals "vpc" and "vmc".

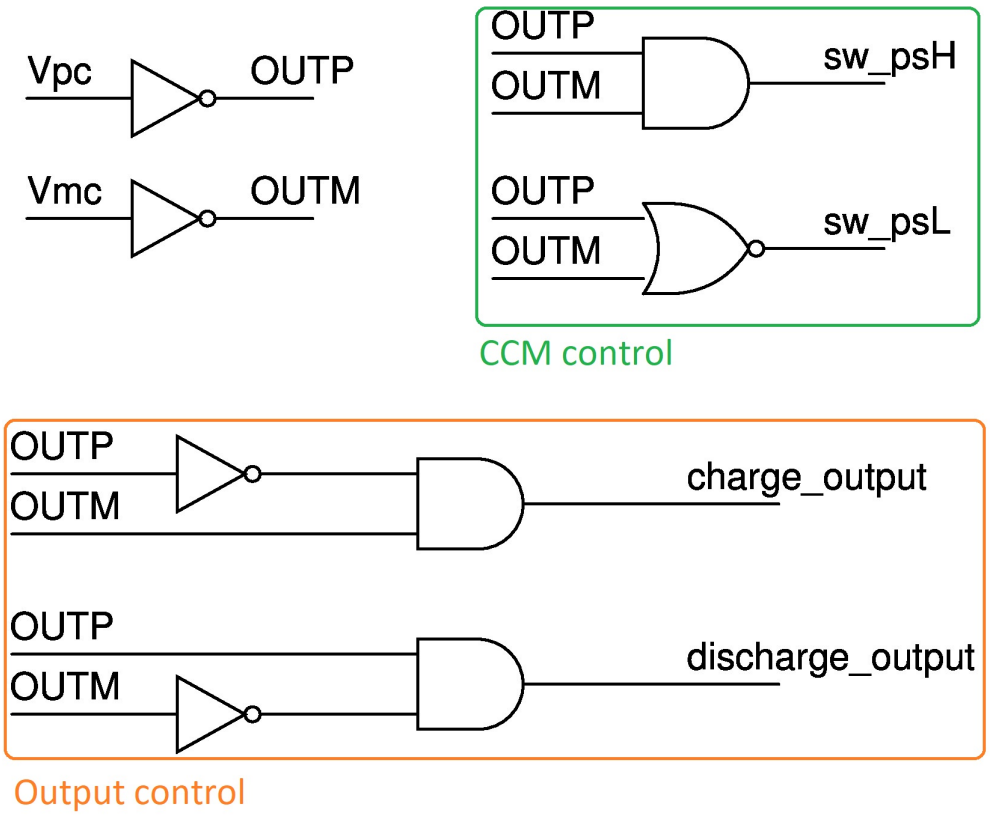


Figure 4.6: DIGOTA logic used for the beahvioural model

When $V_p = V_m$, the charging/discharging speed of the Vpc and Vmc nodes is identical because the integration time constants (τ) are equal. If the inputs have a low value ($V_p < Vth$ and $V_n < Vth$), the output capacitors are charged very quickly because $Rpp << Rpn$ and $Rpm << Rnm$. Conversely, they will discharge much more slowly. The common mode of the output is controlled by the switches Sw_{psH} and Sw_{psL} according to the logic shown in Figure [4.6]. Under these input conditions, the circuit does not produce any modulation for output control. An example in Fig.[4.7].

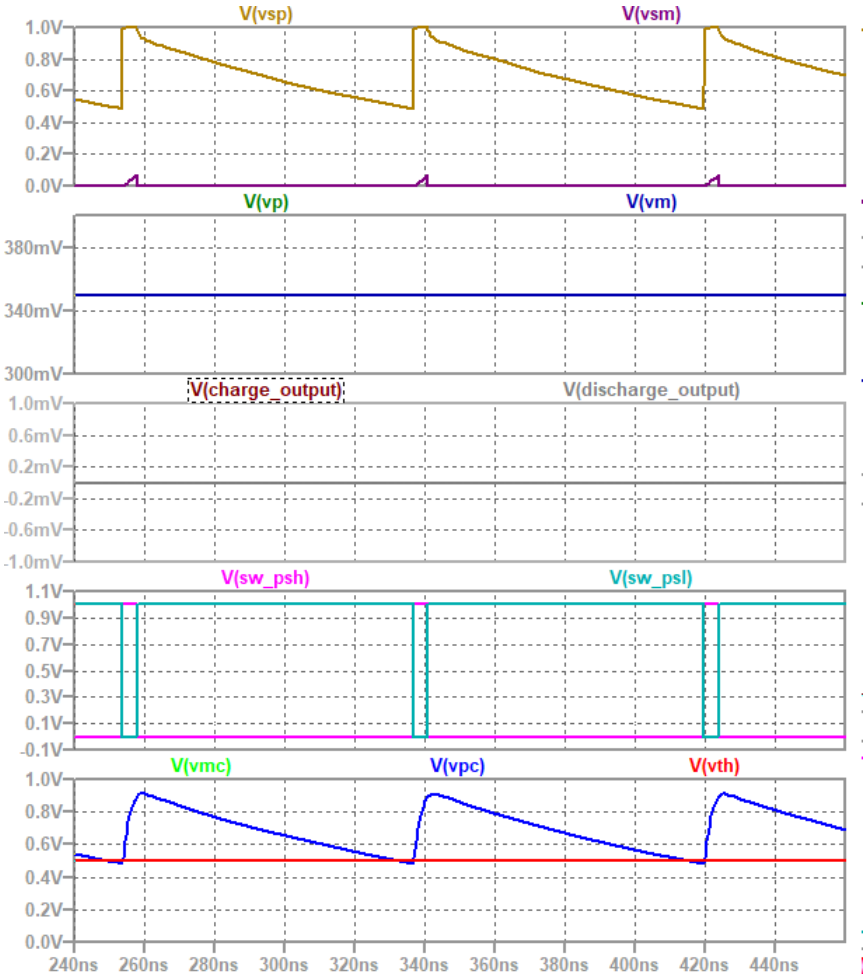


Figure 4.7: An example of behaviour when Vp=Vm=0.35

When $V_p \neq V_m$, the circuit does not behave symmetrically, and the different integration time constants (τ) result in pulse width modulation of the outputs OUTP and OUTM. It can be shown that the difference in duty cycle of the outputs depends on the voltage difference between the input nodes. If $V_p > V_m$, pulses are generated on the charge_output signal, whereas pulses are generated on the discharge_output signal when $V_p < V_m$. The two examples in Figures [4.8] and [4.9].

For $V_p < Vth$ AND $V_m < Vth$:

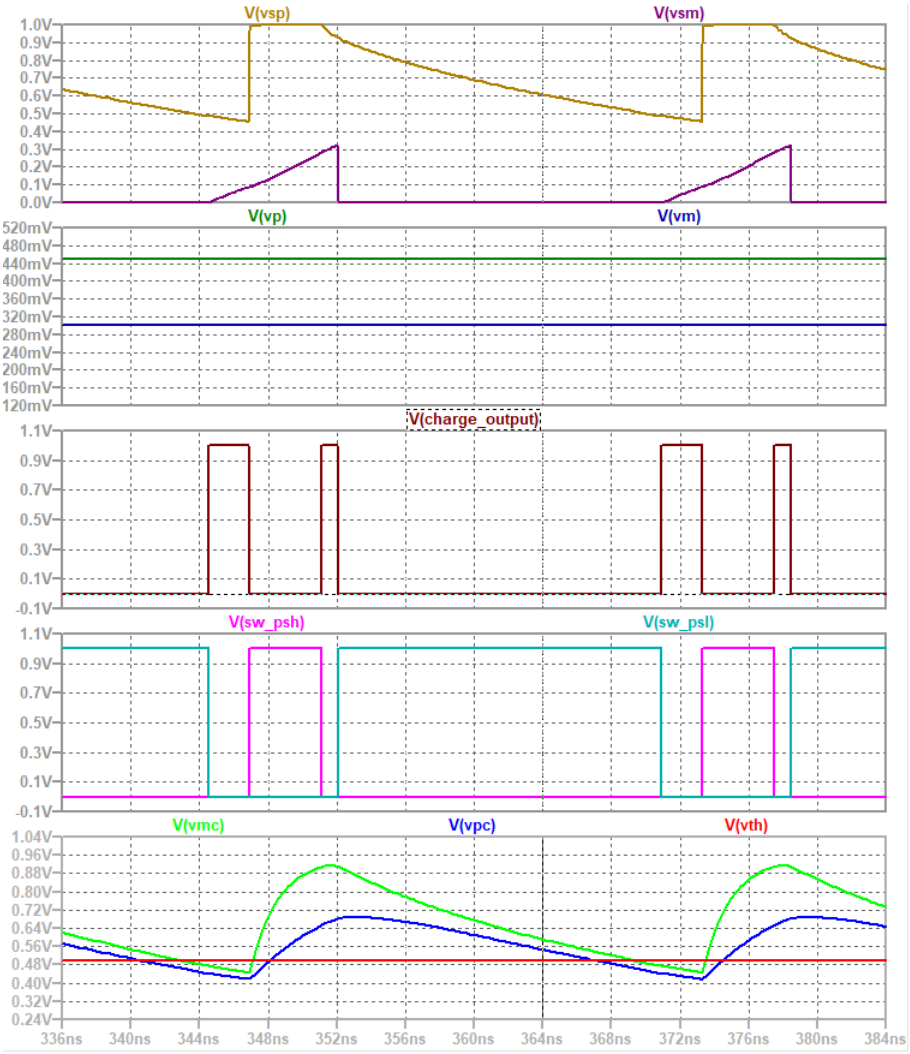


Figure 4.8: An example of behaviour

For $V_p > Vth$ AND $V_m > Vth$:

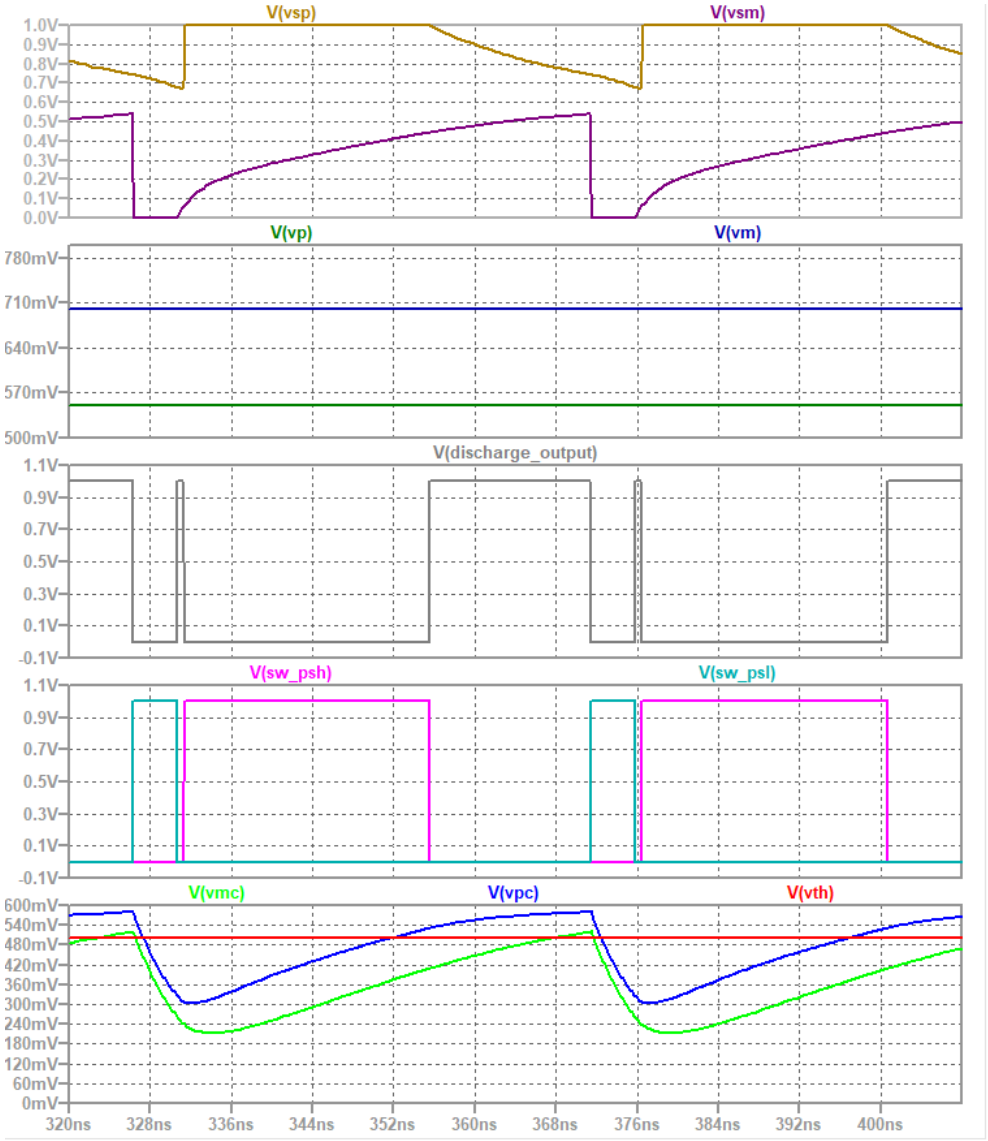


Figure 4.9: An example of behaviour

With the simulated and described results in Figures [4.8] and [4.9], it has been demonstrated how it is possible to produce a differential output despite V_p, V_m being greater than Vth or V_p, V_m being less than Vth.

4.2 Design

4.2.1 Functional blocks

The amplifier is made by the following macro-blocks:

- Input blocks
- Common mode control circuit
- Output driver

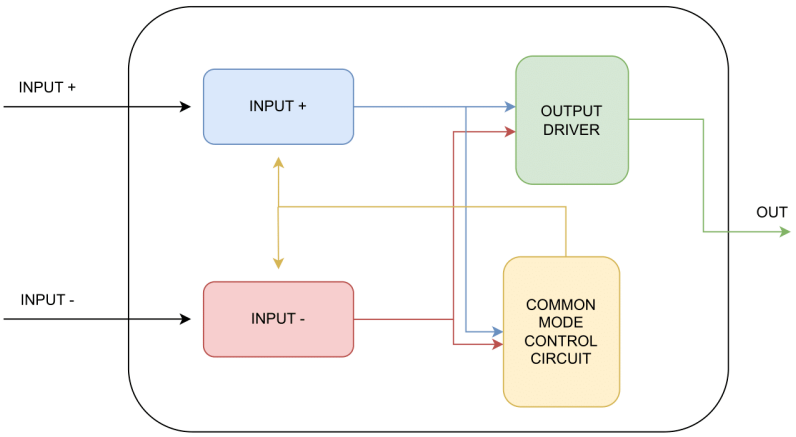


Figure 4.10: Architecture

4.2.2 Input blocks

The input blocks are composed by a chain of inverters. The first one is the floating inverter, this feature permits to adjust the input common mode. The second one is designed to have a threshold equals to half vdd.

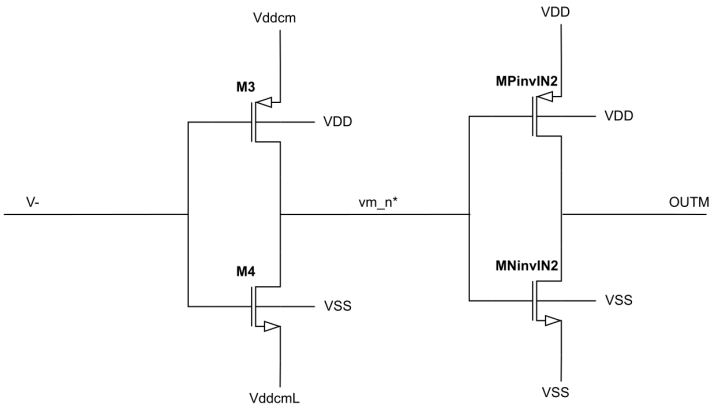


Figure 4.11: Floating inverter (minus-input)

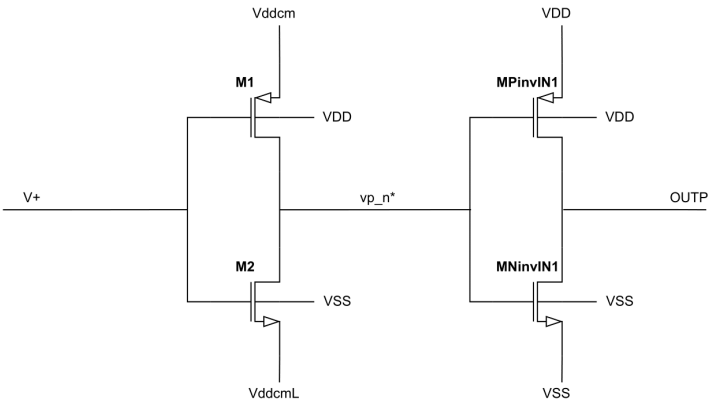


Figure 4.12: Floating inverter (plus-input)

4.2.3 Common mode control circuit

The circuit provides the supply voltage for the floating inverters. This circuit implements the control logic for the input common mode according to the

truth table [3.1].

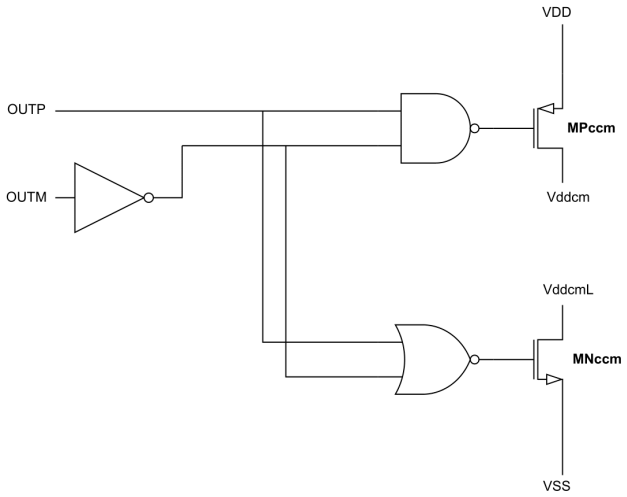


Figure 4.13: The circuit that controls the input common mode

4.2.4 Output driver

The circuit implements the logic described in [3.1] to drive the output capacitance. It is basically a tristate buffer.

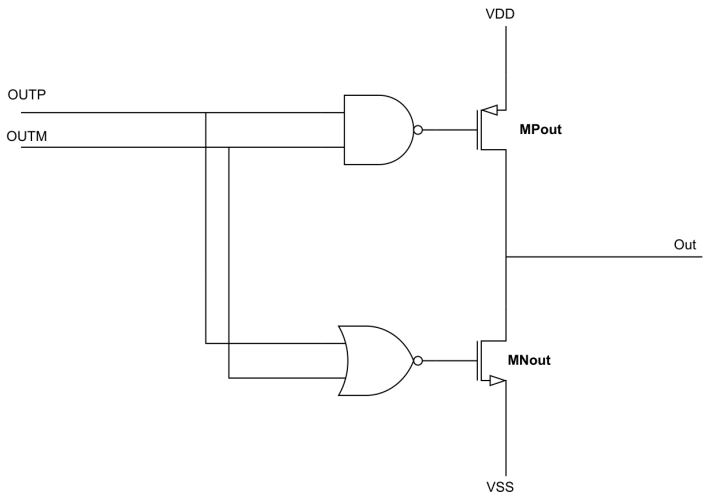


Figure 4.14: The circuit that controls the output node

4.2.5 Sizing and design component values

Tail and output capacitances of the FI have not been added. The simulated capacitance has been intrinsic to the system nodes. The output buffer is designed to charge a $10pF$ output node. The transistors' aspect ratios are reported in [4.1]:

	W (um)	L (um)
M1/M3	10	0.18
M2/M4	10	0.18
MPccm	10	0.18
MNccm	1	0.18
MPout	0.80	0.18
MNout	0.25	1.25
MPinvIN	3.5	0.18
MNinvIN	0.25	0.35

Table 4.1: Transistors sizing

4.2.6 Example of operation

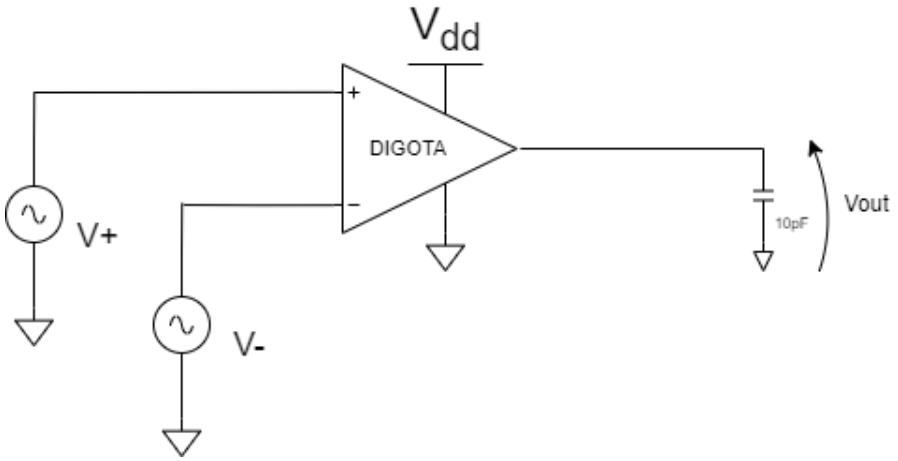


Figure 4.15: Testbench example of operation

In this example the op-amp has been arranged in open-loop configuration without the feedback net. The terminals have been set to:

- $V_{dd} = 0.4V$
- $v_+ = 0.40 \cdot V_{dd}$
- $v_+ = 0.39 \cdot V_{dd}$
- Output node v_{out} connected to a $C_L = 10pF$

In this condition the C_L is expected to be loaded up to V_{dd} by the op-amp, because $v_+ > v_-$.

At the beginning the $OUTP$ and $OUTM$ node voltages are $0V$ because $v_+, v_- < VT = V_{dd}/2$. The common mode control circuit shown in [4.2.3] loads the supply capacitance of the floating inverters. This makes possible to compare the output of these last with the next buffer. It has the threshold voltage equal to $V_{dd}/2$. What happens is that the delays of the circuit causes the internal nodes vn_p^*, vn_n^* to be loaded more then needed and the circuit jumps to a condition where $OUTP$ and $OUTM$ are equals to V_{dd} and the common mode control circuit acts in an opposite way. The results is that the overall circuit keeps oscillating between this two conditions.

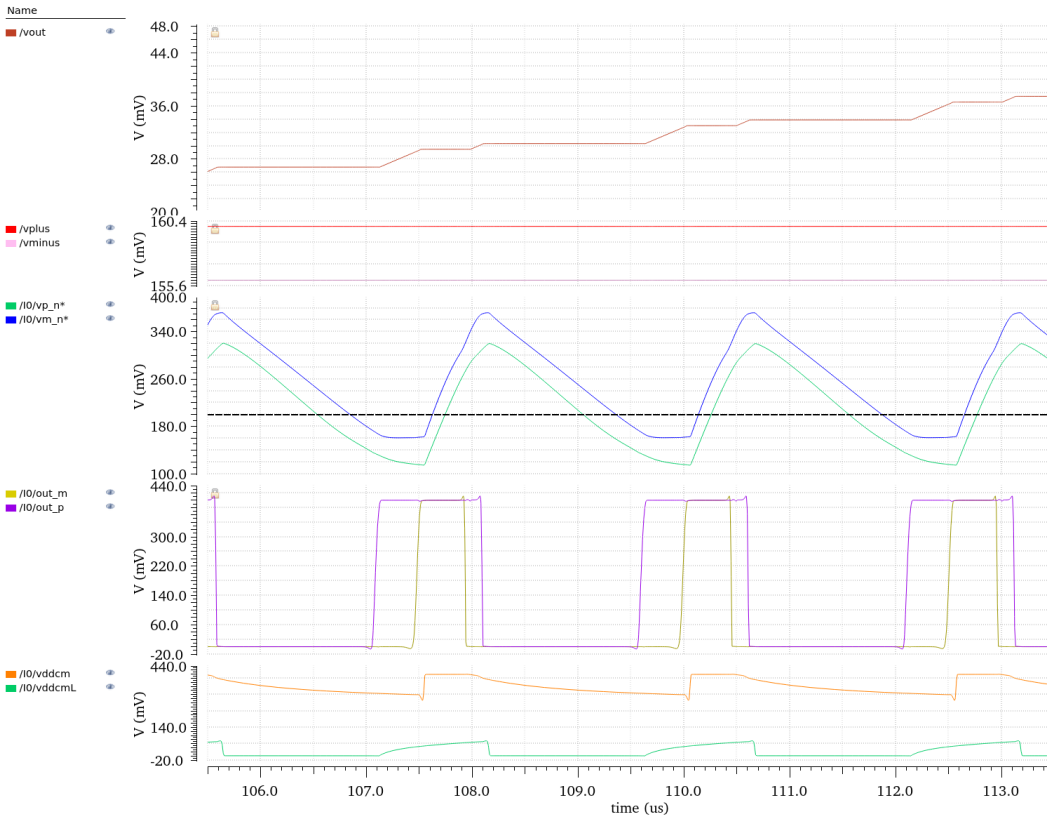


Figure 4.16: Waveform

The figure demonstrates the oscillatory behavior of the system. It can be observed that in each cycle, the load capacitance is charged by the output buffer. This occurs because during the transition, the loading of the FI output by the common-mode compensation stage happens asymmetrically due to the disparity of the input signals. The charging and discharging time of the two nodes are different. This behavior gives rise to the characteristic signal modulation of the digota.

4.3 Schematic simulations

Several parameters are evaluated with the testbench in figure [4.17].

4.3.1 Testbench for evaluating the frequency response

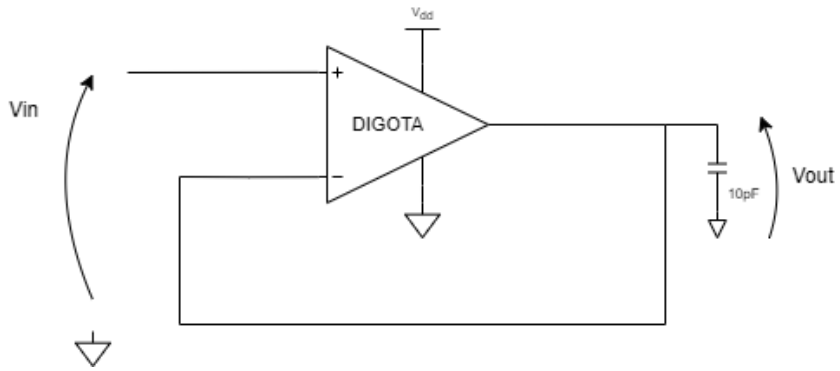


Figure 4.17: Testbench

$$V_{in}(t) = \frac{V_{cc}}{2} + \frac{V_{pp}}{2} Sin(2\pi f_{in} t) \tag{4.6}$$

$$v_d(t) = V_{in}(t) - V_{out}(t) \tag{4.7}$$

By varying f_{in} is possible to obtain the transfer function of the amplifier evaluating the ratio [4.12].

$$A_{ol} = \frac{V_{out}(t) - \frac{V_{cc}}{2}}{v_d(t)} \tag{4.8}$$

The frequency response of the Device under test has been evaluated in transient analysis performing the Fast Fourier transform of [4.6] and [4.7], the ratio is calculated in magnitude and phase.

$$V_{in}(t) \quad \xrightarrow{FFT} \quad Vin(f) \tag{4.9}$$

$$V_{out}(t) \quad \xrightarrow{FFT} \quad V_{out}(f) \tag{4.10}$$

$$v_d(t) = V_{in}(t) - V_{out}(t) \quad \xrightarrow{FFT} \quad Vd(f) \tag{4.11}$$

$$A_{ol} = \frac{V_{out}(f_{in})}{V_d(f_{in})} \tag{4.12}$$

The magnitude and phase of [4.12] has been calculated for different value of V_{pp} of the input signal V_{in}.

4.3.2 Results

Thanks to this testbench the DC gain, GBW and the PM have been evaluated.

DC gain

The maximum DC gain is $44.55dB$ ($168.85\frac{V}{V}$) reported in table [4.4], it has been obtained $@V_{pp} = 250mV, \quad f_{in} = 10Hz$.

GBW and Phase margin

The value of GBW is $43kHz$, it has been measured $@V_{pp} = 10mV$. The phase margin has been evaluated as $PM = \angle A_{ol}(GBW) + 180° = 110°$.

4.3.2.1 Transfer function ($@V_{pp} = 10mV$)

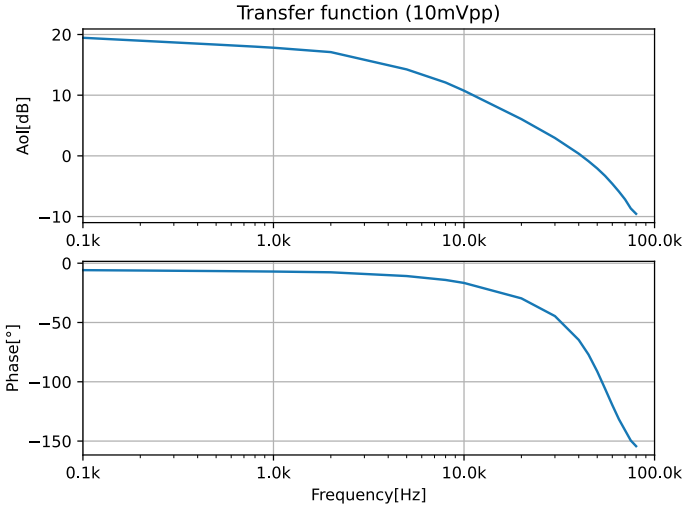


Figure 4.18: Transfer function ($@V_{pp} = 10mV$)

Frequency[Hz]	**Aol[dB]**	**Phase[°]**
100	19.46	-5.85
200	18.98	-6.17
500	18.34	-6.63
800	18	-6.898
1000	17.82	-7.04
2000	17.1	-7.66
5000	14.25	-10.83
8000	12.09	-14.12
10000	10.74	-16.65
20000	6.057	-29.65
30000	2.95	-44.61
40000	0.358	-64.68
45000	-0.873	-77
50000	-2.07	-91.23
55000	-3.298	-105.9
60000	-4.598	-119.6
65000	-5.884	-131.6
70000	-7.17	-140.9
75000	-8.664	-149.5
80000	-9.549	-154.3

Table 4.2: Transfer function ($@V_{pp} = 10mV$) [Measured point]

4.3.2.2 Transfer function (@$V_{pp} = 100mV$)

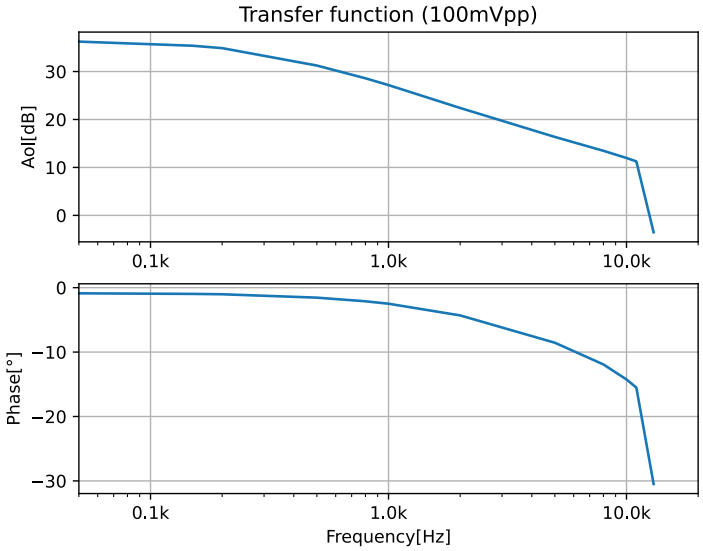


Figure 4.19: Transfer function (@$V_{pp} = 10mV$) [Measured point]

Frequency[Hz]	**Aol[dB]**	**Phase[°]**
50	36.24	-0.8785
150	35.38	-0.9689
200	34.88	-1.025
500	31.25	-1.55
800	28.59	-2.115
1000	27.17	-2.492
2000	22.4	-4.308
5000	16.36	-8.549
8000	13.47	-11.92
10000	11.97	-14.25
11000	11.26	-15.51
13000	-3.525	-30.48

Table 4.3: Transfer function (@$V_{pp} = 100mV$) [Measured point]

4.3.2.3 Transfer function (@$V_{pp} = 250mV$)

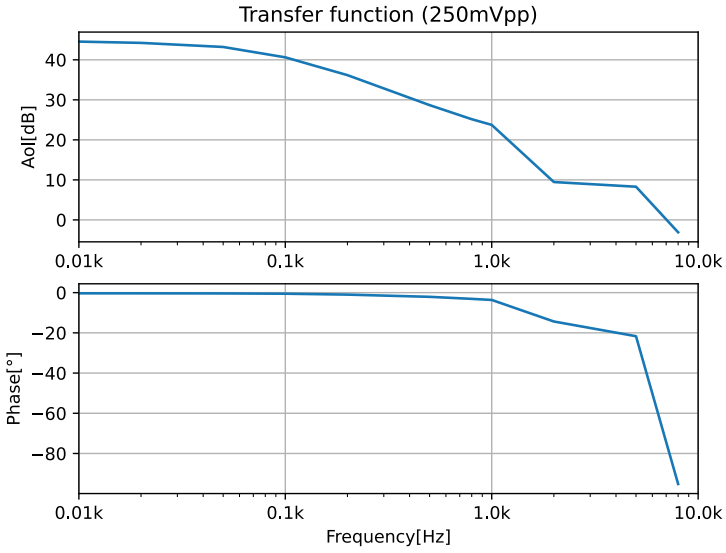


Figure 4.20: Transfer function (@$V_{pp} = 250mV$)

Frequency[Hz]	**Aol[dB]**	**Phase[°]**
10	44.55	-0.337
20	44.23	-0.3501
50	43.21	-0.3921
100	40.62	-0.532
200	36.17	-0.9808
500	28.68	-2.081
800	25.16	-3.094
1000	23.74	-3.632
2000	8.29	-21.67
5000	9.46	-14.35
8000	-3.097	-95.18

Table 4.4: Transfer function (@$V_{pp} = 250mV$) [Measured point]

4.3.2.4 Transfer function (@$V_{pp} = 300mV$)

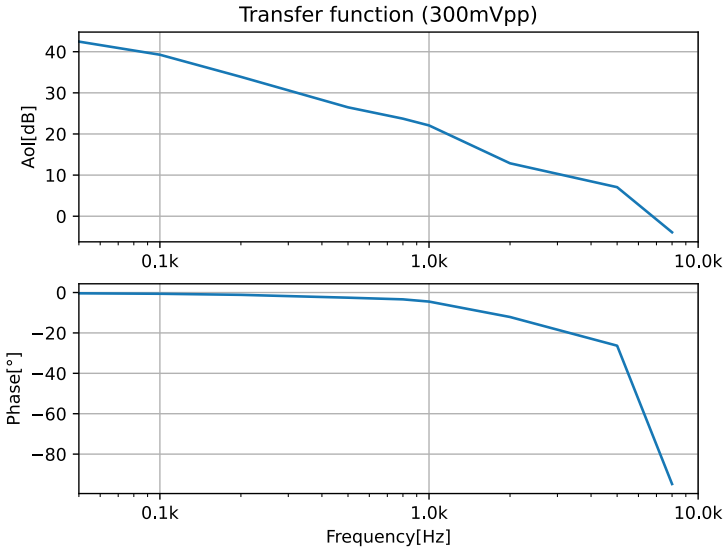


Figure 4.21: Transfer function (@$V_{pp} = 300mV$)

Frequency[Hz]	**Aol[dB]**	**Phase[°]**
50	42.46	-0.3922
100	39.27	-0.6118
200	33.89	-1.149
500	26.48	-2.551
800	23.72	-3.383
1000	22.08	-4.481
2000	12.87	-12.12
5000	7.063	-26.32
8000	-3.909	-94.8

Table 4.5: Transfer function (@$V_{pp} = 300mV$) [Measured point]

4.3.3 Testbench for evaluating the PSRR

PSRR

The supply noise has been set to $V_{noise} = \frac{V_{pp_{noise}}}{2} sin(2\pi ft)$ where $V_{pp_{noise}} = 40mV$. The nominal V_{dd} is equal to $400mV$.

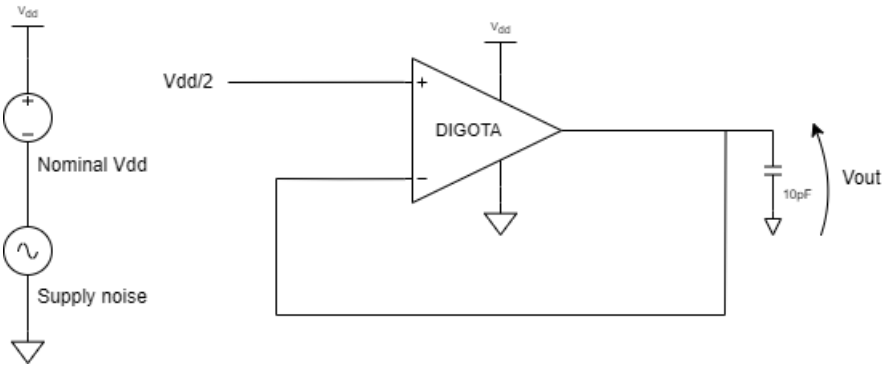


Figure 4.22: Testbench PSRR

The value of PSRR is higher then $38dB$ as shown in figure [4.23].

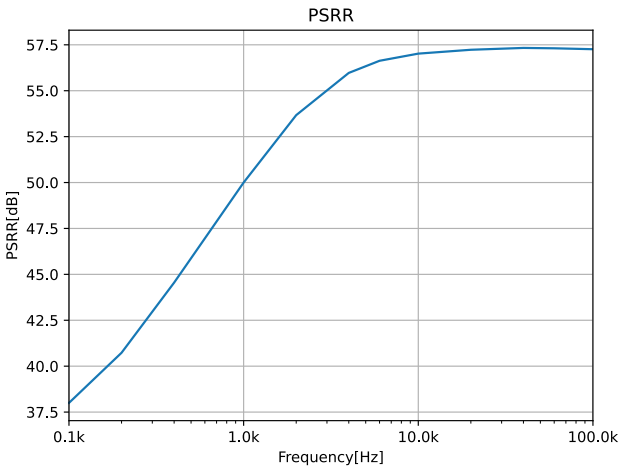


Figure 4.23: PSRR

4.3.4 Testbench for evaluating the Slew rate

Slew rate

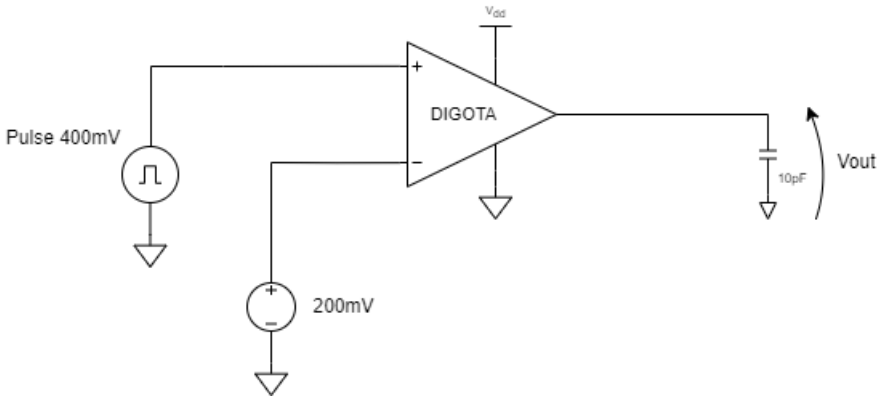


Figure 4.24: Testbench SR

Two value of SR have been obtained from this simulation:

- $SR+ = 6.131kV/s$
- $SR- = 7.114kV/s$

The mean of the two value is $SR = 6.623kV/s$.

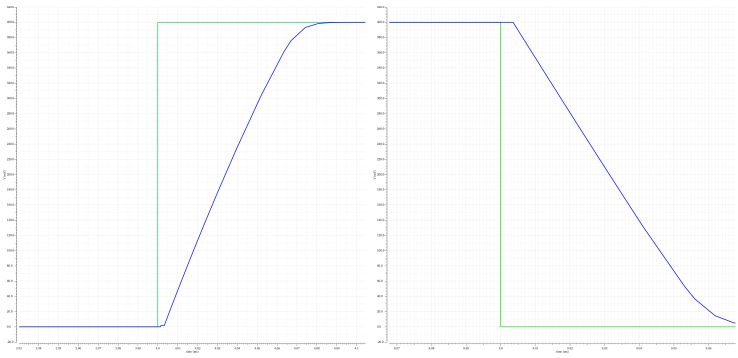


Figure 4.25: SR

4.3.5 Testbench for evaluating the CMRR

CMRR

The circuit is biased at 400mV, and the input stimulus signal is centered at the midpoint of the amplifier's dynamic range (Vdd/2).

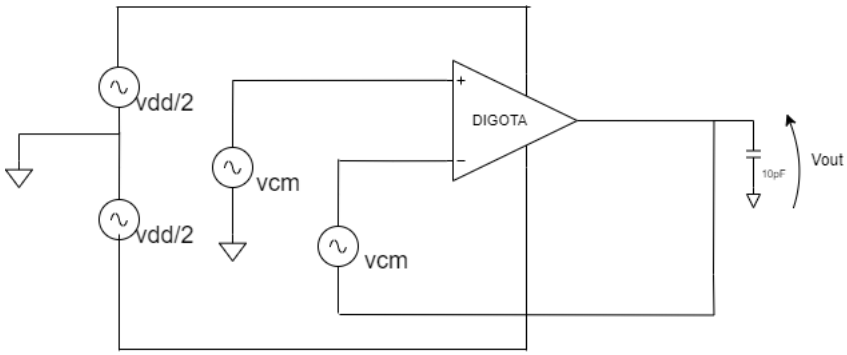


Figure 4.26: Testbench CMRR

The value of CMRR is greater then $41dB$. It has been measured at a frequency of 500Hz by varying the value of the common-mode amplitude.

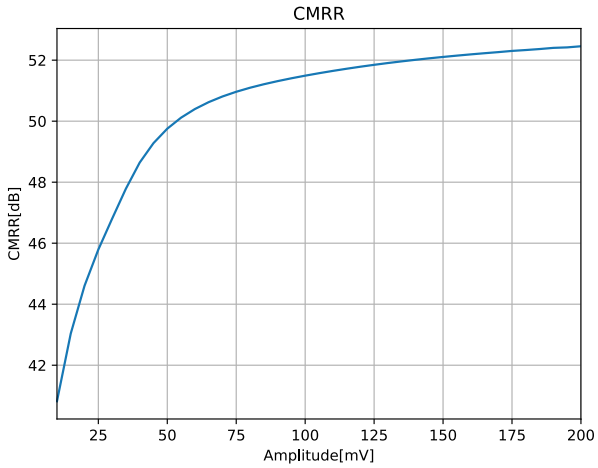


Figure 4.27: CMRR

4.3.6 Testbench for evaluating the THD

THD

The amplifier has been configured as a voltage follower and has been stimulated with a test signal.

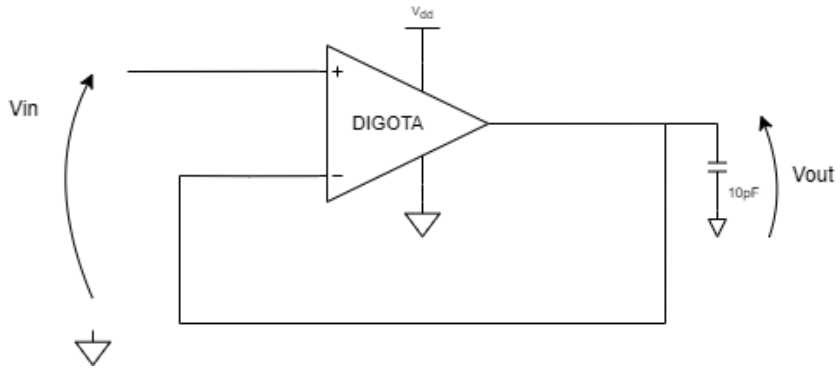


Figure 4.28: Testbench THD

By varying the frequency of the test signal, the THD curves of the output node have been plotted against the input signal amplitude.

4.3.6.1 Results

The mimimum measured THD value is 0.339%, observed at $20Hz$ with an input signal amplitude of $V_{pp} = 230mV$.

		Frequency			
	THD(%)	**20Hz**	**50Hz**	**100Hz**	**500Hz**
Amplitude Vpp (mV)	**10**	3.432	3.46	3.56	3.856
	30	1.813	1.912	1.992	2.21
	50	1.409	1.492	1.558	1.747
	70	1.036	1.099	1.148	1.358
	90	0.887	0.9402	0.977	1.285
	110	0.8164	0.8564	0.887	1.285
	130	0.6734	0.7015	0.7284	1.243
	150	0.5492	0.5689	0.593	1.255
	170	0.4583	0.4724	0.497	1.334
	190	0.3964	0.4082	0.437	1.477
	210	0.3571	0.3743	0.412	1.711
	230	0.3393	0.3639	0.416	2.076
	250	0.3404	0.3666	0.463	2.615
	270	0.3628	0.3861	0.5634	3.365
	290	0.4154	0.4644	0.7379	4.268
	310	0.4918	0.5905	1.027	5.306

Table 4.6: THD table

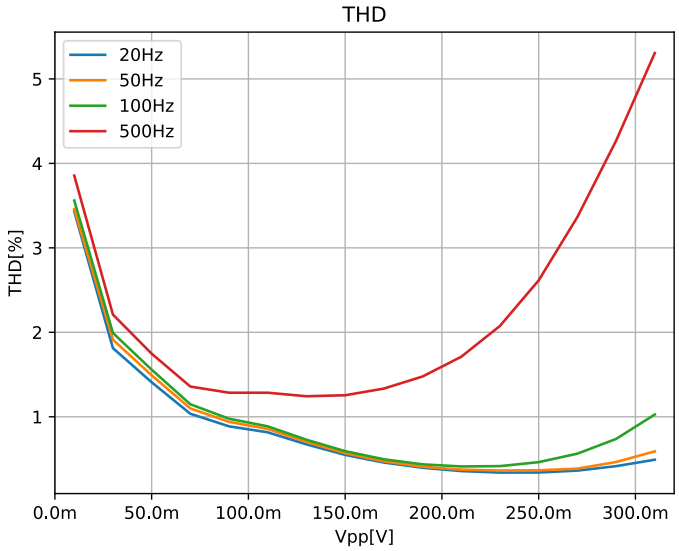


Figure 4.29: THD

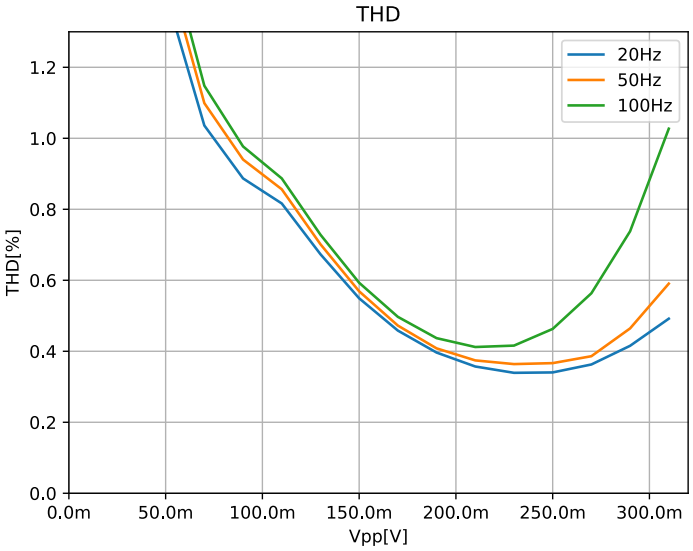


Figure 4.30: THD

4.3.7 Testbench for evaluating the power consumption

Power

The amplifier has had a sinusoidal input with a frequency of 100Hz. The absorbed current/power has been evaluated as a function of the input sinusoid amplitude.

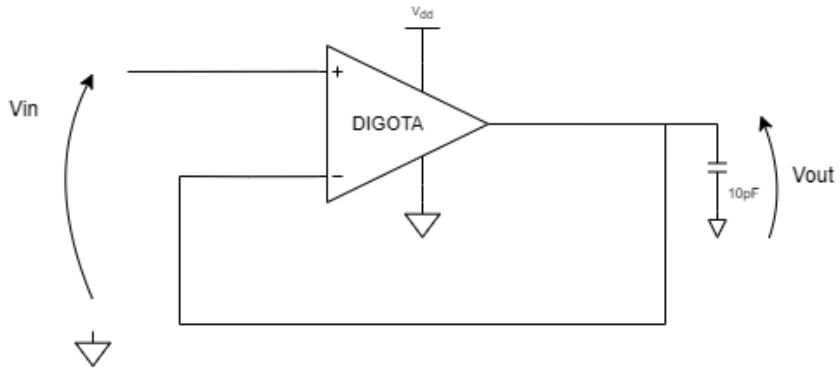


Figure 4.31: Testbench average power consumed

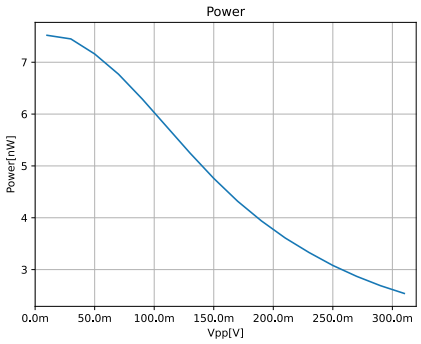


Figure 4.32: Power

The average value has been obtained as 4.83nW. It has been observed that the dissipated power is higher at the center of the dynamic range because the circuit's self-oscillation frequency is higher compared to the limit.

4.3.8 Figure of merits

The two figures of merit have been evaluated using the obtained results. The gbw has been achieved with an input signal amplitude of 10mVpp.

$$FOM_S = \frac{GBW \cdot C_L}{P_{diss}} = \frac{0.043MHz \cdot 10pF}{0.00483\mu W} = 89\left[\frac{MHz \cdot pF}{\mu W}\right] \tag{4.13}$$

$$FOM_L = \frac{SR \cdot C_L}{P_{diss}} = \frac{0.006623V/\mu s \cdot 10pF}{0.00483\mu W} = 15.11\left[\frac{V \cdot pF}{\mu s \cdot \mu W}\right] \tag{4.14}$$

4.3.9 Summary of simulations

The gbw has been achieved with an input signal amplitude of 10mVpp. The DC-gain has been obtained with an input signal amplitude of 250mVpp.

Supply Voltage [mV]	400
Load [pF]	10
Power [uW]	0.00483
DC gain [dB]	44.5
GBW [kHz]	43
Average SR [V/ms]	6.62
In-band input noise [uV]	23.55
CMRR [dB]	41
PSRR [dB]	38
THD [%]	0.34
FOMs [MHz pF / uW]	89
FOMl [(V/us) pF / uW]	15.1

4.4 Post-Layout simulations

Layout

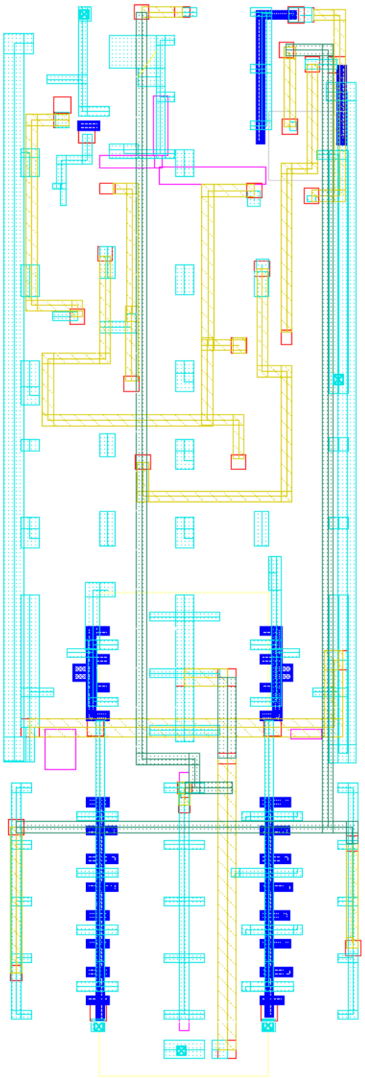


Figure 4.33: Floating-inverter DIGOTA Layout

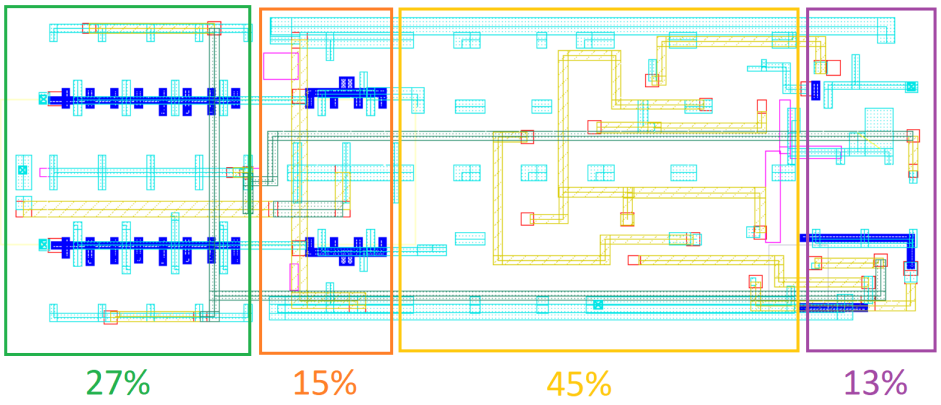


Figure 4.34: Floating-inverter DIGOTA Layout functional blocks

In figure [4.34] is reported the layout realization of the floating inverter DIGOTA. The total size is $270(\mu m)^2$ $(27\mu m \cdot 10\mu m)$. The green box contains the floating inverters, the orange one contains the input buffers, the yellow one contains the digital part and finally the purple one contains the tristate buffers for the output and the floating inverters supply.

4.4.1 Post-layout results

The post-layout simulation results have been obtained using the TSMC180 model libraries at room temperature, after passive parasitic extraction from the layout view.

Supply Voltage [mV]	400
Load [pF]	10
Power [uW]	0.00523
DC gain [dB]	42.5
GBW [kHz]	41
Average SR [V/ms]	6.46
In-band input noise [uV]	29.37
CMRR [dB]	39
PSRR [dB]	37
THD [%]	0.41
FOMs [MHz pF / uW]	78.4
FOMl [(V/us) pF / uW]	12.4

With the same testbench as before, the result has not changed significantly, likely due to the compact layout design where the influence of parasitic elements on the circuit behavior is minimal.

4.4.2 Montecarlo simulations

The parameters simulated with Monte Carlo simulations have differed from the values obtained with simulations of typical models. The component mismatch has significantly affected the functioning of the system. 100 statistical samples have been evaluated for each measured parameter. The histograms have represented only the samples that have turned out to be functional. For some combinations of component corners, the system has not self-oscillated.

4.4.2.1 DC gain distribution

The histogram in Fig. [4.35] shows the distribution of the DC gain for 86 out of 100 functional samples. The average DC gain is 35.3dB with a standard deviation of 5.4dB. The result demonstrates that the circuit is dependent on process variability.

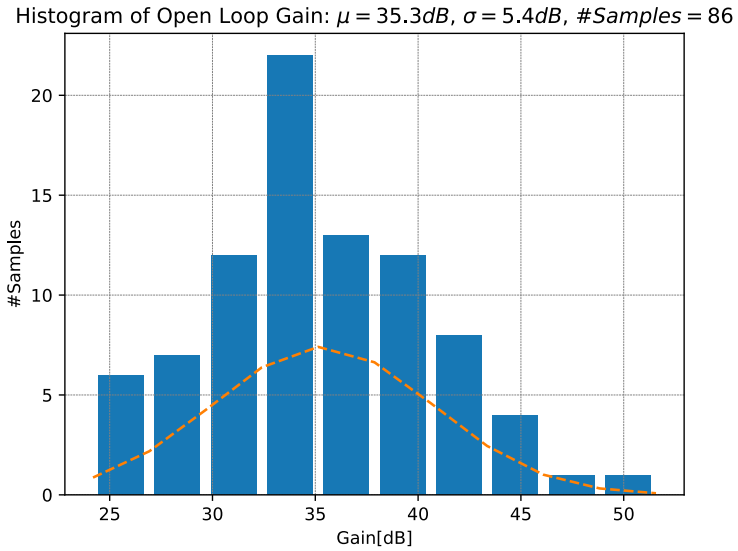


Figure 4.35: DC Gain distribution

4.4.2.2 THD distribution

The histogram in Fig. [4.36] shows the distribution of the THD for 86 out of 100 functional samples. The average THD is 1.3% with a standard deviation of 0.8%. In this case as well, the high value of sigma indicates a high dependence on process variability.

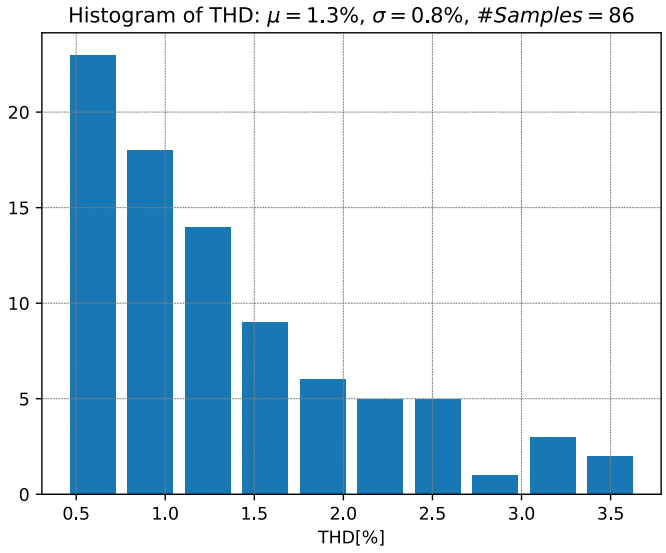


Figure 4.36: THD Distribution

4.4.2.3 Power distribution

The histogram in Fig. [4.37] shows the distribution of the Power dissipated for 86 out of 100 functional samples. The average is 3.5nW with a standard deviation of 0.2nW. In this case as well, the high value of sigma indicates a high dependence on process variability.

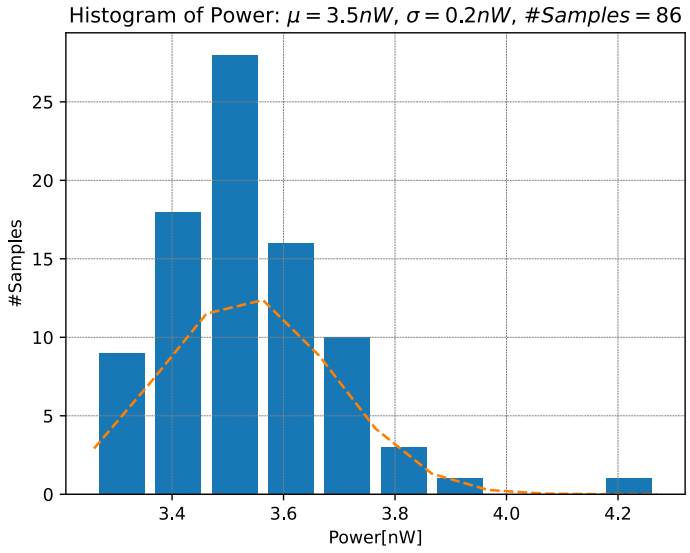


Figure 4.37: Power distribution

4.4.2.4 Voltage offset distribution

The histogram in Fig. [4.38] shows the distribution of the input voltage offset for 86 out of 100 functional samples. The average is 0.1mV with a standard deviation of 2.7mV.

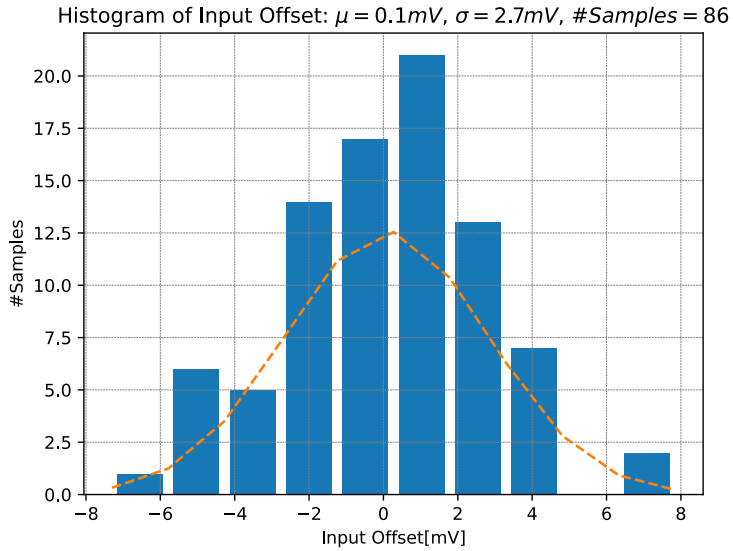


Figure 4.38: Input offset distribution

4.4.2.5 GBW distribution

The histogram in Fig. [4.39] shows the distribution of the slew rate for 100 functional samples. The average is $36.3kHz$ with a standard deviation of $12.6kHz$.

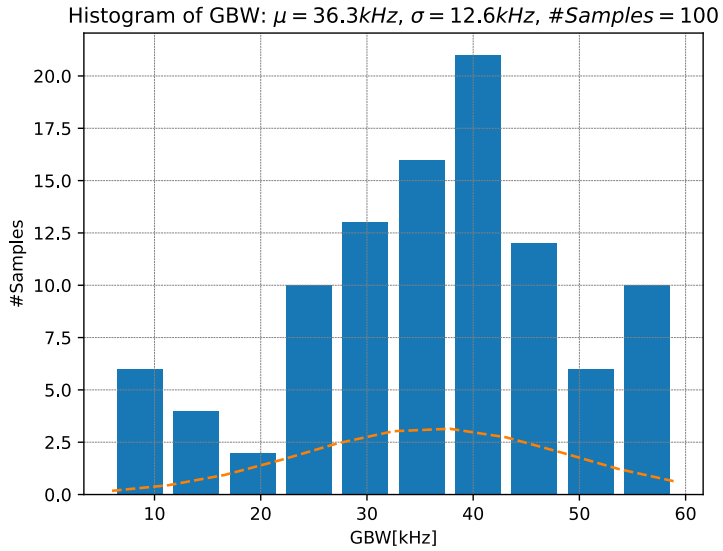


Figure 4.39: GBW distribution

4.4.2.6 SR distribution

The histogram in Fig. [4.40] shows the distribution of the slew rate for 100 functional samples. The average is $7.2V/\mu s$ with a standard deviation of $4.3V/\mu s$ for SR+ and $7.4V/\mu s$ with a standard deviation of $2.1V/\mu s$ for SR-.

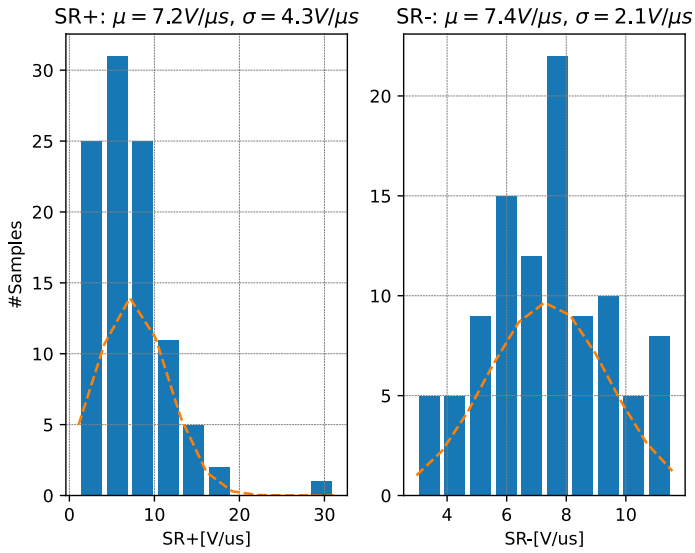


Figure 4.40: SR distribution

Chapter 5

Comparison with State-of-the-Art

Based on the results obtained from the floating inverter DIGOTA and other DIGOTA presented in the past, a comparison of performance parameters has been conducted. The comparison primarily reveals that the GBW is greater compared to previous solutions. This can be justified because the self-oscillation frequency is higher, resulting in higher power consumption. Another advantage is that the footprint or area occupancy is lower.

Performance	**DB-OTA** [21]	**DB-OTA (Muller-C)** [22]	**This Work***	**Unit**
Technology	180	180	180	nm
Supply Voltage	0.3	0.3	0.4	V
DC Gain	35	30	35.3	dB
GBW	0.850	0.250	36.3	kHz
Slew Rate	0.5	0.085	7.3	V/ms
THD	3	2	1.3	%
C Load	80	150	10	pF
Power	2	2.4	3.5	nW
Area	1426	982	270	μm^2
FOMs	34	15.6	103.7	$\frac{MHz \cdot pF}{\mu W}$
FOMl	20	5.3	20.9	$\frac{V \cdot pF}{\mu s \cdot \mu W}$

Conclusions

In this thesis, the design of a DIGOTA in TSMC180 technology has been presented with the aim of exploring a new circuit solution for common-mode input control, in order to compare it with other previously proposed DIGOTAs.

Firstly, the IoT trend has been introduced, justifying the performance demands of the hardware required for building systems that operated in this context.

An overview of the main performance characteristics of operational amplifiers has been provided analytically. The state of the art has been explored, highlighting the main techniques for designing low-power amplifiers, including the digital-based approach, with solutions that have been documented in the literature.

The structure of the floating inverter has been displayed, and a simplified model has been created to demonstrate how it can be employed in controlling the common mode of a digital differential pair. Finally, the design has been presented, demonstrating how the circuit was sized.

Subsequently, the performance obtained from simulations of the schematic with the nominal component characteristics has been showcased. Additionally, all the testbenches used have been displayed. After the schematic simulations have been conducted, the circuit layout has been constructed, and the same testbenches have been utilized to assess the performance of the extracted view, highlighting results that have been comparable with the previous ones.

Monte Carlo simulations, on the other hand, have highlighted how process variability has significantly influenced this particular type of structure. Despite the strong process dependence, the estimated average values have been compared with the state of the art. Following the comparison, it can be concluded that with a smaller area, it has been possible to achieve good results in terms of GBW at the same gain level.

Appendix

MATLAB code

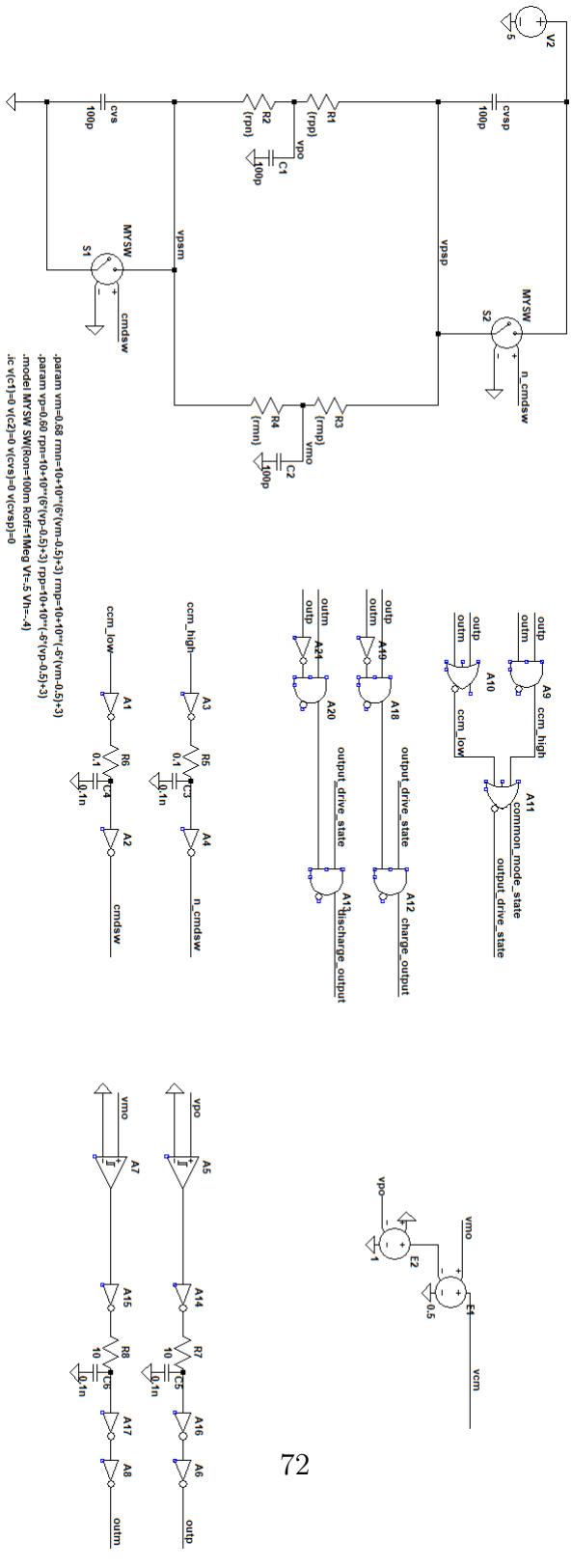
Digital operational transconductance amplifier behavioural description

```
2
clear all
close all
clc

t = 0:1e-4:1;

vt = 0.5;
c_out = 1;
c_cmp = 1;

ip_out = 10e-3;
in_out = -10e-3;
ip_cmp = 10e-3;
in_cmp = -10e-3;

v_out = zeros(size(t));
v_cmp = zeros(size(t));
d_v_out = zeros(size(t));
d_v_cmp = zeros(size(t));

v_p_ = zeros(size(t));
v_m_ = zeros(size(t));

v_p = .4*sin(4*pi*t)+ 0.4;
v_m = ones(size(t))*0.6;
%v_m = ones(size(t))*0.6;
beta=1/1; %Beta = 1 voltage follower operation


for i = 1:1:size(t')


    if i == 1
        v_p_(i) = v_p(i) / 2;
        v_m_(i) = v_m(i) / 2;
```

```
    else
        %uncomment for closed loop operation
        %v_m(i) = v_out(i-1)*beta;
        v_p_(i) = v_p(i) / 2 + v_cmp(i-1) / 2;
        v_m_(i) = v_m(i) / 2 + v_cmp(i-1) / 2;
    end

    if v_p_(i) >= vt
    v_op(i) = 1;
    else
    v_op(i) = 0;
    end

    if v_m_(i) >= vt
    v_om(i) = 1;
    else
    v_om(i) = 0;
    end


    if v_op(i) == 1 && v_om(i) == 0
        io = ip_out;
        icmp = 0;
    elseif v_op(i) == 0 && v_om(i) == 1
        io = in_out;
        icmp = 0;

    elseif v_op(i) == 0 && v_om(i) == 0
        io = 0;
        icmp = ip_cmp;
    elseif v_op(i) == 1 && v_om(i) == 1
        io = 0;
        icmp = in_cmp;
    end

    d_v_out(i) = io/c_out;
    d_v_cmp(i) = icmp/c_cmp;

    v_out(i) = sum(d_v_out);
    v_cmp(i) = sum(d_v_cmp);

    if v_out(i) < 0
        v_out(i) = 0;
        d_v_out(i)= 0;
    elseif v_out(i) > 1
        v_out(i) = 1;
        d_v_out(i)= 0;
    end


end

figure
hold on
ylabel("Voltage [V]")
title('input v_p e v_m')
plot(t,v_p,'r')
plot(t,v_m,'b')

figure
```

```
subplot(5,1,1)
grid on
hold on
ylabel("Voltage [V]")
xlabel("Time [s]")
plot(t,v_p,'r')
plot(t,v_m,'b')
ylim([0 1])
legend("v_p","v_m")

subplot(5,1,2)
grid on
hold on
plot(t,v_p/2+v_m/2,'r')
plot(t,v_p-v_m,'b')
plot(t,zeros(size(t)),':','color',[0,0.5,0],'linewidth',0.1)
xlabel("Time [s]")
ylabel("Voltage [V]")
ylim([-0.7 1])
legend("vcm","vd")

subplot(5,1,3)
grid on
hold on
ylabel("Voltage [V]")
xlabel("Time [s]")
plot(t,v_op,'r')
plot(t,v_om,'b')
ylim([0 1])
legend("v_p'","v_m'")

subplot(5,1,4)
grid on
hold on
ylabel("Voltage [V]")
xlabel("Time [s]")
plot(t,v_cmp,'r')
ylim([0 1])
legend("vcmp")

subplot(5,1,5)
grid on
hold on
ylabel("Voltage [V]")
xlabel("Time [s]")
plot(t,v_out,'r')
legend("vout")
```

FI DIGOTA behavioural model



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