POLITECNICO DI TORINO

Master's Degree in Electronical Engineering

Design of an Ultra-Low-Power Digital-Based Potentiostat for Wearable Biosensors

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Abstract

Continuous and non-invasive monitoring of metabolites, biological markers, and drugs exploiting wearable biosensors is even more important as an instrument to monitor the evolution of diseases and, in general, to improve the quality of life in both personal and professional contexts.
Real-time monitoring of chemical agents is possible thanks to a new class of wearable biosensors, which, thanks to their extremely small dimensions and low power consumption, can be applied directly to the skin or to clothes, offering several benefits. Wearable applications require innovative electrochemical sensors with extremely small dimensions, low cost, and ultra-low power consumption. Acquisition systems based on standard operational amplifiers designed with conventional analog techniques are not able to satisfy the requirements of wearable biosensors, motivating an increasing interest in alternative solutions, like a Digital-Based (DB) approach.

In this context, the purpose of the thesis is to design, optimize, verify, and test on-chip a Digital-Based acquisition system for electrochemical sensors (Digital-Based Potentiostat) for the monitoring of glucose with very low power consumption. The circuit is meant to be integrated on silicon in a 130nm CMOS technology by STMicroelectronics.
The DB-potentiostat is an acquisition system made up of a Digital-Based operational transconductance amplifier (DIGOTA) in feedback with an electrochemical cell. In addition to the improvements brought by the DIGOTA, new biosensing techniques based on nanostructuration processes are explored in order to enhance the sensing capability of the system.
Starting from the optimization of [11] with respect to the technology provided by STMicroelectronics, the characterization of the potentiostat has been performed; its response, steady-state error, and sensitivity have been evaluated. The layout has been designed returning an occupied area of the prototype equal to 1104 μm^2, therefore suitable for wearable application. With a typical corner process, at 27 °C has been evaluated a power consumption of 19.1 nW; from post-processing simulations a sensitivity of 41 LSB/mM is figured out.

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Acronyms

opamp
Operational amplifier

IC
integrated circuit

DB
Digital Based

ULV
Ultra-low-voltage

ULP
Ultra-low-power

Bio/CMOS
Interafce between circuits and biological materials

WE
Working electrode

CE
Counter electrode

RE
Reference electrode

Chapter 1

Introduction

In the last years, microelectronics has significantly advanced thanks to the introduction of nano-scale CMOS technology for integrated circuits (IC). The design of CMOS interfaces for micro-scale sensing system has also taken advantage of this progress, allowing the design of biosensors of extremely small dimensions. These considerations have opened up new areas of research interest, among which Body-Dust[7] that targets the implementation of micrometer-scale sensors with dimensions comparable with human cells. Wearable biosensors aim, similarly, is to implement a new class of biosensors that can be applied directly on the human body, for instance, on clothes or directly on the skin. The versatility of wearable biosensors makes them suitable for a wide range of applications, and their development and usage continue to grow significantly. They offer significant potential to enhance health, quality of life, and productivity in both personal and professional contexts. The fields of possible applications of these sensors are different, but one of the most interesting is medical care. These sensors are designed to monitor physiological parameters in real-time, creating a continuous health monitoring system for the prevention and treatment of diseases. As sensor technology continues to advance, it holds the promise of revolutionizing health-care by providing continuous, non-invasive, and personalized health monitoring, ultimately leading to better health outcomes and quality of life. These kinds of applications require innovative electrochemical sensors with extremely small dimensions, low cost, and ultra-low power consumption.
Acquisition systems based on standard operational amplifiers designed with conventional analog techniques are not able to satisfy the ultra-low power, low dimensions, and low-cost requirements of wearable biosensors, motivating an increasing interest in alternative solutions.

1.1 Thesis Objectives

The aim of this thesis is to design, optimize, verify, and test on chip a digital-based acquisition system (Digital-based potentiostat) for electrochemical sensors for glucose detection with very low power consumption. The circuit is meant to be integrated on silicon in a 130 nm CMOS technology by STMicroelectronics. The designed digital-based potentiostat entails a digital-based operational amplifier in feedback with an electrochemical cell. The output signal is proportional to the detected concentration of glucose.
The implementation of the Digital-based operational amplifier turns out to be a stimulating challenge because of its possible applications. It simulates a standard analog feedback operational amplifier, providing several advantages such as ultra-low supply voltage, ultra-low power consumption, and smaller dimensions. In particular, the supply voltage value is kept equal to 0.5 V, the targeted power consumption is in the order of nW, and the desired area occupies thousands of square micrometers.
In addition to this, the multidisciplinary footprint of this thesis leads to an in-depth analysis of the electrochemical aspects, which is done to create a model useful to simulate the cell from an electrical point of view.

1.2 Thesis Overview

After this introduction, the thesis is organized as follows:

- Chapter 2, a revisitation of the redox reactions' basic concepts and classical potentiostat-based measurement systems is proposed. Moreover, a brief overview of the electrochemistry exploited in this design is provided.
- Chapter 3, an in-depth analysis of the state-of-art is presented; the DB-opamp and the DB-potentiostat are analyzed in detail;
- Chapter 4, this chapter is dedicated to the sizing of the transistor circuit and the characterization of the main parameters;
- Chapter 5, the simulation results for both the DB-opamp and the DB-potentiostat are presented;
- Chapter 6, a detailed description of the pad-ring and the layout is proposed. Post-Layout Simulations (PLS) are also reported;
- Chapter 7, summarizes the thesis work and shows future perspectives.

Chapter 2

Electrochemical sensors: basic concepts

In this chapter, the basics of potentiostat-based measurements are explained. A brief revisitation of redox reactions and biosensing techniques is proposed to introduce classical CMOS potentiostat circuits. To overcome the limits of standard sensing techniques, innovative biosensing based on the nanostructuration of electrodes is presented, highlighting its advantages with respect to classical methods. Furthermore, the standard electrical model of an electrochemical cell is discussed; finally, a new model is developed to be tested in feedback with the prototype.

2.1 Classical Potentiostat-based measurement

The basics of classical integrated CMOS potentiostat-based measurements are presented. Potentiostat-based measurements are based on redox reactions, a specific class of chemical reactions that generate current; for this reason, a short introduction to this family of reactions is proposed. Biosensing techniques are then described, pointing out the advantages of innovative methods; finally, the chronoamperometric method is discussed.

2.1.1 Redox reaction

Redox reactions are chemical processes in which there is a transfer of electrons between two chemical substances. These reactions involve the oxidation of one substance (loss of electrons) and the reduction of another substance (gain of

electrons). The current generated is proportional to the concentration of the substances involved in the reaction. Measuring the generated electrical current means directly monitoring the relevant parameters of a chemical reaction, in particular the concentration of molecules implicated in the process. Electrodes are used at the Bio/CMOS interface to sense the current involved in the redox process. Usually, a specific biological component (e.g., an enzyme) is immobilized on the electrode; this biological component can selectively recognize and interact with the target biomolecule. When the target biomolecule binds to the biological marker, it can trigger a redox reaction. In this reaction, electrons are transferred between the biomolecule, the biological recognizer, and the electrode; the electron transfer generates a current sensed by the CMOS interface. This current is directly proportional to the rate of the reagents and, consequently, the concentration of the biomolecule in the sample.
Designing a Bio/CMOS interface that allows the correct collection of data from redox reactions becomes a fundamental challenge to provide a sensitive means for biomolecule detection in applications such as medical diagnostics. The classical measurement system based on the described process is the potentiostat-based measurement.

2.1.2 Biosensing techniques

Biosensing techniques for the detection of glucose are presented. Classical methods based on oxidases are analyzed and compared with newer techniques based on electrode nanostructuration, as in [1].

Biosensing based on oxidases

A classic diagnostic portable system like a glucose's sensor allows to monitor the concentration of glucose in the plasma. Traditionally, this is done by exploiting oxidases, enzymes that enhance biochemical reactions. More generally, oxidases are enzymes that transform their own substrates (e.g., glucose) into some products and hydrogen peroxide. The quantity of hydrogen peroxide produced is directly proportional to glucose‘s level of reagents, so it is possible to monitor glucose‘s level simply by counting the molecules of hydrogen peroxide.

Non-enzymatic detection of glucose

Previously discussed sensors based on oxidases are strongly dependent on external conditions like temperature and humidity. This becomes a great disadvantage because several calibration circuits and a switching system are

needed in order to have a reliable measure. It means an increasing number of components that involve an increase in terms of area and power consumption, implications that are not compatible with wearable applications. To solve this problem, a different approach is used: new-generation sensors based on the non-enzymatic catalysis of glucose are exploited. The main differences with respect to the classical sensors are explained in [5]: nanomaterials at the Bio/CMOS interface are used to directly oxide the glucose; the redox reaction creates a current proportional to the concentration of glucose without using intermediate molecules like enzymes. The nanostructuring process applied to electrodes brings several significant advantages. Nanostructuring significantly increases the electrode's surface area compared to conventional electrodes. The expanded surface area provides more active sites for chemical reactions, leading to enhanced reactivity and sensitivity. The larger surface area allows for greater contact with analytes or reactants, making nanostructured electrodes highly sensitive. They can detect low concentrations of target molecules or ions, which is crucial in sensing applications. Moreover, nanostructured electrodes promote faster electron transfer due to shorter diffusion distances.
In summary, the direct interface between glucose and nanostructured metal guarantees higher performance with respect to classical sensing techniques. For this reason, it has been decided to use this kind of approach in this thesis work. Platinum electrodes are widely used as glucose‘s biosensors thanks to their chemical stability, electrochemical conducivity, and biological compatibility. In particular, platinum screen-printed electrodes [1] will be nanostructured to perform non-enzymatic biosensing and tested in feedback with the potentiostat test chip.
At the same time, nanostructuration processes lead to significant modifications of the electrical characteristics of the electrochemical cell. To define our system from an electrical point of view, it becomes necessary to analyze the models already present in the literature and adapt them for our purposes.

2.1.3 Chronoamperometry at fixed potential

The chronoamperometric method is a sensing technique to study the evolution of a chemical reaction and, in particular, to monitor the concentration of the species involved in the process.
It allows us to monitor the current flux in a redox reaction at constant potential, changing the concentration of the metabolite. The potential of the solution can

[1] http://www.dropsens.com/en/pdfs_productos/new_brochures/550_c550.pdf

be kept constant using a potentiostat that controls and maintains the redox potential of an electrochemical cell, regardless of the current flowing through the cell. The figure shown below depicts the usual trend of this kind of acquisition: every metabolite injection results in current steps, and the relationship between current variations and variations of the metabolite‘s concentration is linear.

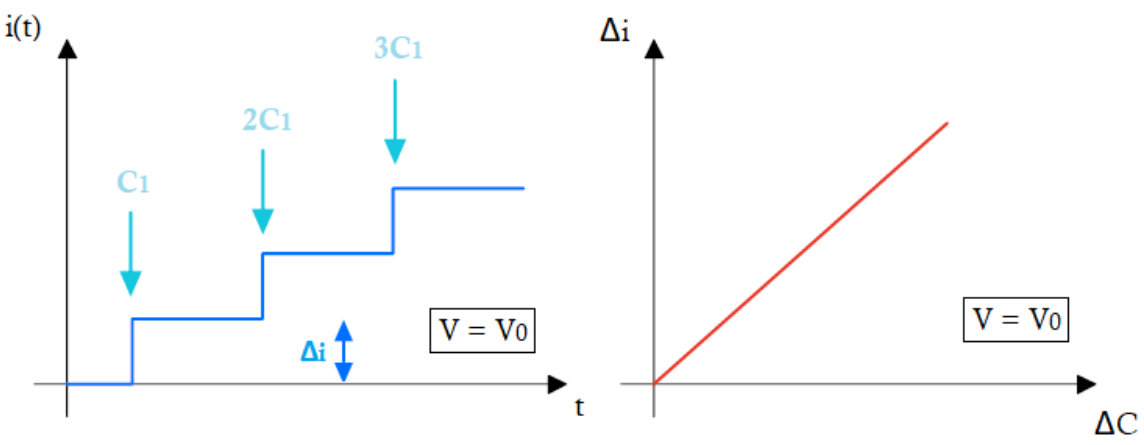


Figure 2.1: Chronoamperometry at fixed potential

In this context, a potentiostat-based circuit can be used to monitor the concentration of metabolites in a redox reaction. The potential at the reference electrode (RE) is fixed, and the potentiostat maintains a constant potential at the working electrode (WE), ensuring that the electrochemical reaction occurs under controlled conditions needed to apply the chronoamperometric method. The current generated by the redox reaction in the working electrode flows into the counter electrode (CE), driving the potentiostat. By designing a potentiostat with characteristics suitable for the electrochemical cell, it is possible to measure the current flowing, estimate the electrons involved in the reaction, and determine the metabolite concentration. The role of the electrodes in a potentiostat is explored in the next section.

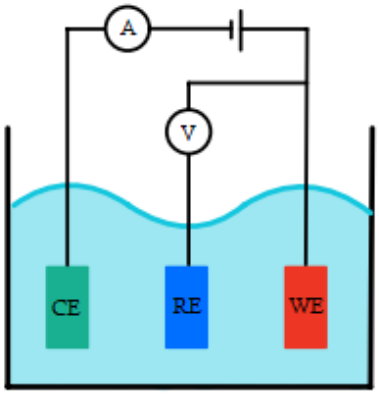


Figure 2.2: Electrochemical cell

A set of differential equations describes, from an analytical point of view, the behavior of redox reactions that take place in an electrochemical cell.
In particular, Cottrell's equation gives the relationship between the current increase obtained by increasing the metabolite concentration:

$$\Delta i = \frac{nFa\sqrt{D}\Delta C}{\sqrt{\pi \Delta t_0}}$$

Where:

- Δi is the current variation;
- n is the number of electrons involved in the redox reaction;
- F is the Faraday constant;
- a is the area of the electrode;
- D is the diffusion coefficient;
- ΔC is the metabolite concentration variation;
- Δt_0 is the time interval between metabolite injection and the current-increment measure.

2.2 Electrical modeling of an electrochemical cell

In this section, the standard electrical modeling of an electrochemical cell is presented.

2.2.1 Electrochemical three-electrode cell

An electrochemical cell exploits redox reactions to generate a current. The three-terminal electrochemical cell is composed of three electrodes:

- a working electrode (WE) where the redox reaction takes place, it contains all the biological and technological materials required by the biodetector;
- a reference electrode (RE) that supplies the right potential to have a correct reaction;
- a counter electrode (CE), needed to avoid current measurement problems due to voltage drops across the solution resistance.

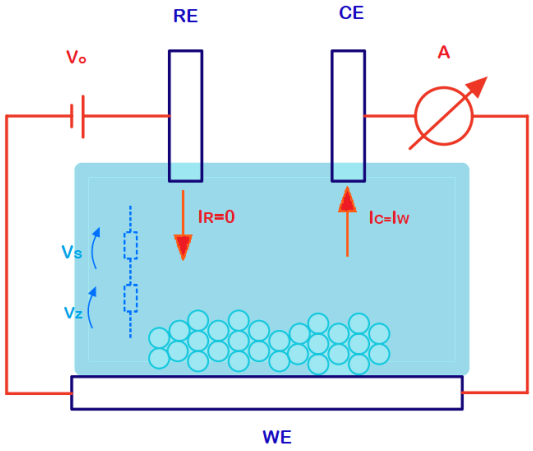


Figure 2.3: Three-electrode electrochemical cell

2.2.2 Electrical model of a single electrode

It is possible to develop an electrical model of a single electrode starting from physical considerations, as explained in [3]. A salt solution with its own resistance R_S is needed for a correct redox reaction; the electrode/solution interface is instead modelled with the resistance R_L. The capacitance C_{DL} is due to the accumulation of solution ions at the Bio/Cmos interface, this creates a double layer capacitance in front of the polarized electrode. This capacitance is also used to describe the reaction considering non idealities like the double layer phenomenon. This phenomenon refers to the formation of an electric charge layer on the surface of the electrode immersed in an electrolytic solution to sense a redox reaction. Ions in the solution can be attracted to or repelled from the electrode depending on their charge. Positive ions (cations) are attracted to the negative electrode (cathode), while negative ions (anions) are attracted to the positive electrode (anode). This movement of ions near the electrode surface creates a layer of electric charges in the region immediately adjacent to the electrode.

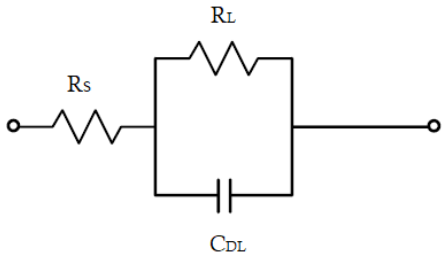


Figure 2.4: Electrical model of a single electrode

2.2.3 Electrical model of the electrochemical cell

Considering the electrochemical three-electrode cell previously discussed the overall electrical model is shown below. Is possible to modelize the RE as a single resistance because through it does not flow any current.

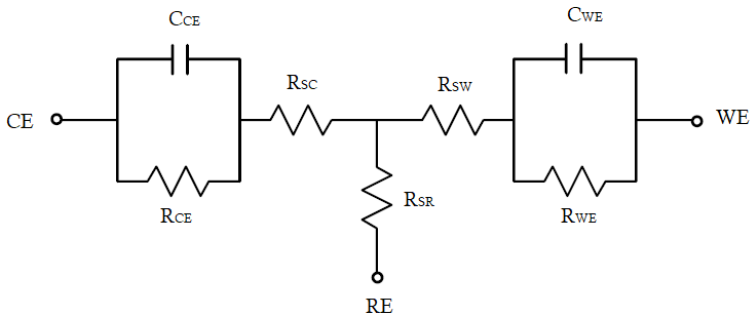


Figure 2.5: Electrical model of the electrochemical cell

For the WE and CE impedance characterization in magnitude and phase are exploited data reported in [8].
To model the WE, instead, the algorithm presented in [6] has been used to fit the magnitude and phase curves obtained, obtaining a parallel RC model as follows.
This model will be modified later taking into consideration modifies brought by nanostructuration process.

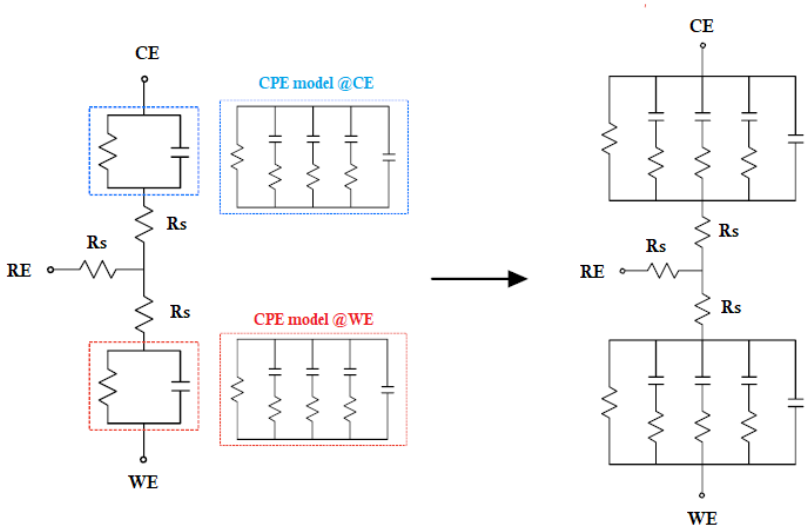


Figure 2.6: Parallel electrode model

2.3 Classical integrated CMOS potentiostat

A potentiostat is a data acquisition system that implements electrochemical sensing. It consists of an operational amplifier in feedback with the electrochemical cell, a front-end acquisition system is required to correctly collect data. The system can have different configurations according to the terminal that is connected to ground, but the behavior of the entire system remains unchanged. The grounded WE is the most common solution because it reduces the number of required components.

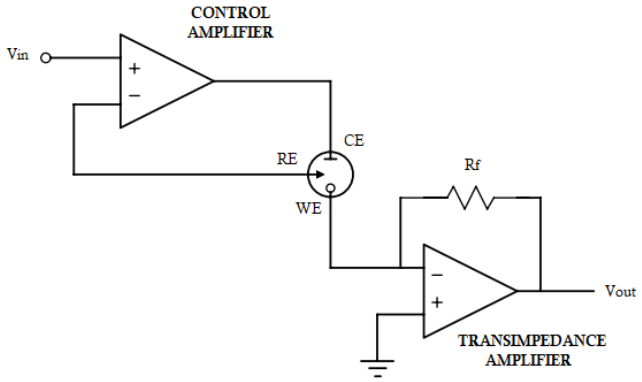
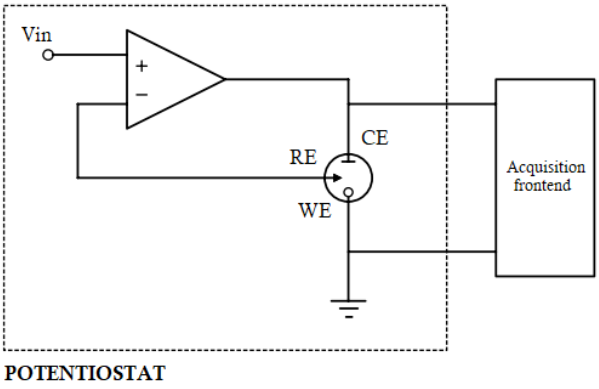


Figure 2.7: Grounded WE configurations with operational amplifiers

In the picture above, WE is virtually at ground due to the null differential input voltage of the transimpedance amplifier. This second amplifier provides amplification of the current that flows through the WE. Moreover, if a digital output is needed, the system must be followed by an ADC converter.



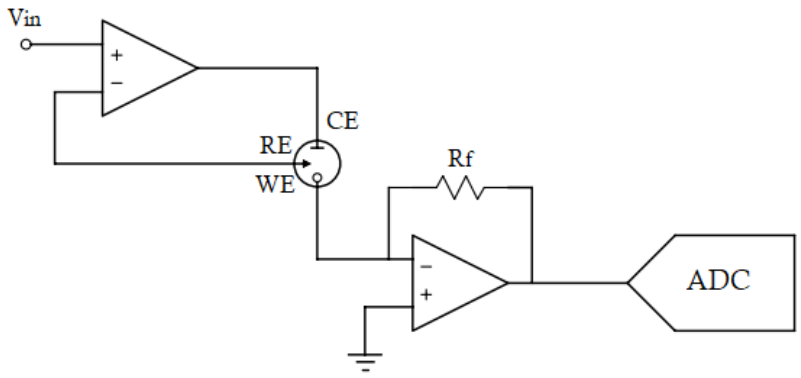


Figure 2.8: Potentiostat-based data acquisition system

A very accurate current measurement is required to estimate the concentration of metabolites involved in the redox; typically when the system has to handle a small current in the nano-ampere range. In these cases, a current-to-frequency conversion is used in classical integrated CMOS circuit, in order to obtain a reliable method to measure currents emerging from the WE. The circuit that implements this method is depicted.

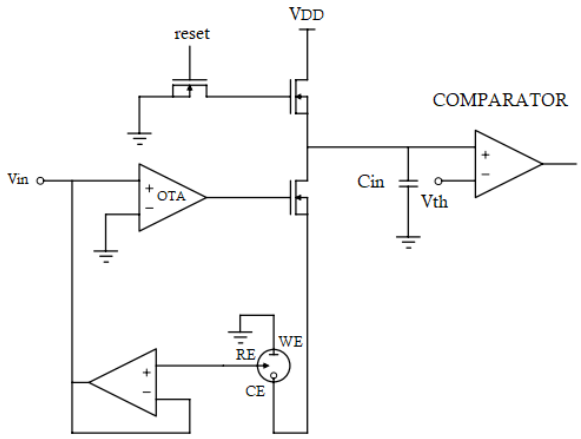


Figure 2.9: Current-to-frequency conversion (from [3])

It is possible to describe the behavior of this circuit by distinguishing two phases according to the charge (discharge) of C_{in}. Initially, C_{in} is charged thanks to the connection with the power supply V_{DD}; a comparator monitors the voltage drop across the capacitor; once the threshold voltage of the comparator is overcome, the switch that connects the supply voltage is opened. V_{DD} is disconnected, and C_{in} discharges through the electrochemical cell; in this way, the current flowing into the WE determines the time of discharge.

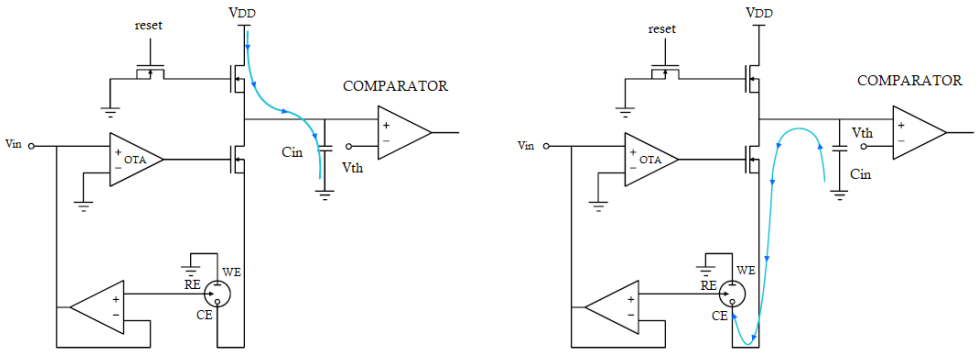


Figure 2.10: Current-to-frequency conversion phases (from [3])

It is easy to understand that the circuits described in this section are not compatible with the Body-Dust concept; in fact, classical CMOS potentiostats have a larger area with respect to the targeted micrometer scale and a higher power consumption than the nanowatt desired. To achieve these goals, in addition to use digital-based circuits, is useful to exploit new sensing technique (i.e., electrode nanostrcturation) in a potentiostat-based system.

2.4 Platinum nanostructured electrode

Nanostructuration guarantees high performace in electrochemistry, this advantages have been already discussed previously. In this section, instead, the changes that the nanostructuration brings in terms of area, and, consequently, in the electrical characteristics are discussed.
Nonostructured platinum electrodes are obtained as explained in [1]. This nanostrcturation method is based on a free-electrodeposition process done directly on the electrode metal; in such a way is eased the complexity of a classical nonostructurazion process; among all electrodeposition protocols this results the simplest, fastest and cheapest.

Electrodeposition affects the area of the electrodes and, in particular, increase the area of a factor 5. Working around one of the oxidation peaks shown in the voltagram below (peak I at -200 mV is chosen) is possible to fix the electrical properties of the cell and the creation of a model is possible.

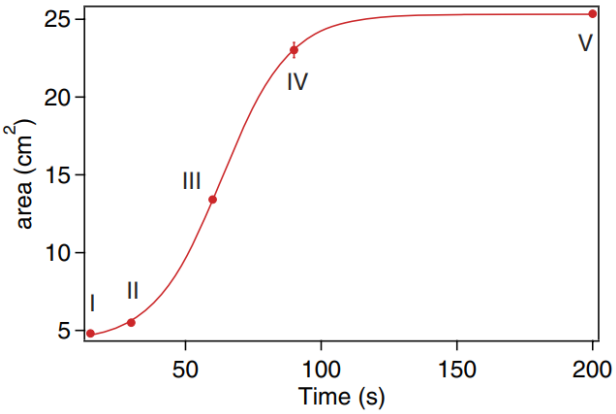


Figure 2.11: Evolution of the electrode area (from [1])

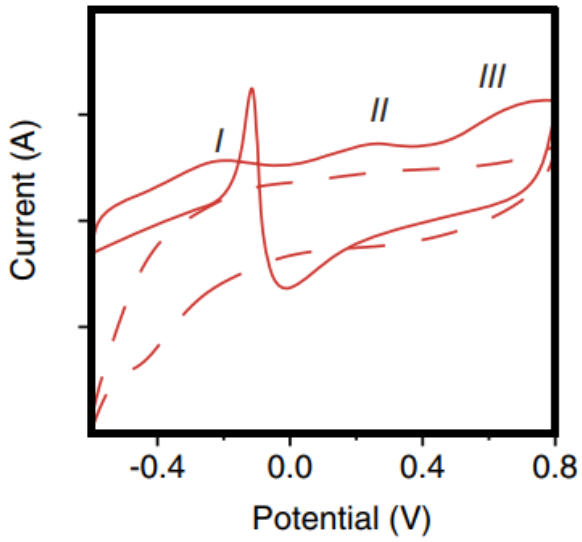


Figure 2.12: Pt nanostructured electrode voltagramme (from [1])

It is possible to extract the electrical model of the wanted electrode simply by scaling the components' values presented in [11], considering the ratio of the

areas occupied by the electrodes. It is important to take into account that this model will present some errors due to second-order effects of nanostructuration, which are impossible to be know a priori.

2.4.1 Nanostructured electrode model

In this section, the standard electrical model is modified, considering the changes due to the nanostructuration process.
A model of a nanostructured platinum electrode for non enzymatic detection of glucose is not available in literature, so, has become necessary to customize a model that achieve the cell's characteristic required by the potentiostat. The electrical model of the cell will be useful later on to simulate and validate the overall circuit. In this test environment is intended the usage of a Dropesense screen-printed platinum electrode, which geometry is characterized by a circular WE of 4 mm and a CE with a circular crown shape. As derived at the beginning of the section, working around the oxidation peak presented at 200 mV is possible to linearize the model and obtain a new model simply scaling the components value with respect to the ratio of the area.

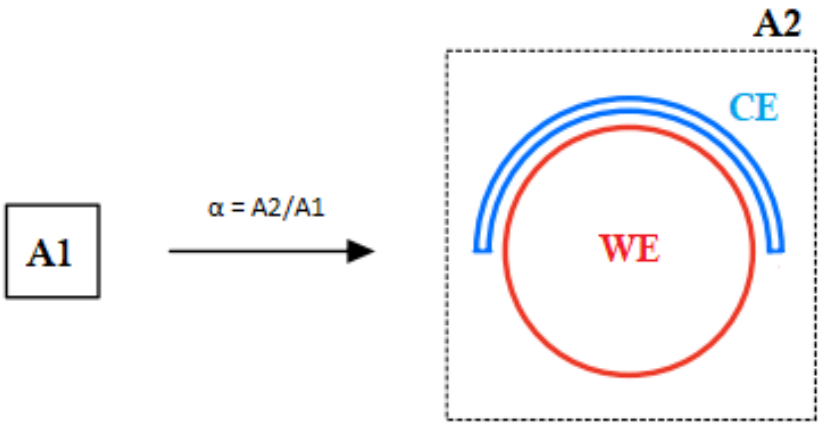


Figure 2.13: Area scaling

Has been taken as reference the electrode reported in [11], with rectangular shape and micrometer dimensions.

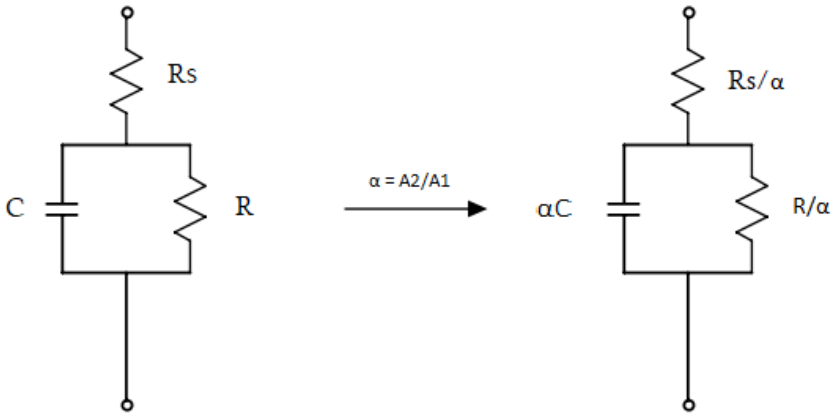


Figure 2.14: Components scaling

Starting from the components' value of the electrochemical cell reported in [11], the following values are obtained.

WE			
R		C	
[11]	This work	[11]	This work
30.4GΩ	3.04MΩ	500pF	4.95μF
318MΩ	31.8kΩ	280pF	2.8μF
3.3MΩ	330Ω	160pF	1.6μF
34kΩ	3.4Ω	210pF	2.1μF

Table 2.1: WE components'value

CE			
R		C	
[11]	This work	[11]	This work
4.2GΩ	750kΩ	2nF	11.2μF
76.9MΩ	14.34kΩ	1.2nF	6.7μF
1.5MΩ	268Ω	140pF	784nF
28kΩ	5Ω	1.2nF	6.7μF

Table 2.2: CE components' value

The value of the solution resistance can be evaluated with the formula given:

$$R_s = (\sigma_{PBS} * \frac{A}{r})^{-1} = 7.54\Omega$$

Where $\sigma_{PBS} = 12$ mS/cm is the conductivity of a buffered saline solution, A is the area, and r is the radius.

2.5 Faradic current

In this section, the amount of current flowing through the electrochemical cell is predicted. Knowing from [1] the sensitivity of the cell and considering the circular shape of the WE (d = 4 mm), the following is obtained:

$$S = S_0 A = 4\frac{\mu A}{mMcm^2} * 0.04cm^2 = 0.5\frac{\mu A}{mM}$$

In the human body, the typical glucose physiological range results in an order of: (3–8) mM, and the expected current range flowing through the electrochemical cell in standard conditions is:

$$(1.5 - 4)\mu A$$

Knowing that the sensitivity of the cell is directly proportional to its area and the nanostructuration process increases the surface contact area by a factor of five, the expected current range flowing through the nanostructurated cell is:

$$(7.5 - 20)\mu A$$

This current is modeled from a circuital point of view as an ideal current generator that sinks current from the WE to the CE.

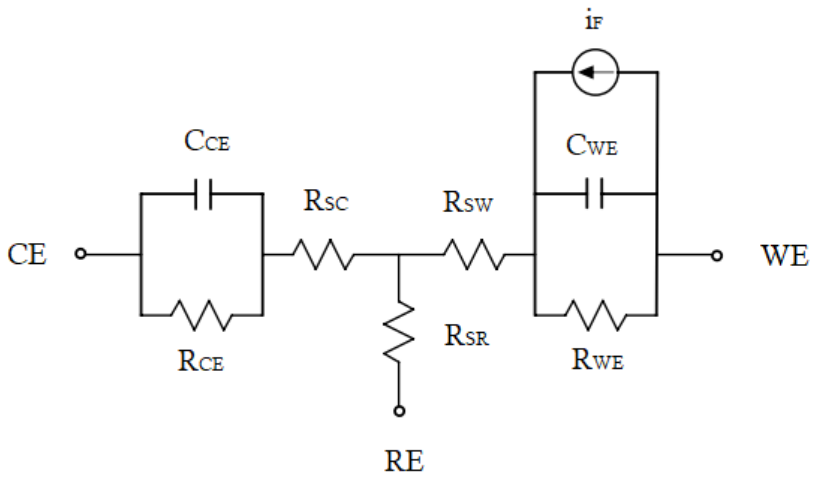


Figure 2.15: Faradaic current model

2.6 Final electrical model

To validate obtained data, a comparison with an empirically tested model of a nanostructurated electrochemical cell already present in literature is performed. In [10] is presented a carbon electrode nonastructurated with gold, impedance values are reported.

	Bare C electrode	C electrode Au nanostrucurated
1Hz	80kΩ	18kΩ
10Hz	13kΩ	2.5kΩ
100Hz	1.3kΩ	220Ω

Table 2.3: Nanostructuration effect on the impedace of a generic electrode

Is possible to notice that the maximum error is, as in our case, of an order of magnitude. Taking into account that nanostructuration process brings secondary effects not known a priori, it has been decided to estimate a possible error of two orders of magnitude on the impedance value of the cell. So, until an empirical evaluation of the cell is not performed, the potentiostat must be provided of a trimming circuit that allows to compensate the possible error.

Chapter 3

Digital-Based Amplifier and Potentiostat

The analysis of the state-of-art is proposed in this chapter. Classical potentiostat-based measurement limitations have been discussed in the previous chapter, in particular underlining constraints in terms of occupied area and power consumption. In order to achieve the requirements of wearable applications, the digital-based transconductance operational amplifier is presented. At the end of the chapter, the DB potentiostat is presented in detail, underscoring all the differences compared with the traditional sensing technique.

3.1 Digital-Based Operational Amplifier

Wearable biosensors have limiting requirements in terms of occupied area and power consumption, targets not achievable by circuits designed with classical analog techniques. With respect to analog OTAs, Digital-Based operational amplifiers [4] bring significant savings in terms of occupied area and power consumption. In this section, a differential, self-oscillating digital OTA suitable for microscale biosensing described in [9] and [12] is analyzed.

3.1.1 Architecture and working principle

DIGOTA's goal is to achieve conventional analog OTA performances using a digital approach. To describe the behavior of the DB-opamp, the analysis of the MullerC-based DIGOTA reported in [9] is detailed below. Like any OTA, DIGOTA amplify a differential input $V_D = V_+ - V_-$, rejecting the common

mode component $V_{CM} = (V_+ + V_-)/2$.
The DIGOTA shown below is taken from [9] and presents a MullerC-based implementation. It is composed of an input stage, a common mode compensation block, and an output stage.

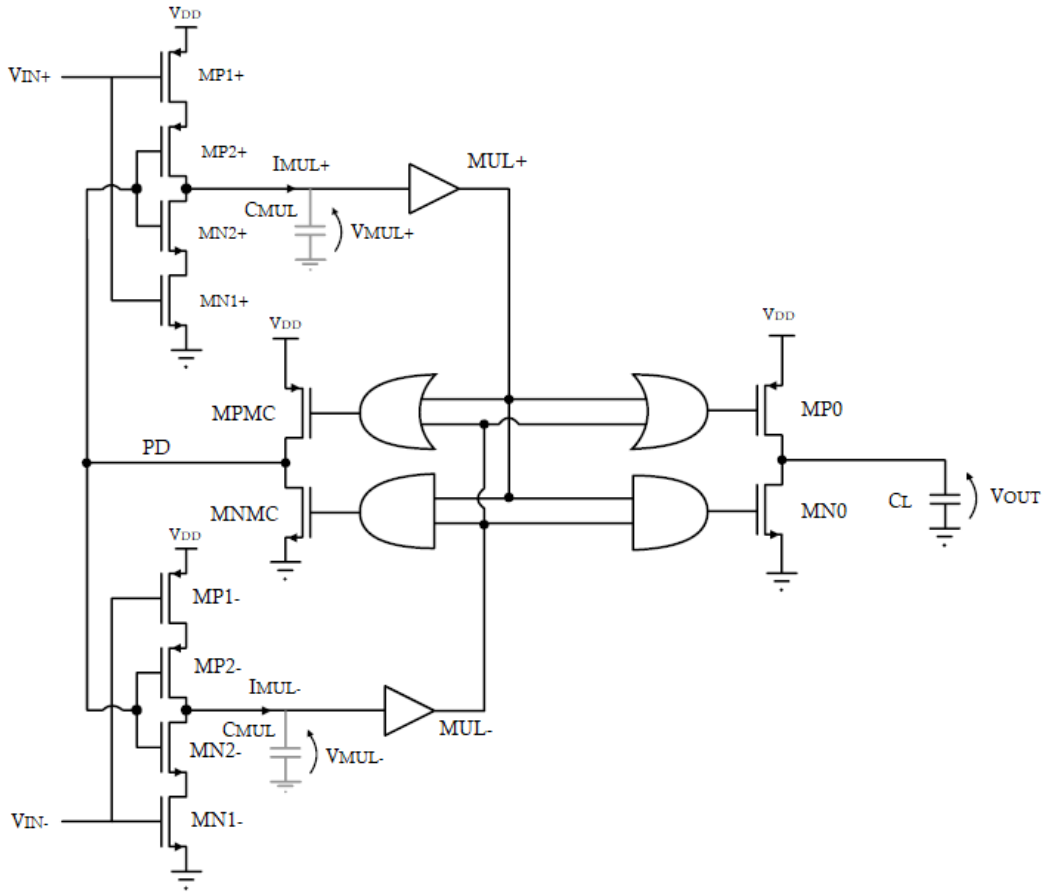


Figure 3.1: MullerC-based DIGOTA schematic

The working principle of this circuit is based on the translation of the input signal into a binary variable, which is processed by the logic that activates different blocks according to the binary value. To better understand the working principle of the circuit, it is useful to consider a couple of inverters where a differential voltage is applied. This pair generates an output signal comparing the inputs with the trip point (V_{trip}) of the inverters: for large signals, the

output saturates to V_{DD} or to ground, according to the sign of the input voltage. In these cases, the common mode voltage is farther away from V_{trip} and the codes (1,0) or (0,1) are generated, respectively for $V_D < 0$ and $V_D > 0$. On the contrary, if V_{trip} is close to the common mode voltage ($|V_{CM} - V_{trip}| < V_D/2$) the common mode voltage is predominant, and the codes (0,0) or (1,1) are generated.

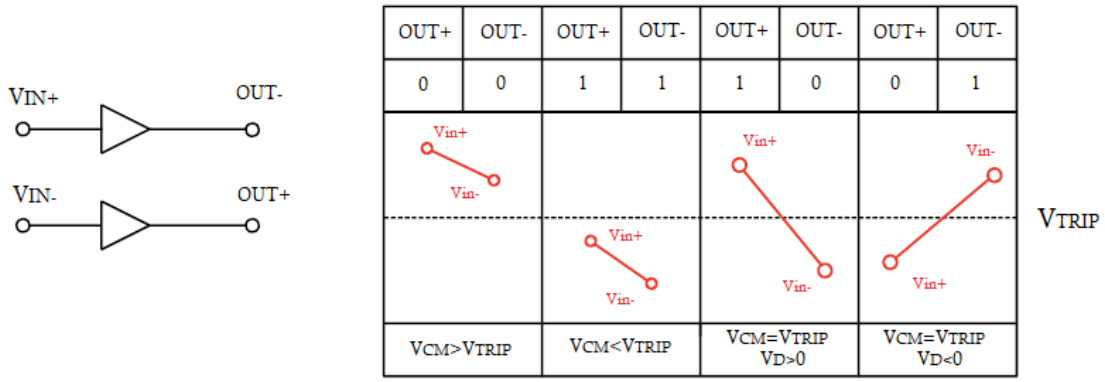


Figure 3.2: Code conversion working principle

The input stage consists of two MullerC elements followed by two inverters. The input voltage charges the MullerC capacitances (C_{MUL}), then V_{MUL} is processed by the inverter pair in order to obtain a binary code. The binary code is supplied to the logic that processes it. If the code is (0,1) or (1,0), the output stage will be turned on. On the contrary, the output stage will be kept in high impedance while the common mode compensation stage is driven. The common mode compensation block is composed of a pull-up circuit and a pull-down circuit, both driven by the signal PD. Instead, if the code is (0,0) or (1,1), compensation networks are alternatively turned on, leading to an oscillation of the output voltage. This brings the circuit into a natural oscillation condition with an oscillation period T_0 equal to: $T_0 = 1/f_0 = V_{DD}CMUL/I_{CM}$.
The self-oscillating common mode compensation loop drives the circuit into different states according to the detected code. A state transition graph can be derived according to the values of V_{MUL} and PD.

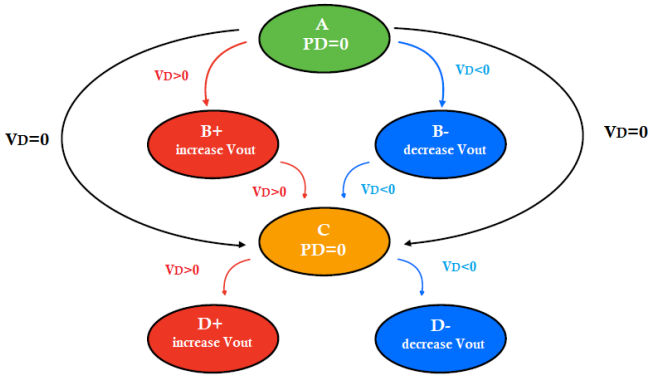


Figure 3.3: Logic states transition graph

The output stage is a push-pull; it is activated when code (1,0) or (0,1) is detected. When $V_D > 0$ the pull-up transitor (pMOS) is turned on, sinking current into the load and increasing V_{out}. On the contrary, if $V_D < 0$, the pull-down (nMOS) transistor is turned on, a current is absorbed from the capacitive load and V_{out} is decreased.

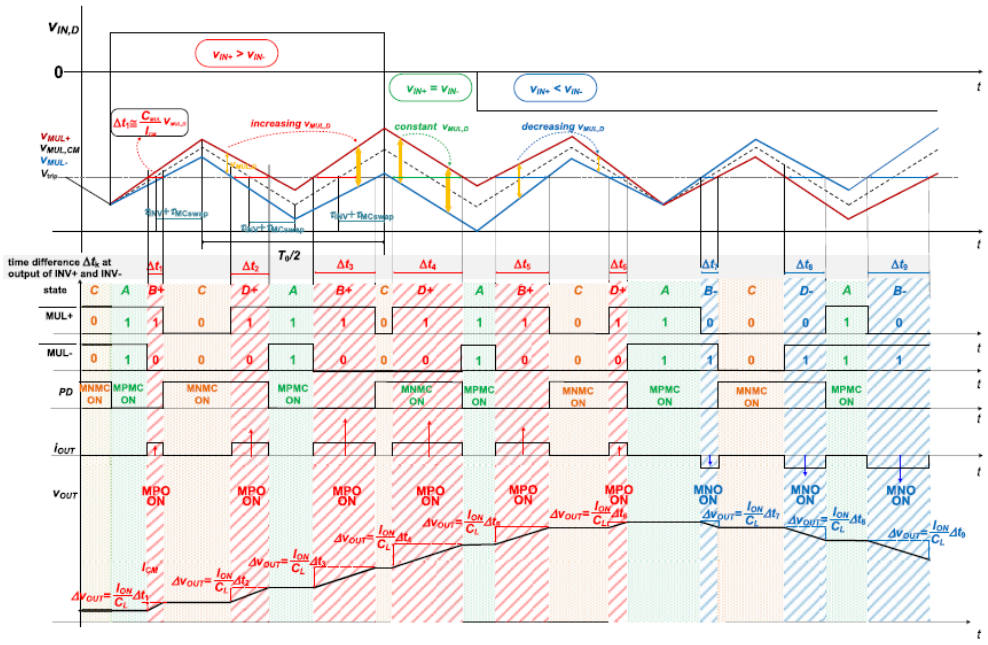


Figure 3.4: DIGOTA waveform (from [9])

3.1.2 Main characteristic

The following derivations from [9] are reported to provide a quantitative overview of the DIGOTA feature in terms of gain, stability and power consumption.

Transfer function

The DIGOTA voltage gain transfer function is:

$$A_D(s) = \frac{V_{OUT}(s)}{V_D(s)} = \frac{2g_m r_0 \frac{I_{ON}}{I_{CM}} \frac{r_{OUT} C_{MUL}}{T_0}}{(1 + s r_{OUT} C_L)(1 + s r_0 C_{MUL})}$$

This relationship can be obtained by considering each stage of the circuit. Since the input stage is a linear analog circuit, it is possible to extract its small signal equivalent circuit to derive its transfer function:

$$\frac{V_{MUL,D}}{V_D} = \frac{g_m r_0}{1 + s r_0 C_{MUL}}$$

The output stage of the DIGOTA is turned on when the code obtained from the inverters presents two different bits. This means that the input voltage of one digital inverter crosses the trip point before the other one, causing a delay of a Δt, whose value is dependent on the magnitude of V_D. During this amount of time, the capacitance of the MullerC element is discharged through a common-mode current, leading to a contribution equal to:

$$\frac{\Delta t_k}{V_{MUL,D}} = \frac{C_{MUL}}{I_{CM}}$$

During Δt, the output stage handles the current flowing into the capacitive load (C_L), which is in parallel to the output impedance (r_{out}). The summation of these current pulses can be expressed in the Laplace domain as:

$$\frac{V_{OUT}(s)}{\Delta t_k} = \frac{\frac{r_{out} C_{MUL}}{T_0}}{1 + s r_{out} C_L}$$

From the complete transfer function, the DIGOTA DC gain is:

$$A_{V0} = 2g_m r_0 I_{ON} \frac{r_{out} C_{MUL}}{T_0 I_{CM}}$$

Looking at the frequency behavior, two real poles are found.

$$s_{p1} = -\frac{1}{r_{out} C_L} \qquad s_{p2} = -\frac{1}{r_0 C_{MUL}}$$

s_{p1} is the dominant pole since C_L is orders of magnitude larger than C_{MUL}, while r_{out} and r_0 are close to each other. The gain-bandwidth product results in:

$$f_{GBW} = A_{V0} f_c = \frac{A_{V0}}{2\pi r_{out} C_L}$$

Power consumption

One of the main characteristics of the DIGOTA is that it can provide the same performance as an analog amplifier while ensuring extremely low power consumption. This is possible because, unlike a classic OTA, it does not work at a fixed operating point, and therefore static power consumption is almost zero. The power consumption of the DIGOTA can be expressed as the sum of different components: the consumption of the exploited logic elements, the output stage, and the leakage component.

$$P_{DIGOTA} = P_{logic} + P_{out} + P_{leak}$$

The dynamic power of the logic gates is directly proportional to the frequency of the system, and it is defined as the power needed to charge (or discharge) midway nodes of the network, so it is related to the number of commutations of the circuit; it is expressed as:

$$P_{logic} = \frac{2}{T} C V_{DD}^2$$

P_{out} is the power needed to charge (or discharge) the load capacitance; similarly, it is defined as:

$$P_{out} = f_s C_L V_{OUT}^2$$

The leakage power is given by the product of I_{leack} times V_{DD}. I_{leack}, anyway, is strongly dependent on the technology process used.

3.2 Digital-Based Potentiostat

A revisitation of the DB-potentiostat presented in [11] is proposed. This circuit targets enzymeless blood glucose sensing with direct digitalization. This work's aim is to meet the requirements of the new generation of biosensors by achieving micrometer dimensions while providing power consumption in the nW range. A power supply of 0.4 V is used to achieve a power consumption of 4.7 nW, occupying an area of 460 μm^2.
The system is designed to interact with a micrometer-square WE made of platinum nanospheres, nanostructured as explained in [1]; chronoamperometric method is used. A grounded WE configuration is exploited; hence, the RE potential is fixed and the faradaic current flows between WE and CE.

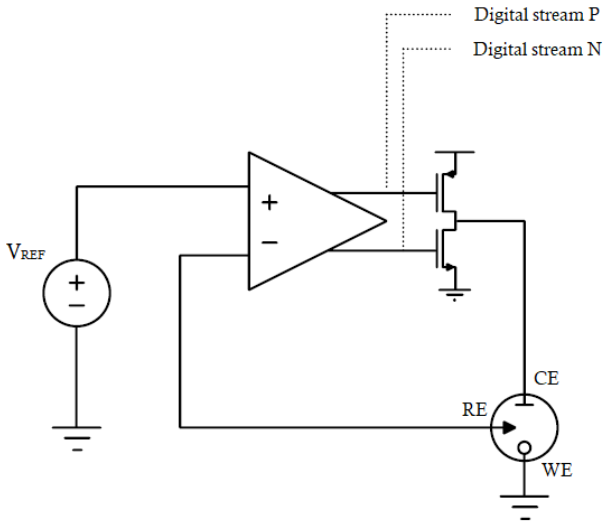


Figure 3.5: Digital-Based potentiostat

3.2.1 Architecture and working principle

The presented architecture is based on a DB-opamp in feedback with an electrochemical cell. With respect to the DB-opamp, this circuit presents two main differences: floating inverters are used in the input stage instead of MullerC elements, and two D flip-flops are inserted in the logic chain. The first change is done to improve energy efficiency due to the fact that floating inverters do not generate any DC current; flip-flops, instead, are used to break the natural oscillation of the DB-opamp, making the circuit sequential.

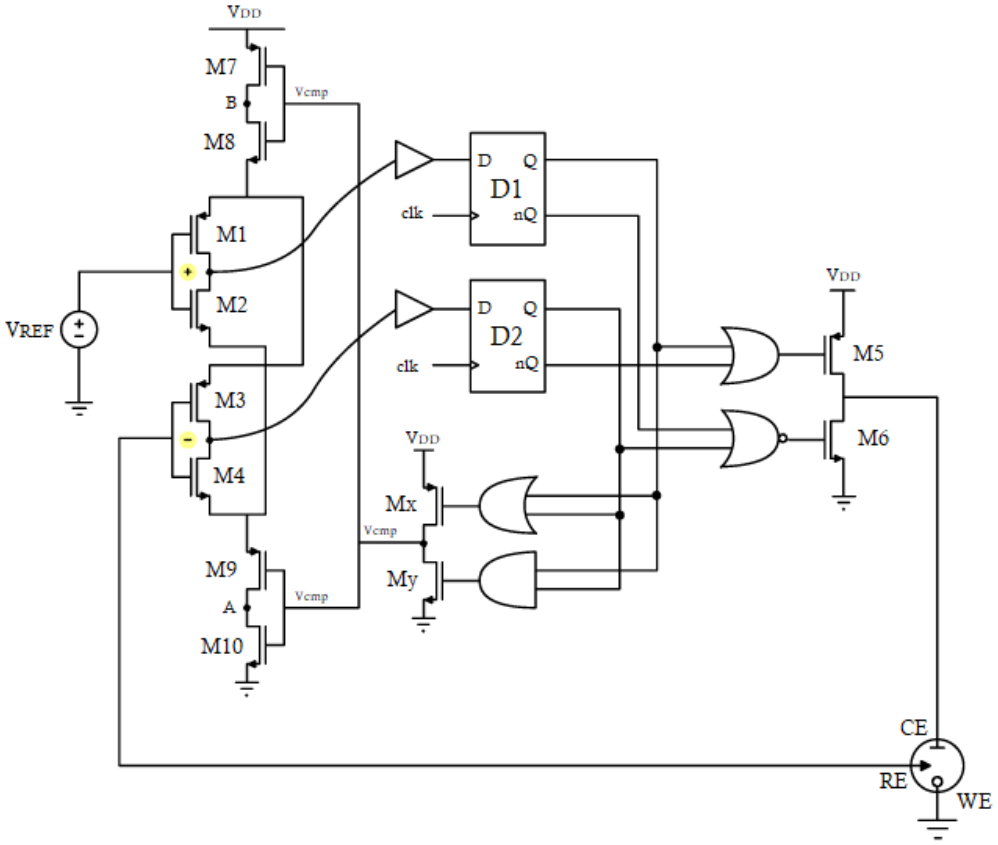


Figure 3.6: Digital-Based potentiostat schematic

Input voltages (V_+, V_-) are compared with the trip-point voltages of two digital inverters and translated into a binary variable. If D1 = 0 and D2 = 1, V_D is positive, the pMOS M5 is activated, and current is sourced into the load. On the contrary, if D1 = 1 and D2 = 0, $V_D < 0$ V, the nMOS M6 is activated and a current is sinked from the load.
In both cases, when the output stage is active, the current flowing through it is nearly constant, independently from the output voltage; and, considering a single clock cycle, it is possible to estimate the charge packet exchanged between the DB-opamp and the electrochemical cell as $I * T_{CLK}$.
Considering the entire sensing period and not only one clock cycle, the potentiostat, driven by the electrochemical cell, injects into the it a charge proportional to the faradaic current developed by the redox reaction. Therefore, it is possible

to estimate the faradaic current (I_F) averaging the current flowing into the CE with respect the entire sensing period. The formula to express the faradaic current with respect to I_{CE} is reported below:

$$I_F = \frac{pI_P - nI_N}{M}$$

where:

- p is the number of positive pulses;
- I_P is the costant current flowing through M5;
- n is the number of negative pulses;
- I_N is the costant current flowing through M6;
- M is the total number of pulses;

From this reasoning, it is possible obtain a digital value proportional to I_F processing the streams of pulses at the gates om M5 and M6; in this way, an analog-to-digital converter (ADC) is not needed in this kind of data acquisition system, saving power and area.
If the values stored inside the FFs are equal, instead, the sign of the differential input voltage cannot be detected, and the output stage is kept in high impedance. In this situation, the logic drives the compensation network according to the sign of V_D. In particular, when dealing with a code equal to (0,0), M_x is turned on while M_y is off, so M9 changes the logic value of the node A, precharged at 0 V by M10. If the code is equal to (1,1), M_y is turned on; M8 discharges the node B, precharged at V_{DD} by $M7$. In this way, the compensation block provides to the input inverter a dynamic bias to charge their input; the sign of V_D can therefore be detected, and in the next clock cycle, a useful code will be available.

3.2.2 Waveforms analysis

The purpose of this section is to analyze in detail the behavior of the DB-potentiostat, exploiting the waveforms obtained during the simulations. It is important to observe that the potential at the RE remains constant for a certain amount of time; after that, V_{RE} will diverge. The divergence of the voltage at the RE is linked to the saturation of the voltage at the CE; when V_{CE} reaches 0 V, the DIGOTA cannot dispense current, so it is not able to keep the potential at the RE constant. The system is meant to monitor the

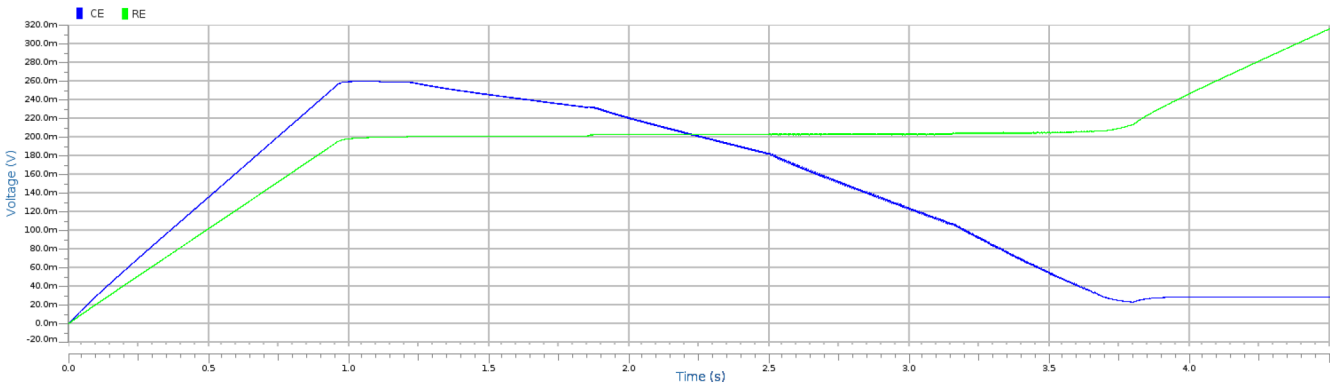


Figure 3.7: V_{RE} and V_{CE} during an acquisition

Waveforms of each stage are depicted.

Input stage

During the transient, the voltage across the inverter (Figure 3.8) converge thanks to the dynamic bias provided by the compensation network. These voltages are the inputs of the digital buffers; they sense their level and compare it with their V_{TRIP}, returning a digital signal (Figure 3.9). These signals are sampled by the FFs; Qs (Figure 3.10) are the digital output of the flip-flops; they are processed by the logic, and, according to their values, the rest of the circuit is driven.

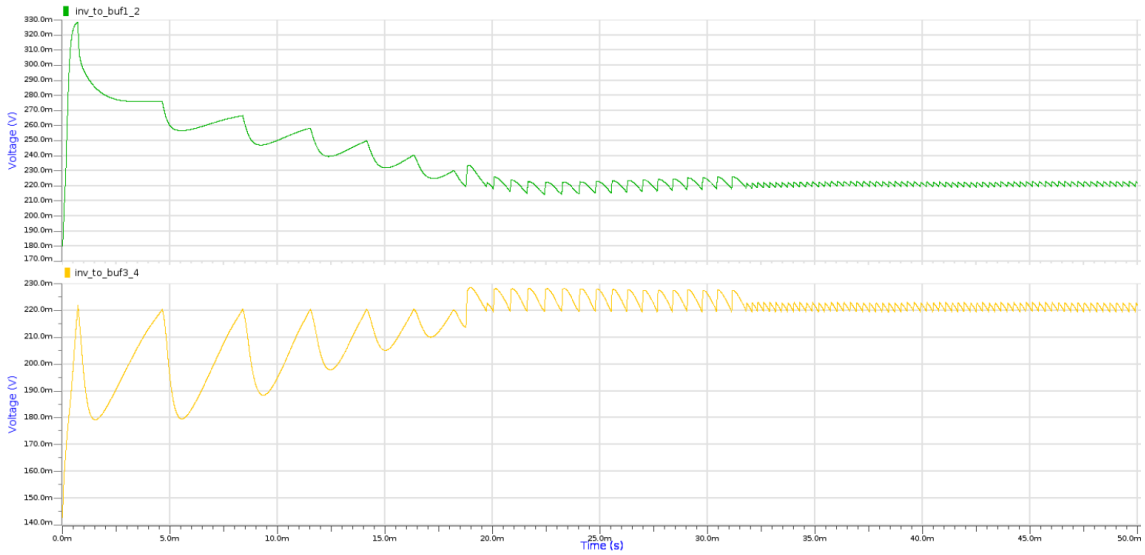


Figure 3.8: Inverter-to-Buffer voltages

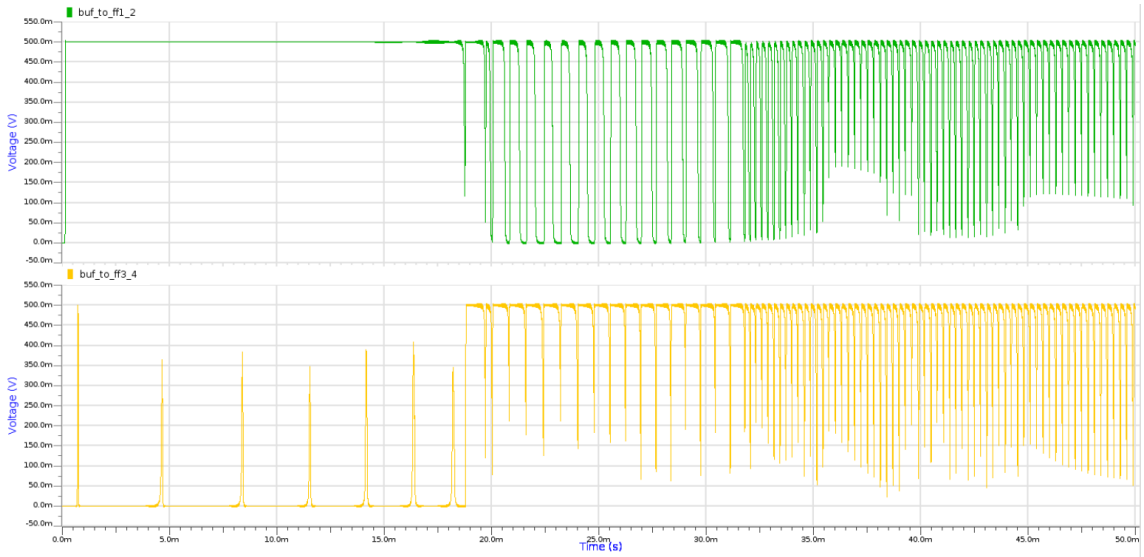


Figure 3.9: Buffer-to-FlipFlop voltages

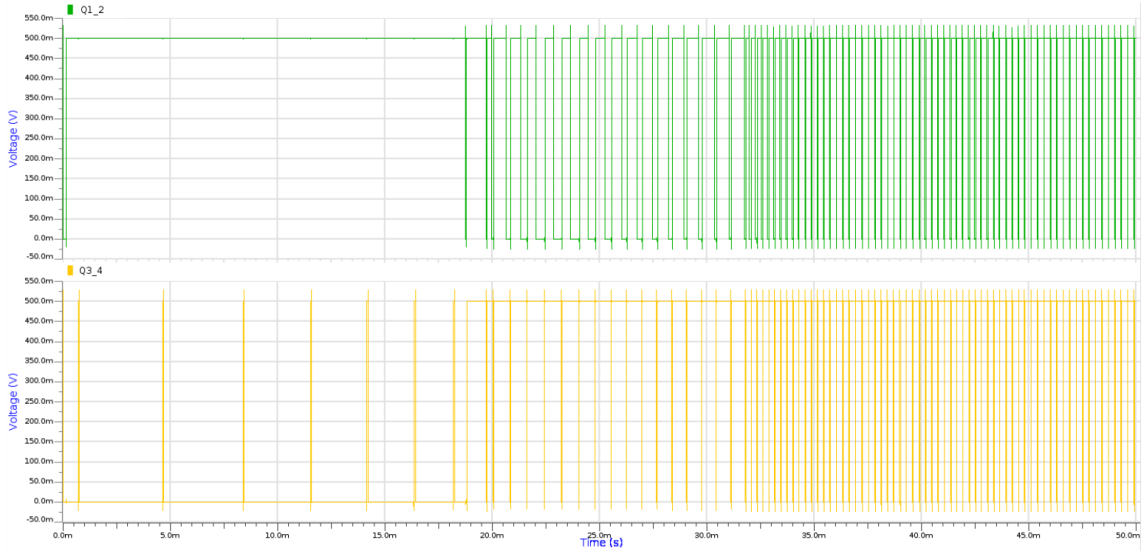


Figure 3.10: Flip Flops output

Output stage

The output stage, when active, provides a current to the cell through M5 and M6; these output transistors are driven by two digital signal. The signals out_digN and out_digP (Figure 3.11) are the the real output of the acquisition

system, post-processing evaluations return the value of the faradaic current involved in the redox reaction taking into account the number of positive and negative digital pulses during the entire acquisition. The current exiting from the output stage is coherent with the digital pulses and is depicted in Figure 3.12.

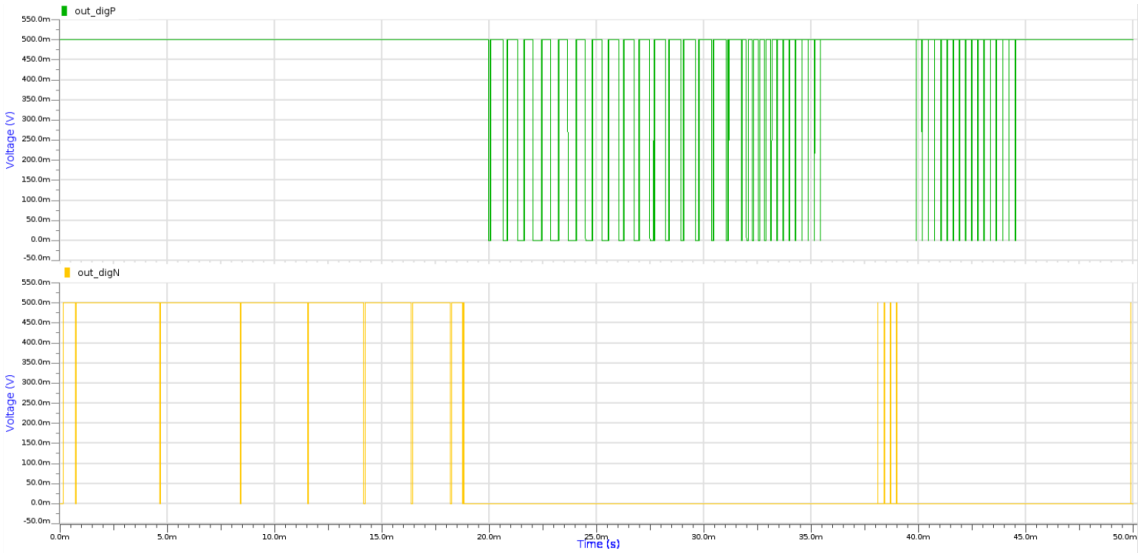


Figure 3.11: Digital outputs

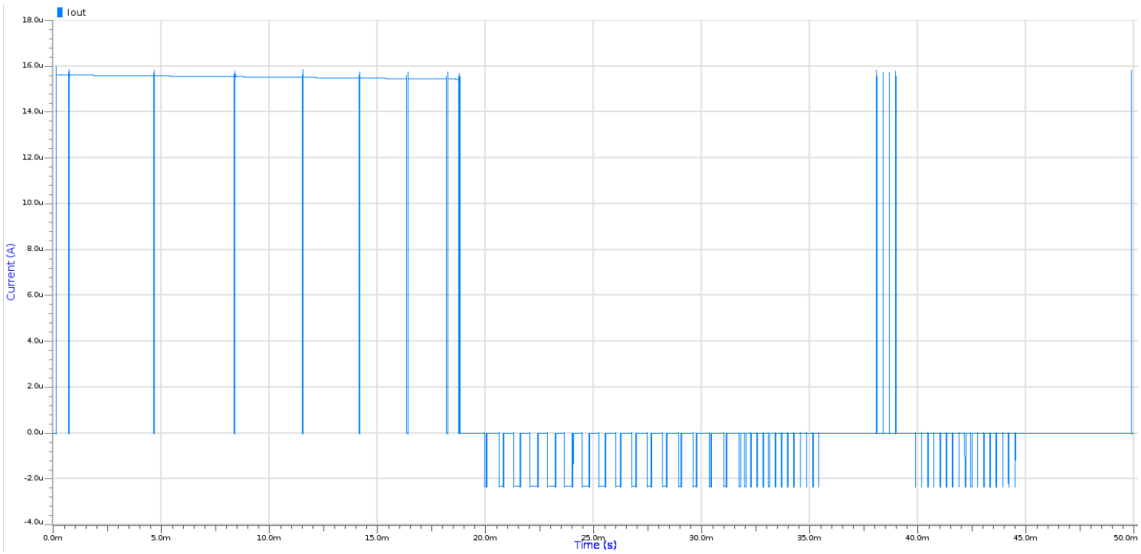


Figure 3.12: Output current

Common mode compensation network

In the picture below is possible to observe the behavior of the compensation voltage. It is driven by Mx and My and, when the the voltage at the RE is constant, its pulses

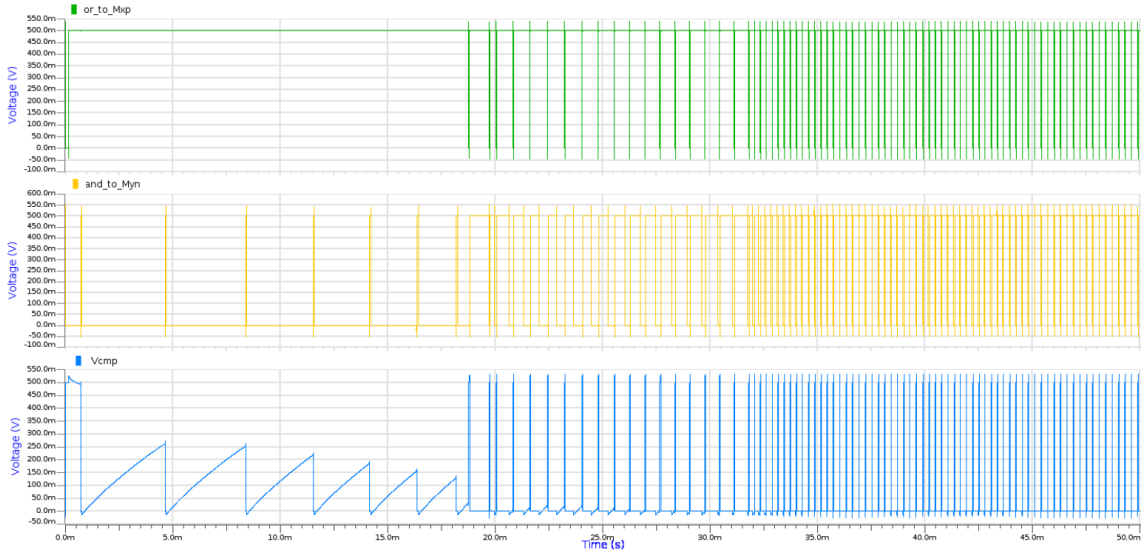


Figure 3.13: OR/AND driving Mx/My & Vcmp

Chapter 4

Design of a Digital-Based Potentiostat

Once the basic concepts of a DB potentiostat have been discussed, the optimization of the circuit will be presented. A CMOS 130 nm technology provided by STMicroelectronics is used. In particular, in this chapter, the reasoning behind the transistors' sizing and the characterization of the main parameters of the circuit are explained. The design of the trimming circuit and the characterization of the standard cells are also reported.

4.1 General considerations

The main parameters of the circuit are discussed below. The aim of this section is to explain the choices made for these values.

4.1.1 Power supply

Wearable applications require a power supply rail in the range of a few hundreds of nV, and, in particular, [11] refers to a $V_{DD} = 0.4$ V. In this thesis work, instead, it has been decided to proceed with a power supply of 0.5 V. Increasing this value guarantees that transistors will work anyway in sub-threshold region; moreover, a faster response and better reliability are obtained.

4.1.2 Working frequency

High frequency is not required for this kind of application; for this reason, a clock frequency of 50 kHz has been used. The correct timing of all the logic

elements of the circuit (both combinatorial and sequential) is ensured at 50 kHz, but this is not guaranteed for higher frequencies. For this reason, it is suggested to use the described prototype at the specified frequency or with lower values.

4.1.3 Reference voltage

V_{REF} has been set taking into account the oxidation potential of glucose and is inserted into the simulation with an ideal voltage generator. Figure 2.12 depicts the voltammogram of a redox reaction of a platinum solution interacting with glucose; this reaction is sensed by exploiting nanostructured platinum.
An oxidation peak at 200 mV is present; here, the reaction presents higher sensitivity and higher stability. A reference voltage of 200 mV has been set to simulate the oxidation peak condition.

4.1.4 Output capacitance

The first step to simulate the potentiostat is to check the functioning of the DB-opamp. To do this, a voltage-follower configuration has been exploited, and a load capacitance is used to simulate the electrochemical cell. Considering the cell's model created in Chapter II, the value of the output capacitance has been estimated to be equal to 5 μF with a possible maximum error of one decade. So, the output capacitance value has been estimated to be in the order of $500nF \leq C \leq 50\mu F$.

Power supply	0.5 V
Clock frequency	50 kHz
Reference voltage	200 mV
Load capacitance	5 μF

Table 4.1: Potentiostat main parameters

4.2 Transistor sizing

The design of an opamp is a complex, multidimensional problem in which several different constraints have to be taken into account. In this section, the reasoning for the transistors sizing at each stage is discussed separately. Anyway, considering the overall range of possible values that the load capacitance can assume, this configuration is no longer optimized; a trimming circuit to tune the variable load is designed to avoid this problem.

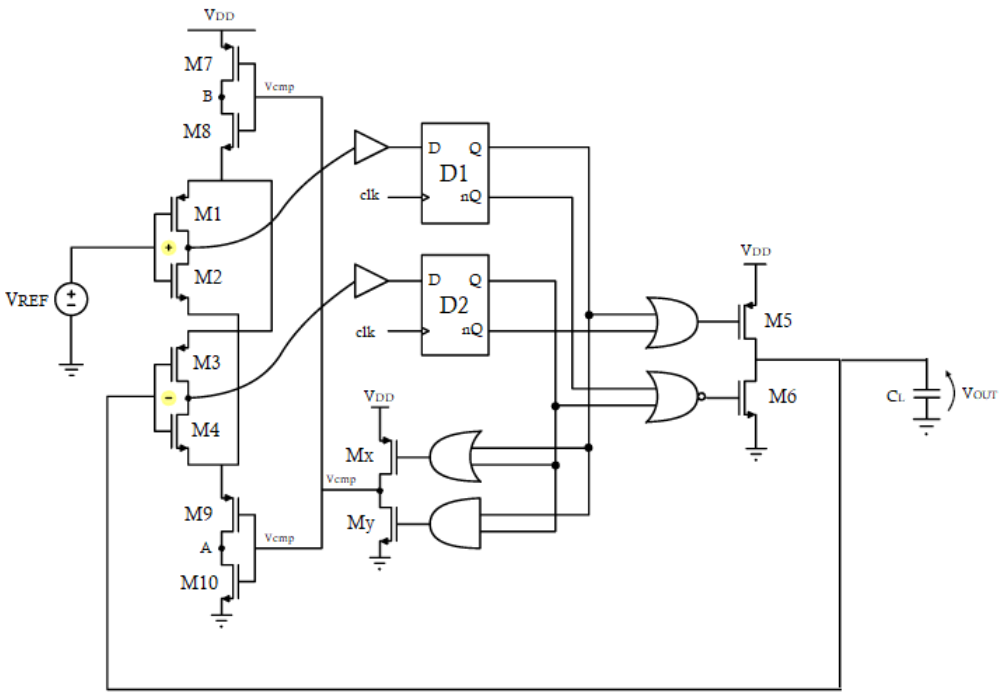


Figure 4.1: DIGOTA with buffer configuration and C_L

4.2.1 Input stage

Operational amplifiers working in sub-threshold region deal with low voltages, for this reason their performance can be affected by noise or by fluctuations of the supply voltage. The input stage of the DIGOTA must guarantee, as in a classical OTA, an adequate transconductance (g_m) and a good immunity to noise (ability of acircuit to operate correctly even in the presence of electrical

interference) in order to do not affect the input signal, as discussed in [2].
If the transistors of the input stage turn out to be too small they will not conduct correctly, leading to errors in operations of the DB-opamp. On the other hand, if their value is too large the response will be too slow and the timing will not be respected, moreover, in this case power consumption is increased. Correct operation are found with a width equal to 5 μm, but has been decided to keep the width value slightly bigger (6 μm) to have a reliable response. The value of the lengths kept at the minimum value; the resulting aspect ratio of the transistor of the input stage is: $\frac{W}{L}_{1,2,3,4} = \frac{6\mu m}{0.22\mu m}$

4.2.2 Output stage

In this section, the optimization of the single output stage considering an optimum load of 5 muF is described. The design of the entire trimming circuit is performed later, starting from the considerations made here.
The output stage strength is designed to provide a suitable current at the electrochemical cell. In order to do this, constraints on the faradaic current and on the electrode capacitance are considered. The desired response time of the system is in the order of (10-100) ms, a value of the output capacitance of 5μF and a reference value of 200 mV are used. Choosing an arbitrary rising time of 50 ms and considering the capacitor equation:

$$\frac{dV}{dt} = \frac{I}{C}$$

A current of 15 μA is needed. Furthermore, this current value turns out to be suitable for the value of the faradaic current found in Chapter II.
The output stage should behave like a constant current generator, so the transistors should not suffer from the channel length modulation phenomenon; to avoid this, the transistors' length has been increased. To satisfy these constraints, the optimal size of the transistors in the output stage turned out to be equal to: $\frac{W}{L}_{5,6} = \frac{5\mu m}{1\mu m}$ with a number of devices in parallel equal to 25.
To drive such a large output stage, a driver chain made by inverters of increasing strength is employed. The driving strength is the capability of providing sufficient current to efficiently charge the capacitance of the driven circuit. In this case, the output stage is much larger than the driving circuit; for this reason, a cascade of drivers of increasing strength is used.
The driving inverters have been designed considering that the output capacitance at the OR/NOR ports driving the output stage is of 2 pF, while the capacitive load is 250 times higher, in the order of 500 pF. The optimum number of driving stages turned out to be:

$$N_{OPT} = ln\left(\frac{C_L}{C_O}\right) \simeq 5$$

Where C_L=500 pF and C_O=2pF. The β factor that represents the relationship between the aspect ratio of the transistors is:

$$\beta = \left(\frac{C_L}{C_O}\right)^{1/N} \simeq 2$$

Considering the availability of the standard logic cells, to maintain optimal performances, it has been decided to use a lower number of stages with a higher β factor; in particular, both values of N and β have been set equal to 4.

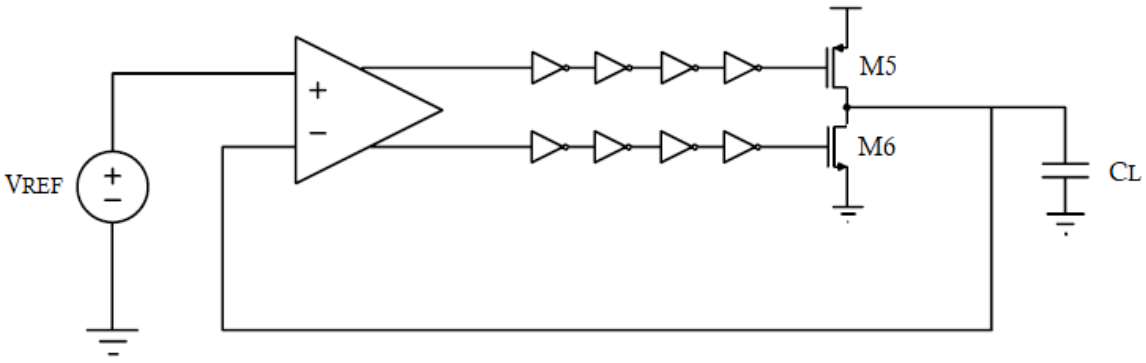


Figure 4.2: Inverter cascade driving the output stage

4.2.3 Common mode compensation block

The common mode compensation block is composed of two floating inverters that provide a dynamic bias to the input stage. In this way, the signal exiting from the input inverters is charged to detect the sign of the differential voltage. In the circuit described in [11], compensator's charge was accumulated on the parasitic capacitance of the biasing inverters; in this thesis, a very small MOM capacitor of the value of 50 pF has been inserted in each couple of floating inverters to guarantee good reliability.

The table below summarizes the aspect ratio of transistors of each stage.

		$\frac{W[\mu m]}{L[\mu m]}$	Number of devices in parallel
Input stage	M1,M2,M3,M4	$\frac{6}{0.22}$	1
Output stage	M5,M6	$\frac{5}{1}$	25
CM compensator	M7,M8,M9,M10	$\frac{3}{0.18}$	1

Table 4.2: Transistors aspect ratio

4.3 Design of the trimming circuit

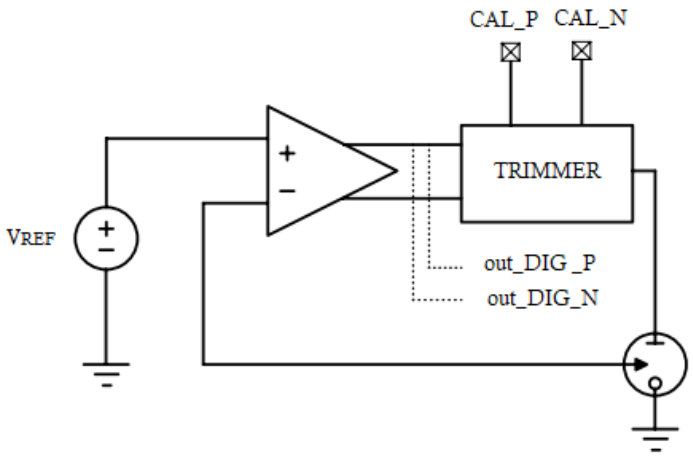


Figure 4.3: DB Potentiostat with trimming circuit

In Chapter II, a model of the electrochemical cell is proposed, and, for the resulting equivalent capacitance, a possible error of one order of magnitude is considered. To have a reliable system, it has been taken as a conservative choice to have a margin of an order of magnitude for each extreme, so the resulting capacitance has an optimum value of 5 μF, varying in the range $(500nF - 50\mu F)$. The output stage has been designed to satisfy the constrains imposed by the cell, and to handle the error tolerance, a trimming circuit has been implemented.

8 bits are required to cover 2 decades of possible values, so 8 branches are needed in which the transistors are weighted according to the bit that they represent. A switch is needed to access a single transistor; a code, provided from the outside world, manages the switches, generating a current proportional to it. An 8-bit calibration signal drives two batteries of switches from outside; in this way, it is possible to access nMOS and pMOS transistors separately. To generate a current proportional to the optimal configuration (without trimming), all the transistors have the same W/L as in the standard case and their parallelism is weighted according to the power of 2 with respect to the branch they occupy. For example, in the optimum case, the parallelism of the transistors of the output stage is equal to 25, and, to implement it, the trimming word must be equal to 00011001.

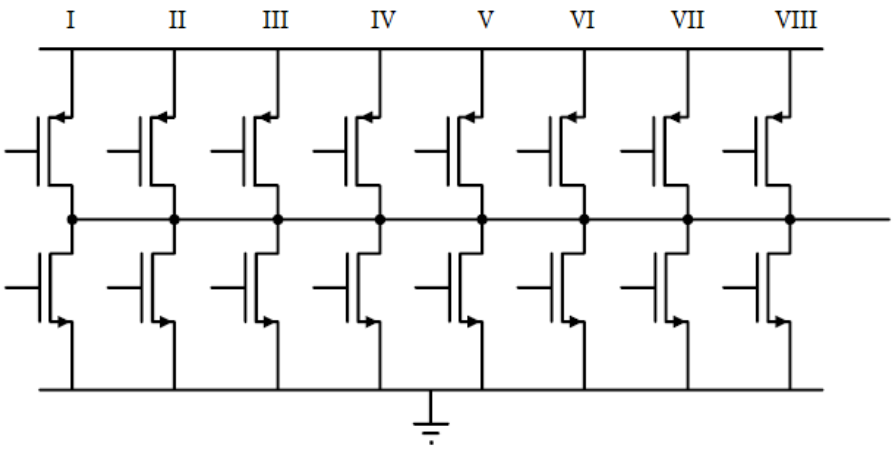


Figure 4.4: Output stage parallelism for each branch of the trimming circuit

	I	II	III	IV	V	VI	VII	VIII
W/L	$\frac{5\mu m}{1\mu m}$	$\frac{5\mu m}{1\mu m}$	$\frac{5\mu m}{1\mu m}$	$\frac{5\mu m}{1\mu m}$	$\frac{5\mu m}{1\mu m}$	$\frac{5\mu m}{1\mu m}$	$\frac{5\mu m}{1\mu m}$	$\frac{5\mu m}{1\mu m}$
Gates in parallel	1	2	4	8	16	32	64	128

Table 4.3: Output stage parallelism for each branch of the trimming circuit

During the design, two different approaches, detailed below, have been explored.

4.3.1 Gate-trimming circuit

In the gate-trimming circuit, the switches are placed on the gates of each transistor. In this approach, calibration signals enable each section of the trimming, making it sensitive to the out_dig_P or out_dig_N signals from the DIGOTA logic. When a section is disabled, the gate is driven to have its pull-up/pull-down devices always off, regardless out_dig_P or out_dig_N signals. This is a simple implementation and does not require modifying the architecture of an output stage. Each pMOS is on when both the driving signals are low, therefore an OR gate is needed; on the contrary, an nMOS is on when the digital output and the calibration signal are high, so an AND gate is required. It is possible to characterize the gate-trimming circuit using the truth tables defined by the digital output of the potentiostat and the calibration signal.

out_DIG_P	CAL_P	
0	0	0
0	1	1
1	0	1
1	1	1

Table 4.4: P-calibration truth table for gate-trimming circuit

out_DIG_N	CAL_N	
0	0	0
0	1	0
1	0	0
1	1	1

Table 4.5: N-calibration truth table for gate-trimming circuit

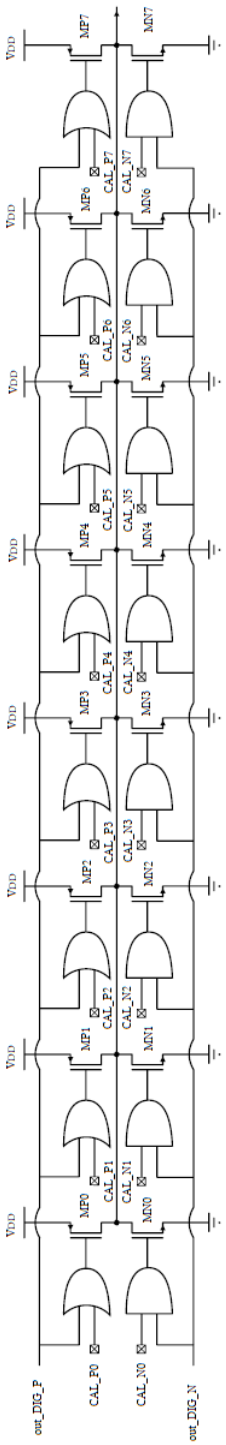


Figure 4.5: Gate-trimming circuit

This solution gave precise control of the output, although the main drawback is the delay accumulated through the logic gates in the case of large calibration codes. Sub-threshold standard logic cells, as discussed in detail later, present large delays varying environmental conditions, in particular with temperature. Large calibration codes involve the commutation of all the gates of the gate-trimming circuit; the resulting delay is too large and is not compatible with the constraints imposed by the clock signal. For this reason, this solution is not applicable to this trimming circuit, and it has been decided to move forward with a circuital topology that guarantees faster responses.

4.3.2 Drain-trimming circuit

In this approach, switches are placed on the drains of M5 and M6. These switches can be connected or disconnected according to calibration codes.

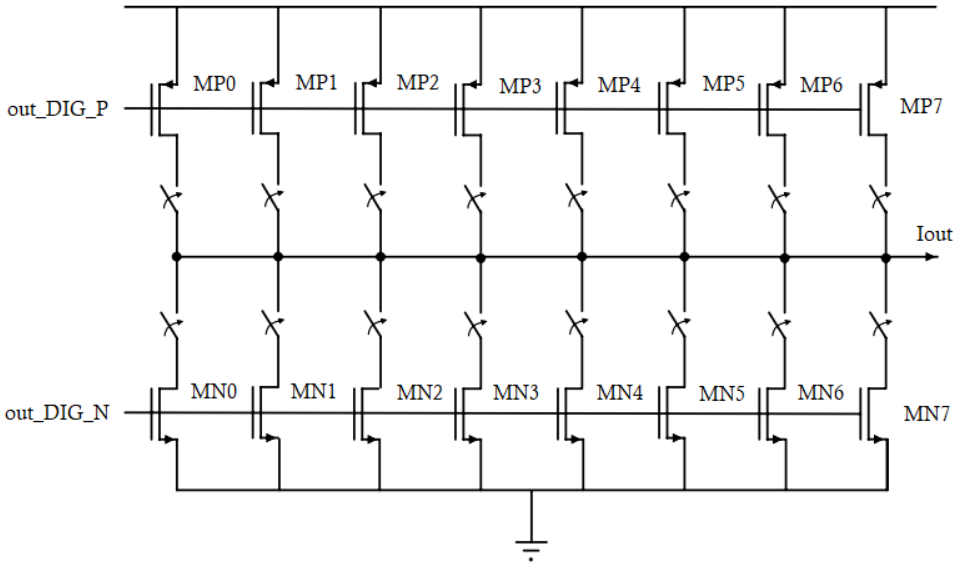


Figure 4.6: Drain-trimming general schematic

Switches are implemented with MOS transistors in sub-threshold region. The main goal of these switches is to provide a fast response with respect to the gate-trimming case, keeping the power consumption at the minimum value. For this reason the size of the transistor is kept as small as possible: the width has a really low value while the length is minimum. For the implemented switches,

the has been set: $\frac{W}{L}_{switch} = \frac{0.7\mu m}{0.13\mu m}$ Although, each switch must be able to handle the current generated by the corresponding transistor, to do this for each branch, the number of devices in parallel implemented for the switch is equal to the number of transistors implemented in parallel.

	I	II	III	IV	V	VI	VII	VIII
W/L	$\frac{0.7\mu m}{0.13\mu m}$	$\frac{0.7\mu m}{0.13\mu m}$	$\frac{0.7\mu m}{0.13\mu m}$	$\frac{0.7\mu m}{0.13\mu m}$	$\frac{0.7\mu m}{0.13\mu m}$	$\frac{0.7\mu m}{0.13\mu m}$	$\frac{0.7\mu m}{0.13\mu m}$	$\frac{0.7\mu m}{0.13\mu m}$
Gates in parallel	1	2	4	8	16	32	64	128

Table 4.6: Switches parallelism for each branch of the trimming circuit

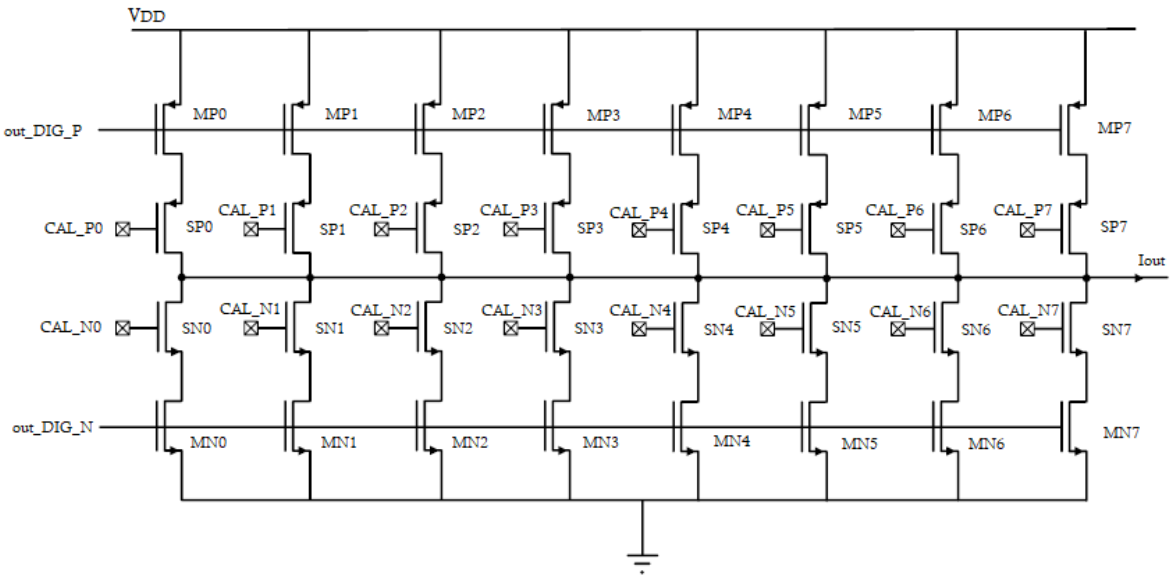


Figure 4.7: Drain-trimming circuit

This topology allows to guarantee the correct behavior of the system independently from the real capacitive value of the electrochemical cell. Anyway, for a circuit like this, is possible to predict an high power consumption compared to the targeted one. Because of this, a trimming circuit able to cover a lower tuning range has been designed starting from previous considerations. To distinguish them, the test chip described till now is called "Chip H", while the one with halved trimming circuit is called "Chip L".

4.3.3 Chip L design

The trimming circuit allows to have a reliable measure independently from the real error on the load capacitance estimation. Anyway, the drivers of the digital outputs need to be over-sized for a large calibration network like the one presented until now ("Chip H"), resulting in a significant increase in power consumption. This reason led to the design of a smaller trimming circuit. In particular, considering that the current flowing into the supply of the driving chain is of 4 nA, it has been possible to estimate a power consumption of 2 nW, which is therefore comparable with the overall consumption. The desired consumption should be negligible (in the order of the pico-watt); for this reason, the number of branches is cut to achieve this purpose. The branches of the trimming circuit are halved to reach a power consumption in the order of 500 pW. This reduction brought a simpler implementation and conspicuous power savings.

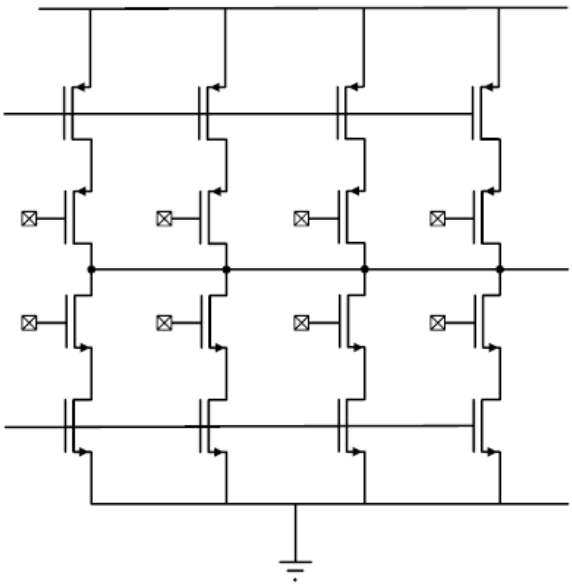


Figure 4.8: Chip L trimming circuit

4.4 Characterization of the logic ports

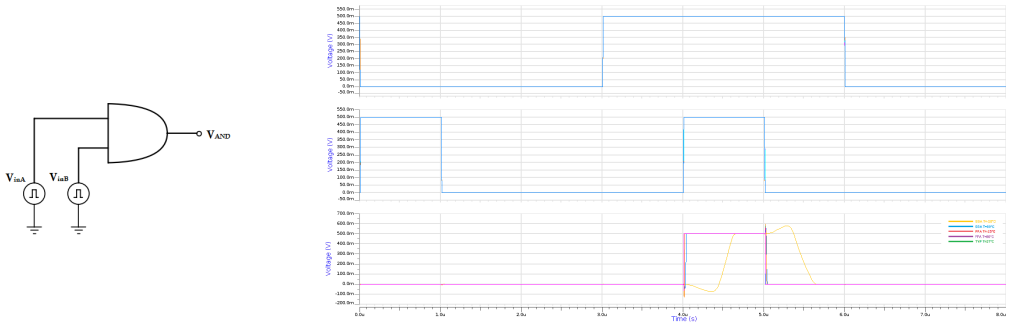
In this section, the characterization of the library standard cell is performed to ensure the correct behavior of the logic in a ULV/ULP domain. Each port is characterized with the given values V_{DD} and f_{CLK}; to verify the robustness of the design, the correct operation of the ports in the process' corners has been verified varying the temperature.
Process corners, in the fabrication of integrated circuits, refer to specific variations or extremes in the manufacturing process parameters that can affect the performance, reliability, and functionality of the product. These corners are defined to ensure that the manufactured ICs can operate under a wide range of conditions and meet their specified performance requirements.
Common process corners are listed:

- Nominal Process Corner: This is the average or typical manufacturing condition. It serves as a baseline for IC performances.
- Slow Process Corner: This corner represents the worst-case scenario for performance. It involves low V_t, higher process variability, lower V_{DD}, and lower temperature conditions. ICs manufactured in this corner are expected to operate slower but with greater reliability.
- Fast Process Corner: This corner represents the best-case scenario for performance. It involves high V_t, lower process variability, higher V_{DD}, and higher temperature conditions. ICs manufactured in this corner are expected to operate faster but may consume more power.
- Intermediate cases: In addition to the above, it is important to consider intermediate cases. For example, a low-power corner may involve a lower V_{DD} to optimize for energy efficiency.

By characterizing the IC under various process corners, it is possible to ensure the robustness and reliability of the prototype across a range of operating conditions. As discussed above, the slow corner turns out to be the most critical, in particular for ULV-ULP purposes; for this reason, particular attention is given to it.

4.4.1 AND port

To simulate the AND gate, two square waves have been used. An automatic tool from Cadence calculated the rising and falling time in the indicated conditions; as previously specified, a particular focus is given to border corners: SSA (slow-slow analog) at very low temperature and FFA (fast-fast analog) at very high temperature. The simulation setup is sketched below.



(a) Simulation setup **(b)** AND timing

Figure 4.9: AND gate characterization with V_{DD}=0.5V under process corner

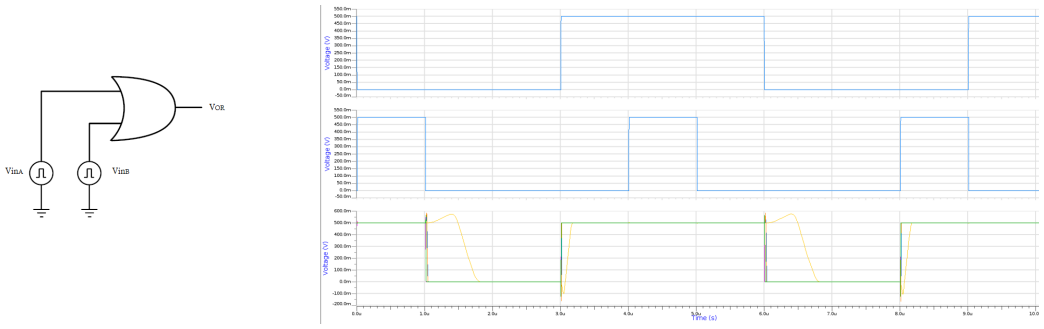
In the picture above, the results of the simulation are shown. The AND gate correctly turns on when both driving signals are high; the pace of commutations depends on the corner process. In particular, the yellow line represents the SSA corner at low temperatures, its delay with respect to the other cases is evident. A table showing the delays in different cases is reported.

T [°C]	Corner	$T_{rise}[ns]$	$T_{fall}[ns]$
27	TYP	6.99	6.49
-25	SSA	529.1	467.04
80	SSA	29.18	23.43
-25	FFA	11.43	18.56
80	FFA	3.16	3.7

Table 4.7: AND timinig table

4.4.2 OR port

The simulation setup for the OR port is equal to the previous case. Waveforms obtained by simulations are shown.



(a) Simulation setup **(b)** OR timing

Figure 4.10: OR gate characterization with V_{DD}=0.5V under process corner

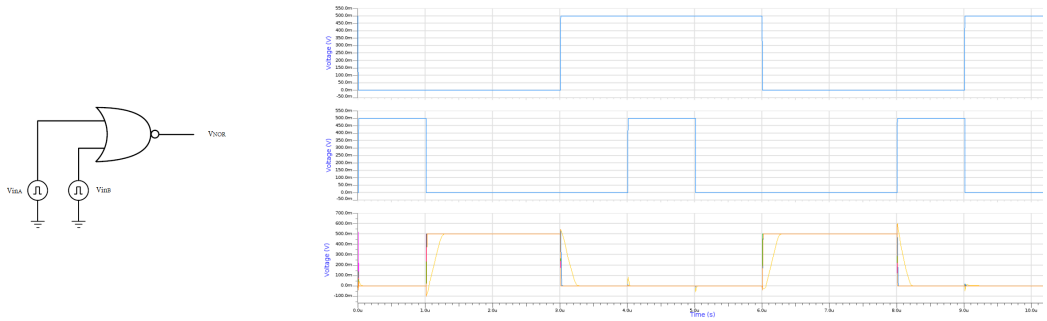
The OR gate correctly turns on when one of the two square signals is high. The simulated gate works correctly, but, as before, the process corner SSA (yellow line) has a huge impact on the commutations' time, as reported in the table below.

T [°C]	Corner	$T_{rise}[ns]$	$T_{fall}[ns]$
27	TYP	42.57	107.25
-25	SSA	637.42	889.95
80	SSA	126.73	221.22
-25	FFA	92.75	612.57
80	FFA	9.76	47.18

Table 4.8: OR timinig table

4.4.3 NOR port

The same pattern as before is followed for the simulation of the NOR gate.



(a) Simulation setup **(b)** NOR timing

Figure 4.11: NOR gate characterization with V_{DD}=0.5V under process corner

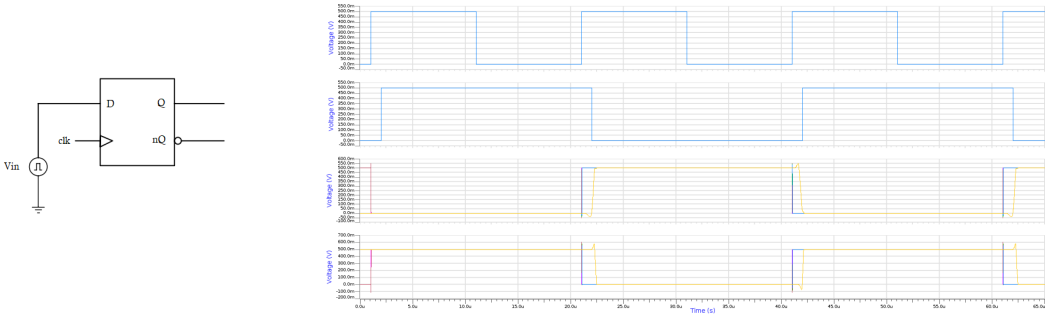
The output of the NOR gate is high when both input signals are zero. In this case, there are smaller delays, as reported below. This is due to the fact that the or gates are made up of nor gates followed by inverters; therefore, in this case, the delay due to the inverters is not present.

T [°C]	Corner	$T_{rise}[ns]$	$T_{fall}[ns]$
27	TYP	46.97	34.58
-25	SSA	272.79	181.55
80	SSA	271.75	25.12
-25	FFA	80.06	5.94
80	FFA	11.99	5.12

Table 4.9: NOR timinig table

4.4.4 Flip flop

D flip-flops are used in [11] to sample the input signal. These have been tested using a pattern similar to the previous one; a clock signal at the frequency of 50kHz is provided to sample the input data. The results are presented.



(a) Simulation setup **(b)** FF timing

Figure 4.12: Flip-flop characterization with V_{DD}=0.5V under process corner

The flip-flop correctly handles data, sampling on the rising edge of each clock period. The SSA corner process has a critical impact on its performance. With respect to sequential gates investigated previously, the FF has larger delays due to its complex structure; the inverted output (nQ) presents in general larger delay due to the presence of the inverter.

		Q		nQ	
T [°C]	Corner	T_{rise} [ns]	T_{fall} [ns]	T_{rise} [ns]	T_{fall} [ns]
27	TYP	45.83	38.28	47.75	54.75
-25	SSA	1120.22	804.33	1037.41	1341.56
80	SSA	52.41	41.37	51.75	63.05
-25	FFA	27.88	27.75	34.29	33.45
80	FFA	5.42	5.28	6.15	6.17

Table 4.10: FF timing table

Chapter 5

Results

In this section, the potentiostat's performance has been analyzed. Initially, a voltage-follower configuration has been tested to check the behavior of the DB-opamp, and then, the correct functioning of the complete potentiostat has been verified.
Only transient simulations have been performed because of the non-linearity of the circuit due to the presence of flip-flops. Simulations have been performed considering the choices explained in the previous chapters:

- V_{DD}= 0.5V
- f_{clk}= 50kHz
- V_{REF} = 200mV

The reference voltage (V_{REF}) has been set to 200 mV to exploit the oxidation peak of the nanostructured platinum depicted in Figure 2.12. To strengthen the parasitic capacitances at nodes A and B, two small MOM capacitors of the value of 50 pF have been inserted in the schematic. A metal-oxide-metal (MOM) capacitor is a metal capacitor constructed using an insulating layer of metal oxide between two conductive metal layers. This type of capacitor has been chosen for its small size. To improve the reliability of the prototype, it has been decided to insert a power-down (PD) signal to set the capacitances at nodes A and B at 0 volts when the circuit is turned on; this choice allows for one degree of freedom more during the prototype's test.

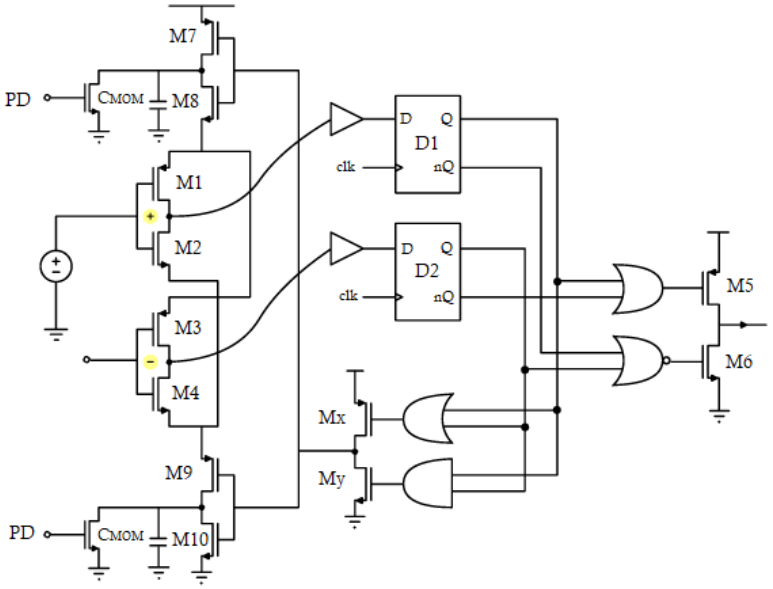


Figure 5.1: DIGOTA with PD signal and MOM capacitors

5.1 Voltage-follower configuration

Testing the correct operations of the DB-opamp becomes a crucial step to guarantee the correct operation of the potentiostat. For this purpose, a voltage-follower configuration has been used.

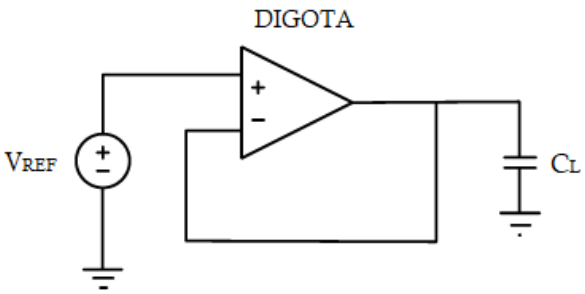


Figure 5.2: DIGOTA with voltage follower configuration and load capacitance

The DIGOTA has been tested by checking its operations in non-ideal environmental conditions. From the simulations has been possible to notice that the crucial process corner is the slow-slow (SSA) at low temperature: working in this corner at temperature lower than 0°C the response time of the circuit is too slow and it is not able to maintain correct operations. For this reason the functioning of the circuit is reported, as well as in the typical case, at the corners process borders.

- 0°C SSA corner
- 27°C Typical corner
- 80°C FFA corner

Anyway, considering the wearable purpose of the prototype, the expected temperature range for using the DB-potentiostat is (34-41)°C. All the simulations below are obtained with Cadence Virtuoso.

5.1.1 5 μF load

The waveform considering an optimum load ($C_L = 5\mu$F) are reported.

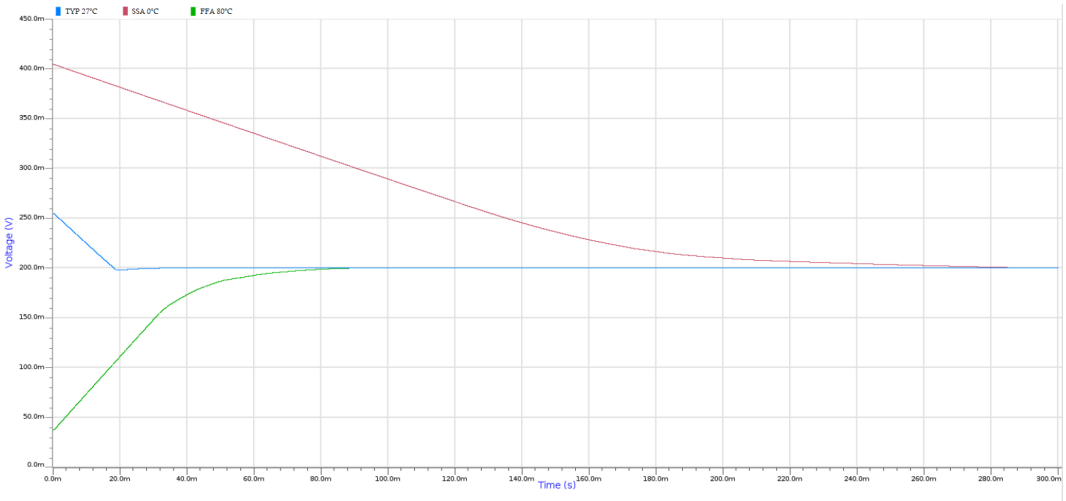


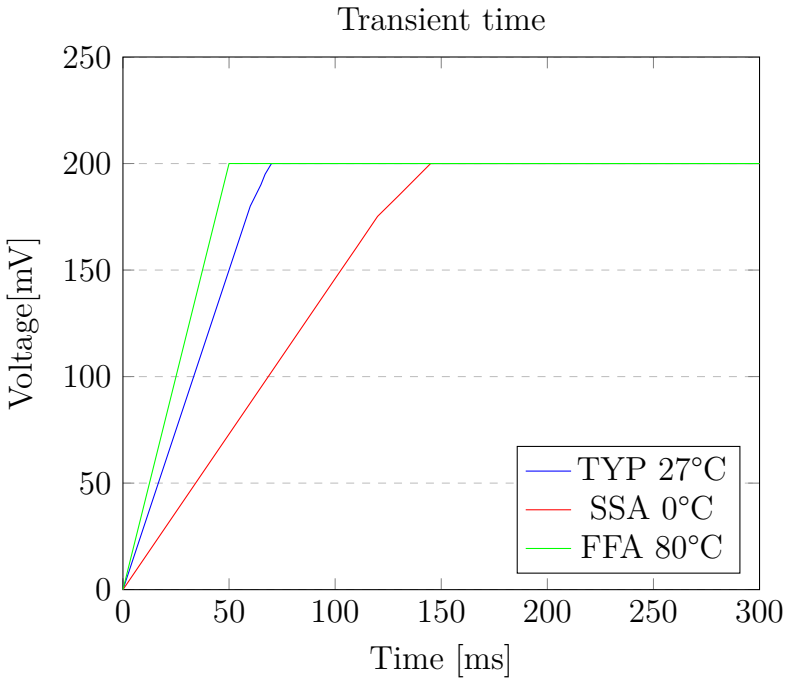
Figure 5.3: V_{OUT} transient response with load capacitance of 5μF

Performance analysis

Behavioral conditions have a crucial impact on the performances of the DIGOTA. The transient time has been evaluated as the time needed by the DIGOTA to

reach the desired output voltage (200mV); the power consumption, instead, has been calculated as the product of V_{DD} times the average current flowing into the DIGOTA's dedicated supply.

Is important to notice that, at the beginning of the transient, the simulator evaluates the bias point of the circuit, setting an initial value of V_{OUT}. Considering the slope of the output voltage in different conditions, the transient with a null initial output voltage is reported below.



Transient times and power consumption have been listed below.

T [°C]	Corner	Transient[ms]	Power consumption[nW]
0	SSA	145	1.22
27	TYP	67	19.1
80	FFA	42	350

Table 5.1: 5uF load Performance analysis

The performance of the typical case reflects what is expected: the transient time is around 60 ms, and the power consumption is in the order of nW. The

power consumption is an order of magnitude higher with respect to [11] because of the increase in V_{DD}. The conditions on the process corners involve the variation of parameters such as temperature, speed, and pressure. All these factors impact transient time and power consumption. In the SSA case, the power consumption is decreased with respect to the nominal case because a lower threshold leads to slower commutation of the circuit and consequently a lower amount of power dissipated. On the contrary, the FFA corner foresees a higher consumption of power and a faster transient.

5.1.2 0.5 μF load

The aim of this section and the following one is to check the correct behavior of the trimming circuit. To drive an output of 500nF, a trimming word equal to 3 has been used (25/2 = 2.5 rounded up). The results of the simulations are shown.

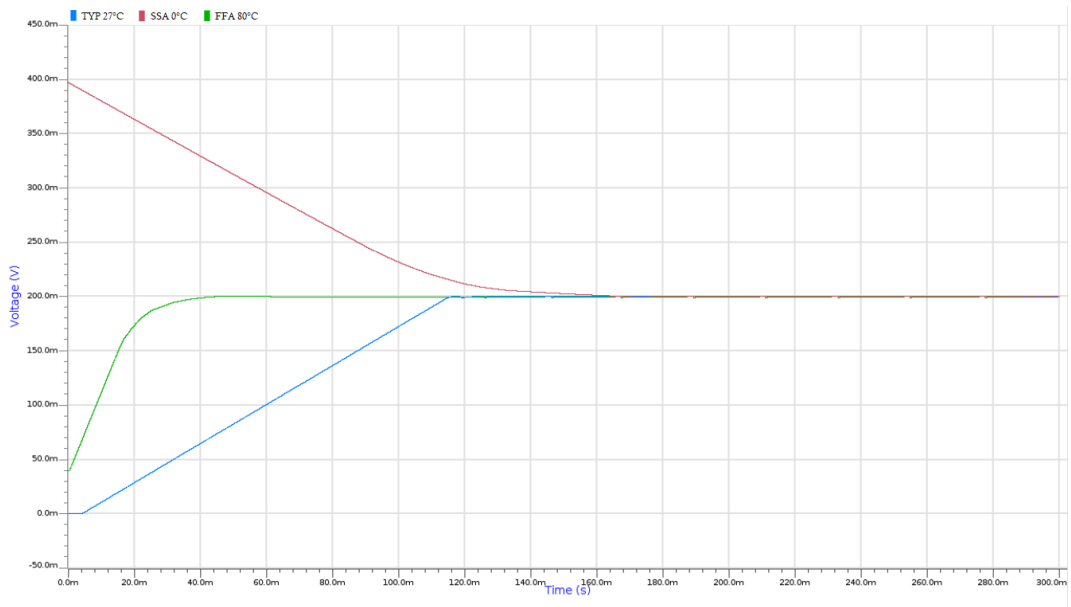
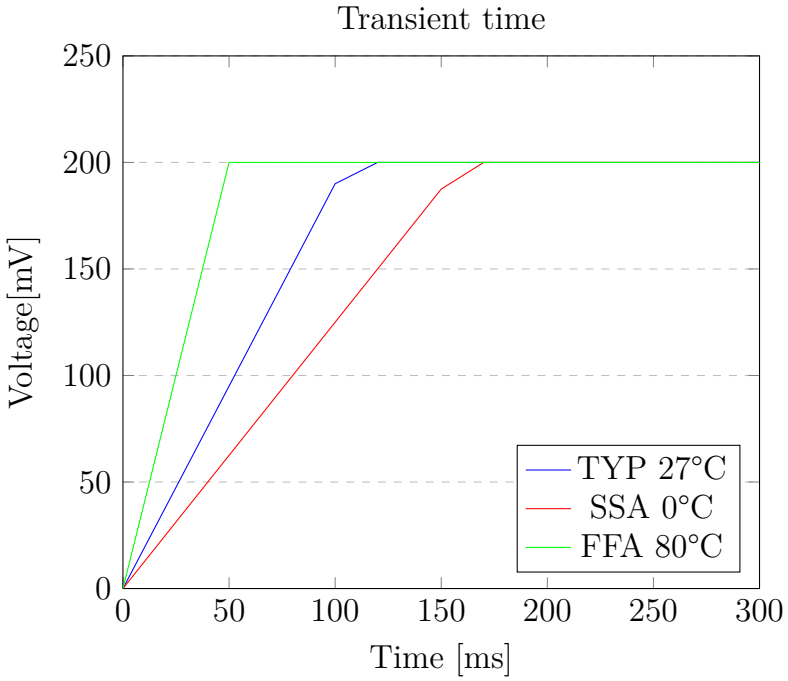


Figure 5.4: V_{OUT} transient response with load capacitance of 0.5μF

Performance analysis

Values of transient time and power consumption are listed.



T [°C]	Corner	Transient[ms]	Power consumption[nW]
0	SSA	170	1.15
27	TYP	100	20.35
80	FFA	55	143

Table 5.2: 0.5uF load Performance analysis

The obtained results are aligned with the ones obtained in the optimum case; the trimming circuit shows a good response in the outlined situation.

5.1.3 50 μF load

As before, the trimming circuit has been tested, and a large trimming word (equal to 250) has been used to drive an output of 50μF. The results of the simulations are shown.

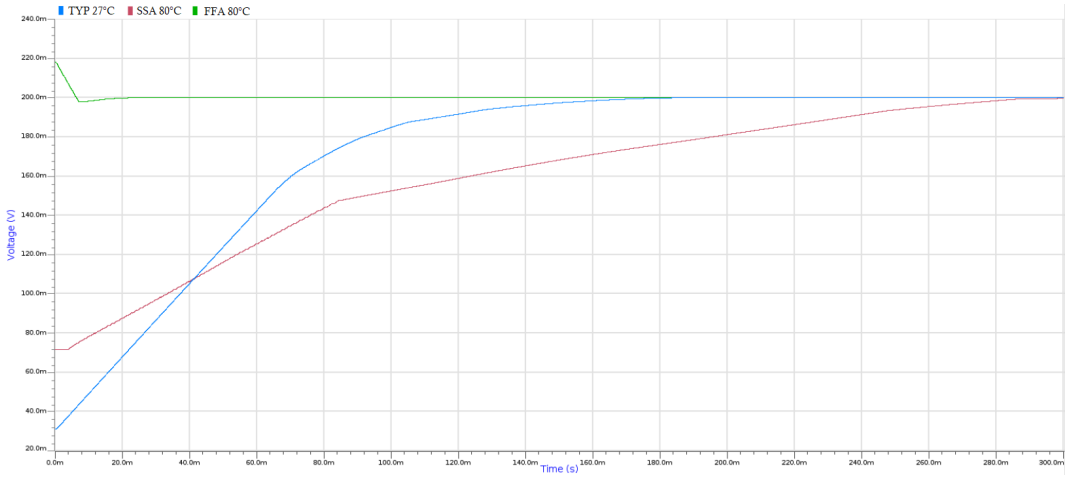
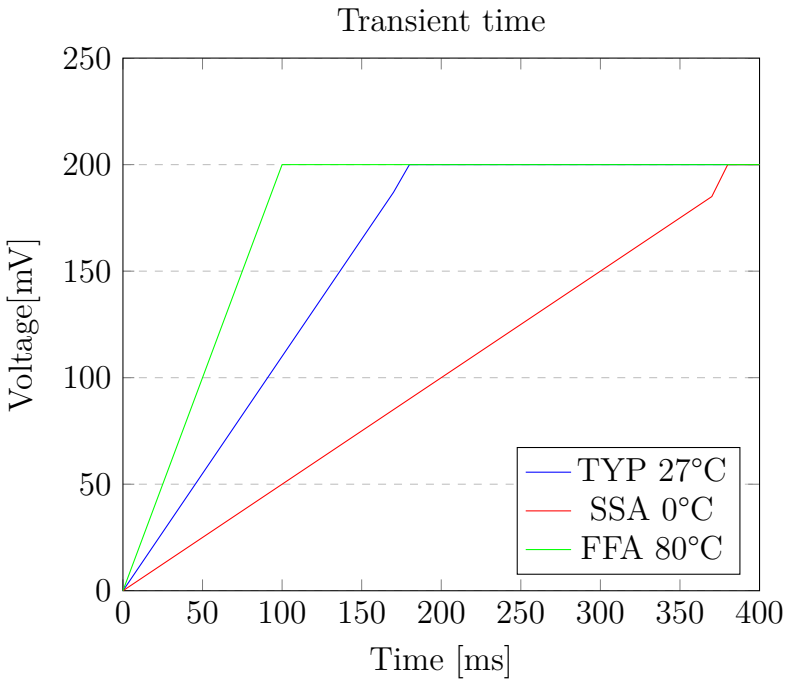


Figure 5.5: V_{OUT} transient response with load capacitance of 50μF

Performance analysis

Values of transient time and power consumption have been reported also for the case of C_L=50μF.



T [°C]	Corner	Transient[ms]	Power consumption[nW]
0	SSA	350	5.67
27	TYP	160	28.7
80	FFA	100	400

Table 5.3: 50uF load performance analysis

Due to such a high output capacitance value, the transient is dilated. Furthermore, charging this load for a long period of time requires greater power consumption than in previous cases.

5.2 Chip L results

This section is dedicated to the analysis of the results obtained from the testing of the chip L. A voltage follower configuration has also been used in this case; the considered output capacitance is in the order of C_L=500nF and a code equal to 3 has been provided to both the 4-bit calibration signals.

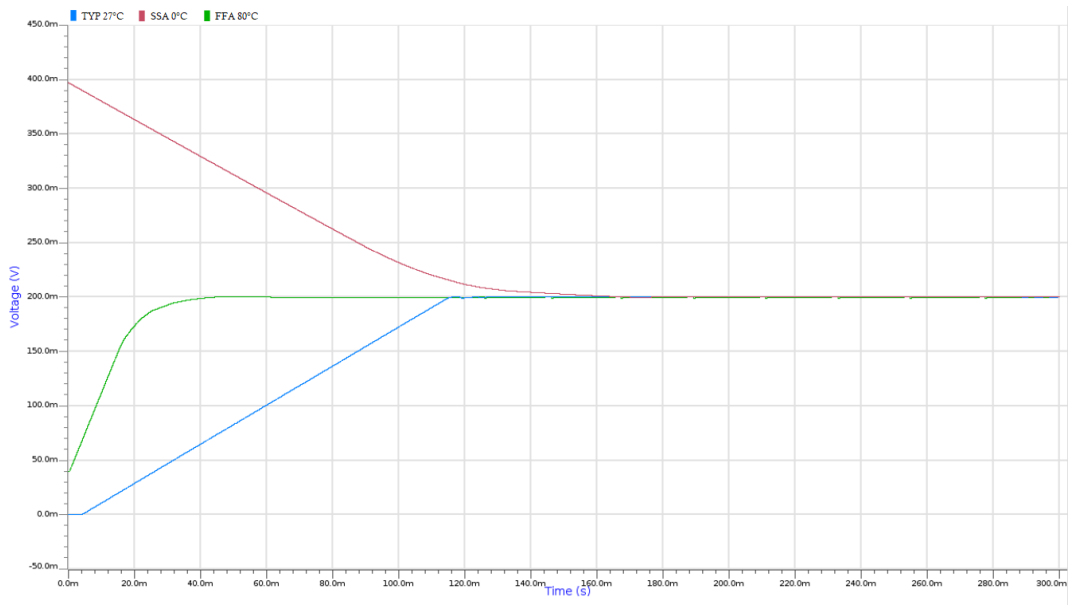
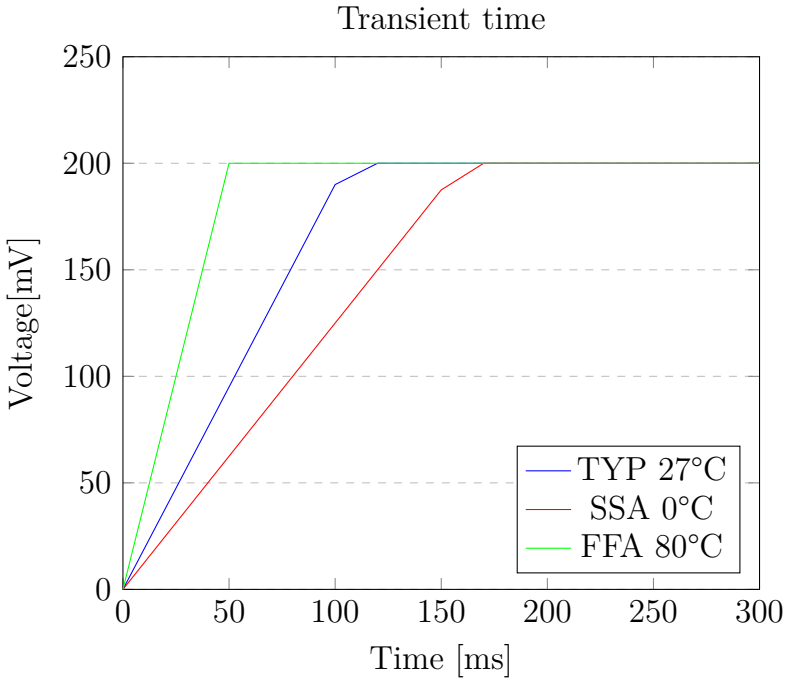


Figure 5.6: Chip L transient response



T [°C]	Corner	Transient[ms]	Power consumption[nW]
0	SSA	155	1.07
27	TYP	90	19.98
80	FFA	52	136.55

Table 5.4: Chip L performance analysis

As expected, performance is compliant with the results obtained in Section 5.1.2. It is important to underline that, in the typical case, the current flowing into the power supply dedicated to the driver chain is equal to $I_{scorp} = 410$nA, where V_{scorp} is the dedicated supply; the discussion concerning the power supply domains is deepened in the next chapter. The power consumption is around 200 pW, resulting negligible in the overall consumption.

5.3 Potentiostat configuration

Finally, the performance of the DB-potentiostat has been investigated. The circuit is made up of the DB-opamp in feedback with the electrical model of the electrochemical cell. The values of the components of the cell refer to Tables 2.1 and 2.2, and the cell's model that includes the faradaic current (Figure 2.15) has been used. I_f is set in order to have, during the acquisition time, a staircase current that simulates a variation of glucose of 10 mM.

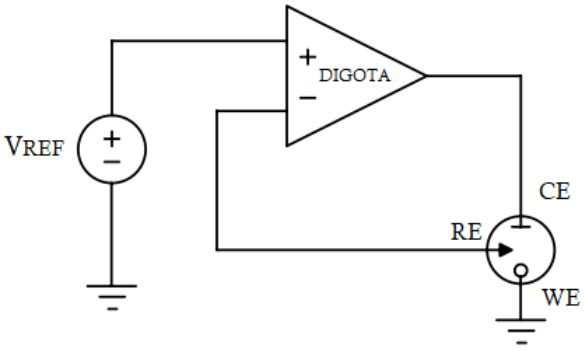


Figure 5.7: Potentiostat setup

Simulations needed to validate performance and operations under varying PVT conditions have been reported: convergence time and saturation time are validated during simulations, the error on the V_{RE} is evaluated, and the sensitivity of the circuit is obtained with post-processing simulations.

5.3.1 Transient response

In this section the transient response of the potentiostat under different PVT conditions is evaluated. The convergence time is the time needed by the potentiostat to reach the 200 mV working condition at the RE. The saturation time, instead, defines the time interval in which the acquisition can occur; after this period, V_{RE} diverges, and it is not possible to have other acquisitions if the circuit has not been reset. The potentiostat response is shown.

In the picture below the results obtained in typical conditions are shown. The acquisition window is equal to 2 seconds with a convergence time of 600ms and a saturation time of 2.6 s.

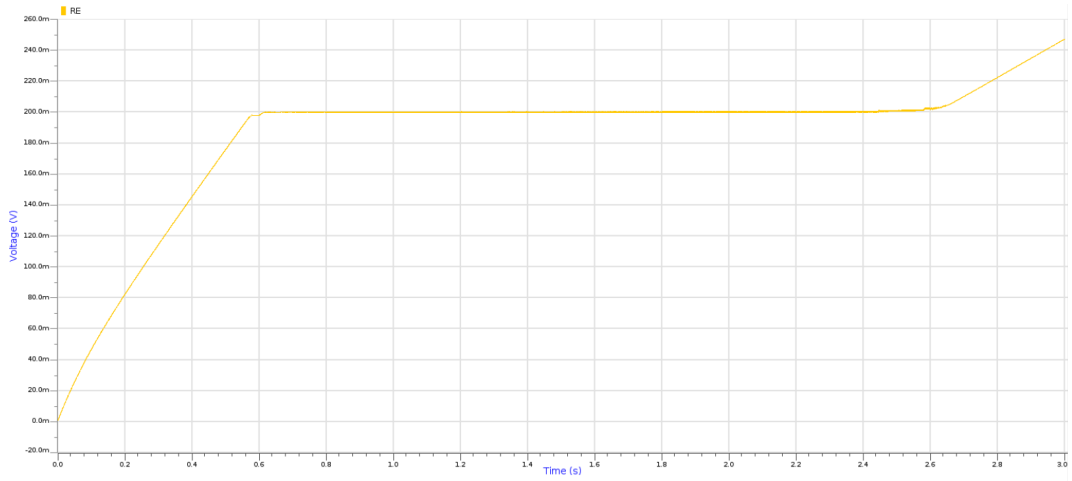


Figure 5.8: Potentiostat response with typical corner process @27°C

The SSA corner results are compliant with what expected: the convergence time is slower respect to the typical case and its value is equal to 0.8 s. The acquisition time is of 1.6 seconds since the saturation of the potentiostat occurs after 2.4 s.

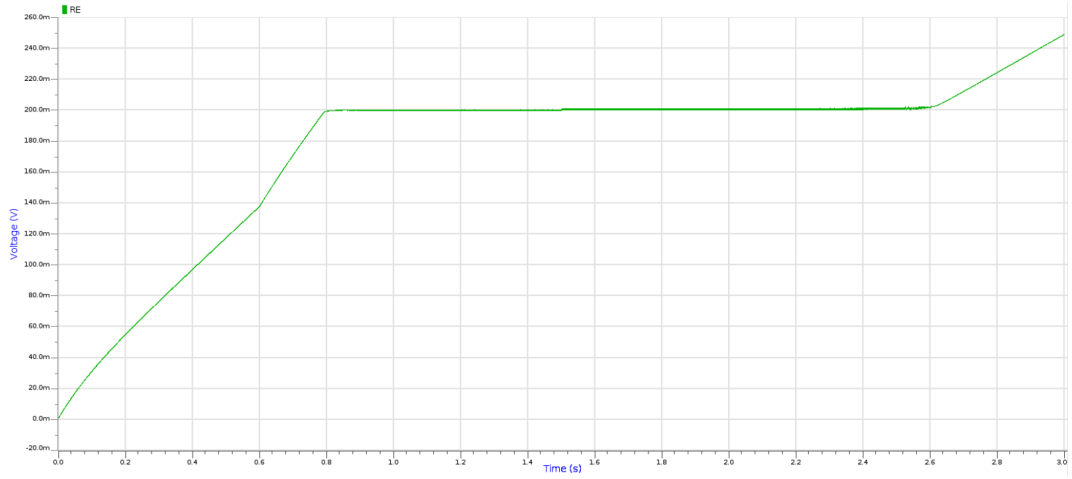


Figure 5.9: Potentiostat response with SSA corner process @0°C

The last case analyzed is the best for acquisition time: convergence time is smaller and equal to 0.4 s, saturation time is close to previous cases with a value of 2.5s, defining am acquisition interval of 2.9 s. Although the acquisition time is the best obtained, it will later be possible to see how this corner at very high temperatures will bring clear disadvantages in terms of error and

sensitivity

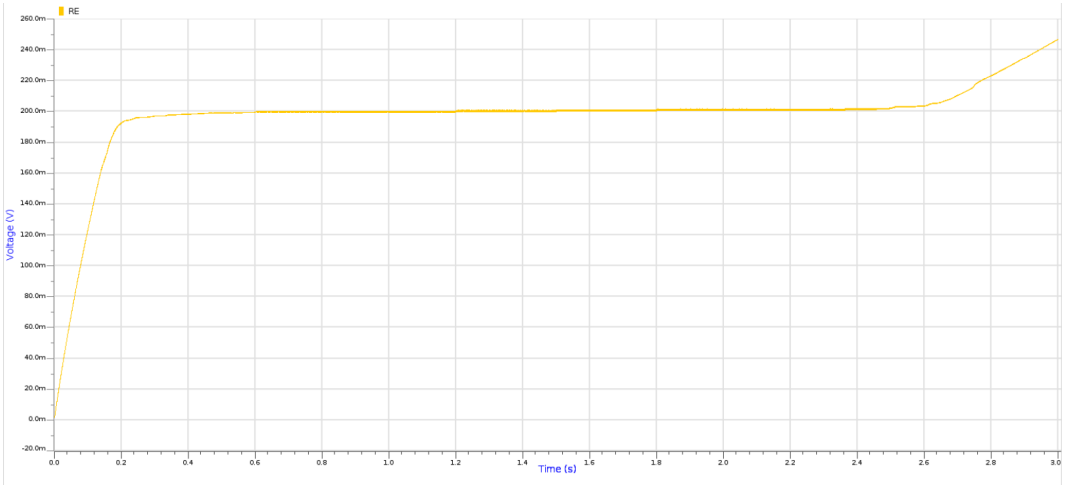


Figure 5.10: Potentiostat response with FFA corner process @80°C

Finally the different responses have been sketched on the same graph to figure out the variation of the acquisition window of the potentiostat.

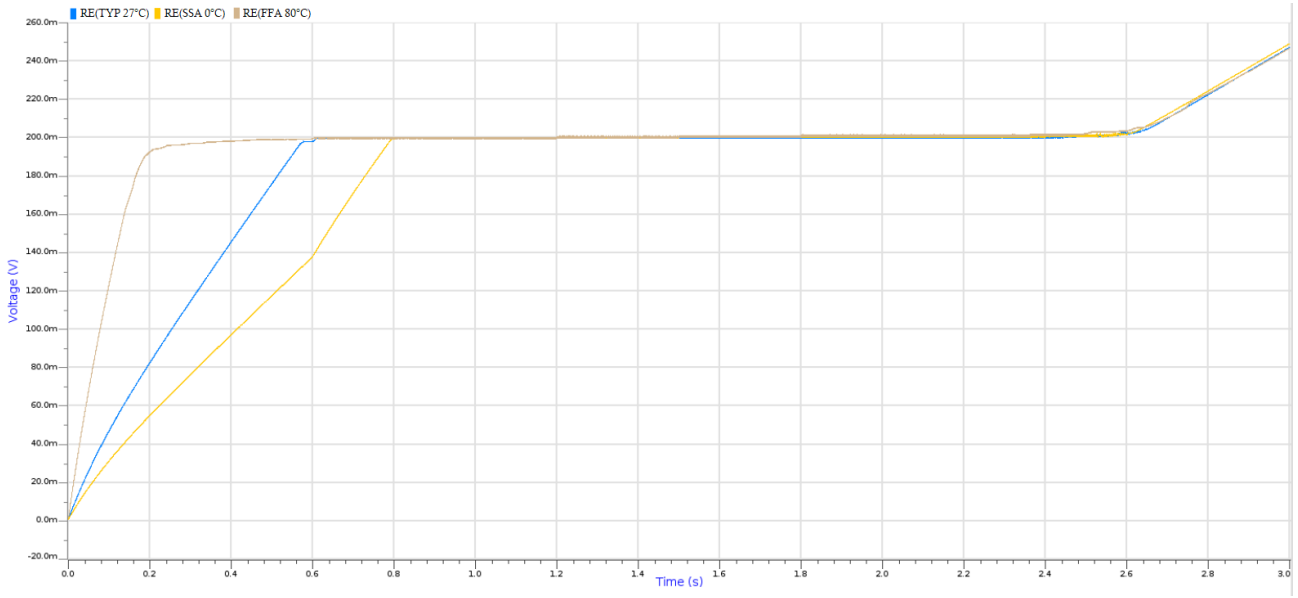


Figure 5.11: Potentiostat response comparison (in blue the TYP process corner @27°C, in red the SSA process corner @0°C, in green the FFA process corner @80°C)

T	Corner	$t_{convergence}$ [s]	$t_{saturation}$ [s]	$t_{acquisition}$ [s]
27°C	TYP	0.6	2.6	2
0°C	SSA	0.8	2.4	1.6
80°C	FFA	0.4	2.5	2.9

Table 5.5: Potentiostat timing

The data reported in the table above are coherent with the results obtained during the test of the DB-opamp: high temperatures and a fast process corner guarantee a faster response, contrary to what happens in the slow corner. The saturation time is nearly constant in both cases, so the polarizing current of the RE turns out to be nearly constant. The acquisition interval of the potentiostat at low temperature in the slow corner process is small compared to the others but still acceptable.

5.3.2 Steady-state error

The ripple of a signal is the periodic variation of its amplitude. It is important to monitor the variation of the voltage across the reference electrode in order to maintain the conditions required for a correct redox reaction. In this section, the error present on V_{RE} under steady-state conditions and its ripple have been evaluated. This is done by exploiting the measurement tool embedded in Cadence Virtuoso.

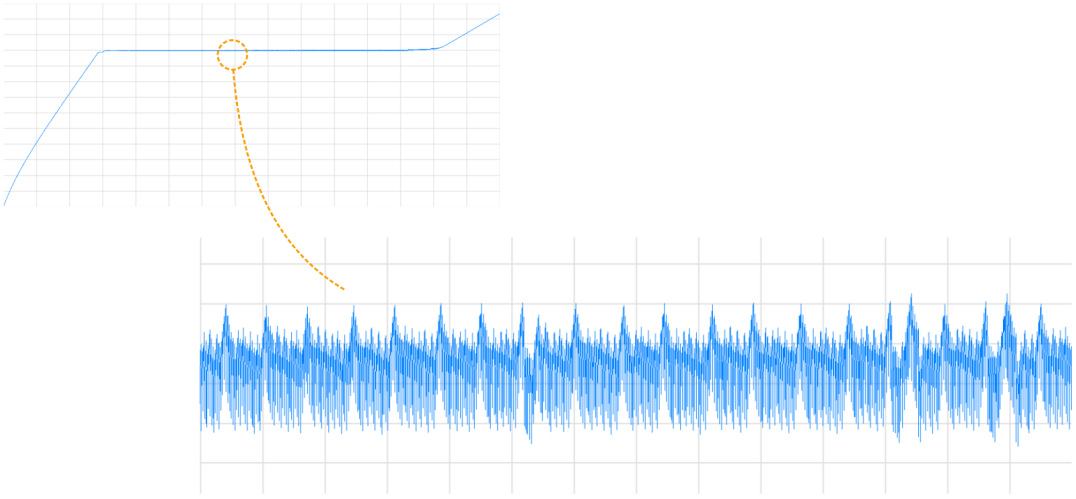


Figure 5.12: Error on RE voltage in steady-state

In the figure below is depicted the ripple of the V_{RE} in Figure 5.8 (typical process corner at 27°C). The peak-to-peak value (V_{REpp}) of the RE voltage is equal to 851.82μV, with a minimum value of V_{REmin} = 199.63mV and a maximum value of V_{REmax} = 200.48mV. The average value is of V_{REavg} = 200.16mV, so, an error of 160μV is present in steady state condition.

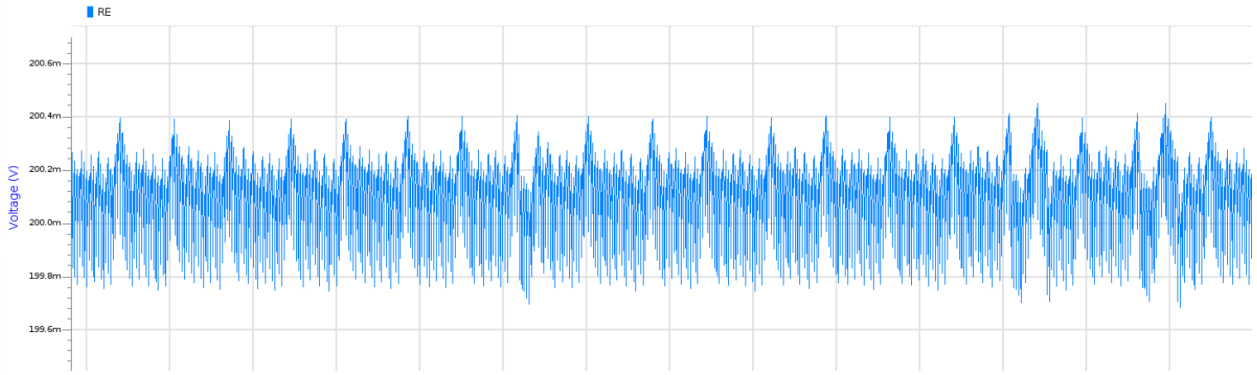


Figure 5.13: Ripple in the RE voltage under typical case

Due to slower commutations of the circuit, the ripple on V_{RE} in steady-state operation under SSA corner process at 0°C has been resulted slightly smaller. In this situation, the peak-to-peak value is of 623.78μV with a minimum and a maximum value of the RE voltage respectively of 199.80mV and 200.43mV; the average value of V_{RE} under SSA corner process at 0°C is 200.14mV. Despite of a reduced acquisition interval this operation condition returns a smaller error.

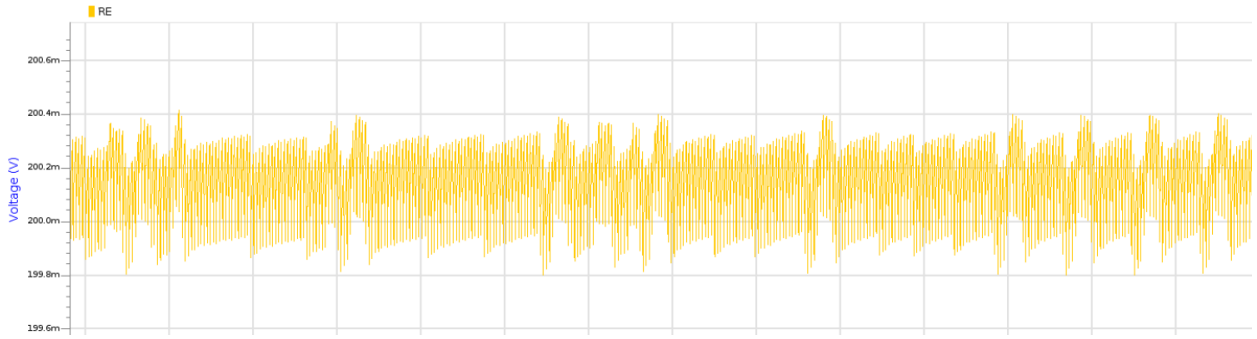


Figure 5.14: Ripple in the RE voltage under SSA case

The FFA corner process at 80°C represent the worst scenario in terms of error on the reference electrode voltage. Here, the peak-to-peak value of the ripple is of 1.15mV, the minimum value of voltage is of 199.81mV while the maximum value is of 200.96mV; the average voltage in steady-state operation is of 200.59mV.

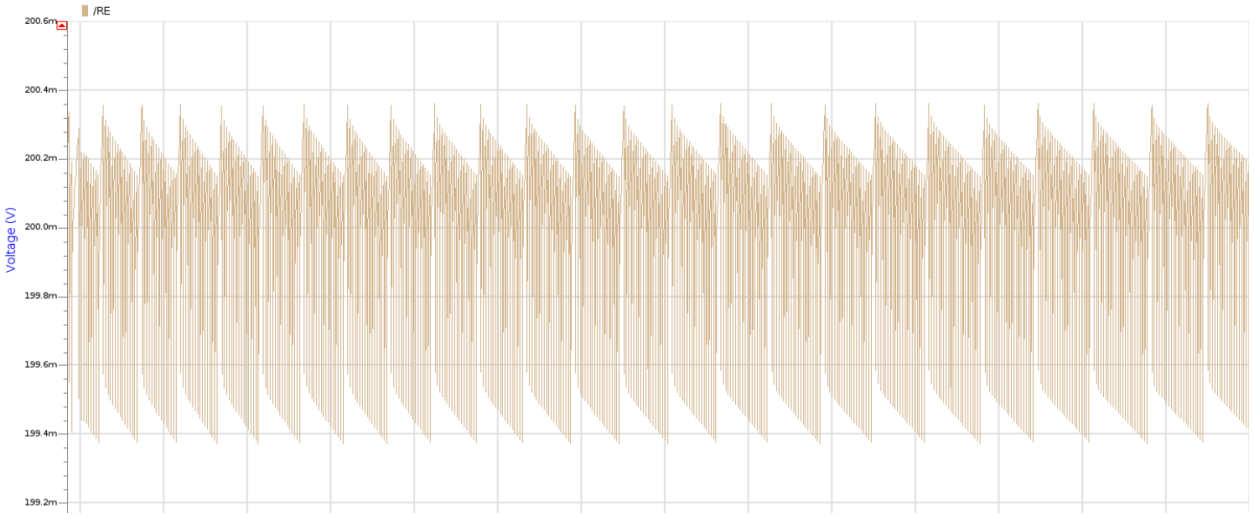


Figure 5.15: Ripple in the RE voltage under FFA case

The results presented in this section are summarized below.

T	Corner	V_{REavg}[mV]	$V_{REpp}[mV]$	V_{REmin}[mV]	V_{REmax}[mV]
27°C	TYP	200.16	0.85	199.63	200.48
0°C	SSA	200.14	0.62	199.80	200.43
80°C	FFA	200.59	1.15	199.81	200.96

Table 5.6: Potentiostat errors on V_{RE}

5.3.3 Post-Processing evaluation

The sensitivity represents the increase in the binary code (ΔCODE) compared to the increase in the glucose concentration (ΔC) in steady state. Exploiting post-processing tools from work [11] (reported in Appendix A), it is possible to evaluate the current sensed by the system from the simulations. In particular, the moving average of the digital outputs of the potentiostat has been calculated, and considering the total number of current pulses in the acquisition window, the expected faradaic current is returned.

The least significant bit (LSB) has been evaluated considering the minimum current that, in this circuit, can be translated into the digital domain. The minimum representable current is given by the division of a single current pulse by the number of clock cycles.

$$LSB = I_{pulse}/N$$

The stream has been averaged over N = 1024 clock cycles, and the code/concentration curve shows a sensitivity of 41 LSB/mM in the optimal case. Below are the sensitivity graph and the chronoamperogram under 2mM injections.

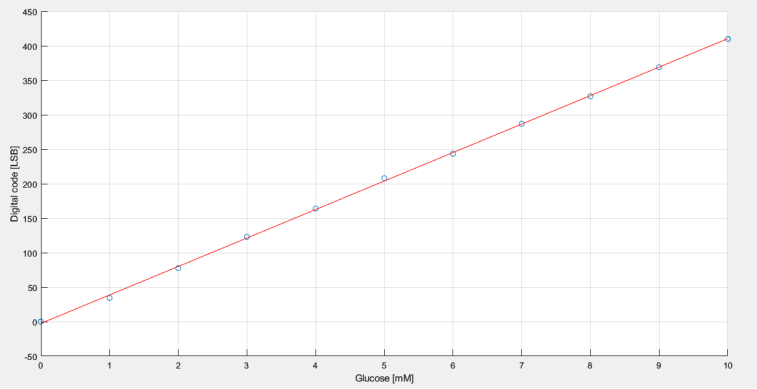


Figure 5.16: Sensitivity with typical process corner @27°C

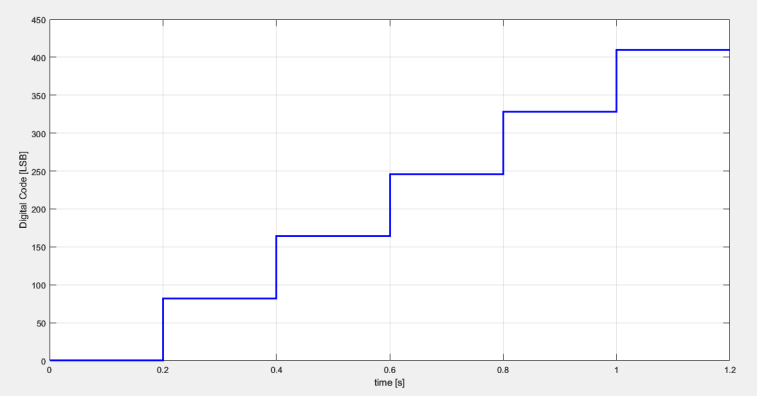


Figure 5.17: Staircase acquisition with typical process corner @27°C

The sensitivity of a measurement in an IC refers to how much the measurement is affected by variations in process parameters. The sensitivity has been evaluated also in non-ideal cases. The potentiostat becomes more sensitive to changes in slow process parameters at low temperatures, meaning that small changes in temperature can have a significant impact on circuit performance. On the contrary, in fast process parameters at high temperatures, the sensitivity decreases despite the acquisition interval is increased. Below the border cases are depicted.

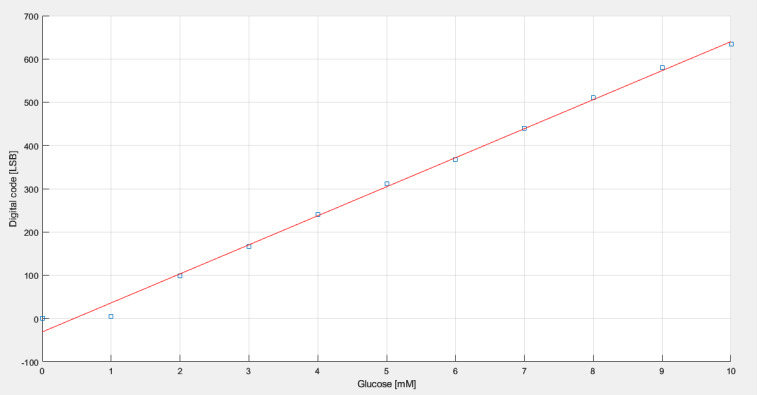


Figure 5.18: Sensitivity with SSA process corner @0°C

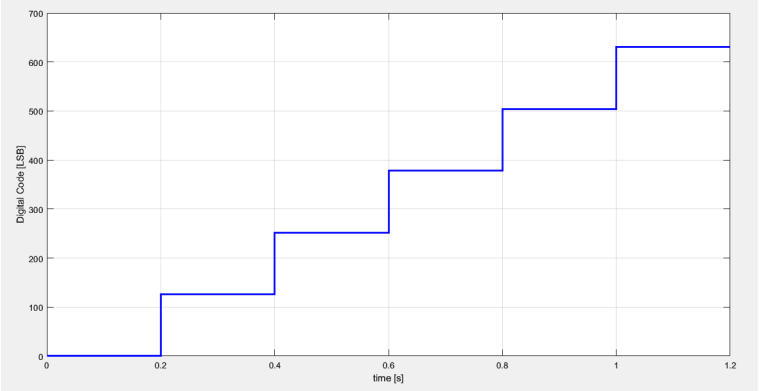


Figure 5.19: Staircase acquisition with SSA process corner @0°C

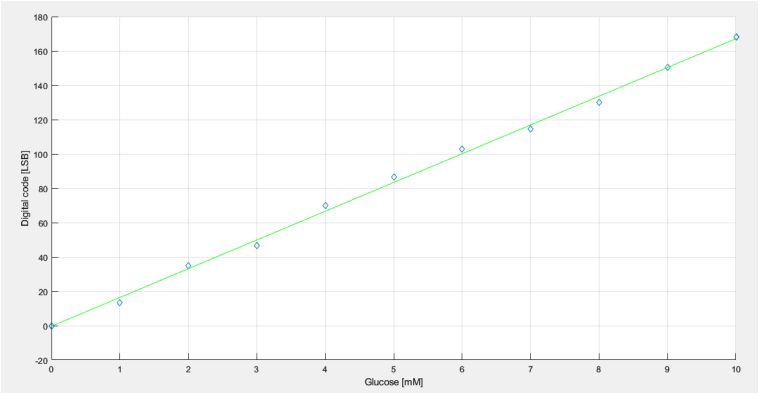


Figure 5.20: Sensitivity with FFA process corner @80°C

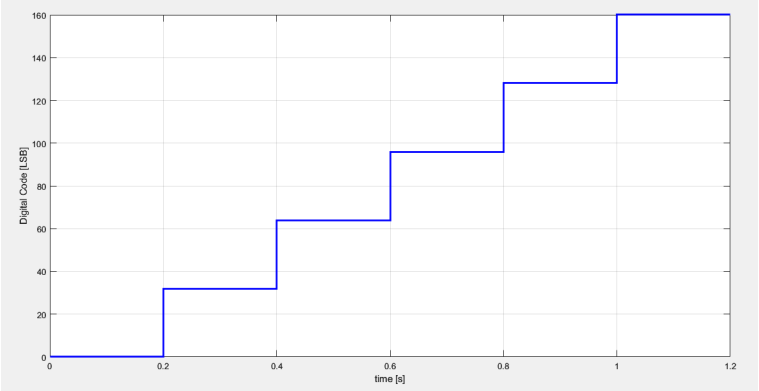


Figure 5.21: Staircase acquisition with FFA process corner @80°C

Finally, the sensitivities have been plotted on the same graph to underline the variations due to different PVT conditions. In blue, the typical case represents what discussed previously. The SSA process corner at low temperatures (in red) brings a significant increment of the slope of the sensitivity while, on the contrary, the FFA corner at high temperatures (in green) decreases the slope of the line. The improvement of the sensitivity on the SSA process corner at low temperature means that the system responds more noticeably and quickly to variations of the concentration of glucose. This is mainly due to the slower commutation of the circuit that allow an improved sensing, despite a smaller acquisition interval. On the contrary, the FFA corner at high temperature case has a larger acquisition window but faster switching leads to a decrease in the sensitivity.

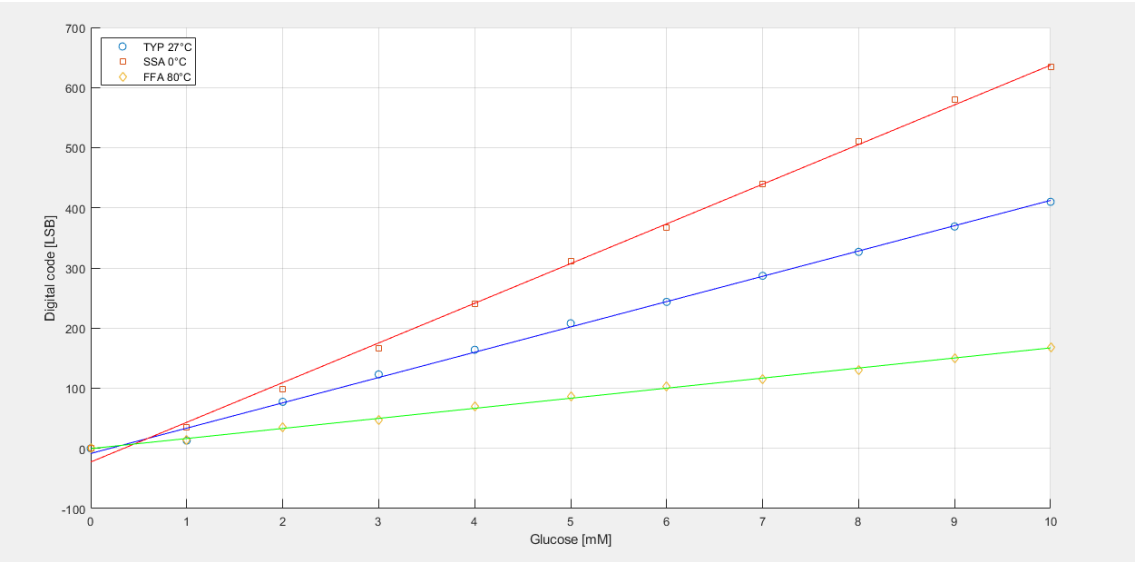


Figure 5.22: Sensitivity comparison (in blue the TYP process corner @27°C, in red the SSA process corner @0°C, in green the FFA process corner @80°C)

Chapter 6

Layout and PLS

In this chapter, the choices made for the supply domain are explained, and the design of the schematic of the pad ring is defined. The layout of both the schematic and the pad ring is performed to have a physical verification of the prototype. At the end of the chapter, post-layout simulations (PLS) are performed to verify the physical behavior of the prototype.

6.1 Power supply domains

In general, splitting the supply voltage into several domains is a useful practice for different reasons, among them increasing the power efficiency, reducing the power consumption, reducing interferences, and improving reliability. This design presents five separate supply domains: four analog domains and one digital domain, as follows:

- VDD_OPAMP_0V5, power supply dedicated to the DB-opamp to evaluate the power consumption;
- VDD_DIG_0V5, dedicated supply for the output stage; in this case, this is done to reduce the possible interferences on the output;
- VDD_SCORP_0V5, power supply dedicated to the trimming driving chain. Its consumption is comparable to the DIGOTA one; for this reason, an intended power supply is provided;
- VDD_AUX_0V5, auxiliary analog domain used to supply the trimming circuit;
- VDD_ANACLAMP_0V5, analog supply rail.

Each supply domain has its own ground reference (i.e., VSS_OPAMP_0V5).

6.2 Top design

To define the physical organization and arrangement of components and interconnections within the IC, the top schematic has been defined. The needed pads are 33, and their functions are listed below.

- 10 supply pads, organized as previously specified;
- 23 I/O pads, among which:
  - 2 inputs (IN_P, IN_N)
  - 1 analog output to put the prototype in feedback with the electrochemical cell (OUT)
  - 2 digital outputs to collect the useful pulses (OUT_DIG_P, OUT_DIG_N)
  - 1 clock signal (CLK)
  - 1 power-down signal (PD)
  - 16 calibration signals (CAL_P<0:7>, CAL_N<0:7>)

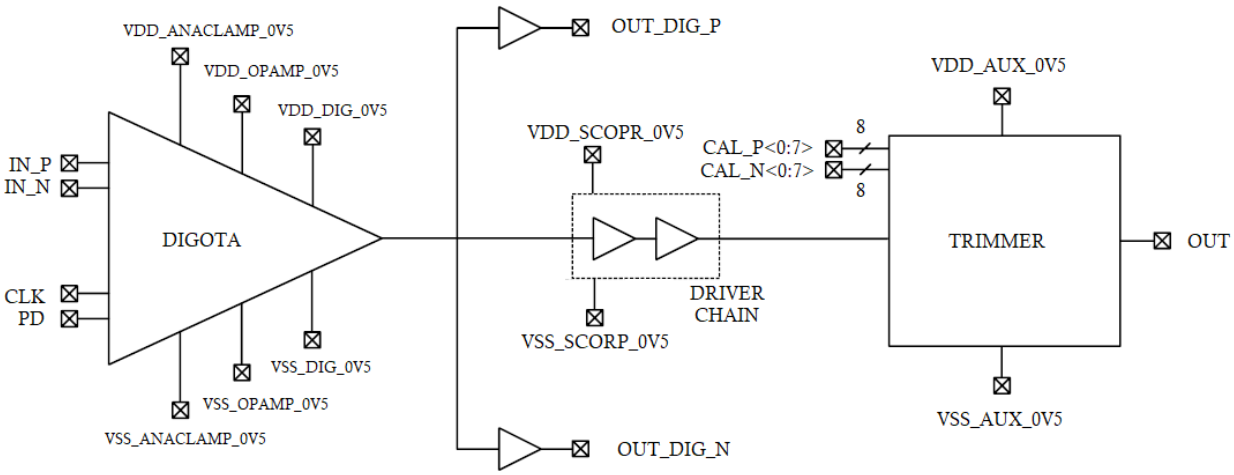


Figure 6.1: Top schematic

It is possible to notice that the digital output (OUT_DIG_P, OUT_DIG_N) are driven as explained in section 4.2.2.

6.3 Design of the Pad Ring

The pad ring has been designed to have a square shape. The left side is dedicated to the analog pads, both for supplies and I/O pads; similarly, the bottom side includes the digital pads, both digital supply and I/O pads. Each of the other two sides is dedicated to one of the 8-bit calibration signals, with the difference that, for space reasons, the right side also contains the pads used for the auxiliary power supply. The total dimension of the pad ring turns out to be equal to 14.4mm^2.

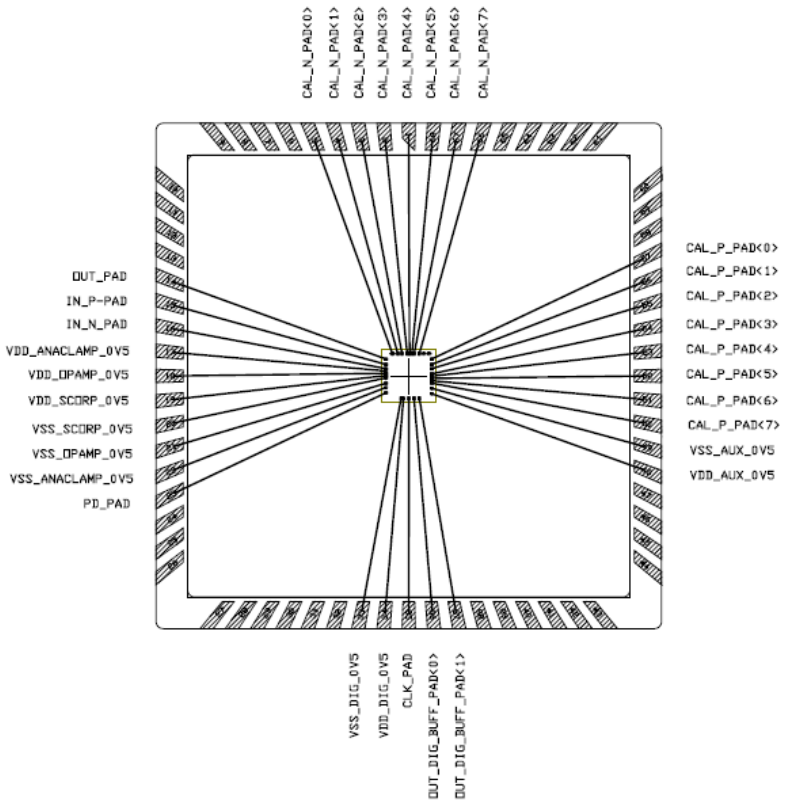


Figure 6.2: Pad ring

The pad ring of the chip L is shown below. The same reasoning have been used in its design but the connected calibration signals are halved.

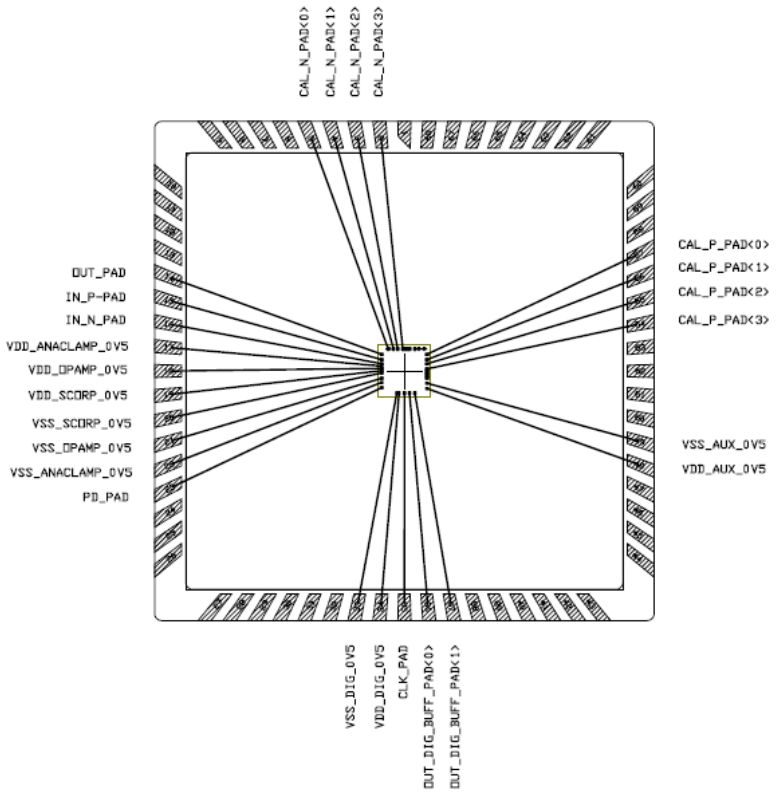


Figure 6.3: Chip L Pad ring

6.4 Layout

ICs manufacturing process require physical layouts for several reasons, in particular to perform Post-Layout Simulations (PLS) considering non-idealities due to physical constrains. To faithfully follow company production standards, the layout of the DB-potentiostat was done in collaboration with STMicreoelectronics.

6.4.1 Schematic layout

The layout of the DIGOTA is depicted below. The value of its area is of $1104\mu m^2$, resulting comparable with the targeted dimensions for wearable applications. Despite the extremely small size of the circuit, it is important to notice that the dimensions of the 50 pF capacitance and of the driving circuit bring a strong increase in the prototype area with respect to the ideal case. The size of the

trimming circuit leads to an over-sizing of the area of the prototype (Figure 6.6). For each pad, both for the supply and for I/O pads, have been used ESD protection diodes. This is done because protection diodes in IC layouts play a critical role in safeguarding sensitive electronic components from electrostatic discharges, overvoltages, and transients, thereby ensuring the robustness and reliability.

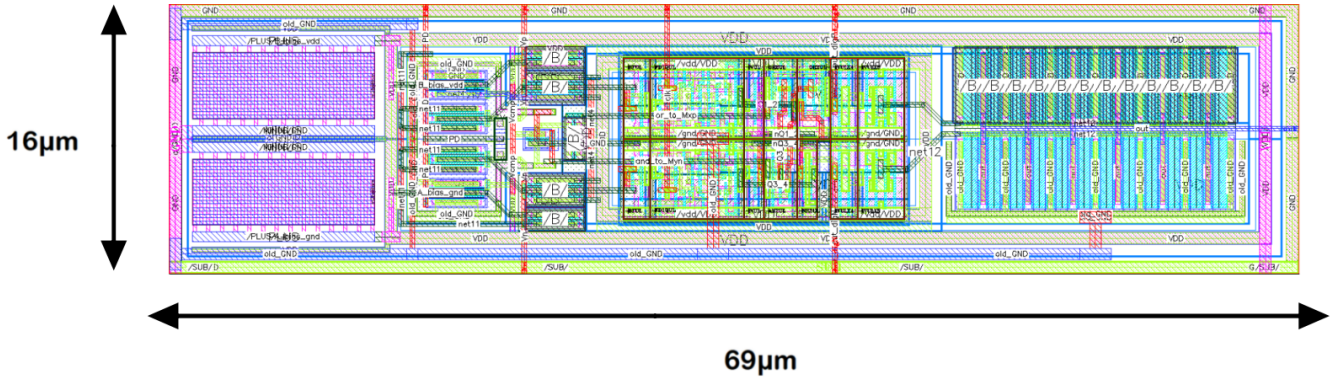


Figure 6.4: DIGOTA layout

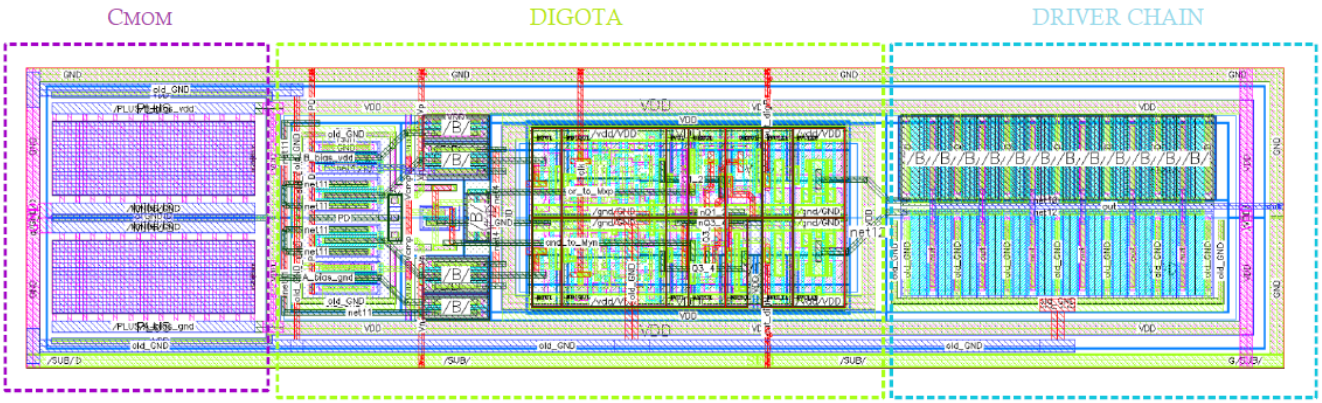


Figure 6.5: DIGOTA layout stages

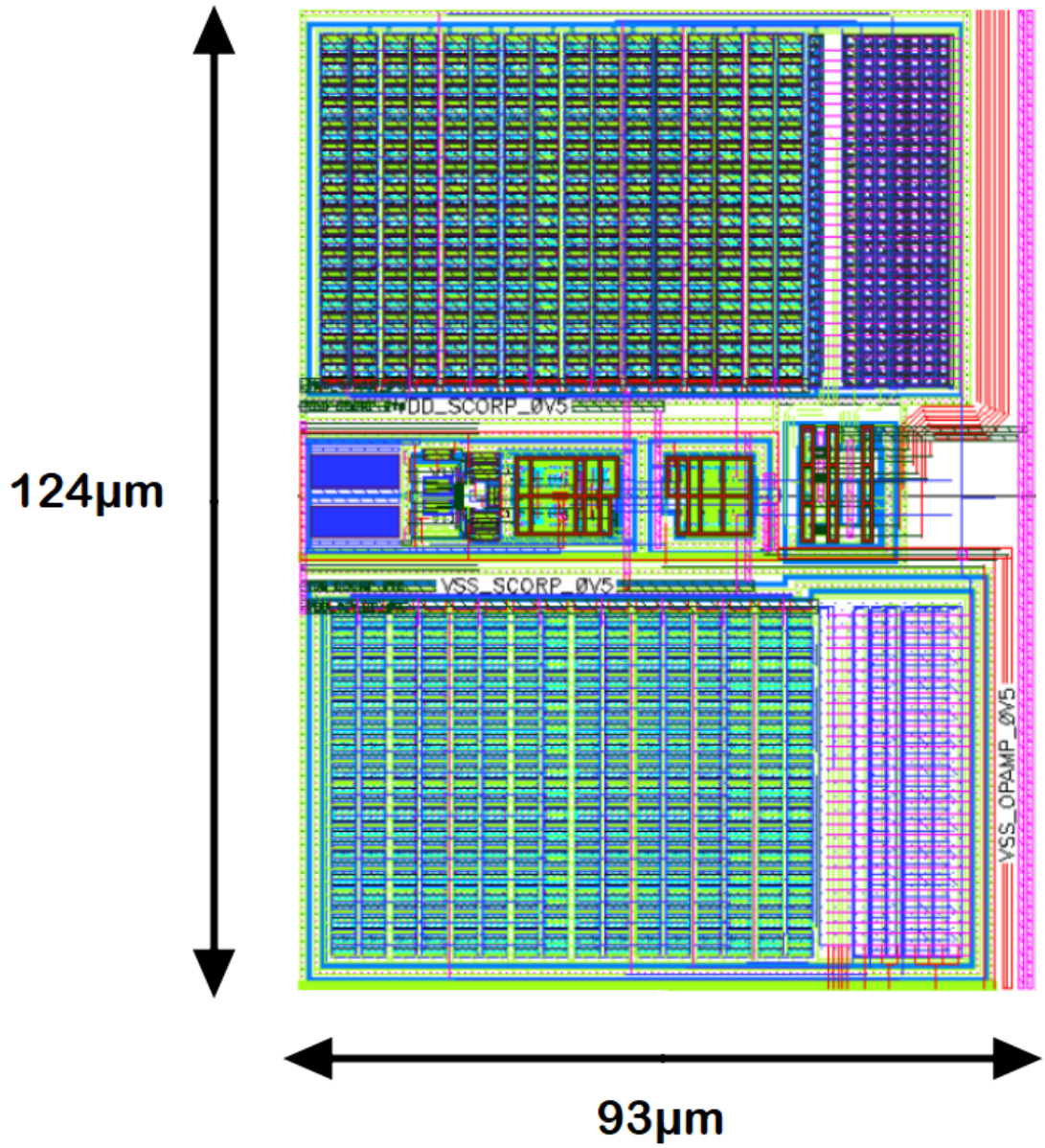


Figure 6.6: DIGOTA layout with trimming circuit

6.4.2 Top layout

In this section, the physical implementation of the pad ring in Section 6.2 is reported. This defines the physical arrangement of how the components of the potentiostat are positioned and connected on the chip's surface.

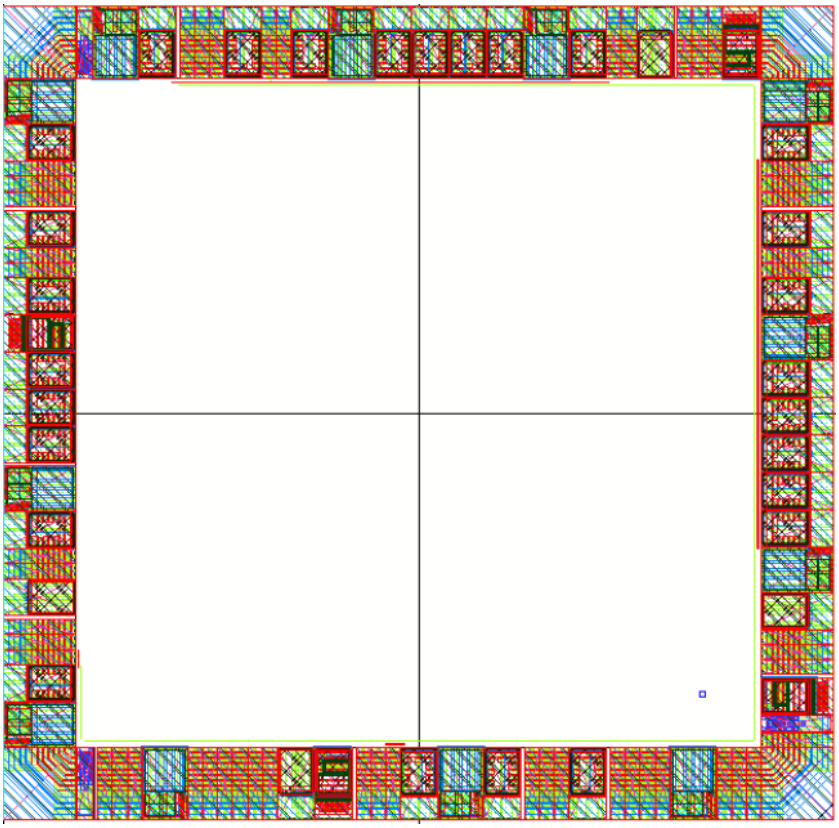


Figure 6.7: Layout of the pad ring

6.5 Post-Layout Simulations

Post-layout simulations (PLS) are a crucial step in IC manufacturing; they validate the performance of the prototype under real-world conditions, considering parasitics and effects due to the pads. Internal interconnections include conductive path between components, introducing capacitive effects. The pads are the contact area between the chip and the external world. PLS are essential to assess how signals pass through them, avoiding issues like delay or interference. In this section, the PLS needed to validate the results shown in Chapter V are presented.

6.5.1 Voltage follower configuration

In this case, the first step consisted of the evaluation of the DIGOTA. The physical layout of each component and physical pads are taken into account during simulations. The voltage follower configuration is tested with a load capacitance of 5μF in the process corners.

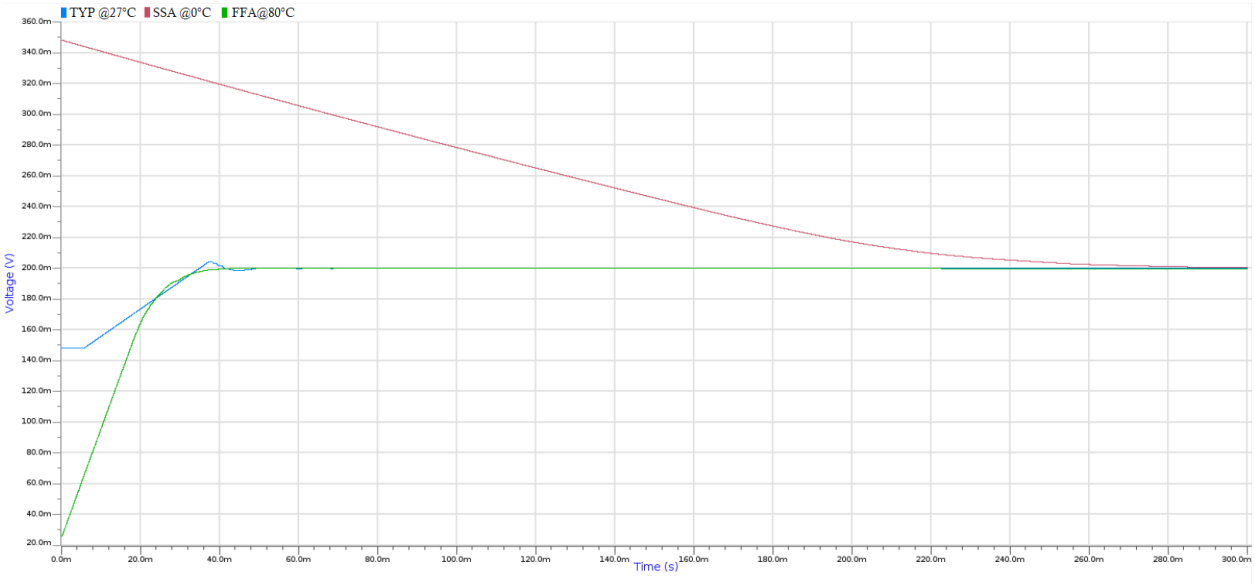
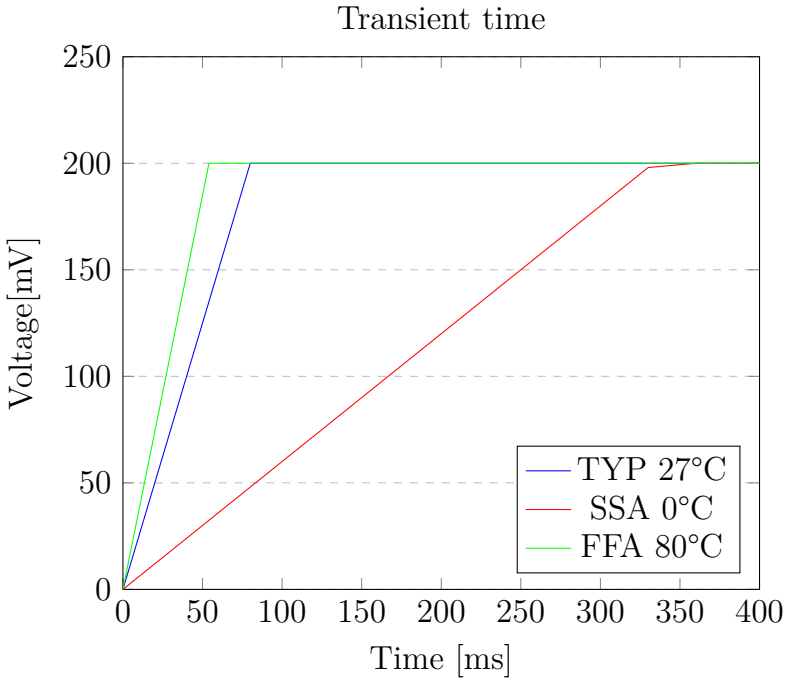


Figure 6.8: Voltage follower PLS



T [°C]	Corner	Transient[ms]	Power consumption[nW]
0	SSA	350	1.67
27	TYP	80	20.08
80	FFA	55	390.91

Table 6.1: PLS with 5μF load performance analysis

Comparing these results with what is obtained in Section 5.1.2, it is possible to notice that the transient time is slightly expanded, like the power consumption. This is attributable to parasitic capacitances that, despite their negligible value, have a light impact on the overall performance. Moreover, it is possible to notice the effects of non-idealities through the spikes on the obtained waveforms, as shown below.

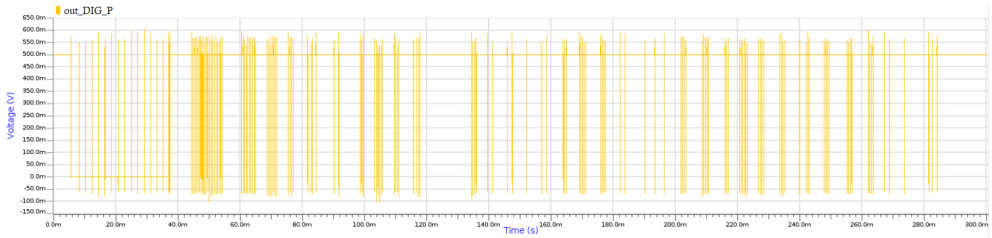


Figure 6.9: Voltage follower PLS - detail

6.5.2 Potentiostat configuration

PLS for the potentiostat are performed, results are compared with data obtained in Section 5.4. In general, what is obtained from post layout simulations appears to be compliant with what is obtained previously. System performance is not affected by parasites introduced by the physical layout. Below is shown the transient response of the potentiostat with PLS.

Transient response

The transient response of the potentiostat taking into consideration physical components has been evaluated.

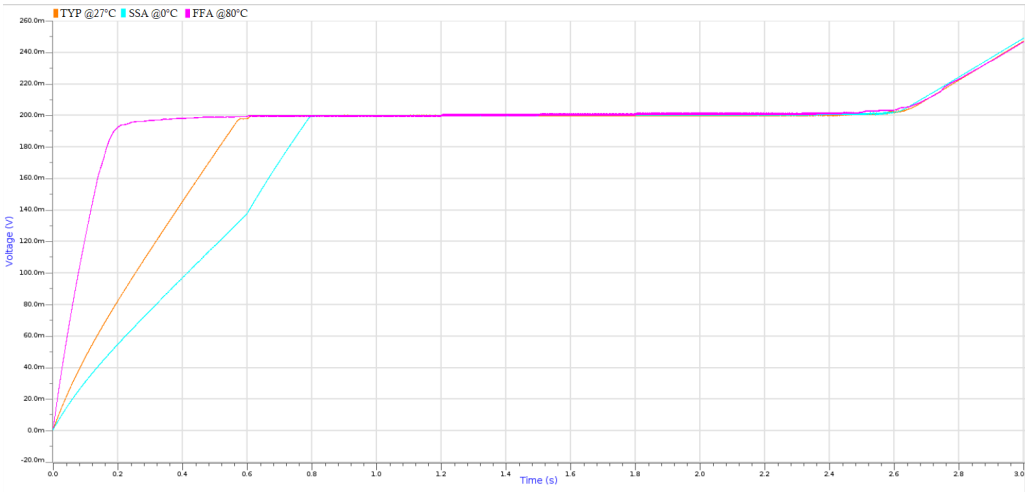


Figure 6.10: Potentiostat response with PLS (in orange the TYP process corner @27°C, in cyan the SSA process corner @0°C, in violet the FFA process corner @80°C)

T	Corner	$t_{convergence}$ [s]	$t_{saturation}$ [s]	$t_{acquisition}$ [s]
27°C	TYP	0.7	2.6	1.9
0°C	SSA	0.85	2.4	1.55
80°C	FFA	0.45	2.5	2.05

Table 6.2: Potentiostat timing with PLS

Steady-state error

In this case, the steady-state error turns out to be slightly increased with respect to the ideal simulations; in any case, the resulting error is negligible. The waveforms obtained in different cases are depicted below, and a summary of the results is presented at the end of the section.

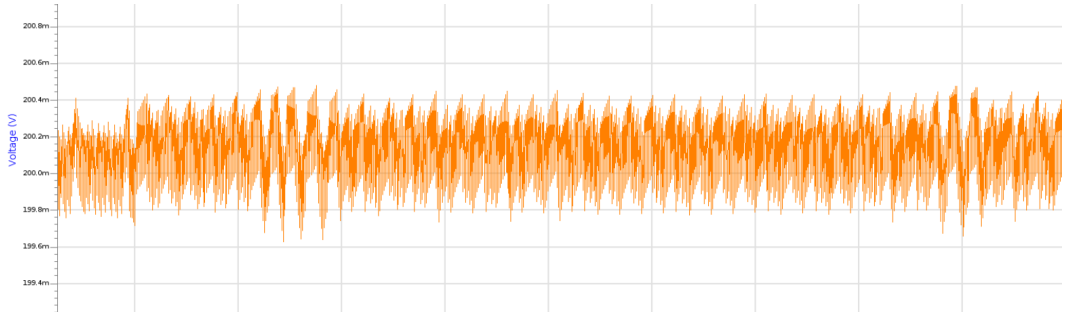


Figure 6.11: PLS - Ripple in the RE voltage under typical case

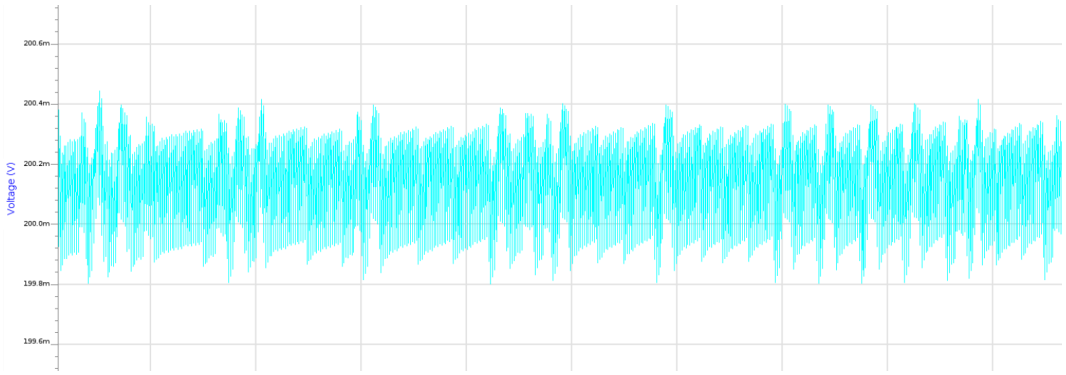


Figure 6.12: PLS - Ripple in the RE voltage under SSA case

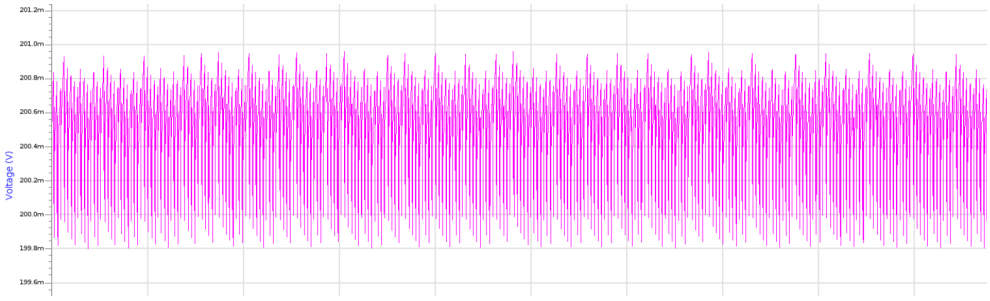


Figure 6.13: PLS - Ripple in the RE voltage under FFA case

T	Corner	V_{REavg}[mV]	$V_{REpp}[mV]$	V_{REmin}[mV]	V_{REmax}[mV]
27°C	TYP	200.16	0.85	199.63	200.48
0°C	SSA	200.17	0.65	199.8	200.45
80°C	FFA	200.6	1.2	199.79	200.98

Table 6.3: Potentiostat errors on V_{RE}

Post-processing evaluation

Given that the post-layout performances are not affected by the non-idealities introduced by the physical design, the sensitivity reported below is also consistent with what was reported previously. The simulation is performed by injecting a current that simulates a variation of glucose of 10mM; after PLS, the resulting sensitivity, in the typical case, turned out to be equal to 40.7LSB/mM.

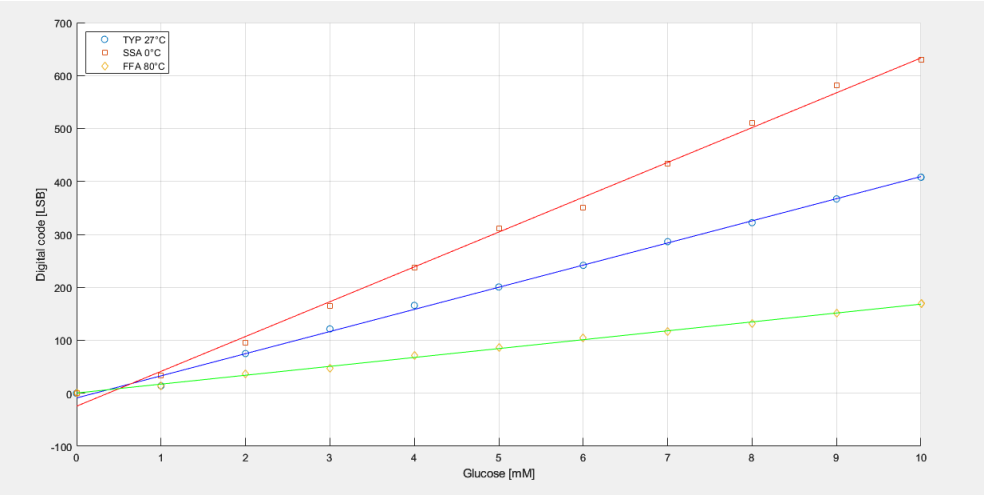


Figure 6.14: PLS - sensitivity comparison (in blue the TYP process corner @27°C, in red the SSA process corner @0°C, in green the FFA process corner @80°C)

Chapter 7

Conclusions and future works

This work presented the design of a DB-Potentiostat for the detection of glucose, implemented in a 130nm technology by STMicroelectronics for wearable biosensing applications. At the beginning of the work, redox chemistry concepts are revisited to introduce classical potentiostat-based measurements, highlighting their limitations. Innovative biosensing techniques based on nanostructuration processes are presented to define the optimum context in which the DB-potentiostat should operate. A literature review outlined the current state of the art, reviewing DIGOTA concepts and DB-potentiostat basics. The optimization of the circuit with respect to the provided technology started considering the constraints imposed by the electrochemical cell. A trimming circuit is designed to compensate for the possible errors related to the capacitance of the cell. The simulation results obtained in the Cadence environment allowed to test the effectiveness of the circuit, ensuring correct operations under different conditions. The layout of the circuit was performed in collaboration with STMicroelectronics. Post-layout simulations are exploited to verify the correct behavior of the physical implementation of the system. The designed DB-potentiostat turned out to occupy an area of 1104 μ m^2; simulations at 27°C with a 0.5 V supply, a 50 kHz clock, and typical process conditions showed a power consumption of 19.1 nW. The resulting sensitivity is 41 LSB/mM. Despite the extremely small size of the circuit, it is important to underline that an over-sizing of the DIGOTA due to MOM capacitors and the driving chain is present. The characteristics of the DB-potentiostat are compatible with the constraints of wearable applications.

7.1 Future prospective

Such a challenging and stimulating activity lays the foundation for a broader activity with the final aim of manufacturing a functional biosensor complete in all its aspects. The testing of the prototype will allow to verify on-chip the performance of the design. An empiric evaluation of the capacitance of the electrochemical cell is needed to customize the topology and remove the trimming circuit; in addition to this, to reduce the dimension, an investigation of a more suitable technology can allow to avoid the MOM capacitors used in the prototype. To create a complete working sensor, a battery-less sensor can exploit an energy harvester for its independence from the supply, and a communication protocol should be defined to communicate sensed data.

Hopefully, this work will offer new insights into the research for wearable biosensors and will contribute to growth this fascinating and ever-evolving field.

Appendix A

Appendix

A.1 Potentiostat Post Processing

```
// VerilogA for VerilogAMS, counter, veriloga

`include "constants.vams"
`include "disciplines.vams"

module integrate_PULSE(clk,ref,dd,CNTP,CNTM,out);

output out;
input clk, ref,dd,CNTP,CNTM;
electrical clk,ref,dd,CNTP,CNTM,out;

real cnt,countP, countN;
real Vdd,Vcnt,VCNTP,VCNTM,vtrans_clk;
parameter integer N = 1024

parameter real trise = 0.1e-9;
parameter real tfall = 0.1e-9;
parameter real tdel = 0.1e-9;

//parameter real Vup = 0.000168;     // Ip*T/C
//parameter real Vdw = 0.000270;     // Im*T/C
parameter real Inn = 15.5e-6;
parameter real Ipp = 2e-6;
parameter real dT = 20e-6;
real IP;
real IN;
real TotalTime;
```

```
28
29 genvar i,j;
30 real Qp[N-1:0];
31 real Qn[N-1:0];
32
33 analog begin
34     @(initial_step)
35     begin
36         IP = Ipp*dT;
37         IN = Inn*dT;
38         TotalTime = N*dT;
39         Vdd=V(dd,ref);
40         vtrans_clk=Vdd/2;
41         countP=0;
42         countN=0;
43         cnt=0;
44         for(j=0; j<N; j=j+1)
45             begin
46                 Qp[j]=0;
47                 Qn[j]=0;
48             end
49     end
50
51     @(cross(V(clk,ref)-vtrans_clk, 1))
52     begin
53         VCNTP = V(CNTP,ref);
54         VCNTM = V(CNTM,ref);
55         countP=0;
56         countN=0;
57         for(j=0; j<N-1; j=j+1)
58             begin
59                 Qp[j]=Qp[j+1];
60                 countP = countP + Qp[j];
61                 Qn[j]=Qn[j+1];
62                 countN = countN + Qn[j];
63             end
64
65
66
67         if(VCNTP < vtrans_clk)
68         begin//
69
70                     Qp[N-1] = IP;
71                     countP = countP + IP;
72                             //$display("CNTP");
73         end
74         else//
```

```
75
76          begin
77                  if(VCNTM > vtrans_clk)
78                      begin
79                      Qn[N-1] = IN;
80                      countN = countN + IN;
81                              //$display("CNT N");
82                      end
83                  else
84                      begin
85                          Qp[N-1] = 0;
86                          Qn[N-1] = 0;
87                      end
88          end //
89
90          cnt = (countP-countN)/TotalTime;
91          //$display("cnt = %e",cnt);
92      end // cross end
93
94
95 V(out,ref) <+ transition(cnt,tdel,trise,tfall);
96
97      end // analog end
98 endmodule
```

A.2 Matlab code

Sensitivity.m

```
Glucose = [0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10]; % glucose values [mM]
DigitalCODE = [0, 13, 77.5, 123, 164, 208, 243.6, 287, 326.8, 369, 410]; % digital values
DigitalCODE_SSA = [0, 35, 98, 166, 240, 311, 367.7, 438.9, 510, 580, 633.8]; % digital values SSA
DigitalCODE_FFA = [0, 13.3, 35, 46.6, 70, 86.5, 103, 114.7, 130, 150.2, 168]; % digital values FFA

% evaluate linear regression
coefficients = polyfit(Glucose, DigitalCODE, 1); % Plot  first degree polynomial
coefficients_SSA = polyfit(Glucose, DigitalCODE_SSA, 1);
coefficients_FFA = polyfit(Glucose, DigitalCODE_FFA, 1);

% extract the coefficients of the regression line
slope = coefficients(1); % Coefficiente angolare (pendenza)
slope_SSA = coefficients_SSA(1);
slope_FFA = coefficients_FFA(1);
intercept = coefficients(2); % Termine noto
intercept_SSA = coefficients_SSA(2);
intercept_FFA = coefficients_FFA(2);

% generate regression line
regression_line = slope * Glucose + intercept;
regression_line_SSA = slope_SSA * Glucose + intercept_SSA;
regression_line_FFA = slope_FFA * Glucose + intercept_FFA;


% data plot
scatter(Glucose, DigitalCODE, 'o'); % sketch the points
hold on;
scatter(Glucose, DigitalCODE_SSA, 'square');
hold on;
scatter(Glucose, DigitalCODE_FFA, 'diamond');
hold on;
plot(Glucose, regression_line, 'b'); % sketch the regression line
plot(Glucose, regression_line_SSA, 'r');
plot(Glucose, regression_line_FFA, 'g');

% labels
xlabel('Glucose [mM]');
ylabel('Digital code [LSB]');
```

```
39
40 % depict slope and intercept
41 fprintf('slope: %.2f\n', slope);
42 fprintf('intercept: %.2f\n', intercept);
43 fprintf('slope: %.2f\n', slope_SSA);
44 fprintf('intercept: %.2f\n', intercept_SSA);
45 fprintf('slope: %.2f\n', slope_FFA);
46 fprintf('intercept: %.2f\n', intercept_FFA);
47
48 grid on;
49 hold off;
```

Staircase acquisition.m

```
1 t = [0, 0.2, 0.4, 0.6, 0.8, 1, 1.2]; % time
2 DigitalCode = [0, 82, 164, 246, 328, 410, 410]; % Digital Code
3
4 % Plot the staircase graph
5 stairs(t, DigitalCode, 'b-', 'LineWidth', 2);
6
7 % labels
8 xlabel('time [s]');
9 ylabel('Digital Code [LSB]');
10
11 grid on;
```

Bibliography

[1] Taurino I. Sanzó G. Mazzei F. et al. «Fast synthesis of platinum nanopetals and nanospheres for highly-sensitive non-enzymatic detection of glucose and selective sensing of ions». In: (Oct. 2015).

[2] Luca Magnelli Francesco Amoroso Felice Crupi Gregorio Cappuccino and Giuseppe Iannaccone. «Design of a 75-nW, 0.5-V subthreshold complementary metal–oxide–semiconductor operational amplifie». In: *International journal of circuit theory and applications* 23 (2012).

[3] Sandro Carrara. *Bio/CMOS Interfaces and Co-Design*. Springer Cham, 2012.

[4] P. S. Crovetti. «A Digital-Based Analog Differential Circuit». In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 60 (2013).

[5] Dhara K. Mahapatra D.R. «Electrochemical nonenzymatic sensing of glucose using advanced nanomaterials». In: *Microchim. Acta* 185 (2018).

[6] Dhara K. Mahapatra D.R. «RC models of a constant phase element». In: *Int. J. Circuit Theory Appl.* 41 (2013).

[7] Carrara S. Pantelis G. «Body Dust: Miniaturized Highly-integrated Low Power Sensing for Remotely Powered Drinkable CMOS Bioelectronics». In: *arXiv physiscs* 10 (2018).

[8] Adam Wang Doohwan Jung Dongwong Lee and Hua Wang. «Impedance Characterization and Modeling of Subcellular to Microsized Electrodes with Varying Materials and PEDOT:PSS Coating for Bioelectrical Interfaces». In: (Mar. 2021).

[9] Toledo P. Crovetti P. Aiello O. Alioto M. «Design of Digital OTAs With Operation Down to 0.3V and nW Power for Direct Harvesting». In: *IEEE Transactions on circuits and systems* 68 (2021).

[10] Victoria V. Shumyantseva Sandro Carrara Valter Bavastrello D. Jason Riley Tatiana V. Bulko Konstantin G. Skryabin Alexander I. Archakov Claudio Nicolini. «Direct electron transfer between cytochrome P450scc and gold nanoparticles on screen-printed rhodium–graphite electrodes». In: *Biosensors and Bioelectronics* 21 (2005).

[11] S. Carrara R. Rubino and P. Crovetti. «Direct Digital Sensing Potentiostat targeting Body-Dust». In: *IEEE Biomedical Circuits and Systems Conference (BioCAS).* (2022).

[12] Toledo P. Crovetti P. Klimach H. Musolino F. Bampi S. «Low-Voltage, Low-Area,nW-Power CMOS Digital-Based Biosignal Amplifier». In: *IEEE Access* 10 (2022).