POLITECNICO DI TORINO

Master degree
in Nanotechnologies for ICTs

Master's Degree Thesis

3D Silicon-based Tunnel FET technology: fabrication process and electrical TCAD simulations

Supervisors
prof. Gianluca Piccinini
Dr. Chiara Elfi Spano
Dr. Fabrizio Mo
Supervisors' signature

. . . . . .
. . . . . .

Candidates
Roberto Poma
Enrico Monfrino

Candidates' signature

. . . . . .
. . . . . .

Academic year 2022-2023

Abstract

MOSFET devices represented the basis of the electronics, but in the last years the scaling of the dimensions required by the technology caused the appearance of some problems, such as short channel effects and power dissipation. To overcome these drawbacks different solutions are possible and one of them is to change the nature of the device to TFET. Thanks to different conduction mechanism (tunneling) several advantages can be achieved; the most relevant are lower off-current, and so lower power dissipation, and smaller subthreshold swing.
In this thesis the design and the analysis of TFET devices are discussed through the use of the software Synopsys TCAD Sentaurus, by simulating realistic fabrication processes. The purpose is to investigate structures based on homojunctions and materials commonly used in the production of traditional MOSFET. For this aim a modification of the doping, to take advantage from the tunneling, is performed and a comparison with MOSFET examples present in literature is made, mantaining for all approximately the same channel dimension (50 nm).
For simplicity the study starts from the analysis of a planar structure, useful to understand and define the correct models to describe, as close as possible to reality, the electronic transport.
The work continues to 3D devices, namely Fin and NSGAA TFETs; the key point is the optimization of the structures with the intention to improve, as much as possible, the behavior of the devices without changing its nature; for this reason several analysis on the effects on the figures of merit (I_{ON}, I_{OFF}, SS e V_{TH}) of the parameters, such as channel length, oxide thickness and so on, are carried out.
The results show very promising values for what concern the off current ($\simeq 10^{-14}$A/μm), even if a low on current ($\simeq 10^{-9}$A/μm for a single device) and high SS values ($>$ 100 mV/dec rather than $<$ 66 mV/dec) are obtained, in agreement with the related literature results.
Finally a comparison between these optimized structures, other TFETs present in literature and the counterparts MOSFETs are performed in order to understand the validity of this study.

"se nel mondo esistesse un po di bene, e ognun si considerasse suo fratello, ci sarebbero meno pensieri e meno pene, e il mondo ne sarebbe assai più bello"
[Pacciani]

Contents

List of Tables

List of Figures

Acronyms and physical constants

V_{TH} : Threshold Voltage
SS : Subthreshold Swing
Eg : Semiconductor energy gap
Ec : Conduction band
Ev : Valence band
V_G or **V_{GS}** : Gate voltage
V_{DS} : Voltage applied between source and drain
I_{DS} : Device current
$I_{DS,0}$: Reference planar current
J_{DS} : Device linear current density
H_{Fin} : Fin height
W_{Fin} : Fin width
q : Electron charge = 1.60217663 x 10^{-19} C
$\hbar$: Reduced Planck's constant = 1.054571817 x 10^{-34} J*s
FET : Field Effect Transistor
JLT : JunctionLess transistor
NCT : Negative Capacitance transistor
TCAD : Technology Computer-Aided Design
SRH : Shockley-Read-All (or trap-assisted) recombination process
NS : NanoSheet
GAAFET : Gate-All-Around FET

Chapter 1

Introduction

1.1 From MOSFET to TFET

MOSFET (acronym of metal-oxide-semiconductor field-effect transistor) is a type of device widely used in both digital and analog electronics.
For what concern the structure, "it consists of a capacitor, constituted by an electrostructure formed by three layers of different materials (substrate, oxide and metal), flanked by two terminals, called source and drain" [18]. The substrate, also known as body, consists of a doped semiconductor. Above it there is a thin insulating layer called gate oxide, composed of silicon dioxide or dielectrics with high electrical permittivity, such as hafnium dioxide. Such a layer is necessary in order to isolate the gate contact, which must only provide the electrostatic control, and avoid loss of power, caused mainly by the leakage of charges from the gate. In fact the gate current has to be the lowest possible to realize an ideal behavior of the MOS. Finally there is the gate, made with conductive material: at the beginning of this technology polycrystalline silicon (polysilicon) was the best choice (from the moment that metal deposition technique was not good enough to provide the desired results) thanks to its tunable electron affinity through doping, then, with the scaling of the technology, the use of metals for the gate was necessary [15]. The terminals of source and drain, finally, are also composed of semiconductor, doped in the opposite way: if the substrate has a doping type p the two terminals have doping type n, and vice versa. Depending on whether the body semiconductor doping is n or p type, the transistor is named pMOSFET and nMOSFET, respectively (structures represented in figure 1.1).

The MOSFET is a barrier device, so its operating mechanism depends on the voltage applied to the gate. Depending on it the region of substrate that connects drain and source can be rich in holes, depleted, or rich in electrons [15]. Considering a nMOSFET, the first situation is called accumulation and it happens when the applied gate voltage is negative and it is less than the Flatband one;in this case the holes are collected at the interface between the oxide and the semiconductor, due to the fact that the last is p-type. The second situation instead is reached when the gate voltage is positive, higher than the flatband but less with respect to the threshold one. Continuing to increase the voltage

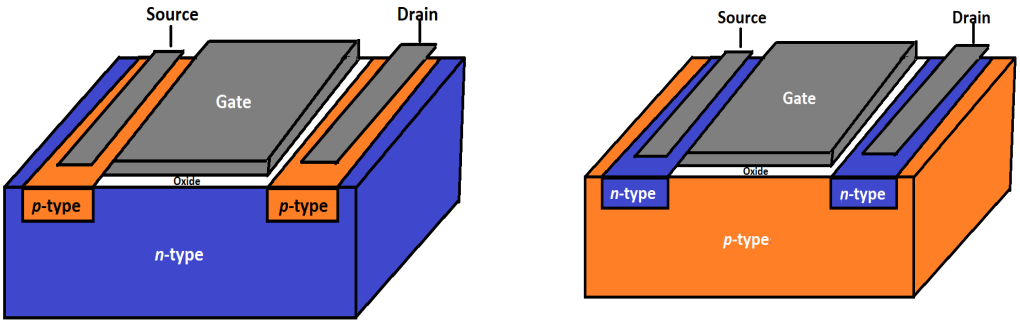


Figure 1.1: MOSFET possible structures

the third situation is obtained: the channel has a huge number of electrons and it is in the ON state. This happens because the holes are pushed down toward the bottom of the substrate while the negative charges are attracted to the interface oxide-semiconductor. All the situations for both the structures are explained in the figure 1.2

Electronics greatly benefits from the possibility of reducing the size of the circuits: this has led to the miniaturization of MOSFET, whose dimensions has reduced from several micrometers to the order of nanometers. Examples of advantages are the higher current in the on state, the greater speed (due to smaller gate capacitance) and a smaller area occupied, so higher integration density. Clearly there are also drawbacks when the gate length becomes of the order of few nm: carrier velocity saturation, heat production, gate current (due to tunneling) and subthreshold current. In the last years the dimensions of the devices became so small that the disadvantages overcame the benefits of the scaling itself; a first idea to turn around this problem was to move from planar to 3D-structures such as FinFET and GAAFET [20].
The first is a multigate device where the shape of the channel forms a fin; these devices have significantly faster switching times and higher current density than planar technology. The second is similar to a FinFET transistor but the gate material surrounds the channel from all sides.
All these structures, described up to now, rely on the conduction mechanism of thermoionic emission; this one has limitations that cannot be avoided when we go to scale our devices, such as the theoretical value of the SS (66 mV/dec) and the high I_{OFF}. To overcome these limits several implementations are possible, such as junctionless transistors (JLT), negative capacitance transistors (NCT) and tunneling transistors (TFET) [20]. Among these the one we will consider is the tunneling transistor, based on a different conduction mechanism. The basic idea is to make electrons pass from source to drain not by overcoming a barrier (like in a MOSFET) but by tunneling through it. This not only should provide a better SS,thanks to a faster turning on of the conduction mechanism, but also a lower I_{OFF} .

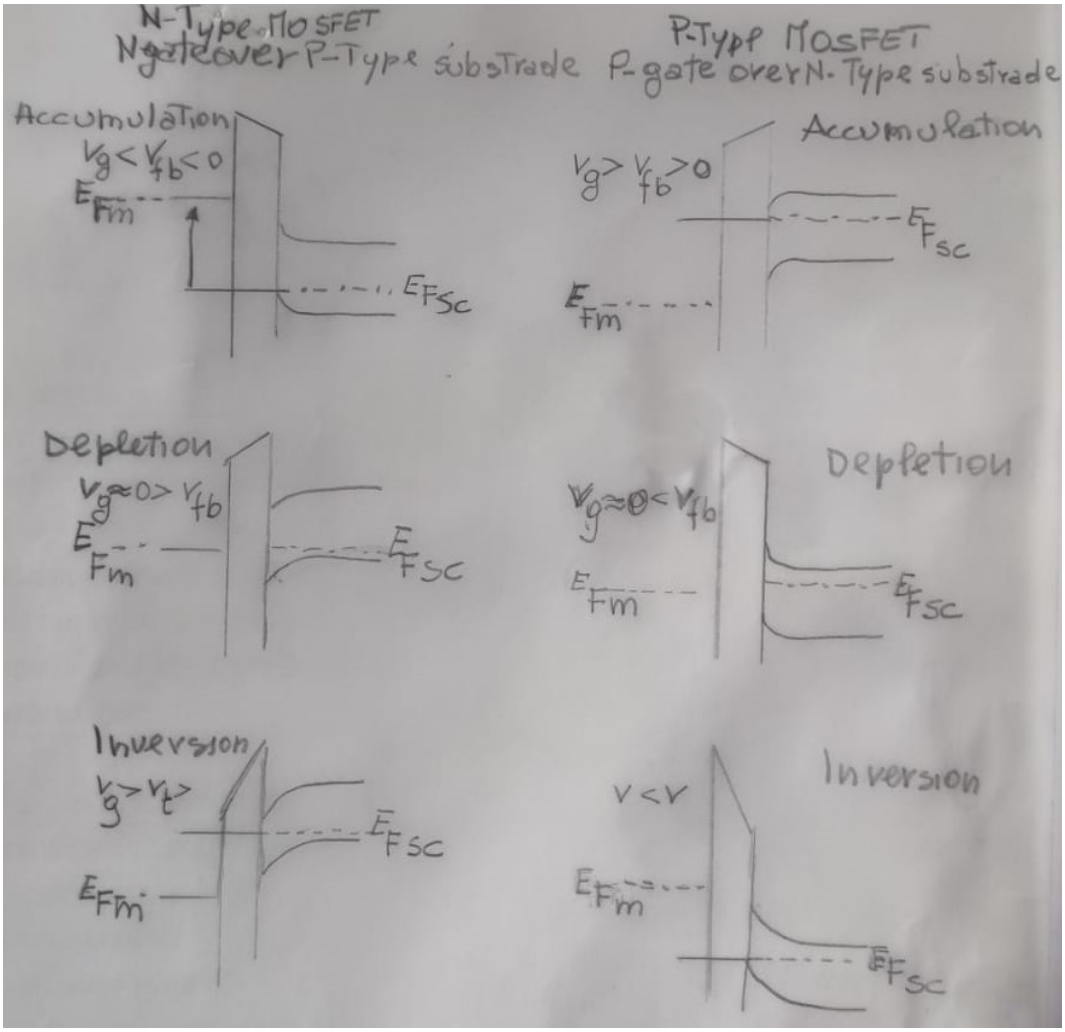


Figure 1.2: Operating conditions of p and n MOSFETs

1.2 TFET basics

The basic TFET structure is similar to a MOSFET except that the source and drain terminals of a TFET are doped of opposite types (figure 1.3). A common TFET device structure consists of a P-I-N (p-type, intrinsic, n-type) junction, in which the electrostatic potential of the intrinsic region is controlled by a gate terminal. From now on all the reasonings are made considering n-type devices but similar results are true also for p-types [20][21].

Depending on the applied voltage, different operating conditions are possible. At the equilibrium state no external bias are applied ($V_{gs} = V_{ds} = 0$). In this case there are

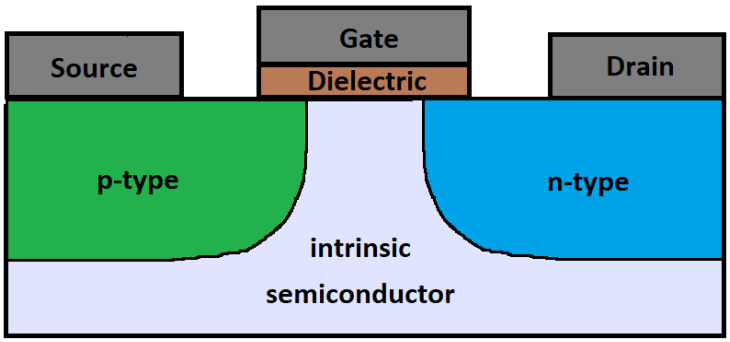


Figure 1.3: TFET basic structure

two depletion region formed, one at Source-Channel junction and one at Channel-Drain region. Very few electrons are injected into Drain side and hence lead to negligible current in OFF state because the conduction band of the intrinsic material is above the valence band of the p-type side (figure 1.4a).
Applying a positive value of V_{ds}, always in off condition, some electrons start to flow from the intrinsic channel to the drain, due to the shift of the bands of it, but however the current is small since no gate voltage is applied (figure 1.4b).
The on condition is reached applying a value of V_{gs} able to shift the conduction band (CB) of the intrinsic material below the VB of the source side. When this situation happens, since the p side is full of electrons, a huge number of them start to flow and then go to the drain (see figure 1.4c). Since this mechanism is fast, the growth of the current is high and as a consequence the SS is small, less than the one of a MOSFET.
From a mathematical point of view the on current depends on the Transmission probability((1.1)), which formula can be derived from the Schrodinger equation through the WKB approximation, so considering the source-channel junction as a quasi-triangular barrier with thickness λ, called natural length [22].

$$T_{WKB} = \frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar(E_g + \Delta\Phi)}. \tag{1.1}$$

The involved parameters have the following meanings:

1. $\lambda = \sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}} t_{Si} t_{ox}}$ natural length;

   (a) ϵ_{Si} is the Silicon dielectric permittivity;

   (b) ϵ_{ox} is the Oxide dielectric;

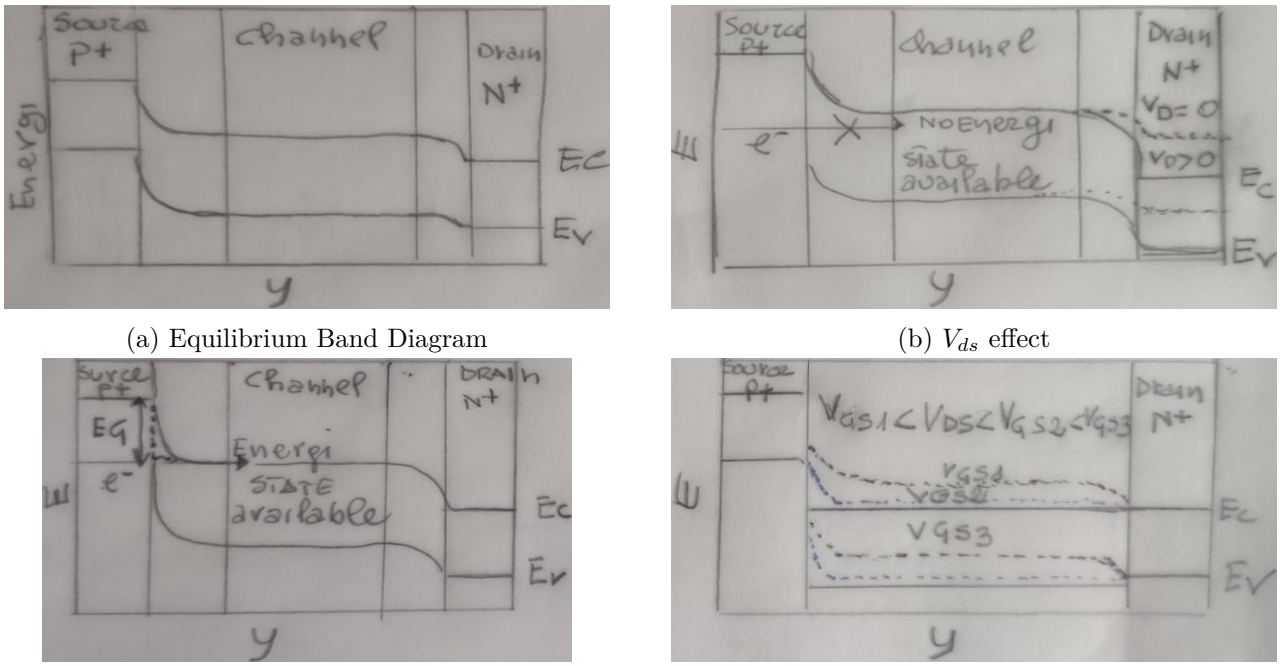
   (c) t_{Si} is the Silicon layer thickness

   (d) t_{ox} is the Oxide layer thickness

2. m^* effective mass of the carriers;

3. E_g is the Silicon Band gap energy;

4. $\Delta\Phi$ is the tunneling region;



(a) Equilibrium Band Diagram

(b) V_{ds} effect

(c) On state

(d) V_{gs} effect

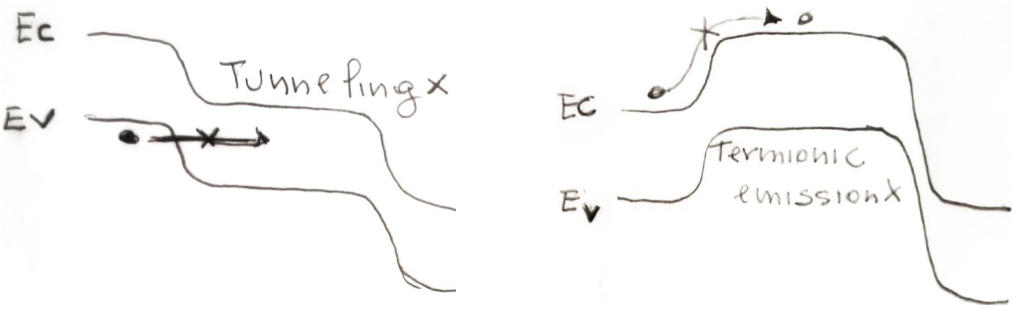
Figure 1.4: Working regions of a TFET

1.3 TFET advantages

From a theoretical point of view TFET, thanks to its peculiar conduction mechanism, offers several improvements with respect to MOSFET; in particular, as previous said, a lower I_{off} current and a better subthreshold slope SS. This features allow to overcome some problems and make TFET a serious possibility for existing but especially future technological applications and scaling [20].

1.3.1 Better I_{off}

For what concern the off- current, the strength of the TFET devices is that, exploiting a tunneling conduction mechanism, whenever the on state conditions are missing, the transmission probability drops down exponentially with the λ thickness (refers to equation 1.1). This happens because, as shown in figure 1.5a, if the conduction band of the channel region is above or almost aligned to the valence band of the source one, the tunneling path is equal to the entire intrinsic material; this makes the probability, for an electron, to pass from source to drain ideally null and so the final off current almost zero. Obviously there are other phenomena that should be considered that contributes to the leakage current, and so this is never zero, but with respect to an equivalent MOSFET device it will be always lower. In fact, looking at 1.5b, also in this case the barrier prevents the flowing of electrons from source to drain, but however the probability will be higher compared to the previous case.



(a) TFET (b) MOSFET

Figure 1.5: Off conduction mechanisms

From a physical point of view this is due to the fact that in thermoionic conduction, there will always be a certain number of electrons with an energy higher than the barrier, explained by the Fermi-Dirac distribution (figure 1.6)

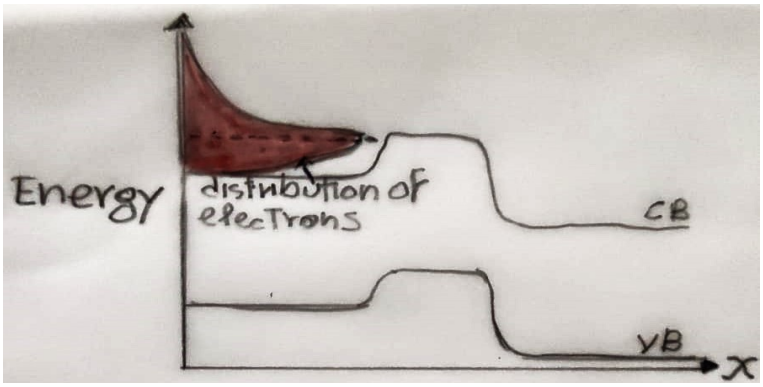


Figure 1.6: Tail off-state conduction in MOSFET

1.3.2 SS: below the thermal limit

The subthreshold swing SS is one of the figures of merit of FETs and it can be computed as the inverse of the subthreshold slope. This quantity can be computed through the equation [10]:

$$SS = [\frac{dlog_{10}I_D}{dV_{GS}}]^{-1} \tag{1.2}$$

It is related to the speed of the device and so how fast it switch on/off with the applied gate voltage; for this reason SS should be as small as possible
In standard MOSFET this quantity could be simplified with the value

$$SS = 2.3mV_T \tag{1.3}$$

where

1. m $= 1 + \frac{3t_{ox}}{x_{d0}}$ is the slope factor;
2. x_{d0} is the maximum extension of the depleted region;
3. $V_T = \frac{q}{k_b T}$ is the equivalent in voltage of the temperature;

From this can be observed that there is a lowest limit that, considering a room temperature of 300K, is approximately 60 mV/dec (refers to figure 1.7). In fact m cannot be lower than one (due to its definition) and V_T is a physical constant.
In TFET this limit doesn't exist because of different conduction mechanism. Recalling the eq (1.2), it can be expressed in two factors

$$SS = [\frac{dlog_{10}I_D}{dV_S}]^{-1}\frac{dV_{GS}}{dV_S} \tag{1.4}$$

Thanks to tunneling the first term, related to value $2.3V_T$ of the eq (1.3), can be lower than it. From a physical point of view it is equal to say that the device has been cooled down and, as a result, the overall value of the SS could be lower than 60 mV/dec.

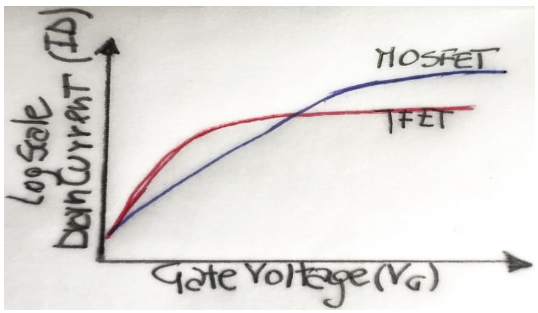


Figure 1.7: SS: MOSFET vs TFET

1.3.3 A new V_{TH} definition

Searching in literature [24], what can be discovered is that TFETs generally show a lower threshold voltage with respect to MOSFETs. From a physical point of view this can be explained because of the different conduction mechanism; in fact a new definition of V_{TH} exists: it is defined as the gate voltage at which the top of the source valence band is aligned to the bottom of the channel conduction band. From this concept, it is possible to guess that not only the device tends to turn on very fast, but also that the threshold voltage can be tuned in a certain way, depending by the structure parameters. This could result in a great advantage from the moment that a lower V_{TH} of the transistors means a lower power consumption for the circuits. From a mathematical point of view V_{TH} can be evaluated as the second derivative of the transcharacteristic with respect to the gate voltage V_G ((1.5).

$$V_{TH} = max(\frac{\partial^2 I_D}{\partial^2 V_{GS}}) \tag{1.5}$$

1.4 TFET issues

After talking about the advantages of TFET, it is necessary to also emphasize the disadvantages. Among the figures of merit, the one that is worse than the MOSFET is certainly the I_{on}. In addition, there are problems due to the structure of this type of devices, such as ambipolarity, which is not completely disposable, and other more controllable, explained below as second-order problems. [20]

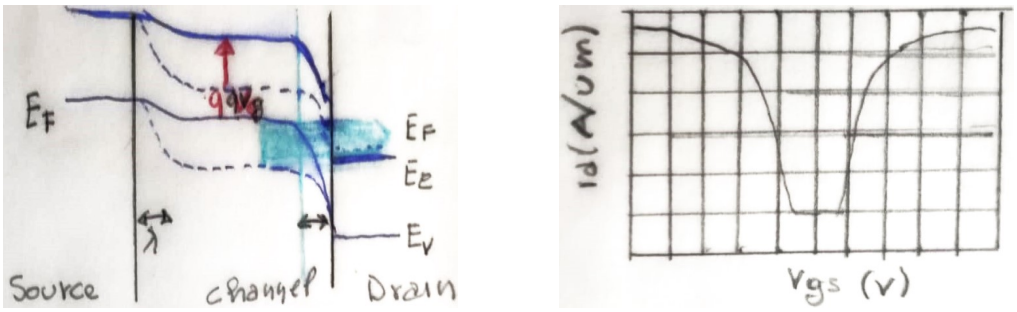
1.4.1 Poor I_{on}

The low I_{on} is probably the main reason why TFET are not yet widely used in modern circuits. In fact the on-current, being these quantum mechanics devices, is governed by band-band tunneling (BTBT) of electrons and it is related to the barrier width between the channel and the highly doped source region. As a consequence typical values are approximately 10^{-6} A/μm, much less than the ones of a generical MOSFET, that are 10^{-3} A/μm. [21]
From a mathematical point of view, it is useful to consider the equation (1.1). Since the current depends by this transmission probability, it has to be maximized. Some solutions are possible, such as reduce λ, so have a steep source junction, reduce E_g or the effective mass $m*$.

1.4.2 Ambipolarity

The ambipolarity is a peculiar feature present only in TFETs, due to the nature of the device. This phenomenon consists in a current that is generated from drain to source when the applied V_{DS} is too low or negative. What happens is that, turning off the device ($V_{GS} = 0$), the conduction band of the drain goes below the valence band of the channel (figure 1.8a) and so a hole current starts to flow; so, despite the device should be off, the drain current starts to increase again.

Generally this is a detrimental effect because because if this happens too early ($V_{Ga} > V_{TH}$, where V_{Ga} is the gate voltage at which ambipolarity occurs) the device doesn't really turn off or anyway the I_{OFF} get worse, as shown in figure 1.8b.



(a) Working principle (b) Transcharacteristic

Figure 1.8: Ambipolarity effect in TFETs

This effect can't be avoided because is an intrinsic property of TFETs, but the device can be properly designed in order to shift the ambipolarity to lower or negative voltages. In this way the operating range of the circuit is not afflicted by this problem.

1.4.3 Second order problems

Finally there are less relevant problems, related to the design of the structure. The first two are linked to the source region and they depend by the its doping while the last one is associated to the channel region and in particular to the gate voltage applied.

- Source degeneracy
  In some cases an higher source doping can be useful but it can't be freely increased; in fact what happens is that, if the source doping is too high, it can become degenerate and this means that the Fermi level is pushed below the valence band. As consequence the available states for tunneling decrease and the tunneling path is on the average higher: so in the end the number of electrons that can tunnel through the barrier decrease.

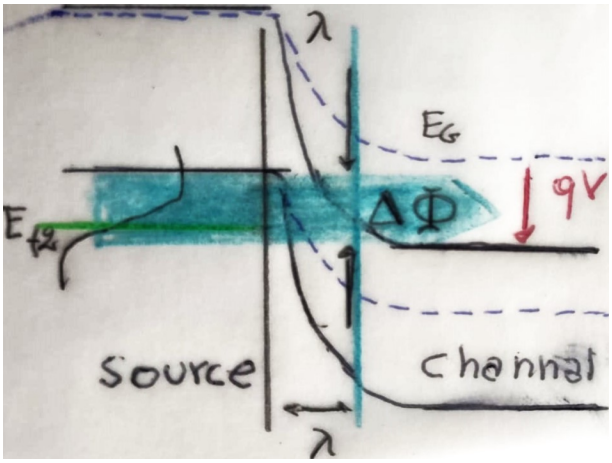


Figure 1.9: Source degeneracy

- Source depletion
  On the other hand, if the source doping is too low, part of the depleted region tends to fall inside the source and as result the effective tunneling barrier results thicker.

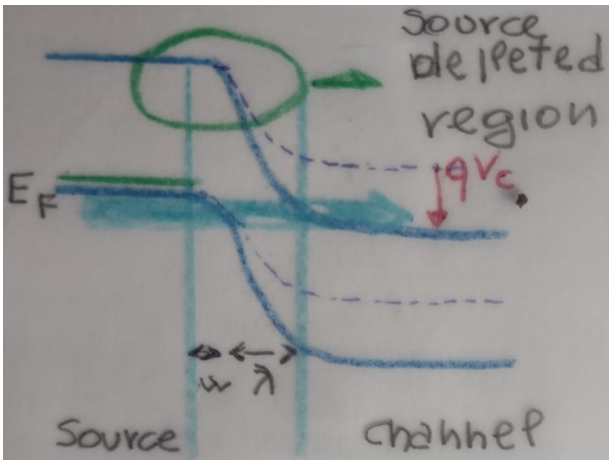


Figure 1.10: Source depletion

- De-biasing
  TFETs generally work with depleted channel and inversion layer is unwanted. The de-biasing effect occurs when the applied V_{GS} is too high and the device goes in inversion; when this happens there is a "pinning" of the channel and is impossible to further control it through V_{GS}.

1.5 Conclusive statements

In the end, considering the reasonings seen up to now, all the expected features are reasumed in the table 1.1

Figures of merit	MOSFET	TFET
I_{ON}	10^{-3} A/μm	10^{-6} A/μm
I_{OFF}	10^{-8} A/μm	10^{-14} A/μm
VTH	$\simeq 0.4V$	$\simeq 0.2V$
SS	>60mV/dec	<60mV/dec

Table 1.1: Figures of merit comparison: MOSFET vs TFET

1.6 Possible implementations

After explaining the conduction principle and the consequent advantages and disadvantages of TFET, exist possible implementations to make this type of device a conceivable replacement of the MOSFET. In fact there are many techniques to improve what are already the strengths, such as the low I_{OFF} and the SS, but also to reduce intrinsic defects, such as poor I_{ON} or ambipolarity.

- **SOI employment**
  Silicon-on-insulator (SOI) is a fabrication technique that consists in creating an oxide layer (BOX) that isolates the body from the silicon overlay; in this way the first becomes only a mechanical support while the second can be fully used for the device creation.
  This technology, despite the high manufacturing costs that represent the main reason why it is not largely used, offers several huge advantages. The main consequence of using SOI wafers is that the device works with a fully depleted channel, eliminating some of parasitic effects that are present in bulk devices. In particular it eliminates latch-up currents because avoids possible junctions between parts of the device with different dopings, it reduces, thanks to the fully depleted channel, the leakage currents and moreover it lowers the parasitic capacitances among the device.
  As results, exploiting this technology, it is possible to obtain a lower I_{OFF} and a further reduction of the SS. [23]

- **High-k dielectric**
  They are a family of insulators that shown a very high dielectric constant with respect to the silicon dioxide one; the main used is Hafnium dioxide (HfO_2) thanks to its compatibility with current fabrication processes.
  The reason why we rely on them is linked to the further scaling having in the last years: in fact as the thickness of the old gate oxide SiO_2 scales below 2 nm, some problems appear. At first is technologically challenging and expensive to obtain a layer of silicon dioxide smaller than 2nm with a good quality, but with the Hafnium

dioxide is possible to use a thicker gate oxide layer (considering $\epsilon_{HfO_2} \simeq 6\epsilon_{ox}$ you can use $t_{HfO2} \simeq 6t_{ox}$), satisfying the C_{ox}relation (1.6)

$$\frac{\epsilon_{ox}}{t_{ox}} = \frac{\epsilon_{HfO_2}}{t_{HfO2}}, \tag{1.6}$$

In this way not only the fabrication process is simplified, but other problems related to a thin gate oxide are avoided, such as the breakdown of the oxide and the increasing of the gate tunneling leakage current. [20][21]

- **Asymmetric doping**

  Doping in an asymmetric way source and drain it is possible to modify the barriers at the interfaces of the device improving it [8]. In fact, looking at figure 1.11, we can see that, increasing the doping of the source, the depleted region falls almost entirely inside the channel and so the width of the barrier decreases; with this is possible to have a higher on-current , because of the higher tunneling probability, but also a lower off-current, reducing the ambipolarity effect. Moreover these properties are strictly related to the threshold voltage and the SS and so we can enhance also them.

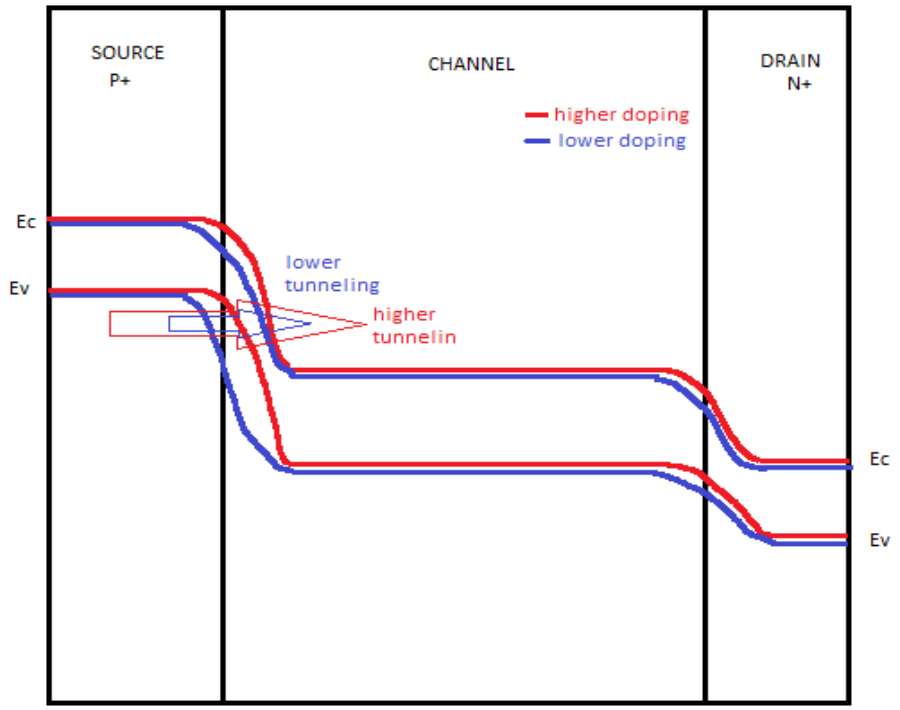


Figure 1.11: Depleted region doping dependency

- **Multi-gate**

  The presence of more than one gate is a beneficial technology that offers almost the same improvements as happen in MOSFETs. In fact, having a multi-gate structure, provides a better electrostatic control on the channel region ensuring full depletion and more polarized electric field along the vertical direction. As a consequence it impacts on the current of the device, improving both on and off states [20][21].

- **Channel doping**

  From a practical point of view lightly doping (p^-) the channel region can give beneficial effects ensuring to have a complete turning off of the device when no gate voltage is applied. This happens because we go to increase the barrier between source and channel, avoiding unwanted tunneling without affecting the behavior.

- **Metal workfunction** The choice of the metal as gate has an important impact for what concerns the ambipolarity; employing the best one allows to eliminate this effect for gate voltage greater than zero maintaining the lowest possible I_{off}. Generally it happens because we have a shift of the ambipolarity toward negative V_{GS} for low workfunction metals; in the moment that it is not more present, it is not convenient to further reduce the workfunction because there is an increasing of the off current [25].

1.7 Overview on thesis

Full-Si TFETs are well known in literature [16] and in particular their critical issues regarding the difficulties in the scaling of the technology and the deterioration of their main advantages like the off current and the Subthreshold Swing. However we decided to study this standard design in order to understand why this happens, what are the causes and what is possible to do to overcome these limitations maintaining a known technology, fully compatible with actual commercially employed manufacturing processes.
In Part I of our thesis we focus our attention on a 2D planar TFET; this choice has been made to investigate and understand the proper physical models to be considered in order to perform the electrical simulations of TFET devices, exploiting shorter simulation times with respect to 3D structures. With this purpose an analysis over the effects of the different physical mechanisms has been performed and the contributes are compared in order to evaluate their efficacy in describing tunneling and conduction inside the device. The structure consists in a simple bulk TFET device with a width, set by Sentaurus, of 1 μm and a channel length of 50 nm; finally a further study has been made regarding the band diagram and the current at the equlibrium and different voltages to make sure that the device works as expected.
In Part II we have developed the first 3D device that is a fin-shaped TFET; the first chapter describes all the fabrication processes in order to obtain this structure, making reference to the command file in the appendix B, used in the sprocess tool of Sentaurus; in the second chapter, starting from the optimized structure, electrical simulations are performed by computing the transcharacteristic and output characteristic by varying the

voltages in order to appreciate the V_G and V_{DS} dependence. In our study we have chosen as supply voltages $V_G = 1V$ and $V_{DS} = 1V$; although for the future the expected voltages for the nodes are of the order of 0.6-0.7 V we set them to 1V because our devices are not so scaled and it should be fine considering that standard devices with the same dimensions as ours use higher voltages.
Finally, in the last chapter, is investigated the transcharacteristic dependence by the physical parameters, in particular the channel length, the thickness of the oxide, different metals employed as gate and the channel doping.
In the third and last part a second and more complex 3D structure, the NSGAA TFET, is studied by keeping the same physical parameters (oxide thickness, channel length, etc). The analysis performed are similar to the ones done for the FinTFET and so again there is a detailed fabrication process description, an electrical and a parameters dependence analysis.

Part I

PLANAR

Chapter 2

Structure

The structure of the planar that we consider in the following is very simple: it is created through the sentaurus tool sprocess and consists in a all Silicon bulk device with a fixed channel length of 50nm, while the dimensions of source and drain are equal to 25 nm each. For what concern the doping, we exploit some implementations such as the asymmetric doping between source and drain (about 10^{20} and 10^{18} respectively) and the p^- doped channel (10^{15}). Since this TFET is made by Silicon, as acceptor has been chosen Boron while as donor Arsenic. Finally the structure is completed by the gate oxide and the gate metal: the first is made by 2nm of Hafnium (even if a very thin layer of silicon dioxide is present in order to represent what is made at current manufacturing processes) while the second by Aluminum, whose workfunction of 4.1 eV is optimised to obtain the best figures of merit considering the p^- doped channel. Finally the contacts are made by Copper. As previous said, although is a 2D device, a width of 1 μm is set by Sentaurus.
The overall structure is represented in figure 2.1.

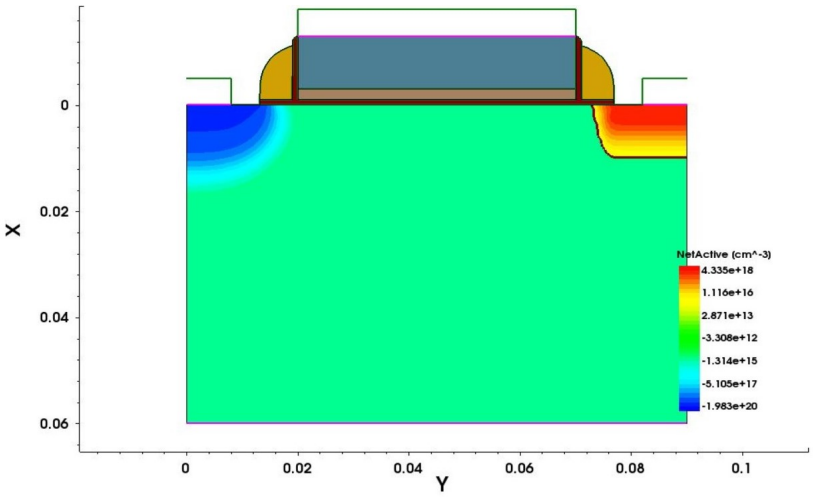


Figure 2.1: Planar TFET structure

Since TFET is a barrier device it is very important to shown the potential, due by the doping considered(figure 2.2). In fact the shape is obtained through the Poisson equation

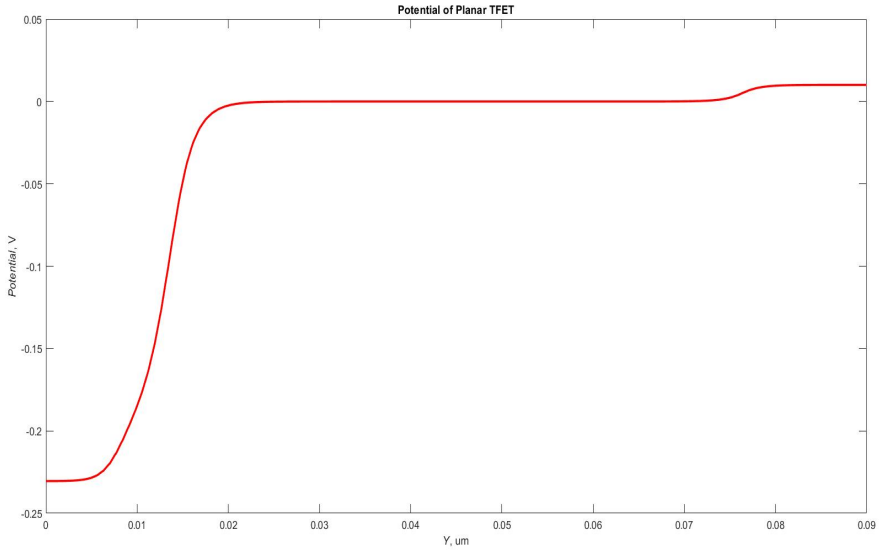


Figure 2.2: Potential of Planar TFET

[20], that linked the electrostatic potential Φ with the charge density ρ and the dielectric constant ϵ (2.1)

$$\frac{\partial^2\Phi}{\partial x^2} + \frac{\partial^2\Phi}{\partial y^2} + \frac{\partial^2\Phi}{\partial z^2} = -\frac{\rho}{\epsilon}. \tag{2.1}$$

From figure 2.2 it is possible to see that the potential is negative in source and channel regions since both of them are doped by Boron while the potential becomes positive in the drain region because of the presence of the Arsenic.

Chapter 3

Models Analysis

In order to describe in a complete and correct way the tunneling in our bulk TFET, several models are analyzed [13]. The first ones, implemented in the sdevice tool of Sentaurus, are *Fermi*, *Mobility(Tunneling)* and *Recombination(Band2Band(Hurkx))*. They are set in the following way:

Physics
{
Fermi
Mobility(Tunneling)
Recombination(Band2Band(Hurkx))
}

Firstly the Fermi statistic is included. More correct than the Boltzmann one, it becomes important for high values of carrier densities ($> 10^{19}$ cm^{-3})) in the active regions of the device, as happens in our case. From a mathematical point of view, the electron (3.1) and hole (3.2) densities are computed with the following formulas

$$n = N_C F_{1/2}(\frac{E_{F,n} - E_C}{kT}) \tag{3.1}$$

$$p = N_V F_{1/2}(\frac{E_V - E_{F,p}}{kT}) \tag{3.2}$$

where $F_{1/2}$ is the Fermi integral of order 1/2.
The second model concerns the mobility of the carriers; in particular it goes to consider possible tunneling events occuring through the channel or between the gate and the channel itself (leakage).
Finally a generation-recombination(GR) process, that concerns the exchange of carriers between conduction and valence bands, is implemented. In particular it is the Hurkx one that, similar to the other band-to-band tunneling models, models the tunneling carriers by an additional GR process, whose contribution is expressed as

$$R_{net}^{bb} = AD(\frac{F}{1V/cm})^P exp(\frac{BE_g(T)^{3/2}}{E_g(300K)^{3/2}F}) \tag{3.3}$$

where A,B and P are coefficients, D is a parameter that depends by the carrier concentrations and by a parameter α and F is the electric field.
Considering these first models, the resulting transcharacteristic at V_{ds} is represented in figure 3.1

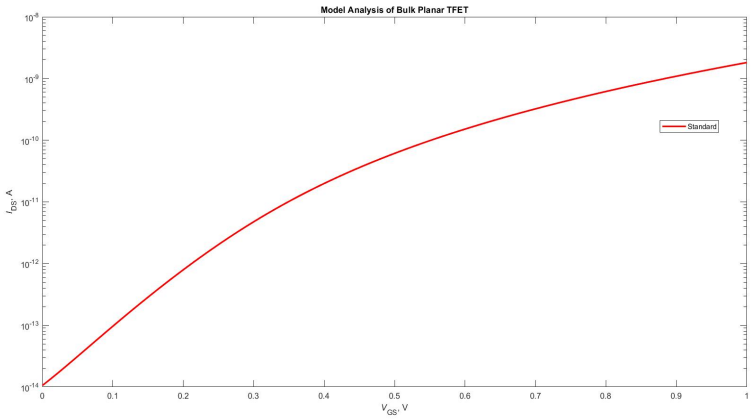


Figure 3.1: $I_{DS}(V_{GS})$ with standard models

These three models represent our basis to describe the tunneling. In the following we add one model at a time to see its effect on the transcharacteristic.

- **Hydrodynamic**
  It is a model to describe the carriers transport in a semiconductor. It can be defined through continuity equations

$$\nabla J_n = qR_{net,n} + q\frac{\partial n}{\partial t} \tag{3.4}$$

$$-\nabla J_p = qR_{net,p} + q\frac{\partial p}{\partial t} \tag{3.5}$$

  Clearly (3.4) is for electrons while (3.5) is for holes; R_{net} is the recombination rate, J is the current density, n and p are the electron and hole density,respectively. In fact all the quantities with the pedix n are referred to electrons while the ones with p to holes.
  What differs the hydrodynamic model from others is the definition of J_n(eq (3.6)) and J_p ((3.9)). In fact they become

$$J_n = \mu_n(n\nabla E_C + kT_n\nabla n - nkT_n\nabla ln\gamma_n + \lambda_n f_n^{td} kn\nabla T_n - 1.5nkT_n\nabla lnm_n) \tag{3.6}$$

$$J_p = \mu_p(p\nabla E_V - kT_p\nabla p + pkT_p\nabla ln\gamma_p - \lambda_p f_p^{td} kp\nabla T_p + 1.5pkT_p\nabla lnm_p) \quad (3.7)$$

The terms involved are linked to the spatial variations of electrostatic potential, electron affinity, band gap, gradient of the concentration, carrier temperature gradient and spatial variation of the effective masses. Other informations can be found in the Sentaurus manual. [13]
Since this model is suitable for devices with small active regions, we implement it and the consequent current is (figure 3.2)

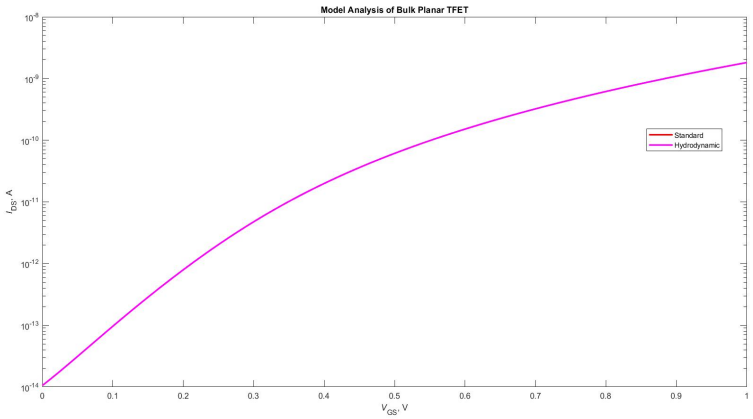


Figure 3.2: $I_{DS}(V_{GS})$ with standard models and Hydrodynamic

- **Incomplete Ionization**

Generally, in silicon, dopants can be considered to be fully ionized at room temperature because the impurity levels are sufficiently shallow. However, when impurity levels are relatively deep compared to the thermal energy or the working temperature is low, incomplete ionization must be considered. For these situations, Sentaurus Device has an ionization probability model based on activation energy. The concentration of ionized impurity atoms can be written as

$$N_D = \frac{N_{D,0}}{1 + g_D exp(\frac{E_{F,n} - E_D}{kT})} \quad (3.8)$$

$$N_A = \frac{N_{A,0}}{1 + g_A exp(\frac{E_A - E_{F,p}}{kT})} \quad (3.9)$$

Where N_0 is the substitutional concentrations, g is the degeneracy factor for the impurity levels and E the ionization energy; as usual, n-pedix is referred to electrons quantities while with p to holes one [13].

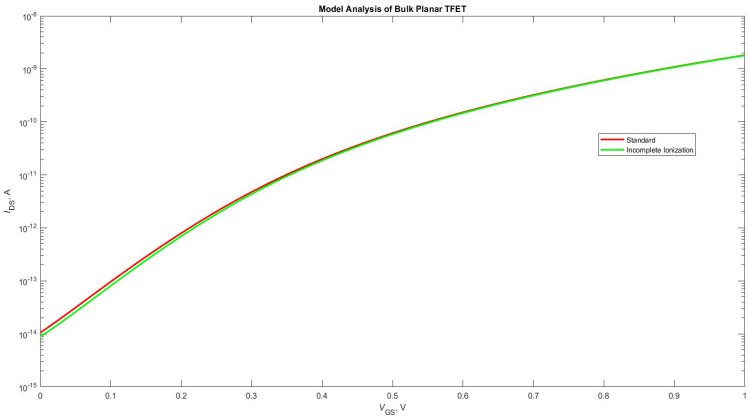


Figure 3.3: $I_{DS}(V_{GS})$ with standard models and Incomplete Ionization

Considering this model in the Physics section of Sdevice, we obtain (removing the Hydrodynamic one) the following current (3.3).

As shown in figure 3.3 a variation is present, especially near the I_{OFF} value. This confirms that this model is correct for our device because the value of the doping, above all the source one, is high (p^{++}) and so it has to be considered.

- **Mobility refinement**
  Then we try to implement some models concerning the mobility in the following way:

  Physics
  {
  ...
  Mobility(Tunneling DopingDep HighFieldsaturation Enormal)
  ...
  }

  Since *Tunneling* has already been mentioned, let's analyze the other three.
  For what concern the command *Enormal*, it selects the calculation of the field perpendicular to the interface between semiconductor and the insulator. In fact in the channel region of a TFET, this electric field forces carriers to interact strongly with this surface, scattering with acoustic surface phonons and surface roughness. Since there are several models to compute this field, the one choiche by default is the Lombardi one. As a consequence the mobility can be calculated through the following formula

$$\frac{1}{\mu} = \frac{1}{\mu_b} + \frac{D}{\mu_{ac}} + \frac{D}{\mu_{sr}} \tag{3.10}$$

  Where D is a damping, μ_b is the bulk mobility, μ_{ac} is the contribute due to acoustic

phonon scattering and μ_{sr} is the one attributed to surface roughness scattering. The formula (3.10) is given by the Matthiessen's rule. Other informations can be found on the Sentaurus manual. The effect of *Enormal* is represented in figure 3.4.

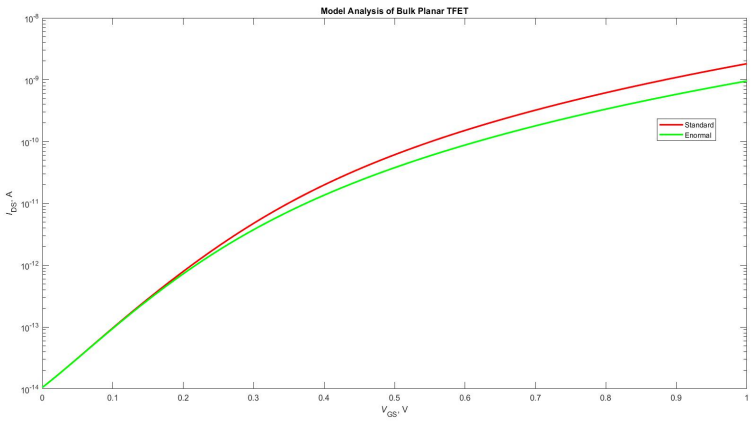


Figure 3.4: $I_{DS}(V_{GS})$ with standard models and Enormal

DopingDep instead takes into account the fact that, in doped semiconductors, scattering of the carriers by charged impurity ions leads to degradation of the carrier mobility. Between the several options, the Masetti model is the one considered. The dependence of the mobility by the doping and the definition of the parameters can be found on the Sentaurus manual [13]. The effect on the current can be observed in the figure 3.5.

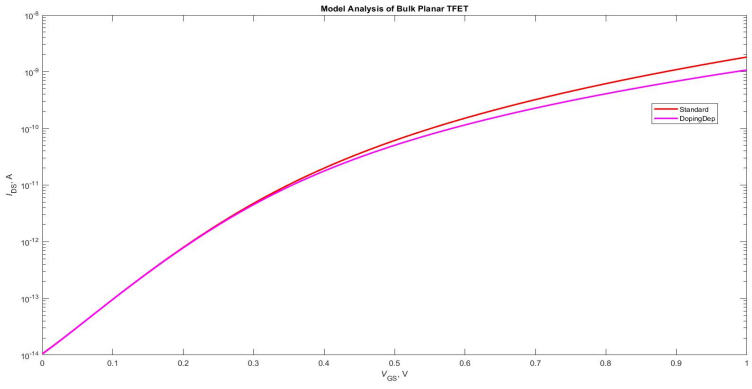


Figure 3.5: $I_{DS}(V_{GS})$ with standard models and doping dependace of the mobility

Finally the command *HighFieldSaturation* states that, in presence of high electric fields, the carrier drift velocity is no longer proportional to the electric field, the mobility is not constant and so the velocity saturates to a finite speed. Although Sentaurus has different models, the one used here is the Canali model, which computes the mobility as

$$\mu = \frac{(\alpha+1)\mu_{low}}{\alpha + [1 + (\frac{(\alpha+1)\mu_{low}F_{hfs}}{v_{sat}})^{\beta}]^{\frac{1}{\beta}}} \tag{3.11}$$

μ_{low} is the low-field mobility, v_{sat} is the saturation velocity and F_{hfs} is the driving field. More details can be find on the Sentaurus manual [13].

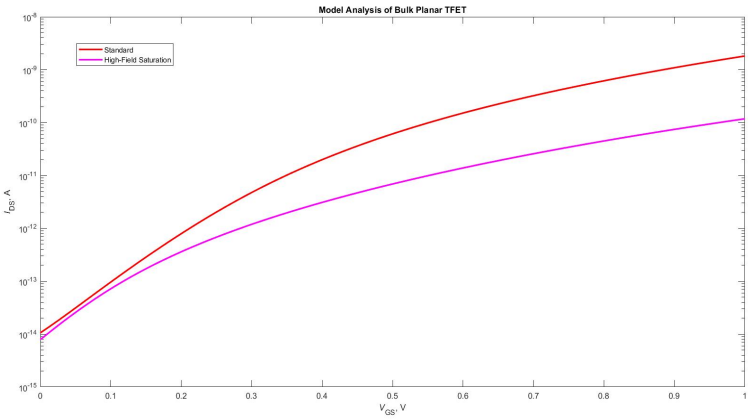


Figure 3.6: $I_{DS}(V_{GS})$ with standard models and high-field saturation of the mobility

Looking at figure 3.6, you can see that this model has an huge impact on the transcharacteristic, in particular on the ON current; this is due to the fact that this device not only suffers of very high electric fields, but its channel is not short enough to consider ballistic transport.

- **Band Gap Narrowing**
  The command *BandGapNarrowing* takes into account the shrink of the BG that occurs when the impurity concentration is particularly high. From a mathematical point of view it can be expressed as

$$E_{bgn} = \Delta E_g^0 + \Delta E_g^{Fermi} \tag{3.12}$$

  where ΔE_g^0 is determined by the particular bandgap narrowing model used while ΔE_g^{Fermi} is an optional correction to account for carrier statistics. We choose the Slotboom model and the ΔE_g^0 used can be found on the Sentaurus manual [13]. We implement it on the sdevice in the following way
  Physics
  {

.....
EffectiveIntrinsicDensity(BandGapNarrowing(Slotboom) Fermi)
....
}

The effect of this model can be seen in the figure 3.7 and it can be observed an improvement of the I_{on}/I_{off} ratio.

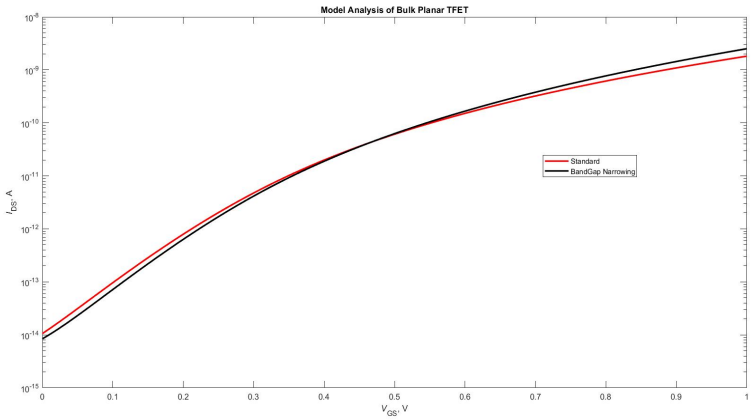


Figure 3.7: $I_{DS}(V_{GS})$ with standard models and BandGap Narrowing

- **Recombination refinement** Then we try to implement some models in the Recombination part: *SRH(DopingDep)* and *Auger*.
  SRH considers the recombination due to deep defect levels in the gap. From a mathematical point of view it is computed through the following formula

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \tag{3.13}$$

  where n and p are the electrons and holes concentrations while τ is the carriers lifetime. In particular the argument DopingDep involves a doping dependence of the lifetimes of the carriers inside the material. The effect of *SRH(DopingDep)* is represented in the figure 3.8

  Although there are no differences with the standard path, we consider it for completeness.
  Auger takes into account a recombination process that involves three bodies (2 electrons and 1 holes or the opposite). The rate of this band to band mechanism is given by the following formulas (3.14)

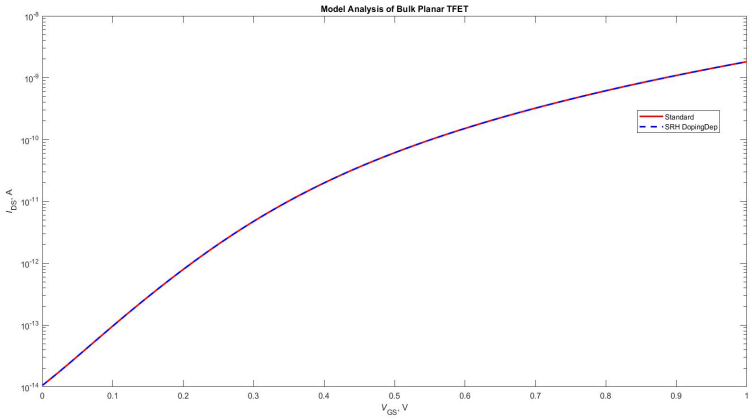


Figure 3.8: $I_{DS}(V_{GS})$ with standard models and SRH(DopinDep)

$$R^{A}_{net} = (C_n n + C_p p)(np - n^2_{i,eff}) \tag{3.14}$$

where C_n and C_p are the temperature-dependent Auger coefficients.

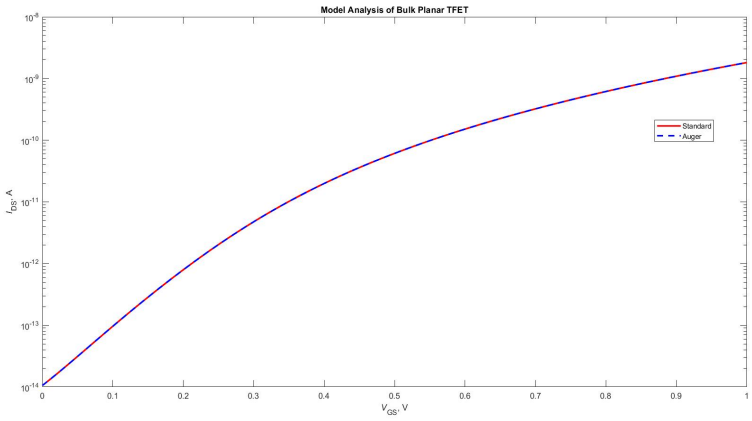


Figure 3.9: $I_{DS}(V_{GS})$ with standard models and Auger

Again the new curve is equal to the standard one (3.9) but in order to be accurate the Auger model has to be considered.

- **Density Gradient**
  Since TFET is based on a quantum effect, we prefer to include quantization effects in the classical device simulation. This is realized, from a mathematical point of view, introducing a potential-like quantity Λ_n in the classical electron density formula:

$$n = N_C F_{1/2}\left(\frac{E_{F,n} - E_c - \Lambda_n}{kT_n}\right) \tag{3.15}$$

  Similarly for holes. Density gradient is one of the several models that give a definition to Λ_n, that can be seen on the Sentaurus manual [13]. We apply this model in the sdevice section in the following way:

  Physics
  {
  .....
  eQuantumPotential
  hQuantumPotential
  ....
  }

  Obtaining the following plot (fig 3.10)

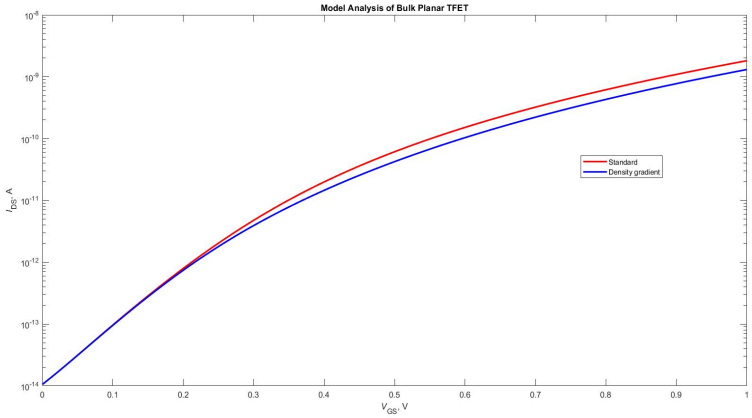


Figure 3.10: $I_{DS}(V_{GS})$ with standard models and Density gradient

We can appreciate a little variation for increasing voltages, but also the computational cost is very high.

- **Complete**
  Finally the complete *Physics* section used in Sdevice is written in [mettere nelle ultime pagine] and the consequent current is (fig 3.11)

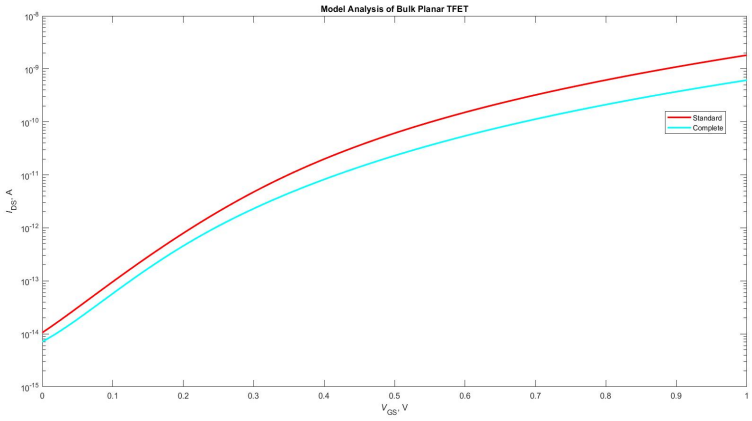


Figure 3.11: $I_{DS}(V_{GS})$ with all the relevant models

The figures of merit of this transcharacteristic are reported in the table 3.1

I_{ON}	I_{OFF}	I_{ON}/I_{OFF}	V_{TH}	SS
6.1222e-10 A/μm	7.1303e-15 A/μm	8.5862e+04	$\simeq$ 0.4	107

Table 3.1: Figures of merit of our bulk planar TFET

These quantities are almost acceptable: in fact the I_{ON}/I_{OFF} ratio is approximately 10^5, as needed by a TFET, and the other quantities are right since we not consider some boosters that can improve them.

Chapter 4

Electrical simulations

After determining the physical models to describe the tunneling effect appropriately (consistent with the values found in literature [1]), electrical simulations were performed. At first it is important to show the band diagram at equilibrium (figure 4.1): in this way we understand what is the "starting point" of our device; as we expected [20], in this situation the conduction band of the intrinsic material is above the source one and so only few carriers flow through the channel.

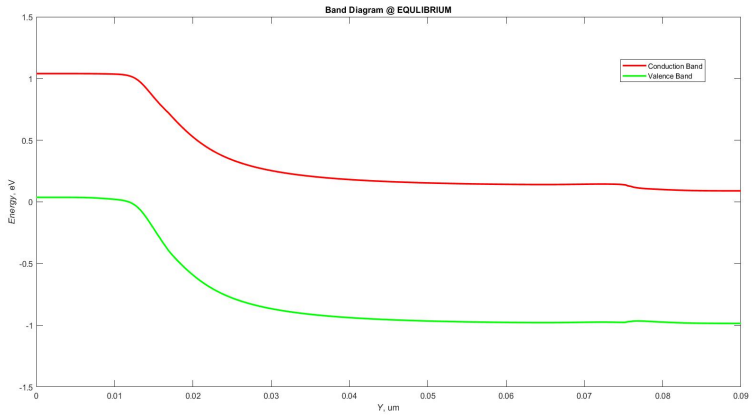
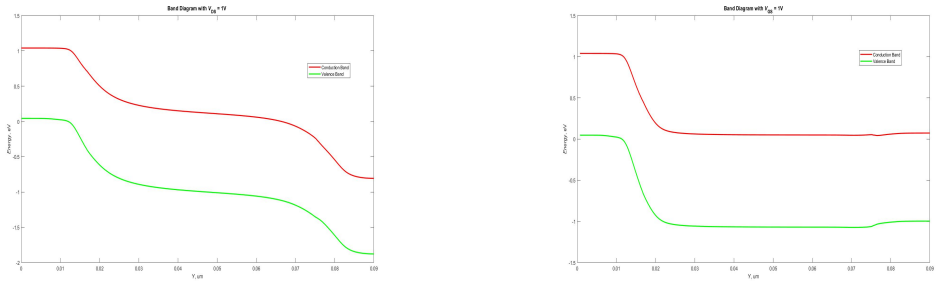


Figure 4.1: Band diagram at equilibrium

In order to appreciate the behavior of this planar bulk TFET, different voltages are applied, both to gate (from 0 to 1 V) and drain (from 0 to 1 V). The effect of them is represented in figure 4.2
In figure 4.2a is shown the effect of the drain voltage that only shift the conduction



(a) $V_{DS} = 1V$ (b) $V_{GS} = 1V$

Figure 4.2: Effect of drain and gate voltages

and valence bands of the drain region of the planar TFET downward. As a consequence, even if some electrons can flow, the device is off. In figure 4.2b instead the gate voltage is applied and a movement of the conduction and valence bands of the channel region is appreciate, again downward. In this case the conduction band is quite equal to the valence band of the source region and so a certain value of current start to be present. The displacement in both cases is always toward the bottom because the applied voltages are positive.
In order to have a complete turn on of the TFET, both the voltages has to be applied and the values chosen as reference are 1V. With them the consequent band diagram is (figure 4.3): it is possible to see that the conduction band of the channel is below the VB of the source thanks to the gate voltage but also the bands of the drain are shifted downward, facilitating the flow of electrons from source to drain.

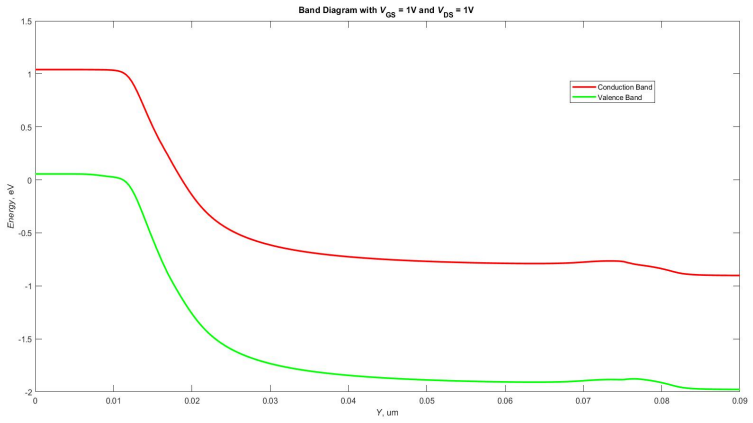
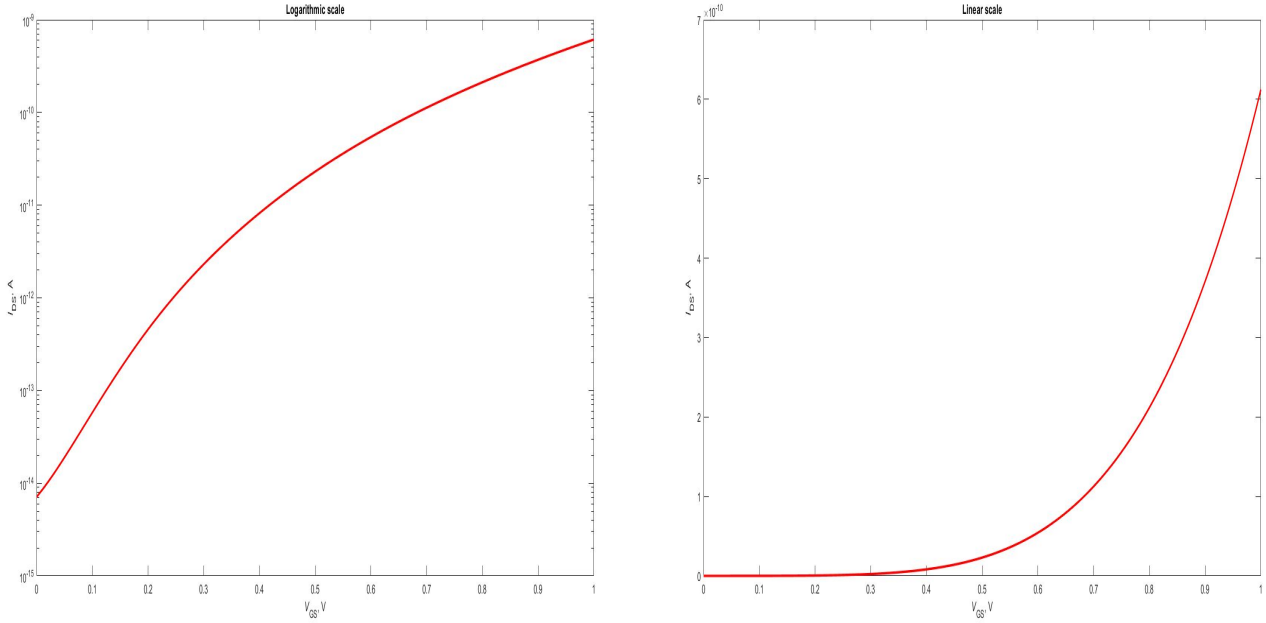


Figure 4.3: Band diagram of the ON condition

For what concern the current, it is plotted in figure 4.4
The logarithmic scale (fig 4.4a) is useful to appreciate the values of I_{ON}, I_{OFF} but



(a) Logarithmic scale

(b) Linear scale

Figure 4.4: Transcharacteristic of Bulk Planar TFET

also the slope while the linear scale (fig 10.13) to see the value of V_{TH}, that is approximately the value of voltage for which the current becomes different from zero. It is interesting to see the effect of the variation of a voltage maintaining the other constant.

4.1 Transcharacteristic: V_{DS} dependance

The following plot (4.5) is obtained for a gate voltage in the range (0-1)V for V_{DS}=1,2 and 3V. What is possible to see is that, increasing V_{DS}, the I_{ON} increases but also the I_{OFF}. In particular the last where, for V_{DS} = 3V, is very high, showing an ambipolar effect. Looking at the table 4.1, it can be understood that this planar bulk TFET is optimized to work in a range of drain voltage less than 3V. In fact, although the I_{ON} continues to grow with the increasing of V_{DS}, the variation is very small compared to the increase of the I_{OFF} which grows by almost three orders of magnitude when V_{DS} becomes 3V. In other words, with the increase of V_{DS} one of the disadvantages of the TFET is contrasted, that is the low I_{ON}, but another one is increased, that is the ambipolarity. In order to understand what are the best working conditions the ratio of I_{ON}/I_{OFF} has to be seen, which from literature [23]

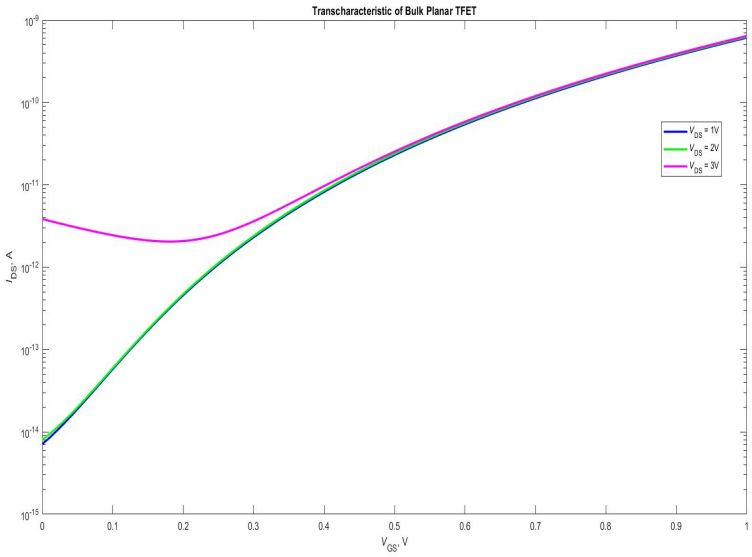


Figure 4.5: Transcharacteristic with V_{DS} 1V, 2V and 3V

V_{DS}	I_{ON}	I_{OFF}	I_{ON}/I_{OFF}
1V	6.1222e-10 A/μm	7.1303e-15 A/μm	8.5862e+04
2V	6.2622e-10 A/μm	8.0329e-15 A/μm	7.7957e+04
3V	6.4083e-10 A/μm	3.8439e-12 A/μm	166.7134

Table 4.1: Figures of merit comparison for different V_{DS}

must be about 10^5. Since it is reached for V_{DS} = 1V and 2V but not for 3V, this last one has to be avoided.

4.2 Output characteristic: V_{GS} dependance

The output characteristic analysis shows a good behaviour: the current seems to increase in a linear way for every value of V_{GS}, the saturation is reached in all cases and the threshold can be localized in a range between 0.2 and 0.5 V.

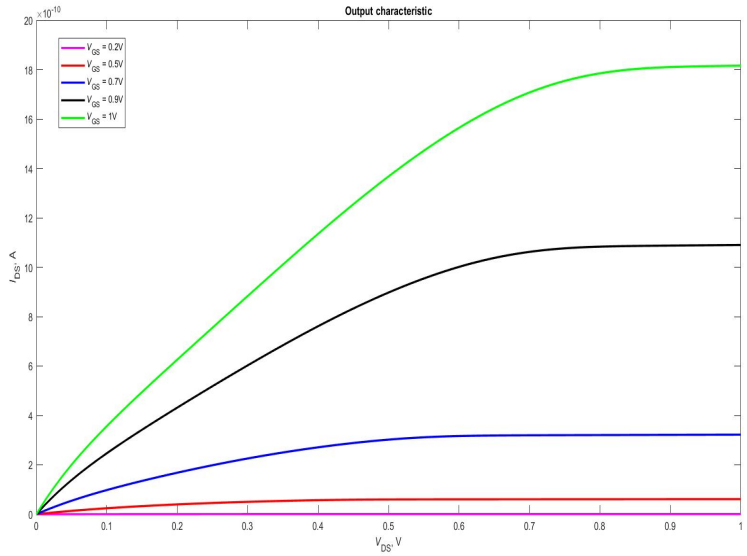


Figure 4.6: Output characteristic comparison

Part II

FINTFET

Chapter 5

Structure

The creation, as for the prototype device (planar), is done on the Sentaurus tool Sprocess [14]. The implementation is made following rigorous fabrication steps from a practical point of view; this because the transistor is thought for a realistic realization.
The standard structure consists in an initial substrate (5.1) made in silicon, which dimensions are 180 nm of heigth, 62 nm of width and 100 nm of length; it is p-doped and the concentration is 10^{15}.

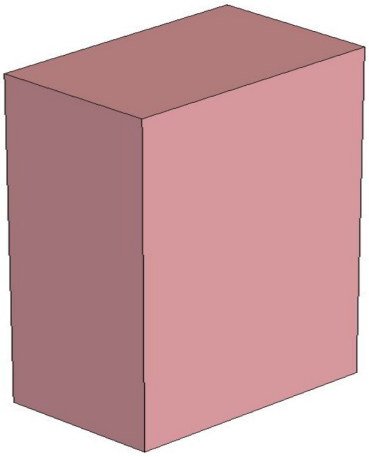


Figure 5.1: Initial substrate of the FinFET

The first step is the creation of the Fin from the substrate; to do this a non-litographic technique, called sidewall image transfer (SIT), is performed. So a first thermal oxidation is done with a temperature of 900 °C for 4 minute, obtaing an oxide layer of about 3.5 nm; after this a layer of silicon nitride is deposited above it with a thickness of 16.5 nm. Then another layer of amorphous silicon is grown over it with a thickness of 19.5 nm and after is etched with a proper mask; then oxide layer is

firstly deposited in an isotropic way and then etched anisotropically. In this way the remaining oxide near the amorphous silicon will define the width of our Fin.
At this point an etching of a-Si, nitride (using the remaining oxide as a mask), oxide and silicon is performed obtaining the Fin (5.2).

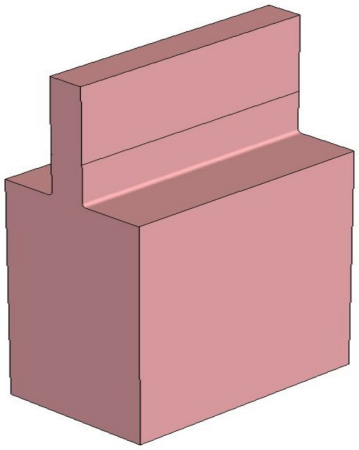
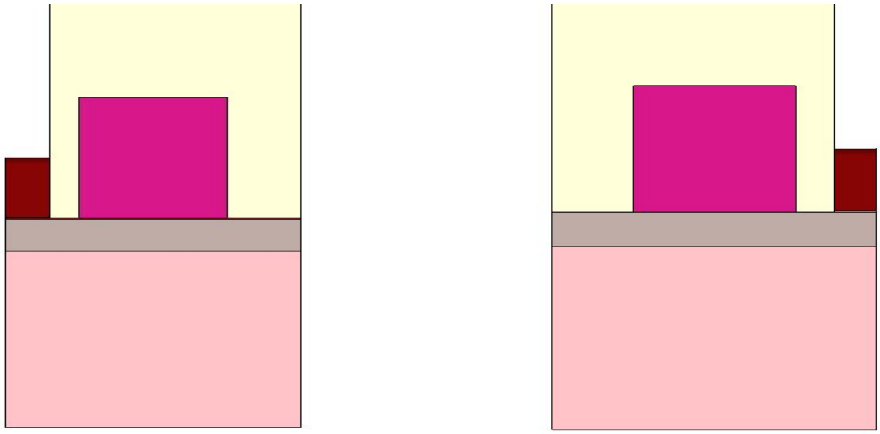


Figure 5.2: Fin structure

After that two regions of TEOS, a chemical organic compound, are obtained at the sides of the Fin in order to physical separate it from the substrate. Then the shape is rounded with an anisotropic etching and deposition of thin layer of silicon (this is done because it could be useful in order to perform an epitaxial growth over it to apply stress along the channel); at this point there is the creation of the dummy gate: firstly an oxide layer is deposited to prevent unwanted damages of silicon during the dummy gate removal, then the surface is covered with polysilicon and finally it is removed from the source and drain regions.
The construction of the device continues with the definition of the doping profile; given the nature of the TFET, it is not possible to perform this in one step. In fact source and drain are doped in an opposite way, so to at least two steps are necessary: firstly a resist is deposited, through a mask, over the gate and drain regions leaving the source exposed and a boron implantation is performed (5.3a), then the resist is removed and in an analogue way is performed the doping of the drain using phosphorus (5.3b) (look at A for more details). In order to activate the dopants a very rapid (fraction of ms) thermal annealing with a temperature of 1050 °C is realised obtaining figure 5.4.



(a) Source creation (b) Drain creation

Figure 5.3: Source-Drain doping setup

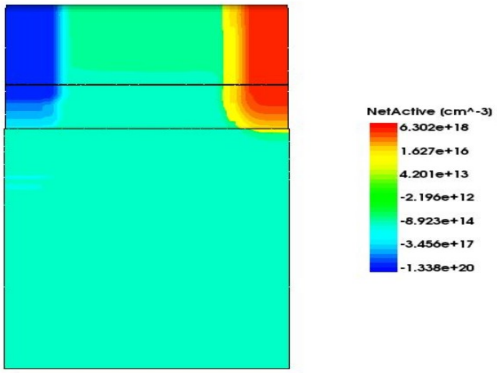


Figure 5.4: Final doping profile

At this point an oxide layer is deposited isotropically and removed with an anisotropic etching, remaining only at the sides of the dummy gate and the same is made with the silicon nitride, creating the spacers (figure 5.5).
After this steps, the silicidation is performed. This process consists into grown the TiSilicide in the source and drain regions above the silicon. Then a thick layer of PSG is deposited over the whole device and etched in order to protect the Source and Drain contacts and planarize the structure. This is useful to protect it during the dummy gate removal: in fact the polysilicon and the oxide in the gate region are removed (5.6a) and then the M-O-S structure is obtained depositing here the oxide (for technological compatibility), the hafnium and finally the aluminum with proper thicknesses(5.6b).

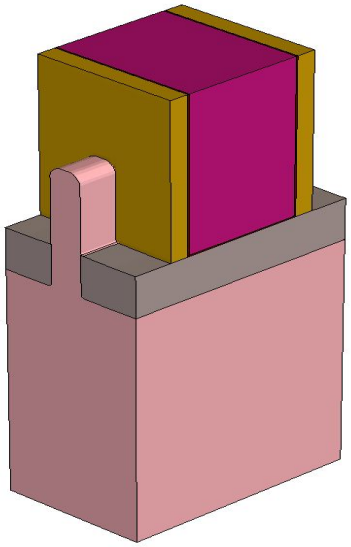
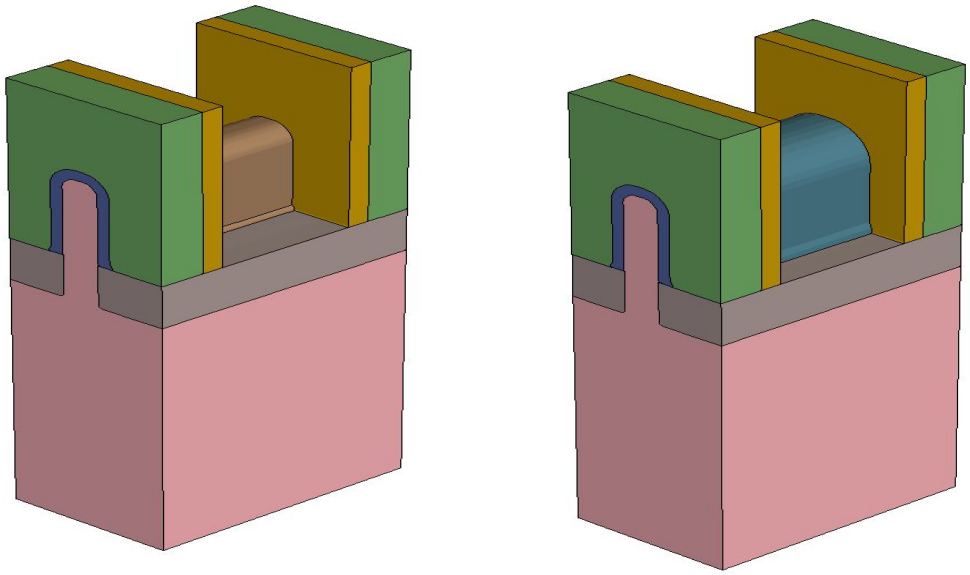


Figure 5.5: Creation of the spacers



(a) Silicdation, PSG deposition and Dummy gate removal

(b) Gate aluminum deposition

Figure 5.6: Gate aluminum deposition

The last step is the contacts deposition and definition: for this scope the cavity over the gate is filled with tungsten while two holes are digged in the PSG above source and drain and filled with tungsten. Finally the structure is completed by shaping the

gate contact and surrounding it with silicon nitride(5.7). To conclude the sprocess

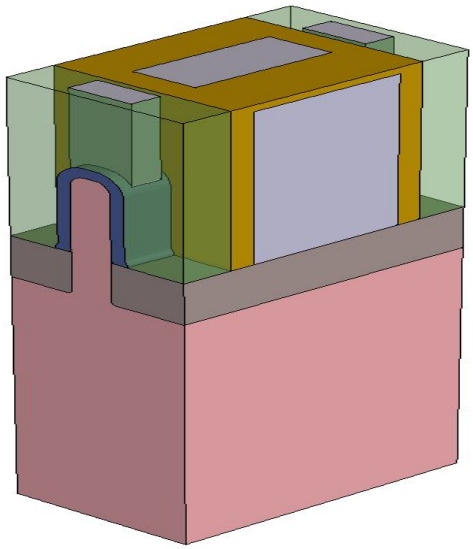


Figure 5.7: Final structure

definition a proper meshing of the device in the region of interest is performed and in particular for what concern the silicon channel (where the conduction takes place) (5.8).

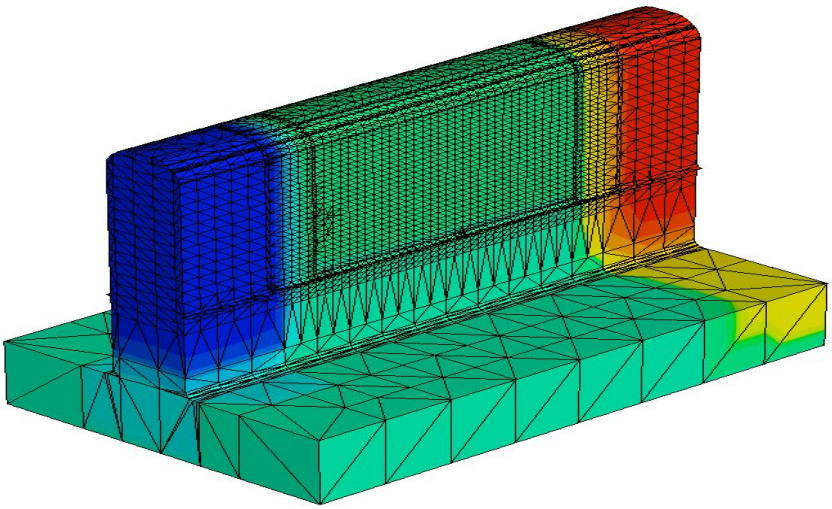


Figure 5.8: Mesh

Chapter 6

Electrical simulations

Using the same sdevice considered for the planar TFET, the following electrical simulations can be performed; consider that all the band diagrams related to the FinFET structure are inverted on the abscissa due to the definition of the device on sentaurus.
At the equilibrium condition the band diagram is (6.1).

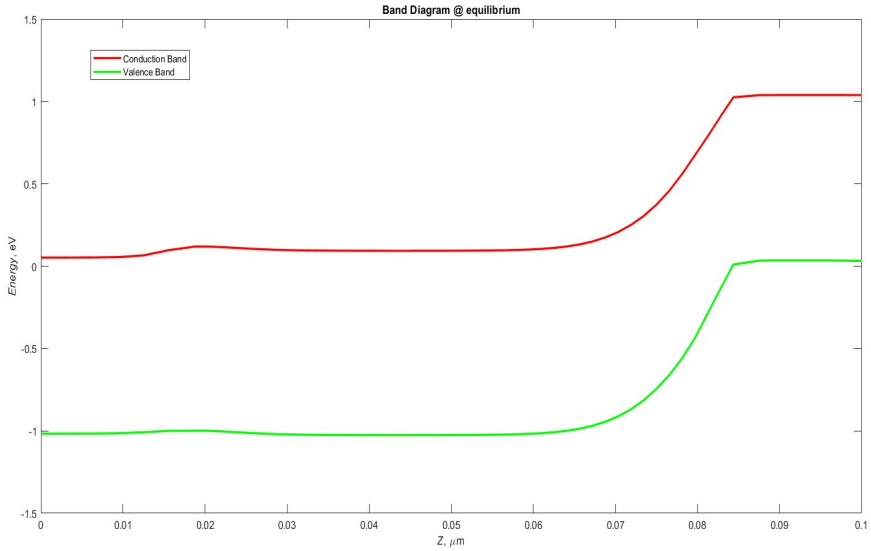


Figure 6.1: Band diagram at equlibrium

Applying the reference voltages (V_{GS} = 1V and V_{DS} = 1V) it becomes (6.2) and the consequent transcharacteristic is (6.3).
The band diagrams behave as expected and in a coherent way with respect to what

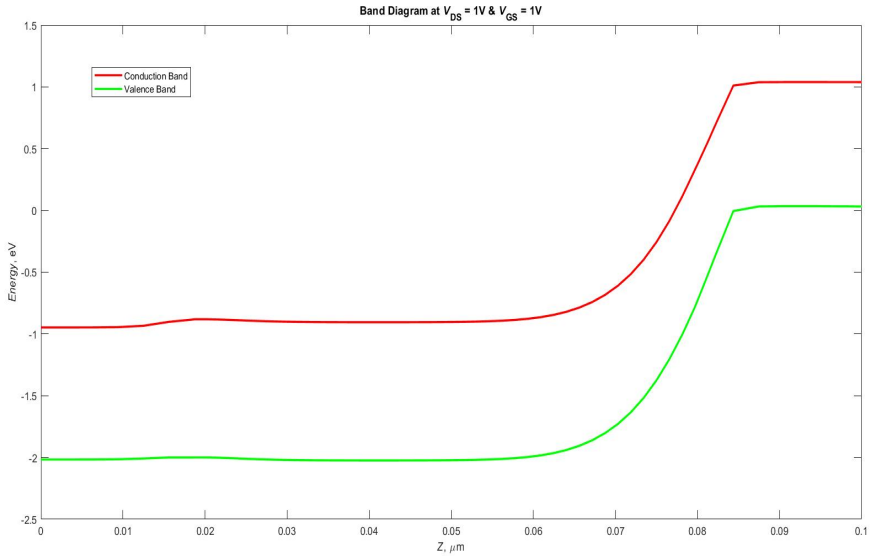


Figure 6.2: Band diagram at standard voltages

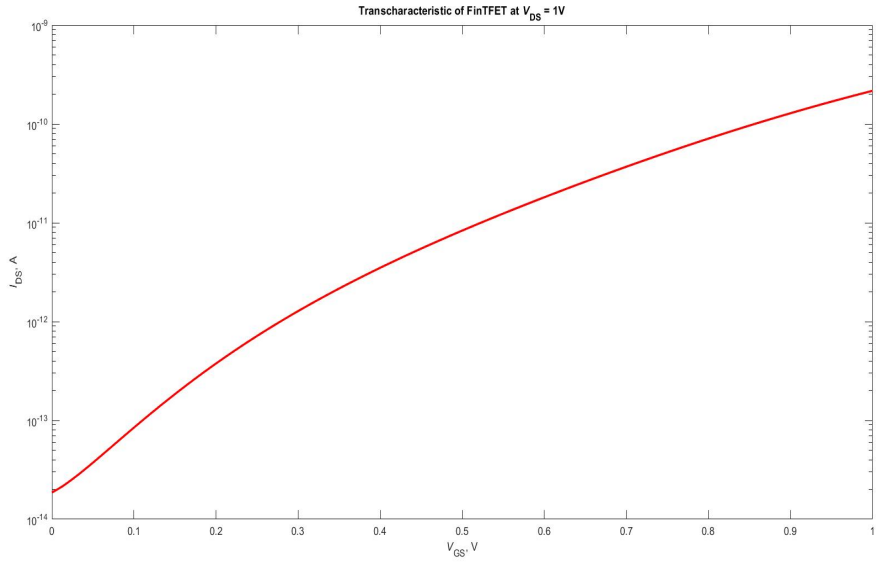


Figure 6.3: $I_{DS}(V_{GS})$ for the standard FinTFET @V_{DS}=1V

happened in planar structure; however, differently from the reference structure, a small "hump" appears at the drain-channel interface, slowing down the device. In

fact this defect can represent a barrier that does not allow the electrons to pass for value of voltage near to the threshold condition. This consideration results in a worse transcharacteristic, with respect to the planar one (4.4a), for what concern the threshold voltage and the subthreshold swing.
Moreover can be observed that the I_{ON} value is lower, but considering that also the cross section of the channel is lower (recall that the planar width is 1 μm), it is realistic; indeed, if it is considered the current per unit length (6.1) [20], for this structure the I_{ON} is about 2 nA/μm while for the planar structure was of the order of 0.6 nA/μm. Instead, for what concern the I_{OFF}, due to different possible causes such as a less regular doping profile with respect to the planar structure, it turns on to be slightly higher ($\simeq$ 0.2 pA/μm) with respect to the planar device ($\simeq$ 7 fA/μm); however this should not be a critical problem from the moment that it remains in an acceptable range.

$$I_{DS,0} = \frac{I_{DS}}{2H_{Fin} + W_{Fin}}. \tag{6.1}$$

6.1 Transcharacteristic: V_{DS} dependance

Similar to the planar case, there is an increase of the ambipolarity with the V_{DS} voltage, but compairing 6.4 and 4.5, it is possible to see that in the FinFET structure this dependence is stronger and the ambipolarity becomes detrimental for lower value of the applied voltage. As a consequence must be taken into account that for this kind of device there is a lower range for the possible V_{DS}.
This probably happens due to the smaller dimensions of the Fin with respect to the planar; this causes a huger voltage drop on the drain region and so a greater shift in terms of band diagram that increases the ambipolarity current from drain to channel. Moreover you have to consider that the doping profile is different due to the different complexity in its definition for 3D structures, so a different behavior is expected.

6.2 Output characteristic: V_{GS} dependance

Considering the output characteristics taken at different gate voltages (6.5), it is possible to observe that at low values of V_{DS} the curves increase in a non-linear way; this is probably due to the hump seen before and to the non ideal doping profile of the source. Moreover it is possible to localize the threshold voltage between 0.2-0.5 V and to appreciate a good saturation of the current in considered range of V_{GS}, although, looking at figure 6.5, this seems to be slightly worse for high values of V_{GS}.

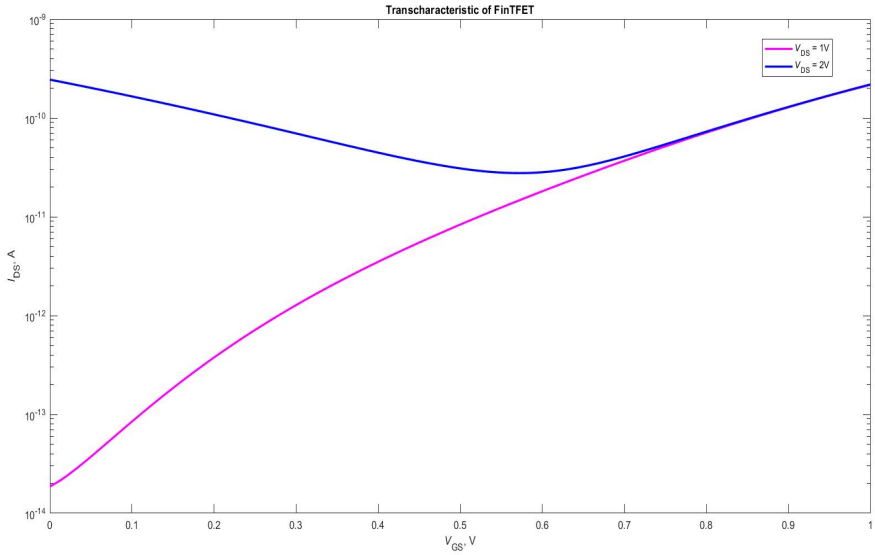


Figure 6.4: $I_{DS}(V_{GS})$ with different V_{DS}

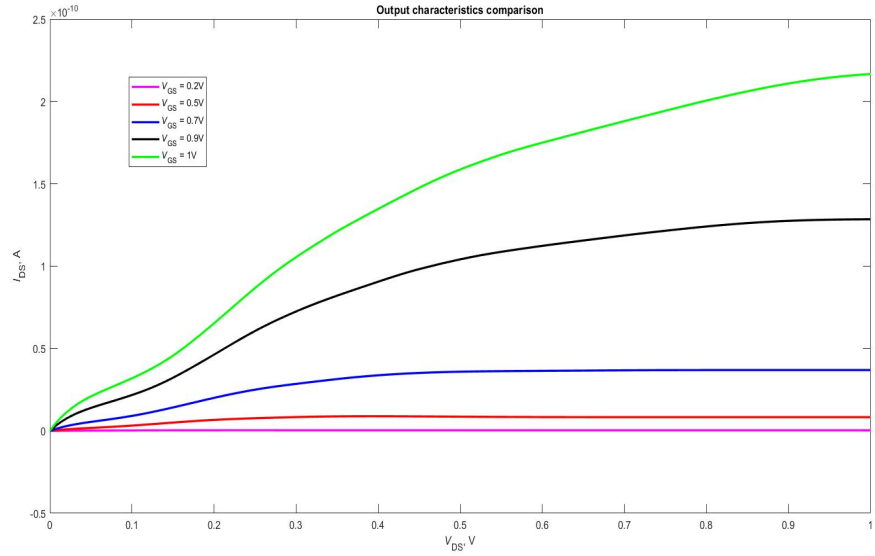


Figure 6.5: Output characteristic comparison

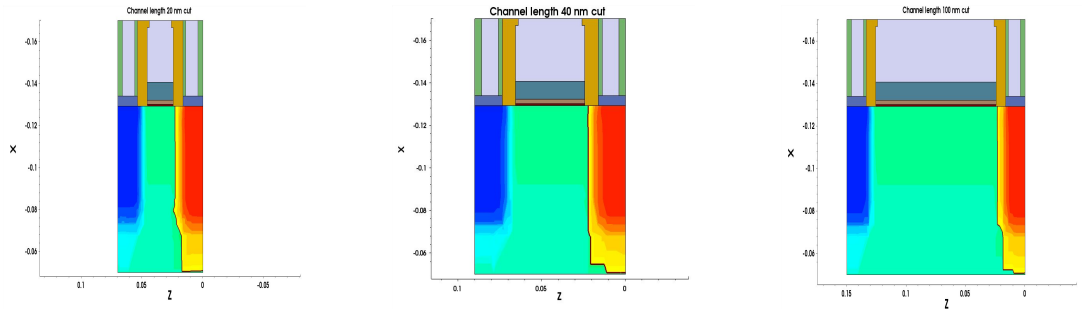
Chapter 7

Parameters dependence

In this chapter will be evaluated the impact of the different physical parameters involved in the TFinFET structure. In particular, starting from the standard device, the parameters are modified one by one keeping the rest unchanged and an evaluation of the effects is performed looking at the new transcharacteristics; every time that a new variable is modified, the previous one is restored to the standard value. All the transcharacteristics are computed at fixed $V_{DS} = 1V$ and V_{GS} between 0 and 1V in order to compare each other.
If relevant also the band diagrams are shown otherwise refer to figure 6.2.

7.1 Channel length

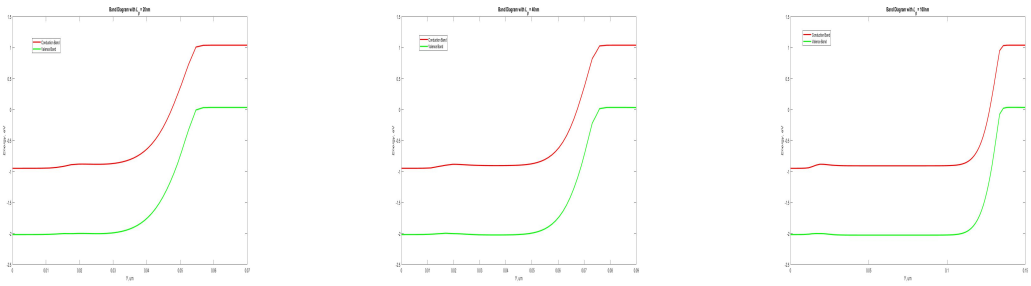
The first parameter that is treated is the channel length. Clearly it has a huge impact on the current and, in particular, the values investigated are 20, 40, 50 (reference value) and 100 nm. The modifications of the device, expect for the standard value, are represented in the figure 7.1



(a) $L_g = 20nm$ (b) $L_g = 40nm$ (c) $L_g = 100nm$

Figure 7.1: Device modification with different channel length

Changing the channel length, the band diagram changes accordingly obviously; as a consequence it is important to represent it (fig 7.2) From this figures is possible



(a) $L_g = 20nm$ (b) $L_g = 40nm$ (c) $L_g = 100nm$

Figure 7.2: Band diagram with different channel length

to understand what impact they have on the transcharacteristic: In fact, increasing the channel length from 50nm to 100nm no problems appear while decreasing it the two junctions (source-channel and channel-drain) become no more distinguishable, causing the deterioration of the features of the device, clearly appreciable from the $I_{DS}(V_{GS})$ curves (7.3)

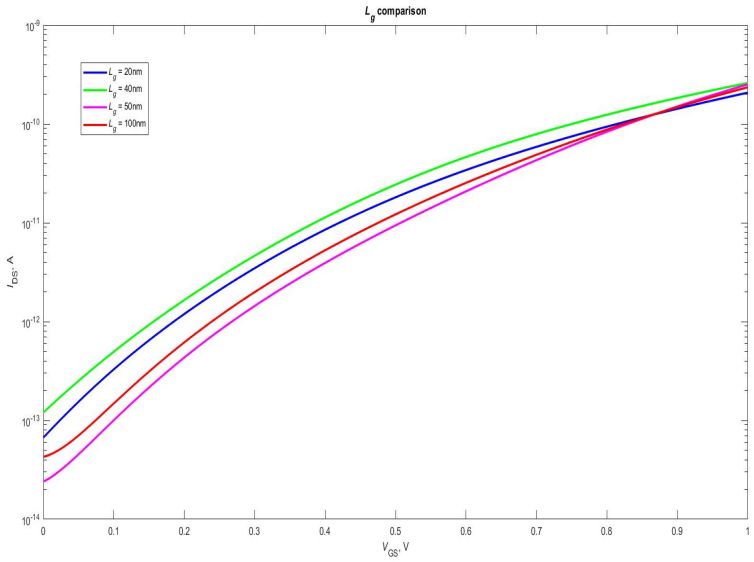
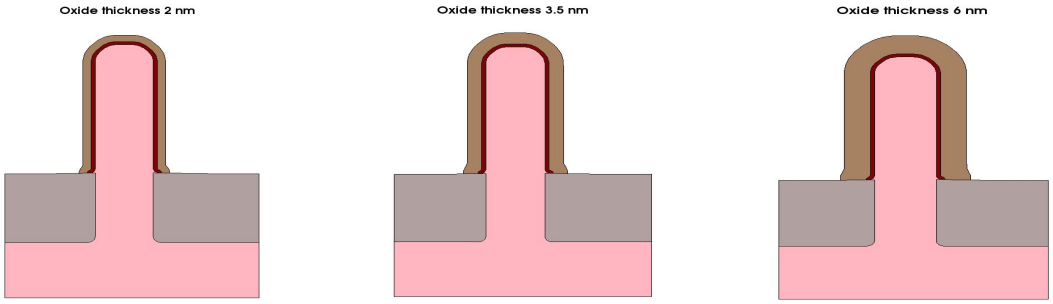


Figure 7.3: $I_{DS}(V_{GS})$ with different channel length

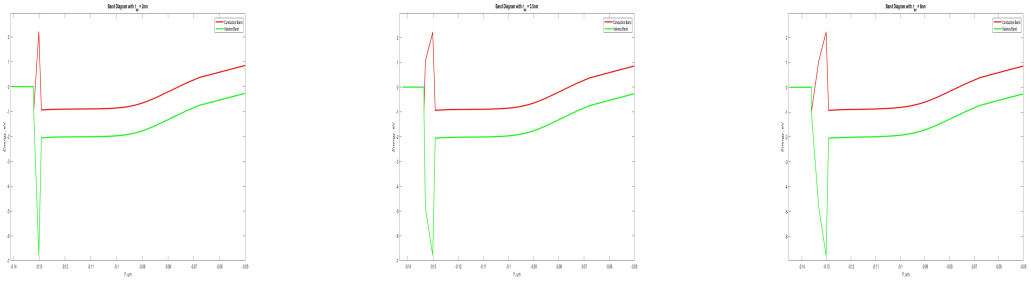
7.2 Oxide thickness

In this section is analyzed how the device transcharacteristic changes by varying the thickness of the gate oxide layer. In particular what changes is the thickness of the hafnium oxide while the silicon dioxide remains of 1 nm; As shown in figure 7.4 the thicknesses chosen for this analysis are 2 nm (standard), 3.5 nm and 6 nm and for completeness the band diagrams along the MOS direction are reported in figure 7.5.



(a) 2 nm (b) 3.5 nm (c) 6 nm

Figure 7.4: Oxide thicknes



(a) 2 nm (b) 3.5 nm (c) 6 nm

Figure 7.5: M-Ox-S band diagram

What is possible to see from the trancharacteristics comparison (figure 7.6) is that, increasing the thickness of the oxide, we have a rigid shift of the curve towards lower current values. This happens because for higher oxide thickness decreases the gate leakage current, but on the other hand the electrostatic control on the channel is decreased resulting in a lower I_{ON}.
So in the choice of this parameter it must be taken into account that there is a trade-off between the on and the off current; this is the reason why for the standard device was chosen a thickness of 2 nm, in fact even if in this way the off current increases it is possible to obtain an higher on current that is one of the weakness of this technology.

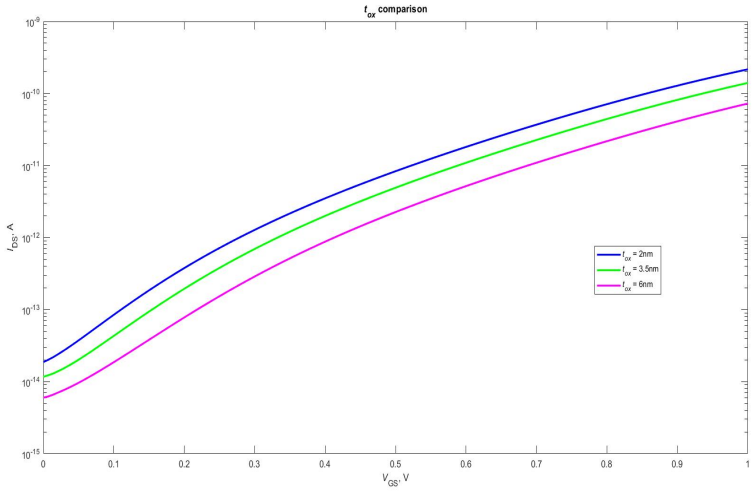


Figure 7.6: $I_{DS}(V_{GS})$ with different oxide thickness

7.3 Metal workfunction

Another important parameter, that has an huge impact on the device behavior, is the choice of the gate metal and in particular its workfunction. In fact it plays an important role in the definition of the device threshold voltage and, as it is possible to see in figure 7.7, on the tuning and the compensation of the ambipolarity in the operative gate voltage range.
During the analysis different material has been tested, but only the relevant one are shown, and the most suitable one results to be the Aluminum and especially the amorphous crystalline configuration (WF $\simeq$ 4.1 eV); in fact, always referring to figure 7.7, it is possible to state that for lower values of WF the ambipolarity seems to shift towards negative gate voltages, however it is not convenient to choice too small values because with this shift there is also an increment of the I_{OFF}. On the contrary the higher is the WF the more the ambipolarity starts to enter inside the operative range making the device unusable as in the case of Copper. So it is necessary, depending on the type of structure you are realizing, to properly choose the gate metal in order to obtain the best trade-off obtaining the lowest possible I_{OFF} avoiding any problem caused by ambipolarity.

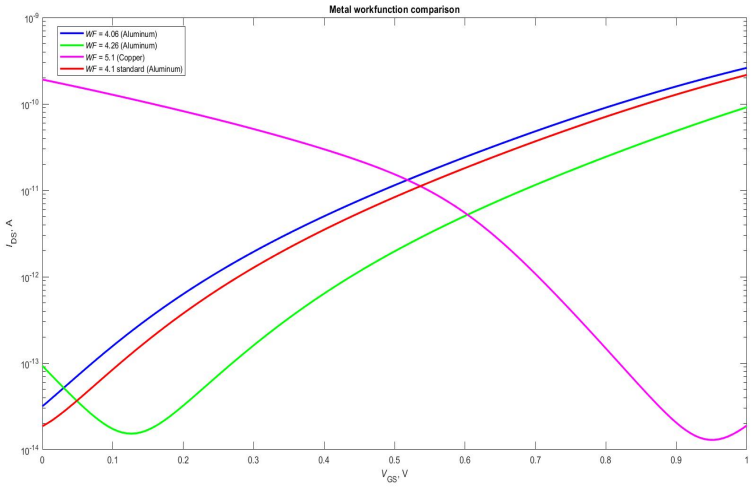


Figure 7.7: $I_{DS}(V_{GS})$ comparison with different gate metal. The blue curve refers to aluminum (110), the red one to amorphous aluminum, the green one to aluminum (111) while the magenta curve to Copper (100).

7.4 Channel doping

It is possible and, as it will be shown, necessary to properly choose the channel doping; in fact, as stated above, TFETs are barrier devices and the current is deeply related to it. Practically speaking, modifying the doping it is possible to promote the tunneling between source and the channel or to counter it.
For the standard structure an optimal channel p-doping of $10^{15}cm^{-3}$ has been chosen; this is in accordance with the theory of the device and allows a correct functioning. Looking at figure 7.8 can be seen that using higher values for the channel doping the transcharacteristic tends to remain unaltered in the on condition, but ambipolarity starts to appear, while choosing lower values, like for the $10^{14}cm^{-3}$ case, the device starts to shows a worse behavior and in particular it seems like it is always turned on.
Moreover also an n-type doping has been tested (7.9) and as expected the conduction inside the device has been largely enhanced ($I_{ON} \simeq 10^{-6}$ A), but as in the previous case the device can not be turned off at all.

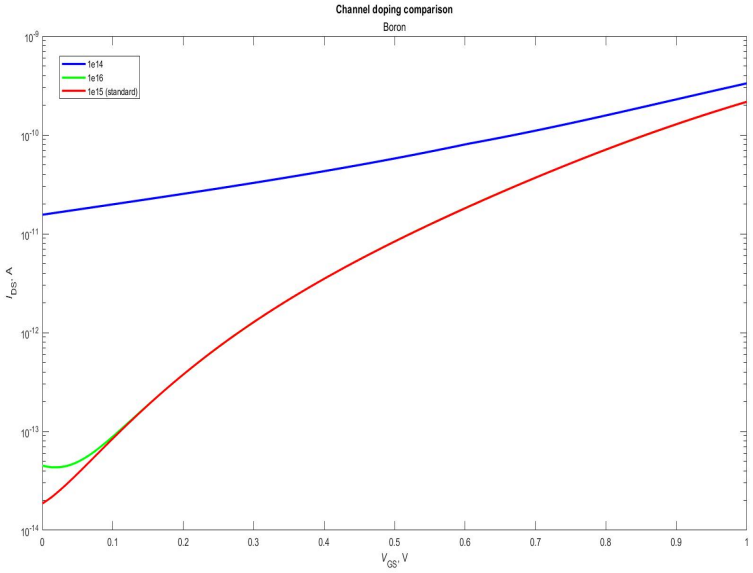


Figure 7.8: $I_{DS}(V_{GS})$ with different channel doping

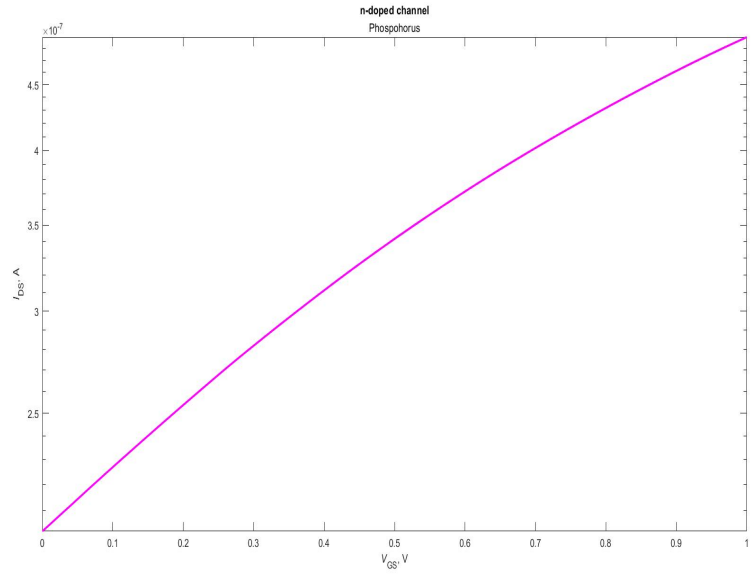


Figure 7.9: $I_{DS}(V_{GS})$ with a n-doped channel doping

7.5 Conclusions on FinTFET

Considering the results obtained, regarding the standard devices,the FinFET structure provides some advantages with respect to the planar one, but also other problems that seems to be strictly related to a more complex fabrication of the device; in particular the doping implantation and diffusion have the hugest impact on the performances. In fact, dealing with two different doping species (Boron and Phosphorus) it is very difficult to control the diffusion of both of them at the same time, so in the end one of them will have a worse profile. Moreover due to the three-dimensionality of the structure some issues related to the diffusion appear (this will be more evident in the NSGAAFET). These practical defects imply worsen figures of merit with respect to the expected ones, but they remain still in agreement if compared with the ones found in literature ([2],[4],[9], [16]).
However, from the performed analysis, it is possible to derive some important information about how this kind of devices behave with respect to the physical and structural parameters; for what concern the channel length, in this case, the best choice is 50nm: in fact, going below this value, some detrimental effects appear and, with this Silicon homostructure, is not possible to further shrinking the device. Considering the oxide thickness, it turns out that there is a trade-off between I_{ON} and I_{OFF}, so if you want to have the maximum possible I_{ON} at the expense of the I_{OFF} the right choice is to select the lowest possible thickness (depending on the lattice vector of the oxide and on the technology), while on the contrary a thicker layer can be deposited.
For the choice of the metal gate, Aluminum (in particular its amorphous configuration) seems to be the best choice for Silicon TFETs; however for different structure you have to consider that metals with lower WF provides a left-shift of the ambipolarity, but of course also an increasing of the I_{OFF}, on the contrary with higher WF the opposite happens. Finally the channel doping has a lower impact on the figures of merit and it is introduced in order to have a correct operation of the TFET; working on this parameter won't provide any improvement.

Part III

GAAFET

Chapter 8

Structure

The NSGAAFET structure is defined in the same way as the FinFET: in fact the substrate has a height of 120 nm, a width of 62 nm and a total length of 100 nm, of which 50 nm represent the channel; again the initial doping concentration is p^- (precisely 10^{15} cm^{-3} of Boron).
In order to obtain the nanosheets, isotropic depositions of silicon and silicon germanium above the whole substrate are performed with a certain thickness: the one of silicon represents the nanosheet height while the one of silicon germanium will be the space between the nanosheets. As happens for the FinFET, also in this case a SIT process is necessary: at first an oxide layer is obtained through a thermal oxidation, then, again isotropically, nitride and amorphous silicon are deposited (8.1).

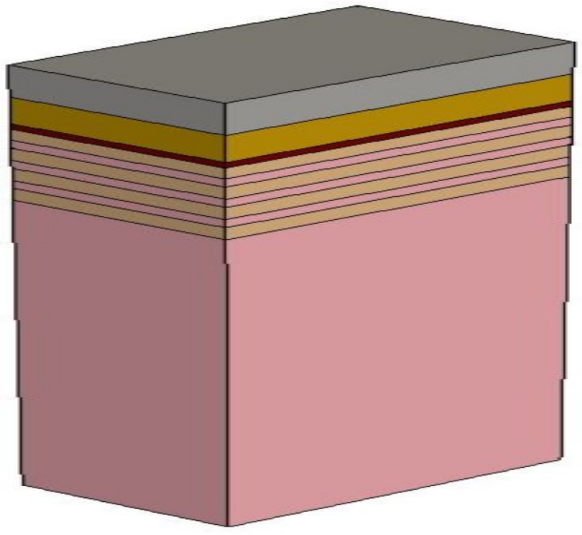


Figure 8.1: Nanosheet stack fabrication

After this the last one is etched with a proper mask and an oxide layer is firstly deposited in an isotropic way and then etched anisotropically. In this way the remaining oxide near the amorphous silicon will define the width of our nanosheet. At this point, using the oxide "wall", there is the complete etching of the amorphous silicon and of the silicon nitride (except for the region below the oxide) and then the etching of the oxide itself using the silicon nitride as a mask. After that there is the iterative etching of the silicon and silicon germanium using one of them to etch the other. This steps are used to obtain the nanosheets (8.2)

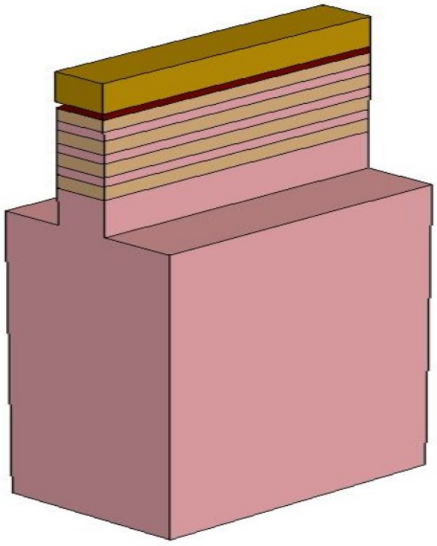


Figure 8.2: Nanosheet stack

At this point a deposition of TEOS on the bottom sides of the nanosheets is performed and then oxide and silicon nitride are etched. Then silicon and silicon germanium are etched to define source and drain regions and these contacts are recreated by depositing silicon, but before this step a triple implantation, with different energies (1, 10,20 keV), and a successive very long annealing (1050 °C for 400 seconds) are performed in order to obtain the right channel doping in the nanosheets. Then an oxide layer is deposited isotropically and, through a mask, polysilicon is deposited as a dummy gate (8.3).

For what concern the doping definition, it is similar to the Fin one, so has been chosen a very rapid annealing (0.05 ms) with a temperature of 1050 °C in order to keep the dopants in the source and drain regions; the implantation is localized by using a photoresist to cover the other parts of the device. The final doping is represented in figure 8.4

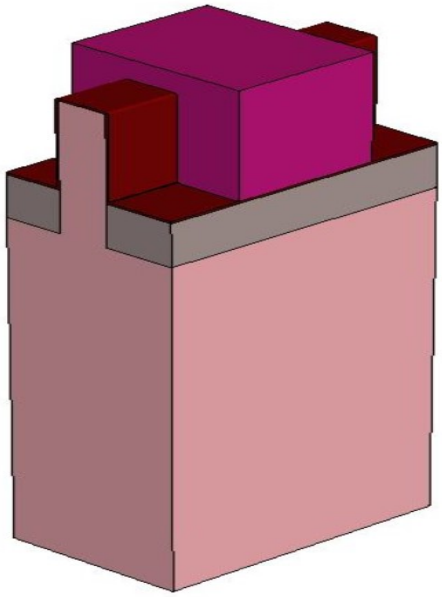
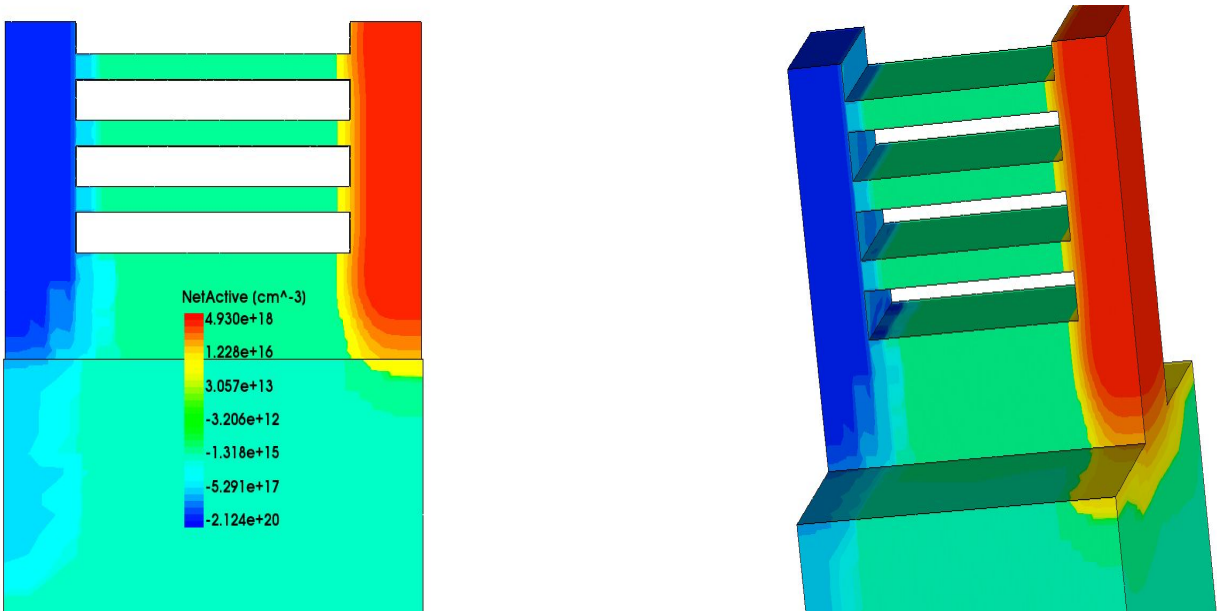


Figure 8.3: Dummy gate fabrication



(a) doping

(b) doping "spikes"

Figure 8.4: Overview on doping of GAAFET

After that, the oxide is removed everywhere and it is deposited only at the right and left sides of the dummy gate, as happens for the nitride that acts as spacer to better

isolate the contacts; TiSilicide is obtained above the source and drain regions and then PSG is deposited to protect them for the dummy gate etching. It is removed with also the oxide and the silicon germanium, leaving the necessary space for the gate stack fabrication (figure 8.5). This is realised with three isotropic depositions:

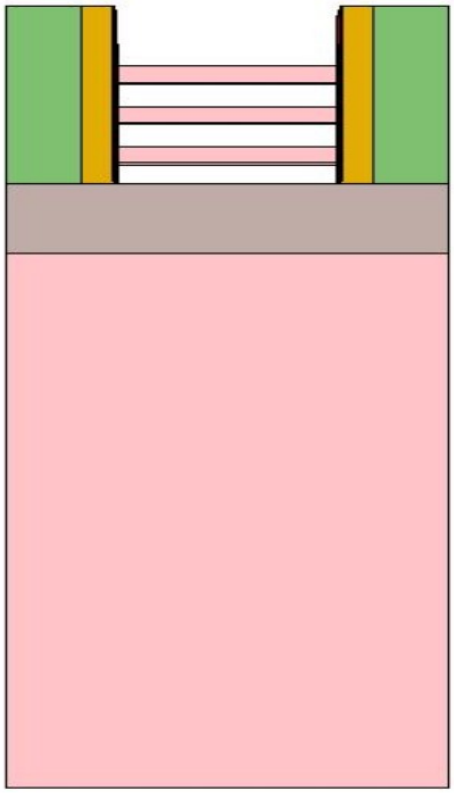


Figure 8.5: Nanosheet

oxide, hafnium and aluminum. After them, the remaining empty space is filled by Tungsten, that acts as a contact, and with a layer of nitride, that garantees a better isolation for the contacts. Finally also the drain and source contacts are realised: through masks PSG is etched and tungsten is deposited; the final structure is 8.6

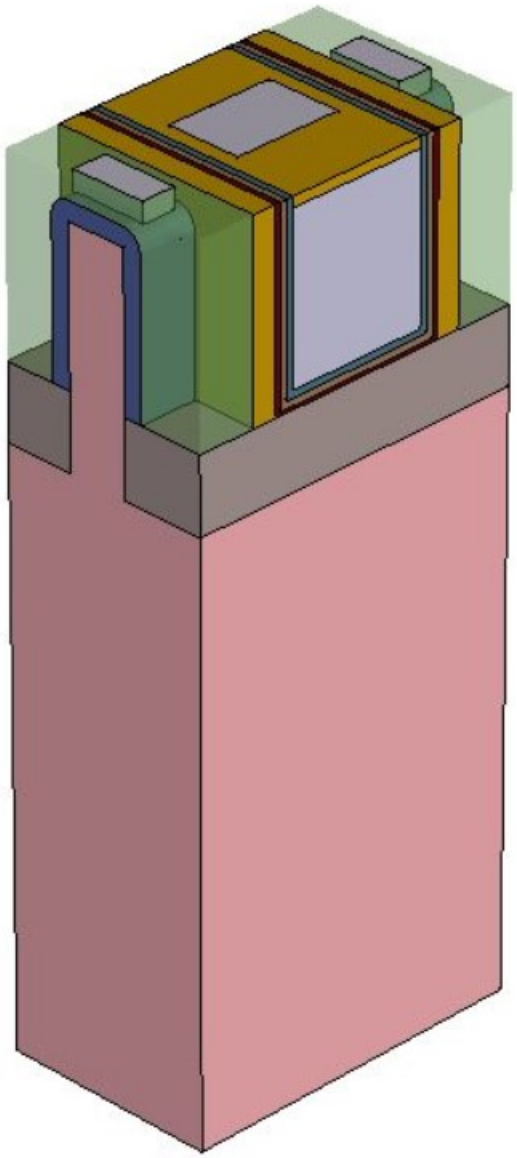


Figure 8.6: NSGAAFET final structure

Chapter 9

Electrical simulations

As for the case of the Fin-TFET device, due to the definition of the structure in sentaurus, the band diagrams are inverted on the abscissa. At the equilibrium condition the band diagram is (9.1).

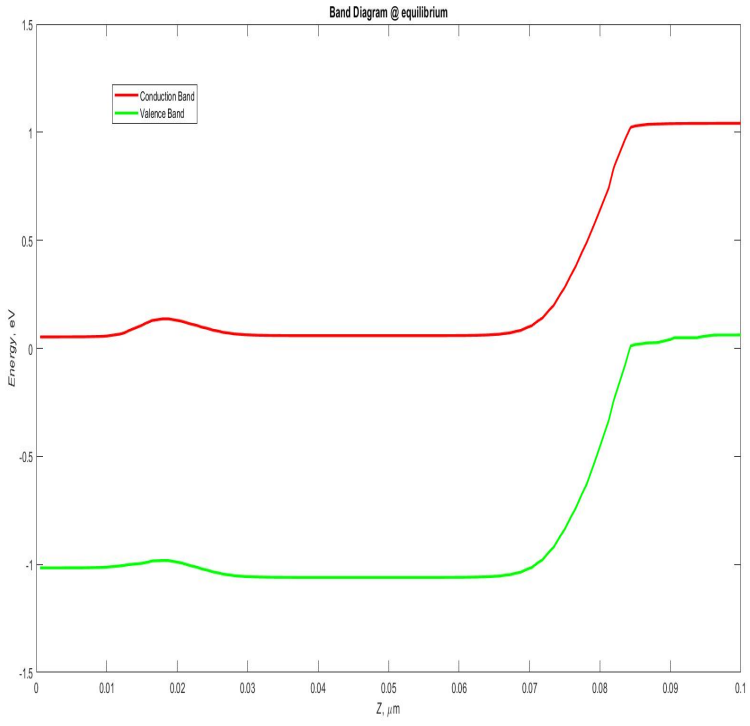


Figure 9.1: Band diagram at equilibrium of GAAFET

Applying the reference voltages (V_{GS} = 1V and V_{DS} = 1V) it becomes (9.2) and the consequent transcharacteristic is (9.3). The band diagrams are similar to the Fin device, so also in this case an "hump" is present between the channel and the drain (with its implications); small variations can be appreciated, but considering a more complex structure is difficult to obtain an identical doping profile. This variation in the doping profile is due to a different doping diffusion near the edges of the structure (like the one present near the nanosheets) and, as you will see, this lead to different discrepancies between the two structures and to different parameter dependence of the NSGAA-TFET with respect to the Fin-TFET.
For what concern the current, in this case we have three conductive channels, so to compute the current per unit length a slightly different formula is employed (9.1) [20]. The resulting values for the I_{ON} and I_{OFF} currents are respectively about 9.5 nA/μm and 0.5 pA/μm, so both of them are higher with respect to the Fin-TFET.

$$I_{DS,0} = \frac{I_{DS}}{2H_{NS} + W_{NS}} * 3. \tag{9.1}$$

It is important to underline that the complexity in the doping in not only a minor

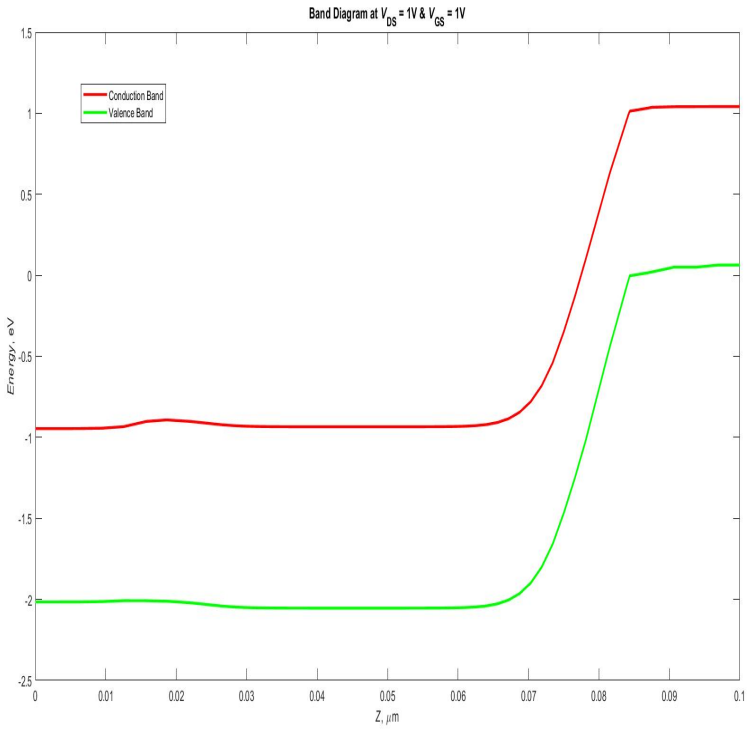


Figure 9.2: Band diagram of GAAFET at V_{DS} = 1V and V_{GS} = 1V

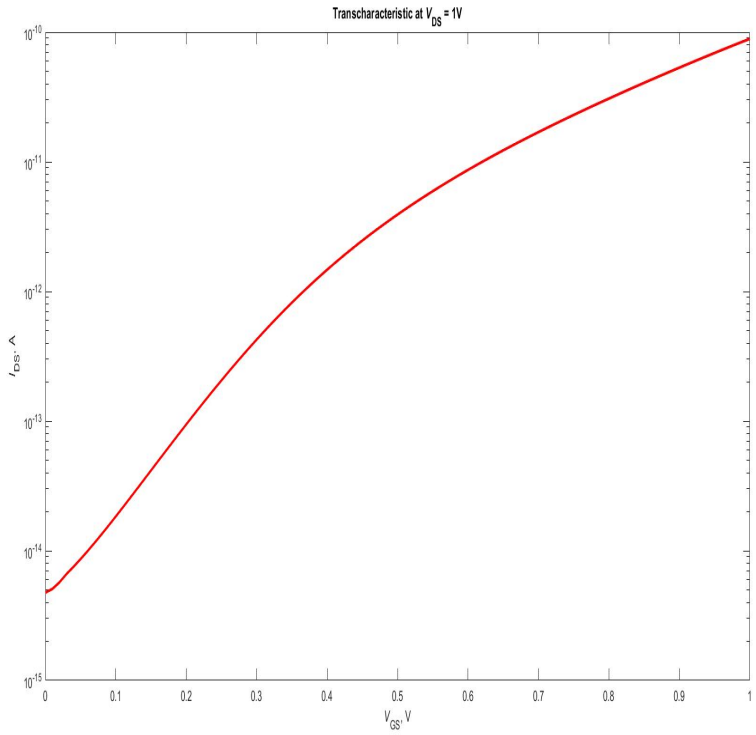


Figure 9.3: $I_{DS}(V_{GS})$ at $V_{DS} = 1V$

issue, but determines most of the detrimental effects affecting the device. In fact a non optimized doping method for this kind of structures, considering also the 2 different impurities employed (Boron and Phosphorus), leads to rough doping profiles and to the formation of doping "spikes" near the edges of the structure due to different diffusion properties. These "spikes" strongly affect the conduction through the nanosheets increasing the I_{OFF} exponentially. The solution reported in 8.4 is obtained exploiting a large tilt angle in the doping process ($\simeq 60°$) and a very fast thermal annealing in order to "contain" the diffusion of the Boron that tends to accumulate near the edges.

9.1 Transcharacteristic: V_{DS} dependance

The figure obtained agrees with what we expected from a theoretical point of view [20][21]. In fact the I_{ON} doesn't change with V_{DS} (it is clamped) while the I_{OFF} increases with the increasing voltage, showing a strong ambipolarity. As happens for the FinFET (same reasons), this effect is strongly detrimental already at 2 volts (look figure 9.4) and so the operation condition is $V_{DS} = 1V$.

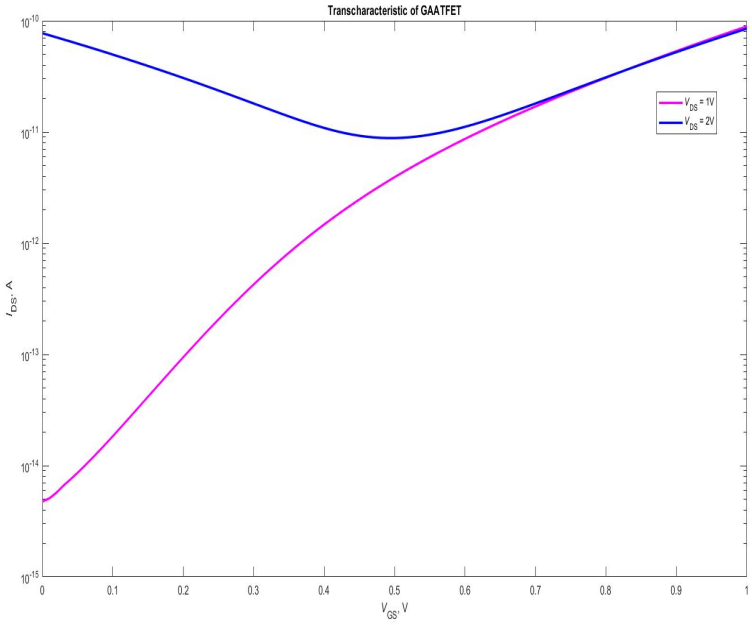


Figure 9.4: $I_{DS}(V_{GS})$ comparison for $V_{DS} = 1V$ and 2V

9.2 Output characteristic: V_{GS} dependance

For what concern the output characteristic, looking at figure 9.5, we have the same strange behavior already seen in FINTFET, but in this case it is even worse from the moment that there seems to be a double threshold. What we think is that, together with the problems depicted in the previous case, this is due to the presence of a parasitic channel, below the nanosheets, that turns on in a different moment with respect to the them.

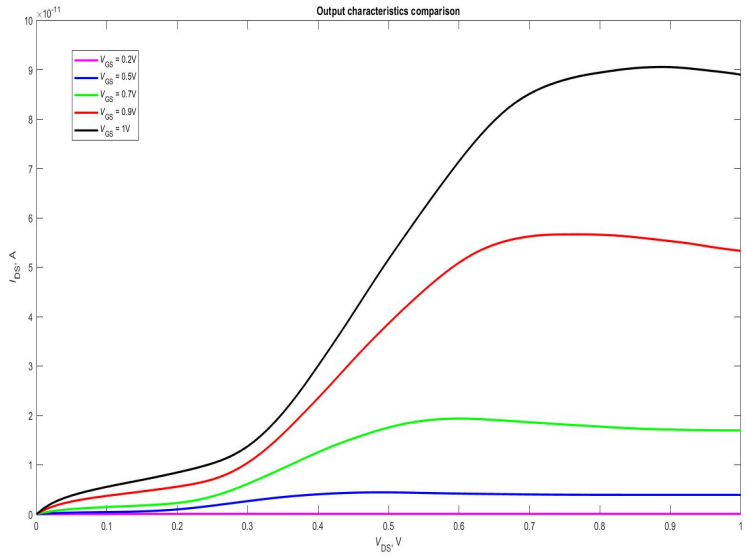
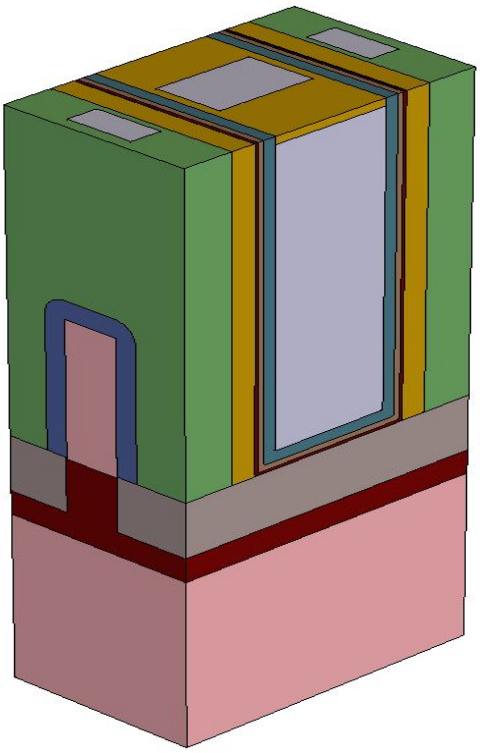


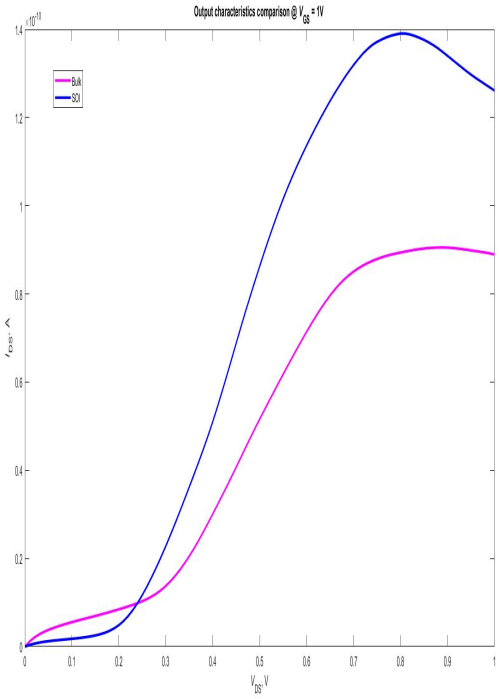
Figure 9.5: $I_{DS}(V_{DS})$ comparison for different V_{GS}

To confirm this theory we have modified the NSGAATFET by implementing a SOI solution (figure 9.6a); in this way a possible parasitic channel should disappear and a single threshold should remain in the output characteristic.

As we can see from figure 9.6b the expectations appear satisfied and only one threshold can be recognised in the SOI case. Consider that the SOI structure is not optimized (random doping and geometrical parameters) so we restrict its validity only to confirm our hypothesis.



(a) SOI NSGAATFET structure



(b) SOI vs Standard NSGAA output comparison

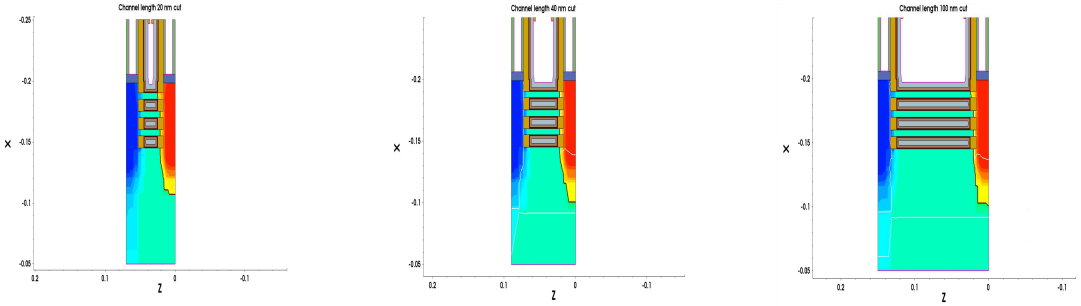
Chapter 10

Parameters dependence

In this chapter will be evaluated the impact of the different physical parameters involved in the TGAAFET device. In particular, starting from the standard structure, the parameters are modified one by one keeping the rest unchanged and an evaluation of the effects is performed looking at the new transcharacteristics; every time that a new variable is modified, the previous one is restored to the standard value. All the transcharacteristics are computed at fixed $V_{DS} = 1V$ and V_{GS} between 0 and 1V in order to compare each other. If relevant also the band diagrams are shown otherwise refer to figure 9.1

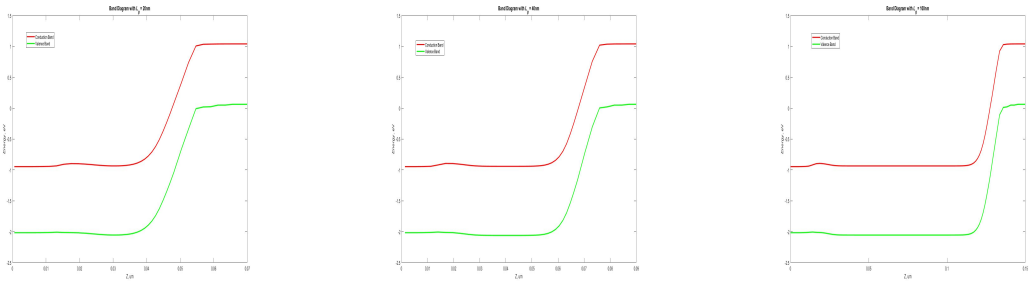
10.1 Channel length

The first parameter that is treated is the channel length. Clearly it has a huge impact on the current and, in particular, the values investigated are the same of the FinFET case (20, 40, 50 (reference value) and 100 nm). The modifications of the device, expect for the standard value, are represented in figure 10.1 and the corresponding band diagrams are in the figure 10.2.



(a) $L_g = 20$ nm (b) $L_g = 40$ nm (c) $L_g = 100$ nm

Figure 10.1: Channel length impact on the device



(a) L_g = 20 nm (b) L_g = 40 nm (c) L_g = 100 nm

Figure 10.2: Band diagram with different channel length

Looking at figure 10.3 it is possible to see that there is a more coherence than the FinFET case for the curves with higher channel length; this happens because the presence of the gate-all-around provides a stronger electrostatic control on the channel and so a better bending of it (fig 10.2). Also in this case for L_g = 20 nm the transcharacteristic deteriorates due to the fact that the two junctions are not more well defined (fig 10.2a). Obviously when the channel length is modified is difficult to obtain the same doping profile, so small variations are present between the curves and this explains why they start from slightly different values of I_{OFF} and they intersecate several times.

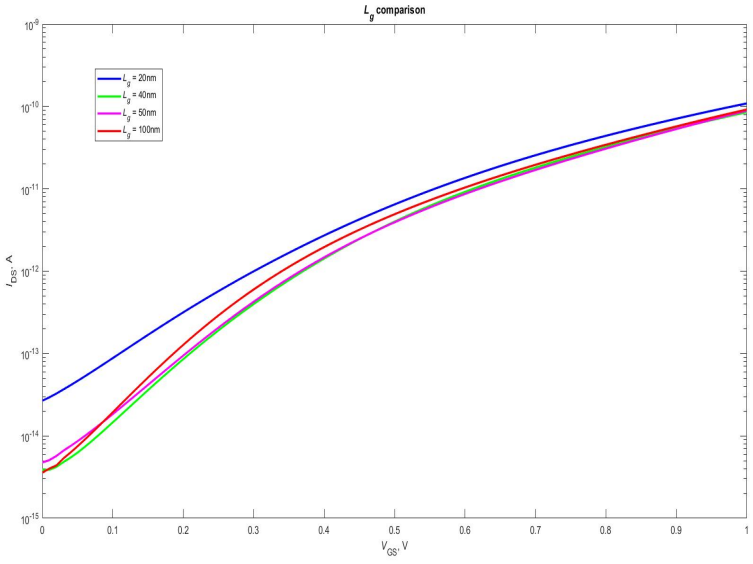
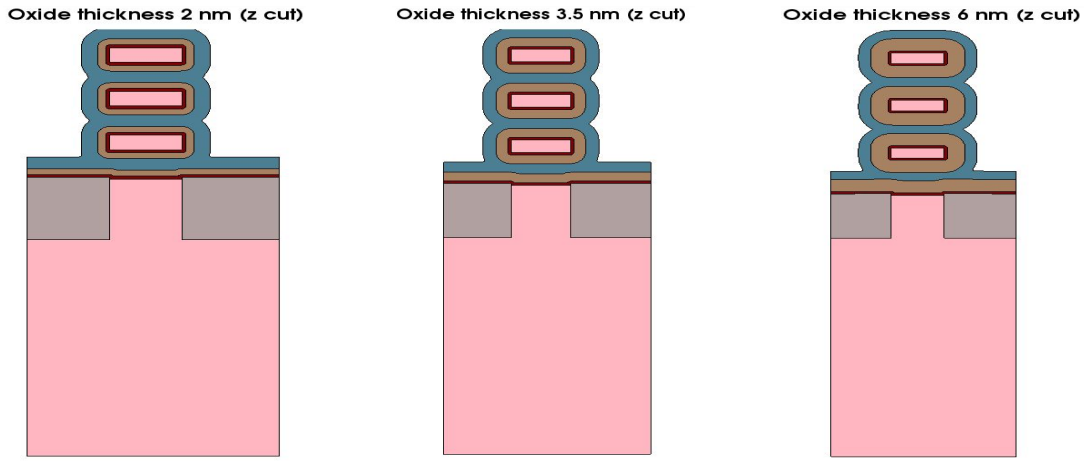


Figure 10.3: $I_{DS}(V_{GS})$ with different channel length of GAAFET

10.2 Oxide thickness

The second parameter that is analyzed is the the gate oxide layer thickness and how the device transcharacteristic changes by varying it. As before what changes is the thickness of the hafnium oxide while the silicon dioxide remains of 1 nm; Again the thicknesses chosen for the analysis are 2 nm (standard), 3.5 nm and 6 nm (fig 10.4). For what concern the band diagram in this case only the standard one is reported (fig 10.5) from the moment that there is no significant variation between them.



(a) 2 nm (b) 3.5 nm (c) 6 nm

Figure 10.4: Oxide thickness

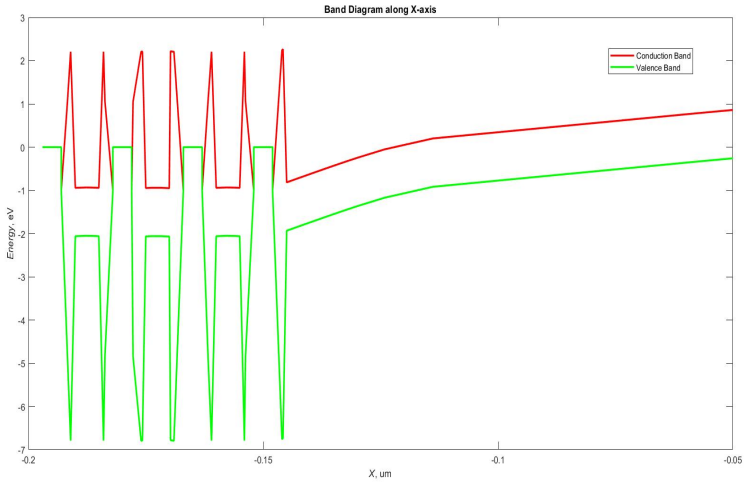


Figure 10.5: Band diagram of the standard GAAFET along X-axis

For what concern the transcharacteristic, in the TGAAFET case we have a very interesting behaviour: in fact even if, similarly to the FinFET case, increasing the oxide thickness there is a lowering of I_{ON} and I_{OFF}, this shift is no more rigid so, as you can see from figure 10.6, in this case the choice of a thicker layer is preferable. In fact from the point of view of I_{ON}/I_{OFF} ratio for 6 nm thick oxide this value is almost 6 orders of magnitude while for the standard one (2 nm) is 4; also in this case we have chosen 2 nm to obtain the greater I_{ON}, but it is important to underline that, overcoming the low-I_{ON} current problem of TFETs, the best choice for device characteristics should be 6 nm.

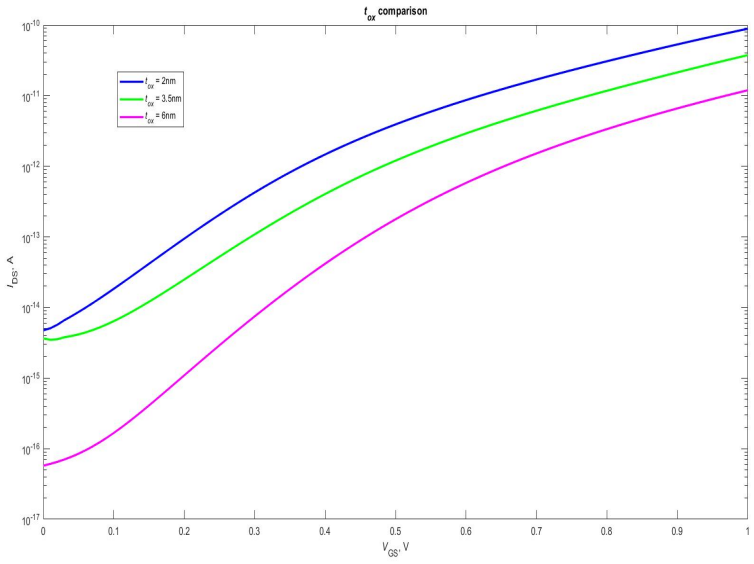


Figure 10.6: $I_{DS}(V_{GS})$ with different thickness oxide of GAAFET

10.3 Metal workfunction

Also in this case the metal workfunction impact on the device transcharacteristic is investigated; looking at figure 10.7 no important variations seem to appear with respect to the FinFET case, except for a higher "ambipolarity resistance" of the device (look at the curves representing WF = 4.26 eV in fig 7.7 and fig 10.7). So the best choice for the NSGAATFET remains the Aluminum with its amorphous configuration (WF $\simeq$ 4.1 eV).

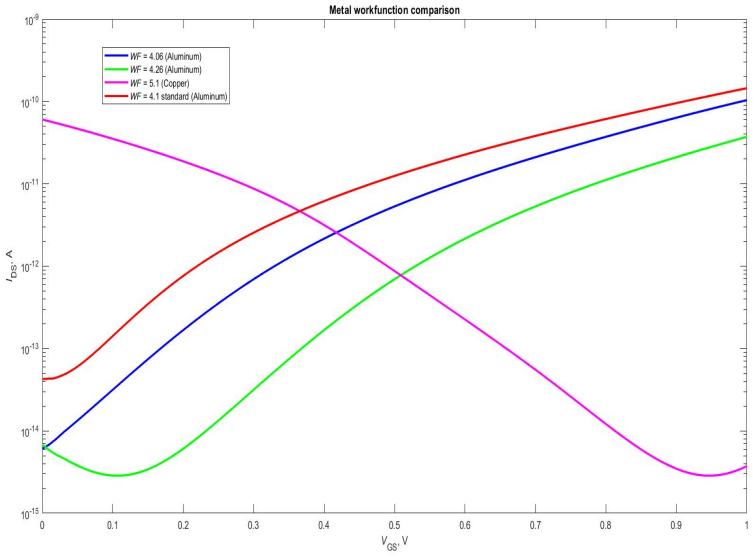


Figure 10.7: $I_{DS}(V_{GS})$ with different metal gate

10.4 Channel doping

As before a proper value for the channel doping must be chosen in order to promote the tunneling between source and the channel. In the NSGAATFET case the doping cannot be defined through the wafer doping, but from the moment that the structure is created over it, the channel doping must be defined through an implantation and annealing steps; as consequence the doping values are not precised and slightly change depending by the position and the nanosheet. For the standard structure an optimal channel p-doping of $10^{15}cm^3$ has been chosen; this is in accordance with the theoretical device [20] and allows a correct functioning. Looking at figure 10.9 can be seen that using different values for the channel doping the transcharacteristic tends to remain unaltered, so an higher "ambipolarity resistance" of the GAAFET

seems to be confirmed from the moment that, in the FinFET case (fig 7.8) for doping value of about 10^{16} ambipolarity starts to appear.

(a) 10^{14} (b) 10^{16}

Figure 10.8

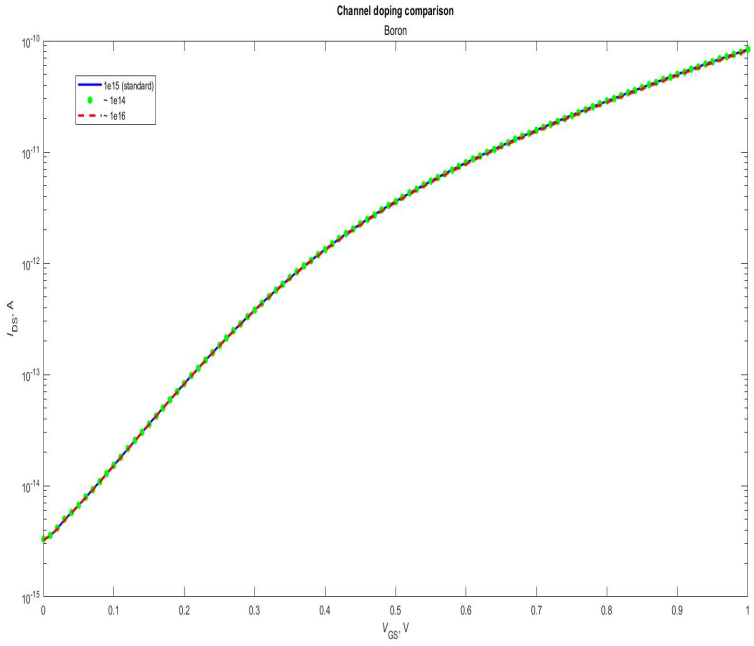
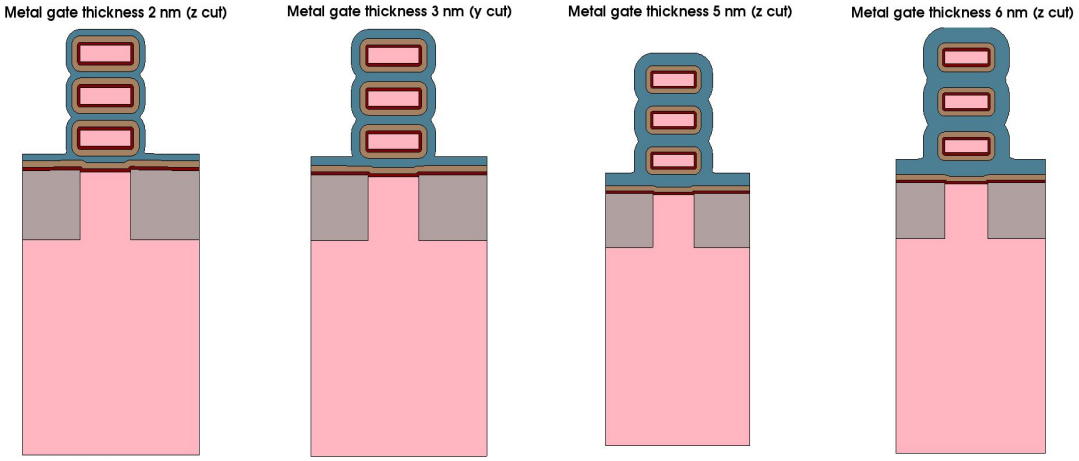


Figure 10.9: $I_{DS}(V_{GS})$ with different values of channel doping

10.5 Metal gate thickness

In this chapter we analyze the effect of the metal gate thickness on the transcharacteristic. The standard value chosen is 4 nm and, as we can see from figure 10.11, the structure has been optimized for a thickness of 4 nm. In fact, going to increase or decrease this value without changing anything else, causes a deterioration of the current and, in particular, of the off-value (ambipolarity amplification). Always looking at figure 10.11 is possible to see that, getting away from the standard value, the curve get worse: for 2 nm is worse than 3 nm and 6 nm is worse than 5 nm.



(a) 2 nm (b) 3 nm (c) 5 nm (d) 6 nm

Figure 10.10: y-cut of GAAFET with different metal gate thickness

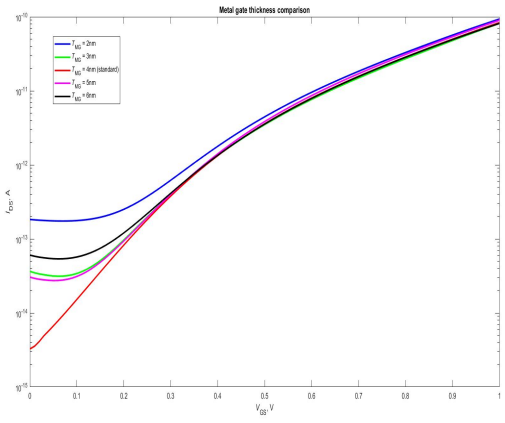


Figure 10.11: $I_{DS}(V_{GS})$ comparison with different metal gate thickness

10.6 Conclusions on NSGAATFET

Considering the results obtained, the NSGAATFET structure provides some advantages with respect to the previous devices; also in this structure some problems, strictly related to the geometrical complexity , appear and in particular, as stated before, the doping implantation and diffusion become even more difficult to perform. In fact, looking at figure 8.4b, there is an accumulation of the doping near the edges of the structure (source-channel interface) that creates "doping spikes", influencing the electrical behavior.
Moreover, differently from the previous devices, other parameters that were irrelevant, now play an important role, not only from a physical point of view, but also from a practical one; significant is the metal gate thickness, because not only modifying it the entire structure geometry changes, but, from the moment that the device exploits a GAA technology, it influences also the electrostatic control on the nanosheets.
As a consequence all these issues imply worsen figures of merit with respect to the expected ones, but they remain still acceptable if compared with the ones found in literature ([8][12][16][20][21]).
In conclusion, even if this simulated device doesn't provide coherent or better performances with respect to the state-of-the-art, can be used to analyze the influence of the different parameters on the device figures of merit; this can be useful for the design of different TFET structures (heterostructure TFET,vertical TFET,SAA TFET,etc) and their implementation.
Considering the channel length, in this case we have a better scaling of the device, in fact, even if we have chosen 50 nm as standard length (to make comparison with the previous TFET devices), for a length of 40 nm the device preserves its behaviour (fig 10.1b) and it is preferable from a technological point of view. However also in this case for 20 nm channel length the behavior degenerates and it is no more a good choice. For what concern the oxide thickness the same trend shown by the FinTFET is present, but in this case is more interesting: in fact, as seen in figure 10.6, there is no more a rigid shift, so for different implementations of this device, thicker oxide should be the best choice, of course providing a lower I_{ON}, but much more lower I_{OFF}. You must take into account that, modifying the oxide thickness, also the spacing between the nanosheets changes causing variations in the geometry of the structure, so all other parameters must be changed accordingly otherwise some unexpected variations can occour. For the choice of the metal gate, the results are the same of the FinTFET (except for a higher "ambipolarity resistance" of the device), so Aluminum (in particular its amorphous configuration) seems to be the best choice. So still remain the workfunction "ambipolarity shift" trend; lower WF provides a left-shift of the ambipolarity, but of course also an increasing of the I_{OFF}, on the contrary with higher WF the opposite happens. The channel doping in this case has a negligible effect on the figures of merit, considering reasonable values (from 10^{14} to 10^{16}) and working on this parameter won't provide any improvement. Finally, for what concern the metal gate thickness, we find a very strong influence

of this parameter on the electrical behavior of the device; in particular seems to be a small range of values that allow the best performances for the device. From the experience acquired by our simulations, we suggest two possible procedures for the optimization of the structure: the first consists in defining all the physical and geometrical parameters a priori and then you go to tune the metal gate thickness in order to optimize the behavior of the electrical simulation; the second method (the one chosen by us) starts by firstly defining the geometrical parameters, after the metal gate thickness (accordingly to the technology node that you want to realize) and then look for the optimization, especially through the doping concentration and profile.

Part IV

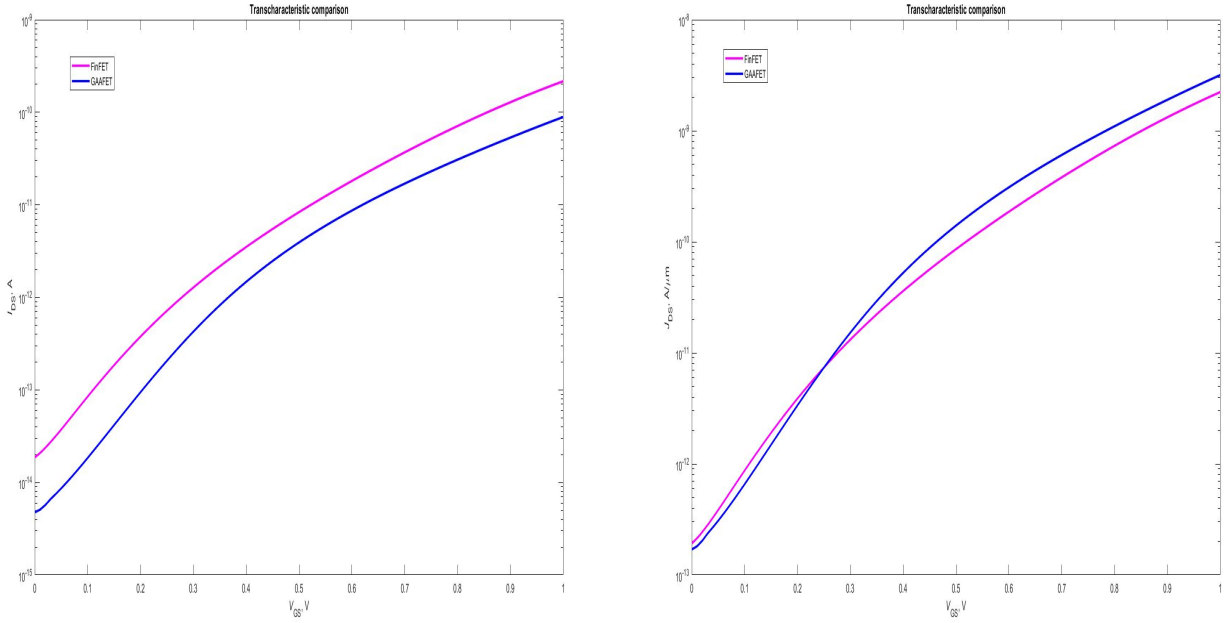
Final conclusions

In this last part of the thesis we want to discuss some comparisons in order to better understand the behavior of our devices; in particular we have chosen to provide comparisons between our 2 devices, analysing advantages and drawbacks of different technologies employed resuming, through images and tables, their figures of merit.

Finally we remark the main results obtained in our study, how they can be used to design alternative structures based on tunneling effect and we suggest some possible implementations that could improve the performances of our structures, overcoming the main limitations.

10.7 TFET technology comparison

First of all we're going to compare the transcharacteristics of our FIN- and NSGAA-FET devices in order to better understand how they behaves respectively. In particular, we report the current and the current density (related to the channels dimensions) of the devices, considering the same biasing.



(a) Current comparison FIN- vs NSGAA-

(b) Current density comparison FIN- vs NSGAA-

Figure 10.12: TFET technology comparison: FinFET vs NSGAAFET

As we can see, from figure 10.12a, the two devices seems to behave quite linearly, in the sense that they maintain approximately the same I_{ON}/I_{OFF} ratio, but looking at figure 10.12b we can observe that the NSGAAFET overcomes the FINFET performances with a lower J_{OFF} and a greater J_{ON}. This reflects the behavior we expected from the devices, but the improvement is lower than the theoretical one ([2][10][20][21]); however there are all the reasons to choose the second device instead of the first. To look these results from a numerical point of view you can refere to tables 10.1 and 10.2.

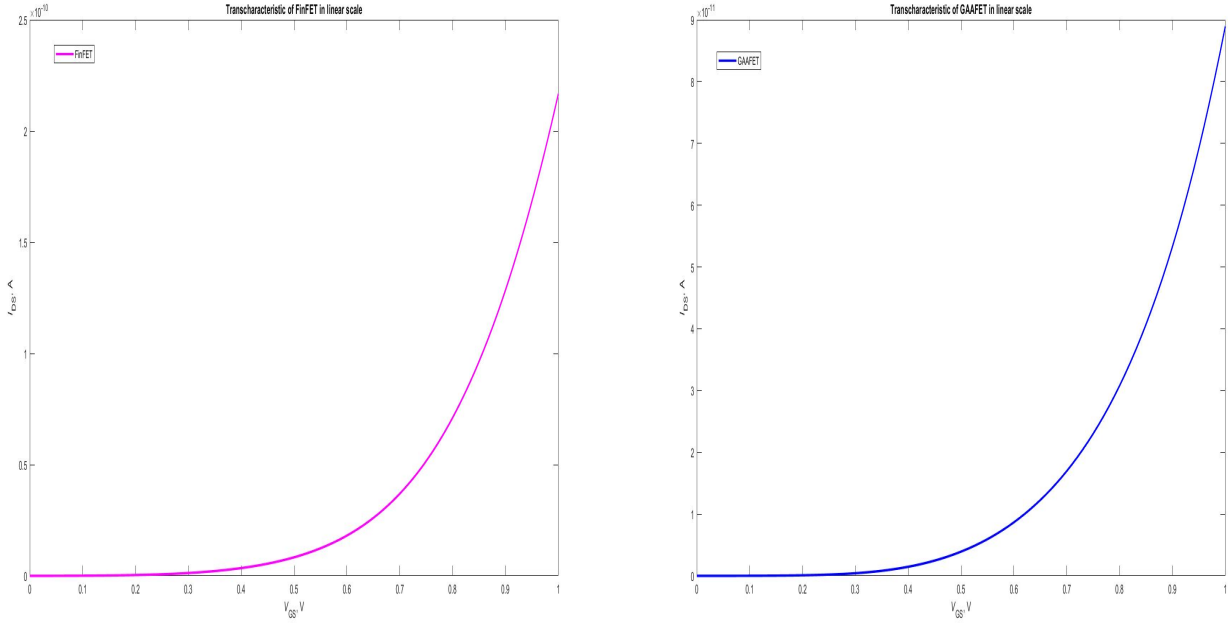
Figures of merit	FinTFET	NSGAATFET
I_{ON}	$2.1671*10^{-10}$ A	$8.8955*10^{-11}$ A
I_{OFF}	$1.8657*10^{-14}$ A	$4.7550*10^{-15}$ A
I_{ON}/I_{OFF}	$1.1615*10^{4}$	$1.8708*10^{4}$
V_{TH}	$\simeq$ 0.3V	$\simeq$ 0.3V
SS	$\simeq$144 mV/dec	$\simeq$148 mV/dec

Table 10.1: Figures of merit comparison between FinTFET and NSGAATFET

Figures of merit	FinTFET	NSGAATFET
J_{ON}	$2.2341*10^{-9}$ A/μm	$3.1769*10^{-9}$ A/μm
J_{OFF}	$1.9234*10^{-13}$ A/μm	$1.6982*10^{-13}$ A/μm

Table 10.2: Current density comparison between FinTFET and NSGAATFET

For what concern the threshold voltage we used the equation 1.5 and, as can be confirmed by looking figure 10.13, we obtained $\simeq$0.3V for the FinTFET and $\simeq$0.3V for the NSGAATFET; these values are coherent with the theory ([20][21]) and in fact are considerably lower with respect to common MOSFET devices. Instead, to compute the Subthreshold Swing, considering that these kind of devices (Tunnel FETs) are not linear in off condition, we applied equation 1.4 only in a restricted linear segment of the curves near the off state (low V_{GS}); in this way we have obtained $\simeq$144 mV/dec for the FinTFET and $\simeq$148 mV/dec for the NSGAATFET. These values are far away from the expected ones and in particular they are much slower than the ideal devices; In fact even if our devices seem to turn on quite rapidly (small threshold voltage) they require high voltages to reach considerable current values.



(a) FinFET (b) GAAFET

Figure 10.13: Linear transcharacteristic

In conclusion not all the merits of the TFET are achieved, but this was predictable since our devices have shown some issues like in the not ideal doping profile and so the band diagram behavior; in fact one of the main limitations is that, due to this aspect, we're not able to reduce the channel length over a certain value, where TFET would show better performances.

10.8 Actual results and next steps

To conclude the discussion we want to remark the main achievements reached during the study of these devices; in particular we discovered promising current values for both I_{ON} and I_{OFF}, even if they require a further improvement to become competitive, and interesting threshold voltages for all the devices, coherent with the expected theoretical ones. Moreover, during the design of the devices through TCAD Sentaurus tools, we have employed not only real fabrication processes, but also the same generally used during the fabrication of standard MOSFETs; this quality, combined with the choice of designing bulk-structures, make this kind of devices attractive for prototype testing from the moment that, not only the same machinery used for actual production can be employed, but also that the costs of the development should be low.
Another important result of this thesis is the dependence on the physical and structural parameters that we have discovered during our analysis; in fact, these dependencies should remain valid also for different technologies and geometries, and could provide a useful tool to refine, or tune, different TFET devices.
In the end, we reserve the right to suggest the implementations that we believe have the most impact on performance: the first, and probably the most impacting one, is to pass from a full-silicon structure to a heterostructure, exploiting materials with engineered bandgap, in order to maximize not only the tunneling current, but also the speed (subthreshold swing); in fact, as we have seen during this study (look at band diagrams in sections 6 and 9), one of the main problems of our devices is that the different regions (source, channel and drain) do not show a net variation in terms of bandgap and this affect the speed of the device in a consistent way.
The second implementation that provides a great improvement on the device performance, as seen in the section 9.2, is to create these kind of structure on a SOI wafer; in fact from the analysis of the output characteristic (fig. 9.6b) we have seen how the generation of a parasitic channel below the main one tends to create a double threshold and to increase the off current.
Another important change that will improve considerably the behavior of the TFET is to reduce the channel length; for what concern our devices (bulk and full silicon) we run into several problems about the doping profile and the Band diagram bending near the electrodes causing the impossibility to go below 40-50 nm [16]. From the moment that, the tunneling is closely dependent by the distance traveled and that, for very short channels, the conduction become ballistic, TFET technology would greatly benefit of this improvement, but in order obtain shorter devices a finer doping technique and the employment of heterostructure may be necessary.
Finally there are other implementations that can impact on the performance of the TFETs in a positive way, that must be investigated regardless of the type of device being designed, such as the choice of the metal gate deciding to use a proper metal alloy, the application of a better doping technique able to define precise regions, the choice of a different gate oxide material in order to limit the gate-channel tunneling leakage current and increase the control over the channel at the same time (obviously

it must be taken into account the process compatibility) and then another possibility is to move toward different geometries. Looking in literature there are several other options able to increase the performance of TFET technology like SAA-TFET (Source All Around TFET), pocket-doping, Vertical TFET and so on, but these possibilities are more complex to realise.
To conclude the discussion, we think that this technology is not only interesting under several point of view, but it is also very promising for the theoretical advantages in part confirmed in this study, where the analyzed devices where realized employing materials commonly used for standard MOSFETs like silicon and aluminum, so not the best choices, but still valid.

Appendix A

Planar Sprocess

```
# 2D nTFET bulk
math coord.ucs
# Declare initial grid (half structure)

line x location= 0.0 spacing= 5.0<nm> tag= SiTop
line x location= 60.0<nm> spacing= 10.0<nm> tag= SiBottom
line y location= 0.0 spacing= 25.0<nm> tag= Left
line y location= 90<nm> spacing=25.0<nm> tag= Right

# Silicon substrate definition
region Silicon xlo= SiTop xhi= SiBottom ylo= Left yhi= Right

# Initialize the simulation
init concentration=1e15<cm-3> field= Boron !DelayFullD
AdvancedCalibration
struct tdr=n@node@_NMOS_substrate0; #substrate
grid set.min.normal.size= 1<nm> set.normal.growth.ratio.2d= 1.5
mgoals accuracy= 1e-5

pdbSet Oxide Grid perp.add.dist 1e-7

# Gate oxidation

mask name= oxide_neg left=20<nm> right= 70<nm> negative
deposit material= {Oxide} type= anisotropic time= 1 rate= {0.001} mask= ox-
ide_neg
deposit material= {HfO2} type= anisotropic time= 1 rate= {0.002} mask= ox-
ide_neg
```

Poly gate deposition

deposit material= {PolySilicon} type= anisotropic time= 1 rate= {0.010} mask= oxide_neg

struct tdr= n@node@_MOS;

Poly reoxidation

deposit material= {Oxide} type= isotropic time= 1 rate= {0.001}
struct tdr= n@node@_Poly_oxidation ; # Poly Reox

Nitride spacer

deposit material= {Nitride} type= isotropic time= 1 rate= {0.006}
struct tdr= n@node@_Spacer_init ; Spacer deposition
etch material= {Nitride} type= anisotropic time = 1 rate= {0.0084} isotropic.overetch= 0.01
struct tdr= n@node@_Spacer_final ; Spacer etch

etch material= {Oxide} type= anisotropic time= 1 rate= {0.001}
struct tdr= n@node@_Oxidation_removal ; # Spacer oxide removal

Source

refinebox Silicon min= {0.018 0.0} max= {0.0 0.024} xrefine= {0.001 0.001 0.001} yrefine= {0.001 0.001 0.001} add
grid remesh

mask name= source_neg left= 0<nm> right= 7.5<nm>
photo thickness= 0.2<μm> mask= source_neg

implant Boron dose= 5e17<cm-2> energy= 0.01<keV> tilt= 7<degree> rotation= -90
struct tdr= n@node@_LDDS ; # LDD Implant

strip Photoresist
Drain

refinebox Silicon min= {0.0 0.066} max= {0.018 0.090} xrefine= {0.001 0.001 0.001} yrefine= {0.001 0.001 0.001} add
grid remesh

mask name= drain_neg left= 70<nm> right= 90<nm>

photo thickness= 0.2<μm> mask= drain_neg

implant Arsenic dose= 0.8e12<cm-2> energy= 0.1<keV> tilt= 7<degree> rotation= 90
implant Arsenic dose= 0.8e12<cm-2> energy= 0.5<keV> tilt= 7<degree> rotation= 90
implant Arsenic dose= 0.8e12<cm-2> energy= 1.0<keV> tilt= 7<degree> rotation= 90

struct tdr= n@node@_LDDD ; # LDD Implant
strip Photoresist

diffuse temperature= 1050<C> time= 0.001<s> ; # Quick activation

struct tdr= n@node@_LDD_diffusion ; # LDD Diffuse
etch material= {PolySilicon} type= anisotropic time= 1 rate= {0.010}
deposit material= {Aluminum} type= anisotropic time= 1 rate= {0.010} mask= oxide_neg
etch material= {Aluminum} type= cmp coord= -0.013
etch material= {Oxide} type= cmp coord= -0.013
refinebox Silicon min= {0.0 0.019} max= {0.005 0.071} xrefine= {0.001 0.001 0.001} yrefine= {0.001 0.001 0.001} add
grid remesh

Contacts creation

mask name= contacts left= 8<nm> right= 82<nm>
deposit material= {Copper} type= anisotropic time= 1 rate= {0.005} mask= contacts

struct tdr= n@node@_S_D_contacts ; # Aluminium etching 1

mask name= contact_gate left= 32.5<nm> right= 57.5<nm> negative
deposit material= {Copper} type= anisotropic time= 1 rate= {0.005} mask= oxide_neg

struct tdr= n@node@_Gate_contact ; # Gate contact creation

Mesh
refinebox clear
refinebox Silicon min= {-0.001 0.0} max= {0.02 0.091} xrefine= {0.0005 0.0005 0.0005} yrefine= {0.0005 0.0005 0.0005} add
grid remesh

```
refinebox Oxide min= {0.001 0.018} max= {-0.014 0.071} xrefine= {0.001 0.001 0.001}  yrefine= {0.001 0.001 0.001} add
grid remesh

refinebox Aluminum min= {0.001 0.018} max= {-0.014 0.071} xrefine= {0.001 0.001 0.001}  yrefine= {0.001 0.001 0.001} add
grid remesh
refinebox HfO2 min= {0.001 0.018} max= {-0.014 0.071} xrefine= {0.001 0.001 0.001}  yrefine= {0.001 0.001 0.001} add
grid remesh

# save final structure:
# - 1D cross sections
SetPlxList {BTotal NetActive}
WritePlx n@node@_NMOS_channel.plx y=0.07 Silicon
SetPlxList {AsTotal BTotal NetActive}
WritePlx n@node@_NMOS_ldd.plx y=0.006 Silicon
SetPlxList {AsTotal BTotal NetActive}
WritePlx n@node@_NMOS_sd.plx y=0.08 Silicon

# Contacts
contact bottom name = bulk Silicon
contact name = gate x = -0.016 y = 0.04 Copper
contact name = source x = -0.0026 y = 0.002 Copper
contact name = drain x = -0.0026 y = 0.088 Copper

struct tdr= n@node@_presimulationnew

exit
```

Appendix B

FinTFET Sprocess

The work is divided in 8 sprocess in order to reduce the computational cost.

```
math coord.ucs
math numThreads=4
AdvancedCalibration 2017.09
pdbSet Mechanics StressRelaxFactor 1
# Solver Enhancement
pdbSet Math diffuse 3D ILS.hpc.mode 4
pdbSet Mechanics EtchDepoRelax 0
# meshing parameters
mgoals resolution= 1.0/3.0 accuracy= 1e-5
pdbSet Grid SnMesh max.box.angle.3d 175
grid set.min.normal.size= 0.005/1.0
set.normal.growth.ratio.3d= 2.0
set.min.edge= 1e-7 set.max.points= 1000000
set.max.neighbor.ratio= 1e6

# Structure parameters, [um]
define D [expr (@Lg@+0.05)]
define HalfD [expr ($D*0.5)]
define H 0.06 ;# Fin exposure
define STI 0.02 ;# STI
define Hfin [expr ($H - $STI)] ; Fin height
define HalfLg [expr (@Lg@*0.5)] ;# Half gate length
define Tox 0.002 ;# Total thickness of gate insulator
define LSpacer 0.008 ;# Length Spacer
#thickness of gate insulator
define Tiox 0.0007 ;#Gate interlayer oxide thickness
define Tihfo2 0.001 ;#Gate high-k
#RMG (metal stack)
```

```
define TiN1 0.0015 ;# First layer TiN
define TaN2 0.0020 ;# Second layer TaN
define TiN3 0.0050 ;# Third layer TiN
define TiAl4 0.0050 ;# Fourth layer TiAl
# Doping parameters, [/cm3]
define Nsub 1e15 ;#Substrate doping (1.6e15)
define Nepi 5.0e17 ;#channel doping
define Nsd 5.0e12 ;#SD doping [/cm2]
define Next 5.0e12 ;#S/D extension doping [/cm2]
define Nstop 1.0e13 ;#channel stop doping [/cm2]

line x location= -70.0<nm> spacing=10.0<nm> tag= SiTop
line x location= 20.0<nm> spacing= 10.0<nm>
line x location= 50.0<nm> spacing= 20.0<nm> tag= SiBottom

line y location= 0.0 spacing= 50.0<nm> tag= Left
line y location= 0.062<um> spacing= 50.0<nm> tag= Right

line z location= 0.0 spacing= 50.0<nm> tag= Back
line z location= $D<um> spacing= 50.0<nm> tag= Front

#substrate
region Silicon xlo= SiTop xhi= SiBottom ylo= Left yhi= Right zlo= Back zhi=
Front substrate
init concentration=$Nsub<cm-3> field=Boron wafer.orient= {0 0 1} flat.orient= {1
1 0} !DelayFullD

refinebox name= nw min= {-0.12 0 0.0} max= {-0.05 0.11 0.1} xrefine= 5<nm>
yrefine= 10<nm> zrefine= 50<nm>
grid remesh
struct tdr= n@node@_nFinFET1
#–Epi layer with known doping concentration (well)
temp_ramp name= epi temperature= 750<C> time= 4.5<min> Epi epi.doping= {
Boron= $Nsub<cm-3> } epi.doping.final= { Boron= $Nsub<cm-3> } epi.model=
1 epi.thickness= $H
diffuse temp_ramp= epi
struct tdr= n@node@_nFinFET2
exit


init tdr= n1_nFinFET2
#Sidewall Image Transfer (SIT)
diffuse temperature= 900<C> time= 4.0<min> O2
deposit material= {Nitride} type= isotropic time= 1<min> rate= 0.0165
deposit material= {AmorphousSilicon} type= isotropic time= 1<min> rate= {0.0195}
```

```
struct tdr= n@node@_nFinFET3
mask name= fin left= 0<nm> right= 38<nm> back= -1 front= 0.17<um> negative
etch material= {AmorphousSilicon} type= anisotropic time= 1<min> rate= {0.04}
mask= fin
struct tdr= n@node@_nFinFET4
deposit material= {Oxide} type= isotropic time= 1 rate= {0.015}
etch material= {Oxide} type= anisotropic time= 1 rate= {0.015} isotropic.overetch=
0.1
struct tdr= n@node@_nFinFET5
etch material= {AmorphousSilicon} type= anisotropic time=1<min> rate= {0.3}
struct tdr= n@node@_nFinFETa
etch material= {Nitride} type=anisotropic time= 1<min> rate= {0.02}
struct tdr= n@node@_nFinFETb
etch material= {Oxide} type= anisotropic time=1 rate= {0.02} struct tdr= n@node@_nFinFETc
etch material= {Silicon} type=anisotropic time=1<min> rate= {$H} isotropic.overetch=
0.03
struct tdr= n@node@_nFinFETd
mater add name=TEOS new.like=oxide
deposit material= {TEOS} type= isotropic time= 1<min> rate= {($H+0.0165)}
struct tdr= n@node@_nFinFET7
etch material= {TEOS} type=cmp etchstop= {Nitride} etchstop.overetch=0.01
struct tdr= n@node@_nFinFET8 ;# TEOS CMP
etch material= {TEOS} type=isotropic time=1 rate= {(0.0165+0.003+$Hfin)}
etch material= {Nitride} type=anisotropic time=1 rate= 0.02
etch material= {Oxide} type= anisotropic time=1<min> rate= {0.01}
struct tdr= n@node@_nFinFET9
#Fin rounding etch material= {Silicon} type= isotropic rate= {0.004} time= 1.0
deposit material= {Silicon} type= isotropic rate= {0.004} time= 1.0 selective.materials=
{Silicon}
struct tdr= n@node@_nFinFET10 ;# Fin rounding
exit


init tdr= n3_nFinFET10
define Nstop 1.0e10 ;#channel stop doping [/cm2]
#Dummy gate
deposit material= Oxide type= isotropic time=1 rate= {$Tiox}
struct tdr= n@node@_nFinFET12a
deposit material= {Polysilicon} type= fill coord= -0.17
mask name= gate back= ($HalfD-$HalfLg)<um> front= ($HalfD+$HalfLg)<um>
etch material= {Polysilicon} type= anisotropic time=1 rate= {0.17} mask= gate
struct tdr= n@node@_nFinFET12b ;# Dummy Gate
exit
```

```
init tdr= n4_nFinFET12b
#S/D extension
refinebox name= sd min= {-0.13 0 0.0} max= {-0.04 0.062 $D} xrefine= 2<nm>
yrefine= 5<nm> zrefine= 2<nm>
grid remesh
#SOURCE DOPING
mask name= source_neg back= -1 front= ($D-0.015)<um> negative ;
photo thickness= 1<um> mask= source_neg
define Next 9e16
implant Boron dose= $Next<cm-2> energy=0.5<keV> tilt=45<degree> rotation=-
90<degree>
implant Boron dose= $Next<cm-2> energy=0.5<keV> tilt=-45<degree> rotation=-
90<degree>
struct tdr= n@node@_nFinFET13a ;# retrograde source doping
strip Photoresist
# DRAIN DOPING
mask name= drain_neg back= (0.013)<um> front= 1 negative ;
photo thickness= 1<um> mask= drain_neg
define Next 3e12
implant Phosphorus dose= $Next<cm-2> energy=1<keV> tilt=45<degree> rotation=-
90<degree>
implant Phosphorus dose= $Next<cm-2> energy=1<keV> tilt=-45<degree> rotation=-
90<degree>
implant Phosphorus dose= $Next<cm-2> energy=5<keV> tilt=45<degree> rotation=-
90<degree>
implant Phosphorus dose= $Next<cm-2> energy=5<keV> tilt=-45<degree> rotation=-
90<degree>
struct tdr= n@node@_nFinFET13b ;# retrograde drain doping
strip Photoresist
diffuse temperature=1050<C> time=0.0001<s>
struct tdr= n@node@_nFinFET14 ;# Final doping
exit


init tdr= n5_nFinFET14
etch material= {Oxide} type=anisotropic time=1 rate=1.0
deposit material= {Oxide} type= isotropic time=1<min> rate= {$Tiox} selec-
tive.materials= {PolySilicon}
struct tdr= n@node@_nFinFET15
etch material= {Oxide} type=cmp etchstop= {PolySilicon} etchstop.overetch=0.001
struct tdr= n@node@_pGAA16
deposit material= {Nitride} type= isotropic time=1<min> rate= {$LSpacer} se-
lective.materials= {Oxide}
struct tdr= n@node@_nFinFET17 ;# Spacer
etch material= {Nitride} type=cmp etchstop= {PolySilicon} etchstop.overetch=0.001
```

```
struct tdr= n@node@_nFinFET18 ;# Spacer
exit


init tdr= n6_nFinFET18
# Silicidation
deposit material= {TiSilicide} type= isotropic rate= 0.12*$Hfin time= 1.0 temper-
ature= 450 selective.materials= {Silicon}
struct tdr= n@node@_nFinFET20 ;# Silicidation
# Planarization PSG
mater add name= PSG
ambient name=Silane react add
reaction name= PSGreaction mat.l= Phosphorus mat.r= Oxide mat.new= PSG
new.like= Oxide ambient.name= {Silane} diffusing.species= {Silane}
deposit material= {PSG} type= isotropic time=1 rate= {0.2}
etch material= {PSG} type=cmp etchstop= {Nitride} etchstop.overetch=0.01
struct tdr= n@node@_nFinFET21 ;# PSG
# Dummy gate etching
mask name= gate_neg back= ($HalfD-$HalfLg)<um> front= ($HalfD+$HalfLg)<um>
negative
#strip Polysilicon
etch material= {Polysilicon} type=anisotropic time=1 rate= {1}
etch material= {Oxide} type=anisotropic time=1 rate= {0.1} mask=gate_neg isotropic.overetch=0.01
struct tdr= n@node@_nFinFET22 ;# SiO2 removal
# Gate stack fabrication
define Tiox 0.001
deposit material= {Oxide} type= isotropic time=1 rate= {$Tiox} selective.materials=
{Silicon}
struct tdr= n@node@_nFinFET23 ;# SiO2
define Tihfo2 0.002
deposit material= {HfO2} type= isotropic time=1 rate= {$Tihfo2} selective.materials=
{Oxide}
struct tdr= n@node@_nFinFET24 ;# HfO2
exit


init tdr= n7_nFinFET24
# MIG
mater add name= TiAl new.like= Aluminum
deposit material= {Aluminum} type= isotropic time=1 rate= {0.0085} selective.materials=
{HfO2}
struct tdr= n@node@_nFinFET25 ;# gate deposition
ambient clear
deposit material= {Tungsten} type=fill coord= -0.2
struct tdr= n@node@_nFinFET26 ;# W fill
```

```
etch material={Tungsten} type=cmp etchstop= {PSG} etchstop.overetch=0.01
struct tdr= n@node@_nFinFET27 ;# metal gate cmp
etch material= {Tungsten} type=isotropic time=1 rate= {0.003}
deposit material= {Nitride} type=fill coord=-0.2
etch material= {Nitride} type=cmp etchstop= {PSG} etchstop.overetch=0.01
struct tdr= n@node@_nFinFET28
mask name=s left=18<nm> right=40<nm> back=($D-0.014)<um> front=($D-
0.004)<um> negative
mask name=d left=18<nm> right=40<nm> back=4<nm> front=14<nm> nega-
tive
mask name=g left=18<nm> right=40<nm> back=($HalfD-$HalfLg+0.001)<um>
front=(HalfD+HalfLg-0.001)<um> negative
etch material= {PSG} type=anisotropic time=1 rate= {0.1} mask=s
struct tdr= n@node@_nFinFET29
etch material= {PSG} type=anisotropic time=1 rate= {0.1} mask=d
struct tdr= n@node@_nFinFET30
etch material= {Nitride} type=anisotropic time=1 rate= {0.1} mask=g
struct tdr= n@node@_nFinFET31
deposit material= {Tungsten} type=fill coord=-0.2
etch material= {Tungsten} type=cmp etchstop= {Nitride} etchstop.overetch=0.01
struct tdr= n@node@_nFinFET32
exit


init tdr= n8_nFinFET32
transform cut location= -0.05 down
# clear the process simulation mesh
refinebox clear
refinebox !keep.lines
line clear
# reset default settings for adaptive meshing
pdbSet Grid AdaptiveField Refine.Abs.Error 1e37
pdbSet Grid AdaptiveField Refine.Rel.Error 1e10
pdbSet Grid AdaptiveField Refine.Target.Length 100.0
# Set high quality Delaunay meshes
pdbSet Grid sMesh 1
pdbSet Grid Adaptive 1
pdbSet Grid SnMesh DelaunayType boxmethod
pdbSet Grid SnMesh CoplanarityAngle 179
pdbSet Grid SnMesh MaxPoints 2000000
pdbSet Grid SnMesh max.box.angle.3d 179
grid set.min.normal.size= 1.0/1.0
set.normal.growth.ratio.3d= 1.0
set.max.points= 2000000
set.max.neighbor.ratio= 1e6
```

```
refinebox name= drain min= {-0.087 0.0 0.0} max= {-0.135 0.062 0.025} xrefine=
4<nm> yrefine= 4<nm> zrefine= 4<nm> materials= {Silicon}
refinebox name= source min= {-0.087 0.0 $D-0.025} max= {-0.135 0.062 $D} xre-
fine= 4<nm> yrefine= 4<nm> zrefine= 4<nm> materials= {Silicon}
refinebox name= channel min= {-0.087 0.0 $HalfD-$HalfLg-0.005} max= {-0.135
0.062 $HalfD+$HalfLg+0.005} xrefine= 2<nm> yrefine= 2<nm> zrefine= 2<nm>
materials= {Silicon}
refinebox name= gate_mio min= {-0.087 0.0 $HalfD-$HalfLg-0.002} max= {-0.143
0.062 $HalfD+$HalfLg+0.002} xrefine= 5<nm> yrefine= 5<nm> zrefine= 5<nm>
materials= {Aluminum}
grid remesh
struct tdr= n@node@_nFinFET33 ;# remeshing
contact bottom name= bulk Silicon
contact name= gate x= -0.140 y= 0.014 z= $HalfD Tungsten
contact name= source x= -0.14 y= 0.0166 z= $D-0.010 Tungsten
contact name= drain x= -0.14 y= 0.0166 z= 0.010 Tungsten
struct tdr= n@node@_presimulation !Gas
exit
```

Appendix C

NSGAATFET Sprocess

```
math coord.ucs
math numThreads=4
AdvancedCalibration 2017.09
pdbSet Mechanics StressRelaxFactor 1
pdbSet Math diffuse 3D ILS.hpc.mode 4
pdbSet Mechanics EtchDepoRelax 0
mgoals resolution= 1.0/3.0 accuracy= 1e-6
pdbSet Grid SnMesh max.box.angle.3d 175
grid set.min.normal.size= 0.005/1.0
set.normal.growth.ratio.3d= 2.0
set.min.edge= 1e-7 set.max.points= 1000000
set.max.neighbor.ratio= 1e6

define STI 0.02 ;# STI
define Tns 0.005 ;# Thickness nanosheet
define Spacing 0.010 ;# Space between nanosheet (SiGe)
define H [expr 4*$Spacing + 3*$Tns + $STI] ;# Fin exposure
define Hfin [expr ($H - $STI)] ;# Fin height

define HalfLg [expr (@Lg@*0.5)] ;# Half gate length
define Tox 0.002 ; Total thickness of gate insulator
define LSpacer 0.008 ; Length Spacer
define D [expr (@Lg@+0.05)] ; Total length of the device
define HalfD [expr ($D*0.5)] ; Half device length

define Tiox 0.001 ;#Gate interlayer oxide thickness
define Tihfo2 0.002 ;#Gate high-k
define TiN1 0.004 ;# layer TiN
define Nsub 1.0e15 ;#Substrate doping
define Nsd 3.0e12 ;#SD doping [/cm2]
```

```
define Next 2.0e12 ;#S/D extension doping [/cm2]
define Nstop 1.0e13 ;#channel stop doping [/cm2]

line x location= -70.0<nm> spacing=10.0<nm> tag= SiTop
line x location= 20.0<nm> spacing= 10.0<nm>
line x location= 50.0<nm> spacing= 20.0<nm> tag= SiBottom

line y location= 0.0 spacing= 50.0<nm> tag= Left
line y location= 0.062<μm> spacing= 50.0<nm> tag= Right

line z location= 0.0 spacing= 50.0<nm> tag= Back
line z location= $D<μm> spacing= 50.0<nm> tag= Front

#substrate
region Silicon xlo= SiTop xhi= SiBottom ylo= Left yhi= Right zlo= Back zhi=
Front substrate

init concentration=$Nsub<cm-3> field=Boron wafer.orient= 0 0 1 flat.orient= 1
1 0 !DelayFullD

refinebox name= nw min= -0.12 0 0.0 max= -0.05 0.11 $D xrefine= 5<nm> yre-
fine= 10<nm> zrefine= 50<nm>
grid remesh
#–Epi layer with known doping concentration (well)
deposit material= Silicon type=isotropic time=1 rate= $H
struct tdr= n@node@_nGAAFET1a
deposit material= SiliconGermanium type=isotropic time=1 rate= $Spacing
deposit material= Silicon type=isotropic time=1 rate= $Tns
deposit material= SiliconGermanium type=isotropic time=1 rate= $Spacing
deposit material= Silicon type=isotropic time=1 rate= $Tns
deposit material= SiliconGermanium type=isotropic time=1 rate= $Spacing
deposit material= Silicon type=isotropic time=1 rate= $Tns
deposit material= SiliconGermanium type=isotropic time=1 rate= $Spacing
struct tdr= n@node@_nGAAFET1b

#Sidewall Image Transfer (SIT)
diffuse temperature= 900<C> time= 4.0<min> O2
deposit material= Nitride type= isotropic time= 1<min> rate= 0.0165
deposit material= AmorphousSilicon type= isotropic time= 1<min> rate= 0.0195
struct tdr= n@node@_nGAAFET1c ;#deposit SiO2, hardmask, mandrel
mask name= fin left= 0<nm> right= 38<nm> back= -1 front= ($D+0.001)<μm>
negative
etch material= AmorphousSilicon type= anisotropic time= 1<min> rate= 0.04
mask= fin
struct tdr= n@node@_nGAAFET1d
```

deposit material= Oxide type= isotropic time= 1 rate= 0.015
etch material= Oxide type= anisotropic time= 1 rate= 0.015 isotropic.overetch= 0.1
struct tdr= n@node@_nGAAFET1e
etch material= AmorphousSilicon type= anisotropic time=1<min> rate= 0.3
etch material= Nitride type=anisotropic time= 1<min> rate= 0.02
struct tdr= n@node@_nGAAFET1f
etch material= Oxide type= anisotropic time=1 rate= 0.02
struct tdr= n@node@_nGAAFET1g
etch material= Silicon SiliconGermanium type=anisotropic time=1<min> rate= $H
struct tdr= n@node@_nGAAFET1h
mater add name=TEOS new.like=oxide
deposit material= TEOS type= isotropic time= 1<min> rate= ($H+0.0165)
etch material= TEOS type=cmp etchstop= Nitride etchstop.overetch=0.0001
struct tdr= n@node@_nGAAFET1i

etch material= TEOS type=isotropic time=1 rate= (0.0165+0.002+$Hfin)
etch material= Nitride type=anisotropic time=1 rate= 0.02
etch material= Oxide type= anisotropic time=1<min> rate= 0.01
struct tdr= n@node@_nGAAFET2 ;# Fin
mask name= inner back= ($HalfD-$HalfLg-$LSpacer)<um> front= ($HalfD+$HalfLg+$LSpacer)<μm>
etch material= Silicon SiliconGermanium type= anisotropic time=1 rate= $Hfin mask= inner
######## CHANNEL DOPING
define Next 4e9
implant Boron dose= $Next<cm-2> energy=1<keV> tilt=7<degree> rotation=-90<degree>
implant Boron dose= $Next<cm-2> energy=1<keV> tilt=-7<degree> rotation=-90<degree>
implant Boron dose= $Next<cm-2> energy=10<keV> tilt=7<degree> rotation=-90<degree>
implant Boron dose= $Next<cm-2> energy=10<keV> tilt=-7<degree> rotation=-90<degree>
implant Boron dose= $Next<cm-2> energy=20<keV> tilt=7<degree> rotation=-90<degree>
implant Boron dose= $Next<cm-2> energy=20<keV> tilt=-7<degree> rotation=-90<degree>
diffuse temperature=1050<C> time=400<s>
struct tdr= n@node@_nGAAFET3
mask name= fin_dummy left=20.3<nm> right=38<nm> back=-1<um> front= ($D+0.001)<$\mu$m>
mask name= fin_dummy_neg left=20.3<nm> right=38<nm> back=-1<um> front= ($D+0.001)<$\mu$m> negative
deposit material= Silicon type= anisotropic time=1 rate= 1 mask= inner
struct tdr= n@node@_nGAAFET4

etch material= Silicon type= anisotropic time=1 rate= 1 mask=fin_dummy
struct tdr= n@node@_nGAAFET5
etch material= Silicon type=cmp etchstop= SiliconGermanium etchstop.overetch=0.001
struct tdr= n@node@_nGAAFET5.5

#Dummy gate
deposit material= Oxide type= isotropic time=1 rate= $Tiox
struct tdr= n@node@_nGAAFET6
deposit material= Polysilicon type= fill coord= -0.27
mask name= gate back= ($HalfD-$HalfLg)<um> front= ($HalfD+HalfLg)<um>
etch material= Polysilicon type= anisotropic time=1 rate= 0.5 mask= gate
struct tdr= n@node@_nGAAFET7

#S/D extension
refinebox name= sd min= -0.18 0 0.0 max= -0.12 0.062 $D xrefine= 2<nm> yrefine= 5<nm> zrefine= 2<nm>
grid remesh
SOURCE DOPING
mask name= source_neg left= 0<nm> right= 1 back= -1<nm> front= ($D-0.008)<$\mu$m> negative ;
photo thickness= 0.3<μm> mask= source_neg
struct tdr= n@node@_nGAAFET8_controllo
define Next 5e18
implant Boron dose= $Next<cm-2> energy=1.5<keV> tilt=45<degree> rotation=-90<degree>
implant Boron dose= $Next<cm-2> energy=1.5<keV> tilt=-45<degree> rotation=-90<degree>
struct tdr= n@node@_nGAAFET8 ; retrograde source doping
strip Photoresist
DRAIN DOPING
mask name= drain_neg left= 0<nm> right= 1 back= (0.011)<um> front= 1 negative ;
deposit material= Photoresist type= anisotropic time= 1<min> rate= 0.3 mask= drain_neg
photo thickness= 0.3<μm> mask= drain_neg
struct tdr= n@node@_nGAAFET9_controllo
define Next 1e13
implant Phosphorus dose= $Next<cm-2> energy=1<keV> tilt=45<degree> rotation=-90<degree>
implant Phosphorus dose= $Next<cm-2> energy=1<keV> tilt=-45<degree> rotation=-90<degree>
implant Phosphorus dose= $Next<cm-2> energy=5<keV> tilt=45<degree> rotation=-90<degree>
implant Phosphorus dose= $Next<cm-2> energy=5<keV> tilt=-45<degree> rotation=-90<degree>

```
etch material= Nitride type=anisotropic time=1 rate= 0.02
struct tdr= n@node@_nGAAFET9 ; retrograde drain doping
strip Photoresist
diffuse temperature=1000<C> time=0.00005<s>
struct tdr= n@node@_nGAAFET12 ;# Final doping

init tdr= n2_nGAAFET12
mask name= gate_neg back= ($HalfD-$HalfLg)<um> front= ($HalfD+$HalfLg)<μm>
negative
mask name= inner_neg back= ($HalfD-$HalfLg-$LSpacer)<μm> front= ($HalfD+$HalfLg+$LSpacer)<μ
negative
etch material= Oxide type=anisotropic time=1 rate=1.0
etch material= SiliconGermanium type= anisotropic time=1 rate= 0.5 mask= gate
deposit material= Oxide type= isotropic time=1<min> rate= $Tiox selective.materials=
PolySilicon
etch material= Oxide type=cmp etchstop= PolySilicon etchstop.overetch=0.001
mask name= spacer_neg back= ($HalfD-$HalfLg-$LSpacer)<μm> front= ($HalfD+$HalfLg+$LSpacer)<μ
negative
deposit material= Nitride type= anisotropic time=1<min> rate= 0.5 mask=spacer_neg
etch material= Nitride type=cmp etchstop= PolySilicon etchstop.overetch=0.001
struct tdr= n@node@_nGAAFET13 ;# Spacer
# Silicidation
deposit material= TiSilicide type= isotropic rate= 0.007 time= 1.0 temperature=
450 selective.materials= Silicon
struct tdr= n@node@_nGAAFET14
# Planarization PSG
mater add name= PSG
ambient name=Silane react add
reaction name= PSGreaction mat.l= Phosphorus mat.r= Oxide mat.new= PSG
new.like= Oxide ambient.name= Silane diffusing.species= Silane
deposit material= PSG type= isotropic time=1 rate= 0.5
etch material= PSG type=cmp etchstop= Nitride etchstop.overetch=0.01
struct tdr= n@node@_nGAAFET15
# Dummy gate etching
etch material= Polysilicon type=anisotropic time=1 rate= 0.5
etch material= Oxide type=isotropic time=1 rate= 0.5 mask=gate_neg isotropic.overetch=0.01
struct tdr= n@node@_nGAAFET16
etch material= SiliconGermanium type=isotropic time=1 rate= 1
struct tdr= n@node@_nGAAFET17
# Gate stack fabrication
deposit material= Oxide type= isotropic time=1 rate= $Tiox
etch material= Oxide type=cmp etchstop= Nitride etchstop.overetch=0.01
struct tdr= n@node@_nGAAFET18 ;# SiO2
deposit material= HfO2 type= isotropic time=1 rate= $Tihfo2 selective.materials=
Oxide
```

```
etch material= HfO2 type=cmp etchstop= Nitride etchstop.overetch=0.01
struct tdr= n@node@_nGAAFET19 ; HfO2
deposit material= Aluminum type= isotropic time=1 rate= $TiN1
etch material= Aluminum type=cmp etchstop= Nitride etchstop.overetch=0.01
struct tdr= n@node@_nGAAFET20 ;# TiN1 deposition
diffuse temp=500<C> time=1.0e-6<s> stress.relax
ambient clear
deposit material= Tungsten type=fill coord= -0.5
etch material= Tungsten type=cmp etchstop= PSG etchstop.overetch=0.01
etch material= Tungsten type=isotropic time=1 rate= 0.003
struct tdr= n@node@_nGAAFET21
deposit material= Nitride type=fill coord=-0.5
etch material= Nitride type=cmp etchstop= PSG etchstop.overetch=0.01
struct tdr= n@node@_nGAAFET22
mask name=s left=18<nm> right=40<nm> back=($D-0.014)<μm> front=($D-
0.004)<μm> negative
mask name=d left=18<nm> right=40<nm> back=4<nm> front=14<nm> nega-
tive
mask name=g left=18<nm> right=40<nm> back=($HalfD-$HalfLg+0.009)<μm>
front=($HalfD+$HalfLg-0.009)<μm> negative
etch material= PSG type=anisotropic time=1 rate= 0.1 mask=s
etch material= PSG type=anisotropic time=1 rate= 0.1 mask=d
etch material= Nitride type=anisotropic time=1 rate= 0.1 mask=g
deposit material= Tungsten type=fill coord=-0.5
etch material= Tungsten type=cmp etchstop= Nitride etchstop.overetch=0.01
struct tdr= n@node@_nGAAFET23
transform cut location= -0.05 down
# clear the process simulation mesh
refinebox clear
refinebox !keep.lines
line clear
# reset default settings for adaptive meshing
pdbSet Grid AdaptiveField Refine.Abs.Error 1e37
pdbSet Grid AdaptiveField Refine.Rel.Error 1e10
pdbSet Grid AdaptiveField Refine.Target.Length 100.0
# Set high quality Delaunay meshes
pdbSet Grid sMesh 1
pdbSet Grid Adaptive 1
pdbSet Grid SnMesh DelaunayType boxmethod
pdbSet Grid SnMesh CoplanarityAngle 179
pdbSet Grid SnMesh MaxPoints 2000000
pdbSet Grid SnMesh max.box.angle.3d 179
grid set.min.normal.size= 1.0/1.0
set.normal.growth.ratio.3d= 1.0
set.max.points= 2000000
```

set.max.neighbor.ratio= 1e6
refinebox name= drain min= -0.130 0.0 0.0 max= -0.250 0.062 0.025 xrefine= 3.5<nm> yrefine= 3.5<nm> zrefine= 3.5<nm> materials= Silicon
refinebox name= source min= -0.130 0.0 $D-0.025 max= -0.250 0.062 $D xrefine= 3.5<nm> yrefine= 3.5<nm> zrefine= 3.5<nm> materials= Silicon
refinebox name= drain_Ti min= -0.130 0.0 0.0 max= -0.250 0.062 0.025 xrefine= 2<nm> yrefine= 2<nm> zrefine= 2<nm> materials= TiSilicide
refinebox name= source_Ti min= -0.130 0.0 $D-0.025 max= -0.250 0.062 $D xrefine= 2<nm> yrefine= 2<nm> zrefine= 2<nm> materials= TiSilicide
refinebox name= channel min= -0.130 0.0 $HalfD-$HalfLg-0.002 max= -0.250 0.062 $HalfD+$HalfLg+0.002 xrefine= 2<nm> yrefine= 2<nm> zrefine= 2<nm> materials= Silicon
refinebox name= gate_mio min= -130 0.0 $HalfD-$HalfLg-0.002 max= -0.250 0.062 $HalfD+$HalfLg+0.002 xrefine= 4<nm> yrefine= 4<nm> zrefine= 4<nm> materials= Aluminum
grid remesh
struct tdr= n@node@_pGAA41 ;# remeshing
contact bottom name= bulk Silicon
contact name= gate x= -0.265 y= 0.026 z= $HalfD Tungsten
contact name= source x= -0.265 y= 0.026 z= $D-0.010 Tungsten
contact name= drain x= -0.265 y= 0.026 z= 0.010 Tungsten
struct tdr= n@node@_presimulation !Gas
exit

Appendix D

Sdevice

```
File
{
Grid ="n@previous@_presimulation_fps.tdr"
Parameter = "sdevice.par"
Output = "n@node@_log"
Plot = "n@node@_des.tdr"
Current= "n@node@_des.plt"
}
Electrode
{
{ name="source" Voltage=0.0 }
{ name="drain" Voltage=0.0 }
{ name="gate" Voltage=0.0 }
{ name="bulk" Voltage=0.0 }
}
Physics
{
Hydrodynamic
Fermi
IncompleteIonization
Mobility(Tunneling DopingDep HighFieldsaturation Enormal)
EffectiveIntrinsicDensity( BandGapNarrowing(Slotboom) Fermi )
Recombination(SRH(DopingDep) Auger Band2Band(Hurkx))
Temperature=300
eQuantumPotential
hQuantumPotential
}
Plot{
eDensity hDensity
ConductionCurrentDensity
```

```
TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
eMobility/Element hMobility/Element
eVelocity hVelocity
eQuasiFermi hQuasiFermi
ElectricField/Vector Potential SpaceCharge
ElectrostaticPotential
Doping DonorConcentration AcceptorConcentration
SRH Band2Band Auger
AvalancheGeneration eAvalancheGeneration hAvalancheGeneration
eGradQuasiFermi/Vector hGradQuasiFermi/Vector
eEparallel hEparallel eENormal hENormal
BandGap
BandGapNarrowing EffectiveBandGap
Affinity ElectronAffinity
ConductionBandEnergy ValenceBandEnergy
eQuantumPotential hQuantumPotential
eQuasiFermiEnergy hQuasiFermiEnergy
}
Math
{
-CheckUndefinedModels
Extrapolate
Derivatives
RelErrControl
Digits=5
Iterations = 500
NoSRHperPotential
Number_of_Threads = 4
ExitOnFailure
}
Solve
{
CoupledPoisson
Coupled(Iterations=100 LineSearchDamping=1e-4){ Poisson eQuantumPotential }
Coupled{ Poisson eQuantumPotential Electron}
Save( FilePrefix= "n@node@_init")
NewCurrentPrefix = "n@node@_IdVd1"
Quasistationary(
InitialStep=0.001
MinStep=1e-7 MaxStep=0.025
Goal{ Name="drain" Voltage= 1 } )
{Coupled{ Poisson eQuantumPotential Electron }
CurrentPlot(Time=(Range=(0 1) Intervals=100))
}
NewCurrentPrefix = "n@node@_IdVg1"
```

```
Quasistationary(
InitialStep=0.001
MinStep=1e-7 MaxStep=0.025
Goal{ Name="gate" Voltage= 1 })
{ Coupled Poisson eQuantumPotential Electron }
CurrentPlot(Time=(Range=(0 1) Intervals=100))
}
}
```

Bibliography

[1] Sazzad, H., Nafis, M., Showmik, S., Jibesh, K. S. (2020). A Comprehensive Study on Tunneling Field Effect Transistor using Non-local Band-to Band Tunneling Model.

[2] Vergallo, D. (2018). Analysis and Simulation of Emerging FET Devices: FinFET, TFET.

[3] Vandenberghe, W., Verhulst, A., Groeseneken, G., Soree, B., Magnus, W. (2019) Analytical Model for a Tunnel Field-Effect Transistor

[4] Jang, H. K., Hyun, W. K., Garam, K., Sangwan, K., Byung-Gook, P. (2019). Demonstration of Fin-Tunnel Field-Effect Transistor with Elevated Drain.

[5] Nelaturi Nagendra Reddy and Deepak Kumar Panda 2022 J. Micromech. Microeng. 32 085001 Design and investigation of dielectric modulated triple metal gate-oxide-stack Z-shaped gate horizontal pocket TFET device as a label-free biosensor

[6] Syed, A. A., Naushad, A. (2021). Design of a triple pocket multi-gate material TFET structure for low-power applications.

[7] Sweta Chander1, Sanjeet Kumar Sinha2, Prince Kumar Singh3 and Ashish Kumar Singh (2021) Design of HeterojunctionTunnel Field-Effect Transistors with SiO2 isolation between Source and Drain for Low Power Application

[8] Jie, L., Qian, X., Anpeng, H., Zheng, W. (2020). Effects of Drain Doping Profile and Gate Structure on Ambipolar Current of TFET.

[9] Caminiti, A. (2019). Evaluation of TFETs perfromances for low power applications.

[10] Coppolelli, B. (2022) Modeling of Tunnel-FETs: accurate calibration of numerical and semi-analytical models

[11] Choi, Y., Hong, Y., Ko, E., Shin, C. (2020) Optimization of double metal-gate InAs/Si heterojunction nanowire TFET

[12] A Shaker et al 2020 Semicond. Sci. Technol. 35 025007 Source-all-around tunnel field-effect transistor (SAA-TFET): proposal and design

[13] «TCAD Sentaurus Device Manual, Synopsys, Inc., Mountain View, CA, USA, 2020»

[14] «TCAD Sentaurus Process Manual, Synopsys, Inc., Mountain View, CA, USA, 2020»

[15] Smerklo, L., Nevzorov, V., Behen, V., Nevzorova, T., Galkina, L. (2002) The design basis of general components for high-power MOSFET CAD

[16] Uygar E. A., Daniel H. M., Ian A. Y. (2015). Tunnel Field-Effect Transistors: Prospects and Challenges.

[17] Victor De Bodt Sivieri et al 2015 ECS Trans. 66 187 Vertical Nanowire TFET Diameter Influence on Intrinsic Voltage Gain for Different Inversion Conditions

[18] Wikipedia (2023) https://en.wikipedia.org/wiki/MOSFET

[19] Wikipedia (2023) https://en.wikipedia.org/wiki/Tunnel field-effect transistor

[20] Donati, S., Slide "Micro and Nanoelectronic devices", Politecnico di Torino, (2022)

[21] Vacca, M. Slide "Technology for nanoelectronic systems", Politecnico di Torino, (2022)

[22] Lev Davidovich Landau and Evgenii Mikhailovich Lifshitz. Quantum mechanics: non-relativistic theory. Vol. 3. Elsevier, 2013.

[23] RADHAKRISHNAN SITHANANDAM, MAMIDALA JAGADESH KUMAR (2018) A New On-Chip ESD Strategy Using TFETs-TCAD Based Device and Network Simulations.

[24 Md. Ziaur Rahman Khan. (2017). Physics-Based Generalized Threshold Voltage Model of Multiple Material Gate Tunneling FET Structure

[25 Ashcroft, Mermin (1976). Solid-state physics.