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Development of load modulated power amplifiers for communications in sub-6 GHz bands

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Abstract

The rapid evolution of wireless communication has led to greater demands on higher data rates and wider spectrum. As one of the final stages in the transmitter chain before the antenna, Power Amplifiers (PAs) are responsible for handling significant signal power that is fed into the antenna. Moreover, due to the growing need for higher data rates, PAs are often driven to adopt signals with high peak-to-average power ratio. Therefore, they play a crucial role and encounter stringent challenges in terms of achieving wide operational bandwidth and high efficiency performance, especially when working at the average output power lower than the saturation one, namely in output back-off.

This thesis presents the analysis, design and implementation of an RF-input sequential Load Modulated Balanced Amplifier (LMBA). This architecture is able to modulate the impedance seen by a pair of power amplifiers in a quadrature balanced configuration, by modifying the amplitude and the phase of an external control signal injected into the isolation port of the output coupler. Compared to conventional single-ended or Doherty power amplifiers, LMBAs extend better the high-efficiency power range and are able to achieve high back-off efficiency across a wider bandwidth.

A hybrid prototype is designed and simulated, based on commercial 10-W GaN packaged transistors, to achieve highly efficient performance in the 5G N77 frequency band (from 3.3 GHz to 4 GHz) at 9-dB output power back-off. The simulation results achieve a wideband performance with 50% drain efficiency and 35% power added efficiency for maximum output power above 43 dBm, and 40% efficiency and 35% PAE for 9-dB output back-off in the whole bandwidth. Future developments of this thesis work would be the measurement and verification of the fabricated circuits.

Acknowledgements

During the preparation of this Master's thesis, I received countless help from my supervisors, colleagues, friends, and family. I would like to express my sincerest gratitude to all of them. Their advice and support contributed significantly to the successful completion of this thesis.

First and foremost, I am deeply grateful to my supervisors, Prof. Camarchia Vittorio and Dr. Piacibello Anna, for their invaluable guidance, instruction and support. Their expertise, insightful comments, and thoughtful encouragement played a pivotal role in the selection of the research topic, the design work, and the writing and correction of the thesis. I greatly appreciate their passion, patience, and the enlightening ideas they shared with me.

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Table of Contents

List of Tables

List of Figures

Acronyms

ADS
Advanced Design System

BPA
Balanced Power Amplifier

CSP
Control Signal Power

CA
Carrier Amplifier

DPA
Doherty Amplifier

FET
Field-effect Transistor

IMN
Input Matching Network

LMBA
Load Modulated Balanced Amplifier

MN
Matching Network

OBO
Output Power Back-off

OMN
Output Matching Network

PA
Power Amplifier

PAE
Power Added Efficiency

PAPR
Peak-to-average Power Ratio

RF
Radio Frequency

SLMBA
Sequential Load Modulated Balanced Amplifier

Chapter 1

Introduction

1.1 Motivation

The rapid evolution of wireless communications is requiring microwave based front-ends which are able to sustain increasingly stringent specifications. As the technology standard develops towards the fifth-generation (5G), the ever-growing demands on data rate and spectrum efficiency lead to the use of modulated signals with high peak-to-average (PAPR) in radio frequency (RF) systems. Regarding the transmitter, the spectrum is expanding towards higher frequencies and power amplifier (PA) results to be the bottleneck of the design. In particular, PAs are desired to have simultaneously wide operational bandwidth, good linearity and high efficiency at large output power back-off (OBO) in order to reduce the cost, spacing and complexity. However, such design goals are always challenging since the requirements for linearity and bandwidth are always in conflict with back-off efficiency in conventional PA design. A common strategy for efficiency enhancement is the load modulation technique and many PA architectures have been proposed, such as Doherty Amplifier (DPA) [1], envelop tracking [2] and outphasing [3]. Among them, DPA has become one of the most popular PA architectures in cellular base stations due to its low complexity and good reliability. Nevertheless, in upcoming 5G systems, DPA design becomes more difficult while further increasing the bandwidth.

Recently, a new PA architecture called Load Modulated Balanced Amplifier (LMBA) was proposed in [4] and many variations have been demonstrated in [5, 6, 7], where an additional control signal is injected into the isolation port of the output quadrature coupler. The active load modulation of the balanced power amplifiers (BPAs) is realised by varying the amplitude and phase of control signal generated by the control signal power (CSP) PA. One special configuration was proposed in [8] and it was named as Sequential Load Modulated Balanced Amplifier (SLMBA),

where the CSP PA is also called carrier PA (CA). The most important feature of SLMBA is that, there is no load modulation effect at the carrier output and the additional power increase of the SLMBA is entirely provided by the BPA pair due to the saturation status of the carrier, which eventually allows it to achieve high efficiency performance at deep OBO level [9].

This thesis work is dedicated to the implementation of the SLMBA architecture using identical transistors. The available commercial packaged device is the Cree 10W GaN (gallium nitride) HEMT. The amplifier is targeted on the 5G mobile network at $N77$ frequency band (from 3.3 GHz to 4 GHz). The design environment is PathWave Advanced Design System (ADS). Summarizing, the design process consists in:

- Preliminary analysis of LMBA theory
- Evaluation of the packaged GaN HEMT transistor
- Design of various functional blocks (stabilization networks, matching networks, combining/splitting networks,...)
- Assembly and simulation of SLMBA architecture
- Creation of the layout and Electromagnetic simulation.

The initial target specifications of the SLMBA are listed in Table 1.1.

Frequency	Power Gain	P_{SAT}	Efficiency	OBO
(3.3-4) GHz	12 dB	36 dBm	best effort	9-dB

Table 1.1: Summary of the target performance of this thesis work.

1.2 Thesis organization

The thesis is organized as follows.

The present chapter gives the background on power amplifiers in wireless communication systems and reviews some essential fundamentals. Chapter 2 demonstrates various load modulation architectures, ranging from the traditional DPA to the more advanced SLMBA. Circuit design details about the SLMBA are illustrated in Chapter 3, which includes the characterisation of packaged devices and the design of biasing networks, matching networks, power splitting and combining networks. In Chapter 4, the implementation of the SLMBA is described in terms of the microstrip circuit schematic and the layout view. Finally, Chapter 5 concludes the thesis by evaluating and summarizing the performance of the presented SLMBA.

1.3 Power amplifiers in wireless communication

Nowadays, wireless communication is ubiquitous throughout the world. In all wireless systems, signals containing information are modulated and transmitted by the transmitter (TX), while the modulated signals are received and reconstructed by the receiver (RX), as it is shown in Figure 1.1 [10]. This transmission requires the electromagnetic waves to be sent over a long distance via air, which means that in the transmitter the signal power fed into the antenna must be sufficiently high. The power budget therefore has a significant impact on the transmitter front-end, resulting in PA being the decisive component in the final performance of the RF system in terms of power gain, efficiency, linearity, etc.

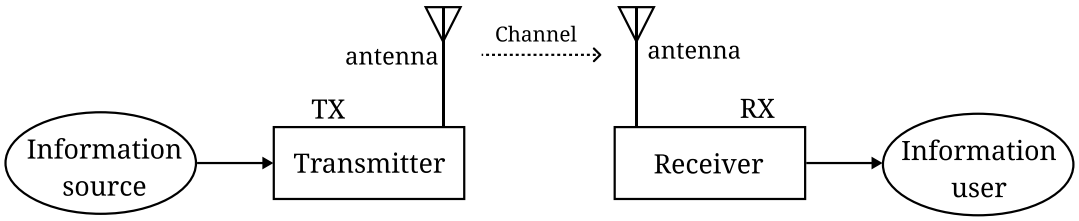

Figure 1.1: Wireless communication chain.

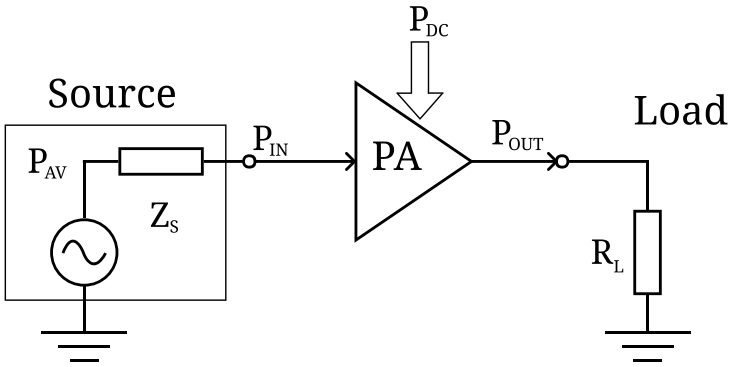

Figure 1.2: General schematic of a power amplifier.

1.3.1 PA basics

The RF power amplifier is a quasi-linear system which amplifies the low power RF signal into a high power RF signal while maintaining the waveform fidelity and minimizing distortion, which is achieved by drawing additional power P_{DC} from

a DC supply. A simple scheme is shown in Figure 1.2, where PA is connected at the input to an equivalent source with available power P_{AV}, and at the output to an equivalent load R_{L}. The input and output impedance are considered to match the normalized system impedance (typically 50 Ω). The PA input usually is a narrowband signal centered around f_0 with total input power P_{IN}, which is the actual power delivered to the PA and is different from the available power P_{AV} due to the reflection losses. The output power P_{OUT} is the power delivered to the load and it is measured at the fundamental frequency. Since PAs always exhibit nonlinear effects, such as harmonic distortion, the amplifier behavior depends on not only the input signal level, but also on the spectrum of the input signal.

Several performance indicators, known as figures of merit, can be used to characterize a PA's performance.

Saturation output power

The maximum output power, also called saturation output power $P_{\mathrm{OUT,sat}}$, is limited by the active device used in the PA. For transistors, the limitation comes mainly from the breakdown voltage and the maximum drain current.

OBO

Before reaching the maximum power, the distance from the saturation power is represented by OBO:

$$OBO|_{\mathrm{dB}} = 10\log_{10}\frac{P_{\mathrm{OUT,sat}}}{P_{\mathrm{OUT}}(f_0)}. \tag{1.1}$$

Power gain

The amplification ability of PA is described by the power gain. Specifically, the operation gain G_{op} is defined as the ratio between the output power delivered to the load and the input power delivered to the PA, i.e.:

$$G_{\mathrm{op}} = \frac{P_{\mathrm{OUT}}(f_0)}{P_{\mathrm{IN}}(f_0)}, \tag{1.2}$$

and the transducer gain G_{tr}:

$$G_{\mathrm{tr}} = \frac{P_{\mathrm{OUT}}(f_0)}{P_{\mathrm{AV}}(f_0)}, \tag{1.3}$$

which is the ratio between the output power delivered to the load and the available power at the source.

Efficiency

The efficiency η is the ratio between the output RF power and the DC power consumed from the DC supply:

$$\eta = \frac{P_{\mathrm{OUT}}(f_0)}{P_{\mathrm{DC}}}. \tag{1.4}$$

Power added efficiency

If considering also the input power in the budget as well, the Power Added Efficiency (PAE) is defined as:

$$PAE = \frac{P_{\mathrm{OUT}}(f_0) - P_{\mathrm{IN}}(f_0)}{P_{\mathrm{DC}}} = \eta\left(1 - \frac{1}{G_{\mathrm{op}}}\right). \tag{1.5}$$

It is obvious from (1.5) that, a higher power gain leads to a smaller gap between the PAE and η.

Stability

The stability of the active device is a crucial aspect for PA design. It is essential to prevent any undesired oscillations not only within the operational frequency band but also outside of it, particularly at low frequencies [11, 12]. Some criteria have been developed to determine whether a two-port is unconditionally stable or potentially unstable [13].

The two-parameter unconditional stability criteria are defined as:

$$K = \frac{1 - |S_{22}|^2 - |S_{11}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} > 1, \tag{1.6}$$

where Δ must satisfy:

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1. \tag{1.7}$$

And the one-parameter unconditional stability criteria are defined as:

$$\mu_1 = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^*\Delta| + |S_{12}S_{21}|} > 1, \tag{1.8}$$

$$\mu_2 = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^*\Delta| + |S_{12}S_{21}|} > 1. \tag{1.9}$$

Maximum available gain (MAG)

If the two-port is unconditionally stable and the optimum termination exist [13], the maximum available gain (MAG) is defined as:

$$MAG = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2 - 1}\right). \tag{1.10}$$

1.3.2 PA classifications

PAs are commonly implemented with a single transistor in electronic circuits. A single-ended PA based on Field-effect Transistor (FET) device is presented in Figure 1.3. The PA is classified according to its operation modes.

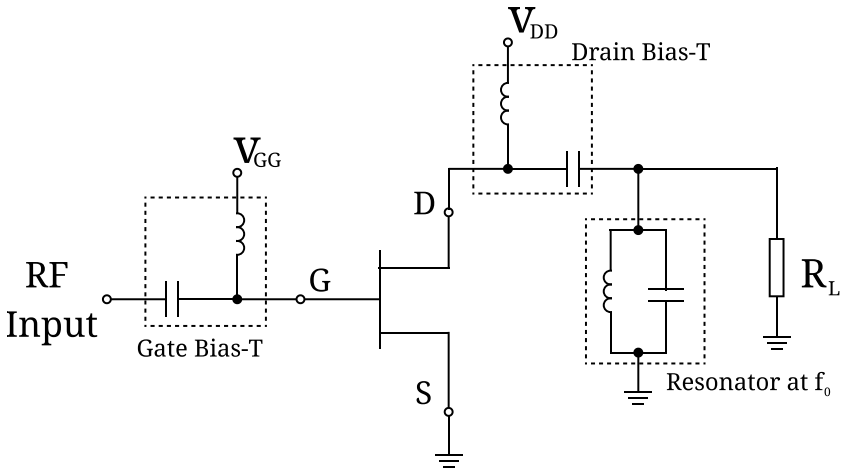

Figure 1.3: Power amplifier in single-ended configuration based on FET device with tuned load.

Considering an ideal FET model, which is a non-linear voltage controlled current source when the drain voltage varies within the range of knee voltage $V_{\mathrm{DS,k}}$ to breakdown voltage $V_{\mathrm{DS,br}}$, in order to obtain the maximum output voltage swing the drain bias should be chosen at the center of the dynamics. From the output and transfer characteristic of an ideal FET device in Figure 1.4 [10], where non-linear g_{m} effect is neglected, PA classes A, AB, B and C are determined by their different quiescent bias points, especially by the gate bias.

Class-A

In a Class-A amplifier, the transistor is biased at half of the gate threshold voltage such that it is always conducting even without input, as shown in Figure 1.5 [10].

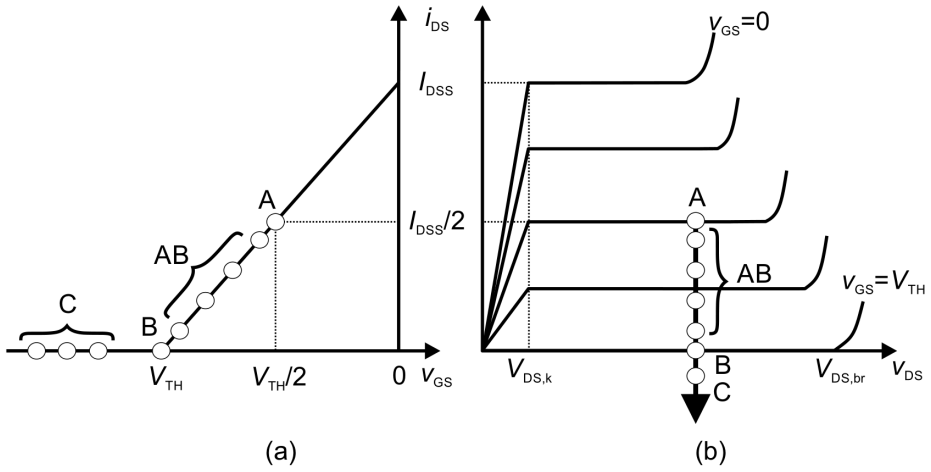

Figure 1.4: (a) Transfer characteristics and (b) output characteristics of ideal FET, with different bias point classifications ([10]).

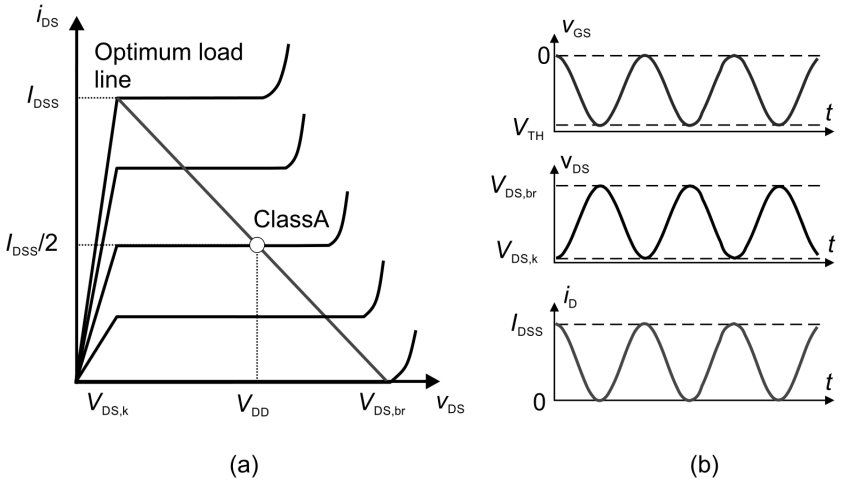

Figure 1.5: Ideal Class-A PA waveforms at maximum voltage drive: (a) output characteristics with the dynamic load line and (b) time domain signal waveforms ([10]).

In other words, the amplifier draws a significant amount of power from the power supply, generating heat and reducing efficiency. However, it has the best linearity since there is no distortion at the output before input signal reaches saturation (still under the assumption of constant g_{m}, i.e., linear transfer characteristics).

The device will observe a fundamental load of R_{L} and a short circuit at all the other harmonics, as described in Figure 1.3. The PA can deliver the maximum output power only when the FET device is reaching simultaneously the maximum

voltage and current dynamics. Which means the PA should see its optimum load as:

$$R_{\mathrm{L}} = R_{\mathrm{opt,A}} = \frac{V_{\mathrm{DS,br}} - V_{\mathrm{DS,k}}}{I_{\mathrm{DSS}}}, \tag{1.11}$$

where I_{DSS} is the maximum drain current under zero gate bias voltage. The maximum RF output power is evaluated as:

$$P_{\mathrm{RF,max}} = \frac{1}{2} \cdot \frac{V_{\mathrm{DS,br}} - V_{\mathrm{DS,k}}}{2} \cdot \frac{I_{\mathrm{DSS}}}{2}. \tag{1.12}$$

Meanwhile the DC power absorbed from the supply is:

$$P_{\mathrm{DC}} = \frac{V_{\mathrm{DS,br}} - V_{\mathrm{DS,k}}}{2} \cdot \frac{I_{\mathrm{DSS}}}{2}. \tag{1.13}$$

Thus the maximum efficiency of Class-A PA is:

$$\eta_{\mathrm{max,A}} = \frac{P_{\mathrm{RF,max}}}{P_{\mathrm{DC}}} = 50\%. \tag{1.14}$$

Class-B

In a Class-B amplifier, the active device is biased at the gate threshold voltage V_{TH}. Figure 1.6 [10] illustrates that the device conducts only when there is an input signal present. This reduces the amount of wasted power when there is no input, making it highly efficient, but strongly non-linear due to the fact that the output current is half-wave rectified.

The optimum load that maximizes the voltage and current swing at the same time is:

$$R_{\mathrm{opt,B}} = \frac{V_{\mathrm{DS,br}} - V_{\mathrm{DS,k}}}{I_{\mathrm{DSS}}} = R_{\mathrm{opt,A}}. \tag{1.15}$$

The maximum RF output power and DC power can be derived as [13]:

$$P_{\mathrm{RF,max}} = \frac{1}{2} \cdot \frac{V_{\mathrm{DS,br}} - V_{\mathrm{DS,k}}}{2} \cdot \frac{I_{\mathrm{DSS}}}{2}, \tag{1.16}$$

$$P_{\mathrm{DC}} = \frac{V_{\mathrm{DS,br}} - V_{\mathrm{DS,k}}}{2} \cdot \frac{I_{\mathrm{DSS}}}{\pi}. \tag{1.17}$$

Therefore, the maximum efficiency of the Class-B PA is:

$$\eta_{\mathrm{max,B}} = \frac{P_{\mathrm{RF,max}}}{P_{\mathrm{DC}}} = \frac{\pi}{4} = 78.5\%. \tag{1.18}$$

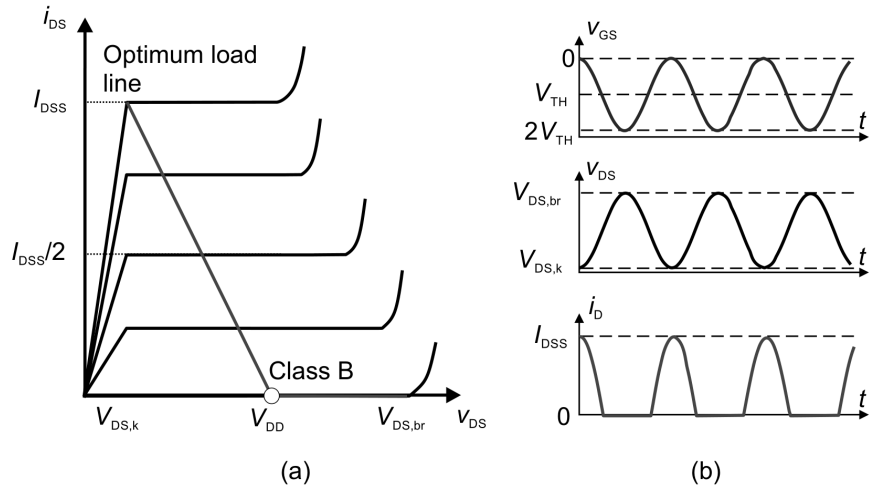

Figure 1.6: Ideal Class-B PA waveforms at maximum voltage drive (a) Output characteristics with the dynamic load line (b) Time domain signal waveforms ([10]).

Class-AB

In a Class-AB amplifier, the FET device is biased between the threshold and half of the threshold, which means it conducts slightly more than half of the time. More specifically, the conduction angle α refers to the portion of the input signal cycle during which the device conducts. For Class-A the conduction angle is 2π, and for Class-B $\alpha = \pi$. In general Class-AB are the one for any α between π and 2π. As a compromise between Class-A and Class-B, Class-AB provides a balance between efficiency, gain and linearity.

Class-C

As the gate bias voltage decreases below V_{TH}, the conduction angle decreases to less than π and the PA passes from Class-B to Class-C. Theoretically for zero conduction angle the PA would have 100% efficiency. However, the output signal is significantly distorted and the gain is equal to zero. Figure 1.7 and 1.8 [13] demonstrate efficiency, PAE, transducer gain and optimum load as a function of conduction angle. In Figure 1.7 the PAE is initially evaluated by Class-A operation gain and in Figure 1.8 the transducer gain and optimum load conductance are normalized to the values in Class-A.

The basic characteristics are listed in Table 1.2.

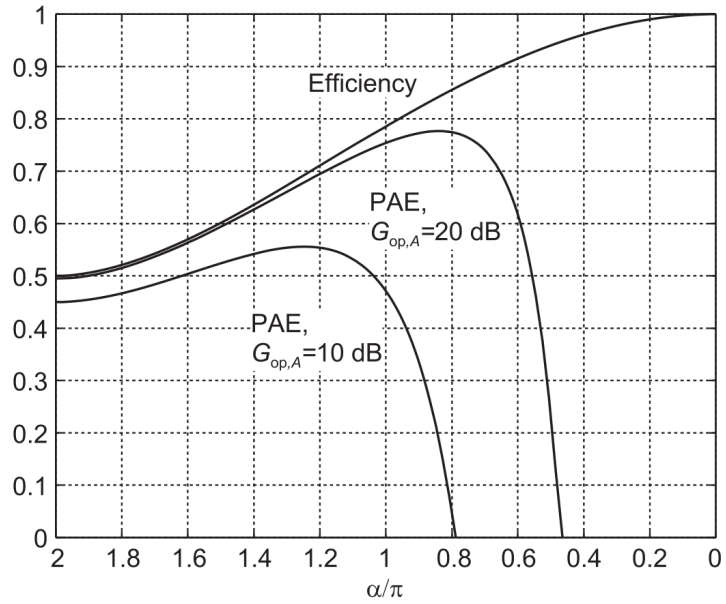

Figure 1.7: Efficiency and PAE as a function of the conduction angle α for different Class-A operational gain values ([13]).

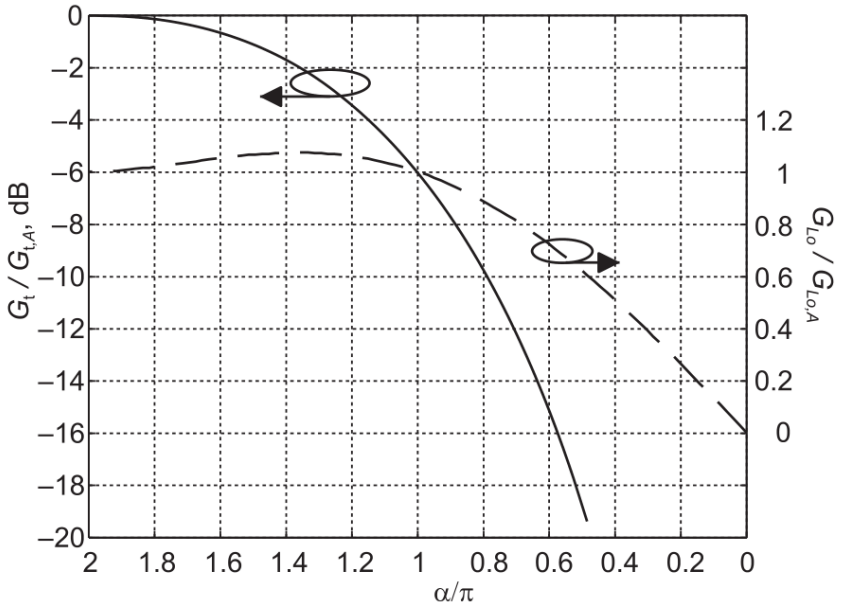

Figure 1.8: Normalized transducer gain G_{tr} (left axis) and optimum conductance G_{Lo} (right axis) as a function of the conduction angle α ([13]).

Classes	V_{GG}	I_{DD}	α	$\eta_{\max}$ [%]
A	$\frac{1}{2}V_{\mathrm{TH}}$	$\frac{1}{2}I_{\mathrm{DSS}}$	2π	50
AB	$V_{\mathrm{TH}} < ... < \frac{1}{2}V_{\mathrm{TH}}$	$0 < ... < \frac{1}{2}I_{\mathrm{DSS}}$	$\pi < ... < 2\pi$	$50 < ... < 78.5$
B	V_{TH}	0	π	78.5
C	$... < V_{\mathrm{TH}}$	0	$0 < ... < \pi$	100

Table 1.2: Summary of the characteristics for different PA classes.

Chapter 2

Theoretical Fundamentals

Conventional single-ended PAs typically achieve their highest efficiency when the input signal drives them to output saturation. However, with the rapidly increasing prevalence of high PAPR signals, this approach is no longer suitable for modern communication systems. The challenge lies in developing PAs that can boost efficiency before reaching output power saturation, addressing the need for improved efficiency in the back-off region.

2.1 From Doherty to LMBA

2.1.1 Doherty Amplifier

A common solution for this issue is the Doherty Amplifier. The concept of the DPA was invented by W.H.Doherty in 1936 [14]. The working principle involves the use of two PAs, named as the Main and Auxiliary amplifiers, which drive current into a common node and modulate each other's load. The schematic is shown in Figure 2.1.

The transistor model is simplified into a ideal current generator model, which is shown in Figure 2.2. The impedance seen by generator 1 is:

$$Z_1 = Z_\mathrm{L} \cdot \left(1 + \frac{I_2}{I_1}\right). \tag{2.1}$$

In a classical 6-dB OBO DPA, the maximum efficiency is achieved at output saturation and at the 6-dB OBO point. When the input power is low, with the input voltage less than half of the maximum, the output power is only provided by the Main amplifier, which is biased in Class-B and loaded with $2R_\mathrm{opt}$. As the input power increases, the Auxiliary amplifier, biased in Class-C, becomes active, and the load seen by the Main PA is modulated from $2R_\mathrm{opt}$ to R_opt. It can be determined from (2.1) that the load impedance Z_L should be $\frac{1}{2}R_\mathrm{opt}$. The current and voltage

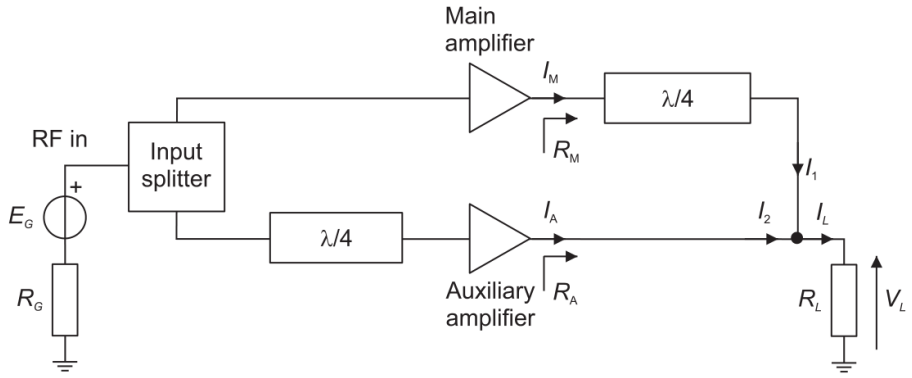

Figure 2.1: General schematic of a DPA ([13]).

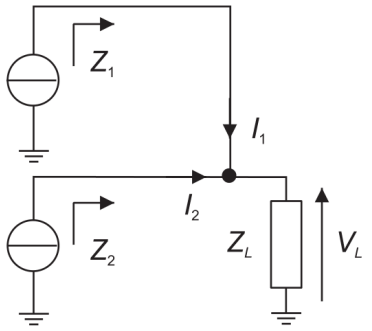

Figure 2.2: Simplified scheme of the output section for a DPA ([13]).

behavior for both the Main PA and the Auxiliary PA, as well as the operation of load modulation, are illustrated in Figures 2.3 and 2.4.

Finally a comparison of the efficiency performance between a DPA and a Class-B PA is presented in Figure 2.5.

Challenges of DPA

While DPA is a widely adopted architecture, its applications remain limited by the intrinsic bandwidth constraints arising from its reliance on narrowband matching structures, for example the $\lambda/4$ impedance inverter in Figure 2.1. Consequently, DPA faces challenges when it comes to widening its operational bandwidths and modifying its topology to extend the high efficiency OBO region, as highlighted in [1, 15, 16, 17, 18, 19].

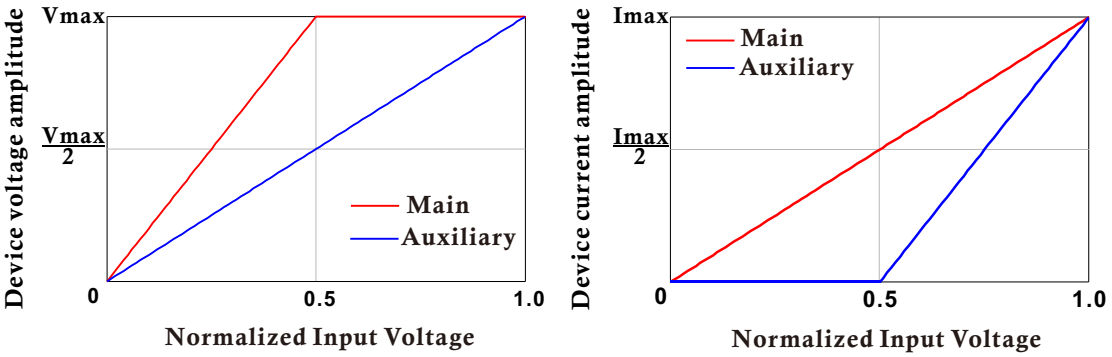

Figure 2.3: Voltage (left) and current (right) behavior versus normalized input voltage of DPA.

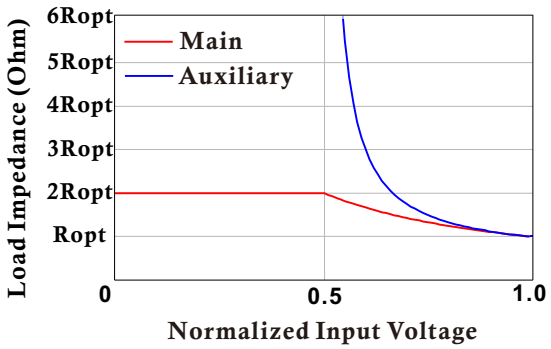

Figure 2.4: Load modulation operation of DPA.

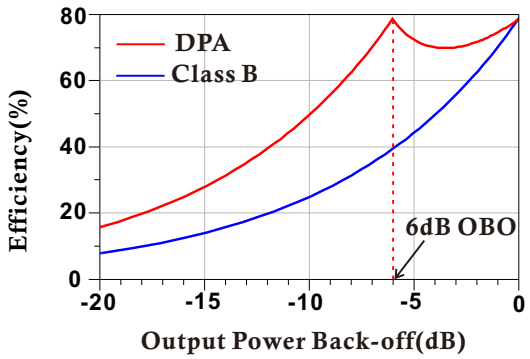

Figure 2.5: Comparison of efficiency performance between DPA and Class-B PA.

2.1.2 LMBA

In recent years a new architecture called Load Modulated Balanced Amplifier (LMBA) was introduced [4], and developed in various versions [5, 6, 7, 8, 20, 21]. Figure 2.6 illustrates the general structure of the LMBA with two inputs, while Figure 2.7 exhibits the LMBA with single RF input.

The two Balanced Power Amplifier (BPA)s are biased in Class-AB and the Carrier Amplifier (CA) is biased in Class-C mode. Figure 2.8 is the simplified model with ideal current generators at the output coupler plane. It also summarizes the LMBA working principle. The Z-parameter matrix of the 3-dB couper is expressed

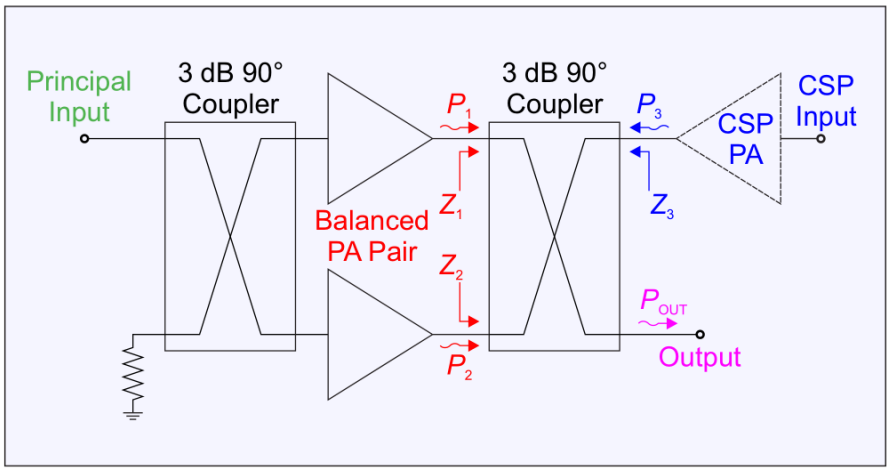

Figure 2.6: Schematic of the dual-input LMBA ([9]).

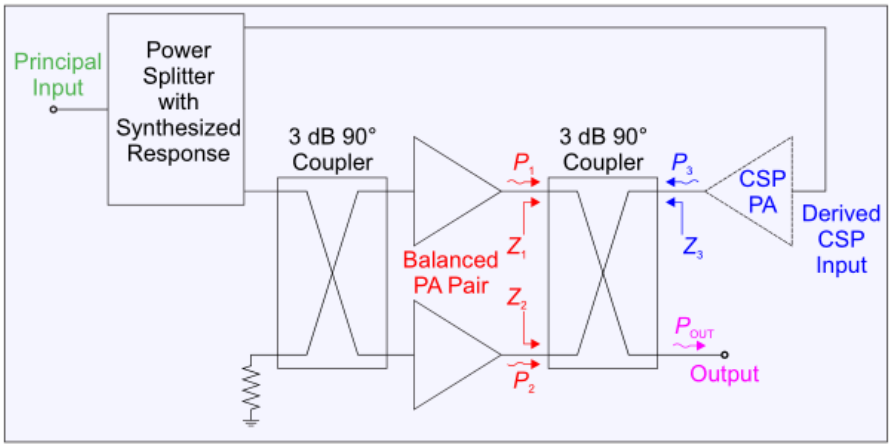

Figure 2.7: Schematic of the single-input LMBA ([9]).

as:

$$\hat{\mathbf{Z}}_{\mathbf{coupler}} = Z_0 \cdot \begin{bmatrix} 0 & 0 & j & -j\sqrt{2} \\ 0 & 0 & -j\sqrt{2} & j \\ j & -j\sqrt{2} & 0 & 0 \\ -j\sqrt{2} & j & 0 & 0 \end{bmatrix}. \tag{2.2}$$

The impedance seen by CA is identical to the coupler characteristic impedance:

$$Z_3 = Z_0. \tag{2.3}$$

It can be derived from (2.2) and (2.3) that for BPAs, they have the same impedance

as:

$$Z_1 = Z_2 = Z_0 \left(1 + \sqrt{2} \cdot \frac{I_C}{I_B}\right). \tag{2.4}$$

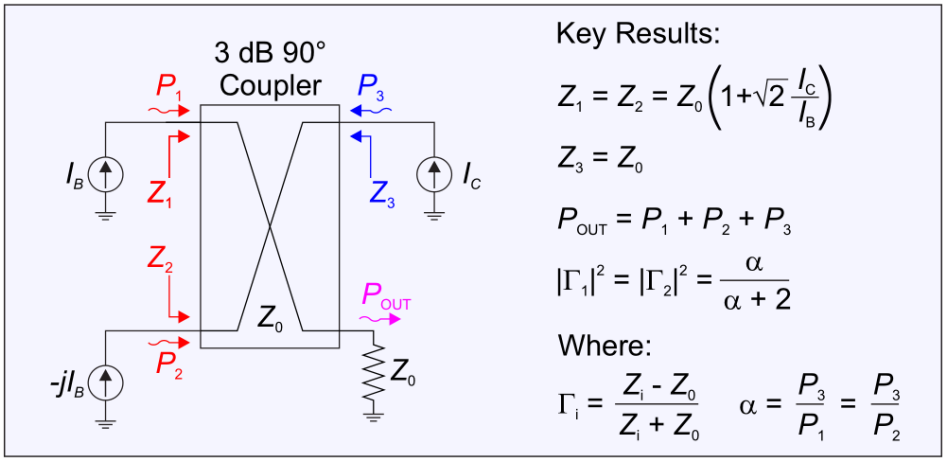

Figure 2.8: LMBA working principle with ideal current generator ([9]).

For small input signals, the BPAs are on and the CA is off. When BPAs reach their saturation, the CA turns on and modulates their load, thus enhancing efficiency and providing additional power to the output load. In Figure 2.6 the CA input can be modified both in amplitude and phase, and in Figure 2.7 only the amplitude of CA can be controlled by having a different power ratio in the the power splitter. In these configuration the OBO is determined by the saturation output power:

$$OBO = \frac{P_{\mathrm{OUT,sat}}}{P_{1,\mathrm{sat}} + P_{2,\mathrm{sat}}}, \tag{2.5}$$

$$P_{\mathrm{OUT,sat}} = P_{1,\mathrm{sat}} + P_{2,\mathrm{sat}} + P_{3,\mathrm{sat}}, \tag{2.6}$$

where the OBO is a positive number in linear scale.

Differently from the DPA, the LMBA offers the advantage of controllable efficiency enhancement in the OBO region by tuning the amplitude and phase of the Carrier amplifier. It also exhibits a potentially wider operational bandwidth.

2.2 SLMBA

In order to obtain a larger OBO, special techniques are investigated and developed in [8, 20]. As it is shown in Figure 2.9, in this case the BPAs are biased in Class-C, while CA is biased in deep Class-AB. In SLMBA configuration, the PA is working in a sequential way, i.e., for small input signals CA is on and BPAs are off, while

for large input signal the CA saturates and BPAs turn on. Since it is biased in the opposite way from the original LMBA, it is also called "Inverted LMBA" [8]. And due to the fact that it works really similar to a DPA, it is also called "Presude-Doherty LMBA" [20]. The most important feature is that there is no load modulation for CA, which is beneficial for wideband operation, but at the same time may be critical for reliability [8].

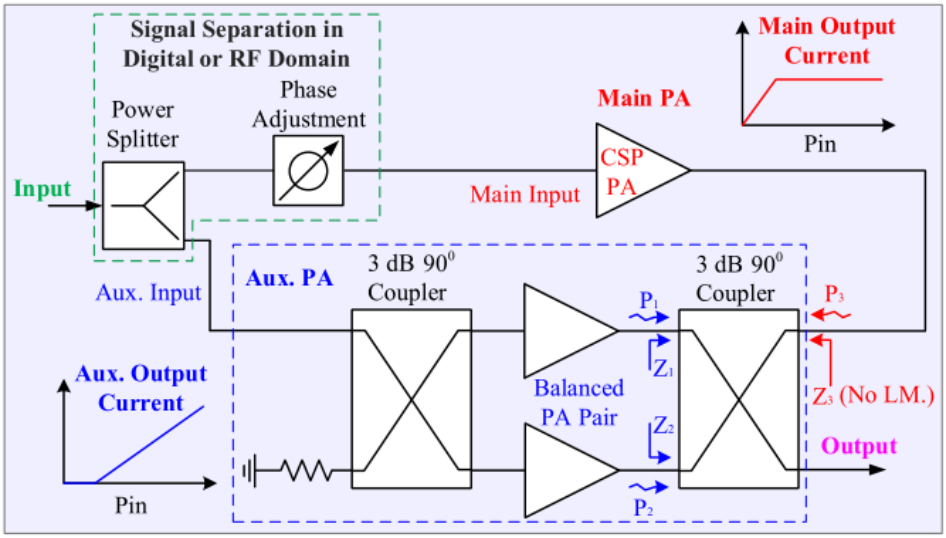

Figure 2.9: Schematic of the SLMBA ([9]).

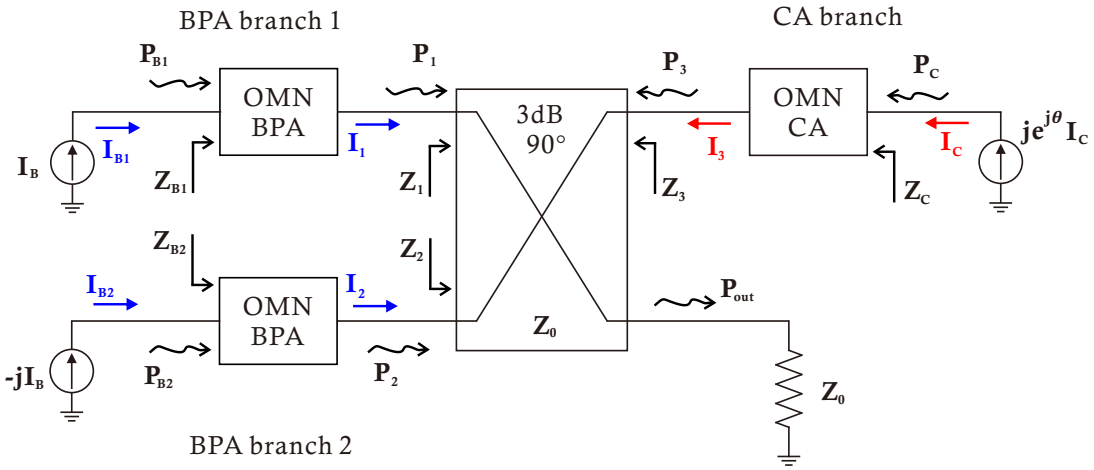

Figure 2.10: SLMBA working principle with ideal current generator.

Differently from the original LMBA (2.5), a larger OBO is determined as:

$$OBO = \frac{P_{\mathrm{OUT,sat}}}{P_{3,\mathrm{sat}}}. \tag{2.7}$$

As it is shown in Figure 2.10, considering also the presence of ideal matching networks between coupler and PAs, the impedance transformation coefficient can be defined as:

$$\gamma_{\mathrm{B}} = \sqrt{\frac{Z_{1,2}}{Z_{\mathrm{B1,2}}}}, \tag{2.8}$$

$$\gamma_{\mathrm{C}} = \sqrt{\frac{Z_3}{Z_{\mathrm{C}}}}. \tag{2.9}$$

Since the OMNs are lossless, based on conservation of energy it gives:

$$I_{\mathrm{B1,2}} = \gamma_{\mathrm{B}} I_{1,2}, \tag{2.10}$$

$$I_{\mathrm{C}} = \gamma_{\mathrm{C}} I_3. \tag{2.11}$$

From the coupler plane to the current generator plane the saturation load impedance can be expressed as:

$$Z_{\mathrm{B1,sat}} = Z_{\mathrm{B2,sat}} = Z_{\mathrm{B,sat}} = \frac{Z_0}{{\gamma_{\mathrm{B}}}^2}\left(1 + \sqrt{2} \cdot \frac{I_{\mathrm{C,max}}}{I_{\mathrm{B,max}}} \cdot \frac{\gamma_{\mathrm{B}}}{\gamma_{\mathrm{C}}} \cdot e^{j\theta}\right). \tag{2.12}$$

With lossless OMNs, the power dissipation can be expressed as:

$$P_{\mathrm{C,sat}} = P_{3,\mathrm{sat}} = \frac{1}{2}{I_{\mathrm{C,max}}}^2 \cdot Z_{\mathrm{C,sat}}, \tag{2.13}$$

$$P_{\mathrm{B,sat}} = 2 \cdot P_{\mathrm{B1,sat}} = 2 \cdot P_{\mathrm{1,sat}} = 2 \cdot \frac{1}{2}{I_{\mathrm{B,max}}}^2 \cdot Z_{\mathrm{B,sat}}. \tag{2.14}$$

Consider the phase of CA is 0. It can be derived from the above equations (2.6), (2.7), (2.8), (2.9), (2.10), (2.11), (2.12), (2.13) and (2.14) that the saturation power ratio between $P_{\mathrm{B,sat}}$ and $P_{\mathrm{C,sat}}$ are:

$$P_{\mathrm{B,sat}} = (OBO - 1)\, P_{\mathrm{C,sat}}, \tag{2.15}$$

and the current ratio between $I_{\mathrm{B,max}}$ and $I_{\mathrm{C,max}}$ is:

$$I_{\mathrm{B,max}} = \frac{\sqrt{2 \cdot OBO} - \sqrt{2}}{2} \cdot \frac{\gamma_{\mathrm{B}}}{\gamma_{\mathrm{C}}} \cdot I_{\mathrm{C,max}}. \tag{2.16}$$

2.3 SLMBA preliminary simulation with ideal current generators

For a SLMBA with 9-dB OBO, selecting $Z_{\mathrm{B,sat}} = 23\ \Omega$ and $Z_{\mathrm{C,sat}} = 200\ \Omega$, the corresponding γ_{B} and γ_{C} can be determined as 2.137 and 0.5. The current ratio between $I_{\mathrm{B,max}}$ and $I_{\mathrm{C,max}}$ is calculated as 5.496. A preliminary simulation with ideal current generators is performed using ADS software synthesizing the results from theoretical equations, and the circuit is shown in Figure 2.11. The current behavior at both coupler plane and CG plane is shown in Figure 2.12. The load modulation of SLMBA is shown in Figure 2.13, where the CA branch exhibits no load modulation effect. Finally the efficiency performance of SLMBA is compared with DPA and Class-B in Figure 2.14.

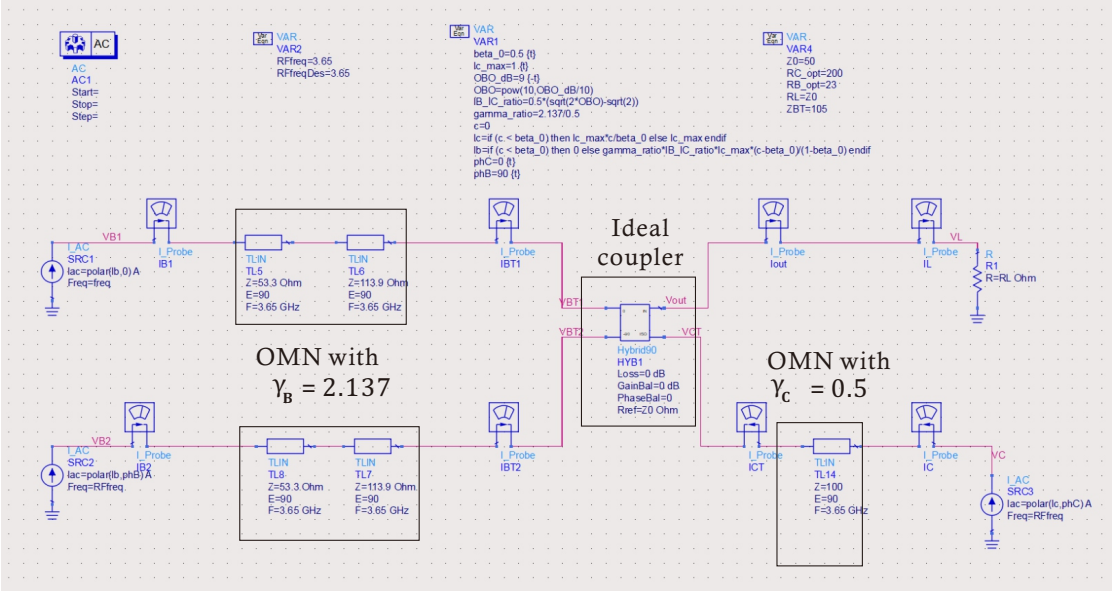

Figure 2.11: SLMBA with ideal current generator.

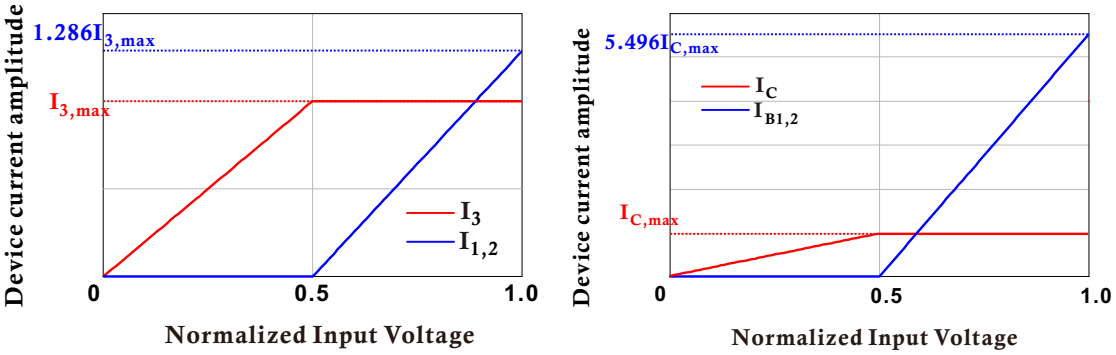

Figure 2.12: SLMBA current behavior at coupler plane (left) and at CG plane (right) versus normalized input voltage.

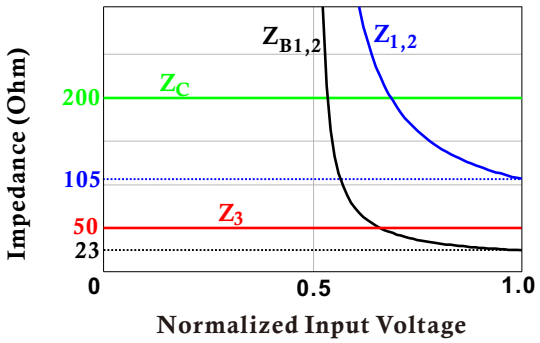

Figure 2.13: Load modulation operation of SLMBA.

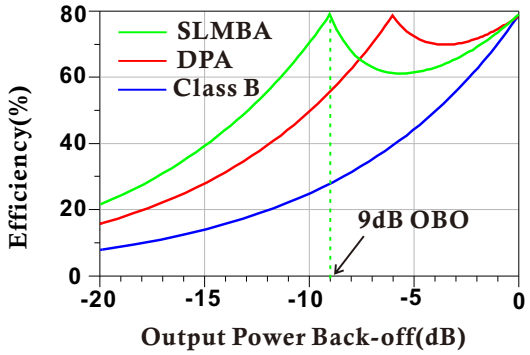

Figure 2.14: Comparison of efficiency performance.

Chapter 3

Circuit Design

The SLMBA design flow is explained in details in this chapter. In this case, the specifications are compatible with the adoption of three identical transistors, which simplifies the prototyping. Therefore, 10-W GaN HEMTs from Wolfspeed Inc. are chosen (CGH40010F). The design begins with the investigation of single device characteristics. Subsequently, the optimum input and output impedance for both the balanced amplifiers and the carrier amplifier are explored, followed by the design of corresponding matching networks in ideal transmission lines. To simplify the circuits and minimize the phase difference between branches, the input matching network is designed to be identical for all transistors. Finally, the design also includes combining and splitting networks for the branch-line coupler, Wilkinson divider with even power splitting ratio, and the phase compensator. The design environment is Keysight Advanced Design System (ADS).

3.1 Device Characteristics

The initial step in PA design begins with evaluating the characteristics of a single-stage transistor. This involves investigating the DC characteristics, stability and loading condition of the transistor. This preliminary analysis guides the design of the stabilization and DC biasing network, as well as the estimation of a simplified linear model for the output parasitic elements of the active device.

3.1.1 DC bias point selection

DC simulations are performed by sweeping the bias voltages at the drain and gate terminal of the transistor with ideal biasing networks. The output characteristic is presented in Figure 3.1, which illustrates that the knee voltage is 5V and the breakdown voltage is 140V, approximately. With the help of the datasheet

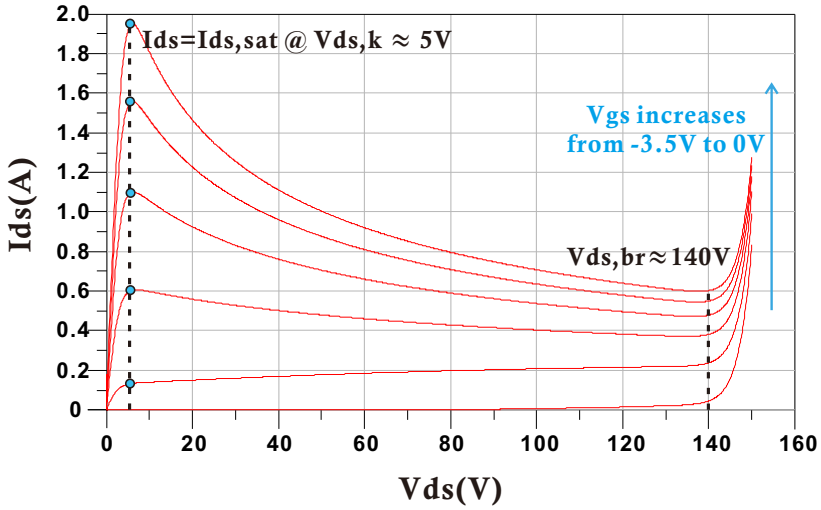

Figure 3.1: Output characteristic of the packaged transistor CGH40010F.

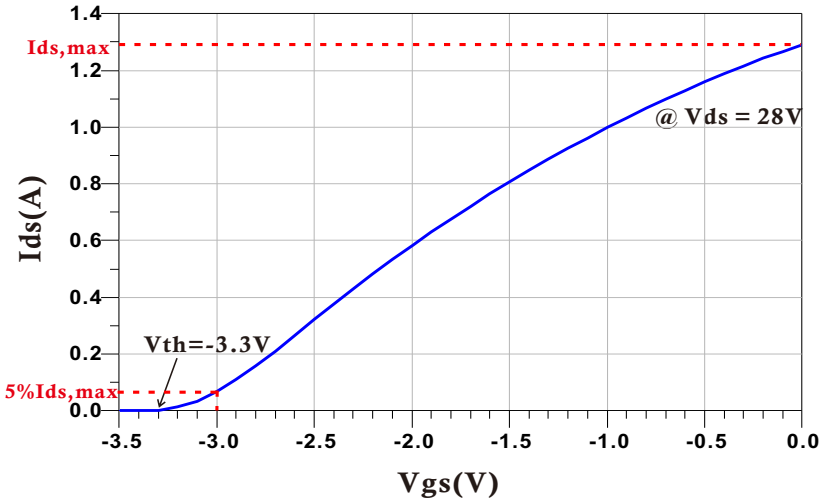

Figure 3.2: Transfer characteristic at $V_{\mathrm{ds}} = 28\mathrm{V}$.

provided by Wolfspeed, a reasonable drain bias is selected to be 28V for high-power applications. Hence the corresponding transfer characteristic is obtained in Figure 3.2. Near the threshold voltage of -3.3V, it can be observed that the turn-on phase of the transistor is not ideal. A possible solution for determining the deep Class-AB quiescent point involves setting the drain current to reach 5% of the maximum current $I_{\mathrm{ds,max}}$. As a result, the gate bias is -3V.

3.1.2 Stabilization and DC biasing network

Active devices are typically not unconditionally stable at all frequencies and in all operating conditions. It is common to enforce either unconditional or, at least, conditional stability to make the amplifier more robust to noise and oscillations caused by other disturbances. Some possible stabilization networks are shown in Figure 3.3 [13]. The one adopted for this design in that of Figure 3.4. PAs commonly adopt input stabilization and avoid the feedback and output networks, which would have a strong impact on the output power and efficiency. The network was optimized with the primary goal of ensuring stability across the entire bandwidth and achieving a gain high and flat within the operational band.

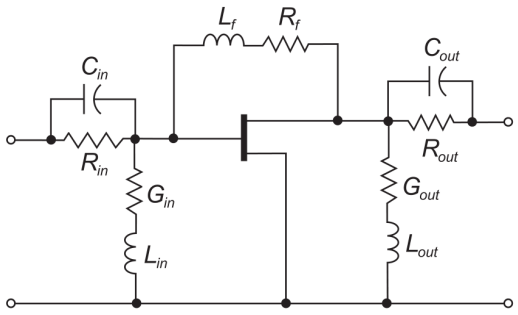

Figure 3.3: Typical solution for stabilizing a transistor ([13]).

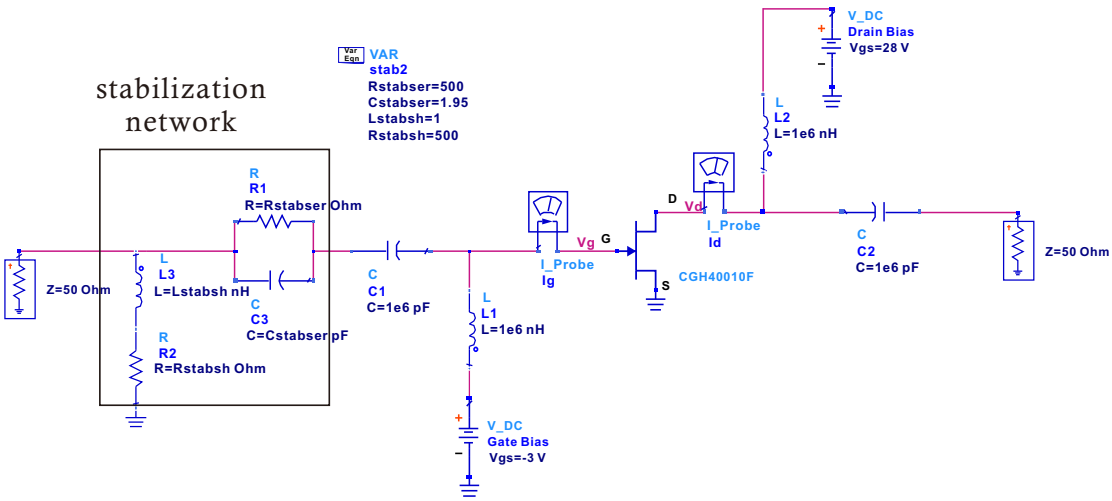

Figure 3.4: Stabilization circuit with ideal biasing network.

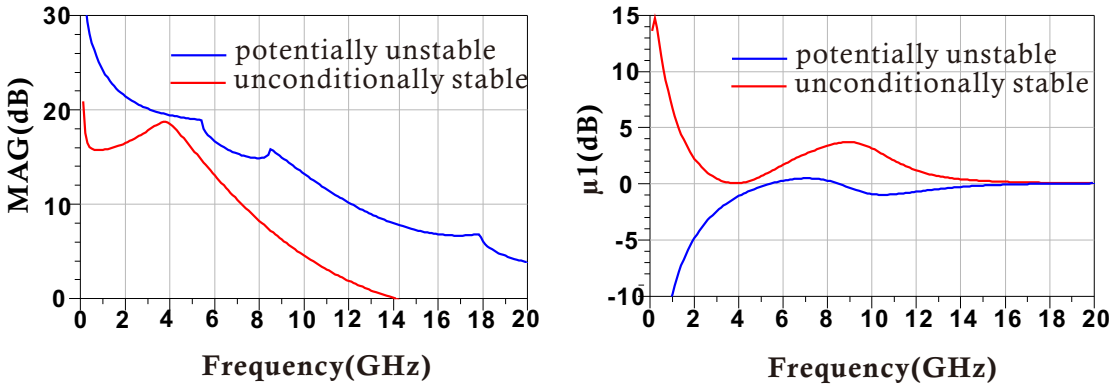

Figure 3.5: MAG (left) and $\mu 1$ (right) for the device before (blue) and after (red) the stabilization over 0 to 20 GHz bandwidth with ideal biasing network.

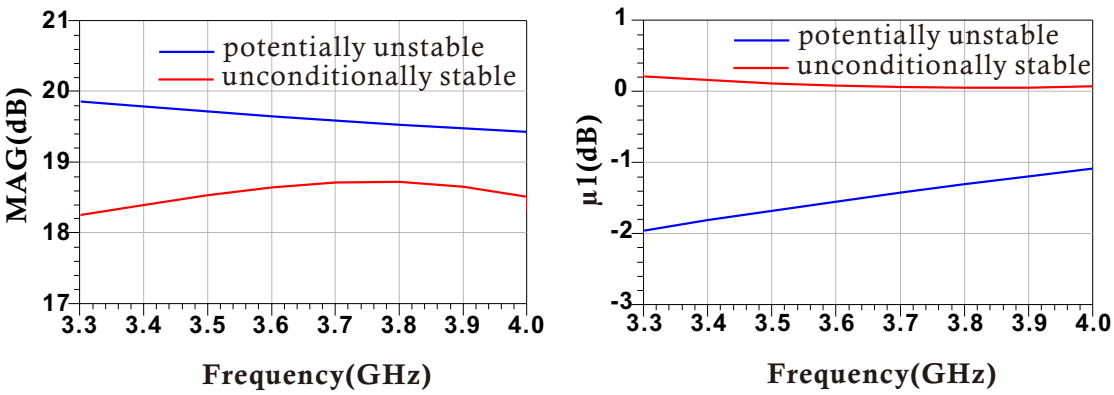

Figure 3.6: MAG (left) and $\mu 1$ (right) for the device before (blue) and after (red) the stabilization in the operational bandwidth with ideal biasing network.

The investigation results of device stability with ideal biasing networks are shown in Figure 3.5 and 3.6. Without the stabilization network, the active device is potentially unstable in the operational bandwidth from 3.3GHz to 4GHz, as it is illustrated in blue curves. It means that oscillations might occur and saturate the amplifier. After applying the stabilization network, the results are illustrated by the red curve in Figure 3.5 and 3.6. The μ parameter is larger than 1 (or 0dB), which indicates that the active device is unconditionally stable all over the bandwidth from 0 to 20 GHz. Additionally, it achieves a flat gain above 18 dB in the working bandwidth.

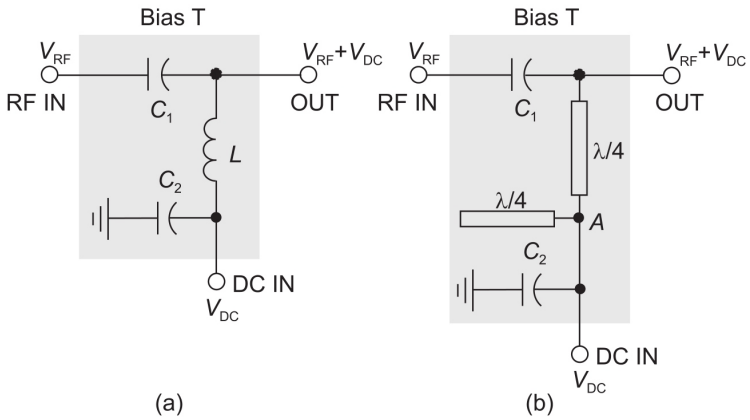

Figure 3.7: (a) Lumped parameter and (b) distributed parameter examples of realistic biasing network ([13]).

The ideal bias tee, highlighted in Figure 1.3, is realized by a series capacitor and a shunt inductor only. In the real-case scenario, the DC biasing network is designed with the specific topology to ensure effective decoupling between DC and RF signals [13]. Figure 3.7 demonstrates two examples of both lumped parameter and distributed parameter bias tees. To address the impact of the input biasing network on device stability, biasing networks were separately designed and optimized for the input and output stages. After several attempts at optimization, the implemented structure is shown in Figure 3.8, where the DC input path consists of four parallel capacitor branches with capacitance values of 3.3 pF, 100 pF, 2.2 nF, and 22 nF respectively. Moreover, under the consideration of limiting the gate current and protecting the active device, especially for CA branch which would be pushed into deep saturation, the two stabilization resistors with values of 680 Ω and 3.9 kΩ are used. The stability analysis results for this integrated structure are displayed in Figure 3.9 and 3.10. The stability conditions for both in-band and out-of-band operations are ensured, with the MAG still remaining between 18 dB and 19 dB within the operation band.

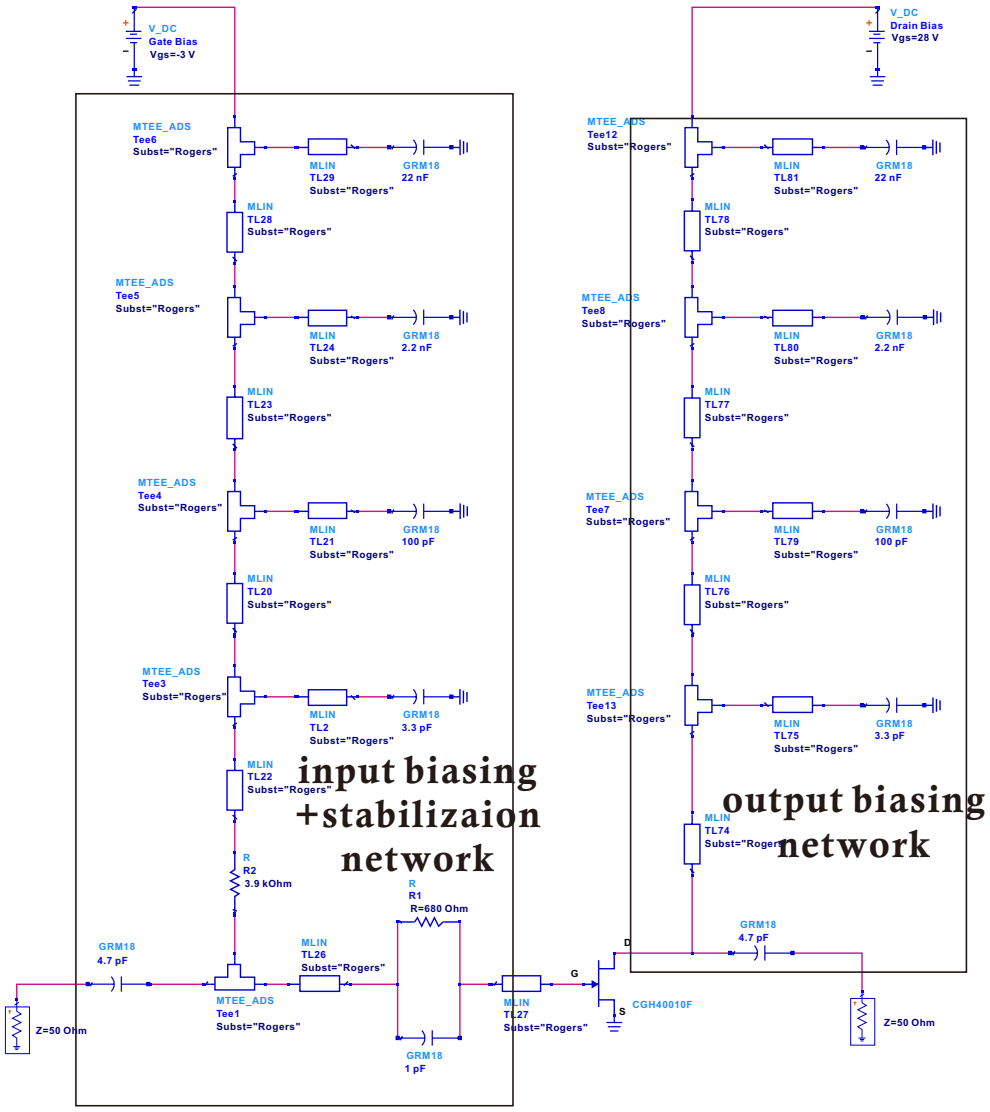

Figure 3.8: Stabilization circuit with real biasing network.

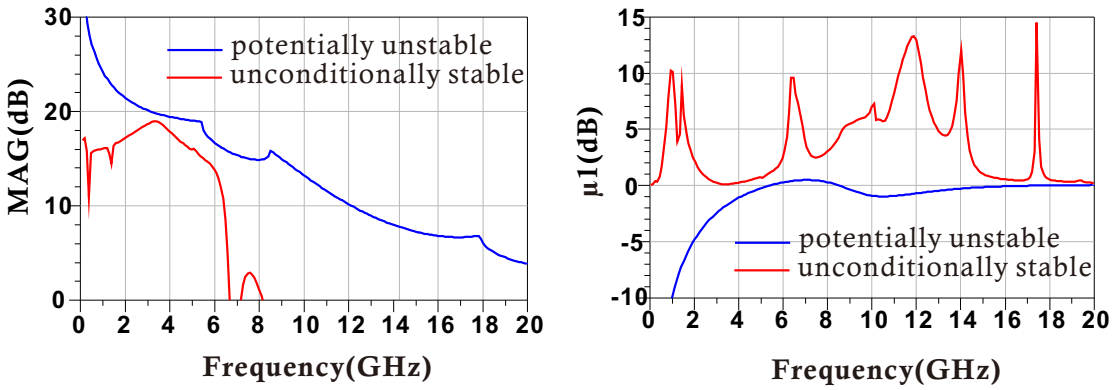

Figure 3.9: MAG (left) and $\mu 1$ (right) for the device before (blue) and after (red) the stabilization over 0 to 20 GHz bandwidth with real biasing network.

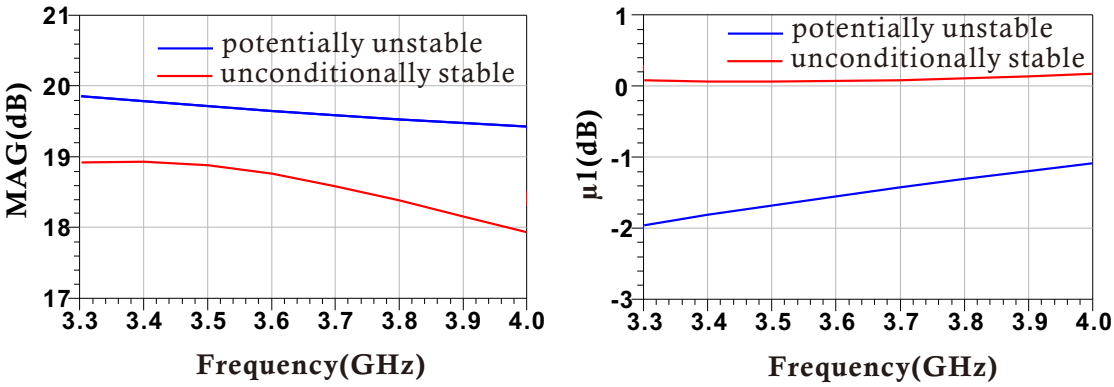

Figure 3.10: MAG (left) and $\mu 1$ (right) for the device before (blue) and after (red) the stabilization in the operational bandwidth with real biasing network.

3.1.3 Output load determination

As illustrated in the previous chapter, in order to reach the desired OBO performance the saturation power of CA should be compatibly small. This indicates the fact that the load impedance for the CA device must differ from that of the BPA. To investigate the saturation power and the load impedance at intrinsic current generator plane of the active device, the one-tone harmonic balance (HB1) simulations are initially performed for the single-ended PA at center frequency 3.65 GHz.

2-LC Parasitic Model

The parasitic model of the active device is examined to facilitate the design of appropriate matching networks. Based on the analysis of the transistor model CGH40010F, a 2-LC parasitic model is constructed and presented in Figure 3.11 [22, 23, 20]. The schematic of HB1 simulation is shown in Figure 3.12, where 2-LC parasitic model is implied. The transistor model itself provides information about the intrinsic current (idi) and voltage (vdsi) at the CG plane. Then the 2-LC model is optimized and evaluated under large signal conditions in HB1 simulation, which allows for the re-obtaining of the fundamental drain current at the intrinsic CG plane. The values of the parasitic capacitance and inductance are C_{out1}=0.68 pF, C_{out2}=0.94 pF, L_{out1}=0.34 nH and L_{out2}=0.54 nH, as reported in Figure 3.12.

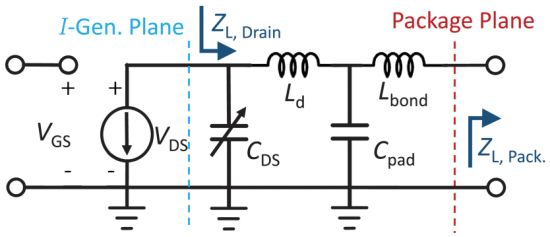

Figure 3.11: 2-LC parasitic model of CGH40010F ([20]).

Balanced PA

From the analysis in the previous chapter, it is straightforward that BPA devices need to provide a relatively large saturation power. Firstly, a source-pull analysis is performed to identify the optimum input impedance. As it is shown by red curve in Figure 3.14, P_{IN} is effectively matched with P_{avs}. Secondly, a load-pull analysis is performed to study the saturation power and determine the corresponding real load at the CG plane. After several tuning processes, the maximum saturation

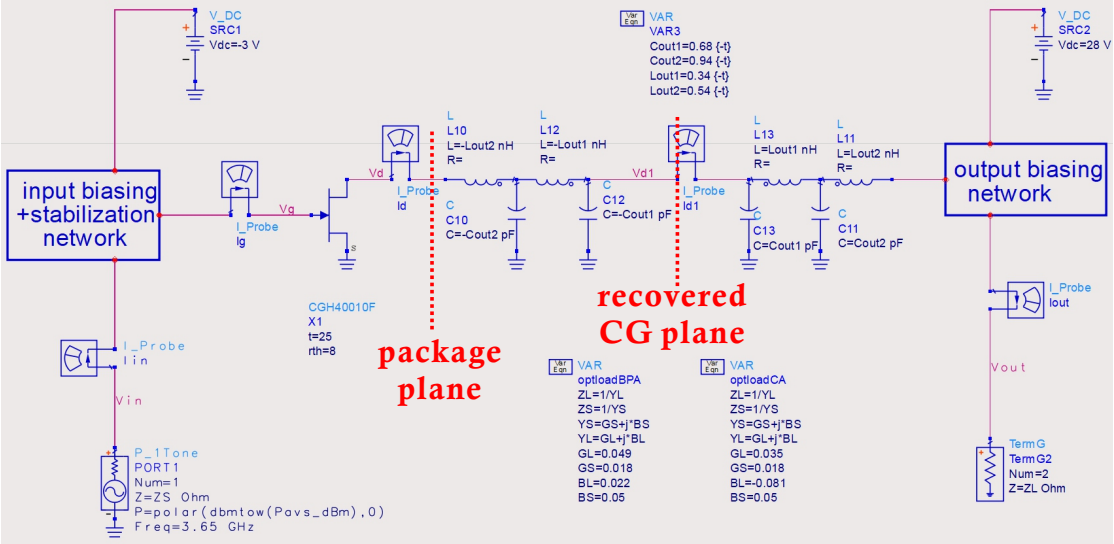

Figure 3.12: Schematic of HB1 simulation circuit with 2-LC parasitic model.

power of the device is determined to be 41dBm, as reported in Figure 3.14. Based on this point, the optimum real load at the BPA's intrinsic plane is selected to be $R_{\mathrm{B,opt}} = 23\ \Omega$, as shown in Figure 3.15. It is linked to achieving both the maximum saturation power and the maximum saturation current.

Carrier PA

Since the transistors in both branches are identical, for CA branch which needs to provide a lower power, the transistor should have a larger load at the CG plane. From equation (2.7), it can be determined that the $P_{\mathrm{C,sat}}$ should be 8.4 dB less than $P_{\mathrm{B,sat}}$. However, in the HB1 simulation, the presence of a large real load at intrinsic plane would cause the transistor to saturate early. This not only decreases the gain and efficiency of the CA device, but also increases the complexity of the matching network design. To mitigate these issues, a suitable load must be re-evaluated. Hence, the input impedance of the CA device is maintained the same as that of the BPA. As it is shown by red curve in Figure 3.14, P_{IN} is still effectively matched with P_{avs}. Meanwhile the similar load-pull analysis is performed. After several tuning processes, the saturation power of CA device is selected to be 35.7 dBm with a maximum PAE greater that 50%, and the optimum real load at the CA intrinsic plane is chosen to be $R_{\mathrm{C,opt}} = 165\ \Omega$. The results are shown in Figure 3.13, 3.14, 3.15 and 3.16.

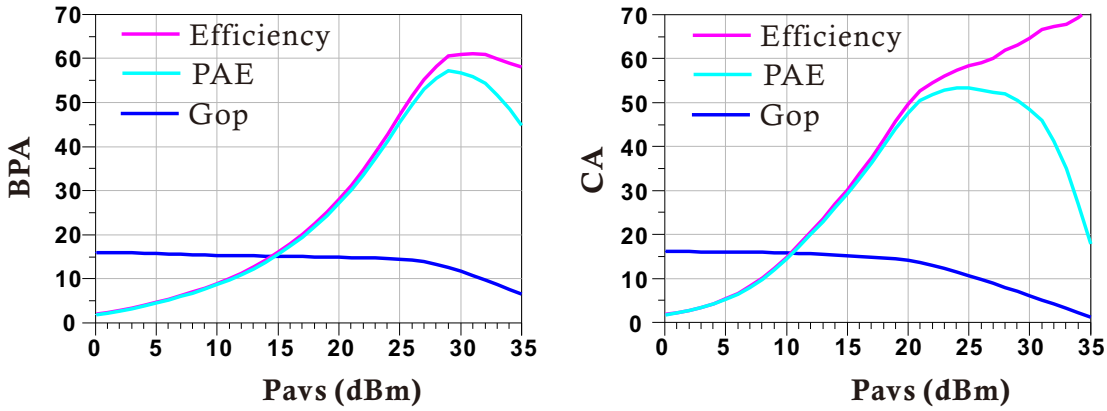

Figure 3.13: Efficiency and gain performance for single-ended transistor with BPA load (letf) and CA load (right).

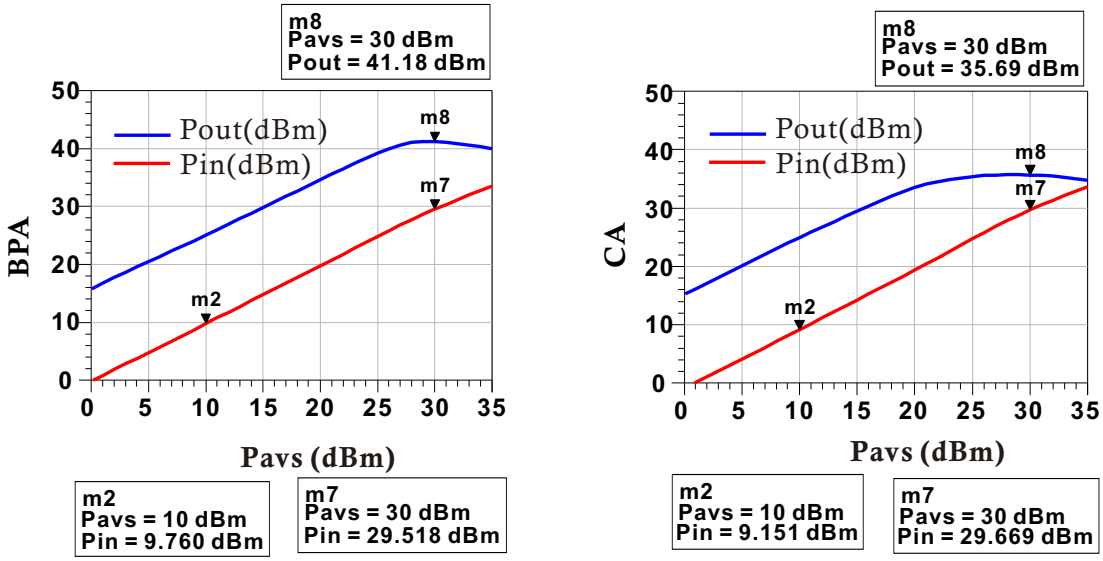

Figure 3.14: Input and output power for single-ended transistor with BPA load (letf) and CA load (right).

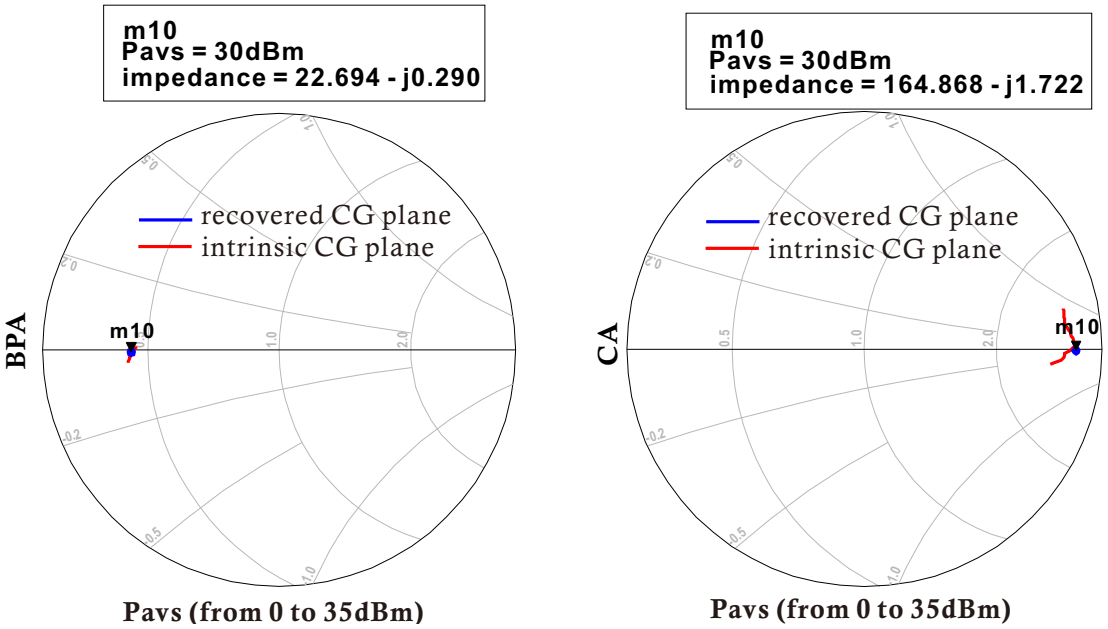

Figure 3.15: Optimum load of BPA (left) and CA (right) at CG plane.

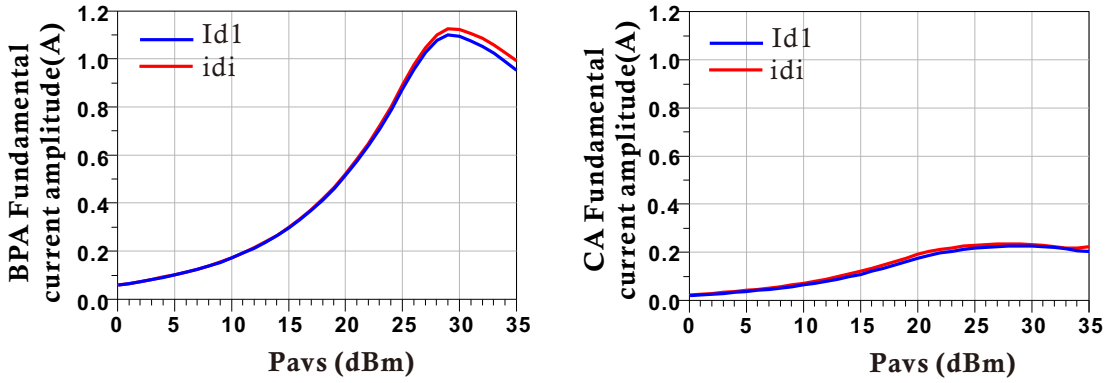

Figure 3.16: Fundamental current amplitude of BPA (left) and CA (right) at CG plane.

3.2 Matching networks

The impedance matching networks are one of the most critical sections in PA design. They have a direct impact on maximizing the power transfer and maintaining the quality of signals through out the system. Thus, fine-tuning and proper optimizations are essential.

3.2.1 Output matching networks

As it is determined by the previous chapter, the output matching network will transfer the certain load impedance at the coupler plane into the optimum load impedance at the CG plane. After some optimization loop, the OMNs of the both BPA and CA branches are settled to have a wide impedance matching bandwidth and a similar phase transition characteristic.

BPA branch

The OMN of BPA branch is designed as Figure 3.17. It consists of lines and stubs. It transfer Z_{BT} into R_{optB}. The S-parameter behavior of the BPA's OMN is shown in Figure 3.18.

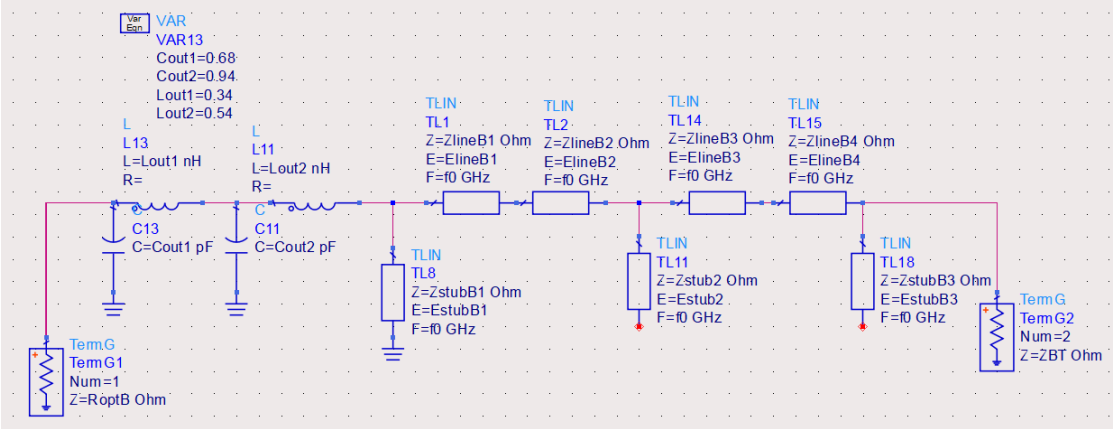

Figure 3.17: OMN of BPA branch in ideal transmission lines.

CA branch

The OMN of CA branch is designed as Figure 3.19. It transfer Z_{CT} into R_{optC}. The S-parameter of the CA's OMN is shown in Figure 3.20.

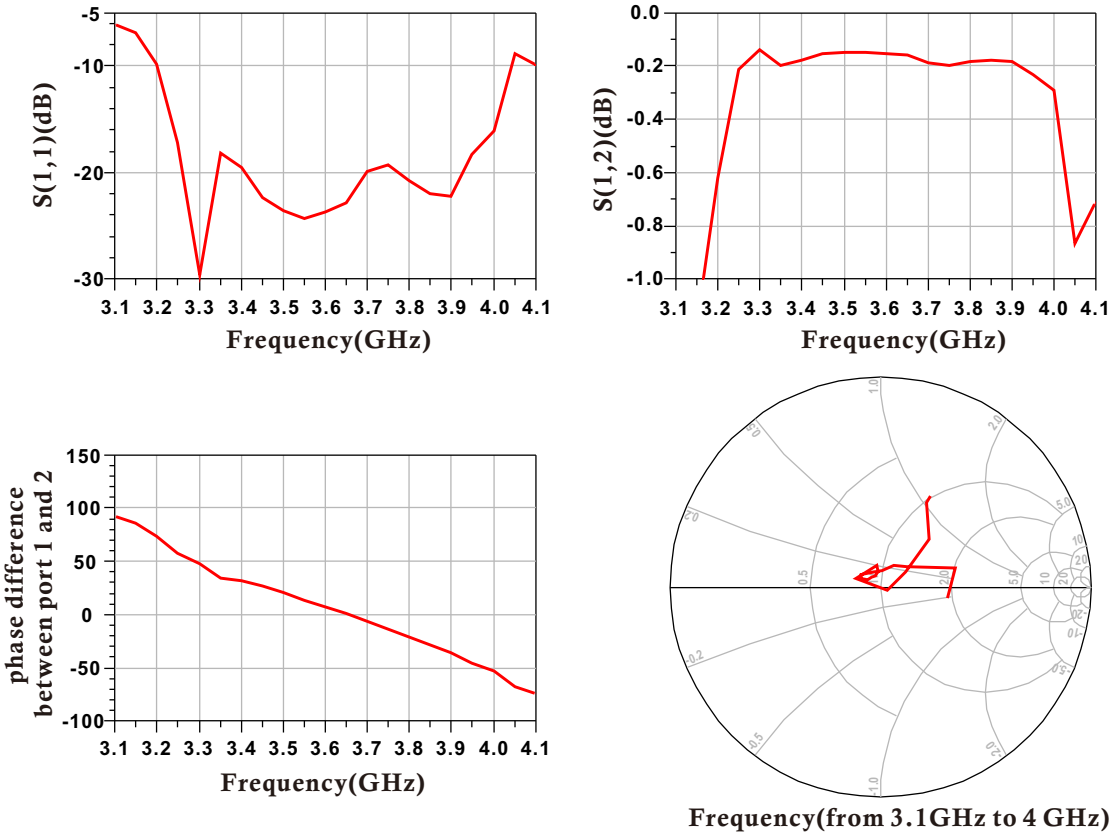

Figure 3.18: S-parameter behavior of the BPA's OMN.

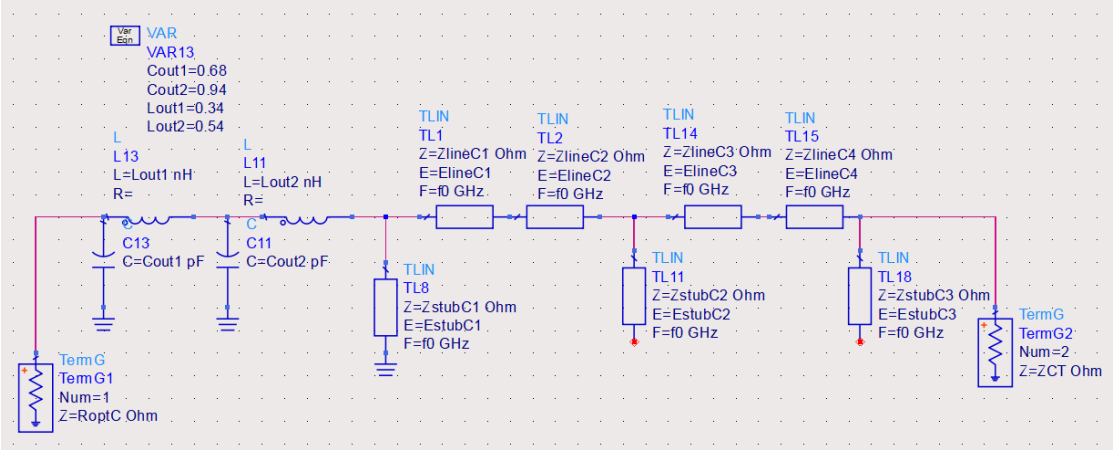

Figure 3.19: OMN of CA branch in ideal transmission lines.

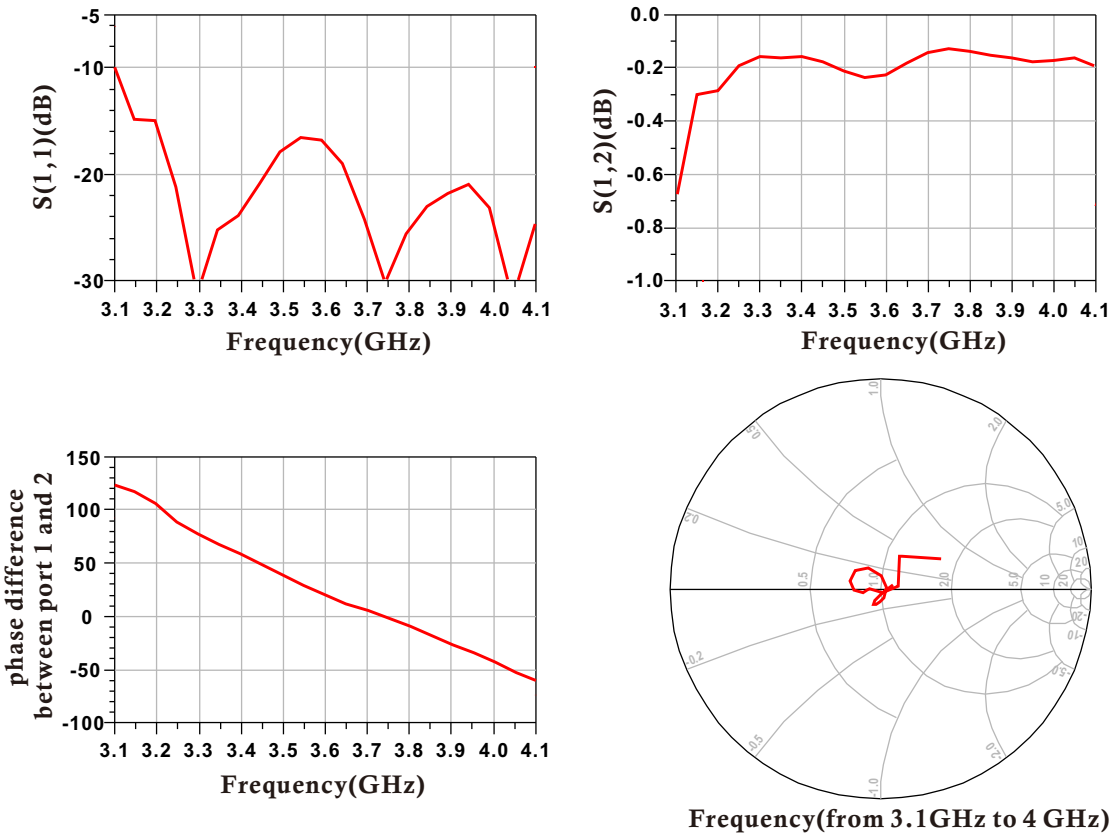

Figure 3.20: S-parameter behavior of the CA's OMN.

3.2.2 Input matching network

In order to ensure a consistent phase difference between the two branches and simplify the design process, the same IMNs are employed for all transistors. The IMN is designed to maintain a wider bandwidth than the target working bandwidth, providing some extra margin for potential frequency shift issues in the future work. The optimized structure and the S-parameter results are shown in Figure 3.21 and 3.22, respectively.

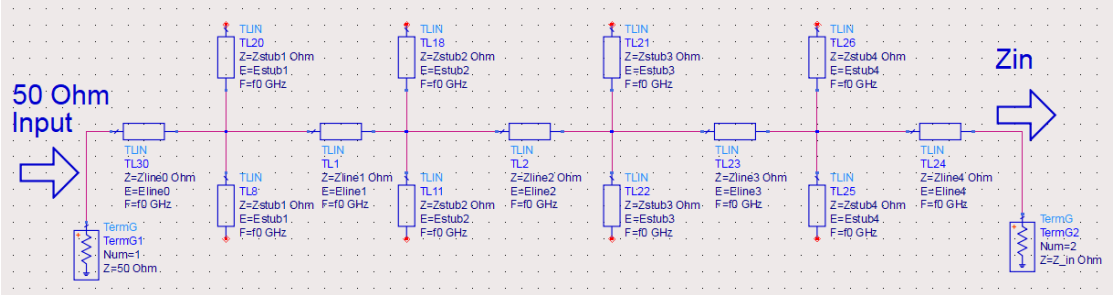

Figure 3.21: Schematic of the IMN in ideal transmission line.

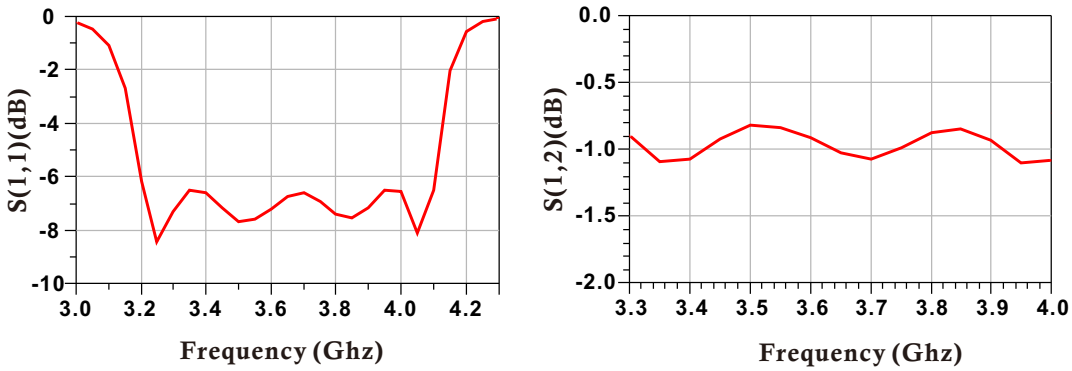

Figure 3.22: S-parameter behavior of the IMN.

3.3 Combining and splitting networks

3.3.1 3-dB 90° Branch-line Coupler

The 3-dB 90° branch-line coupler is a four-port microwave device which is widely used for power splitting and combining applications. It is specially designed to split an input signal into two equal output signals with a 90° phase shift between them, while ensuring also good isolation between the ports. The equal power division results in a 3-dB power loss from the input to each of the outputs.

Two identical branch-line couplers are used at the input and output of the balanced pair, as shown in Figure 2.9.

The branch-line is in its basic single section form is rather narrowband. There are other ways of implementing 3-dB 90° couplers, such as the Lange one [13], but they are not suitable for the selected implementation. Therefore, for wideband operation, a specific configuration is introduced. It consists of two quarter-wavelength transmission line sections connected in series. The two sections are symmetrically arranged. The optimum design has already been well discussed in [24]. Therefore a 2-section Butterworth 3-dB coupler is selected and implemented in Figure 3.23. It's S-parameter response is shown in Figure 3.24.

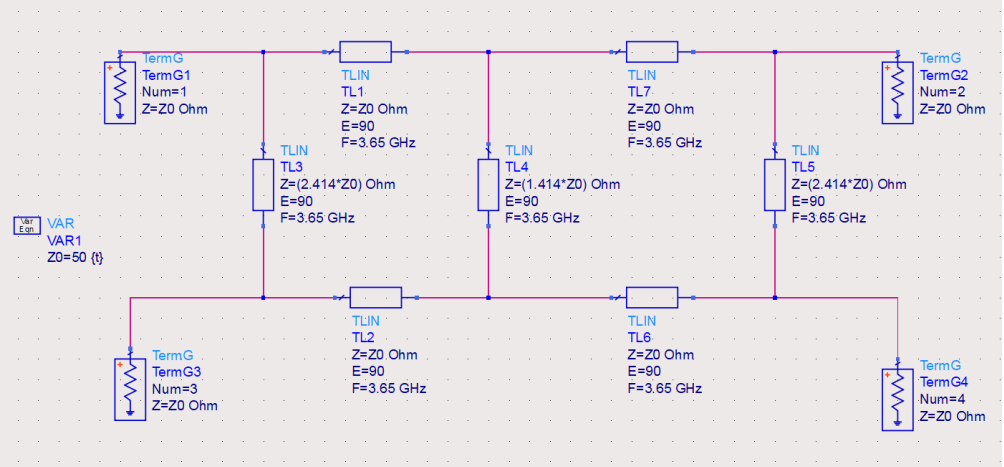

Figure 3.23: Schematic of the 2 section 3-dB branch-line coupler.

3.3.2 Wilkinson Power Divider

The Wilkinson power divider is a passive device used for power splitting applications. It is designed to divide an input signal equally between two output ports while providing good isolation between the ports. The two output signals are in phase.

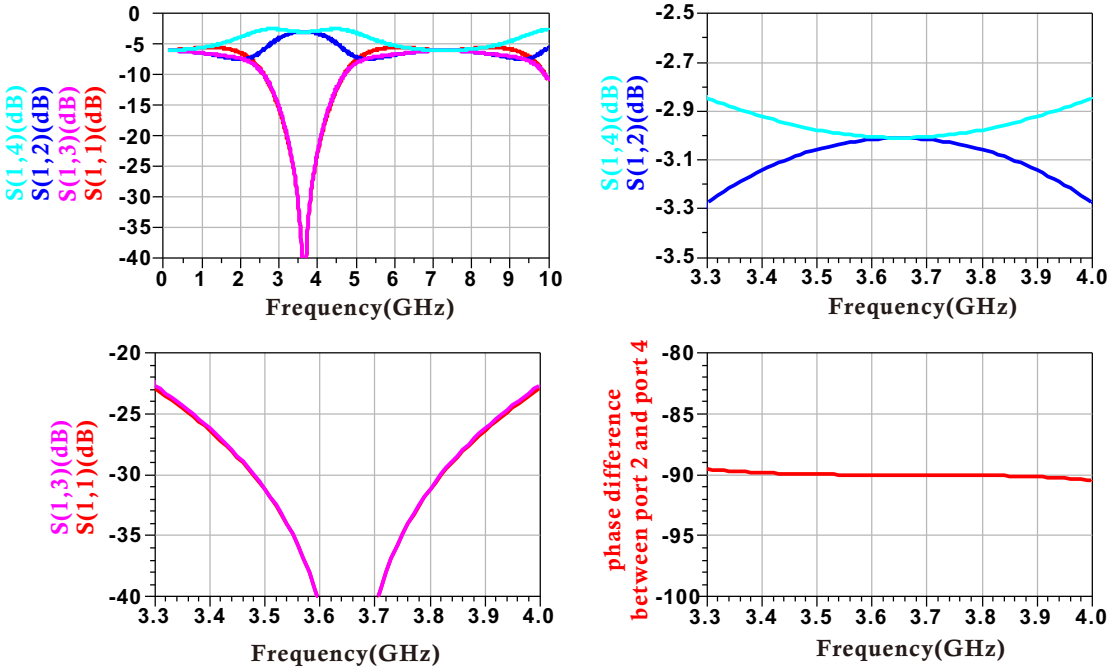

Figure 3.24: S-parameter performance of the 3-dB coupler.

The Wilkinson divider is used at the input of the SLMBA, as shown in Figure 2.9.

For wideband operation, the 2-section Wilkinson divider is developed. It consists of two impedance transformation sections connected in parallel. Each section is typically a quarter-wavelength transmission line, with characteristic impedances designed to achieve the 3-dB power division. The input signal is applied at the common node of the two sections, and the outputs are taken from the other ends. The optimum design for widebande behavior has already been well discussed in [25]. Therefore, a 2-section Wilkinson divider is selected and the circuit is shown in Figure 3.25. The S-parameter characteristic is shown in Figure 3.26.

3.4 Phase compensator

For SLMBA, the phase difference between CA and BPA branches is crucial since it affects greatly the load modulation operation and the combination of the output power. By applying a phase compensator, the phase difference between the BPA and CA branches can be accurately controlled, leading to improved performance and signal combination at the PA output.

In Figure 2.9, the phase compensator is located on the CA branch after the power splitter.

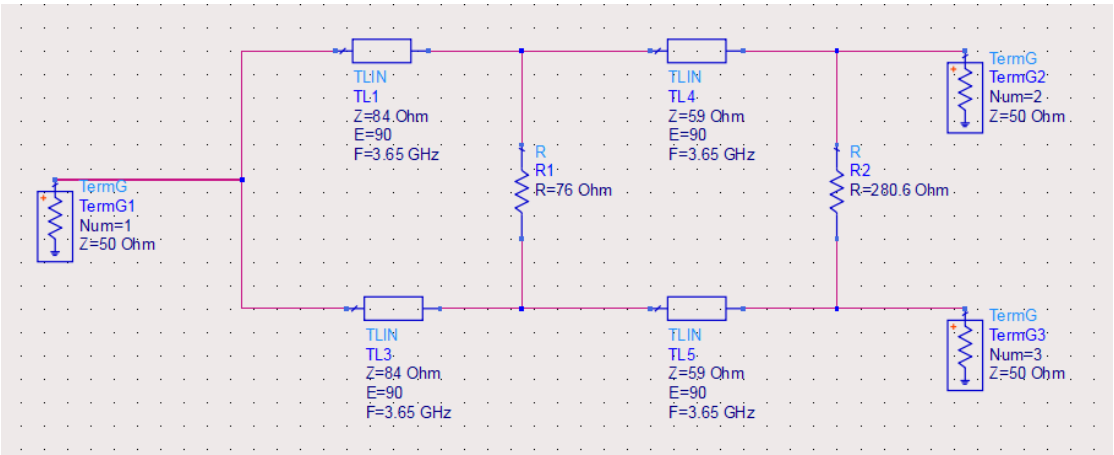

Figure 3.25: Schematic of the 2 section Wilkinson divider.

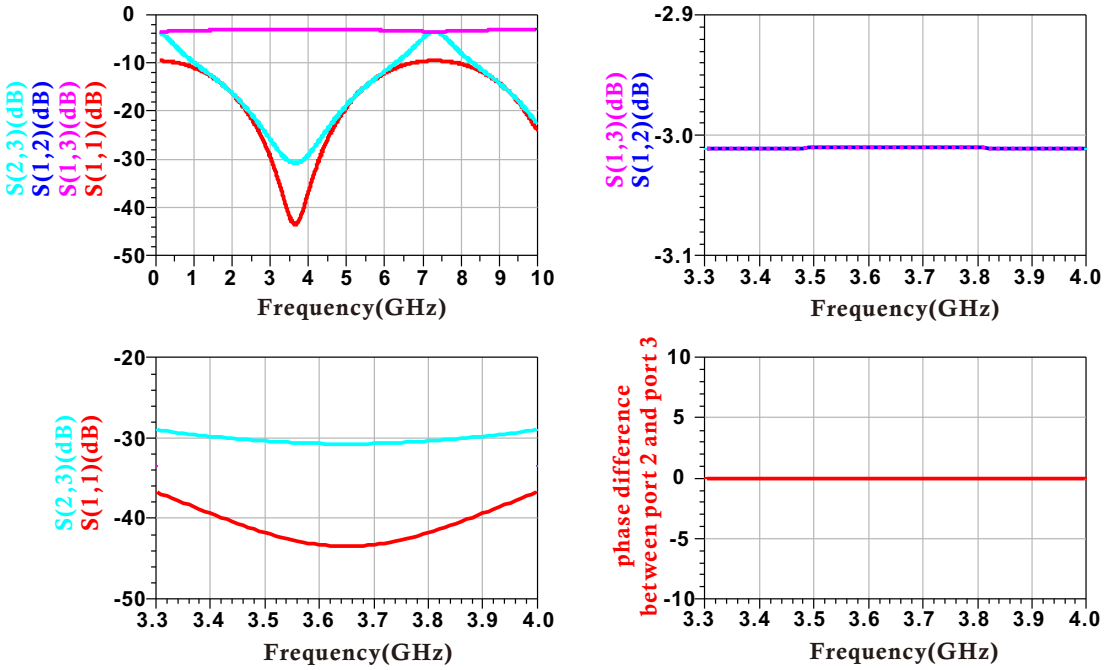

Figure 3.26: S-parameter performance of the Wilkinson divider.

As shown in Figure 3.27, the SLMBA circuit is simulated with two ideal input and the optimum phase different is determined frequency by frequency. According to the actual phase relationship, it is determined that the phase compensator for this design should be located on the BPA branch after the power splitter. Therefore, a 4^{th} order filter match at 50 Ω was implemented. The circuit of the phase compensator is show in Figure 3.28 and the S-parameter behavior of it is displayed in Figure 3.29.

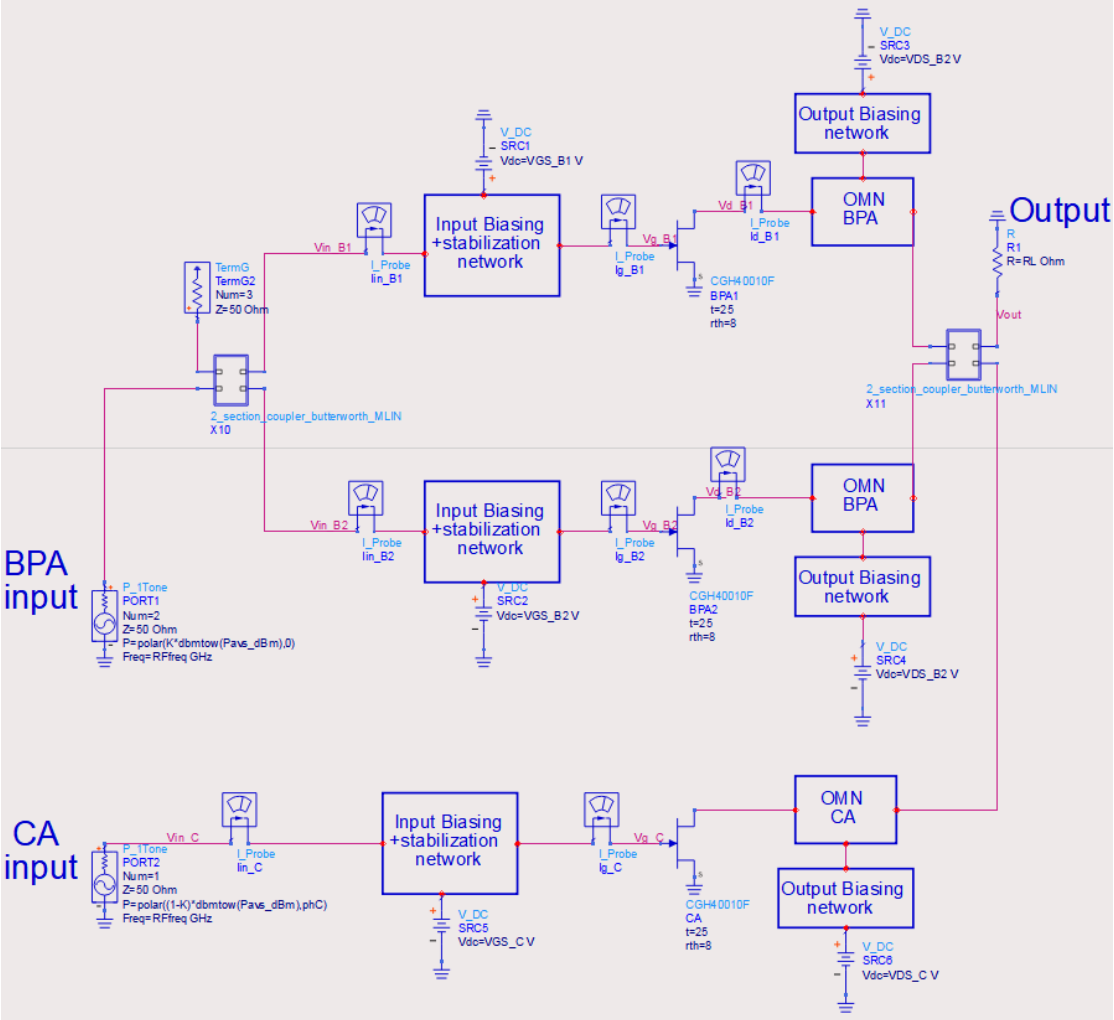

Figure 3.27: Schematic of the SLMBA with two input ports.

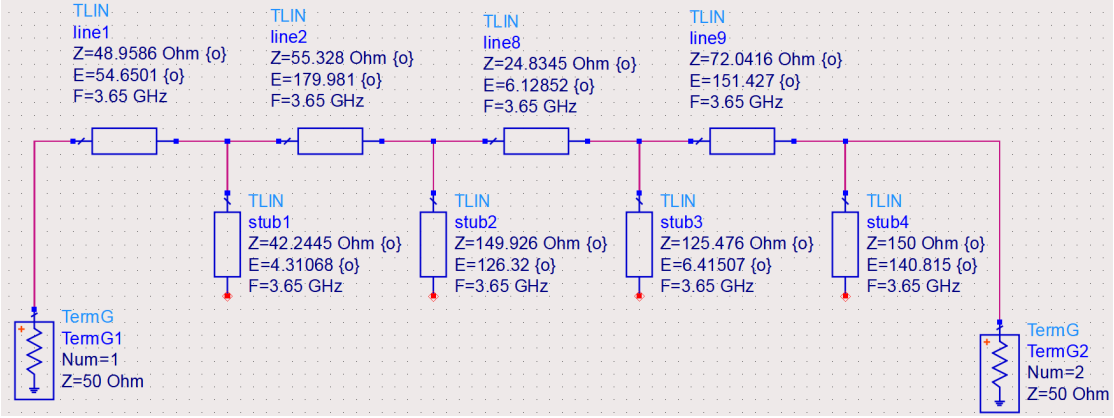

Figure 3.28: Schematic of the phase compensator.

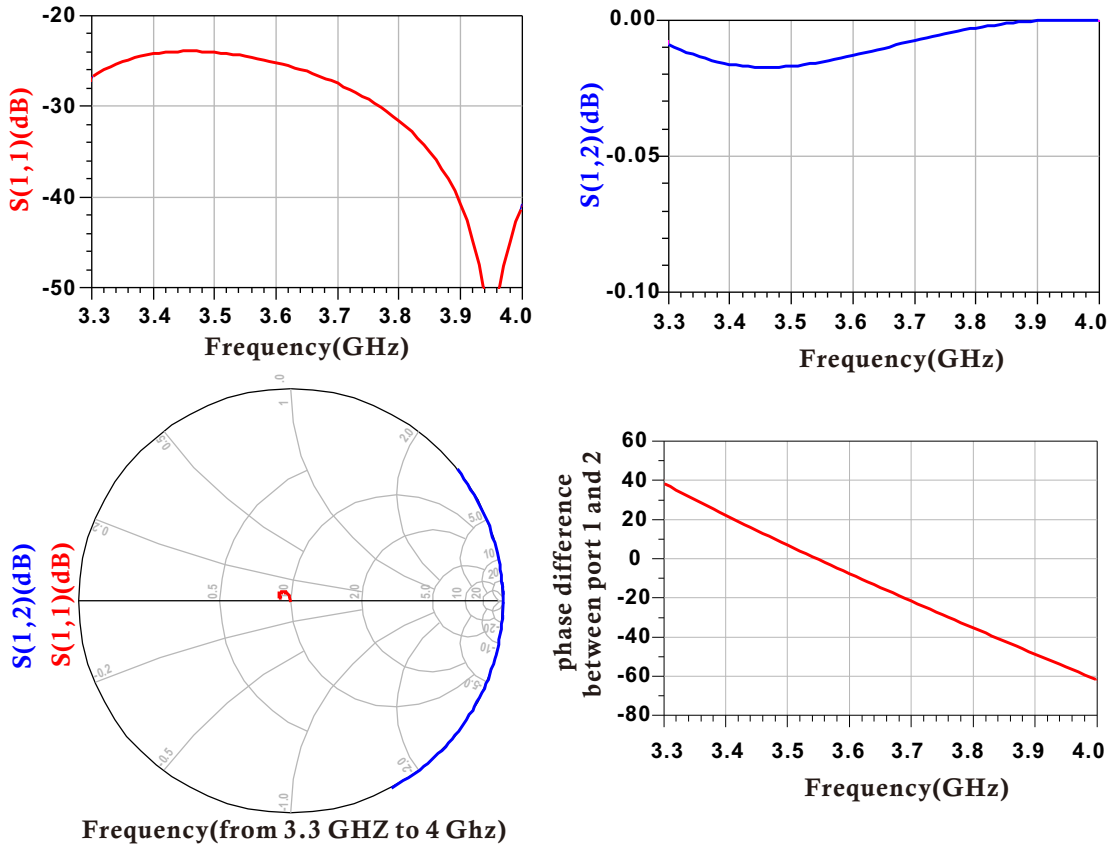

Figure 3.29: S-parameter performance of the phase compensator.

Chapter 4

Circuit Implementation and Layout Planning

The hybrid circuit is constructed on a Roger4350B substrate with a relative dielectric constant of 3.66. To fabricate the SLMBA, several modifications were made to ensure a realistic layout that meets the physical constraints. Translated from the circuits with ideal transmission lines, the microstrip circuits were optimized to have a compatible width and length among lines and stubs, and to align with the ideal performance as close as possible. Additionally, the electromagnetic (EM) simulations were set up to accurately evaluate the practical performance.

4.1 Microstrip implementation

The microstrip is a quasi-TEM transmission line made by two parallel metal conductors and a layer of dielectric substrate in between, as illustrated in Figure 4.1 [13].

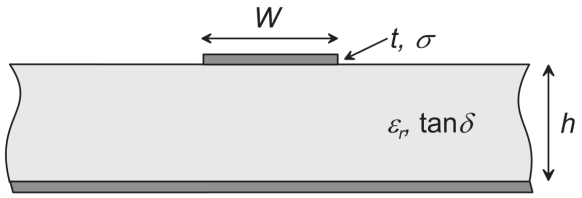

Figure 4.1: Cross-section of a microstrip ([13]).

The substrate material is Roger4350B with the relative dielectric constant ε_{r} = 3.66, the tangent loss tanδ = 0.0037 and the thickness h = 0.76 mm, while the conductor material is copper with the conductivity $\sigma = 5.9 \times 10^7\,\mathrm{S/m}$ and the

thickness $t = 35$ μm. The translation of the ideal transmission line design into the microstrip implementation is carried out initially with the help of the Microstrip Calculator embedded in ADS, and an optimization phase follows.

4.2 Biasing networks

4.2.1 Input biasing and stabilization network

Based on the circuit shown in Figure 3.8, the input biasing and stabilization networks were re-optimized to accommodate the actual connection interfaces with real components. The width of the line in DC path is limited by the direct DC connection to the supply, and port ends needs to be wide enough for soldering the resistors, capacitors and transistors. After several optimizations, the adopted circuit and the layout are presented in Figure 4.2.

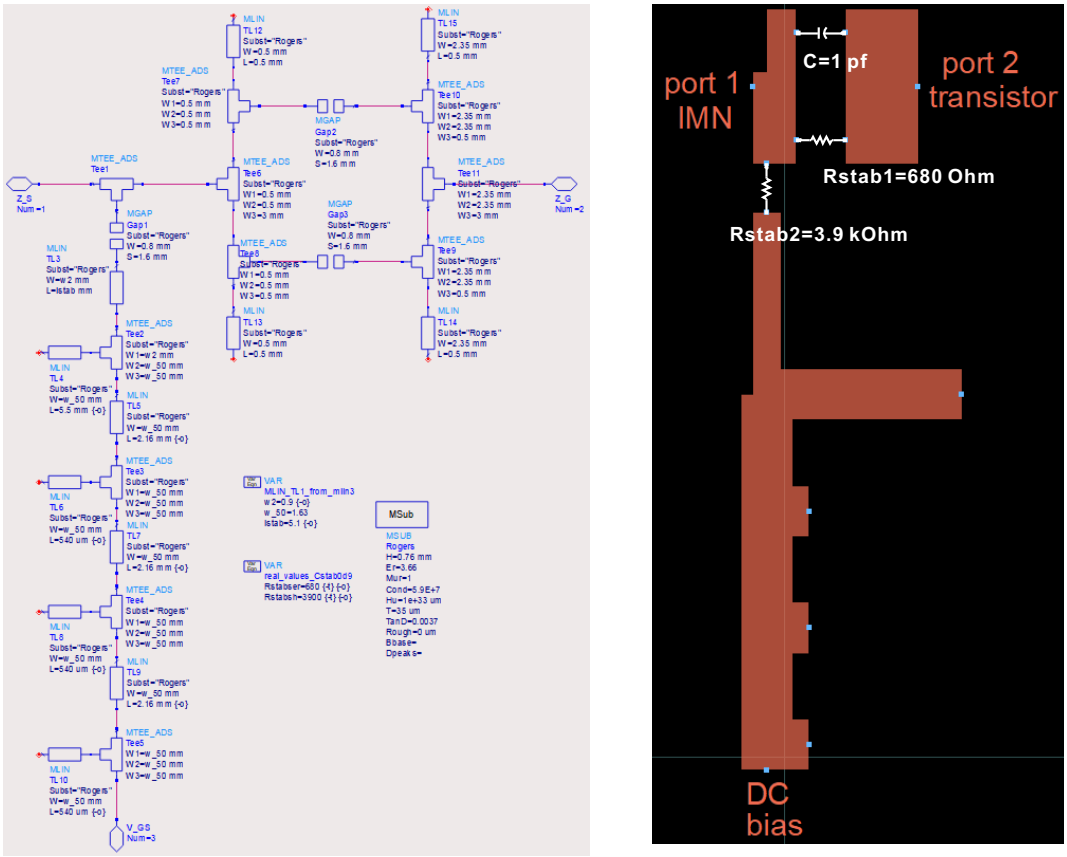

Figure 4.2: Microstrip schematic (left) and layout (right) of the input biasing and stabilization network.

4.2.2 Output biasing network

Regarding the output biasing network from Figure 3.8, further optimizations were performed to determine suitable line width in the DC path and at the port ends. After a proper tuning, the employed circuit and the corresponding layout are shown in Figure 4.3. Moreover, a bend was created at the midpoint of a long section to reduce the overall dimension of the final layout.

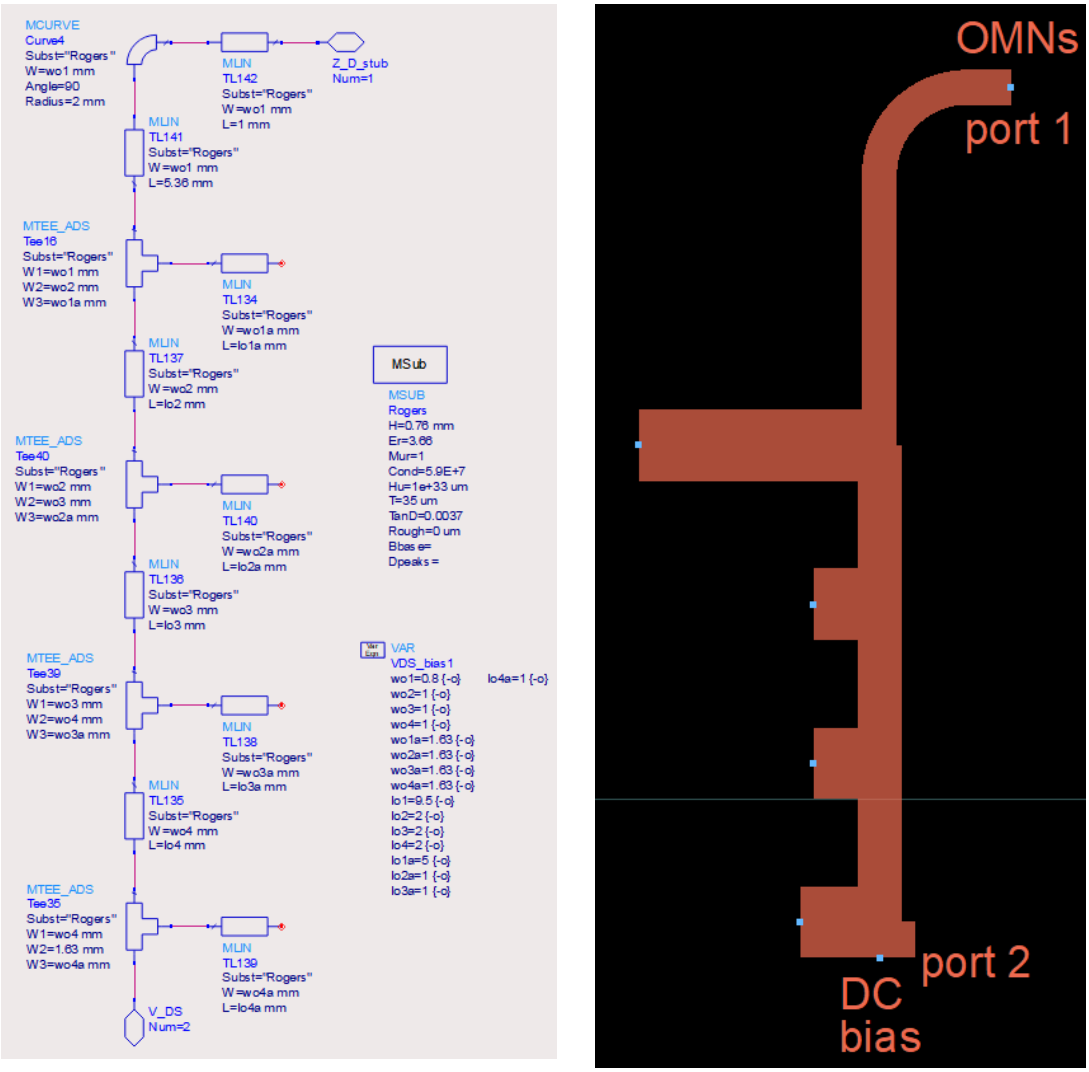

Figure 4.3: Microstrip schematic (left) and layout (right) of the output biasing network.

4.3 Matching networks

The microstrip implementation of the matching networks requires careful consideration since it is the most sensitive part of the design, introducing losses and potentially having a significant impact on the PA performance. It needs to be optimized, taking into account the physical dimensions as well as the impedance matching accuracy.

4.3.1 Output matching networks

BPA branch

Compared to Figure 3.17, the circuit was re-optimized by adding two extra lines to adapt the connections, as illustrated in Figure 4.4. The layout is shown in Figure 4.5.

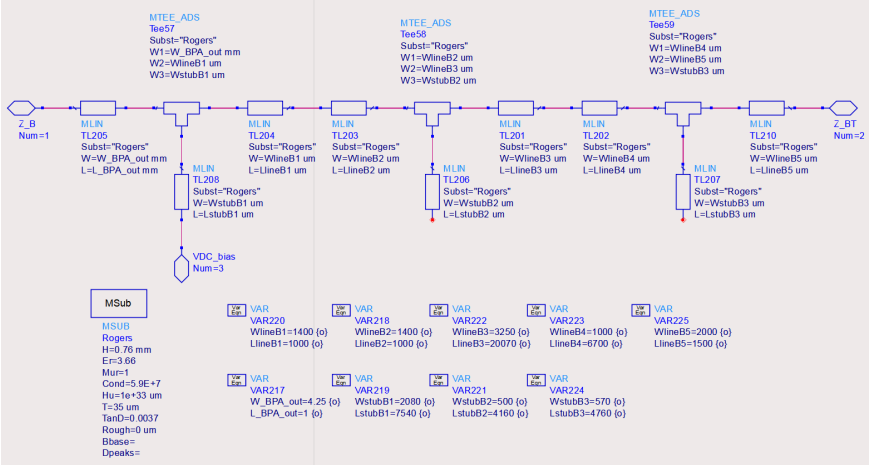

Figure 4.4: OMN of BPA branch in microstrip.

Figure 4.5: Layout of BPA's OMN.

CPA branch

In order to meet the limitations and enhance the performance, the OMN for CA was re-optimized using a symmetrical-stub structure. Extra pieces of lines were added for connections, and the longest stubs were bent to save some area in the final layout. The circuit is shown in Figure 4.6 and the layout of it is shown in Figure 4.7.

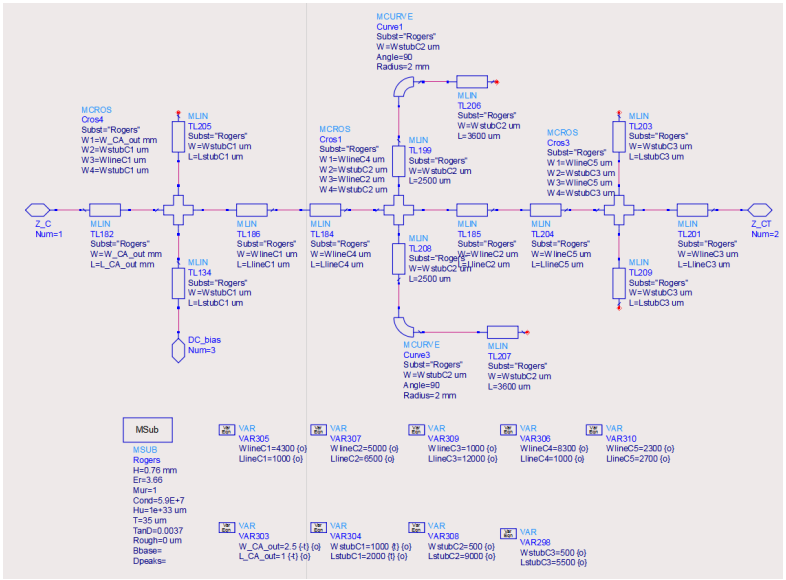

Figure 4.6: OMN of CA branch in microstrip.

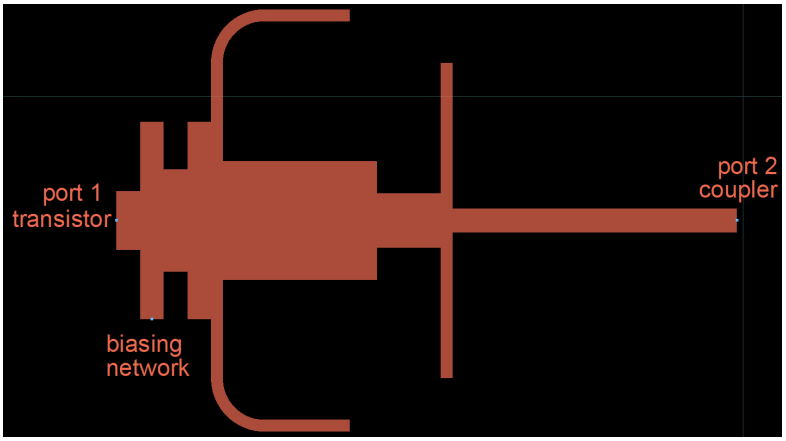

Figure 4.7: Layout of CA's OMN.

4.3.2 Input matching network

The IMN was optimized to ensure a proper spacing between adjacent stubs, taking into account the width of the lines and stubs. This optimization was performed to avoid rapid transitions in the connections, which can introduce impedance mismatch and signal degradation. By stressing a smooth and gradual transition, the optimized IMN helps maintaining the signal integrity and enhance the overall performance of the circuit. The optimized circuit is shown in Figure 4.8. The layout is shown in Figure 4.9.

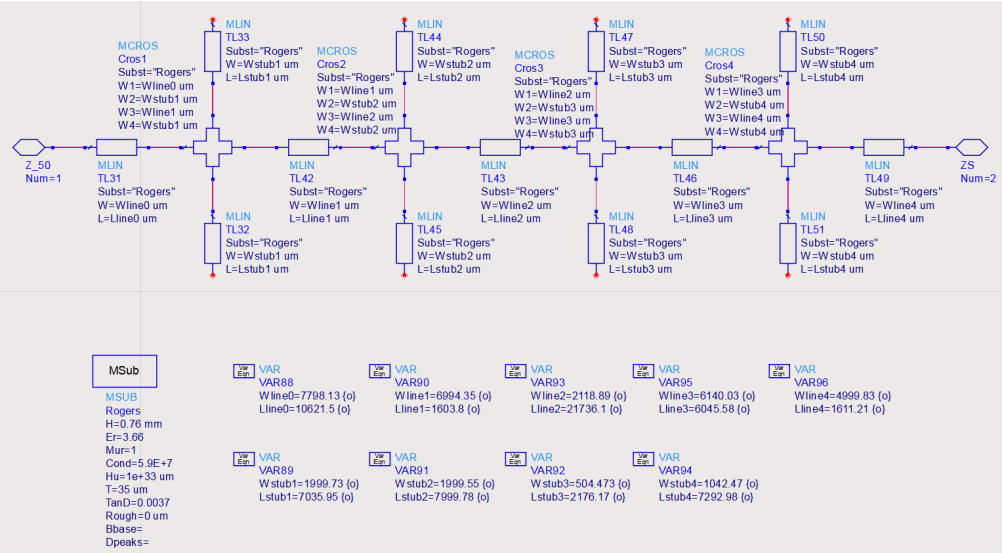

Figure 4.8: IMN in microstrip.

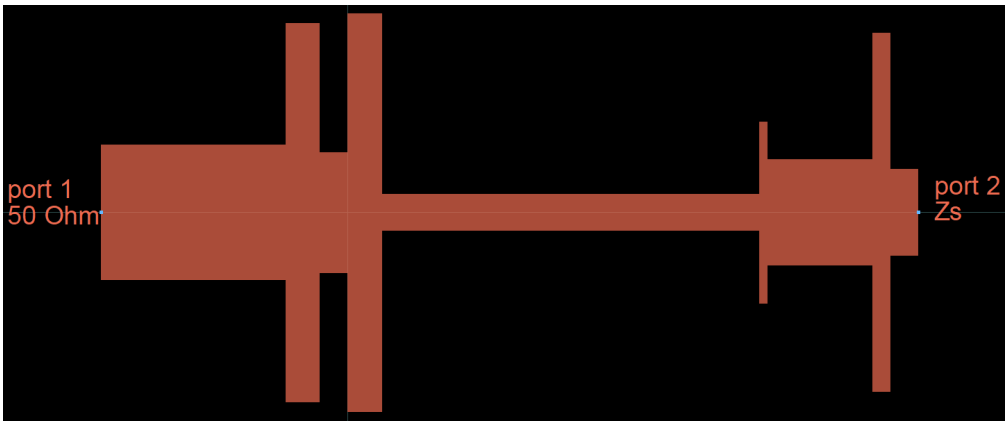

Figure 4.9: Layout of IMN.

4.4 Combining and splitting networks

4.4.1 3-dB 90° Branch-line Coupler

During the realization of the coupler, it was observed that there were frequency shift issues, indicating the need for adjustments in the width and length of the structure. These adjustments were made while maintaining the symmetrical structure of the branch-line coupler. The goal was to optimize the coupler's performance and ensure accurate signal coupling between the input and output ports. After proper tuning, the desired frequency response was recovered and the adopted 3-dB 90° branch-line coupler is displayed in schematic (Figure 4.10) and layout (Figure 4.11).

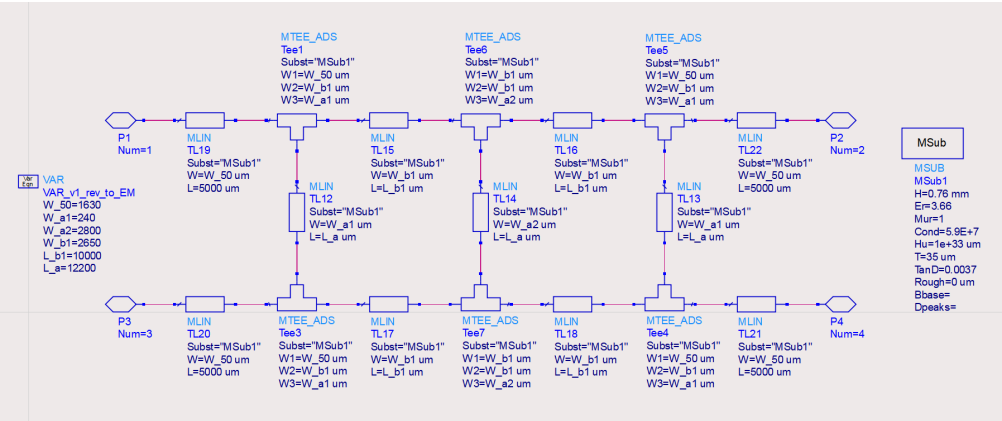

Figure 4.10: 2-section branch-line coupler in microstrip.

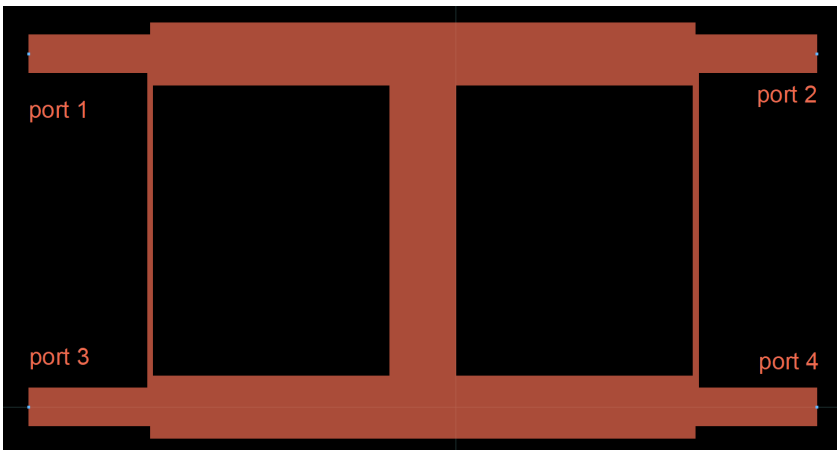

Figure 4.11: Layout of 2-section 3-dB branch-line coupler.

4.4.2 Wilkinson divider

As for the power divider, the quarter-wavelength lines were implemented using circular shapes. This was optimized to achieve the desired electrical length for proper signal splitting. The circular shape helps in maintaining the impedance characteristics and reducing unwanted reflections or impedance mismatches. By carefully designing the dimensions of the circular lines, the Wilkinson divider can effectively divide the input power into equal portions without significant signal loss or distortion. The schematic and layout are shown in Figure 4.12 and 4.13.

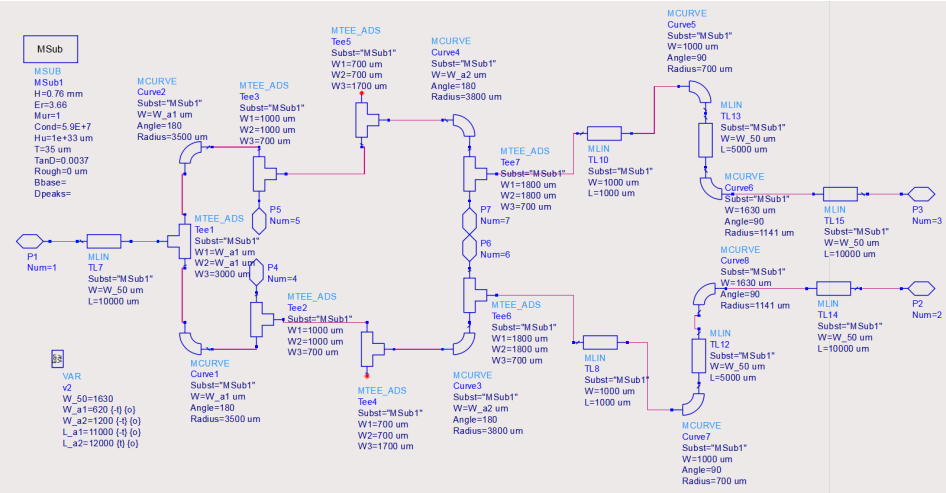

Figure 4.12: 2-section Wilkinson divider in microstrip.

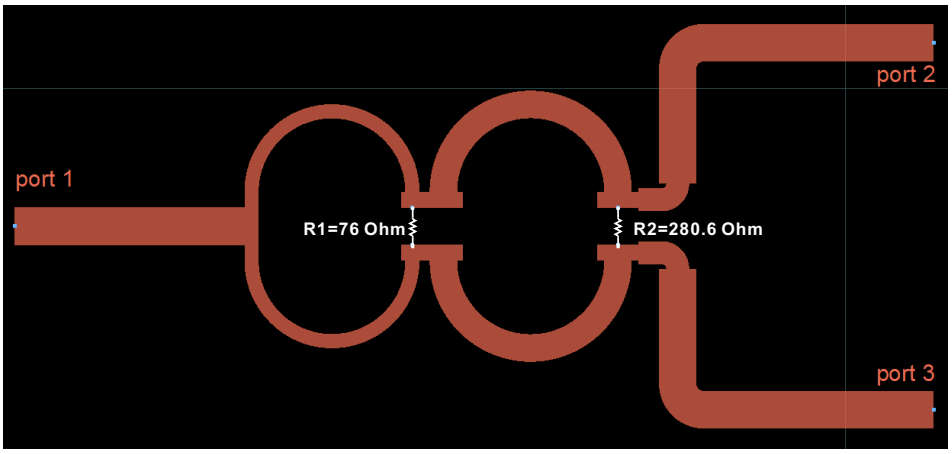

Figure 4.13: Layout of 2-section Wilkinson divider.

4.5 Phase Compensator

The phase compensator was re-designed using a symmetrical-stub structure to ensure coherence with the desired phase response. The circuit was optimized to achieve the desired phase shift at different frequencies by carefully tuning the dimensions of the stubs and lines. The schematic and layout are shown in Figure 4.14 and 4.15.

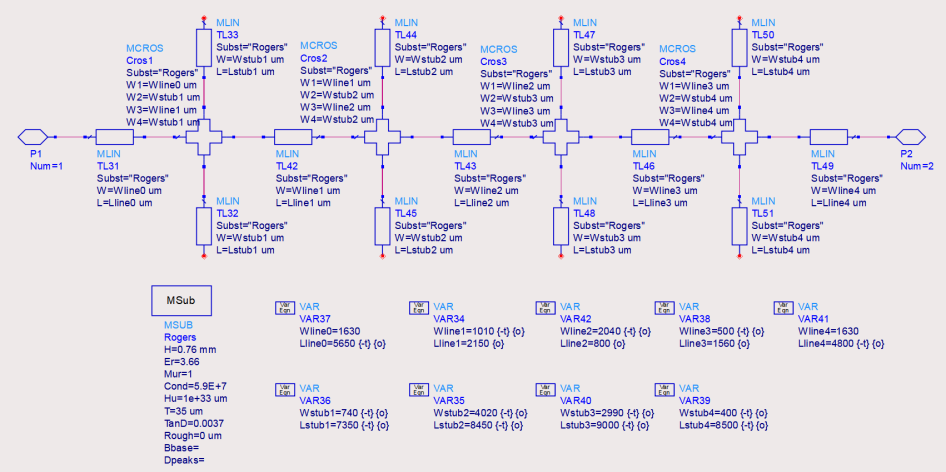

Figure 4.14: Phase compensator in microstrip.

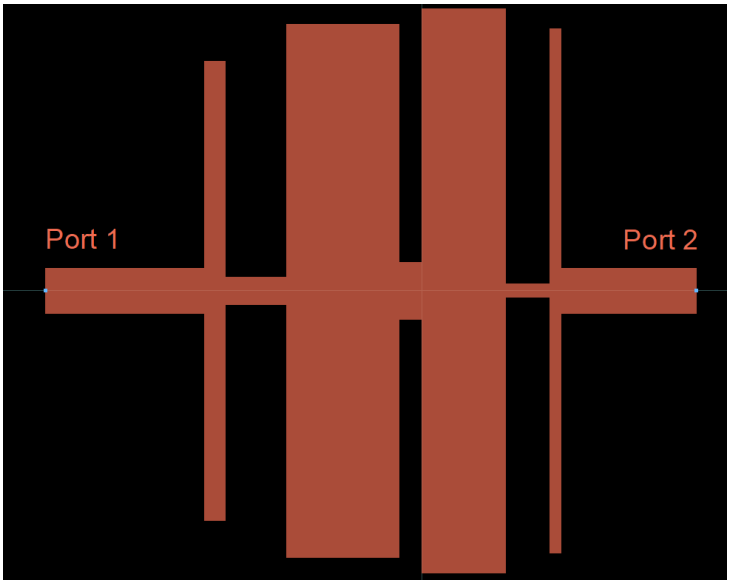

Figure 4.15: Layout of phase compensator.

4.6 SLMBA final layout

The final layout of the SLMBA is shown in Figure 4.16. In addition to the sections that have been discussed previously, the layout also includes the ground plane, DC bias connection pads, and tuning sections for future experiments. The overall dimensions of the final layout is 19.6 cm $\times$ 12.8 cm. With the complete circuit design and layout, the SLMBA is now ready for the fabrication.

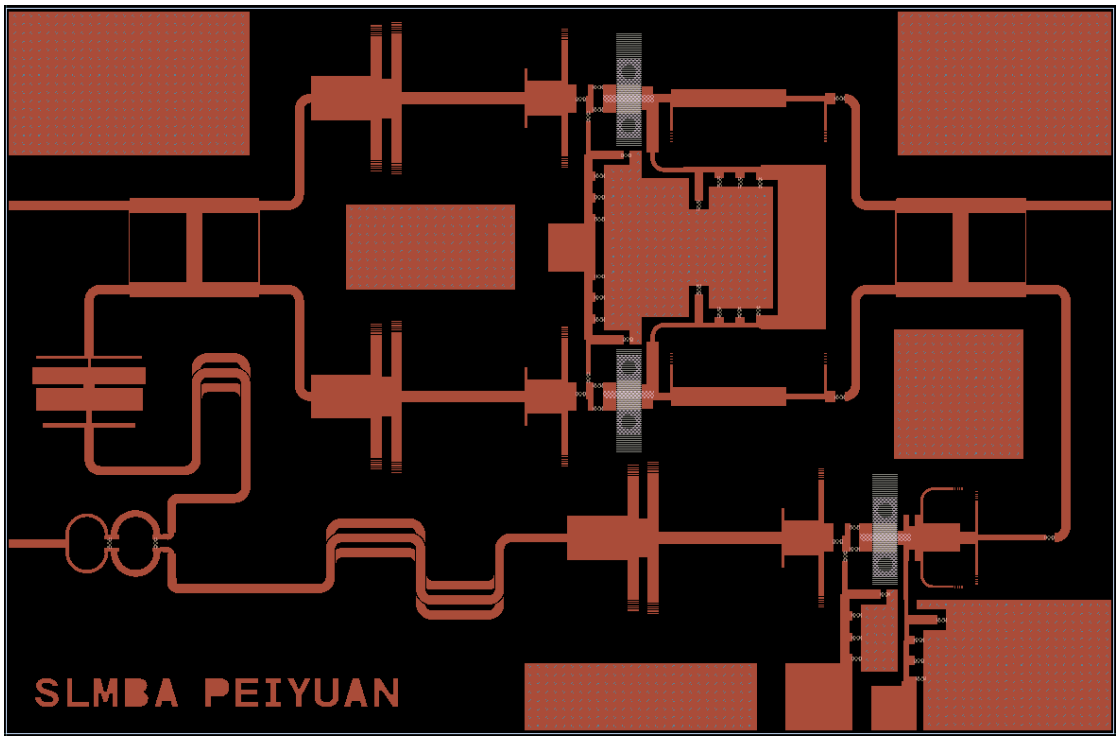

Figure 4.16: Final layout of SLMBA.

4.7 Electromagnetic Simulation

After creating the layout, EM simulations were introduced to precisely analyze the individual parts of the circuit. They can accurately evaluate the behavior of the circuits in real-world scenarios. These simulations were initially tested using S-parameter analysis for individual circuit components. Then the circuits were combined into a larger block using the SLMBA configuration to perform a comprehensive simulation. The settings for the EM simulation, such as mesh density, frequency range, ports definition and convergence algorithm, are critical to obtaining accurate results.

4.7.1 EM simulations for different networks

With the proper setup, EM simulations for different networks were performed and the results were compared with those obtained from the circuit simulations. The comparison of all the circuit blocks between the circuit simulations and EM simulations is shown in the following figures (Figure 4.17, 4.18, 4.19, 4.20, 4.21, 4.22, 4.23, 4.24). From these results, it is evident that the circuit is correctly translated into the layout, and both exhibit consistent performances.

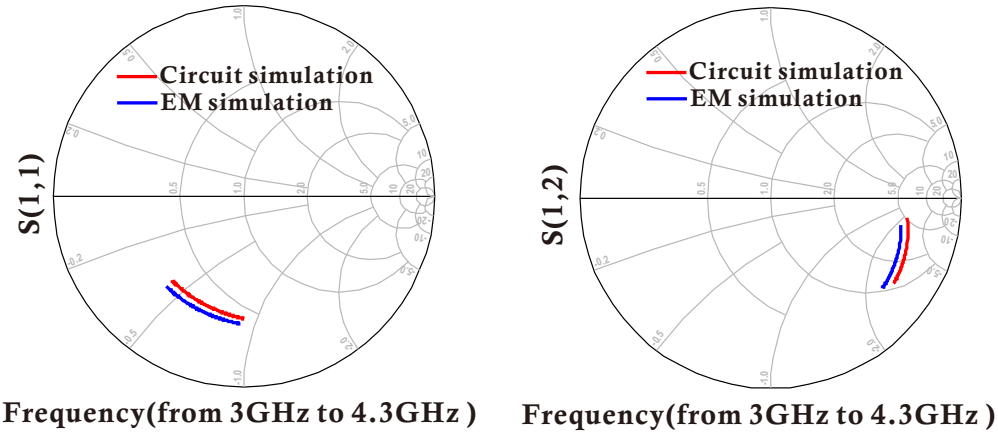

Figure 4.17: S-parameter comparison of the input biasing and stabilization network between the microstrip circuit and the EM simulation.

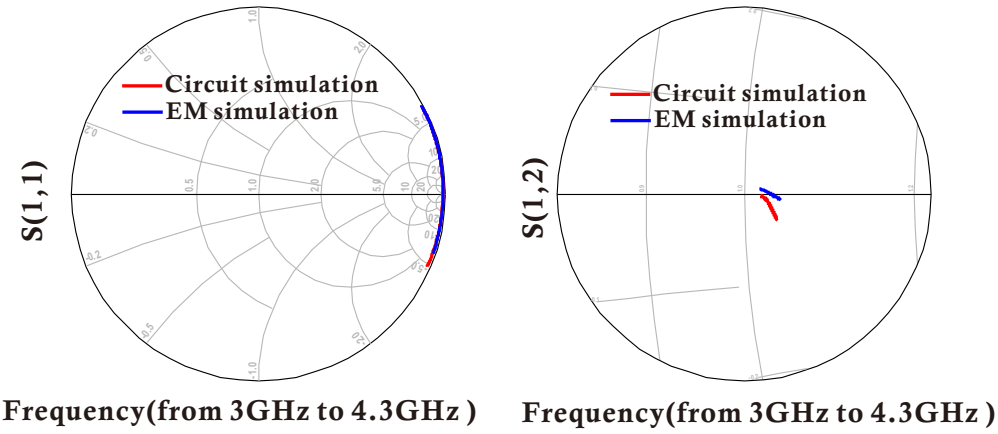

Figure 4.18: S-parameter comparison of the output biasing network between the microstrip circuit and the EM simulation.

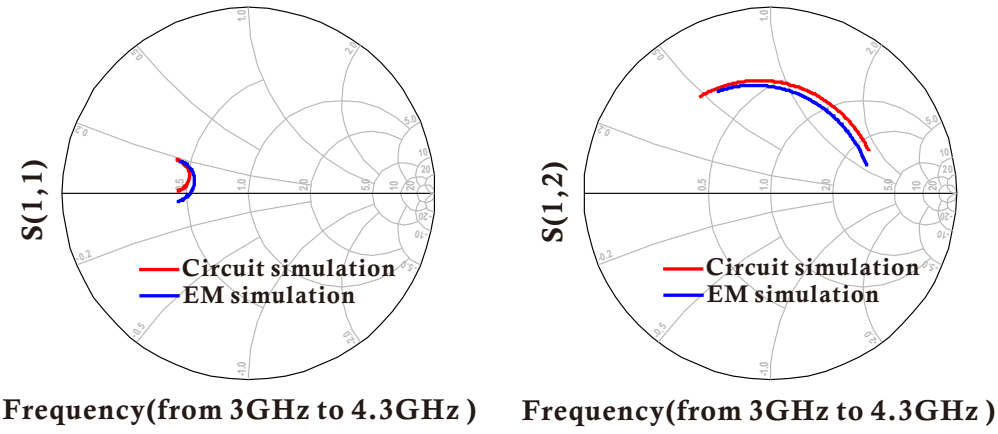

Figure 4.19: S-parameter comparison of the BPA's OMN between the microstrip circuit and the EM simulation.

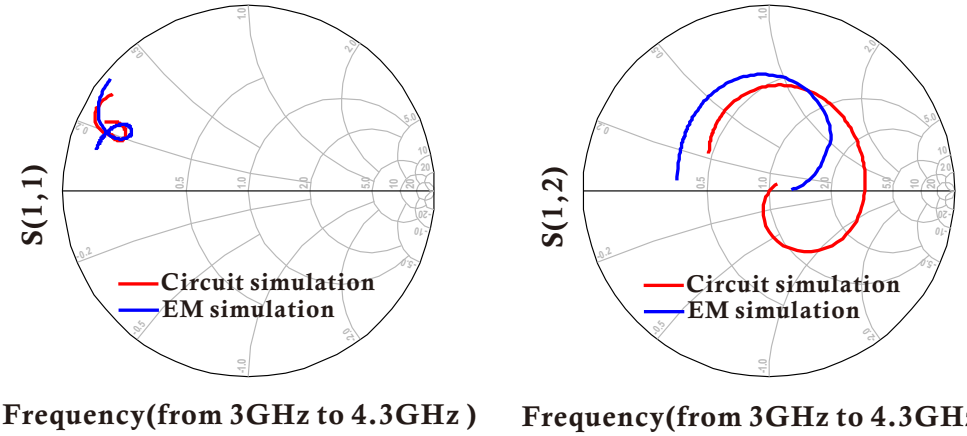

Figure 4.20: S-parameter comparison of the CA's OMN between the microstrip circuit and the EM simulation.

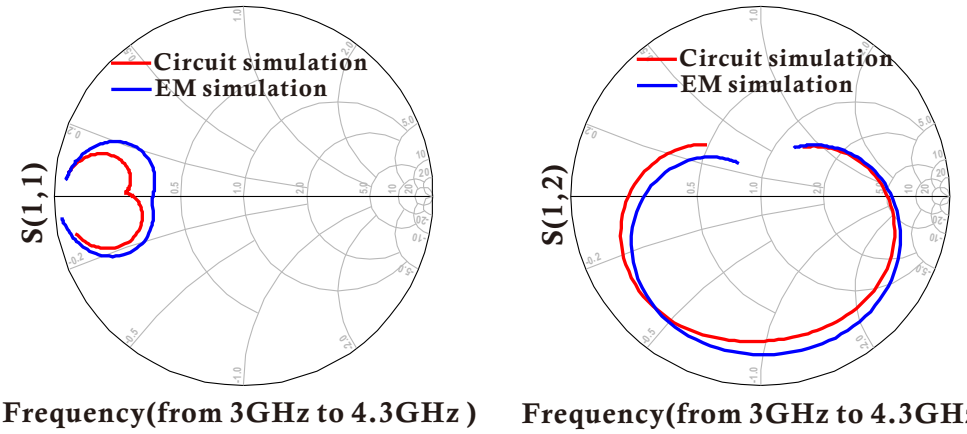

Figure 4.21: S-parameter comparison of the IMN between the microstrip circuit and the EM simulation.

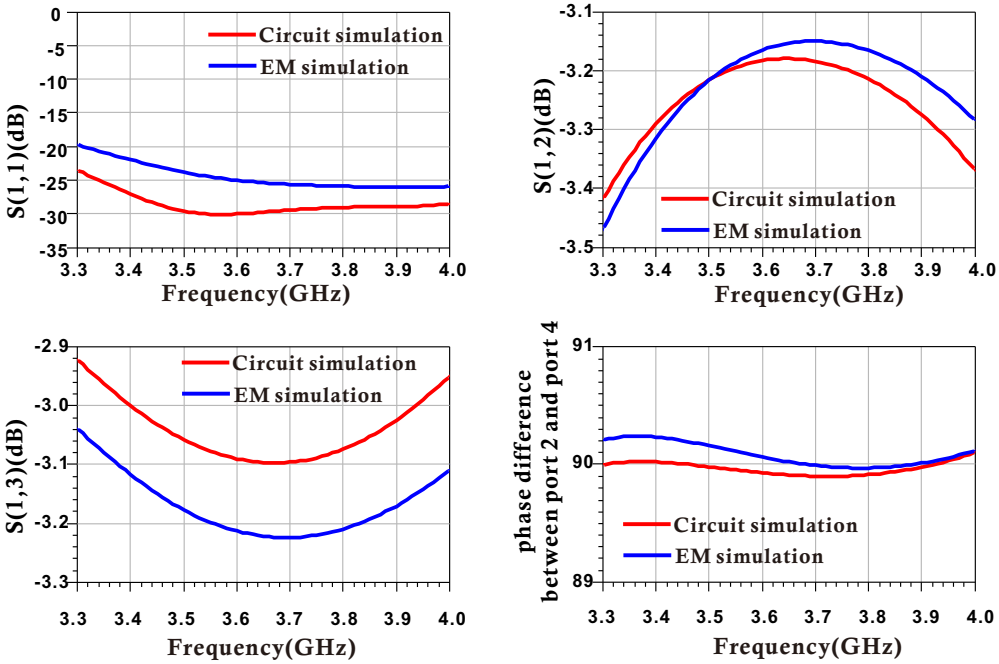

Figure 4.22: S-parameter comparison of the branch-line coupler between the microstrip circuit and the EM simulation.

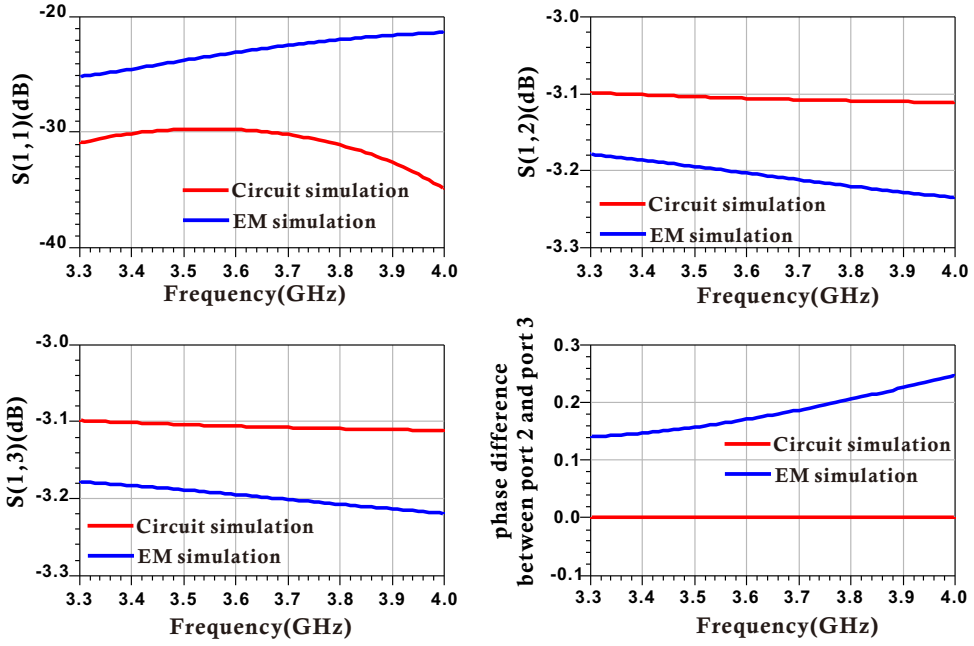

Figure 4.23: S-parameter comparison of the Wilkinson divider between the microstrip circuit and the EM simulation.

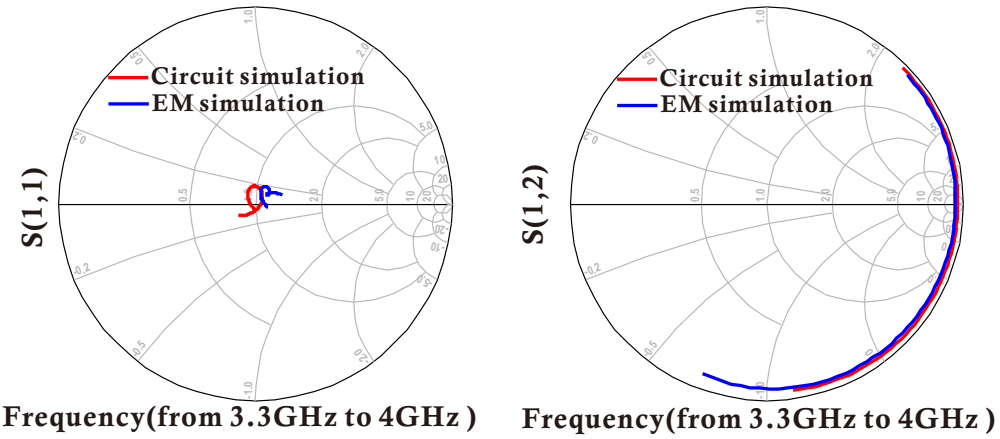

Figure 4.24: S-parameter comparison of the phase compensator between the microstrip circuit and the EM simulation.

4.7.2 Final simulation of SLMBA

The final step involves using the sub-circuits generated from the EM simulation, which provide a more realistic representation of the circuit behavior, to verify the performance of the SLMBA in real-world conditions. The circuit is presented in Figure 4.25.

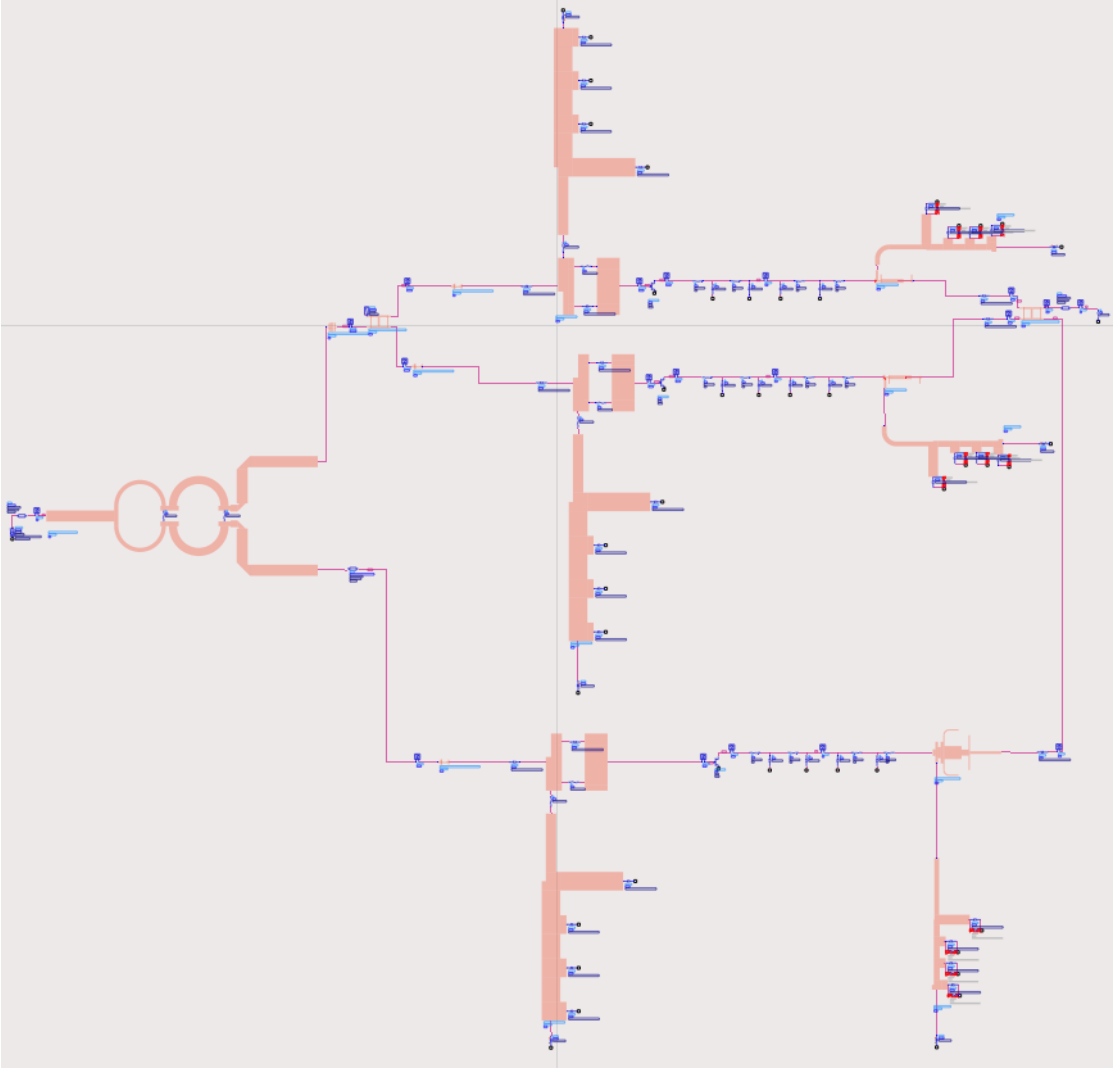

Figure 4.25: Schematic of SLMBA with components from EM simulation.

Finally, the overall performance of the SLMBA is presented, regarding the results obtained from both circuit simulations and EM simulations. The results are summarized in Figure 4.26 and 4.27. Based on the EM simulation results, which is more reliable and accurate, it is evident that the designed SLMBA successfully

achieves wideband performance in terms of efficiency, output power and gain. The circuit exhibits a uniform saturation output power of 43 dBm over the entire bandwidth. Additionally, the small-signal gain remains above 11 dB with a narrow variation interval of only 1 dB. At saturation, the drain efficiency ranges from 40% to 60%, while the PAE varies from 28% to 40% within the working band. At a 9-dB output back off, the drain efficiency maintains a stable value of approximately 40% and the PAE remains around 35% within the working band. These performance metrics highlight the successful design and implementation of the SLMBA for wideband applications.

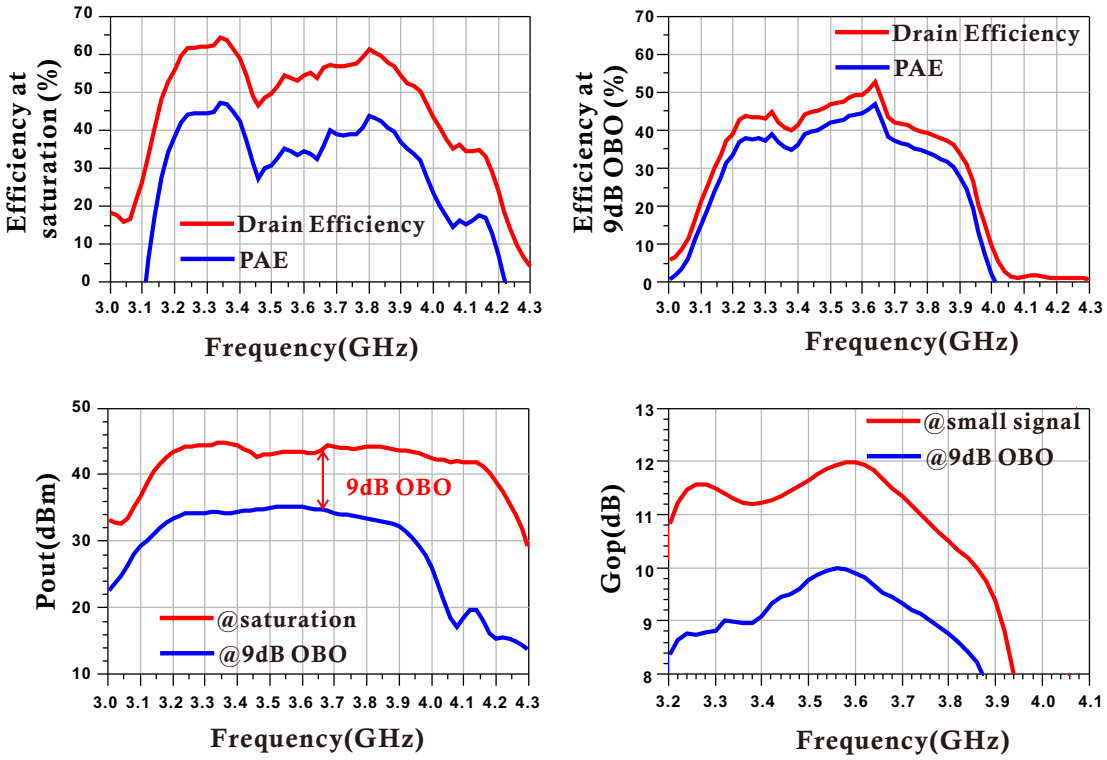

Figure 4.26: Summary of the SLMBA performance in Microstrip circuits.

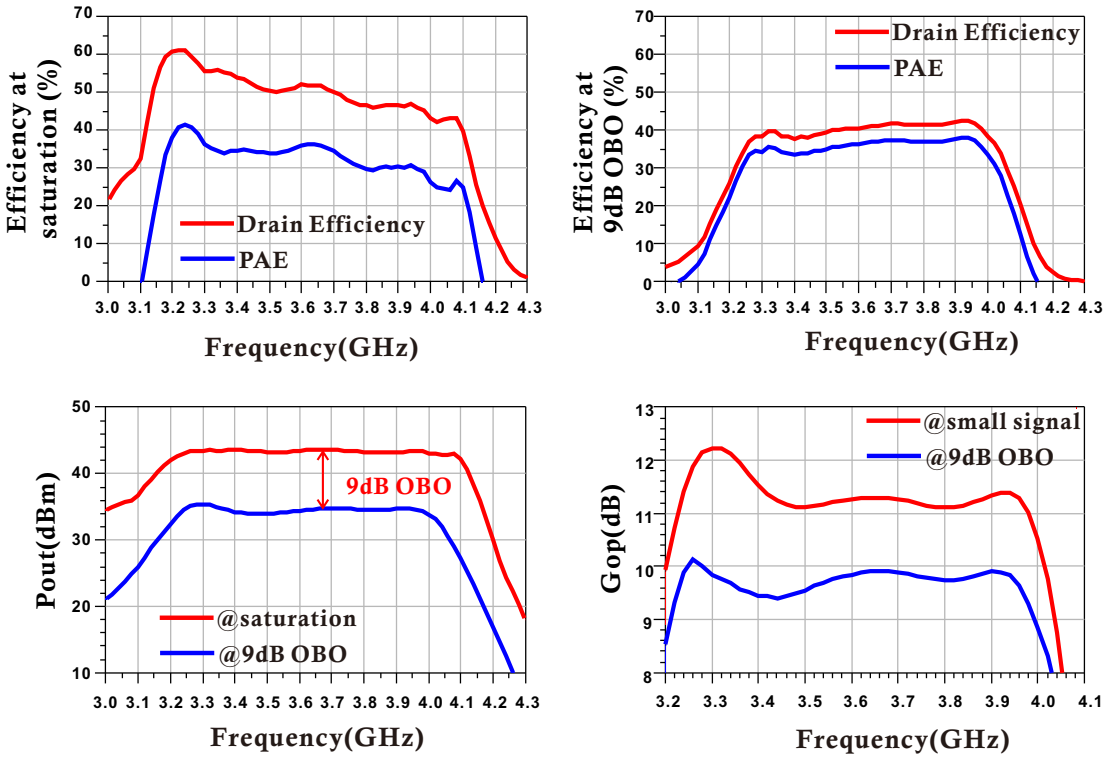

Figure 4.27: Summary of the SLMBA performance with components from EM simulations.

Chapter 5

Conclusion

This thesis project presents the theory analysis and circuit design of an RF-input SLMBA for 5G applications in the N77 frequency bands (from 3.3 GHz to 5 GHz). The optimized PA design demonstrates the ability to achieve high efficiency, wide bandwidth, and a large OBO range. It achieves a stable saturation output power of 43 dBm (approximately 20 W) across the entire bandwidth. The small-signal gain exceeds 11 dB with a variation interval of only 1 dB. The PAE remained at a wideband level above 30%, even in the deep OBO range of 9 dB. Furthermore, the output power and efficiency remain uniform over the designed fractional bandwidth of 19%. The hybrid circuit has a final dimension of 19.6 cm $\times$ 12.8 cm.

However, it is worth noting that the use of an over-driven carrier PA could potentially impact the overall performance and reliability of the SLMBA. To mitigate the risks associated with extreme over-driven stages, the addition of limiters or clippers in the CA branch can provide the protection. Additionally, it is necessary to highlight that in this thesis work, where identical transistors were used for both BPA and CA branches, the carrier PA was forced to be underused due to a sub-optimal load that was significantly larger than the optimum one. This suggests that further optimization and fine-tuning of the load conditions in the carrier PA branch could potentially lead to improved performance of the SLMBA.

Further improvements for this thesis work could include exploring the use of different transistors in the BPA and CA branches. This could optimize the loading conditions in the CA branch, thereby enhancing overall efficiency performance.

The next stages of the project involve the fabrication and measurements to verify the design and validate the obtained results. These steps will provide meaningful insights into the practical feasibility and performance of the SLMBA design, and further contribute to the understanding and advancement of SLMBA architecture in 5G applications.

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