POLITECNICO DI TORINO

Master's Degree in Electronic Engineering

Master's Degree Thesis

BAT-MAN 2nd life

Data acquisition system for Lithium-ion cells SoH and SoC estimation

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Abstract

Lithium-ion batteries play a vital role in the rapidly expanding electric vehicle market. However, the challenges associated with battery use, reuse, and disposal remain significant.

The BAT-MAN 2nd Life project aims to extend BAT-MAN, a device designed by Brain Technologies for diagnosing lead-acid batteries, to characterize lithium-ion batteries. State of Health (SoH) and State of Charge (SoC) are crucial metrics used to evaluate the battery's behavior for its future life and can be obtained by employing specific algorithms.

This thesis aims to prototype a device for acquiring the electrical parameters needed to characterize lithium-ion cells. The system was designed to validate the theoretical algorithms and serve as a starting point for an application-specific device capable of autonomously managing battery diagnosis and characterization.

After an initial research phase, a discharge system was designed to discharge the battery at a selected current that remains constant throughout the test, irrespective of battery variations and environmental changes. Three discharge modes were implemented: constant, step, and random. The constant mode is used to determine the actual battery capacity by discharging at low currents to avoid stressing the battery and calculating the total depleted charge. The step mode enables the characterization of battery behavior under higher current stress, while the random mode adds additional test points to the model. The system was designed to prevent current spikes that could harm its components or the battery in the case of state transitions or faults, employing real-time battery voltage monitoring for safety purposes.

The system behavior is managed by a microcontroller, with data being collected and sent via UART to a PC for post-processing, generating plots, and arranging the data in CSV format to feed algorithms (developed separately) thanks to a Python script. The system's firmware was developed on the STM32 platform, implementing a finite state machine on FreeRTOS. The entire test process is automated due to its time-consuming nature, with each discharge cycle preceded by a charge performed using a commercial charger.

The system prototype was implemented on a stripboard and extensively tested in the laboratory. The results aligned with the expected models. Furthermore, the system provides ample room for improvement, both in terms of hardware, such as the development of a PCB or an ASIC, and firmware capabilities, as it has the potential to track current profiles in addition to constant current discharging.

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Chapter 1

Introduction

1.1 Project goal

Energy storage plays a crucial role in the transition toward a sustainable economy. Renewable energy sources, while essential for future power generation, are not readily available on demand due to their inherent characteristics. To address this issue, new and efficient energy storage means are needed.

Transportation, a major contributor to climate change, requires reducing reliance on fossil fuels. As a result, electric motors are substituting traditional internal combustion engines. Significant investments in energy storage solutions are needed to accomplish this transition, with a current focus on lithium-ion (Li-ion) batteries.

Li-ion batteries intended for automotive applications must meet stringent performance criteria. First and foremost, they must deliver high power output to ensure vehicle comfort, safety, and maneuverability. Adequate total capacity is vital to provide sufficient range for the vehicle. High-cost battery packs with superior capacity and performance characteristics are utilized to fulfill these requirements. Nonetheless, current technologies result in a shorter lifespan for automotive battery packs than anticipated, leading to their replacement at around 80% of the total expected lifecycle. [1]

Conversely, batteries used for daily energy storage have less stringent demands, mainly pack size flexibility and lower current requirements. The cost factor significantly impacts the widespread adoption of energy storage batteries, as automotive battery packs account for a significant part of the total vehicle cost. The current pricing renders storage batteries economically unfeasible in the same context. [2]

The ecological transition could rely on Li-ion batteries' full lifecycle utilization. The extension of automotive batteries' use to the energy storage field could be a potential key factor for its success.

Presently, a widely accepted method for certifying a used battery for re-qualification is lacking. Simultaneously, battery use must cease at a suitable point to ensure its longevity in the second life. To address this challenge, a simple and cost-effective device is required to monitor and assess the battery's State of Health.

The BAT-MAN 2nd Life project goal is to design a system that can estimate the necessary parameters to characterize the used battery, collecting the on-field data safely and accurately and feeding it to advanced algorithms that will process it accordingly.

1.2 Thesis outline

This thesis aims to develop a prototype for testing Li-ion batteries, acquiring significant electrical parameters required for battery characterization.

- Study of BAT-MAN architecture and analysis of its compatibility with Li-ion technology;
- Hardware and firmware design according to technical specifications of common Li-ion cells and requirements for a proper outcome from the algorithms that will process the data (measurement accuracy, resolution, timing constraints);
- Test and debug on breadboard and stripboard prototype with commercial power supply;
- Full functional test with Li-ion cells on stripboard final prototype.

1.3 Li-ion batteries

Lithium-ion batteries (Li-ion batteries) are electrochemical devices that currently represent the main choice of supply for portable electronic devices, energy storage, and automotive battery packs, thanks to their optimal performance metrics. [3]

These batteries were first introduced to the market in the early 1990s and have since undergone significant advancements in their performance and applications. The basic structure of a Li-ion battery typically consists of a graphite anode, a LiCoO2 or LiMn2O4 cathode, and a lithium-ion conducting electrolyte. [4] The electrolyte is responsible for facilitating the movement of lithium ions between the electrodes during charge and discharge cycles. [3]

Li-ion batteries have become crucial in the market due to their numerous advantages over other battery technologies. Initially commercialized for portable electronic devices such as cell phones and laptops, Li-ion batteries have now expanded their applications to electric vehicles (EVs) and grid-level energy storage systems (ESSs). [3] This shift in demand can be attributed to the increasing need for sustainable transportation and energy systems.

In the past, lead-acid batteries were the dominant technology for various applications. However, Li-ion batteries have emerged as a superior alternative due to their higher energy density, longer cycle life, and lower self-discharge rate.

1.4 Battery current and charge/discharge rate

A convenient notation to indicate the battery current is the C-rate. C-rate considers battery current and capacity and expresses how they are related: it is inversely proportional to the hours needed to discharge a battery completely. At a 1C rate, the battery will fully discharge

in 1 hour, at 2C in 30 minutes, and so on. This notation allows to normalize with respect to battery capacity, that differs a lot among batteries. [5] [6]

For example, if a battery with a capacity of 2000 mAh is charged/discharged at a rate of 0.5C, it should discharge/charge at a current of 1A, and the discharge process should be completed within 2 hours.

It is important to note that an excessively high charge/discharge rate can hurt battery performance. This can result in increased heat generation, reduced battery life, and potential safety hazards. To ensure optimal battery performance and safe operation, manufacturers provide recommended charge/discharge rates. It is crucial to follow these guidelines to avoid compromising battery performance and maintain safety while operating the battery.

1.5 Battery internal impedance

Several factors determine the internal impedance of lithium-ion cells. One relevant aspect is the electrolyte material's internal resistance, which impacts the flow of ions within the cell. In addition, the internal impedance is affected by the composition and structure of the materials used for the electrodes, which include both the anode and cathode.

When an external load is connected to the battery, the resulting current generates a voltage drop across the internal impedance. As a result, the voltage measured at the battery terminals differs from the battery open-circuit voltage.

The battery's internal resistance is usually different for charge and discharge. Moreover, it is dependent on the battery's state of charge. Higher internal resistance is related to reduced battery efficiency. Also, as heat is generated by charging energy, thermal stability decreases. [5]

1.5.1 Nominal capacity

Nominal capacity, also known as rated capacity, is a quantity provided by the manufacturer that expresses the ideal amount of charge that the battery can store or, in other words, the maximum amount of charge that the battery can provide under ideal conditions.

1.5.2 Real capacity

The real capacity is the actual value of the battery. This value may differ from the rated capacity provided by the manufacturer for various reasons, including aging and temperature. Contrary to what is generally thought, the value of the actual capacity may be greater than the rated value, as the rated capacity stated in the manufacturer's documentation is an average figure. It should be added that although the battery's capacity decreases during its lifespan, during a short initial phase, a possible additional release of lithium would enhance the capacity of the battery. [7]

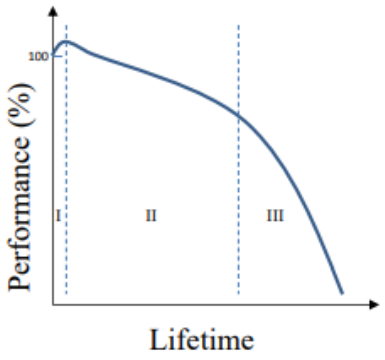


Figure 1.1: Typical evolution of capacity during the battery lifetime, expressed as relative performance [7]

1.6 State of Charge

A battery's State of charge (SoC) is an expression of the present capacity as a percentage of maximum capacity. [5]

Considering at instant t_0 the fully charged battery, the amount of battery charge at instant t can be calculated as follows:

$$Q(t) = Q_0 - \int_{t_0}^{t} I(\tau)\, d\tau$$

Where I(t) is the discharge current of the battery. With these considerations, the State of Charge can be defined as follows:

$$SoC = \frac{Q(t)}{Q_0} = \frac{Q_0 - \int_{t_0}^{t} I(\tau)\, d\tau}{Q_0}$$

The maximum battery charge Q_0 is sometimes set equal to the nominal capacity C_N, sometimes equal to the effective capacity C_R. [8]

The State of Charge (SOC) is a non-dimensional value ranging from 0 to 1, which indicates the battery's remaining capacity as a percentage. It is important to clarify that a SoC of zero does not imply a fully depleted battery; rather, it means that further discharge would result in irreversible damage to the battery.

1.7 State of Health

Due to aging and usage (charging and discharging), batteries gradually deteriorate, resulting in a decrease in capacity and an increase in internal resistance. This is why the state of health (SoH) of a battery is often measured by its capacity. The state of health is typically defined as follows:

$$SoH = \frac{C_R}{C_N} \cdot 100\%$$

where C_R represents the actual capacity and C_N denotes the nominal capacity. Since a battery's actual capacity in its initial life cycles may exceed the nominal value, the SoH can sometimes be greater than 100%. However, to ensure performance requirements are met, once the SoH falls below the threshold of 0.8 (80%), the useful life cycle of the battery should be considered terminated, according to IEEE standards. [9]

Chapter 2

State Of Art

2.1 BAT-MAN

BAT-MAN is a device developed by Brain Technologies for online SoH and SoC estimation of lead-acid 12 V automotive batteries by measuring battery voltage, current, and temperature. It serves the purpose of a Battery Manager and embeds SoH and SoC estimators designed by Brain Technologies. The device was realized on a PCB along with a framework for its utilization, including an Android app and proper case and connections to enable direct mounting on car batteries. [10]

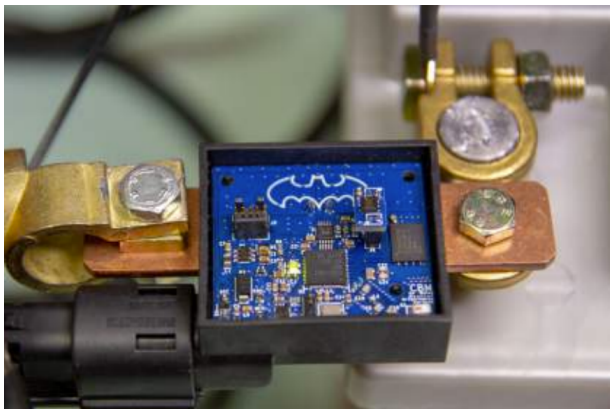


Figure 2.1: BAT-MAN [10]

The starting point of this thesis was exactly the analysis of Bat-Man technology and its eventual compatibility with Li-ion technology.

Unfortunately, it was quickly clear that a new device had to designed from scratch. Li-ion batteries work at different values and therefore need a redefinition of the technical requirements; they have peculiar behavior differences compared to lead-acid technology and pose additional challenges in many aspects, for example, overcharge and over-discharge

conditions resulting and safety matters in general. However, BAT-MAN's key concepts and purposes served as guidelines throughout the new design phase.

2.2 BAT-MAN 2nd life

This thesis aims to develop appropriate test instrumentation that can be incorporated into the research path adopted by Brain Technologies regarding lithium-ion batteries. So, it is worth highlighting the framework used to study and characterize the batteries.

A multi-model approach was studied for battery modeling and simulation. Since factors like the definition of empty or full battery, capacity, and State of Charge (SoC) or State of Health (SoH) hold substantial influence over the results obtained from the conducted tests, a rigid and reliable energetic framework was established to ensure consistent outcomes. These parameters were elaborated with a novel perspective to estimate SoH efficiently using the ERMES algorithm. [11]

ERMES refers to a proprietary algorithm developed by Brain Technologies that utilizes a diverse range of models to estimate intricate parameters, such as the State of Health (SoH). The core concept involves employing multiple observers, each initialized with a predetermined value for the target parameter. The data undergo simultaneous processing by these observers, and their respective outputs are then evaluated against a specific algorithm, selecting the minimum error model for the resulting SoH estimation. [11] [12] [13]

Applying the ERMES algorithm along with a broader multi-model approach showed promising results in addressing the challenge of estimating the State of Health (SoH) for a Li-ion cell.

This framework needs further validation through on-field experimentation. Physical battery data procedures should align with those employed in the simulation based on mathematical models to ensure accuracy and consistency.

2.3 Current devices

A wide range of devices offer the capability to test batteries and provide valuable information about their status at many different levels. The inherent ambiguity of the technical terms and the absence of standards in Li-ion batteries characterization made it difficult to have a clear idea of the products effectively able to provide all the necessary parameters for this thesis purpose and the procedure used to acquire those parameters.

SoH and SoC are common parameters that already available devices have the goal of estimating. Most of the time, however, the battery status indication corresponds to a rough estimate of parameters or has different starting points for battery testing (i.e., the employed assumption of fully discharged/fully charged battery) compared to the ones established by the BAT-MAN 2nd Life project. [11]

The most documentation-complete and accurate devices are typically costly, in the order of magnitude of 1000 dollars but possibly even more.

For example, Cadex C700 C-Series is a complete yet costly test setup for many kinds of batteries and sizes. It provides several functionalities and test modes to acquire different

parameters regarding battery life cycle, aging, and more. [14]

Figure 2.2: Cadex C7000 C-Series Battery Analyzer[14]

Therefore, despite the challenges it brought to the design, special attention was paid to keeping the device low budget.

The need for large datasets for the characterization of lithium cells, obtained by testing and aging the batteries themselves, implies that the market is rapidly evolving in search of devices that allow these procedures to be performed at low cost and automated. This thesis project fits into this context.

Chapter 3

Requirements Specification

3.1 Main features

The device must implement the following features:

- Automatically perform charging and discharging cycles on the battery;
- Manage discharging and charging cycles;
- Acquire battery voltage;
- Acquire battery current;
- Compute battery capacity (through Coulomb counting algorithm);
- Log collected data;

3.2 Test configuration

The system must be able to perform a set of pre-configured battery tests automatically. A battery test is defined as a series of current pulses sourced by the battery. The user defines all battery tests at compilation time, providing all the necessary parameters:

$$Tests\ Configuration = \{\{I, T, N_{step}, Mode\}, \{I, T, N_{step}, Mode\}, \{I, T, N_{step}, Mode\}, ...\}$$

I	Discharging current
T	Period of the discharging pulses
$Nstep$	Number of steps
$Mode$	Type of discharging

Table 3.1: Test configuration parameters

3.2.1 Discharging current

This value represents the current the system should drain from the battery under test. The user provides this value as a multiplication factor of the battery capacity (i.e., 1C, 0.5C). It is up to the system to compute the discharging current in Amperes based on the battery capacity. This implies the system is aware the nominal characteristics of the battery under test.

3.2.2 Period of discharging pulses

This value represents the time between two current pulses. Knowing the capacity of the battery, the discharging current, and the total number of steps, the system can determine T_{ON} as follows:

$$T_{ON}[s] = \frac{3600 \cdot C}{I \cdot N_{step}}$$

During this time, the system should drain the discharging current from the battery and keep it constant. During T_{OFF}, the system should not drain any current from the battery.

3.2.3 Number of steps

This value represents how often the system should apply a discharging current pulse to the battery for each cycle. It is a theoretical value based on the battery's nominal capacity and is used to compute T_{ON}. The system should keep applying pulses until the battery is discharged, regardless of the configured number of steps. At that time, the system passes to the next configured discharge cycle. Before running a new discharge cycle, the system should carry out a charge cycle and let the battery rest for a period T. After the resting period, the system can apply a new discharging cycle. When no more cycles are present, the system can consider the whole test finished and go to IDLE state.

3.2.4 Discharge mode

This parameter represents what type of discharging the system should apply to the battery among:

0	Constant current discharge
1	Characterizing discharge
2	Random discharge

Table 3.2: Battery discharge modes

Constant current discharge

This mode is characterized by a single continuous discharging step. When the user requests this type of test, the system should ignore unnecessary parameters and apply the configured discharge current. The system keeps applying such current until the battery is discharged. At that time, the test finishes, capacity value is updated and the system can go to IDLE

state. This discharge mode is designed primarily to determine the effective capacity of the battery under test. Ideally, every test sequence should start with a constant test.

Figure 3.1: Constant current discharge test

Characterizing discharge

This mode is characterized by a discharging current and a nominal number of steps configured by the user. The system should drain that current during T_{ON} and no current during T_{OFF}. During the application of the discharging current, the system should monitor the battery voltage and stop the cycle when it detects a dead battery.

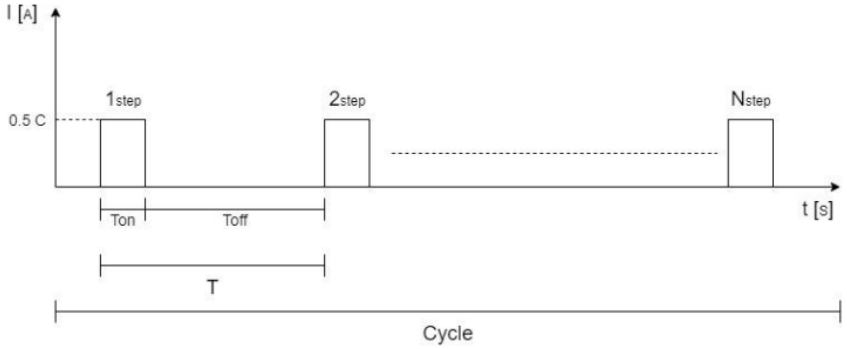


Figure 3.2: Characterizing discharge test

This mode is particularly useful to characterize the battery, stressing it at significant test points.

Random discharge

This mode is characterized by random values for T_{ON} and T. It is up to the system to generate such parameters. The system stops the cycle upon detecting a discharged battery.

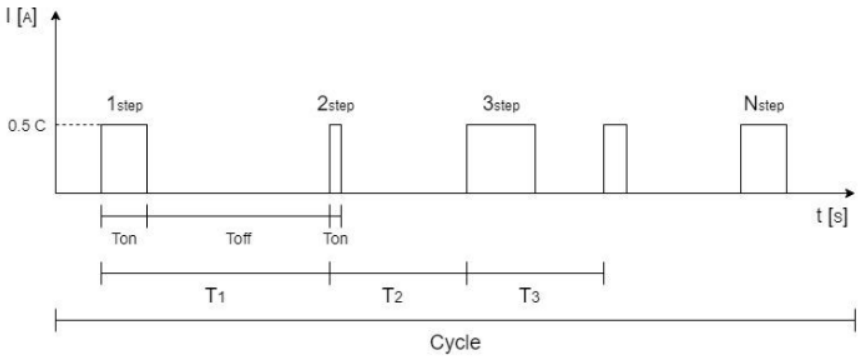


Figure 3.3: Random discharge test

This mode is used to gather other test points to enrich the dataset.

3.3 Management of discharge and charge cycle

3.3.1 Discharge cycle

The system must be able to draw currents from the battery under test from 500 mA up to 10 A. During a discharging cycle, the system sets a current to drain from the battery with the goal of keeping it constant. To achieve this, the system should implement a control algorithm that checks the actual discharging current and adjusts it properly. During the discharging phase, the system should also monitor parameters, such as battery voltage and total depleted charge, to prevent over-discharge. The system must achieve these features regardless of the discharging mode. As previously discussed, the system should drain current from the battery only during T_{ON}.

3.3.2 Charge cycle

The system should leave the battery on charge until it is fully charged. A full charge can typically be reached by detecting when the charger current drops under a certain threshold or leaving the battery connected to the charger for a sufficient time, provided the charger stops automatically when the battery is fully charged.

3.4 Battery voltage and current measurement

The system should measure the voltage and current of the battery under test. Sampled data is then logged and provided to an external system. The system must:

- Acquire battery voltage with a resolution of at least 25 mV (1% of minimum battery voltage of interest);
- Acquire battery current with a resolution of 5 mA (1% of minimum battery voltage of interest);

- Acquire battery voltage and current with a sample rate of 10 ms at most;
- Detect critical voltage and current values to prevent damage to the battery under test;

3.5 Charge and discharge automation

The system should automatically track the discharging profiles and charge the battery after each discharge cycle. No actions are required by the user. The system must satisfy the following functional requirements:

- Monitor the battery voltage to determine when the discharge cycle ends;
- Stop discharge cycle and start charge cycle;
- Fully charge the battery;
- Stop the charge cycle and go to the next discharge cycle;

3.6 Output file definition

The data logged from the device must be converted to CSV format so that it can be directly elaborated for model validation and SoH estimation.

This file must contain a Header for each test in which the following parameters are reported:

- Sampling time (log)
- Test type (constant discharge, step discharge, random discharge).
- Test current
- Cut-off voltage

In addition, the following data must be submitted for each measurement:

- Sample number (used to reconstruct the time sequence)
- Current
- Battery voltage
- Q (integral of the current)

Data resolution of transmitted and acquired data can be different, provided it stays compliant with the specifications.

Chapter 4

Hardware design

4.1 Introduction

The system was designed considering three parts: the discharge section, the charge section, and the battery.

Considering the specifications, the discharge section provided a way to discharge the battery in a specified manner. The charge section was nothing more than a charger able to fully and safely charge the cell under test. The battery section was the battery itself, along with its case and connections.

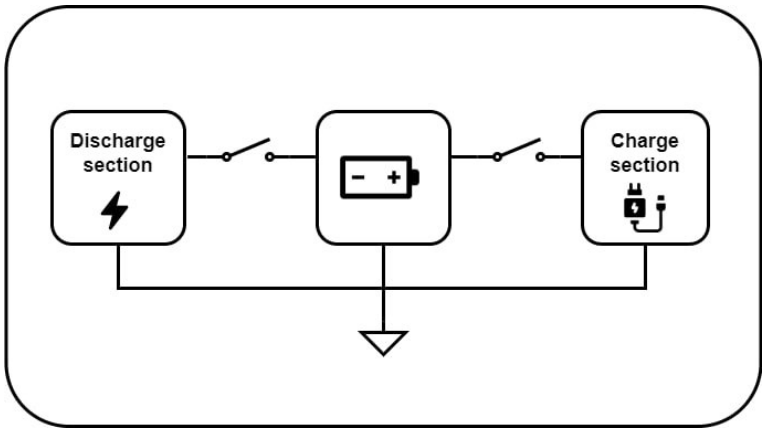


Figure 4.1: Functional scheme

4.2 Discharge section design

4.2.1 Preliminary Design Considerations

DC Motors

The first considered solution was to attach a few DC motors to a microcontroller powered by the battery.

Figure 4.2: DC Motors [15]

This idea would have allowed a simple, cost-effective, easy-to-drive system. However, checking the options available on the market, it quickly became clear that the most common motors drained very low currents concerning the considered lithium-ion battery cells. [15] This would have meant absurdly long simulation time and difficulty in guaranteeing the correct system behavior over such a huge time span. Moreover, current is related to torque, so it's difficult to derive an easy relationship between driving voltage and draw current.[16]

Lamp

An alternative that was first considered due to its straightforward implementation consisted of bulb lamps.

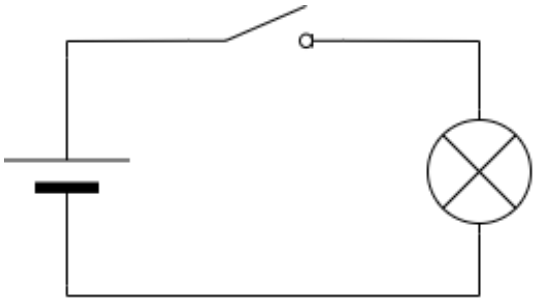


Figure 4.3: Lamp scheme

Again, the load would have been simple, and the system should have performed the simple task of switching on and off a light that would consume power and drain current. Nevertheless, there were many clear drawbacks:

- Lamps for this project's purposes were intended to be highly inefficient, consuming much power: the market progresses in the opposite direction, and considering the voltages at which the system works, it immediately appeared complex to find an available solution. More profound research showed that some suitable products existed but were old and out of stock.
- Even if it were possible to obtain such devices, maybe from the used market or old dismissed devices, it would have been difficult to ensure a constant current discharge from the battery, considering the resistive behavior of this kind of lamp.
- Lack of flexibility: more lamps could be placed in parallel to draw more current, but it would have been difficult to discharge at different rates.

Digital potentiometer

Looking at the easiness of design and the possibility of setting different discharge currents based on the test to be performed, a simple solution could be a potentiometer properly connected to the battery.

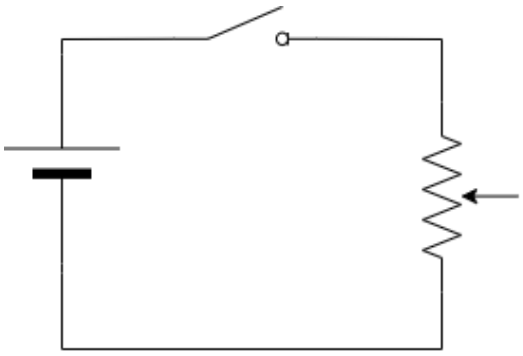


Figure 4.4: Potentiometer scheme

By setting the value of the potentiometer, it would have been possible to draw the desired current from the battery. The system would then have monitored the current as the battery voltage decreased to keep the discharge constant. This kind of design also allows targeting more complex discharge profiles by modifying the load to follow the desired current. Unfortunately, the available digital potentiometers on the main vendors' portals didn't meet the system requirements. They usually were in the order of magnitude of kΩ or tens of kΩ, therefore not allowing a suitable current for this project's purposes, even using more than one potentiometer in parallel. Finding a sufficiently small potentiometer to reach the desired values by driving several of them in parallel would have been possible, but the complexity would have become too high. However, despite the solution not being feasible, the idea of dynamically modifying the current discharged and even following a discharge profile appeared interesting. It was kept as a desirable feature for the rest of the design process.

Set of resistances

Similarly to the digital potentiometer concept, using several resistances in parallel with some switches to connect and disconnect them depending on the desired resistance value

appeared interesting.

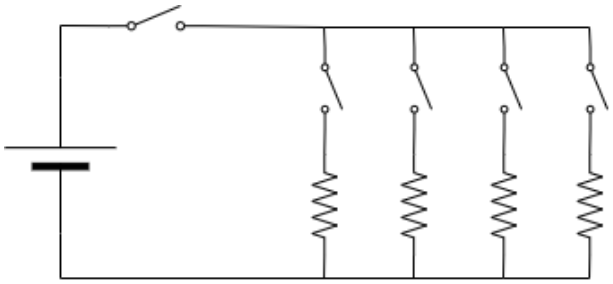


Figure 4.5: Set of resistors scheme

The system would have been able to dynamically change the load, compensating for the voltage variation of the battery and eventually following a discharge profile. The idea was basically to create a digital potentiometer from scratch. Some drawbacks led to discarding this solution too:

- Complexity quickly arose with few desired values, either by considering the addition of one resistor per desired current value or the need to calculate the parallel between many resistances at run time to adjust properly.
- A higher complexity also meant a difficult driving of the resistances due to the many parallel switches.
- The available current values would have been difficult to characterize due to tolerances.
- The discharge current options were coarse and quite irregular due to the various combination of different resistances. A net of resistors of the same value would have overcome this defect. However, providing the desired flexibility in terms of discharge options was hard.
- Power consumption was critical: for higher currents, very small resistors were needed, eventually as small as the series resistance of common switches, leading to huge measurement uncertainties.

LDO

Low-Dropout regulators provide a stable output voltage and a negligible current difference between input and output. An adjustable LDO could be used with the battery as input to provide a stable voltage on a suitable load (i.e., a resistor) to have a constant current discharge. [17]

The current on the load would have been determined by the voltage on the output, which could be set by a digital potentiometer and adjusted dynamically, as shown in figure 4.6

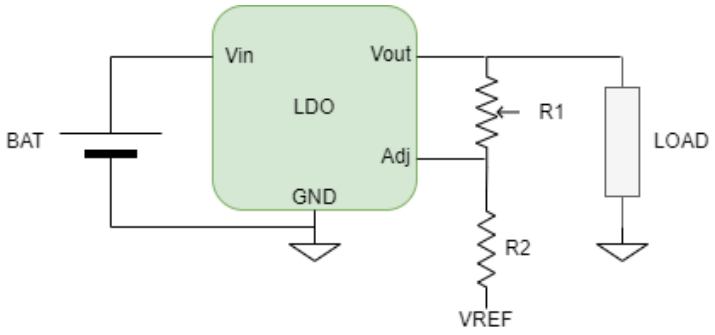


Figure 4.6: LDO Scheme

There were, however few clear drawbacks to this configuration:

- Power dissipation was huge and difficult to manage. [18]

$$P = (V_{in,avg} - V_{out,avg}) \times I_{in,avg}$$

$$with(V_{in,avg} - V_{out,avg}) > V_{droput,min}$$

- Low voltage swing available: significant dropout is present when higher currents are needed. The regulator output could typically swing between 1.2 V and 2 V at most for the desired currents, considering batteries that were discharged when their voltage got under 3 V.

If the chosen load granted a linear relationship between voltage and current, the ratio V_{MAX}/V_{min} must have been around 4 to have the desired current span. The main problem was V_{REF}, a bandgap fixed reference voltage of LDOs around 1.2 V for most available devices. Scaling the available voltage in the range of 0 to 800 mV would have granted the required V_{MAX}/V_{min} ratio.

Introducing configurations like voltage subtractors, the $I_{out} = I_{in}$ relationship was not maintained. Diodes could theoretically be used to lower the voltage on the load, but there weren't suitable ones. Different resistors could be used to target a specific discharge current but with higher complexity and cost.

While it was technically possible to lower the LDO V_{REF} by other means, providing an external reference and regulating the actual one by using proper resistors [19], complexity increased, and the power dissipation was still a problem difficult to overcome.

Still, the internal architecture of the LDO provided interesting insights which were taken into account for the following design steps.

Current sink

Considering the need for flexibility, the difficulty in finding plug and play solution able to satisfy every specification, and the huge operating range requested, the suitable choice was, finally, a current sink designed from scratch, stemming from the working principle of an LDO and its internal architecture. [17]

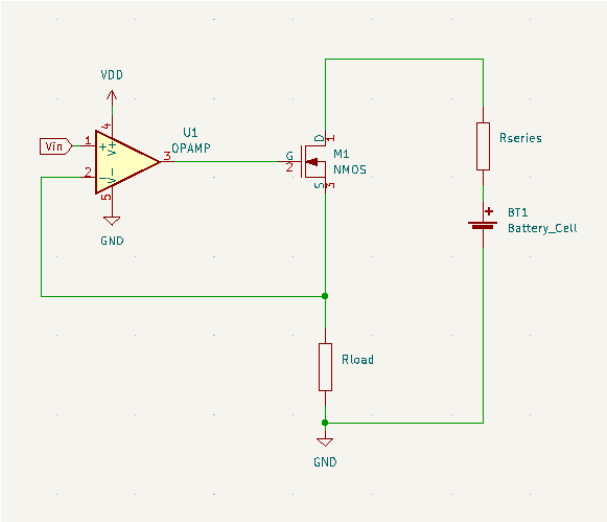


Figure 4.7: Basic current sink scheme

The circuit was rather simple: an op amp driving the gate of an nMOS, which was connected to the battery on the drain, to the inverting input and a load resistor on the source. The op-amp received an input voltage on the non-inverting input and adjusted its output until the voltage difference between the inputs was ideally zero. This meant that the voltage applied on the non-inverting input was the same voltage set on the resistor. Therefore the current sunk was V_{in+}/R. The MOS was needed to compensate for the variations in the battery voltage during discharge: no matter the drain voltage (i.e., the + battery voltage), as long as the MOS was in saturation region and the load resistance did not change, the drain current was constant, as well as the voltage on the resistor. The voltage variations fell on the V_{DS}, and the op-amp was in charge of adjusting its output accordingly, meaning it increased the V_{GS} if the V_{DS} decreased, guaranteeing the same current. It is worth noting that, although the system adjusted to meet the set current without needing external intervention, thermal drifts and disturbances might alter the actual current discharged. Therefore, a microcontroller was required to control the operating flow, monitor the physical quantities, and adjust the circuit inputs when needed. This system satisfied all the specifications: hardware simplicity, current sunk directly by the battery, decoupled battery and supply, and operating range. The simulation showed consistent behavior compared to the expected one.

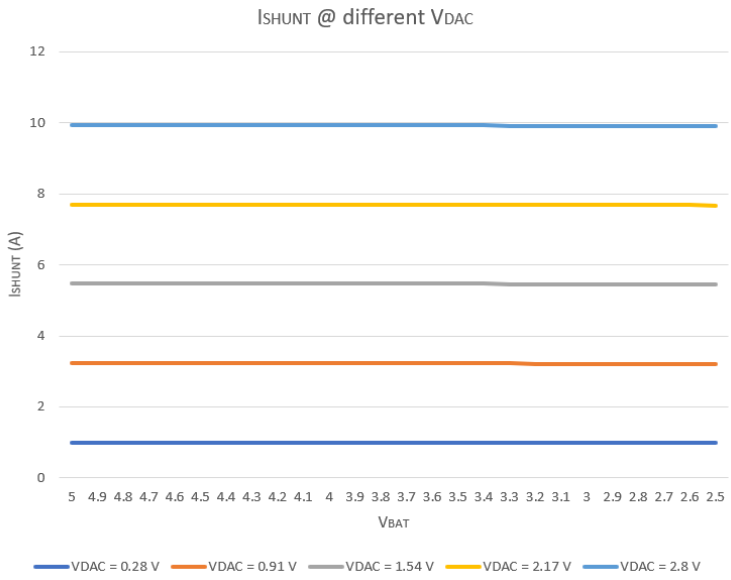


Figure 4.8: Current sink simulation at different V_{DAC} with variable V_{BAT}

Before any further analysis, the main concern about this topology feasibility was power dissipation:

- **nMOS power dissipation**: due to the currents that the device had to withstand, the MOS was highly solicited: power MOSFETs only had to be considered, along with a cooling system to prevent overheating.
- **Load resistor**: the resistor had to be low value for the same reason. Most commercial resistors cannot withstand such power. The chosen solution to overcome this problem was lowering the resistor value: considering a resistor of a few mΩ, power dissipation was still critical but could be handled. Choosing a resistor of such values also meant no need for a shunt resistor: it was used both as load and as shunt, reading its voltage to get the current value.

Brief research on the main components vendors confirmed that power dissipation, although critical, could be addressed with some attention in choosing the right components, available on the market without extraordinary costs and suitable for new designs. Further simulations confirmed an appropriate behavior for the desired application. The current sink was, in the end, the choice for the continuation of the project, starting from this simple topology to add features according to the system specification and tuning until satisfactory results were met.

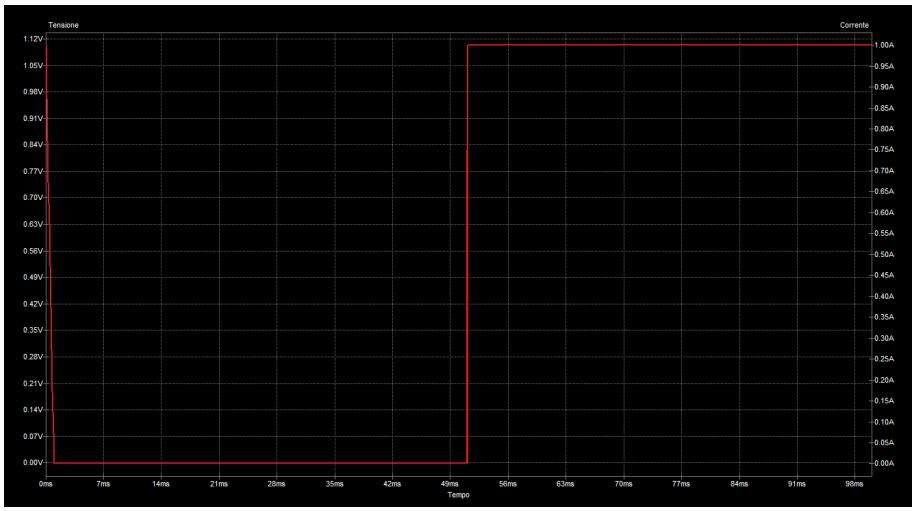


Figure 4.9: Discharge current, response to DAC step

4.2.2 Current sink design

Starting from the chosen current sink topology, some features and components were added to better meet the project requirements.

Feedback resistors

The first modification to the simple current sink topology was the addition of a feedback network. This provided some flexibility concerning the ratio between the inverting input and the actual resistor voltage.

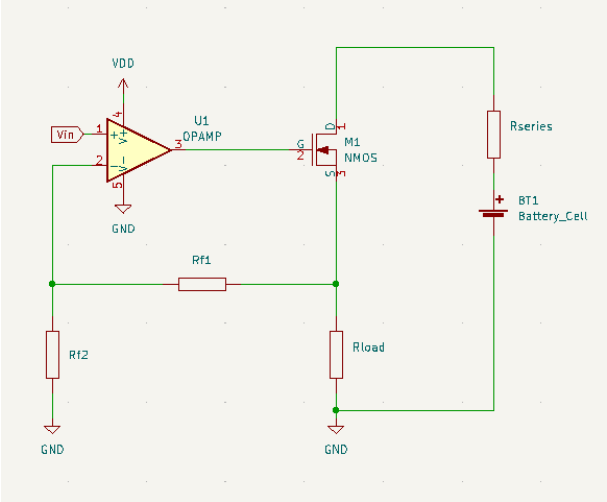


Figure 4.10: Current sink with feedback resistors

$$I_{BAT} = I_{DS}$$

$$I_{shunt} = I_{DS} \times \frac{R_{f1} + R_{f2}}{R_{shunt} + R_{f1} + R_{f2}}$$

$$V_{shunt} = I_{shunt} \times R_{shunt}$$

$$V_{-} = V_{shunt} \times \frac{R_{f2}}{R_{f1} + R_{f2}}$$

$$V_{-} = V_{+}$$

$$I_{BAT} = V_{+} \times \frac{R_{f1} + R_{f2}}{R_{shunt} \times R_{f2}} \times \frac{R_{shunt} + R_{f1} + R_{f2}}{R_{f1} + R_{f2}}$$

Switch

The system had to be able to disconnect the load from the battery, either for safety reasons or to allow to charge the battery, activating the charging and discharging section alternatively. Simply setting the op-amp input to 0 V was not sufficient: theoretically, with 0 V on the non-inverting input, the inverting input should have been at 0 V, too; to obtain such a result, the op-amp output would have been low enough to have the MOS below the threshold, actually disconnecting the discharge circuit from the battery. However, with the MOS open, the system would have been open loop. Therefore, low voltages and disturbances, along with the op-amp offsets, would have made the op-amp saturate, the MOS conducting, and put the system at risk.

The position of the switch itself was not trivial. A high-side switching was not possible: brief research of available components showed a lack of pMOS switches or relays that were through-hole, could withstand currents up to 10 A, and worked at the system's supply voltages. On the other hand, a suitable low-side switch could be found on the market but presented other critical issues: its series resistance was comparable to the shunt and quite variable; measurements and loop performance would the be significantly affected, making the regulation slower and more difficult. The final choice was to put the switch on the op-amp output. This solution brought the gate voltage to 0 when the switch was on, effectively disconnecting the discharge section from the battery. The simulation showed proper behavior, except for some driving problems due to the op-amp being shorted to ground when the switch was on. This was addressed by adding a resistor on the op-amp output.

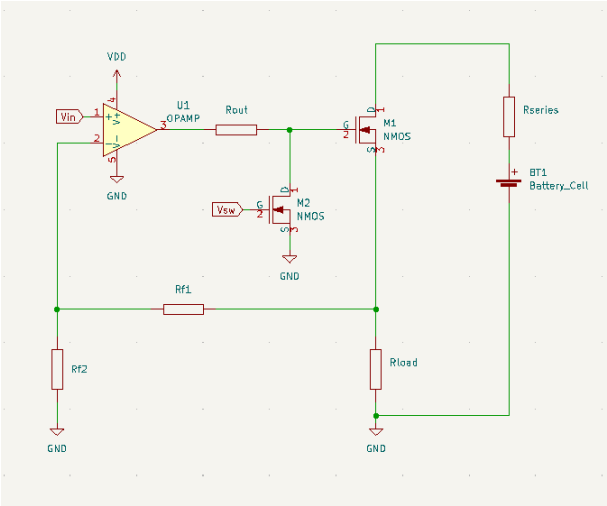


Figure 4.11: Current sink with switch

Inputs and outputs

The circuit needed to interface with a microcontroller in charge of controlling the operations of switching on and off the load, setting the proper current value, and acquiring data. It is worth noting where the circuit interacted with the micro:

- **Current setting**: the proper current value could be set by applying a certain voltage on the non-inverting pin of the op-amp. Such value could be provided via a DAC output.
- **Current sensing**: the actual discharge current could be calculated from the shunt voltage. Therefore, the shunt could be connected to one of the ADC inputs for the micro to obtain this value.
- **Voltage sensing**: the battery voltage had to monitored during the whole test for characterization and safety purposes. Again, this voltage was provided to an ADC channel.

Every input and output had to be decoupled, either by internal buffers provided by the microcontroller or external ones. Moreover, the shunt voltage was likely very low and needed amplification.

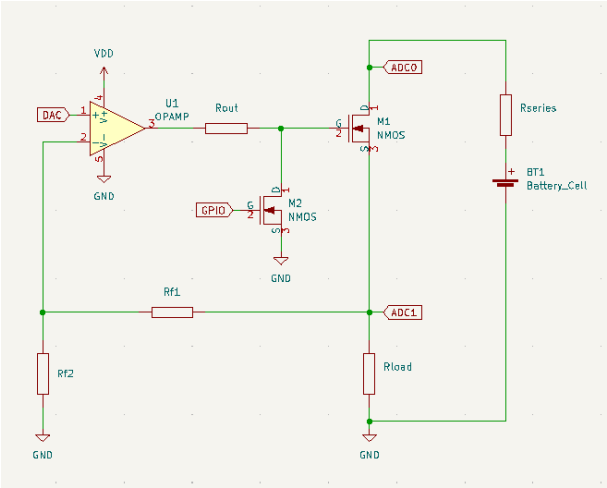


Figure 4.12: Current sink with input/output labels

4.2.3 Components choice

The components were chosen following low-budget criteria and restricting, where possible, to through-hole mounting, considering the goal to prototype on breadboard and stripboard.

Board

The board was the starting point of the design: Nucleo STM32 boards were chosen because they offered a smart, user-friendly environment for firmware development, along with a rich set of peripherals allowing the necessary operations for this project's scope: ADC, DAC, GPIOs, UART. [20] Specifically, NUCLEO-G0B1RE was chosen since it offered the necessary features at a low-cost and was immediately available for purchase and delivery.

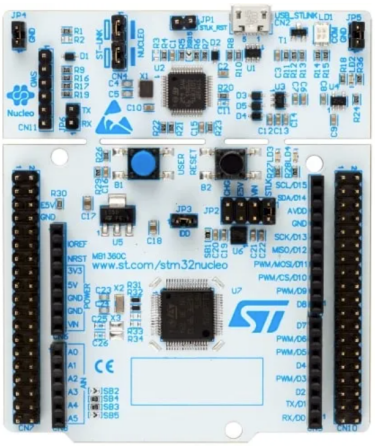


Figure 4.13: NUCLEO-64 STM32 Nucleo-G0B1RE [21]

Generic features:

- ST-LINK USB V_{BUS} or external power supply
- Micro-USB connector for ST-LINK
- On-board ST-LINK debugger/programmer
- Free software libraries
- Output supply: 5 V or 3.3 V output pins can be used as a single supply for the system. [22]

The microcontroller equipped on the chosen board is STM32G0B1RET6. Based on the high-performance Arm® Cortex®-M0+ 32-bit RISC core, operating at frequencies up to 64 MHz, this microcontroller offers extensive integration capabilities suitable for various applications in consumer, industrial, and appliance domains, as well as Internet of Things (IoT) solutions. [20]

- LQPF64 package
- Supply: 1.7 V to 3.6 V
- Low power
- -40 to 125 °C operating temperature range
- Low-power RTC
- Internal voltage reference buffer
- Clock: 4 to 48 MHz crystal oscillator
- Memory: memory protection unit (MPU); high-speed embedded 144 kB SRAM, up to 512 kB Flash with read protection, write protection, proprietary code protection, securable area; DMA
- Communication: 3 I2Cs, 3 SPIs, 1 full-speed USB, 2 FD CANs, 6 UARTs
- Analog/Digital conversion: 14 external + 3 internal 12-bit ADC channels, 2 12-bit DACs
- Timers: PWM, general-purpose
- GPIO: 60 pins; push-pull or open-drain as output; with or without internal pull-up or pull-down as input; FT GPIOs are 5 V tolerant [20]

It is worth discussing further about the ADC since it had a crucial role in the system's functioning. The ADC is a 12-bit analog-to-digital converter based on a SAR and can operate up to 2.5 MSps on 14 external + 3 internal channels, as previously mentioned. It also has a hardware oversampler of up to 256 samples, up to 16 effective bits. It can be triggered by timers or I/O. It can generate interrupts and DMA requests. [20]

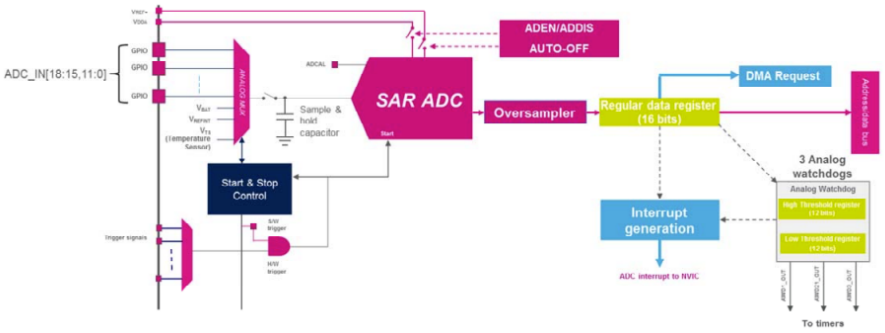


Figure 4.14: ADC block diagram [23]

Its reference voltage can be the supply, set by default, an external supply source, or the VREFBUF internal buffer. VREFBUF is an LDO regulator which can be adjusted to 2.048 V or 2.5 V. It provides a very accurate and stable voltage reference. [20] Since using a lower voltage reference for analog blocks allow for better quantization, the 2.048 V was chosen. [24]

$$Quantizationstep(3.3V_{REF}) = \frac{V_{REF,3.3}}{2^{12}} = 0.8mV$$

$$Quantizationstep(2.048V_{REF}) = \frac{V_{REF,2.048}}{2^{12}} = 0.5mV$$

The 2.048 V reference improved the quantization step amplitude by about 37%. To set the 2.408 V reference, a modification had to be made on the board by desoldering a bridge.

Shunt resistor

The main factors to consider for the shunt choice were power rating, minimum shunt voltage, tolerance, and thermal coefficient.

First of all, the power dissipated by the resistor is

$$P = I^2 \times R$$

The lower the resistor, the lower the power dissipation, the lower the heating.

On the other hand, higher shunt values allowed for a better quantization compared to the measurable LSB of the ADC, and a very low resistor would have meant very low voltages, with negative effects on measurement accuracy. The suitable range considering the values and power ratings available on the market, was 10-100 mΩ. Above 40 mΩ, however, the resistors found on the market at low prices had higher tolerances, from 5% upwards, while lower value resistors usually had 1% tolerance. SMD resistors offered more options but required higher mounting complexity and different support than a stripboard.

With the 12-bit ADC resolution, the $2.048V$ voltage reference, and a resistor between 10 mΩ and 40 mΩ, $V_{LSB}/V_{shunt,min}$ spanned between 1.25% and 5% considering currents down to 0.5C, while it went up to 10% considering 0.2C discharge.

Considering that the higher current ranges were more interesting from a characterization point of view and implied higher power dissipation and higher sensed voltages, the final choice was a 10 mΩ resistor.

Finally, the temperature coefficient: it was crucial that the resistor didn't heat up to a point where its resistance value changed significantly. The shunt value was considered a fixed value for the current regulation, so every change was a term of error: the DAC would have set a wrong value, resulting in a different discharge current than intended.

Temperature coefficient indicates in ppm/°C the variation. A TCR below 100 ppm/°C was enough to have a maximum drift of 1% from the nominal value over an 80°C range.

The starting idea was to use a wire-wound resistor for robustness and easiness of mounting and dissipating heat. However, they were either expensive or had higher tolerances. A considered suitable example is the THS10R10J resistor.

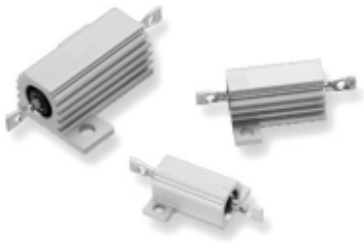


Figure 4.15: TE THS series wirewound resistors [25]

- Resistance: down to 10 mΩ
- Power rating: @25°C
  - with Heatsink: 10 W
  - without Heatsink: 5.5 W
- Tolerance: 5%
- Temperature coefficient: 50 ppm/°C

[25]

Then, considering the choice of a 10 mΩ resistor, which implied a power dissipation of up to a few W only, heat dissipation became less critical, and it was possible to consider a different kind of resistors, better suiting the system's requirements. Specifically, open-air resistors, which didn't need active dissipation. The OAR3R010FLF resistor satisfied all the requirements.

Figure 4.16: TT Electronics OAR resistor [26]

- Resistance: down to 2.5 mΩ
- Power rating @85°C: 3.0 W
- Tolerance: 1%
- Temperature coefficient: 20 ppm/°C [26]

Additionally, the eventual heat was concentrated in a hotspot properly isolated from the circuit.[26]

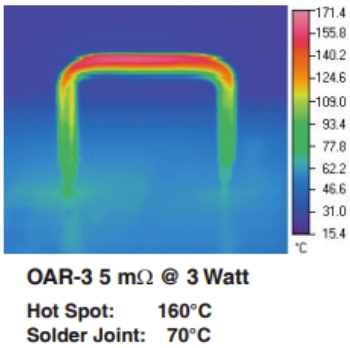


Figure 4.17: TT Electronics OAR hotspot [26]

Load MOS

The first element to consider for the MOS choice was its I-V characteristics. The MOS had to be in saturation for its intended purposes: I_{DS} had to be constant along the battery voltage range. Moreover, available V_{GS} values had to be able to determine the full current range specified by the requirements. Considering that the MOS gate was driven by the op-amp, supplied by the NUCLEO 5 V port, the desired current range had to be obtained with a V_{GS} between 2 V and 4 V, keeping some margin over the rails. At the same time, the minimum threshold voltage could be too low because of the need to switch off the discharge section by setting a below-threshold gate voltage. Through-hole nMOS of this kind were available with minimum threshold voltages around 1 V and a required V_{GS} between 2 V and

3 V for the corresponding drain current range. Then, power dissipation had to be taken into account. The nMOS acted as a dynamic load and was responsible for most system power dissipation. The drain-source current corresponded to the discharge current, so it could be as high as 10 A. At the same time, the V_{DS} was almost equal to the battery voltage, as the shunt voltage was very low. With a worst-case battery voltage of 5 V and 10 A discharge current, the nMOS had to dissipate roughly:

$$P = 5V \times 10A = 50W$$

Power MOSFETs available on the market could usually withstand such power, remaining in the SOA, provided the heat was properly dissipated. Through-hole ones also typically offered a metal tab on the drain that allowed them to be easily attached to a heatsink. To better address power dissipation problems, two nMOS were placed in parallel, ideally splitting in half the power each one had to dissipate.

The IRL3803PBF nMOSFET was chosen since it was the cheapest available power MOS compliant with the specific.

Figure 4.18: IRL3803PBF MOSFET [27]

- I_D max: 140 A
- $R_{DS,ON}$ max: 9 mΩ
- Power rating @25°C: 200 W
- $V_{GS,th}$ min: 1.0 V
- V_{GS}, I_D @25°C: 2.0 V , 0.04 A ; 3.0 V , 11 A
- Thermal resistance:
  - Junction-to-Case: max 0.75 °C/W
  - Case-to-Sink: typ 0.50 °C/W
  - Junction-to-Ambient: max 62 °C/W

  [27]

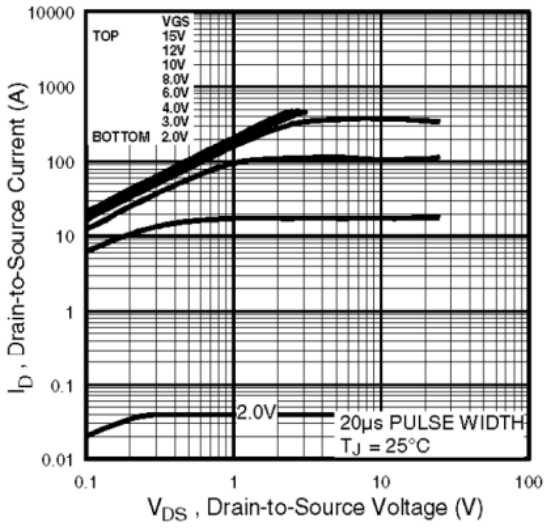


Figure 4.19: IRL3803PBF Characteristics [27]

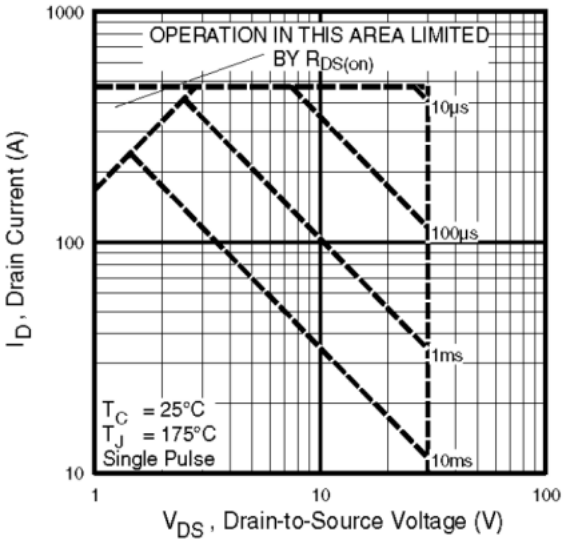


Figure 4.20: IRL3803PBF SOA [27]

Heatsink

The heatsink was taken from a used PC. The MOS metal tab could be screwed into the heatsink and actively cooled with a vent. The active dissipation appeared excessive com-

pared to the system's needs; however, it allowed a safer approach in case of overheating.

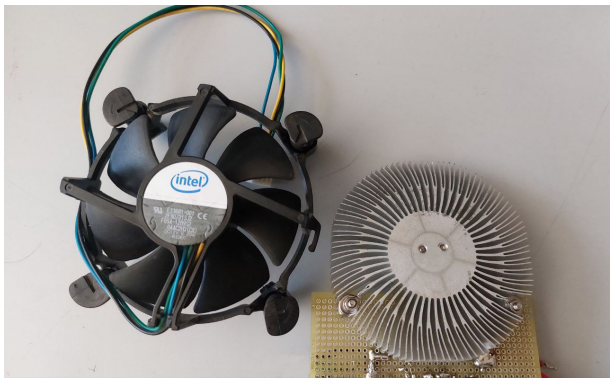


Figure 4.21: Heatsink

Driving opamp

The operational amplifier responsible for the load driving had to be single supply (5 V) and have a low input offset voltage, which limited the minimum current that could be set. Although not strictly necessary, additional parameters considered were the Gain-Bandwidth product and whether it was rail-to-rail. The first choice was the MCP6241 because of its availability and low cost.

Figure 4.22: MCP6241 [28]

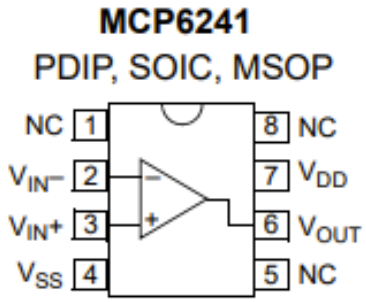


Figure 4.23: MCP6241 pinout [28]

- Supply voltage: 1.8 V to 5.5 V
- Rail-to-Rail Input/Output
- Output Short Circuit Current: Continous
- Max Current at Output and Supply Pins: ±30 mA
- Input Offset Voltage: ±5.0 mV [28]
- Gain Bandwidth Product: 550 kHz

However, a simple laboratory test on the component showed that the input offset voltage on some parts was higher than expected, up to 10 mV. This could not be acceptable, as it prevented the voltage on the inverting input from going lower than that value even if the non-inverting input was zero, resulting in a bound on the minimum discharge current (500 mA, corresponding to around 5 mV on the inverting input, depending on the feedback resistors).

Another component was then chosen for the final implementation: MCP6022. At the cost of a higher price, still not much more significant compared to the total cost, it provided very low offset along with a much higher Gain-Bandwidth product.

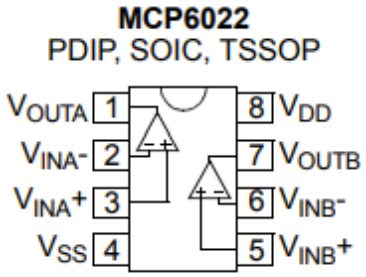


Figure 4.24: MCP6022 pinout [29]

- Supply voltage: 2.5 V to 5.5 V
- Rail-to-Rail Input/Output

- Two op-amps per package
- Output Short Circuit Current: Continous
- Max Current at Output and Supply Pins: ±30 mA
- Input Offset Voltage: ±500 μV [28]
- Gain Bandwidth Product: 10 MHz [29]

Sensing opamp

The MCP6022 was suitable for battery voltage sensing thanks to its low input offset. However, it was not low enough to provide accurate sensing for the discharge current. The shunt voltage could be as low as 5 mV, and no matter the amplification, the input offset voltage was an error term that couldn't be nullified easily and, at the same time, was not negligible, implying by itself a relative error of about 10%. Through-hole op-amps compliant with these requirements were unavailable on the market; hence, the search was broadened to SMD components, along with a PCB to adapt the SOT-23 package to a stripboard. The NCS21801SN2T1G offered an extremely low input offset voltage at a very low price, allowing to mitigate the extra expense of the SOT-23 adapter, available in the PCB3007-1.

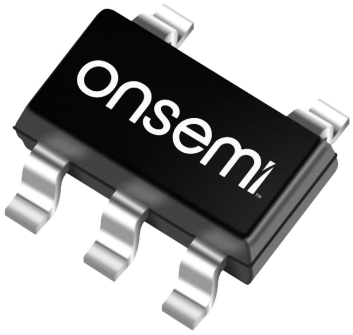


Figure 4.25: NCS21801SN2T1G [30]

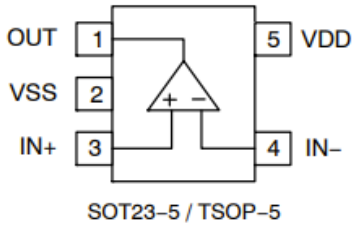


Figure 4.26: NCS21801SN2T1G pinout [30]

- Supply voltage: 1.8 V to 5.5 V

- Rail-to-Rail Input/Output
- Output Short Circuit Current: Continous
- Max Current at Output and Supply Pins: ±10 mA
- Input Offset Voltage: ±10 muV
- Unity Gain Bandwidth: 1.5 MHz [30]

Figure 4.27: PCB3007-1 SOT to DIP adapter [31]

Switch

The switch didn't have particular constraints except for a sufficiently low threshold voltage to allow effective driving from a GPIO. The IRLU024NPBF had a max threshold voltage of 2 V, meaning that the output of a GPIO was well above the necessary voltage to switch it on effectively.

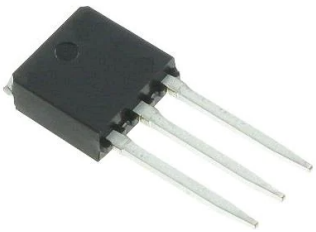


Figure 4.28: IRLU024NPBF [32]

- I_D max: 17 A
- $R_{DS,ON}$ max: 65 mΩ
- Power rating @25°C: 45 W
- Fast switching
- $V_{GS,th}$ min: 1.0 V
- $V_{GS,th}$ max: 2.0 V

- V_{GS}, I_D @25°C: 2.0 V , 0.04 A ; 3.0 V , 11 A
- Thermal resistance:
  - Junction-to-Case: max 0.75 °C/W
  - Case-to-Sink: typ 0.50 °C/W
  - Junction-to-Ambient: max 62 °C/W

  [27]

4.2.4 Conditioning circuits

The circuit could not interact directly with the microcontroller. Every input and output had to be properly conditioned to the suitable value range and also to decouple and address load effects.

DAC

The DAC had to be able to provide a voltage on the non-inverting input of the op-amp ranging from hundreds of mV down to a few mV. A voltage divider was placed between the DAC and the op-amp input to exploit the whole DAC range and have better resolution and accuracy in the voltage setting. The DAC's output impedance is in the order of the tens of kΩ, so it would have affected the equivalent resistance. The circuit had to be decoupled: the DAC is provided with an internal buffer; however, this causes a loss in performance, particularly because it limited the lowest voltage the DAC can reach. [20] Therefore, an additional operational amplifier was inserted between the DAC and the divider.

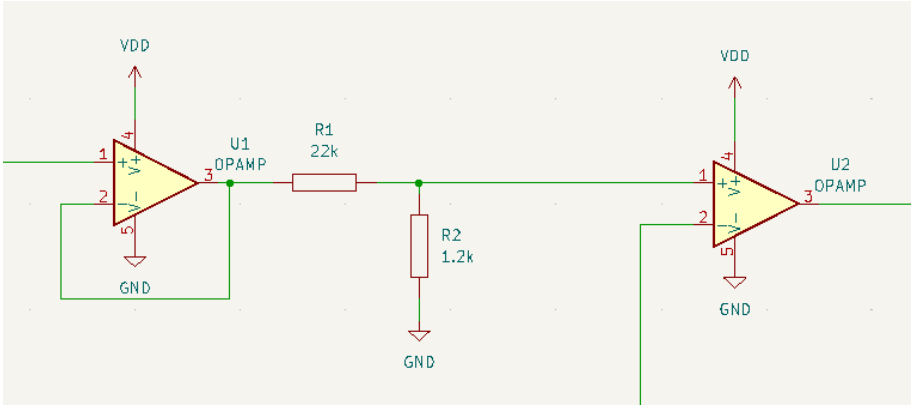


Figure 4.29: DAC conditioning circuit

Switch

The switch didn't need additional hardware. As long as the threshold voltage was sufficiently low, the microcontroller GPIOs could drive the switch correctly.

Battery voltage

For battery voltage sensing, more attention was required. First of all, the ADC input had to be decoupled from the circuit. This was accomplished simply by inserting an operational amplifier in voltage follower configuration between the battery's positive terminal and the input pin. Then, the ADC range had to be considered: considering a battery voltage as high as 5 V and the ADC reference value of 2.048 V, a voltage divider had to be added. The partition factor chosen was 2.5 to have nearly the maximum ADC voltage for the maximum battery voltage. Then again, the interaction between the GPIO input resistance, in the order of the tens of kΩ, and the voltage divider had to be considered. One simple solution would have been to put high resistances for the divider and put the op-amp between the divider and the GPIO. However, no matter how large the resistors might be, this would have implied a constant leakage current on the divider, equal to V_{BAT}/R_{series}. Moreover, the charger behavior would have likely been altered.

Another option could have been adding another operational amplifier as a second buffer between the divider and the GPIO. The added error term would have been equal the operational amplifier's input offset voltage.

The alternative was to carefully choose the resistors: sufficiently high to meet the output current constraints of the op-amp but low enough to have negligible interaction with the ADC input. Considering the circuit was going to be built on a stripboard, and the op-amp voltage offset could be significant compared to the measurement, the latter option was chosen. The chosen resistors were 220 Ω and 330 Ω. Experimental verification showed that the measure was sufficiently accurate compared to the measurement instrumentation accuracy.

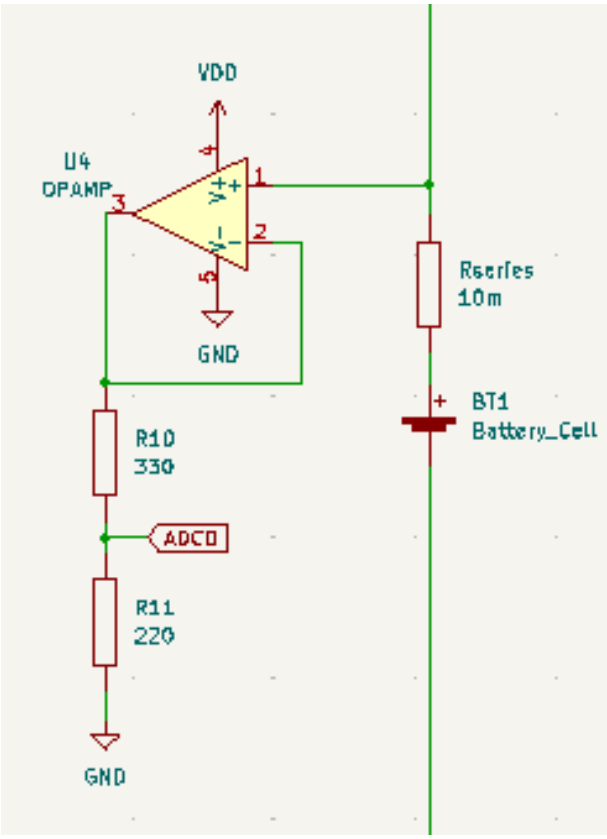


Figure 4.30: V_{BAT} conditioning circuit

Discharge current

For the discharge current sensing, decoupling and amplification were needed. Considering the huge difference between the shunt and the input ADC resistance (mΩ and kΩ respectively), the load effect was negligible. However, keeping in mind that the voltage was taken on a critical node (load MOS source, regulating op-amp non-inverting input), it was worth placing an op-amp to avoid any interaction. Moreover, the shunt voltage was very low and would have resulted in unacceptable accuracy without proper conditioning. An op-amp was then placed as a non-inverting amplifier, with a gain of about 20: the maximum shunt voltage, 100 mΩ, corresponding to 10 A (2C), was amplified to the full ADC range, around 2 V, while the lowest shunt voltage, considering the system specifications, 5 mV, corresponding to 500 mA (0.2C) was amplified to 100 mV, which was the threshold to obtain an acceptable ADC error.

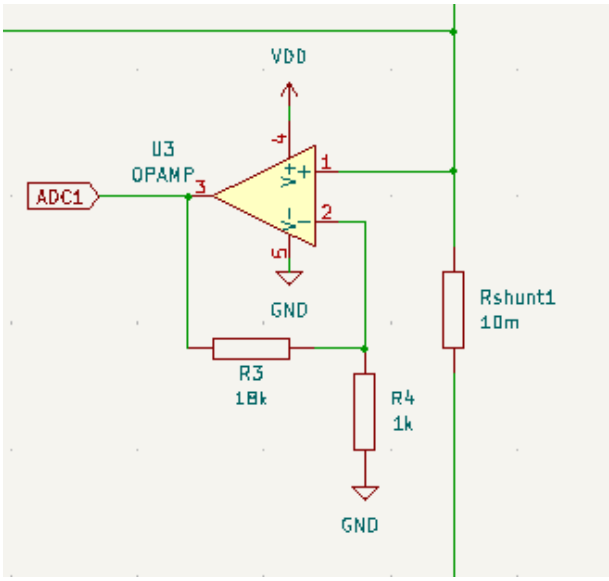


Figure 4.31: V_{SHUNT} conditioning circuit

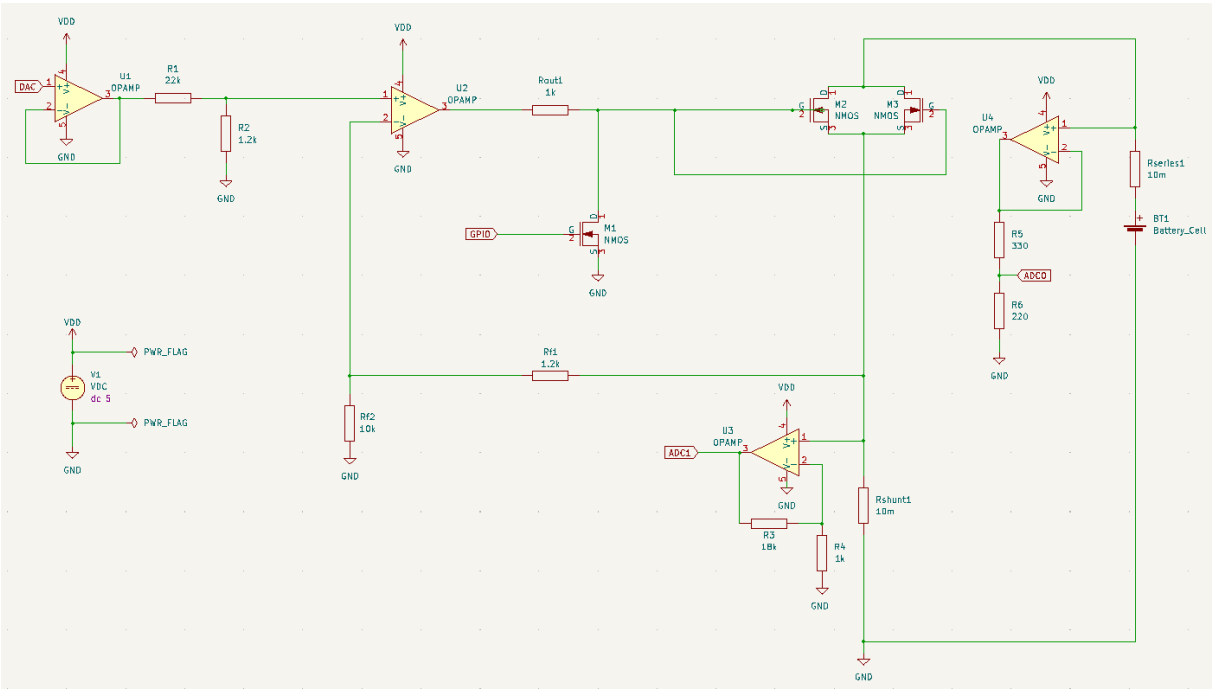


Figure 4.32: Current sink with conditioning circuits

4.2.5 Surge current prevention

DAC steps

Fast variations on the non-inverting input of the op-amp might lead to unexpected current values. The current loop response was not instantaneous: the op-amp output increased to let more current flow in the MOS and raise the inverting input voltage; however, the op-amp output kept rising for a short time after the right inverting input voltage was reached, due to the delay between the output adjustment and the effective voltage rise. Because of the low shunt resistor value, these slight delays might cause huge battery current spikes and ringing. A capacitor was inserted on the non-inverting pin to prevent this, creating an RC net on the DAC output. This RC slowed down the DAC transition and smoothed the waveform, preventing the current peaks. The added delay was negligible compared to the goals of this project. A suitable value for the capacitor was 10 nF, as confirmed by simulation. As an additional precaution, no DAC steps higher than 0.3 V were allowed in firmware.

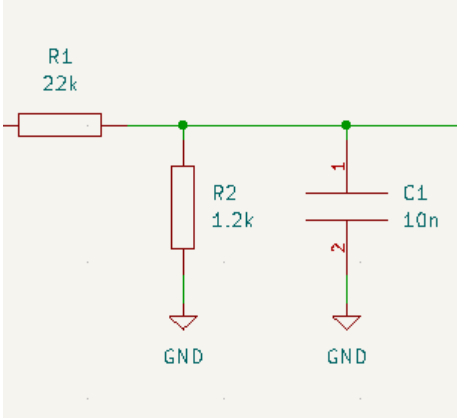


Figure 4.33: DAC RC circuit

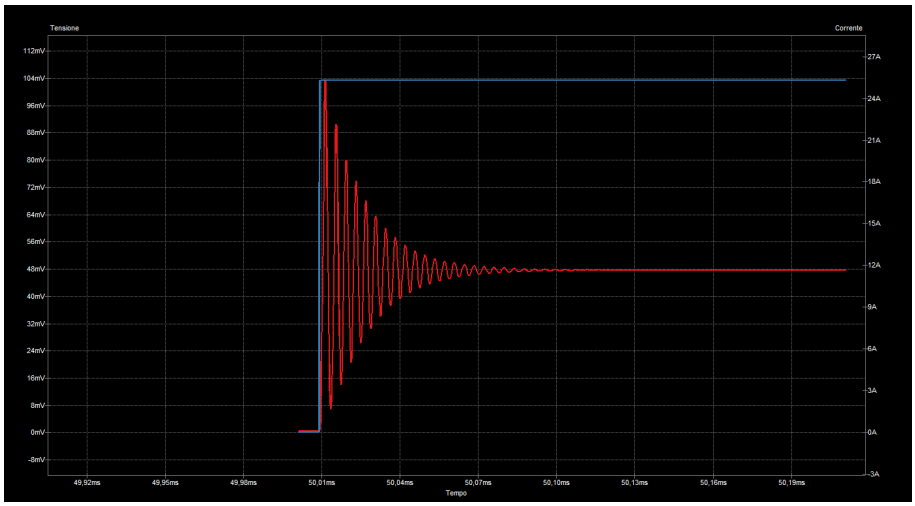


Figure 4.34: Discharge current response to DAC step, without C1

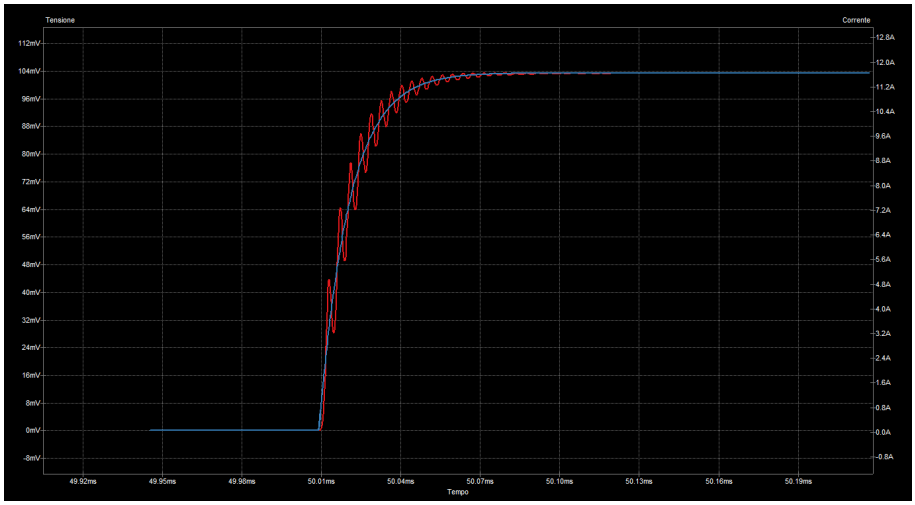


Figure 4.35: Discharge current response to DAC step, with C1

Switch transitions

The load switch represented another source of current peaks: the transitions were critical and posed a threat to the functioning of the circuit, challenging to solve as well. The behavior was analyzed separately for OFF-ON switch transitions and ON-OFF ones (switching the load from ON to OFF and vice versa).

- **OFF-ON switch transitions**: the gate voltage is brought to 0 when the switch closes, actually disconnecting the load from the battery. The loop is open, and the op-amp saturates. A low current flows through the op-amp output resistor. The gate

capacitance of the load and drain-source capacitance of the switch are discharged to ground.

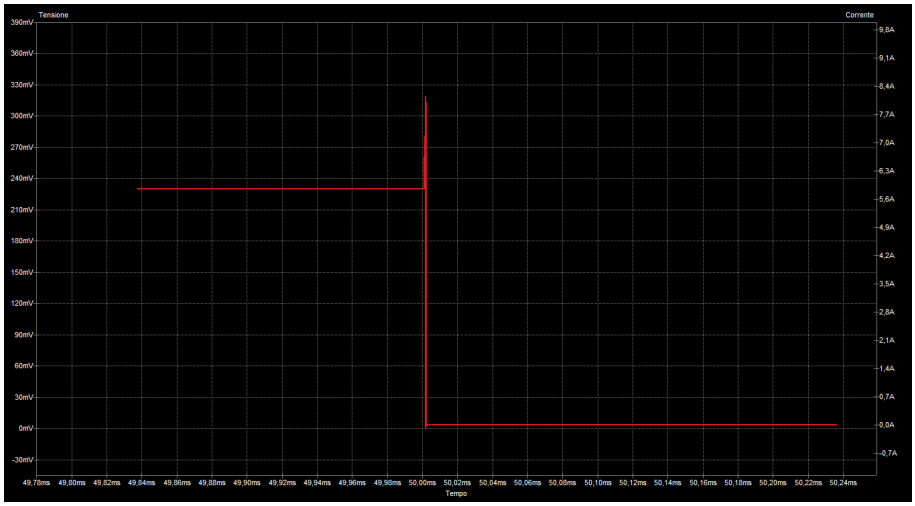


Figure 4.36: Discharge current response to switch OFF-ON transition

- **ON-OFF switch transitions**: the gate voltage rises as the parasitic capacitance is charged. When the gate voltage reaches V_{th}, the nMOS load starts conducting, the loop closes, the shunt voltage increases, and so does the inverting-input voltage, the op-amp output voltage decreases until the V_{GS} is correct to obtain the desired shunt current.

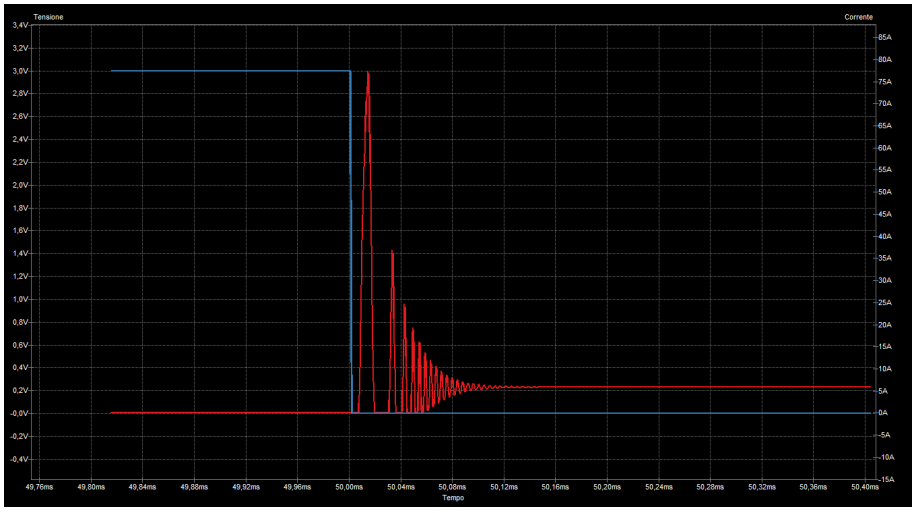


Figure 4.37: Discharge current response to switch ON-OFF transition

The ON-OFF switch transition was particularly critical: the op-amp output did not get

immediately to the correct value when the loop closed, and during this time, the V_{GS} increased over the desired value, possibly implying unsafe currents. Considering the peaks were caused by the excessive gate voltage rise, which was influenced by the loop latency between adjusting the op-amp output and the actual change in the op-amp's inverting input voltage, it could be deduced that:

- Increasing the op-amp output resistance, the peak decreased, but the ringing was more accentuated and persisted longer.

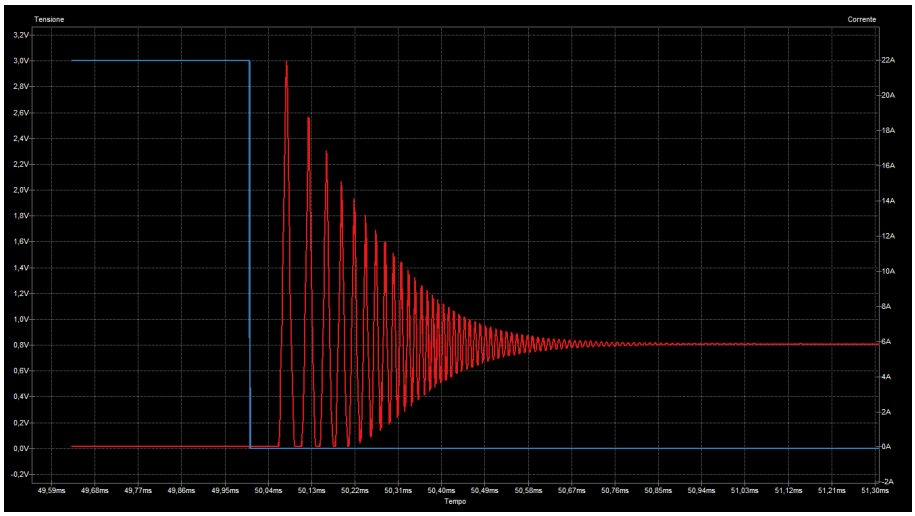


Figure 4.38: Discharge current response to switch ON-OFF transition, $R_{OUT} = 10k\Omega$

- Increasing the value of the shunt resistor resulted in reduced peak values. This was because the surplus voltage remained relatively constant in absolute terms but had a lesser impact on the current value. So, at the cost of higher resistor uncertainty, considering the availability of the components on the market, and power dissipation, a wire-wound resistor of 100 mΩ could significantly lower the spikes, as confirmed by simulation.

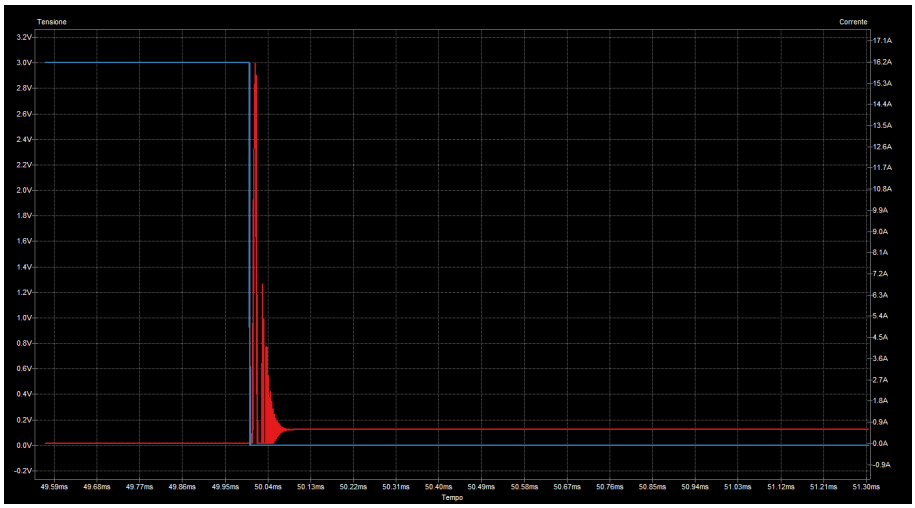


Figure 4.39: Discharge current response to switch ON-OFF transition, $R_{SHUNT} = 100m\Omega$

Although promising, this result was of no help considering the spikes likely harmed the circuit in any case.

Snubber

This problem could possibly be tackled by modifying the voltage waveform at the op-amp output during transitions. By slowing down the gate voltage rise, it was possible to obtain lower peaks. A solution to accomplish such a result was the addition of a snubber circuit across the switch: a small resistor was placed between the switch drain and the load gate and a capacitor in parallel to the switch drain-source, starting with 100 Ω and 100 nF. A small resistor was also placed on the switch drain to prevent the snubber capacitor from being almost shorted to ground.

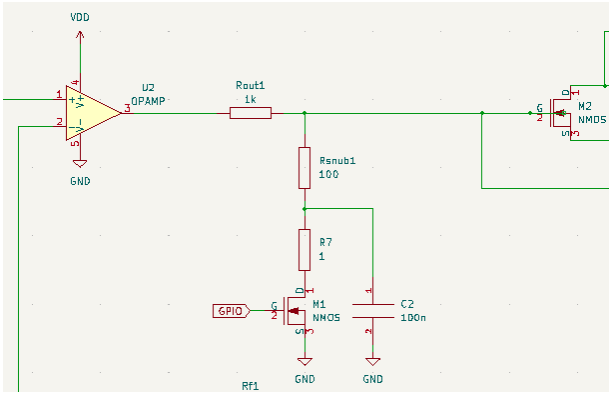


Figure 4.40: Snubber circuit

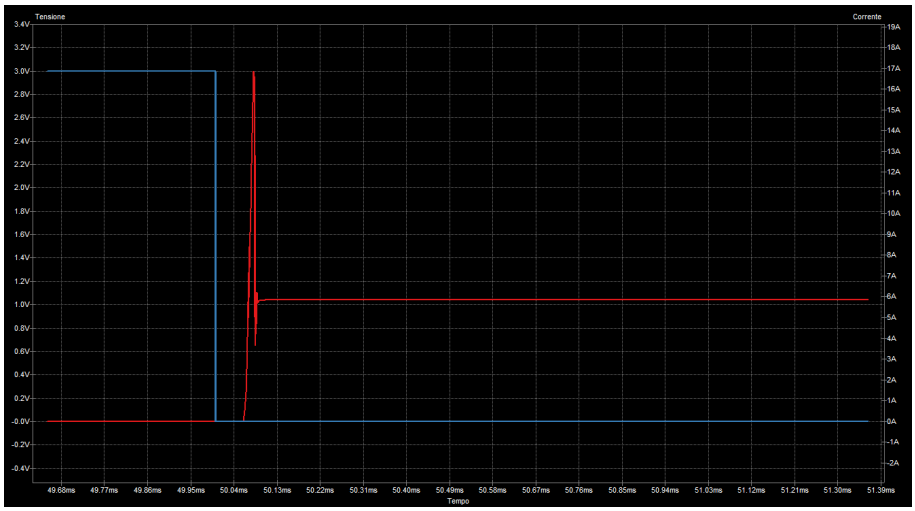


Figure 4.41: Simulation with snubber, $C2 = 100nF, R_{snub} = 100\Omega$

The peaks were significantly reduced, and better results could be obtained by properly tuning the values. It had to be taken into account that the resistor value was bound: when the switch was closed, the voltage drop on the resistor was almost equal to the gate voltage; therefore, to guarantee that the nMOSFETs load were OFF, it had to be:

$$V_{out} \times R_{snub}/R_{snub} + R_{out} < V_{th,min}$$

with $V_{th,min} = 1$ V, as stated by the nMOS datasheet and $V_{out} = 5$ V, given that the op-amp saturated. It is worth noting that the op-amp output might be lower if sourcing its maximum current (i.e., with lower resistances), but in this case, the current was about 5 mA. So:

$$R_{snub} < R_{out} \times \frac{V_{th,min}}{V_{out} - V_{th,min}}$$

$$R_{snub} < 250\Omega$$

A trial and error approach was adopted, bearing in mind that:

- A higher op-amp output resistance lowered the peaks but increased delay.

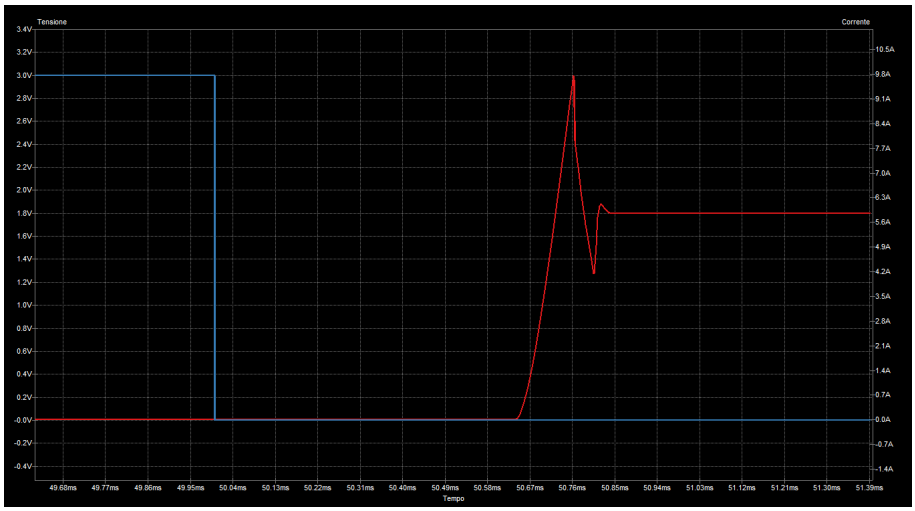


Figure 4.42: Simulation with snubber, $R_{OUT} = 10k\Omega$

- A lower snubber resistor accentuated both peaks and ringing.

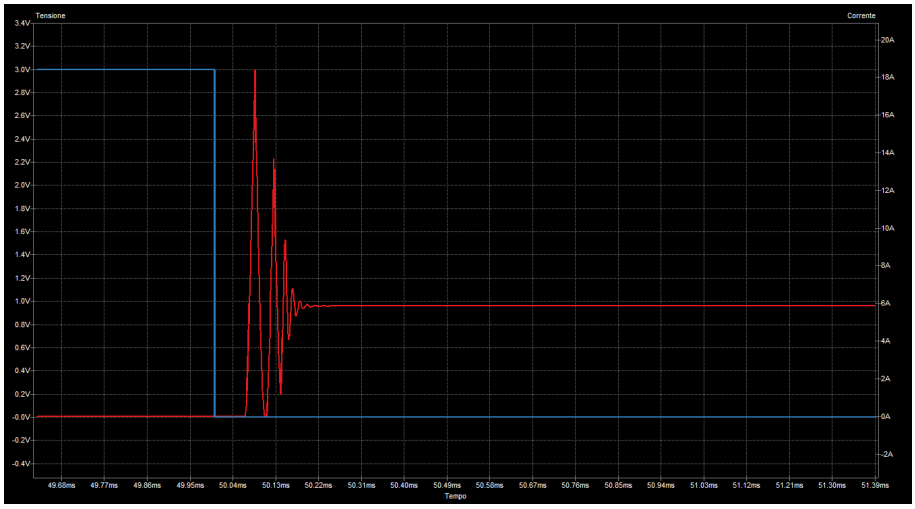


Figure 4.43: Simulation with snubber, $R_{snub} = 10\Omega$

- A higher capacitor improved both peaks and ringing but increased delay.

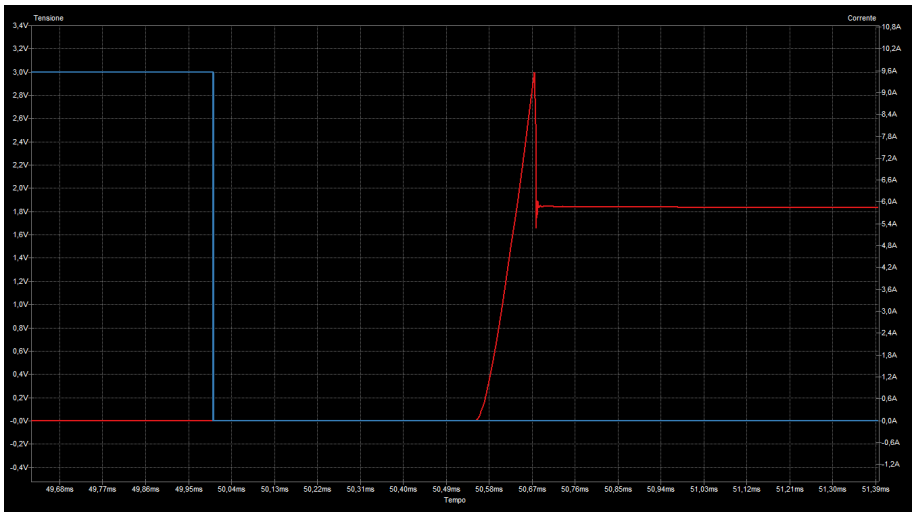


Figure 4.44: Simulation with snubber, $C2 = 1\mu F$

A slight improvement could also be seen by removing the feedback resistor network. Since these resistors provided some flexibility in the ratio between the input and shunt voltage but were not crucial to the correct functioning, they were definitely removed to simplify the circuit.

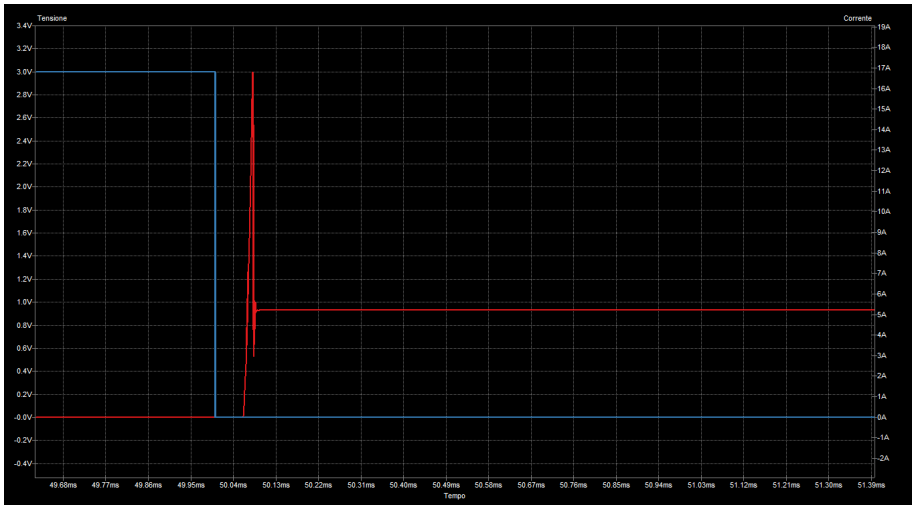


Figure 4.45: Simulation with snubber, no feedback resistors

Despite being unable to solve the peak problem at its root, this configuration was able to mitigate their effect by keeping them under the critical values for battery safety. A suitable configuration was found with a capacitor of 470 nF, a value high enough to have significant effects on the peaks but not too large, in order to avoid managing a capacitor in the order of uF in such a critical section of the circuit.

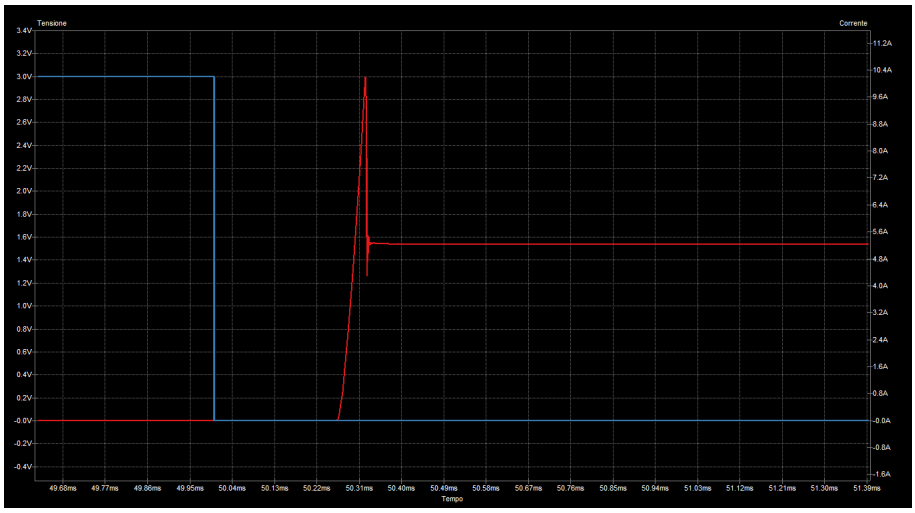


Figure 4.46: Simulation with snubber, C2 = 470 nF, $R_{snub} = 100\Omega$

It's interesting to note that although the absolute value of the peaks increased, their relative magnitude decreased in proportion to the current itself. For instance, at 500 mA, the peak corresponded to about 1100% of the current value (5.5 A peak), whereas around 10 A, it accounted for only about 150% of the current value (15.5 A peak).

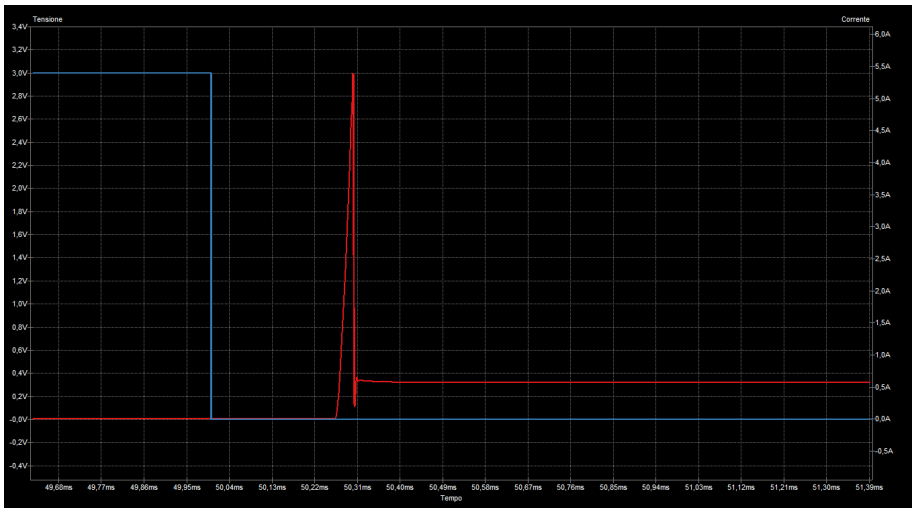


Figure 4.47: Simulation with snubber, 0.2C

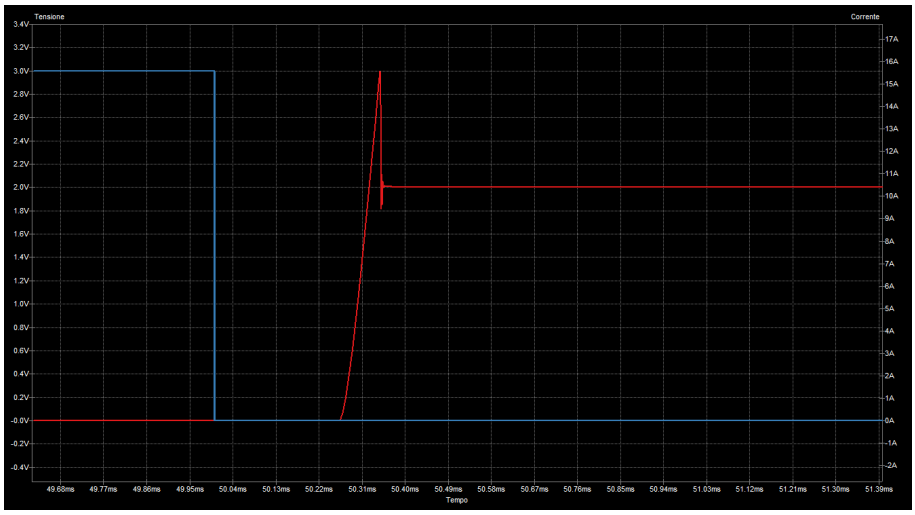


Figure 4.48: Simulation with snubber, 2C

For the batteries considered for this project, typical maximum discharge current values were around 2C, meaning the peaks were safe for low current discharge, but critical for the maximum ones: discharging at 2C, indicatively around 5 A, the peaks were around 7 A for a short duration, which most batteries were able to handle, but beyond the datasheets limits anyway.

A further measure to address this problem was taken firmware-wise. Since the absolute peak value depended on the discharge value, the DAC transition to 0 and the switch opening were separated in firmware, anticipating the former. Even though the peak was still present, it didn't get above 5 A.

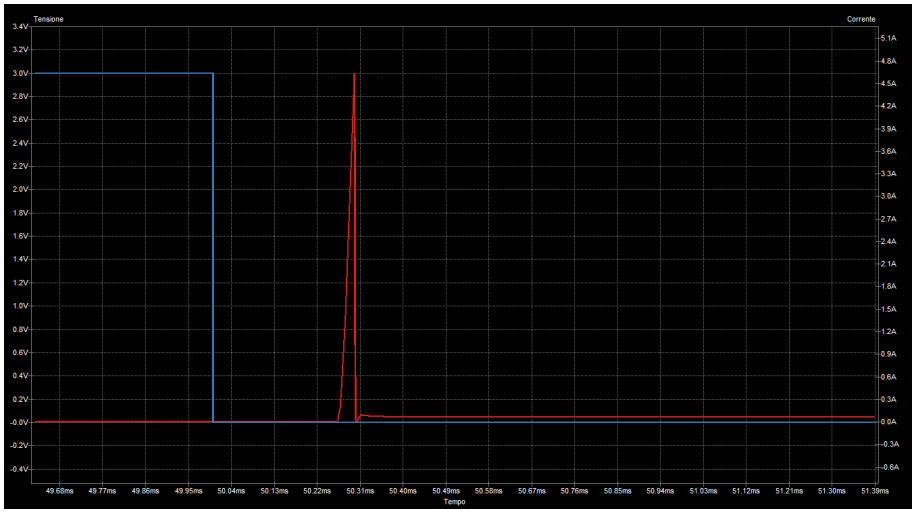


Figure 4.49: Simulation with snubber, DAC = 0

In conclusion, the snubber provided a discharge path for stored energy and helped dampen high-frequency oscillations, effectively lowering the peaks to an acceptable magnitude. Moreover, the firmware modifications avoided the peaks in the circuit's regular functioning. The problem, however, could not be considered solved. An unexpected switch transition during discharge, possibly due to a fault on the switch gate or general disturbances on the circuit, could harm the system. While these modifications were not discarded, it was worth further analyzing the circuit behavior to find a way to get rid of the peaks definitely.

Feedback Capacitance

As already said, the root cause of the peaks was the op-amp output transient not adjusting immediately to the correct value. Further in detail, it could be observed that during switch transitions, there was a delay between when the gate voltage crossed the desired level and when the op-amp detected this change at its inverting input. Various factors, including component characteristics and signal propagation times, caused this delay. With the introduction of the snubber, this did not change substantially, even though the gate voltage rise is slower, almost linear, as shown in figure 4.50, where the gate voltage is the green trace.

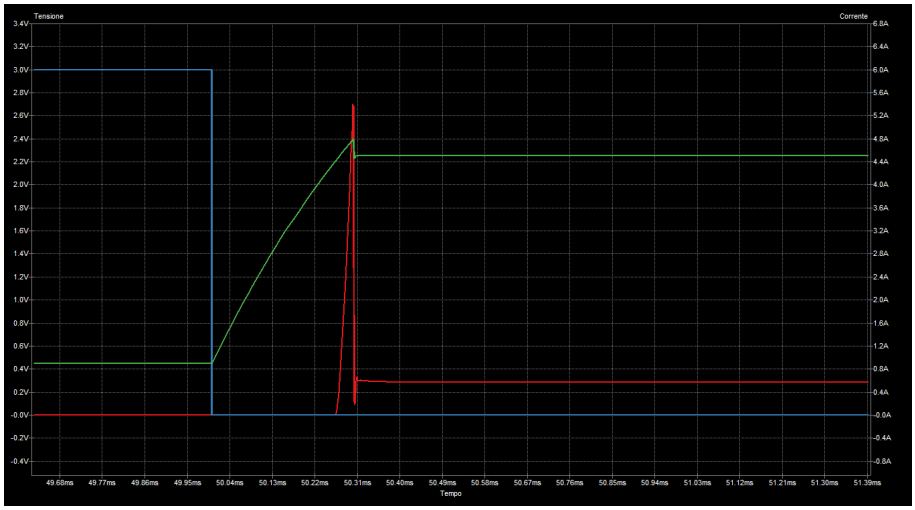


Figure 4.50: Simulation with snubber, gate voltage

To address this issue, a systematic approach was undertaken to mitigate the signal delay and improve the circuit's overall performance during switch transitions. The aim was to reduce the temporal discrepancy between the desired gate voltage and its actual attainment, thus minimizing current peaks and ensuring more precise control. A solution was devised by incorporating a feedback capacitor (C_{fb}) in the circuit's architecture. The presence of the capacitor in the feedback loop helped reduce the delay between variations in the op-amp output and the corresponding changes at the inverting input. The capacitor acted as a low-impedance path during transitions, allowing for faster coupling of voltage changes to the op-amp. This faster coupling helped mitigate current peaks by minimizing the time discrepancy between reaching the desired gate voltage and its actual detection by the op-amp. To control the loop stability, a resistor also had to be added between the shunt and

the inverting input.

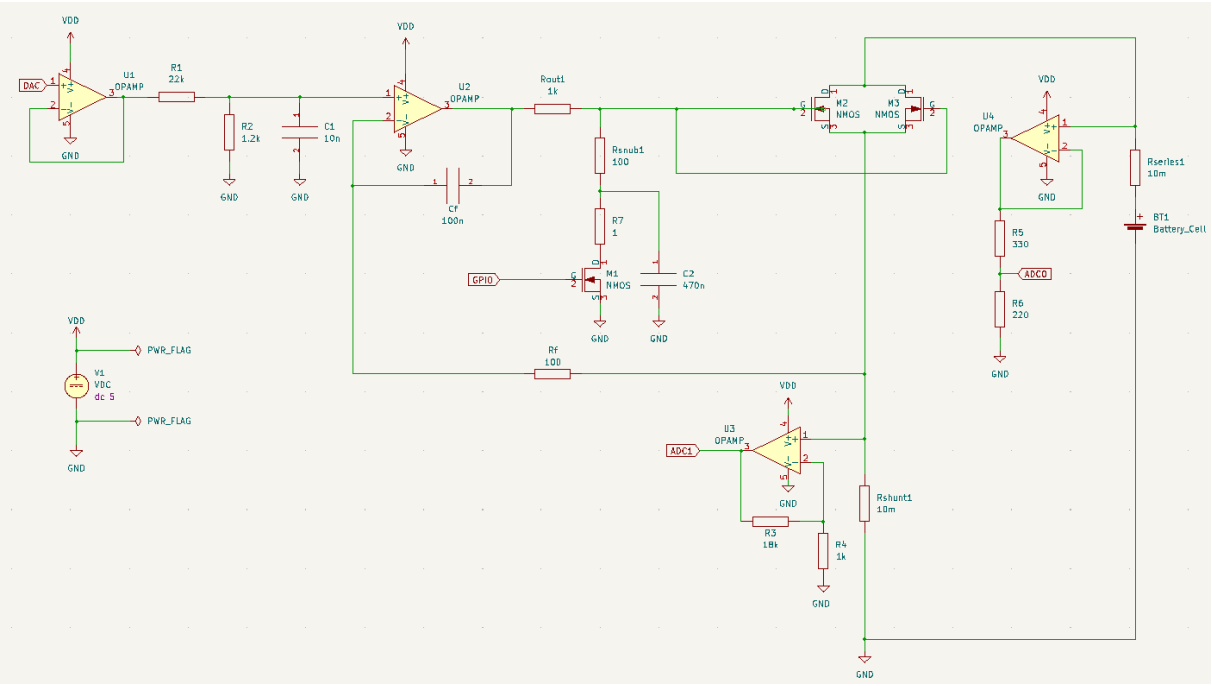


Figure 4.51: Current sink with feedback capacitor

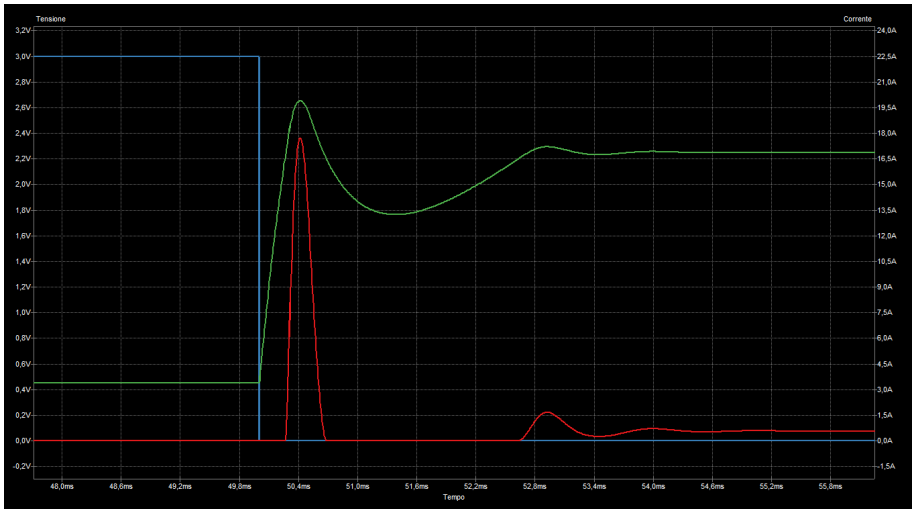


Figure 4.52: Simulation with feedback capacitor

Before tuning the capacitor and resistor values, further circuit modifications had to be made. The simulation showed that this addition by itself was not enough to solve the problem;

however, looking at the signals controlling the loop, some issues could be identified along with some straightforward solutions. First, the output op-amp resistor was a problem: it caused a discrepancy between the op-amp's output voltage and the gate voltage, resulting in current oscillations. Figure 4.53 shows the transition with the gate voltage as the green trace and the op-amp's output as the purple trace.

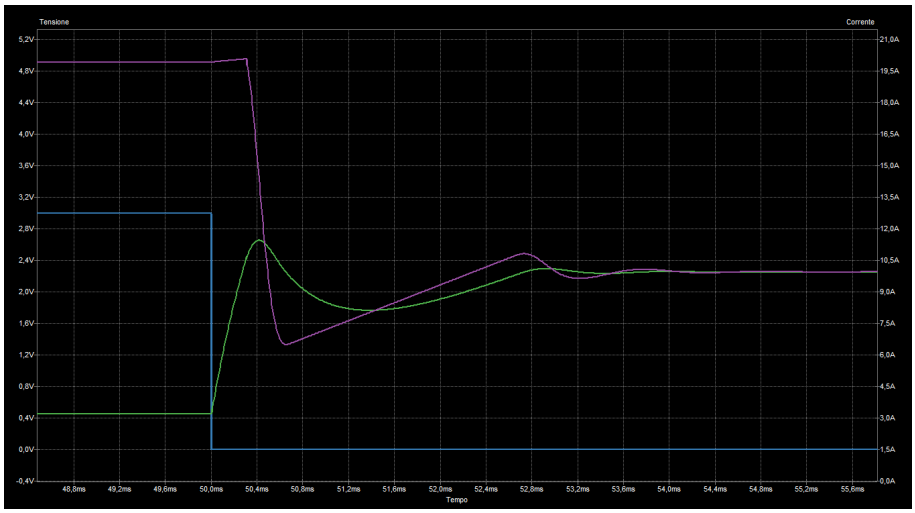


Figure 4.53: Simulation with feedback capacitor, op-amp's output and gate voltage

Two solutions were possible: the first was to move the feedback from the output of the op-amp to the gates.

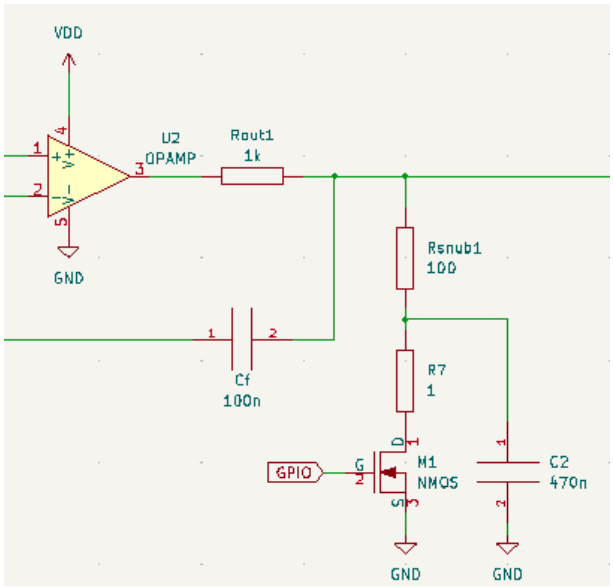


Figure 4.54: Output resistor before feedback capacitor

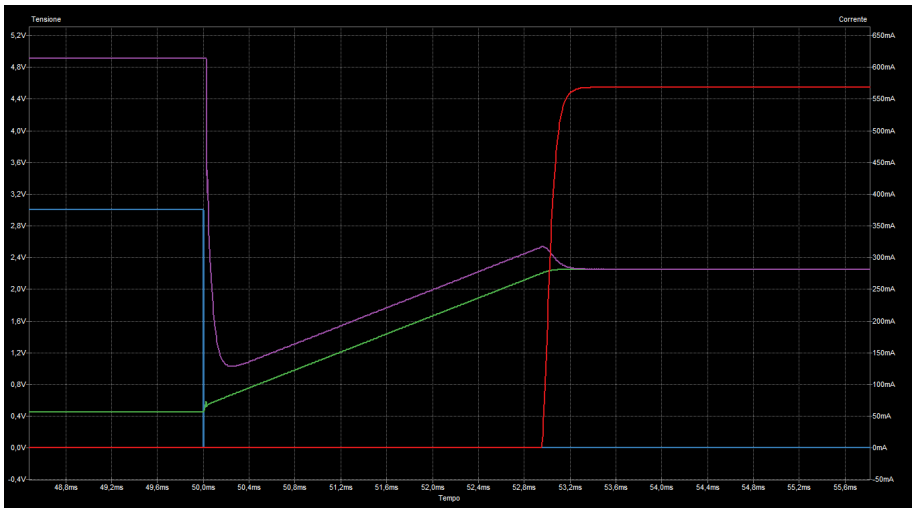


Figure 4.55: Output resistor before feedback capacitor, simulation

The second solution was to move the switch and the snubber before the output resistance, directly connected to the op-amp output. This solution was preferred since it involved another modification that, although not crucial for the functioning, was significant: instead of placing one resistor downstream of the switch and short the gates, one resistor could be connected to each gate, improving individual control over the two nMOS despite their fabrication differences. The snubber resistance had to be changed nonetheless: the op-amp's output was now equal to the gate voltage, so when the switch was closed, it had to be guaranteed to be lower than the minimum threshold voltage. Placing a sufficiently low snubber resistor, since the maximum voltage that the op-amp could provide in this context is limited by its maximum current, the gate voltage was given by:

$$I_{out,MAX} \times R_{snub}$$

It had be:

$$I_{out,MAX} \times R_{snub} < V_{th,min}$$

A resistor of 10 Ω suited these needs.

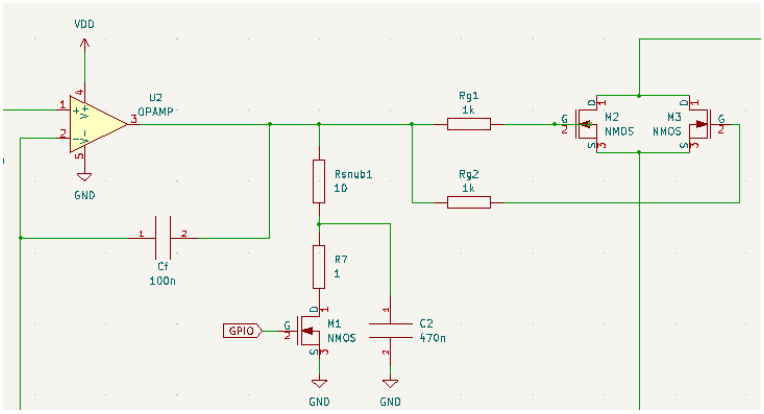


Figure 4.56: Output resistor after snubber, one resistor per gate

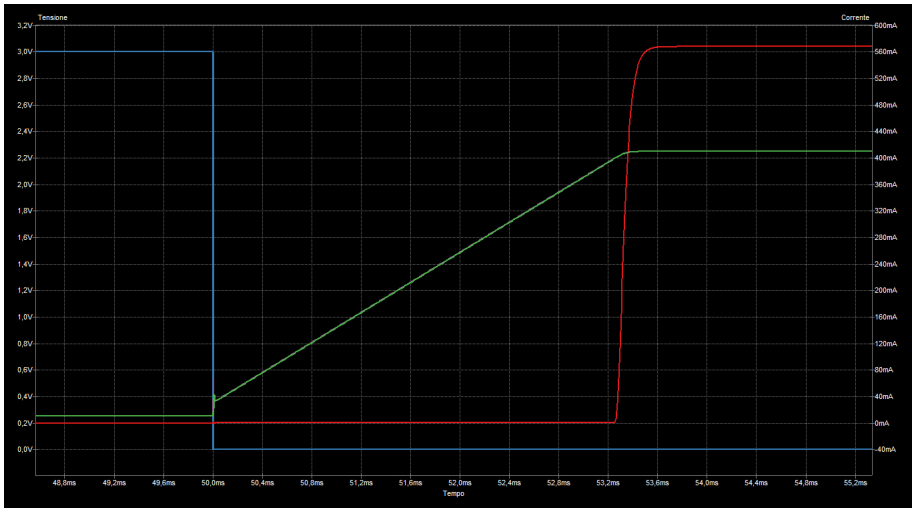


Figure 4.57: Output resistor after snubber, one resistor per gate, simulation

The current step finally appeared smooth and without overshoot. Now, some fine-tuning could be done to improve the circuit performance. First, the snubber capacitor could be reduced to 100 nF. This granted a faster response. The simulation also showed a spike in the op-amp output voltage. Although under control, it could be shaped by properly tuning the feedback capacitor and resistor through simulation and iterative experimentation. The goal was to balance responsiveness and stability while minimizing current peaks during switch transitions. A higher capacitor implied an underdamped current step response and a higher delay between the output voltage change and the current rise.

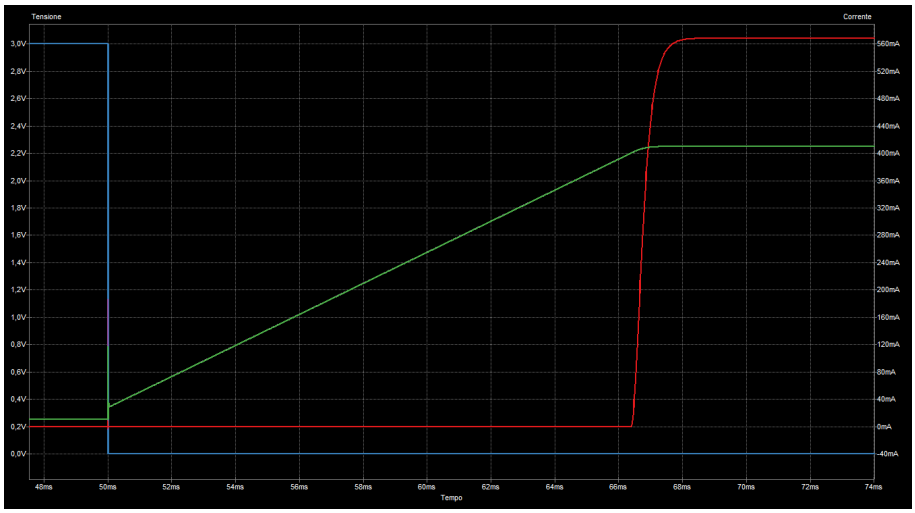


Figure 4.58: Simulation with feedback capacitor, Cf = 1 uF

A low capacitor, instead, made the circuit faster but made the overshoot higher.

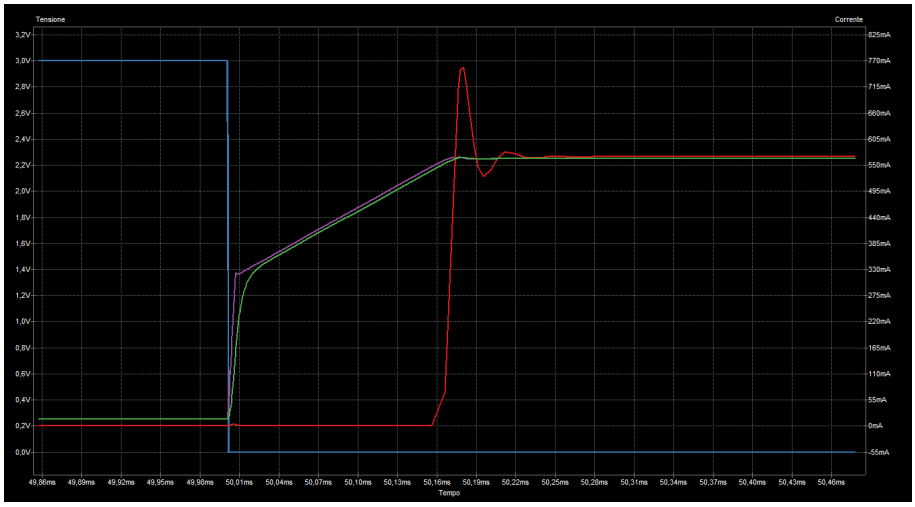


Figure 4.59: Simulation with feedback capacitor, $C_f = 10nF$

The effects on the resistor were similar. Thus, the overall behavior was comparable as long as the product $C_f \times R_f$ was constant. Moreover, lower gate resistances didn't affect the delay much but allowed better shaping of the overshoots.

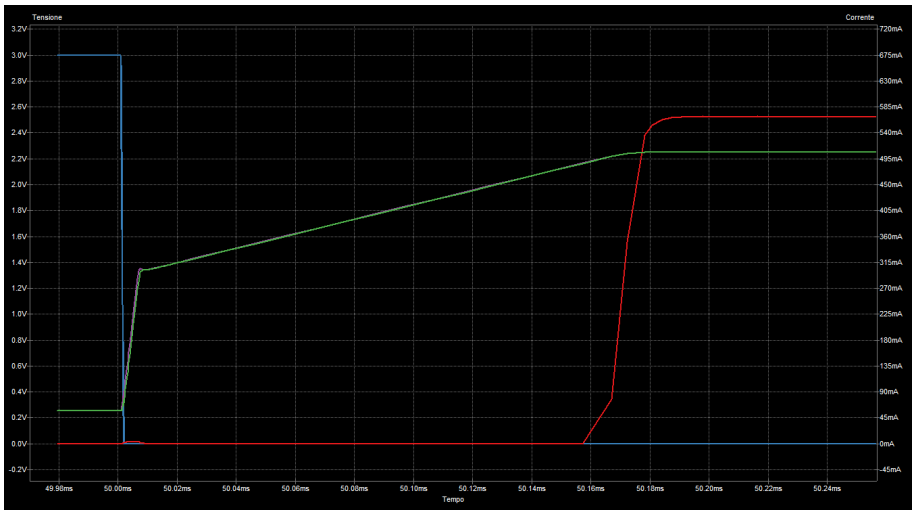


Figure 4.60: Simulation with feedback capacitor, $R_g = 100\Omega$

With 10 Ω gate resistances, 47 nF C_f, 22 Ω R_f, the output voltage and shunt current were shaped as desired. The delay was negligible, there was no overshoot, nor the current profile was particularly underdamped, there were no spikes or ringing on the rising output op-amp voltage.

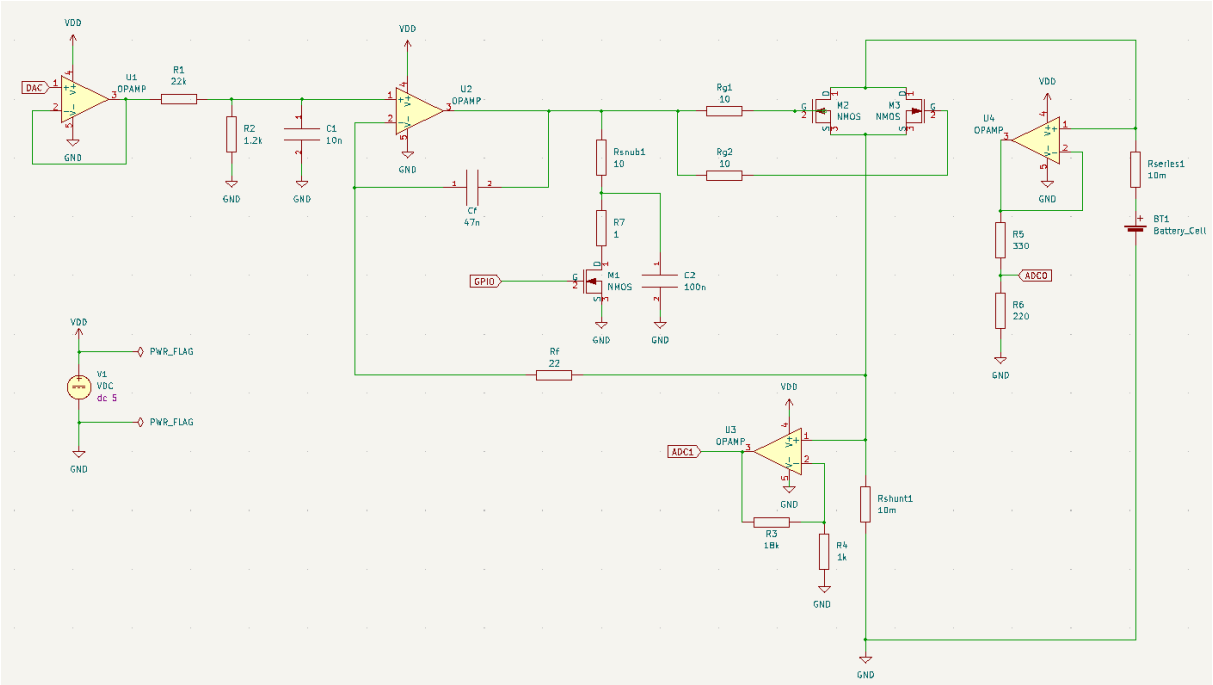


Figure 4.61: Complete circuit

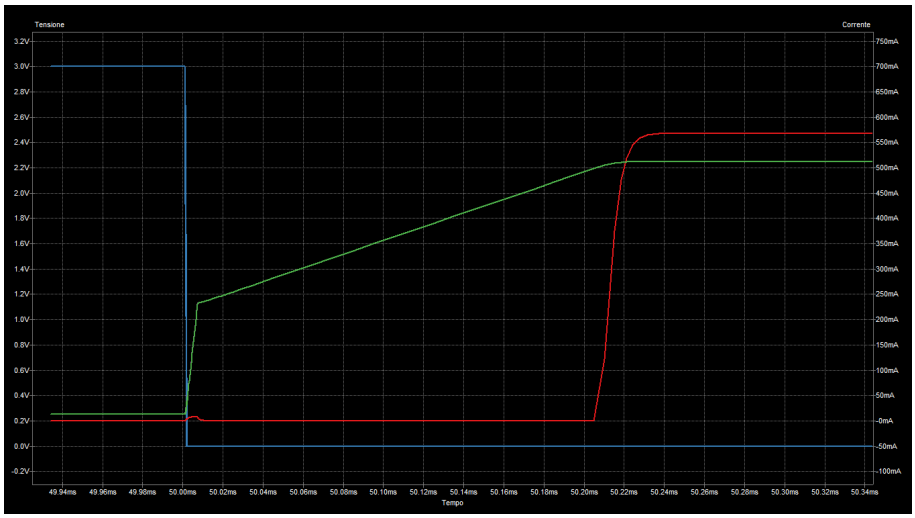


Figure 4.62: Complete circuit simulation

A Monte Carlo simulation was conducted to consider the components' tolerance.

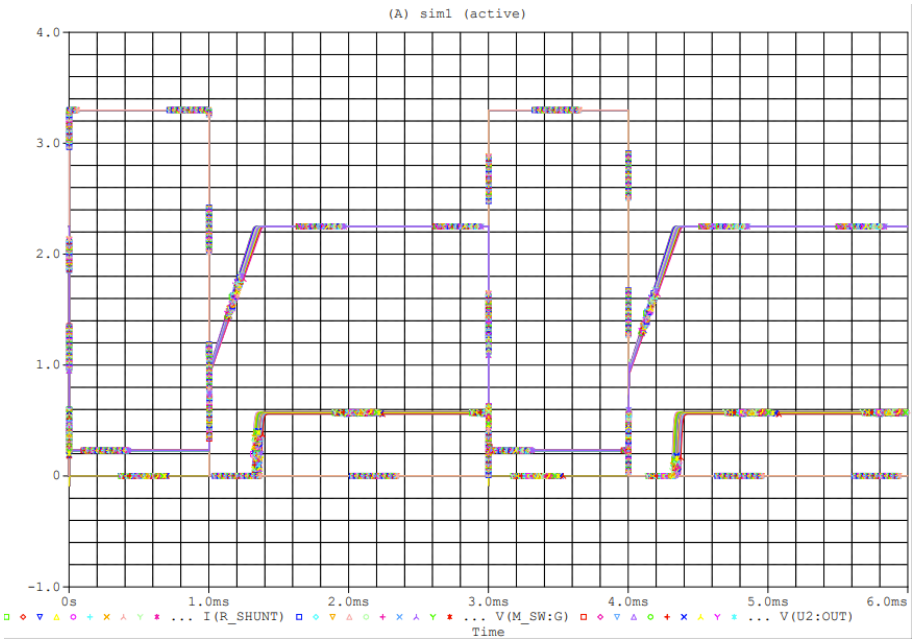


Figure 4.63: Monte Carlo switch transition simulation

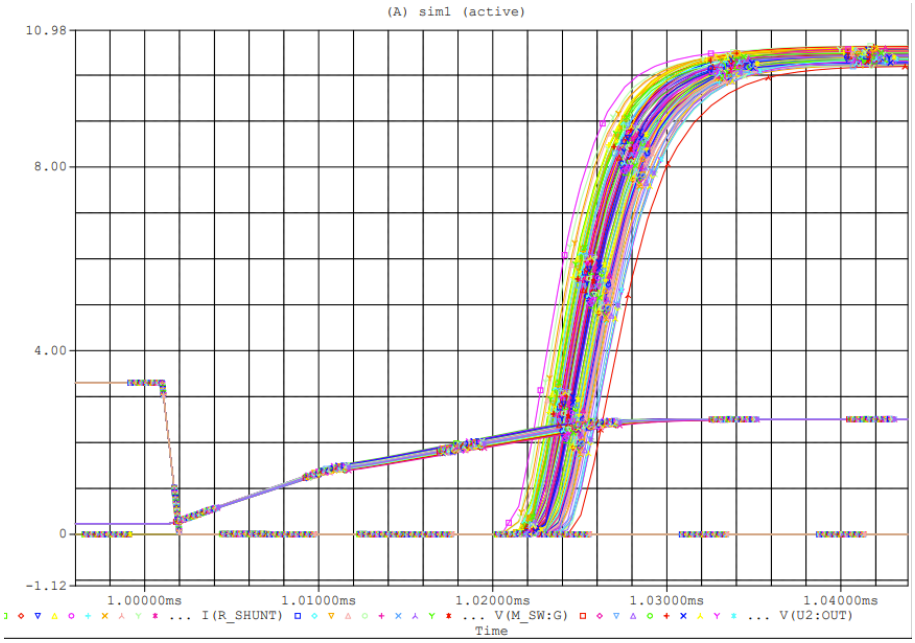


Figure 4.64: Monte Carlo switch ON-OFF transition simulation, 2C

Unfortunately, the falling edge was ignored during this analysis, and it presented threats to the system's integrity. A small negative current on the shunt (-40 mA) was observed but was not considered a safety hazard.

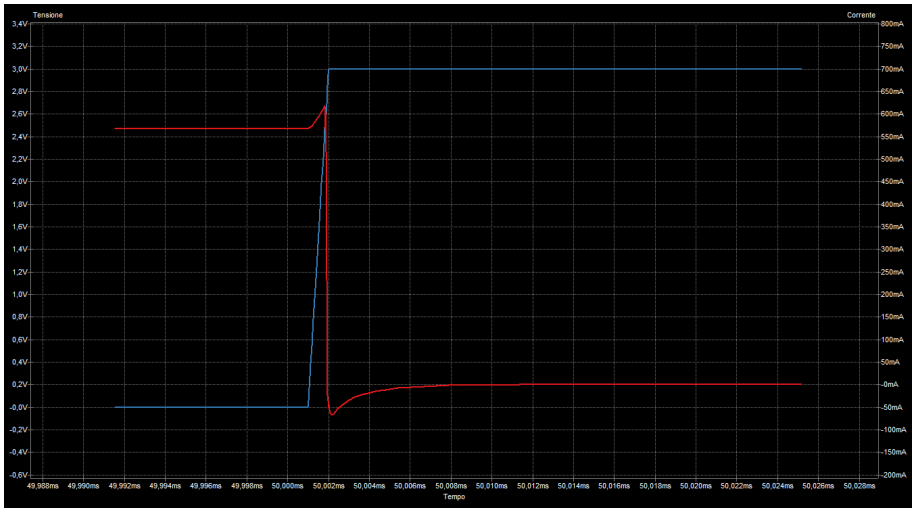


Figure 4.65: Switch OFF-ON transition simulation

Instead, a brief test on breadboard showed that during OFF-ON switch transitions, two switches occasionally broke because of an unbearable current peak. Tracking this current

during this transition, it was possible to understand that most of the current in the switch derived from the snubber and feedback capacitor discharge, accounting for more than 2.5 A impulsive current simulation-wise, as shown by the green trace in figure 4.66. Although the switch could technically be able to withstand such an impulsive current, discrepancies between the real environment and simulation one eventually lead to the switch's failure.

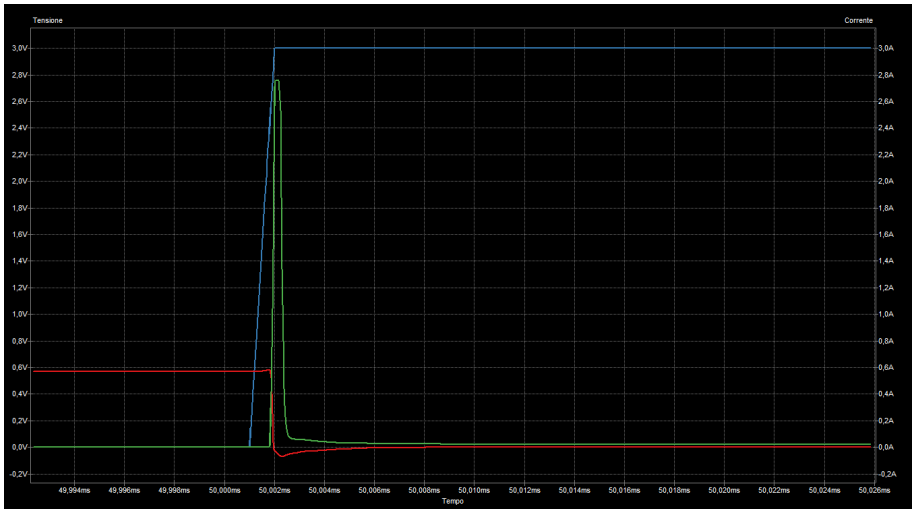


Figure 4.66: Switch OFF-ON transition simulation, current flowing into the switch

Tuning the feedback capacitor and resistor had a light effect on this issue. Instead, a significant result could be obtained working on the gate resistances: using larger resistances deeply affected the current shape. It was the easiest way to lower the peaks on the switch at the cost of some delay. 1 kΩ resistances were enough for a smooth current falling edge. This revert also implied a slight change in C_f and R_f since peaks on the shunt were again present. A safe configuration was obtained with a trade off between optimal performance and stability, making the response slower but anyway acceptable.

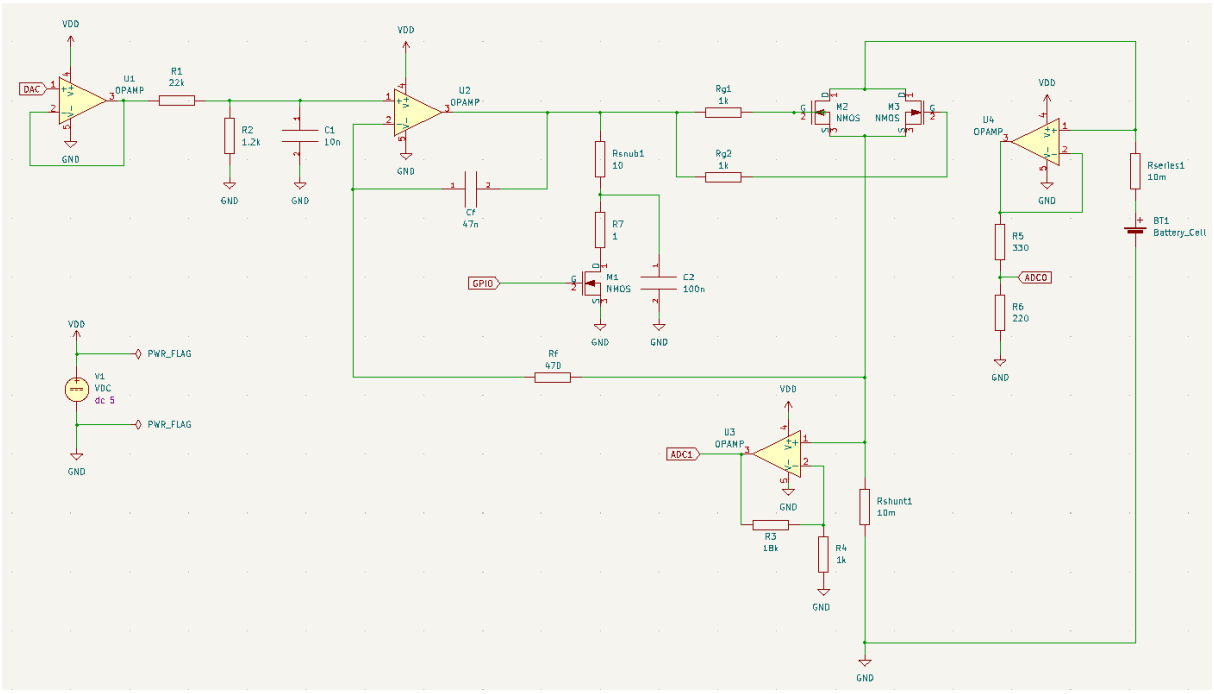


Figure 4.67: Peak free, undershoot safe current sink

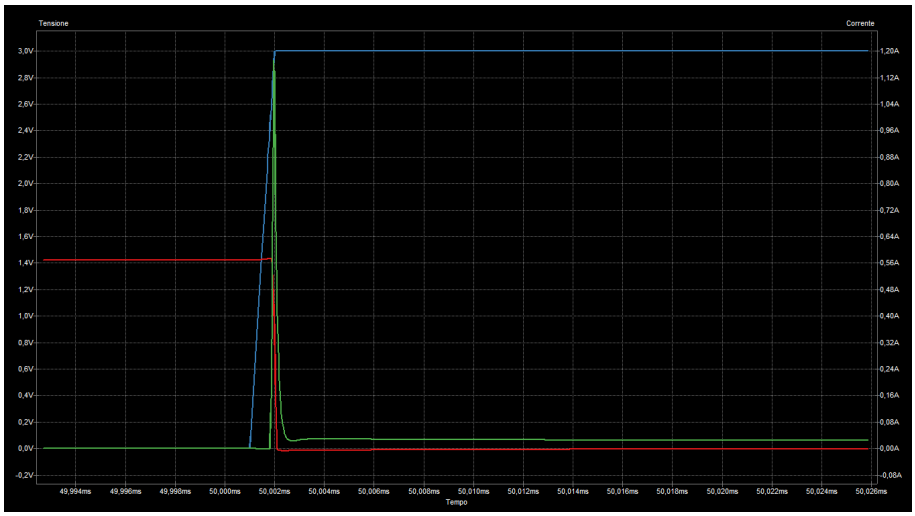


Figure 4.68: Peak free, undershoot safe current sink simulation

The circuit was finally safe from harmful peaks in most situations, including some critical faults. Other risk conditions were monitored at run time in the circuit (sudden voltage drops, current drift). Overheating management was beyond this project's scope; however, its most common effects were handled as aforementioned.

4.2.6 Refinements

After a preliminary test on a breadboard, some further refinements were introduced. First of all, undershoot behavior on the falling edge was inconsistent. Parasitics and fabrication discrepancies of the components on the real circuit likely played an important role in shaping the circuit response. Therefore, the gate resistances were changed to 4.7 kΩ to be more conservative without altering the performance. Another modification required by the preliminary test was the snubber resistor. The op-amp was driving the gates inconsistently, but a slight increase in the resistance, changed from 10 Ω to 22 Ω, was sufficient to fix the problem. Finally, the load had tp be disconnected until discharge began. When flashing code, the GPIOs were high impedance: this could bring the switch off, implying a gate voltage equal to an unpredictable op-amp output voltage. To avoid this problem, a pull-up resistor was added on the switch gate using the 3.3 V output pin available on the board as V_{DD}. The behavior firmware-wise didn't change except for some configuration parameters, and, in this way, the switch was guaranteed to be on until the GPIO was driven low by the microcontroller.

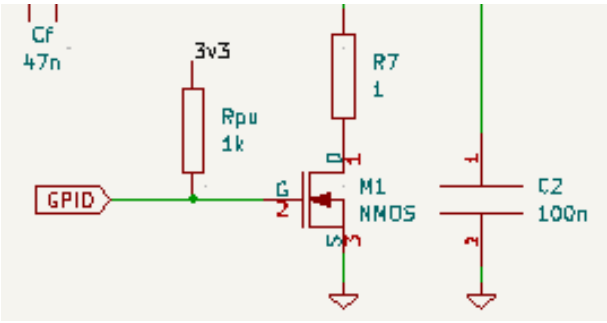


Figure 4.69: Pull-up switch configuration

4.2.7 Final topology

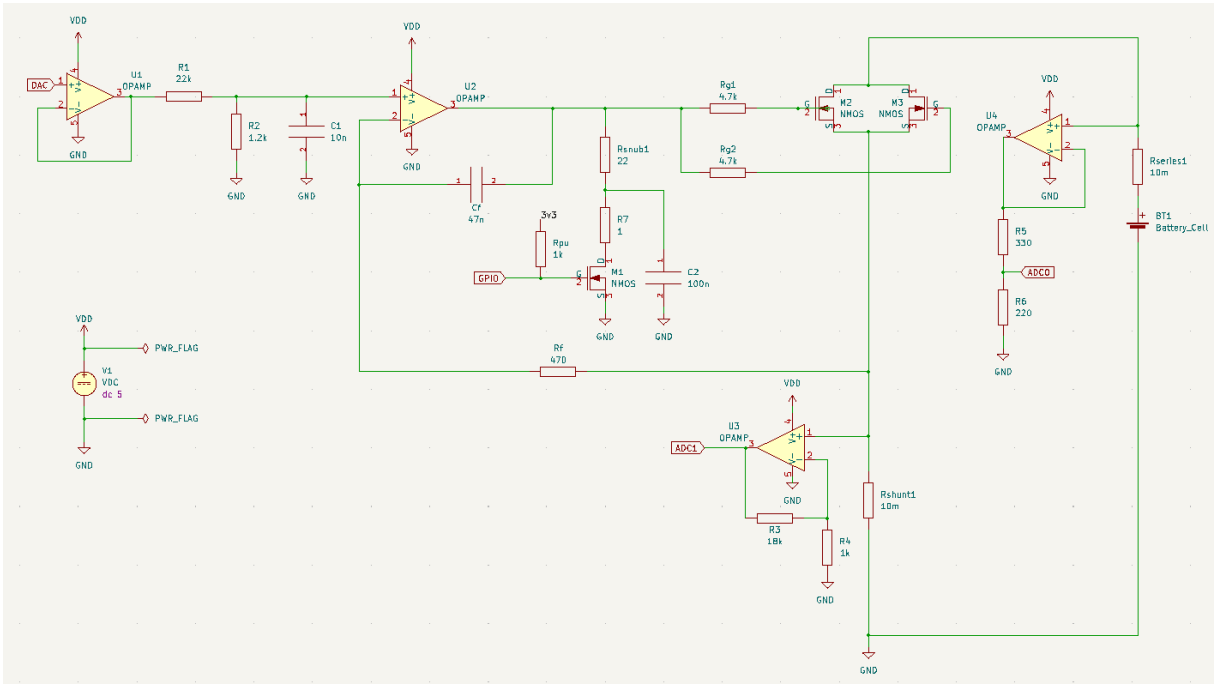


Figure 4.70: Final circuit

The system was thoroughly simulated. No harmful situations nor anomalies were detected, so the system could finally be prototyped and tested.

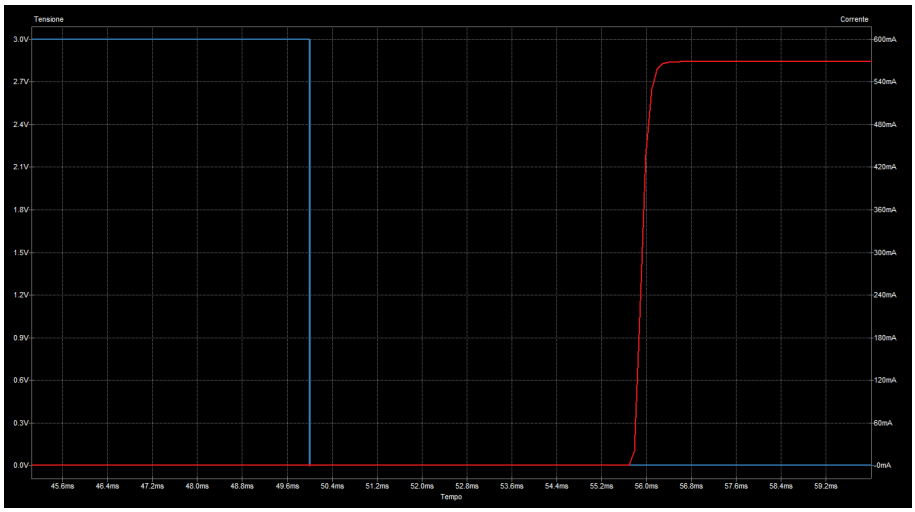


Figure 4.71: Final circuit simulation, switch ON-OFF transition

With a current of 550 mA, the recovery time from a fault on the switch gate was about 6 ms.

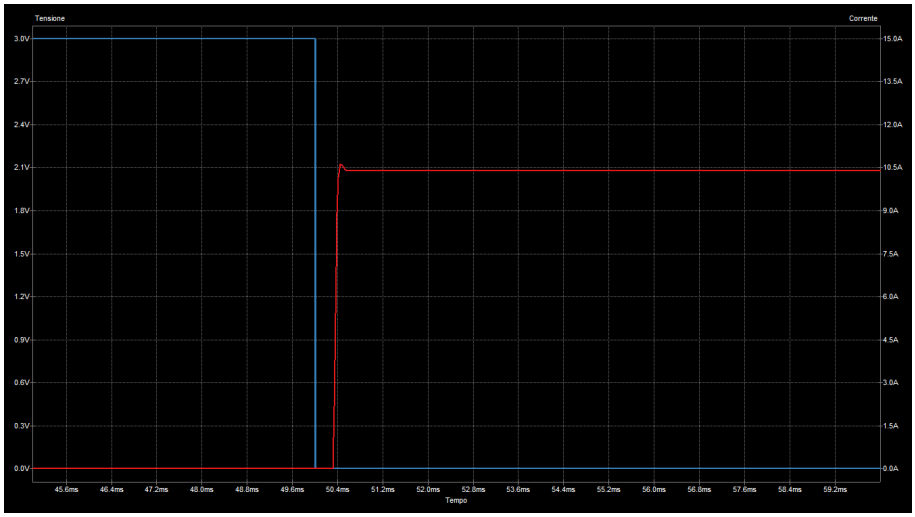


Figure 4.72: Final circuit simulation, switch ON-OFF transition, 2C

With a current of 10.5 A, instead, the behavior was faster, accounting for an approximately 0.5 ms delay. An overshoot was still present but definitely negligible.

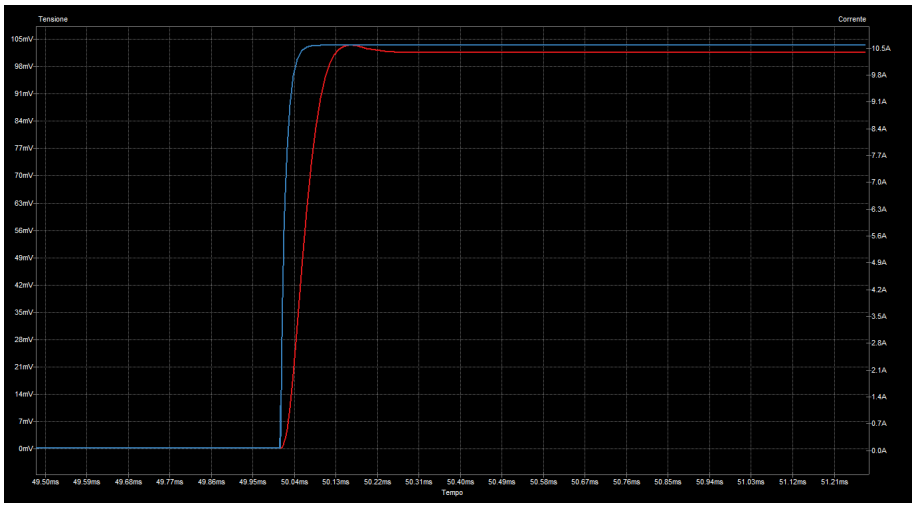


Figure 4.73: Final circuit simulation, DAC 0 to 2 V

Regarding the variations on the non-inverting input provided by the DAC, the worst case was simulated (i.e., DAC transition from 0 to 2 V), and the system responded safely, with a slight overshoot and a fast response (¡ 0.2 ms).

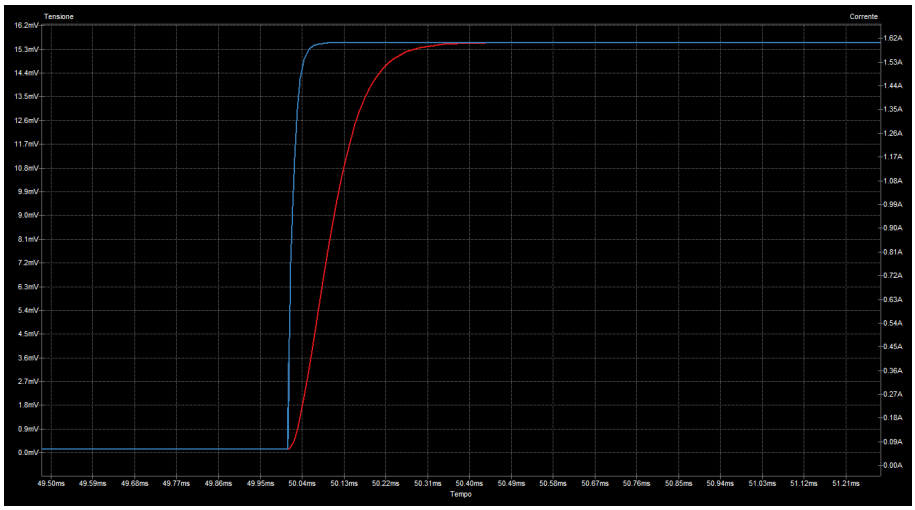


Figure 4.74: Final circuit simulation, DAC 0 to 0.3 V

Anyway, the DAC maximum allowed step was 0.3 V, and in that case, a slightly higher delay was present (¡ 0.4 ms) with an underdamped current rise.

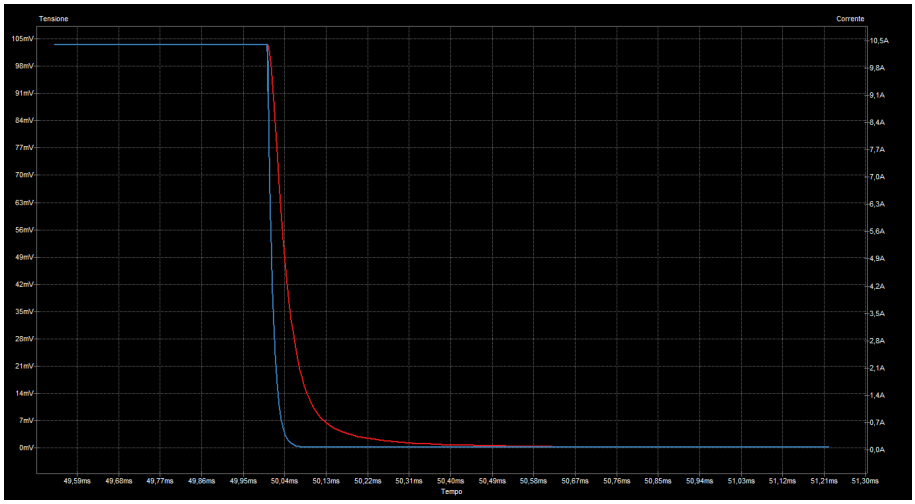


Figure 4.75: Final circuit simulation, DAC 2 V to 0

Finally, all the capacitors inserted along with parasitics taken into account by simulation implied a small delay also in the falling edge. So, to fully switch off the circuit when discharging at maximum current, about 0.3 ms were needed.

4.3 Charge section design

The charge section was composed of fewer elements than the discharge one. It featured a charger and a relay to disconnect the charge section when unnecessary. The charge current measurement was outside this project's scope and was not considered.

4.3.1 Charger choice

The charge had to be as fast as possible since it constituted a bottleneck for the whole test duration. Higher power chargers, though, heated up the battery. A conservative approach was adopted, looking for chargers able to deliver up to 2 A to not stress the battery under test during the prototype validation and avoid safety hazards for heating and higher current, while still maintaining a reasonable charge time.

Some devices able to manage the charge were available on the market. TP4056, for example, is a very popular single-cell lithium-ion battery charger for homemade custom boards, often sold already mounted on a small PCB since it's a SMD component, easy to integrate into a larger prototype. It accomplishes automatic termination of the charge by monitoring the charge current. It was not available on the typical vendors; instead, it could be found on the global market, on general e-commerce sites. Unfortunately, delivery time made it an unfeasible solution. Moreover, it could only source up to 1 A. [33]

Other circuits were available sooner, but they hardly had any documentation and could not be considered safe for the purposes of the project. A custom approach was discarded, both for timing and complexity, since overcharging the battery might lead to dangerous failures.

A commercial charger was chosen for simplicity, estimated delivery time, and safety. There were many possibilities on general e-commerce sites like Amazon, with short delivery times and a wide price range. The most expensive chargers could esteem the battery status and provide a Coulomb Count of the delivered charge. Since the requirements for this project didn't focus on the charge section but only needed the battery to be fully charged before the discharge starts, a lower-end solution was preferred, and the SUNLYTOUR 18650 charger was chosen for several reasons:

- Up to 2 A nominal charge
- Fast delivery
- Low cost
- Useful case for battery holding [34]

Figure 4.76: SUNLYTOUR 18650 charger [34]

4.3.2 Relay choice

A high-side switch was needed to decouple the charge section from the rest of the circuit. High-side pMOS would have been a straightforward solution. Components providing good performances for this project could be easily found on the market, but SMD only. Through-hole ones compliant with the specifications had high costs and long delivery times. Finally, relays were ideally preferred since they are designed for disconnecting and insulating circuit sections: SMD pMOS were then kept as a backup solution.

Mechanical relays were first considered to be able to disconnect the sections physically. Coil voltage and contact current in line with the requirements were not available on the market, so they were discarded. A suitable alternative could be found in the solid state relays, which offered through-hole components at low prices and performances in line with the needs of this project. Solid-state relays also had several relevant advantages over electromechanical ones.

- Price: SSRs tend to be cheaper.
- Power consumption: SSRs consume less than EMRs.
- Operating voltages: SSRs require lower operating voltages.
- Reliability: SSRs offer an enhanced level of reliability. Electrical item life: SSRs have a longer service life.
- Input-output isolation: SSRs offer improved isolation between input and output.
- Contact bounce: SSRs prevent it.
- Size: SSRs have a small form factor. [35]

The choice fell on CPC1706Y from IXYS. The CPC1706Y is a relay equipped with an infrared LED that controls an optically coupled MOS used as an internal switch. [36]

Figure 4.77: IXYS CPC1706Y [36]

- **Maximum load current**: 4A (continuous)
- **On-Resistance**: Typ. 70mΩ; Max. 90mΩ((Test Conditions: I_F=5mA, I_L=1A))
- **Off-State Leakage Current**: Max. 1µA (Conditions: I_F=0mA, V_L =60V)
- **Input Voltage Drop**: Min. 0.9V Typ.1.2A Max. 1.4V (Conditions: I_F = 5mA)
- **Input Control Current to Activate**: Typ.1.4mA Max. 5mA (Conditions: I_l = 1A)
- **Switching speed**:
  - Turn-On: Typ. 0.5ms Max. 5ms (Test Conditions: I_F=5mA, V_L=10V)
  - Turn-Off: Typ. 0.085ms Max. 2ms (Test Conditions: I_F=5mA, V_L=10V)

[36]

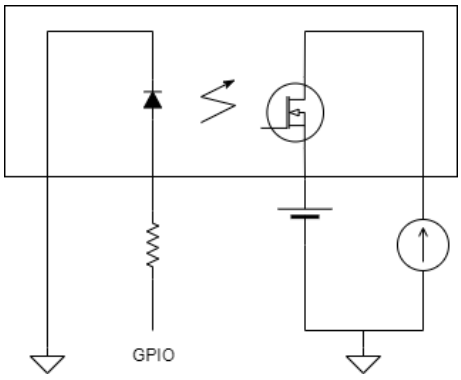


Figure 4.78: Relay push-pull active-high configuration

Initially, the option of driving the relay by connecting a GPIO of the board (in Push-Pull active-high configuration) directly to the infrared led was considered, since it needed very low current. The first condition to check was, in fact that when the output of the GPIO was high, enough current was flowing in the led to activate the MOSFET:

$$I_D = \frac{V_{oh} - V_D}{R} = \frac{2.9V - 1.4V}{R} > 5mA -> R < \frac{1.5V}{5mA} = 300\Omega$$

But at the same time, the series resistor had to be sized so that the current taken from the pin was not more than 8 mA:

$$I_D = \frac{V_{oh} - V_D}{R} = \frac{3.3V - 0.9V}{R} < 8mA -> R > \frac{2.4V}{8mA} = 300\Omega$$

The option of driving the led with an active-low configuration was also evaluated.

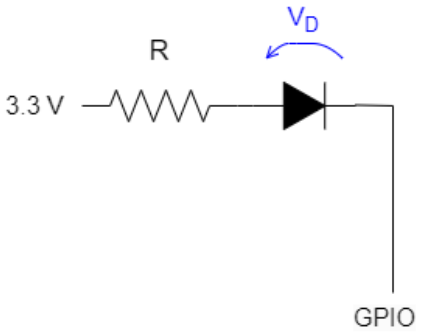


Figure 4.79: Relay push-pull active-low configuration

Again, calculations were made to determine the resistor value that would guarantee sufficient current to turn on the led (and thus close the relay) while not exceeding the limits of the GPIO port.

$$I_D = \frac{V_{3.3} - V_D - V_{ol}}{R} = \frac{3.3V - 1.4V - 0.4V}{R} > 5mA -> R < \frac{1.5V}{5mA} = 300\Omega$$

$$I_D = \frac{V_{3.3} - V_D - V_{ol}}{R} = \frac{3.3V - 0.9V - 0}{R} < 8mA -> R > \frac{2.4V}{8mA} = 300\Omega$$

The last option considered was to use an FT (5 V tolerant) pin in an open drain configuration with an external pull-up. The value of the pull-up had to be such that the relay would have turned on but also that the current drawn from the pin was less than 8 mA.

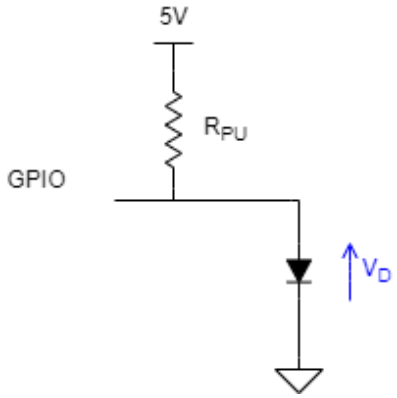


Figure 4.80: Relay pull-up configuration

$$I_D = \frac{V_{AL} - V_D}{R_{PU}} = \frac{5V - 1.4V}{R_{PU}} > 5mA \rightarrow R_{PU} < \frac{3.6V}{5mA} <= 720\Omega$$

$$I_D = \frac{V_{AL}}{R_{PU}} = \frac{5V}{R_{PU}} < 8mA \rightarrow R_{PU} > \frac{5V}{8mA} = 625\Omega$$

It is worth noting that the circuit worked in both configurations, using a 330 Ω resistor to be conservative on the current drawn from the pin. Still, the choice fell on the open-drain configuration with a pull-up resistor of 680Ωdue to the margin it had to be considered safe despite the tolerances.

Chapter 5

Firmware

5.1 Introduction

This chapter describes in detail the firmware developed for the Nucleo STM32 board. The firmware was specifically designed to facilitate the execution and management of tests on Li-ion cells.

The board is equipped with the STM32G0B1RET6 microcontroller, a 32-bit Arm® Cortex®-M0+ core, offering a balance between computational power and energy efficiency.[20] Code writing and versioning were managed with Visual Studio Code configured to support GIT plugins. The STM32 integrated development environment was exploited to configure peripherals, compile and debug. STM32CubeIDE offered a powerful and versatile C development tool based on Eclipse, GCC toolchain, and GBD for debugging, including useful features such as a live variable watcher and register and memory monitors.[37]

The board's set of peripherals played a crucial role in monitoring and managing the execution of tests on the lithium battery. The DAC (Digital-to-Analog Converter) set the battery's discharge current, while the ADC (Analog-to-Digital Converter) provided measurements of battery parameters such as voltage and current. The GPIO (General-Purpose Input/Output) pins provided the necessary flexibility for interfacing external components and devices. The UART (Universal Asynchronous Receiver-Transmitter) also allowed seamless communication with external devices for data transmission. [20]

FreeRTOS middleware was exploited. FreeRTOS is a popular Real-Time Operating System (RTOS) specifically designed for embedded systems, enabling efficient multitasking and streamlined resource management. Using FreeRTOS, the firmware could effectively execute multiple tasks concurrently, leveraging the power of timers and queues. [38]

5.2 Firmware structure

The firmware was structured into three independent tasks, each serving a specific purpose in the overall operation. These tasks included LogicTask, LogDataTask, and UpdateOutputTask, working together to ensure efficient and coordinated functionality. The general

structure of the firmware can be outlined as follows:

- **LogicTask**: organized as a state machine, it analyzed the current state and relevant parameters to determine the subsequent state and the values to be applied to the outputs;
- **LogDataTask**: transmitted data packets to an external pc via UART;
- **UpdateOutputTask**: updated the value of the outputs by assigning them the value determined by the LogicTask.

This firmware structure granted the system modularity and flexibility. Each task operated autonomously, enabling efficient multitasking and optimal resource utilization.

5.2.1 LogicTask

The LogicTask served as the core of the firmware. It managed the system's operative flow, determining the state of the FSM and feeding global buffers that LogDataTask and UpdateOutputTask then read.

Overall structure

The LogicTask was designed as a Finite State Machine, specifically a Mealy machine, consisting of three states: IDLE, DISCHARGE, and CHARGE. A test sequence started when a Header packet was transmitted. Before the transmission of the first Header, the system did not enter the FSM, nor did it collect the sampled values from the ADC. Once the first test Header was sent, the system entered the IDLE state, started collecting ADC values, and initiated packet creation.

The system enteed the IDLE stage under the following circumstances:

- At the start of each test cycle;
- After the CHARGE phase, allowing the battery to cool down;
- At the end of the entire test.

During the CHARGE state, the battery was fully charged.

The system entered the CHARGE stage following the IDLE state in the following situations:

- At the start of each test;
- At the end of the test session, representing the final charging phase.

Within the DISCHARGE state, the battery underwent discharge at a programmed current. The DISCHARGE state was divided into two phases: DischargeOn and DischargeOff. During the DischargeOn phase, the system sank the programmed current from the battery, while in the DischargeOff phase, the battery was allowed to rest so that its voltage could rise again.

Once a test was completed, if the test session was over, a Tail packet was created, placed in the queue, and the system exited the FSM.

A flowchart describing the operation of the LogicTask is shown in figure 5.1.

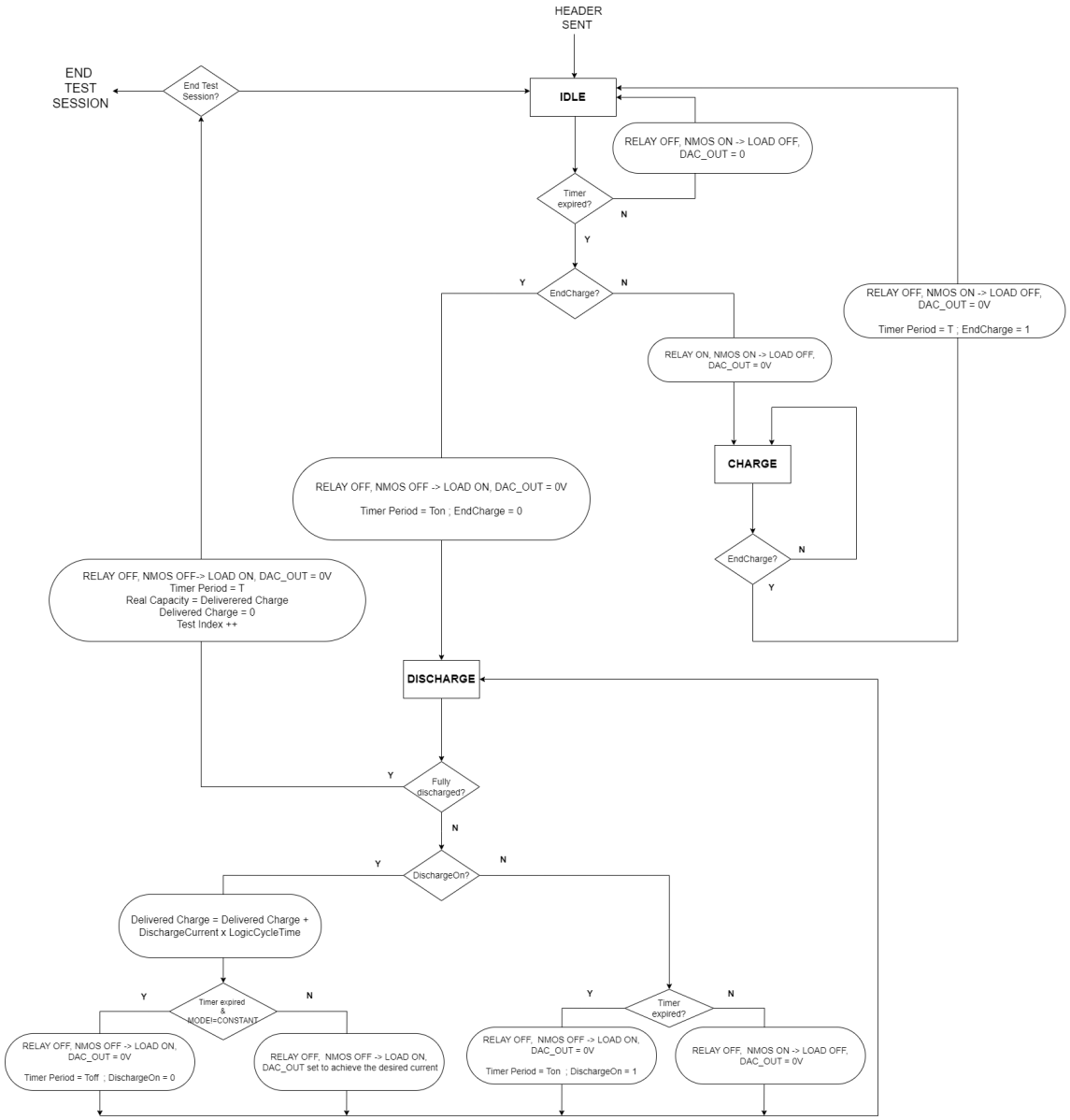


Figure 5.1: Flow chart describing the general structure of the Logic task

Queue item creation

In the LogicTask, packets (items) were created and loaded inside a queue, ready to be sent via UART communication to the external device. Three different types of packages were created inside LogicTask:

- **Header packet**: a packet sent at the beginning of each test in the programmed sequence.

- **Standard packet**: packets sent throughout the execution of the tests. Through these packets, it was possible to reconstruct the behavior of the battery during the entire test.
- **Tail packet**: packet sent at the end of the scheduled test sequence.

A Header packet contained the following information:

- **Mode**: discharge mode of the test (CONSTANT, STEP, RANDOM)
- **SamplingTime**: time between creating one packet and another. Quantity required to reconstruct the time instant associated with a given packet (by simply multiplying by the packet index).
- **IDischarge**: discharge current at which the test was performed.
- **VCutOff**: voltage below which the battery should not be further discharged (greater than the minimum battery voltage for safety issues).

A standard packet contained the following information:

- **VBat**: voltage of the battery under test. The quantity was expressed in LSB on an 8-bit variable, where the maximum value corresponded to 5 V.
- **ICharge**: battery discharge current. The quantity was expressed in LSB on an 8-bit variable, where the maximum value corresponded to 2500 mA.
- **IDischarge**: battery charge current. The quantity was expressed in LSB on a 16-bit variable, where the maximum value corresponded to 10000 mA.
- **QDelivered**: depleted charge during the test. The quantity was expressed in LSB on a 16-bit variable, where the maximum value corresponded to 5200 mAh.
- **Id**: an index used to reconstruct the time instant to which the packet corresponds.

Therefore, the resolution of transmitted data was:

- VBat = 19.53 mV
- ICharge = 9.77 mA
- IDischarge = 0.15 mA
- QDelivered = 0.08 mAh

It is worth noting that measurement resolution is higher; if a higher resolution iss needed for data processing, it is sufficient to expand the packets.

A Tail packet contained the following information::

- **NumOfTests**: number of tests that were performed.
- **RealCapacity**: actual capacity of the battery under test, estimated through a constant test.

ADC values collection

The values that the ADC sampled underwent averaging, specifically 10 samples were taken for each channel of the ADC. The averages converted to analog values were among the parameters that determined the execution of the LogicTask. Since every 5 logic cycles an item (packet) was inserted within the queue, the battery voltage and current values inserted within a packet were nothing more than the average of the values corresponding to the previous 5 logic cycles.

End of Charge

For this thesis, full charge was accomplished by setting a sufficiently long timing interval obtained by the datasheets. This choice was made to simplify the charging section hardware design as much as possible.

However, a smarter way to detect when the battery is fully charged could be by monitoring the charge current and exiting the charge when it gets below a certain threshold. This could be done easily firmware-wise, so the EndCharge function, responsible for checking whether the charge was over, was designed flexibly to accommodate both solutions with few changes. The charge current value (always 0 for this prototype version) was checked against a threshold and, if lower, incremented a counter. The counter's purpose was to avoid false positives by validating the value over more than one cycle. The charge was considered over when the counter reached a certain value, set at compile time by the programmer.

End of discharge

This way, the charge duration could be determined by setting the counter max value to $Charge\_Duration \times LogicTask\_Frequency$. Instead, to determine the end of charge based on the sensed current, it would be sufficient to set the counter max value to a small value, compliant with the requirements about the allowed number of below-threshold cycles. The system remained in this stage until the battery voltage fell below the cutoff (to prevent the cell from reaching critical voltages) or until all the charge was depleted. However, if the test mode was set to CONSTANT, the condition regarding the total depleted charge was not considered. A check was performed to ensure that the total depleted charge remained lower than the estimated battery capacity. Additionally, the system examined whether the battery voltage stayed below the cutoff for a number of cycles higher than an established threshold to prevent false positives.

Output values

Output values were computed by the LogicTask and written in a global array read by the UpdateOutputTask. The LogicTask computed 4 output values:

- **DAC**: DAC value was calculated based on the desired current value. It was equal to 0 when no current was requested. During the DischargeOn phase, based on the actual discharge current value taken from the voltage reading on the shunt made by the ADC, the output value of the DAC was increased or decreased to reach the desired current value. Although the device was designed to avoid current spikes due to sudden increases on the DAC output, a maximum limit was imposed on the voltage increment to reach the desired value gradually.

- **Load Switch**: it was set high when the system was not discharging to bring the load gate voltage to ground. When DischargeOn was entered, it was set low.
- **Charge relay**: it was set high in the CHARGE state to allow charging and low elsewhere.
- **Green LED**: it provided visible information about the system status via a green LED integrated into the board. It was toggled in different ways based on the current state:
  - IDLE: blinked with a 3 s period, DC 20%;
  - CHARGE: blinked with a 3 s period, DC 80%;
  - DISCHARGE: blinked at a frequency proportional to the discharge current, DC 50%;
  - IDLE (end of test sequence): always on.

5.2.2 LogDataTask

The LogDataTask was in charge of transmitting data packets to the pc for further elaboration.

The data to be transmitted was organized by the LogicTask into packets and stored in a queue. Periodically, the LogDataTask checked the queue for available items to transmit. If the queue was empty, the LogDataTask introduced a delay of 500 ms before checking again. However, when items were in the queue awaiting transmission, the delay was reduced to 50 ms. This adjustment ensured the queue did not overflow while the LogicTask continued populating it with data. Packets' structure has been detailed in section 5.2.1.

Again, the goal was to separate the main operations performed by the system, allowing for better modularity and flexibility.

The UART was configured as reported in table 5.1.

Baud Rate	28800 Bits/s
Word Length	8 Bits
Parity	None
Stop Bits	1 Bit

Table 5.1: UART Configuration

The protocol was kept as simple as possible since transmission integrity was out of this project's scope. However, it is worth noting that no substantial problems arose with data transmission.

To convert the transmitted data to the actual value, tabular values are provided to the user following a protocol of the form:

$$Value = ConversionFactor \times TransmittedData + Offset$$

Offset is zero; conversion factor refers to the packet resolution detailed in section 5.2.1.

5.2.3 UpdateOutputTask

The UpdateOutputTask duty was to read a global array written by the LogicTask and update the related output pins. This array was written by the LogicTask and was composed by:

- A 12-bits value that indicated the DAC setting;
- A single bit for switch driving;
- A single bit for relay driving;
- A single bit for the board integrated green LED driving.

The task ran every 10 ms, so it was faster than the LogicTask. This choice was made to ensure a timely refresh of the output value and a quick recovery from faulty output for whichever reason.

The design choice of having a task completely dedicated to output updating was due to the intention of decoupling the calculation of the FSM regarding next state and output values, performed by the LogicTask, from their actual application, performed by the UpdateOutputTask.

The outputs were decoupled as detailed in section 4.2.4. Separate considerations should be made about the green LED: it is integrated on the board and doesn't need any attention for its activation; it was sufficient to write a 0 or 1 to it.

5.3 ADC configuration

The ADC used in the firmware was the integrated 12-bit analog-to-digital converter based on the successive approximation method.

Two specific channels of the ADC were used to acquire two distinct voltage values, which were needed to determine the voltage and discharge current of the battery under test.

As detailed in section 5.2.1, although the measurement of charge current was not required from the specifications, the firmware was prepared to evaluate this quantity in case the hardware is suitably modified to support this operation, so an additional channel was used.

The sampling time common to all channels was set to 160.5 cycles to achieve the maximum ADC external input impedance (R_{AIN}= 50 kΩ), minimizing loading effects and measurement errors.

ADC was configured to run in scan continuous conversion mode. By using the scan (or multichannel) continuous mode, ADC channels were independently converted one after the other. In this mode, when the ADC reached the last channel of the sequence, it restarted and kept going indefinitely. [39]

The ADC, coupled with DMA, ran in circular mode. In this mode, the ADC continuously generated DMA requests even if the last DMA transfer was done. This was because DMA could work in a circular way restarting automatically from the first position after the last transfer was completed. This generated a ring buffer of continuously updated ADC samples.

Some measurements were taken to estimate the accuracy of the ADC. Using the DAC, properly decoupled with an op-amp in voltage follower configuration, different voltage values were set at the input of the ADC channels.

The DAC voltage was stable but needed to be more accurate compared to the configured value. For this reason, the ADC input voltage was appropriately measured with a multimeter.

100 acquisitions were made for each current value set, the one with the largest deviation from the value measured through the multimeter was taken, and the corresponding error was calculated. These empirical analyses found that the ADC error for low voltages of interest was far too high (ADC error almost 4% at 100 mV).

As a result of these analysis, some measures had to be taken to reduce this error contribution. As reported in section 4.2.3, the best available quantization was already accomplished by setting $V_{REF} = 2.048$, therefore:

$$V_{LSB} = \frac{V_{REF}}{2^{12}} = 0.48mV$$

The simplest strategy to increase the accuracy of the battery electrical parameters measurements was averaging. [40]

It was therefore decided to use a buffer to store multiple values acquired from the same channels for further processing (averaging). Specifically, for each channel, the buffer held a collection of 10 values, allowing for calculating mean values. These values played a significant role in determining the behavior of the logic implemented in the LogicTask.

Table 5.2 shows the empirical estimations of ADC maximum deviations from the actual measured voltage values. The minimum current value of interest was 500 mA, corresponding to an ADC input of 100 mV. The minimum battery voltage value of interest was 2 V, corresponding to 800 mV, so it was not critical.

Input Voltage ADC (mV)	**Expected value (LSB)**	**Read value (LSB)**	**Absolute error (LSB)**	**Absolute error (mV)**	**Percentage error**
99,7	200	204	4	2	2
120,3	241	244	3	1,5	1,24
136,7	274	278	4	2	1,46
156,1	313	317	4	2	1,28
174,7	350	353	3	1,5	0,86
195,1	391	395	4	2	1,02
294	588	595	7	3,5	1,19
393	786	792	6	3	0,76
492	984	991	7	3,5	0,71
796	1592	1604	12	6	0,75
982	1964	1979	15	7,5	0,76
1464	2928	2950	22	11	0,75
1940	3880	3907	27	13,5	0,69

Table 5.2: Empirical evaluation of ADC error when averaging with 10 samples

Another possible strategy for increasing the resolution of analog-to-digital conversion was oversampling. Several optimization methods exist, and most of these techniques are based

on the same principle: oversampling the input signal with the maximum ADC capability and decimating the input signal to enhance its resolution. Some of these methods require particular signals (white noise, triangle wave) to be added to the ADC input signal. [41] These methods can increase the effective number of bits by increasing the Signal to noise ratio (SNR). These strategies exploiting oversampling were not adopted because of their complexity.

Having established the frequency of the ADC (f_{ADC} = 64MHz), the number of channels, and the number of cycles per conversion, it was possible to calculate the total time required to complete the measurement of all quantities of interest.

The conversion time, associated with a single channel, was the sum of the configured sampling time plus the successive approximation time depending on data resolution:

$$t_{CONV} = t_{SAMPLE} + t_{SAR} = (160.5\, cycles + 12.5\, cycles_{|12bit}) \cdot \frac{1}{f_{ADC}} =$$

$$= 173\, cycles \cdot \frac{1}{64MHz} = 2,7\mu\,\mathrm{sec}$$

Thus the time required to convert all the input voltages was:

$$t_{TOT} = t_{CONV} \cdot N_{channels} \cdot N_{samples\ per\ channel} = 2,7\mu s \cdot 10 \cdot 3 = 81\mu s$$

Chapter 6

Testing

A thorough testing campaign for verification and validation was conducted. Starting from unit tests, all the parts of the system were integrated until satisfactory results were reached. Physical quantities were checked with multimeter and oscilloscope, while test execution was monitored by logging data to the pc and elaborating the log file through a Python script. The Python script simply parsed the log file, converted the data into the related measure and arranged it in a CSV format and generated plots.

Tests were conducted on breadboard first and then on stripboard. Stripboard implementation was chosen for prototyping instead of directly designing a PCB in order to have maximum flexibility for possible modifications on the requirements, that could be swiftly implemented in this way.

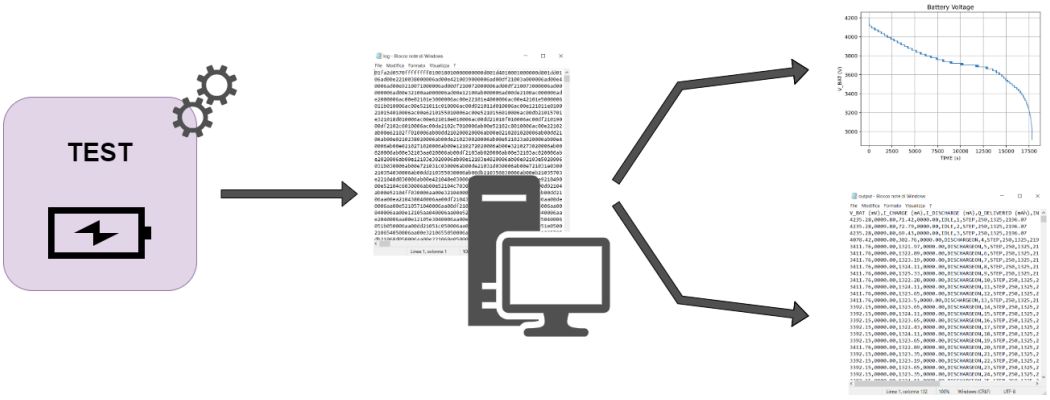


Figure 6.1: Test flow

6.1 Proper functioning of the firmware through additional task

To test the proper functioning of the firmware, with a primary focus on ensuring accurate state transitions within the LogicTask, an additional task was developed to simulate the battery behavior during a test. This task merely generated the values of the electrical parameters monitored in the test (voltage, charge, and discharge current). The values read from the ADC were saved in an array that was not being considered by the LogicTask, so as not to compromise firmware testing.

6.2 Breadboard-mounted discharge circuit tests

The circuit was initially mounted on a breadboard to verify the system's operation was consistent with expectations. All components were mounted on breadboards, excluding the control MOSFETs and the discharge shunt, since currents exceeding 500 mA flowed through them. At this stage, tests were performed using a current-limited power supply to prevent any damage to the circuit due to unwanted current spikes.

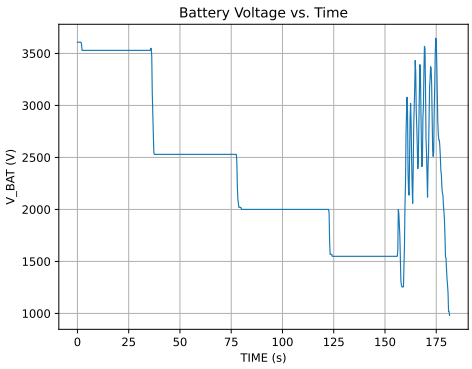
6.2.1 Constant, Step and random tests

Constant tests

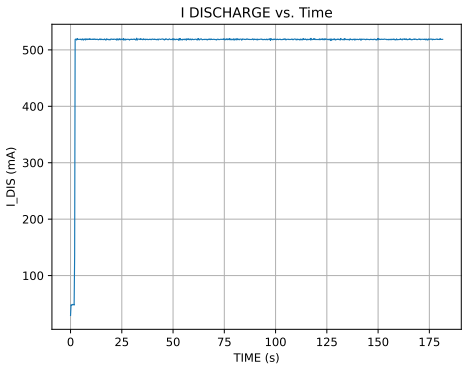
First, constant mode was tested. The value of the rated capacity was set to realistic values. It should be noted that this type of testing ends only when the battery voltage falls below the established cut-off value since they are mainly used to evaluate the effective capacity of the battery under test. These preliminary tests were also carried out to determine the current regulation accuracy of the discharge circuit.

The configuration parameters of a constant current test were (rated capacity set to 2600 mAh):

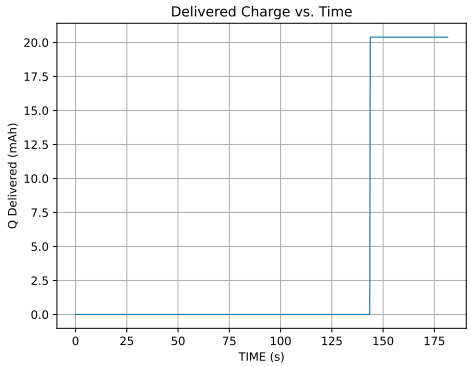
- **Test mode**: CONSTANT
- **Discharge current**: 0.2C (520 mA)
- **Discharge pulse period**: T = 2 s (cooling time set to 2 seconds).
- **Number of steps**: 1 (since this was a constant mode test, only one discharge pulse is needed. In this mode, anyway, the T_{ON} parameter was not considered anyway).



(a) Voltage set through the power supply



(b) Regulated discharge current



(c) Depleted charge

Figure 6.2: CONSTANT 0.2C test with current-limited power supply; breadboard-mounted circuit

The figure 6.2 displays the results of this brief test. At the start of the test, a voltage drop was observed due to the power supply's internal impedance and the resistive contributions of the wires. These contributions caused a reduction in the measured voltage at the power supply output when a current was drawn. The test's goal was to ensure the current's stability by manually changing the applied voltage and checking the current stayed constant.

The image demonstrates that the current remained consistently stable throughout the test, despite the voltage fluctuations introduced to the power supply. The test promptly concluded once the set voltage dropped below the specified cut-off value (with only 1 cycle allowed below $V_{\text{CUT-OFF}}$).

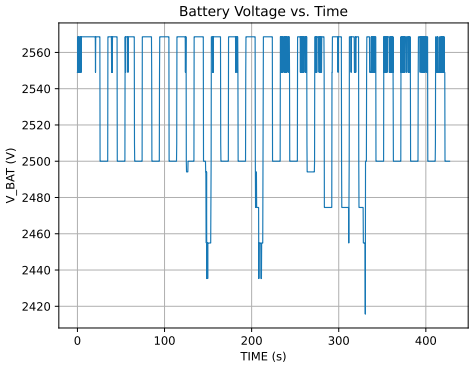
Step tests

Next, characterizing tests were carried out. In the reported case, the rated capacity was set to 26 mAh so that quick tests could be carried out without having to discharge at high currents since the heatsink had yet to be mounted. The test parameters were:

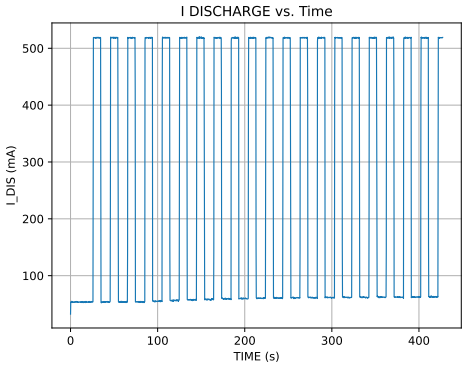
- **Test mode**: STEP
- **Discharge current**: 20C (520 mA Total discharge time = 3 min)
- **Discharge pulse period**: T=20s (cooling time set to 20 seconds)
- **Number of steps**: 180

$$T_{on} = \frac{TotalDischargeTime}{I \cdot N_{step}} = \frac{3min}{20} = \frac{180s}{20} = 9s < T = 20s$$

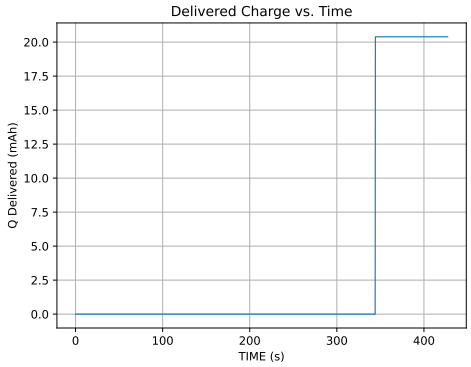
The figure 6.3 displays the results of this brief STEP test. The number of discharge steps specified serves as a rough guideline and primarily determines the duration of the T_{ON} steps: in fact, the test concluded in the middle of the 21st discharge step. The test ended once the depleted charge reached the nominal capacity, although the graph depicting the depleted charge shows a lower value since the resolution of 20.31 mAh.



(a) Voltage set through the power supply



(b) Regulated discharge current



(c) Depleted charge

Figure 6.3: STEP 0.5C test with current-limited power supply; breadboard-mounted circuit

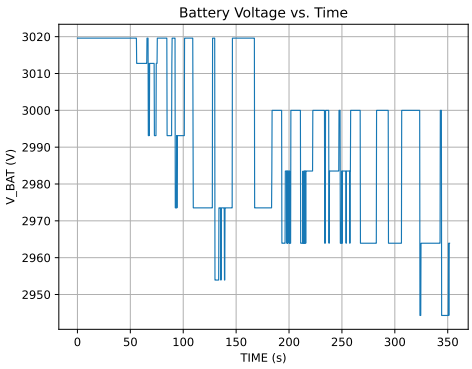
Random tests

Random tests were carried out last. Again, for convenience, the value of the rated capacity was set to unrealistically low values. The discharge pulse period and duty cycle are random values that change from step to step, in this type of test in fact the values of T and T_{ON} given in the configuration parameters are nothing but boundaries (T corresponds to T_{MAX} and T_{ON} corresponds to $T_{ON,\ min}$). Clearly, if the value of T is less than the minimum T_{ON} for a given discharge step, the time the battery will deliver current will be less than the minimum T_{ON}.

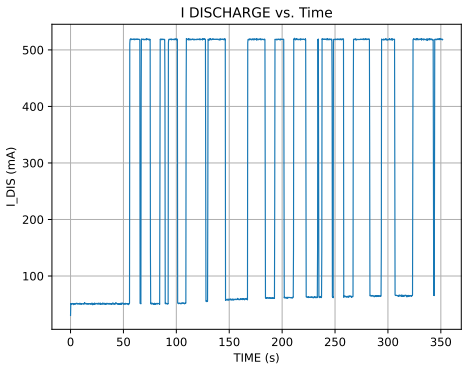
A random test parameters were:

- **Test mode**: RANDOM
- **Discharge current**: 20C (520 mA)
- **Discharge pulse period**: T = 50 s
- **Number of steps**: 180 ($T_{ON,\ min}$ = 1 s)

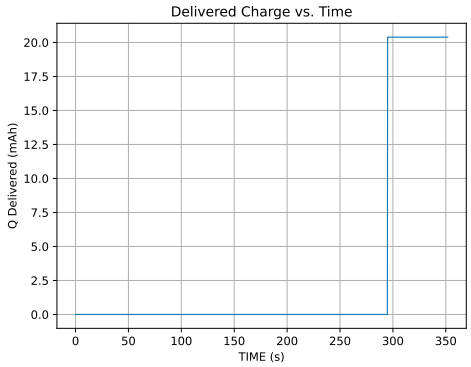
$$T_{ON,min} = \frac{TotalDischargeTime}{I \cdot N_{step}} = \frac{3min}{180} = \frac{180s}{180} = 1s < T = 20s$$



(a) Voltage set through the power supply



(b) Regulated discharge current



(c) Depleted charge

Figure 6.4: RANDOM 0.5C test with current-limited power supply; breadboard-mounted circuit

The results of this RANDOM test are shown in figure 6.4. Again the test ended once the depleted charge reached the value of the real capacity (which corresponded to the nominal capacity since this test was not performed consequentially to a CONSTANT one, that would have updated the capacity value).

6.2.2 DAC transitions

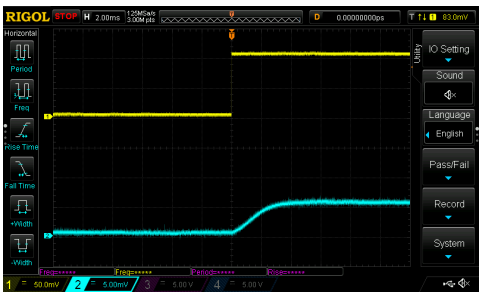
Furthermore, an additional procedure was performed to examine the discharge current trend resulting from DAC voltage transitions. This involved employing an oscilloscope to read the voltage across the discharge shunt and the DAC output. The two aspects of interest in these analyses were:

- the time delay between DAC transition and discharge current transition
- the presence or absence of any current spikes arising from DAC voltage transitions

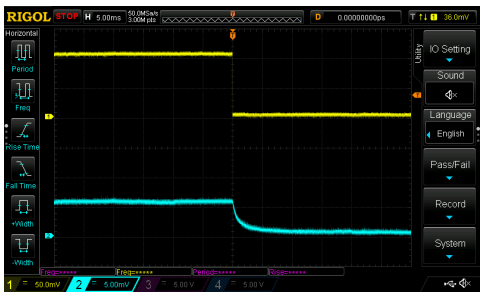
Since the circuit was mounted on a breadboard at this stage of testing, no checks were made

at currents exceeding 1 A.

It can be seen from figure 6.5a that the time between the DAC voltage increment (from 0 V to 5 mV) and the instant when the shunt voltage started to rise iwa negligible. Nevertheless, the shunt voltage takes almost 4 ms to reach 5 mV (that corresponds to a discharge current of 500 mA), which is still significantly less than the cycle time of the LogicTask (50 ms). As for the falling edge (discharge current going from 500 mA to 0 A), as can be seen in figure 6.5b, the time between the DAC decrement and the instant when the shunt voltage started to fall was 0, but the falling time was around 10 ms.



(a) Discharge current rising edge due to DAC increment (0 A to 500 mA)

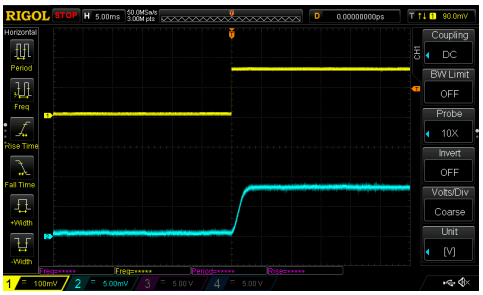


(b) Discharge current falling edge due to DAC decrement (500 mA to 0 A)

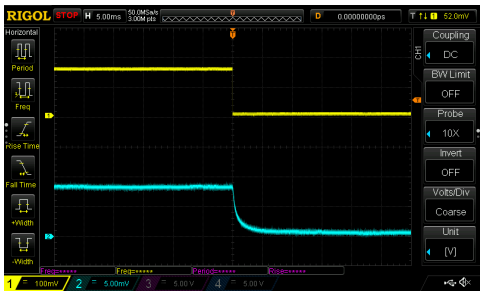
Figure 6.5: Oscilloscope screenshots; DAC voltage (yellow) and shunt voltage (blue); breadboard-mounted circuit; DAC 0 V to 100 mV, discharge current 0 A to 500 mA, and vice versa

The check was repeated using the same procedure, first switching the DAC from 0 to 150 mV (resulting in a discharge current of approximately 750 mA) and later switching it backward. The oscilloscope screenshots depicting this test can be observed in figure 6.6. The shunt voltage took nearly 3 ms to reach 7.5 mV (75 0mA discharge current), which was shorter than the time encountered at 500 mA discharge.

Regarding the falling edge (when the discharge current went from 750 mA to 0 A), there was almost no delay between the DAC decrement and the moment the shunt voltage starts to decrease. However, the falling time was approximately 10 ms, exactly as in the previous case.



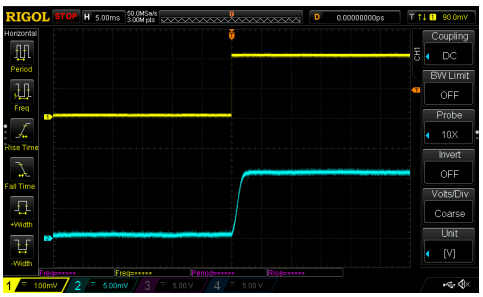
(a) Discharge current rising edge due to DAC increment (0 A to 750 mA)



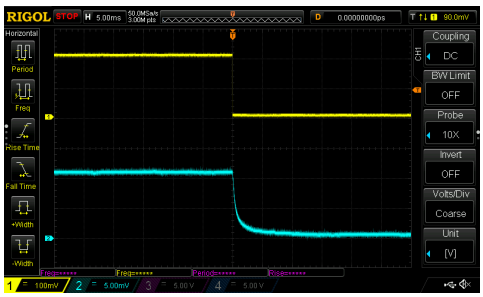
(b) Discharge current falling edge due to DAC decrement (750 mA to 0 A)

Figure 6.6: Oscilloscope screenshots; DAC voltage (yellow) and shunt voltage (blue); breadboard-mounted circuit; DAC 0 V to 150 mV, discharge current 0 A to 750 mA, and vice versa

In Figure 6.7, the DAC voltage transitions from 0 to 200 mV and vice versa are illustrated, along with the corresponding shunt voltage transitions (from 0 to 5 mV and backward). As expected, the rising time of the shunt voltage was even lower than in the previous case, while the falling time was always around 10 ms. In none of the three cases did overshoot or undershoot occur on the shunt voltage as a result of the DAC transitions.



(a) Discharge current rising edge due to DAC increment (0 A to 1 A)



(b) Discharge current falling edge due to DAC decrement (1 A to 0 A)

Figure 6.7: Oscilloscope screenshots; DAC voltage (yellow) and shunt voltage (blue); breadboard-mounted circuit; DAC 0 V to 200 mV, discharge current from 0 A to 1 A, and vice versa

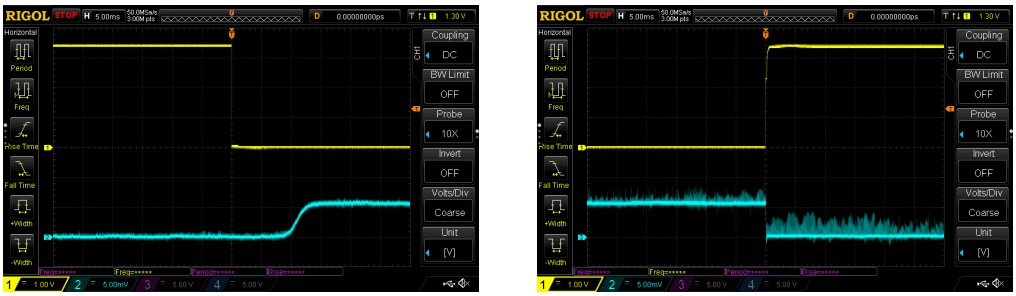
The behavior of the circuit in these three cases shows that t_{rise} of the shunt voltage decreases as the discharge current increased, but that t_{fall} was always around 10 ms regardless of what the discharge current was.

6.2.3 Evaluation of current peaks due to faults

Subsequently, a series of tests were conducted on the breadboard circuit to obtain an initial estimation of the potential current spikes that could arise when activating or deactivating the pull-down MOS while the DAC value was not set to 0. Although the firmware was

structured to prevent this kind of transition, it was prudent to consider the possibility of unforeseen faults. Different hardware measures were implemented to minimize the problem, and these additional checks were done to ensure no potential risks could compromise the device.

Initially, the DAC was set to 100 mV. Since the pull-down MOS was active (V_{GS} set to 3.3V), the discharge current was 0 (shunt voltage at 0) despite the DAC value being set to have a current of 500 mA. Subsequently, the pull-down MOS was deactivated, allowing the driving MOS to conduct. As depicted in figure 6.8a, the shunt voltage did not exhibit any overshoot in the presence of this fault. The shunt voltage took approximately 8 ms, encompassing propagation delay and rising time, to reach a value of 5 mV. However, it is worth noting that since this is a fault scenario rather than a standard transition, the precise timing was not of significant concern.

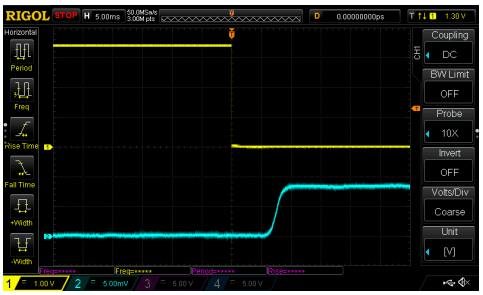


(a) Pull-down MOS ON-OFF transition, 500 mA discharge current

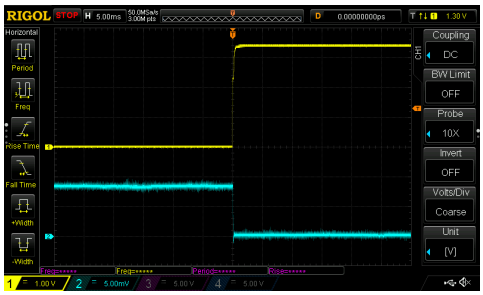
(b) Pull-down MOS OFF-ON transition, 500 mA discharge current

Figure 6.8: Oscilloscope screenshots; pull-down MOS V_{GS} (yellow) and shunt voltage (blue); breadboard-mounted circuit; pull-down MOS turning ON/OFF with 100 mV DAC (500 mA discharge current)

Figures 6.9 and 6.10 show the results of the checks made by setting the DAC at 150 mV and 200 mV respectively (750 mA and 1 A discharge current). In both the first and second cases, there were no current spikes due to the pull-down MOS turning off, but there were small undershoot spikes due to the pull-down MOS turning on.

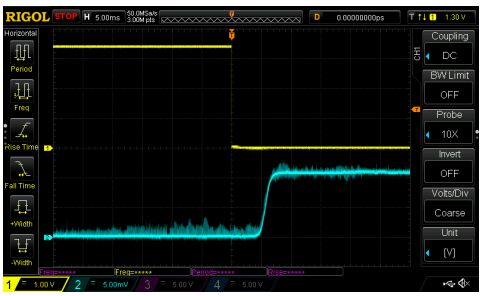


(a) Pull-down MOS ON-OFF transition, 750 mA discharge current

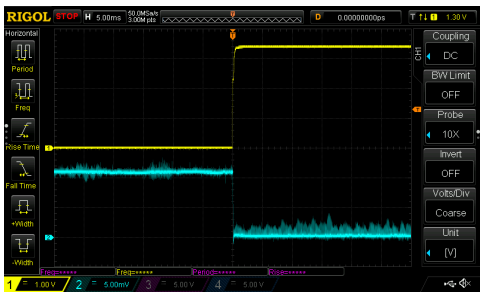


(b) Pull-down MOS OFF-ON transition, 750 mA discharge current

Figure 6.9: Oscilloscope screenshots; pull-down MOS V_{GS} (yellow) and shunt voltage (blue); breadboard-mounted circuit; pull-down MOS turning ON/OFF with 150 mV DAC (750 mA discharge current)



(a) Pull-down MOS ON-OFF transition, 1 A discharge current



(b) Pull-down MOS OFF-ON transition, 1 A discharge current

Figure 6.10: Oscilloscope screenshots; pull-down MOS V_{GS} (yellow) and shunt voltage (blue); breadboard-mounted circuit; pull-down MOS turning ON/OFF with 200 mV DAC (1 A discharge current)

6.3 Stripboard-mounted discharge circuit tests

After the successful breadboard tests, the circuit was mounted on stripboard for its final version.

To gain a comprehensive understanding of the circuit's behavior and obtain a more realistic prediction of its performance during battery tests, the identical tests previously conducted on the breadboard-mounted circuit were replicated with the stripboard-mounted circuit.

By subjecting the circuit to these parallel tests on different mounting platforms, it became feasible to identify any potential disparities or discrepancies that could arise between the two setups.

6.3.1 Mounting rationale

The system mounting was planned thoroughly and in advance: the circuit was divided into sections, arranged with locality and proximity criteria, meaning that all the components related to a certain section could not be scattered and sections interacting with each other had to be as close as possible (i.e., current sensing and driving loop).

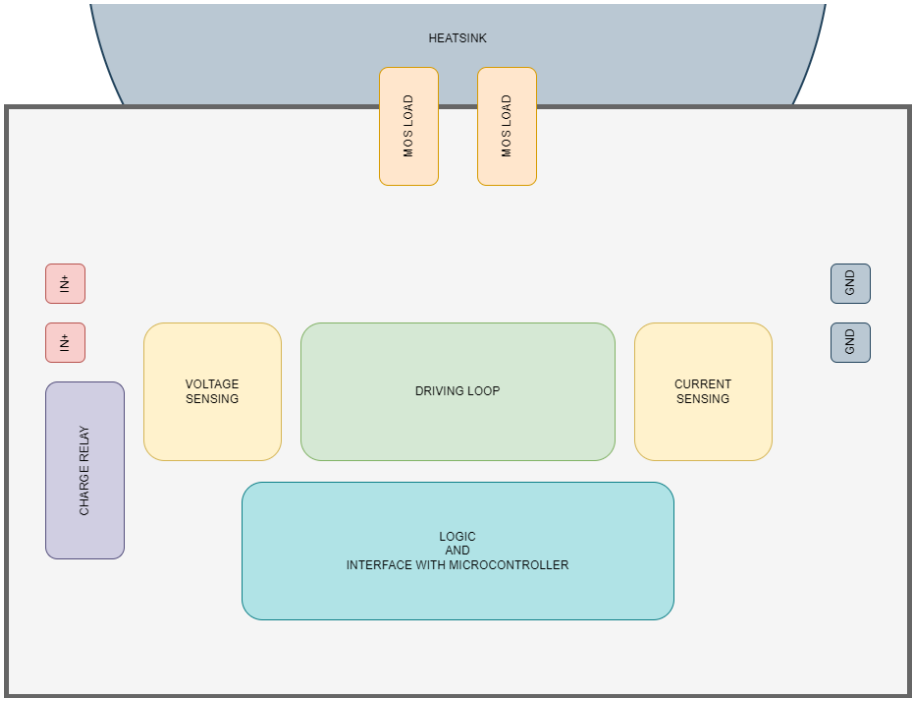


Figure 6.11: Mounting scheme

1% tolerance resistors were used where their values needed to be as accurate as possible. Film capacitors were preferred over ceramic ones, but considering the system behavior, they didn't make much difference. 1 MΩ resistors were placed across the gate-source of each MOSFET, providing a path for discharge in case an excess charge was accumulated on the MOS gate, preventing it from turning on inadvertently.

The starting point of the mounting was the load MOSFETs: their drain could be directly mounted on the heatsink, thanks to the metal tab. They were then soldered to the center of the stripboard edge. Much space was left to the current path, both because of the decision to keep the power and control parts separated as much as possible to avoid disturbances and because the heatsink made it difficult to access the other side of the stripboard.

The current path was completed with the shunt from source to ground, along with a direct connection to the current sensing and driving loop sections, and two clamps to accommodate the cables going to the battery. 1 mm cables were used for these connections to withstand high currents and minimize the resistive effect of the wires.

The driving loop was mounted directly below the load MOS. The two-op amp package chosen

for the MCP6022 allowed some flexibility in mounting choices. Specifically, a single chip was used for the DAC buffer and the driving op-amp, with the former feeding its output into the divider and then into the non-inverting input of the latter.

The current sensing was placed next to the driving loop and close to the shunt resistor itself in order to minimize losses and disturbances on the already low shunt voltage. For the voltage sensing, another clamp was mounted to accommodate a 4-wire measuring with GND and V_{BAT} wires going directly to the battery poles, bypassing the high current path.

The charge relay was placed on one side of the board since it did not occupy much space, exploiting the already present current path for discharging but with an opposite current verse.

Several ground nodes were connected together thoughtfully in order to avoid floating grounds and oscillations on the ground plane.

Finally, the circuit was interfaced with the board by soldering jumpers and properly labeling them.

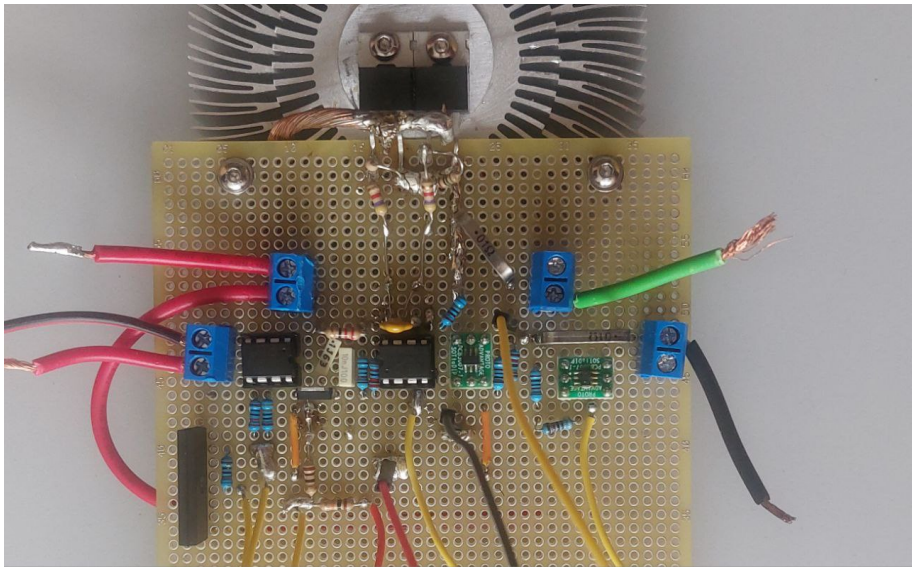


Figure 6.12: Stripboard prototype

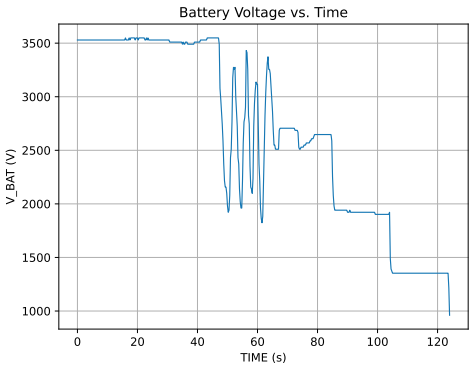
For full functional tests, an additional shunt resistor from the spare components was placed low-side with respect to the charger to act as a test point to study the charger behavior. Using a multimeter to measure the current directly was not feasible since it interfered with the charger's functioning. So, by measuring the voltage across the shunt, it was possible to determine the maximum current that the charger was able to deliver and ensure that the charge wasn't affected by custom connections. A spare precision op-amp, supplied separately, was added, too, since the low shunt voltage alone was comparable with the instrumentation resolution and needed amplification.

6.3.2 Constant, Step and random tests

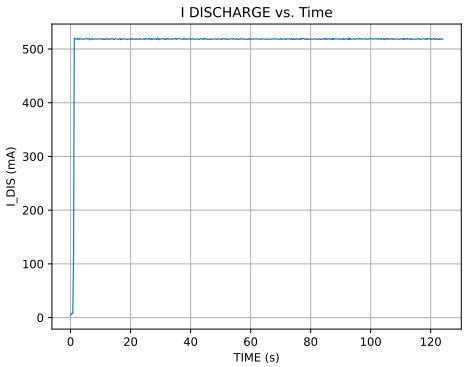
This subsection reports the results of tests performed with the circuit mounted on a stripboard, again using a current-limited power supply instead of a battery.

Constant

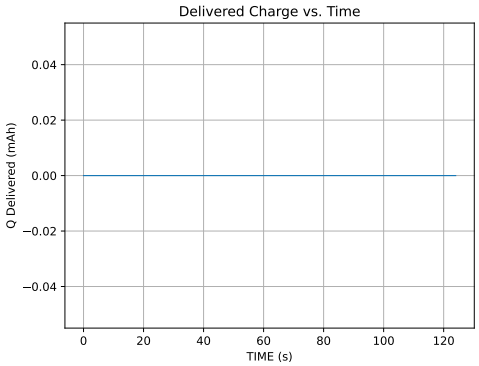
The voltage, current, and depleted charge graphs related to a CONSTANT 0.2C test (rated capacity set at 2600 mAh, thus discharge current of 520 mA) are shown below.



(a) Voltage set through the power supply



(b) Regulated discharge current



(c) Depleted charge

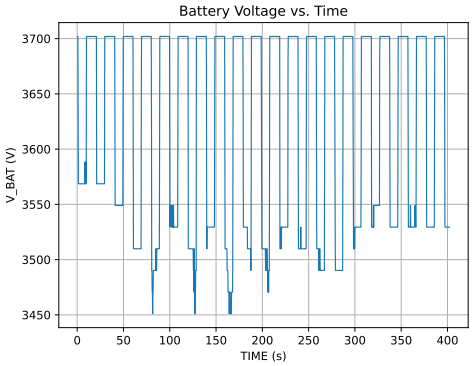
Figure 6.13: CONSTANT 0.2C test with current-limited power supply; stripboard-mounted circuit

The pictures show that despite the voltage fluctuations applied to the power supply, the current remained stable at around 520 mA throughout the test. Due to the short duration of the test, the charge depletion shown in the graph remained consistently at 0, not even reaching the minimum resolution.

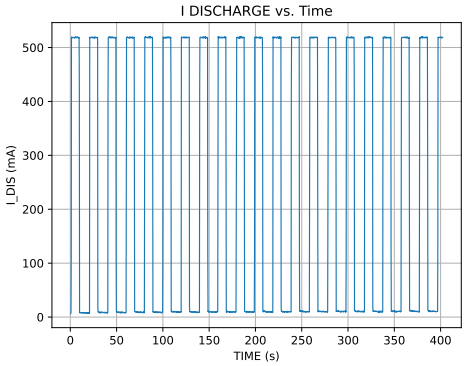
Step

The voltage, current, and depleted charge graphs related to a STEP 20C test (rated capacity set at 26 mAh, thus discharge current of 520 mA) are shown in Figure 6.14.

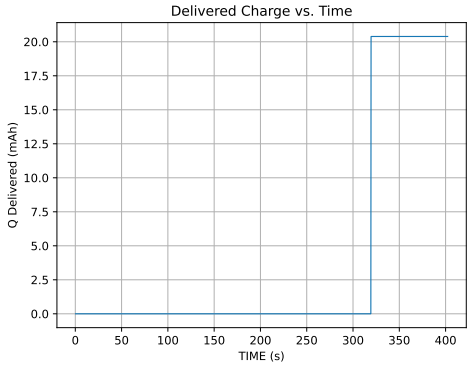
It can be seen that current regulation was performed correctly throughout the test. There were voltage drops during the T_{ON} phases (discharge pulses) due partly to the internal resistance of the power supply and partly to the connections. The test ended when the depleted charge reached the real capacity (which corresponded to the nominal capacity in this case).



(a) Voltage set through the power supply



(b) Regulated discharge current



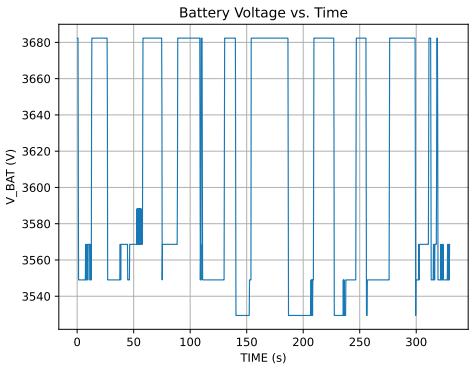
(c) Depleted charge

Figure 6.14: STEP 0.5C test with current-limited power supply; stripboard-mounted circuit

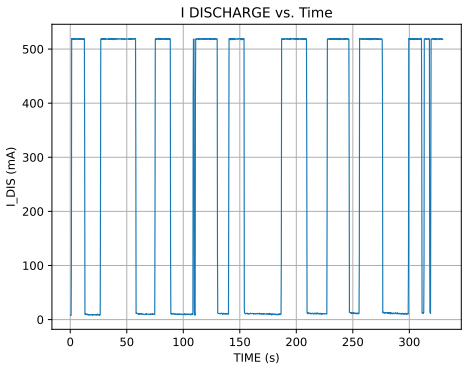
Random

The electrical characteristics plots related to a RANDOM 20C test (rated capacity set at 26 mAh, thus discharge current of 520 mA) are shown in figure 6.14.

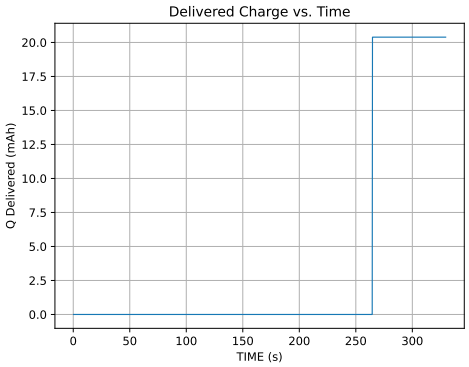
Again, the test ended following the achievement of rated capacity. The voltage dips obtained during the discharge pulses were attributed to the internal series resistance of the power supply and the connections to the power supply itself.



(a) Voltage set through the power supply



(b) Regulated discharge current



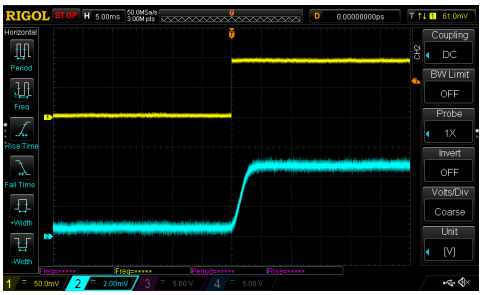
(c) Depleted charge

Figure 6.15: RANDOM 0.5C test with current-limited power supply; stripboard-mounted circuit

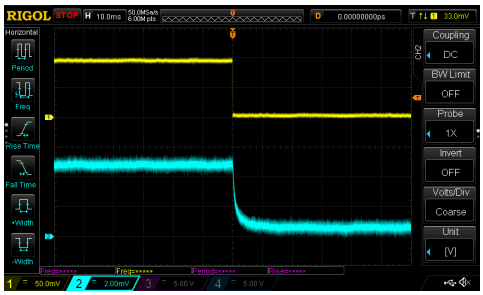
6.3.3 DAC transitions

As done with the breadboard-mounted circuit, the behavior of discharge current in relation to DAC voltage transitions was evaluated. Screenshots showing transitions of the DAC output and changes in the discharge current (voltage across the shunt) are reported.

As a first test, the DAC was switched from 0 to 100 mV (corresponding to a 0 A and 500 mA discharge current, respectively) and vice versa, leaving the pull-down MOS open. The obtained results (figure 6.16) were roughly identical to those obtained with the breadboard-mounted circuit. The response time of the shunt voltage to the DAC increase was about 4 ms, while the falling time of the shunt voltage (as a result of the DAC decrease) was around 10 ms.



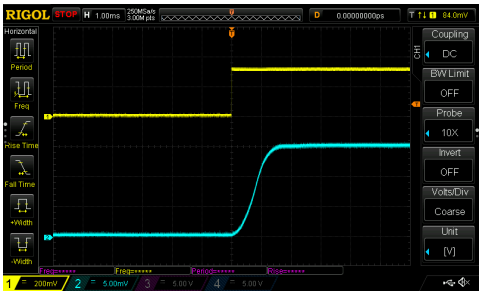
(a) Discharge current rising edge due to DAC increment (0 A to 500 mA)



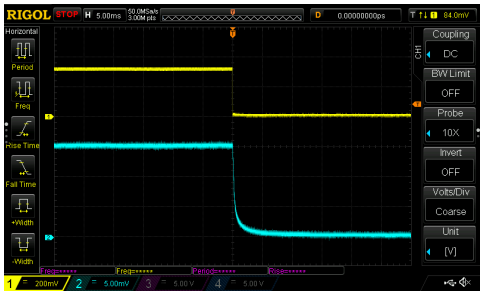
(b) Discharge current falling edge due to DAC decrement (500 mA to 0 A)

Figure 6.16: Oscilloscope screenshots; DAC voltage (yellow) and shunt voltage (blue); stripboard-mounted circuit; DAC 0 V to 100 mV, discharge current 0 A to 500 mA, and vice versa

The same procedure was repeated, this time increasing/decreasing the DAC voltage by 300 mV (corresponding to a discharge current of 1.5 A). As expected, by increasing the DAC voltage increment, the rise time of the shunt voltage was reduced (about 1.6 ms as shown in figure 6.17a), and there was no overshoot. Figure 6.17b shows the shunt voltage trend following the decrease of DAC voltage to 0. Unlike all previous checks, including those on breadboard, there was for the first time a reduction of the falling time to about 5 ms (in previous cases, it was always around 10 ms).



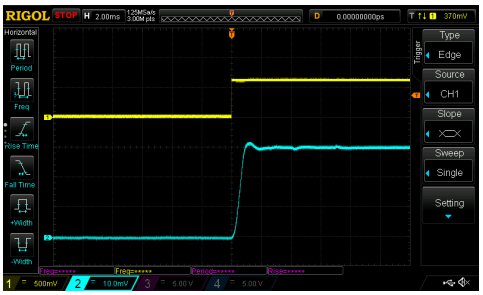
(a) Discharge current rising edge due to DAC increment (from 0 A to 1.5 A)



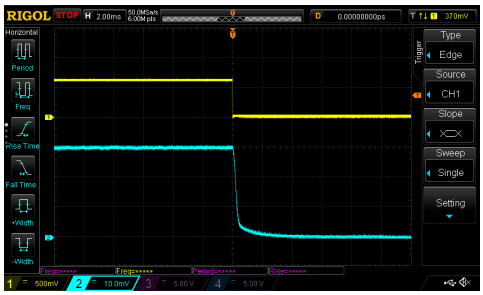
(b) Discharge current falling edge due to DAC decrement (1.5 A to 0 A)

Figure 6.17: Oscilloscope screenshots; DAC voltage (yellow) and shunt voltage (blue); stripboard-mounted circuit; DAC 0 V to 300 mV, discharge current from 0 A to 1.5 A, and vice versa

Finally, shunt voltage transients due to DAC voltage steps of 600 mV were checked. Although decreasing the shunt voltage from 60 0mV to 0 V (figure 6.18b) resulted in a further decrease of the shunt voltage transient (t_{fall} around 2 ms), increasing the DAC from 0 V to 600 mV (figure 6.18a) resulted in a slight overshoot of the shunt voltage. In face of this last check, it was decided to impose a maximum increase on the DAC voltage of 300 mV via FW to prevent any unwanted current spike during test execution.



(a) Discharge current rising edge due to DAC increment (0 A to 3 A)



(b) Discharge current falling edge due to DAC decrement (3 A to 0 A)

Figure 6.18: Oscilloscope screenshots; DAC voltage (yellow) and shunt voltage (blue); stripboard-mounted circuit; DAC 0 V to 600 mV, discharge current 0 A to 3 A, and vice versa

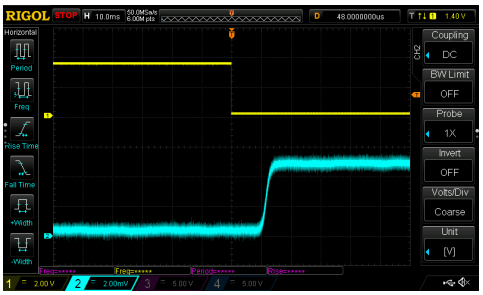
6.3.4 Evaluation of current peaks due to faults

Finally, tests were performed to quantify current spikes due to faults (pull-down MOS switching OFF/ON at non-zero DAC voltages).

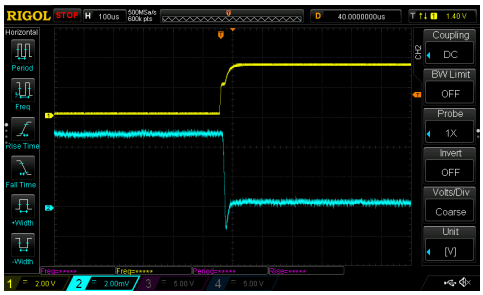
Figures 6.19, 6.20 and 6.21 depict tests where faults were replicated at three distinct DAC voltages, namely 100 mV, 300 mV, and 600 mV.

In none of the aforementioned scenarios did the deactivation of the pull-down MOS while the DAC output retained a non-zero value result in any current overshoots. Additionally, it is notable that the shunt voltage's response time to the deactivation of the switching MOS was inversely proportional to the DAC voltage (although since this is an abnormal condition not expected during the test execution, the timing is not particularly relevant).

Regarding the faults induced by the activation of the pull-down MOS, progressive increments in voltage undershoots could be observed in the shunt voltage as the DAC voltage, and correspondingly, the discharge current escalated. The recorded voltage undershoot values standed at approximately 1.5 mV, 3 mV, and 6.5 mV (equivalent to 150 mA, 300 mA, and 700 mA). These values significantly surpassed those obtained on breadboard and simulation visualization, suggesting that the issue likely stemmed from parasitic effects resulting from soldering on the stripboard.

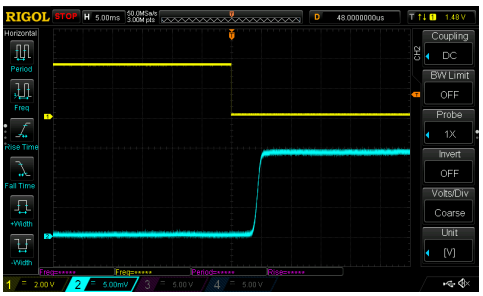


(a) Pull-down MOS ON-OFF transition, 500 mA discharge current

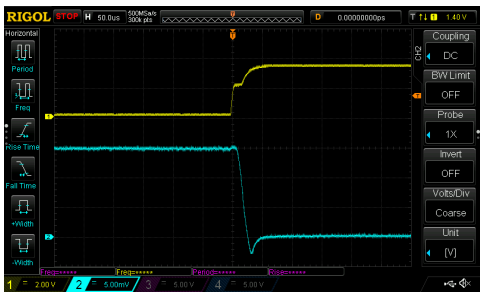


(b) Pull-down MOS OFF-ON transition, 500 mA discharge current

Figure 6.19: Oscilloscope screenshots; pull-down MOS V_{GS} (yellow) and shunt voltage (blue); stripboard-mounted circuit; pull-down MOS turning ON/OFF with 100 mV DAC (500 mA discharge current)

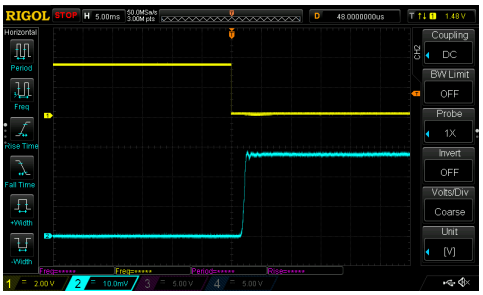


(a) Pull-down MOS ON-OFF transition, 1.5 A discharge current

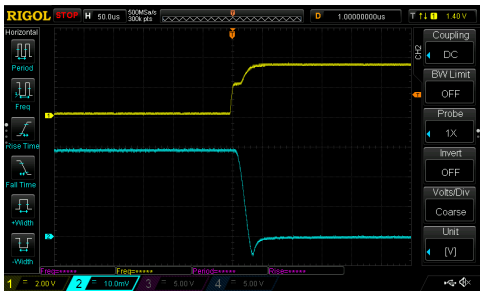


(b) Pull-down MOS OFF-ON transition, 1.5 A discharge current

Figure 6.20: Oscilloscope screenshots; pull-down MOS V_{GS} (yellow) and shunt voltage (blue); stripboard-mounted circuit; pull-down MOS turning ON/OFF with 300 mV DAC (1.5 A discharge current)



(a) Pull-down MOS ON-OFF transition, 3 A discharge current



(b) Pull-down MOS OFF-ON transition, 3 A discharge current

Figure 6.21: Oscilloscope screenshots; pull-down MOS V_{GS} (yellow) and shunt voltage (blue); stripboard-mounted circuit; pull-down MOS turning ON/OFF with 600 mV DAC (3 A discharge current)

6.4 Battery Tests

While the power supply was a controllable source with overcurrent protection and no safety risks in case of overvoltages or current spikes in the circuit, live tests with the battery were exposed to this kind of hazard due to the lack of protection circuits on the battery themselves.

As shown in figure 6.22, a proper environment was set up in order to allow live monitoring of battery current and voltage through a voltmeter and an ammeter. Moreover, the ammeter internal fuse was exploited as an additional protection against overcurrents. The ammeter internal fuse didn't allow currents higher than 10 A for a few seconds.

After thoroughly testing the reliability and safety of the discharge section only, the charger was inserted for complete tests. Since the ammeter interfered with the charging, resulting in a lower charge current than the expected one, it was removed later.

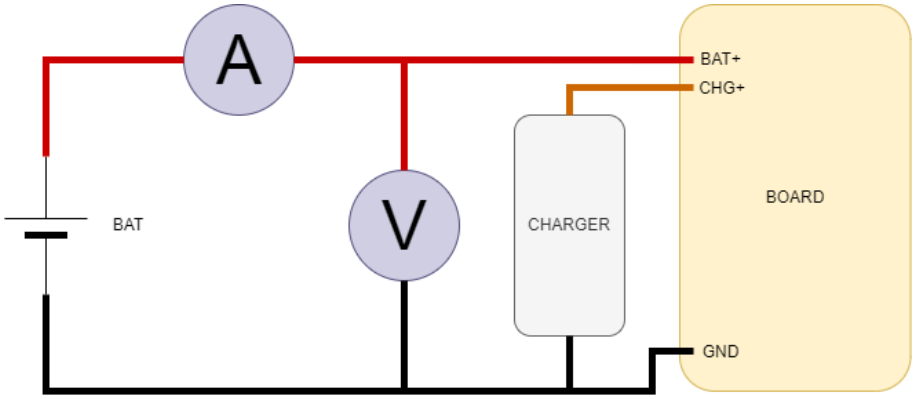


Figure 6.22: Test environment scheme

6.4.1 Selected batteries

The decision to choose these batteries was based on several factors, including their affordability, rechargeability within a reasonable amount of time, and the opportunity to test the circuit across a reasonable range of currents. Since the availability of individual cells in the market was limited and quite expensive compared to the total budget for the device, two batteries from different manufacturers were selected, the SANYO UR18650ZT and the SAMSUNG ICR1865026F. One backup cell was bought for each cell.

UR18650ZT

Figure 6.23: UR18650ZT Panasonic Lithium-ion Rechargeable Cell

- **Rated capacity**: Min. 2650 mAh
- **Capacity**: Min. 2700 mAh; Typ. 2800 mAh
- **Nominal Voltage**: 3.7 V
- **Charging**: CC-CV (constant voltage with limited current) Std. 1890 mA, 4.30 V, 3.0 hrs
- **Discharge Cutt-Off voltage**: 3 V
- **Charge temperature**: 0 to +45°C
- **Discharge temperature**: -20 to +60°C [42]

As can be seen in the figure 6.24, as the rate of discharge decreased, the amount of depleted charge from the battery increased, which is why all CONSTANT tests performed to assess the effective capacity of the battery were performed at 0.2C.

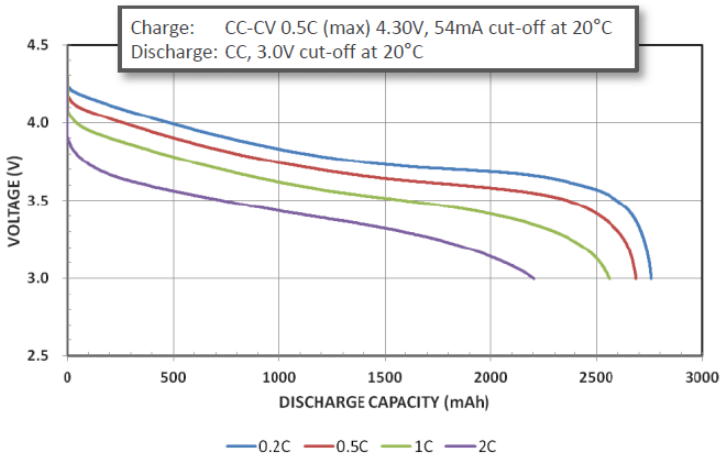


Figure 6.24: UR18650ZT discharge characteristics by rate of discharge

ICR1865026F

Figure 6.25: ICR18650-26F SAMSUNG Lithium-ion Rechargeable Cell

- **Rated capacity**: 2600 mAh (0.2C, 2.75 V discharge)
- **Minimum Capacity**: 2550 mAh (0.2C, 2.75 V discharge)
- **Nominal Voltage**: 3.7 V
- **Charging Method**: CC-CV (constant voltage with limited current)
- **Charging Current**: Standard charge: 1300 mA ; Rapid charge : 2600 mA
- **Charging time**: Standard charge: 3 hours; Rapid charge : 2.5 hours
- **Max Discharge current**: 5200 mA (ambient temperature 25℃)
- **Discharge Cutt-Off voltage**: 2.75 V
- **Charge temperature**: 0 to 45℃
- **Discharge temperature**: -20 to 60℃ [43]

6.4.2 UR18650ZT Tests

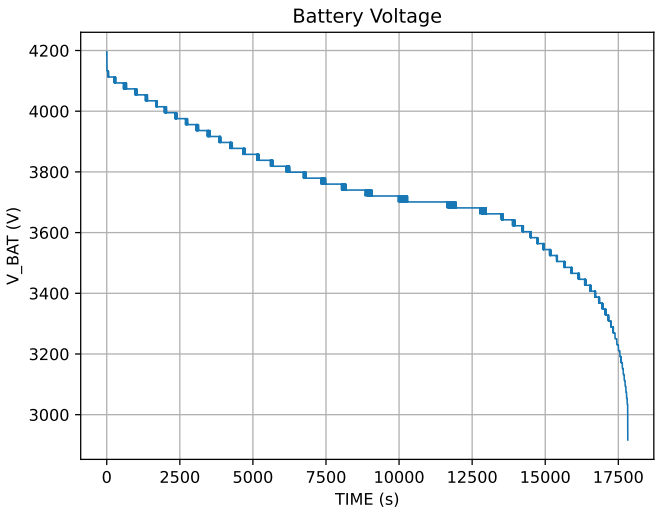
Constant test

The constant mode test parameters were:

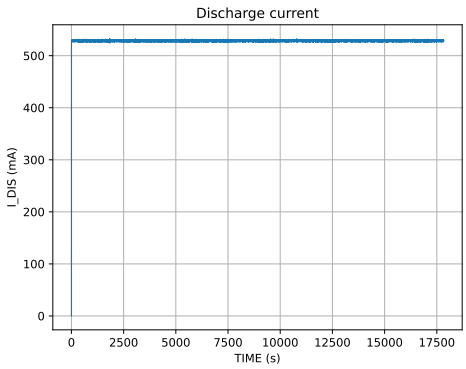
- **Discharge current**: 0.2C (530 mA)
- **Discharge pulse period**: T = 1 s (the test was started with a charged battery, so the cooling time was set to a negligible value to start the discharge stage as soon as possible.).
- **Number of steps**: 1 (since this was a test constant, only one discharge pulse was needed, although, in this mode, the T_{ON} parameter was not considered anyway).

The test result (figure 6.26) was coherent with the expected one. The battery voltage profile followed the pattern shown in the datasheet and, in general, was the typical discharge curve of these kinds of batteries. [44] The discharge current was almost constant, as expected. The coherence of the measured current with the effective one in the circuit was verified manually throughout the whole test, observing variations of about 10 mA.

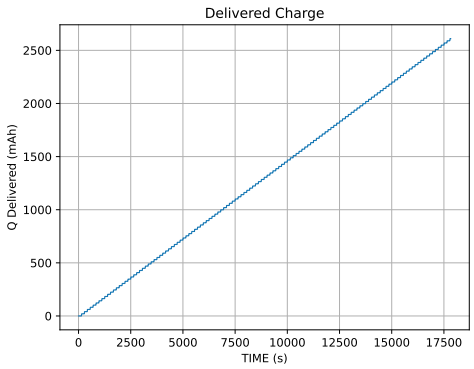
Consequently, the delivered charge had a linear trend, again consistent with the expectations, accounting for an effective capacity of around 2650 mAh, therefore consistent with the nominal data.



(a) Battery voltage during test



(b) Regulated discharge current



(c) Depleted charge

Figure 6.26: CONSTANT 0.5C test on UR18650ZT battery

Step test

The configuration parameters of a step test that was performed on the UR18650ZT battery are given below:

- **Discharge current**: 0.5C (1.3 A)
- **Discharge pulse period**: T = 1200 s (20 min)
- **Number of steps**: 12

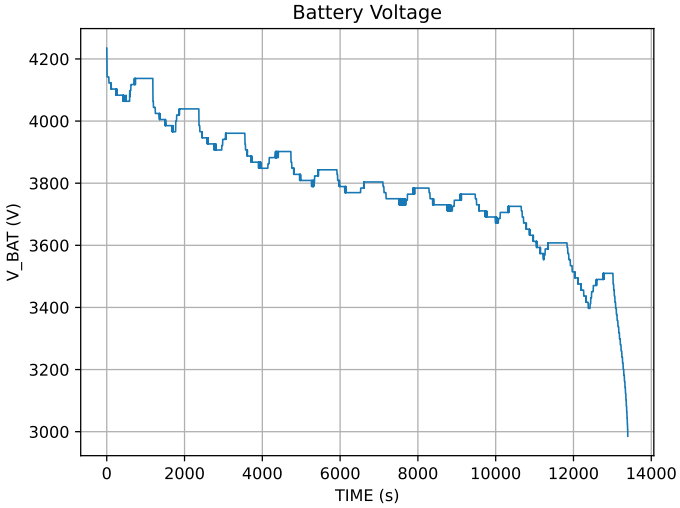
Since the discharge rate was set to 0.5C, the estimated total time to discharge the lithium-ion cell was 2 h.

The discharge pulse time T_{ON} was calculated as follows:

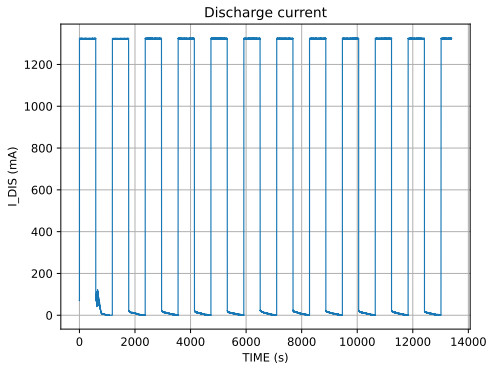
$$T_{ON} = \frac{TotalDischargeTime}{I \cdot N_{step}} = \frac{2h}{12} = \frac{120min}{12} = 10min -> DC = \frac{T_{ON}}{T} = \frac{10min}{20min} = 0.5$$

From empirical tests, it was inferred that a 50% duty cycle was sufficient to let the battery voltage stabilize after a discharge pulse.

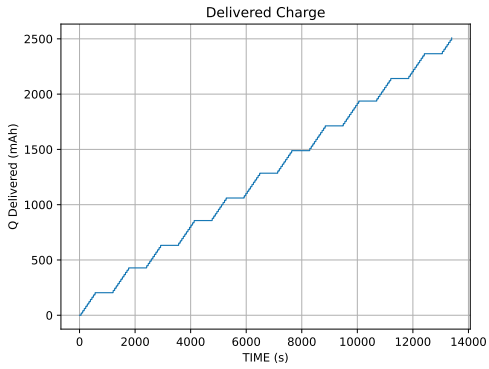
Although the value of T was 20 minutes, since the test starts with a charged battery, the firmware was appropriately modified to start the discharge immediately, without waiting for an unnecessary cooling time.



(a) Battery voltage during test



(b) Regulated discharge current



(c) Depleted charge

Figure 6.27: STEP 0.5C test on UR18650ZTF battery

The behavior appeared again consistent. As expected, the test was shorter because the

higher current stressed the battery more.

It is worth noting that even when the discharge was deeper, particularly at the end of the test and at the beginning, where the voltage variation was significant in a short time, T_{off} was still sufficient to let the battery recover its stable status.

Voltage drops could be seen as soon as the discharge started due to the connections' resistive contribution and internal impedance.

The discharge current showed the expected pattern, with the only interesting detail being that it didn't reach 0 A as soon as the discharge was stopped. Instead, there was a transient likely due to capacitance discharging over the circuit. After the first discharge, a more pronounced transient could be observed; however, it didn't impact the whole test and was not present in successive transitions, so it could be classified as a local phenomenon.

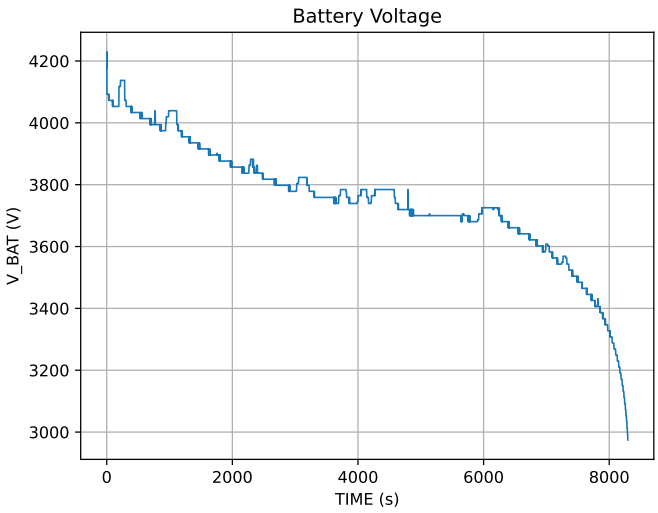
Random test

The RANDOM test parameters were:

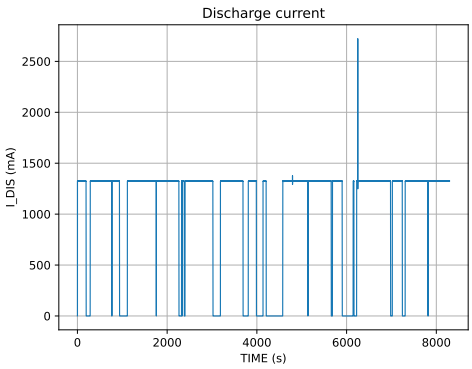
- **Discharge current**: 0.5C (520 mA, Total Discharge time = 2 h)
- **Discharge pulse period**: T = 1500 s (25 min)
- **Number of steps**: 7200

$$T_{ON,min} = \frac{TotalDischargeTime}{I \cdot N_{step}} = \frac{2h}{7200} = 1s$$

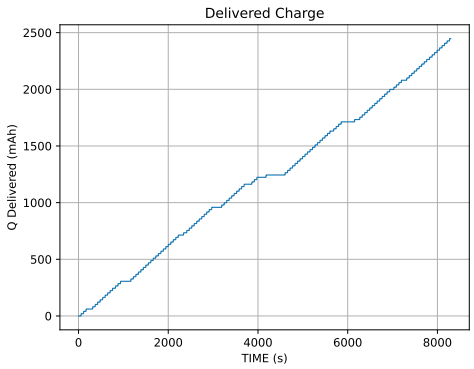
As already stated, the number of steps in a RANDOM test was uniquely set to indicate the minimum T_{ON}. Imposing a higher N_{STEP} value would not have resulted in a lower $T_{ON,min}$ value anyway since the code was structured so that it was always greater than or equal to 1 s.



(a) Battery voltage during test



(b) Regulated discharge current



(c) Depleted charge

Figure 6.28: RANDOM 0.5C test on UR18650ZTF battery

On the one hand, the test showed a similar behavior to the step one, with steps of variable duration. On the other, the voltage trend was comparable to the constant one due to the generated pattern, just shorter because of the higher current.

Because of this latter analogy, during test execution, heat generation was way more significant than during the constant test. The test was carried out with passive cooling, without installing the vent, and even though the heat was not excessive, it clearly showed that at currents above 1.2 A, active cooling would become crucial to overcome the possibility of long discharge phases.

Moreover, the discharge plot highlighted a huge current peak around the 6000 s mark. A small ripple had already appeared around the 5000 s mark. Due to the distance between the two, they were assumed to be uncorrelated. Both spikes happened during discharge, and

their cause was hard to detect: it could either have been a wrong sample on the ADC, a wrong packet, or an unforeseen oscillation on the DAC. Assuming a current spike physically happened, it can be inferred that the system had a prompt response, possibly adjusting the DAC to compensate for the unexpected event in a short time: the spike was composed of 4 samples, so it accounted for 200 ms at most. Considering the duration of the entire test, it didn't actually affect the outcome.

Still, such spikes could pose a threat to battery safety, and even though they were never recorded again in successive tests, they should be monitored throughout the development of the system.

6.4.3 ICR1865026F Tests

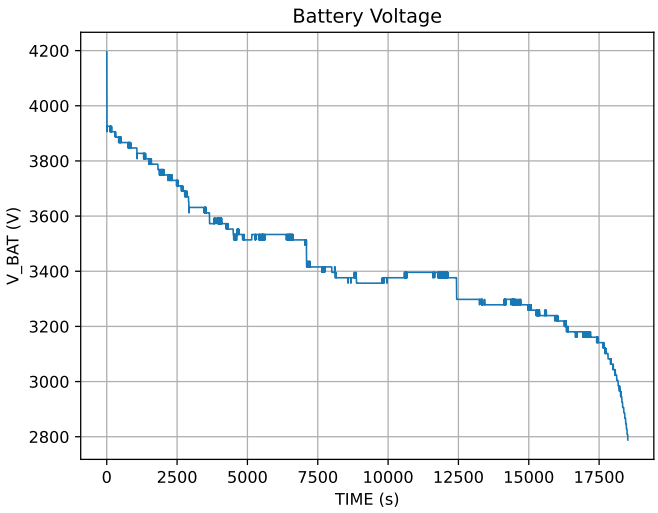
The same tests performed on the UR18650ZT were replicated.

Constant test

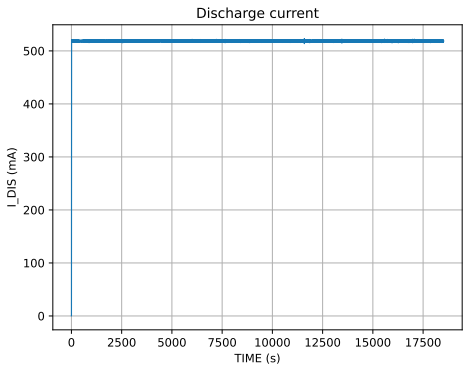
The results of a CONSTANT test performed on an ICR18650-26F battery with a discharge rate of 0.2C (530 mA) are shown in figure 6.29.

The results appeared consistent with the UR18650ZT one, despite not being as smooth. It's worth highlighting two sudden voltage drops around the 7400 s mark and the 12500 s mark: they happened when the desk where the test was performed was inadvertently bumped. The 100 mV drop was visible on the multimeter connected to the circuit, probably due to some poor connection, and the system detected it accordingly.

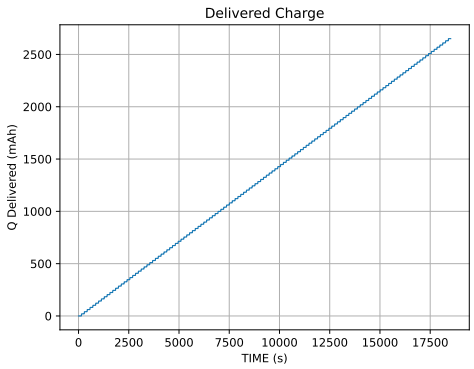
This implied the need to better isolate the test environment since the circuit was sensible to mechanical disturbances and improve the connection's robustness as much as possible.



(a) Battery voltage during test



(b) Regulated discharge current

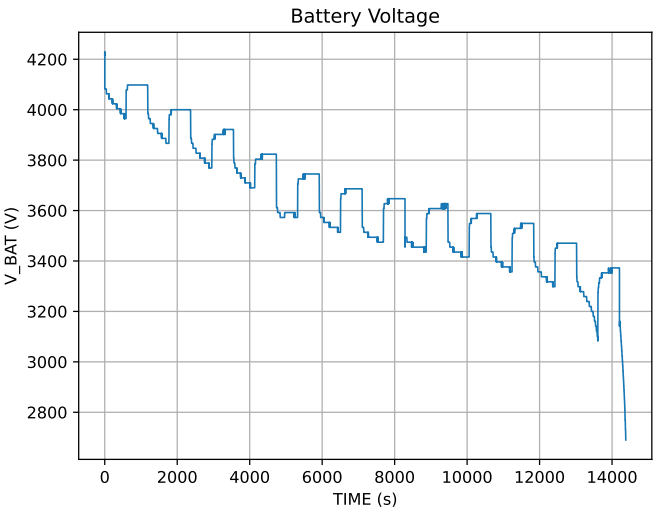


(c) Depleted charge

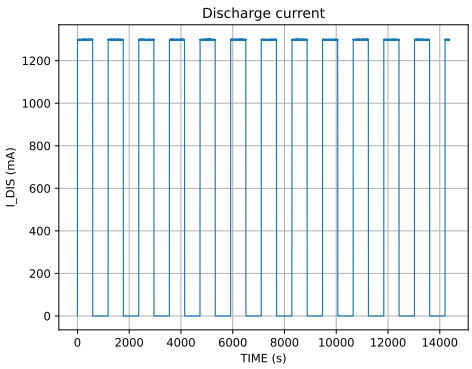
Figure 6.29: CONSTANT 0.5C test on ICR18650-26F battery

Step test

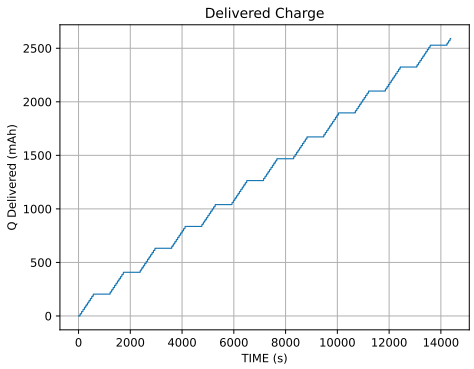
The results of a STEP test performed on an ICR18650-26F battery with a discharge rate of 0.5C (1325 mA) are shown in figure 6.30. A discharge pulse time T_{ON} of 10 minutes (number of steps set to 12) and a discharge pulse period T equal to 20 min (Duty Cycle of 50%) was set for the test.



(a) Battery voltage during test



(b) Regulated discharge current



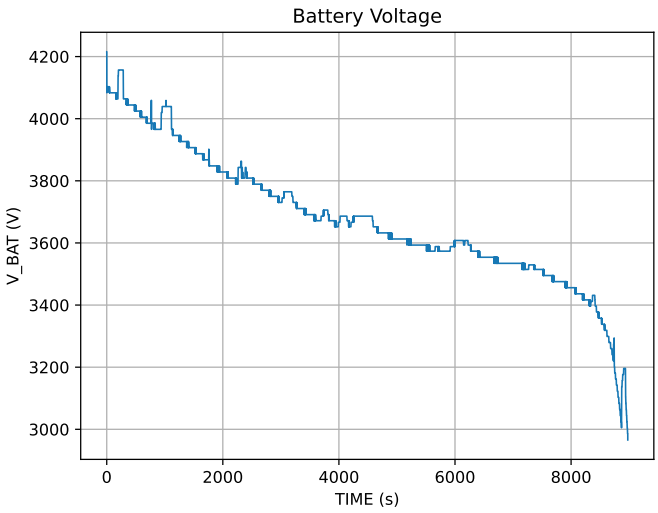
(c) Depleted charge

Figure 6.30: STEP 0.5C test on ICR18650-26F battery

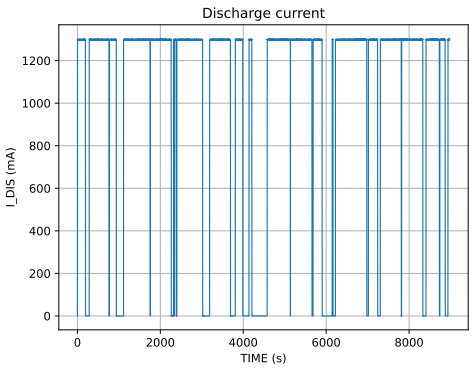
The behavior was again consistent with the UR18650ZT one, except for a higher drop when the system started discharging.

Random test

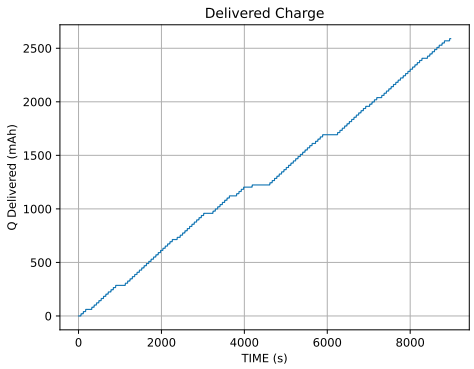
The results of a RANDOM test performed on an ICR18650-26F battery with a discharge rate of 0.5C (1325 mA) are shown in figure 6.31.



(a) Battery voltage during test



(b) Regulated discharge current



(c) Depleted charge

Figure 6.31: RANDOM 0.5C test on ICR18650-26F battery

The result was once again similar to the test performed on the UR18650ZT.

Although not clearly visible from the plots, by analyzing the CSV output file in detail, it could be deduced that the test was terminated due to the delivered charge crossing the effective capacity threshold. This showed an important result: it proved the system effectively took into account the desired factors to decide whether to end the test, considering that until this test, the termination had always been caused by the voltage crossing the critical voltage threshold.

6.4.4 Test outcome

The system showed consistent behavior, compliant with the technical requirements. Whether the tests were complete or divided into separate sub-tests, it was able to carry out the required operations with satisfactory accuracy and no significant drift over the test course. The system was exposed to external disturbances since tests lasted several hours; however, it was able to react efficiently and manage faults to resume regular operations quickly, maintaining the test valuable.

External connections, loose contacts, and mechanical stress were the main sources of disturbances on the circuit, adding noise to the measurement or offsets to the voltage seen at the board inputs compared to the real battery one. This practically implied an accuracy degradation of the results, both because of the sensed noise or a premature exit from the test because of the battery voltage sensed under the threshold, even if it was actually still above it.

However, it is worth noting that the time differences were quantified in minutes, with the total test time being several hours. Connections and soldering were carefully refined until their effect was satisfactory, though never negligible.

Giving detailed documentation about these uncertainties would be very time-consuming and is out of this project's scope.

Overall, it can be concluded that as long as the environment was guaranteed to be isolated from external interference, the system proved reliable for its intended purposes.

Chapter 7

Conclusions and future perspectives

7.1 Conclusions

This thesis aimed to develop a prototype able to discharge a battery in a safe and controlled environment and collect the electrical parameters necessary to characterize a Li-ion cell.

Starting from the requirements stated by the already existing theoretical algorithms, the device was designed, mounted on a stripboard, and went through a thorough verification and validation process.

The final stripboard prototype accomplished the desired results, providing a test environment to collect preliminary data for algorithms validation and development and a starting point for more complex and accurate test benches.

The prototype was able to perform complete tests without manifesting performance issues or accuracy deterioration over several hours, different test conditions, battery heating, and external disturbances.

The data transmission proved not problematic despite no robust control on data integrity was performed. A Python script allowed for fast and effective processing of the log. It generated the final outcome of the device in the form of a CSV file ready to be fed to the algorithms for SoH and SoC estimation, executed externally.

The device was also able to successfully recover from disturbances that may have occurred during test execution, resuming the proper execution in a short time without invalidating the whole test. Poor connections or mechanical stress showed increased uncertainty on the collected parameters but didn't compromise the significance of the tests.

The behavior during critical parts of the tests was consistent; in particular, current spikes during transitions were contained.

Measurement accuracy was limited by the discrete nature of the prototype and the need to use through-hole components. Components tolerances significantly impacted the ex-

pected uncertainty, and discrete connections implied not negligible parasitic capacitance and resistive contributions, which affected the whole system. These effects were lowered as much as possible by choosing the most accurate available components, paying attention not to increase the prototype cost significantly, and refining connections and soldering until satisfactory results were reached. Ultimately, the uncertainty contributions were carefully tackled to meet sufficient accuracy compared to the requirements.

Overall, the device successfully tackles the required functions and is able to perform the necessary operations consistently over the whole test duration.

7.2 Future perspectives

The developed prototype constitutes a solid starting point, leaving ample floor for further development of the BAT-MAN 2nd Life project while already delivering a ready-to-use device to test batteries and collect useful physical data.

First, further tests should be performed at higher currents to verify the correct functioning in the whole operating range. The tests run on the prototype covered the actual range of planned tests for this thesis scope only.

Then, the system may be improved over several features. Since the architecture was finally verified and proved consistent, the following step to enhance the accuracy and overall performance of the system is the integration on PCB or the development of an ASIC.

A more complex charge section could also be designed, providing a way to monitor the charge current and reduce the test time by exiting the charge when the current gets below a threshold.

Firmware-wise, with few modifications, it could be possible not just to discharge at a certain constant current but also to track different and more complex current profiles. This could be useful to widen the range of tests that could be accomplished both for characterization purposes and general research on Li-ion batteries' behavior and response to different stress conditions.

Further in time, many devices like this one may be interconnected in a more complex system, with the goal of pipelining or parallelizing the charge and discharge of several cells. This would imply more profound modifications on firmware and hardware, along with new challenges related to power dissipation and complexity of the system, but would significantly cut the test time, resulting in a crucial improvement for a battery testing device.

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