POLITECNICO DI TORINO

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GaN DC/AC Multilevel Converter for PV Application

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Summary

Nowadays, energy conversion plays a significant role in sustainable growth . Efficient energy conversion systems are based on power electronic converters thatare switching circuital structures. In renewable energy conversion, smart grid arrangement, energy storage management, and sustainable transport systems, the multilevel converter topologies are attractive solutions to increase input voltage management, improve output waveform quality and reduce harmonic content. The Wide Bandgap (WBG) switching devices, as GaN transistors, are an important development challenges in recent years to improve efficiency with a reduction in the application dimensions.
The thesis work treated about the design, with electrical and thermal simulations, of three level flying capacitor inverter for photovoltaic application for connections to the American electricity grid. Will be done evaluations of power losses, thermal analysis, ripple analysis and electrical schematics drawing.

Acknowledgements

Usando un percorso guidato da Baden Powell cercherò di ringraziare chi mi è stato vicino durante questo percorso.
“Quando la strada non c’è, inventala!”
Voglio ringraziare i miei relatori che mi hanno saputo accompagnare al meglio in questo percorso di tesi, tra salite e discese, aiutandomi ad affrontarlo al meglio.
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“Sforzati sempre di vedere ciò che splende dietro le nuvole più nere...”
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“Il vero modo di essere felici è quello di procurare la felicità agli altri”
Ringrazio la mia famiglia: mamma, papà, le mie sorelle e i miei nonni per avermi sostenuto sempre. La vicinanza della famiglia è fondamentale per riuscire a camminare lungo il percorso tortuoso della vita. Grazie per aver condiviso le mie scelte, avermi accompagnato e sostenuto.
"Sorridono e cantano anche nelle difficoltà"
Grazie ai miei amici. Non c’è persona che non abbia bisogno di aiuto per affrontare un sentiero nuovo. E nel momento della stanchezza, della sete, della lontanza ci siete stati ed è per questo che vi ringrazio. La strada è ancora lunga e per fortuna so di avervi con me per percorrerla in spensieratezza.
“...guardate lontano, e anche quando credete di star guardando lontano, guardate ancora più lontano!”.

A Giorgia, la mia famiglia e i miei nonni
Pippo e Giovanna.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

Nowadays, energy conversion plays a significant role in sustainable growth. Efficient energy conversion systems are based on power electronic converters that are switching circuital structures. In renewable energy conversion, smart grid arrangement, energy storage management, and sustainable transport systems, the multilevel converter topologies are attractive solutions to increase input voltage, improve output waveform quality and reduce harmonic content. The target of increasing energy efficiency and reliability while reducing the overall size of the developed solutions is paramount in modern power electronics applications for energy conversion, both from renewable and traditional sources. Together with advanced topologies such as multilevel ones, it is necessary to select latest generation power electronic devices to obtain ever more efficient and compact conversion systems.

Wide bandgap (WBG) switching devices for converter applications have emerged to address these sustainable development challenges in recent years. Among the WBG devices currently on the market, high electron mobility gallium nitride (GaN) transistors (HEMTs) offer significant advantages and prospective over existing silicon-based alternatives, such as super-junction transistors (MOSFETs) or IGBTs and in several high-frequency applications also respect to other well know WBG devices such as Silicon Carbide (SiC) MOSFETs.

This thesis is developed at one of the leading international companies designing and developing GaN FET devices, the Efficient Power Conversion Corporation (EPC). The thesis work activity was conducted closely with the EPC Centre of Excellence on motor control applications with GaN FET devices in Volpiano.

The thesis work dealt with the study and design of a three-level flying capacitor inverter for photovoltaic applications. The inverter is thought of as part of a system which will include a dc/dc converter between the solar panel and the inverter bus which will be the subject of future studies. The application is also sized to be connected to the American grid and therefore with an output voltage of $110V_{RMS}$ and a grid frequency of $60Hz$. The complete application system block scheme is depicted in Fig.1.1. The thesis work is composed by the following points:

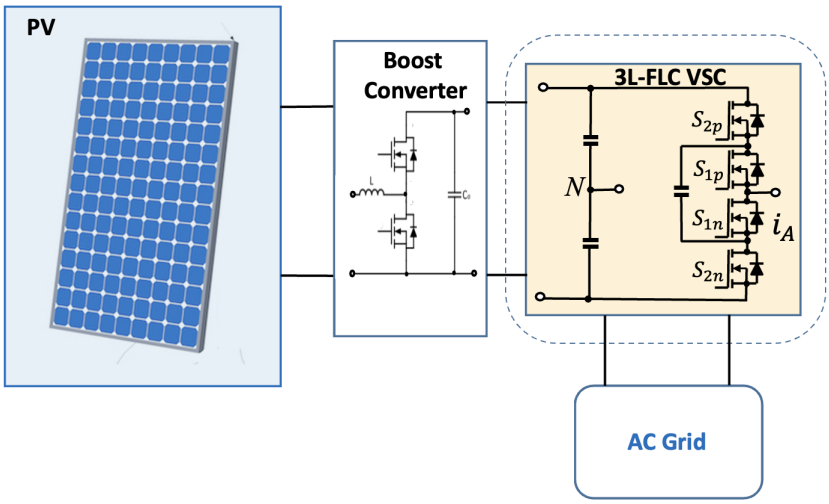


Figure 1.1: Overall application system block scheme.

- Study of GaN devices. The characteristics of GaN technology and especially of GaN FETs have been described. Furthermore, the electrical characteristics of GaN FETs have been analysed in particular the drain-source voltage behaviour, the On-Resistance ($R_{DS(on)}$) of devices, the threshold GaN FETs voltage and the GaN transistors in terms of capacitance and charge are explored. The mean methods to drive a GaN have been investigated;

- Analysis of multilevel converter topologies. The state of art of the topologies for multilevel converters have been explored by analysing the advantages and disadvantages of each topology. Furthermore, a comparison was made among the several topologies considered to obtain the best compromise with respect to the application of three-level inverters and the selected EPC GaN FET devices;

- Design and simulation of the inverter. Simulations were made using LT-Spice and PLECS environments to define the electrical and thermal behaviour of the inverter. The power losses of the inverter deriving from the conduction of the switches and from the commutation of them have been calculated. A thermal analysis and a study of the system efficiency were achieved to define the maximum inverter output parameters and the most appropriate configuration. Analysis of ripple across the dc-link, flying capacitors and phase inductor have been done;

- Sizing and drawing of the electrical schematic. Components were sized and selected from among the existing ones to be included in a future implementation of the inverter. Furthermore, the electrical schematic was drawn defining parts such as power supplies, connectors, measurement circuits to have as complete as possible design to lead to a future realization of a layout.

Chapter 2

GaN Transistor

2.1 Introduction

Gallium nitride (GaN) is a very hard, mechanically stable wide bandgap semiconductor. GaN devices presents higher breakdown strength, faster switching speed, higher thermal conductivity and lower on-resistance with respect to silicon-based devices. The crystalline structure of the Gallium Nitride material features a hexagonal shape named "wurtzite" (Fig. 2.1).This crystal structure also gives GaN piezoelectric properties that lead to its ability to achieve very high conductivity compared with other semiconductor materials.
GaN power devices are high electron-mobility transistors (HEMTs) belonging to the wide-bandgap materials (WBG). The HEMTS transistor use a two-dimensional electron gas named (2DEG) which is generated by the interaction between two crystalline physical materials with diverse atomic spacing and band gaps in the junction realized. The effect of the polarization makes the 2DEG phenomena in the heterojunction (AlGaN/GaN). This is the cause of the electrons' high mobility outcome.
In the Fig.2.2, is reported a comparison between significant material properties of Silicon (SI), Silicon-Carbide and GaN devices. In the chart is reported that the characteristics of WBG devices are better than Silicon devices. GaN and Silicon-Carbide transistor have different behaviours, indeed Sic devices present better thermal conductivity with respect to GaN devises instead an higher electron mobility is a GaN peculiarity due to HEMT characteristics. GaN devices electron mobility is high. It is typically around $2000 cm^2/Vs$. The electron mobility value in GaN-based devices is almost 100 times higher than Silicon Carbide MOSFETs. This advantage characteristic is reflected in the reduction of the low ON resistance values. This topic will deeper discuss in the next sections. As consequence is possible to achieve devices with smaller areas compared with Si and SiC devices.

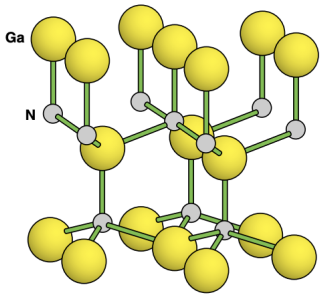


Figure 2.1: Wurtzite GaN crystal space disposal.[1]

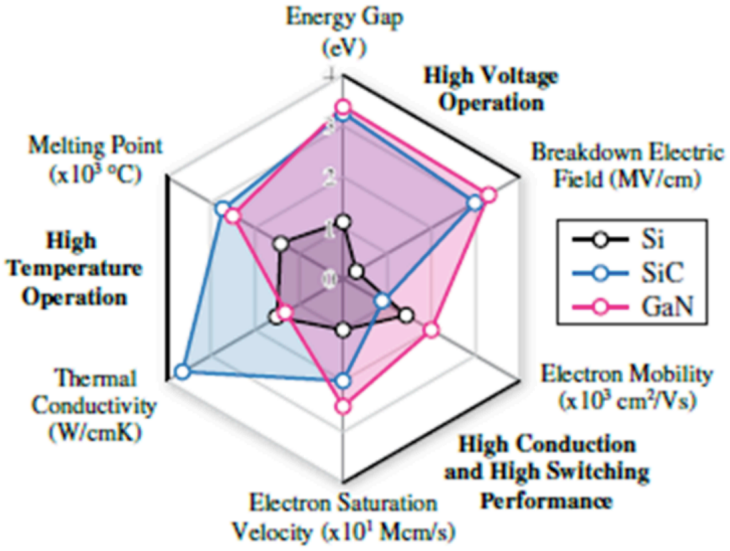


Figure 2.2: Radar chart of the significant technological characteristics of Si, 4H-SiC, and GaN transistors at ambient temperature (25 °C).[2]

2.2 GaN Power Devices Arrangement

The GaN-based power devices are lateral physical structure as field effect transistor (FET), showing a current conduction channel between the Drain and Source areas. A gate voltage value controls the conduction current amplitude. As the FET devices, the depletion mode is the basic GaN structure, featuring a normally on switch. A basic structure of a depletion GaN FET is depicted in Fig.2.3,the gate electrode is obtained through a Schottky contact. The application of a negative voltage to the gate with respect to the

source, leading the device to the OFF state. In the Fig.2.3a the 2DEG created in the heterojunction (AlGaN/GaN) above described is highlighted. Starting of this basic structure the designer developed an off structures. A normally off GaN FET is obtained through an enhanced structure (e-mode), as depicted in the structure of Fig.2.3b no-conduction channel is observable. The GaN gate layer, positively charged (p-type), attains the e-mode structure of the GaN transistor. The gate layer is grown-up on the AlGaN barrier. The p-type layer does not allow the two-dimensional electron gas at VGS under a device threshold voltage, obtaining a normally off device. The 2DEG is fully re-established by a positive voltage between the gate and the source (appropriately greater than the threshold voltage). In reverse conduction, an equivalent diode action appears when the gate voltage is under the device threshold voltage. The voltage drop in the GaN equivalent diode is higher than a typical body diode of a Si MOSFET. No reverse recovery charge, Qrr, is shown in the GaN equivalent diode because no minority carriers are involved in the conduction, as described in the next sections.

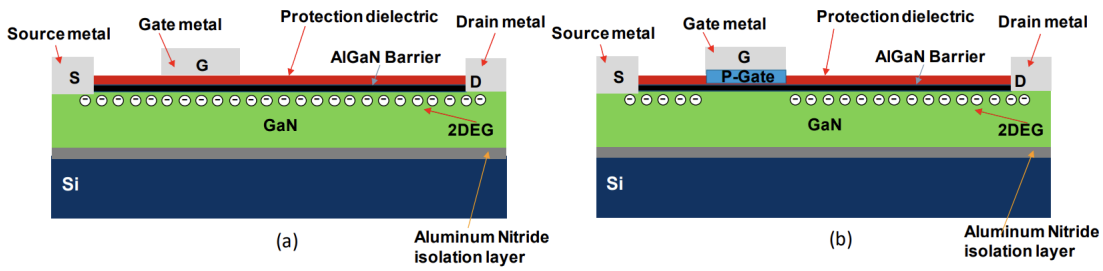


Figure 2.3: (a) simplified structure of a d-mode GaN FET (normally on). (b) simplified structure of a e-mode normally off GaN FET. [2]

The cascode layout is a further GaN-based transistor together with a Si MOSFET (Fig.2.4b). The cascode structure is arranged adding a low voltage (LV) MOSFET in series with the d-mode GaN source, achieving a normally off switch. The cascode solution combines the structural simplicity of d-mode GaN technology and its HEMT characteristics with the simplified gate-driving procedure of the Si MOSFET. The GaN FET Gate is linked to the Source of the MOSFET to keep the GaN device in the on state, while the MOSFET is implemented for the commutations. The reverse cascode operation appears when LV Si MOSFET is turned off. Consequently, the GaN switch is also turned off. In this condition, a reverse voltage appears to the GaN switch and a current flows in the body diode of the MOSFET and into the channel of the d-mode GaN FET with a reduced voltage drop. The GaN FET is a naturally bidirectional device however a lower-off-state reverse voltage arise (i.e., <1V). This low voltage drop can be considered during dead times in half-bridge operations. The cascode configuration may be used in low-voltage applications (<200 V); nevertheless, in high-voltage applications (from 650 V up to 1200), it features a viable usage for higher-current switches.

A direct-drive GaN power transistor is a modified arrangement of the cascode configuration (Fig.2.4c). The d-mode GaN gate terminal is not connected, and four terminals appear. In this device layout arrangement, the Si MOSFET is implemented as a protection switch to avoid shoot through (it furnish also an enable gate signal after the converter start-up). A negative unipolar voltage directly drives the d-mode GaN FET to switch-off. The main advantage is the independent driving of the d-mode GaN FET, using its switching properties and preventing the uncontrolled switching feasible in the conventional cascode layout. Compared to the previous cascode solution, a drawback is the increase in stray inductances. Furthermore, the two gates necessary increase the device package pins.
The EPC GaN which will be used in this thesis work are e-mode GaN from EPC. All structures discussed before are represented in the Fig.2.4.

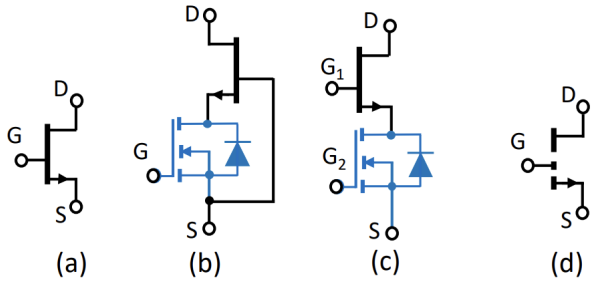


Figure 2.4: a) d-mode GaN FET (normally on) (b) Normally off cascode layout with d-mode GaN FET. (c) Direct-drive cascode with d-mode GaN. (d) e-mode GaN FET (Normally off). [2]

2.3 GaN Electrical Characteristics

In this section are discussed the basic electrical characteristics of GaN devices as:

- Drain-Source Voltage;
- ON-Resistance;
- Threshold Voltage;
- Capacitance;
- Reverse conduction.

2.3.1 Drain-Source Voltage

The rated breakdown voltage (BV_{DSS}) between the source and drain terminals of a GaN transistor is determined by several factors as:

1. The fundamental breakdown electric field (E_{Crit}) of GaN;
2. The specific design of the device;
3. The specifics of the epitaxial layers;
4. Internal insulating layers in the device structure above the gate, source and drain electrodes;
5. The underlying substrate material properties.

A semiconductor transistor will break down and conduct current (I_{DSS}) when the electrical field of any material which compose it is exceeded and may destroy itself in the process. When a transistor of any kind is in the blocking state, before breakdown voltage, the "leakage current" I_{DSS} will flow between terminals. There are three components of leakage current in a transistor and the sum of these components is equal to I_{DSS}. The leakage current components are represented in Fig.2.5 [1] that describes measured current in an enhancement-mode transistor with a breakdown voltage above 700V. The example in Fig.2.5 introduces a GaN with Silicon substrate material and is connected to source potential. The current of the example in the Fig.2.5 has been normalized to a 1mm-wide gate structure. The I_{DSS} become a significant factor for power losses. The drain-to-source

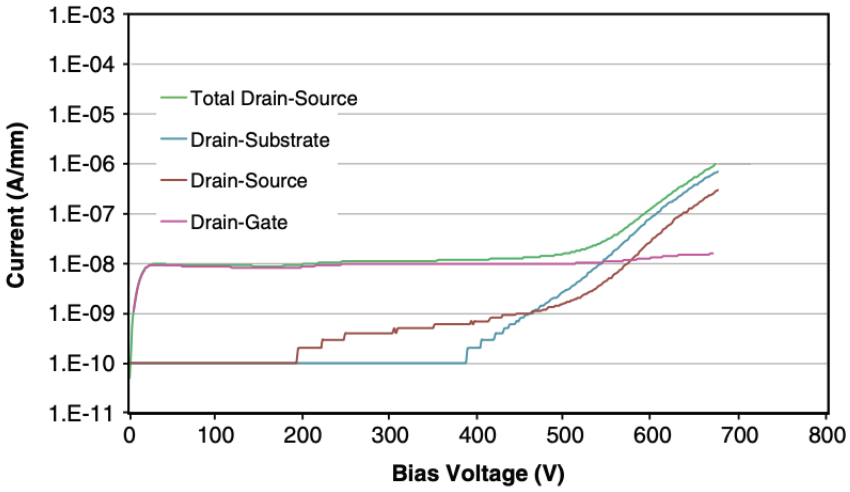


Figure 2.5: Leakage current components: drain-gate leakage, drain-source leakage, drain substrate leakage, and total I_{DSS}. [1]

leakage current can also vary with temperature. Fig.2.6 shows a family of curves, from an available enhancement-mode transistor (EPC2045) with one-meter gate width, that represent the leakage current measured at various temperature.

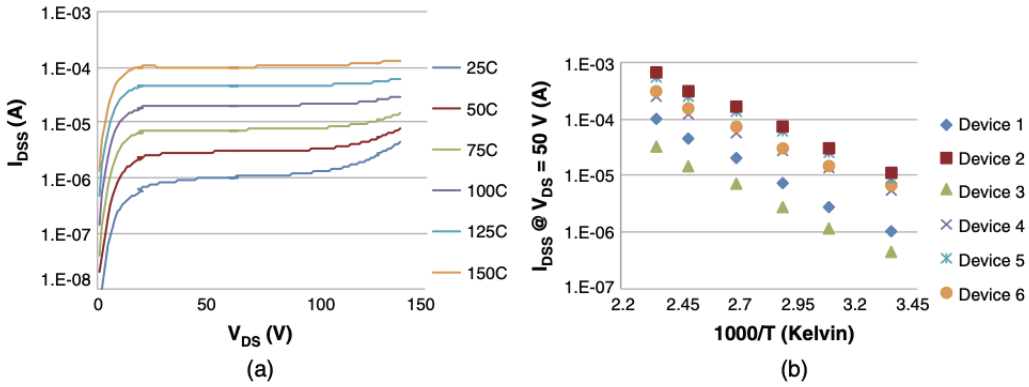


Figure 2.6: EPC2045:(a)I_{DSS} as a function of V_{DS} varying temperature;(b)I_{DSS} measured at $V_{DS} = 50V$ of 6 different devices of the same part type varying temperature. [1]

2.3.2 On-Resistance ($R_{DS(on)}$)

The on-resistance of a transistor is the sum of all the resistance elements that make up the device. Fig.2.7 shows the foremost elements that contribute to the RDS(on) of the device. The source and drain metals must connect to the 2DEG zone by the AlGaN barrier. These components of resistance are named contact resistance (R_C). Electrons then flow in the 2DEG with a resistance R_{2DEG}. This resistance is determined by the mobility of the electrons (μ_{2DEG}), the number of electrons created by the 2DEG (N_{2DEG}), the distance the electrons have to travel (L_{2DEG}), the width of the 2DEG (W_{2DEG}), and the universal charge constant, q ($1.6 * 10^{-19}C$). The R_{2DEG} can be described by (2.1).

$$R_{2DEG} = L_{2DEG}/(q \cdot \mu_{2DEG} \cdot W_{2DEG}N_{2DEG}) \tag{2.1}$$

The number of electrons in the 2DEG will depend on the amount of strain induced by the AlGaN barrier. However, under the gate electrode, 2DEG could have a lower concentration than in the region between the gate and drain electrodes. The electron concentration depends on the gate structure related on the particular process used, and the heterostructure arranged. The voltage applied to the gate influences electron concentration also. For example, fully enhanced gate will show a higher electron concentration compared with a partially enhanced gate. An approximation of the R_{HEMT} represented in Fig.2.7 is explained in the following formula (Eq.2.2[1]):

$$R_{HEMT} = 2 \cdot R_C + R_{2DEG} + R_{2DEG(Gate)} \tag{2.2}$$

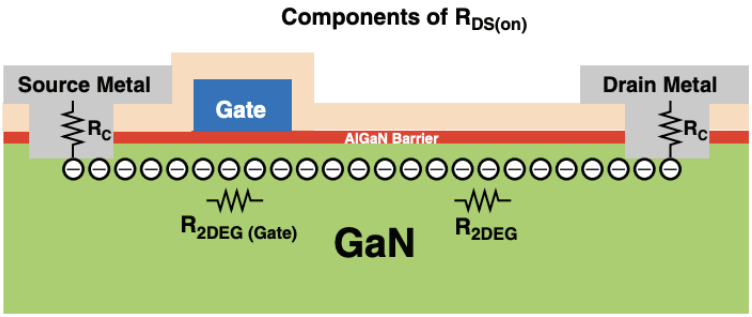


Figure 2.7: The GaN HEMT cross section featuring the foremost components of $R_{DS(on)}$ [1]

Additional parasitic resistance ($R_{parasitic}$) can come in the form of metal resistance from the multiple metal buses that conduct the current from the individual source and drain electrodes to the terminals of the transistor. In a power conversion circuit, the conduction losses of the transistor are quite significant and therefore the device is typically used either fully turned on, or fully turned off. For this reason, is important to define a key parameter for specifying any power transistor that is the on-resistance, $R_{DS(on)}$, defined in the (2.3) [1]:

$$R_{DS(on)} = R_{HEMT(FullyEnhanced)} + R_{parasitic} \tag{2.3}$$

The $R_{DS(on)}$ is function also the gate-to-source voltage as shown in Fig.2.8 . In the graphs in Fig.2.8 is possible to notice that the resistance of 2DEG rapidly decreases until it is fully enhanced at about $V_{GS} = 4.5V$. The Fig.2.8a represent the $R_{DS(on)}$ as a function of several currents while the Fig.2.8b as a function of temperature.

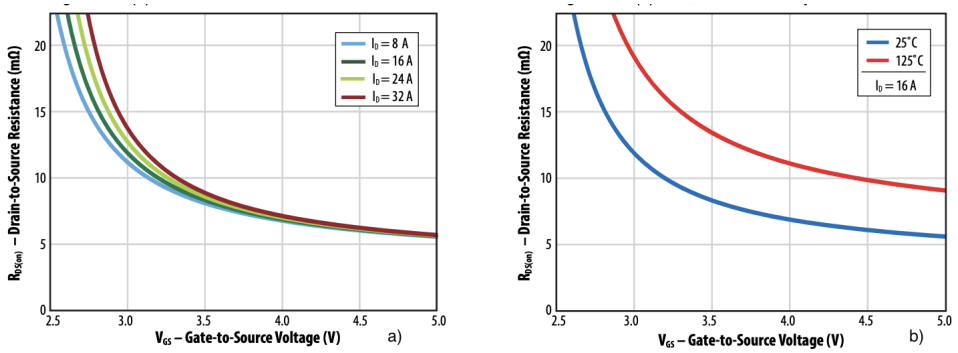


Figure 2.8: $R_{DS(on)}$ of an enhancement-mode GaN transistor (EPC2045) as a function of several drain current (a) and temperature (b).[3]

2.3.3 Threshold Voltage

For a power device, the threshold voltage is the voltage required to be applied to the gate-to-source to begin conducting current in the device. In other words, the threshold voltage defines the voltage below which the device is off. An enhancement-mode or cascode device has a positive threshold voltage, and a depletion-mode device has a negative threshold voltage. For a GaN power device, the threshold voltage is when the 2DEG underneath the gate is fully depleted by the voltage applied in the gate electrode [1]. This condition appears when the voltage on the gate equilibrates the voltage produced by the piezoelectric strain in the AlGaN/GaN barrier. Because the strain stress in the AlGaN barrier is relatively constant with temperature, as are the voltages generated by the internal metallurgy, the threshold voltage in a GaN HEMT is relatively constant with temperature as shown in Fig.2.9. In the Fig.2.10 is possible to notice the difference of threshold voltage decrease due the temperature with 100V Infineon BSC060N10NS3 Si MOSFET. The voltage threshold rapidly decreases with respect to GaN in Fig.2.9 with increasing temperature.

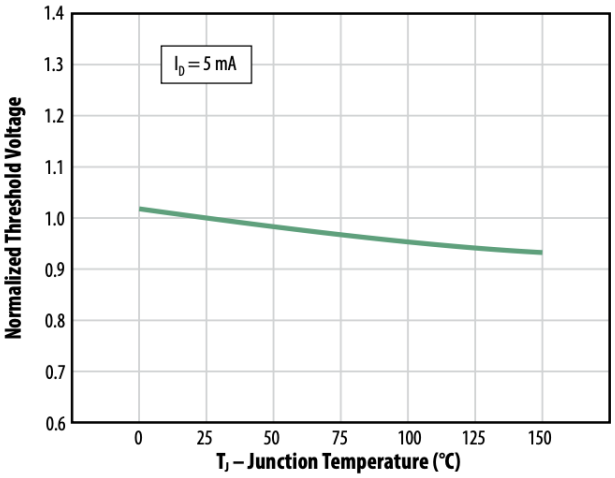


Figure 2.9: Normalized Threshold Voltage vs. Temperature (EPC2045).[3]

2.3.4 Capacitance and Charge

Capacitance is a significant electric inner component that causes the energy to be lost in the GaN transistor during a transition from the on-state to the off-state or vice versa. The capacitance (C) determines the quantity of charge (Q) that needs to be furnished to the different device terminals to change the voltage across those terminals (Q = C*V). The faster this charge is supplied, the faster the device will change voltage. There are three main elements of capacitance related to a FET:

1. gate-to-source capacitance (CGS);

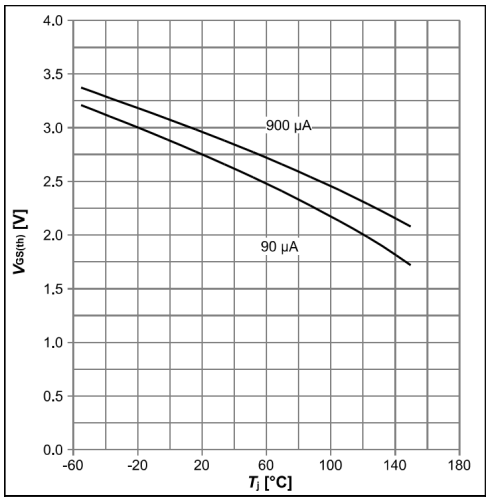


Figure 2.10: Gate threshold voltage vs. temperature (BSC060N10NS3 Infineon).[4]

2. gate-to-drain capacitance (C_{GD});
3. drain-to-source capacitance (C_{DS}).

The Fig.2.11 illustrates the physical origin of each of these capacitances. To design the

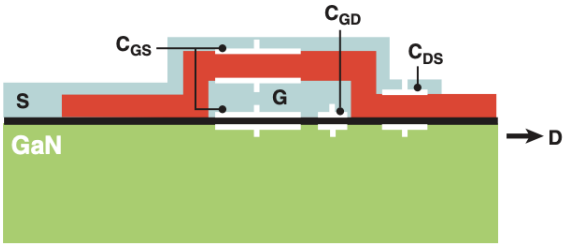


Figure 2.11: Schematic of GaN transistor capacitive sources.[1]

capacitances of the transistor usually is taken into account the equivalent input terminals capacitance ($C_{ISS} = C_{GD} + C_{GS}$), or output terminals capacitance ($C_{OSS} = C_{GD} + C_{DS}$). These capacitances are a function of the voltage applied to various terminals. Fig.2.12 shows how the values change for an enhancement-mode HEMT, as the voltage from drain-to-source increases. The reason for the drop in capacitance as VDS increases is that the free electrons in the 2DEG of GaN are depleted [1]. For example, as shown in Fig.2.12, the initial step down in C_{OSS} is caused by the depletion of the 2DEG near the surface. The result of integrating the capacitance between two terminals across the range of voltage applied to the same terminals is the amount of charge (Q) that is stored in the capacitor. Since current-integrated-over-time equals charge, it is often very convenient to look at the amount of charge necessary to change the voltage across various terminals

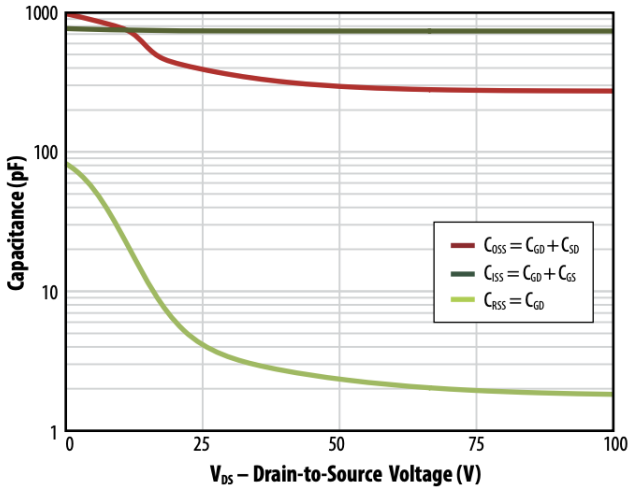


Figure 2.12: EPC2045 capacitance vs. drain-to-source voltage[3]

in the GaN HEMT. Fig.2.13 shows the amount of gate charge, Q_G, that must be supplied to increase the voltage from gate-to-source to the desired voltage. Q_G is the integrated value of C_{ISS} from the starting voltage on the gate to the ending voltage. In the Fig.2.13 it can be seen that about 5 nC is needed to bring the gate voltage from 0V yo 5 V, which will ensure the device is fully turned on. If the gate drive is capable of supplying 1 A of current, it will take about 5 ns to achieve this voltage. Is also important to notice that the C_{GS} and C_{ISS} are typically more variable with respect to the gate voltage than the drain voltage indeed the Fig2.12 is referred to C_{ISS} with V_{GS} = 0V.The Q_{GD} and Q_{GS} are also specified separately because they impact the voltage and current switching transition speeds, respectively. Also, the ratio of these two values, called the Miller ratio (Q_{GD}/Q_{GS}), is often an important metric to determine the point at which a device might turn on due to a voltage transient applied across the drain and source. An example is reported in Fig.2.14 where the Miller ratio is a function of drain voltage. A Miller ratio of less than one will guarantee dv/dt immunity as in the case in Fig. where is represented a comparison between GaN FETs and Mosfets.

2.3.5 Reverse Conduction

V_{SD} is the voltage drop across the device when voltage is applied from source-to-drain that is the reverse direction from the normal forward FET conduction. In a Si MOSFET, there is a p-n junction that creates a diode from the body (p) in the structure to the drain (n) of the device. It is, therefore, called a body-drain diode. However, in an enhancement-mode GaN HEMT transistors do not have a p-n diode, but they do conduct in a way similar to a diode in the reverse direction. Fig.2.15 shows how this “body diode” forward voltage drop varies with source-drain current. The body diode is formed by turning on the 2DEG in the reverse direction using the drain-gate voltage to enhance the channel, if

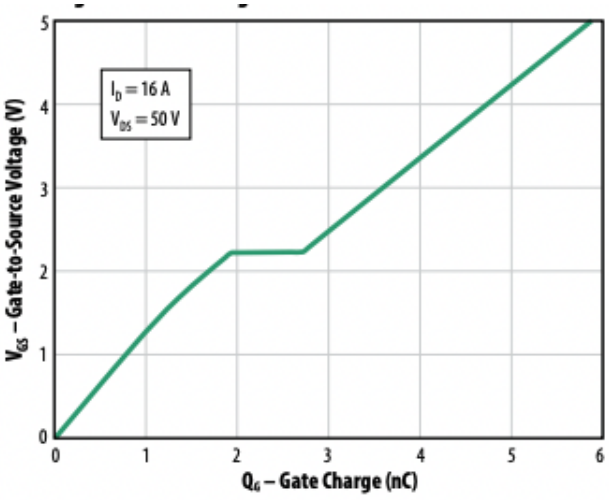


Figure 2.13: EPC2045 capacitance vs. gate-to-source voltage[3]

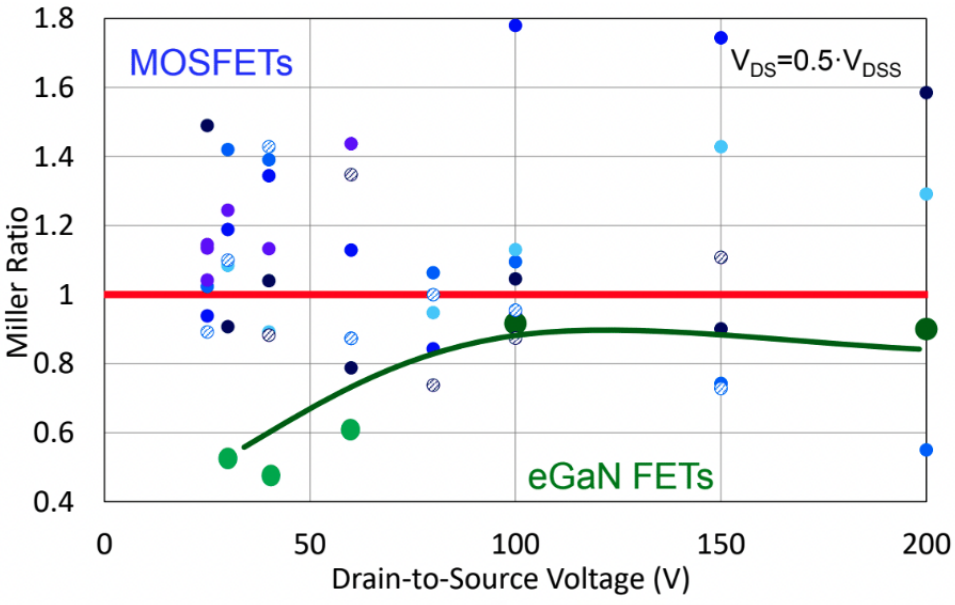


Figure 2.14: Comparison between GaN FETs and Mosfets Miller ratio.

the gate voltage is lowered below 0 V, the forward drop will increase proportionately. For example, if the gate drive of a circuit turns off the GaN HEMT by applying a negative 1 V to the gate, the V_{SD} at 0.5 A will be 2.8 V instead of 1.8 V with 0 V_{GS}. Because the reverse conduction in a GaN transistor is due to the turning on of the 2DEG, the forward voltage drop will change with temperature in much the same way as the $R_{DS(on)}$ changes with temperature in forward conduction. In an Si MOSFET, the reverse conduction is due to a p-n junction diode. Contrary to a GaN HEMT, the diode forward drop goes down

with temperature in the Si MOSFET [1].

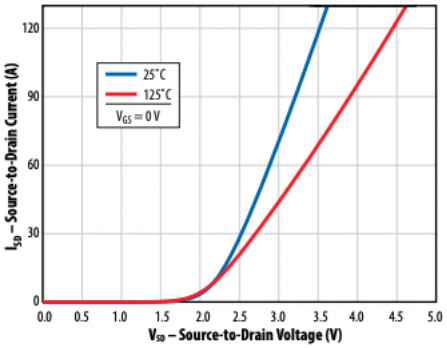


Figure 2.15: EPC2045 V_{SD} drop vs. source-drain current and temperature. [3]

2.4 Driving GaN

The overall charge accumulating at the gate terminal is lower than a MOSFET with similar output current and voltage characteristics. This feature results in faster switching and a significant reduction in gate drive losses. The gate driver circuit is a crucial system to optimize the advantageous switching characteristics of these HEMT devices. To be compatible with e-mode GaN FETs, the gate driver must have a suitable Under voltage lockout (UVLO) control for 5 V drive, low pull-up and pull-down resistances, small footprint, and isolation with sufficient common-mode transient immunity (CMTI) to withstand the high dv/dt. Other beneficial features of some e-mode GaN-compatible drivers include integrated voltage regulators, bootstrap management, and very narrow pulse width capability. In case of half-bridge legs, low-side gate drivers can be combined with high-voltage signal isolators with high CMTI for high-voltage designs without a single IC solution. The gate-source voltage to turn-on the e-mode GaN FET depending on the full enhancement of the device channel. It can be achieved by applying 4 V or greater. The recommended value of the operating turn-on gate voltage is 5 V with a resistance while the absolute maximum gate-to-source voltage is 6 V. The curves depicted in Fig.2.16 show the dependences of the gate driver resistance and the Gate voltage to obtain the output current. The gate voltage of 5 V allows to obtain the enough gain to reach the device higher current with the minus gate resistance considered and the high dynamic characteristics. The conductive channel is interrupted by a voltage under the threshold value (between 0.7 V-2.5 V with typical around 1.4 V – for EPC2010). Generally, a voltage $V_{GS} = 0V$ is enough for turn-off the device, but the high dv/dt impact on the inner capacitors would provokes a shoot through phenomenon especially in half-bridge topology. From which the suggested gate voltage for a safe turn-off is -2 V

to prevent any non-desired turn-on events that could appear due to VDS voltage changes.

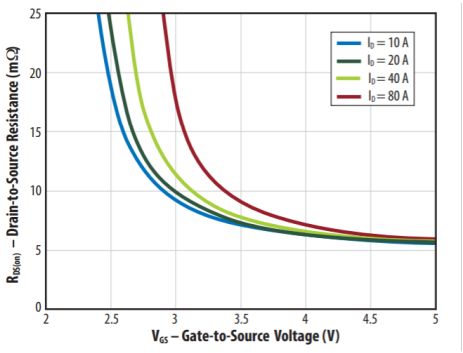


Figure 2.16: R_{DSon} vs V_{GS} for various current to obtain the optimal GaN drive voltage and resistance for EPC2001.

2.4.1 dv/dt Immunity

The inner capacitors are involved in the switching characteristics and the dv/dt impact when the GaN is in off-state (e.g. Bridge Configuration) lead an unwanted voltage in the gate path that can be turn-on the device. A high drain positive voltage slew rate (dv/dt) of an off-state device can occur in both hard-switching and soft-switching applications and is characterized by a rapid recharge of device capacitances, as shown in Fig.2.17. In Fig.2.17a a switching leg with GaN FET and inner capacitances and gate resistance are shown with the current path due to the dv/dt effect. The dead time t_d, on and t_d, off is also considered to avoid cross conduction as shown in Fig.2.17b. The dv/dt effect a spurious gate voltage can be appear and its peak value must have maintained under the threshold voltage (see Fig.2.17b) During this dv/dt event, the drain source capacitance (C_{DS}) is also charged. At the same time, the gate-drain capacitors are also charged (C_{GD}) and gate-source (C_{GS}) in series. If not addressed, the charging current through the C_{GD} capacitor will flow through and charge C_{GS} beyond V_{TH} and turn on the device. This event, sometimes called Miller turn-on and well known to MOSFET users, can be very dissipative. To determine the dv/dt susceptibility of a power device, it is necessary to evaluate a Miller charge ratio (Q_{GD}/Q_{GS1}), as a function of the drain-to-source voltage. A lower Miller ratio will ensure theoretical dv/dt immunity.

2.4.2 di/dt Immunity

An increasing current through an off-state device, as shown in Fig.2.18a, will induce a step voltage across the common source inductance (CSI). This positive voltage step will generate an opposite voltage across C_{GS}. Increasing current causes the gate voltage

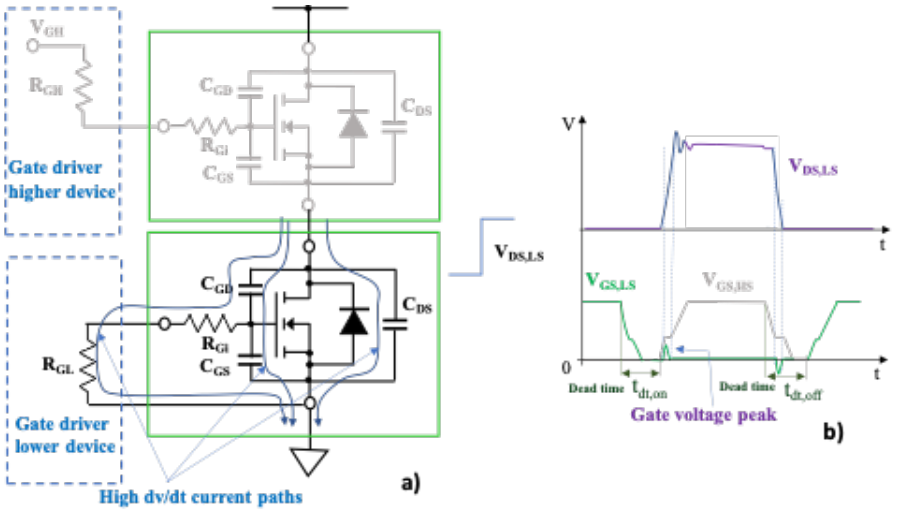


Figure 2.17: a) Bridge leg schematic with the device capacitors model and the dv/dt current paths during the operative condition of higher GaN turn-on and lower GaN in off-state. b) qualitative waveforms of node voltage $V_{DS,LS}$ and gate voltages of both lower and higher switching devices with shoot-through phenomena highlighted.

to be driven to a negative value. With insufficient off-state gate LCR resonant tank damping, this initial negative voltage step across the gate could induce a positive spike and cause an unintentional firing and shoot-through, as shown in Fig.2.18b. It is possible to avoid this di/dt firing type by damping the gate quench loop sufficiently, although some undershoot may be preferred, as described in the dV/dT immunity case above. However, increasing gate power loop damping through an increase in gate pulldown resistance would negatively impact dv/dt immunity. Therefore, adjusting the gate resistance alone for marginal Miller ratio devices may not be sufficient to prevent di/dt and dv/dt firing. The CSI influences Gate and Drain-Source voltage (Fig.2.18b) ringing. Limiting stray inductance (CSI) through improved packaging and device layout is a viable solution. This is accomplished by separating the gate and power loops to as close to the GaN device as possible and minimizing the internal source inductance of the GaN device, optimizing the package layout; This procedure is valid for both gate and power loop.

2.4.3 Driver Circuit Requirements

As discussed above, the driver circuit must not only provide the necessary voltages and currents needed by the gate to charge and discharge the internal capacitances. Still, it must also allow safe switching while avoiding dangerous ringing as much as possible. The integrated driver circuits solution reduces the parasitic inductances by placing the gate driver as close as possible to the GaN FET power transistor [5]. The driver circuit schematic for an inverter leg is reported in Fig.2.19a. The GaN FET model with the

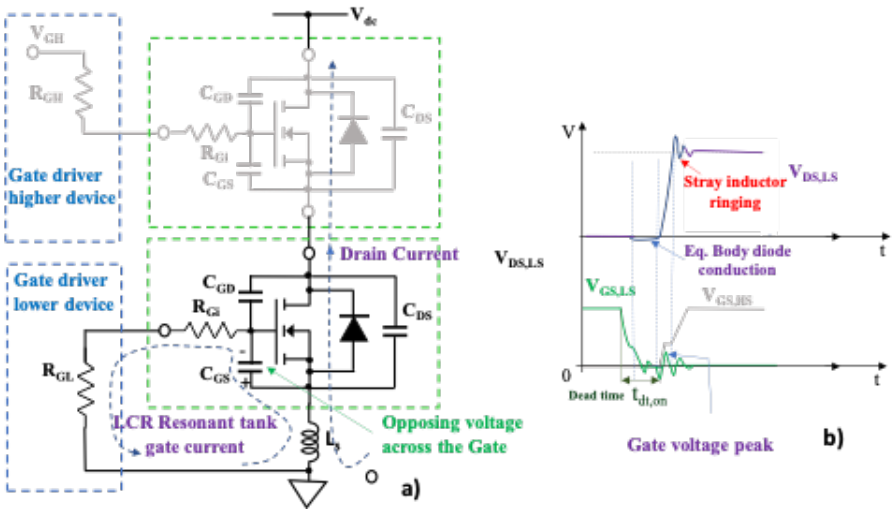


Figure 2.18: Impact of a positive di/dt of an off-state device with common-source inductance. b) Qualitative waveforms of node voltage $V_{DS,LS}$ and gate voltages of both lower and higher switching devices with ringing due to the CSI stray inductance.

parasitic capacitors and the stray inductor L_{SS} in the source path of L_S are considered. With the gate resistance is feasible, (similar to a MOSFET device), to regulate di/dt and the dv/dt. In many gate-driving circuit solutions, the on and off paths are done with separate gate resistances. A bootstrap circuit is used in the integrated solutions to power the high-side gate driver. The CB capacitance (from Fig.2.19a) must provide the gate charge required. CB can be found by:

$$C_B \geq \frac{Q_G}{V_{dd} - V_{FB} - R_B \cdot I_B - V_{GG,off}} \tag{2.4}$$

where $V_{GG,off}$ is the minimum voltage allowed across the capacitor C_B during the off-state of the high-side MOSFET, while V_{FB} is the forward diode voltage of the bootstrap circuit. The PWM command signal processed by the logic circuit is sent through a level shift circuit to the high-side switch depicted in Fig.2.19b. The level-shifter MOSFET must maintain the V_{DC} voltage but the current request is very low, from which this MOSFET features low area in IC implementation. The bootstrap solution reported in Fig.2.19b is an alternative solution compared with the arrangement of Fig.2.19b. In this case a high-voltage diode (breakdown voltage over the V_{DC} considered) is connected to the high-side drain. The power losses of the driver circuit P_{Dr} become noteworthy as the switching frequency increases. The losses depend on the resistor network R_{GG},on at turn-on, the $R_{GG,off}$ at turn off and, the to the gate charge by:

$$P_{Dr} = \Delta V_{GS} \cdot Q_G \cdot f_{sw} \cdot \left(\frac{R_{GG,on}}{R_{GG,on} + R_G + R_{Gi}} + \frac{R_{GG,off}}{R_{GG,off} + R_G + R_{Gi}}\right) \tag{2.5}$$

In Eq.2.5, the internal gate resistance R_{Gi} of the GaN FET device is also considered [1]. The gate current peak I_G, peak at the turn-on pulse (t_{on}) is related to the input capacitances as in Eq.2.6.

$$I_{G,peak} = \frac{(C_{GS} + C_{GD}) \cdot V_{GS}}{t_{on}} \tag{2.6}$$

Furthermore, the driving circuit may feature additional monitoring and protection circuits. As example, for power supply under-voltage and overcurrent, or short-circuit. Short circuit protection acts in a hard switching fault (HSF) or a fault under load (FUL) dangerous conditions [6].

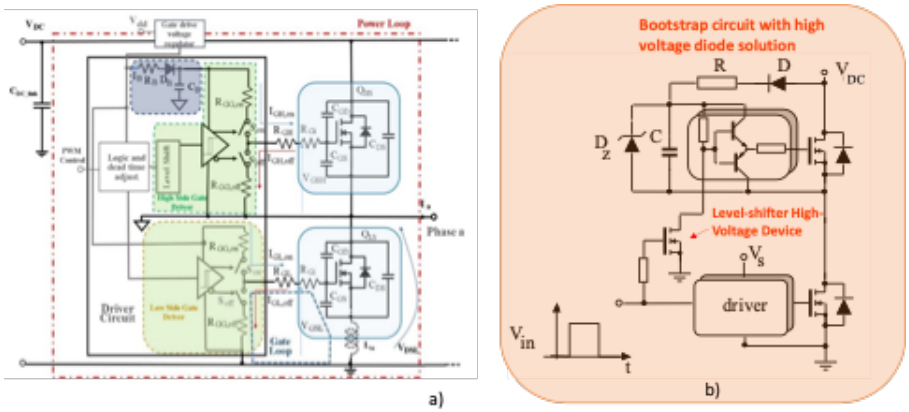


Figure 2.19: a) driver circuit and power stage schematic for a switching leg. b) Level shift circuit principle with an alternative bootstrap circuit solution.

Chapter 3

Multilevel Topologies

3.1 Introduction

The multilevel converters are an evolution of the two-level converter concept. Modular Multilevel Converters (MMCs) are based on an identical basic cell, replicated n-times and interconnected with a few other components, usually diodes and capacitors, until the specific structure of the converter is obtained. The output of the MMC is a stepped waveform voltage, which depends on the converter levels. The switching of the power devices allows the capacitor voltages addition reaching high voltages at the output, while the power switches have to withstand only reduced voltages ([7]). The MMCs are useful for the possibility of splitting the total voltage of the DC-link on several active devices. In this way, they can withstand very high voltages (hundreds of kilovolts) contributing overall to drive loads of extreme power (hundreds of megawatts). Furthermore, in a multilevel converter, the availability of different voltage steps allows to more accurately emulate the trend of a sinusoidal voltage. For this reason, the harmonic level, that can be calculated according to the Fourier analysis, it is naturally more contained in the multilevel reconstruction than the only two square wave levels (obtained in the two-level inverters). This results in a reduced Total Harmonic Distortion (THD). The THD decreases the more the voltage steps are numerous, increasing the power quality. In Fig.3.1 the evolution concept of the multilevel solution is shown [8]. In Fig.3.1a the two-level switching pole is reported with the output voltage waveform, while in Fig.3.1b there is the principle of the three-level switching pole with the improved output waveform quality. Finally, in Fig.3.1c the concept of multilevel switching pole is generalised for n levels. The output voltage of Fig.3.1c is related to 9-levels converter, the output voltage THD, in this case, is even more reduced than in the previous case

In this section will be proposed several topologies of three level converters taking in exam the advantages and disadvantages of all of them. The goal of this section is to analyse the characteristic of following topologies to choose one to be taken into consideration to develop the most suitable multilevel converter for the objective of the thesis work.
The topologies will be discussed in the next sections are:

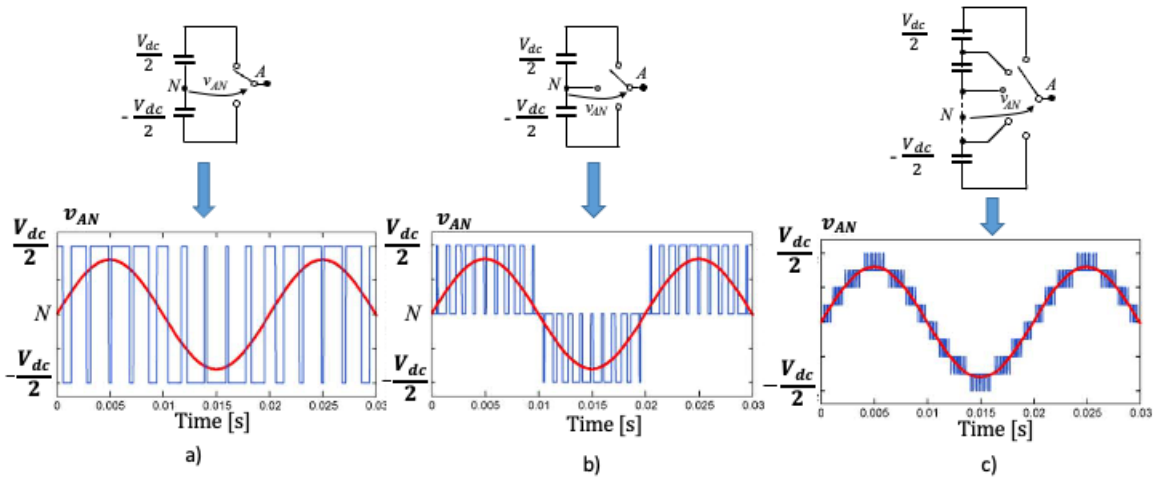


Figure 3.1: Multilevel principle and output waveforms: a) two-level switching pole, b) three-level switching pole, c) n-level switching pole and output waveforms with n=9.[8]

- Diode Clamped Inverter (NPC) Topology;
- T-Type Converter;
- Cascaded H-Bridge inverter;
- Cascaded Half Bridge inverter;
- MMC Converter;
- Heric Converter;
- Flying Capacitor Converter.

3.2 Diode-Clamped Inverter Topology

The Diode-Clamped inverter or Neutral Point Clamped multilevel converter is distinguished by the use of diodes clamping (Fig.3.2), which have the role of blocking the reverse voltage across the dc bus capacity. The neutral point (hence the name of the topology) to which reference is made for voltage, is the central node common of the dc-bus capacitors. Using m to indicate the number of voltage levels desired, to design the converter will need a dc bus consisting of $m-1$ capacitors, $2\cdot(m-1)$ switching devices

and $(m-1)\cdot(m-2)$ clamping diodes. It is very important to properly size the clamping diodes, because they have to withstand different voltage values depending on how many capacitors the dc buses are connected to them.
The NPC converter is simple to control. For example, it needs a PWM modulation with two carriers shifted by 180 degrees in three levels configuration. The NPC topology presents some disadvantages:

- Use of clamping diodes (components to be sized, reverse recovery, etc. . .);
- Unequal use of the switches during the commutations (switches appropriately dimensioning, considering the current which can withstand.;
- The NPC inverter has a large commutation loop which increases the parasitic inductances;

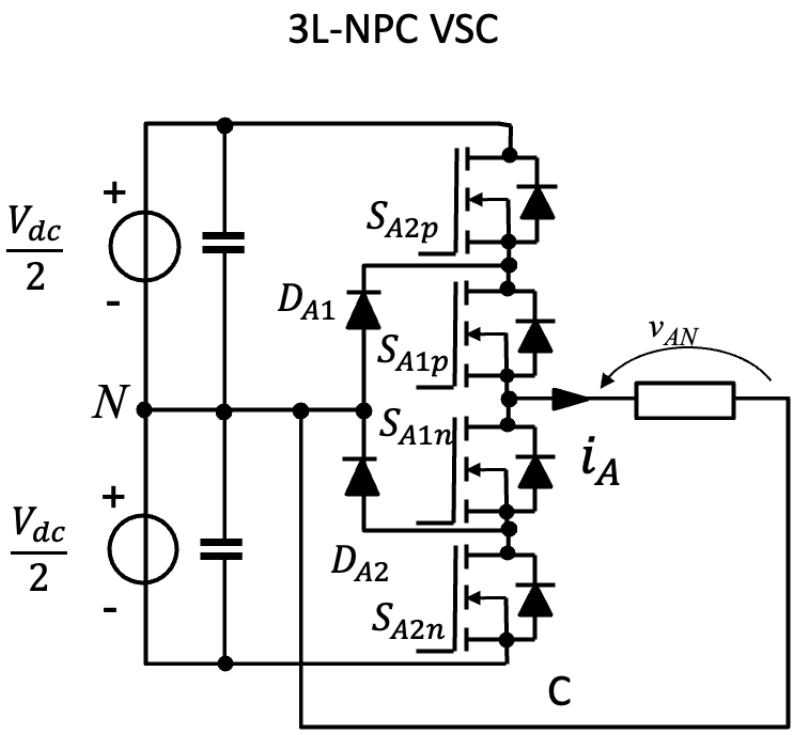


Figure 3.2: NPC three level single phase inverter.

3.3 T-Type Converter

The basic topology of the three level T-Type Converter is depicted in Fig.3.3. The conventional two-level VSC topology is extended with an active, bidirectional switch to the dc-link midpoint. In the case of conventional GaN transistors that cannot block the voltage in both directions, two GaN switches are used in antiparallel (Fig.3.3). For this application is important the sizing of the switches because the S1 and S2 switches must withstand the voltage of dc-bus while the S11 and S22 can be sized with $V_{dc}/2$. This application presents disadvantages discussed below:

- The application will be discussed in this thesis work considering GaN transistor which are not controlled in bidirectional mode, for this reason will need to use two different switch in the neutral node. This has an important role in terms of conduction losses;
- The switches S1 and S2 must withstand the whole dc-bus voltage that could be a problem to find the right GaN transistor;

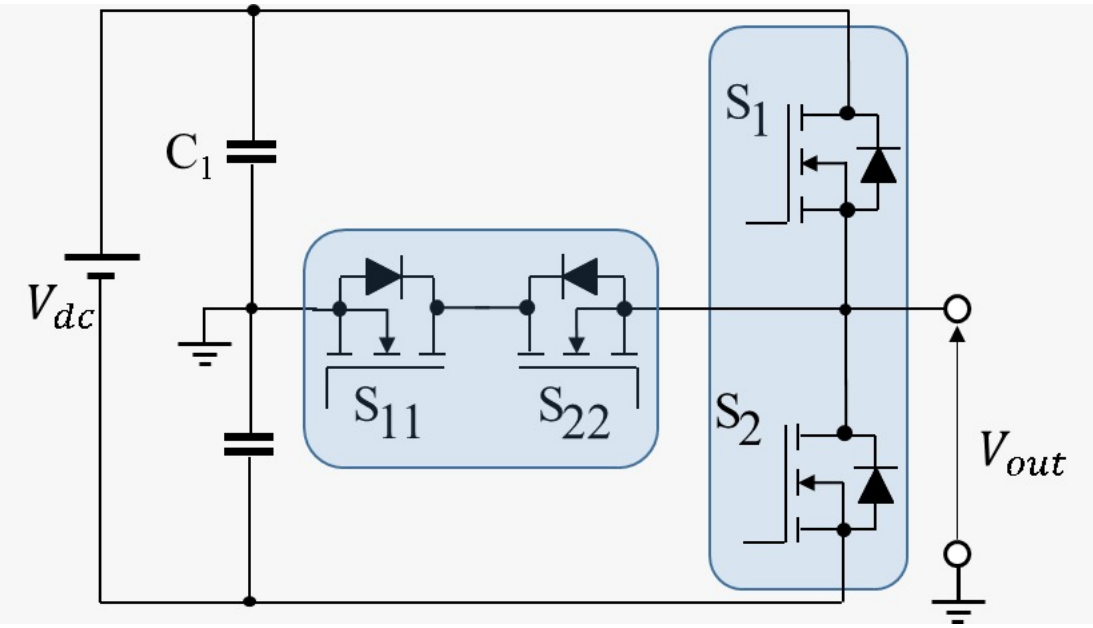


Figure 3.3: 3-L T-Type Converter.

3.4 Cascaded H-Bridge Inverter

The Cascaded H-Bridge inverter is composed by a Full-Bridge inverter cells connected in series to reach the number of levels desired. The single Full-Bridge cell (Fig.3.4) can

obtain three voltage levels: $(+V_{dc},0,-V_{dc})$. To increase voltage levels is possible to connect another Full-Bridge cell in the "0" point. In that case each new cell is equivalent to add two more voltage levels. The power switches are very simple to determine because depending on how many cells are used $(4 \cdot m)$. It is possible to notice that this topology: is very modular in its configuration, based on only addition of cells to increase the voltage levels; is a standard configuration with respect to the control and topology; presents a number of components less than the others topologies of this section (Tab.3.1). The disadvantages of this topology are:

- Requires an isolated power supply for each level (or H-bridge);
- The common mode voltage on the dc-bus must be taken into account.

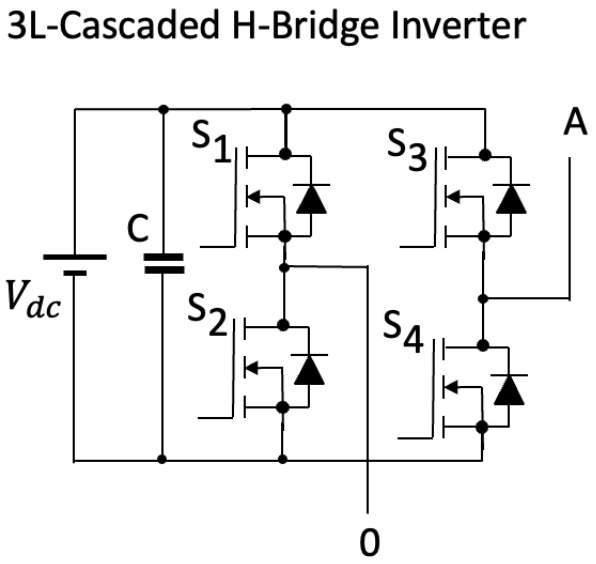


Figure 3.4: Cascaded H-Bridge 3L-single phase inverter.

3.5 Cascaded Half Bridge Inverter

The Cascaded Half Bridge multilevel converter is composed by a series connection between two-level Half Bridge cells. The single cell can generate in output $\pm V_{dc}$. Adding one cell with appropriate switch state it is possible to generate the 0V state and add a voltage level. In this configuration the voltage levels depend on number of cells. For example, for three levels one need to connect two cells, for four levels three cells in series

etc. This configuration permits with respect to cascaded H-Bridge to achieve one level proportional to how many cells are added. The ChalfB inverter produces $\pm 2V_{dc}$ while the switches sense only the V_{dc} as voltage stress around themselves [9]. This topology can be used with unequal DC sources. The disadvantage of this topology are:

- Requires an isolated power supply for each Half-Bridge Cell;
- The connection of two capacitor in series for each cells increases the number of capacitor each level.

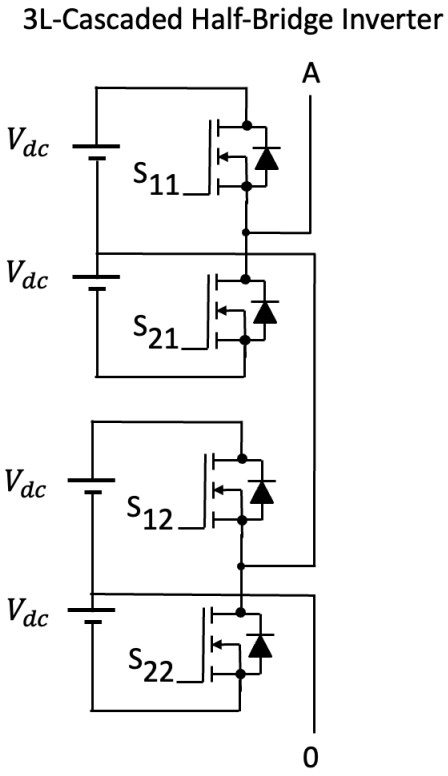


Figure 3.5: Cascaded Half-Bridge 3L-single phase inverter.

3.6 MMC Converter

The MMC Converter topology is composed by several Full-Bridge or Half-Bridge (Fig.3.6) cells depending on the number of voltage levels desired. This topology is very interesting because permits to obtain output voltage from different dc source as in case of solar panels as in Fig.3.6. Moreover, it is a very modular topology which permits

the increase of voltage levels adding a cell and more simple replacement of cells than other topologies (for example NPC topology) in case of fault. Another advantage of this topology is a better output current THD than NPC topology [10]. The disadvantages of this topology are:

- Requires more components with respect to other topologies discussed in this section (inductors to size, more flying capacitors (C) ecc.);
- The voltage balance and control of single flying capacitors requires a more difficult control with respect to standard topologies.

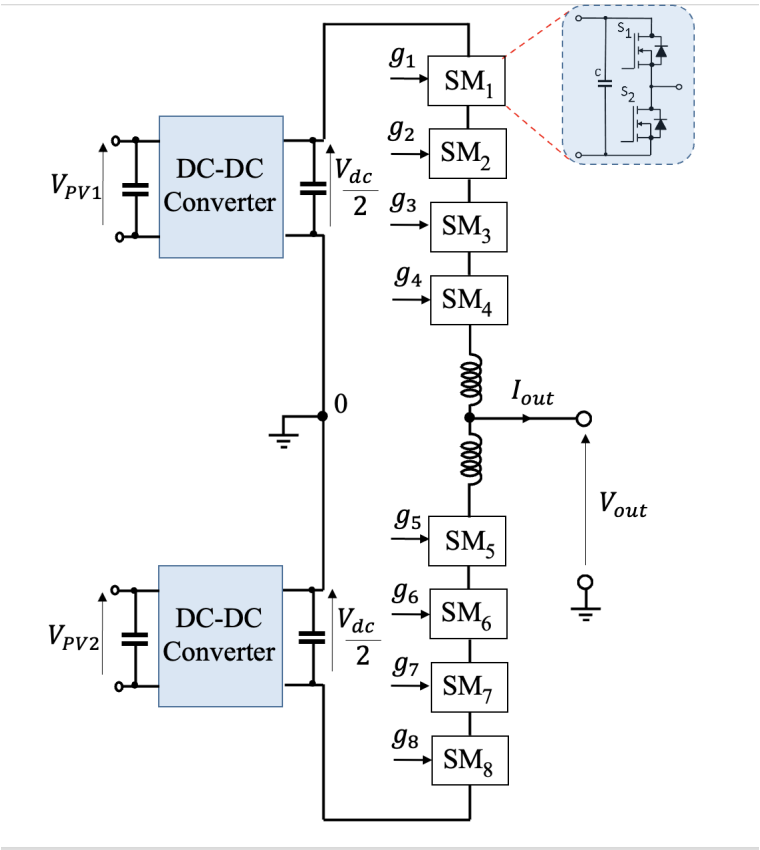


Figure 3.6: N-Level MMC converter..

3.7 Heric Converter

The Heric converter topology develops from Full-Bridge topology adding two more switches on the load side. This topology has been taken into consideration because

permits to overcome the problem of Common Mode Voltage on the dc-bus in the Full-Bridge converter [11]. The leakage current of common mode which is formed in the 0V state, flows, with appropriate control, through the two "AC Switch" (S1 and S2) shown in Fig.3.7. With these two more power switches is possible to confine the leakage current of CM Voltage in the load loop through the inductances of load. The Full-Bridge side control is the same as Full-bridge converter while the "AC Switches" are controlled in the 0V state with low switching frequency. The disadvantage of this topology is:

- Considering that the thesis work concerns a multilevel inverter with GaN transistor, the two "AC Switches" should be GaN. However, these two switches must switch at a much lower switching frequency than those of the Full-Bridge and therefore it is disadvantageous to use GaN devices.

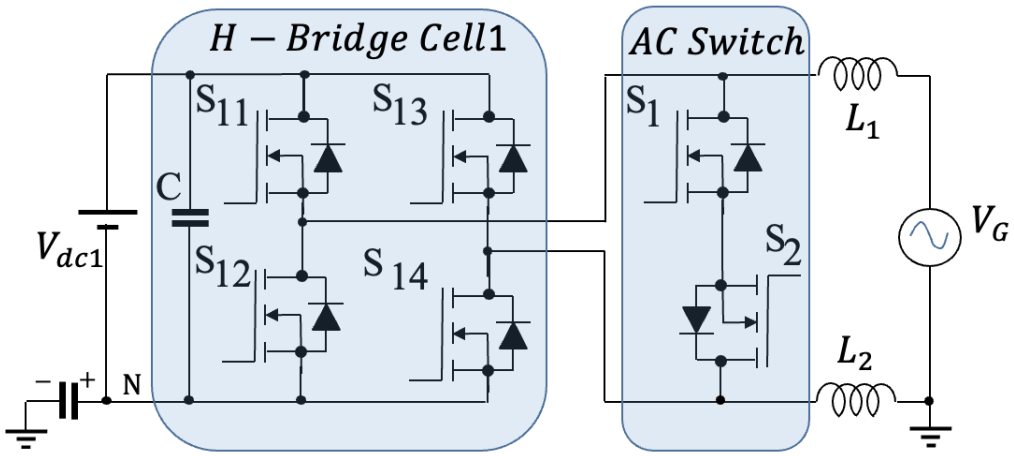


Figure 3.7: 3-L Heric Converter.

3.8 Flying Capacitor Converter

The Capacitor-clamped (or Flying Capacitor) topology derives from one simplification of the Diode-clamped structure, and provides for the use of supplementary capacitors (clamping capacitors) in addition to those already present on the dc bus as in Fig.3.8, in order to synthesize the different voltage levels desired at the output. These capacitors replace the clamping diodes of the previous configuration. To obtain m output voltage levels, is required a dc-bus consisting of $m-1$ capacitors, $2\cdot(m-1)$ switch and $(m-1)\cdot(m-2)/2$ clamping capacitance. The voltage applied to each component, except the clamping capacitors, is the same and is equal to $V_{dc}/(m-1)$. The clamping capacitors

are charged to different voltage values, for example $V_{dc}/2$ for 3-L converter in Fig.3.8, to produce the output voltage waveform while the switches are switched to combine the various charge voltages of the capacitors. The Flying capacitor topology permits to add output voltage levels inserting another flying capacitor and other two switches replicating the cell highlighted in yellow in the Fig.3.8.
The disadvantages of this topology are:

- The topology presents more capacitors to size which increase with the increase of voltage levels;
- The topology needs a specific control strategy for the Start-up and Shut-down to charge and discharge the capacitors without being damaged.

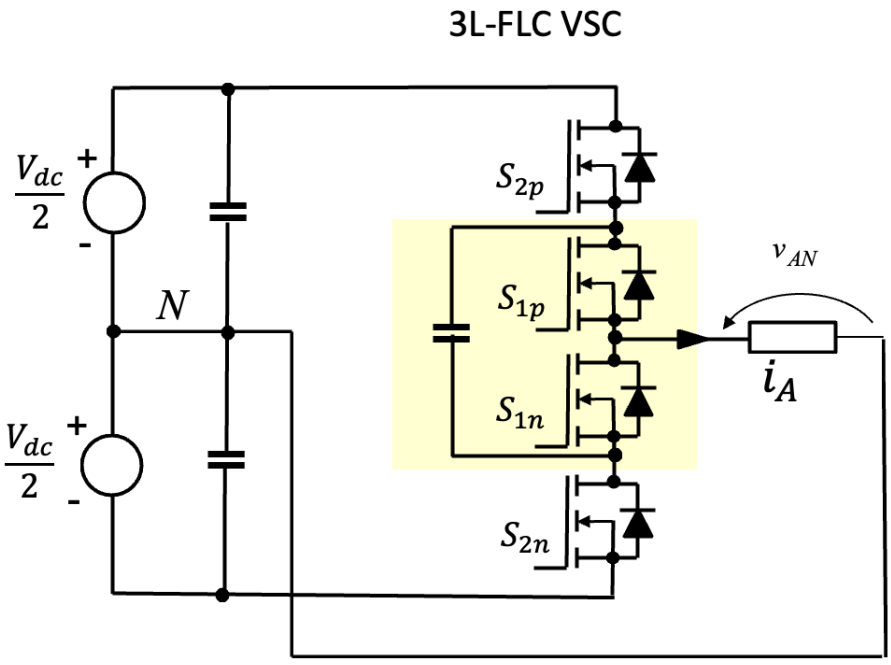


Figure 3.8: 3-L Flying Capacitor converter.

3.9 Conclusions

A summary of the principal characteristics of the topology discussed in this chapter is reported in this section. In Tab.3.1 are listed the number of components for each topologies while in Tab.3.2 are shown the voltage stress for each component in the

topologies discussed in this chapter. In this tables is considerable to notice that the MMC topology presents the higher number of switches and components. Another important data is the voltage stress in the switches which is the whole dc-bus voltage in CHB, CHalfB and Heric converters. The number of power supply has been important to define the kind of source which should be used.
In conclusion the topology which is chosen for the application that will be treated in the next sections is Flying Capacitor topology because:

- Considering the GaN transistors which will be used and the dc-bus voltage of 400V the voltage stress of switches could not equal to dc-bus total voltage;
- The modularity of this topology permits to add new cells in case to have more voltage levels;
- The topology presents a defined control mode;
- The topology permits to consider this application on microinverter with single PV voltage supply.

Table 3.1: 3-L topology components.

	NPC	Flying Cap	CHB	CHalfB	MMC	T-Type	Heric
Switches	4	4	4	4	8/16	2 + 2	4 + 2
Clamping diodes	2	0	0	0	0	0	0
dc-Bus Capacitor	2	2	1	2	2	2	1
Flying Capacitor	0	1	0	0	2 for each cell	0	0

Table 3.2: 3-L topology voltage stress.

	NPC	Flying Cap	CHB	CHalfB	MMC	T-Type	Heric
Switches	$V_{dc}/2$	$V_{dc}/2$	V_{dc}	V_{dc}	$V_{dc}/2$	V_{dc} and $V_{dc}/2$	V_{dc}
Clamping diodes	V_{dc}	0	0	0	0	0	0
dc-Bus Capacitor	$V_{dc}/2$	$V_{dc}/2$	V_{dc}	V_{dc}	V_{dc}	$V_{dc}/2$	V_{dc}
Flying Capacitor	0	$V_{dc}/2$	0	0	$V_{dc}/2$	0	0
Power Supply	1	1	1	2	1	1	1

Chapter 4

Application design and simulations

4.1 Introduction

In this chapter will be discussed the design of the application topic of this thesis work. In a general view, the objective of the chapter is to design via simulations with electrical and thermal simulation software (PLECS), a multilevel single-phase flying capacitor GaN transistor-based inverter for PV panel applications. The input voltage on the inverter dc-bus (V_{dc}) in Fig.4.1 must be $400V$. To obtain the V_{dc} from PV panel, the inverter discussed in this thesis work must be interfaced with the PV panel via a boost converter, indeed, to have a V-DC voltage of 400V, the panel voltage must be increased via the DC/DC converter. In this essay only the inverter side will be considered. The output voltage (V_{out}) which the application will have to reach, will have to be the American grid voltage about $110V_{RMS}$. Therefore, the peak output voltage on the load should be around $155V$. The frequency of output voltage will have to be 60Hz which is also the American grid frequency.
The converter will have to have a series capacitor to obtain the neutral point (N). For this reason, each capacitors in series have to withstand half the V_{dc} voltage. The flying capacitors connected between S_{2p} and S_2n have to sustain half V_{dc} voltage as shown in the chapter before.
PLECS simulations will be used in this chapter, to design the principal characteristics of the multilevel inverter which are listed below:

- Application GaN transistor;
- Modulation technique of the three level Flying Capacitor converter;
- Power Losses Analysis;
- Thermal Analysis;
- dc-bus and Flying Capacitor Capacitances.

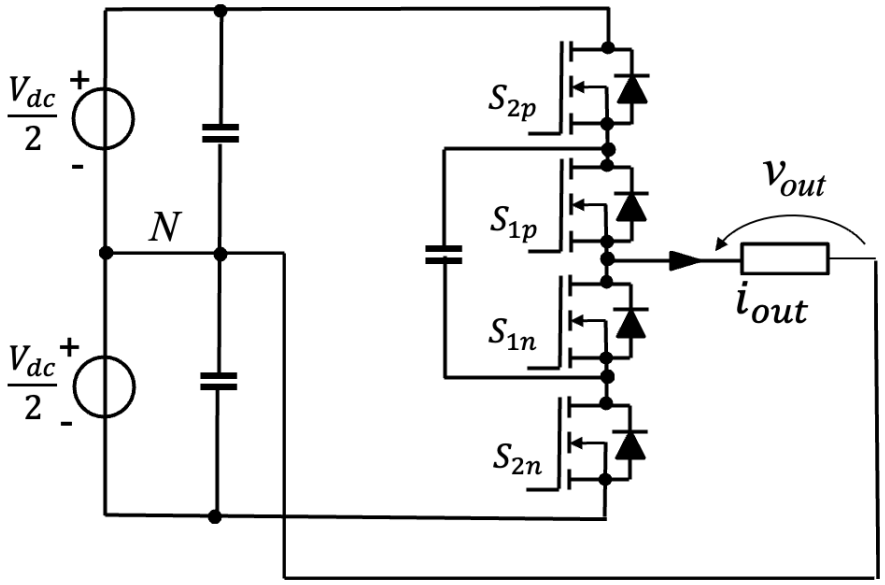


Figure 4.1: Electric circuit model of the multilevel application.

4.2 EPC2050 GaN Transistor

The transistor selected for the 3-L Flying Capacitor converter is the EPC2050. The EPC2050 is an enhancement mode GaN transistor made by Efficient Power Conversion Corporation. This FET is $1.95x1.95mm$ large. The pads to connect source, drain and gate of the FET are made with solder bumps (Fig.4.2). The pads are set as in Fig.4.3. The blue circles are the drain pads in the center of the die. The red circles in the two sides of the die are the source pads while only one pad is used for gate connection (Grey circle).
The EPC2050 GaN transistor can withstand 350V of drain-source voltage (V_{DS}). For this

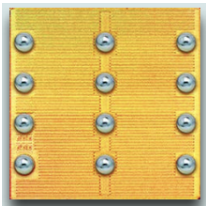
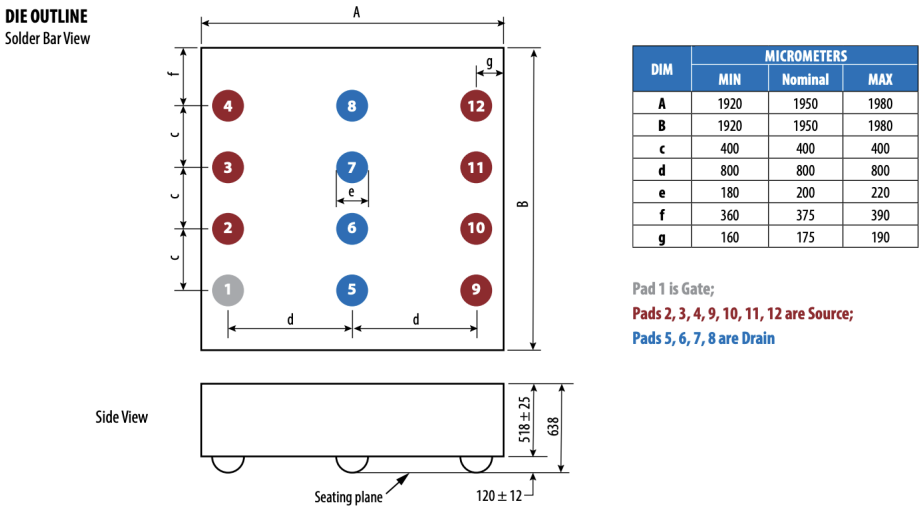


Figure 4.2: EPC2050 die view[12].

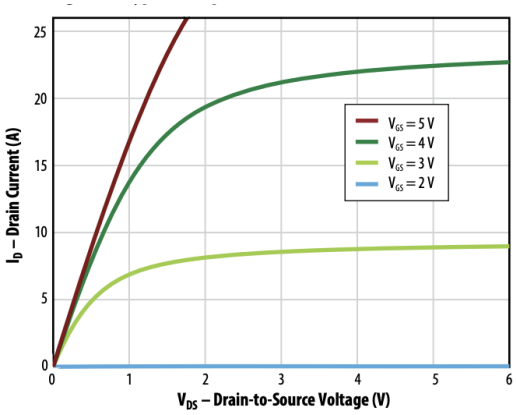
reason, it is suitable for application treated before. Indeed as discussed in the Tab.3.2 of the last chapter, the transistor of flying capacitor topology must sustain $V_{dc}/2$ minimum. In this case the minimum voltage on which to size the devices is about 200V. The more appropriate device for this application is the EPC2050 because can withstand over 200V



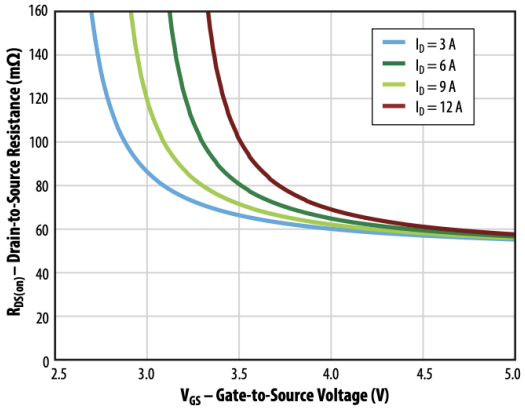
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	1920	1950	1980
B	1920	1950	1980
c	400	400	400
d	800	800	800
e	180	200	220
f	360	375	390
g	160	175	190

Figure 4.3: Pads mechanical schematics. [12]

of rated voltage and also it is able to withstand over 300V of nominal rated voltage. That voltage characteristic is important to give safety in terms of devices over-voltage stress. The typical gate-source voltage (V_{GS}) to obtain ON state is typical 5V [12]. In Fig.4.4a is shown the behaviour of V_{DS} during the transistor ON state related to the drain current I_D ad the V_{GS}. It is important to notice as at the typical value of V_{GS} (5V) the voltage drop of V_{DS} is less than other smaller values. In Fig.4.4b the behaviour of the on state resistance ($R_{DS,on}$) related to V_{GS} and I_D is described. The typical value of $R_{DS,on}$ of $60m\Omega$ is reached when the V_{GS} is on the typical value of 5V. The maximum value of $R_{DS,on}$ is $80m\Omega$ [12].



(a) EPC2050 V_{DS} vs. I_D and V_{GS}



(b) EPC2050 $R_{DS,on}$ vs. V_{GS} and I_D

Figure 4.4: EPC 2050 datasheet graphs.[12]

Another important feature of EPC2050 is the reverse drain-source characteristic. GaN devices don't present reverse recovery charge Qrr as discussed in the chapter 1 and therefore does not present a body diode. The current can flow in the device in both ways. The source-drain current I_{SD} causing a voltage drop explained in the graph in Fig.4.5 which depend on the device temperature.

The main characteristics of EPC2050 are reported in the Tab.4.1

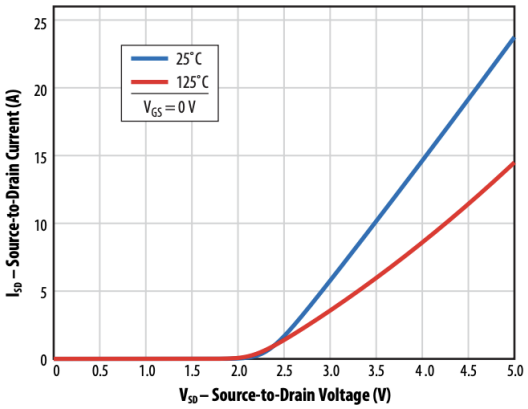


Figure 4.5: EPC2050 Reverse Drain-Source Characteristics. [12]

Table 4.1: EPC2050 main characteristics.

Parameter	**Value**	**Unit**
Max Drain-to-Source Voltage (Continuous) V_{DS}	350	V
Max Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C) V_{DS}	420	V
Max Drain Current (Continuous (T_A = 25°C)) I_D	6	A
Max Drain Current (Pulsed (25°C, T_{PULSE} = 300μs)) I_D	26	A
Max Gate to Source Voltage V_{GS}	-4 to 6	V
Operating Temperature T_j	-40 to 150	V
Typical $R_{DS,on}$	55	mΩ
Max $R_{DS,on}$	80	mΩ

4.3 Modulation Technique

In a multilevel FC inverter, the modulation technique must consider the behaviour of Flying Capacitors. The currents of FC must have a zero mean value. To reach zero mean value capacitor currents it is important that the duty cycles of the cells (m) in Fig.4.6 must be equal at stady state. To get a multilevel output voltage, the cells must use individual carriers phase shifted by $2\pi/m$ same as an interleaving. This modulation technique also obtains a frequency multiplication effect that will be discussed later. In the thesis work application case, the two carriers are shifted by 2π because there are only two cells (m) to reach three voltage levels. A block model of Flying Capacitor inverter control is shown in Fig.4.7. The $v_0(t)$ is the peak maximum output voltage of the application ($110 \cdot \sqrt{2}$ V) that it is normalized on 400V (V_{dc}). After have shifted and saturated the signal, $v_c(t)$ it is compared with the two carrier shifted as shown in Fig.4.7. The signals $q_{1p}(t)$ and $q_{1n}(t)$ are the gate commands for S_{1p} and S_{1n} (Fig.4.1) while q_{2p} and q_{2n} are the commands for S_{2p} and S_{2n}. The PWM modulation with two carriers shifted as said before creates

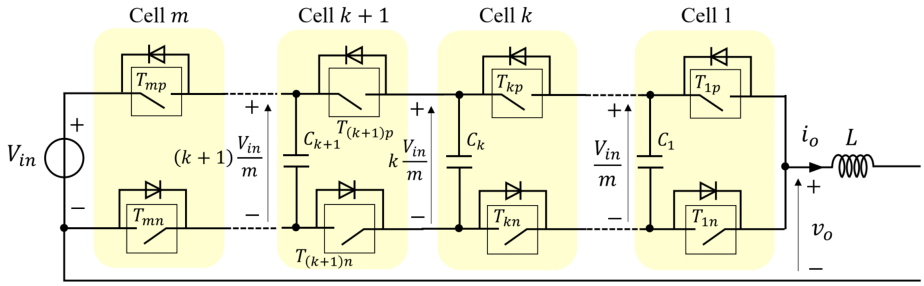


Figure 4.6: Flying capacitor converter circuit scheme. [13]

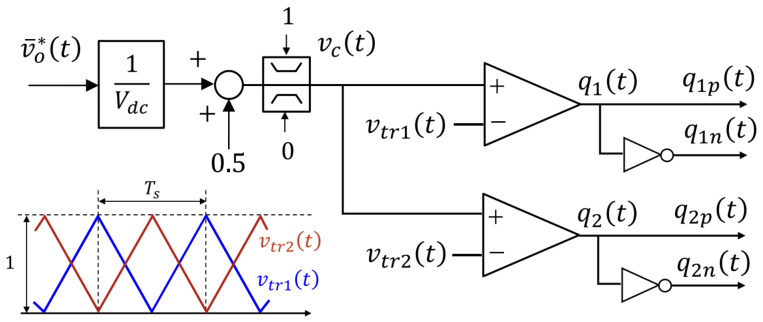


Figure 4.7: PWM modulation block model. [13]

a doubling effect on the output voltage frequency. In Fig.4.8 it is possible to notice this effect. The switching frequency on the example in Fig.4.8 it is 100kHz while the square wave of the output voltage simulated in the PLECS model has 200kHz of frequency and $5\mu s$ of time switching period. Therefore, this will be important in frequency choose and in ripple sizing.

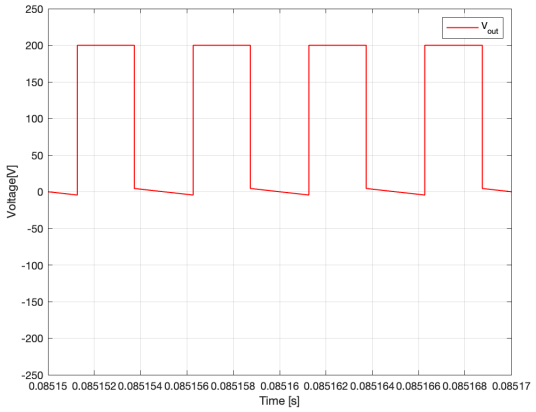


Figure 4.8: Output Voltage waveform ($f_{sw} = 100KHz$ and $v_0(t) = 110V_{RMS}$).

4.4 Power Losses Analysis

In this section will be discussed the power losses of the multilevel converter. In this analysis will be considered the power losses of the switching cells to arrive, with simulation results, to select the better compromise in terms of power losses and converter performance.
The analysis will follow the point of view listed below:

- Devices switching losses;
- Devices conduction losses;
- Devices considerations.

4.4.1 Analysis Model

To analyse the power losses in the switches of the multilevel converter is used simulations results by LT-Spice circuit model. Before start discussing about the results, the principal characteristics of the model will be explained.
The circuit model of LT-Spice simulations for EPC2050 switching and conduction losses calculation is shown in Fig.4.9. As shown in Fig.4.9, the circuit is composed by two EPC2050 devices. The LT-Spice model of EPC2050 was taken from EPC-Co libraries. In the circuit are modeled also the parasitic inductances between GaN transistors with $100pF$ inductors and the parasitic inductances which modeled the connection between devices and the ground or the voltage source. The Power supply in the circuit is modeled with a DC voltage source (V1) that will be varied depending on the simulations. The output is modeled with continuous current source (I1).
The simulation frequency (f_{sw}) is set to 100 kHz with a dead time (dt) of 50 ns as in Fig.4.9. The switches control LT-Spice model is shown in Fig.4.10. The 5V command to switch on the devices is generated by a pulse voltage source with five and zero voltage limits and a switching period (T_{per}) calculated by $1/pwm$. The ON and OFF command are given by two switches (Example: S2 and S1 in Fig.4.10). To model the gate driver chosen for this application, that will be discussed in the next chapter, the main characteristics for on-mode case are put into GDon parameters, following gate driver datasheet. For gate driver off-mode case the parameters are in GDoff side in Fig.4.10. In the control circuit are also considered the external On-Resistance (R_{gon}) and OFF-Resistance (R_{goff}) set to 10Ω and $480m\Omega$ to have a right dv/dt during switching period. The connection between the control circuit in Fig.4.10 and the gate of the EPC2050 presents a parasitic inductance (Fig.4.9) about 1 nF to model the PCB connection.

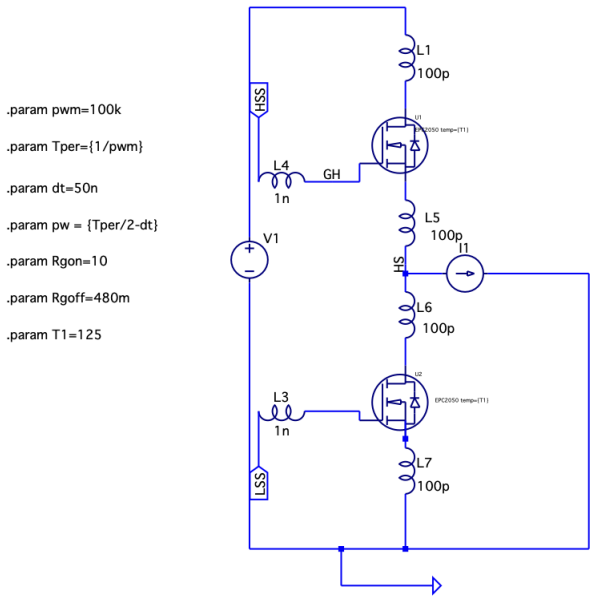


Figure 4.9: LT-Spice Power Circuit model.

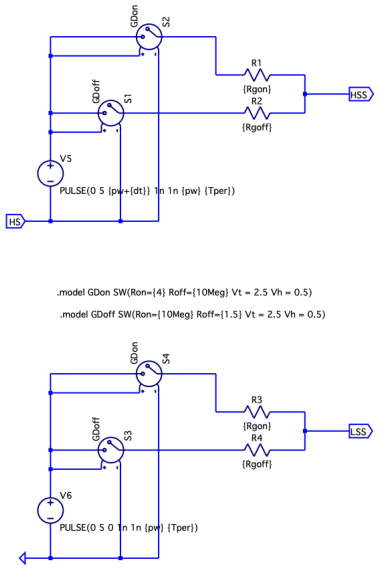


Figure 4.10: LT-Spice switches control model.

4.4.2 Switching Losses

During the switches commutations are important to analyse the power losses of the switches. To find the power losses analysis during the commutation are used the LT-Spice simulations with the circuit models shown in Fig.4.9 and Fig.4.10. The switching losses analysis are determined varying the input voltage of the model (V1) and the output current (I1). The switching losses are fundamental to characterize the behaviour of the switches during the switching period. The simulations were made with three input voltage values such as 150V, 200V and 250V and different devices voltages as $25°C$, $90°C$ and $125°C$. For current values ranging from 0A to 26A have been taken into consideration in the simulations to describe the EPC2050 behaviour considering until the maximum current value indicated by the datasheet. To arrive to the switching losses will be evaluated the energy used during switching through LT-Spice energy calculator.
The switching losses are divided into two cases: switching losses during the on-commutation of the transistor and switching losses during the off-commutation.
The commutation which the transistor is switched in on-state, is described in the Fig.4.11. In the on-state commutation the drain-source voltage drops to near 0V while the transistor starts to conduct and the drain current (I_D) rises up to 10A that it is the simulation current value. The energy of the on-state commutation (E_{on}) is calculated by LT-spice just when the voltage drops to more than 0V and the current rises to 10A. The results of the simulations are reported in Figs.4.13,4.14,4.15. As shown in the plots, the E_{on} behaviour depends on the temperature and the voltage applied on the devices. In terms of voltage it is important to notice that the E_{on} at the same operating temperature, increases with the devices voltage. For example, in the Fig.4.13a the E_{on} maximum value at 26 A of drain current (I_D) is about $50\mu J$ while in the Fig.4.15a it is possible to notice that the E_{on} reaches more than $90\mu J$. Another important aspect is the increase of E_{on} with respect to temperature. The increasing of E_{on} is not relevant as in the case dependent on the temperature but it is possible to note that with the same applied voltage there is an increase of E_{on} as the temperature increases. For example, in Fig.4.14a the E_{on} at 26 A I_D is about little more $70\mu J$ while at the same conditions with an increase of temperature until $125°C$ the E_{on} increase about $75\mu J$.

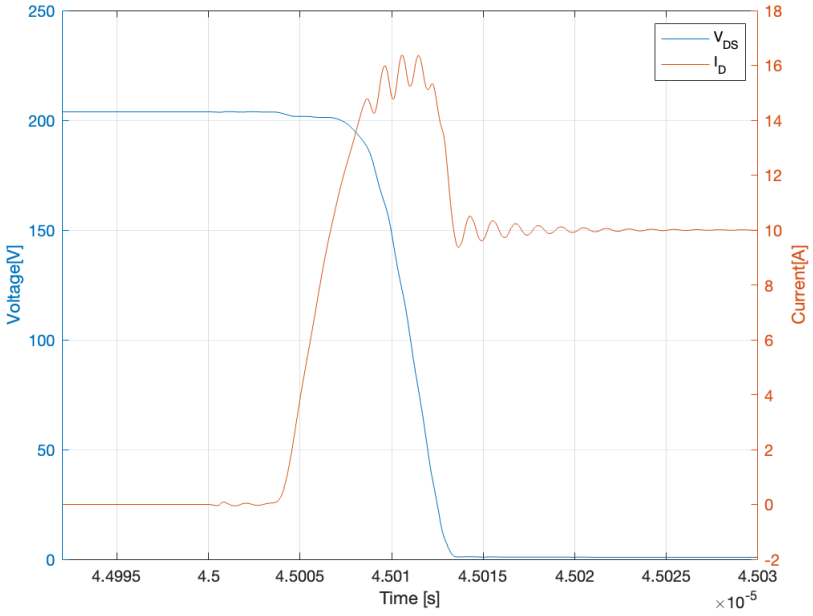


Figure 4.11: Switching on of EPC2050 GaN transistor LT-Spice simulation waveforms (100kHz, $I_D = 10A$).

During the off-state commutation the behaviour is shown in Fig.4.12. To switch on the current of the devices I_D goes to zero with ringings due to parasitic inductances of the simulation model. Instead the devices voltage raise up to 200V which it is the voltage applied on the devices during the commutation in Fig.4.12. Also in this case thanks to the model described in the Fig.4.9 and finding the energy (E_{off}) present during the switching in Fig.4.12 using LT-Spice, the results of the E_{off} depending on the devices applied voltage and the temperature are described in Figs.4.13,4.14,4.15. The E_{off} reaches much smaller values than E_{on}. For example, in Fig.4.15, can be seen how the E_{on} reaches values just under $100\mu J$ while the E_{off} around $4\mu J$. The E_{off} curve is more constant than E_{off}. In fact, we do not have a steep rise in values with increasing current but rather there is a trend that grows slightly from 0A to 26A. For example taking into account the simulation results in Fig.4.13b, the E_{on} increases from about $3\mu J$ to about $50\mu J$ while the E_{off} increases from about $1.30\mu J$ to more or less $2.3\mu J$.
The results of E_{on} and E_{off} will be used in PLECS simulations to describe the real behaviour of the EPC2050 devices during the commutations.

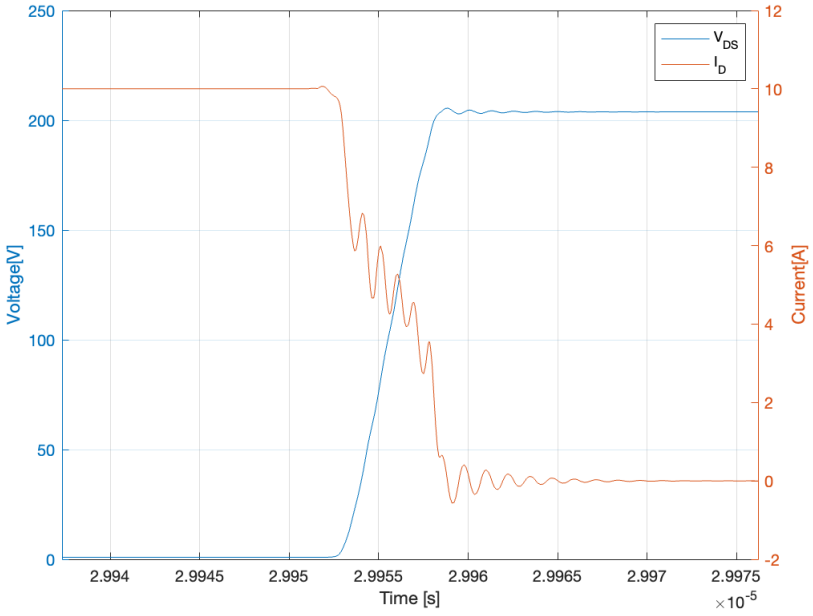
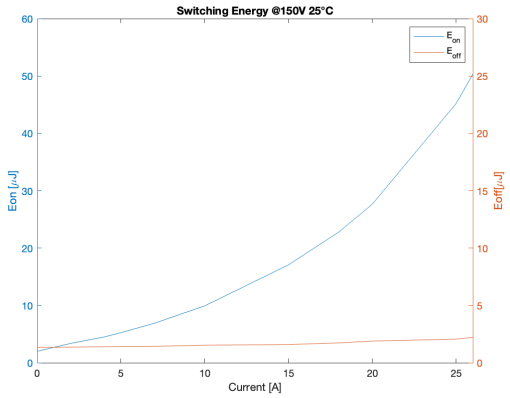
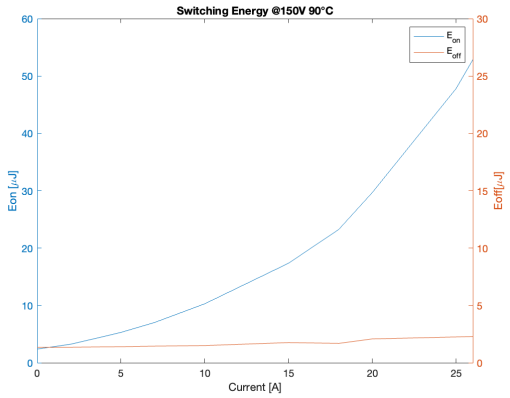


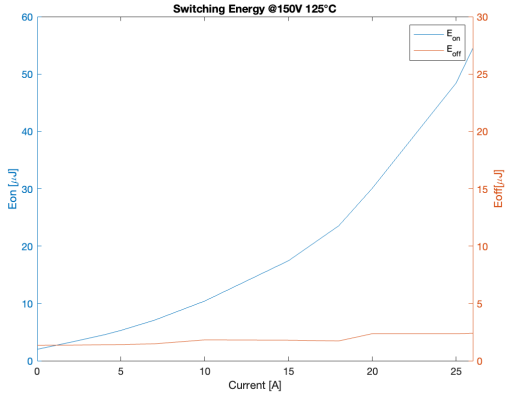
Figure 4.12: Switching off of EPC2050 GaN transistor LT-Spice simulation waveforms (100kHz, $I_D = 10A$).



(a) E_{on} and E_{off} with 25°C of devices temperature.

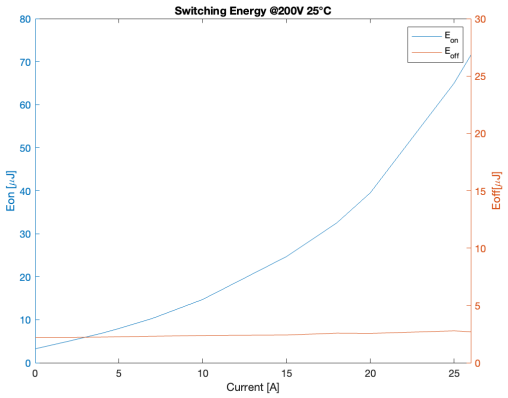


(b) E_{on} and E_{off} with 90°C of devices temperature.

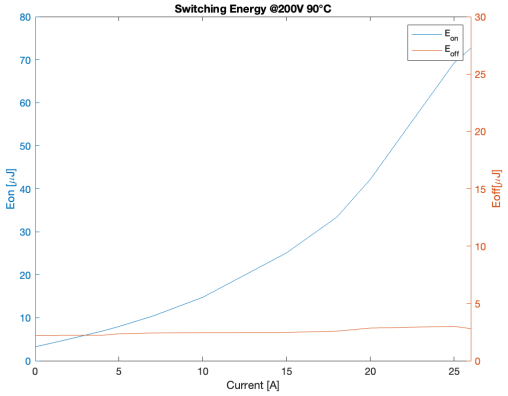


(c) E_{on} and E_{off} with 125°C of devices temperature.

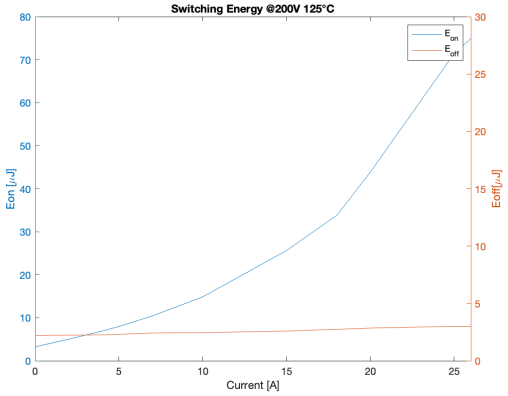
Figure 4.13: E_{on} and E_{off} related to current with 150 V input voltage.



(a) E_{on} and E_{off} with 25°C of devices temperature.

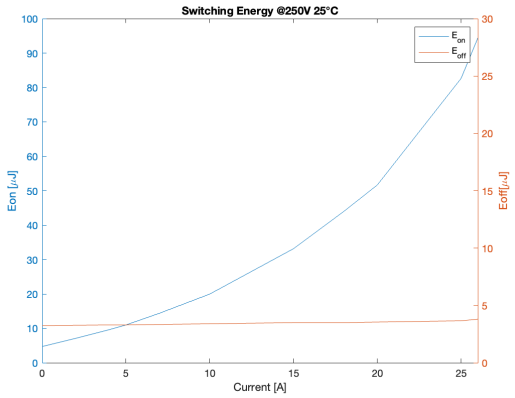


(b) E_{on} and E_{off} with 90°C of devices temperature.

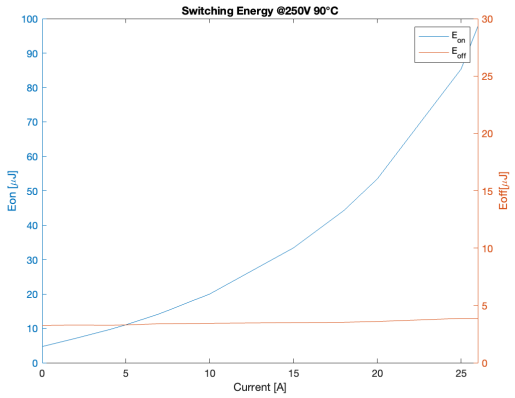


(c) E_{on} and E_{off} with 125°C of devices temperature.

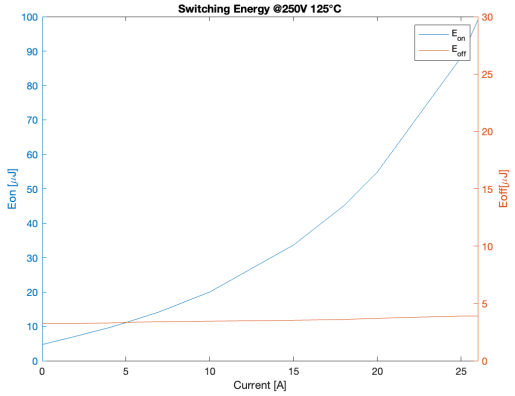
Figure 4.14: E_{on} and E_{off} related to current with 200 V input voltage.



(a) E_{on} and E_{off} with 25°C of devices temperature.



(b) E_{on} and E_{off} with 90°C of devices temperature.



(c) E_{on} and E_{off} with 125°C of devices temperature.

Figure 4.15: E_{on} and E_{off} related to current with 250 V input voltage.

4.4.3 Conduction Losses

To describe the GaN transistor EPC2050 it is important to define the conduction losses caused by the passage of current through the transistors.
In a real switch during the on-state the voltage drop across the device is not zero (Fig.4.16). For this reason the device produces power losses.

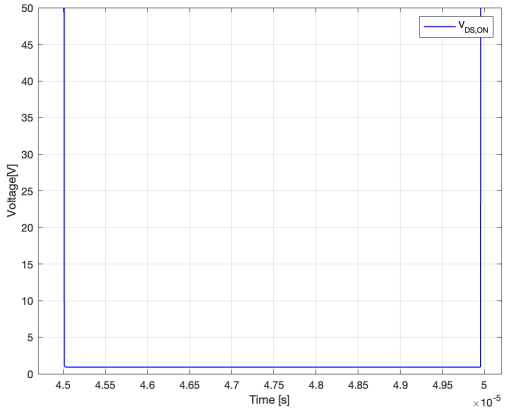


Figure 4.16: $V_{DS,ON}$ during the on-state of EPC2050. LT-Spice simulation results (125°C, 200V and 10A).

The conduction losses during on-state depending on on-state resistance ($R_{DS,on}$). However $R_{DS,on}$ is very temperature dependent. As shown in Fig.4.17 the resistance depending on junction temperature of the device. In the case of EPC2050 the $R_{DS,on}$ increase its value by two times at 150°C. This aspect greatly influences the trend of the voltage drop during the on state and therefore the behaviour in terms of conduction losses. To get an idea of the voltage drop relative to the on state, through simulations with the LT-Spice model in Fig.4.9, the results shown in Fig.4.18 are taken as a reference. In the plots is shown the $V_{DS,ON}$ as a function of junction temperature of the device in on-state. The voltage drop increase with the increasing with the increasing of the current across the device. Moreover, at the same current the voltage drop values obtains by junction temperature of 125°C is more than 25°C simulation value results precisely because of the great dependence of the resistance on the temperature discussed before.

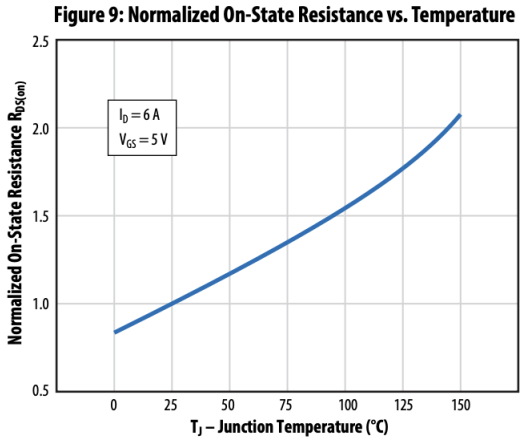


Figure 4.17: EPC2050 normalized $R_{DS,on}$ as a function of junction temperature T_j.[12]

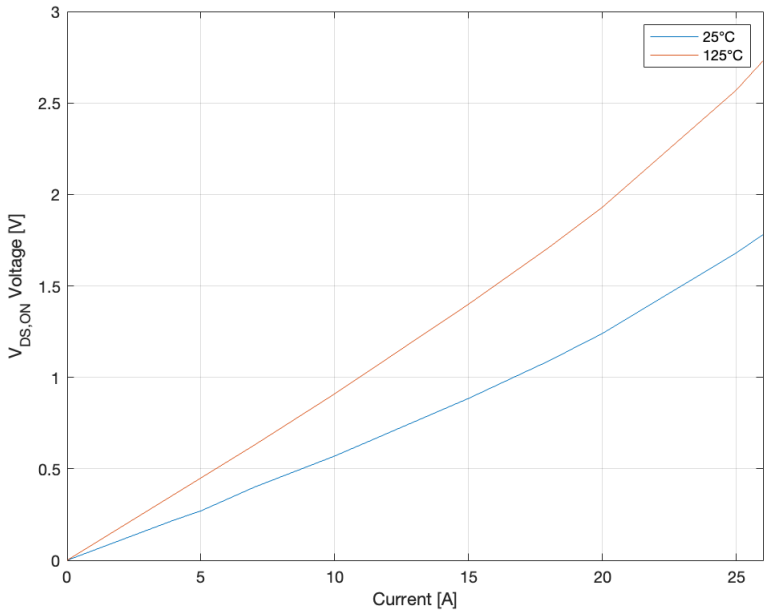


Figure 4.18: $V_{DS,ON}$ as a function of temperature and current LT-Spice simulation results.

As said in the previous chapter, the GaN transistors do not present body diode but permit to be crossed by the current from the source to the drain. This behaviour named reverse conduction is possible when the device is turned off. But also in this case there is a voltage drop on the device. This voltage drop, as in on-state case, produces power losses on the devices. The voltage drop in reverse conduction (V_{SD}) is possible to obtain when the V_{GS} is equal to 0V. The behaviour of voltage drop in reverse conduction is described in Fig.4.19.

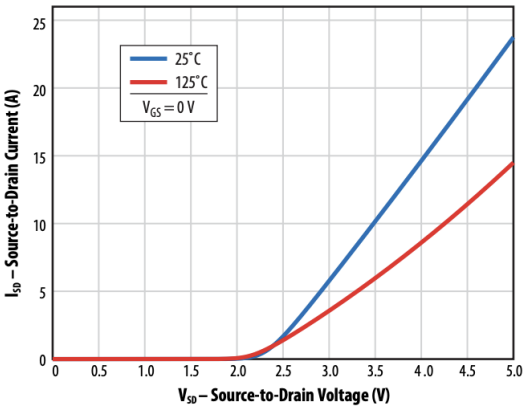


Figure 4.19: Source-to-Drain voltage as a function of temperature and Source-Drain current.

In terms of currents the voltage drop definitely rises as the current increases. Moreover the V_{SD} increases with temperature at the same Source-to-Drain I_{SD} current conditions. The voltage drops arise from conduction and reverse conduction across EPC2050 will be inserted as a Look Up Table (LUT) in PLECS simulation model to estimate the real behaviour of the transistors during the multilevel inverter working.

4.4.4 Power Losses Considerations

The results of switching and conduction losses as described in the previous sections are used as look up table to describe the real behaviour of the EPC2050 devices during the inverter working. In the Fig.4.20 is shown an example of LUT inserted in the PLECS inverter model. LUT are important to describe the power losses of the total system. As defined before the study of power losses is related only about switches losses and power losses due to other factors will not be considered.

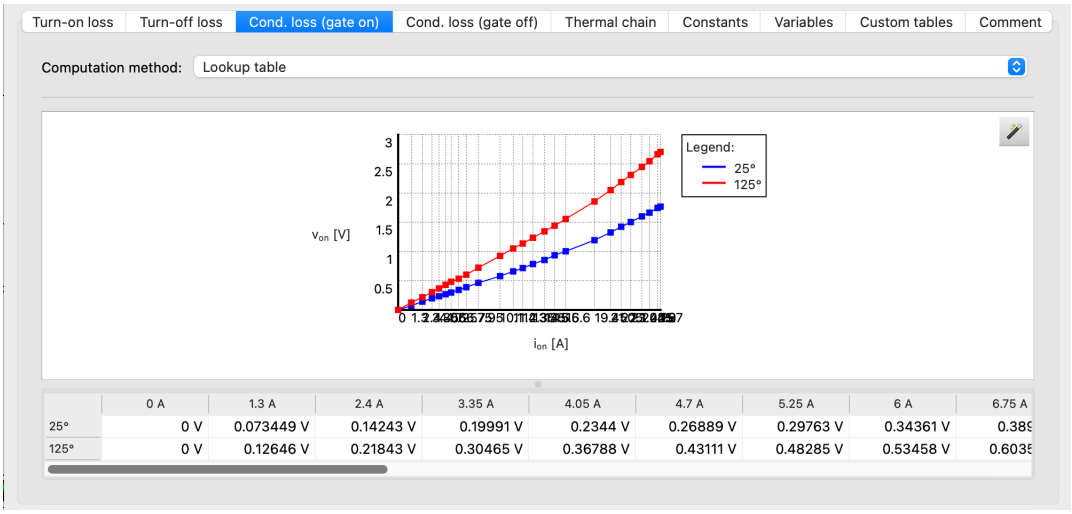
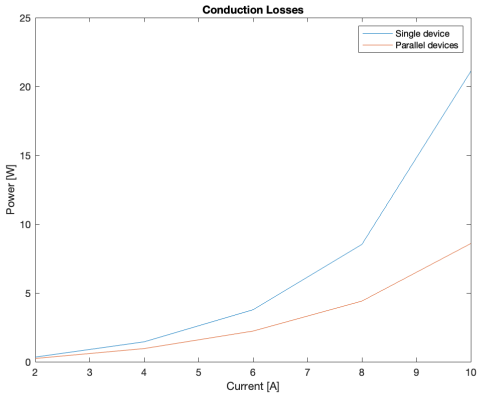


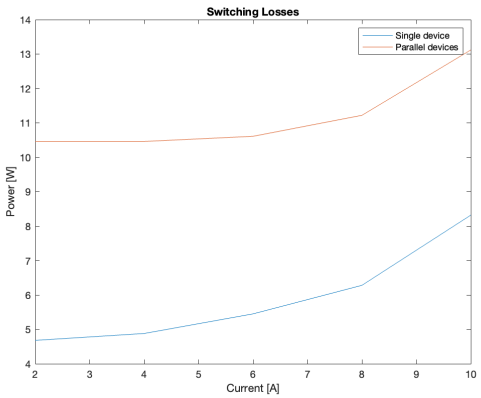
Figure 4.20: $V_{DS,ON}$ LUT on PLECS model.

To define the power losses is used the PLECS circuit model described in Fig.4.25. Taking into consideration the circuit model in Fig., in addition to the components already seen above, there is a heatsink modeled as a blue box on the power cells. Moreover, the heatsink is connected to a thermal resistance and a temperature generator which describes the ambient temperature ($25°C$). The resistance and generator in thermal side of the circuit modeled the thermal circuit. However the thermal circuit shown in Fig.4.25 is not the definitive thermal model of the inverter but only a temporary model functional for the analysis that will be described in this section.
Simulations were made to see, with this temporary model, what were the trends in terms of power losses for the single device using the model in Fig.4.22a. Furthermore, a model with several devices in parallel was also considered, in this case two, following the circuit present in Fig.4.22b. This analysis with two parallel transistors were considered to understand if there are advantages in terms of power losses considering two devices instead of one. The trends of power losses are described in the plots in Fig.4.21 which are the results of simulation with single and parallel devices ($V_{DC} = 400V$ and $V_out = 110V_{RMS}$). As described in Fig.4.21 the conduction losses start to be very relevant after some current values. This aspect is very important in terms of power losses because conduction losses in Fig.4.21a they become really relevant as the current increases with respect to the switching losses in Fig.4.21b which more or less have a trend with a less increasing curve. Another aspect is highlighted in Fig.4.21a. The conduction losses decrease significantly in the parallel devices' configuration. Instead, the switching losses increase with parallel devices configuration. Therefore considering that the conduction losses are more decisive as power losses, above all by increasing the output current, then switching losses, the model in the Fig.4.22b was chosen as the definitive model of the application treated in this thesis work. Indeed with the parallel devices an increase in output current is allowed thanks to the fact that the current in the devices will be half and that therefore

the conduction losses are decreased. Moreover, decreasing the current across the devices also having a smaller temperature increase in the devices than single device configuration that will be treated later.

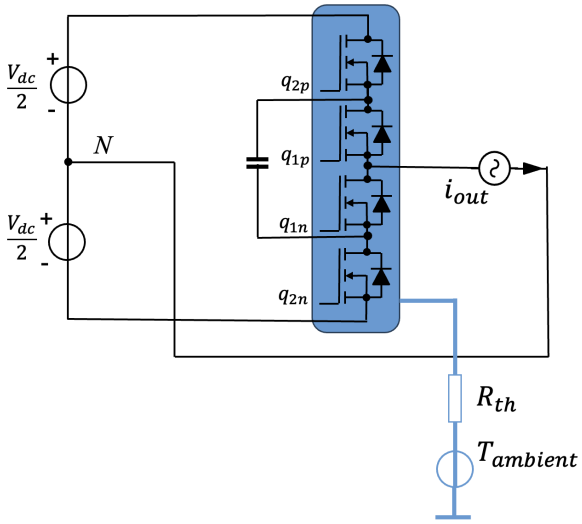


(a) PLECS simulations results. Total conduction losses with single and parallel devices.

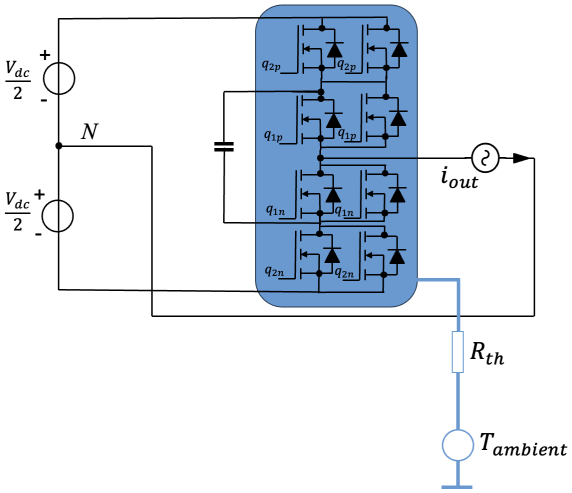


(b) PLECS simulations results. Switching losses with single and parallel devices.

Figure 4.21: Comparison between single and parallel devices total power losses of PLECS simulations.



(a) PLECS inverter circuit model with single devices.



(b) PLECS Inverter circuit model with parallel devices.

Figure 4.22: PLECS Inverter circuit model with temporary thermal model.

4.5 Thermal Analysis

4.5.1 GaN Thermal Model

When using surface mount packaged power semiconductors, the PCB constitutes the main heat conduction path for the mounted devices and it is especially critical when no case-side cooling is implemented. Furthermore, packaged devices have multiple thermal interfaces between the die and the PCB. In comparison, chip scale packaged (CSP) devices have direct metallic contacts (solder) that offer good electrical and thermal conductance path into the PCB. The heat then spreads into the conductive layers of the PCB where it benefits from the large PCB area (compared to exposed FET area) and dissipates into ambient. Each of the mentioned PCB components introduce some thermal resistance to heat flow and should be modeled for an accurate characterization. In Fig.4.23 are described the thermal resistance between the die of the GaN FET and the PCB to the ambient. As shown in Fig.4.23 from the die to PCB there is thermal resistance R_{J-PCBT} which modeled the junction-to-PCB thermal resistance. Another resistance is the $R_{z,PCB}$ thermal resistance which modeled the thermal resistance of the PCB considered conductive layers between FR4 insulating layers. In the model, three regions are considered for the PCB stack, a top region constituting half of the conductor layers with their FR4 insulation (typically, 5 or 10 mils thick), a similar bottom stack with the remaining half of conductor layers and FR4 spacing, and a central region of FR4 core which separates the bottom and top regions and it is usually thicker and more insulating. The respective contribution of the top and bottom surface to heat dissipation may differ, and thus the two layers (top and bottom) are considered as separate heat conduction paths. If are present thermal vias will behave as thermal connectors to allow heat to conduct from the top stack to the bottom stack. Two temperature nodes are defined for the PCB top and PCB bottom node in the region underneath the FET (Fig.4.23) with the respective thermal resistances to ambient(R_{PCBT-A} and R_{PCBB-A})[14].

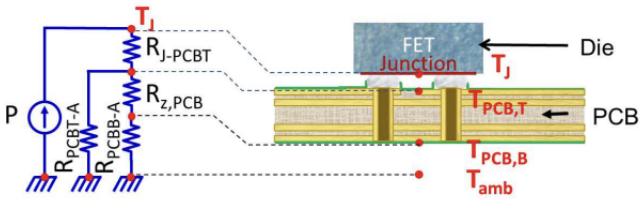


Figure 4.23: Thermal resistive circuit showing thermal resistances at PCB side (board-side).[14]

In applications with high power densities, additional cooling may be required to limit self-heating effects by adding a thermal solution to dissipate more heat from the backside (i.e., case-side) of the FETs. The die of CSP GaN FETs is exposed with the

silicon substrate having a low junction-to-case thermal resistance ($R_{th,JC}$ in Fig.4.24), in comparison to devices plastic packaged [14], and as such can more effectively benefit from back-side cooling. As in Fig.4.24 the heatsink is situated in the case side of the transistor to better dissipated the heat [14] and determines the R_{HSk} . Another dissipation interface named heat-spreader it can be placed just below the heatsink which introduces a high conductivity area (copper material) for heat to spread and conduct away from the device and reduce hot spots. This introduce the R_{HSp} thermal resistance. To ensure good thermal conductance, thermal-interface materials (TIM) are placed at the contact between the devices and the heatsink bottom surface. TIMs have good thermal properties and come in different forms (pads, gels, putties. . .) and are selected depending on the application. This is modeled with R_{TIM} thermal resistance. For smaller FETs, the top surface area may be comparable to that of the die sides and as such, heat removal can be enhanced by adding more TIM around the FETs using TIM gel or gap filler. This adds a heat conductance path from the die sides to the sink, and from the top PCB copper to the sink. These paths are represented by their respective thermal resistances R_{GF} shown in the network of Fig.4.24

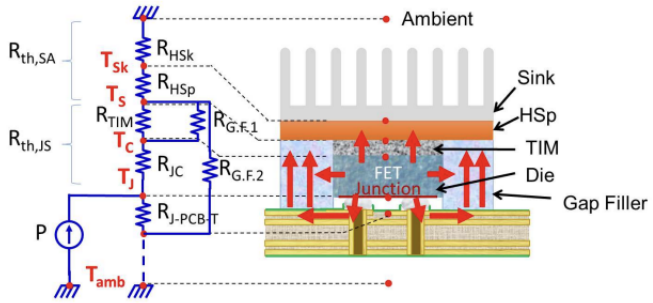
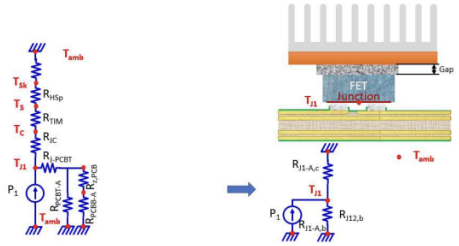
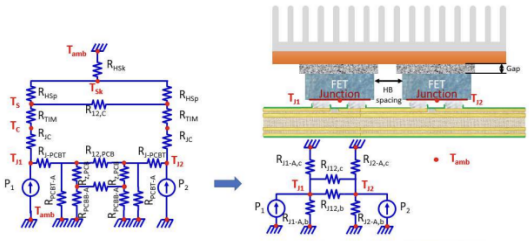


Figure 4.24: Thermal resistive circuit showing back-side cooling with TIM pad, gap filler material, a heatspreader and a heatsink.[14]

After setting up the thermal resistances that constitute the thermal system, the circuit model would resemble the schematic shown in Fig.4.25a for a single FET, and Fig.4.25b for a half-bridge configuration. The full circuit is simplified to extract the overall resistances to ambient through the board-side path ($R_{th,J-PCB-A}$), and through the case-side path ($R_{th,J-C-A}$) if a back-side cooling solution is present.



(a) Schematic of a Single FET.



(b) Half-bridge configuration.

Figure 4.25: Full thermal resistive circuit model and circuit model after simplification[14].

4.5.2 Thermal Tool

A tool of EPC-Co named GaN Power Bench tool is used to design the thermal circuit of the multilevel inverter. This thermal calculator provides quick estimates for the thermal performance parameters of PCB-mounted GaN devices subject to both board-side cooling through forced convection, and backside cooling through a thermal solution consisting of a heat spreader and heatsink. The model accounts for the PCB construction (size, stack-up and via density), die sizes, power losses, TIM materials and heatsink solution. The model allows to compare the thermal performance of the GaN FETs with and without backside cooling and can be used to quickly estimate the effect of using different TIM pads and TIM gap fillers. In addition, the cooling effect of the heat spreader and heatsink can be quickly assessed. Two configurations are considered: one for a single FET (Fig.4.25a) and another for two FETs in a half-bridge circuit (Fig.4.25b). The different input parameters required for the model can be inputted using a simple and intuitive graphical user interface (GUI) after which the model calculates individual thermal resistances values (R_{th}) and the operating junction temperatures (T_J) for a defined power loss [15]. In the Fig.4.26 is shown an example of GUI page where is possible to choose the number of devices, the serial number of devices and other features as the number of thermal vias or the power losses in the device. In the other pages is possible to obtain the heatsink characteristics with heatsink calculator and it is possible to add TIM and other features that construct the real FET thermal interface.
At the end of GUI are generated the single thermal resistances to put in a resistive circuit model to simulate the thermal behaviour of the GaN FET.

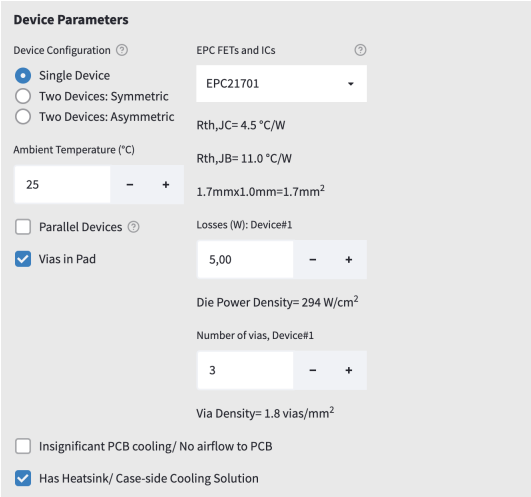


Figure 4.26: Screen of one Graphical User Interface page.

4.5.3 Multilevel Inverter Thermal Circuit Model

To define the thermal circuit model for thermal analysis in PLECS simulator is necessary to make the following assumptions considered as a input on the thermal calculator of GUI discussed in the previous section:

- For this model an aluminium heatsink above the case with a size of 50mm and 15 fins is considered. It is also considered a TIM with thermal conductivity of $6W/m \cdot K$ and TIM gap/bondline thickness of $0.5mm$. The air flow to heatsink is defined on 100 LFM that is the worse case airflow condition;

- The PCB is composed by 6 copper layers with $2oz$ of thickness. The total PCB thickness is $1.6mm$. The air flow also in this case is set on 100 LFM;

- Are not considered liquid or gel gap fill and heatspreader;

- For the S_{2p}, S_{2p1}, S_{2n},S_{2n1} in Fig.4.28, is used the "Two Devices: Symmetric" configuration in Fig.4.26. This configuration uses the half bridge simplified model shown in Fig.4.25b. It is assumed that these devices thermally influence each other without affecting the other devices. The resistances obtained with this configuration will be named in the thermal circuit as $R_{th..}$.

- For the S_{1p},S_{1p1},S_{1n},S_{1n1}, in Fig.4.28, is used another configuration with respect to the other devices. The configuration is named "Parallel Devices" also considering the half bridge model. In this configuration the devices are considered as an array of 4 transistors which influence each other in terms of heat dissipation. The GUI page to set the parallel setup is shown in Fig.4.27. It is assumed that the two devices in parallel, in addition to being thermally connected to themselves, are also

connected to the other two devices in parallel via other $R_{pthj12...}$. The resistances obtained with this configuration will be named in the thermal circuit as $R_{pth..}$.

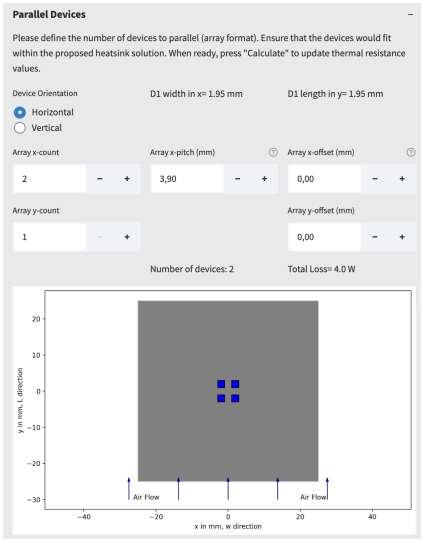


Figure 4.27: Parallel Devices GUI page.

The definitive thermal circuit model obtained from the assumptions discussed above is shown in Fig.4.28. As in the simplified half bridge circuit model in Fig.4.25b are defined:

- Thermal resistances from junction to ambient in the case-side named R_{thj-A_c} and R_{pthj-A_c};
- R_{thj-A_b} and R_{pthj-A_b} which represent the junction-to-ambient thermal resistances considering PCB side;
- R_{thj12_b},R_{thj12_c}, R_{pthj12_c}, R_{pthj12_b} as thermal resistance between the two neighboring transistor junctions board-side and case-side.

The thermal resistances obtained with the GaN POWER BENCH are reported in the Tab.4.2.

Table 4.2: Thermal resistance values.

Parameter	**Value**	**Unit**
R_{thj-A_c}	22	$°C/W$
R_{thj-A_b}	44.9	$°C/W$
R_{pthj-A_c}	26.6	$°C/W$
R_{pthj-A_b}	56.9	$°C/W$
R_{thj12_b}	41.5	$°C/W$
R_{thj12_c}	137.6	$°C/W$
R_{pthj12_c}	89.9	$°C/W$
R_{pthj12_b}	38.1	$°C/W$

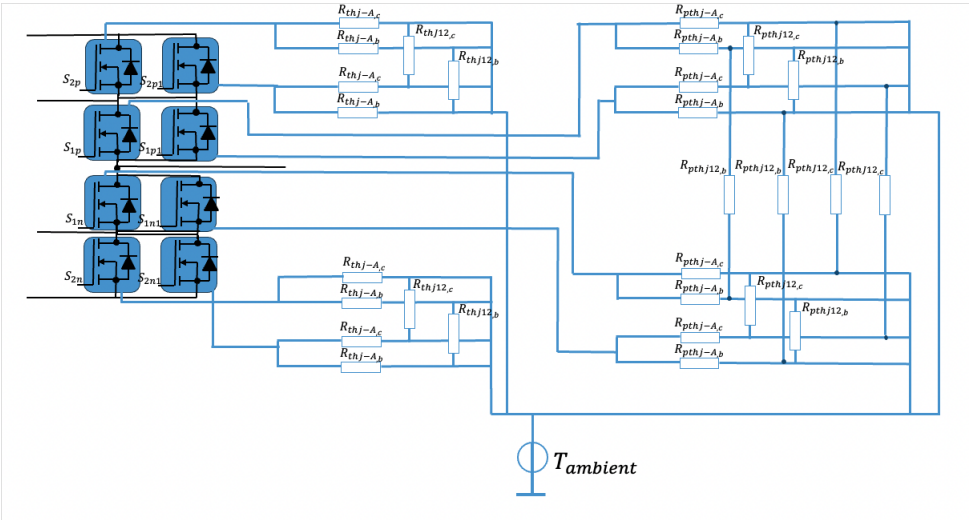


Figure 4.28: Multilevel inverter thermal resistive circuit.

4.6 Switching Frequency

The switching frequency of the inverter is defined with two parameters: efficiency and thermal management of the system.
To get an idea of the efficiency trend of the total system, efficiency maps have been produced taking into account two possible switching frequencies to be evaluated: $100kHz$ and $200kHz$. In this efficiency map, as for the analysis of power losses, other power losses other than those in the switches have not been considered. The map is represented in Fig.4.29. It is possible to analyse that the efficiency varying due to the switching frequency and the current. The $100kHz$ curve has higher values in terms of efficiency than the $200kHz$ curve. Moreover the $100kHz$ switching frequency presents a peak value above to 98.5%. For this reason, the switching frequency chosen for the multilevel inverter is $100kHz$ to stay with high efficiency percentages to have a margin on power losses in the output inductor and other power losses of the application. Furthermore, will be considered as output current a value from $10A$ to maximum $15A$ as going further, the efficiency would drop considerably.

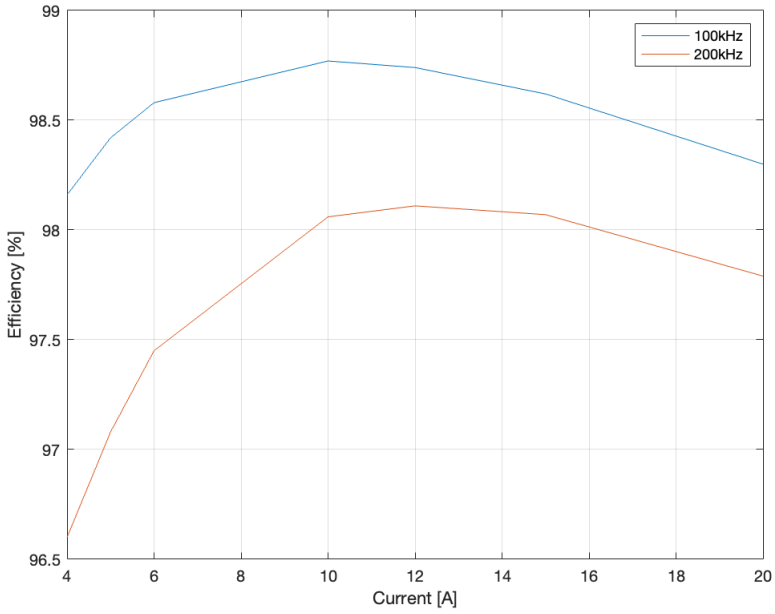
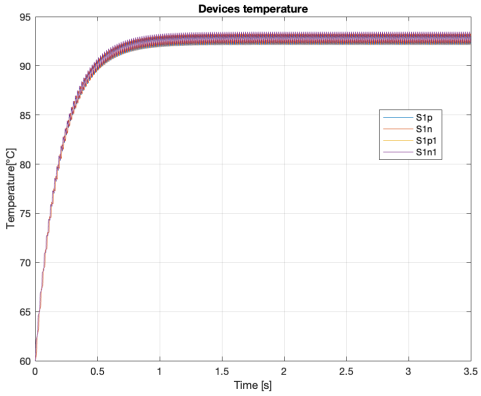


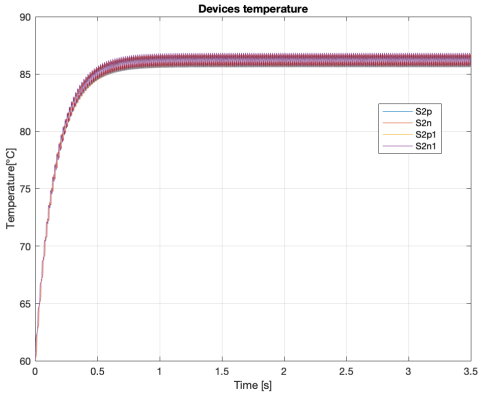
Figure 4.29: Efficiency map with two switching frequency values depending on output current of the system.

To validate the maximum output current in terms of thermal point of view simulations have been made. The thermal model in Fig.4.28 is used with a ambient temperature of $60°C$ to be consistent with the application for solar panels exposed to the sun, and an output current of $15A$ at $100kHz$ of switching frequency. The simulations results are

shown in Fig.4.30. The temperature in the four devices $S_{1..}$ is between $90°C$ and $95°C$ while the temperature in $S_{2..}$ devices is between $85°C$ and $90°C$. In both cases the temperature is consistent with the maximum temperature values allowed by the device ($150°C$).



(a) Thermal behaviour of $S_{1..}$ switches at $15A$ and $100kHz$ of switching frequency.



(b) Thermal behaviour of $S_{2..}$ switches at $15A$ and $100kHz$ of switching frequency.

Figure 4.30: Junction temperature of application devices.

4.7 Ripple Evaluation

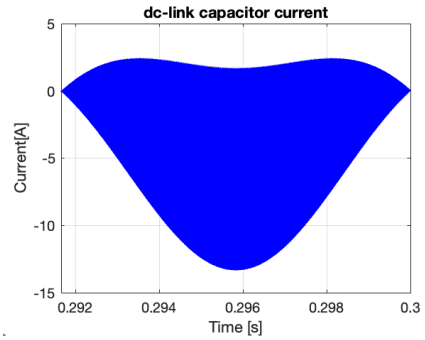
4.7.1 dc-link Capacitance

To define the analysis of dc-link voltage ripple, the system was studied with $15A$ output current, $110V_{RMS}$ output reference voltage at $60Hz$. The voltage ripple is calculated

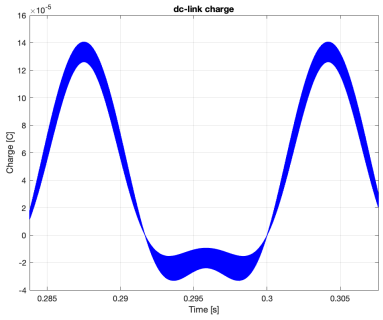
through the (4.1).

$$\Delta v = \frac{\Delta Q}{C} \tag{4.1}$$

Assuming a ripple of 2% of the input voltage, to find the correct value of dc-link capacitance, the designer has to consider the current in the dc-link and integrate it to find the charge. In Fig.4.31a is shown the dc-link current waveform. It is possible to notice how the current waveform has half time period with respect to $60Hz$ output frequency. The current has been integrated giving the waveform in Fig.4.31b. Calculating the delta of the charge and 2% of $400V$ (input voltage of the system) the capacitance result value is $21\mu F$.



(a) dc-link simulation current waveform.

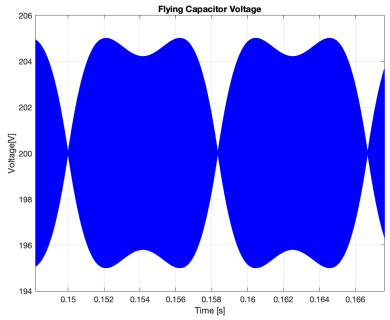


(b) dc-link charge simulation waveform.

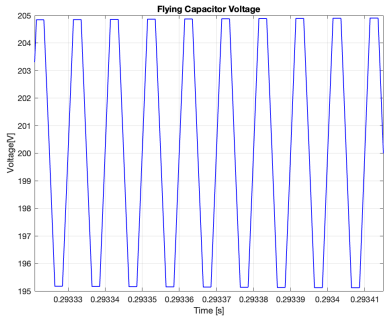
Figure 4.31: dc-link simulation results.

4.7.2 Flying Capacitor capacitance

The voltage behaviour of the flying capacitor is shown in Fig.4.32a. The voltage ripple is represented in the Fig.4.32b. The ripple of flying capacitor presents peak values which will be considered for the capacitance calculation. The ripple of the flying capacitor has a particular characteristic. It increases as the modulation index decreases. For this reason, an output voltage 90% lower than that defined for the application will be considered for the voltage ripple analysis. The output current is imposed to maximum system value of $15A$ and $60Hz$ of output frequency.



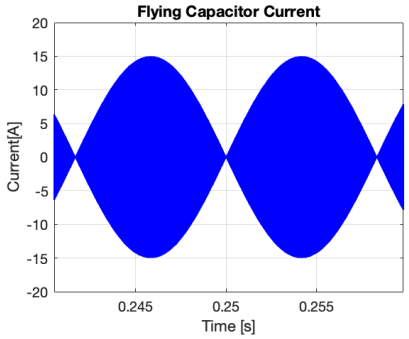
(a) Flying capacitor simulation voltage waveform.



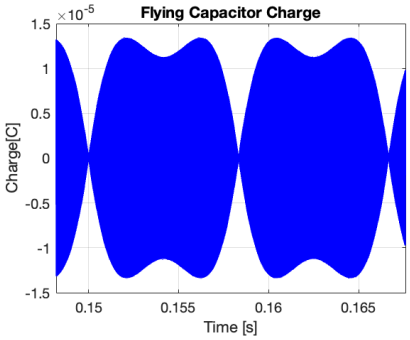
(b) Zoom of flying capacitor voltage simulation waveform.

Figure 4.32: Flying capacitor simulation waveform.

Assuming a voltage ripple of 5% of the voltage applied across the flying capacitor ($200V$), the capacitance value is defined with the eq.4.1. The flying capacitor current is shown in Fig.4.33a. Integrating the current is defined the charge of the capacitor in Fig.4.33b. Getting the ΔQ on the peak value of charge, the capacitance value of flying capacitor results $2.68\mu F$



(a) Flying capacitor simulation current waveform.



(b) Flying capacitor charge simulation waveform.

Figure 4.33: Flying capacitor simulation waveform.

4.7.3 Inductor ripple

To estimate the inductance of the phase inductor has been imposed a current ripple from 10% to 20%. For this consideration an approximation of the inductance chosen for this application could be from $50\mu H$ to $100\mu H$. With a $100\mu H$ output inductor the simulated current waveform is shown in Fig.4.34.

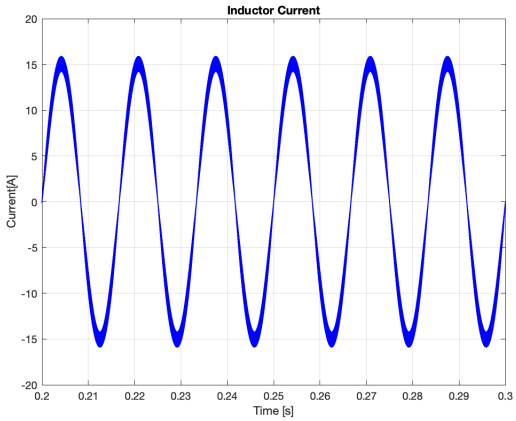


Figure 4.34: Phase inductor current.

4.8 Conclusions

The multilevel inverter GaN based for PV application designed can present the following characteristics:

- An output current from $10A$ to $15A$;
- Switching frequency of $100kHz$;
- Output Power from $800W$ to around $1kW$.

Chapter 5

Converter Schematic

5.1 Introduction

The components chosen for the flying capacitor 3-L inverter will be analysed in this chapter. The characteristics of each component will be described in order to have an idea on the realization of the application prototype. Furthermore, the schematic project (Appendix A) for the construction of a future board will be analysed.

5.2 dc-link Capacitors

The dc-link chosen structure is described in the schematic in Fig.5.1. The dc-link structure is composed by a series of capacitors to obtain the neutral point connection for the single phase multilevel converter. For this reason, the capacitance calculated in the design chapter, it will have to be doubled to have the connection in series. The hybrid structure presented in the Fig.5.1 permit to achieve roughly the desired capacitance value without having a lot of capacitors. The capacitors have been sized to sustain more than $200V$ which is the half dc-bus voltage.
The hybrid structure is composed by one electrolytic capacitor and 10 ceramic capacitors.

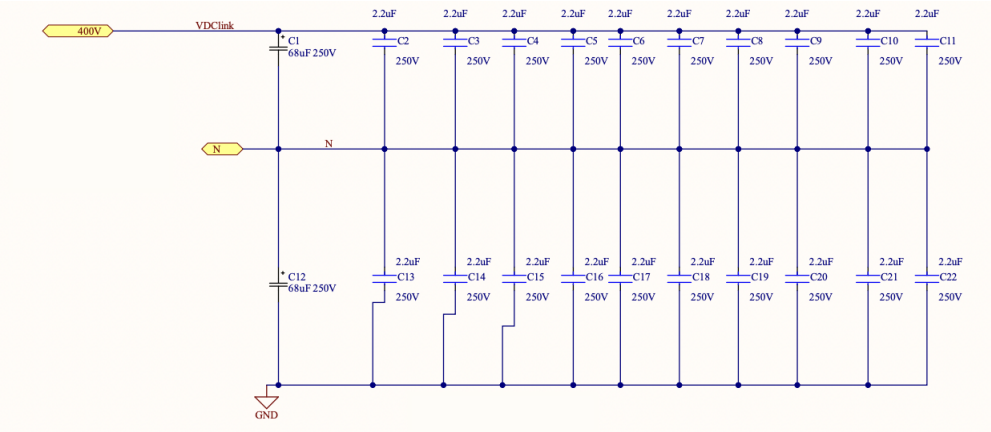


Figure 5.1: dc-link capacitors schematic.

The chosen electrolytic capacitor is a $68\mu F$ capacitor of Nichicon which of which can have an indicative example in Fig.5.2. The main characteristics of the UCY2E680MHD capacitor is described in Tab.5.1.

Figure 5.2: Example of Nichicon electrolytic capacitor.

Table 5.1: UCY2E680MHD Capacitor main characteristics.

Parameter	Value	Unit
Rated Capacitance	68	μF
Rated Voltage	250	V
Rated Current	615	mA_{RMS}

The chosen ceramic capacitors are $2.2\mu F$ capacitors of TDK. The C5750X7T2E225K250KA capacitor is shown in Fig.5.3. The main characteristics are described in Tab.5.2 and in Fig.5.4. As shown in Fig.5.4a the real capacitance at 200V is around $800nF$ due the capacitance change with increasing voltage. For this reason, the considered capacitance for this application is $800nF$. In the Fig.5.4b are shown the temperature behaviour with respect to the capacitor current. The considered curve is the red one which describe the temperature increasing with $100kHz$.

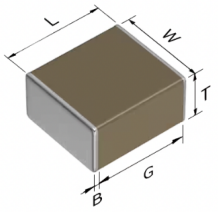
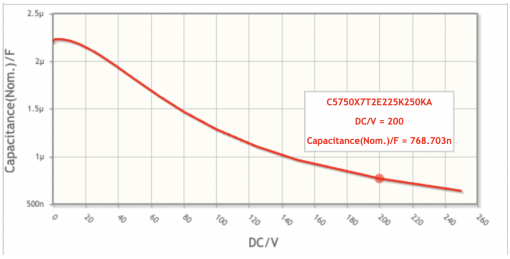


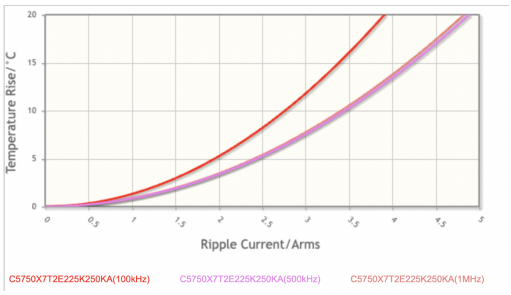
Figure 5.3: Example of TDK ceramic capacitor.

Table 5.2: C5750X7T2E225K250KA Capacitor main characteristics.

Parameter	Value	Unit
Rated Capacitance	2.2	μF
Rated Voltage	250	V
Dissipation Factor	2.5	%
Temperature Characteristic	X7T	



(a) TDK C5750X7T2E225K250KA Capacitance behaviour.



(b) TDK C5750X7T2E225K250KA.

Figure 5.4: TDK C5750X7T2E225K250KA datasheet characteristics [16].

Considering the structure in Fig.5.1 the total capacitance of the dc-link is around $38\mu F$ that is more than the capacitance value described in the design chapter. The ripple obtained with this capacitance value is less than 2%.
Through simulations in PLECS, the maximum current reached by the dc-link is $3.9A_{RMS}$ in the case in which there is a maximum output current of $15A_{peak}$. To verify if the chosen capacitors can support this current value, it is advisable to calculate the series resistances (ESR) of the capacitors. The ESR is calculated with the following equation:

$$ESR = \frac{DF}{w \cdot C} \tag{5.1}$$

In the (5.1), DF is the dissipation factor, w is the angular frequency of the system and C the capacitance. The Nichicon capacitor has $4.68m\Omega$ while the TDK capacitor

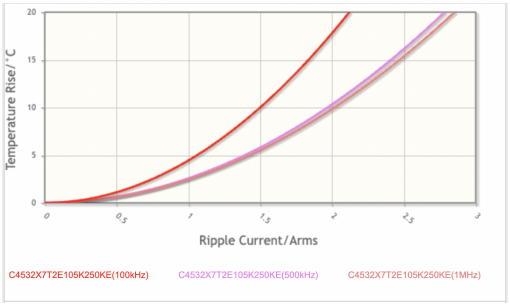
5.5$m\Omega$. Considering that there is a series connection the resistance value considered above should be multiplied by two. Furthermore, having 10 TDK capacitors per series, the total resistance must be divided by ten. With these considerations, by partitioning the current, the Nichicon capacitor will have to withstand 410mA and the remaining value will be divided on the ten TDK capacitors. Two considered capacitor can be considered suitable at these conditions.

5.3 Flying Capacitors

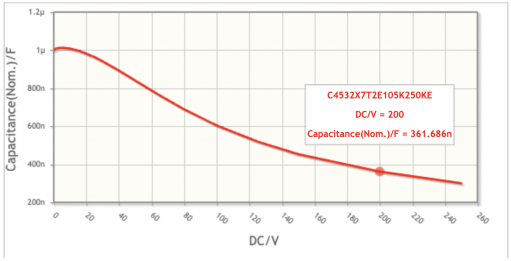
The Flying capacitor bench is composed by nine 1μF TDK C4532X7T2E105K250KE capacitors. The main characteristics of the capacitors are described in the Tab.5.3 and in the Fig.5.5.

Table 5.3: TDK C4532X7T2E105K250KE Capacitor main characteristics.

Parameter	Value	Unit
Rated Capacitance	1	μF
Rated Voltage	250	V
Dissipation Factor	2.5	%
Temperature Characteristic	X7T	



(a) TDK C4532X7T2E105K250KE current behaviour.



(b) TDK C4532X7T2E105K250KE current behaviour.

Figure 5.5: TDK C4532X7T2E105K250KE datasheet characteristics [17].

The capacitance at 200V which is the flying capacitor voltage (as described in the design chapter), is around 362nF as shown in Fig.5.5b. For this reason, with nine capacitors in parallel the total flying capacitor capacitance is more than 2.68μF obtained in the previous chapter. This means that will have a lower ripple than desired, but the capacitors will be able to support the maximum current of 7A_{RMS} obtained by simulation at a maximum output current of 15A_{peak}.

5.4 Gate Driver

The chosen gate driver is the onsemi NCP51820 gate driver. The gate driver shown in Fig.5.6 is an high-speed gate driver suitable to drive enhancement mode (e-mode) high electron mobility transistor (HEMT) and gate injection transistor (GIT), gallium nitrade (GaN) power switches in off-line, half-bridge power topologies. The NCP51820 can withstand up to $650V$ of voltage. The main characteristics are reported in Tab.5.4.

Figure 5.6: Onsemi NCP51820 gate driver.

Table 5.4: Onsemi NCP51820 gate driver main characteristics.

Parameter	**Value**	**Unit**
Recommended low-side and logic-fixed supply voltage V_{DD}	$9to17$	V
Maximum Voltage	650	V
Typical source current	1	A
Typical sink current	2	A
Low-side driver positive bias voltage output V_{DDL}	-0.3 to 5.5	V
High-side driver positive bias voltage output V_{DDH}	-0.3 to 5.5	V

The application treated in this thesis work needs three gate driver components. Two to control the switches S_{2p} and S_{1p} (Fig.4.1) and one to control the switches S_{1n} and S_{2n}. As shown in Fig.5.7, the gate driver to control S_{1n} and S_{2n} received two PWM signals from microcontroller through the two input ports H_{in} and L_{in}. The gate driver is used in d-mode connecting the DT input port to VDD which is set at $12V$. The two half bridge output ports are connected to drive the two power switches gates.

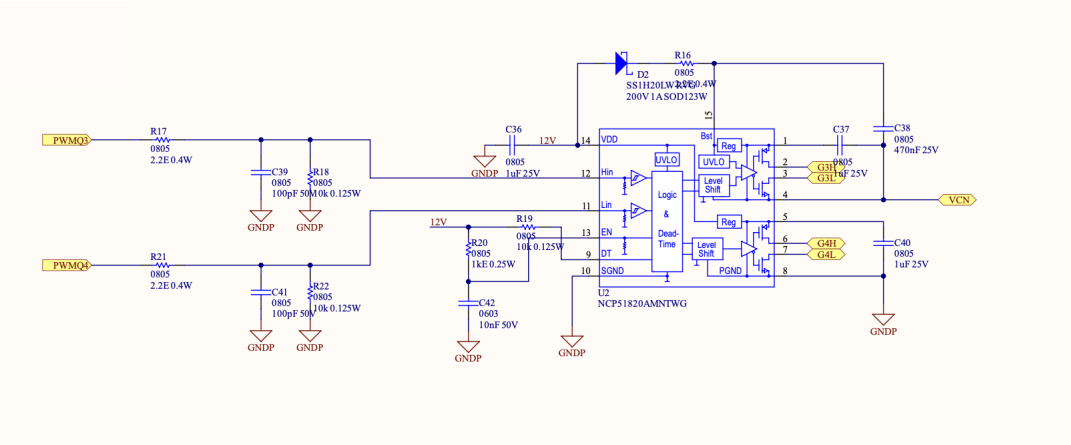


Figure 5.7: S_{1n} and S_{2n} gate driver schematic.

To drive the S_2p or S_{1p} instead a single gate driver is used. This choice was made to avoid that, if the switches are turned on together, the bootstrap is not charged and therefore the abnormal shutdown of one of the devices happens. In this case, as shown in Fig.5.8, gate driver receives a single PWM input signal. To use this gate driver to control single device, only the H_{in} input port is used. The input port L_{in} is connected to ground. As the same for the input also only the high-side output port is used and connected with power switches gates. Another difference between the is that the bootstrap capacitor in B_{st} input port, in this case, is connected to a charge pump (will be discussed in next section) which has the role of always keeping it charged and always allowing the gate driver to turn on.

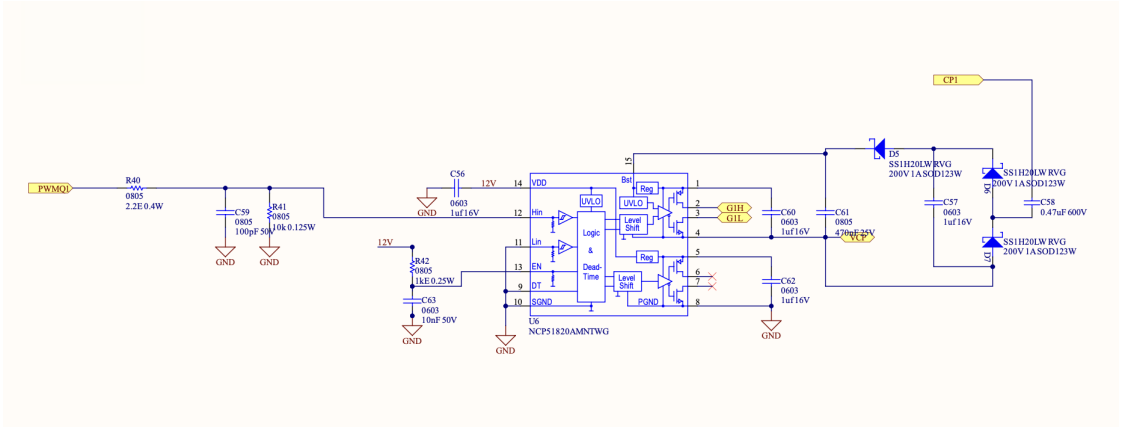


Figure 5.8: S_{2p} or S_{2n} gate driver schematic.

5.5 Capacitors pre-charge

To avoid damaging the dc-link capacitors and the flying capacitors, when switched on and off, the converter needs a discharge and charge circuit.
During the start up at first the switches S_{2p} and S_{2n} are turned-on to permit, through a soft-start resistance, to charge the flying capacitors from 0V to $200V$. After the flying capacitor reaches the desired voltage, the switches are turned off to allow charging of the dc-link up to 400V.
The shut-off is composed by two phases. At first when the dc supply is disconnected, the dc-link capacitor is discharged by a resistance connected in parallel. When the voltage of dc-link capacitors drops to $200V$, the switches S_{2p} and S_{2n} in reverse conduction mode, permit to discharge the flying capacitor which with the dc-link capacitors will be discharged to $0V$ using the resistance.
In the application case it was chosen to use a PTC to avoid the use of a relay. To choose the right component, the charge energy of the dc-link and the flying capacitor was added. The charge energy of the capacitors is described in the following equation:

$$E_C = \frac{1}{2} \cdot C \cdot V^2 \tag{5.2}$$

The E_C depends on the capacitance (C) and the square of the applied voltage (V). The total charge energy, calculated with the capacitance values discussed in the previous sections, is around $3J$.
The resistance chosen, in this application, for the charge and discharge of the capacitors is the PTC Thermistor PTCEL13R600LBE of Vishay (Fig.5.9). This thermistor is also Inrush Current Limiter and Energy Load-Dump. The main characteristics are described in the Tab.

Figure 5.9: PTC Thermistor PTCEL13R600LBE of Vishay.

5.6 Charge Pump

To supply the gate driver bootstraps of S_{2p} and S_{1p} is used a charge pump. In the Fig.5.10 is shown the schematic of the application charge pump. With SN74LVC2G14DCKR Dual Schmitt-Trigger Inverter of Texas Instrument, connects to resistances and capacitors

Table 5.5: PTC Thermistor PTCEL13R600LBE main characteristics.

Parameter	Value	Unit
V_{LINK} MAX (V_{DC})	500	V
E_{MAX} (1 CYCLE AT 25°C)	150	J
Thermal time constant	105	s
Operating temperature range	-40 to 105	°C
Dissipation Factor	14	mW/K

circuit is obtained a $300kHz$ oscillator which produces a square wave of $0-5V$. The square wave is used as the input for ST L6743BD gate driver which in turn produces a square wave of 0-12V. This square wave signal is connected at the gate driver bootstrap capacitor (CP1 port) through a capacitor. The simulated value of this capacitor is around $0.47\mu F$ as described in Fig.5.8. The charge pump system needs two different supply: $5V$ for the *Texas Instrument* component and $12V$ for the gate driver of *ST*.

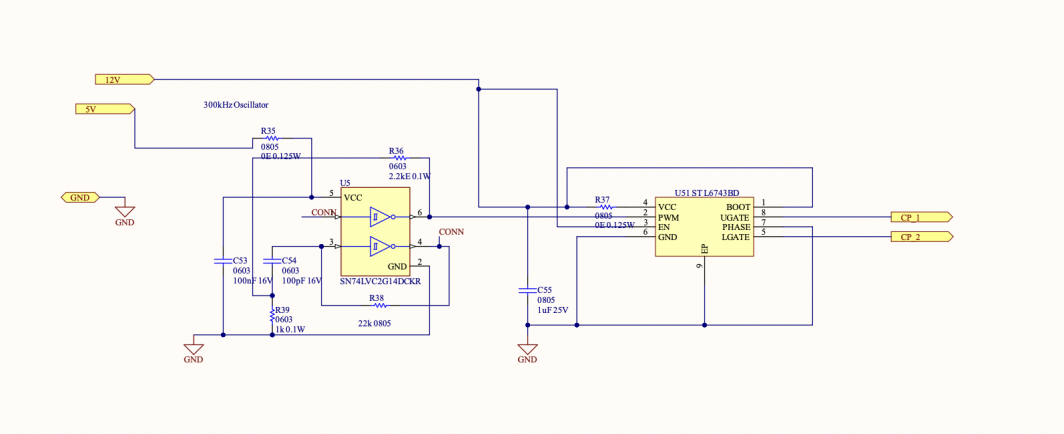


Figure 5.10: Charge Pump schematic.

5.7 Power Supplies

In this section are listed the application power supplies. The power supplies leaving aside the 400 V that will be supplied by the solar panel after a stage with a boost converter, which are used for the system have been:

- $12V$ to supply power cells gate drivers and charge pump gate driver;
- $5V$ to supply the Dual Schmitt-Trigger Inverter of Texas Instrument of the charge pump;
- $3.3V$ to supply sensing devices.

5.7.1 12 V Power Supply

To supply power cells gate drivers a 12V power supply is required. This power supply is obtained using a DC/DC converter that brings the voltage from 400V to 12V. The chosen DC/DC converter is the EPM1210SJ of *Tamura* which is shown a component example in Fig.5.11. The main characteristics are reported in the Tab.5.7. The DC/DC converter is connected to the power input of 400V.

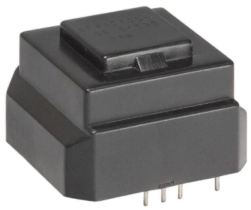


Figure 5.11: Tamura DC/DC converter example.

Table 5.6: Tamura EPM1210SJ DC/DC converter main characteristics.

Parameter	**Value**	**Unit**
Input Voltage range	110 to 450	V_DC
Rated output voltage	12	V
Rated Power	12	W

5.8 5 V Power Supply

To supply the charge pump, Dual Schmitt-Trigger Inverter of *TI*, is required 5V power supply. The circuit in Fig.5.12. From 12V, obtained by the DC/DC converter discussed above, is obtained 5V of voltage output. The 5V is obtained through the MP4581. The MP4581 is a Buck Converter of Monolithic Power Systems (MPS). The MPS converter can sustain an output voltage from 10 to 100V suitable with the 12V supplied. The output is in the range from 1V to 30V. In this case the output voltage will be used is 5V which is in the output voltage range described in the datasheet.

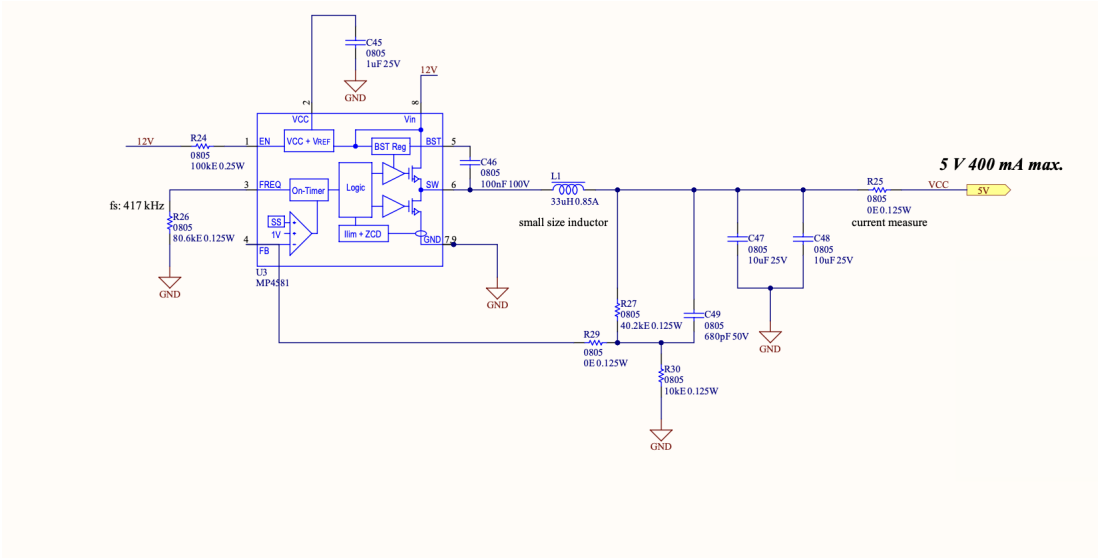


Figure 5.12: 12V to 5V circuit schematic.

5.9 3.3 V Power Supply

To supply the voltage sensing and the current sensing, need $3.3V$. For this reason, there was a need to have a power supply to get 3.3V. The Fig.5.13 shown the schematic circuit of 3.3 voltage supply. To obtain $3.3V$ from $5V$ is used a TLV75533PDRVR of *Texas Instrument* which is low-dropout regulator as described in Fig.5.13.

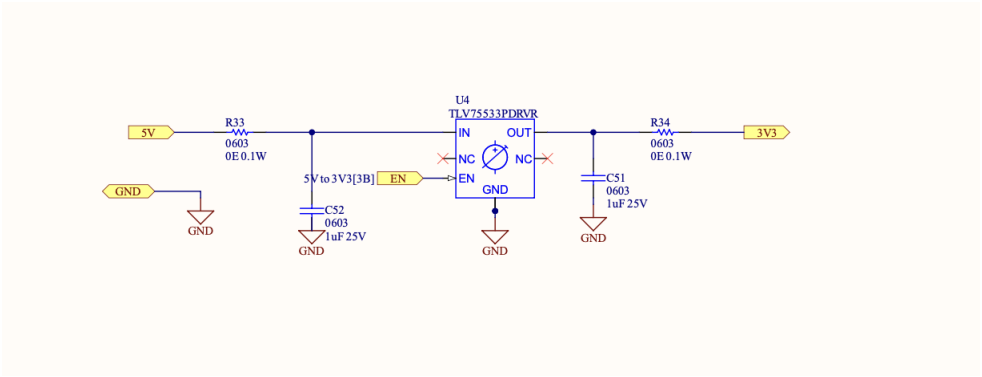


Figure 5.13: 3.3 voltage supply schematic circuit.

5.10 Sensing circuits

In this section are analysed the sensing circuits that will be used as microcontroller input signals for the system control. The sensing circuits which will be discussed are:

- Voltage sensing for dc-link, flying capacitors and phase voltage;
- Current sensing for the phase current.

5.10.1 Voltage sensing

The dc-link capacitors voltage it is important to measure to always have under control that its value is 400V which is the desired input voltage. For this reason, as shown in Fig.5.14, a voltage divider has been created. The voltage divider is composed by three resistors of $43.2k\Omega$ and one resistance of $1k\Omega$. To size the $1k\Omega$ resistance a voltage divider was made considering the maximum input voltage ($400V$) in such a way as to have, in the resistance in parallel to the output capacitor, $3.3V$ which is the maximum output measurable by the microcontroller.

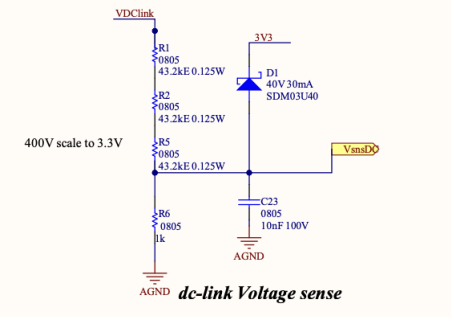


Figure 5.14: Voltage divider for dc-link voltage sensing.

The voltage sensing of the flying capacitors was realized using a differential amplifier as shown in Fig.5.15 where the input are the two flying capacitors connection nodes. At the inputs of differential amplifier circuit three resistors were chosen, two with a value of 330k and one with a value of 1k. To choose the values of the remaining resistances, the gain to be obtained at the output considering 3.3V at the output of the operational amplifier and $250V$ at the input was calculated using the eq.(5.3). To obtain the value of the resistances the gain has been multiplied by the sum of the input resistances as in the eq.(5.4) and the resulting value is $9k\Omega$. The operational amplifier used for this circuit is the OPA2365 of *Texas Instrument*.

$$G = \frac{3.3}{250} \tag{5.3}$$

$$R_7 = (330k + 330k + 1k) \cdot G \tag{5.4}$$

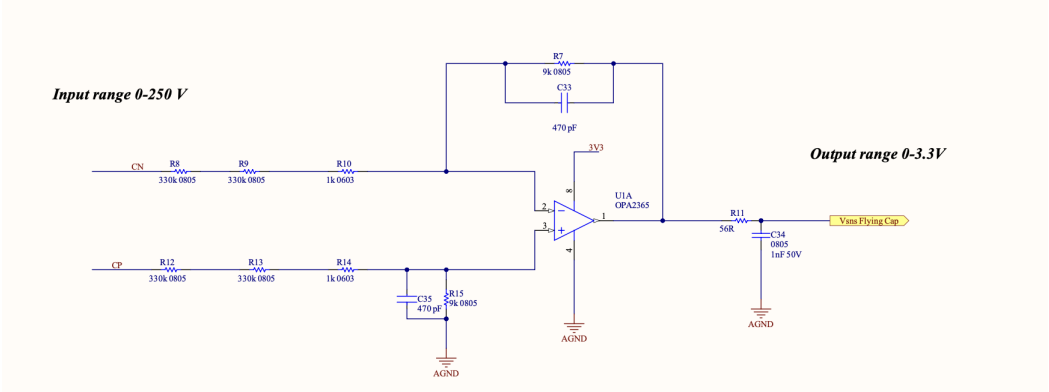


Figure 5.15: Voltage flying capacitors sensing. Differential amplifier schematic circuit.

To sense the phase voltage a differential amplifier was also created in this case. The input are connected on the phase and neutral point nodes. The possible maximum output voltage of the application, as discussed in the previous chapter, is about $110 \cdot \sqrt{2}$ of amplitude (around $156V$). For this reason, the input voltage of the differential amplifier is of 200V to have a margin. In this case, however, since the signal is sinusoidal, a level shifter must be used to make the output signal in the range of $0 - 3.3V$. The level shifter is obtained with the resistances R_{71} and R_{63}. The other resistance values are obtained likewise the flying capacitors voltage sensing considering $400V$ of voltage input. To obtain the level shifter resistances, the resistances of $5.49k\Omega$ were multiplied by two to obtain a value around $11k\Omega$.

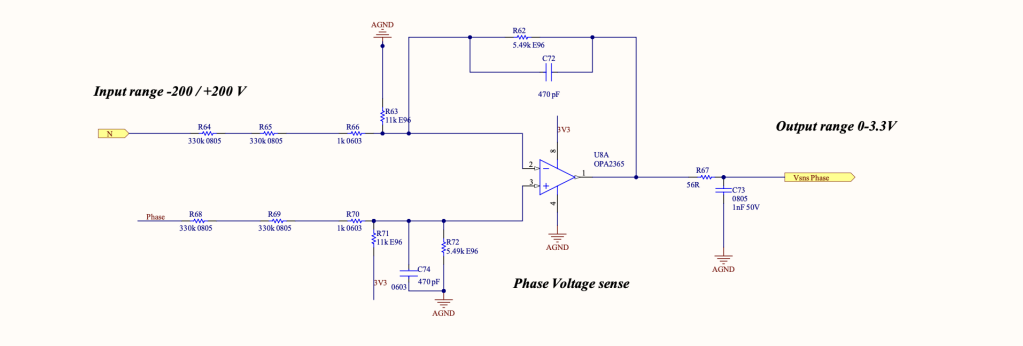


Figure 5.16: Phase voltage sensing. Differential amplifier schematic circuit.

5.11 Phase inductor

As discussed in the design chapter, the inductance value to obtain the required ripple chosen is $100\mu H$. The inductor chosen is the *CODACA* CPER3231-101MC inductor (Fig.5.17). The main characteristics of the *CODACA* inductor are reported in the Tab.**??**.

Figure 5.17: CODACA CPER3231-101MC inductor [18].

Table 5.7: Tamura EPM1210SJ DC/DC converter main characteristics.

Parameter	**Value**	**Unit**
Inductance	100	μH
Typical I_{RMS}	25	A

Chapter 6

Conclusions

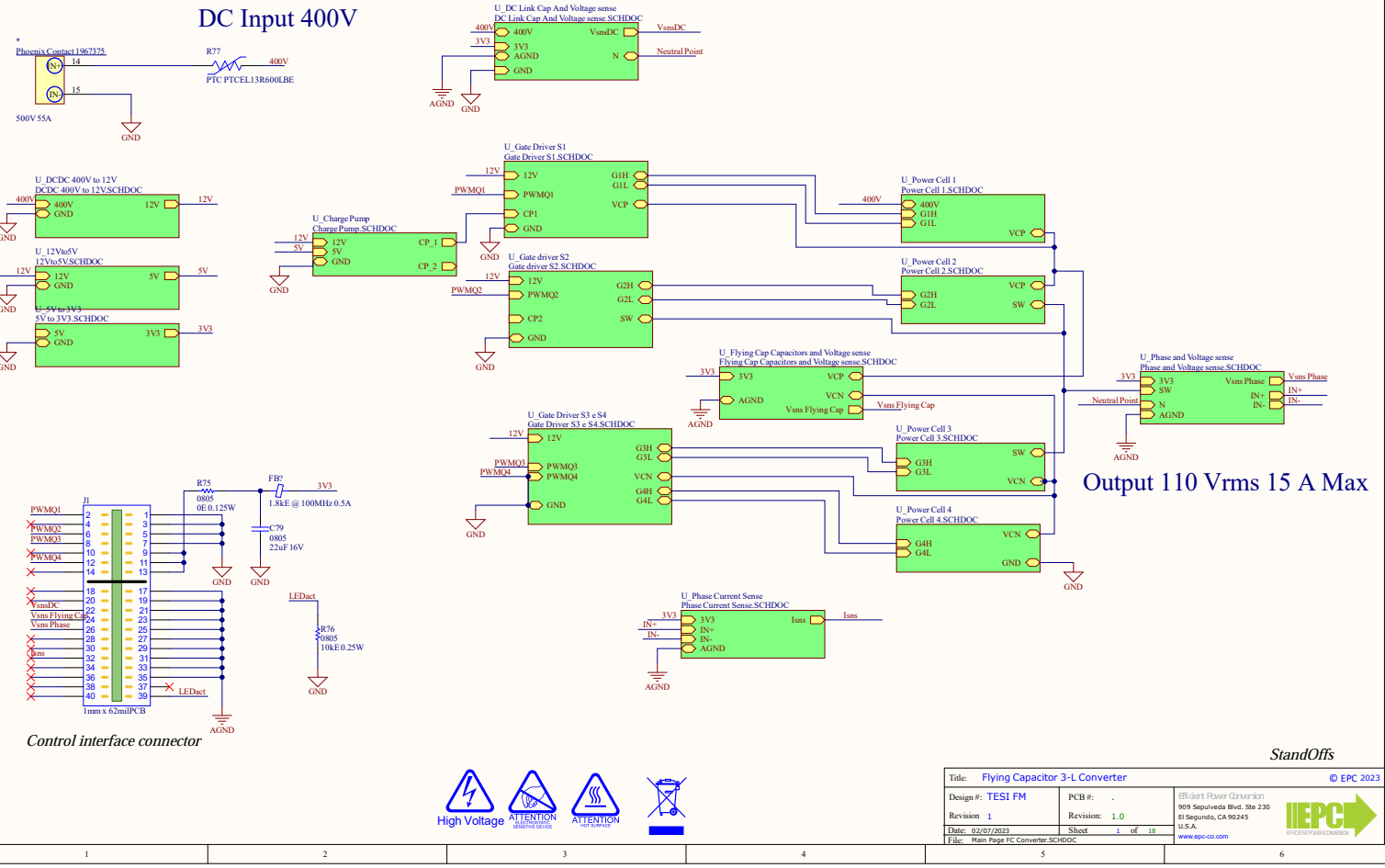
The thesis work involved designing and engineering of a flying capacitor three levels GaN based inverter for photovoltaic applications. The inverter of the application described in this thesis work is the last stage between the solar panel and the grid connection. A dc/dc converter must be provided to bring the voltage from the output voltage of the photovoltaic panel to that of the inverter's dc bus of 400V. The inverter is designed to provide an output voltage equal to the American grid voltage of $110V_{RMS}$ and with a frequency of $60Hz$.
The converter system is simulated using the LT-Spice and PLECS software. The converter can reach an output power slightly higher than $1kW$ with a maximum output current of $15A$. The last generation of WBG GaN FETs characteristics permits to increase the switching frequency of the system with an increase in system efficiency with consequent size reduction. The inverter GaN devices have very low switching losses. Two devices in parallel for each power cell has been designed to decrease the converter conduction losses.
In general my personal contributions to this thesis were:

- Study and insight into GaN transistor technology with a focus on e-mode devices;
- The Analysis of state of art of multilevel converter topologies. Different topologies comparison have been carried out to obtain the best compromise compatible with the devices of EPC source;
- Converter design through LT-Spice and PLECS environments to study electrical and thermal characteristics of the 3-L application inverter;
- Drawing of the electrical schematic of the system and overall design of the inverter in all its parts including the sizing of the components to be used.

Starting from the work described in this thesis, a prototype will be created including the layout and the experimental tests to validate the achieved target with the simulations.

Appendix A

Multilevel Converter schematics


DC Input 400V
Phoenix Contact 1967375
500V 55A
R77
PTC PTCEL13R600LBE
U_DC Link Cap And Voltage sense
DC Link Cap And Voltage sense.SCHDOC
U_DCDC 400V to 12V
DCDC 400V to 12V.SCHDOC
U_12Vto5V
12Vto5V.SCHDOC
U_5Vto3V3
5V to 3V3.SCHDOC
U_Charge Pump
Charge Pump.SCHDOC
U_Gate Driver S1
Gate Driver S1.SCHDOC
U_Gate driver S2
Gate driver S2.SCHDOC
U_Gate Driver S3 e S4
Gate Driver S3 e S4.SCHDOC
U_Power Cell 1
Power Cell 1.SCHDOC
U_Power Cell 2
Power Cell 2.SCHDOC
U_Power Cell 3
Power Cell 3.SCHDOC
U_Power Cell 4
Power Cell 4.SCHDOC
U_Flying Cap Capacitors and Voltage sense
Flying Cap Capacitors and Voltage sense.SCHDOC
U_Phase and Voltage sense
Phase and Voltage sense.SCHDOC
U_Phase Current Sense
Phase Current Sense.SCHDOC
Output 110 Vrms 15 A Max
J1
1mm x 62milPCB
Control interface connector
R75
0805
0E/0.125W
FB?
1.8kE @ 100MHz 0.5A
C79
0805
22uF 16V
R76
0805
10kE/0.25W
LEDact
StandOffs
High Voltage
ATTENTION
ATTENTION
Title: Flying Capacitor 3-L Converter
© EPC 2023
Design #: TESI FM
PCB #: .
Revision 1
Revision: 1.0
Date: 02/07/2023
Sheet 1 of 18
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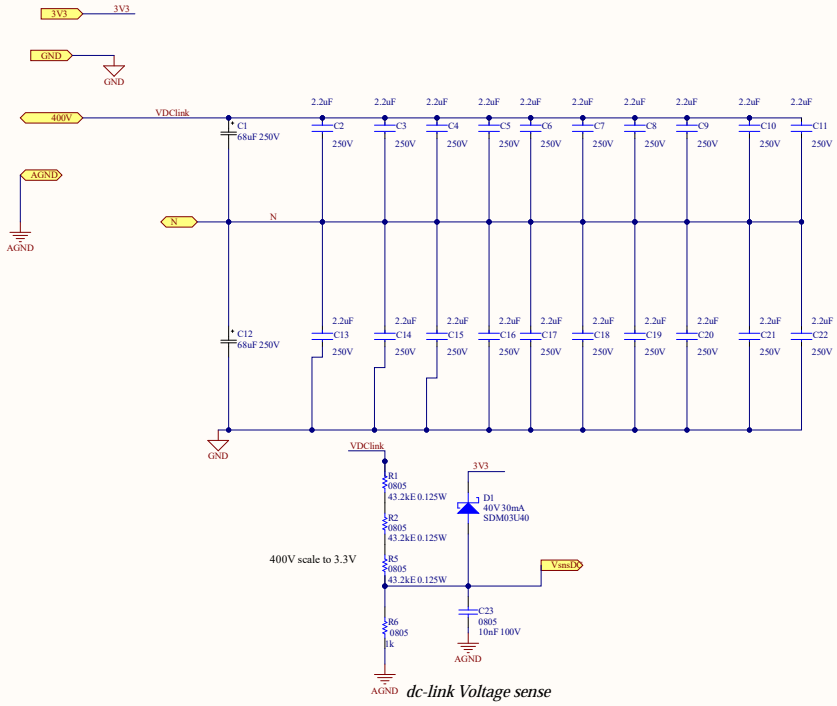
Efficient Power Conversion
909 Sepulveda Blvd. Ste 230
El Segundo, CA 90245
U.S.A.
www.epc-co.com



dc-link Voltage sense

Title: dc-link capacitor and voltage sense		© EPC 2023
Design #: .	P/N#: .	Efficient Power Conversion 909 Sepulveda Blvd. Ste 230 El Segundo, CA 90245 U.S.A. www.epc-co.com
Revision 1		
Date: 30/06/2023	Sheet 2 of 18	
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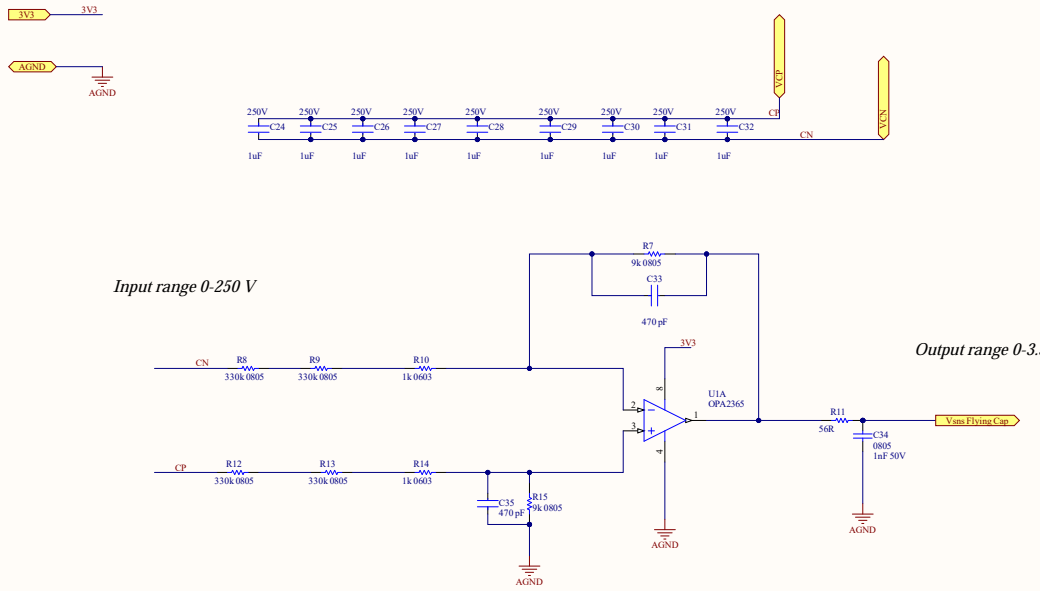

Input range 0-250 V

Output range 0-3.3V

Flying Cap Voltage sense

Title: Flying Capacitors and voltage sense		© EPC 2023
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Revision 1		
Date: 02/07/2023	Sheet 3 of 18	
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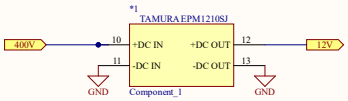
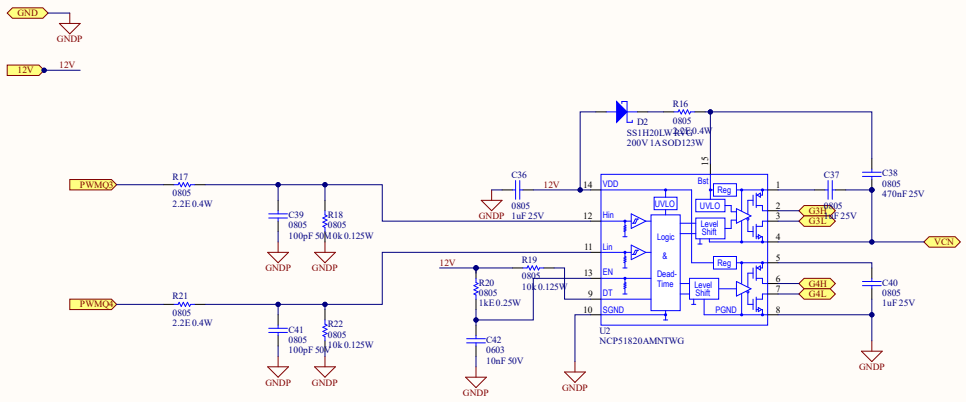
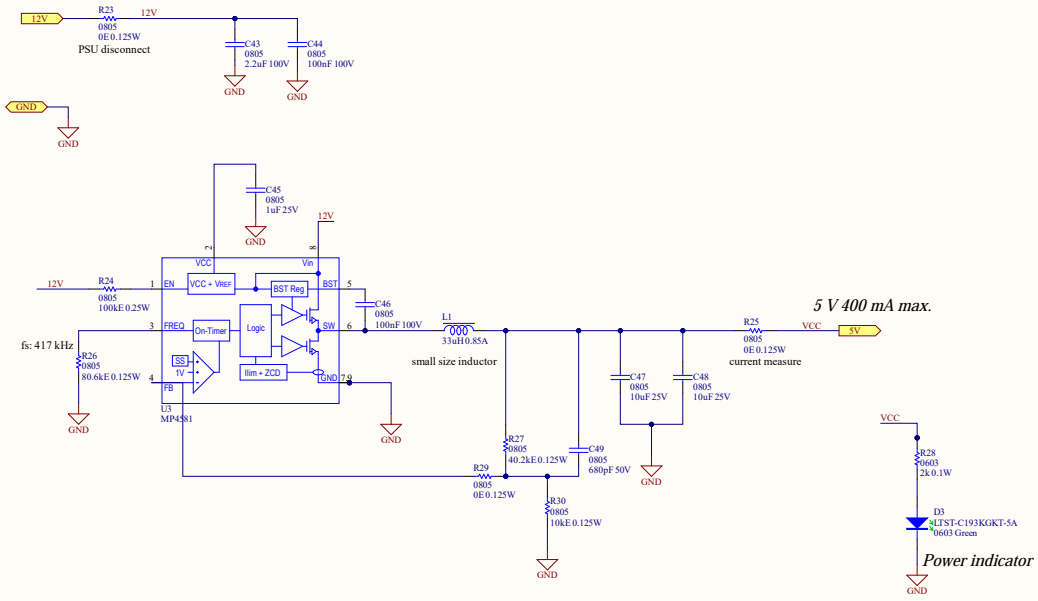


Title: dc/dc converter 400V to 12V		© EPC 2023
Design #: .	P/N#: .	Efficient Power Conversion 909 Sepulveda Blvd. Ste 230 El Segundo, CA 90245 U.S.A. www.epc-co.com
Revision 1		
Date: 02/07/2023	Sheet 4 of 18	
File: DCDC 400V to 12V.SCHDOC		



Title: Gate driver 3 e 4		© EPC 2023
Design #: .	P/N#: .	Efficient Power Conversion 909 Sepulveda Blvd. Ste 230 El Segundo, CA 90245 U.S.A. www.epc-co.com
Revision 1		
Date: 02/07/2023	Sheet 5 of 18	
File: Gate Driver S3 e S4.SCHDOC		

10 Vmin. to 100 Vmax.



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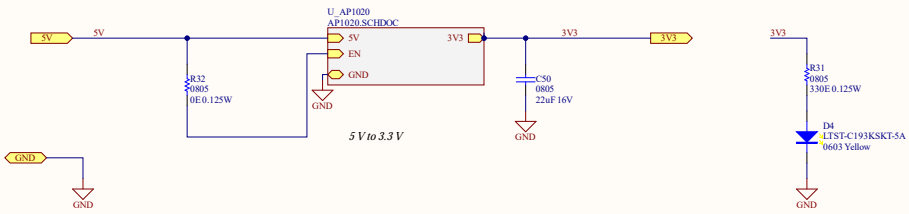
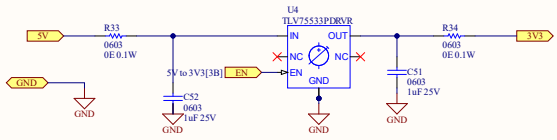
Design #: .		P/N#: .	Efficient Power Conversion 909 Sepulveda Blvd. Ste 230 El Segundo, CA 90245 U.S.A. www.epc-co.com
Revision 1			
Date: 02/07/2023	Sheet 6 of 18		
File: 12Vto5V.SCHDOC			

3V3 500 mA max.



Power indicator

Title: 5V to 3.3V		© EPC 2023
Design #: .	P/N#: .	Efficient Power Conversion 909 Sepulveda Blvd. Ste 230 El Segundo, CA 90245 U.S.A. www.epc-co.com
Revision 1		
Date: 02/07/2023	Sheet 7 of 18	
File: 5V to 3V3.SCHDOC		



Title: AP1020		© EPC 2023
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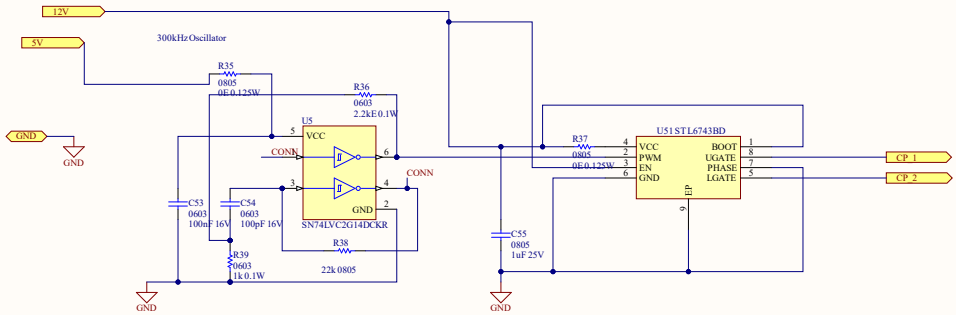
Revision 1		
Date: 02/07/2023	Sheet 8 of 18	
File: AP1020.SCHDOC		



Title: Charge pump		© EPC 2023
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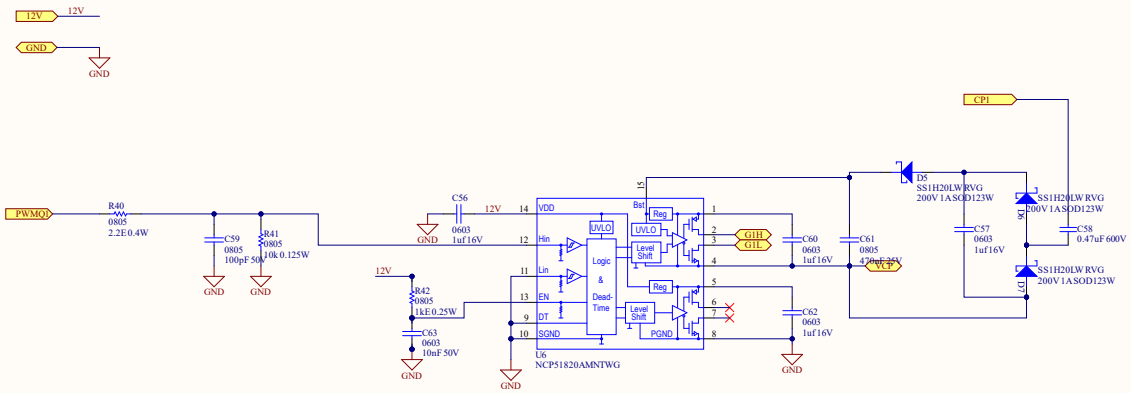
Revision 1		
Date: 02/07/2023	Sheet 9 of 18	
File: Charge Pump.SCHDOC		



Title: Gate driver 1		© EPC 2023
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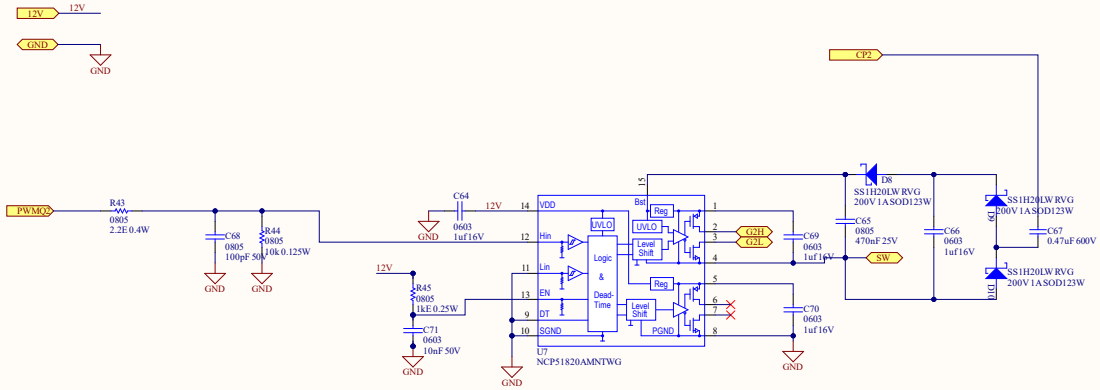
Revision 1		
Date: 02/07/2023	Sheet 10 of 18	
File: Gate Driver S1.SCHDOC		



Title: Gate driver 2		© EPC 2023
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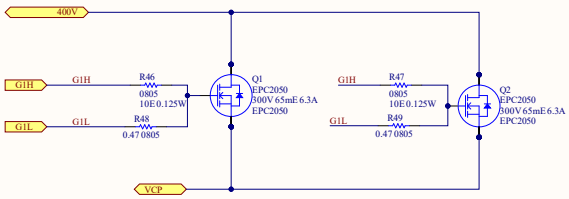
Date: 02/07/2023	Sheet 11 of 18	
File: Gate driver S2.SCHDOC		



Title: Power Cell 1		© EPC 2023
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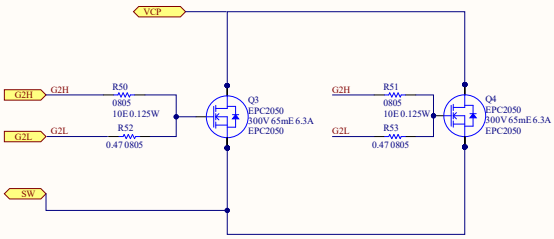
Revision 1		
Date: 02/07/2023	Sheet 12 of 18	
File: Power Cell 1.SCHDOC		



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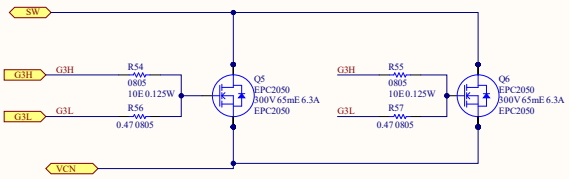
Revision 1		
Date: 02/07/2023	Sheet 13 of 18	
File: Power Cell 2.SCHDOC		



Title: Power cell 3		© EPC 2023
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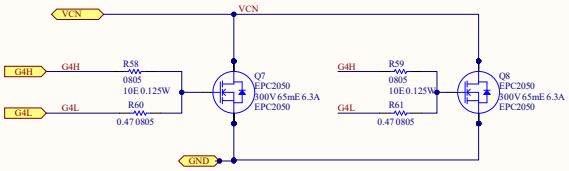
Revision 1		
Date: 02/07/2023	Sheet 14 of 18	
File: Power Cell 3.SCHDOC		



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Design #: .	P/N#: .	Efficient Power Conversion 909 Sepulveda Blvd. Ste 230 El Segundo, CA 90245 U.S.A. www.epc-co.com
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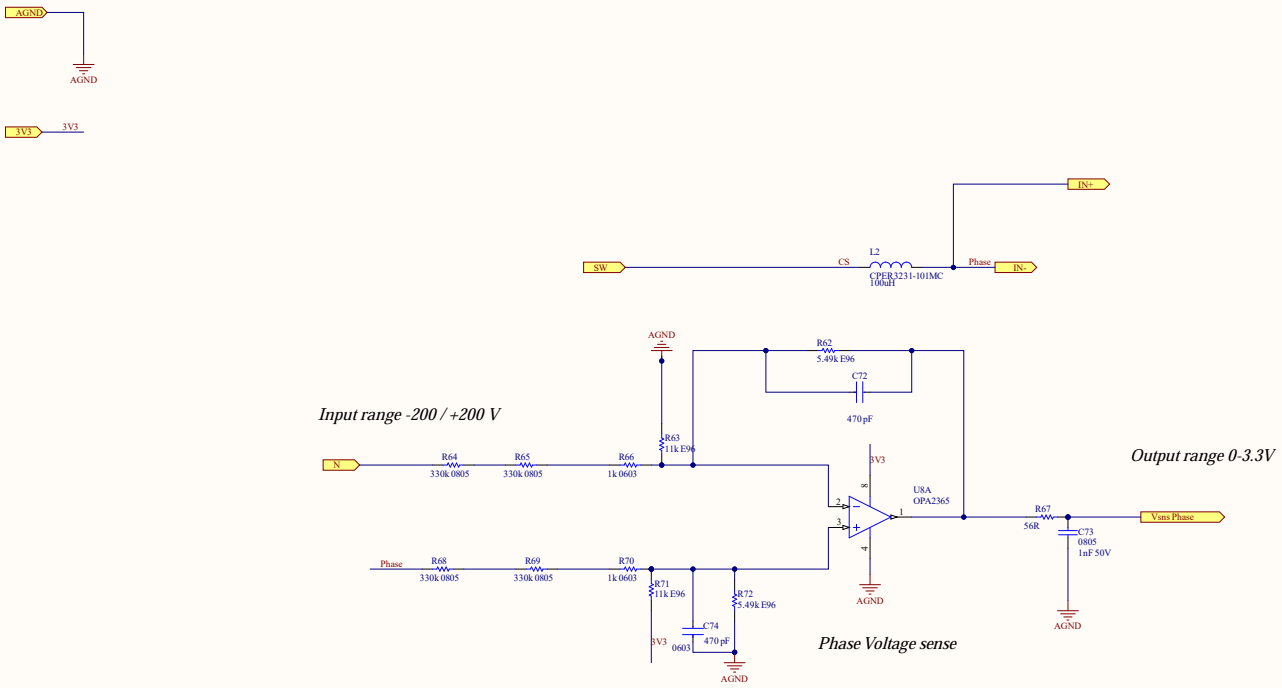
Date: 02/07/2023	Sheet 15 of 18	
File: Power Cell 4.SCHDOC		



Title: Phase and voltage sense		© EPC 2023
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Date: 02/07/2023	Sheet 16 of 18	
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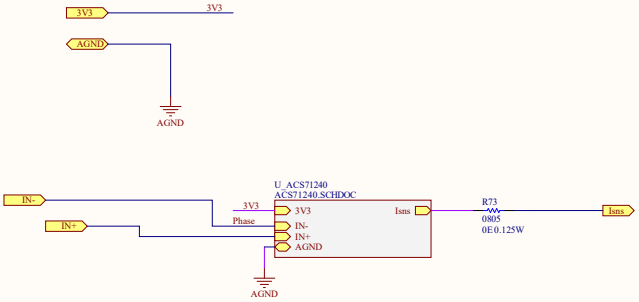

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Design #: .		P/N#: .	Efficient Power Conversion 909 Sepulveda Blvd. Ste 230 El Segundo, CA 90245 U.S.A. www.epc-co.com
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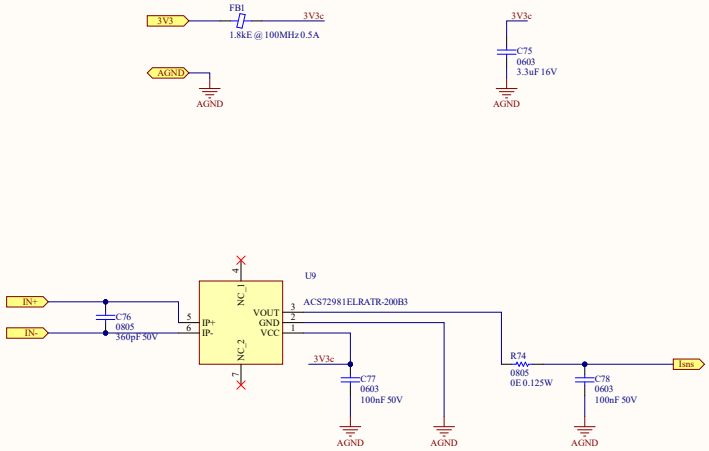
Date: 02/07/2023	Sheet 17 of 18		
File: Phase Current Sense.SCHDOC			



Title:	ACS72981ELRATR-200B3		© EPC 2023
Design #: .		P/N#: .	Efficient Power Conversion 909 Sepulveda Blvd. Ste 230 El Segundo, CA 90245 U.S.A. www.epc-co.com
Revision 1			
Date: 02/07/2023		Sheet 18 of 18	
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