POLITECNICO DI TORINO

Master's Degree in Electronic Engineering

Master's Degree Thesis

Development of a wideband MMIC Doherty Power Amplifier for 5G applications in the FR1 frequency bands

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April 2023

Summary

The power amplifier is the final stage in the transmitter chain of modern wireless communication systems and has therefore a significant impact on overall performance. Nowadays communication systems require to be compact and affordable. To accomplish this, their cooling system must be simple and small, and as a result, the power amplifier in the system should be efficient. Moreover, wireless communications evolve toward higher data rates that need wide frequency bands and high-complexity modulation schemes. These solutions lead to a high peak-to-average power ratio, which requires the communication systems to work at power levels lower than the maximum they are designed for. Therefore, the ability of a power amplifier to maintain its performance in terms of efficiency and linearity for lower power levels has become crucial. In this context, the Doherty amplifier has become one of the most popular solutions for back-off efficiency enhancement. Combining two amplifiers through a load-modulation network it can maintain high efficiency across a large power range.

The proposed thesis presents the design of an MMIC Doherty Power Amplifier for 5G applications in the FR1 frequency bands (3.3 GHz-5 GHz). The amplifier achieves 37 dBm of saturated output power and 20 dB of small-signal gain over a 41 % operating bandwidth. The minimum efficiency over a 5 dB back-off range is 25 % while efficiency at Break is equal to or larger than the saturation value. This result shows the effective efficiency enhancement behavior of the circuit. To the best of my knowledge, the designed Doherty amplifier achieves the widest bandwidth among the Monolithic integrated circuit GaN DPAs reported in the literature with a two-stage configuration and at least 37 dBm of saturated output power. The design has been carried out on a 150 nm GaN HEMT process exploiting the material's superior power density to achieve more than 5 W delivered output power in a 3.7 mm x 3.3 mm chip area. PathWave Advanced Design System has been used for circuit simulation. The design implements a two-section peaking combiner specific for wideband performance.

The present thesis work is part of a commercial project pursued by the faculty mentor and her research group on a wideband high efficiency Doherty power amplifier for FR1 bands and it constitutes the first step toward the circuit realization.

The design is being manufactured by WIN Semiconductors Corp and measurements to assess simulated results will follow. Future developments of the research project foresee addressing comprehensively the topic of load insensitivity and to investigate linearity enhancement techniques to be included in subsequent power amplifier design.

Acknowledgements

I want to express my gratitude to my supervisor, Dr. Anna Piacibello, and to Professor Vittorio Camarchia for their willingness and contagious enthusiasm in assisting me during this thesis work. I also want to thank them for the dynamic environment they created for my colleagues and myself, as well as for including me in many events that fueled my interest in the field. Thank you to my friends and to my colleagues at Politecnico di Torino. Finally, I owe my family the greatest gratitude for always supporting me during these years, as you all are my best teachers.

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Acronyms

5G	fifth-generation
ADS	advanced design system
DPA	doherty power amplifier
DRC	design rule checking
EM	electromagnetic
GaAs	gallium-arsenide
GaN	gallium-nitride
HB	harmonic balance
HEMT	high electron mobility transistor
IMN	input matching network
ISM	interstage matching network
MAG	maximum available gain
MIMO	multiple-input multiple-output
MMIC	monolithic microwave integrated circuit
MN	matching network
OBO	output power backoff
OMN	output matching network
PA	power amplifier
PAE	power added efficiency

PAPR peak-to-average power ratio

PDK process design kit

pHEMT pseudomorphic-HEMT

Psat saturated output power

QWT quarter wavelength transform

Ropt optimum load

TL transmission line

VSWR voltage standing wave ratio

Chapter 1

Introduction

The power amplifier (PA) is the final stage in the transmitter chain of modern wireless communication systems and has therefore a significant impact on overall performance. Nowadays communication systems require to be compact and affordable. To accomplish this, their cooling system must be simple and small and as a result, the PA in the system should be efficient.

Moreover, complex modulation schemes are employed in order to achieve high data rates. They lead to high peak-to-average power ratio (PAPR) signals which require the communication systems to work at power levels lower than the maximum they are designed for i.e., in back-off (see Section 1 of this Chapter for a detailed explanation). Therefore the PA in the system must be efficient not only for the power level they are designed for but in the whole back-off region. In this context, the Doherty amplifier technique [1] is one of the most popular solutions for back-off efficiency enhancement.

Another strategy used to achieve high data rates is to widen the frequency band of operation. In addition, high-performing PAs that cover many frequency bands represent a new frontier to achieve complete interoperability within contemporary communication networks [2].

In this context the proposed thesis project presents the design of an integrated doherty power amplifier (DPA) for 5G applications, addressing the challenge of designing a PA with good power and gain performance, according to the current standards, while enhancing the back-off efficiency and achieving a frequency band as wide as 41%.

The thesis content is organized as follows. In the next section of Chapter 1, some fundamentals about power amplifiers and PA figures of merit are presented as well as the main aspects of the Doherty amplifier technique. The requirements specification for the circuit design is listed in depth in Chapter 2, along with preliminary investigations on the topology and technology choices. The steps and solutions adopted for the circuit-level design are examined in detail in Chapter

3 while the layout implementation and a critical discussion on the performance are covered in Chapter 4. Finally, Chapter 5 analyzes some final circuit issues and presents some observations concerning load sensitivity and linearity while anticipating developments in the future.

1.1 Power amplifiers for RF and microwave frequencies

Figure 1.1 shows the role of a power amplifier in a transceiver as one of the last stages, right before the antenna that transmits the signal. After the information is upconverted and filtered, to avoid radiating outside the system's frequency range, the power amplifier increases the signal power to an appropriate level so that it may be sent through the antenna.

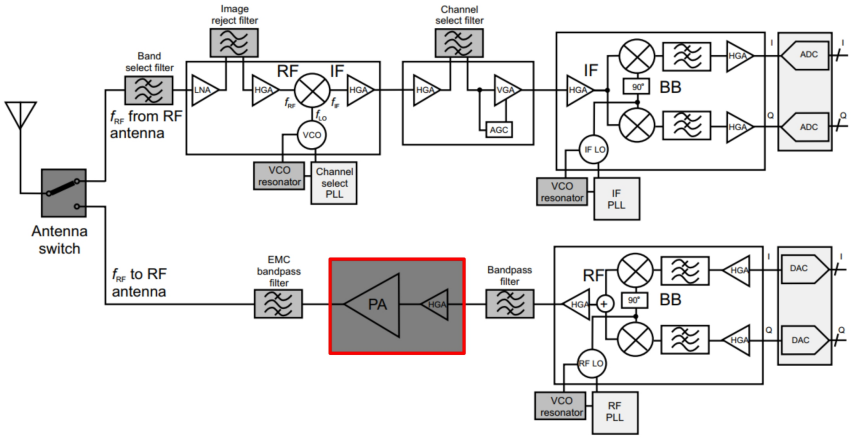

Figure 1.1: Transceiver architecture [3]

Figure 1.2 shows a typical one-stage circuit for a power amplifier: the most relevant part is an active device for microwave circuits with a common source configuration. The device is biased through Bias-Tee circuits (see Chapter 3.1.3) at the gate and drain while the information signal is provided at the input through an input matching network (IMN) and transferred at the output through an output matching network (OMN).

Power amplifiers are conventionally divided into classes. Considering a sinusoidal input signal of period T, Figure 1.3 shows that the active device is always turned on in class A, while in classes B and C, it is on only for 50% and less than 50% of the period, respectively. In these class B and C cases, the drain current swing corresponds to a set of sine pulses containing many harmonics that must be taken care of to deliver a correct output signal with suitable power, linearity, and efficiency

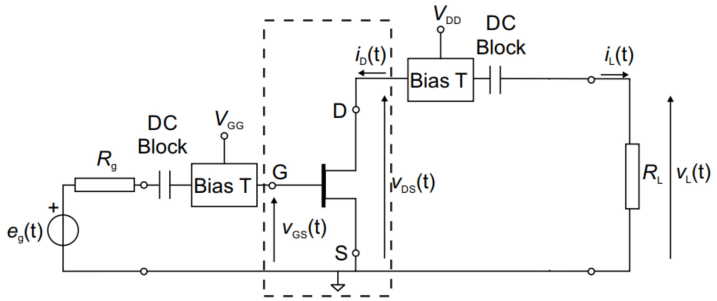

Figure 1.2: Simplified schematic of a single-device power amplifier [4].

levels. Since a transistor's turn-on is not instantaneous in real-world applications, class AB is defined as the mode in which the device is on for a duration of 50% to 100% of the time period T. Figure 1.4 shows the transcharacteristics and output characteristics of an ideal device. It illustrates the biasing conditions necessary to obtain the different PA classes.

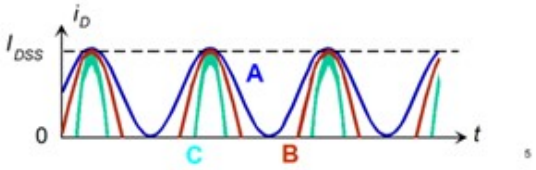

Figure 1.3: Class A, B, and C drain current [3]

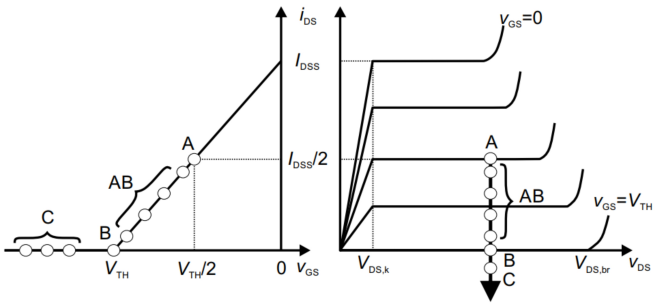

Figure 1.4: Transcharacteristics and output characteristics with bias points of different PA classes. [4]

Figure 1.5 shows some of the relevant parameters of a power amplifier, such as the output power at the fundamental frequency and the transducer gain defined as

the ratio between the output power and the available power at the fundamental (1.1).

$$G_T = \frac{P_{out}(f_0)}{P_{av}(f_0)} \tag{1.1}$$

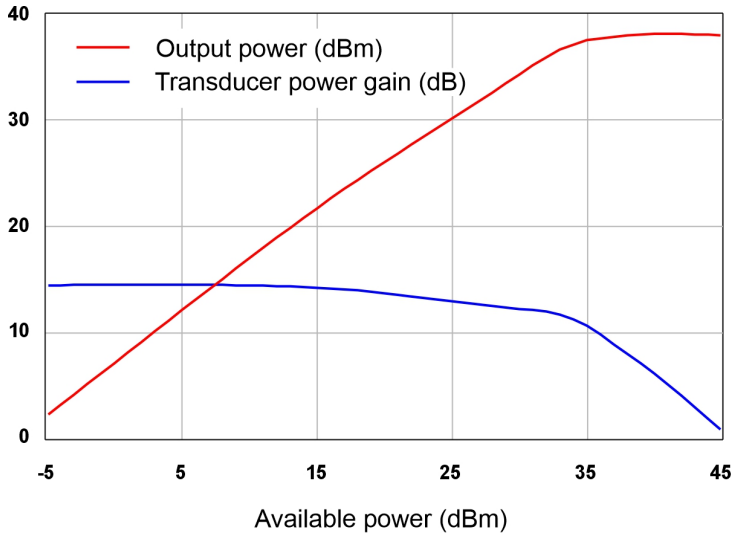

Figure 1.5: Output power (P_{out}) and transducer power gain (G_T) versus available power at the input.

As previously said, efficiency is a critical figure of merit that measures how well the PA converts DC power into RF power delivered to the load and, conversely, how much DC power is dissipated. Two main parameters are used to estimate this behavior: the efficiency, defined as the ratio between the RF output power and the DC power coming from the supply (1.2), and the power added efficiency (PAE), defined as in (1.3), that takes into account the impact of the RF input power needed to achieve the desired RF output power (i.e., it accounts for the gain of the device). Figure 1.6 shows an example of efficiency and PAE performances for a PA.

$$\eta = \frac{P_{out}(f_0)}{P_{DC}} \tag{1.2}$$

$$PAE = \frac{P_{out}(f_0) - P_{in}(f_0)}{P_{DC}} \tag{1.3}$$

Modern communication systems require complex modulation schemes to achieve high data rates. For many of these, the signals to be transmitted have a variable envelope. Since power is proportional to the square of the signal amplitude, this leads to a variable power at the input of the system. To model this behavior the

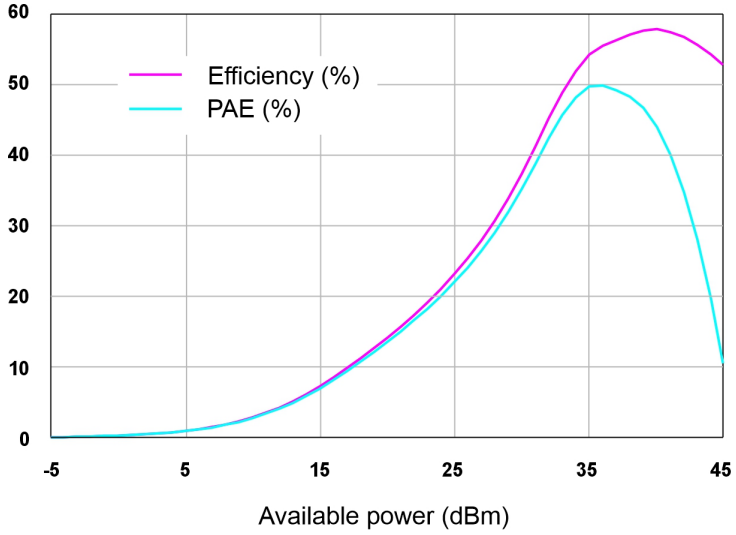

Figure 1.6: Efficiency and PAE versus available power at the input.

PAPR is introduced as the ratio between the signal instantaneous peak power and the average signal power [3].

When the input signal has a high PAPR, the PA operates at lower levels than those intended for maximum performance, which reduces efficiency among other parameters. Figure 1.7 shows an example of efficiency performance for a PA. The difference in dB between the maximum output power and the output power level corresponding to the input signal is defined as output power backoff (OBO). It can be observed how, for an increasing OBO, there is an efficiency degradation with respect to the maximum output power condition.

1.2 The Doherty Power Amplifier

Specific PA architectures have been proposed over the years to overcome the issue of the efficiency drop in back-off. These can be mainly divided into two categories, namely *load modulation* [5] and *supply modulation*. They act on the loading condition and on the supply voltage level of the PA, respectively, to maintain a high-efficiency operating condition over a given dynamic range (e.g., in a 6 dB OBO range). Among these techniques, a very popular and widely adopted solution is the Doherty PA [1].

Figure 1.8 illustrates the basic DPA architecture: it is composed of two PAs that interact in such a way as to keep the overall efficiency almost independent of the applied power in a certain back-off range. The two combined power stages are referred to as the Main (or Carrier) and the Auxiliary (or Peak) amplifier [3].

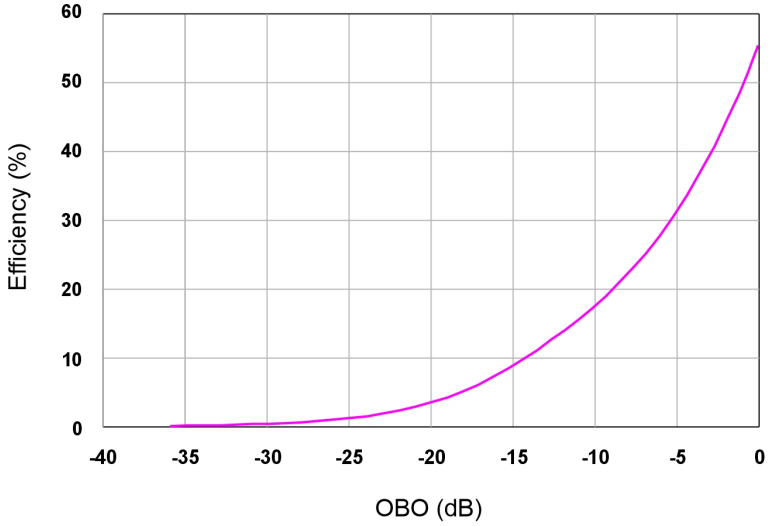

Figure 1.7: Typical behaviour of a PA efficiency performance versus OBO.

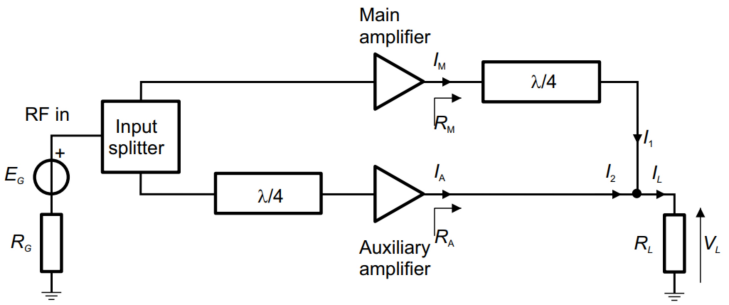

Figure 1.8: Scheme of the Doherty amplifier [3]

Before discussing the functioning of a DPA, two fundamental principles are introduced: the active load-pull principle and the load-inversion principle. The notion of active load-pull indicates the ability to change the impedance value of an RF load by injecting a current from a second, phase coherent source [5]. In Figure 1.9 two amplifiers are modeled by ideal current generators that are both connected to a resistive load. It is possible to derive (1.4), which illustrates how the resistance seen by generator #1 relies on the current injected by generator #2.

$$R_1 = R_L \frac{(I_1 + I_2)}{I_1} \tag{1.4}$$

On the other hand, the load-inversion principle derives from the transmission line (TL) theory. It illustrates that the load seen at the input of a quarter wavelength transform (QWT) is the characteristic impedance of the line (Z_0) squared, divided

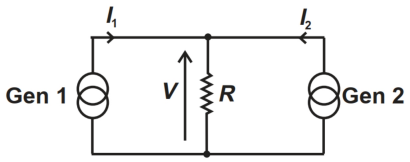

Figure 1.9: Ideal current generators (Gen) model [5]

by the load of the line (Z_L) (1.5). When this principle is applied to a TL with a characteristic impedance equal to R_L and load given by (1.4), the resistance seen at the input is (1.6).

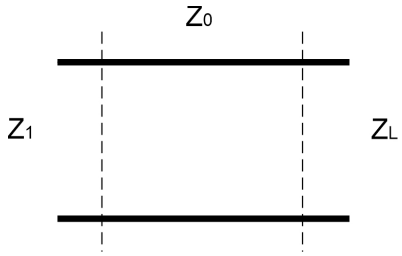

Figure 1.10: Impedance inverter quarter wavelength transform

$$Z_1 = \frac{(Z_0)^2}{Z_L} \tag{1.5}$$

$$R_1 = R_L \frac{I_1}{(I_1 + I_2)} \tag{1.6}$$

Both these principles can be now applied to the Doherty case modeled in Figure 1.11, in which the output load is connected to the Main amplifier through an impedance inverter QWT line and directly to the Auxiliary amplifier [6]. According to (1.6), the action of the Auxiliary generator is to reduce the impedance seen by the generator #1 and in the specific case of equal currents the load seen by the Main is halved.

Considering a classical 6 dB DPA, Figure 1.12 shows current and voltage behaviors for the Auxiliary and Main amplifiers. In the low-power region, corresponding to an input voltage interval (0, $\frac{V_{max}}{2}$), the Main is on, and its current amplitude increases, while the Auxiliary is off and does not inject current in the load. Therefore, the load seen by the Main is the actual load R_L. This is two times larger than the optimum load, making the Main voltage reach the maximum value for an input voltage half of the maximum input voltage swing [6].

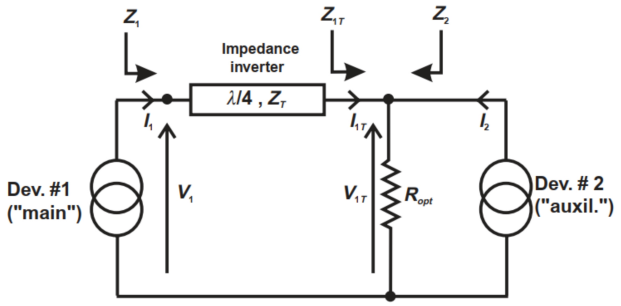

Figure 1.11: Output section of a DPA, where the active devices are modeled as ideal current generator.

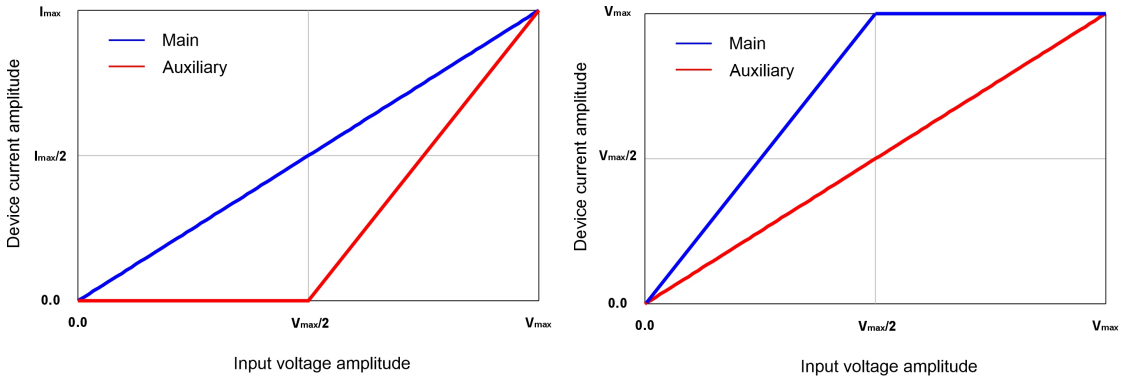

Figure 1.12: Typical current (left) and voltage (right) behavior for Main and Auxiliary amplifiers in a DPA.

With this arrangement, for an input voltage equal to $\frac{V_{max}}{2}$, the Main amplifier reaches the maximum efficiency, since both the RF output power and the DC power are halved with respect to the maximum power level.

In the high-power region ($\frac{V_{max}}{2}$, V_{max}), the Auxiliary amplifier starts conducting and it injects a current that changes the load seen by the Main, reducing it, and allowing the Main voltage swing to remain constant and maximum in the whole range [Figure 1.12]. Assuming the two amplifiers' current amplitudes are equal, at V_{max} both amplifiers reach the maximum value of efficiency. Figure 1.13 shows the efficiency curve versus input voltage: it can be seen how the maximum is reached two times, for $\frac{V_{max}}{2}$ and V_{max}, and how the efficiency remains inside an 8% variation from the maximum, in the ($\frac{V_{max}}{2}$, V_{max}) range. Note that the power level corresponding to the Auxiliary turn-on is usually referred to as "Break" or OBO, while the maximum power condition is referred to as "Saturation".

Regarding the biasing of the devices, a common choice for the Main is to choose

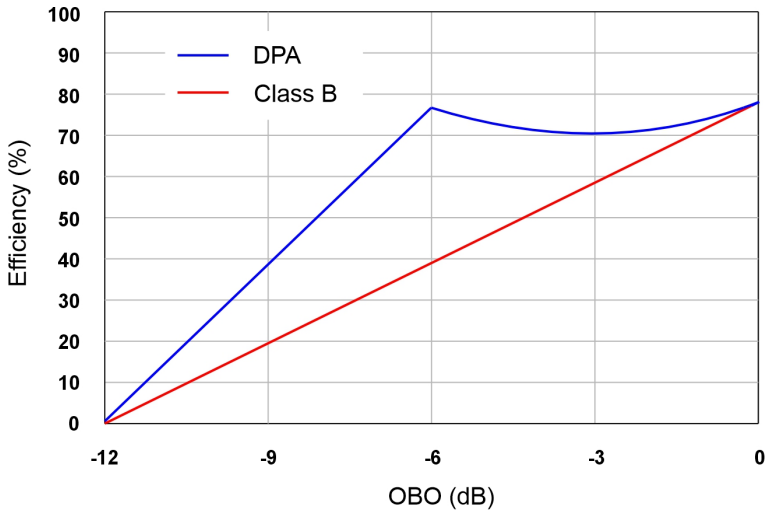

Figure 1.13: Comparison of the efficiency performance of an ideal DPA (blue) and a class B PA (red) versus OBO.

Class B or AB: this choice leads to a maximum theoretical efficiency of 78% equal to the maximum for a single-ended amplifier. On the other hand, to have the Auxiliary turn on for a higher input voltage with respect to the Main, a common choice is to bias it in Class C. Note that some specific strategies must be applied for the Auxiliary to be able to reach the same maximum current swing as the Main, despite its Class C operation. For example, a possibility is to use an Auxiliary device with twice the periphery of the Main one, for it to have double the transconductance.

Figure 1.14 summarizes the load modulation for both Main and Auxiliary devices. It can be noted how the load seen by the Main passes from two times the optimum value ($2R_{opt}$) at Break, to the R_{opt} at Saturation. On the other hand, the load seen by the Auxiliary passes from an ideally infinite value before the Break, when the device is still off, to the optimum value R_{opt}.

In Figure 1.8 it can be seen that, to complete the scheme of a DPA, a QWT is introduced before the Auxiliary device to add a 90° phase delay and compensate the phase difference between the amplifiers introduced by the impedance inverter QWT. As a result, the signals at the load are coherent in phase. At the input of a 6 dB DPA, an even power splitter is used to equally divide the power between the two branches.

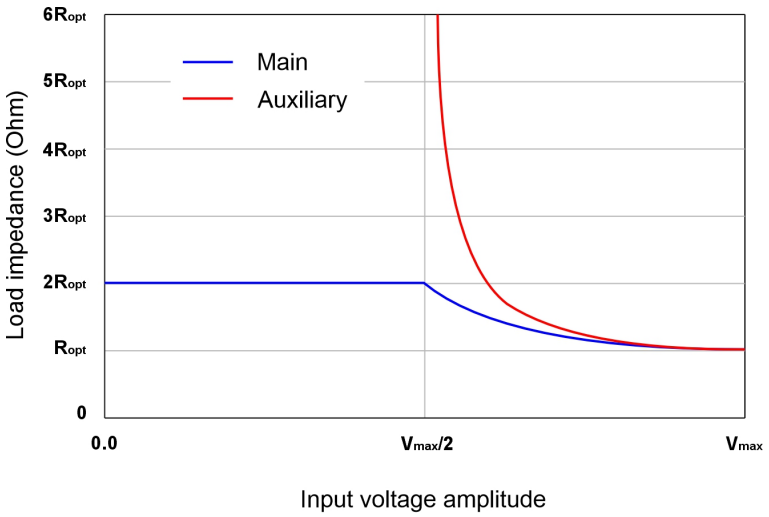

Figure 1.14: Load modulation for Main and Auxiliary.

Chapter 2

Requirements specification

This chapter is devoted to the specification of the requirements fixed by the commercial project from which this thesis work was generated and to illustrate the preliminary steps of the design activity, i.e., the selection of the technology, with a focus on two alternatives gallium-arsenide (GaAs) and gallium-nitride (GaN), and the determination of the power budget.

First, the main project requirements are specified and a subset of these is derived, which is going to be addressed by the present thesis. In fact, the project requirements are well above the present state of the art and require a degree of experience that are beyond the target of a MSc thesis, hence the need of deriving a set of specifications to address initially. Further work aimed at the achievement of the full set of specifications is going to be developed over a 2-year time span by a team of designers in this research group.

2.1 Target performance

In Table 2.1, the target performance set by the project specifications is summarized, focusing on the following parameters: frequency of operation, gain, saturated output power (Psat), efficiency, OBO, voltage standing wave ratio (VSWR), and chip area.

Frequency	Gain	Psat	Efficiency	OBO	VSWR	Chip area
(3.3-5) GHz	20 dB	37 dBm	Best effort	5 dB	2.5:1	3.7mm x 3.3mm

Table 2.1: Target performance based on the project specifications

The proposed thesis activity focuses on the design of a DPA for 5G applications in the FR1 frequency bands N77 (3.3-4.2) GHz and N79 (4.4-5) GHz. Since it is

chosen to design a wideband DPA, rather than a dual-band DPA covering the two non-adjacent bands separately, these frequencies lead to a working bandwidth of 41%, estimated considering a (3.3-5) GHz frequency range and 4.15 GHz center band frequency.

The required small signal gain is at least 20 dB. This implies the use of on-chip drivers, since the transistors for power applications at microwave frequencies usually have limited gain.

The minimum saturated output power of 37 dBm corresponds to 5 W.

A relatively uniform efficiency performance should be maintained over a 5 dB OBO range, justifying the choice of a Doherty configuration. To the best of my knowledge, no design examples have been found in the literature fulfilling all the specifications of the present project. Some examples for single-stage amplifiers are listed in [7, 8, 9, 10, 11, 12, 13, 14]. Given the challenging requirements, no further complexity has been added by specifying a minimum efficiency.

VSWR tolerance specification refers to insensitivity to load variations. This is currently a hot topic in PA design techniques for fifth-generation (5G) communication systems since the exploitation of massive multiple-input multiple-output (MIMO) envisages up to hundreds of antennas. The element-to-element coupling of the antennas causes large impedance variations i.e., VSWR variations and Doherty output power and power added efficiency performances are often drastically degraded even under moderate antenna VSWR variation [15]. Since load mismatch insensitivity is currently an open research topic with no well-established solution at monolithic microwave integrated circuit (MMIC) level, a two-step approach is followed. The designed MMIC DPA is developed trying to maximize the performance in ideal output-matching conditions. Subsequently, the possibility to implement a load-insensitive variant with the adoption of a balanced structure [16, 15] is investigated.

The design is being manufactured by WIN Semiconductors Corp. [17]. Due to some constraint imposed by the foundry for the multi-project wafer realization, the provided dimensions for the circuit layout are 3.7mm x 3.3mm.

2.2 Technology and topology selection

Two technologies have been initially considered: a GaN/SiC high electron mobility transistor (HEMT) process and a GaAs pseudomorphic-HEMT (pHEMT) process, both with 0.15 μm gate length. The considerations detailed below have led to the choice of the GaN/SiC for the technology and a 6 dB Doherty configuration [5][Figure 2.1] with individual final stage devices for the topology.

GaN-based active devices have demonstrated excellent power density capabilities over the last few decades, outperforming GaAs devices by approximately one order

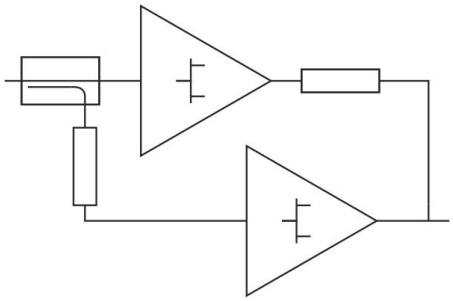

Figure 2.1: Simple Doherty topology with individual devices, suitable to achieve the target output power in GaN.

of magnitude up to millimeter waves. Figure 2.2 shows the power sweep for a 10x100 μm device in the selected process, resulting in 36.4 dBm saturated output power. Combining two of these devices in a Doherty configuration is enough to provide the target 37 dBm Psat without the need for further power combination, leading to the simplest topology for the DPA. On the other hand, the lower power density of GaAs makes it necessary to use more complex topologies, such as the ones in Figure 2.3 where two DPA cells are combined in parallel, to reach the same 37 dBm target output power level.

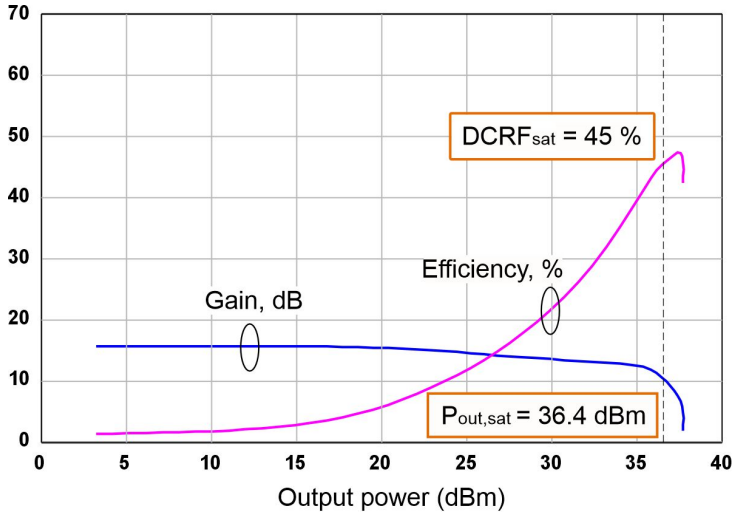

Figure 2.2: Simulated large signal performance of the (10x100μm) device in the GaN/SiC process.

Another characteristic of GaN is the high 28 V dc-supply voltage, with respect to the 6 V dc-supply of GaAs, which results in higher load impedance beneficial for wide bandwidth designs.

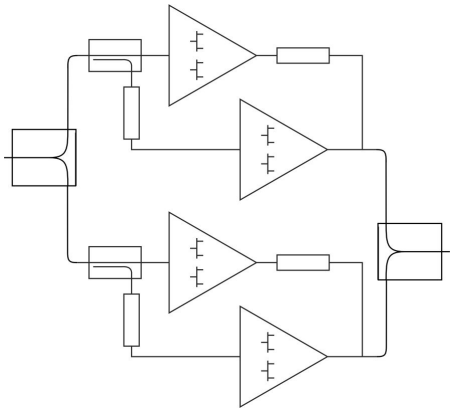

Figure 2.3: Combined Doherty topology, required to achieve high output power in GaAs.

Figures 2.4 and 2.5 show a comparison between the performance of GaN and GaAs transistors whose size allows to achieve the output power levels compatible with the topologies of Figures 2.1 and 2.3, respectively. It can be observed that GaAs has higher (60 %) efficiency compared to GaN (46 %) and also a higher gain at saturation (13 dB versus 9 dB). However, the reduced GaN performance is most likely compensated by the higher power density and topology simplicity. The additional power combination required in GaAs and the related losses would cause a significant drop in the efficiency of the overall MMIC PA, reducing or possibly canceling the advantage observed at the device level.

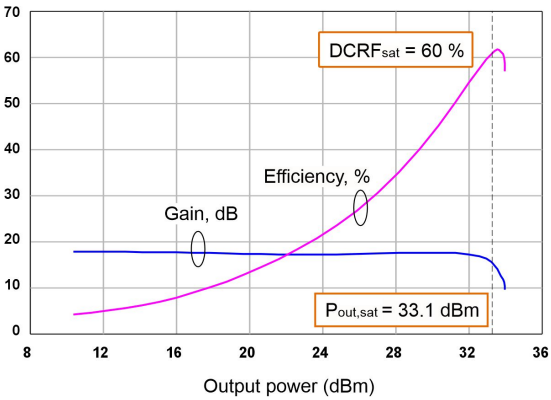

Figure 2.4: 2x(8x150μm) GaAs device simulated large signal performance

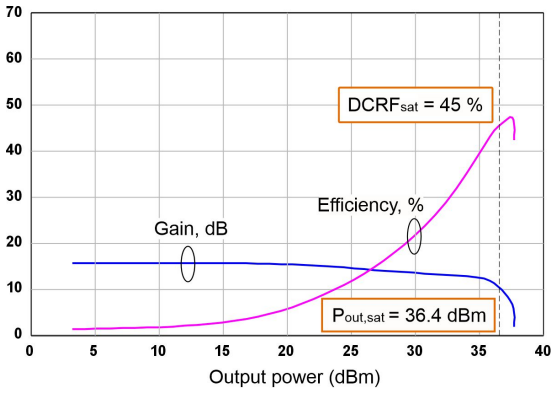

Figure 2.5: (10x100μm) GaN device simulated large signal performance

A further consideration that favors GaN is that the provided metal layers for

layout realization are two for both technologies. Therefore, the implementation of metal connections for power combination and bias lines must be carried out carefully and a simple topology such as the one in Figure 2.1 is an advantage. Furthermore, a simpler routing of the bias lines reduces the risk of oscillations due to coupling effects and internal loops.

The provided considerations led to the choice of the 0.15 μm gate-length GaN/SiC HEMT process as technology. For the present design, the classical 6 dB Doherty topology with equal input power splitting, introduced in Chapter 1, has been chosen. It can leave some margin in the face of the required 5 dB OBO and, as a further advantage, it can be implemented using the same transistor size for the Main and Auxiliary amplifiers.

2.3 Transistor size determination

In the selected Doherty topology, each transistor must provide half of the required output power. The required Psat of 37 dBm is increased by 2 dBm to have a margin for losses and variation from peak performance over the band, resulting in 39 dBm of target output power. Each transistor must then deliver at least 36 dBm output power. Table 2.2 summarizes the requirements for the final stage transistor.

Psat [dBm]	Gain [dB]	Efficiency [%]
36	10	Best effort

Table 2.2: Final stage active device requirements

First, the smallest device available in the library with dimensions of 4 fingers x 50 μm width is studied with DC, small-signal, and harmonic balance (HB) simulations to evaluate its output power and to estimate how much larger the final device needs to be to meet the required power specifications. A preliminary study on such a device allows for a check of the simulated results against those provided in the process design kit (PDK) confidential documentation, where simulations-measurements comparisons are also shown. The results comply with the documentation and result in a 29.6 dBm Psat. A power increase of about a factor 4 i.e., 6 dB is then estimated to meet the target 36 dBm Psat.

Two different devices with dimensions 8x100 μm and 10x100 μm are then evaluated. The same procedure as the 4x50 μm transistor is applied with DC, small-signal, and HB simulations. In Table 2.3 the results of the HB simulation and a preliminary load-line evaluation over the (3.3-5) GHz bandwidth are shown: note that the minimum value over the bandwidth is listed for each performance parameter.

Device dimensions	Psat [dBm]	Gain @sat [dB]	Ropt [Ω]	Efficiency [%]
8x100 μm	35.1	9.2	70	46.4
10x100 μm	36.4	8.7	60	42.6

Table 2.3: Simulated large signal performance of the considered active devices

The 10x100 μm transistor is providing 36.4 dBm of Psat versus the 35.1 dBm of the 8x100 μm, with comparable saturation gain of 8.7 dB and 9.2 dB, respectively, and comparable efficiency of order of 40%. Eventually, the 10x100 μm solution is chosen due to its higher Psat, which gives a further 1.3 dBm of output power margin to compensate for the losses. It also provides an optimum load closer to the RF standard 50 Ω, which can be beneficial for the subsequent synthesis of wideband matching and combining networks.

Chapter 3

Design

The design flow is described in detail in this chapter. A summary of the design procedure is the following. First, the final stage of the DPA is addressed: the gate and drain bias point are selected, the transistor is stabilized, and the optimum load is determined. Secondly, the driver stage is developed following a procedure analogous to the final stage. The optimum load information is used to design the interstage matching network (ISM), between the driver and final stage, and the IMN, at the input of the driver stage. Later, the combiner is designed: the topology is chosen, the parameters of the transmission lines are determined, the combiner is optimized, and the parasitic compensation is embedded in it. The previous subcircuits are assembled in the DPA topology and the bias of the auxiliary branch is determined. The DPA circuit is simulated and optimized for performance improvement. The input power splitter is finally added, and the circuit is inspected for gain control outside the bandwidth and stability.

3.1 Active Devices' study

3.1.1 Bias point selection

A DC simulation is performed by sweeping the gate voltage between -3 and 1 V and the drain voltage between 0 and 60 V. Ideal bias networks are used at the input and output of the device, since at this stage a performance estimation is sufficient. The results are shown in Figure 3.1

The drain terminal is biased at 28 V as suggested by the foundry for high-power applications. Regarding the gate bias, in Chapter 1 it has been expressed the need for a Class B amplifier in the Main branch of a DPA. According to theory [5] Class B amplifiers foresee biasing the gate of the amplifier in correspondence with the turn-on of the transistor. Since real transistors do not have a sharp turn-on, an

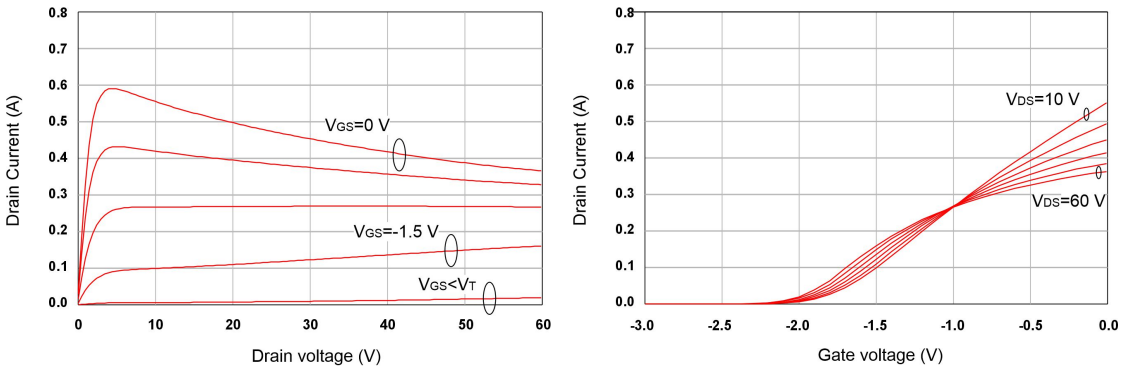

Figure 3.1: Output (left) and transfer (right) DC IV characteristics of the (10x100 μm) transistor

interval of voltages is identified in (-1.9, -1.5) V corresponding to (4, 26) % of the maximum current. HB simulations are performed with variable gate bias in the selected range: results show that over the bandwidth the efficiency is in the range (42, 52) % for all gate bias while the gain changes considerably from 9 dB to 16 dB respectively at gate bias -1.9 V and -1.5 V, in agreement with the 6 dB gain loss of Class B with respect to Class A.

An intermediate bias of 12% of the maximum current, corresponding to -1.7 V, is selected granting a small signal gain in the range (13.9, 14.9) dB over the bandwidth.

3.1.2 Stabilization

The device needs to be stabilized while making the gain as high as possible and flat over the target bandwidth (3.3-5) GHz.

The one-parameter stability criterion illustrated in [3] is applied: the parameter *mu* is evaluated in a small signal simulation, and it is required to be larger than 1 for unconditional stability. Figure 3.2(a) (blue curve) shows the device before stabilization: it is not unconditionally stable, with *mu* lower than 1, both in-band and outside the band. Note that the graph presents a logarithmic scale therefore the mu parameter can be observed as lower than 0 dB.

Figure 3.2(b) (blue curve) shows the maximum available gain (MAG) parameter graph for the potentially unstable device. It can be observed the device has a gain larger than 0 dB up to 60 GHz. Therefore, the stability is imposed in the whole frequency range (0-60) GHz to prevent oscillations.

It is well known that a transistor can be stabilized by adding resistors at its input and that adding reactive elements the frequency at which the stabilization takes

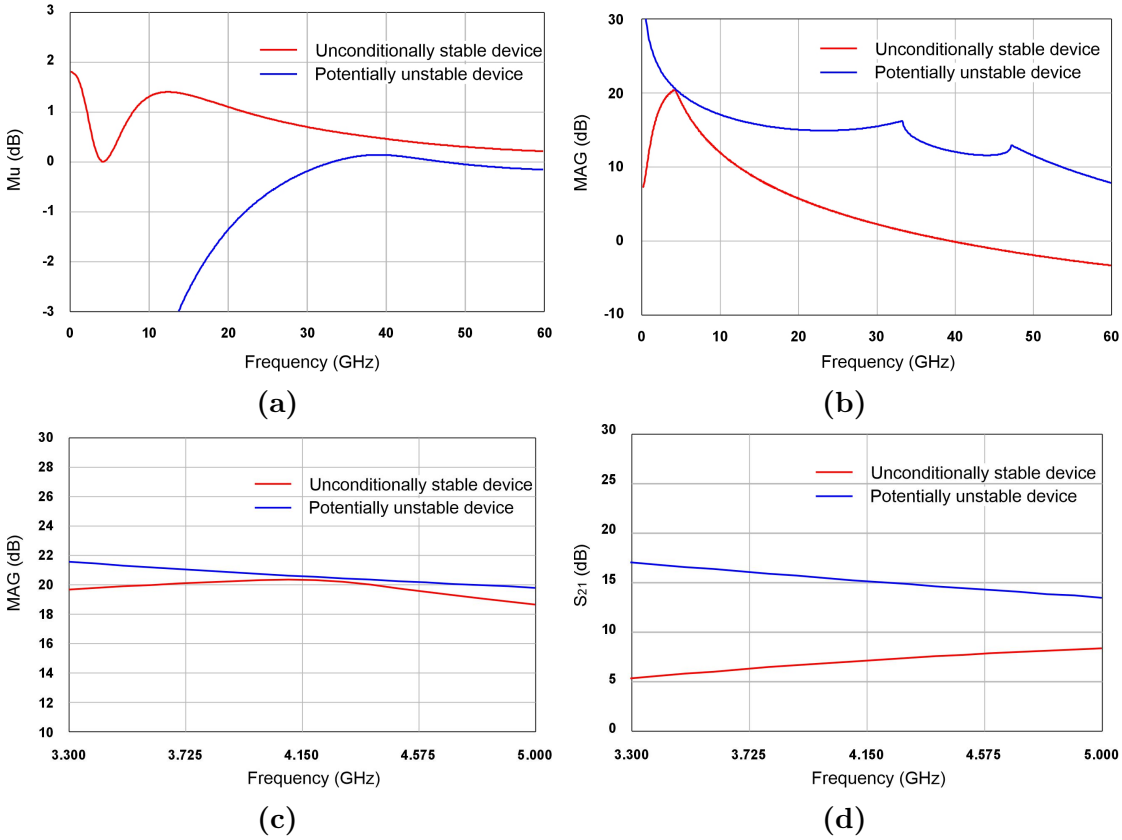

Figure 3.2: Mu parameter (a), MAG (0-60) GHz (b), MAG (3.3-5) GHz (c) and S_{21} (d) for the unconditionally stable device (red) with ideal stabilization network

place can be controlled. The device is therefore stabilized with ideal components with the input network shown in Figure 3.3: a series RL network in parallel to the gate is used to stabilize the device at low frequencies; a parallel RC network in series to the gate stabilize the device at high frequencies.

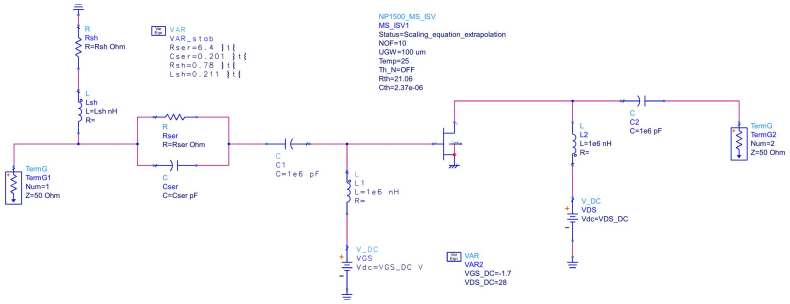

Figure 3.3: Stabilization network with ideal components

Figure 3.2 (red curve) shows the unconditionally stable device: *mu* parameter larger than 1 over the whole (0-60) GHz range (a); MAG close to the MAG of the non-stabilized device in the band of interest (c); gain parameter S_{21} within a 4 dB variation (d).

In the second step, ideal components are substituted with ones that embed some parasitic effect. It is verified that stability and gain are maintained, through *mu*, MAG, and S_{21} parameters.

Note that stabilizing the device at low frequencies while keeping in-band gain high is challenging since the target band is at comparatively low frequencies and the stabilization network also influences the band.

3.1.3 Bias network and bias sensitivity

Following the theory in [4] an ideal bias network is composed of a series capacitor and a shunt inductor that separate the RF and the DC path [Figure 3.4]. In fact, ideally, the shunt inductor represents an open circuit for the RF signal preventing it from reaching the feeding point, while the series capacitor presents an open circuit to the DC signal, avoiding it to affect the RF loads at the input and output of the device.

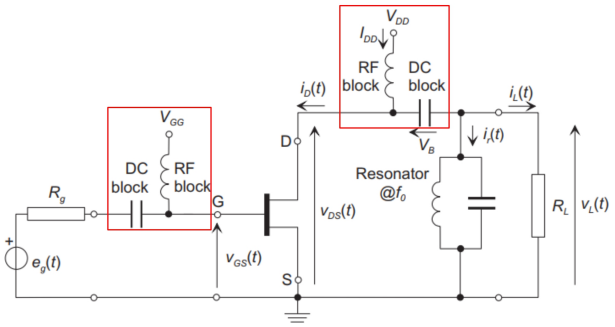

Figure 3.4: Ideal Bias-Tee (highlighted in red) location in a single-device power amplifier [3].

A realistic bias circuit [Figure 3.5] also needs some capacitors toward ground close to the DC supply. In a real implementation indeed the inductor presents a load different from an open circuit to the RF signal. This is not a problem as long as after the inductor there is at least one capacitor that presents to the RF signal a short circuit to ground. The RF and DC paths are then successfully decoupled since the RF signal will not reach the DC feeding point. With this method, the circuit can also be decoupled from feeding line interferences and load changes.

At the input of the device, the shunt inductor is included in the stabilization circuit. Figure 3.6 shows the final input bias network with the stabilization network

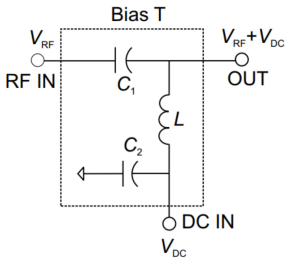

Figure 3.5: Example of a realistic Bias-Tee circuit [4].

included. Note that two levels of capacitors are implemented to decouple the in-band and the lower frequency components of the signal.

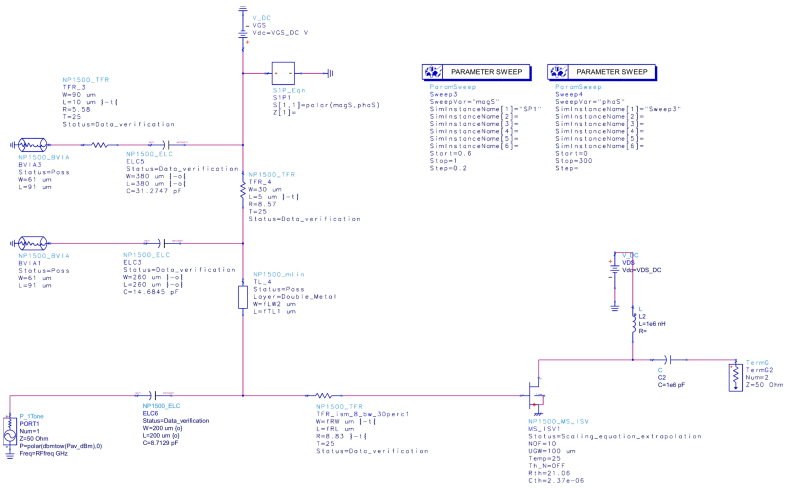

Figure 3.6: Input bias and stabilization network within a small-signal simulation for circuit sensitivity to variable loads on the feeding line

Due to the relatively low target frequencies, the needed capacitor to ground has significant dimensions (260 μm x 260 μm) at center band. Therefore, it is impossible to apply a 10x increase in capacitance value for the second level of capacitors due to the constraint on the overall chip area (3.7 mm x 3.3 mm). Instead, second-order capacitors will be used with dimensions (380 μm x 380 μm) close to the first-order ones. As a consequence, at frequencies much lower than the target band (below hundreds of MHz, approximately), the Bias-Tee does not act as a short circuit. These frequencies will need to be shorted with off-chip capacitors. For this reason, the sensitivity of the circuit to off-chip elements connected to the bias pads is tested. A variable load is connected to the gate feeding path to simulate load changes due to an off-board feeding connection. The small signal simulation

shows *mu* parameter does not change up to 900 MHz, which is acceptable since it is sufficiently below that target band. Off-chip capacitors will need to take care of lower frequencies and their variation.

Figure 3.7 shows the device output bias network implemented with the same real ground capacitors of the device's input. Note that both the Main and the Auxiliary devices have been provided with their own output bias in order to lower the maximum DC current and to use narrower microstrip lines for the feeding line and inductor realization, reducing the overall size of the circuit.

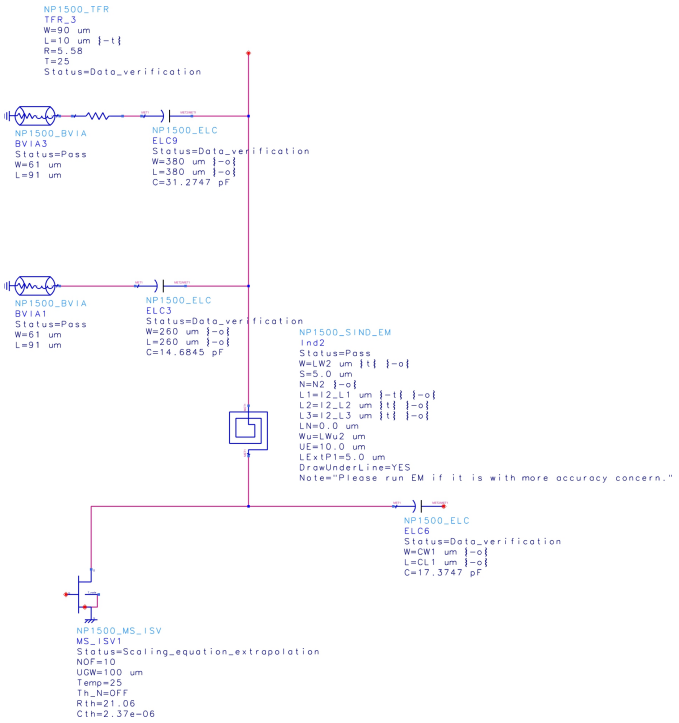

Figure 3.7: Active device with output bias network

At the device's input [Figure 3.6], a series resistor is added between the ground capacitors to further improve stability. At the output [Figure 3.7], this is not possible, since the drain current is many orders of magnitude higher than the gate current, and passing through the resistor would dissipate power and lower the overall efficiency.

3.1.4 Optimum load selection

The optimum load estimation is described in the following steps.

At first, the assumption of negligible device parasitic is made and the optimum load is extracted with formulas for an ideal Class B amplifier [5] with drain

bias voltage $V_{DS} = 28V$, knee voltage $V_{knee} = 4V$ and maximum drain current $I_{DSS} = 0.786A$ (3.1).

$$R_{opt} = \frac{2(V_{DS} - V_{knee})}{I_{DSS}} = 61\Omega \tag{3.1}$$

Secondly, the HB simulation and load-line considerations are used to better estimate this value, for the stabilized device. The load is tuned by searching the maximum efficiency value. Figure 3.8 (left) shows the maximum efficiency of 48%, measured in correspondence of PAE peak, obtained for a 62.25 Ω load that is therefore identified as the optimum load for efficiency; in Figure 3.8 (right) the dynamic load lines are shown.

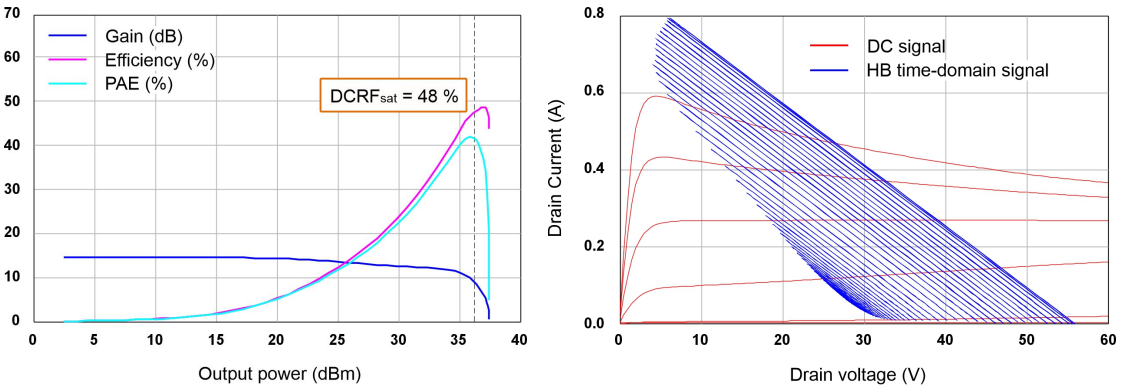

Figure 3.8: Large signal 1-tone simulation on the (10x100 μm) GaN device: power sweep (left) and dynamic load lines superimposed to the DC output characteristics (right).

Finally, the parasitic effect is considered: the resulting optimum load changes from a real value to a complex value. Large signal load-pull simulations are performed to estimate it. The results are shown in Figure 3.9 with an optimum load of (35+j39) Ω. For later steps, specifically, the combiner design, since a parasitic compensation is foreseen a real value for the optimum load is considered. In fact, the real value of 62.25 Ω is estimated to be the optimum load for a device with no parasitic elements at the output.

3.2 Driver and Matching Networks

3.2.1 Driver size and position

The need for a driver stage introduced in Chapter 2.1 is here illustrated in more detail. The HB power sweep of the final Main device [Figure 3.8 (left)] shows a

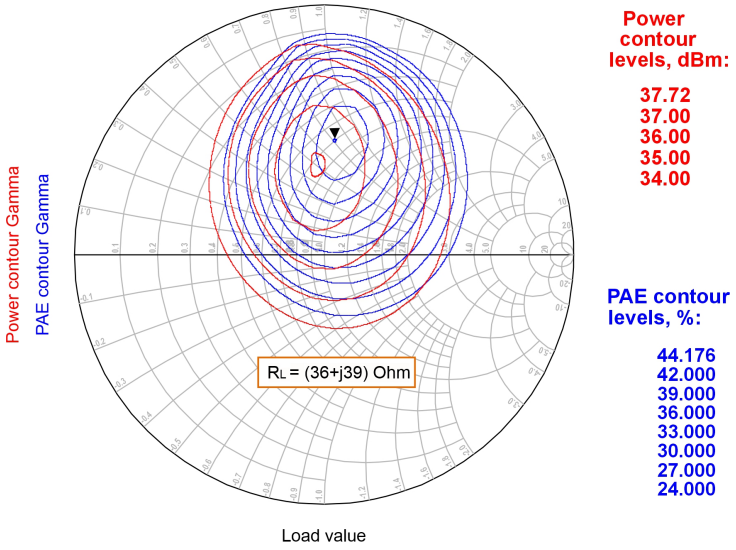

Figure 3.9: Simulated load-pull contours on the final stage device: output power (red) and PAE (blue). The marker highlights the optimum load for PAE.

small signal gain of about 15 dB at center frequency, while the specification for the overall gain is 20 dB. Furthermore, a symmetric 6-dB DPA has a small-signal gain loss of 3 dB with respect to the Main device gain, since the input power is divided equally between the PA branches but in small signal conditions the Auxiliary device is off [6]. Considering this, an additional device, the driver is added to the chain before the final stage device to provide more gain and satisfy the specifications. Note that even if two driver stages would have been a safer choice the chip size constraints limited the choice to one single driver.

Two DPA topologies are possible for the insertion of driver stages [Figure 3.10]: a single-driver approach in which the driver precedes the Doherty structure, and the dual-driver topology with foresees one driver for each branch of the DPA. In [18] is concluded that the single-driver approach must be preferred when the final stage device has a reasonable gain larger than 10 dB, due to its simplicity and compactness. Instead, when the final transistor has low gain, the dual-driver approach is required to prevent significant efficiency reduction. In this case the gain of the final device is slightly higher than 10 dB, but non-negliglible losses are expected in the matching networks due to both ohmic and mismatch effects. Therefore, in order to maintain high efficiency, the dual-driver topology is chosen.

From the power budget plan [Figure 3.11] a better understanding of the driver specifications can be achieved. The required final stage output power is 36 dBm. Considering 2 dBm of losses introduced by the ISM, and considering the final stage gain of 10 dB the driver needs to provide 28 dBm of output power. Furthermore, to satisfy the overall small signal gain specifications, the driver stage needs a gain

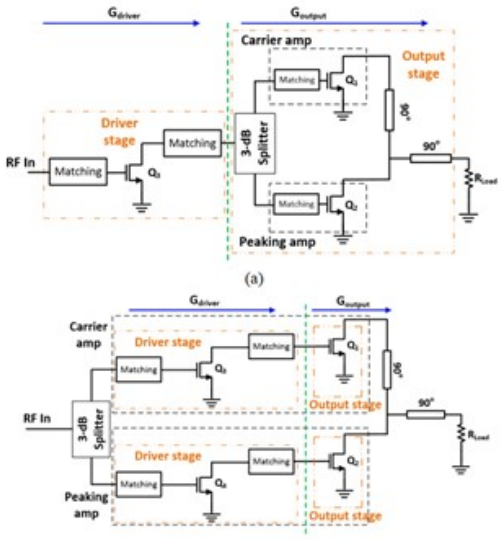

Figure 3.10: Driver topologies

larger than 10 dB.

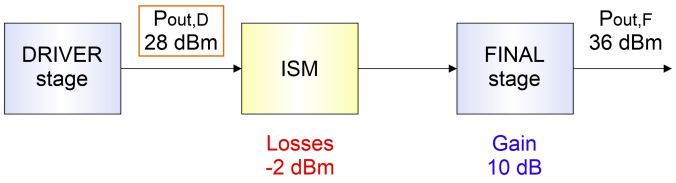

Figure 3.11: Power budget plan

The device must achieve the desired output power and gain without entering too strong compression, to ensure a limited impact on the final linearity performance, especially in terms of gain compression. Also, the driver should not be exceedingly oversized, since the lower the final stage gain, the higher the driver stage's impact on the final efficiency performance. Therefore, it is decided to request that the driver meets the output power and gain requirements for 3 dB gain compression. Note that similar consideration holds for the driver efficiency: due to low final stage gain the driver must have good efficiency performance to avoid degrading the overall efficiency performance.

The device periphery is now selected. The choice must not only take into account the output power, gain, efficiency, and linearity considerations but it should also result in optimum driver load that leads to a low impedance transformation ratio in order to achieve wide bandwidth [19].

A typical choice in multi-stage PA design is that the driver periphery is half

Pout [dBm]	Gain [dB]	Efficiency [%]
28	10	Best effort

Table 3.1: Target large signal performance for the driver device

of the final stage one [20, 21]. However, it might be the case that the gain of the final stage is high enough to allow for a smaller driver, thus enhancing efficiency [22], or conversely that the gain is so low, especially at frequencies close to the process cut-off frequency (f_T), that the drivers have the same periphery as the power devices [23], which has typically a negative impact on the overall efficiency.

The driver bias point is initially selected equal to the Class AB final stage bias. After evaluating different driver sizes, the 6x75 μm transistor is chosen. The stabilized device satisfies the requirements, providing for 3 dB gain compression 32 dBm of saturated power, 12.6 dB of gain, and 42% of efficiency at center band.

From the HB simulation of the stabilized ideal device, an optimum impedance of 100 Ω is estimated, which results to be the lower optimum impedance value for the different driver sizes evaluated. The power sweep and load line are shown in Figure 3.12.

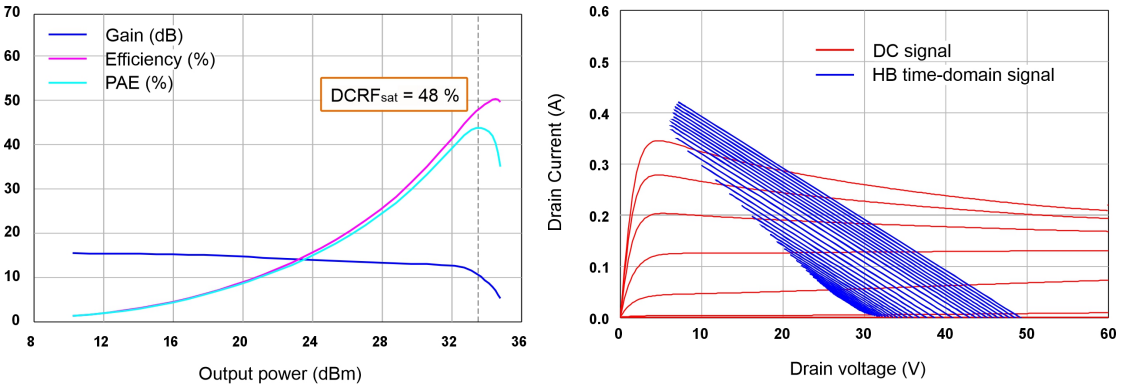

Figure 3.12: Large signal 1-tone simulation on the (6x75 μm) GaN driver device: power sweep (left) and dynamic load lines superimposed to the DC output characteristics (right)

3.2.2 Interstage Matching Network

An ISM is used to transform the final stage input impedance into the driver's optimum load.

The final stage input impedance is estimated at center band with a small-signal

simulation of the device closed on its optimum load of 62.25 Ω and resulted in (13+j9) Ω. Driver optimum real load was previously estimated in 100 Ω. The goal is to get a matching of at least -10 dB over the bandwidth while having a flat gain, to achieve uniform performance for the overall circuit and to minimize the losses. The parameters used for these purposes are S_{11} for matching and S_{21} for gain, extracted from a small-signal simulation.

An initial second-order filter LCLC topology is selected [Figure 3.13]: a first-order filter would not be enough to cover a 41 % bandwidth, while a third-order filter would add too many losses to the filter due to the used technology. To minimize losses, the matching network shares the final stage input bias series capacitor and the driver output bias LC components, with their real ground.

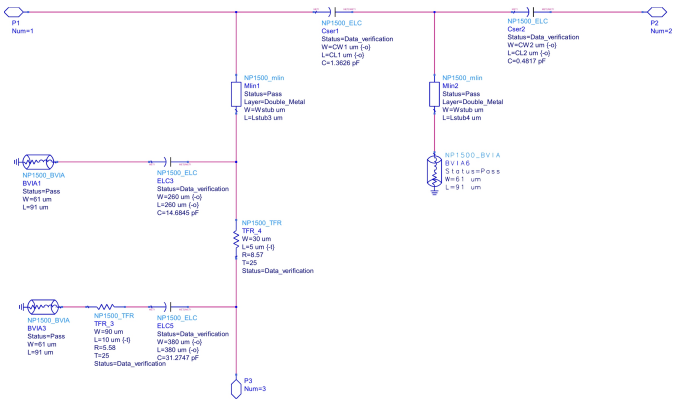

Figure 3.13: ISM subcircuit: second-order filter topology

First, the LCLC filter is designed considering the final stage input impedance at center band. Secondly, this circuit is optimized to match the frequency-dependent input impedance over the bandwidth for large signal power conditions. The dependent impedance is then substituted with the final stage and the matching network (MN). Simulations are performed at this stage and results are worse than expected with a non-uniform gain over the bandwidth and the gain at the band's lower limit degraded by several dB.

It is assumed the interaction between the matching network and the device stabilization network is affecting the gain and the MN is re-optimized to restore a uniform gain. Figure 3.14 shows the performances of the optimized ISM in the band: matching lower than -6 dB, gain in the range (12-14) dB, within 2 dB variation. Note that the best matching achieved is sub-optimal. This is due to the requirements of achieving matching and flat gain over a 41 % bandwidth while using two stages only.

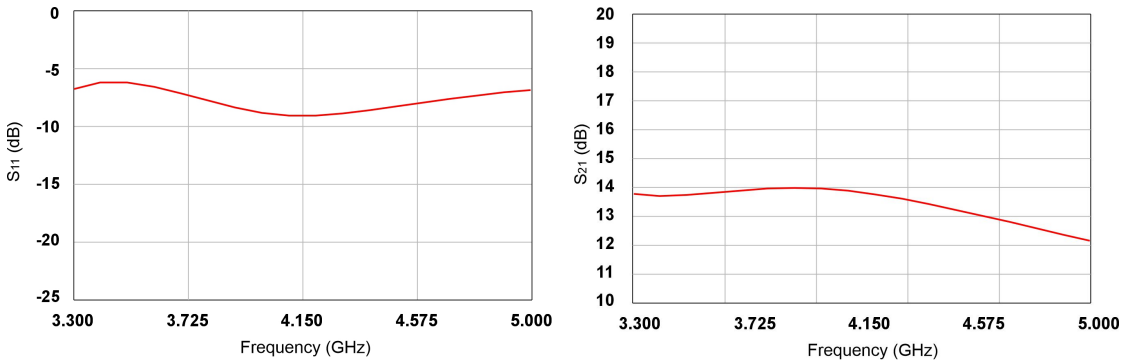

Figure 3.14: ISM performance in terms of matching (S_{11}) (left) and gain (S_{21}) (right)

3.2.3 Input Matching Network

The aim of the IMN is to transform the driver input impedance estimated in (33+j28) Ω into the input 50 Ω of the whole circuit. The same topology as the ISM is implemented, but without the need for feeding lines and real grounds. The same design flow is applied. Figure 3.15 shows the IMN circuit whose performances in terms of matching lower than -6 dB and gain in the range (12-14) dB are analogous to the ones of ISM, as expected since the topology is same and the impedances to match are close.

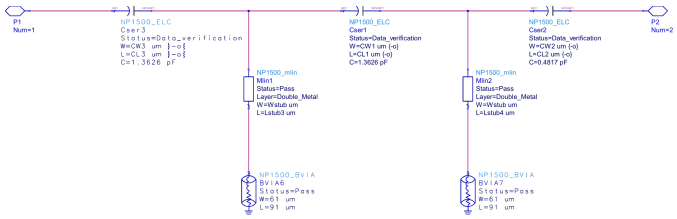

Figure 3.15: IMN subcircuit: second-order filter topology

The MN are then combined to form the Main branch of the Doherty which comprehends IMN, driver stage, ISM, and final stage [Figure 3.16], and their performances are tested with small-signal and HB simulations. A non-uniform gain over the bandwidth is observed. Further optimization of the MNs separately results to be the best approach to improve it. Figure 3.17 shows the large-signal performance of the branch while Figure 3.18 shows the small-signal results with a gain variation successfully reduced to 6 dB.

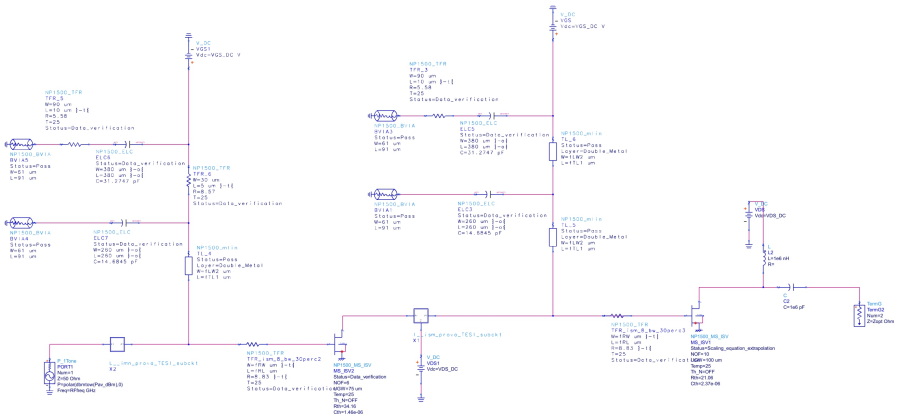

Figure 3.16: IMN-driver-ISM-final stage Main chain

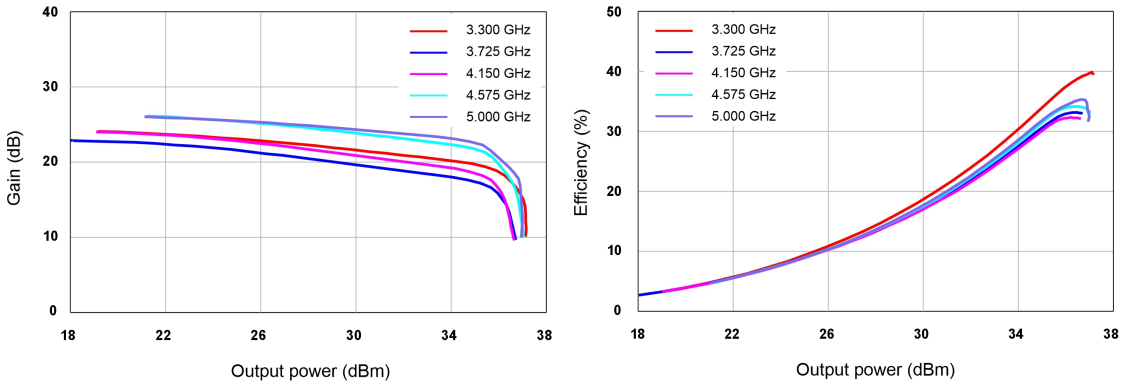

Figure 3.17: Main DPA branch large signal performance for five frequencies in the target bandwidth: gain (left), efficiency (right).

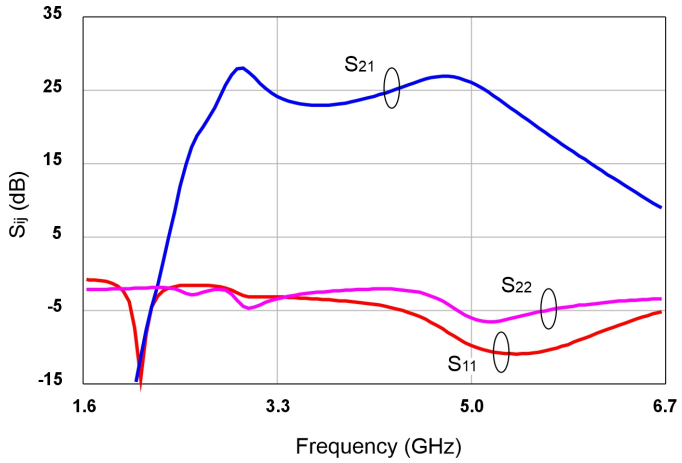

Figure 3.18: Main DPA branch small signal performance

3.3 Doherty combiner design

3.3.1 Combiner

As introduced in Chapter 1, the combiner's aim in a DPA is to implement the load modulation, i.e., to present to devices the right loads for different input power levels, to achieve high efficiency in OBO. Furthermore, in this case, the designed circuit has to provide it on a wide frequency band.

Three different topologies are implemented in ideal transmission lines considering a 50 Ω optimum load, and their performances are compared over the target bandwidth:

- "classical" Doherty combiner with $\lambda/4$ impedance inverter [3], shown in Figure 3.19;
- "lambda-half" combiner [24], shown in Figure 3.20;
- "two-section peaking" combiner, shown in Figure 3.21 [25].

The "two-section peaking" combiner is implemented by applying principles and design formulas from [26] for the characteristic impedances of the lines.

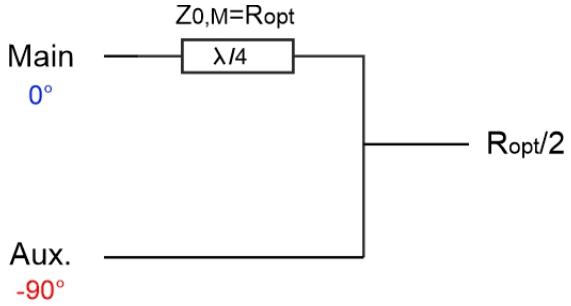

Figure 3.19: Classic combiner

The parameters used for comparison are $\Gamma_{dM,OBO}$ i.e., Main reflection coefficient at Break; $\Gamma_{dM,sat}$ and $\Gamma_{dA,sat}$ i.e., Main and Auxiliary reflection coefficients at saturation. They are defined in (3.2), (3.4), and (3.3): Z_d represents the impedance at the devices' drain, while M and A represent the Main and Auxiliary amplifiers respectively

$$\Gamma_{dM,OBO} = \frac{Z_{dM,OBO} - 2R_{opt}}{Z_{dM,OBO} + 2R_{opt}} \tag{3.2}$$

$$\Gamma_{dM,sat} = \frac{Z_{dM,sat} - R_{opt}}{Z_{dM,sat} + R_{opt}} \tag{3.3}$$

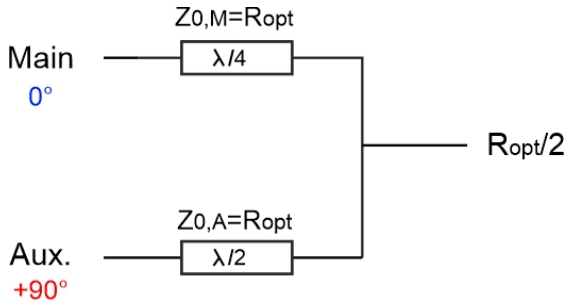

Figure 3.20: Lambda-half combiner

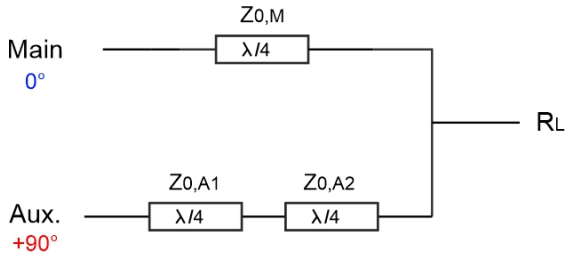

Figure 3.21: "Two-section peaking" combiner

$$\Gamma_{dA,sat} = \frac{Z_{dA,sat} - R_{opt}}{Z_{dA,sat} + R_{opt}} \tag{3.4}$$

The Main efficiency at Break is determinant for the overall efficiency at Break, since it is the only device turned on, while both Main and Auxiliary efficiencies are relevant at saturation because both devices are turned on.

From Figure 3.22 we can observe that the "two-section peaking" combiner is providing the best matching at Break over the bandwidth ($\Gamma_{dM,OBO}$<-24dB) while providing good matching in saturation ($\Gamma_{dM,sat}$<-10dB, $\Gamma_{dA,sat}$<-17dB). It is also feasible from the TLs width point of view since the characteristic impedances respect the limit 20μm<Z_0<80μm. This combiner topology is therefore chosen for the circuit implementation. It is then realized with microstrip lines and optimized for the desired optimum load of 62.25 Ω. Figure 3.23 shows its final performance: $\Gamma_{dM,OBO}$<-23dB, $\Gamma_{dM,sat}$<-10dB, and $\Gamma_{dA,sat}$<-14dB.

Note that, while the results are good, it is difficult to make it behave as the [26] is suggesting i.e., to make $\Gamma_{dM,OBO}$ curl while keeping $\Gamma_{dM,sat}$ close to the center of the Smith Chart. This is probably due to the target optimum load and power levels which are not in the same range of application of the publication. This topic would need further investigation.

Later, devices' output bias are included in the circuit, to ensure its influence are negligible: its inductors are optimized to achieve that. Different positions for the

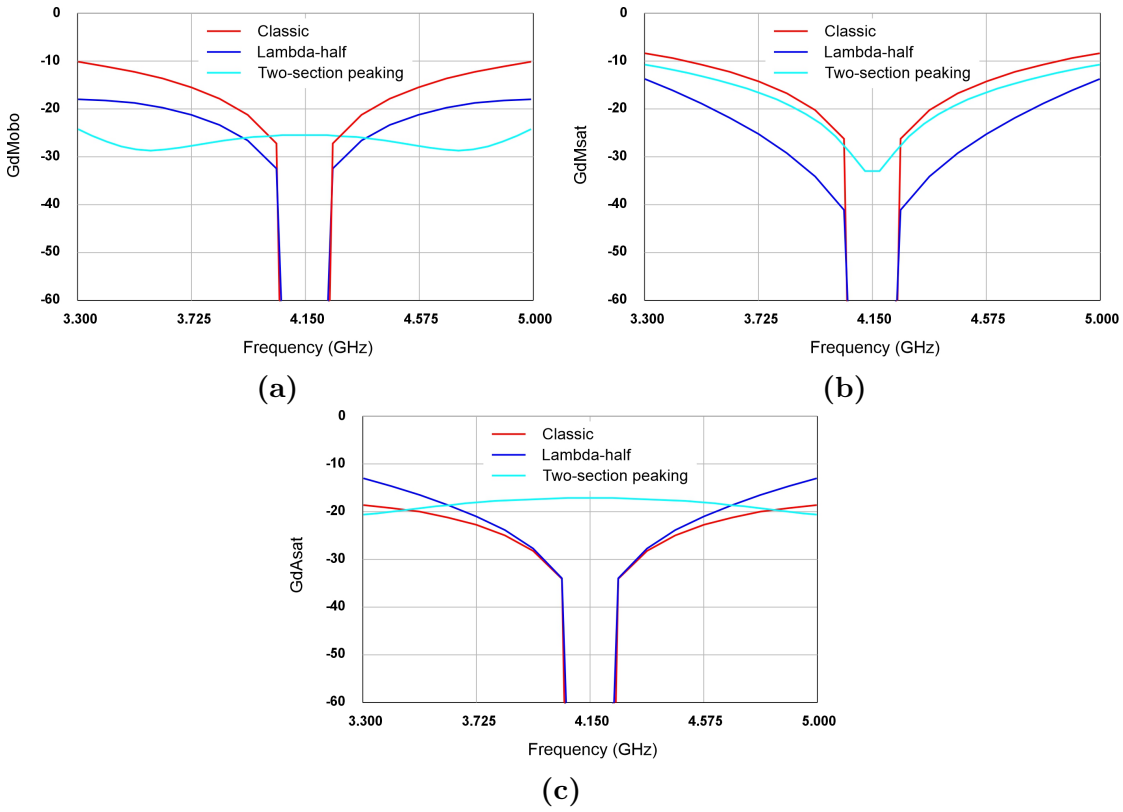

Figure 3.22: Small signal performance evaluation for three combiner topologies: $\Gamma_{dM,OBO}$ (a), $\Gamma_{dM,sat}$ (b), and $\Gamma_{dA,sat}$ (c).

bias are simulated, searching for combiner bandwidth improvements: the best one results to be the classical collocation at the devices' drains.

3.3.2 Parasitic compensation

In the parallel activity of the research group on the GaAs DPA, parasitic effects are negligible at Sub-6 GHz frequencies. The same assumption is not suitable for the GaN case. An RLC circuit is chosen to model the parasitic [Figure 3.24]: an inductor in parallel to the transistor drain output and a capacitor in series to the drain output. The stabilized (10x100 μm) device is turned off and simulated in small-signal conditions. The optimizer is used to make the model and the device output behave in the same way. The RLC values obtained are 5000 Ω, 0.019 nH, and 0.442 pF. The 5000 Ω resistance is later considered negligible with respect to the transistors' drain-to-source resistance.

Different compensation solutions are analyzed such as embedding parasitic in the device output bias circuit, using a different output bias topology and the

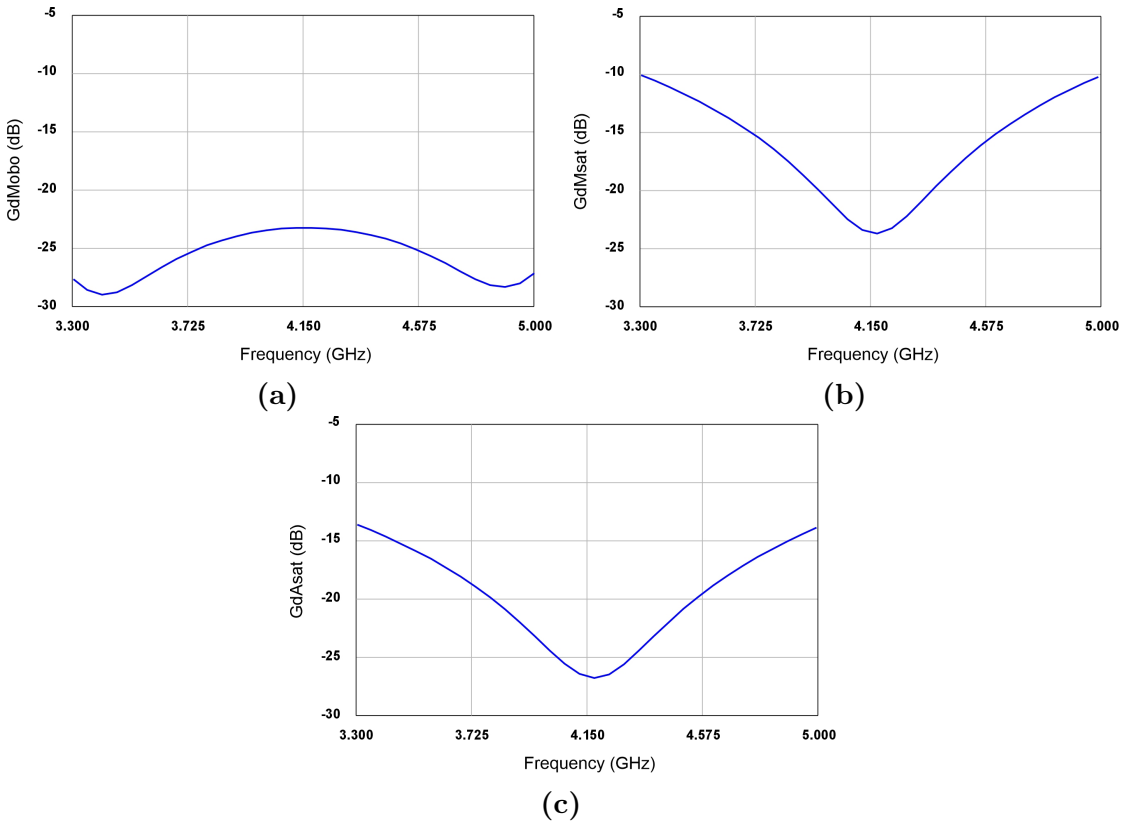

Figure 3.23: "Two-section peaking combiner" small signal performance: $\Gamma_{dM,OBO}$ (a), $\Gamma_{dM,sat}$ (b), and $\Gamma_{dA,sat}$ (c).

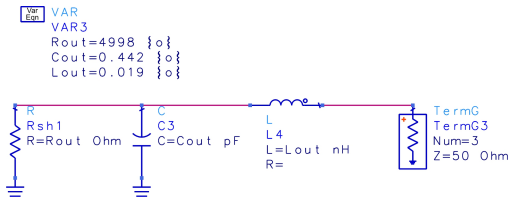

Figure 3.24: (10x100μm) GaN device output parasitics as represented by an RLC model.

compensation method shown in the publication [26]. The best solution results to be last, i.e., embedding parasitic compensation in the combiner: one shunt capacitor is added after the first quarter wavelength transform in each branch, the quarter wavelength transform lengths are shortened, and the characteristic impedance of the lines is increased. This method corresponds to a pi-topology implementation of the quarter wavelength transform. Note that the characteristic impedances needed for perfect compensation are not feasible i.e., $Z_0 < 10\mu$m, $Z_0 > 80\mu$m. A best-effort

design is then performed with the use of the optimizer. As expected, the resulting characteristic impedance and transmission line lengths differ from the results of the publication. The final combiner is shown in Figure 3.25. Its performances are shown in Figure 3.26 where they are compared to the ones of the same combiner implemented with ideal TLs: a good level of agreement is observed.

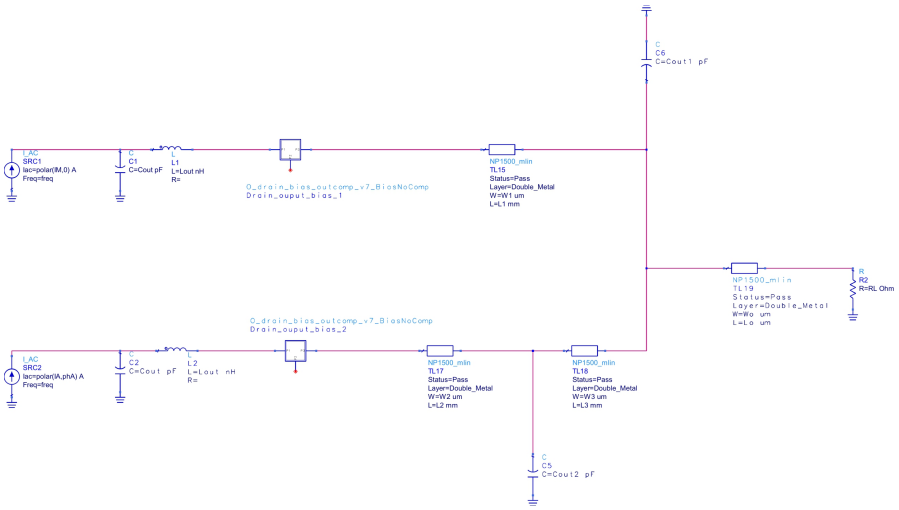

Figure 3.25: Combiner with parasitic compensation

It is then tested by attaching the real device's network to it: the simulation shows the DPA is not modulating for all the frequencies. Optimizing the combiner within the whole DPA circuit simulation is not possible: due to the complexity of the circuit and the computational limits of the machine the simulations are performed on the optimization would require days. The combiner is therefore optimized alone but this is not enough. Since embedding parasitic compensation usually has more losses at high frequencies the combiner is re-optimized alone on a slightly larger bandwidth (3.3-5.1) GHz. This leads eventually to a load modulation at all frequencies shown in Figure 3.27. The resistance values are different over the bandwidth, in the (57, 83) Ω range at Break and (35, 53) Ω at saturation but a uniform variation of factor 1.6 can be observed on the whole bandwidth, close enough to the ideal factor 2 [Chapter 1].

3.4 Auxiliary Bias Point Selection

As illustrated in Chapter 1 in the Auxiliary branch of the DPA an amplifier biased in Class C is needed to achieve the load modulation. It is chosen to use the same chain, consisting of IMN-driver stage-ISM-final stage, for both the Main and Auxiliary branches to minimize the phase difference between the two branches.

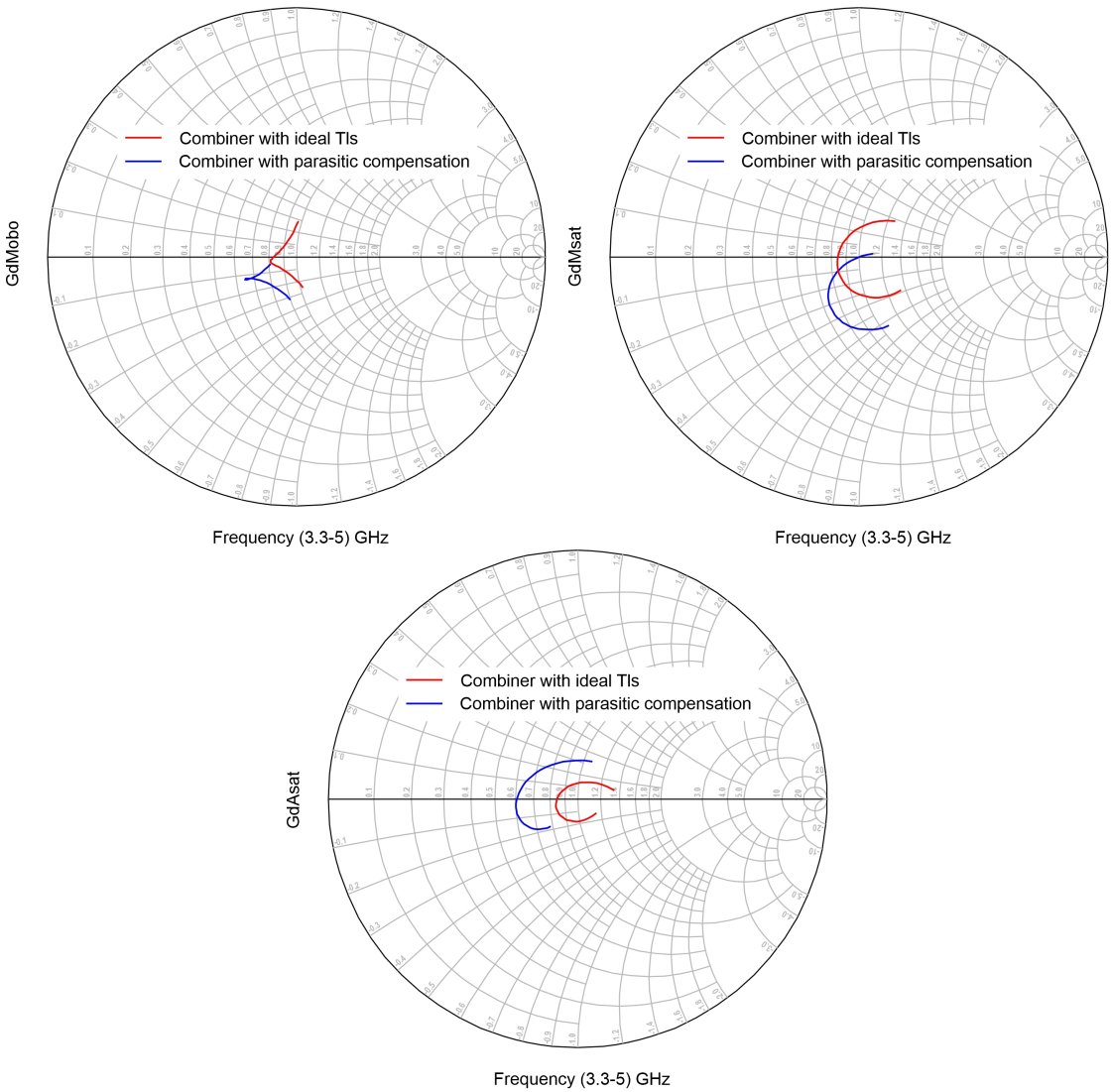

Figure 3.26: "Two-section peaking combiner" small signal performance evaluation: ideal TLs implementation (red), parasitic compensation implementation (blue).

A suitable bias for the Auxiliary chain is selected: the Auxiliary needs to turn on when the Main reaches the maximum efficiency on the $2R_{opt}$ load, which is estimated to happen in correspondence of 27 dBm available power; the Break is then estimated to be reached for a 15 dBm available power, to have a 6 dB OBO.

Different gate bias are evaluated for the Auxiliary chain, by looking at the drain current of the final stage to ensure it turns on in correspondence of the target available power of 15 dB [Figure 3.28].

The overall DPA performances versus Auxiliary gate bias variations are then

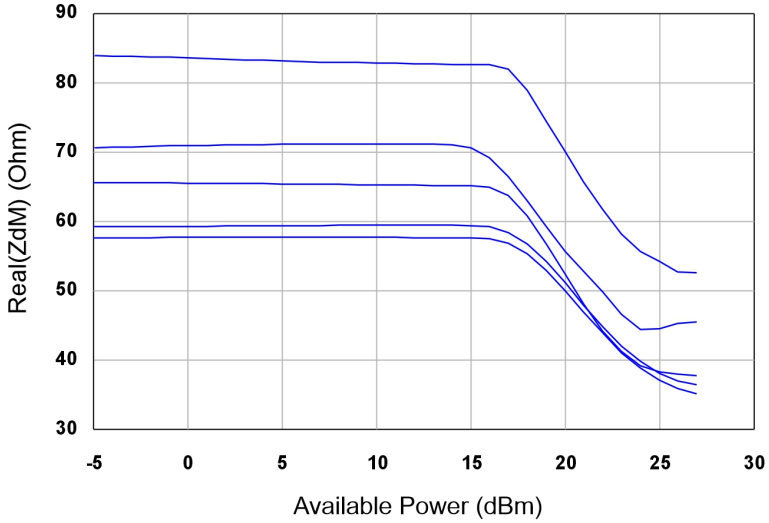

Figure 3.27: Resistance evaluated at the drain of the Main final-stage device: load modulation is shown.

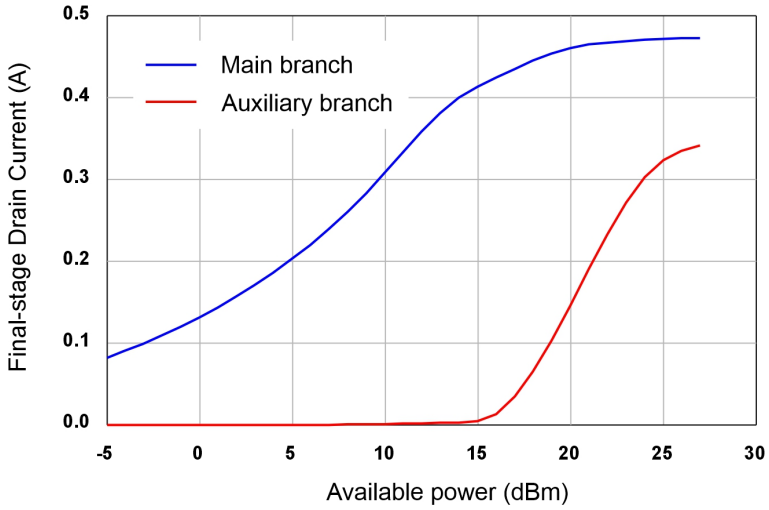

Figure 3.28: Main and Auxiliary current turn-on at center band

observed. Different gate bias for the driver and final stages are also evaluated. Gain and linearity performances as well as efficiency ones are considered. The selected final bias are -2.4 V for the driver stage and -3.4 V for the final stage. The consequent DPA gain and efficiency performances are plotted in Figure 3.29 (continuous line) where they are compared to a bias closer to Class C for both driver and final stage. It can be observed that a gate bias more in Class C for both stages, provides less linearity i.e., less gain after the Break point while giving

higher efficiency, while a bias closer to Class B for one of the stages provides more linearity.

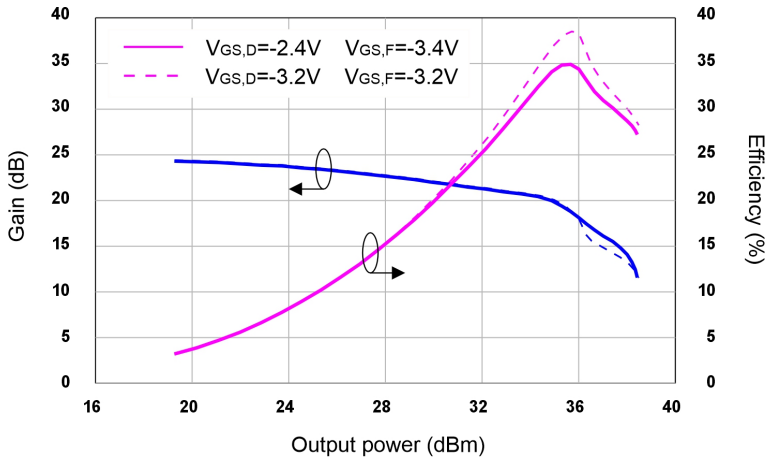

Figure 3.29: DPA performance at center band

3.5 Dual input Doherty architecture

After evaluating gain and efficiency curves, the DPA performances in terms of saturated output power, gain, and efficiency are evaluated in more detail. At this stage, the input power splitter is not present yet [Figure 3.30].

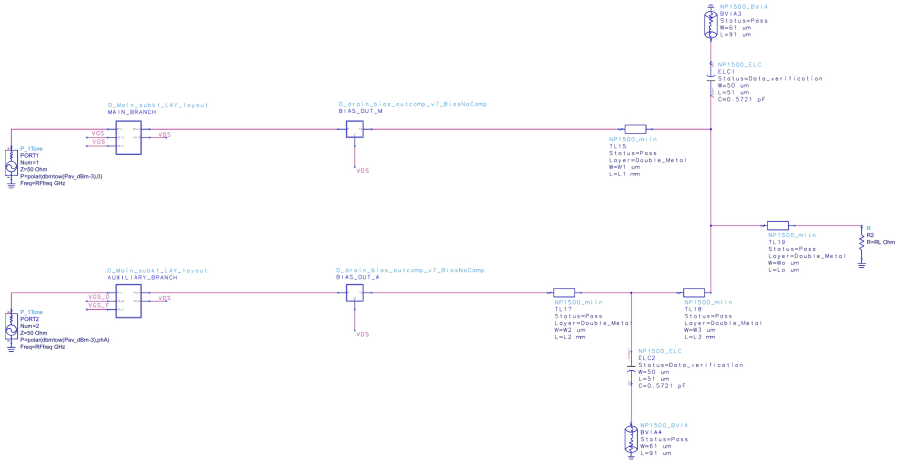

Figure 3.30: Dual input Doherty architecture without input splitter

One main problem with the gain is encountered: it is varying more than 5 dB over the bandwidth. To solve this issue, two strategies are applied. First, the

MNs S_{21} parameter is optimized to make the device gain more uniform over the bandwidth. Secondly, the final stage optimum load previously set to 62.25 Ω is optimized to make the efficiency and PAE vary less from Break to saturation and to achieve more uniform performance against input power sweep. This can be seen from the PAE curves in Figure 3.31 obtained by changing the load from R_{opt} to $2R_{opt}$. We can see that for 46 Ω R_{opt} the variation is less than 2 %, while it's larger than 9 % for 62.25 Ω. The value of 46 Ω is therefore chosen as the new optimum load.

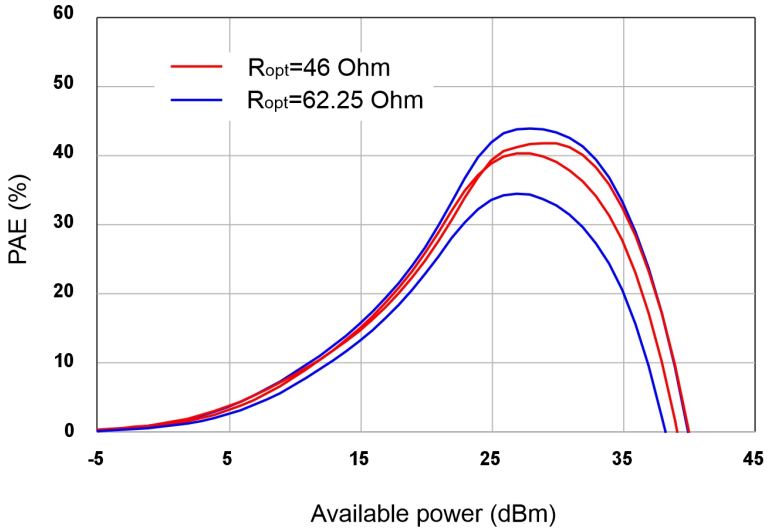

Figure 3.31: Device PAE Ropt 62.25 Ω (blue), Ropt 46 Ω (red)

The combiner is then re-designed on the new R_{opt} following the procedure illustrated in Chapter 3.3, while for the ISM only an optimization is needed. Figure 3.33 shows the dual input DPA final small signal gain: it is larger than 22 dB with a 4 dB variation over the bandwidth. On the other hand, Figure 3.32 shows the large signal performance: efficiency at saturation larger than 26 % while larger than 24 % at Break and minimum saturated power larger than 38 dBm. The requirements specification are therefore met.

3.6 Lange Power Splitter

The aim of the input power splitter is to divide the input power equally between the DPA branches while providing the correct phase shift for power combination i.e., +90° to the Auxiliary branch or equivalently -90° to the Main branch. To satisfy the wideband requirement of the circuit a Lange coupler is chosen over a Wilkinson power divider and a branch line coupler. Note that it also provides the

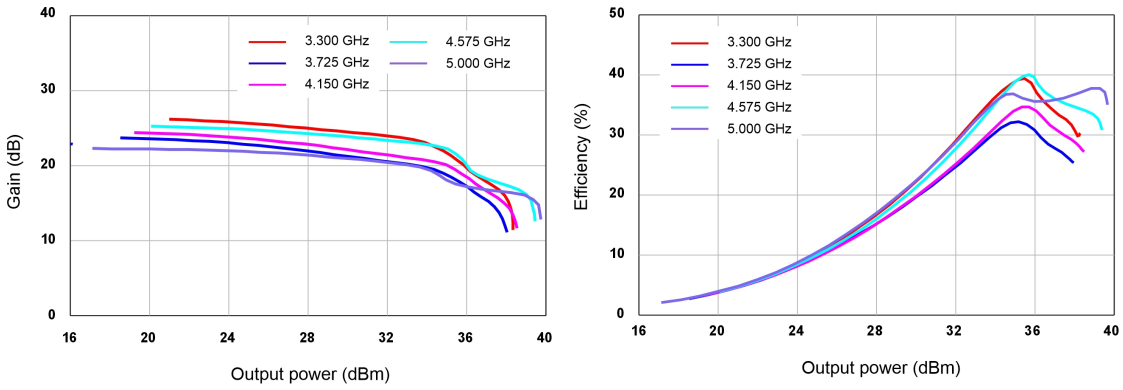

Figure 3.32: Dual input DPA large signal performance for five frequencies in the target bandwidth: gain (left), efficiency (right).

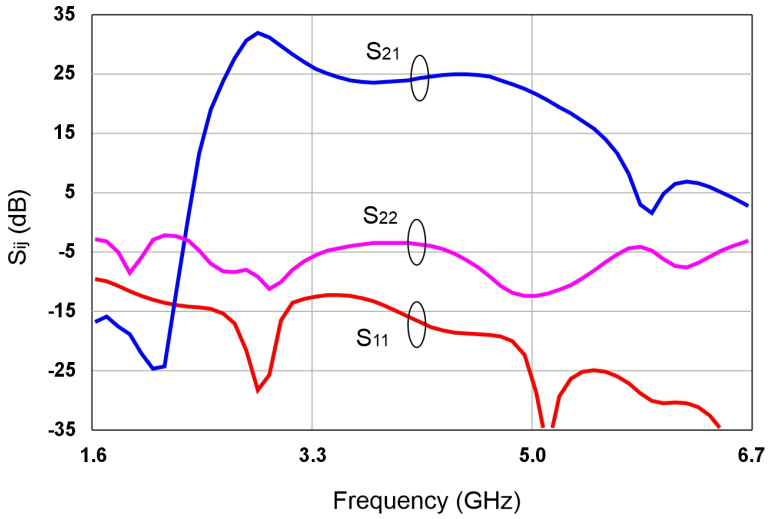

Figure 3.33: Dual input DPA small signal performance

needed phase shift.

At first, an ideal 50 Ω Lange is designed: width, spacing, and length of the transmission lines are estimated with formulas from [3]. Note that the Lange *NP1500_mlang* component is already present in the provided process design kit. This is optimized within a small signal simulation to achieve -3 dB coupling and 90° phase shift on the target band.

In Figure 3.34 the resulting performance can be observed. Over the target bandwidth (3.3-5) GHz an acceptable -3.5 dB minimum coupling factor is achieved, while the desired 90° phase shift is achieved within an acceptable 1.6° variation interval. As a final consideration, the Lange length of 7 mm suggests that the

component layout will require to be modified and bent to fit the chip area (3.7 x 3.3) mm^2. This will be discussed in the following Layout chapter.

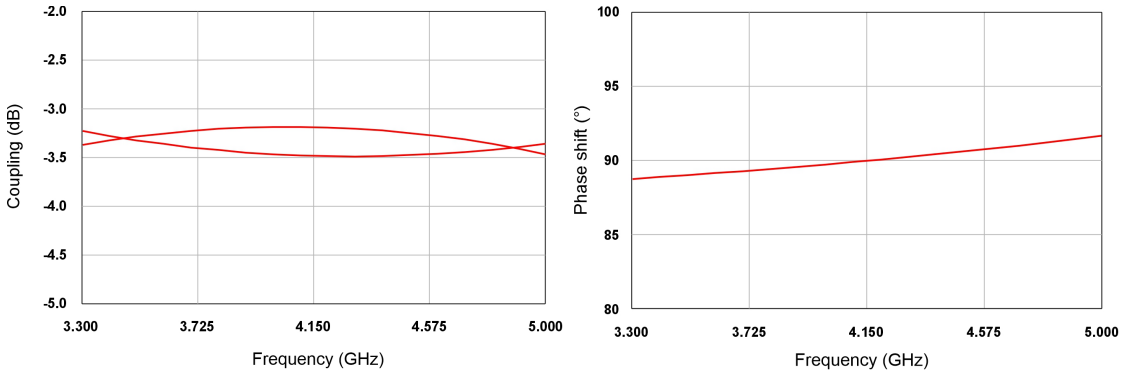

Figure 3.34: Lange power splitter small signal performance: coupling (left) and phase shift (right)

3.7 Out-of-band gain control

At this point of the design a small signal circuit simulation is performed on the overall circuit and the S_{21} parameter i.e., the gain is evaluated both in-band and outside the target band. Out-of-band high gain is sought after: it is undesired since it can cause oscillations and interferences to other systems. In Figure 3.35 the gain performance of the Main branch without S_{21} control can be seen: the gain remains higher than 0 dB outside the upper band limit, from 5 GHz up to 17 GHz while it is under control i.e., lower than 0 dB, for the other frequencies in the (0-40) GHz range.

Since the Auxiliary device is turned off in the small signal simulation, the Main chain is only investigated as responsible for S_{21} rise. An additional component is added in different locations in the circuit schematic to find the proper component and place that could influence the S_{21} parameter. Two solutions are founded: adding an additional shunt capacitor to both matching networks, on both branches; using two series inductors, instead of one, in the final stage output bias on both branches. Due to later considerations on circuit size, the second solution is discarded.

The next step is re-optimizing the MNs with the additional component. Note that the constraint of low gain after the upper band limit is added to the already challenging requirements of low S_{21}, high in-band gain, and flat in-band gain. Figure 3.36 and 3.37 show the modified ISM with the additional shunt capacitor and its performance respectively. A matching lower than -5 dB is achieved, together

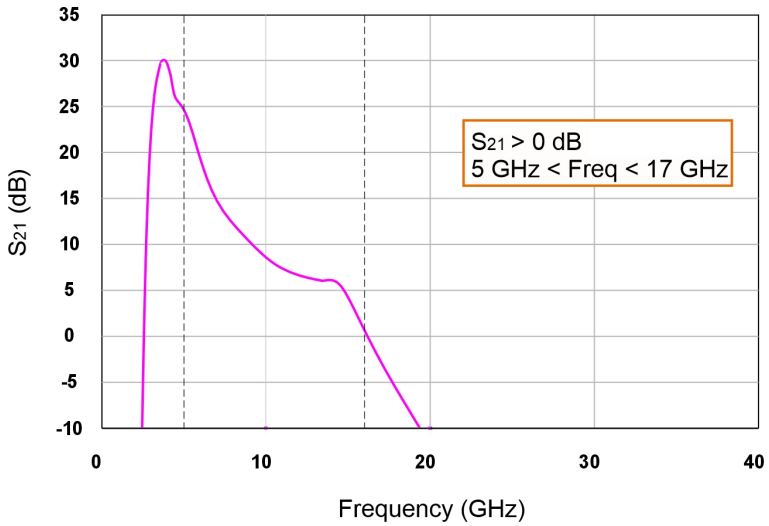

Figure 3.35: Main branch gain (S_{21}) in the absence of out-of-band gain control.

with a flat gain larger than 13 dB and inside a 1 dB variation interval in addition to the new feature of gain lower than 3 dB for out-of-band frequencies larger than 7 GHz. For the IMN subcircuit analogous performance in terms of matching, gain flatness and out-of-band gain suppression is achieved.

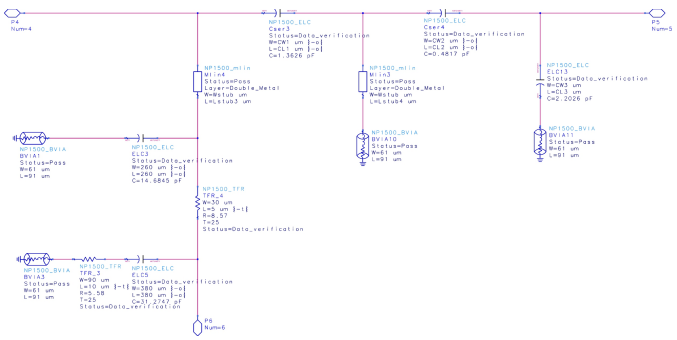

Figure 3.36: ISM subcircuit with additional shunt capacitor for out-of-band gain control

The optimization process is stopped after a few iterations with an overall gain of about 0 dB at 7 GHz, but a gain still larger than 0 dB in the (5-7) GHz band (Figure 3.38). The out-of-band gain suppression is therefore achieved in the wide (0-40) GHz frequency range except for the (5-7) GHz range where it can be still improved.

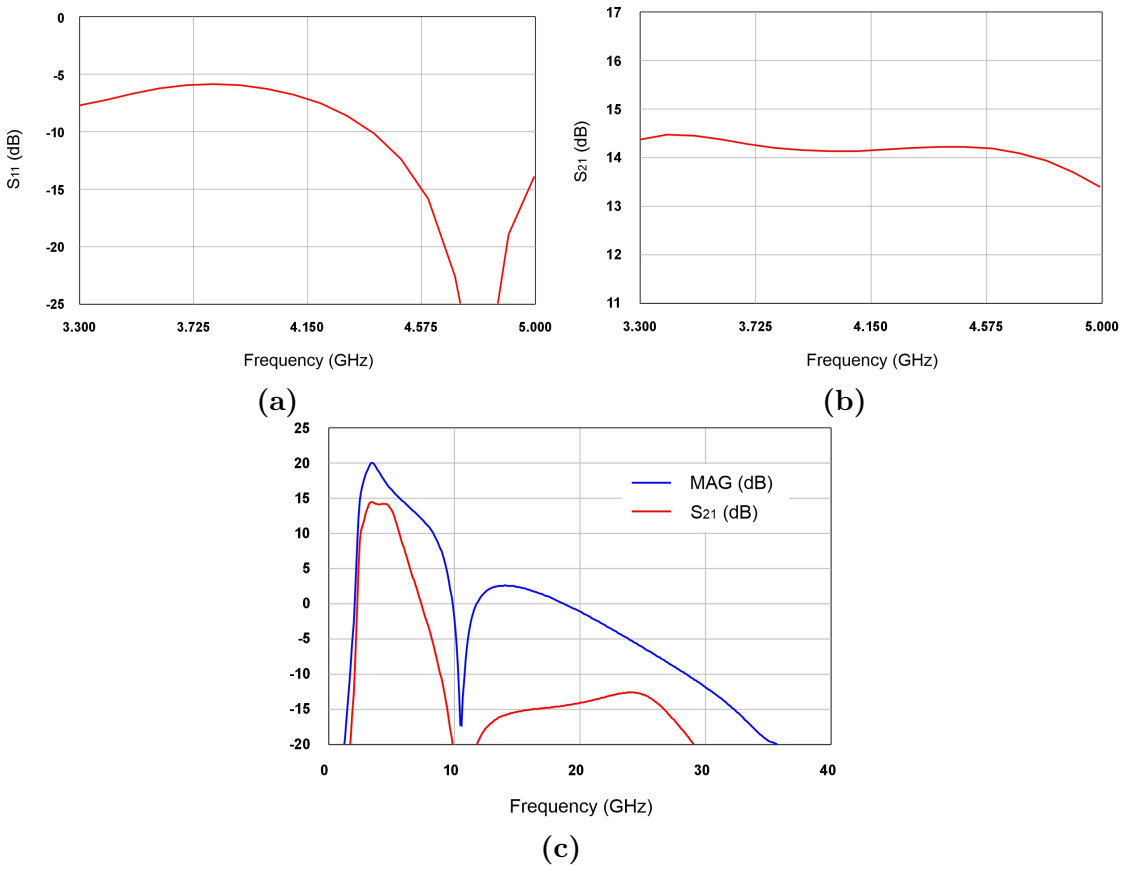

Figure 3.37: ISM performance in the presence of out-of-band gain control: matching (a), gain (3.3-5) GHz (b), gain and MAG (0-40) GHz (c).

3.8 Stability

In order to ensure the stability of the circuit and prevent it from oscillating many checks are performed during the design flow. At first, device-level stability is ensured by applying the single-parameter criterion in small signal conditions [3], as described earlier in this chapter. Secondly, circuit-level tests are performed to find critical issues before translating the circuit-level into the layout equivalent. Finally, the last inspections are performed on the layout to find the effects of coupling lines and nearby components on the overall stability performance. Note that these tests, while they are necessary for designing a stable circuit, are not sufficient to ensure the circuit's stability.

Two kinds of stability checks are carried out circuit level: Ohtomo small signal stability test and STAN large signal stability test. Ohtomo test [27] [28] allows a graphical check of circuit stability on the Smith Chart. It is implemented by

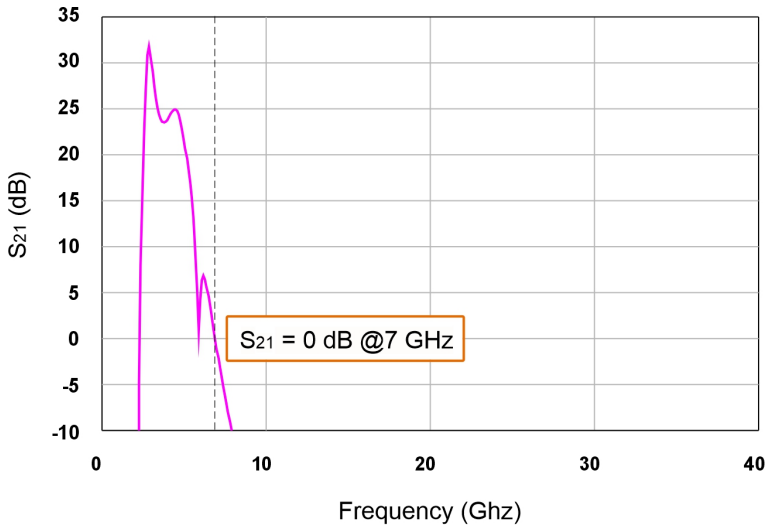

Figure 3.38: Main branch gain (S_{21}) in the presence of out-of-band gain control.

adding generators to gates and drains of each transistor (for a total of 8 devices in the present case). Then a small signal S-parameter simulation is carried out. In Figure 3.39 the S_{11} parameter corresponding to the placement of the generators at the driver gate on the Auxiliary branch and at the final stage drain on the Main branch is shown as an example. The S_{11} traces are inside the Smith Chart for every frequency meaning that the circuit is stable. The test is repeated with variable loads on the feeding lines, such as it was done for Bias-Tee earlier in the chapter: the outcome is still a stable circuit.

On the other hand, the STAN tool [29] is a patented solution capable of assessing the stability of microwave circuits in large signal conditions. The STAN approach calculates a single-input, single-output transfer function linearized around a given steady state. The simulated frequency response of the linearized circuit is fitted to a rational polynomial transfer function. If no poles on the right-half plane are found, it is considered stable.

A perturbation input signal is therefore applied in different places of the circuit and the right-half poles are searched for; the procedure is repeated for various perturbation frequencies in the range (0-40) GHz and for various bias: nominal bias, all devices on, all devices off. The test results in just one unstable outcome at about 2.6 GHz with the perturbation on the Drain of the final stage of the Main branch: a couple of poles-zeros close to each other on the right side of the complex plane is found. Performing a test on a smaller frequency range (2-3) GHz, the poles-zeros canceled out themselves pointing out most likely a numeric problem and a stable circuit. An example of STAN simulation results can be found in Figure 3.40.

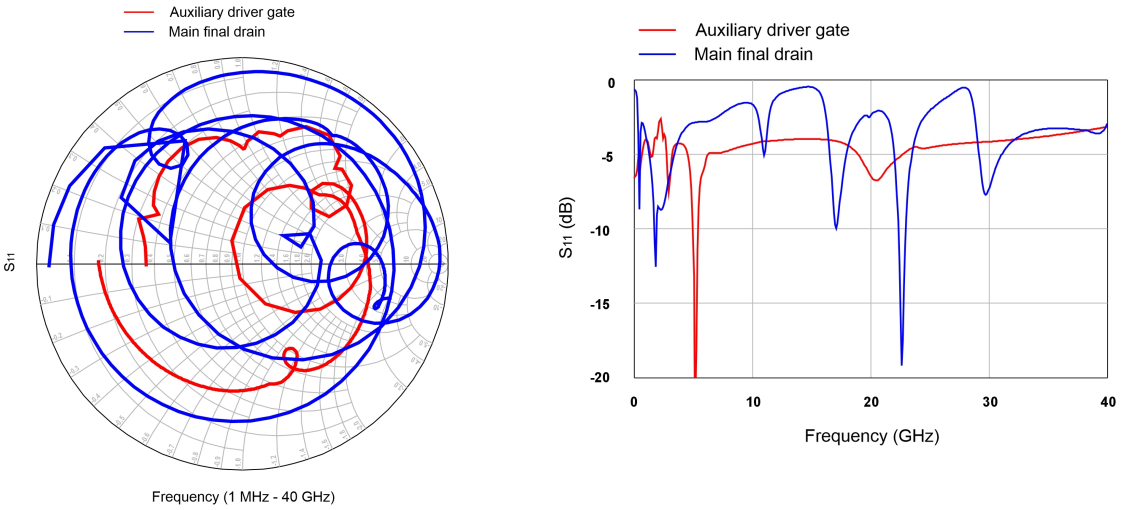

Figure 3.39: Example of Ohtomo test results: Smith Chart representation (left), reflection coefficient magnitude representation (right).

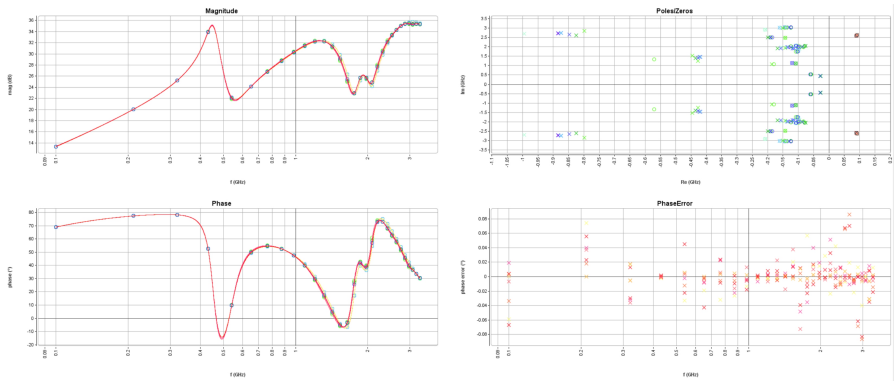

Figure 3.40: Example of STAN test results: estimated transfer function (left), poles/zeros (right)

3.9 Synthesized loads verification

This section compares the load-pull of the single device with the load synthesized and presented to the Main and Auxiliary devices in the final circuit. The analysis is carried out at saturation and the efficiency results are compared in terms of behavior versus frequency (five frequency points in the bandwidth).

In Section 3.1.4, the Main device was stabilized, and a load-pull template was used to determine the optimum load for maximum efficiency. The same load-pull results are presented in this section, but with the synthesized load values

superimposed. To perform the comparison, the single device's input power has been decreased by 3 dB to match the effect of the input power splitter in the DPA.

It can be seen in Figure 3.41 and 3.42 that the synthesized loads at saturation (green curve) are not the optimal loads for maximum efficiency and power, but their behavior versus frequency closely follows the load-pull circles, resulting in a uniform behavior across the bandwidth.

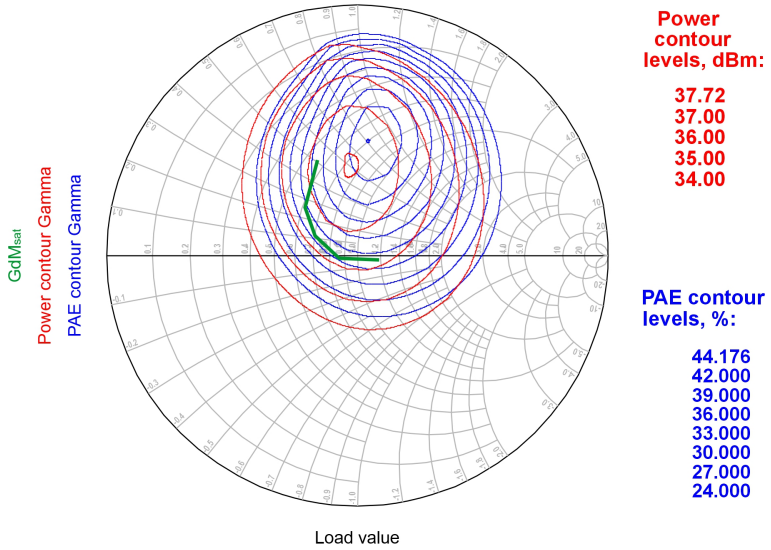

Figure 3.41: Synthesized loads presented to the Main final stage device (green) superimposed to the device's load pull contours output power (red) and PAE (blue).

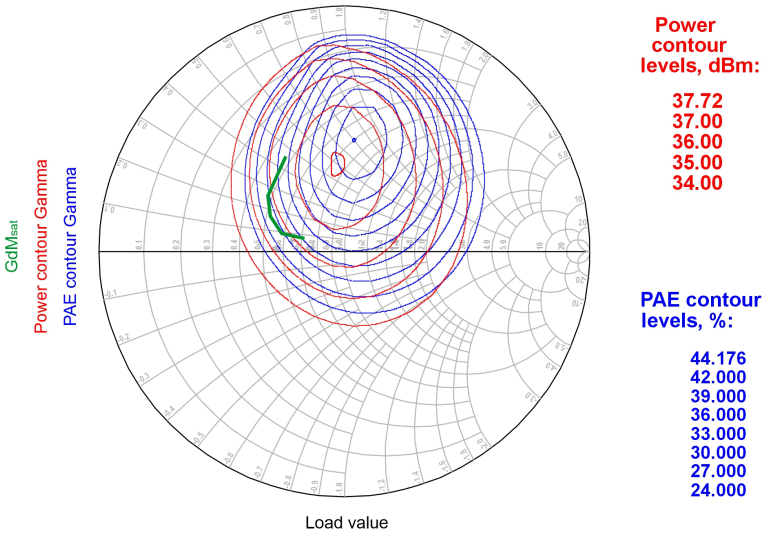

Figure 3.42: Synthesized loads presented to the Auxiliary final stage device (green) superimposed to the device's load pull contours output power (red) and PAE (blue).

Chapter 4

Layout planning

The next design step is to translate the circuit-level designed DPA into the corresponding layout-compliant version that can be manufactured. An additional constraint related to this step is to fit the DPA layout into the (3.7 x 3.3) mm^2 chip area while maintaining the target performance.

Initially, a preliminary version of the layout of the circuit is generated to get a first idea of the subcircuits size and to understand which sections need to be modified the most. Secondly, each subcircuit is translated into its layout equivalent, following the process design rules and checking their compliance with the design rule checking (DRC), which verifies if all the constraints imposed by the process technology are met. An important constraint for the layout design in the present process is the presence of only two layers of interconnections. Therefore, since extensive use of bridges is not feasible, a careful design must be carried out to connect the external bias to the inner part of the circuit topology.

In order to maintain as much as possible unchanged the performance during the translation from circuit-level to layout, electromagnetic (EM) simulations are utilized intensively in this phase for the proper tuning of lines and other layout elements using the EM simulator tool in advanced design system (ADS). They are especially important for components that have a significantly different layout than the standard one. Furthermore, they can estimate the resulting performance when nearby subcircuits influence each other.

4.1 Approximate layout and initial downscaling

An example of a layout translation of a schematic circuit is presented for the stabilization network of the final stage device: Figure 4.1 shows the stabilization network schematic realized with ideal components; Figure 4.2 shows the schematic view where real components are used and the microstrip lines and T-junction

interconnections necessary for a real implementation are inserted; finally, Figure 4.3 shows the layout translation of the stabilization network. Note that since the target frequency band is below 6 GHz, small variations in the layout shapes do not affect the performance.

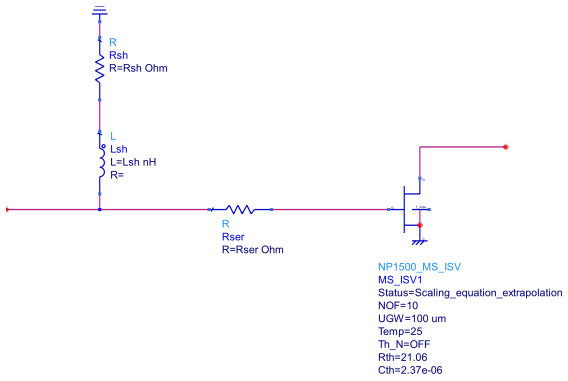

Figure 4.1: Stabilization network schematic with ideal components.

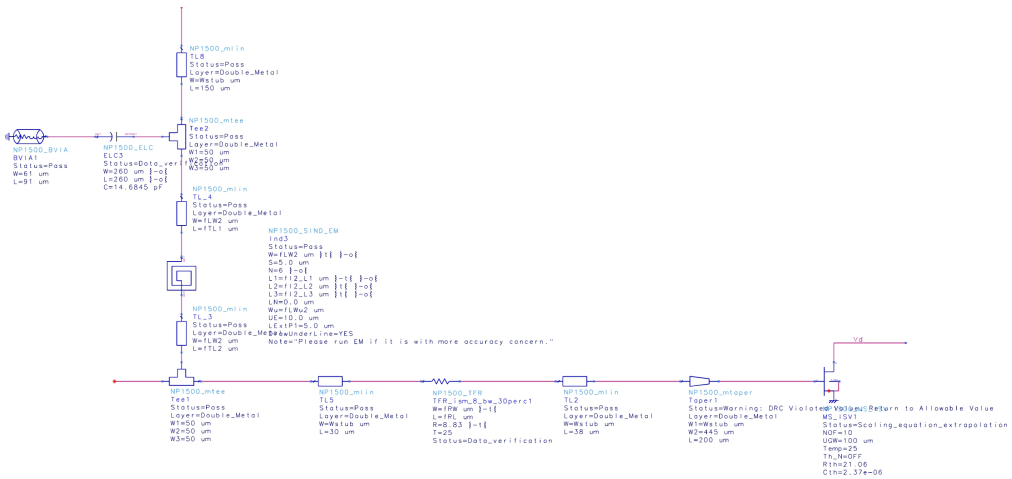

Figure 4.2: Stabilization network schematic with real components.

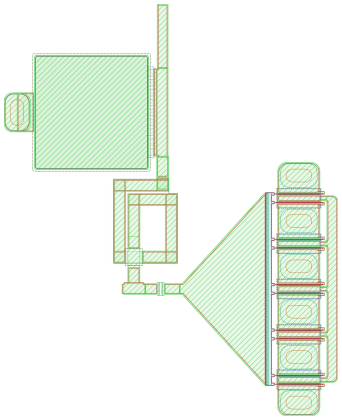

Figure 4.3: Stabilization network layout.

First, an initial layout of the complete circuit is generated. From a first look, the sections that need to be modified the most are the MNs and feeding networks, whose extensive use of microstrip lines as inductors leads to a large footprint. These networks are redesigned, substituting microstrip lines with inductors where possible and reducing every dimension in general. Note that, as previously stated, MNs design is challenging due to the many requirements that must be satisfied. This change adds one level of complexity since the library inductors are not easily optimized or tuned.

An example of the final compact layout for the ISM is presented in the following figures. Figure 4.4 shows the circuit-level schematic for the ISM, Figure 4.5 (left) presents the initial layout with long bulky microstrip lines and finally Figure 4.5 (right) shows the optimized ISM compact layout where microstrip lines are substituted with inductors where possible.

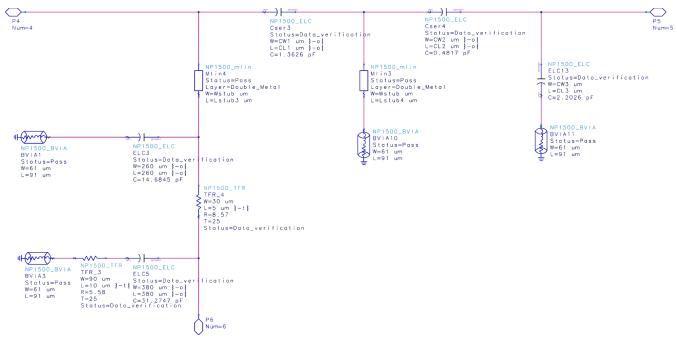

Figure 4.4: ISM subcircuit

Secondly, the size of the Lange power splitter and the combiner subcircuits needs to be reduced: due to the low frequency range of operation (3.3-5) GHz,

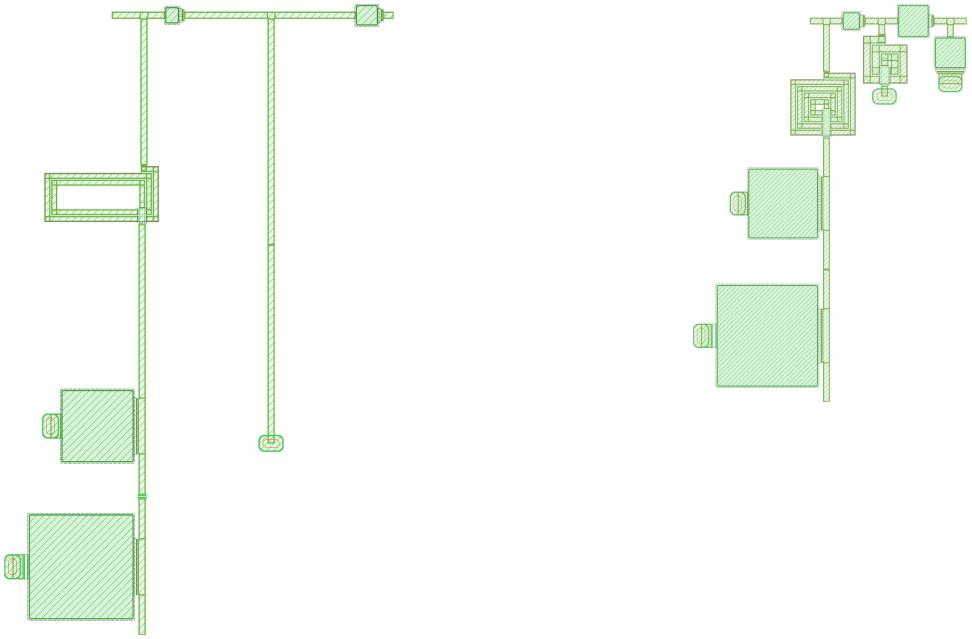

Figure 4.5: ISM initial bulky layout (left) and compact layout (right).

the required transmission line lengths are several millimeters long, exceeding the chip size specifications by themselves, as it can be seen in Table 4.1. Note that they cannot simply be shrunk due to the impact of this operation on the in-band matching.

Chip size	Combiner segments			Lange
Area	L1	L2	L3	Length
(3.7 x 3.3) mm^2	2.6 mm	4 mm	6.4 mm	7.2 mm

Table 4.1: Lange and combiner dimensions

As a consequence, their electrical lengths differ from their physical ones, and there is a generalized change in circuit parameters such as coupling factor, bandwidth, and losses. Many iterations of EM simulations will be needed to reach acceptable results.

4.2 Layout optimization, DRC and EM simulations

The applied design flow for the subcircuits' layout translation foresees starting from the output of the DPA and proceeding toward the input, i.e., from the combiner to the input power splitter. In fact, the circuit's performance depends on matching the best loads at each stage and this procedure allows to re-optimize the preceding subcircuits on the schematic before proceeding with their layout translation.

Each layout implementation is simulated with the EM tool. Choosing the correct settings for this simulation, such as the number of nodes of the mesh, ports feeding type, and frequency plan, is crucial since the wrong settings of these parameters can lead to meaningless results. To prevent that, the EM simulation results are constantly compared to the less exact but more reliable schematic ones. EM simulations are also heavy and time-consuming, so everything must be properly set in the first simulation.

As previously mentioned, the combiner is addressed first. The circuit-level schematic of Figure 3.25 is translated into the layout version of Figure 4.6: it is composed of three microstrip lines, which can be identified by their different widths. The heavy bending leads the TLs to have an electrical length shorter than the physical one therefore, the lines are lengthened and their actual electrical length is verified through EM simulations. Figure 4.7 illustrates the performance comparison between the circuit-level solution and the final layout solution. The match is satisfactory for all the matching figures of merit: $\Gamma_{dM,OBO}$, $\Gamma_{dM,sat}$, and $\Gamma_{dA,sat}$.

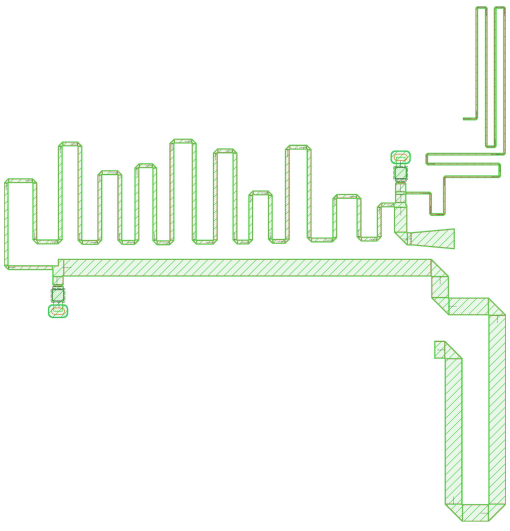

Figure 4.6: Combiner layout

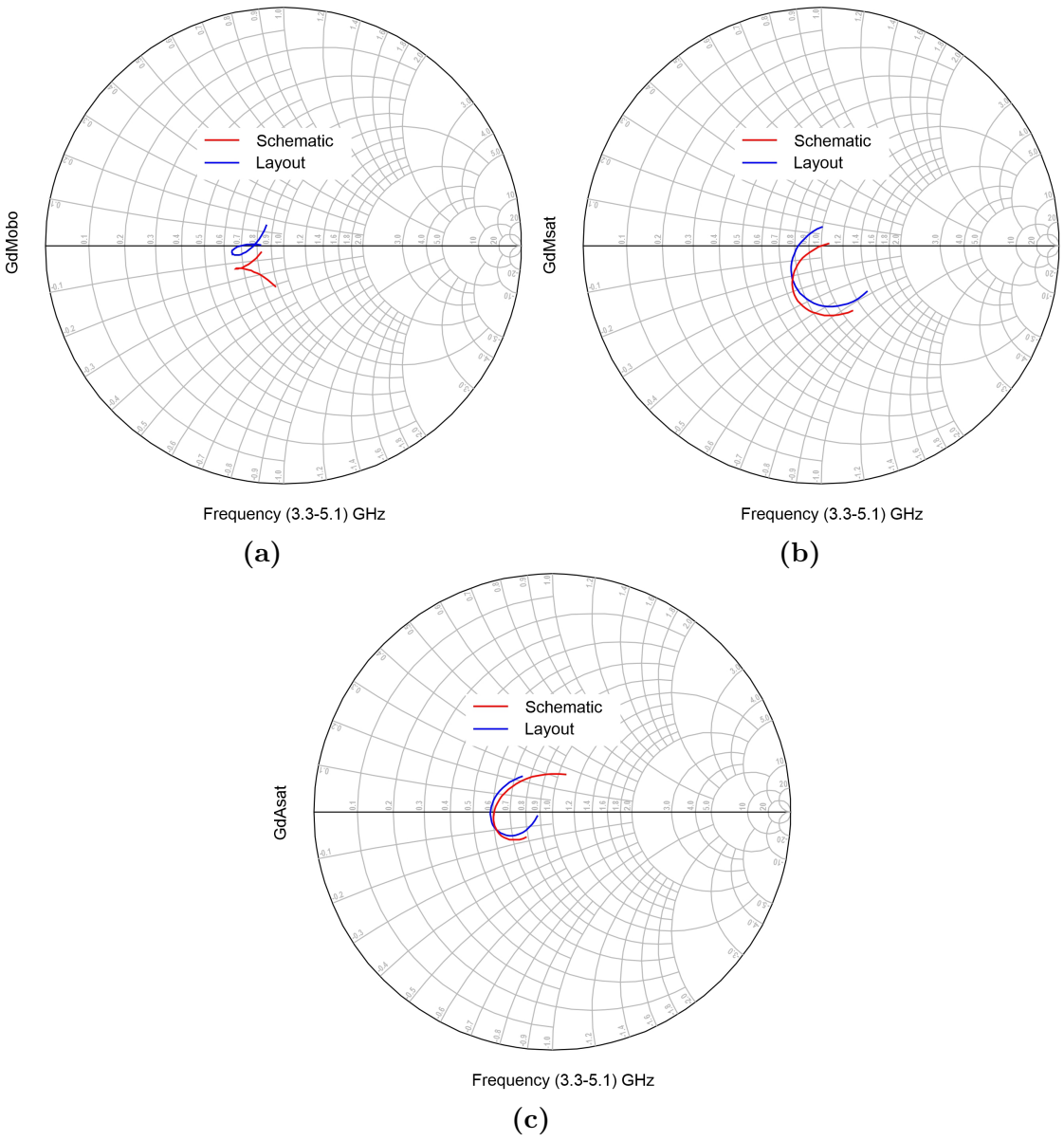

Figure 4.7: Combiner small signal performance schematic (red) - layout (blue) comparison: $\Gamma_{dM,OBO}$ (a), $\Gamma_{dM,sat}$ (b), and $\Gamma_{dA,sat}$ (c).

The final stage output bias layout is then realized and simulated with the EM tool (Figure 4.8), at first alone, and once its correct behavior is verified, it is attached to the combiner (Figure 4.9). Note that, due to the complexity of the EM simulation, the decoupling capacitors are added at a second stage.

Figure 4.10 shows a later version of the output bias inductor whose bridge is widened; in fact, this is the section of the inductor that is limiting the DC current

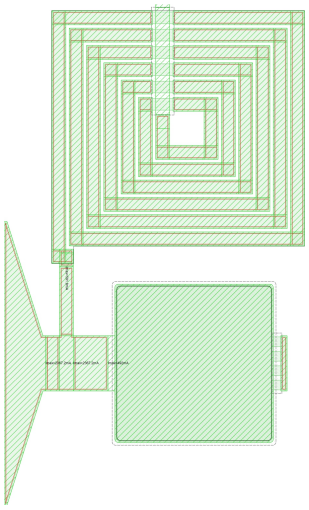

Figure 4.8: Final stage output bias layout.

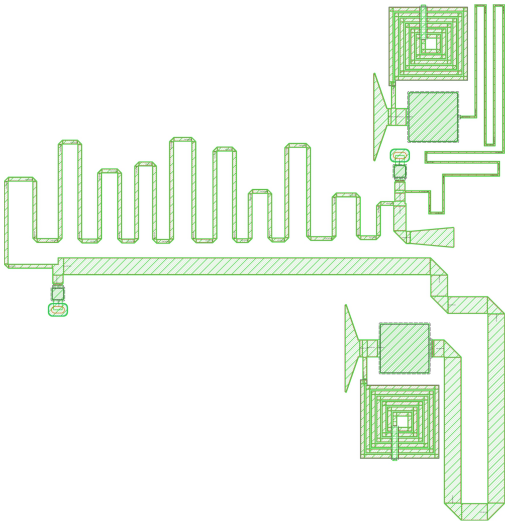

Figure 4.9: Combiner and Final stage output bias layout.

the component can withstand. By widening the bridge only, the inductor can handle the required 676 mA DC current while its transmission lines' width is kept at 20 μm, and the overall inductor size is restrained.

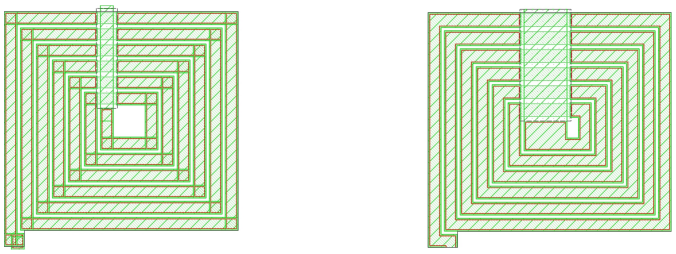

Figure 4.10: Inductor bridge widening: the final layout is presented on the right.

The ISM implementation is then addressed. In Chapter 4.1, its layout translation is presented and the result can be seen in Figure 4.5 (right). Here the following step is illustrated: an EM simulation is performed on the ISM together with the final stage input bias and stabilization circuit (Figure 4.11). Many iterations of optimization are needed to make it comply with the schematic performance.

A comparison of the final results is shown in Figure 4.12: the S_{11} is improves in the layout version to a maximum of -7 dB, while the S_{21} is slightly sub-optimal, losing 2 dB in the band (also in consideration of the higher losses estimated by EM simulations) and worsening for low frequencies. Note that the comparison is valid

only up to 5 GHz; due to the complexity of the EM simulations, the simulation frequency range is limited. An analogous procedure and results are obtained for the IMN and its bias and stabilization circuits.

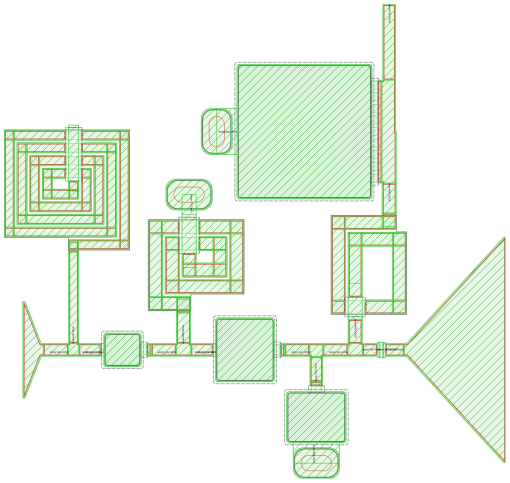

Figure 4.11: ISM and Final stage input bias and stabilization network

The last subcircuit to be converted is the Lange input power splitter whose final layout can be seen in Figure 4.13. Due to its quarter-wavelength transmission lines, it is the largest component in the circuit and needs to be heavily transformed, leading to parameters worsening. Figure 4.14 shows the final performance obtained after optimization: the coupling factor is decreased only by 0.5 dB over the band, while the phase delay variation increases over the bandwidth but is confined within a 7° interval. Note that the isolated port of the coupler is closed on a large 50 Ω resistive termination, which is made as large as possible to better dissipate the residual power.

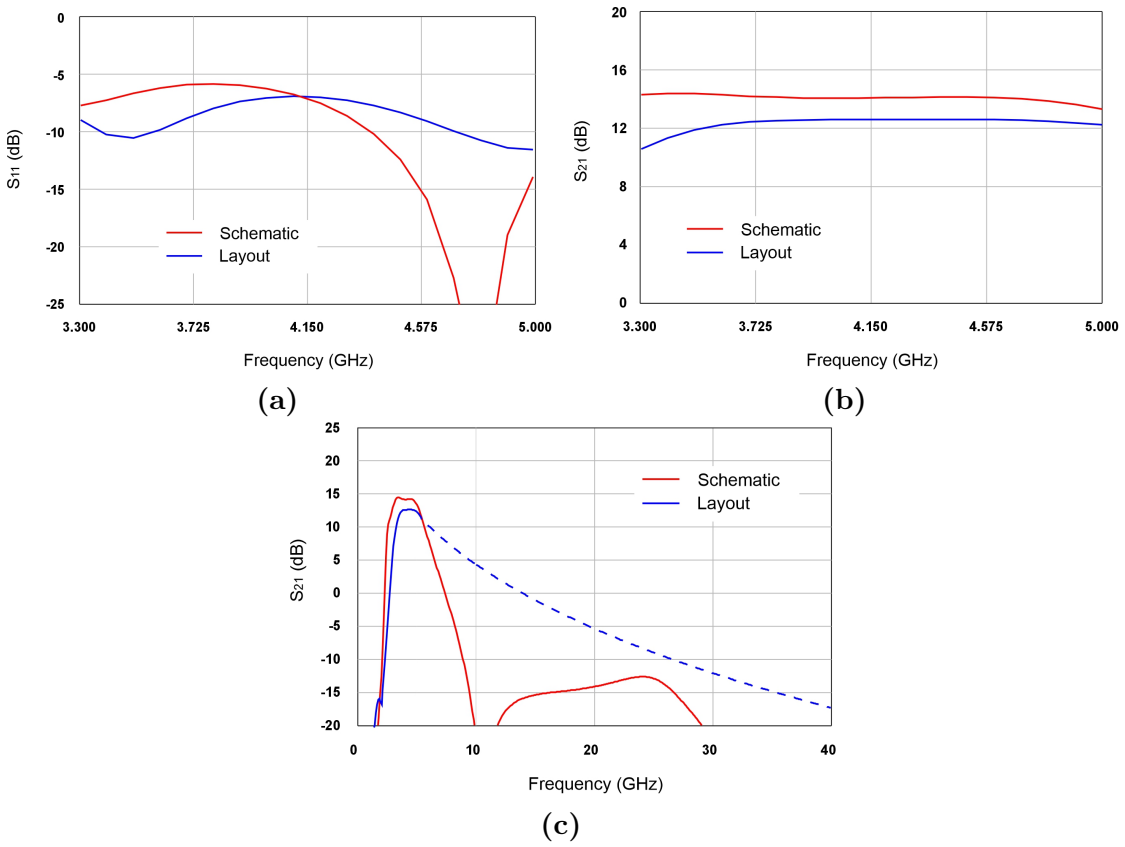

Figure 4.12: ISM and Final stage small signal performance schematic (red) - layout (blue) comparison: matching (S_{11}) (a), in-band gain (S_{21}) (b), and gain (S_{21}) over the (0-40) GHz range (c).

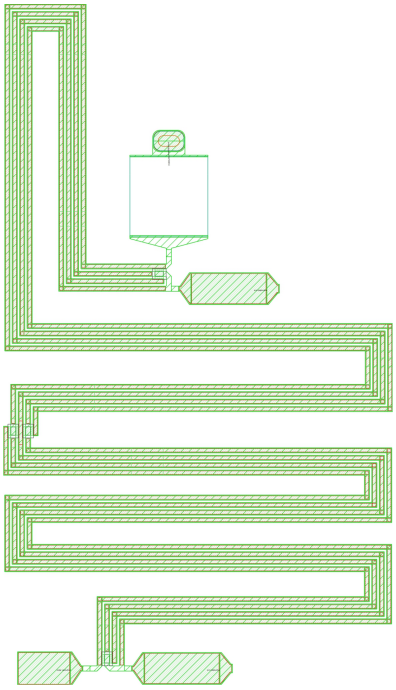

Figure 4.13: Lange layout

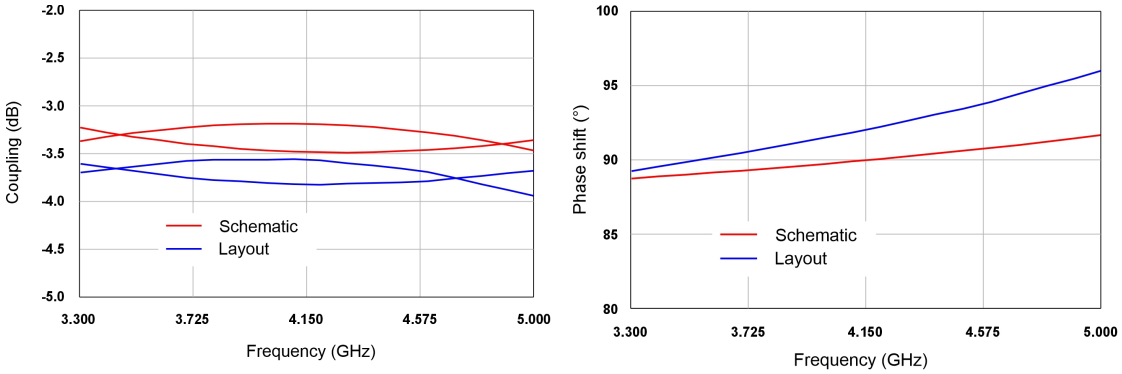

Figure 4.14: Lange small signal performance schematic (red) - layout (blue) comparison: coupling (left), phase shift (right),

4.3 Final performance: impact of EM blocks

The final layout of the designed DPA is presented in Figure 4.15. The final layout occupies the whole chip area without the second-level decoupling capacitors, which are then impossible to add on-chip. Therefore, further capacitors will be needed off-chip in order to make the feeding line stable against external variations.

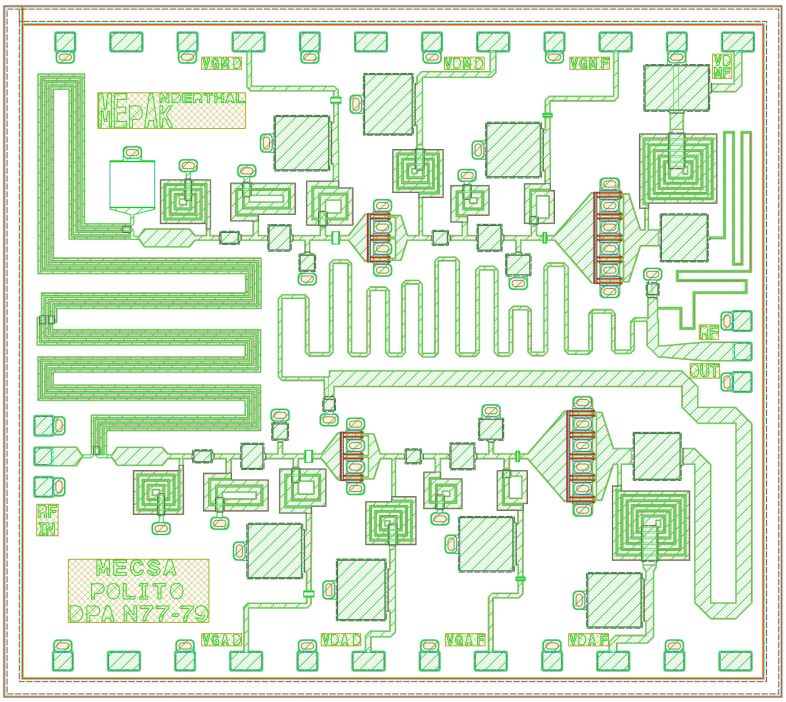

Figure 4.15: Final layout: RF pads on the left side (DPA input) and on the right side (DPA output); DC pads on the upper and lower side. Overall dimension: 3.7mm x 3.3mm.

In Figure 4.16 the large signal performance versus the output power is shown for the EM-designed blocks at five frequencies in the band. The saturated output power is larger than 37.5 dBm, leaving a 0.5 dB margin with respect to the requirements. The designed circuit achieves a minimum efficiency of 25 % at saturation and at 5 dB OBO, with uniform results over the bandwidth. These values show the effective efficiency enhancement in back-off, where the efficiency equals the saturated one.

In Figure 4.17 (bold curve) the small-signal performance is shown. The gain is comprehended in a (20-23) dB interval, achieving the required minimum 20 dB value, with only 3 dB of gain variation over the bandwidth. Note that, as before, the EM simulation is accurate only up to 5 GHz to limit the simulation time. The same graph shows a comparison with the schematic small-signal performance: the main difference is a gain reduction of 2 dB at the upper limit of the bandwidth. A

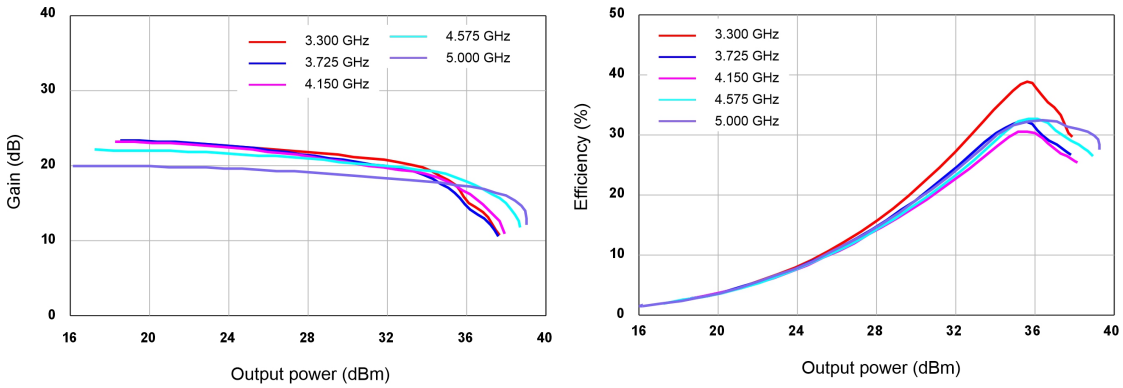

Figure 4.16: EM-designed circuit large signal performance for five frequencies in the target bandwidth: gain (left), efficiency (right).

possible cause can be the Lange layout realization, which has a big impact on the overall small signal performance of the amplifier also in consideration of the losses of the realized structure.

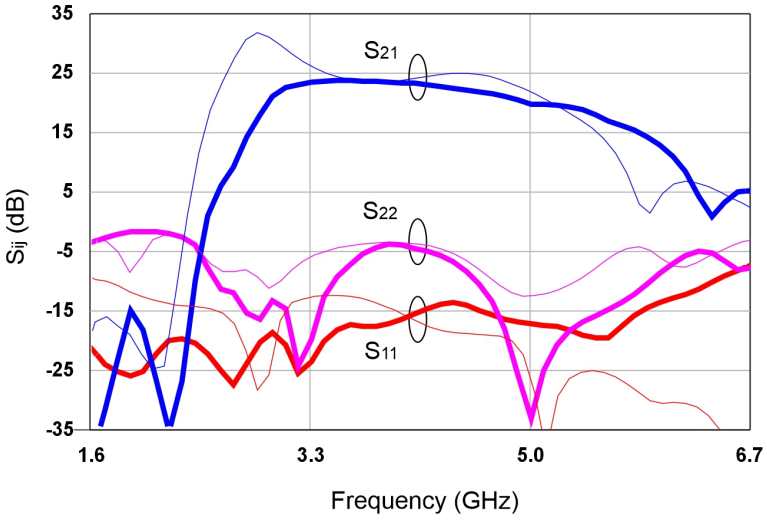

Figure 4.17: Small Signal performance comparison: layout (bold) versus schematic (thin).

Figure 4.18 shows the comparison between layout and circuit-level large signal performance at saturation. Over the bandwidth, the layout version of the design presents only a 0.5 dB saturated power penalty with respect to the corresponding circuit-level simulation, a comparable efficiency with a slight change in efficiency curve shape but uniform results over the bandwidth, and similar gain performance.

Therefore, the matching between the circuit-level and layout EM simulations can be considered satisfactory.

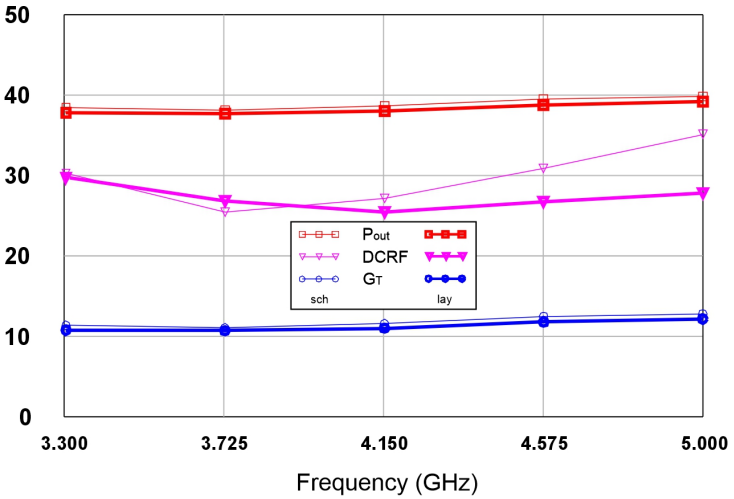

Figure 4.18: Large signal performance schematic (thin) - layout (bold) comparison at saturation: output power (squares), efficiency (triangles), and gain (circles).

With respect to the initial specifications of Table 2.1 we can conclude that the requirements are met in terms of small signal gain, output power, and output back-off and that the performance is uniform over the 41% bandwidth while succeeding in realizing a layout circuit to be manufactured in a (3.7 x 3.3) mm^2 chip area. The VSWR considerations are detailed in the next chapter.

Chapter 5

Final considerations and future developments

In this chapter, the final circuit is further analyzed to investigate future development strategies. First, the loads synthesized and presented to the Main and Auxiliary devices in the final Doherty circuit are compared to the optimum loads for power and efficiency obtained with load-pull simulations. Second, the load insensitivity performance of the circuit is examined, and a balanced topology is considered a potential future improvement. Finally, the linearity performance of the circuit is investigated because, while linearity is not one of the goals of the current design, it has become increasingly important in the field of high frequency power amplifiers over the last decade.

5.1 Load insensitivity

In this section, the circuit sensitivity to load variations from the optimum 50 Ω load is examined, as anticipated in Chapter 2. The examination is conducted at the circuit level for the center band frequency of 4.15 GHz.

First, a load mismatch corresponding to a VSWR of 2.5:1 is applied to the circuit, and the power, gain, and efficiency performance are examined. The worst-case scenario load is used for the simulation: according to (5.1) [30] VSWR 2.5:1 corresponds to a load reflection coefficient magnitude of 0.429. A load with the corresponding magnitude and a variable phase is then applied to the circuit.

$$VSWR = \frac{1 + |\Gamma|}{1 - |\Gamma|} \tag{5.1}$$

Figure 5.1 compares the circuit performance (red curves) with the 50 Ω optimum load performance (blue curve): it shows how the output saturated power is 34.6dB

in the worst case, varying by 4 dBm, the small signal gain is spread in a 5 dB variation interval, and the minimum efficiency in the OBO range passes from 25 % to 10 %, varying by 20 %. We can conclude that performance is severely degraded.

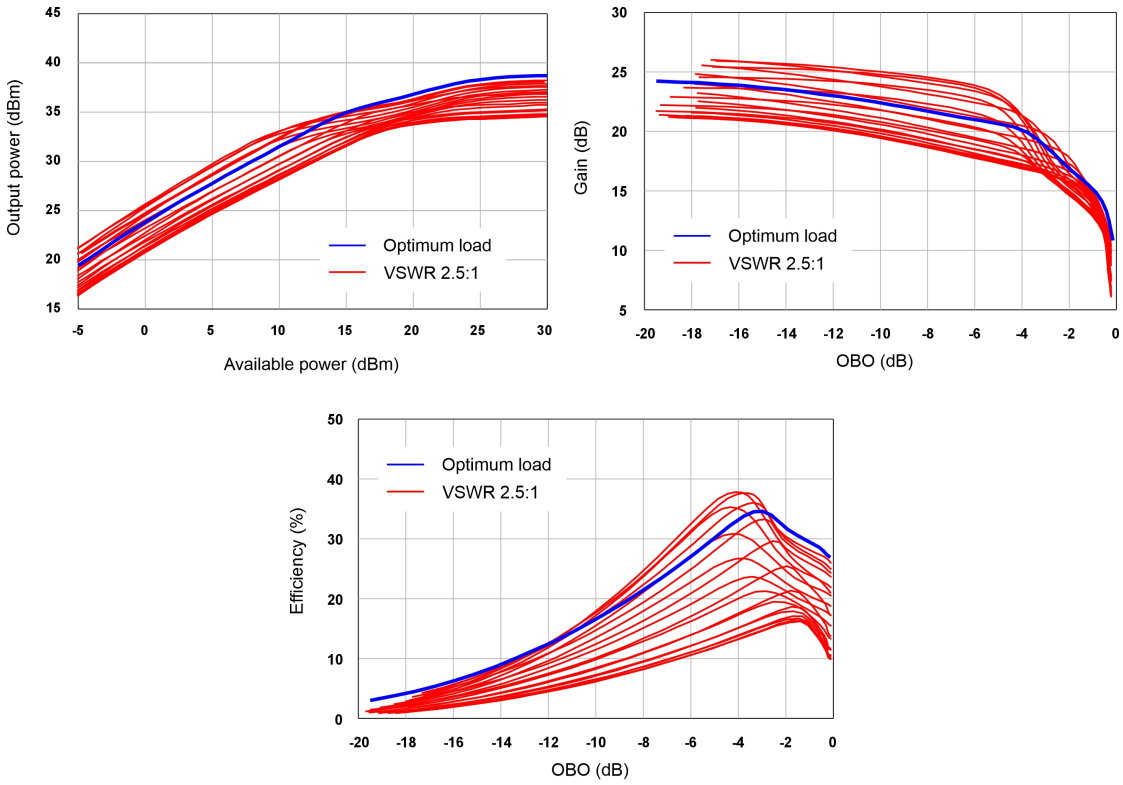

Figure 5.1: Large signal performance under optimum loading (blue) and 2.5:1 VSWR load mismatch conditions (red).

Second, a balanced version of the circuit is built to ensure that the load insensitivity is improved, and it is compared to the unbalanced version. The balanced topology, due to the proper use of couplers, leads to a low output reflection coefficient [3], thus enhancing the load mismatch insensitivity.

The ideal behavior of a balanced topology is investigated with an HB simulation at center frequency of 4.15 GHz and optimum load conditions. Figure 5.2 shows that the saturated output power is 3 dBm higher than in the single stage case (in agreement with the doubled periphery), still keeping the same gain and efficiency of the single stage (no additional losses). Figure 5.3 further stresses that the performances versus OBO are identical.

The balanced topology performance when using real lossy couplers remains almost unchanged preserving an almost ideal behaviour.

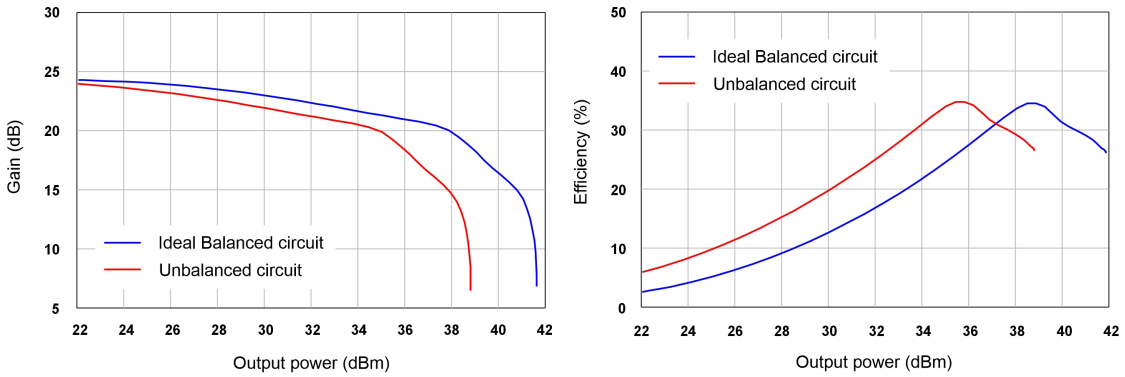

Figure 5.2: Unbalanced circuit (red) ideal balanced circuit (blue) large signal performance versus output power.

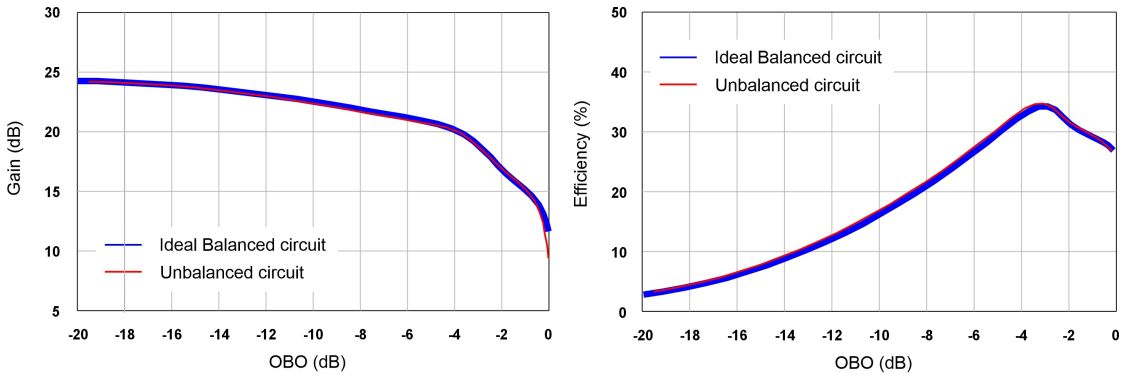

Figure 5.3: Unbalanced circuit (red) ideal balanced circuit (blue) large signal performance versus OBO.

The advantages of the balanced topology results evident from Figure 5.4 where for the worst-case mismatched load condition, balanced and unbalanced circuits are compared. The minimum saturated output power variation is reduced to 2 dBm, the small signal gain variation is only 1 dB, and the efficiency variation reduces from 20% to 6%. We can conclude that the balanced topology dramatically improves load insensitivity.

Finally, some considerations on the implementation of the balanced topology are presented. This topology needs complex bias interconnections: the number of transistors is doubled, but the device drain, the Main device gate, and the Auxiliary device gate still require three separate biases, as in the unbalanced case [Figure 5.5].

As previously stated, the process design kit has only two interconnection layers.

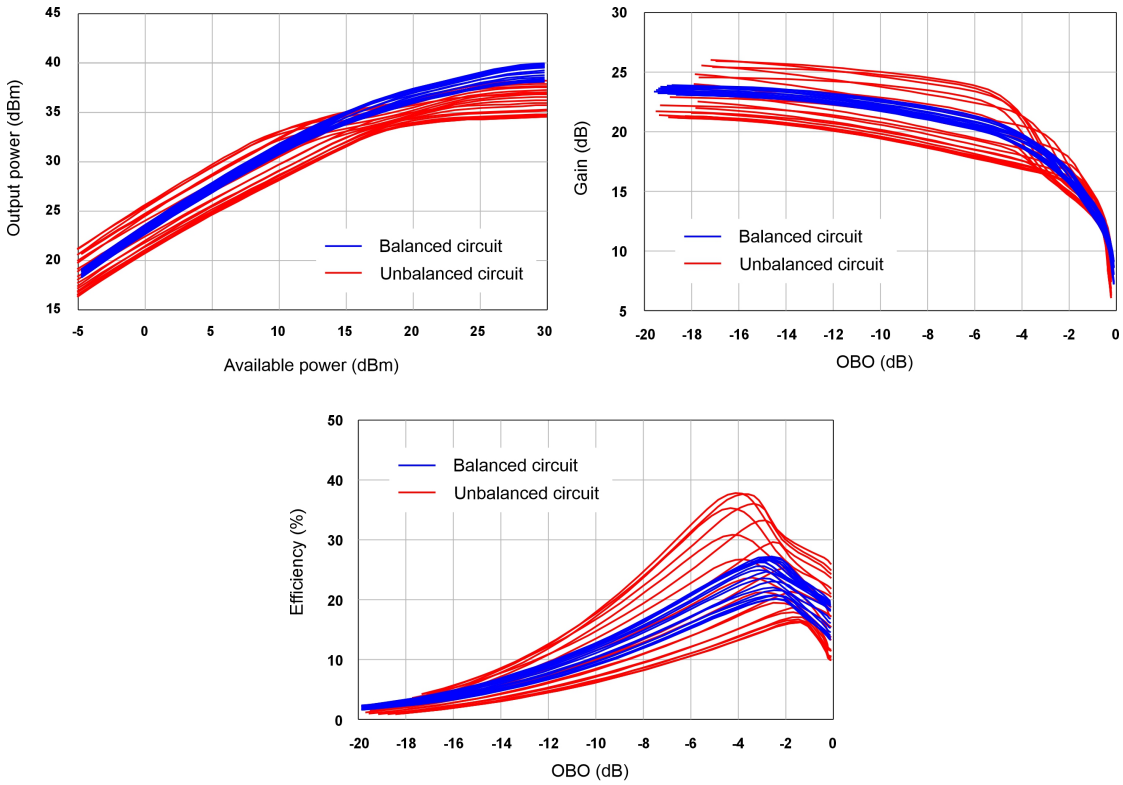

Figure 5.4: Unbalanced circuit (red) real balanced circuit (blue) large signal performance.

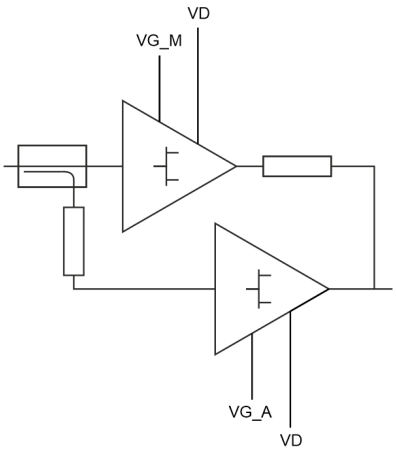

Figure 5.5: Illustration of an unbalanced circuit topology with highlighted feeding lines.

This makes it difficult to provide the necessary voltages to the devices placed in the internal branches of the architecture, as shown in Figure 5.6. A possible implementation relies heavily on the use of bridges and single-layer interconnections.

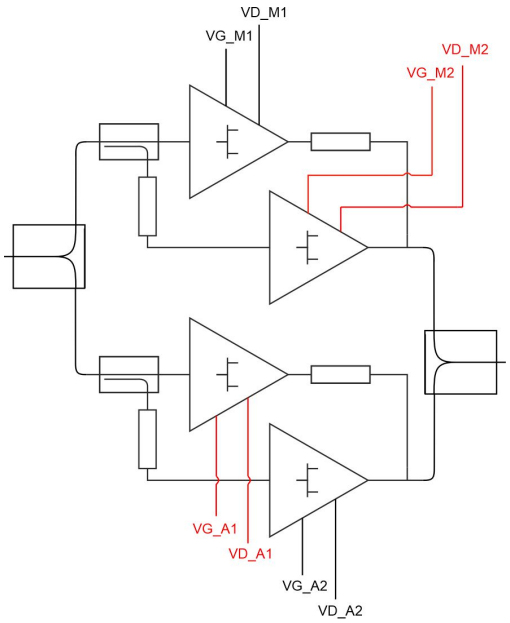

Figure 5.6: Illustration of a balanced circuit topology with highlighted feeding lines: the bias lines of the internal branches are marked in red.

5.2 Linearity

Even though linearity was not one of the main circuit's initial goals, it has a big impact on the PA design choices and deeply affects the performance of the entire transmitter. While efficiency-oriented power amplifiers' design allows for reducing size and cost of modern transceivers, the need for high data rates requires complex modulation schemes, which in turn require good linearity performance. Thus, linearity and efficiency cannot be separated in modern designs. Nowadays, the design of linear PAs, in particular Doherty PAs, faces the challenge of a lack of a design methodology that focuses not only on the combiner but also on the number of driver stages and position within the PA architecture. This is critical because, despite being highly linear, very-low gain single-stage demonstrators are not suitable for use in any real-world scenario, and the addition of external drivers that are not optimized for the specific PA typically degrades both efficiency and linearity significantly.

In this section, the linearity performance of the realized Doherty PA is examined

using the AMPM figure of merit. The AMPM estimates the phase shift introduced in a PA when the input signal amplitude is modified [5]. It can be defined as:

$$AMPM = \text{phase}\left(\frac{V_{\text{out}}}{V_{in}}\right) - \text{phase}\left(\frac{V_{\text{out},0}}{V_{\text{in},0}}\right) \tag{5.2}$$

Figure 5.7 shows the linearity performance of the implemented circuit for five frequencies equally distributed in the bandwidth. When only the Main branch is turned on, the AMPM remains limited (-2°, 6°) and degrades significantly (-17°, 35°) in the OBO region, i.e. when the Auxiliary branch is turned on. These results respect the theory that the linearity performance of a DPA is dominated by the Main device for low input powers while it degrades in the OBO region due to the Auxiliary turn-on [31]. It should also be noted that the AMPM values are both positive and negative, which is not always the case for DPA performance. Some cases in the literature present only positive or only negative AMPM values [32].

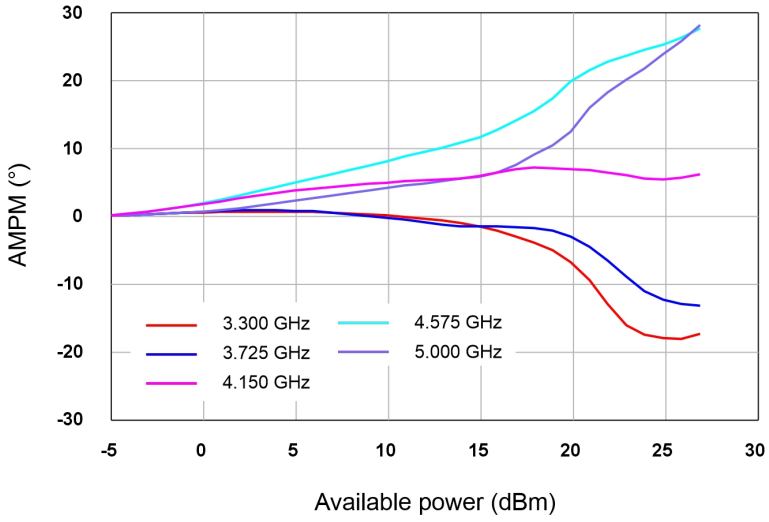

Figure 5.7: Synthesized DPA linearity performance (AMPM) versus available input power for five frequencies in the bandwidth

Linearity is influenced by many factors [5]. One of the less studied aspects is the number of driver stages and their position within the PA architecture. This is important, since very-low gain single-stage demonstrators, although highly linear, are not suitable to be adopted in any real-case scenario, and the necessary addition of external drivers that are not optimized for the specific PA typically degrades both efficiency and linearity significantly. This topic requires further investigation and theoretical study.

A possible approach would foresee the analysis of various PAs already manufactured in different technologies and with different architectures to assess the effect of

the driver stages on the overall performance. The comparison of different PAs that are based on the same technology and architecture but differ in the number and position of drivers would follow, in order to estimate their leverage on the overall performance.

5.3 Conclusions

The proposed thesis project presents the design of an MMIC DPA for 5G applications in the FR1 frequency bands (3.3 GHz-5 GHz), which successfully satisfies the requirement specifications presented in Chapter 2.

The designed amplifier achieves 37.5 dBm of saturated output power, which corresponds to more than 5 W, with a 0.5 dB margin over the specification. The circuit reaches a small-signal gain larger than 20 dB, with only a 3 dB variation interval. A minimum efficiency of 25% is attained over a 5 dB back-off range, and similar values are reached for OBO and saturation showing the effective efficiency enhancement behavior of the Doherty topology. The reported performances are uniform over the 41 % bandwidth. Therefore, the circuit succeeds in providing real-case scenario performance both in terms of output power and gain in the delimited (3.7 x 3.3) mm^2 chip size while presenting a remarkable frequency band of 41 %. It is now being manufactured by WIN Semiconductors Corp.

The design flow has been presented at the circuit and layout levels and the outcomes show a good agreement between the schematic and layout performance thanks to the intensive use of EM simulations. The next step would be assessing these results against the measured performance of the circuit to determine how good the simulations are in estimating the real implementation of the circuit. The following actions toward the fulfillment of the complete range of specifications of the wider commercial project this work is part of would require implementing the load insensitivity considerations presented in Chapter 5.1 while the more profound understanding of the subject gained thanks to this work could be applied to go through a re-design of the circuit targeting higher efficiency performance. An ambitious follow-up foresees including linearity aspects in the investigation as this aspect is becoming increasingly important in the power amplifier design.

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